HIGH-PERFORMANCE, MULTI-FACETED RESEARCH SONAR ELECTRONICS

by

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Abstract

This thesis describes the design, implementation and testing of a research sonar system capable of performing complex applications such as coherent Doppler measurement and synthetic aperture imaging. Specifically, this thesis presents an approach to improve the precision of the timing control and increase the signal-to-noise ratio of an existing research sonar.

A dedicated timing control subsystem, and hardware drivers are designed to improve the efficiency of the old sonar's timing operations. A low noise preamplifier is designed to reduce the noise component in the received signal arriving at the input of the system's data acquisition board. Noise analysis, frequency response, and timing simulation data are generated in order to predict the functionality and performance improvements expected when the subsystems are implemented. Experimental data, gathered using these subsystems, are presented, and are shown to closely match the simulation results, thus verifying performance.

Keywords: Sonar electronics; signal conditioning; timing control; low-noise preamplifiers

"Many of life's failures are people who did not realize how close they were to success when they gave up."

— *Thomas A. Edison*

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
AUV	Autonomous Underwater Vehicle
CDR	Coherent-to-Diffuse Ratio
CMRR	Common Mode Rejection Ratio
DAB	Data Acquisition Board
DCM	Digital Clock Manager
DC	Direct Current
Diff-amp	Differential amplifier
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
HDD	Hard Disk Drive
I/O	Input/Output
IC	Integrated Circuit
In-amp	Instrumentation amplifier
LNA	Low-noise Amplifier
NG	Noise Gain
NPSD	Noise Power Spectral Density
Op-amp	Operational amplifier
PCB	Printed Circuit Board
PC	Personal Computer
RF	Radio Frequency
RTI	Rated at the Input
RTO	Rated at the Output

SNR	Signal-to-Noise Ratio
TVG	Time-varying Gain
URL	Underwater Research Laboratory

Chapter 1

Introduction

This thesis describes the design, implementation and testing of a research sonar system capable of performing complex applications such as coherent Doppler measurement and synthetic aperture imaging. Achieving useful results for such complex applications requires that the sonar system meet two important criteria: maintaining precise timing control, and achieving high signal-to-noise ratio (SNR). This chapter discusses the historical and technical background that led to this research, summarizes the accomplishments, and outlines the rest of the thesis.

1.1 Background and motivation

In this thesis, the performance of a sonar system is improved to increase the speed and accuracy of the timing control of the system and increase the SNR of the received signal. In the past, sonar systems were designed employing specialized techniques and equipment [1, 2, 3, 4, 5]. Such methodology requires heavy financial investment in the development of application-specific systems that lack the versatility required in a research sonar. Recently, the electronics necessary to implement versatile systems have become more readily available, so that the development of such systems can now be achieved in both a cost-effective and time-efficient manner [6, 7, 8, 9]. The sonar system currently used in the Underwater Research Laboratory (URL), which from this point onwards will be referred to as the URL sonar system, is an example of such a design which allows for versatility and minimizes cost, while starting to address the timing control and SNR issues. This sonar system has performed well for a variety of applications, such as side-scan imaging and bathymetric

applications [10]. However, the URL sonar system is limited when applied to more complex applications, such as coherent Doppler measurement and synthetic aperture imaging due to shortcomings related to timing control and the level of attainable SNR. This thesis addresses these shortcomings and devises strategies to eliminate them.

1.1.1 A review of the URL sonar system

The URL sonar system uses a Field Programmable Gate Array (FPGA) to generate a common system clock, which it references to generate the transmit signals and to drive the sampling clock for the data acquisition board (DAB). At the start of each ping cycle, these processes are triggered simultaneously in order to maintain synchronization between the transmit and acquisition subsystems. In the URL sonar system, software is used to initiate the trigger, meaning that the ping time of the system is determined by software.

1.1.1.1 Summary of the existing timing control problems

Figure 1.1 shows an example of the received signal for two ping cycles, using the URL sonar system approach. Where $A(t)$ represents the envelope of the instantaneous amplitude of the signal, t_1 represents the acoustic travel time, Δt_1 represents the time required to store the data, and Δt_2 represents the time required to set-up and initiate a ping sequence.

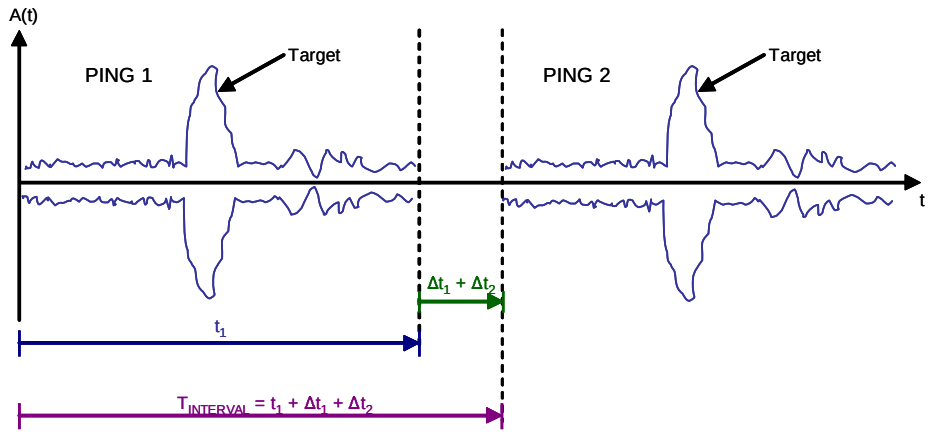

Figure 1.1: Representation of the received signal "envelope" for two ping cycles, including the setup time

A limitation of the approach used in the URL sonar system can be seen in Figure 1.1. When a non-dedicated computer, such as a Windows operated Personal Computer (PC), is used to trigger the start of each ping sequence, Δt_2 becomes random, since it depends on the priority of the software call in the Windows servicing queue, and although proper timing can be maintained for a single ping cycle, synchronization between successive ping cycles is lost. Therefore, although data are aligned for a given ping, the relationship in time between successive pings becomes unpredictable. This random time interval manifests itself as an unknown phase for targets moving relative to the sonar.

Another concern arises when considering the speed of execution of such an approach, which is slow, due to the long time interval, $T_{interval}$, between the start of successive ping cycles. Even if the time overhead of the system could be minimized by completely eliminating Δt_1 and Δt_2, for practical target ranges, the acoustic travel time t_1 would still be too long to recover useful Doppler information about the target using successive ping cycles.

1.1.1.2 Solutions to the timing control problems

A sonar capable of pulse-to-pulse coherent Doppler measurements and synthetic aperture imaging was implemented as shown in Figure 1.2. In this system, the control of all time

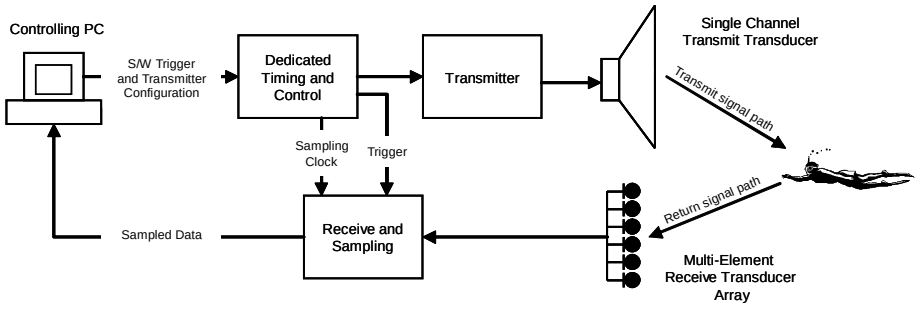

Figure 1.2: Block diagram showing the timing and configuration control for the proposed sonar system

critical processes are passed to a dedicated computer, while using the PC for system configuration, and data storage only. By using this approach, Δt_2 is reduced and set to a fixed predictable value. Δt_1 is also reduced because of the overlapping structure of the system, meaning that sampled data can be dumped to the computer at the same time that the

DAB's buffers are acquiring new data. In order to facilitate coherent Doppler measurements for reasonable ranges, the system is capable of transmitting multiple pulses in a ping cycle, as described in [11, 12].

An FPGA is used as the dedicated computer for the system, and it generates the logic necessary to implement the timing control and trigger for the system processes. Additional features on the FPGA, such as the digital clock managers (DCMs) are used to ensure that the strict timing requirements for the clock are met, minimizing problems such as clock skew and clock jitter.

1.1.1.3 Summary of the existing SNR problem

Echoes arriving at the acquisition circuitry of the URL sonar system are susceptible to two major sources of disturbance, as shown in Figure 1.3. These are: intrinsic noise sources

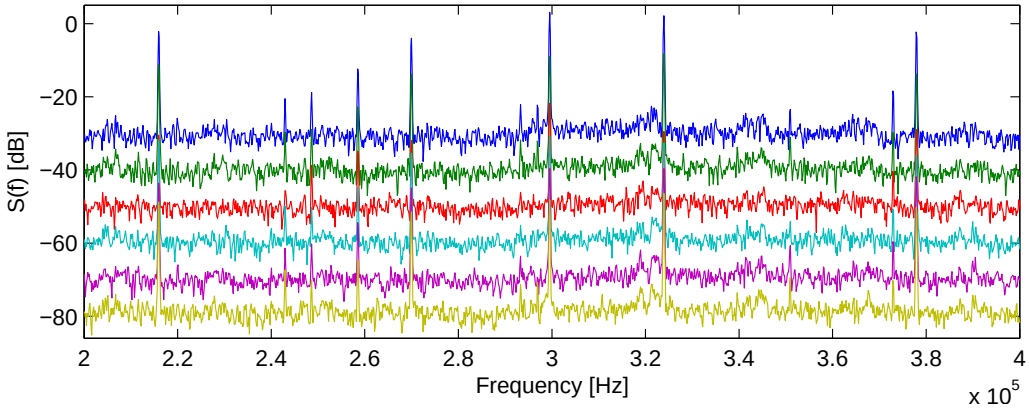

Figure 1.3: Power spectral density of a received signal obtained using the URL sonar system with the transmitter off, and interfaced to a six channel, 300 $[kHz]$ transducer. Where $S(f)\,[dB]$ is the power representation of the quantization number associated with the sampled receive signal. Each channel is offset by $-10\,[dB]$. The average broadband noise level is approximately $-30\,[dB]$. Interference lines occur through out the frequency band.

generated by the transducer, preamplifier circuit components, and the DAB; and extrinsic noise sources generated by electromagnetic interference (EMI) and common-mode voltages. Specifically, the intrinsic noise sources increase the broadband noise level of the system, masking the signal, and limiting the minimum recoverable signal. These noise sources

become increasingly significant as return signal strength weakens due to the increased propagation distance for long range targets. The extrinsic noise sources result in interference lines in the receive signal's power spectrum that may be in close proximity to the pass-band of interest, significantly limiting the practical bandwidth of the system. The interference generated by these noise sources has the same characteristics as the actual signal, which is received at the transducer array. As a result, the angle estimation, used during processing, will be adversely affected, since the estimation algorithm cannot distinguish between the signal and the interference. Specifically, the estimation algorithm misinterprets the interference as plane waves arriving at the transducer array. These "phantom" plane waves will have zero-phase, since their corresponding signals (interference) are in phase with each other on all the transducer's channels, meaning that the differential phase across the transducer array elements will be computed as zero, and implying that the signal arrives perpendicular to the array. Therefore, in terms of the processed bottom profile, the interference will appear as a target extending out broadside to the transducer array. These extrinsic noise sources increase as the length of the cables between the receive transducers and receive electronics are increased. Therefore, limiting the noise contributions of the intrinsic and extrinsic sources is crucial for maximizing the SNR for the returning signals and thus improving the performance of the sonar system.

1.1.1.4 A solution to the SNR problem

Ever improving technology has led to the availability of ultra low noise and low distortion analog electronic components, such as those described in [13, 14]. By utilizing such devices along with known design techniques [15, 16], the effects of disturbances generated by the intrinsic noise sources can be reduced, and the broadband noise spectrum level of the system can be significantly lowered, as compared to the URL sonar system.

A receiver that is designed with a differential front-end has the ability to reject signals that are common to both its inputs, and can be useful in reducing and eliminating EMI and common-mode voltages attempting to enter the sonar's receive subsystem. Applying such an approach, along with known suppression techniques such as filtering, shielding and proper grounding [15, 16, 17], can be used to minimize the interference lines seen in the pass-band of the URL system.

A system which takes advantage of these techniques can achieve significant reductions in the overall noise introduced in to the system, and thus, a significant improvement in the

SNR, as compared to the URL sonar system.

1.2 Contribution of the new sonar system

Using an FPGA development board to control the timing operations of the system and a user-programmable system clock, the speed, precision and predictability of the sonar system was improved. A ping cycle takes approximately $500\,[ms]$ for a target located $300\,[m]$ from the sonar, as compared to $1\,[s]$ using the URL system. Noise generated by the receive system was reduced such that the noise voltage of the preamplifier was found to be approximately $1.03\,\left[\frac{nV}{\sqrt{Hz}}\right]$ at $300\,[K]$, which is equivalent to the noise generated by $66\,[\Omega]$ resistor. This is significantly lower than the noise generated by the most quiet transducer presently available in the URL, and represents a significant improvement over the URL system, which has a noise voltage of approximately $2.93\,\left[\frac{nV}{\sqrt{Hz}}\right]$ at $300\,[K]$, and dominates the noise generated by the receive system.

Two techniques that utilized a differential input front-end on the receive preamplifier, as opposed to a single-ended front-end were investigated in order to suppress the interference lines observed in the power spectrum of the received signal. These techniques tested the beneficial properties associated with transformer action, and differential amplifiers (diff-amps).

A novel approach was developed in order to investigate the effects of inserting a transformer on to the front-end of the receive preamplifier. This novel approach was based on a standard method used to measure the admittance characteristics (admittance versus frequency) of transducers. Using this approach, the transformer's interactions with the receive transducer, and its effect on the frequency response of the receive system were observed, in real-time, on an oscilloscope.

Transformers were shown to offer useful benefits for sonar systems operating in a narrow frequency band, suppressing common-mode signals and minimizing source loading effects by tuning out parasitic capacitances that exist in the transducer and the interfacing cables. However, the application of a transformer in a wide-band system, such as the URL sonar system, was not desirable, because of the receive signal attenuation that occurs due to impedance mismatching of the source and the load over a wide frequency range.

The diff-amp technique was shown to suppress the interference lines, and also keep the practical useable bandwidth of the system. However, this approach was also shown to have

adverse effects on the broadband noise performance of the receive system, resulting in a broadband noise power loss of $4\,[dB]$ (theoretical), $5.5\,[dB]$ (measured), when compared to the URL sonar system, and a loss of $13\,[dB]$ (theoretical), $14.5\,[dB]$(measured), when compared to the new single-ended design. This represents an important compromise that must be considered when choosing an approach for receive preamplifier design.

Ultimately, the single-ended front-end solution was chosen to be the most favorable design because of the superior broadband noise characteristics of presently available op-amps, as compared to diff-amps. This meant that the interference lines were still present in the power spectrum of the received signal. However, for the URL research sonar setup, these common-mode interference lines can be managed in the field by applying grounding points, using shielding techniques, and slightly shifting the sonar's operating frequency to interference free regions. The resulting reduced noise contribution of the preamplifier led to an improvement in the SNR of the overall receive system.

1.3 Thesis organization

This thesis is organized into five chapters. Chapter 1 gives an introduction to the sonar system design problem, outlines the motivation for undertaking such a problem and gives insight into how the problem can be solved, accompanied by a summary of results. Chapter 2 describes the approach taken to solve the timing-related issues existing in the URL's sonar system. Chapter 3 describes the approach taken to solve the SNR related shortcomings of the receive electronics of the old sonar system, using noise reduction and EMI suppression techniques. Chapter 4 provides experimental results to verify that the sonar system works. The document concludes in Chapter 5 which summarizes major results and suggests improvements and recommendations for future work on the sonar system. Complete timing and noise analysis, schematics, and other important calculations are provided in the appendices.

Chapter 2

Improving the Timing of a Sonar System

This chapter describes the approach taken to overcome the timing issues existing in the URL sonar system (old sonar system). Solving these issues requires that a new timing control system be designed to better manage and maintain the precise timing operations of the sonar. The new algorithms and additional features of the new timing control results in an increased ping rate for the sonar, and enhances its capabilities to generate and transmit more complex waveforms. This chapter briefly reviews the existing timing-related shortcomings of the URL sonar system, discusses the approach taken to eliminate these shortcomings, and explains the additional features used to expand the application capabilities of the sonar system. Simulation data are also presented to verify the successful implementation of the new timing control subsystem.

2.1 A brief review of the timing control issues in the URL sonar system

In the URL sonar system, an FPGA creates and references a common clock source to generate transmit signals and drive the sampling clock for the DAB. Synchronization between the transmission and acquisition subsystems is maintained by simultaneously triggering these processes at the start of each successive ping cycle.

The timing relationships that exist between some of the important signals generated

during an operating cycle of the URL sonar system are shown in Figure 2.1. Where Δt_{svc}

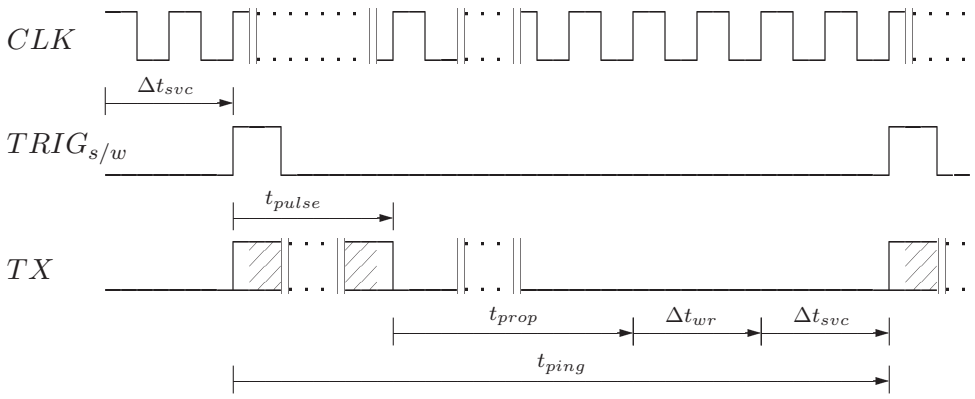

Figure 2.1: Timing diagram showing the relationship between the signals generated on the software trigger ($TRIG_{s/w}$) and the transmit pulse (TX) lines with respect to the system clock (CLK) during an operation cycle of the URL sonar system.

is the time required to setup and initiate a ping/trigger sequence, t_{pulse} is the time required to generate the pulse envelope, t_{prop} is the acoustic travel time, Δt_{wr} is the time taken to write acquired data to physical storage, and t_{ping} is the overall ping period of the system. Figure 2.1 shows that the overall ping period, t_{ping}, consists of the pulse generation and propagation times, t_{pulse} and t_{prop}, and the data transfer and servicing delays, Δt_{wr} and Δt_{svc}, as shown in Equation 2.1.

$$t_{ping} = t_{pulse} + t_{prop} + \Delta t_{write} + \Delta t_{svc} \tag{2.1}$$

Synchronization between the transmit and receive subsystems is maintained by initiating software triggers and pulse envelopes on the same reference clock edge for each ping cycle.

Since the URL sonar system uses software to control triggering, the ping time of the system is determined by software. This poses a problem because the start of each ping/trigger sequence depends on the priority of a software call in the PC's instruction servicing queue, and causes Δt_{svc} to become random. Therefore, although proper timing can be maintained for a single ping cycle, synchronization between successive ping cycles is lost, since the time interval between successive pings is inconsistent. This random time interval manifests itself as an unknown phase between pings for targets moving relative to the sonar.

Another shortcoming of the URL sonar system is that it is capable of generating only a single pulse envelope per ping cycle. Figure 2.2 illustrates the issue associated with using this system to obtain Doppler information using consecutive pulse envelopes. From the

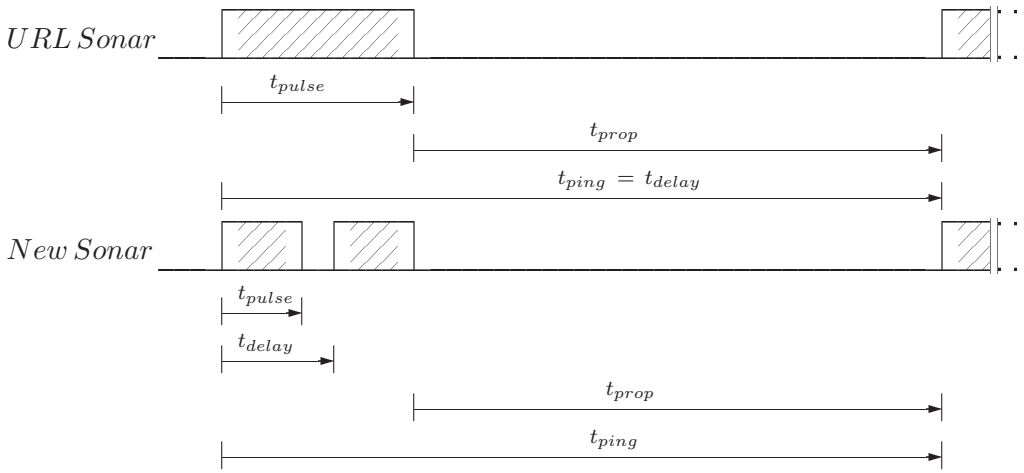

Figure 2.2: Timing diagram comparing the single pulse envelope per ping transmit scheme of the URL sonar system with the proposed multiple pulse envelope per ping transmit scheme of the new sonar system, ignoring setup,Δt_{svc}, and write time,Δt_{write}.

timing diagram for the URL sonar system in Figure 2.2, the ping time, t_{ping}, and the delay between the start of consecutive pulse envelopes, t_{delay}, are the same. As the target range increases t_{ping} also increases, since it depends on the acoustic travel time between the sonar and the target, t_{prop}. Therefore, targets located at practical distances from the sonar will have long delays between the start of consecutive pulse envelopes, hence, obtaining Doppler information using consecutive pulse envelopes is impractical in this case.

Expanding the capability of the URL sonar system to generate multiple pulses per ping cycle, such that t_{delay} no longer depends on t_{ping}, as shown in Figure 2.2, means that the time between consecutive pulses can be reduced, and should improve the system's Doppler performance for practical target ranges using the consecutive pulse approach, as discussed in [11, 12].

2.2 Improving on the shortcomings of the URL sonar system

2.2.1 A dedicated timing control subsystem

The timing issues in the URL sonar system are solved by creating a dedicated timing control system that is initiated, but not controlled by a PC software trigger. A block diagram of this timing control system is shown in Figure 2.3. In the new timing system, the PC is used

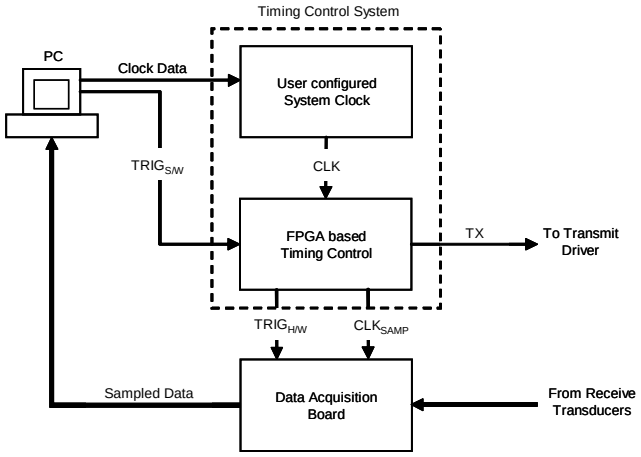

Figure 2.3: Block diagram of the new sonar timing control system, emphasizing the control lines for the system reference clock, CLK, the PC generated software trigger, $TRIG_{s/w}$, the hardware trigger to the DAB, $TRIG_{h/w}$, the DAB's sampling clock, CLK_{SAMP}, and the transmit signal bus, TX.

to configure the system reference clock, provide an initial software trigger to the FPGA and store the retrieved data. The FPGA is responsible for generating the DAB's sampling clock, triggering the DAB, and generating transmit pulse sequences.

The timing relationships between the signals generated on the control lines of the new timing system during an operation cycle are shown in Figure 2.4. Δt_{svc} is the time to setup and initiate a software trigger, δt_{wait} is a short delay generated to ensure that synchronization is maintained between the FPGA-generated hardware trigger and the DAB's sampling process over the sonar's entire operating cycle, and is explained in greater detail in the following section. t_{pulse} is the time taken for a pulse envelope, t_{prop} is the acoustic travel time, Δt_{write} is a fixed time delay to write acquired data to PC storage and prepare for new data, and t_{ping} is the overall ping period. Similar to the operation of the URL sonar system's

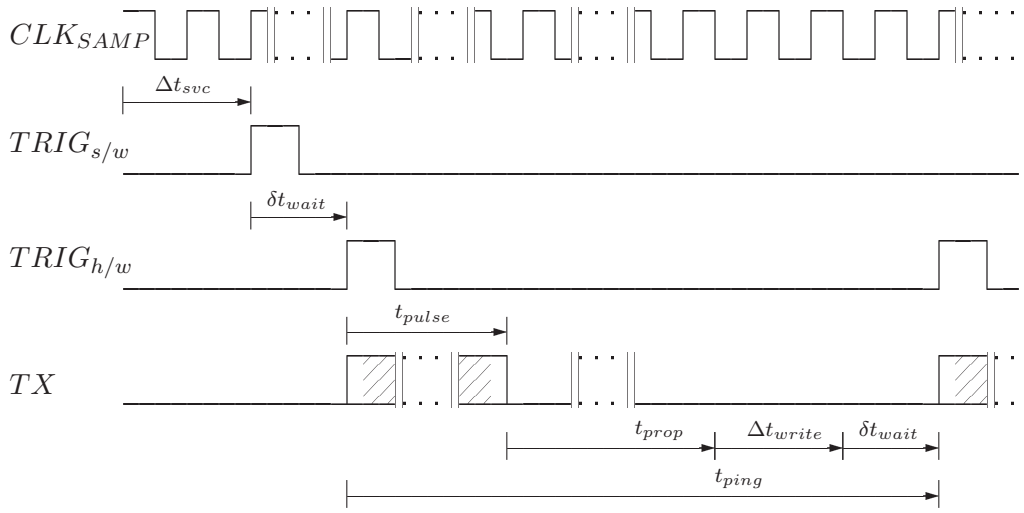

Figure 2.4: Timing diagram showing the relationship between the signals generated on the control lines of the new timing control subsystem during an operation cycle, and referenced to the rising edge of the sampling clock.

timing control, shown in Figure 2.1, a PC generated software trigger initiates an operating cycle after an initial setup time, Δt_{svc}. On recognizing this trigger, the FPGA-based timing module is activated, and after a short delay, δt_{wait}, it simultaneously generates a hardware trigger to the DAB and a ping sequence on the TX bus. However, unlike the URL sonar system, subsequent DAB-triggers and ping sequences are initiated by the FPGA-timing module and not by the PC's software trigger. In this way, the precise timing capabilities of the FPGA are used to establish and maintain synchronization between ping cycles, while the PC is used to poll for FPGA-triggered events, and initiate data storage routines after each triggered event has occurred. As a result, the unpredictability in the ping period that is caused by Δt_{svc} is eliminated, and for a given operating cycle, the ping period becomes a known and fixed value, as represented by Equation 2.2.

$$t_{ping} = t_{pulse} + t_{prop} + \Delta t_{write} + \delta t_{wait} \tag{2.2}$$

In the new system, the duration of Δt_{write} is both a critical and limiting factor in determining the minimum overall ping period of the system for a specific target range. Since processes in the FPGA-timing module run independently of the PC, in order to properly capture all of the acquired data, the PC must complete all of its tasks and be ready before each FPGA event occurs. Fixing too small a value to Δt_{write} results in data loss due to

missed FPGA-triggered events, while too large a value results in impractically long ping periods.

2.2.1.1 Maintaining synchronization between the FPGA-generated trigger and the DAB's sampling process for consecutive pings during an operating cycle of the sonar

The DAB that is interfaced to the receive preamplifier is a high performance, 16-bit acquisition board that uses $\Sigma - \Delta$ converters to generate high resolution digital samples, as described in [18]. In order to generate a 16-bit sample, the DAB must oversample data at a rate that is a multiple of the true sample rate. Specifically, the DAB can be configured to oversample by eight, four, two or one times (multiplied by) the true sample rate (one times only generates a 12-bit sample). The DAB also requires a clock input that is twice the chosen oversampling rate in order to generate its sampling clock. This oversampling clock is configured by the user, generated by the FPGA during the start-up process of the timing control subsystem, and fed into the external clock input of the DAB. On receiving a valid clock, the DAB starts to sample data. However, none of the sampled data are recorded until the DAB receives a hardware trigger from the FPGA, which indicates the start of a ping.

The FPGA generates and transmits a hardware trigger to the DAB at the start of each ping cycle. In the new timing control subsystem, only the initial hardware trigger generated by the FPGA is determined by a software trigger event that is initiated by the user at the start of an operating cycle, and depends on the PC's servicing priorities. As a result, the initial hardware trigger always arrives at the DAB at some arbitrary phase in the DAB's sampling process. On receiving this hardware trigger, the DAB is designed to wait for a specific phase of its sampling process before it starts recording data, meaning that the time between the first hardware trigger and the first recorded sample is random. In order to maintain synchronization over successive pings in an operating cycle, each of the remaining FPGA hardware triggers must occur at the same time as the initial trigger, relative to the DAB's sampling phase. In the new system, this is achieved by generating a counter in the FPGA that tracks the time delay between hardware triggers, ensuring that trigger signals are only sent to the DAB on counts that are multiples of the DAB's sample process length. This results in a short delay, δt_{wait}, that pads the ping time such that this condition is met.

2.2.1.2 Asynchronous data transfer

The URL sonar system uses synchronous I/O routines to transfer valid data from the DAB's buffers to the PC's hard drive (HDD). For each ping cycle using the URL sonar system (old sonar system), an entire ping must be read into the PC's virtual memory and then completely written to the HDD before another ping cycle begins. Data transfer rates between the DAB's buffers and the PC's virtual memory tend to be fast, since the DAB utilizes a pair of swing buffers to simultaneously store newly acquired data and transfer stored data to the PC's virtual memory. However, data transfer rates between the virtual memory and the HDD tend to be comparatively slow and limit the speed of the overall I/O operation. Using this approach in the new sonar system would require that Δt_{write} be set to its maximum value in order to capture all of the FPGA-triggered events, and would result in the slowest possible ping rate for the system. This issue is addressed by taking advantage of the asynchronous capabilities of the DAB and the PC. Figure 2.5 shows a flowchart representation of the I/O scheme developed for the new sonar system. Using this scheme, the system transfers as much data as possible from the DAB's buffers into virtual memory before starting to write to the HDD, and writes as much data as possible from the virtual memory to the HDD after all the ping sequences in an operating cycle have completed. During the intermediate stage, data are written to the HDD at the same time as the virtual memory fills with new data. In this way, Δt_{write} can be significantly reduced, as compared to the URL sonar system, since the system no longer waits for data to be completely written from virtual memory to the HDD before initiating its next ping cycle. As a result, t_{ping} is also reduced and the ping period of the system is shortened. The resulting increased ping rate leads to an increase in the density of data that the sonar can generate when passing over a target area. This is especially beneficial for sonars that operate with very narrow beamwidths, since segments of the target area previously missed, due to the slower ping rate, can be captured.

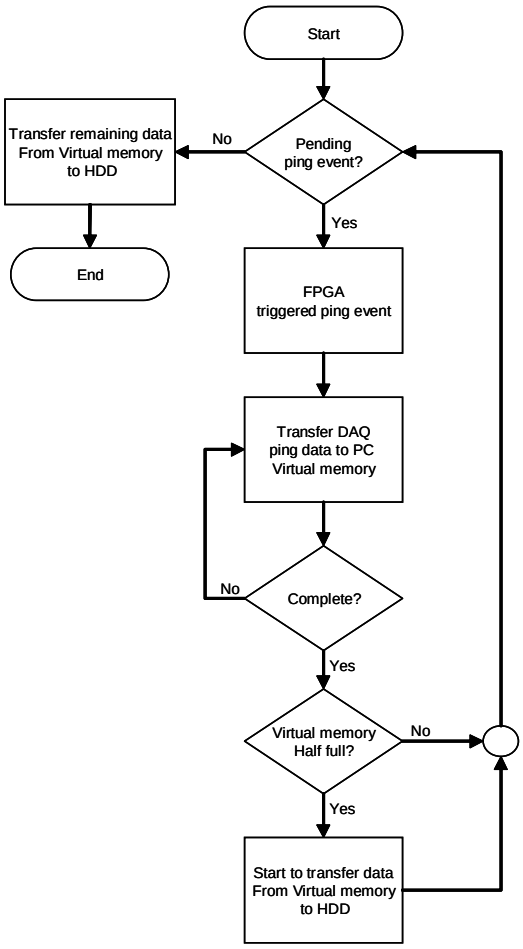

Figure 2.5: Flowchart showing the I/O scheme for new sonar system.

2.2.2 Generating multiple pulses in a ping cycle

An additional feature of the new sonar system is its capability to transmit multiple pulses in a ping cycle and therefore perform Doppler applications such as those described in [11, 12].

The single and multiple pulse schemes are compared in the timing diagram shown in Figure 2.6. Where Δt_m is the pulse width in single pulse mode, Δt_d is the pulse width in multiple pulse mode, Δt_{pulse} is the time between successive pulses, and t_{ping} is the ping period. When the single pulse approach is used, Δt_{pulse} is the same as t_{ping} and therefore depends on the acoustic travel time and the time needed to store the acquired data. However,

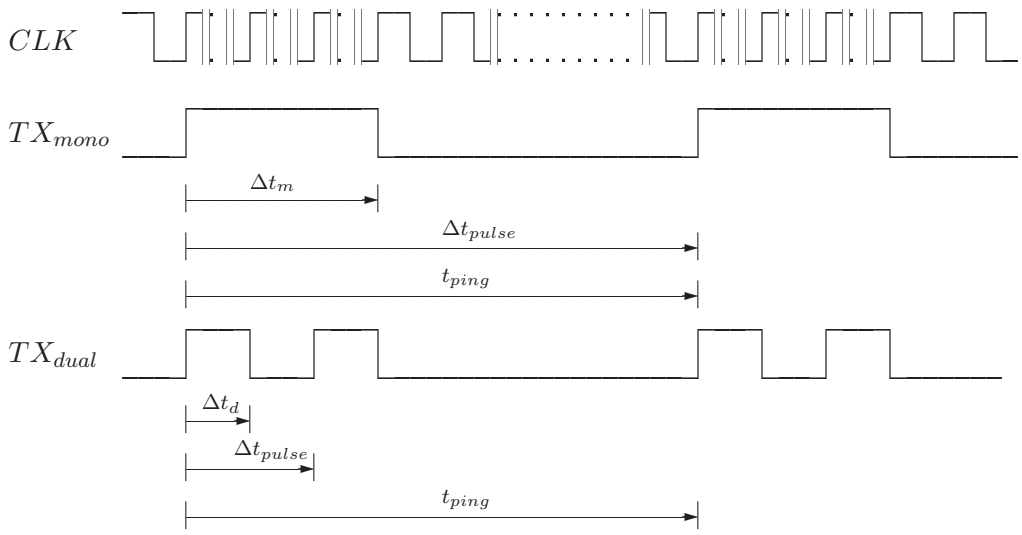

Figure 2.6: Timing diagram comparing the generation of the transmit pulses, with respect to the reference clock, for single pulse, TX_{mono}, and multiple pulse, TX_{dual}, schemes, during an operating cycle the new sonar system.

in the multiple pulse approach, Δt_{pulse} is set independently of t_{ping} and can be significantly reduced, such that its duration is very short as compared to t_{ping}. Therefore, the multiple pulse approach proves to be more practical for retrieving useful Doppler information from targets located at reasonable distances from the sonar, since it enables the sonar to detect slight target motions that would have been missed in the time taken between ping cycles.

2.2.3 Functional description of the FPGA-timing control block

A simplified block diagram of the modules that constitute the FPGA block for the timing control system is shown in Figure 2.7, and for completeness, a schematic diagram of the FPGA-timing control block is shown in Appendix A.1.

From Figure 2.7, the externally generated clock signal is fed through a DCM, part of the FPGA's clock distribution network, in order to ensure a clean and reliable clock reference source with 50% duty cycle, low clock jitter and skew. The output of the DCM is used as a reference clock source for all of the components in the FPGA-timing control block. When prompted, the FPGA is serially loaded with parameters from the PC that determine the

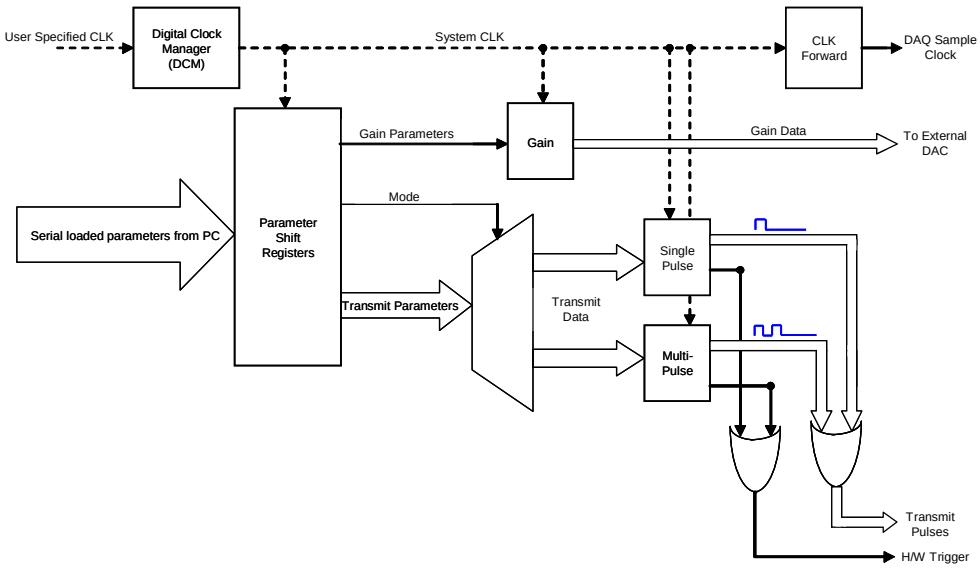

Figure 2.7: Functional block diagram of the FPGA-timing control module.

operating characteristics of the sonar. The FPGA can operate in either single-pulse or dual-pulse mode, and on selecting a mode, parameters are passed to the corresponding transmit module, which generates the appropriate trigger and transmit pulse signals on the system clock edge. The system clock is fed through a clock-forwarding module before being used as the DAB's sampling clock in order to ensure that all signals leave the FPGA synchronously, and thus synchronization between the timing control and DAB is maintained.

2.2.3.1 Verification of the ping period parameters through simulation

The parameters of the overall ping period for the new system, expressed in Equation 2.2, are simulated and shown in Figures 2.8 - 2.13.

The transmit pulses and DAB-trigger generated with respect to the DAB's sampling clock are shown in Figure 2.8. The parameter, δt_{wait}, is represented by the delay between the rising edge of the trigger signal and the start of the transmit pulses, and occurs eight clock cycles after the rising edge of the trigger, which corresponds to a delay of $208\,[ns]$ in this case. The dead time of eleven clock cycles, $286\,[ns]$, that exists between the end of the start counter and the first rising edge of the transmit pulse is necessary for the transmitter

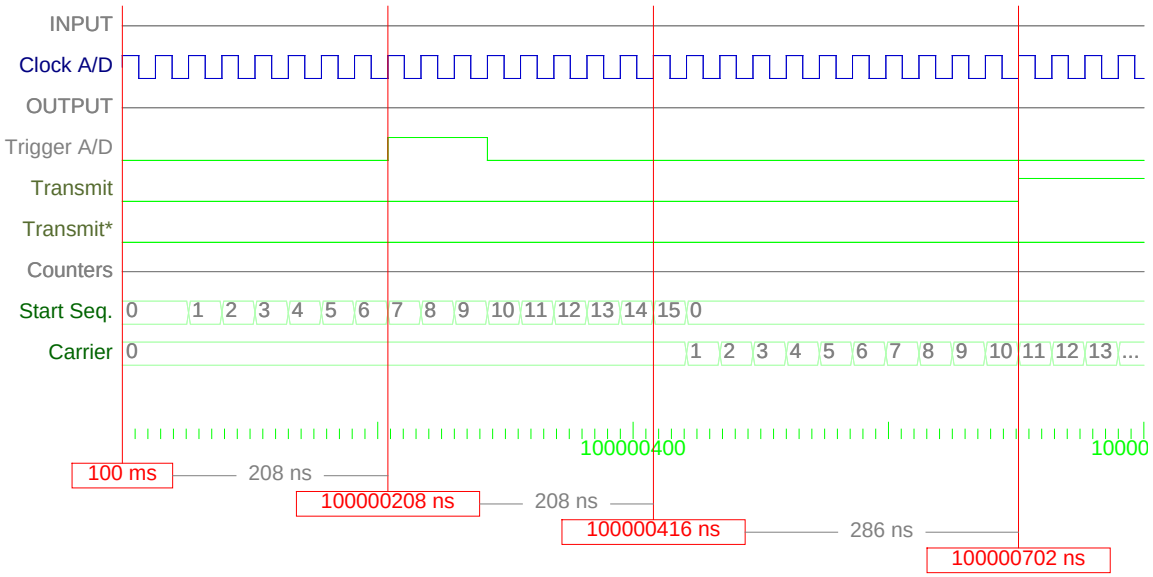

Figure 2.8: Timing simulation, created using ModelSim 6.2g, relating the FPGA-generated hardware trigger and the transmit signals w.r.t. the DAB's sampling clock. The timing module is configured to operate in single-pulse mode at 300 $[kHz]$, with a pulse width of 20 carrier cycles for 10 pings at a target 5 $[m]$ from the sonar.

stage of the system and is explained using Figure 2.9.

Instead of linear amplification, the sonar system uses an H-Bridge circuit to deliver power to its transmit transducer load [19]. In order to drive the H-Bridge, the FPGA generates a complementary pair of transmit pulses, $Transmit$ and $Transmit^*$. Figure 2.9 shows the relationship between these pulses generated on the transmit bus. In order to avoid shorting either side of the H-Bridge at any instant during operation, a dead time between the rising edges of the FPGA's transmit pulses is required, such that both pulses are never high at the same time. Figure 2.9 shows a dead time of eleven clock cycles between the rising edges of $Transmit$ and $Transmit^*$, which corresponds to 284 $[ns]$ in this case. This dead time provides a sufficient safety margin for using the H-Bridge.

An expanded view of the signals simulated in Figures 2.8 and 2.9 is shown in Figure 2.10 in order to demonstrate the generation of the pulse envelope in terms of carrier cycles. The parameter, t_{pulse}, is measured between the start of the transmit sequence and the falling edge of the last generated carrier cycle in a pulse. In this case, it is approximately 66.6 $[\mu s]$.

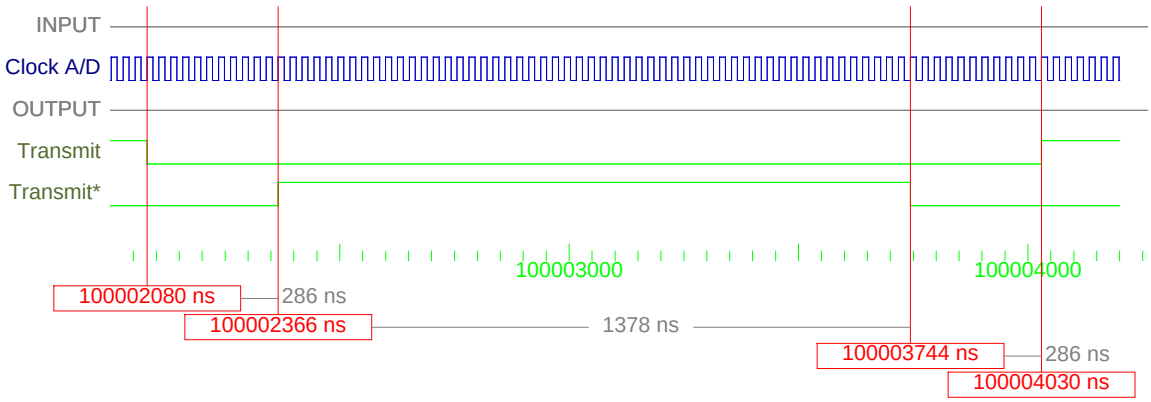

Figure 2.9: Timing simulation, created using ModelSim 6.2g, emphasizing the dead time between the FPGA-generated complementary transmit signals w.r.t. the DAB's sampling clock. The timing module is configured to operate in single-pulse mode at 300 $[kHz]$, with a pulse width of 20 carrier cycles for 10 pings at a target 5 $[m]$ from the sonar.

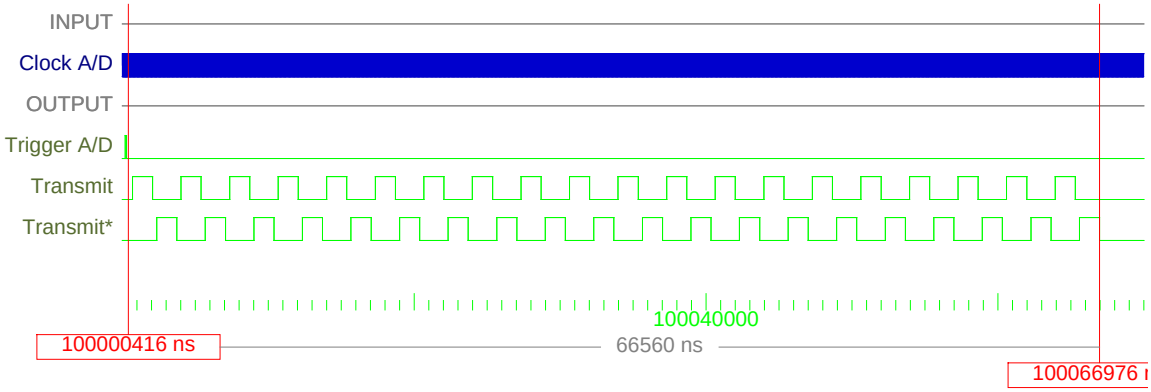

Figure 2.10: Timing simulation, created using ModelSim 6.2g, showing the FPGA-generated transmit signal envelope w.r.t. the DAB's sampling clock. The timing module is configured to operate in single-pulse mode at 300 $[kHz]$, with a pulse width of 20 carrier cycles for 10 pings at a target 5 $[m]$ from the sonar.

The pulse envelope shown in Figure 2.10 is further expanded in Figure 2.11, which emphasizes the relationships between the pulse envelope, acoustic travel time, t_{prop}, and data transfer delay, Δt_{wr}. The parameter t_{prop} is measured between the falling edge of the

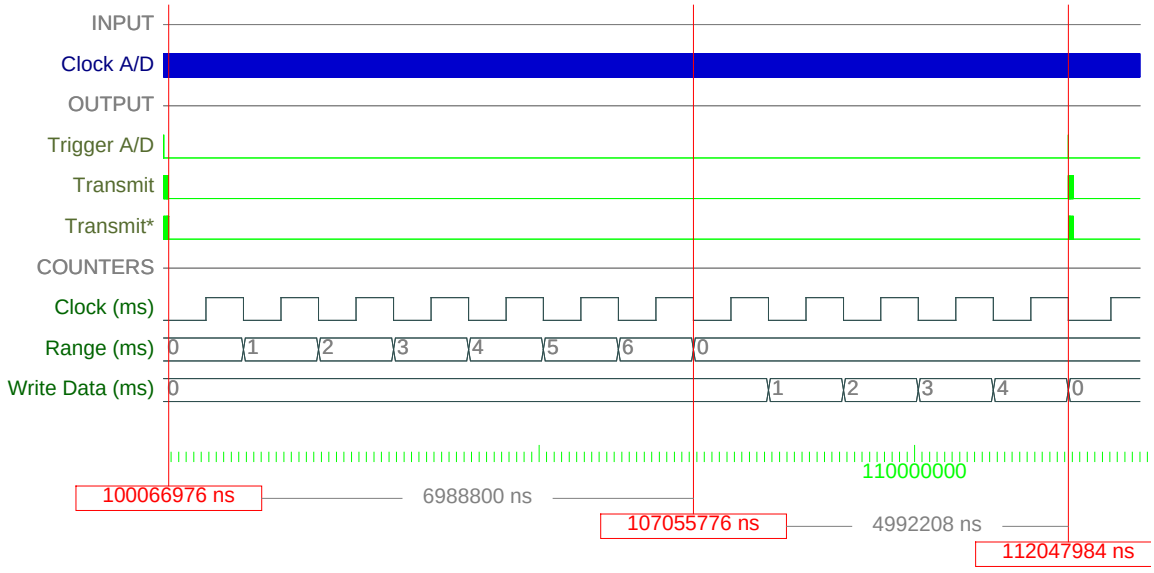

Figure 2.11: Timing simulation, created using ModelSim 6.2g, showing the FPGA-generated propagation and write delays w.r.t. the millisecond timer based on the DAB's sampling clock. The timing module is configured to operate in single-pulse mode at 300 $[kHz]$, with a pulse width of 20 carrier cycles for 10 pings at a target 5 $[m]$ from the sonar.

last generated carrier cycle and the start of the *Write Data* counter, and is 7.0 $[ms]$ in this case. The *Write Data* counter generates the data transfer delay, which is hardware limited, since it depends on the data transfer rate of the PC. This parameter must be configured by the user, based on the hardware used. For the purposes of simulation, Δt_{write} is set to 5.0 $[ms]$.

The simulated ping period of the new system is found by substituting these parameters into Equation 2.2, and agrees with the theoretical ping period calculated in Appendix A.2.

$$t_{ping} = 66560\,ns + 6988800\,ns + 4992208\,ns + 208\,ns \approx 12\,ms \tag{2.3}$$

The simulation waveforms generated when the new sonar system is configured in multiple pulse mode are shown in Figures 2.12 and 2.13. When compared to Figures 2.10 and 2.11,

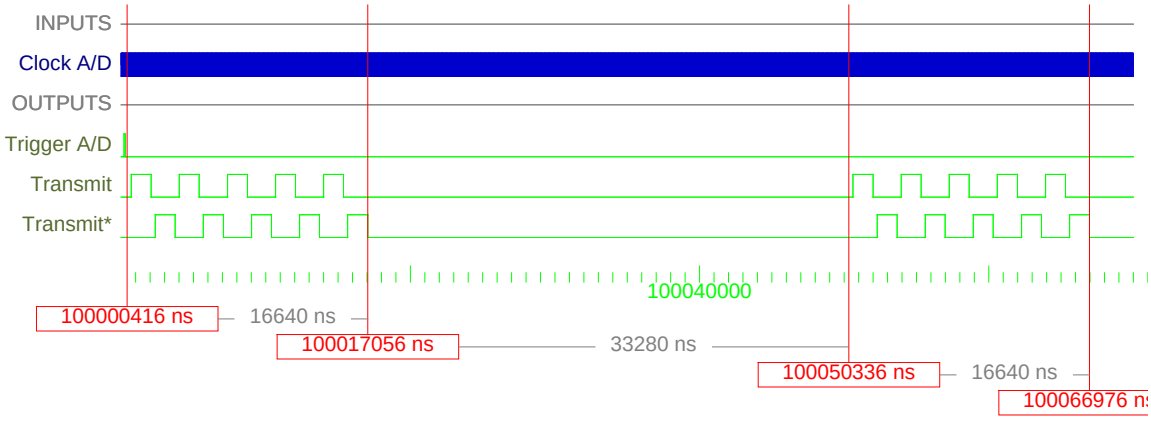

Figure 2.12: Timing simulation, created using ModelSim 6.2g, showing the FPGA-generated transmit signal envelope w.r.t. the DAB's sampling clock. The timing module is configured to operate in multi-pulse mode at 300 $[kHz]$, with a pulse width of 5 carrier cycles and a delay between pulses of 10 carrier cycles for 10 pings at a target 5.0 $[ms]$ from the sonar.

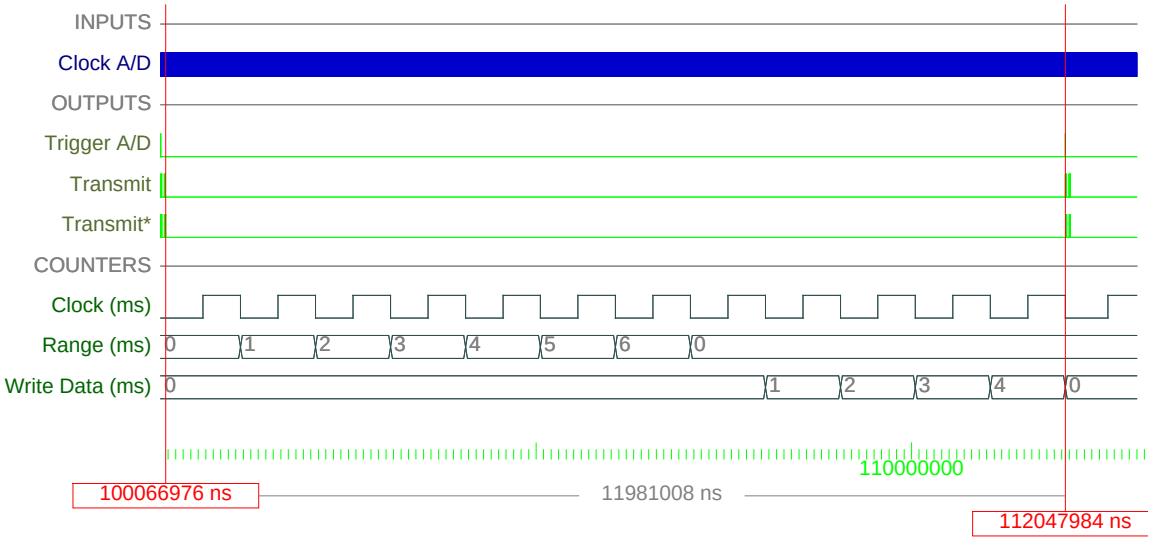

Figure 2.13: Timing simulation, created using ModelSim 6.2g, showing the FPGA-generated ping period. The timing module is configured to operate in multi-pulse mode at 300 $[kHz]$, with a pulse width of 5 carrier cycles and a delay between pulses of 10 carrier cycles for 10 pings at a target 5.0 $[ms]$ from the sonar.

in which the sonar is configured with equivalent overall pulse envelope and ping period parameters, Figures 2.12 and 2.13 show that delay between successive pulses can be set to be much shorter than the time taken for a ping cycle. In this case, the separation between two pulses is 33.3 $[\mu s]$, as compared to a ping period of 12 $[ms]$.

2.3 Summary of the benefits of an improved timing control on sonar performance

The timing control issues that hindered the performance of the URL sonar were solved by implementing a dedicated timing control system. This new timing control relies on an FPGA development board to ensure precise and fixed timing delays, and maintain synchronization between the transmit and receive subsystems of the sonar. In order to increase the ping rate of the sonar, a new data transfer algorithm was developed and implemented to interface the PC, timing control, and acquisition systems. Finally, an additional mode of operation was designed into the new timing control, which allowed the sonar to generate more than one transmit pulse envelope in a ping cycle. In this mode, the new sonar is capable of producing more complex transmit waveforms, allowing for further research into the development of algorithms for Doppler and synthetic aperture processing.

Chapter 3

Improving the SNR of a Sonar System

This chapter describes the approach taken to improve the SNR at the receiver of the URL sonar system (old sonar system), and provides theoretical and simulated data to justify the measured performance results discussed in Chapter 4. An improvements in SNR is achieved by minimizing elements specific to the URL's preamplifier that contribute to the overall noise of the receive system. By designing a new preamplifier with primary consideration being to minimize its noise effects, the overall noise contribution of the receive system is reduced, and thus the SNR at receiver is improved. These improvements are beneficial to the performance of the system, resulting in an increased practical useable bandwidth and an improvement in the system's capability to retrieve weak signals. This chapter briefly reviews the existing SNR related shortcomings of the URL's preamplifier, identifies the sources of these issues, and discusses the approach taken to minimize them.

Simulation data for the newly designed preamplifier are presented in order to predict the theoretical performance of the new subsystem, which can be compared to the measured results. The simulation data are calculated at both the input and output of the preamplifier (DAB-input) in order to determine the preamplifier's frequency response to noise. It should be noted that signals at the output of the preamplifier have been amplified by an overall gain of $49\,[dB]$, which equates to the combination of the cascaded gains of the low noise amplifier (LNA), time-varying gain (TVG) and output buffer stages, which are $20\,[dB]$, $29\,[dB]$, and $0\,[dB]$, respectively. For all calculations, the absolute operating temperature is assumed to

be 300 $[K]$, which is the typical operating temperature of a printed-circuit board (PCB).

In designing the new preamplifier, three noise suppression techniques, applied at the front-end of the preamplifier, are investigated. The first technique utilizes a low noise single-ended front-end to reduce the broadband noise generated by the preamplifier. While the other two techniques, diff-amp and transformer action, investigate differential front-end solutions that minimize the common-mode disturbances entering the system through the preamplifier. It is suggested that utilizing any of these techniques can be beneficial in preamplifier design. Both the diff-amp and the transformer solutions are useful in suppressing common-mode signals, and therefore, should reduce the interference lines existing in the power spectrum of the receive signal. However, in practice, the performance of the transformer is limited when applied to wide-band systems, such as the URL sonar system, due its impedance characteristics, and diff-amps currently available cannot compete with the broadband noise performance of existing op-amps. Therefore, the single-ended front-end solution is recommended as the best choice for the design, because of its superior broadband noise performance. It is also recommended that care should be given to grounding and shielding so as to reduce common mode interference sources as much as possible.

3.1 A brief review of the SNR issues in the URL sonar system

The consequences on the power spectrum of the major disturbances that adversely affect the noise power and limit the SNR of the URL sonar system are shown in Figure 3.1. These disturbances result in increased noise power and cause interference lines to appear throughout the power spectrum of the received signal. Specifically, internally generated noise sources from the transducer, preamplifier, and DAB increase the broadband noise power of the system, masking and limiting the minimum recoverable signal. Externally generated noise sources from EMI and common-mode voltages couple into the return signal path, resulting in the appearance of interference lines that may occur in close proximity to the pass-band of interest and significantly limit the practical bandwidth of the system. This chapter considers noise sources which are generated by and enter the system through the receive preamplifier.

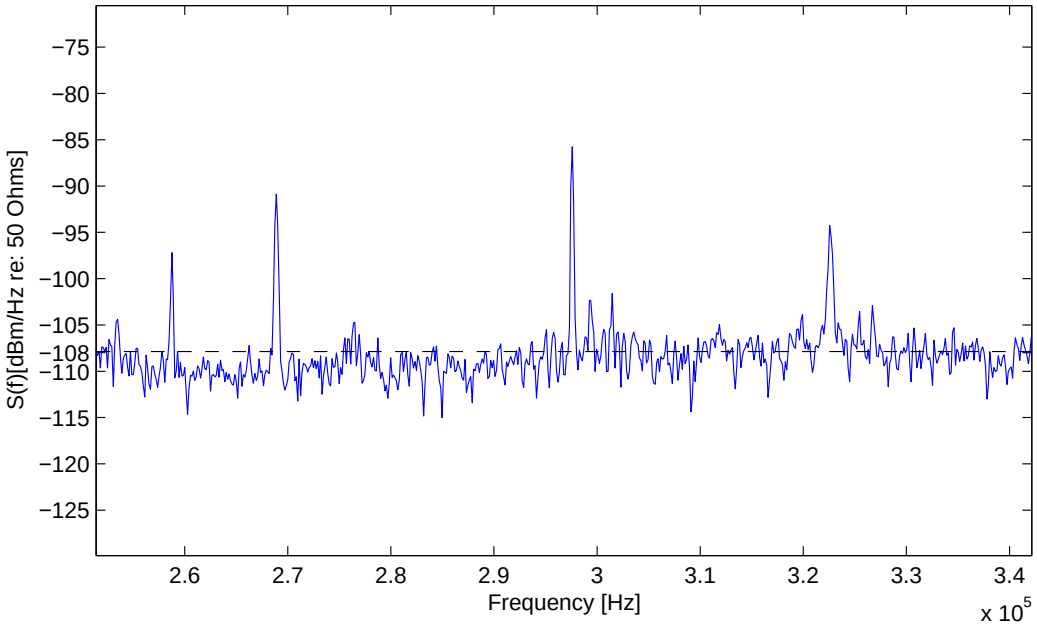

Figure 3.1: Power spectral density showing the output of a single channel of a of six channel, 300 [kHz] transducer, obtained using the URL sonar system receiver with the transmitter off, and an overall preamplifier gain setting of 49 $[dB]$. Where $S(f)$ is the power of the sampled receive signal in dBm referred across a 50 $[\Omega]$ load. The average broadband noise power spectral density (NPSD) is approximately $-108\,[\frac{dBm}{Hz}\,re:50\,\Omega]$. Interference lines are visible through out the pass-band.

3.1.1 Noise generated by the receive preamplifier of the URL sonar system

Noise sources generated by circuit components within electronic systems have been thoroughly researched and characterized in the literature [16, 20, 21, 22], and various analytical and pre-build manufacturing techniques have been designed to model, suppress and negate their effects [15]. In systems operating in the hundreds of kilohertz frequency range, such as the URL sonar system, the dominant noise source is likely to be thermal noise. A reasonable estimate of the noise contribution of these systems can be predicted using analytical methods, such as those described in [23, 24]. Furthermore, in multistage cascaded circuits, the first stage amplifier usually establishes the "noise floor" of the circuit [16], as once the signal has been amplified, the noise contribution due to subsequent stages becomes less

significant. This is especially important in the URL's preamplifier, which uses a ladder attenuation network IC [25] for its second stage TVG control, and thus requires an ultra low-noise amplifier preceding this stage to achieve the best noise performance. A close estimate of the noise contributed by the URL's preamplifier can be found by calculating the noise generated by its front-end LNA, as shown in Appendix B.1, and summarized in Table 3.1. Comparing the results in Table 3.1 to Figure 3.1 shows that the estimated noise power spectral density (NPSD) of the LNA stage closely matches the measured NPSD of the entire preamplifier. Furthermore, since the noise generated by the receive system is dominated by the URL's preamplifier, the shape of the NPSD plot is mainly influenced by the preamplifier's frequency response, which is flat in the frequency region of interest.

Table 3.1: Noise contributed by the front-end LNA stage of the URL's preamplifier rated at the input (RTI) and output (RTO) of the preamplifier.

Noise	Voltage $\left[\frac{nV}{\sqrt{Hz}}\right]$	Power $[\frac{dBm}{Hz}\ re: 50\,\Omega]$
RTI	2.93	-157.65
RTO	825.67	-108.65

3.1.2 Noise coupling into the URL sonar system

Figure 3.2 shows the receive transducer interfaced to the preamplifier through a shielded twisted-pair cable, and demonstrates the paths noise sources can take to enter the signal path of the system. E_D models the noise sources generated by devices external to the sonar that capacitively couple into the cable's shield, resulting in a current that flows to ground through the cable's shield. E_{AB} models the potential difference existing between the grounding points of the two sub-systems, and also causes a current to flow through the cable's shield. For the configuration shown in Figure 3.2, the currents flowing through the cable's shield, due to E_D and E_{AB}, are coupled into the signal path through the parasitic capacitances that exist between the cable's shield and the conducting wires.

Since the URL sonar system uses a single-ended front-end to interface to its transducer, no common-mode rejection is provided and the system is susceptible to the effects of these noise sources, which are common to both inputs of the preamplifier. The effect of these noise sources is evidenced by interference lines in the power spectrum of the signal. These

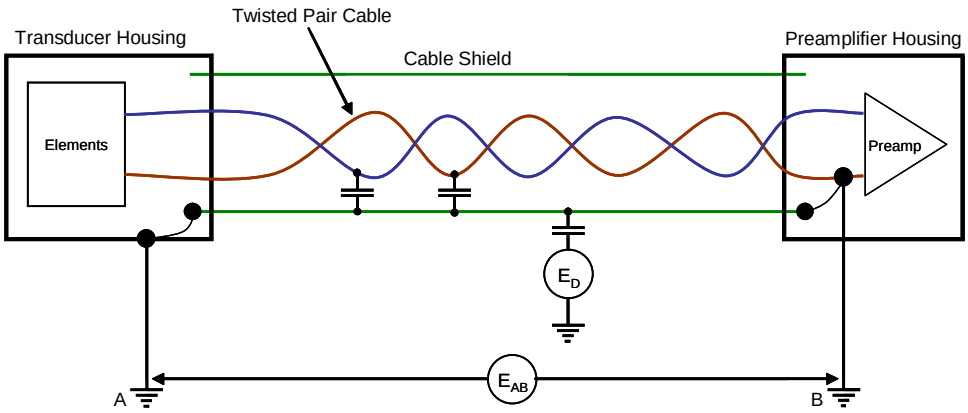

Figure 3.2: Model of the cable interface between the receive transducer and the preamplifier showing the paths noise sources can take via the cable shield to enter the signal path of the system. E_D represents the noise sources generated by devices external to the sonar, and E_{AB} represents the potential difference that exists between the grounding points of the two sub-systems.

lines, which may be in close proximity to the pass-band of interest, can significantly limit the practical bandwidth of the system. These noise sources increase as cable lengths and junctions increase between the two subsystems.

3.2 Improving on the SNR shortcomings of the URL sonar system

3.2.1 Reducing the contribution of the noise generated by the receive preamplifier

The new receive preamplifier is designed to generate less intrinsic noise than the transducers to which it is connected. In this way, the preamplifier is no longer the dominant noise source in the receive system, and instead the noise performance of the system is limited by the impedance of the transducer.

The intrinsic noise sources generated by the existing preamplifier were reduced by choosing components with low noise characteristics and by lowering the values of their surrounding resistive components. Improvements to the front-end LNA were of particular importance, since this stage establishes the "noise floor" of the preamplifier.

3.2.1.1 Functional description of front-end LNA stage

The new LNA stage is shown in Figure 3.3. The op-amp chosen for this stage, described in

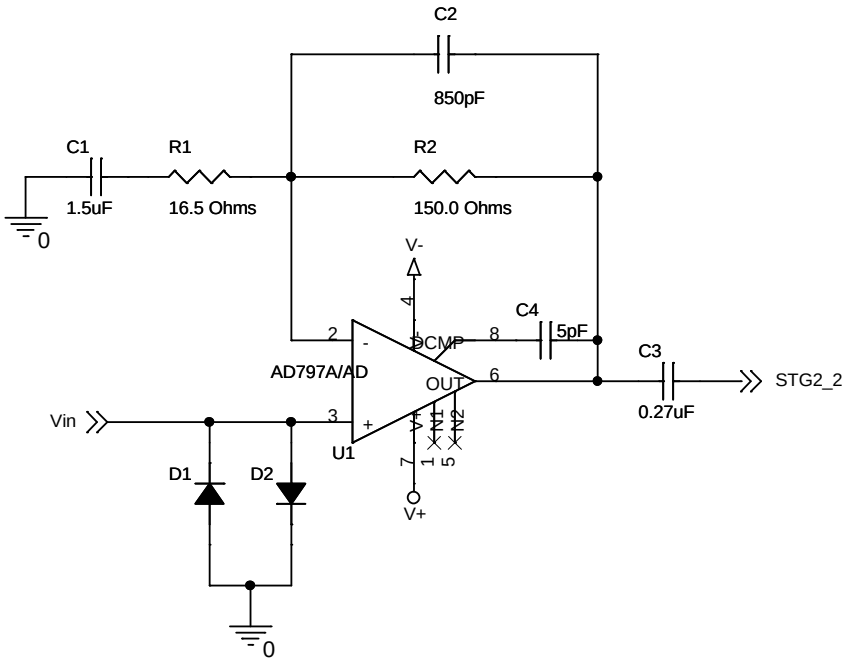

Figure 3.3: Partial schematic diagram of the new single-ended preamplifier showing the new front-end LNA stage, including limiting diodes.

[13], has very low noise, low distortion and low output impedance characteristics over the operating frequency range of the sonar system. The stage is designed with no termination or bias current compensation resistors, but instead relies on the op-amp's high non-inverting impedance, $10\,[M\Omega]$, to terminate the incoming signal. Using this approach preserves the receive signal strength by reducing the loading effects that occur when the transducer is interfaced to the preamplifier, and improves noise performance by eliminating the noise sources due to the shunt terminating and bias current compensation resistors. However, this approach also results in a significant increase in the DC offset voltage generated by the stage, as shown in Appendix B.2. This increase in offset voltage is due to an unusually large imbalance in input currents, which is caused by the bias cancelation feature of the op-amp [13]. High-pass filters formed by component pairs C_1, R_1, and C_3 and the input resistance of

the preamplifier's second stage eliminate the effects of this DC offset on subsequent stages of the preamplifier.

R_1 and R_2 set the gain for the stage, and are very small to reduce their noise contributions. This is possible since the op-amp chosen has high output current drive specifications, between $30\,[mA]$ and $80\,[mA]$. Therefore, it is capable of handling high feedback currents and sourcing very low impedance loads without being overloaded.

C_2 and R_2 create a low-pass filter that, in combination with the low pass filter of the output buffer stage, limits the bandwidth of the amplifier, reducing the effects of aliasing when the signal is sampled.

Finally, D_1 and D_2 limit the signal at the input of the op-amp, and prevent the output of the LNA stage from being driven into saturation. The characteristics of the front-end LNA are summarized in Table 3.2, and the frequency response of the preamplifier is shown in Figure 3.4. A complete schematic of the new preamplifier is provided in Appendix B.3. Figure 3.4 shows that the front-end LNA stage of the new preamplifier has a gain

Table 3.2: Summary of specifications and components for the front-end LNA of the new preamplifier.

Filter Specifications:			
	Lower [3 dB] Cutoff (f_{hp})	10.0	kHz
	Upper [3 dB] Cutoff (w/ output buffer) (f_{lp})	800.0	kHz
	DC Gain (A_v)	10.1	$\frac{V}{V}$
Component Values:			
	R_1	16.5	Ω
	R_2	150	Ω
	C_1	1.5	μF
	C_2	850	pF
	C_3	0.27	μF
	C_4	5	pF

of approximately $20\,[dB]$ and nearly linear phase over the frequency band of interest. The $-3\,[dB]$ break frequencies of the preamplifier occur at approximately $10\,[kHz]$ and $800\,[kHz]$, respectively.

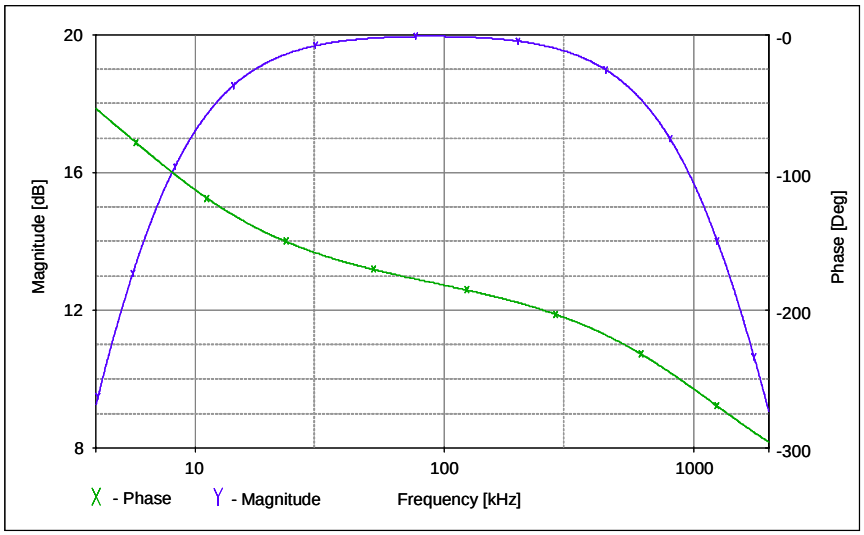

Figure 3.4: Frequency response of the new preamplifier with the single-ended front-end LNA and the TVG gain set to $0\,[dB]$ (i.e. an overall preamplifier gain of $20\,[dB]$).

3.2.1.2 Noise analysis of the front-end LNA stage

Table 3.3 summarizes the results of the noise analysis calculated using the noise model for the LNA stage of the new preamplifier, shown in Figure 3.5. Complete noise calculations

Table 3.3: Noise contributed by the new front-end LNA rated at the input (RTI) and output (RTO) of the new preamplifier.

Noise	Voltage $\left[\frac{nV}{\sqrt{Hz}}\right]$	Power $[\frac{dBm}{Hz}\ re:50\,\Omega]$
RTI	1.028	-166.74
RTO	289.69	-117.74

for the new LNA stage can be found in Appendix B.4.

Comparing the results in Tables 3.1 and 3.3 shows an expected improvement in NPSD of approximately $9\,[dB]$. The expected noise voltage at the input of the new preamplifier is approximately 1.028 $\left[\frac{nV}{\sqrt{Hz}}\right]$, which is equivalent to the noise generated by a $64\,[\Omega]$ resistor, and much lower than the minimum real component of the impedance, $155\,[\Omega]$, measured for

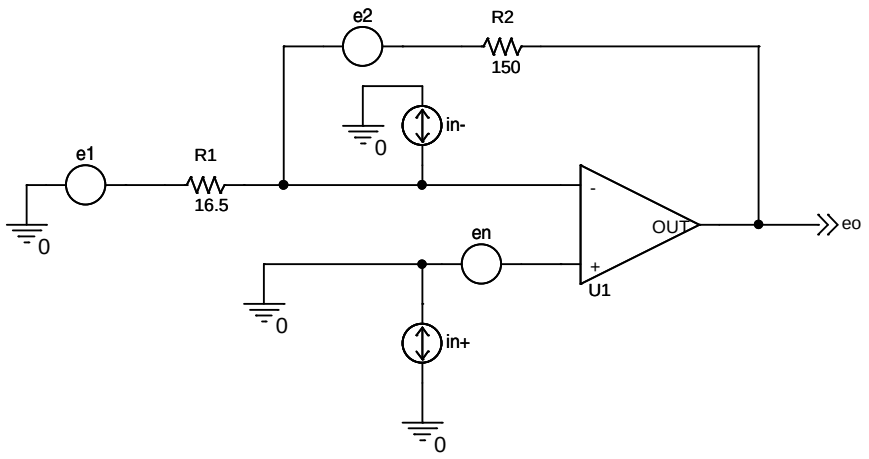

Figure 3.5: Noise model for the new front-end LNA, ignoring bandlimiting capacitors.

the transducers currently available in the URL.

The simulated noise responses for the new LNA and the complete preamplifier are shown in Figures 3.6, and 3.7. From Figure 3.6, the broadband noise voltage of the new front-

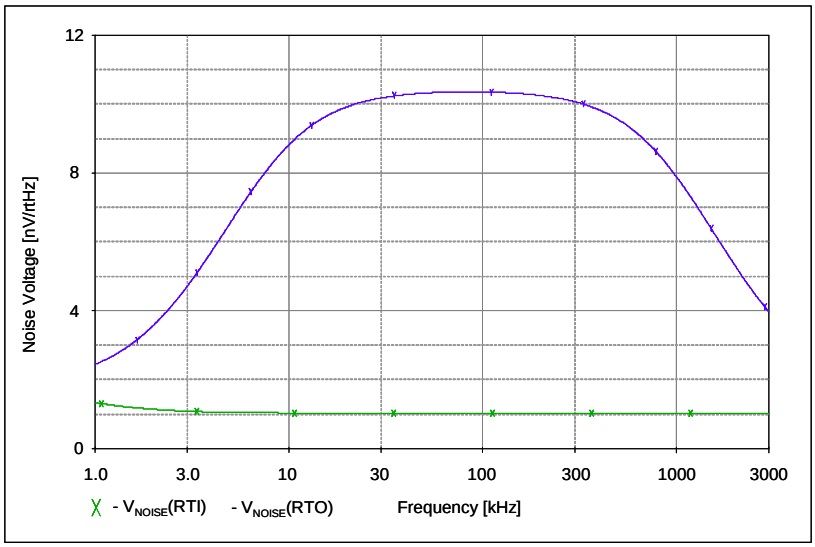

Figure 3.6: Simulated noise spectral density response of the new front-end receive LNA, including bandlimiting capacitors. Where V_{onoise} is the noise voltage (RTO), and V_{inoise} is the noise voltage (RTI).

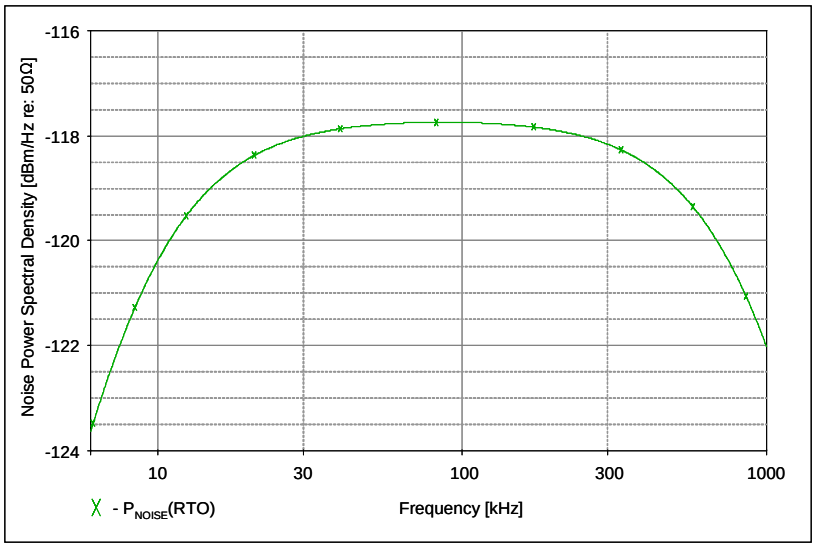

Figure 3.7: Simulated NPSD at the output of the new preamplifier, including bandlimiting capacitors. The overall gain of the preamplifier is 49 $[dB]$.

end LNA is 1.028 $\left[\frac{nV}{\sqrt{Hz}}\right]$ (RTI) and 10.37 $\left[\frac{nV}{\sqrt{Hz}}\right]$ (RTO), and corresponds to the calculated values summarized in Table 3.3. The plot also shows that the noise voltage at the output of the new LNA will be bandlimited between 6 $[kHz]$ and 1.2 $[MHz]$ due to the filtering capacitors in the stage.

The noise response of the complete preamplifier, in Figure 3.7, shows that the $-3\,[dB]$ cutoff frequencies occur at approximately 10 $[kHz]$ and 800 $[kHz]$, due to the filtering capacitors in the circuit, and the expected NPSD is approximately -117.7 $\left[\frac{dBm}{Hz}\, re : 50\,\Omega\right]$ over the operating frequency of the sonar, which corresponds to the calculated values summarized in Table 3.3.

3.2.2 Suppressing the interference lines due to EMI and common-mode signals entering the preamplifier

The interference lines caused by common-mode noise entering the receive signal path of the system were reduced by employing a differential stage at the input of the preamplifier. In this way, signals common to both inputs of the preamplifier were rejected, while any voltage differences occurring between the two inputs were amplified. This contrasts to

the single-ended approach, previously discussed, which provides no common-mode rejection and transfers common-mode signals to the output of the stage through its feedback network. Two solutions that utilized differential inputs in the new preamplifier were evaluated. One takes advantage of the high common-mode rejection characteristics of a diff-amp, while the other uses transformer action to reduce interference common to both preamplifier inputs.

3.2.2.1 Differential amplifier front-end solution

Diff-amps are specifically designed to have very high common-mode rejection characteristics over a wide frequency range. This property is particularly useful in the URL sonar system, which can be required to recover very weak signals from noisy environments.

The topology of the monolithic diff-amp chosen for the new preamplifier is shown in Figure 3.8. This diff-amp uses an active feedback architecture, described in [14], to achieve

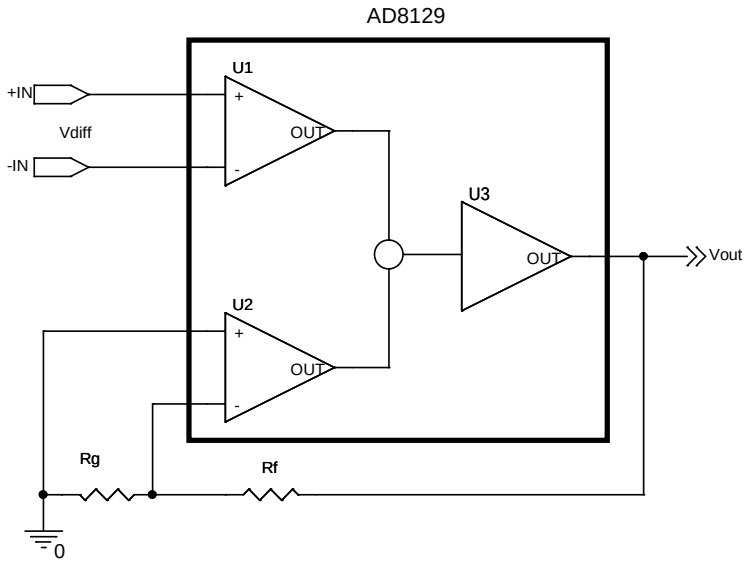

Figure 3.8: Topology of the diff-amp IC used in the front-end gain stage of the new preamplifier.

high common-mode rejection at high frequencies that is independent of input impedance. The circuit built around this amplifier IC has a common-mode rejection ratio (CMRR) between 95 $[dB]$ and 105 $[dB]$ over the frequency range of the receiver system.

The diff-amp chosen has a very high input impedance, 10 $[M\Omega]$, as compared to conventional diff-amps, and therefore is less susceptible to transducer loading, and preserves the

received signal voltage at the input of the preamplifier. Unlike conventional instrumentation amplifiers (in-amps), it does not require precisely matched resistors to achieve high CMRR, or extra op-amps which limit the bandwidth of the system.

3.2.2.2 Functional description of front-end diff-amp stage

Figure 3.9 shows the front-end diff-amp stage designed to eliminate the interference lines. The incoming differential signal at inputs IN^+ and IN^- is subject to very little loading

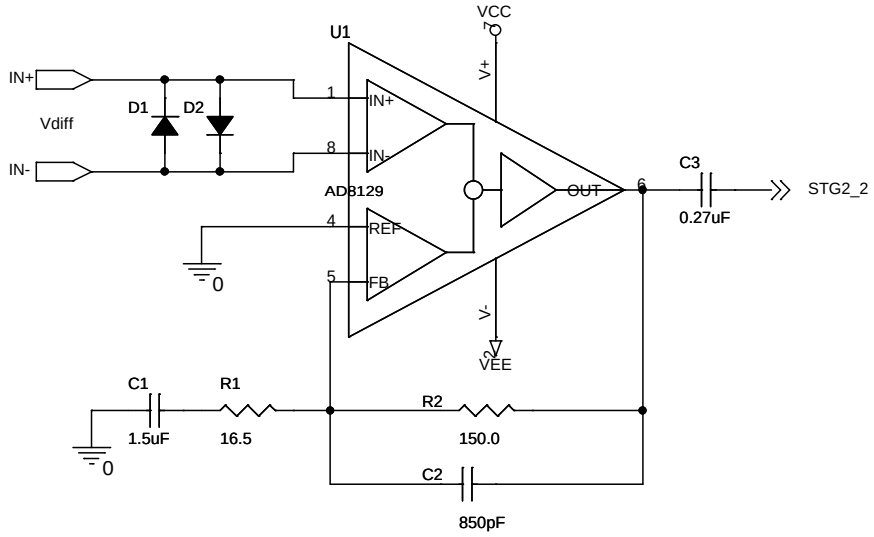

Figure 3.9: Front-end diff-amp stage of the new preamplifier.

effects due to the IC's high input impedance, and common mode signals are highly rejected here due to the IC's high CMRR. Similar to the single-mode solution, high-pass and low-pass filters about the system's frequency range limit the bandwidth of the preamplifier. The characteristics of the diff-amp stage are summarized in Table 3.4, and frequency response plots are shown in Figure 3.10.

Figure 3.10 shows that the diff-amp stage of the new preamplifier has a gain of $20\,[dB]$ and a flat magnitude and nearly linear phase over the frequency band of interest. The $-3\,[dB]$ break frequencies occur at approximately $10\,[kHz]$ and $800\,[kHz]$, respectively.

Table 3.4: Summary of specifications and components for the front-end diff-amp of the new preamplifier.

Filter Specifications:			
	Lower [3 dB] Cutoff (f_{hp})	10.0	kHz
	Upper [3 dB] Cutoff (w/ output buffer)(f_{lp})	800	kHz
	DC Gain (A_v)	10.1	$\frac{V}{V}$
Component Values:			
	R_1	16.5	Ω
	R_2	150	Ω
	C_1	1.5	μF
	C_2	850	pF
	C_3	0.27	μF

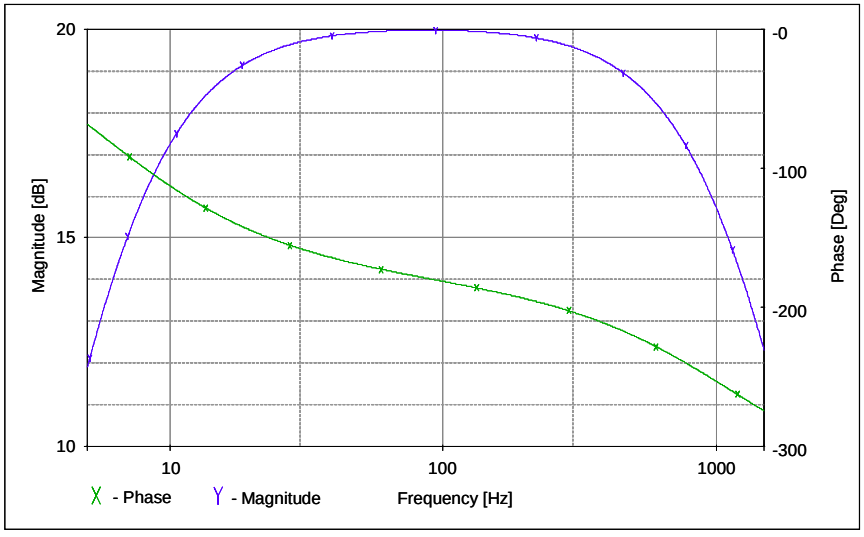

Figure 3.10: Frequency response of the new preamplifier with the front-end diff-amp stage and the TVG gain set to 0 $[dB]$ (i.e. an overall preamplifier gain of 20 $[dB]$)

3.2.2.3 Noise analysis of the front-end diff-amp stage

Table 3.5 summarizes the noise generated by the diff-amp stage of the new preamplifier. When compared to Tables 3.1 and 3.3, Table 3.5 shows a loss in broadband noise performance

Table 3.5: Noise contribution of the new front-end diff-amp stage rated at the input (RTI) and output (RTO) of the new preamplifier.

Noise	Voltage $\left[\frac{nV}{\sqrt{Hz}}\right]$	Power $[\frac{dBm}{Hz}\ re:50\,\Omega]$
RTI	4.5	-153.93
RTO	126.81	-104.93

of $4\,[dB]$, as related to the old preamplifier, and $13\,[dB]$, as related to the new single-ended solution. This loss is significant. This highlights the major drawback in using a diff-amp in low-noise preamplifier design, in that it degrades the broadband noise performance of the preamplifier. Noise voltages of diff-amps and in-amps currently available cannot out-perform the noise voltages achieved by monolithic op-amps. The diff-amp chosen for this stage has a noise voltage of $4.5\left[\frac{nV}{\sqrt{Hz}}\right]$, which swamps the noise contributions of its surrounding components and dominates the noise generated in the stage. Although this noise voltage is very low when compared to other diff-amps and in-amps presently available, it represents a significant loss in performance when compared to $0.9\left[\frac{nV}{\sqrt{Hz}}\right]$ generated by the op-amp used in the singled-ended solution. However, the high common-mode rejection properties of the diff-amp will reduce the interference lines, which previously appeared in the system's pass-band, at least up to the broadband noise level of the preamplifier. Below this level, all signals are masked by the broadband noise, and no other conclusions can be drawn as to the diff-amp's effect on common-mode interference.

The choice between the single-ended and diff-amp solutions represents an important compromise in performance that must be considered in receive preamplifier design. This compromise depends on the practical environment in which the receive system is used. For example, a receive preamplifier that is integrated into a tow-fish package that contains other electronic subsystems, sensors and storage devices, is highly susceptible to common-mode interference, and it is difficult, if at all possible, to modify the preamplifier once the tow-fish is deployed in the field. In such a case, a diff-amp solution that suppresses EMI entering the

system would be more beneficial than achieving an ultra low broadband noise level, since it would preserve the practical bandwidth of the system.

A stand-alone system, such as the URL sonar system, has less rigid common-mode rejection requirements, since the effects of EMI can be managed in the field by applying grounding points, using shielding techniques, and slightly shifting the sonar's operating frequency to interference free regions. In this case, an ultra low broadband noise level, achieved by using the single-ended design, would be useful.

3.2.2.4 The Transformer solution

The URL's receive system operates over a wide frequency range, and therefore requires a wide-band transformer that provides isolation for common-mode signal rejection and maintains its transmission characteristics over a wide range of input frequencies. The electrical equivalent circuit of the front-end receive electronics including a wide-band transformer is shown in Figure 3.11. The derivation of the lumped element models for the transducer and

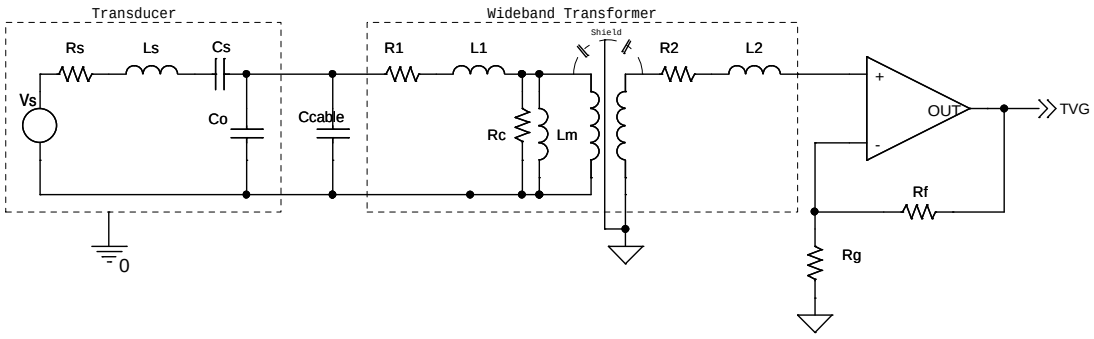

Figure 3.11: Electrical equivalent circuit of the front-end of the sonar receiver operating near resonance showing the receive transducer interfaced to the receive preamplifier through a wide-band transformer. Where: R_s, L_s, C_s represent the mechanical resonance, and C_0 is the clamped capacitance associated with the transducer; C_{cable} represents capacitive losses due to the cable; R_1, R_2, L_1, L_2 represent the winding losses in the transformer, and R_c, L_m represent the core losses and magnetizing inductance associated with the transformer.

transformer are described in [26] and [27], respectively. Grounded electrostatic shielding between the primary and secondary windings of the transformer, reduces the parasitic capacitances that are caused by coupling between the windings at high frequencies [16]. Using

this configuration, the magnetic coupling action of the transformer minimizes common-mode signals entering the receive preamplifier. The transformer provides the added benefit of compensating for signal loss due to capacitive loading by exploiting the parallel resonant circuit formed between its primary winding inductance and the capacitive loads associated with the transducer and the interfacing cable. However, this attribute is only achieved in a narrow-band operating sense, since each transducer, operating around a specific series resonant frequency, in the bandwidth of the preamplifier, has a specific capacitance associated with it, and thus would require its own specific transformer design to benefit from the primary winding tuning effects.

Many of the losses shown in Figure 3.11 on the operating parameters of the system can be minimized or negated by using materials and techniques described in [27]. For example, transducers with high output impedances tend to negate the effects of the resistive winding losses [28], and proper selection of core materials can significantly reduce the transformer's winding and core losses. The major drawback of using a wide-band transformer in the URL receive system is the loss of signal strength due to impedance mismatching. Wide-band transformers are typically designed for 50 [Ω] and 75 [Ω] systems, while for the URL receive system, neither the transducer nor the preamplifier are terminated with these resistances, when operating at series resonance. Therefore, the transformer will have a significant effect on the load seen by the signal at the output of the transducer source, distorting the expected frequency response of the system. This loading effect is verified in Chapter 4, where various transformers are added to the front-end of the single-ended preamplifier design, and experimental data are used to observe the resulting changes in the measured frequency response of the receive system.

3.3 Summary of the major conclusions drawn from the approach taken to improve the receive system's SNR

This chapter discussed the approach taken to improve the SNR at the receiver of the sonar by reducing system noise. Specifically, methods to suppress the noise generated by and entering the system through the receive preamplifier were investigated. In carrying out this investigation, a new single-ended preamplifier was designed to operate with a significantly smaller noise voltage contribution of 1.028 $\left[\frac{nV}{\sqrt{Hz}}\right]$, as compared to 2.930 $\left[\frac{nV}{\sqrt{Hz}}\right]$ generated by

the existing preamplifier, and 1.602 $\left[\frac{nV}{\sqrt{Hz}}\right]$ generated by the most quiet transducer available in the URL.

Two approaches were investigated to minimize the interference lines entering the system due to EMI and common-mode disturbances. These were a differential front-end, and transformer action. A diff-amp IC with an active feedback architecture was used to implement the differential front-end. This amplifier was shown to provide a high enough input impedance to avoid transducer source loading, usually a common drawback of conventional diff-amps, while maintaining common-mode rejection characteristics, which are not available using a single-ended design. By using this approach, it was predicted that the interference lines existing in the power spectrum of the returning signal could be reduced. However, this approach also resulted in a significant loss in broadband noise performance, since available op-amps tend to have better intrinsic noise characteristics than diff-amps and in-amps presently available.

It was suggested that a transformer could be used to reduce the common-mode EMI and ground-loop signals entering the system through the preamplifier. This approach is useful in the narrow-band case, when the system operates close to a single frequency, and has the added benefit of maximizing the received signal by tuning out capacitive losses due to the transducer and cables. However, this solution is more complicated for the wide-band case, when the system needs to operate over a broad range of frequencies. Impedance mismatches between the loads at the input and output of the transformer mean that the transformer can not be assumed to be transparent in the circuit, and results in unpredictable effects on the signal strength and phase due to the changing reflection coefficient.

Of the three approaches suggested in this chapter, the single-ended and diff-amp solution proved to be the most favorable. Both of these solutions had significant benefits, as relates to reducing components of the noise contributed by the receive preamplifier, and thus improved the SNR of the receive system. Choosing between these two approaches highlighted an important performance compromise that must be considered in preamplifier design. This compromise depends on the practical environment in which the receive system is used. In cases where sources of EMI and common-mode disturbances are prevalent and the system is not easily modifiable, such as in tow-fish and Autonomous Underwater Vehicles (AUVs), the common-mode rejection benefits of the diff-amp solution outweigh achieving ultra-low broadband noise levels. However, in stand-alone systems, such as the URL system, common-mode rejection requirements are less rigid, since EMI can be managed by applying grounding

points, using shielding techniques, and slightly shifting the sonar's operating frequency to interference free frequency regions. Therefore, in this case, the single-ended solution was chosen because of its superior broadband noise performance over the diff-amp solution. It was predicted to generate $13\,[dB]$ less broadband noise than the diff-amp solution, which represents a significant difference in performance between the two. Using the single-ended approach meant that the common-mode interference lines were still present in the power spectrum of the receive signal. Presently, in the field, various techniques involving grounding points, shielding, and slightly shifting the sonar's operating frequency are used to get around this problem. It is recommended that these techniques continue to be employed.

Chapter 4

Experimental Data and Results

This chapter presents the experimental results that verify the performance of the new timing control and new preamplifier subsystems designed and discussed in Chapters 2 and 3. The chapter begins with the functional verification of the new timing control subsystem, showing scope data at the output of the subsystem that can be compared to the simulation plots generated in Chapter 2. Experimental data are presented to confirm the proper implementation of the new preamplifier, and can be compared to the analysis and simulation data presented in Chapter 3. The effects of adding a transformer to the front-end of the new preamplifier are also shown in order to verify the claims made in Chapter 3.

4.1 Performance evaluation of the FPGA-based timing control system

This section provides measured results to verify the proper implementation of the new timing control subsystem, described in Chapter 2.

The PC was used to configure the timing control subsystem to operate in single-pulse mode at $300\,[kHz]$, with a pulse width of 20 carrier cycles for 10 pings at a target $5\,[m]$ from the sonar, and the scope was connected to display the four output lines of the timing control, as shown in Figure 4.1. Figures 4.2 - 4.7 show the signals observed on the scope display using these settings. These figures can be compared to the simulation results, shown in Figures 2.8 - 2.13, in Chapter 2, and confirm the parameters of Equation 2.2, in Chapter 2.

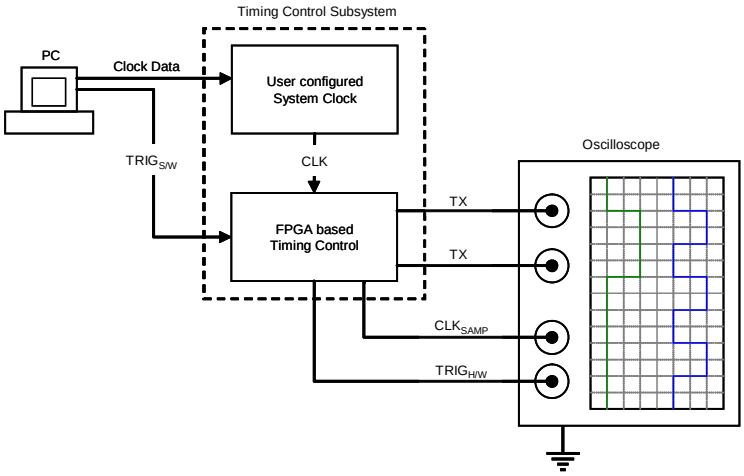

Figure 4.1: Test apparatus used to verify the functionality of the new timing control subsystem.

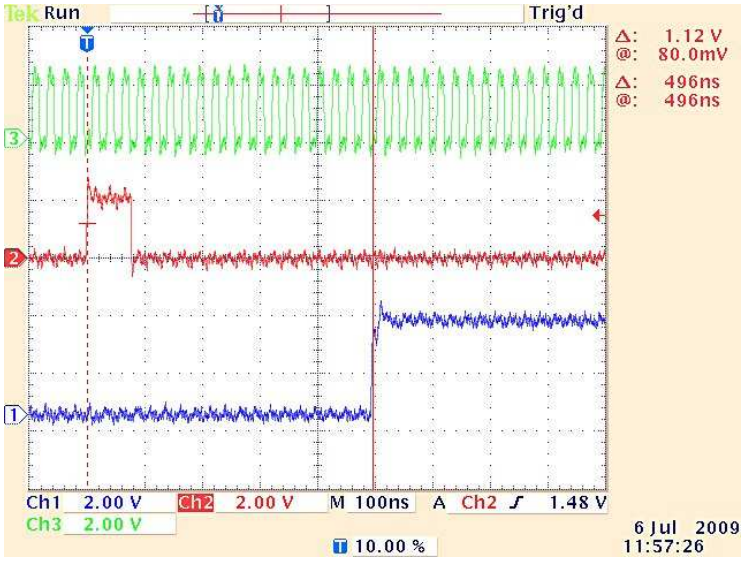

Figure 4.2: Signals generated on the sampling clock (CH3), hardware trigger (CH2), and TX (CH1) lines of the new timing control system during an operation cycle, emphasizing the timing relationship between the FPGA-generated hardware trigger and the first rising edge of the transmit signal envelope w.r.t. the sampling clock.

Figure 4.2 shows the output observed for the FPGA-generated trigger signal, and the start of a transmit signal envelope. From Figure 4.2, it can be observed that the duration of the trigger is three sample clock cycles, and the first rising edge of the transmit envelope occurs 496 $[ns]$ after the rising edge of the hardware trigger, which corresponds to the combination of the short delay, δt_{wait}, and the dead time required for the H-Bridge stage, explained in Chapter 2.

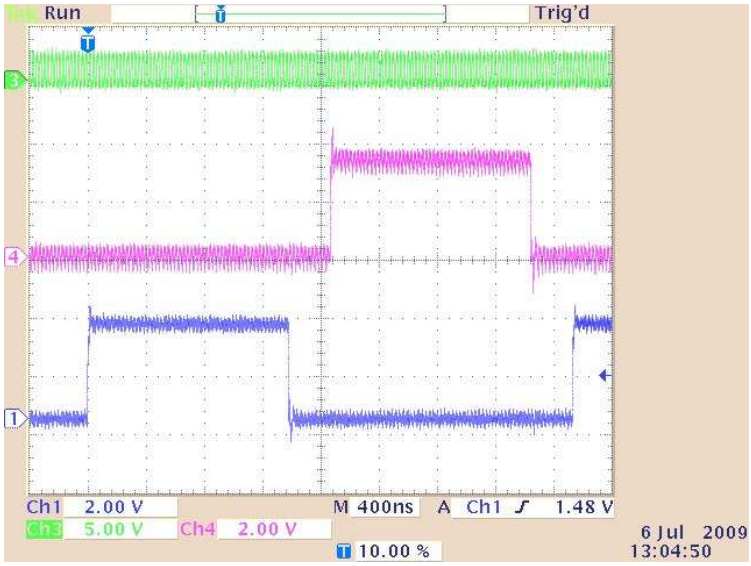

Figure 4.3: Signals generated on the TX (CH1) and TX^* (CH4) lines during an operation cycle, showing the timing relationship between a single cycle of the complementary pair of transmit signals w.r.t. the sampling clock (CH3).

Figure 4.3 shows the relationship between the FPGA complementary transmit signals. A magnified view, Figure 4.4, shows that the time between the first falling edge of the pulse on TX (CH1) and the first rising edge on the TX^* (CH4) is approximately 286 $[ns]$, which corresponds to the eleven sample clock cycles, and provides a sufficient safety margin for the H-Bridge stage. Further verification is provided by measuring the time between the first falling edge on TX^* (CH4) and the next rising edge on the TX (CH1), which is also 286 $[ns]$, as shown in Figure 4.5.

Figure 4.6 shows the entire 20 carrier cycle pulse envelope that is generated on the TX (CH1) and TX^* (CH4) lines. The time between the first rising edge of on the TX (CH1)

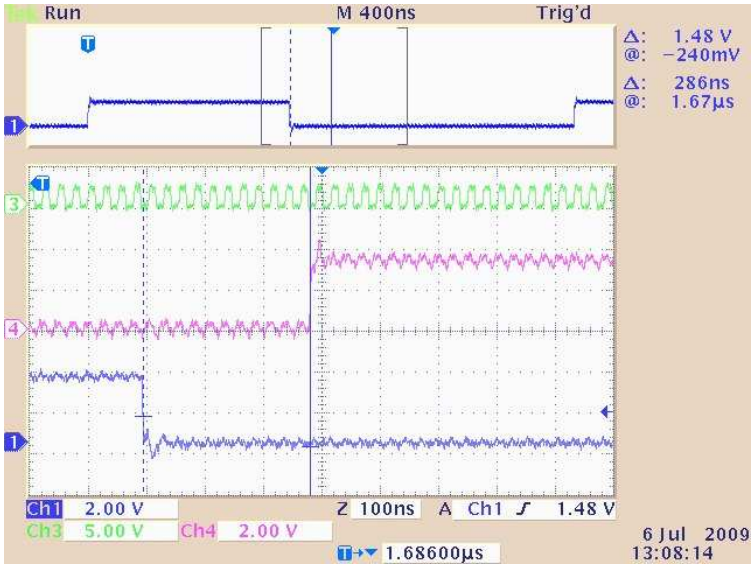

Figure 4.4: Magnified display of the signals generated on the TX (CH1) and TX^* (CH4) lines, showing the dead time between the complementary transmit pulses measured from the falling edge of TX to the rising edge of TX^*, w.r.t. the sampling clock (CH3).

line, and the final falling edge on the TX^* (CH4) line is approximately 66 $[\mu s]$, which equates to the time taken for twenty 300 $[kHz]$ carrier cycles.

Figure 4.7 shows that the time between successive pulse envelopes is approximately 12 $[ms]$, which corresponds to the combination of the acoustic travel time, t_{prop}, and the data transfer delay,Δt_{wr}, discussed in Chapter 2.

Using the PC, the timing control subsystem was reconfigured to operate in multi-pulse mode at 300 $[kHz]$, with a pulse width of 5 carrier cycles and a delay between pulses of 10 carrier cycles for 10 pings at a target 5 $[m]$ from the sonar. Figures 4.8 - 4.9 show the signals observed on the scope display using these new settings, and can be compared to Figure 2.13, in Chapter 2

Figure 4.8 shows the transmit pulse pair generated when the timing control is configured to operate in multi-pulse mode. From Figure 4.8, the time taken for an entire pulse pair envelope is 66.6 $[\mu s]$, which is equivalent to the 20 carrier cycle envelope, previously shown in Figure 4.6. The time taken to generate a single pulse envelope is approximately 17 $[\mu s]$, which equates to five 300 $[kHz]$ carrier cycles. The time between the final falling edge on

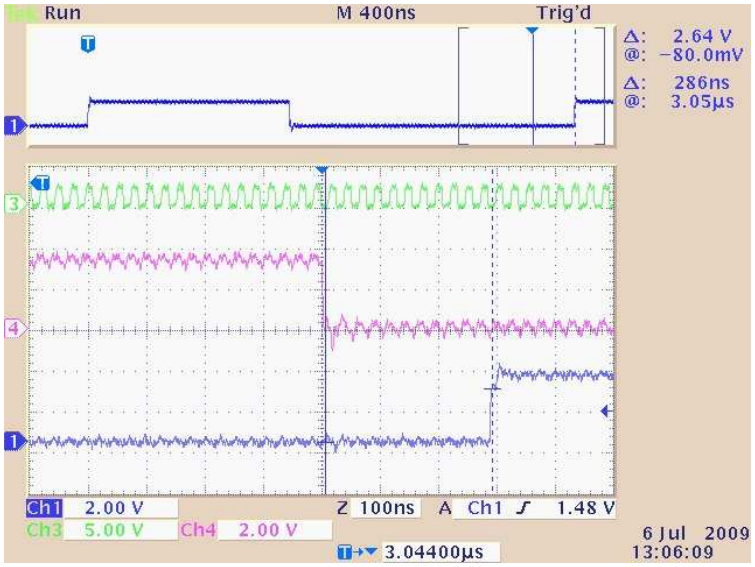

Figure 4.5: Magnified display of the signals generated on the TX (CH1) and TX^* (CH4) lines, showing the dead time between the complementary transmit pulses measured from the rising edge of TX to the falling edge of TX^*, w.r.t. the sampling clock (CH3).

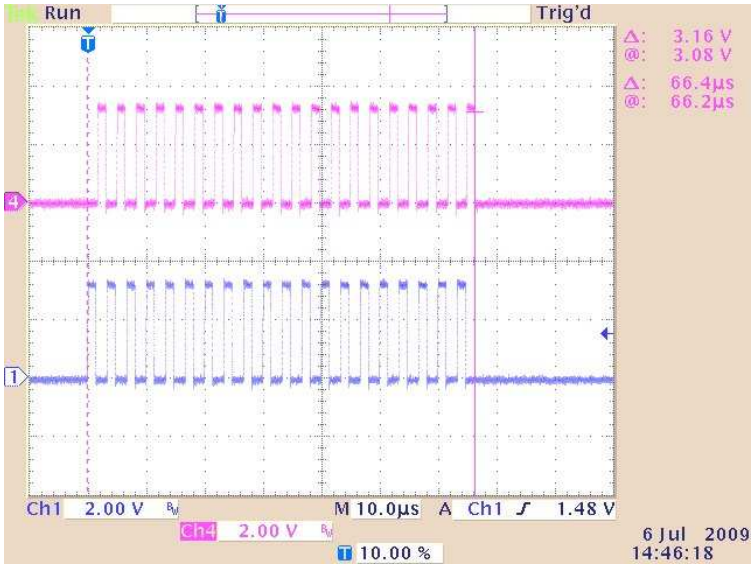

Figure 4.6: An entire 20 carrier cycle transmit burst generated on TX (CH1) and TX^* (CH4) lines, with the scope triggered on the sampling clock (CH3).

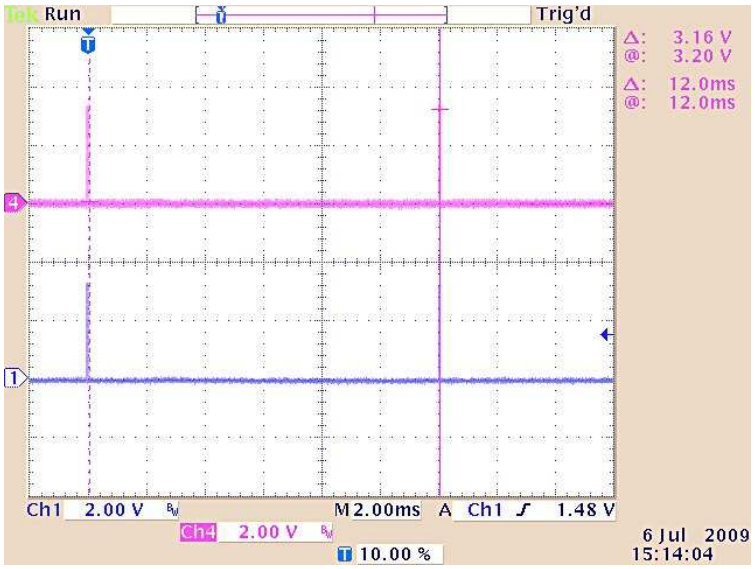

Figure 4.7: Signals generated on the TX (CH1) and TX^* (CH4) lines during an operation cycle, showing the time taken between two ping cycles, with the scope triggered on the sampling clock (CH3).

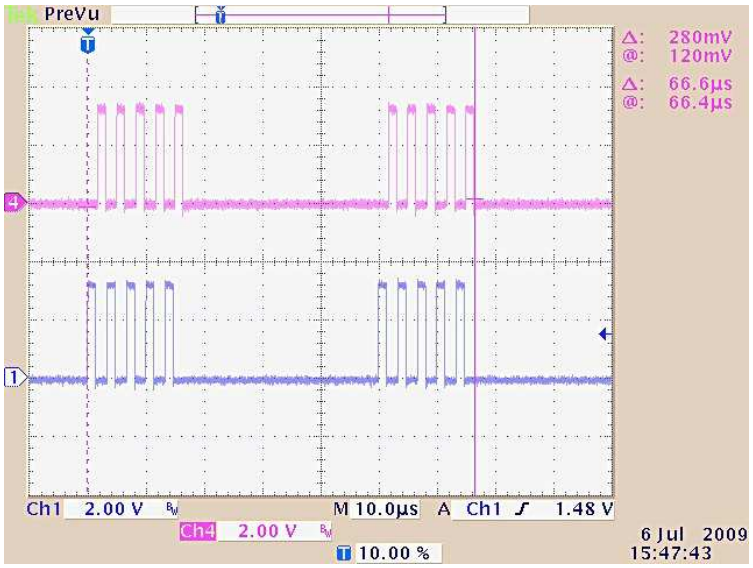

Figure 4.8: FPGA-generated transmit pulses on the TX (CH1) and TX^* (CH4) lines, with the scope triggered on the sampling clock, and the timing control in multi-pulse mode.

the TX^* (CH4) line and the first rising edge of the next pulse burst on the TX (CH1) line is 33.3 $[\mu s]$, and is equal to a delay of ten carrier cycles.

Figure 4.9 shows that the delay between the start of successive pulse pairs is the same as in Figure 4.7, in which the subsystem was configured for the same effective number of cycles, and the same delay.

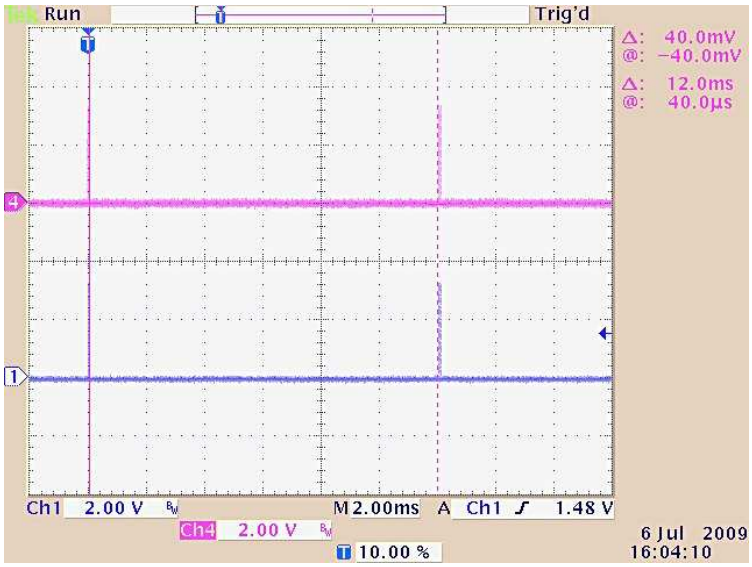

Figure 4.9: Signals generated on the TX (CH1) and TX^* (CH4) lines during an operation cycle, showing the time delay between successive ping sequences with the timing control operating in multi-pulse mode.

The output parameters measured and displayed in this section are observed to closely match the simulated results, shown in Chapter 2, and verify the functionality of the new timing control subsystem.

Figures 4.10 and 4.11 show the resulting transmit pulse envelope generated at the output of the transmitter system (output of the H-Bridge amplifier circuit, discussed in Chapter 2), which drives the transmit transducer load. In Figure 4.10, the transmitter is configured to output a 20 $[V_p]$ pulse train, and the twenty complementary transmit pulses on TX and TX^*, shown in Figure 4.6, are combined, through the H-Bridge, to generate the zero-centered AC waveform necessary to drive the transmit transducer. Similarly, in Figure 4.11, the transmitter is configured to output a 20 $[V_p]$ pulse train, and complementary transmit pulse

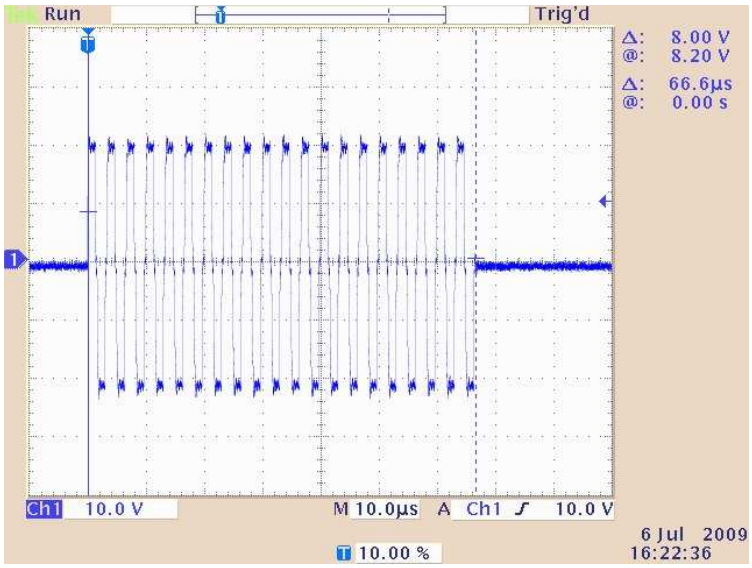

Figure 4.10: Transmit pulse envelope measured at the output of the transmitter, with transmitter voltage set to 20, and the timing control configured for single pulse mode.

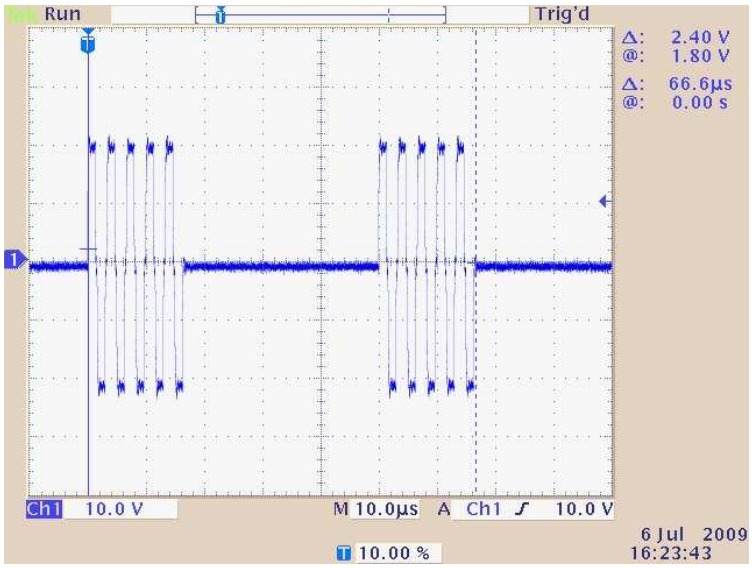

Figure 4.11: Transmit pulse envelope measured at the output of the transmitter, with the transmitter voltage set to 20, and the timing control configured for multi-pulse mode.

pair signals on TX and TX^*, shown in Figure 4.8, are combined, through the H-Bridge, to generate the zero-centered AC waveform necessary to drive the transmit transducer.

4.1.1 Performance of the new timing control during sonar operation

The sonar system was setup for bistatic operation across the four meter test tank in the URL, as shown in Figure 4.12. The new timing control subsystem was configured for 300 $[kHz]$, 40 carrier cycles per pulse envelope, 5 $[m]$ range operation, and the transmitter voltage was set to 20.

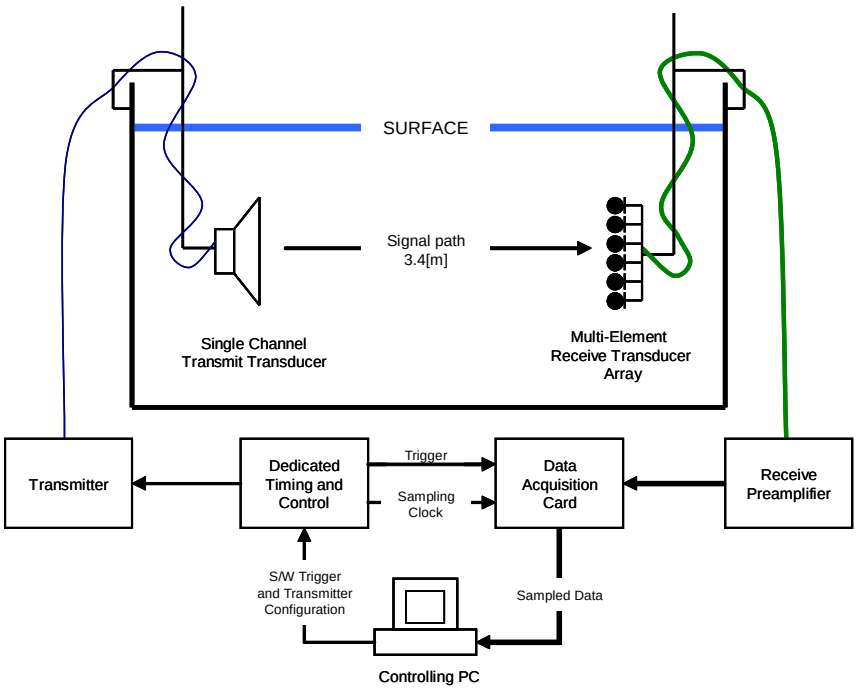

Figure 4.12: Sonar system configured for bistatic operation. The transmit and receive transducers are mounted 3.4 $[m]$ apart.

Figure 4.13 shows the pulse envelope received, in terms of its inphase and quadrature components, for the set-up shown in Figure 4.12. From Figure 4.13, a short received pulse is observed on all channels at a range between 1.5 $[m]$ and 2.0 $[m]$.

A magnified view of Figure 4.13, in Figure 4.14, shows that the signals on each channel start at the same range. This range is observed to be approximately 1.72 $[m]$, which is out a

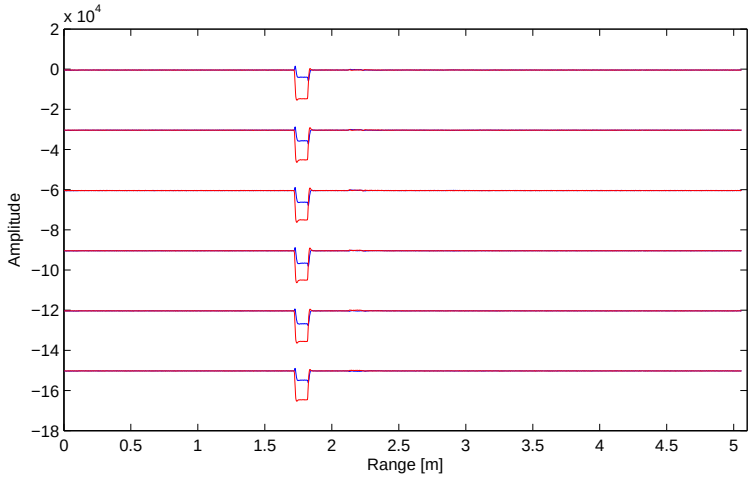

Figure 4.13: Pulses received by a six channel, 300 $[kHz]$ transducer located 3.4 $[m]$ away from the signal source. A single channel, 300 $[kHz]$ transducer is configured to generate a single 40 carrier cycle pulse envelope, and for a range of 5 $[m]$. The received signals are displayed in terms of their in-phase (blue) and quadrature (red) components. The y-axis represents the DAB's digital number corresponding to the signal amplitude and the x-axis is range in meters. Each channel is offset by 30000.

factor of two, but expected, since the system is designed for monostatic operation, meaning that the target range is computed as the distance the acoustic signal has to travel to the target and back to its origin. Therefore, a range of 1.72 $[m]$ in bistatic operation corresponds to half the actual distance, 3.44 $[m]$ in this case. Figure 4.14 also shows that the received pulse envelopes are not perfect square pulses (pulses with infinitely fast rise and fall times), but exhibit gradual rise and fall times. This pulse shaping is expected, and is caused by the bandpass filtering effect of the transmit and receive transducers. Specifically, components of the pulse envelope that occur at frequencies above the upper cutoff frequencies of these transducers are filtered out, resulting in the rounding of the pulse envelope, shown in Figure 4.14.

Figures 4.15 and 4.16 show the corresponding received pulse plots using the same set-up shown in Figure 4.12, but with the sonar operating in multi-pulse mode.

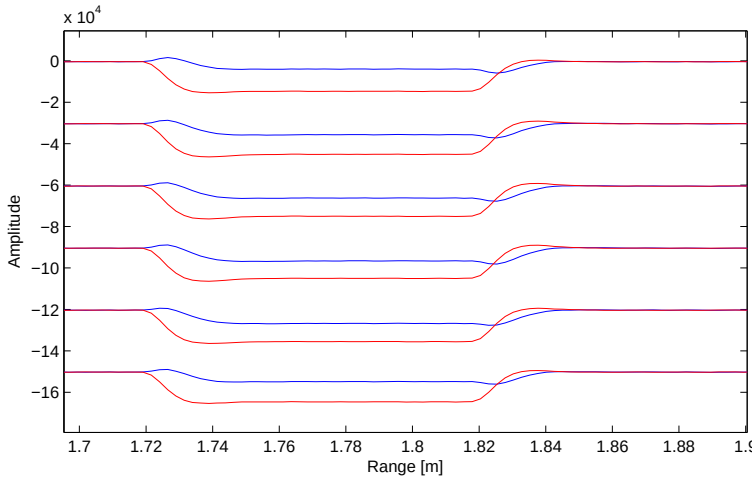

Figure 4.14: Magnified view of the pulses received by a six channel, 300 $[kHz]$ transducer located 3.4 $[m]$ away from the signal source. The sonar is operating in single-pulse mode.

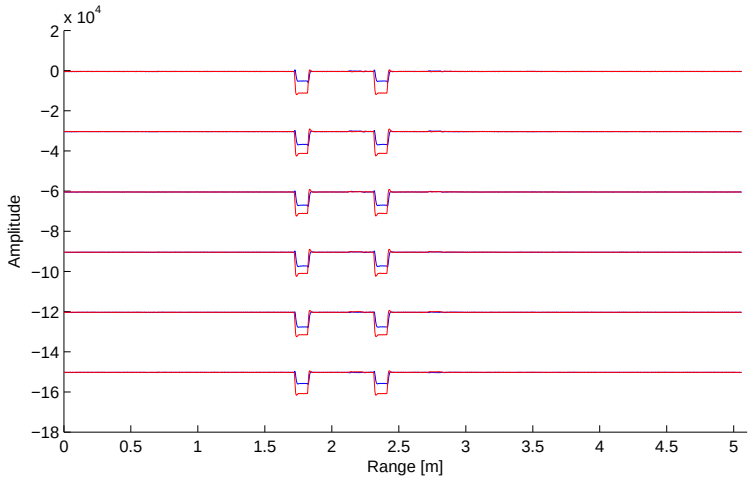

Figure 4.15: Pulses received by a six channel, 300 $[kHz]$ transducer located 3.4 $[m]$ away from the signal source. A single channel, 300 $[kHz]$ transducer is configured to generate two 40 carrier cycle pulse envelope, which are separated by 200 carrier cycles, and for a range of 5 $[m]$. The received signals are displayed in terms of their in-phase (blue) and quadrature (red) components. The y-axis represents the DAB's digital number corresponding to the signal amplitude and the x-axis is range in meters. Each channel is offset by 30000.

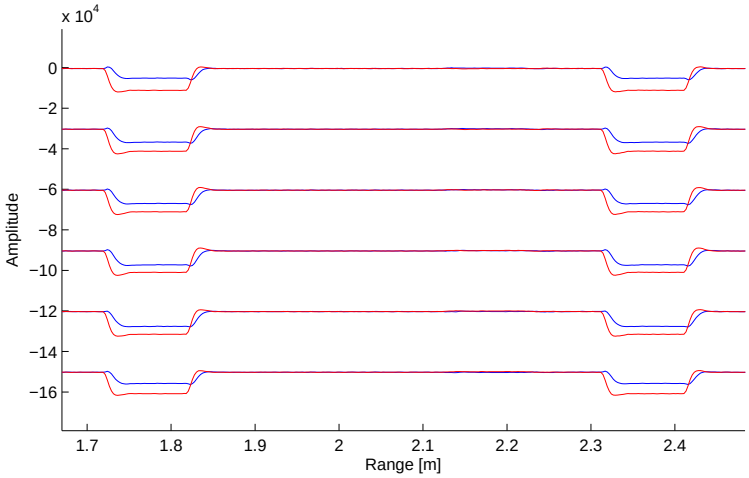

Figure 4.16: Magnified view of the pulses received by a six channel, 300 $[kHz]$ transducer located 3.4 $[m]$ away from the signal source. The sonar is operating in multi-pulse mode.

The sonar was then configured for monostatic operation, as shown in Figure 4.17. The transducer was oriented upright and perpendicular to the surface, and at an angle to the side-wall of the test tank. In this way, backscatter was received from the 4 $[m]$ side-wall of the tank, while reflections due to the surface and reverberation were minimized. The backscatter received from the tank's side-wall was analyzed and compared to the old sonar, in order to verify the degree of coherency between consecutive ping cycles of the new timing control subsystem. The side-wall of the tank is smooth and reflective, therefore the backscatter should exhibit a high coherent component as compared to its diffuse component.

Figure 4.18 shows the received signal decomposed into to its coherent and diffuse components, as described in [29], and averaged over 100 ping cycles. From Figure 4.18, the coherent component, red plot, starts at approximately 85 $[dB\,re:\ ADC\,quantization\,units]$, due to internal reflections when the pulse is initially transmitted. It then rapidly decreases to approximately 20 $[dB\,re:\ ADC\,quantization\,units]$, during the propagation time of the pulse, and before any backscatter is received. A dramatic increase in the coherent component's amplitude occurs when the system starts to receive backscatter from the tank's side-wall, and this amplitude remains relatively constant over the length of the side-wall. Any received signal after 4 $[m]$ is mainly due to reverberations in the tank, and results in the steady decrease in the coherent component's amplitude.

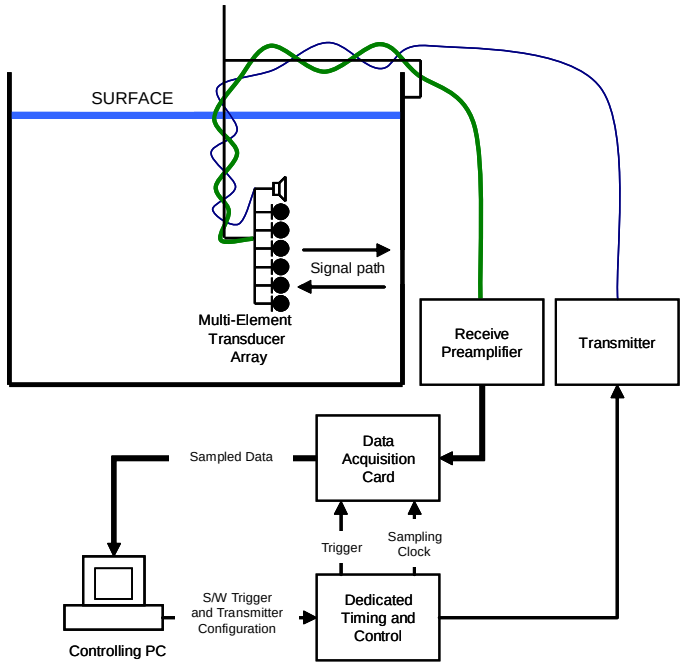

Figure 4.17: Sonar system configured for monostatic operation. The transducer is oriented upright and perpendicular to the surface, and at an angle to the side-wall of the test tank.

The diffuse component, blue plot, represents the noise component of the signal, and maintains an amplitude of approximately $40\,[dB\,re:\,ADC\,quantization\,units]$ level.

The resulting coherent-to-diffuse ratio (CDR), green plot, is approximately $40\,[dB]$, over almost the entire $4\,[m]$ side-wall of the test tank. This closely matches to $40\,[dB]$ found when using the old system. Therefore, it can be said that the new timing control subsystem exhibits at least the same level of coherency between successive ping cycles as the URL sonar (old sonar).

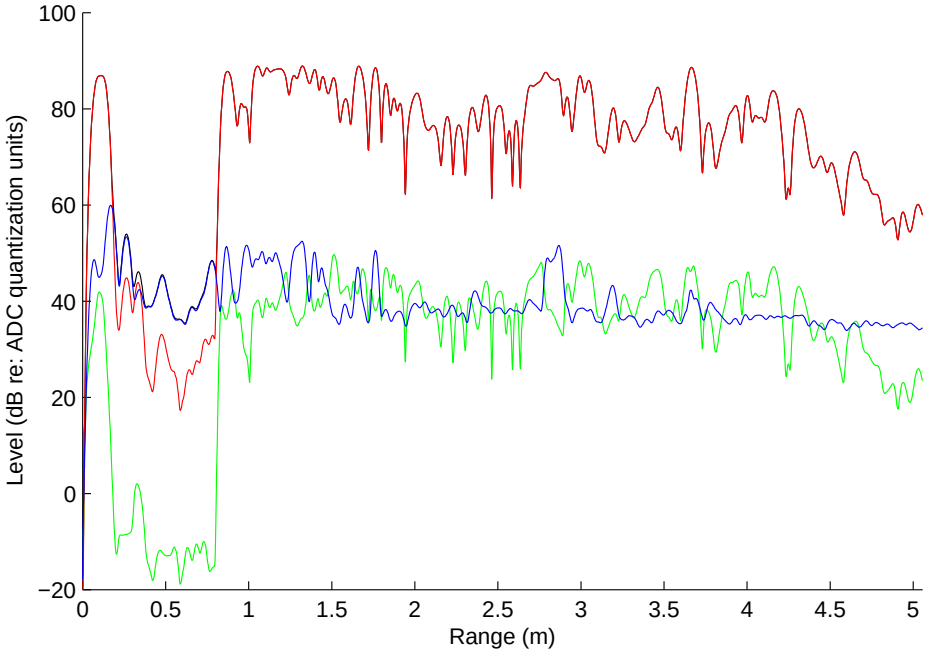

Figure 4.18: Coherent-to-diffuse ratio for signals received from the $4\,[m]$ side-wall of the URL's test tank, using the new timing control subsystem. The coherent component is shown in red, diffuse in blue, and the coherent-to-diffuse ratio in green.

4.2 Performance evaluation of the new preamplifier for the URL sonar system

This section presents experimental data to verify the functionality of the new receive preamplifier designs discussed in Chapter 3.

4.2.1 Verification of frequency response

The measured magnitude versus frequency response plots for the new preamplifier, using the single-ended and diff-amp front-ends, are shown in Figures 4.19 and 4.20. These plots match closely to the simulated data shown in Figures 3.4 and 3.10, of Chapter 3. The $-3\,[dB]$ bandwidth of the both the single-ended and diff-amp front-end plots is approximately $790\,[Hz]$, between $10\,[kHz]$ and $800\,[kHz]$, as expected.

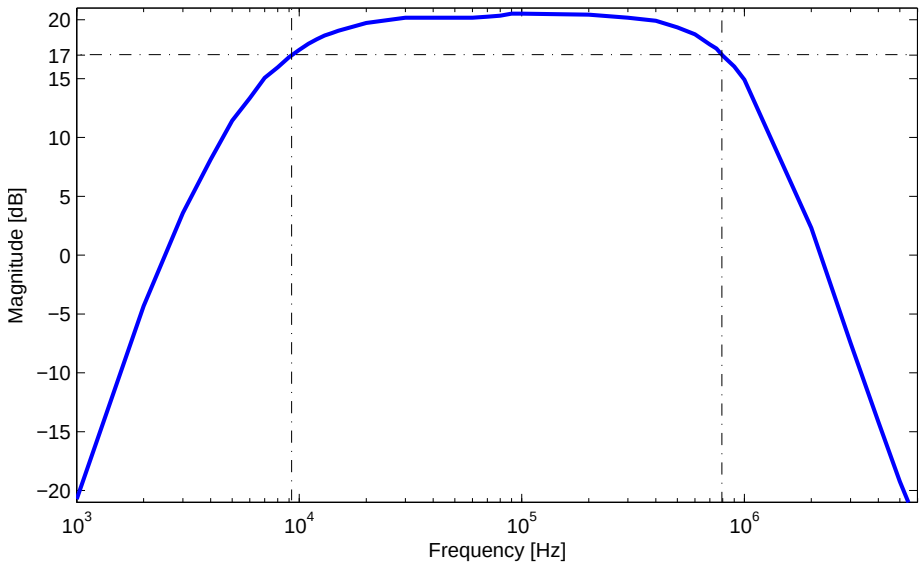

Figure 4.19: Matlab generated plot showing the measured amplitude vs. frequency response of the new single-ended preamplifier. The TVG gain set to 0 $[dB]$ (i.e. an overall preamplifier gain of approximately 20 $[dB]$).

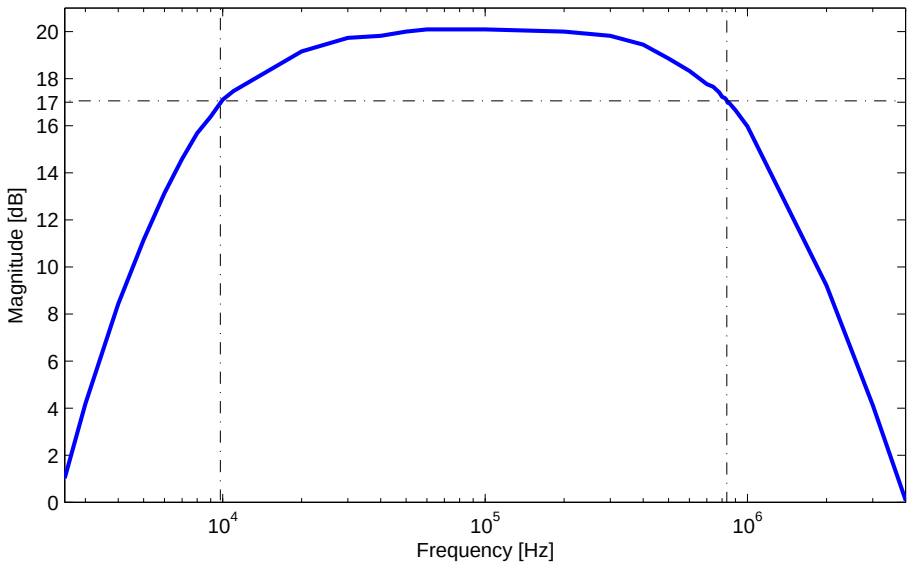

Figure 4.20: Matlab generated plot showing the measured amplitude vs. frequency response of the new preamplifier with diff-amp front-end. The TVG gain set to $0\,[dB]$ (i.e. an overall preamplifier gain of approximately $20\,[dB]$).

4.2.1.1 Frequency response of a transformer-coupled preamplifier

The experiments in this section were designed to investigate the effect inserting a transformer at the front-end of the receive preamplifier had on the received signal over the operating frequency range of the sonar (i.e. the frequency response).

Test equipment set-up The following describes the test equipment set-up required to perform these experiments, in which a test signal is fed through the transducer and a test load, and the resulting output signal, measured across the load, is observed using an oscilloscope (scope).

The function generator is configured to operate in sweep mode, generating a waveform on its sweep output with signal frequency that varies linearly and repeatedly between two set values. This sweep output is connected to the X (CH1) input of the scope.

The RF output of the function generator feeds a test signal in to the test circuit. This output is connected in series with the transducer and the test load.

The output of the test circuit is measured across the test load. This output is connected to the Y (CH3) input of the scope.

By setting the scope to operate in X-Y mode, the output waveform displayed will be an AC sweep of the test circuit, with the x-axis displaying frequency, and the y-axis displaying the amplitude of the output signal.

Transducer admittance The transducer is a frequency-dependent device, which has an admittance that varies with frequency. The shape of the admittance curve with respect to frequency of a typical piezoelectric transducer, similar to those used in the URL, is described in [26]. At low frequencies, the transducer's admittance is small. As frequency increases towards series resonance, the transducer's admittance increases. Admittance reaches a maximum at the transducer's series resonant frequency. Continuing to increase frequency away from series resonance and towards the transducer's anti-resonant frequency, results in a sharp decrease in admittance. At the transducer's anti-resonant frequency, admittance reaches a minimum. Finally, the admittance gradually increases as the frequency increases away from anti-resonance towards other resonant modes of the transducer.

The experiments In the following experiments, the function generator is configured to linear sweep continuously between frequencies $50\,[kHz]$ and $550\,[kHz]$ using a $100\,[mVp]$ sine wave test signal. A single channel transducer which has an operating frequency of

285 [kHz] is used, and the test loads used are a 50 [Ω] resistive load, the single-ended LNA stage of the new preamplifier, and a transformer-coupled LNA stage.

Figure 4.21 shows the first test circuit investigated. The circuit is made up of the source, the transducer and a small, 50 [Ω], resistive load (with respect to the transducer's impedance). In this case, it is expected that the source signal will be loaded down, and

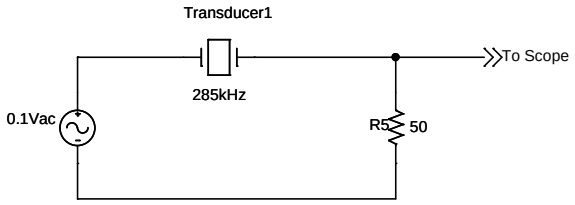

Figure 4.21: Test circuit used to investigate the source loading effects caused by coupling a transducer with a small resistive load.

the output signal, measured across the resistive load, should reflect this. As frequency is increased from 50 [kHz] to 550 [kHz], the transducer's admittance will vary, as described previously. Since the source signal is severely loaded down by the small resistor load, these changes will be directly mimicked by the voltage displayed on the scope.

The output signal of the test circuit described in Figure 4.21 is shown in Figure 4.22. From Figure 4.22, the received signal is observed to be severely loaded down, as compared to the signal source. The maximum output signal is approximately 13 [mV], and occurs at 285 [kHz]. The minimum output signal is approximately 1 [mV], and occurs at 310 [kHz]. As expected, the output signal amplitude varies with frequency, and the output signal is observed to mimic the transducer's admittance curve, described in the previous section. The maximum and minimum voltages displayed on the scope correspond to the maximum and minimum admittances, which occur at the series resonant and anti-resonant frequencies of the transducer. In this case, these are observed to be 285 [kHz] and 310 [kHz], respectively.

Figure 4.23 shows the second test circuit investigated. In this circuit, the 50 [Ω] resistor has been replaced by the single-ended LNA stage of the new preamplifier, described in Chapter 3. The LNA is designed to have a voltage gain of 10 $\left[\frac{V}{V}\right]$, and therefore, the output signal, which is measured across the output of the LNA, will be amplified accordingly. Since the input impedance of the LNA stage is much higher than the transducer's impedance, over the sonar's operating frequency range, it is expected that very little, if any, source signal

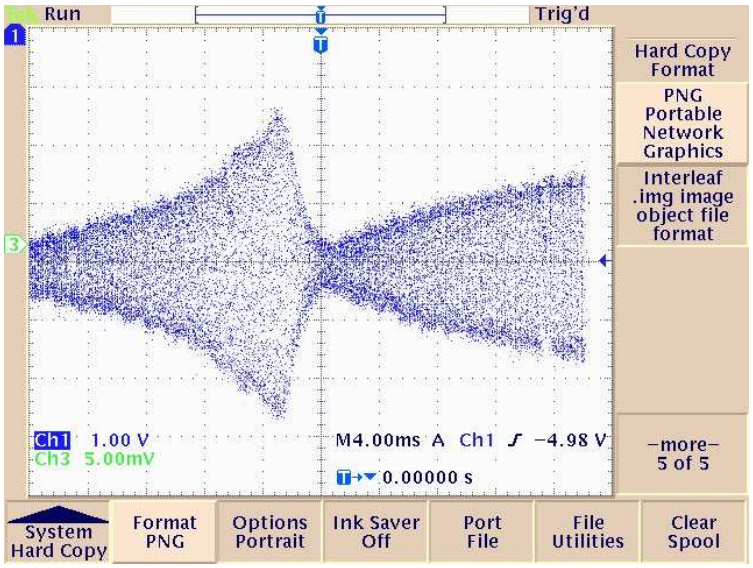

Figure 4.22: AC sweep 50 $[kHz]$ - 550 $[kHz]$ of a 285 $[kHz]$ single channel URL transducer. The scope is set-up such that the x-axis shows 50 $[Hz/div]$ and the y-axis (CH3) shows 5 $[mV/div]$. The input voltage is set to 100 $[mV_p]$.

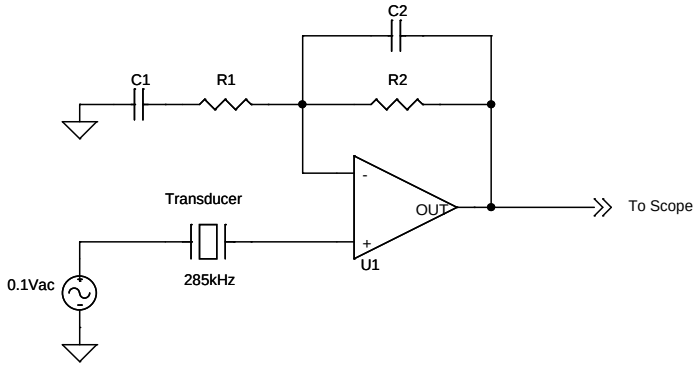

Figure 4.23: Test circuit used to investigate the effects of source loading caused by coupling a transducer with the single-ended LNA stage of the new preamplifier.

loading will occur. Therefore, the measured output voltage, observed on the scope, should be close to the source signal voltage, and remain constant over the entire frequency range that is swept.

Figure 4.24 shows the received signal observed at the output of the LNA stage of the preamplifier. As expected, the output signal voltage is observed to have a maximum am-

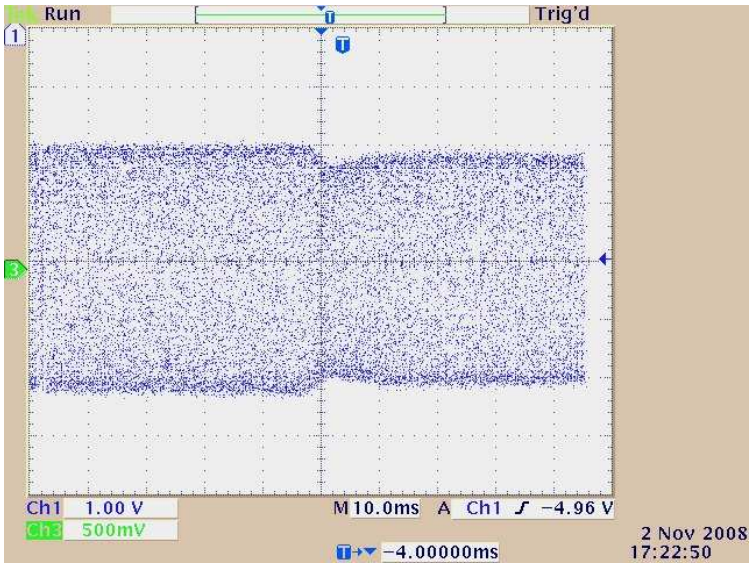

Figure 4.24: AC sweep from 50 $[kHz]$ - 550 $[kHz]$ using the new single-ended preamplifier interfaced to a 285 $[kHz]$ transducer. The scope is set-up such that the x-axis shows 50 $[Hz/div]$ and the y-axis shows 500 $[mV/div]$. The input voltage is set to 100 $[mV_p]$, and measurements are taken at the output of the LNA stage, overall gain is 20 $[dB]$.

plitude of 1 $[Vp]$, which corresponds to ten times the 100 $[mVp]$ source signal. The signal amplitude appears flat over almost the entire 50 $[kHz]$ to 550 $[kHz]$ frequency range, and therefore, the frequency dependent admittance of the transducer does not have much of an effect on the output signal. A small dip in amplitude is observed at approximately 310 $[kHz]$, and is the result of a small loading effect. At this frequency the transducer exhibits very high impedance, which is close to the preamplifier's input impedance, causing slight source loading.

In the final test circuit, shown in Figure 4.25, a transformer is inserted in between the transducer and the single-ended LNA stage. The output signal should maintain the voltage

gain observed in the previous circuit. In this case, using an ideal transformer, the output

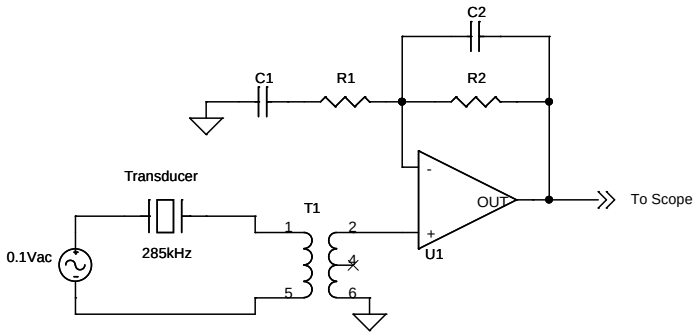

Figure 4.25: Test circuit used to investigate the effects of source loading caused by inserting a transformer in between the transducer and LNA stage of the new preamplifier.

signal, observed on the scope, should be similar to the results shown in Figure 4.24, since the transformer's secondary appears open-circuit. This means that the input impedance of the transformer-coupled LNA stage should be much higher than the transducer's impedance over the entire operating frequency range. However, there are many factors that affect the received signal when a practical transformer is implemented, as previously discussed in Chapter 3. Four transformers were used in the test circuit, shown in Figure 4.25, to investigate their effects on source loading. Some important parameters of these transformers are summarized in Table 4.1, and Figures 4.26 through 4.29 show the output signals, observed on the scope, for the transformer-coupled circuits.

Table 4.1: Some important transformer specifications.

Man.	Part No.	Z_0 [Ω]	Imp. rat.	$-3[dB]$ BW [MHz]
Mini-Circuits	ADTT1-6	50	1	0.015 - 100
Coilcraft	WB1-1TL	50	1	0.100 - 375
Coilcraft	WB1-6TL	50	1	0.050 - 200
Coilcraft	WB2.5-6TL	50	2.5	0.050 - 125

Figure 4.26 shows the output signal for the Coilcraft $WB1-1TL$ transformer, which has an impedance ratio of one, and $-3\,[dB]$ bandwidth between $100\,[kHz]$ and $375\,[MHz]$, when properly terminated with $50\,[\Omega]$. Under these conditions, the output signal, observed on the

scope, should be close to $0.707\,[V]$ at $100\,[kHz]$, achieve a maximum amplitude of $1\,[V]$, and remain constant over the remaining frequency range. However, the waveform shown in Figure 4.26 does not resemble this, and the effects of loading on the output signal appear throughout the entire frequency range. If the transformer was simply reducing the input resistance between the transducer and the LNA stage, and causing the source signal to be severely loaded down, then the output signal should resemble the small resistive load test circuit, shown in Figure 4.22. However, this does not appear to be the case. An amplitude peak of $0.9\,[V]$ occurs at $250\,[kHz]$, and the amplitude fluctuations that occur over the displayed frequency range, suggest that there are other interactions between the transducer, transformer and LNA stage. The effect of these interactions is observed as signal loading and the appearance of other resonance peaks throughout the entire frequency range.

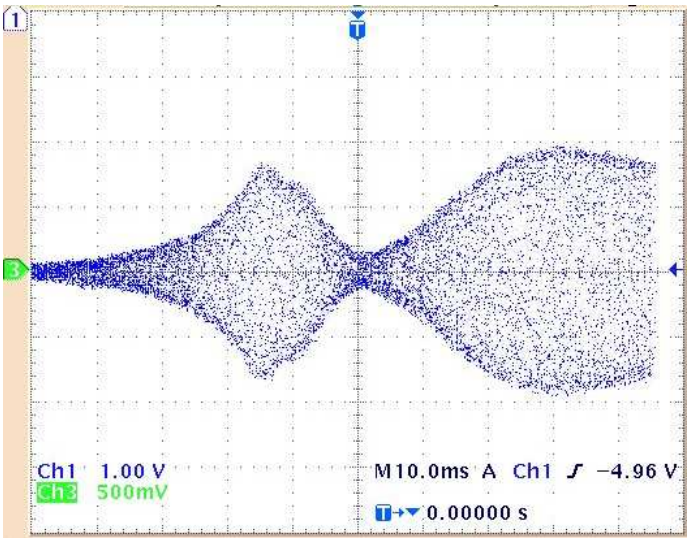

Figure 4.26: AC Sweep showing the frequency response of the new front-end LNA coupled with a WB1-1TL transformer, manufactured by Coilcraft. The preamplifier is connected to a $285\,[kHz]$ transducer.

Figures 4.27 and 4.28 produce similar distorted output waveforms to Figure 4.26. Figure 4.27 appears to be slightly less affected by loading, having an amplitude peak of $1\,[V]$ at $250\,[kHz]$. Figure 4.28 appears to suffer even greater loading, and has an amplitude peak of $0.34\,[V]$ at $285\,[kHz]$.

Figure 4.29 most resembles the response observed in Figure 4.24, but is still distorted.

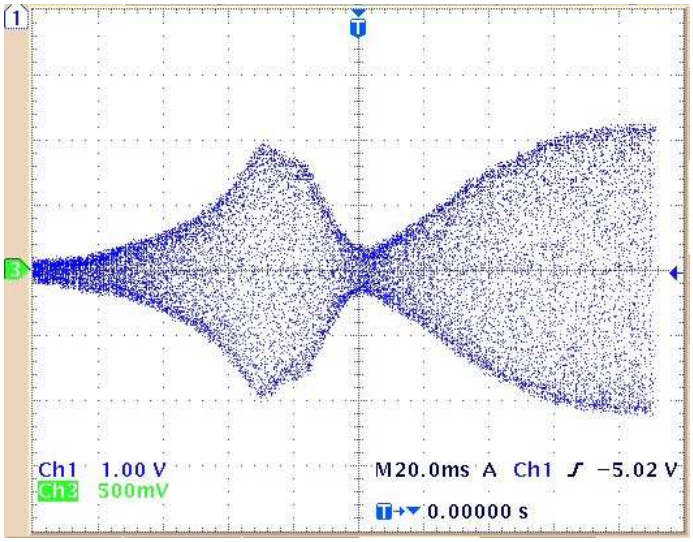

Figure 4.27: AC Sweep showing the frequency response of the new front-end LNA coupled with a WB1-6TL transformer, manufactured by Coilcraft. The preamplifier is connected to a 285 $[kHz]$ transducer.

The maximum output signal is 1 $[V]$ at 150 $[kHz]$, and the signal amplitude fluctuates less over the displayed frequency range. The output signal has an amplitude of approximately 0.8 $[V]$ at the transducers operating frequency, 285 $[kHz]$.

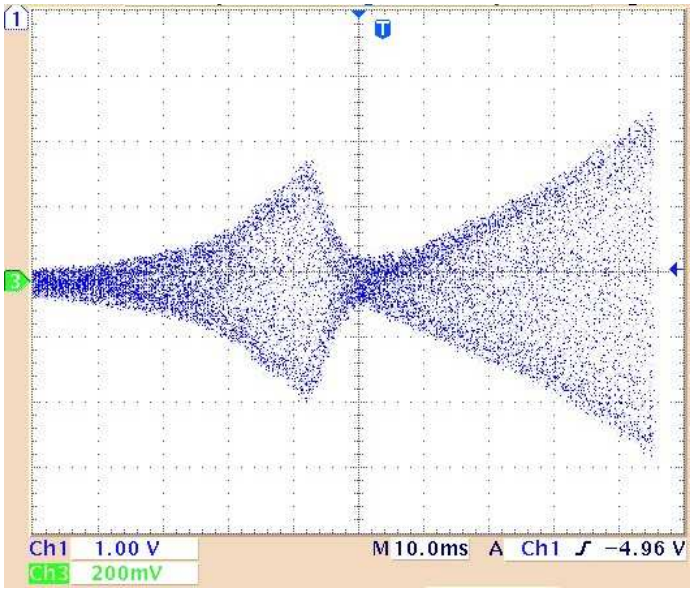

Figure 4.28: AC Sweep showing the frequency response of the new front-end LNA coupled with a WB2.5-6TL transformer, manufactured by Coilcraft. The preamplifier is connected to a 285 $[kHz]$ transducer.

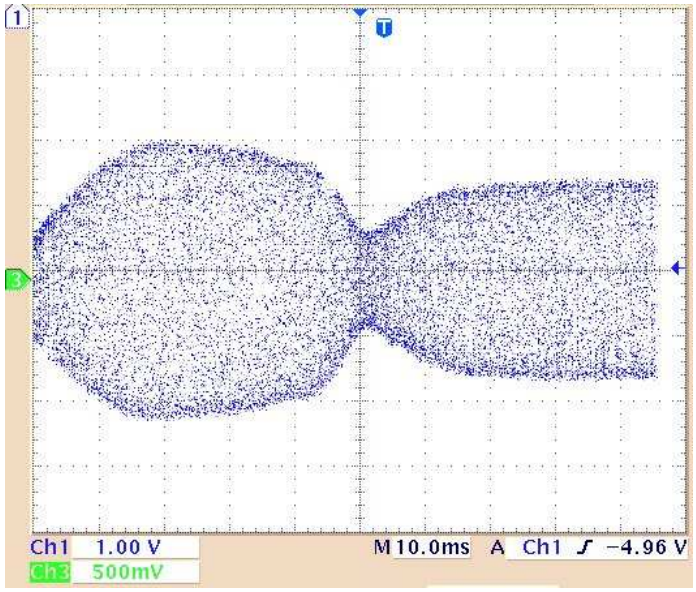

Figure 4.29: AC Sweep showing the frequency response of the new front-end LNA coupled with a ADTT1-6 transformer, manufactured by Mini-Circuits. The preamplifier is connected to a 285 $[kHz]$ transducer.

4.2.2 Verification of noise performance

Figures 4.30 and 4.31 show the NPSD plots generated using the new preamplifier single-ended and diff-amp designs. In order to measure the noise contribution, the inputs of the preamplifier were tied to ground, and the results were measured at the output of the DAB.

Figure 4.30 shows an improvement in broadband noise performance of approximately $9\,[dB]$, as compared to the URL preamplifier, shown in Figure 3.1 of Chapter 3. However,

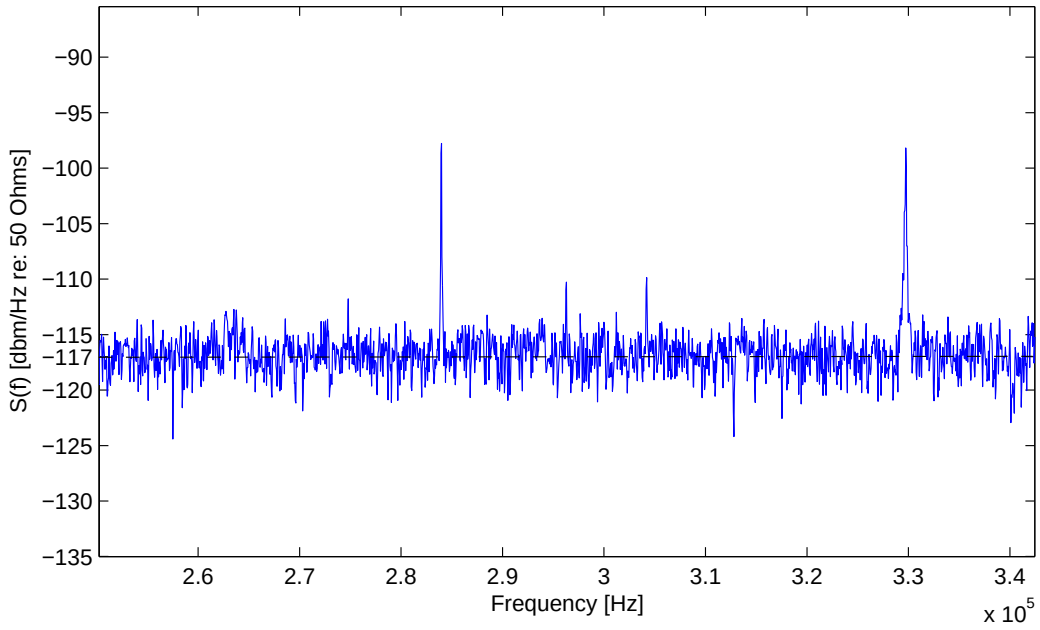

Figure 4.30: Power spectral density showing the output of a single channel of the new preamplifier using the single-ended front-end design. The input of the preamplifier is grounded and the overall preamplifier gain setting of $49\,[dB]$. Where $S(f)$ is the power of the sampled received signal in dBm referred across a $50\,[\Omega]$ load. The average broadband NPSD is approximately $-117\,[\frac{dBm}{Hz}\ re:50\,\Omega]$. Interference lines are visible throughout the pass-band.

interference lines are still visible in the pass-band of the system, and limit the effective bandwidth of the system.

Figure 4.31 has a pass band that is free of interference lines. However, the broadband noise performance has deteriorated significantly. The diff-amp design shows a loss of $14.5\,[dB]$, when compared to the single-ended design, shown in Figure 4.30, and a loss of

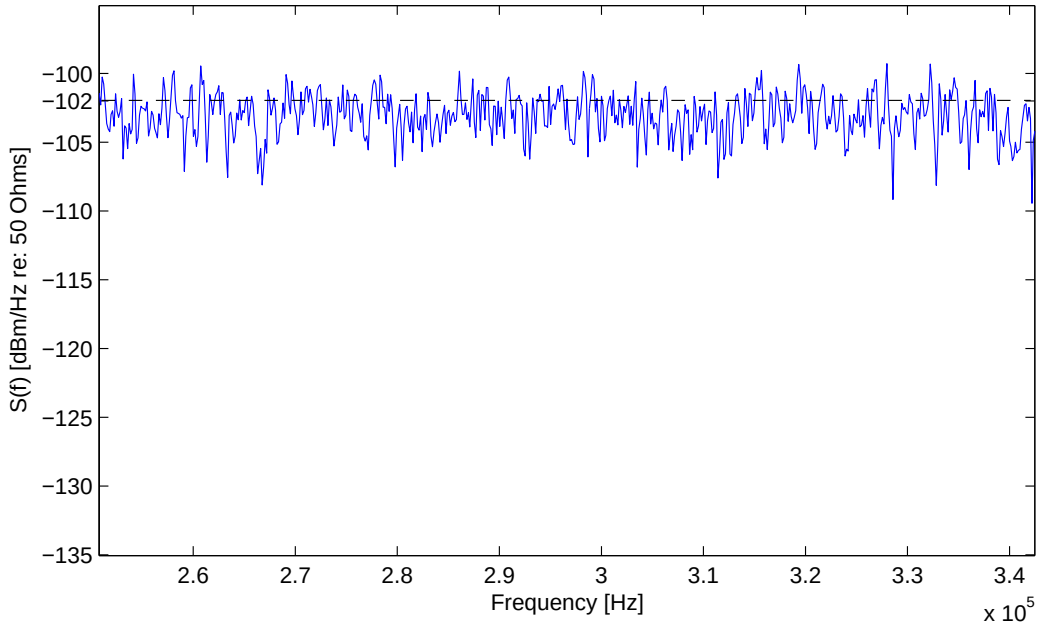

Figure 4.31: Power spectral density showing the output of a single channel of the new preamplifier using the diff-amp front-end design. The input of the preamplifier is grounded and the overall preamplifier gain setting of $49\,[dB]$. Where $S(f)$ is the power of the sampled receive signal in dBm referred across a $50\,[\Omega]$ load. The average broadband NPSD is approximately $-102\,[\frac{dBm}{Hz}\ re:50\,\Omega]$.

$5.5\,[dB]$, when compared to the old preamplifier, shown in Figure 3.1 of Chapter 3. Therefore, it can only be said that the interference lines have been suppressed by at least $5\,[dB]$, since the interference lines might be masked by the high broadband noise level.

4.3 Concluding remarks relating the measured and simulated performance data for the new subsystems

This chapter presented experimental results to verify the performance of the new timing control and new preamplifier subsystems designed and discussed in Chapters 2 and 3. Functional data for the new timing control system was observed and recorded using an oscilloscope, and shown to agree with the corresponding simulation data generated in Chapter 2. Experimental data, in the form of frequency response and noise analysis plots, were

presented, and confirmed the proper implementation of the preamplifier designs discussed in Chapter 3. Measurements using a transformer-coupled preamplifier were presented in order to investigate the effects of transformer action on the frequency response of the receive system. It was shown that a transformer front-end distorted the frequency response, as suggested in the discussion of Chapter 3.

Overall, the results presented showed that an accurate and precise timing control subsystem, which is capable of performing the complex operations discussed in Chapter 2, is successfully implemented. It is also verified that the single-ended front-end preamplifier design was the best design choice for the URL sonar system, because of its superior broadband noise performance, as compared to the diff-amp design, and our ability to work around the interference spikes, as previously discussed in Chapter 3.

Chapter 5

Conclusion

This thesis described the design, implementation and testing of a research sonar system capable of performing complex applications such as coherent Doppler measurement and synthetic aperture imaging. Specifically, improvements to the timing control subsystem and receive SNR of an existing sonar system were explored and implemented in order to enhance its overall performance and capabilities.

The timing-related shortcomings of the existing system were improved on by implementing an FPGA-based dedicated timing control subsystem, which was designed to generate and maintain the precise timing sequences required during the operating cycle of the sonar.

The SNR at the receive system was improved on by identifying and suppressing noise generated by and entering the system through the receive preamplifier. By utilizing various design techniques, these noise contributions were minimized such that, the preamplifier was no longer the dominant noise source in the receive system.

5.1 Improvements to the existing sonar system

Using an FPGA development board to control the timing operations and user-programmable system clock was shown to significantly increase the speed, precision, and predictability of the sonar system. The new timing control subsystem was shown to be capable of providing a fixed and reliable time interval between successive ping cycles, and achieves ping times of $500\,[ms]$ when operating on targets located at $300\,[m]$ from the sonar, as compared to $1\,[s]$ using the URL sonar system (old system). A new operating mode was added to the timing control subsystem, which allowed the sonar to generate more than one transmit pulse

envelope in a ping cycle. In this mode, the new sonar system is capable of producing more complex transmit waveforms.

It was shown that the practical SNR at the receiver of the sonar could be improved by suppressing the noise generated by and entering the system through the receive preamplifier. The sources of the preamplifier's noise contributions were identified as intrinsic noise sources and extrinsic noise sources. The intrinsic noise sources were generated by the preamplifier and affected the broadband noise level of the system. The extrinsic noise sources were generated by external common-mode disturbances, and entered the system through the transducer/preamplifer interface, resulting in interference lines throughout the power spectrum of the received signal. Component selection was shown to reduce the intrinsic noise contributions of the preamplifier, and resulted in a $9\,[dB]$ improvement in the broadband noise performance of the system.

Two suppression techniques that utilized a differential input front-end on the receive preamplifier were investigated in order to suppress the interference lines observed in the power spectrum of the received signal. Of these techniques, it was shown that the diff-amp approach was the most successful at reducing the interference lines, and thus improving the practical bandwidth of the system. However, this solution had a negative effect on the broadband performance of the system, reducing the noise level by $5.5\,[dB]$, as compared to the URL sonar system. The ability to reduce common-mode interference versus achieving an ultra-low broadband noise level represents a major trade-off that must be considered when choosing between the differential ended and single-ended designs.

In order to investigate the second differential approach, which used transformer action, a novel measurement technique was developed. Using this measurement technique, it was shown that transformers could be useful for narrow-band sonar systems, but were not well-suited to the wide-band systems used in the URL.

Ultimately, a single-ended preamplifier solution was chosen, which did not provide rejection of common-mode signals, but offered superior broadband noise performance, as compared to the diff-amp solution. However, it was suggested that the differential approach was still useful, since the choice between the two depended on the operating environment in which the electronics was used. In an environment where common-mode signals were prevalent and the electronics package could not be easily modified, the differential solution would be the better alternative. While in the stand-alone case, such as in the URL sonar, common-mode rejection requirements were less rigid, and could be controlled and managed

in the field.

Using the single-ended approach meant that the interference lines were still present in the receive signal's power spectrum. Currently, in the field, these interference lines are managed by applying grounding points, using shielding techniques, and slightly shifting the sonar's operating frequency to interference free regions.

The new timing control and receive subsystems were shown to improve on the capabilities and performance of the existing URL sonar system. This work provides incentive for further research into the development of algorithms for Doppler and synthetic aperture processing.

5.2 Recommendations for future work

The speed of the new timing subsystem is limited by the memory and processing power of the controlling PC. As the speed and memory capacity of PCs increase and improve, the overhead time needed to transfer and store data between the DAB and the PC can be reduced, and thus the speed of the new timing control can be improved.

The receive preamplifier implemented in this thesis was specifically designed to be interfaced to a high performance, single-ended DAB, available in the URL. Although it has been shown that excellent broadband noise performance levels can be achieved by using a single-ended receiver design, the system has the drawback of being highly susceptible to the effects of common-mode disturbances, since it provides no common-mode rejection. In order to continue to improve on the robustness and versatility of the system, it is recommended that investigation towards a differential solution is continued in the future with an end goal of implementing a completely differential system. This system will consist of a differential input preamplifier interfaced to a differential DAB. Such a system would be immune to the effects of common-mode interference and DC offset issues, and would prove to be extremely useful when operated in electrically noisy environments, such as in tow-fish and AUVs, which contain other electronic components, sensors and storage devices that are external to the receiver system. Although it was shown in this thesis that implementing a differential front-end seriously degrades the broadband noise performance of the system, the fact that this solution achieved significant reductions in common-mode interference entering the system is encouraging and merits further investigation. Currently, third generation Variable Gain Amplifier ICs (VGAs), such as the AD8332, from Analog Devices Inc., present single chip

multipurpose ultra-low noise solutions that work well with both single-ended and differential ended DABs. Designing a preamplifier around this IC would allow for experiments with differential DABs, while improving the noise performance of the preamplifier by reducing the number of external noise producing components needed for the preamplifier design.

In this thesis, an FPGA development board was shown to be a powerful tool in providing precise timing monitoring and control for a research sonar system. Using other features available on the FPGA to implement essential sonar operating tasks, could be an important step in developing a compact and embedded research sonar system. Such a system would be useful in research and commercial industries because of its enhanced portability.

Appendix A

Timing Control Schematics and Calculations

The contents of this appendix is relevant to Chapter 2. It contains example calculations and schematic diagrams associated with the sonar timing control system.

A.1 Schematic diagram of the FPGA-based timing control

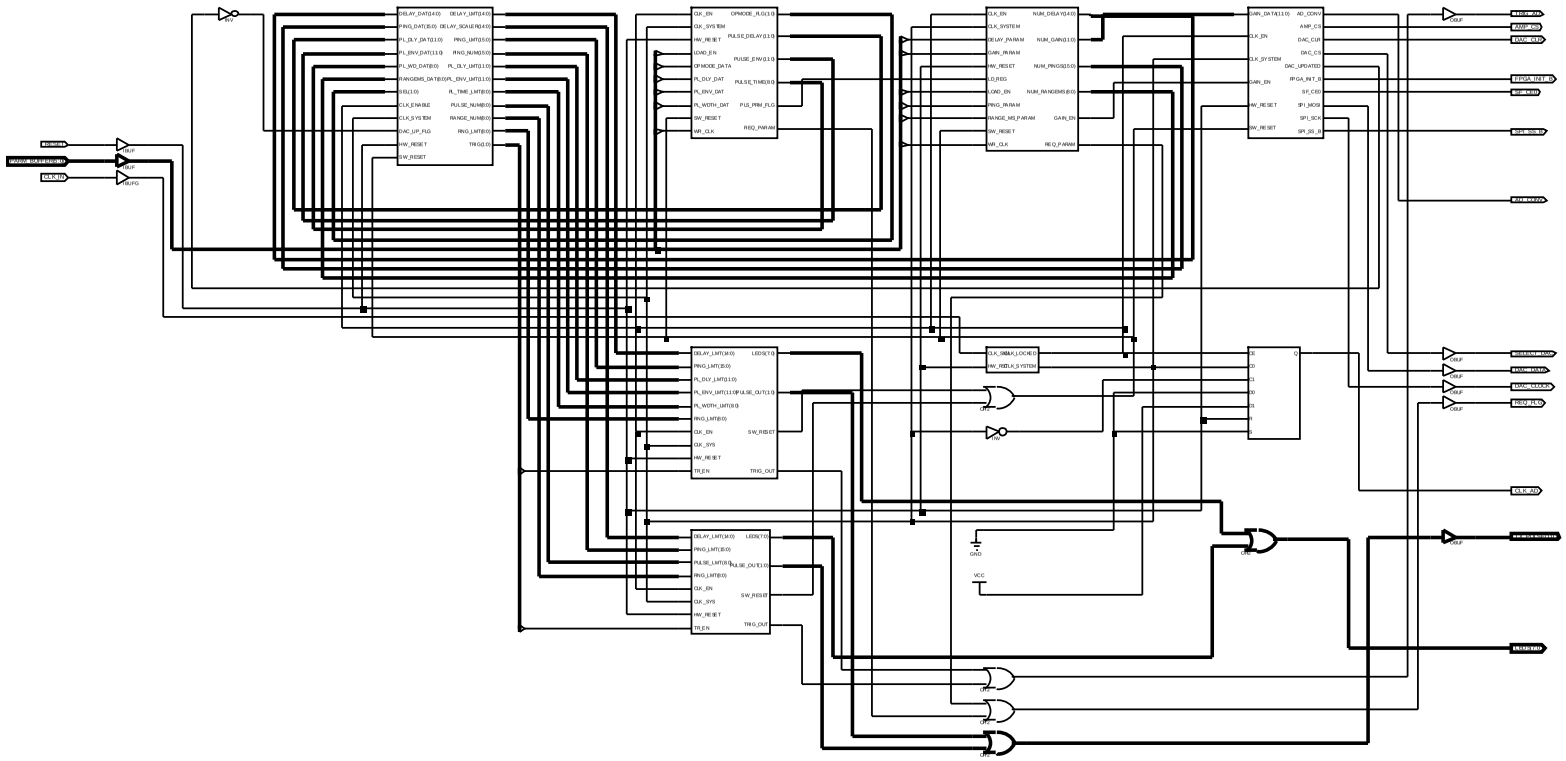

Figure A.1: Complete schematic diagram of FPGA-timing control module used to generate the DAB's sampling clock, the hardware trigger to the DAB, and the transmit pulses.

A.2 Theoretical calculations for the ping rate of new sonar system

In this example the new sonar system is configured for 300 kHz single-pulse mode operation, transmits pulses of 20 carrier cycles for 10 pings at a target five meters from the sonar. The overall ping period can be calculated by applying these parameters to Equation A.1.

$$t_{ping} = t_{pulse} + t_{prop} + \Delta t_{write} + \delta t_{wait} \tag{A.1}$$

Where the time to generate the transmit envelope is:

$$\begin{aligned} t_{pulse} &= \left(\frac{1}{f_{Carrier}}\right) \times pings \\ &= \left(\frac{1}{300[kHz]}\right) \times 20 = 0.066\bar{6}[ms] \end{aligned} \tag{A.2}$$

The acoustic travel time is:

$$\begin{aligned} t_{prop} &= \frac{range[m] \times 2}{sound\,speed[m/s]} \\ &= \frac{5[m] \times 2}{1485[m/s]} \\ &= 6.73[ms] \end{aligned} \tag{A.3}$$

The data transfer time is:

$$\Delta t_{write} = 5[ms] \qquad (user - defined)$$

The start transmission delay is:

$$\begin{aligned} \delta t_{wait} &= 8\,clock\,cycles \times \left(\frac{1}{f_{A/D}}\right) \\ &= 8 \times \left(\frac{1}{38.4[MHz]}\right) \\ &= 208.33[ns] \end{aligned} \tag{A.4}$$

Substituting t_{pulse}, t_{prop}, $\Delta t_{write}\ and\ \delta t_{wait}$ and into Equation A.1

$$\begin{aligned} t_{ping} &= 0.066\bar{3} + 6.73 + 5 + 0.00020833 \\ &= 11.79\,[ms] \approx 12\,[ms] \end{aligned} \tag{A.5}$$

Appendix B

SNR Schematics and Circuit Analysis

The contents of this appendix is relevant to Chapter 3. It contains schematics and circuit analysis associated with the receive preamplifier subsystem designed for the sonar.

B.1 Approximation of the URL sonar system's receive preamplifier noise contribution

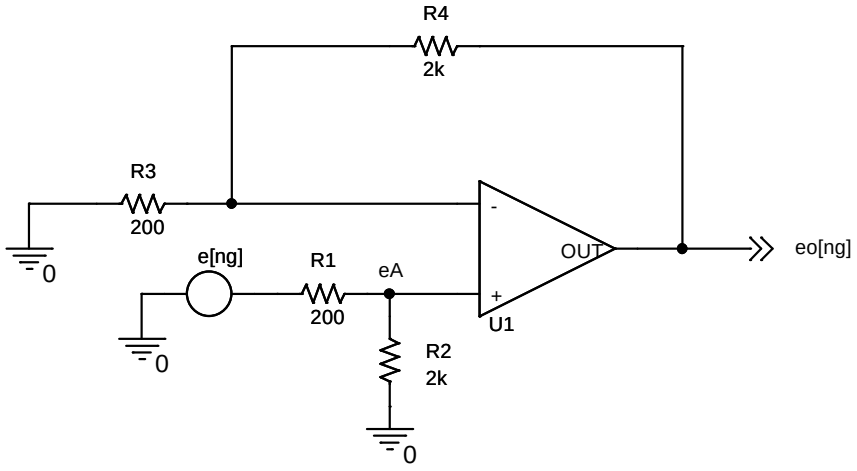

Figure B.1: LNA noise gain model for URL sonar, ignoring bandlimiting capacitors

By definition the noise gain (NG) is the reciprocal of the attenuation from the output of an op-amp to the input of the stage, as modeled in Figure B.1.

By Voltage Divider,

$$e_A = \left(\frac{R_2}{R_1 + R_2}\right) e_{ng} \tag{B.1}$$

For an ideal op-amp, $i_{non-inv} = i_{inv} = 0$. Therefore from Figure B.1, $e_{non-inv} = e_{inv} = e_A$. Applying KCL at *inv* node:

$$0 = e_A \left(\frac{1}{R_3}\right) + \left(e_A - e_{o_{ng}}\right) \frac{1}{R_4} \tag{B.2}$$

$$e_{o_{ng}} \left(\frac{1}{R_4}\right) = \left(\frac{1}{R_3} + \frac{1}{R_4}\right) e_A \tag{B.3}$$

$$e_{o_{ng}} = R_4 \left(\frac{R_3 + R_4}{R_3 R_4}\right) e_A \tag{B.4}$$

$$e_{o_{ng}} = \left(\frac{R_3 + R_4}{R_3}\right) e_A \tag{B.5}$$

Substituting Equation B.1 into Equation B.5,

$$e_{o_{ng}} = \left(\frac{R_3 + R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) e_{ng} \tag{B.6}$$

For $R_1 = R_3$ and $R_2 = R_4$, B.5 becomes,

$$e_{o_{ng}} = \left(\frac{R_2}{R_1}\right) e_{ng} \tag{B.7}$$

Therefore,

$$NG = \frac{e_{o_{ng}}}{e_{ng}} = \frac{R_2}{R_1} \tag{B.8}$$

The complete noise model of the LNA stage of the URL sonar system is shown in Figure B.2. The thermal noise contribution of each component can be found by applying superposition theorem and the results are combined to determine the overall voltage noise spectral density (noise voltage) contribution rated at the input (RTI) or at the output (RTO) of the stage. In this case, the noise voltage contributed by the LNA stage is due to resistive components R_1, R_2, R_3, R_4, and the noise sources of the op-amp e_n, i_n-, i_n+, modeled in Figure B.2.

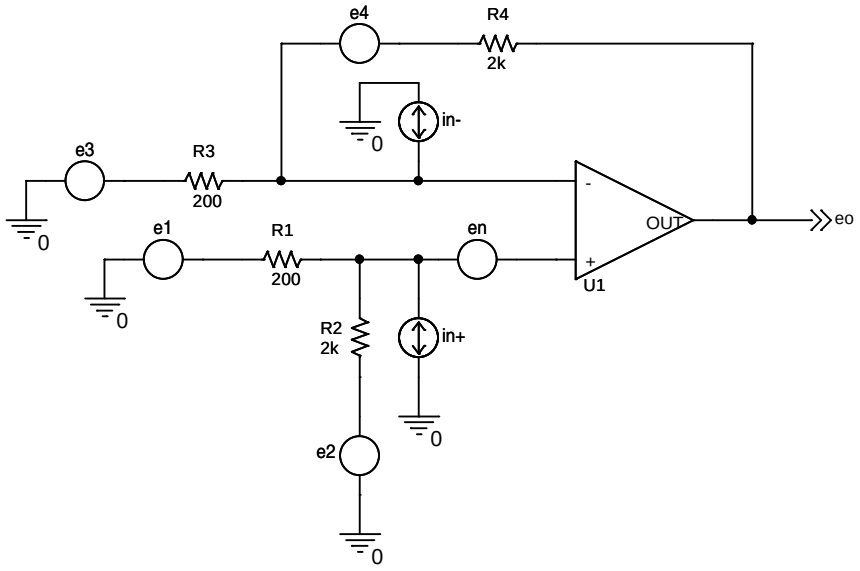

Figure B.2: LNA noise model for the URL sonar system, ignoring bandlimiting capacitors

For an ideal op-amp, $i_{non-inv} = i_{inv} = 0$, and therefore, in this case, $e_{non-inv} = e_{inv} = e_A$. Assuming $e_1 > e_A > e_{o_1} > 0$:

For noise source e_1, due to R_1 (setting all other source to zero).

By voltage divider at the node $e_{non-inv}$:

$$e_A = e_1 \left(\frac{R_2}{R_1 + R_2} \right) \tag{B.9}$$

Applying KCL at node e_{inv}. :

$$0 = e_A \left(\frac{1}{R_3} \right) + (e_A - e_{o_1}) \left(\frac{1}{R_4} \right) \tag{B.10}$$

$$e_{o_1} \left(\frac{1}{R_4} \right) = e_A \left(\frac{1}{R_3} + \frac{1}{R_4} \right) \tag{B.11}$$

$$\begin{aligned} e_{o_1} &= R_4 \left(\frac{R_3 + R_4}{R_3 R_4} \right) e_A \\ &= \left(\frac{R_3 + R_4}{R_3} \right) e_A \end{aligned} \tag{B.12}$$

Substituting B.9 into B.12:

$$e_{o_1} = \left(\frac{R_3 + R_4}{R_3} \right) \left(\frac{R_2}{R_1 + R_2} \right) e_1 \tag{B.13}$$

Therefore, in terms of power spectral density:

$$e_{o_1}^2 = \left(\frac{R_3 + R_4}{R_3} \right)^2 \left(\frac{R_2}{R_1 + R_2} \right)^2 e_1^2 \tag{B.14}$$

In general, the rms noise voltage produced by a resistance in a $1\,[Hz]$ bandwidth is defined as $V_t = \sqrt{4kTR}$, as discussed in [23]. Where k is the Boltzmann constant, T is operating absolute temperature K, R is resistance. Therefore, substituting for e_1 in Equation B.14:

$$e_{o_1}^2 = \left(\frac{R_3 + R_4}{R_3} \right)^2 \left(\frac{R_2}{R_1 + R_2} \right)^2 4kTR_1 \tag{B.15}$$

For noise source e_2, due to R_2 (setting all other source to zero).

By voltage divider at the node $e_{non-inv}$:

$$e_A = e_2 \left(\frac{R_1}{R_1 + R_2} \right) \tag{B.16}$$

By inspection, KCL at node e_{inv} will have the same result as B.12, with $e_{o_1} = e_{o_2}$

$$e_{o_2} = \left(\frac{R_3 + R_4}{R_3} \right) e_A \tag{B.17}$$

Substituting B.16 into B.17:

$$e_{o_2} = \left(\frac{R_3 + R_4}{R_3} \right) \left(\frac{R_1}{R_1 + R_2} \right) e_2 \tag{B.18}$$

Therefore, in terms of power spectral density:

$$e_{o_2}^2 = \left(\frac{R_3 + R_4}{R_3} \right)^2 \left(\frac{R_1}{R_1 + R_2} \right)^2 e_2^2 \tag{B.19}$$

Substituting expression for e_2 into B.19:

$$e_{o_2}^2 = \left(\frac{R_3 + R_4}{R_3} \right)^2 \left(\frac{R_1}{R_1 + R_2} \right)^2 4kTR_2 \tag{B.20}$$

For noise source e_3, due to R_3 (setting all other source to zero). No current through $R_1 \parallel R_2$, therefore $e_A = 0$.

Applying KCL at node e_{inv}. :

$$0 = e_3 \left(\frac{1}{R_3} \right) + e_{o_3} \left(\frac{1}{R_4} \right) \tag{B.21}$$

$$e_{o_3} = -\left(\frac{R_4}{R_3} \right) e_3 \tag{B.22}$$

Therefore, in terms of power spectral density:

$$e_{o_3}^2 = \left(\frac{R_4}{R_3} \right)^2 e_3^2 \tag{B.23}$$

Substituting expression for e_3 into B.23:

$$e_{o_3}^2 = \left(\frac{R_4}{R_3} \right)^2 4kTR_3 \tag{B.24}$$

For noise source e_4, due to R_4 (setting all other source to zero). No current through $R_1 \parallel R_2$, therefore $e_A = 0$. So no voltage drop across R_3 or R_4. Therefore (by inspection):

$$e_{o_4} = e_4 \tag{B.25}$$

Therefore, in terms of power spectral density:

$$e_{o_4}^2 = e_4^2 \tag{B.26}$$

Substituting expression for e_4 into B.26:

$$e_{o_4}^2 = 4kTR_4 \tag{B.27}$$

For op-amp noise voltage source e_n (setting all other source to zero). $e_A = e_n$.

Applying KCL at node e_{inv}. :

$$0 = e_n \left(\frac{1}{R_3}\right) + (e_n - e_{o_n}) \left(\frac{1}{R_4}\right) \tag{B.28}$$

$$e_{o_n} \left(\frac{1}{R_4}\right) = e_n \left(\frac{1}{R_3} + \frac{1}{R_4}\right) \tag{B.29}$$

$$e_{o_n} = \left(\frac{R_3 + R_4}{R_3}\right) e_n \tag{B.30}$$

Therefore, in terms of power spectral density:

$$e_{o_n}^2 = \left(\frac{R_3 + R_4}{R_3}\right)^2 e_n^2 \tag{B.31}$$

For intrinsic noise source i_n^+ (setting all other source to zero). Voltage due to current source i_n^+ at the node $e_{non-inv}$:

$$e_A = i_n^+ (R_1 \parallel R_2) \tag{B.32}$$

$$= i_n^+ \left(\frac{R_1 R_2}{R_1 + R_2}\right) \tag{B.33}$$

Applying KCL at node e_{inv}. :

$$0 = e_A \left(\frac{1}{R_3}\right) + \left(e_A - e_{o_{i^+}}\right) \left(\frac{1}{R_4}\right) \tag{B.34}$$

$$e_{o_{i^+}} \left(\frac{1}{R_4}\right) = e_A \left(\frac{1}{R_3} + \frac{1}{R_4}\right) \tag{B.35}$$

$$\begin{aligned} e_{o_{i^+}} &= R_4 \left(\frac{R_3 + R_4}{R_3 R_4}\right) e_A \\ &= \left(\frac{R_3 + R_4}{R_3}\right) e_A \end{aligned} \tag{B.36}$$

Substituting B.33 into B.36:

$$e_{o_i^+} = \left(\frac{R_3 + R_4}{R_3}\right) \left(\frac{R_1 R_2}{R_1 + R_2}\right) i_n^+ \tag{B.37}$$

Therefore, in terms of power spectral density:

$$e_{o_i^+}^2 = \left(\frac{R_3 + R_4}{R_3}\right)^2 \left(\frac{R_1 R_2}{R_1 + R_2}\right)^2 \left(i_n^+\right)^2 \tag{B.38}$$

For intrinsic noise source i_n^- (setting all other source to zero). No current through R_3, therefore:

$$e_{o_i^-} = i_n^- R_4 \tag{B.39}$$

Therefore, in terms of power spectral density:

$$e_{o_i^-}^2 = \left(i_n^-\right)^2 R_4^2 \tag{B.40}$$

Therefore, by combining Equations B.15, B.20, B.24, B.27, B.31, B.38, and B.40, the overall noise power (RTO) is:

$$\begin{aligned} e_o^2\,(RTO) = &\left(\frac{R_3 + R_4}{R_3}\right)^2 \left(\frac{R_2}{R_1 + R_2}\right)^2 4kTR_1 + \left(\frac{R_3 + R_4}{R_3}\right)^2 \left(\frac{R_1}{R_1 + R_2}\right)^2 4kTR_2 \\ &+ \left(\frac{R_4}{R_3}\right)^2 4kTR_3 + 4kTR_4 + \left(\frac{R_3 + R_4}{R_3}\right)^2 e_n^2 \\ &+ \left(\frac{R_3 + R_4}{R_3}\right)^2 \left(\frac{R_1 R_2}{R_1 + R_2}\right)^2 \left(i_n^+\right)^2 + \left(i_n^-\right)^2 R_4^2 \end{aligned} \tag{B.41}$$

For $R_1 = R_3 \, and \, R_2 = R_4$, as in the URL sonar system, Equation B.41 simplifies to:

$$\begin{aligned} e_o^2\,(RTO) &= \left(\frac{R_2}{R_1}\right)^2 4kTR_1 + 4kTR_2 + \left(\frac{R_2}{R_1}\right)^2 4kTR_1 + 4kTR_2 \\ &+ \left(\frac{R_1+R_2}{R_1}\right)^2 e_n^2 + \left(i_n^+\right)^2 R_2^2 + \left(i_n^-\right)^2 R_2^2 \\ &= \left(\frac{R_2}{R_1}\right)^2 8kTR_1 + 8kTR_2 + \left(1+\frac{R_2}{R_1}\right)^2 e_n^2 + 2\,(i_n)^2\,R_2^2 \end{aligned} \tag{B.42}$$

In terms of NG found in Equation B.8

$$\begin{aligned} e_o^2\,(RTO) &= 8kTR_2\,(1+NG) + e_n^2\,(1+NG)^2 \\ &+ 2\,(i_n)^2\,(NG)^2\,R_1^2 \end{aligned} \tag{B.43}$$

An expression for the noise power spectral density (NPSD) RTI is found by dividing Equation B.43 by the NG^2:

$$\begin{aligned} e_o^2\,(RTI) &= 8kTR_2\left(\frac{1+NG}{NG^2}\right) + e_n^2\left(1+\frac{1}{NG}\right)^2 \\ &+ 2\,(i_n)^2\,R_1^2 \end{aligned} \tag{B.44}$$

Therefore, substituting $R_1 = 200\,\Omega$, $R_2 = 2000\,\Omega$, $e_n = 0.90\,\left[\frac{nV}{\sqrt{Hz}}\right]$, $i_n = 2.0\,\left[\frac{pA}{\sqrt{Hz}}\right]$, $NG = 10$, $k = 1.38 \times 10^{-23}$, $and \, T = 300\,K$ into Equation B.43 and B.44:

$$\begin{aligned} e_o^2\,(RTO) &= 728.64 \times 10^{-18} + 98.01 \times 10^{-18} + 32.0 \times 10^{-18} \\ &= 858.65 \times 10^{-18} \end{aligned} \tag{B.45}$$

$$\begin{aligned} e_o^2\,(RTI) &= 7.2864 \times 10^{-18} + 0.9801 \times 10^{-18} + 0.32 \times 10^{-18} \\ &= 8.5865 \times 10^{-18}\,\left[\frac{V^2}{Hz}\right] \end{aligned} \tag{B.46}$$

By taking the square root of both sides, expressions for the noise voltage RTO and RTI are found:

$$e_o\,(RTO) = 29.30\,\left[\frac{nV}{\sqrt{Hz}}\right] \tag{B.47}$$

$$e_o\,(RTI) = 2.930\,\left[\frac{nV}{\sqrt{Hz}}\right] \tag{B.48}$$

There are two remaining stages in the preamplifier that the signal sees before it reaches the data acquisition board (DAB). The TVG stage, which varies between $0 - 40\,[dB]$, in this case it is set to a constant gain of $29\,[dB]$, which corresponds to $28.18\,\left[\frac{V}{V}\right]$. The output buffer stage of the preamplifier has a gain of $0\,[dB]$, or $1\,\left[\frac{V}{V}\right]$. Therefore, using Equation B.47, the noise voltage at the input of the DAB, which is amplified by the remaining stage gains is:

$$\begin{aligned} e_{AMP} &= 29.30\,\left[\frac{nV}{\sqrt{Hz}}\right] \times 28.18 \times 1 \\ &= 825.67\,\left[\frac{nV}{\sqrt{Hz}}\right] \end{aligned} \tag{B.49}$$

The available noise power in a conductor is given by $N_t = kT\Delta f$ [15]. At $300\,[K]$ (the typical operating temperature of a PC board), the noise power in a $1\,[Hz]$ bandwidth is:

$$\begin{aligned} Noise\,Power|_{dBm} &= 10log\left(\frac{kT\Delta f}{1\,mW}\right) \\ &\approx -174\,[dBm] \end{aligned} \tag{B.50}$$

This represents the minimum noise level that is practically achieveable by a system operating at $300\,[K]$.

The noise power in a $1\,[Hz]$ bandwidth across $50\,\Omega$ is given by:

$$P_N = \frac{e_o^2}{50\,\Omega} \tag{B.51}$$

In dBm, this becomes:

$$P_N|_{dBm\,re:\,50\,\Omega} = 10\log\left(\frac{e_o^2}{(50\,\Omega)(1mW)}\right) \tag{B.52}$$

In general, per Hertz, the NPSD at the output of the preamplifier in $[dBm/Hz]$, and referred across a $50\,\Omega$ load is:

$$\begin{aligned} P_N|_{dBm/Hz\,re:\,50\,\Omega} &= 10\log\left(\frac{825.67n^2}{(50\,\Omega)(1mW)}\right) \\ &= -108.65\,\left[\frac{dBm}{Hz}\,re:\,50\,\Omega\right] \end{aligned} \tag{B.53}$$

B.1.1 Verification of noise calculations through circuit simulation using Pspice

Figure B.3 shows the simulated noise voltage for the front-end LNA of the URL sonar system. The noise voltage in both plots, increases at frequencies below $1\,[kHz]$, due to the influence of $\frac{1}{f}$ noise. At frequencies above $1\,[kHz]$, broadband noise dominates, and the noise voltages are $2.933\,\frac{nV}{\sqrt{Hz}}\,(RTI)$ and $29.33\,\frac{nV}{\sqrt{Hz}}\,(RTO)$. These values confirm the results calculated in Equations B.47 and B.48. The noise spectral density at the output has a $-3\,[dB]$ cutoff frequency at approximately $970\,[kHz]$ due to the low-pass filter formed between the bandlimiting feedback capacitor and the feedback resistor in the circuit.

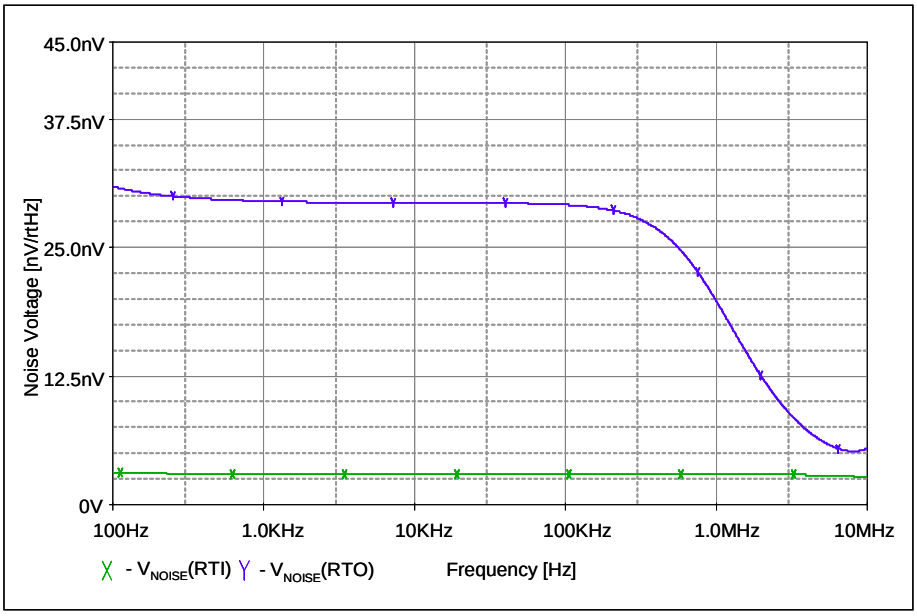

Figure B.3: Simulated noise spectral density (noise voltage) response of front-end receive LNA of URL sonar system RTI and RTO, including bandlimiting capacitors. Where $V_{NOISE}[RTO]$ is the noise voltage at the noise voltage at the rated at the output of the LNA, and $V_{NOISE}[RTI]$ is the noise voltage rated at the input of the LNA.

Figure B.4 shows the simulated noise spectral density referred to the output of the old preamplifier. The $-3\,[dB]$ cutoff frequencies occur at approximately $33\,[kHz]$ and $700\,[kHz]$, due to the filtering capacitors in the circuit, and the power spectral density peaks at approximately $-109\,\left[\frac{dBm}{Hz}\,re:\,50\,\Omega\right]$ over the operating frequency of the sonar, as expected

from Equation B.53.

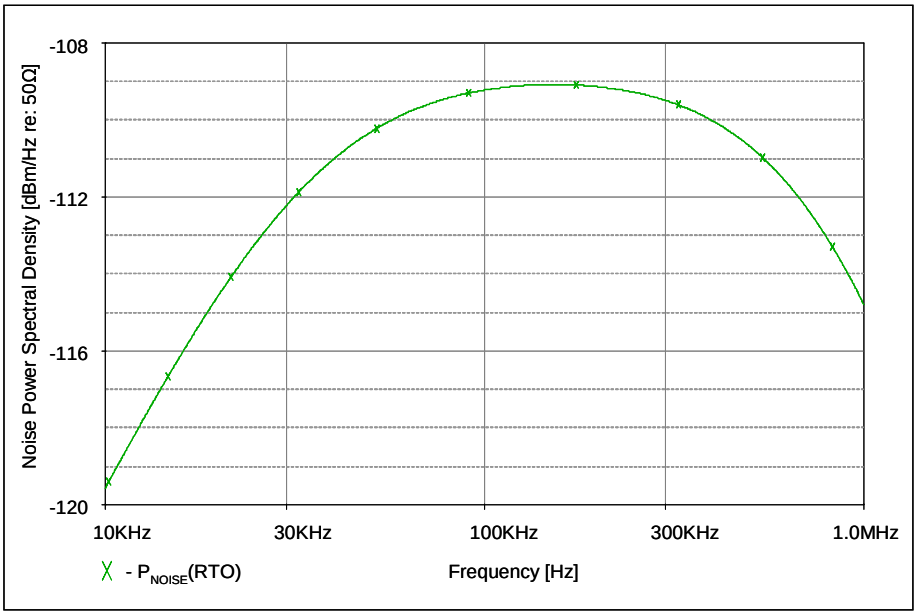

Figure B.4: Simulated NPSD at the output of the old URL preamplifier, including bandlimiting capacitors. The overall gain of the preamplifier is 49 $[dB]$.

B.2 Offset voltage calculations for the front-end gain stage of the new preamplifier

Small offset voltages generated in the first stages of a multistage circuit can be amplified by subsequent stages and produce significant voltage offsets at the output of a system. This large DC offset reduces the maximum voltage range that the signal can swing undistorted, and limits the performance of the system.

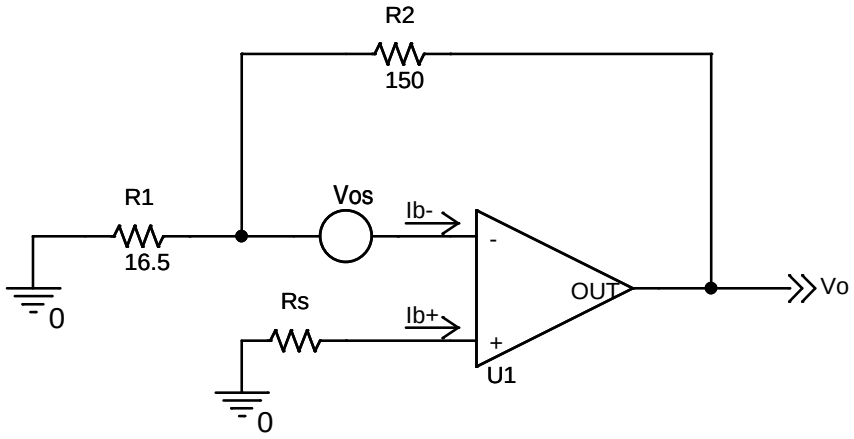

Figure B.5: Offset Voltage circuit model with source connected.

Figure B.5 shows the model used to calculate the DC offset voltage generated by the first stage of the new preamplifier.

The noise gain (NG) for this circuit, defined from the non-interverting input is:

$$NG = 1 + \frac{R_2}{R_1} \tag{B.54}$$

Using superposition theorem:

V_{o1} due V_{os}, with all other sources zeroed. Using KCL at node R_1, R_2, V_{os}:

$$0 = \frac{V_{os}}{R_1} + \frac{V_{os} - V_{o1}}{R_2} \tag{B.55}$$

$$\begin{aligned} V_{o1} &= V_{os}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) R_2 \\ &= V_{os}\left(1 + \frac{R_2}{R_1}\right) \end{aligned} \tag{B.56}$$

V_{o2} due I_b^+, with all other sources zeroed. Using KCL at node R_1, R_2, V_{inv}:

$$0 = \frac{V_{inv}}{R_1} + \frac{V_o s - V_{o2}}{R_2} \tag{B.57}$$

$$V_{o2} = V_{inv}\left(1 + \frac{R_2}{R_1}\right) \tag{B.58}$$

Substituting $V_{inv} = I_b^+ R_s$ into Equation B.58:

$$V_{o2} = \left(I_b^+ R_s\right)\left(1 + \frac{R_2}{R_1}\right) \tag{B.59}$$

V_{o3} due I_b^-, with all other sources zeroed. Virtual ground at node R_1, R_2:

$$V_{o3} = -I_b^- R_2 \tag{B.60}$$

Combining Equations B.56, B.59,and B.60:

$$V_o[RTO] = V_{os}\left(1 + \frac{R_2}{R_1}\right) + \left(I_b^+ R_s\right)\left(1 + \frac{R_2}{R_1}\right) - I_b^- \left(R_1 \parallel R_2\right) \tag{B.61}$$

Dividing B.61 by NG:

$$V_o[RTI] = V_{os} + I_b^+ R_s - I_b^- \left(R_1 \parallel R_2\right) \tag{B.62}$$

If $I_b^+ = I_b^-$ and $R_s = R_1 \parallel R_2$ then $V_o = V_{os}$ (datasheet value [13]). However, with no termination resistor, R_s depends on the transducer. For example, if $R_s = 200\,\Omega$, $V_{os}[max] = 40\,\mu V$ and $I_b = 0.9\,\mu A$, which is high because the op-amp provides no internal compensation in order to maintain its low noise characteristics:

$$\begin{aligned} V_o[RTI] &= 40\,\mu + (0.9\,\mu)\,200 - (0.9\,\mu)\,(14.87\,\Omega) \\ &= 40\ + 180\,\mu - 13.38\,\mu \\ &= 206.6\,\mu V \end{aligned} \tag{B.63}$$

B.3 Schematic diagrams for preamplifier of the new sonar system

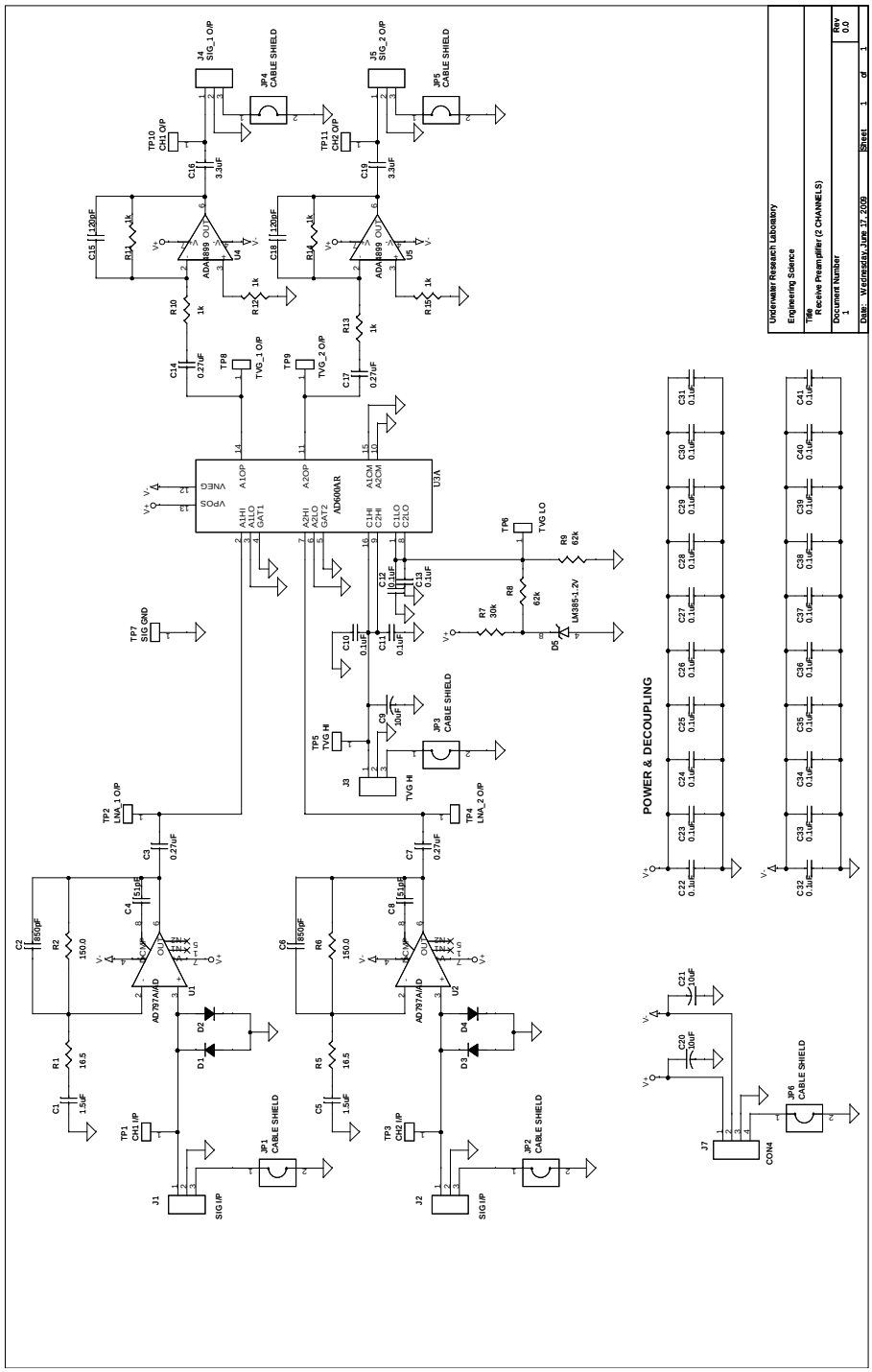

Figure B.6: Complete schematic diagrams of new preamplifier with single-ended front-end

B.4 Approximation of the new preamplifier's noise contribution

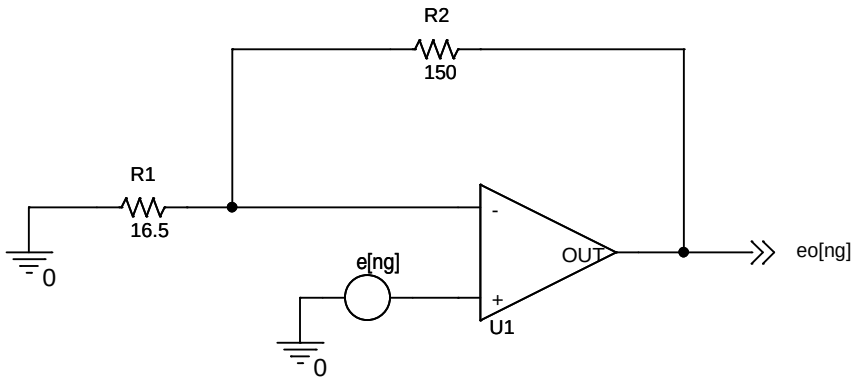

Figure B.7: Noise gain model for new LNA stage of the new preamplifier, ignoring bandlimiting capacitors

The noise gain (NG) of the new LNA stage of the preamplifier can be found from the model shown in Figure B.7.

For an ideal op-amp, $i_{non-inv} = i_{inv} = 0$. Therefore from Figure B.7, $e_{non-inv} = e_{inv} = e_{ng}$. Applying KCL at node e_{ng}:

$$0 = e_{ng}\left(\frac{1}{R_1}\right) + \left(e_{ng} - e_{o_{ng}}\right)\frac{1}{R_2} \tag{B.64}$$

$$e_{o_{ng}}\left(\frac{1}{R_2}\right) = e_{ng}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{B.65}$$

$$\frac{e_{o_{ng}}}{e_{ng}} = R_2\left(\frac{R_1 + R_2}{R_1 R_2}\right) \tag{B.66}$$

$$NG = 1 + \frac{R_2}{R_1} \tag{B.67}$$

The complete noise model of the new LNA stage is shown in Figure B.8. The overall voltage noise spectral density (noise voltage) is found using superposition. In this case, the noise contributors are resistive components R_1, R_2 and the noise sources of the op-amp e_n, i_n-, i_n+.

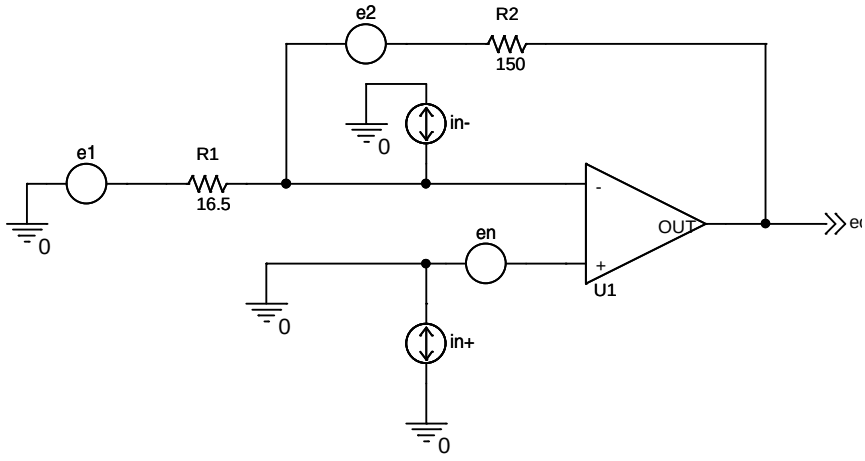

Figure B.8: Noise model of front-end LNA stage for new preamplifier, ignoring bandlimiting capacitors

For an ideal op-amp, $i_{non-inv} = i_{inv} = 0$, and therefore, in this case, $e_{non-inv} = e_{inv} = e_A$. Assuming $e_1 > e_A > e_{o_1} > 0$:

For noise source e_1, due to R_1 (setting all other source to zero). $e_A = 0$

Applying KCL at node e_{inv}. :

$$0 = e_1 \left(\frac{1}{R_1}\right) + e_{o_1} \left(\frac{1}{R_2}\right) \tag{B.68}$$

$$e_{o_1} \left(\frac{1}{R_2}\right) = -e_1 \left(\frac{1}{R_1}\right) \tag{B.69}$$

$$e_{o_1} = -\left(\frac{R_2}{R_1}\right) e_1 \tag{B.70}$$

Therefore, in terms of power spectral density:

$$e_{o_1}^2 = \left(\frac{R_2}{R_1}\right)^2 e_1^2 \tag{B.71}$$

Substituting the noise voltage expression for e_1 in Equation B.71:

$$e_{o_1}^2 = \left(\frac{R_2}{R_1}\right)^2 4kTR_1 \tag{B.72}$$

For noise source e_2, due to R_2 (setting all other source to zero). $e_A = 0$, so no voltage drop across R_2. Therefore (by inspection):

$$e_{o_2} = e_2 \tag{B.73}$$

Therefore, in terms of power spectral density:

$$e_{o_2}^2 = e_2^2 \tag{B.74}$$

Substituting expression for e_2 into B.74:

$$e_{o_2}^2 = 4kTR_2 \tag{B.75}$$

For op-amp noise voltage source e_n (setting all other source to zero). $e_A = e_n$.

Applying KCL at node e_{inv}. :

$$0 = e_n \left(\frac{1}{R_1}\right) + (e_n - e_{o_n}) \left(\frac{1}{R_2}\right) \tag{B.76}$$

$$e_{o_n} \left(\frac{1}{R_2}\right) = e_n \left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{B.77}$$

$$e_{o_n} = \left(1 + \frac{R_2}{R_1}\right) e_n \tag{B.78}$$

Therefore, in terms of power spectral density:

$$e_{o_n}^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 \tag{B.79}$$

For intrinsic noise source i_n^+ (setting all other source to zero). Voltage due to current source i_n^+ at the node $e_{non-inv} = 0$

$$e_{o_{i^+}} = 0 \tag{B.80}$$

For intrinsic noise source i_n^- (setting all other source to zero). No current through R_1, therefore:

$$e_{o_i^-} = i_n^- R_2 \tag{B.81}$$

Therefore, in terms of power spectral density:

$$e^2_{o^-_i} = \left(i^-_n R_2\right)^2 \tag{B.82}$$

Therefore, by combining Equations B.72, B.75, B.79, B.80, and B.82, the overall NPSD (RTO) is:

$$\begin{aligned} e^2_o\left(RTO\right) &= \left(\frac{R_2}{R_1}\right)^2 4kTR_1 + 4kTR_2 + \left(1+\frac{R_2}{R_1}\right)^2 e^2_n + 0 + \left(i^-_n\right) R_2^2 \\ &= 4kTR_2\left(1+\frac{R_2}{R_1}\right) + \left(1+\frac{R_2}{R_1}\right)^2 e^2_n + \left(i^-_n R_2\right)^2 \end{aligned} \tag{B.83}$$

In terms of NG found in Equation B.67

$$e^2_o\left(RTO\right) = 4kTR_2\left(NG\right) + e^2_n\left(NG\right)^2 + \left(i^-_n R_2\right)^2 \tag{B.84}$$

An expression for the NPSD (RTI) is found by dividing Equation B.84 by the NG^2:

$$\begin{aligned} e^2_o\left(RTI\right) &= 4kTR_2\left(\frac{1}{NG}\right) + e^2_n + \left(i^-_n R_2\right)^2\left(\frac{1}{NG^2}\right) \\ &= 4kT\frac{R_1R_2}{R_1+R_2} + e^2_n + \left(i^-_n\right)^2\left(\frac{R_1R_2}{R_1+R_2}\right)^2 \\ &= 4kT\left(R_1 \parallel R_2\right) + e^2_n + \left(\left(i^-_n\right)\left[R_1 \parallel R_2\right]\right)^2 \end{aligned} \tag{B.85}$$

Therefore, substituting $R_1 = 16.5\,\Omega$, $R_2 = 150\,\Omega$, $e_n = 0.90\,\frac{nV}{\sqrt{Hz}}$, $i_n = 2.0\,\frac{pA}{\sqrt{Hz}}$, $NG = 10.09$, $k = 1.38\times10^{-23}$, and , $T = 300\,K$ into Equation B.84 and B.85:

$$\begin{aligned} e^2_o\left(RTO\right) &= 25.06\times10^{-18} + 82.47\times10^{-18} + 0.09\times10^{-18} \\ &= 107.62\times10^{-18} \end{aligned} \tag{B.86}$$

$$\begin{aligned} e^2_o\left(RTI\right) &= 0.246\times10^{-18} + 0.81\times10^{-18} + 0.00088\times10^{-18} \\ &= 1.057\times10^{-18}\,\frac{V^2}{Hz} \end{aligned} \tag{B.87}$$

By taking the square root of both sides, expressions for the noise voltage RTO and RTI are found:

$$e_o\left(RTO\right) = 10.37\frac{nV}{\sqrt{Hz}} \tag{B.88}$$

$$e_o\left(RTI\right) = 1.028\frac{nV}{\sqrt{Hz}} \tag{B.89}$$

The noise voltage at output of the preamplifier is:

$$\begin{aligned} e_{AMP} &= 10.33\,\frac{nV}{\sqrt{Hz}} \times 28.18 \times 1 \\ &= 291.10\,\frac{nV}{\sqrt{Hz}} \end{aligned} \tag{B.90}$$

The NPSD at the output of the preamplifier in dBm/Hz, and referred across a $50\,\Omega$ load is:

$$\begin{aligned} P_N|_{dBm/Hz\ re:\,50\Omega} &= 10\log\left(\frac{291.10n^2}{(50\Omega)(1mW)}\right) \\ &= -117.74\,\left[\frac{dBm}{Hz}\,re:\,50\Omega\right] \end{aligned} \tag{B.91}$$

Bibliography

[1] T. Curtis, "Sonar Technology: Past and Current," Tethnical Rexport, Curtis Technology UK Ltd., http://www.curtistech.co.uk/papers/sonarpc.pdf, Oct. 2004, (date accessed: Oct. 17, 2009).

[2] M. Brissette, J. Hughes-Clarke, J. Bradford, and B. MacGowan, "Detecting small seabed targets using a high frequency multibeam sonar: geometric models and test results," in *OCEANS '97. MTS/IEEE Conference Proceedings*, vol. 2, pp. 815–819, Oct. 1997.

[3] R. Pinkel, H. Merrifield, and J. Smith, "Recent development in doppler sonar technology," in *OCEANS '93. 'Engineering in Harmony with Ocean'. Proceedings*, vol. 1, pp. 1282–1286, Oct. 1993.

[4] T. E. Curtis, "Digital Signal Processign for Sonar. I. The Sonar Problem and Front-end DSP Algorithms," in *Tutorial Meeting on Digital Signal Processing for Radar and Sonar Appications*, vol. 3, pp. 1–27, Sept. 1990.

[5] W. Knight, R. Pridham, and S. Kay, "Digital Signal Processing for Sonar," *Proceedings of the IEEE*, vol. 69, pp. 1451–1506, Nov. 1981.

[6] G. Fischer, A. Davis, and P. Kasturi, "A custom chip set for a frequency-agile high resolution sonar array," *IEEE Journal of Oceanic Engineering*, vol. 32, pp. 416–427, Apr. 2007.

[7] S. Repetto, M. Palmese, and A. Trucco, "Design and assessment of low-cost 3-D sonar imaging system based on a sparse array," in *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*, pp. 410–415, Apr. 2006.

[8] T. Curtis and M. Curtis, "Compact Sonar Surveillance Processing Systems," Tethnical Rexport, Curtis Technology UK Ltd., http://www.curtistech.co.uk/papers/csonar.pdf, Sept. 2004, (date accessed: Oct. 17, 2009).

[9] P. Kraeutner and J. Bird, "A PC-based coherent sonar for experimental underwater acoustics," *IEEE Transactions on Instrumentation and Measurement*, vol. 45, pp. 693–700, June 1996.

[10] J. S. Bird and G. K. Mullins, "Analysis of swath bathymetry sonar accuracy," *IEEE Journal of Oceanic Engineering*, vol. 30, pp. 372–390, Apr. 2005.

[11] A. E. Hay, L. Zedel, R. Craig, and W. Paul, "Multi-frequency, pulse-to-pulse coherent doppler sonar profiler," in *Proceedings of the IEEE/OES Ninth Working Conference on Current Measurement Technology*, pp. 25–29, Mar. 2008.

[12] F. Vernon and W. K. Melville, "Pulse-to-pulse coherent doppler measurements of waves and turbulence," *Journal of Atmospheric and Oceanic Technology*, vol. 16, pp. 1580–1597, Nov. 1999.

[13] Analog Devices Inc., "AD797: Ultralow Noise, Low Distortion OpAmp, Rev. G." www.analog.com/static/imported-files/data_sheets/AD797.pdf, Sept 2008, (date accessed: Oct. 17, 2009).

[14] Analog Devices Inc., "AD8129/AD8130: Low cost 270 mhz differential receiver amplifiers." www.analog.com/static/imported-files/data_sheets/AD8129_8130.pdf, Oct 2008, (date accessed: Oct. 17, 2009).

[15] C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design*. John Wiley and Sons, Inc., New York, 1993.

[16] H. Ott, *Noise Reduction Techniques in Electronic Systems*. John Wiley and Sons, Inc., New York, second edition ed., 1988.

[17] R. Morrision, *Grounding and Shielding: Circuits and Interference*. John Wiley and Sons, Inc., New York, fifth edition ed., 2007.

[18] "ICS-645: Operating Manual," Manual, Interactive Circuits and Systems Ltd., Nov. 2002.

[19] P. Haintz, "Multichannel coherent beam pattern measurement system," Master's thesis, School of Engineering Science, Simon Fraser University, Sept. 2003.

[20] W. M. Marshall, "Fundamentals of low-noise analog circuit design," *Proceedings of the IEEE*, vol. 82, pp. 1515–1538, Oct. 1994.

[21] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. John Wiley and Sons, Inc., New York, fourth edition ed., 2001.

[22] R. Pettai, *Noise in Receiving Systems*. John Wiley and Sons, Inc., New York, 1984.

[23] "SLVA043B: Noise Analysis in Operational Amplifier Circuits," Application Rexport, Texas Instruments, http://focus.ti.com/lit/an/slva043b/slva043b.pdf, 2007, (date accessed: Oct. 17, 2009).

[24] "SBOA066A: Noise Analysis for High Speed Op Amps, Rev. A," Application Rexport, Texas Instruments, http://focus.ti.com.cn/cn/lit/an/sboa066a/sboa066a.pdf, Jan. 2005, (date accessed: Oct. 17, 2009).

[25] Analog Devices Inc., "AD600: Dual, low noise, wideband variable gain amplifier, 0 db to +40 db gain." www.analog.com/static/imported-files/data_sheets/AD600_AD602_.pdf, Oct 2008, (date accessed: Oct. 17, 2009).

[26] D. Stansfield, *Underwater Electroacoustic Transducers: A handbook for users and designers*. Bath University Press, Bath, 1990.

[27] C. Trask, "Designing wide-band transformers for HF and VHF power amplifiers.," *QEX/Communications Quarterly*, pp. 3–15, Apr. 2005.

[28] V. Dumbrava and L. Svilainis, "Application of transformer for improvement of noise performance of ultrasonic preamplifier.," *Ultragarsas (Ultrasound). Kaunas: Technologija.*, vol. 57, pp. 22–28, Apr. 2005.

[29] J. S. Bird, "Subclutter visibility for low-doppler targets," in *Noise and clutter rejection in radars and imaging sensors*, pp. 47–52, 1984.