Design of a Wide Range High Q Varactor using MEMS Technology

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Mahmoud Sam Zahed
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Name: **Mahmoud Sam Zahed**

Degree: **Master of Engineering, Electronics**

Title of project: **Design of a Wide Range High Q Varactor using MEMS Technology**

Examining Committee:

Chair: **Dr. Marinko V. Sarunic**
Assistant Professor of Engineering Science, SFU

Dr. Ash Parameswaran
Senior Supervisor
Professor of Engineering Science, SFU

Dr. Rodney Vaughan
Supervisor
Professor Engineering Science, SFU

Dr. Behrouz Pourseyed
External Examiner
Director of RF Engineering, Sierra Wireless

Date Defended/Approved: October 13, 2009

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Abstract

Recently, the application of MEMS technology in RF and microwave circuits has attracted significant attention. The capabilities of MEMS technology in achieving unprecedented levels of performance make it appealing for RF applications. RF MEMS components could substantially reduce size, weight, power consumption and component counts.

There have been numerous efforts to make a variable capacitor for RF applications. However, each design has focused on a particular aspect of performance, at the expense of the rest.

In this project, a wide range high Q variable capacitor is designed, by means of the MEMS fabrication techniques, for use in RF applications. The inherent limitations of capacitor's tuning range are overcome by designing a suspended structure using the PolyMUMps process. The characteristics of the designed capacitor are simulated and compared against a typical RF capacitor to evaluate its performance. The designed capacitor proves to be an excellent replacement for current RF capacitors.

Keywords: varactor; capacitor; RF; MEMS; PolyMUMPs; wide range

To my parents

Acknowledgement

I would like to express my gratitude to Dr. Behrouz Pourseyed, Dr. Ash Parameswaran, and Dr. Rodney Vaughan for their guidance, support, and mentorship throughout the progress of my project. I owe particular thanks to Dr. Pourseyed, who generously dedicated his time, and motivated me to implement novel ideas in wireless applications.

Finally, I would like to thank my parents for teaching me how to love and supporting me at all times. None of my accomplishments would have been possible without them. I would also like to thank my dear brother, Dara, for his friendship and encouragement.

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1 Introduction

MEMS fabrication techniques have been recently used to overcome the limitations of RF devices and expand their capabilities to unprecedented levels. One of the basic components of any RF circuit is a capacitor. Filtering and matching circuits are the most common applications of capacitors in the RF field. A variable capacitor can make such circuits adaptive or reusable by varying the capacitance over a certain range. There are also circuits requiring tunability that can be implemented by a variable capacitor or a varactor. An example would be a Voltage controlled Oscillator (VCO). However, in recent multiband wireless handheld devices, tunable components require a wide range in a low voltage span. These requirements have traditionally imposed a few constraints on the design of variable components.

This project focuses on designing a wide range RF variable capacitor using MEMS fabrication techniques. It will start off by introducing typical characteristics of an RF capacitor. A few important characteristics are nominal capacitance, tuning range, quality factor, and drive voltage. After identifying the target performance, a brief overview of MEMS fabrication techniques is presented. Details of the popular PolyMUMPs surface micromachining process are provided, and its inherent limitations in design of a variable capacitor are described.

Next, the design of a variable capacitor is studied by evaluating the tuning element. The conducted research is based on a parallel plate capacitor model. Different tuning elements are compared in terms of their potential to achieve the target performance introduced earlier. Once the tuning element is selected, a basic model is designed and characterized. Evaluating the basic model shows how improvements are required to achieve the ideal tuning range.

To extend the tuning range of the basic design, the actuation electrodes are separated from the RF electrodes. Two different implementations of this technique are presented and compared. Moreover, a detailed discussion of the quality factor explains the steps taken to improve the quality factor of the final design.

ANSYS is used as the main simulation tool in this project. Both electrical and mechanical properties of the designs are simulated using ANSYS. Details of the simulation parameters along with the simulation scripts are appended at the end of this document.

Finally, by comparing the simulation results of a few designs, the most attractive design in terms of the characteristics of the MEMS capacitor is identified. After characterizing the final design, its layout is presented in Cadence. This layout will be sent to MEMSCAP for fabrication using the PolyMUMPs process.

2 Device Characteristics

A variable capacitor is to be designed for use in wireless handheld devices. Therefore, the frequency range of the design is picked based on the operating cellular bands. The cellular bands can be divided into low and high groups based on their frequency. While the low band spans from 700MHz to 1GHz, the high band goes from 1.7 to 2.5GHz. Based on these operating bands, the desired tuning rage of the capacitor can be determined. Considering a variable capacitor, the tuning range is defined as the ratio of maximum capacitance to minimum capacitance times a hundred. According to Equation (1), the desired tuning range for each band can be calculated from the frequency limits.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

Consequently, a tuning range of 200% is required for the low band, while the high band tuning range needs to be 220%. Based on this simple calculation, and after considering a safety margin for the design, the tuning range requirement will be set to 400%.

The nominal capacitance can also be calculated by taking a typical inductance value into account. Based on common RF matching circuits used in the referenced bands, the nominal inductance values are about 5 and 10nH for high and low bands respectively. This will give a nominal capacitance value of 5.2pF for the lowest frequency and 0.8pF for the highest.

For both bands, a high quality factor is needed to avoid losses thorough the signal path. The target Q for the desired capacitor will be set to “50 plus” based on the typical RF components used in matching circuits. The major design characteristics to be achieved are summarized in Table 1.

Table 1: Target performance characteristics

	Low Band	High Band
Frequency Range	700 – 1000 MHz	1.7 – 2.5 GHz
Nominal Capacitance	1.3 – 5.2 pF	0.8 – 3.2 pF
Tuning Range	400%	400%
Quality Factor	Above 50	Above 50

With these characteristics in mind, the remaining design variables are to be studied to achieve the optimal performance. The design variables are:

- Driver voltage and current
- Tuning method, i.e. the tunable element in a parallel plate capacitors
- Fabrication technique

The next section provides a brief introduction to MEMS fabrication techniques and describes the fabrication process chosen for the final design.

3 MEMS Fabrication

3.1 MEMS Fabrication Techniques

Silicon micromachining is the process by which MEMS devices are fabricated. It refers to structuring a silicon substrate to create microscopic mechanical parts. Silicon micromachining can be categorized into two technologies, bulk micromachining in which the substrate is etched to create different structures and surface micromachining that creates structures by depositing layers and films on top of the substrate. To create high aspect ratio 3D structures the LIGA process (German acronym for X-ray lithography, electro-deposition and molding) is used. Various materials such as metals, plastics and ceramics are used in the LIGA process to create high aspect ratio devices with electric, magnetic, optic and insulating properties that cannot be made with silicon based devices.

Bulk micromachining is the most mature silicon micromachining technology. It involves removing a significant amount of silicon from the substrate by means of wet or dry etching techniques. Wet etching refers to employing water based etchants, while dry etching uses vapor and plasma etchants to etch different atomic crystallographic planes in the wafer. Atomic bonding of various wafers is also used for the assembled MEMS devices.

Surface micromachining builds up a structure by sequentially adding thin films of structural and sacrificial layers to the wafer. In the end, the sacrificial layers are removed to form the mechanical structure. Surface micromachining has the advantage of creating much smaller devices. Moreover, such devices can be easily integrated into ICs by using the same wafer. Consequently, surface micromachining has been employed as the main technique to create tunable capacitors.

Surface micromachining has been standardized into three fabrication processes depending on the materials used. The next sub-section explains these fabrication processes.

3.2 Fabrication Process, PolyMUMPs

MEMSCAP, a pioneer MEMS fabrication facility, has established the Multi-User MEMS Processes, or MUMPs, as a commercial program that offers cost-effective and proof of concept MEMS fabrication to the world. The idea is to combine a number of designs into a single wafer for fabrication purposes and dice out individual designs at the end. The MUMPS process has proven to be an attractive fabrication process for universities and industries around the that want to make a prototype of their designs.

There are three standard processes as part of the MUMPs program: PolyMUMPs, a three layer polysilicon surface micromachining process, MetalMUMPs, an electroplated nickel process, and SOIMUMPs, a silicon on insulator micromachining process. PolyMUMPs is the most popular fabrication process, and has been extensively used for designing electro-mechanical structures. Therefore, PolyMUMPs has been chosen as the fabrication method for the design presented in this project.

Given the multi-user nature of the MUMPs program, a set of rules are defined for each MUMPs process that have to be followed for successful fabrication. These rules impose inherent limitation on size and dimensions of the design.

The PolyMUMPs process offers three polysilicon layers, namely, Poly0, Poly1, and Poly2. Suspended mobile structures can be made using the last two layers, Poly1 and Poly2. The sacrificial layers are phosphosilicate glass (PSG) and are deposited in between the three polysilicon layers. The available gaps in the design are defined by the thickness of each sacrificial layer. A gold metal plate can only be deposited on the Poly2 layer. The metal layer can be used for probing, bonding, electrical routing, and highly reflective mirror structures. The electrical isolation between the polysilicon and the substrate is achieved by using silicon nitride. The properties of each layer of the PolyMUMPs process are summarized in Table 2.

Table 2: Layers of the PolyMUMPs process, bottom-up order

Layer	Color	Thickness (μm)	R (Ω/sq)	ε_r
Silicon Substrate		525		
Si_3N_4		0.6		4
Poly0		0.5	30	
Oxide1		2		3.8
Poly1		2	10	
Oxide2		0.75		3.8
Poly2		1.5	20	
Metal		0.5	0.06	

MEMSCAP usually sends out the dice as the final product. The release of the sacrificial oxide is expected to be done by the end user at a local facility. However, for an additional fee, the release of the dice can be arranged at MEMSCAP facilities. The release process begins by immersing the structures in a bath of 49% HF at room temperature for 1.5 to 2 minutes. To reduce stiction of the layers, the structure is put in DI (Deionized) water and then alcohol, after which it will be transferred to an oven at 110C for at least ten minutes.

Being a general, multi purpose process, PolyMUMPs is not specifically designed for RF application. Consequently, several performance limiting factors are inherent in the process when used in RF designs. The most important limiting factor in terms of high frequency operation is the capacitive coupling through the substrate.

To achieve the high quality factor required by RF applications, the choice of the substrate has been extensively studied to minimize dielectric losses. To obtain high resistivity substrates, capacitors have been made on alumina or silicon materials. The PolyMUMPs process uses silicon as the substrate, which introduces practical resistivity. Moreover, the isolation between the structural layers and the substrate in the PolyMUMPs process is achieved by silicon nitride. Nevertheless, despite its good isolation properties, silicon nitride still introduces coupling through the substrate.

The other downside of the PolyMUMPs process is the availability of only one metal layer. For the case of a parallel plate capacitor, this means that only one of the plates will be metallic, resulting in a poor quality factor for the capacitor. Moreover, the metal layer is only 0.5μm thick. Considering the RF frequencies of 100MHz to 3GHz, this thickness directly contributes to the skin effect losses through the metal. Imperfections in the fabrication process can also result in a less optimum electrical continuity of the metal layer.

Despite all of the described limitations, PolyMUMPs offers reasonable thickness and resistivity for the structural layers, which makes it popular for electromechanical applications. The next section discusses the choice of the tuning element in a parallel plate capacitor.

4 Tunable Element

Capacitance is defined as the ratio of the accumulated coulomb charge on a structure to the applied voltage as shown in Equation (2). For a parallel plate capacitor, capacitance is merely defined by dimensions and the dielectric material.

$$C = \frac{Q}{V} = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{2}$$

Here, ε_0 is the permittivity of the air and ε_r is the relative permittivity of the dielectric material. Considering a parallel plate capacitor, the tuning mechanism can be the spacing between the plates, the area of the plates, or the dielectric material between the plates. The following sub-sections discuss the limitations and advantages of each method of tuning.

4.1 Dielectric Material

Changing the capacitance by inserting a dielectric material between the plates might seem attractive at first. However, the tuning range achieved by this method depends on the relative permittivity of the dielectric material. In other words, the higher the relative permittivity of the dielectric is, the higher the tuning range of the capacitor will be. Given a specific fabrication process, the relative permittivity of the dielectric is dictated by the material used in the process. Moreover, the suspension of the dielectric material cannot be achieved in many of the fabrication processes including PolyMUMPs.

Nevertheless, this method has been implemented using other fabrication processes and published in literature. Yoon and Nguyen introduced a tunable capacitor by varying the effective inter-plate dielectric constant [1]. In their approach, a movable dielectric is attached to the substrate by a spring structure at a point outside the two plates. The voltage applied between the plates will induce charges on the dielectric, effectively pulling it inside the gap between the plates. Figure 4-1 shows the functional diagram of this capacitor.

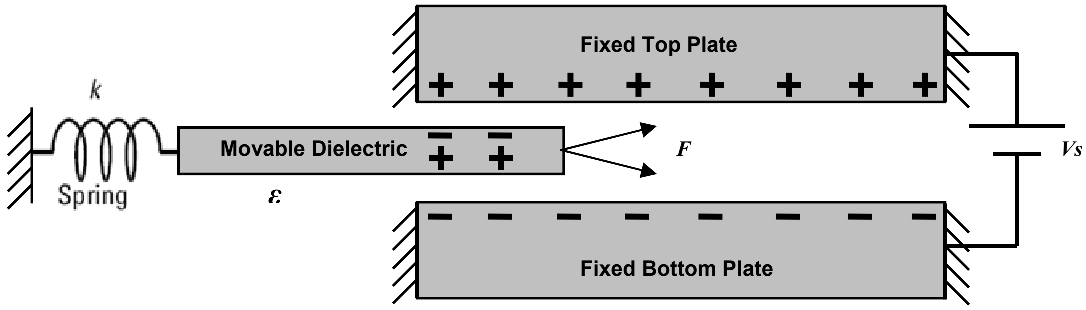

Figure 4-1: Moving dielectric variable capacitor (De Los Santos, 2002)

A prototype sample was made with copper as the plates and plasma enhanced chemical-vapor deposition (PECVD) nitride as the dielectric. The device, with a nominal capacitance of 1.14 pF and characterized between 0.6 and 6 GHz, showed a Q of 218 at 1 GHz, a tuning range of 140%, and a tuning voltage span of 10V.

Apart from the low tuning range, a major drawback of this design is the possibility of imbalanced spring factors. If the spring constant of the dielectric for moving perpendicular to the parallel plates is smaller than its lateral spring constant, the dielectric will move vertically, upon application of voltage, and attach to the closest plate. As a result, the effective force on the dielectric changes and the tuning curve of capacitance versus voltage will be altered unexpectedly.

4.2 Plate's Area

According to Equation (2), the capacitance is linearly dependent on the plate's area. Therefore, to boost the tuning range, the effective area of the plates has to be increased with the same order. Since the plate's spacing is dictated by thickness of the fabrication technology, the area of the plates determines the capacitance value. For a capacitance in the range of pFs, the plates have to be designed with dimensions greater than a few hundreds of μms. Electrostatic tuning of a capacitor, by changing the size of such an area is no easy task.

Having shown low tuning ranges, the early designs were improved by periodically arranging the plates to build arrays of suspended plates, also called comb-drives. The small change of area for each plate was multiplied by the number of plates to result in a noticeable change in capacitance. These plates could be driven by different lateral actuation techniques such as thermal actuation, comb driven electrostatic actuation, or micro-electromechanical digital to analog conversion. Figure 4-2 shows the functional model of this technique.

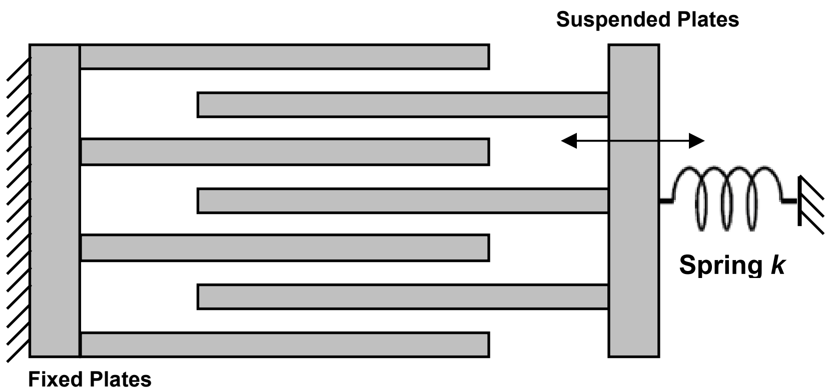

Figure 4-2: Laterally movable plate capacitor (Seok, 2000)

In an example of this method, a surface micro-machined capacitor consisting of a single suspended plate of silicon with 608 comb fingers was developed by Seok [4]. The tuning electrode was made on a pyrex glass to minimize the RF losses through the substrate. The final structure was made by silicon-glass anodic bonding process. The prototyped capacitor showed a tuning range of 150% for a nominal capacitance of 1.4pF and a Q factor of 4 at 1GHz. As mentioned before, a tuning range of 150% is not enough for most RF applications.

4.3 Plate's Spacing

As the last alternative, the plate's spacing can be used to tune a variable capacitor. According to Equation (2), capacitance is inversely proportional to the plate's spacing. Therefore, the slope of change is steep and high tuning ranges can be achieved by small changes in distance. Consequently, changing the plate's spacing is the most promising approach in designing a wide tuning range varactor.

Changing the spacing of a capacitor's plates can be implemented by suspending one of the plates as a mobile structure. Figure 4-3 shows the functional model of this method.

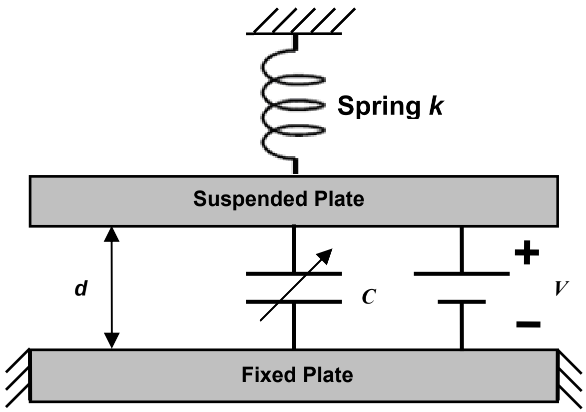

Figure 4-3: Changing the plate's spacing (De Los Santos, 2002)

By applying a voltage between the plates, an electrostatic potential develops that produces an attraction force. The electrostatic force counteracts with the mechanical force of the suspended plate. The position of the suspended plate is determined by the balance of the two forces. Equation (3) shows the equilibrium condition between the forces.

$$kx = \frac{1}{2}\frac{\varepsilon_0 A}{(d-x)^2}V^2 \tag{3}$$

Here, A is the area of the plates, d is the gap between the plates, k is the equivalent stiffness constant of the suspension, x is the displacement of the mobile plate, and V is the applied voltage. Since the electrostatic force increases drastically as the distance approaches zero, at a certain distance, the mechanical force of the suspension can no longer counteract with the electrostatic force and the mobile plate will collapse. Figure 4-4 shows the solution of Equation (2) for different voltages. At a certain threshold voltage, known as the pull-in voltage, the mechanical force curve is tangential to the electrostatic force curve. Solving Equation (3) for tangential curves, the pull-in voltage can be found. Equation (4) shows the obtained expression for the pull-in voltage.

$$V_{pi} = \sqrt{\frac{8kd^3}{27\varepsilon_0 A}} \tag{4}$$

For voltages higher than the pull-in voltage, there is no intersection between the two curves and the mobile plate collapses in absence of equilibrium.

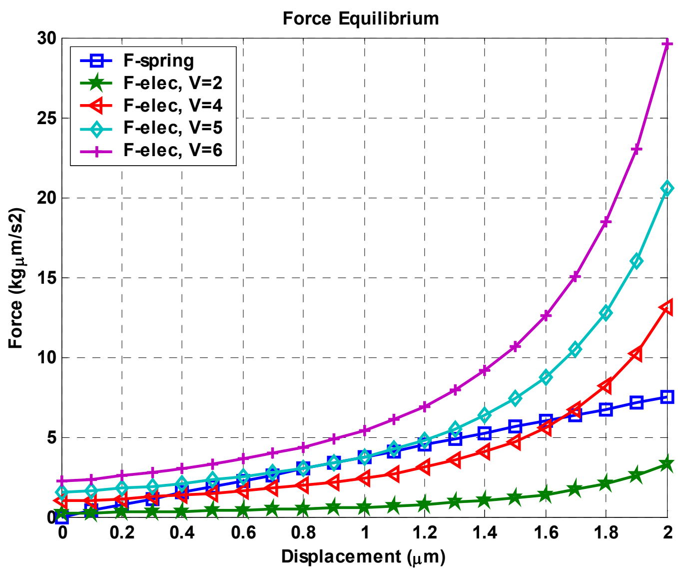

Figure 4-4: Electrostatic and mechanical force equilibrium

It can be shown that the collapse happens when the initial gap has been reduced by one third. The voltage associated with this gap is referred to as the pull-in voltage. Therefore, the most important limiting factor of this method, in terms of tuning range, is the pull-in phenomenon.

Since only 33% of any initial distance can be used towards tuning the capacitor, this method is inherently limited to a tuning range of 150%, and has to be improved to achieve higher tuning ranges. Because the chosen fabrication process is PolyMUMPs, all dimensions and material properties considered for improvements have to comply with PolyMIMPs process rules.

In addition to the pull-in effect, there are three more performance limiting factors in a spring suspended parallel plate capacitor. First, the Q is degraded by the series resistance of the spring. Second, long springs are required to achieve a low drive voltage varactor, and third, the stiffness of the springs limits the tuning range. Moreover, because of the non-linear relationship between the capacitance and the inter-plate distance, step sizes in capacitance are not linear. In other words, the resolution of the variable capacitor is not optimum.

Several improvement techniques have been introduced that, by using the PolyMUMPs process, extend the tuning range of a varactor. However, these techniques have solely focused on extending the tuning range, with no consideration of the implemented capacitance value. In other words, if the capacitance is designed for a nominal value of 0.1pF, a wide tuning range of 600% will only result in a capacitance of 0.6pF, which is not sufficiently wide in RF applications. As explained in section 2, RF applications require capacitance values in the range of 0.5pF to 5pF.

The proposed design in this project uses the spacing between the plates as the tuning mechanism to achieve the target performance outlined in section 2. The next section describes possible improvement techniques to extend the tuning range beyond the pull in distance.

5 Design Models

5.1 Basic Capacitor

To show the limited tuning range of a parallel plate capacitor, a basic PolyMUMPs structure was designed. Figure 5-1 shows the cross section of this basic capacitor.

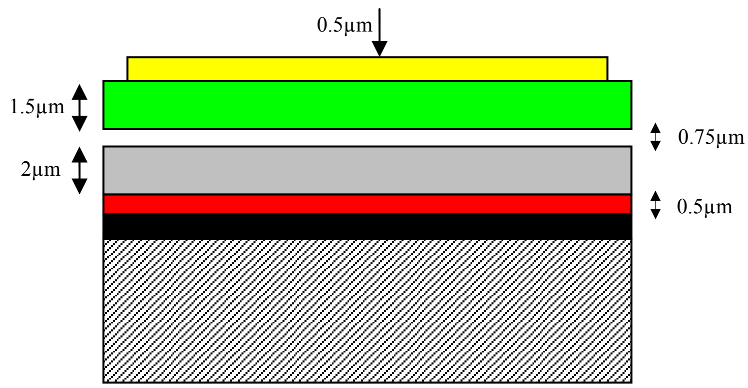

Figure 5-1: Structure of the basic capacitor

Poly2 layer is used as the mobile plate, while Poly1 layer is the fixed bottom plate. The distance between the plates is the thickness of the second oxide layer, which is 0.75µm. The area of the plates was designed to be 230 µm x 210 µm to give a nominal capacitance of 0.57pF. Considering the theoretical tuning range of 150%, which corresponds to travelling one third of the initial gap, it is expected that the capacitance could be varied from 0.57pF to 0.86pF.

Two straight suspensions were designed to allow vertical movement of the mobile plate. Dimensions of the suspensions were chosen for a maximum actuation voltage of 1.5V. The position of the suspensions on the top plate was chosen to maintain balance and maximize the applied force on each cantilever. For a pull-in voltage of 1.5V, the equivalent stiffness of the suspensions can be calculated using Equation (4) to be $7.7\, kg/s^2$. Based on the obtained value of stiffness, length and width of each straight suspension was calculated using the beam bending formula shown in Equation (5).

$$k = \frac{3EI}{l^3} = \frac{Ehb^3}{4l^3} \qquad (5)$$

where k is the equivalent stiffness of the beam, E is the Young's modulus of elasticity, I is the second-area moment, b is the width of the beam, h is the height of the beam, and l is the length of the beam. Figure 5-2 shows the designed structure simulated in ANSYS. The ESSOLVE macro was used to simulate the structure. The structure was broken down to small elements, each called a mesh, to solve for voltage and displacement at every point. The air around the capacitor plates was meshed to an offset distance to account for fringing effects, which is also shown in the picture. All mesh sizes were carefully chosen to provide accurate results. The mesh elements can be seen in Figure 5-2 as different sized triangles. For a coupled field analysis, the adjustment of the electrostatic field mesh to coincide with the deformed structural mesh is vital. In ANSYS, this adjustment is known as mesh morphing. Boundary conditions were set carefully to allow for morphing adjustments. In cases where morphing fails, the ESSOLVE macro re-meshes the electrostatic field such that the elements coincides with the deformed structural mesh.

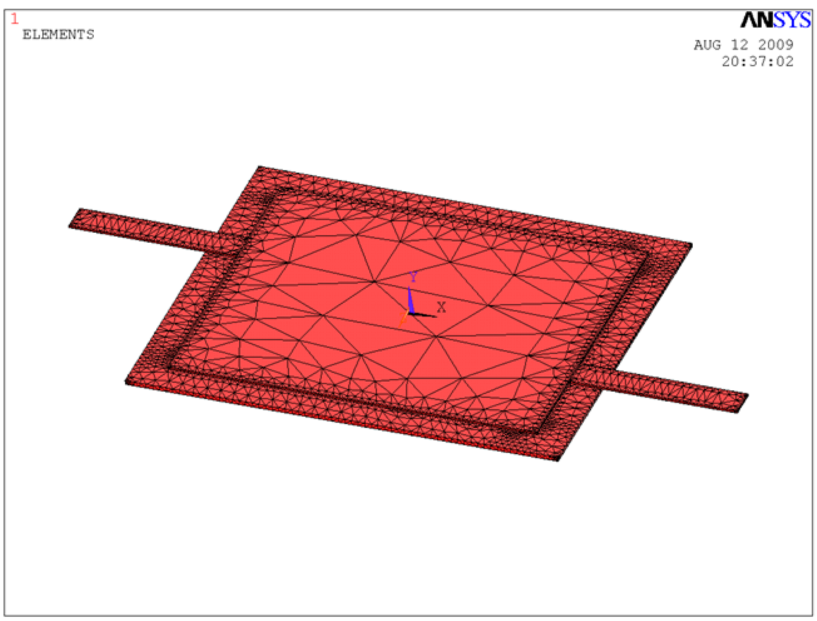

Figure 5-2: Basic capacitor model in ANSYS

Figure 5-3 shows the electrostatic force applied to the mobile plate. Point forces are shown for each node generated by meshing.

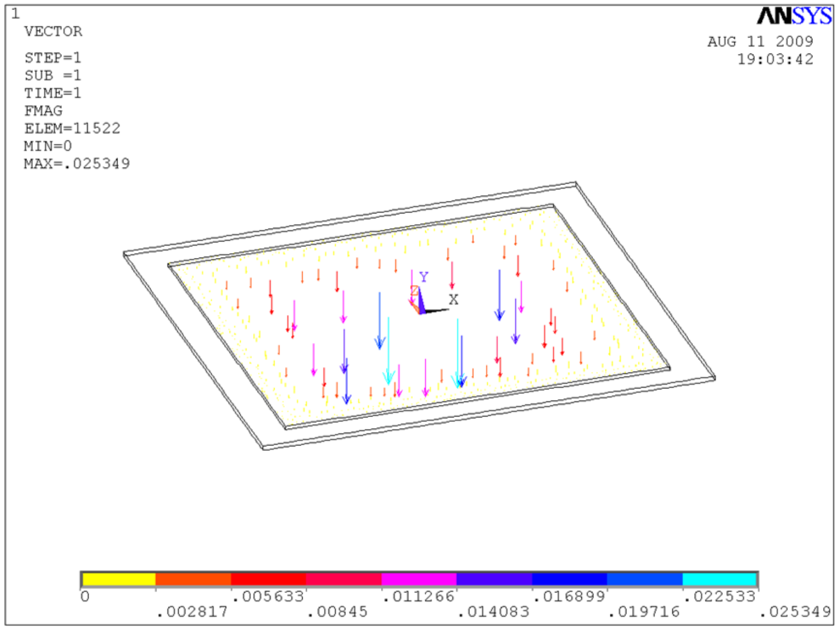

Figure 5-3: Basic capacitor, electrostatic force applied to the mobile plate

To calculate the plate's displacement for an applied voltage, Equation (2) is solved when the voltage is swept from zero to the maximum pull-in value. The resulting theoretical displacement is then compared to that obtained by simulation. The result is shown in Figure 5-4, where simulation follows the theoretical calculations closely. Moreover, it is observed that for an applied voltage of 1.25V, the top plate has travelled by 0.1µm.

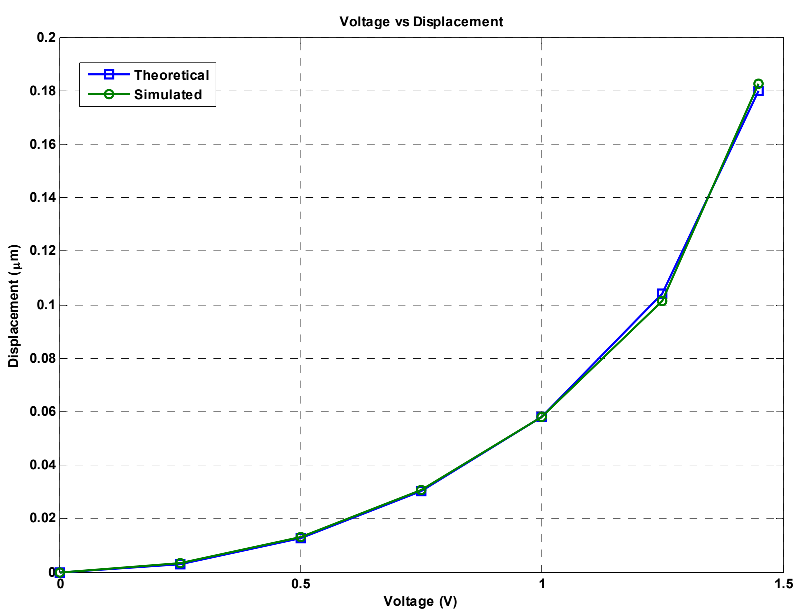

Figure 5-4: Basic capacitor, voltage vs. displacement

Figure 5-5 captures the displacement of the mobile plate for an applied voltage of 1.25V. As expected the top plate has moved down by a maximum of 0.1 μm from its initial position, a result that matches theoretical calculations. The agreement between the theoretical calculations and simulation results confirms the accuracy of the simulation model used. However, Figure 5-5 shows that the mobile plate develops a curvature due to the attached suspensions. In other words, the points on the plate closer to the suspensions have smaller displacements compared to others. The curvature of the mobile plate affects the tuning range of the capacitor as the plate’s position does not change evenly.

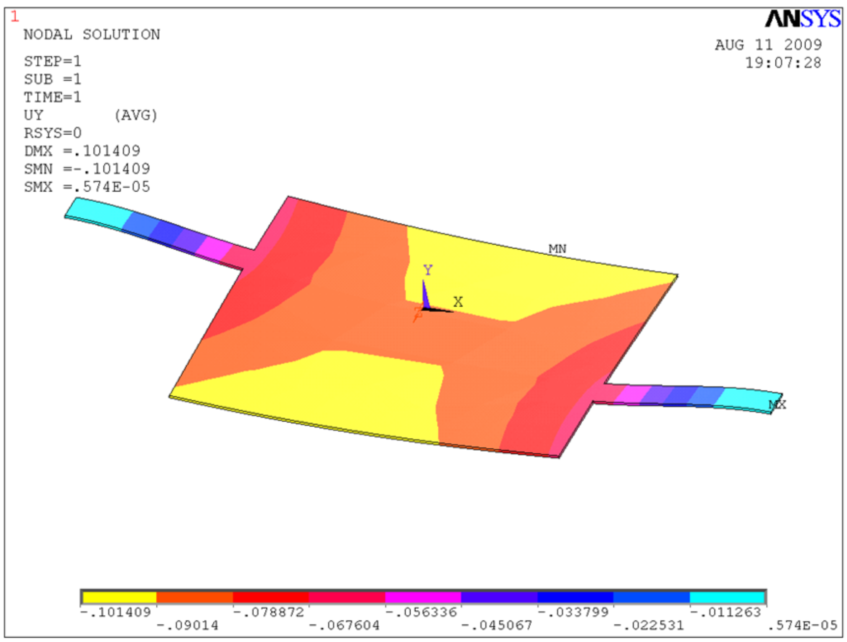

Figure 5-5: Basic capacitor, displacement of the mobile plate for *V*=1.25V

The basic capacitor design clearly shows the pull-in limitation since the simulation does not converge as the voltage reaches the pull-in threshold. Figure 5-6 indicates the capacitance as a function of the applied voltage. For low actuation voltages, the simulated capacitance is higher than theoretical because of the inclusion of the fringing effects in the simulation model. However, as the voltage is increased, the simulated capacitance falls under the theoretical results due to the plate’s curvature.

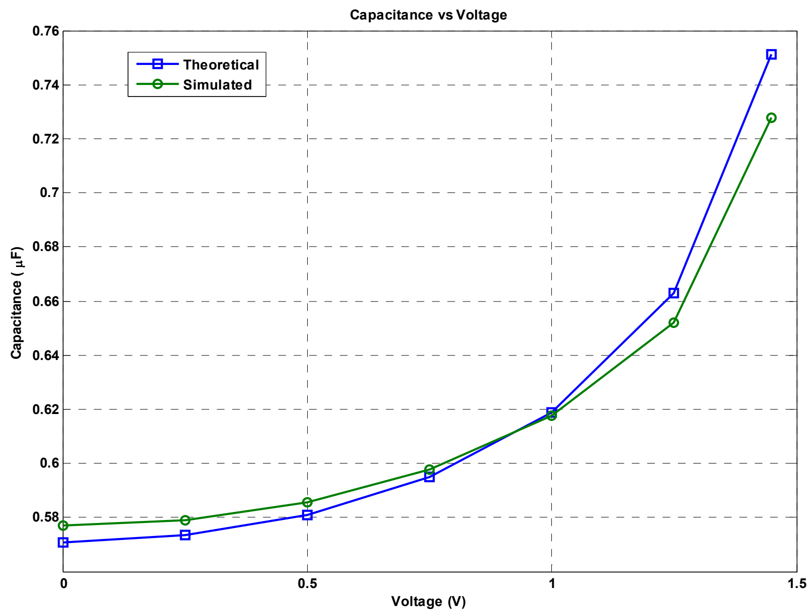

Figure 5-6: Basic capacitor, capacitance vs. voltage

In practice, straight beams are not the best choice of suspensions. Since the fabrication process requires deposition of polysilicon at high temperatures followed by a cooling down period, the mobile structures develop residual stress due to thermal expansion of polysilicon. Moreover, in case of a capacitor, the mobile plate is made of two materials, namely polysilicon and gold, with different thermal expansion coefficients. Therefore, the thermal stress is stronger during the release process, and the mobile plate warps. To avoid this problem, and allow a slight movement in the X-Y plane during the release of the suspended plate, circular suspensions were chosen. Figure 5-7 show the same basic capacitor with circular suspensions. The gray meshed structure shows the original location of the top plate. Again, for an applied voltage of 1.25V, the top plate has moved down by a maximum 0.1 μm. On the other hand, it is observed that the curvature of the mobile plate is more when using circular suspensions. The calculation for the equivalent stiffness of the suspensions follows the same method explained for straight beams. However, instead of Equation (5), the corresponding bending equation of a circular beam is used.

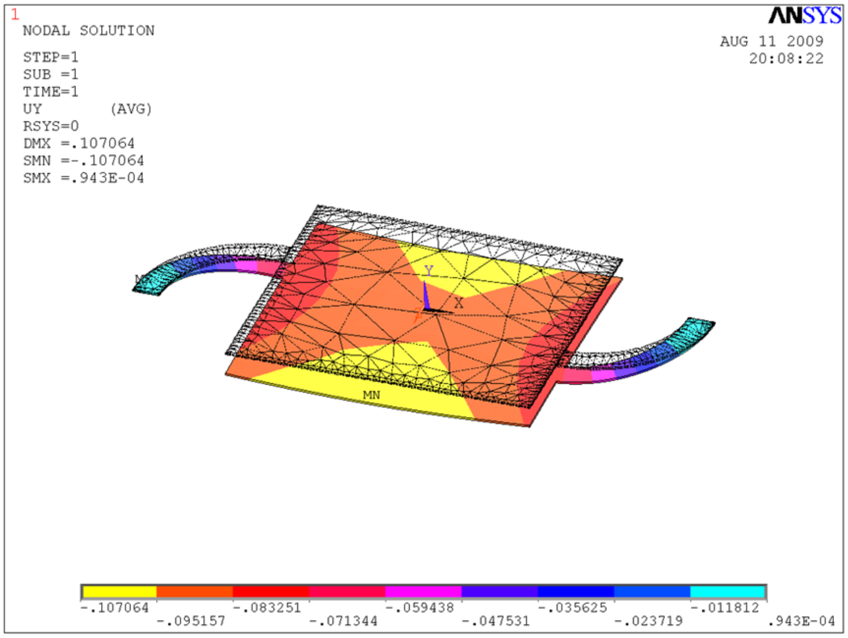

Figure 5-7: Basic capacitor, circular suspension, displacement for *V*=1.25V

The design parameters of the basic capacitor are summarized in Table 3.

Table 3: Parameters of the basic capacitor

Parameter	Size (μm)
Length of the plates	230
Width of the plates	210
Plate's distance	0.75
Length of the straight suspensions	105
Width of the straight suspensions	20
Radius of circular suspensions	80
Width of circular suspensions	20

5.2 Type-1 Extended Tuning Range Capacitor

To extend the tuning range of the basic capacitor, the actuation electrodes can be separated from the RF electrodes. This separation allows taking advantage of a wider tuning range if the distance between the actuation electrodes is more than the distance between the RF electrodes. Two possible design structures can be made using the PolyMUMPs process by using either of oxide1 or oxide2 layers as the plate's separation. Figure 5-8 and Figure 5-9 show these structures.

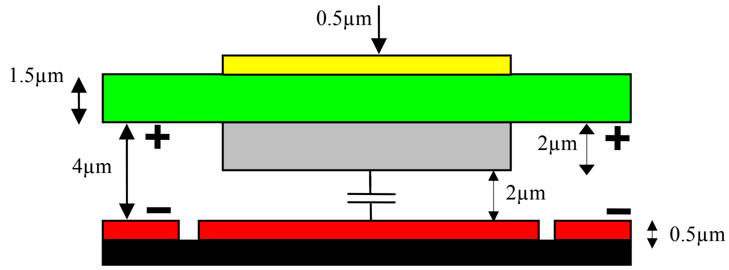

Figure 5-8: Type-1 extended tuning range capacitor

In Figure 5-8, Poly0 and Poly1 are used as RF electrodes. Applying the actuation voltage between Poly0 and Poly2 layers allows for an actuation distance of 4 µm while the distance of the capacitor plates is 2 µm. Because, the pull-in effect happens when the distance between the actuation plates is reduced by one third, 1.33 µm in this case, the tuning range of the capacitor is extended to 300% according to Equation (6), where d_1 and d_2 are the RF and actuation electrodes separations respectively. Nevertheless, this design still suffers from the pull-in effect.

$$TR = \frac{1/(d_1 - d_2/3)}{1/d_1} = \frac{3d_1}{3d_1 - d_2} = \frac{3 \times 2}{3 \times 2 - 4} = 3 \qquad (6)$$

In the next sub-section, a better approach will be introduced to eliminate the pull-in limitation.

5.3 Type-2 Extended Tuning Range Capacitor

Figure 5-9 shows an improved method that, by using the thickness of the PolyMUMPs technology, makes the tuning range of the capacitor extremely wide. In this case, Poly1 and Poly2 layers are used as RF electrodes, while actuation happens between Poly2 and Poly0 layers. Because the distance between the plates of the capacitor (0.75µm) is smaller than one third of the distance between the actuation electrodes (0.92µm), the mobile plate will never experience the pull-in effect, even when the capacitor plates are too close. Since this method theoretically eliminates the pull-in limitation, it was chosen for the design presented in this project.

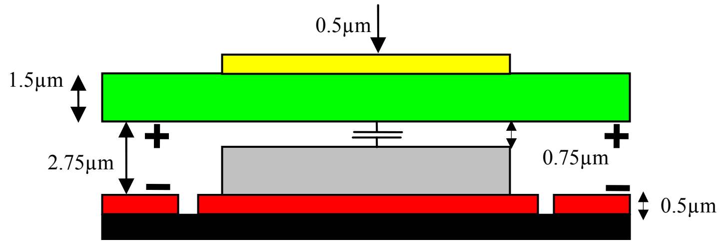

Figure 5-9: Type-2 extended tuning range capacitor

However, the tuning range in such a design will be bounded by the breakdown voltage of air. Therefore, understanding the electrical breakdown of air between the capacitor's electrodes is important. Increasing the voltage beyond the breakdown point annihilates the capacitance model as the dielectric starts to conduct. In other words, there is a minimum spacing between the plates that has to be maintained before breakdown happens. Hourdakis has measured the breakdown voltage of air as a function of electrode separation using a MEMS capacitor [10]. The data shows that, for plate separations greater than 1µm, the breakdown voltage remains above 50V. Consequently, as long as the electrodes separation is more than 0.1µm, the applied voltage can be increased up to 50V with no breakdown.

A drawback of this design is the higher actuation voltage associated with the increase in the actuation distance. Moreover, the effective area of the actuation electrodes is reduced by the area of the RF electrodes. Therefore, to operate with reasonably low actuation voltages, the area of the actuation electrodes has to be proportionally large compared to the RF electrodes. The relative placement of the actuation and capacitor electrodes plays an important role in the balance between the electrostatic and mechanical forces. A center position was chosen to achieve symmetrical actuation.

Targeting a nominal capacitance of 0.5pF, the area of the plates was calculated to be 42354 μm^2 . Based on the obtained area, the RF electrodes were designed as 147µm by 290µm rectangles to facilitate simulation. Next, the actuation voltage was limited to 5V, a typical maximum in electronic circuits. The area of the actuation electrodes and the size of the suspensions were designed based on the pull-in voltage of 5V. PolyMUMPs design rules were considered throughout the design. For example, the minimum distance between the Poly0 structures is mandated by the PolyMUMPs process. Moreover, Poly0 layer should enclose Poly1 layer by at least 4 µm to ensure that Poly0 is an effective ground plane for Poly1 structures. Table 4 summarizes the design parameters of the Type-2 capacitor.

Table 4: Parameters of the Type-2 capacitor

Parameter	µm
Length of actuation electrodes	294
Width of actuation electrodes	437
Actuation gap	2.75
Length of RF plates	147
Width of RF plates	290
RF gap	0.75
Radius of curvature for suspensions	150
Width of suspensions	40

To guarantee that the suspended plates do not warp, it is crucial to maintain a symmetrical structure. The dimensions of the actuation electrodes were designed to maintain symmetry and ensure robustness of the suspensions. Figure 5-10 captures the simulation model of the Type-3 capacitor. Figure 5-10 (a) shows the Poly1 plate of the capacitor and the air region surrounding it. Figure 5-10 (b) illustrates the air region surrounding the Poly1 plate of the capacitor when the Poly1 plate is removed. Figure 5-10 (c) shows the air region between the two plates of the capacitor. As indicated in this graph, the air region is extended beyond the capacitor's plates to account for fringing effects. Dividing the air region between the actuation plates in two parts leads to accurate element sizes during the meshing process. The boundary between the two air regions is fixed with no degrees of freedom. When the air elements are morphed to accommodate for structural movements, this boundary condition prevents the elements from moving past the Poly1 surface. Figure 5-10 (d) illustrates the symmetric actuation electrodes on the bottom plate, along with the centered Poly0 piece used for supporting the fixed Poly1 plate of the capacitor.

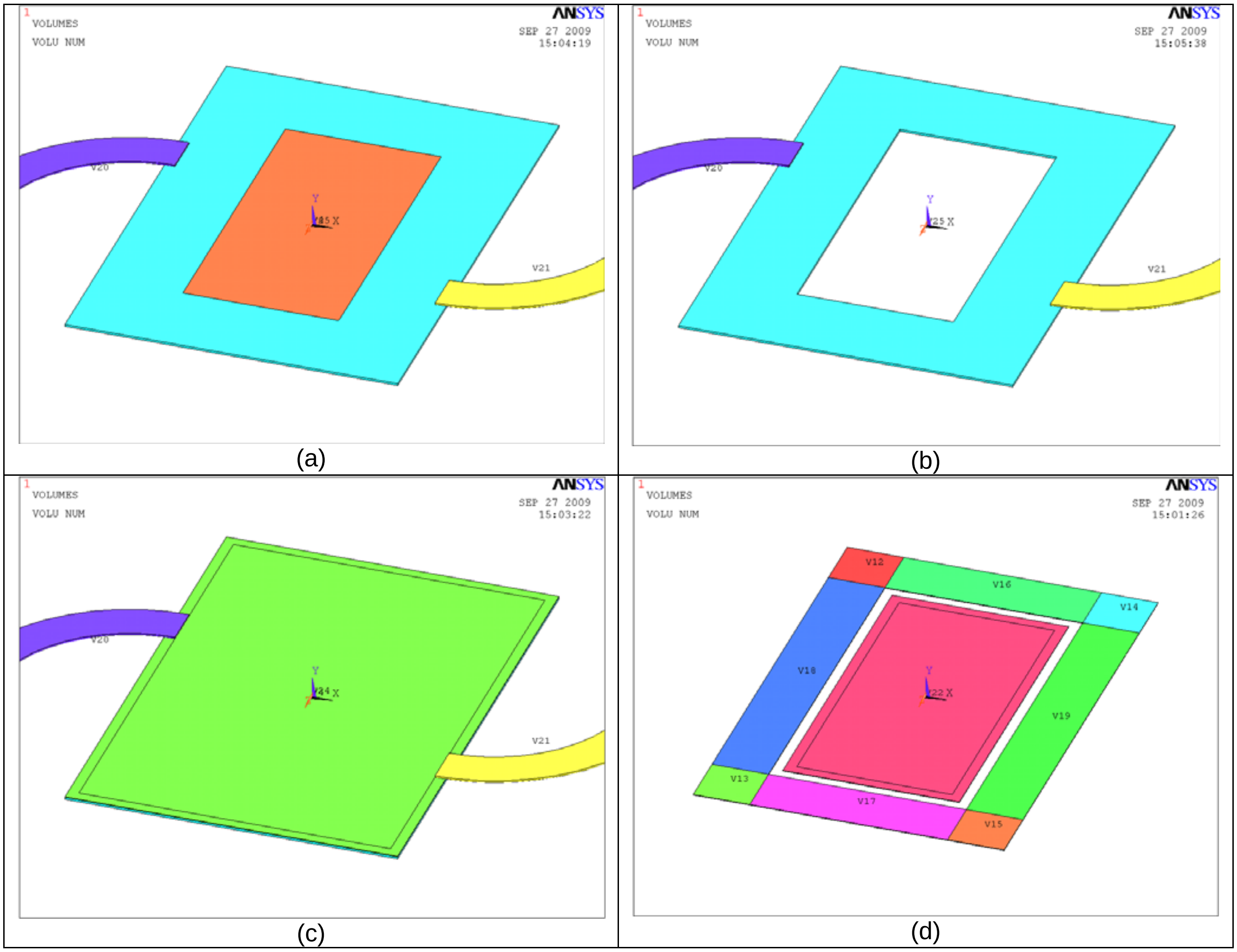

Figure 5-10: Type-2 capacitor, simulation model

The effective area of electrostatic actuation is the area of the mobile plate that falls out of the RF electrode trajectory. The electric filed between the actuation plates has been captured in Figure 5-11.

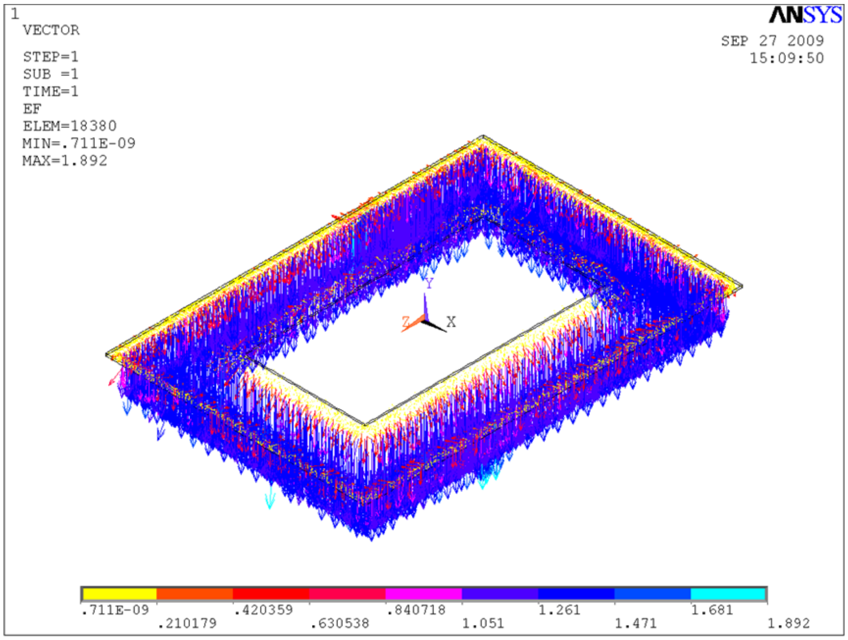

Figure 5-11: Type-2 capacitor, electric field between actuation plates

Careful selection of mesh sizes was required to obtain accurate simulation results in ANSYS. By solving Equation (3) for a ramp voltage of 0V to 5V, displacement of the mobile plate can be obtained as a function of the applied voltage. Figure 5-12 compares the simulation result to the theoretical calculations. Moreover, it is observed that for an applied voltage of 3.25V, the mobile plate moves down by a maximum 0.2µm.

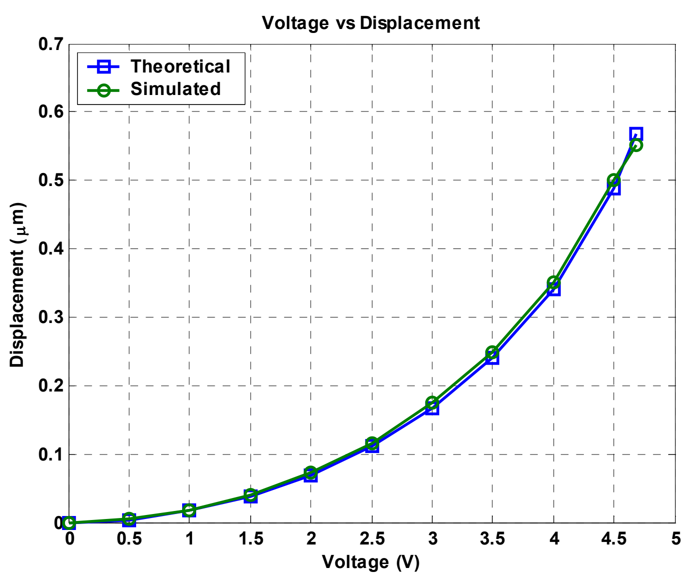

Figure 5-12: Type-2 capacitor, displacement vs. voltage

Figure 5-13 illustrates the simulation run for *V*=3.25V, which validates the simulation model by meeting the theoretical calculations. It should be noted that the curvature of the mobile plate is more compared to the basic capacitor, because the RF electrodes prevent the centre of the plate from being actuated.

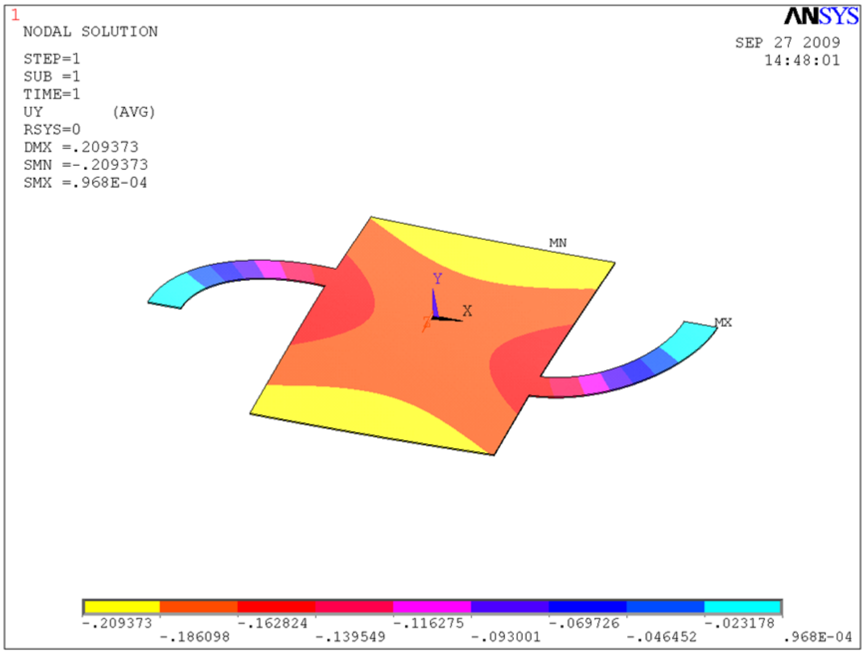

Figure 5-13: Type-2 capacitor, displacement for *V*=3.25V

Because the pull-in limitation is eliminated by this design, the expectation is that the capacitance continues to increase as the voltage is boosted until a breakdown happens. However, as the simulation results show, the structure starts to collapse as the plates get very close. The curvature of the mobile plate and the elastic design of the suspensions add up to make the structure unstable as the voltage reaches its maximum and the two plates get close. The maximum displacement of the mobile plate is 0.552 µm, indicating that only around 74% of the initial gap can be traveled before the simulation diverges. Taking the ratio of the original and maximum separations, the tuning range is expected to be 379%. However, the actual tuning range is about 325% because of the curvature of the mobile plate. Nevertheless, even at maximum displacement, there is still a gap of 0.2µm between the two plates. Therefore reaching the air breakdown voltage is never a concern, specially considering the maximum applied voltage of 5V.

Figure 5-14 shows the deflected plate for $V = 4.5$V. It can be observed that one side of the mobile plate starts to go down more than the other as the plat's curvature increases.

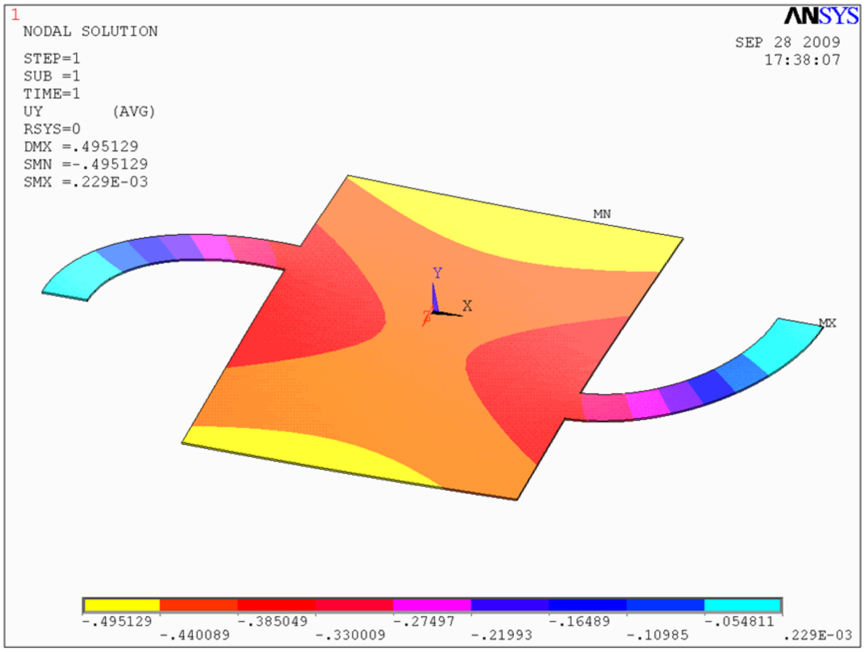

Figure 5-14: Type-2 capacitor, plate's curvature for *V*=4.5V

Rather than the electric breakdown of air, the main limiting factor for the tuning range of this design is the curvature of the moving plate and elastic characteristics of the suspensions. Figure 5-15 shows the curvature of the mobile plate at the maximum displacement of 0.552 μm.

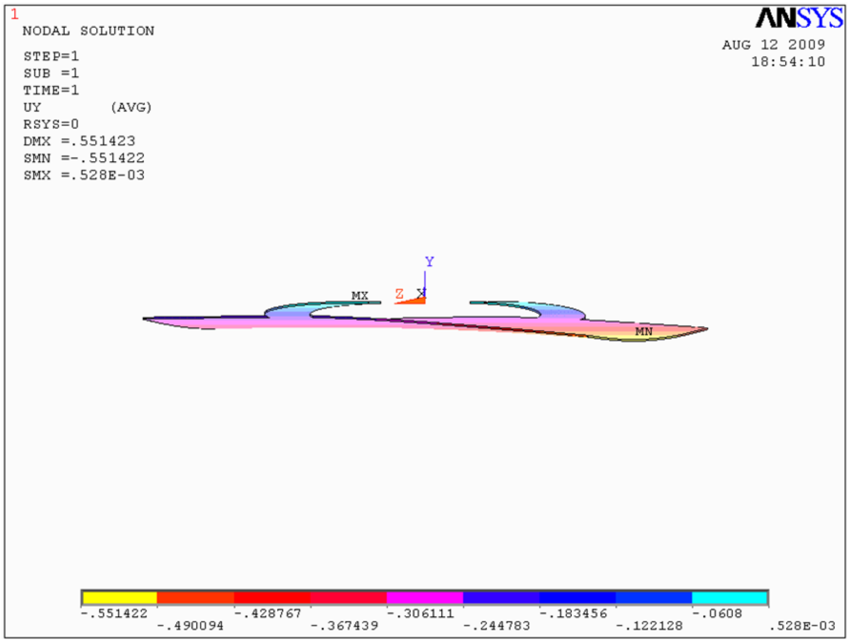

Figure 5-15: Type-2 capacitor, curvature of the mobile plate at max displacement

Nevertheless, the limited tuning range of the basic capacitor has been greatly extended by this design. Figure 5-16 shows the capacitance value as a function of the applied voltage. Again, because of fringing effects, the simulated capacitance is higher than the theoretical predictions at low voltages. As the voltage is increased, the top plate develops more curvature and the simulated capacitance falls short of the theoretical values.

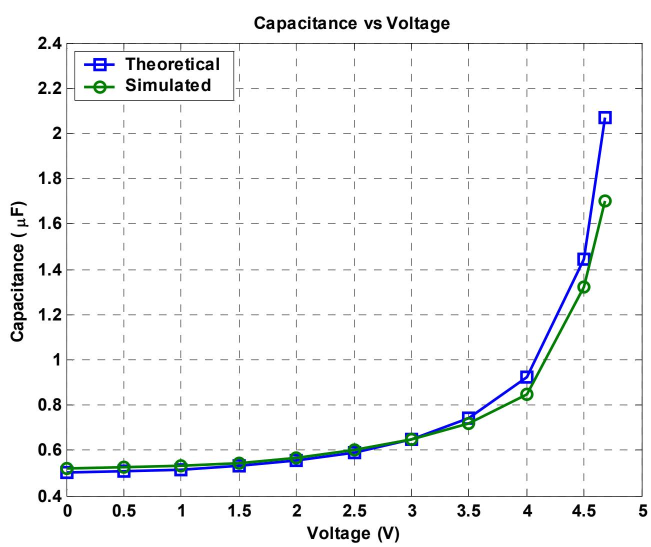

Figure 5-16: Type-2 capacitor, capacitance vs. voltage

What stands out in Figure 5-16 is the steep non-linear tuning curve of the capacitor. To have a better idea of the non-linear relationship between capacitance and displacement, Figure 5-17 shows the non-linear curve of capacitance versus displacement. It is observed that for larger displacements, the capacitance increases with bigger steps. When it comes to tuning the capacitor, the non-linear resolution of this method makes some capacitance values intangible.

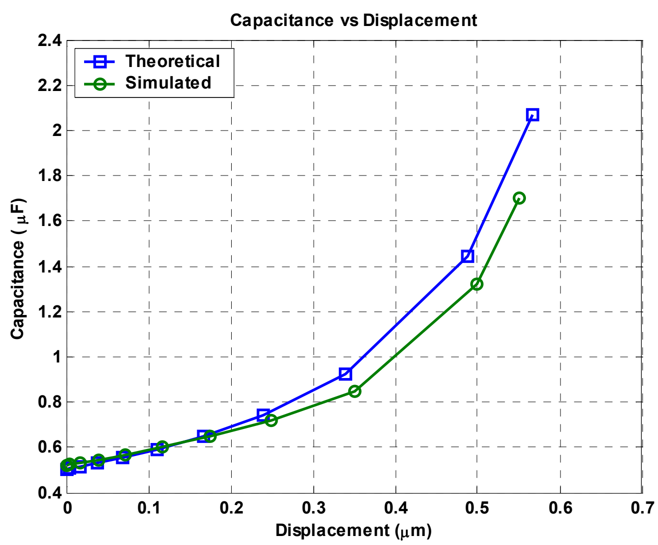

Figure 5-17: Type-2 capacitor, capacitance vs. displacement

5.4 Type-3 High Q Extended Tuning Range Capacitor

Now that the tuning range of the Type-2 capacitor has been simulated, the design can be improved for a higher quality factor.

The quality factor of a capacitor (Q) is a dimensionless quantity that is equal to the capacitor's reactance divided by its series resistance. The quality factor is proportional to the inverse of the amount of energy dissipated in the capacitor, and can be calculated according to Equation (7).

$$Q = \frac{X_C}{R} = \frac{1}{2\pi fRC} \tag{7}$$

Here R is the equivalent series resistance (ESR) of the capacitor, and is proportional to material and dimensions of the fabricated structure. In the case of a variable capacitor, it is inevitable that the quality factor will degrade as the capacitance increases. In such cases, the quality factor for the lowest capacitance value is recorded.

With frequency and capacitance as input constants, the only variable that can affect the quality factor is the equivalent series resistance (ESR). The series resistance can be calculated for a given structure according to Equation (8).

$$R = \frac{\rho l}{A} = \frac{\rho}{h}\frac{l}{w} \tag{8}$$

In Equation (8), ρ is the resistivity in Ohm-meter, l is the length, A is the cross section area, w is the width, and h is the thickness of a given structure. The term ρ/h is called sheet resistance and has a unit of Ω/sq. To have a higher Q, the series resistance should be minimized. Table 2 on page 4, provides the sheet resistance for each of the polysilicon layers. Therefore, according to Equation (8), the series resistance of the structure, is only dependent on its width and length.

Figure 5-18 shows the RF signal path through the Type-2 extended tuning range capacitor. Here the design is expanded by two conductors to include connections between the RF electrodes and the RF pads. For the mobile plate, the RF signal travel through one of the suspensions. In other words, the suspension acts as the conductor for the input RF signal to the mobile plate. The bottom plates however, require a conductor to take the RF signal from the Poly1 layer of the fixed plate to the output pad. Although separate RF pads are used for each plate, Figure 5-18 shows one pad for graphical simplicity. Each conductor contributes to the equivalent series resistance of the capacitor.

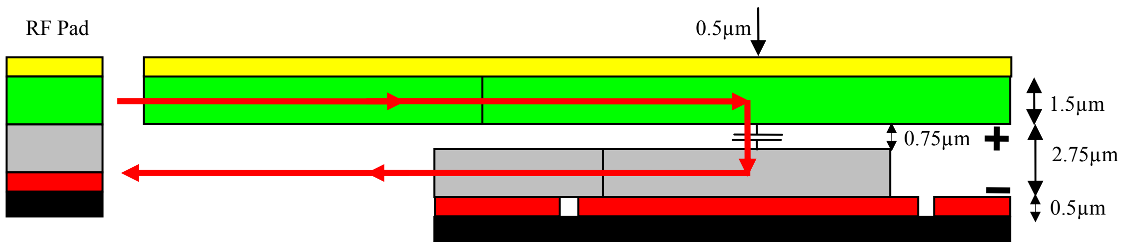

Figure 5-18: Type-3 capacitor, RF signal path

As mentioned before, metal can be deposited on top of the Poly2 layer in the PolyMUMPs process. Therefore, by adding metal on top of the mobile plate and its corresponding conductor the series resistance can be significantly reduced. However, the fixed bottom plate cannot have any metal and therefore, together with its conductor, introduces the most loss in the design. To reduce resistance in the bottom conductor to a degree, a Poly0 layer is put in parallel to the Poly1 layer. The effective parallel resistance of the layers will be less than that of each individual layer.

Moreover, the dimensions of the RF conductors can be adjusted for optimum quality factor. According to Equation (8), the ratio of length over width of the conductor can reduce the equivalent series resistance of the structure. Therefore, the bottom conductor was designed to have a length over width ratio of 0.5. The length over width ratio of the top conductor cannot be optimized for quality factor, because of the opposing requirements for the equivalent stiffness of the suspension beams. However, by depositing metal on top of the suspensions, the series resistance is significantly reduced and can be ignored in practice. Table 5 summarizes the dimensions of the Type-3 high Q extended tuning range capacitor.

Table 5: Parameters of the Type-3 capacitor

Parameter	**μm**
Length of actuation electrodes	294
Width of actuation electrodes	437
Actuation gap	2.75
Length of RF plates	147
Width of RF plates	290
RF gap	0.75
Radius of curvature for suspensions	150
Width of suspensions	40

Based on the design parameters, the equivalent series resistance of the structure is calculated to be 3.75Ω. Therefore, the quality factor is 85 at 1GHz or 50 at 1.7GHz. Naturally, as the capacitance increases with voltage, the quality factor degrades because of the existing inverse relationship. Moreover as the top plate moves down, due to the stretch in the structure, the series resistance increases and further reduces the quality factor.

The layout of the Type-3 capacitor was prepared in Cadence, and is captured in Figure 5-19. All design rules of the PolyMUMPs process have been considered and the Design Rule Check (DRC) test was successful.

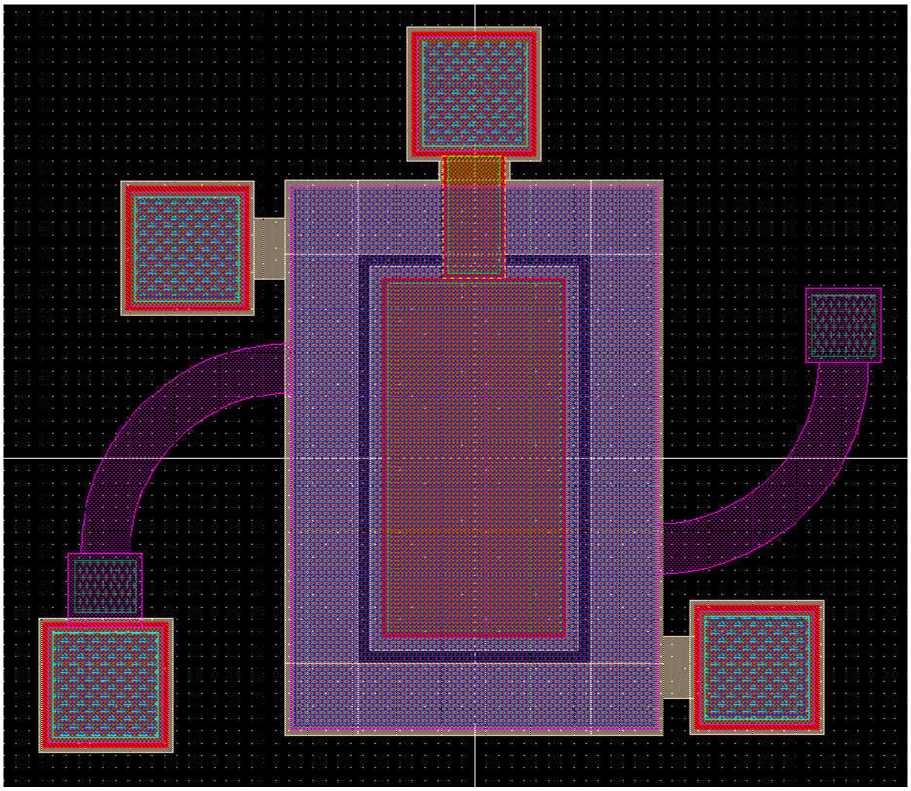

Figure 5-19: Type-3 capacitor, layout

6 Results and Discussions

The target performance characteristics were compared against the characteristics of the Type-3 capacitor. The designed capacitor has a nominal capacitance of 0.5pF. This value was chosen to consider the minimum required capacitance of 0.8pF for the high band, and to minimize the aspect ratio of the design for the purpose of simulation. The same design can be expanded to higher capacitance values for the low band of interest.

The tuning range of the designed capacitance is around 325%, which is close to the ideal value of 400%. Thus, the variable capacitance is this design can be tuned from 0.5 to 1.7pF.

The quality factor of the capacitor is calculated based on its dimensions given in Table 5. The ESR including the suspension beams is 3.75Ω. Therefore, the quality factor for no actuation voltage is 85 at 1GHz and 50 at 1.7GHz. In other words, the quality factor of the Type-3 capacitor meets the target performance.

The design was based on a maximum drive voltage of 5V, which is the typical maximum in electronic circuits. However, a limited voltage entails larger actuation area and requires an increase in the size of the capacitor accordingly. In addition, low actuation voltages lead to less robust mechanical characteristics, often manifested as higher sensitivity to vibration. An alternative solution is the use of voltage boosting circuits. Charge pumps have been successfully used to boost the on board voltage in electronic circuits to 40V. Of course, the complexity of adding the charge pump circuit to the design would be the major downside.

Table 6 summarizes the characteristics of the designed capacitor in comparison to the target performance.

Table 6: Target performance vs. characteristics of the Type-3 capacitor

Parameter	Target	Simulated
Frequency Range	1.7 – 2.5 GHz	1.7 – 2.5 GHz
Nominal Capacitance	0.8 – 3.2 pF	0.52 – 1.7 pF
Tuning Range	400%	325%
Quality Factor	Above 50	50

In conclusion, the design of a variable capacitor using the MEMS technology is highly dependent on the fabrication technology. Most of the design characteristics are dictated by the material and design rules of fabrication. Once a particular fabrication process is chosen, there are only a few parameters that can be changed to improve the characteristics of the design at hand.

As the fabrication technologies evolve, higher quality and performance measures are expected form fabricated devices.

7 Conclusion

This project presented an improved design of a wide range high Q variable capacitor using MEMS fabrication techniques. By identifying a target performance based on typical characteristics of an RF capacitor, the scope of the design was established. A brief research in MEMS fabrication techniques revealed that the popular PolyMUMPs surface micromachining process has been extensively used for similar applications. This process was chosen as the fabrication technique for the design.

Next, the design of a variable capacitor was studied by evaluating the tuning mechanism. Different tuning elements were compared in terms of their potential to achieve the target performance. The spacing between the plates was chosen as the tuning mechanism based on its potential for achieving high tuning ranges. However, simulating a basic model showed that this design is limited in tuning range because of the pull-in effect.

To extend the tuning range of the basic design, the actuation electrodes were separated from the RF electrodes. Two different implementations of this technique were presented and compared. Moreover, the extended tuning range design was enhanced to achieve the high quality factor required in RF applications. Finally, an improved design was introduced, showing characteristics that met the target performance. The layout of the final design was prepared in Cadence and will be sent to MEMSCAP for fabrication using the PolyMUMPs process.

With the successful fabrication of the presented design, RF applications can immensely benefit by reducing their size and dynamically changing their characteristics. An important example of such applications is RF matching circuits.

8 References

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9 Appendices: Simulation Code

Appendix A: Basic Capacitor, Straight Beams

```
/batch,list
/prep7, Basic capacitor straight beams

et,1,123                          ! PLANE123 element for beam region
et,2,123                          ! Temporary element for air region
emunit,epzro,8.854e-6             ! Free-space permittivity, µMKSV units
mp,perx,2,1                       ! Relative permittivity for air

bl=230                            ! Beam length (µm)
poly2=1.5                         ! Beam height
bw=210
cl=105
cw=20
offset=0.5
offset2=1
offset3=20
poly1=2
poly0=0.5
pl=10
pw=10

gap=0.75                  ! Air gap
vltg=1.25                 ! Applied voltage

!  ------------------- Beam ----------------------
Block,-bl/2,bl/2,0,poly2,-bw/2,bw/2      ! Create model
Block,-cl-bl/2,-bl/2,0,poly2,-cw/2-bw/6,cw/2-bw/6
Block,bl/2,bl/2+cl,0,poly2,bw/6-cw/2,bw/6+cw/2

!  -------------------- Poly1 --------------------
Block,-bl/2,bl/2,-gap-poly1,-gap,-bw/2,bw/2
!  -------------------- Air ----------------------
Block,-offset3-bl/2,bl/2+offset3,-gap-poly1,0,-offset3-bw/2,bw/2+offset3
vovlap,all

vsel,s,volu,,6
vsel,a,volu,,7
vsel,a,volu,,8
vatt,1,,1

vsel,s,volu,,9
```

```
cm,air,volu
aslv,s
asel,r,loc,y,-gap
cm,floor,area
vatt,2,,2

allsel,all
vsel,s,volu,,6
vsel,a,volu,,7
vsel,a,volu,,8
smrtsiz,2
vmesh,all

allsel,all
vsel,s,volu,,9
aslv
lsla
lsel,r,loc,y,-(gap+poly1)/2
lesize,all,0.75,,,,,,0
smrtsiz,2
mshape,1,3D
mshkey,0
vmesh,all

allsel,all
nsel,s,loc,y,0
nsel,r,loc,x,-bl/2,bl/2
nsel,r,loc,z,-bw/2,bw/2
cm,cond1,node
d,all,volt,vltg

allsel,all
nsel,s,loc,y,-gap
nsel,r,loc,x,-bl/2,bl/2
nsel,r,loc,z,-bw/2,bw/2
cm,cond2,node
d,all,volt,0

allsel,all
et,1,0                      ! Set structure to null element Type
physics,write,ELECTROS      ! Write electrostatic physics file
physics,clear               ! Clear Physics

et,1,92
et,2,0
```

```
mp,ex,1,170e3                  ! Set Modulus  μN/(μm)**2
mp,nuxy,1,0.34
mp,dens,1,2.329e-15            ! kg/(um)^3

allsel,all                     ! Fix the beams
asel,s,loc,y,poly2/2
asel,r,loc,z,bw/6
asel,a,loc,z,-bw/6
asel,r,loc,x,+cl+bl/2
asel,a,loc,x,-cl-bl/2
da,all,ux,0
da,all,uy,0
da,all,uz,0

allsel,all
finish
physics,write,STRUCTURE     ! Write structural physics file


ESSOLV,'ELECTROS','STRUCTURE',3,0,'air',’floor’,,,10  ! Solve coupled-field
problem

finish

physics,read,ELECTROS       ! Read electrostatic physics file
/post1
set,last                    ! Retrieve results
esel,s,mat,,2               ! Select air elements
etable,fx,fmag,x            ! Retrieve electrostatic forces
etable,fy,fmag,y
etable,fz,fmag,z
ssum                        ! Sum forces
finish

/solu
cmatrix,1,'cond',2,0        ! Compute capacitance matrix coefficients
finish
```

Appendix B: Basic Capacitor, Circular Beams

```
/batch,list
/prep7, Basic capacitor circular beams

et,1,123                    ! PLANE123 element for beam region
et,2,123                    ! Temporary element for air region
emunit,epzro,8.854e-6       ! Free-space permittivity, µMKSV units
mp,perx,2,1                 ! Relative permittivity for air

bl=230                      ! Beam length (µm)
poly2=1.5                   ! Beam height
bw=210
cw=20
offset=0.5
offset2=1
offset3=20
poly1=2
poly0=0.5
pl=10
pw=10
r=78

gap=0.75              ! Air gap
vltg=1.25             ! Applied voltage

!  ------------------- Beam ----------------------
k,1,-bl/2,poly2,-cw/2-bw/6
k,2,-r-cw/2-bl/2,poly2,r-bw/6
k,3,-bl/2,poly2,r-bw/6
k,4,-bl/2,poly2,cw/2-bw/6
k,5,-r+cw/2-bl/2,poly2,r-bw/6
k,6,bl/2,poly2,cw/2+bw/6
k,7,r+cw/2+bl/2,poly2,-r+bw/6
k,8,bl/2,poly2,-r+bw/6
k,9,bl/2,poly2,-cw/2+bw/6
k,10,r-cw/2+bl/2,poly2,-r+bw/6

LARC,1,2,3,r+cw/2
LARC,4,5,3,r-cw/2
l,2,5
l,1,4
al,1,2,3,4

LARC,6,7,8,r+cw/2
```

```
LARC,9,10,8,r-cw/2
l,6,9
l,7,10
al,5,6,7,8
VEXT,1,,,0,-poly2,0,,,,
VEXT,2,,,0,-poly2,0,,,,

Block,-bl/2,bl/2,0,poly2,-bw/2,bw/2      ! Create model

!  -------------------- Poly0 --------------------
Block,-bl/2,bl/2,-gap-poly1,-gap,-bw/2,bw/2
!  -------------------- Air ----------------------
Block,-offset3-bl/2,bl/2+offset3,-gap-poly1,0,-offset3-bw/2,bw/2+offset3
vovlap,all

vsel,s,volu,,6
vsel,a,volu,,7
vsel,a,volu,,8
vatt,1,,1

vsel,s,volu,,9
cm,air,volu
vatt,2,,2

allsel,all
vsel,s,volu,,6
vsel,a,volu,,7
vsel,a,volu,,8
smrtsiz,2
vmesh,all

allsel,all
vsel,s,volu,,9
aslv
lsla
lsel,r,loc,y,-(gap+poly1)/2
lesize,all,0.75,,,,,,0
smrtsiz,2
mshape,1,3D
mshkey,0
vmesh,all

allsel,all
nsel,s,loc,y,0
nsel,r,loc,x,-bl/2,bl/2
nsel,r,loc,z,-bw/2,bw/2
```

```
cm,cond1,node
d,all,volt,vltg

allsel,all
nsel,s,loc,y,-gap
nsel,r,loc,x,-bl/2,bl/2
nsel,r,loc,z,-bw/2,bw/2
cm,cond2,node
d,all,volt,0

allsel,all
et,1,0                          ! Set structure to null element Type
physics,write,ELECTROS          ! Write electrostatic physics file
physics,clear                   ! Clear Physics

et,1,92
et,2,0

mp,ex,1,170e3                   ! Set Modulus  μN/(μm)**2
mp,nuxy,1,0.34
mp,dens,1,2.329e-15             ! kg/(um)^3

allsel,all
asel,s,loc,y,poly2/2
asel,r,loc,x,bl/2+r
asel,a,loc,x,-bl/2-r
da,all,ux,0
da,all,uy,0
da,all,uz,0

allsel,all
finish
physics,write,STRUCTURE         ! Write structural physics file


ESSOLV,'ELECTROS','STRUCTURE',3,0,'air',,,,10  ! Solve coupled-field
problem

finish

physics,read,ELECTROS           ! Read electrostatic physics file
/post1
set,last                        ! Retrieve results
esel,s,mat,,2                   ! Select air elements
etable,fx,fmag,x                ! Retrieve electrostatic forces
etable,fy,fmag,y
```

```
etable,fz,fmag,z
ssum                    ! Sum forces
finish

/solu
cmatrix,1,'cond',2,0    ! Compute capacitance matrix coefficients
finish
```

Appendix C: Type-2 Extended Tuning Range Capacitor Design

```
/batch,list
/prep7, Type-2 Extended Tuning Range Capacitor

et,1,123                    ! PLANE123 element for beam region
et,2,123                    ! Temporary element for air region
emunit,epzro,8.854e-6       ! Free-space permittivity, µMKSV units
mp,perx,2,1                 ! Relative permittivity for air

bl=437                      ! Beam length (µm)
poly2=1.5                   ! Beam height
bw=294
cl=180
cw=40
offset=10
offset2=10
offset3=10
offsetp=0
poly1=2
poly0=0.5
pw=147
pl=290
r=150

gap=0.75                    ! Air gap
vltg=3.25                   ! Applied voltage

! ------------------- Beam ----------------------
k,1,-bl/2,poly2,-cw/2-bw/6
k,2,-r-cw/2-bl/2,poly2,r-bw/6
k,3,-bl/2,poly2,r-bw/6
k,4,-bl/2,poly2,cw/2-bw/6
k,5,-r+cw/2-bl/2,poly2,r-bw/6
k,6,bl/2,poly2,cw/2+bw/6
k,7,r+cw/2+bl/2,poly2,-r+bw/6
k,8,bl/2,poly2,-r+bw/6
k,9,bl/2,poly2,-cw/2+bw/6
k,10,r-cw/2+bl/2,poly2,-r+bw/6

LARC,1,2,3,r+cw/2
LARC,4,5,3,r-cw/2
l,2,5
l,1,4
al,1,2,3,4
```

```
LARC,6,7,8,r+cw/2
LARC,9,10,8,r-cw/2
l,6,9
l,7,10
al,5,6,7,8
VEXT,1,,,0,-poly2,0,,,,
VEXT,2,,,0,-poly2,0,,,,

Block,-bl/2,bl/2,0,poly2,-bw/2,bw/2      ! Create model
!  -------------------- Poly1 --------------------
Block,-pl/2,pl/2,-gap-poly1,-gap,-pw/2,pw/2
!  -------------------- Air ----------------------
Block,-offset3-bl/2,bl/2+offset3,-gap,0,-offset3-bw/2,offset3+bw/2
Block,-offset3-bl/2,bl/2+offset3,-gap-poly1,-gap,-offset3-bw/2,offset3+bw/2
!  -------------------- Poly0 --------------------
Block,-offset-pl/2,pl/2+offset,-gap-poly1-poly0,-gap-poly1,-offset-pw/2,pw/2+offset
Block,-offsetp-bl/2,-offset2-offset-pl/2,-gap-poly1-poly0,-gap-poly1,-offsetp-
bw/2,offsetp+bw/2
Block,pl/2+offset+offset2,offsetp+bl/2,-gap-poly1-poly0,-gap-poly1,-offsetp-
bw/2,offsetp+bw/2
Block,-offsetp-bl/2,offsetp+bl/2,-gap-poly1-poly0,-gap-
poly1,pw/2+offset+offset2,offsetp+bw/2
Block,-offsetp-bl/2,offsetp+bl/2,-gap-poly1-poly0,-gap-poly1,-offsetp-bw/2,-pw/2-offset-
offset2

VOVLAP,all

vsel,s,volu,,20
vsel,a,volu,,21
vsel,a,volu,,23
vatt,1,,1

vsel,s,volu,,24
cm,air,volu
vsel,a,volu,,25
vatt,2,,2

allsel,all
vsel,s,volu,,23
aslv
lsla
lsel,r,loc,y,poly2/2
lesize,all,0.75,,,1,1,0,0,0
smrtsiz,off
mopt,aorder,on
```

```
vmesh,all

allsel,all
vsel,s,volu,,20
vsel,a,volu,,21
smrtsiz,2
vmesh,all


allsel,all
vsel,s,volu,,24
aslv
lsla
lsel,r,loc,y,-gap/2
lesize,all,0.75,,,1,1,0,0,0
vsel,a,volu,,25
aslv
lsla
lsel,r,loc,y,-gap-poly1/2
lesize,all,0.5,,,1,1,0,0,0
smrtsiz,2
mshape,1,3D
mshkey,0
vmesh,all

allsel,all
nsel,s,loc,y,0
nsel,r,loc,x,-bl/2,bl/2
nsel,r,loc,z,-bw/2,bw/2
cm,cond1,node
d,all,volt,vltg

allsel,all
vsel,s,volu,,12
vsel,a,volu,,13
vsel,a,volu,,14
vsel,a,volu,,15
vsel,a,volu,,16
vsel,a,volu,,17
vsel,a,volu,,18
vsel,a,volu,,19
aslv
asel,r,loc,y,-gap-poly1
nsla,s,1
d,all,volt,0
```

```
allsel,all
vsel,s,volu,,4
aslv
asel,r,loc,y,-gap
nsla,s,1
cm,cond2,node

allsel,all
et,1,0                          ! Set structure to null element Type
physics,write,ELECTROS         ! Write electrostatic physics file
physics,clear                   ! Clear Physics

et,1,92
et,2,0

mp,ex,1,158e3                   ! Set Modulus  µN/(µm)**2
mp,nuxy,1,0.22
mp,dens,1,2.329e-15             ! kg/(um)^3

allsel,all
asel,s,loc,y,poly2/2
asel,r,loc,x,bl/2+r
asel,a,loc,x,-bl/2-r
da,all,ux,0
da,all,uy,0
da,all,uz,0

allsel,all
finish
physics,write,STRUCTURE         ! Write structural physics file


ESSOLV,'ELECTROS','STRUCTURE',3,0,'air',,,,10  ! Solve coupled-field

vltg=4.5
ESSOLV,'ELECTROS','STRUCTURE',3,0,'air',,,,10,,2  ! Solve coupled-field

finish

physics,read,ELECTROS           ! Read electrostatic physics file
/post1
set,last                        ! Retrieve results
esel,s,mat,,2                   ! Select air elements
etable,fx,fmag,x                ! Retrieve electrostatic forces
etable,fy,fmag,y
etable,fz,fmag,z
```

```
ssum                          ! Sum forces
finish

/solu
cmatrix,1,'cond',2,0          ! Compute capacitance matrix coefficients
finish
```