IN-PLACE BONDING OF III-V SEMICONDUCTOR HETEROSTRUCTURES

by

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Abstract

Elastically strain-relaxed GaAs/In$_{0.08}$Ga$_{0.92}$As/GaAs heterostructures on GaAs(001) substrates were fabricated. Pseudomorphic heterostructures grown by MOCVD were patterned using conventional photolithography and a sacrificial AlAs layer was removed by selective etching. As etching proceeds and the GaAs/InGaAs/GaAs structure is released from the substrate, elastic strain relaxation occurs and the strain-relaxed structures are weakly bonded in-place to the substrate. The bond between the strain-relaxed structure and the substrate was then strengthened by annealing under conditions similar to those used for whole wafer bonding of GaAs. The strain, composition and thickness of the layers were determined using high resolution X-ray diffraction and the sample surface quality was examined using atomic force microscopy. The degree of strain relaxation of the InGaAs layer is determined by the relative thickness of the GaAs and InGaAs layers in agreement with a force balance model. The increase in the in-plane lattice parameter of the bonded GaAs/In$_{0.08}$Ga$_{0.92}$As/GaAs structures as compared to GaAs is 0.25-0.44%.

To my parents

Acknowledgments

I would like to thank the following individuals: David Lackner and Oliver Pitts for growing the samples used in this experiment, Phil Grant for teaching me how to use the AFM and Grace Li and the 4DLabs staff for their help in the 4DLabs cleanroom. Dr. Karen Kavanagh and Dr. Simon Watkins for their comments and advice regarding this work. Samantha Franks for reminding me to eat during my thesis writing days and Jennifer Godfrey for moral support and cookies. My parents, Annette and Arthur, to whom this thesis is dedicated and my sister, Megan, who introduced me to Ph.D. comics. Finally, Dr. Pat Mooney, my supervisor, who was always available when I had questions and always had helpful advice or suggestions when I was encountering problems.

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Chapter 1

Introduction

III-V semiconductor materials are compound semiconductors which contain elements from column III and column V of the periodic table, with a one-to-one ratio between the elements from each column. Silicon technology $\approx 93\%$ of the market due to the low material cost, easy insulator integration in the form of SiO_2, and higher hole mobility, which in turn leads to a lower logic circuit power consumption. However, III-V semiconductors in general possess a direct bandgap and a higher electron mobility than silicon. These advantages have led to considerable use of GaAs and other III-V materials in both high frequency electronics, such as power amplifiers in cellular phones, and photonic devices, such as light emitting diodes (LEDs)[3]. Additionally, many different III-V compounds are available, allowing a wide range of bandgap energies to be obtained by employing alloys, as demonstrated in Fig. 1.1. This extensive range of energies is particularly useful when attempting to engineer a semiconductor device which requires a specific bandgap. However, while determining which semiconductor material composition is required to obtain the necessary bandgap is simple, growing such a material of sufficient quality may be difficult. The small number of different high-quality crystalline III-V semiconductor substrates (GaAs, InP and GaSb) suitable for the epitaxial growth of such materials limits the range of heterostructures available for device applications. In an effort to expand the range of available substrate lattice parameters, there has been a substantial research effort to develop engineered substrates, which possess surface layers that have a different in-plane lattice constant than the underlying bulk semiconductor.

This research focuses on the in-place bonding method for creating engineered substrates
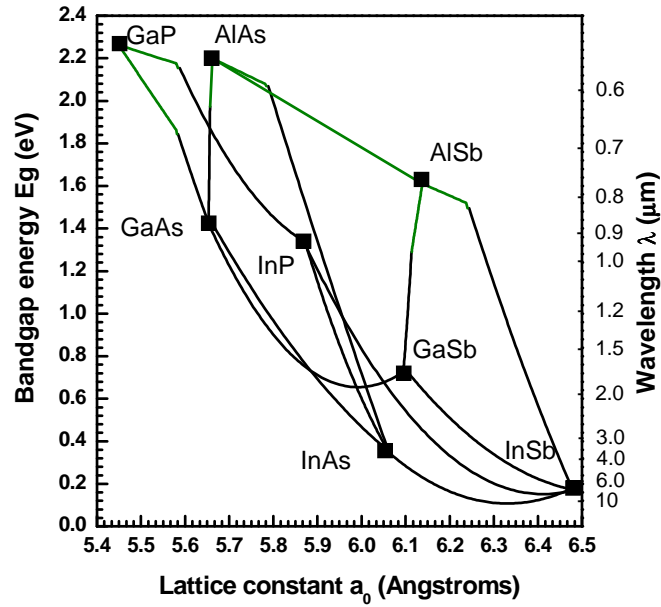
Figure 1.1: Bandgap energy and wavelength vs lattice parameter for various III-V alloys.

as first applied to III-V semiconductor materials. Chapters 2-4 are devoted to background material, dealing specifically with wafer bonding techniques, semiconductor mismatch and strain, and elastic strain relaxation. The following five chapters discuss fabrication processes, measurement methods, and results.

Chapter 2

Wafer Bonding

Wafer bonding is a process in which two wafers adhere to each other at room temperature without applying any manner of gluing layer material. This technique has been used to fabricate engineered substrates by thinning one wafer after bonding to achieve a thin layer of one material on a substrate of a different material. In general, the materials most often used in this process are semiconductor wafers, though metals, oxides and other chemical films have been bonded successfully using this method[17]. As the initial bonding is achieved at room temperature, it is weak compared to chemical bonding within solid crystals. Consequently a high temperature anneal is required to form covalent bonds at the interface before using the bonded material in device processing.

2.1   Development of Wafer Bonding

In 1969 Wallis and Pomerantz reported the bonding of silicon wafers to glass wafers at an elevated temperature under an applied electric field. While this type of bonding is classified as anodic bonding, it served as a framework for later wafer bonding work accomplished in the mid-1980s by Shimbo *et al.* for direct Si-to-Si wafer bonding[39] and by Lasky for creation of silicon-on-insulator (SOI) wafers by wafer bonding[24]. In particular, the SOI technology was initially motivated by increased resistance to undesirable side effects caused by radiation-induced electron-hole pair production[41], as devices fabricated in the silicon layer are protected from the bulk silicon wafer by a silicon dioxide insulator. However, the most notable advantages of such technology became lower device operating voltages

and higher packing density of devices. While initial work dealt specifically with silicon technology, considerable research has also been carried out on bonding III-V semiconductor materials[18, 2, 1].

Wafer bonding is accomplished by bringing two clean, smooth wafers into contact. If the wafers are sufficiently smooth, their surfaces will experience a Van der Waals force attraction at the first point of contact. From this single point, neighbouring atoms will experience a similar attraction, causing the Van der Waals bonding to propagate across the surface of the wafer as the remainder of the wafer is brought into contact. This Van der Waals force is typically induced by one of three mechanisms: the dipole-dipole force between two polar molecules, the dipole induced force between a polar and nonpolar molecule, or the dispersion force between two nonpolar molecules due to temporary dipole moments. These three attractive mechanisms are created by chemical groups called bonding species.

While the required cleaning techniques for whole wafer III-V bonding are more complicated than the corresponding procedure in silicon technology, the means of bonding cleaned wafers remains very similar. However, there exists the additional complication of arsenic desorption when bonding GaAs wafers. In this case, arsenic atoms desorb from the wafer surfaces above 700°C [18], leading to gallium rich surfaces. Consequently, any wafer bonding anneal performed at such temperatures must be carried out in an arsenic rich atmosphere.

2.2 Merits of Wafer Bonding

The refinement and use of the wafer bonding technique led to advances in two major areas: electronic devices and mechanical devices. For electronic device manufacturing, the primary advances came as a result of bonded SOI wafers, which could be cheaply and efficiently produced. These new wafers provided significant layer quality advantages over previous methods in which either amorphous silicon was grown on an oxide layer or an oxide layer was formed beneath an existing high quality silicon layer by high-energy oxygen implantation, known as separation by implanted oxygen (SIMOX)[41]. In the former case, the new silicon layer was not crystalline, and in the latter case, the implantation process resulted in an increased dislocation density. For microelectromechanical (MEMs) devices, wafer bonding was of particular importance in the development and production of semi-

conductor devices which required thin cantilevers or diaphragms. In particular, this led to pressure sensors and accelerometers of much smaller size than those designed prior to advances in wafer bonding technology.

In addition to these well established advances, wafer bonding technology has the potential to provide the means of achieving the integration of optical devices fabricated from III-V materials with silicon integrated circuit technology, providing new types of optoelectronic integrated circuits (OEICs)[41], an advance that would greatly benefit optical-fiber communications. Furthermore, wafer bonding technology may provide new material combinations or buried layers[41].

2.3 Wafer Bonding Complications

While semiconductor wafer bonding might seem like an ideal means of joining two semiconductor materials without introducing a bonding agent, there are a number of complications which may arise from improper preparation of the sample, or poor choice of bonding or annealing conditions. Unbonded interface areas are one of the most common problems in wafer bonding methods; these voids or bubbles can form during the bonding process, storage or an anneal[41]. An example of such an unbonded area is shown in Fig. 2.1. Efforts to understand and eliminate these bubbles have found the causes of their formation during bonding to include: particles on the bonding surfaces, locally rough bonding surface areas, locally low density of bonding species, and trapped air pockets. The bonding species are the specific chemical groups terminating the surface that act as a catalyst for bonding. In the first case, bubbles form as the particles prevent a good bond from forming in the locality of the particle simply by keeping the two wafer bonding surfaces apart. Larger particles result in larger bubbles. Local roughness of the bonding wafers causes bubbles as the surfaces do not lie smoothly together, in this case the bubbles may simply be pits sealed by the wafer bonding process, which creates a void at the interface. Similarly, bubbles formed during either storage or annealing are typically created by: the reaction of interface bonding species and bonding materials (notably hydrogen release, as many wafer bonding processes utilize hydrogen terminated surfaces), the dissociation of bonding groups on the bonding surface, or the outgassing from contaminants either on or within the bonding materials[41].

The above list of causes demonstrates the importance of surface quality in the wafer
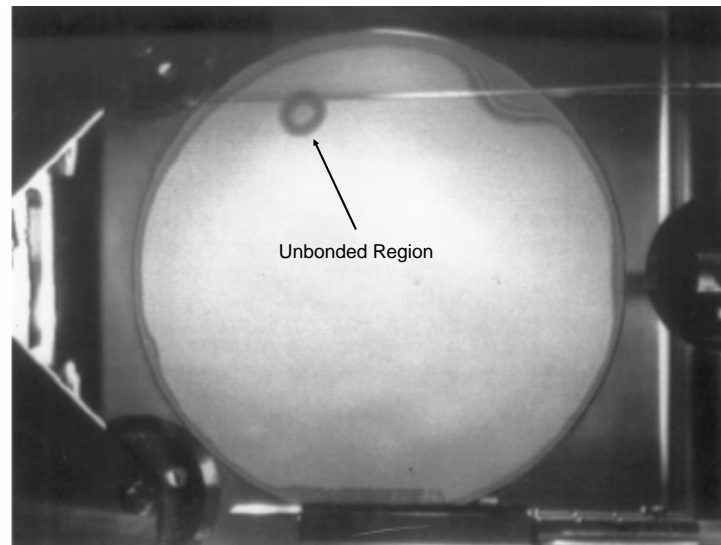
Figure 2.1: Infrared micrograph of whole wafer GaAs-GaAs bonding showing an unbonded region[2].

bonding process. Thus, the surfaces of the wafers to be bonded must possess sufficient smoothness, flatness, cleanliness and reactivity to prevent bubble formation during the bonding process. In silicon bonding this is a relatively simple process, with chemome-chanical polishing providing a sufficiently smooth surface without creating any subsurface damage[36] and a standard RCA clean to remove any surface contaminants[22]. How-ever, surface cleaning is more complicated when applied to III-V semiconductors such as GaAs, as the removal of both the Ga and As oxides must be synchronized, and a simple cleaning solution, such as the RCA clean used in silicon technology, does not exist. Fur-thermore, any wafer surface which has been exposed to air will additionally contain both carbon contaminants and absorbed water[2]. While the water can be thermally removed at low temperatures and any native oxides can be desorbed by heating up to 580°C, ther-mal cleaning cannot remove carbon contaminants completely, and furthermore, it causes increased surface roughness[42] and impurity accumulation. A number of different clean-ing mechanisms have been investigated including electron plasma cyclotron resonance[43] and atomic hydrogen cleaning[2], both of which provide a better final surface than methods similar to those used in silicon cleaning. The second method has been applied to a variety of different III-V materials successfully[1].

2.4   Wafer Bond Strength Tests

The strength of a bonded wafer pair can be defined as the work, W, per unit area associated with the mechanical separation of the pair of bonded surfaces from their original distance at contact, d_0, to infinity under adiabatic conditions as given by equation 2.1

$$W = \gamma_1 + \gamma_2 = \int_{d_0}^{\infty} F(x)dx, \tag{2.1}$$

where γ_1 and γ_2 are the surface energies per unit area of surface 1 and surface 2 at the moment of separation, x is the separation of the two wafers and $F(x)$ is the attraction force per unit area as a function of the separation of the surfaces. The standard method of measuring the surface energy of the bonded wafers is the crack-opening method[27, 41] shown in Fig. 2.2. In this case, when a separating material, such as a razor blade with thickness t_b, is in-
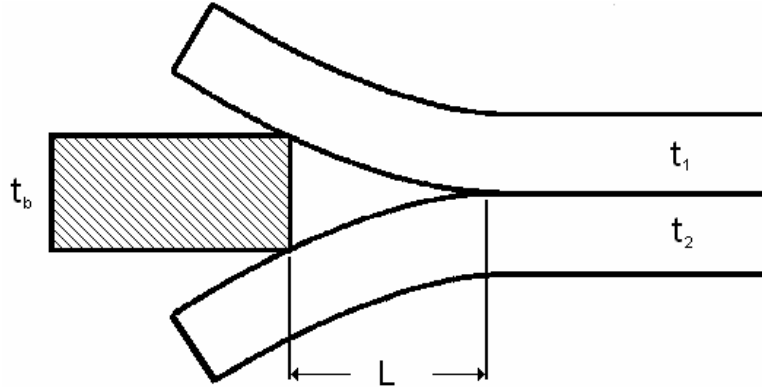
Figure 2.2: Schematic diagram of the crack-opening method of determining the surface energy of a bonded pair. The separation of the two wafers, x is equal to the thickness of the razor blade t_b at the point where the razor is contacting the wafers.

serted between the two wafers, each will bend, and generate a corresponding elastic energy, E_{Elas1} and E_{Elas2} respectively, given by

$$E_{Elasi} = \frac{E_i w t_i^2 t_b^2}{8L^3}, \tag{2.2}$$

where E_i is the Young's modulus and t_i is the the thickness of each wafer. Additionally, the insertion of the blade between the wafers introduces two new surfaces of area Lw, where w is the width of the bonded area (into the page) and L is the crack length. Thus, the total energy for the system is given by

$$E_{total} = E_{Elas1} + E_{Elas2} + (\gamma_1 + \gamma_2)Lw. \tag{2.3}$$

In the equilibrium case where the first derivative of E_{total} with respect to L is zero, the surface energy, or bond strength, can be found by

$$W = \gamma_1 + \gamma_2 = -\frac{3t_b^2 E_1 t_1^3 E_2 t_2^3}{8L^4(E_1 t_1^3 + E_2 t_2^3)} \tag{2.4}$$

for the case of differing materials and thicknesses in the bonded pair[41]. This method remains one of the primary methods of determining the bond strength following wafer bonding. It has been used in whole wafer GaAs/GaAs bonding and demonstrates that such bonded interfaces can achieve bond energies of ~0.7-0.8 J/m², which is close to that of the bulk material[18]. However, this bond testing method is limited strictly to cases where a razor blade or other narrow object may be easily inserted between the bonded layers.

2.5 Summary

Wafer bonding provides a means of obtaining an interface between different materials. This method avoids the introduction of dislocations and the materials involved may not experience strain as a result of the bonding as the bonding can occur at room temperature in some cases. However, this method is limited in possible layer structures to those which may be fabricated on whole wafers and unbonded areas may be present if bonding conditions are not ideal. The traditional method of measuring the bond strength of a wafer bond involves the use of a razor to separate the bonded wafers, with the bond strength defined as the sum of the two surface energies of the wafers.

Chapter 3

Semiconductor Mismatch, Strain & Defects

When growing semiconductor layers of different lattice parameter than that of the substrate, their quality, and thus their usefulness in electronic materials is limited by their critical thickness. The critical thickness of a material is defined as the point at which misfit dislocations within the crystal lattice of the epitaxial layer begin to propagate throughout the lattice. Misfit dislocations form to accommodate the mismatch strain created by a heterostructure containing layers of different lattice parameters.

3.1 Mismatch Strain

Because the lattice constant of InAs is larger than that of GaAs, the alloy $In_xGa_{1-x}As$ has a larger lattice constant than GaAs and a smaller lattice constant than InAs. This lattice constant can be estimated by use of Vegard's law

$$a_{InGaAs} \approx x a_{InAs} + (1-x) a_{GaAs}, \tag{3.1}$$

where $a_{GaAs} = 0.5653$ nm, and $a_{InAs} = 0.6062$ nm, the lattice constants. This law assumes a linear relation, which for InGaAs, is a good approximation. Consequently, when a layer of $In_xGa_{1-x}As$ is grown on a GaAs wafer, there is a lattice mismatch dependent on x, the

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InAs fraction of that layer. This lattice mismatch produces a strain in the plane of the layer

$$\varepsilon_0 = \frac{a_s - a_l}{a_l}, \tag{3.2}$$

This can be rewritten in terms of the Indium composition by substituting equation 3.1 into 3.2 yielding

$$\varepsilon_0(x) = \frac{a_{GaAs} - (x a_{InAs} + (1-x)a_{GaAs})}{(x a_{InAs} + (1-x)a_{GaAs})} = \frac{x(a_{GaAs} - a_{InAs})}{a_{GaAs} - x(a_{GaAs} - a_{InAs})}. \tag{3.3}$$

When inserting the lattice constants of GaAs and InAs, this yields a mismatch strain of $\varepsilon_0 \approx -0.071x$.

The layer stress in the plane of the interface can be written as[12]

$$\sigma = 2\mu\varepsilon_0 \frac{1+\nu}{1-\nu} \tag{3.4}$$

and the strain normal to the interface is given by

$$\varepsilon = \frac{-2\nu\varepsilon_0}{1-\nu} \tag{3.5}$$

where the elastic shear modulus, $\mu = 32.6$ GPa, and Poisson's ratio, $\nu = 0.31$, for GaAs[40]. The elastic energy per unit of interface area produced by this mismatch strain is

$$E = \frac{2\mu h(1+\nu)\varepsilon_0^2}{1-\nu} \tag{3.6}$$

where h is the thickness of the strained layer[12]. Equations 3.3 and 3.6 collectively allow for the calculation of stored elastic energy within an In$_x$Ga$_{1-x}$As layer for a given x. When the stored energy exceeds a critical value, the critical thickness, the energy is relaxed by the formation of misfit dislocations.

3.2 Dislocations in III-V Semiconductors

A dislocation is a line defect found in crystalline materials. Figure 3.1 demonstrates the two basic types of dislocation: edge dislocations and screw dislocations. In the image each vertex can be considered as an atom in the crystal lattice. Edge dislocations occur when a half plane of atoms is missing among full planes, leaving the edge of the remaining half

plane unbonded to atoms in one direction and distorting the crystal lattice as a result. An example of an edge dislocation is shown in Fig. 3.1(a). This image represents a single plane of a material containing an edge dislocation line that lies perpendicular to the page. Screw dislocations occur where a portion of a bulk crystal is offset by one or more atoms as shown in fig. 3.1(b). The screw dislocation line is perpendicular to the face of the crystal, and parallel to the Burgers vector. However, this is a simplistic view of dislocations and those found in semiconductors often contain components of both edge and screw dislocations. Consequently a system of identifying different types of dislocations is necessary, and this is accomplished by the Burgers vector and Burgers circuit[19].

(a) Edge Dislocation   (b) Screw Dislocation
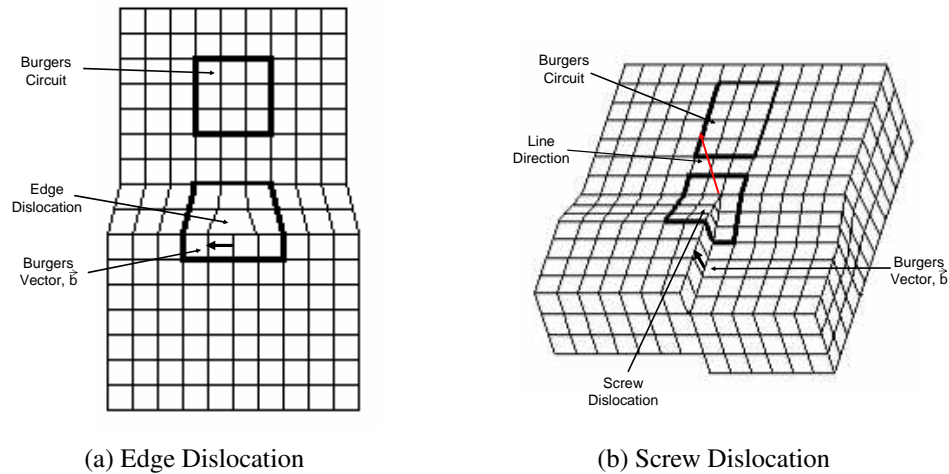
Figure 3.1: Schematic diagram of an edge dislocation and a screw dislocation in a bulk crystal. The respective Burgers circuits and vectors are indicated for each dislocation.

The Burgers circuit is simply a closed atom to atom path taken in a crystal containing no dislocations, as shown in Fig. 3.1. If the same path taken in a crystal containing dislocations does not close, then the path encloses one or more dislocations. The resulting vector that is required to close the loop is called the Burgers vector, $\vec{b}$. For the basic dislocation types, the Burgers vector is normal to the dislocation line for edge dislocations, and parallel to the dislocation line for screw dislocations. It is of particular importance to note that the Burgers vector of a dislocation is always the same, independent of the location of the dislocation within the medium.

Once a dislocation is contained within a crystal, it may move in two primary ways: glide

and climb. Glide occurs along slip planes which are planes within the crystal along which plastic deformation is most likely to occur, and which are generally planes with the highest density of atoms. The direction of the glide is typically in the direction where the atoms are most closely spaced. Climb occurs when a dislocation moves out of its current slip plane and into another slip plane. Climb is primarily driven by vacancies in the crystal lattice and, consequently, occurs more rapidly at higher temperatures. Climb does not usually occur at the temperatures typically used for growth of InGaAs epitaxial layers.

In all diamond or zinc blende crystal structures, the lowest energy slip planes are the {111} planes, and consequently, on <001> oriented substrates the slip planes intersect the interface in <110> lines, which provides the corresponding line directions of misfit dislocations in such structures, as shown in Fig. 3.2. The Burgers vectors of such dislocations is the slip direction and these can be along the line or in the glide plane at 60° to the line direction. However, in the first case, the misfit dislocation is a screw dislocation and relieves no misfit strain. The component of the 60° dislocations perpendicular to the line direction contributes to strain relaxation. Total strain relaxation depends on the number of dislocations per unit length perpendicular to the direction of strain relaxation i.e. those perpendicular to the <110> lines. The 60° Burgers vector is $\vec{b} = \frac{a_l(1\bar{1}0)}{2}$ in a zinc blende crystal, and has a length along the interface perpendicular to the line of $b_\perp = \frac{a_l}{2\sqrt{2}}$ [12]. For an InAs alloy fraction 0.08 the length of the Burgers vector, $\vec{b}$, is 0.20 nm.

3.3 Critical Thickness Behaviour

Initial work on the critical thickness of semiconductor materials was published by Matthews and Blakeslee[29, 30, 31], who determined a mathematical relation for the critical thickness by examining the forces originating from both the misfit strain, F_ε, and the tension of the dislocation line, F_l. For cases where the elastic constants of two layers are equal and isotropic, then

$$F_\varepsilon = \frac{2\mu(1+\nu)}{(1+\nu)} bh\varepsilon \, cos \, \lambda \tag{3.7}$$

where μ is the shear modulus of the strained layer in question, ν is the Poisson ratio, h is the thickness of the strained layer and λ is the angle between the slip direction and the direction perpendicular to the line of intersection of the slip plane and the interface.
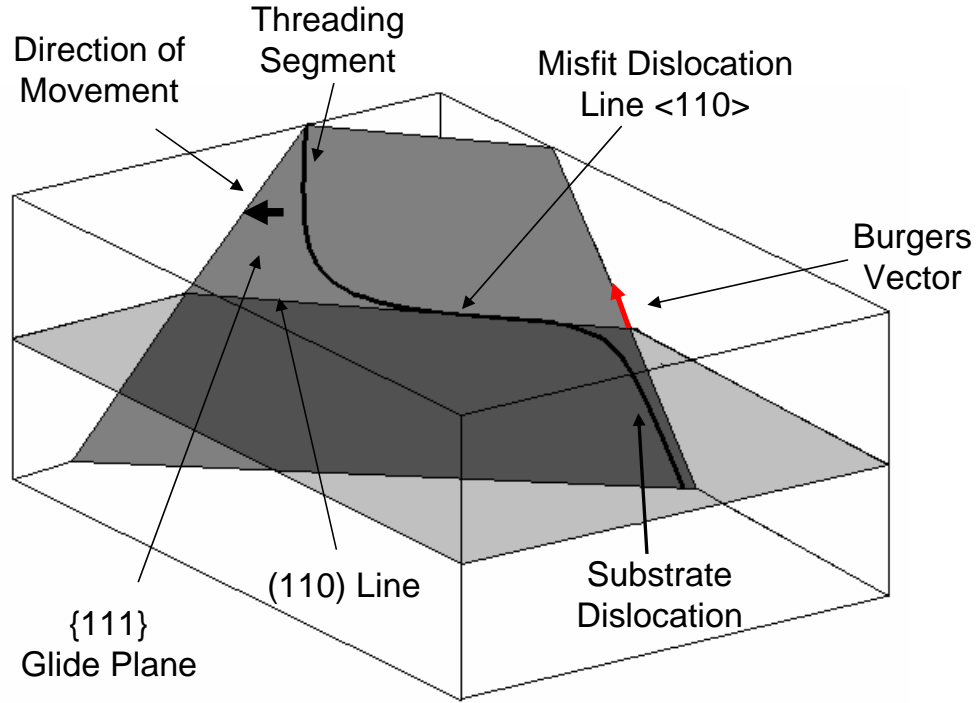
Figure 3.2: The orientation of the glide plane in GaAs/In$_x$Ga$_{1-x}$As structures. Misfit dislocation and corresponding Burgers vector are shown. The (110) line is the intersection of the 111 glide plane with the (001) plane.

Similarly, the tension due to the dislocation line is

$$F_l = \frac{\mu b^2}{4\pi(1-\nu)}((1-\nu\,cos^2\,\alpha)(ln\,\frac{h}{b}+1))$$
(3.8)

where α is the angle between the dislocation line and its Burgers vector.

The critical thickness, h_c is defined as the point at which the threading segment of a dislocation begins to glide as shown in fig. 3.2, and occurs when the misfit strain force, F_ε, is larger than the dislocation line tension force, F_l. And thus, at the critical thickness, $F_{\varepsilon_{max}} = F_l$, and the layer thickness is given by

$$h_c = \frac{b}{8\pi\varepsilon}\frac{(1-\nu\,cos^2\,\alpha)}{(1+\nu)\,cos\,\lambda}(ln\frac{h_c}{b}+1)$$
(3.9)

In the case of GaAs-In$_x$Ga$_{1-x}$As, $\nu = 0.31$, $b = a_l/\sqrt{2}$, $cos(\lambda) = 1/2$ and $cos(\alpha) = 1/2$[40]. For the samples grown for these experiments, the InAs alloy composition, x, is 0.08 resulting in a critical thickness, h_c, of 22 nm.

Figure 3.3 shows the critical thickness of In$_x$Ga$_{1-x}$As for varying Indium concentration calculated from eq. 3.9. The experimental critical thicknesses (diamonds) were determined
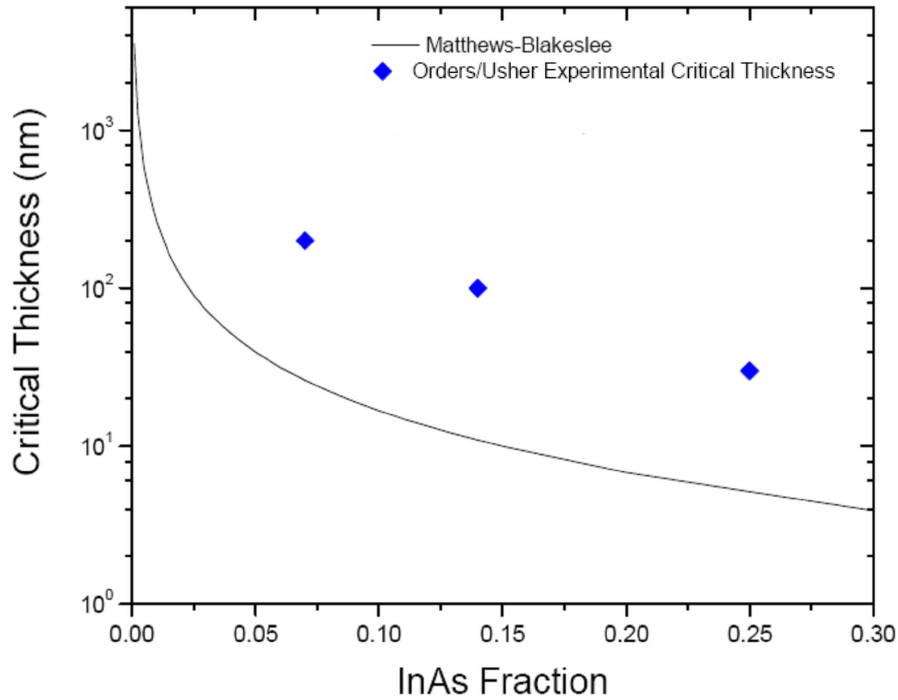
Figure 3.3: Plot of Matthews-Blakeslee theory (equation 3.9) and experimental data points for the critical thickness of various InAs % samples as measured by x-ray diffraction are also shown (diamond)[35].

by measuring the perpendicular lattice spacing by x-ray diffraction and determining the point at which the lattice spacing began to shift, indicating the relaxation of strain[35]. Layers with thicknesses between the points and line may experience movement of dislocations within the material, however the misfit dislocation density is not sufficient to relieve enough strain to observer a detectible shift in the lattice parameter.

However, Freund[12] lists specific limitations of the Matthews-Blakeslee Criterion,

namely that it:

1. Provides the point at which any threading segment may advance, and thus, relaxation may not be detected at this point unless the method of observation provides sufficient resolution to detect the change in strain caused by a single dislocation. Therefore large area measurement techniques such as X-ray diffraction (XRD) will not detect the relaxation caused by a single dislocation as they measure average strain over areas on the order of a square millimeter.

2. Assumes a dislocation exists, and thus, neglects the nucleation of new dislocations. In the case of GaAs, the initial wafers contain $\approx 2 \times 10^3$ dislocations/cm^2.

3. Only indicates the tendency for a threading segment to move, but does not specify the manner of dislocation movement. This means a kinetic model of glide is required to take the movement of dislocations into account when considering critical thickness and relaxation.

4. Examines the case of only a single dislocation in a uniform layer, and assumes that no other dislocations are present.

5. Neglects entirely the effects of glide resistance, surface or interface energy, and surface ledge creation resistance[28, 6], since the criterion is based solely on elastic continuum concepts.

From #1 it is not surprising that the experimental critical thickness as measured by x-ray diffraction is greater than that predicted by the mechanical equilibrium model of Matthews-Blakeslee. This also indicates that although samples grown with thickness below the experimental data of the Orders/Usher experiment should not experience a significant change of the perpendicular lattice spacing[35], there are misfit dislocations present.

3.4 Summary

The difference in the lattice parameters of a semiconductor layer compared to that of the substrate results in strained epitaxial layers. At the critical thickness, this strain begins to relax through movement of dislocations. The critical thickness of the samples used in this

experiment is 22 nm as calculated by the Matthews-Blakeslee equation, 3.9. The experimental critical thickness which is determined from measurements of the lattice constant of an epitaxial layer made by XRD[35] is larger than predicted by Matthews-Blakeslee since this technique is limited in sensitivity, as suggested by Freund[12].

Chapter 4

Elastic Strain Relaxation

When engineering semiconductor devices, it may be desirable to obtain a relaxed or strained layer of semiconductor material without creating dislocations. Several different methods have been used to achieve such layers, including compliant substrates [46, 47] and sacrificial sublayers[37]. This chapter will review the physics of elastic strain relaxation and the use of the two methods mentioned in obtaining elastically strain relaxed materials.

4.1   Physics of Elastic Strain Relaxation

Elastic strain relaxation is strain relaxation that is reversible, and does not introduce dislocations. There are several different methods for achieving elastic strain relaxation, each of which relies on the use of a special sublayer to obtain the desired relaxation. This sublayer is either a compliant layer or a sacrificial layer to be etched away. In each case, the relaxation of the semiconductor material is dictated by the layer structure that was grown on top of the sublayer. While there are limitless layer structures which can be grown, their relaxation behaviour can be broadly classified into three groups: single layer, bilayer and multilayer as shown in Fig. 4.1. The single layer structure consists of a strained semiconductor layer grown on the sublayer. In this case the layer will optimally relax one hundred percent and is limited only by the choice of the method used to cause elastic strain relaxation.

The bilayer structure consists of two layers with a different lattice constant. Typically one layer is strained and the other layer is lattice matched to the substrate. Following the strain relaxation treatment, the two layers share the strain between them. This can result in
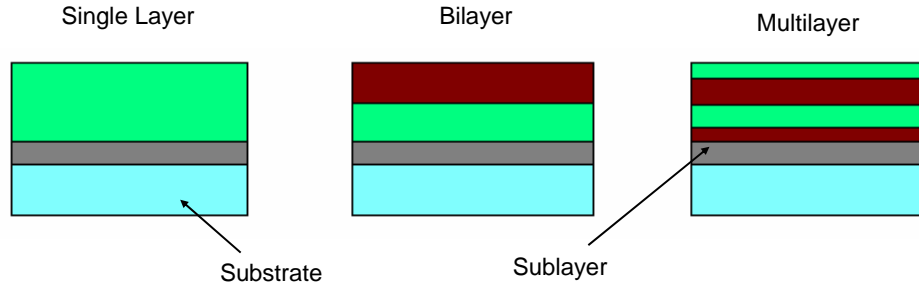
Figure 4.1: Examples of layer structures for single layer, bilayer and multilayer groups.

bending in a manner similar to that of a bimetallic strip if the relaxation method allows for bending. The curvature of a free-standing bilayer bending in one dimension is given by

$$\kappa = \frac{6E_1E_2(t_1+t_2)t_1t_2\varepsilon_0}{E_1^2t_1^4+4E_1E_2t_1^3t_2+6E_1E_2t_1^2t_2^2+4E_1E_2t_2^3t_1+E_2^2t_2^4} \tag{4.1}$$

where E_1 and E_2 are Young's modulus of the two materials, ε_0 is the mismatch, and t_1 and t_2 are the corresponding thicknesses. However, this is a simplified model, since depending on the mechanism used to induce elastic strain relaxation and the shape of the structure experiencing relaxation, the layers may curve in two directions (as a dome would); may not curve at all and instead relax according to the force-balance model discussed below[45]; or may relax under some combination of these mechanisms. While bilayer systems may seem unpredictable, it should be noted that, for any given layer structure, the forces, and thus the relaxation behaviour, remain the same in identical samples.

A multilayer system requires a more complicated model for strain relaxation. However, in the case of a trilayer system as depicted in Fig. 4.2 the relaxation model is simple. In this case the top and bottom layers are of equal thickness, which provides equal magnitude bending forces on both the top and bottom of the middle layer and the bending forces cancel out. This force-balance model, discussed by both Mooney et al. and Freund & Suresh [34, 13], is a model to determine the proportion of mismatch strain that each layer of the structure holds. In the case shown in Fig. 4.2 the mismatch strain between the two materials can be calculated from equation 3.3. The balance of strain between the layers is given by

$$\varepsilon_l - \varepsilon_s = \varepsilon_0 \tag{4.2}$$

where ε_l and ε_s are the elastic strain contained in layers l and s, and the stresses associated
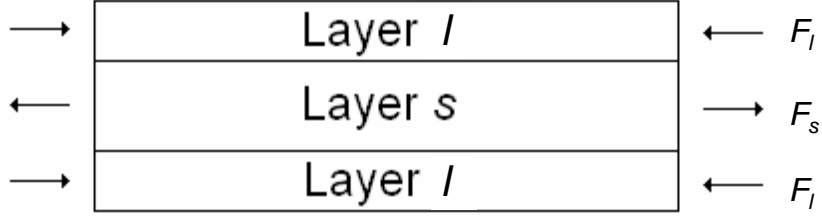
Figure 4.2: Trilayer structure with identical thickness layers l and single layer s. The forces are denoted and given by $F = \frac{P}{A}$, where P is the pressure and A is the cross-sectional area.

with them are $\sigma_l = M_l \varepsilon_l$ and $\sigma_s = M_s \varepsilon_s$, where M_l and M_s are the biaxial moduli for the materials comprising the two layers. Furthermore, as the structure is at equilibrium, the net force on any cross-section must be zero, consequently

$$2\vec{F}_l + \vec{F}_s = 0 \tag{4.3}$$

$$2M_l \varepsilon_l t_l + M_s \varepsilon_s t_s = 0 \tag{4.4}$$

where t_l and t_s are the thicknesses of the respective layers. In this case, equal thicknesses of the l layers will cause the net bending forces to cancel, and thus, by combining equations 4.2 and 4.4 the following relations can be obtained for the elastic strain in each layer

$$\varepsilon_l = -\varepsilon_0 \frac{t_s M_s}{2t_l M_l + t_s M_s}, \ \varepsilon_s = \varepsilon_0 \frac{2t_l M_l}{2t_l M_l + t_s M_s} \tag{4.5}$$

Consequently, for such a structure, the percentage of initial mismatch strain contained within the center layer after the structure has reached equilibrium is easily calculated. Figure 4.3 shows the strain relaxation of layer s as a function of the layer thickness ratio, $t_s/2t_l$.

4.2 Elastic Strain Relaxation using a Compliant Substrate

The use of a compliant substrate as a possible means of elastically relaxing strained thin films was first proposed by Lo [26], and has been successfully used more recently to achieve strain-relaxation in Si/SiGe structures by Yin *et al.* [46, 47]. Yin's work utilized a borophosphorosilicate glass (BPSG) on a Si substrate as a compliant film onto which strained pseudomorphic SiGe films were transferred by wafer bonding. The films were then patterned
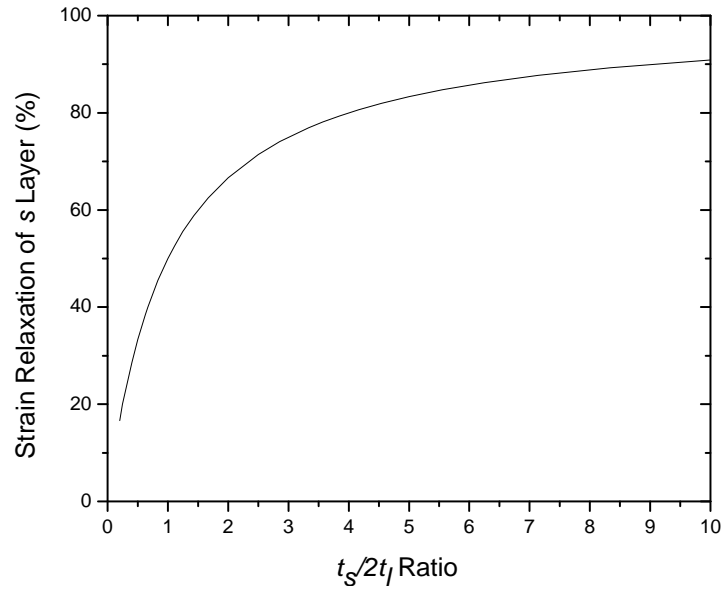
Figure 4.3: Percentage of strain-relaxation occurring within the center layer of a trilayer structure, as shown in fig. 4.2, for different thickness ratios.

into islands of various sizes. The BPSG is initially viscous and consequently the strained SiGe films remain strained following transfer; however, the viscosity of the BPSG drops rapidly when samples are heated above 750 °C allowing the SiGe film to relax as the compliant layer may now flow. It was noted that small islands of SiGe tended to relax laterally as intended, but larger areas frequently relaxed by buckling, which greatly increased the surface roughness of the SiGe film[46]. Additionally, small islands relax faster than large islands. As relaxation occurs, the lattice spacing between the strained atoms either increases (for initially compressively strained layers), or decreases (for initially tensilely strained layers). Since the strained layers are expanding over a fluid-like layer, the rate of expansion is limited by the viscosity of the compliant substrate. Thus, larger islands will take longer to expand, and therefore, relax due to the larger migration of the island edge required to achieve the same net shift in lattice parameter. While the buckling was eliminated through the use of a cap layer, the processing steps required to achieve smooth large areas required a combination of repeated etchs and long anneal times[45]. The compliant substrate method can also be employed to provide uniaxial in-plane strained layers[47]. As the speed at which strain relaxation occurs is dependent on the size of a feature as discussed above, uni-

axial relaxation was accomplished by use of rectangles rather than squares as the shape of the island. However, applying this mechanism to III-V materials has shown a considerable increase in the rms surface roughness of films wafer bonded to BPSG compared to those grown epitaxially on lattice matched substrates[16].

4.3   Elastic Strain Relaxation using a Sacrificial Layer

There are three main techniques for achieving elastic strain relaxation when using a sacrificial sublayer: free-standing structure formation, layer liftoff and in-place bonding. Formation of free-standing structures has been used in both SiGe/Si and III-V semiconductor structures [34, 21]. Principally, it employs a controlled etch of a sacrificial sublayer to cause the strained layer structure to be supported above the substrate by a pillar created from the sacrificial sublayer as shown in Fig. 4.4[33]. In this case, the conditions must be
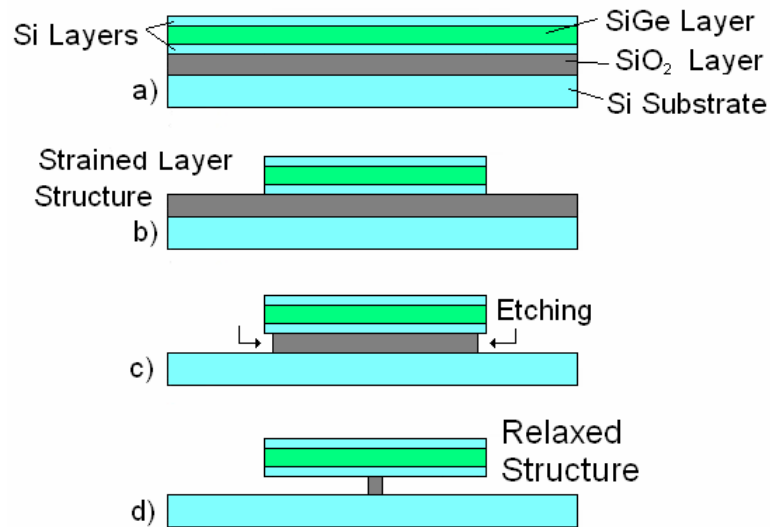
Figure 4.4: Schematic diagram demonstrating formation of a free-standing structure.

such that the supported layer structure does not remain in contact with the substrate following etching. This is typically accomplished by a combination of parameters, including a stiff supported structure and a thick sacrificial layer. The layer will relax as discussed in 4.1. Due to the nature of the mechanism, a bilayer structure is unsuitable for this type of

strain relaxation as bending can freely occur and, consequently, the layer structure subject to bending forces will not be flat. Single layer membranes fabricated in this way have been used for regrowth both with[21] and without[33] prior reinforcement of the pillar.

Layer liftoff is a process involving the complete removal of the sacrificial layer. This allows the strained layer structure to detach from the substrate in the etch solution[37]. The structure is then able to relax as described in section 4.1. A sufficiently thick sacrificial layer prevents the layer from adhering to the substrate during the etch process. The floating layer can then be attached to any new substrate, including those on which semiconductor crystals cannot be grown.

The final method to be discussed that involves a sacrificial layer is in-place bonding[8]. The in-place bonding method is similar to that of layer liftoff, but with the notable difference that the strained layer structure relaxes and then weakly bonds in-place on the substrate. Presently, it is believed that this method may only be used in a water based etchant bath (i.e., most typical acids) and only with hydrophobic material surfaces, as initial work demonstrated that the method failed when hydrophilic surfaces were used[8]. A schematic diagram showing the basic in-place bonding method is shown in Fig. 4.5. Initially, blanket epitaxial SiGe and Si layers were grown on a silicon-on-insulator substrate(Fig. 4.5(a)). Structures were then fabricated by photolithography and etching (Fig. 4.5(b)). The sacrificial SiO_2 sublayer was then removed (Fig.4.5(c)), and during etching, the strained layer relaxed and experienced a hydrophobic attraction to the substrate (Fig.4.5(d))[25]. Finally, when the sample was removed from the etchant bath, strain-relaxation had occurred as described above and the Si/SiGe/Si structure was weakly bonded to the substrate (Fig.4.5(e)). An 800°C anneal was performed to strengthen the bond. This final method was used as a basis for the design of the in-place bonding experiment described in this thesis.
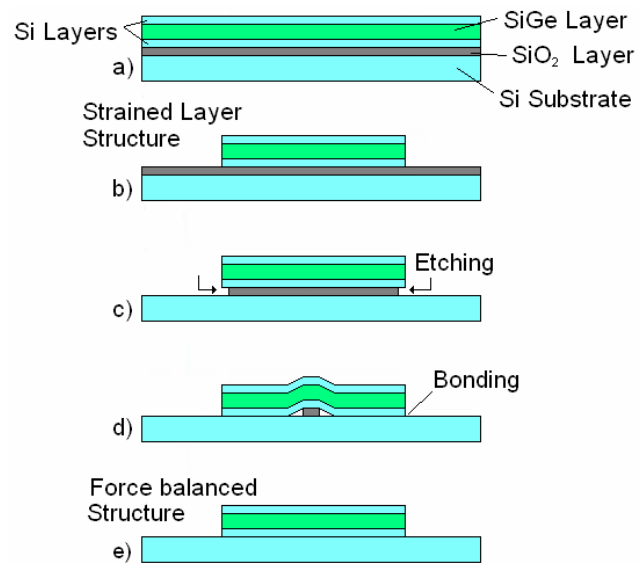
Figure 4.5: Schematic diagram demonstrating a basic in-place bonding process.

Chapter 5

Experiment Overview and Measurement Techniques

This chapter will discuss in detail the experiments performed for this thesis. In particular it will discuss the procedure used and justify the choices made throughout that procedure, including etchant selection and mask design. Furthermore, a discussion of the underlying physics of the methods used to analyze the samples is presented.

5.1   Description of Experiment

The objective of this work was to determine if the in-place bonding method demonstrated in SiGe/Si[8] can be applied to III-V semiconductor materials. This will primarily provide a suitable base technique for further exploration of strain-relaxed engineered substrates in III-V materials. GaAs and InGaAs were chosen as materials since there is an interest in obtaining high quality InGaAs layers, which are usually grown on InP substrates on GaAs substrates, because of the lower cost of GaAs substrates. A GaAs/InGaAs layer structure was chosen as GaAs substrates possess a suitable sacrificial layer, AlAs, which has a lattice parameter close to that of GaAs. The layer structures shown in Fig. 5.1 were grown on GaAs(001) wafers by metal-organic chemical vapour deposition (MOCVD). Since AlAs is essentially lattice matched to GaAs, this layer is unstrained. However, as the lattice constant of the $In_{0.08}Ga_{0.92}As$ layer is 0.6% larger than that of the substrate, the $In_{0.08}Ga_{0.92}As$ layer
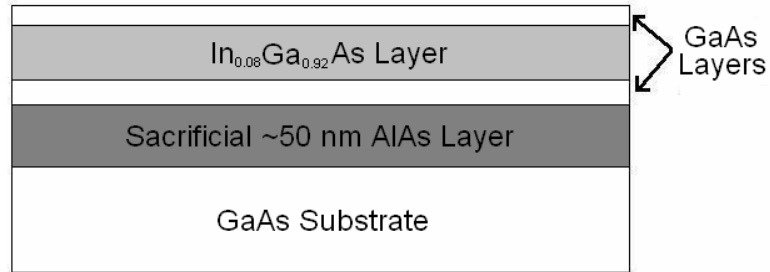
Figure 5.1: Schematic diagram of sample epitaxial layer structure

will be compressively strained, as described in section 3.1. The samples were analyzed with X-ray diffraction (XRD) to determine the alloy composition, the strain, and the layer thickness. Atomic force microscopy (AFM) was used to determine the roughness of each sample. Following this initial characterization, the samples were patterned by conventional optical lithography and etched in a cleanroom environment as shown in Fig. 5.2 to allow the strained layer structure to relax elastically and to achieve in-place Van der Waals bonding.
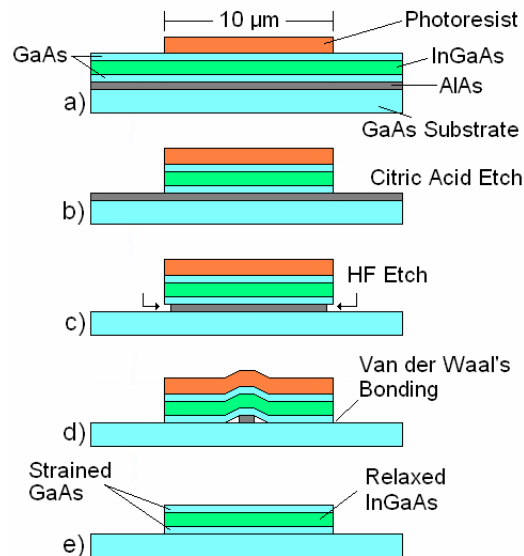
Figure 5.2: Schematic diagram of the cleanroom fabrication process for in-place bonding of a InGaAs/GaAs layer structure.

After the samples were processed, they were analyzed with the aforementioned methods to determine: a) if elastic strain relaxation had occurred, b) if in-place bonding occurred, and c) if significant roughening of surfaces had occurred, which could impact the usefulness of this technique in future experiments. Since elastic strain relaxation has in fact occurred, then select samples will be annealed to improve the bond strength. It should be noted, that while this work is focused on transferring a technique from one set of materials to another, the technique, in itself, is very new and not entirely understood.

5.2 Etchant Chemistry and Behaviour

Etchant selection is very important in any experiment involving different materials and small features. In general, this involves choosing etchants with appropriate etch rates for the desired materials. Selectivity becomes particularly important and is expressed by the ratio of the rates at which the etchant removes two different types of material. In the case of this particular experiment, the samples contain a trilayer structure comprised of a GaAs layer, an InGaAs layer and a GaAs layer as shown in Fig. 5.1. This structure limits the choice of etchants to either a single one with equal etch rates for both the GaAs and the InGaAs layers, or two etchants with high selectivity between the GaAs and InGaAs layers, as etching both materials at unequal rates may change the geometry, and thus the relaxation of the layer structure. The potentially small indium alloy composition of the InGaAs layer indicates that an equal rate etch will provide the most accurate etch. Additionally, this structure sits upon a sacrificial AlAs layer which must be removed without damaging the trilayer structure described above. Consequently, at least two etchants are needed for this experiment, one to etch through the structure, and one to remove the sacrificial layer.

Chemical etching in most III-V semiconductor materials proceeds by an oxidation-reduction reaction at the semiconductor surface, followed by dissolution of the oxide material, resulting in the removal of the semiconductor material[3]. This is generally accomplished through the use of an acid mixed with an oxidizing agent such as hydrogen peroxide (H_2O_2). Etchants are additionally classified into two broad categories: reaction rate limited and diffusion limited. Reaction rate limited etchants have a constant etch rate, the amount of material removed is linearly proportional to the etching time, unaffected by agitation of the etchant, faster at higher temperatures, and susceptible to large changes in etch rate

caused by small changes in the proportions of the etchant components. Diffusion-limited etchants remove an amount of material proportional to the square root of the etch time, experience an etch rate increase when agitated, and possess temperature independent etch rates[9]. Because the various samples to be grown for this experiment have different layer thicknesses, a reaction rate limited etchant is preferable because the etch rate is more easily predicted and would be consistent for all layer thicknesses. However, the measurement and mixing of such an etchant must be done carefully to achieve consistent etch rates.

DeSalvo performed considerable characterization of a citric acid/hydrogen peroxide ($C_6H_8O_7$:H_2O_2) etch, and showed that at a volume ratio of 3:1 it would provide equal etch rates for GaAs and InGaAs with indium alloy composition of 20% or less[9]. The citric acid was prepared by mixing 1 g of anhydrous citric acid crystals with 1 mL of deionized (DI) water. It was necessary to prepare this solution at least one day prior to use, as the citric acid/water reaction is endothermic and wait time is necessary to allow the mixture to return to room temperature. The hydrogen peroxide had a concentration of 30%. This etch is selective, allowing the GaAs/InGaAs etch to proceed to completion without etching of the AlAs layer. This proposed etch was reported to act at a rate of ∼200 nm/min, thus yielding an expected total etch time ranging from 40-70 seconds depending on layer thicknesses of the sample. This range of times also includes additional overetch time to allow for complete removal of material in the areas being etched.

A second etch is required to remove the AlAs layer without damaging the underlying GaAs substrate, or the trilayer GaAs/InGaAs/GaAs structure. In this case, the better method was to use an etchant utilizing an inorganic acid which preferentially attacks the AlAs. Hydrofluoric acid (49% concentration) was chosen as the etchant, as it provided selectivities of greater than 100:1 for high Al content materials.[3] The high concentration was chosen in order to minimize potential damage to the GaAs layers. Due to the extremely small amount of AlAs to be removed, and the high etch rate, the total expected etch time is only on the order of 10-20 seconds. Additionally, the photoresist used is unaffected by either etch. This provides a means to easily preserve the upper structure surface to prevent roughening during the second etch.

5.3 Photolithography and Mask Design

Photolithography is a well established means of patterning semiconductor samples. This process uses a photoreactive compound (photoresist) which either becomes soluble or insoluble in a developer solution after being exposed to ultraviolet light. It is broadly classified, based on the solubility following exposure, into positive resist, where the exposed portions are removed by the developer, and negative resist, where the exposed portions become insoluble and remain following development. The areas to be exposed are defined by a mask which is a glass plate with a chrome pattern on one side. The chrome protects certain areas from exposure to the UV light. Consequently, for this experiment, a commonly used positive photoresist, diazonaphthoquinone (DNQ), was used as the photoresist.

The mask for the photolithography process was designed to meet a number of objectives for this project, as well as to have characteristics which could make it useful for future projects. Specifically, the mask was designed to be usable for both full 2 inch wafers and quarters of 2 inch wafers. Figure 5.3 shows the entire mask pattern. Note that lines marking a circle and a quarter of that circle indicate the size and intended position of full 2 inch wafers and quarter wafers, and are not features on the mask. It was intended that the majority of processing would occur on quarter wafers, which would be affixed to whole wafers using photoresist and aligned with the mask. Additionally, an area of sufficient size to measure with XRD was needed for the patterned area with the maximum surface coverage of the structure of interest. It was determined that an array of either 10 μm, shown in Fig. 5.4(inset) or 20 μm squares with 5 μm spaces between them would provide sufficient spacing between each structure and still provide a high surface area coverage. The features covered 45% and 64% of the array area for the 10 μm and 20 μm structures respectively. These arrays filled a 10x10 mm^2 area which would lie approximately 5 mm from the cleaved edges of a quarter wafer piece, as shown in Fig. 5.3. This area of unpatterned sample provides the ability to measure both the patterned and unpatterned area using XRD following sample processing. Three additional features, shown in Fig. 5.4, were included on the mask in unused areas. The sample label was included to ease distinction between samples patterned with different array sizes without the need to use a microscope. The etch rate marks were included to provide an area to quantify the etch rates of various etchants being used if necessary. The alignment marks were included to allow for the possibility of
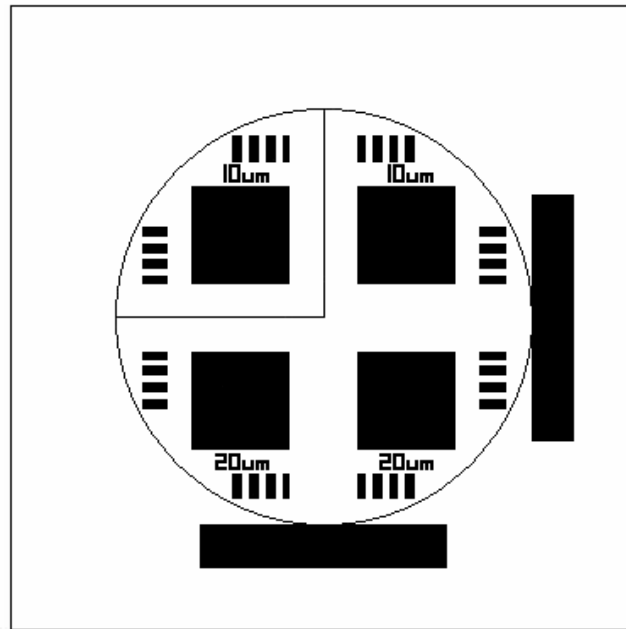
Figure 5.3: Image of full mask pattern, the large bars at the edges of the full wafer marker are used to align the wafer. The large squares are patterned arrays of 10 μm and 20 μm features.

using this mask later as part of a multimask patterning procedure, where alignment marks would be necessary.

5.4 X-Ray Diffraction Technique

Any radiation striking a material will be both scattered and absorbed. X-ray diffraction makes use of photons that are elastically scattered from the electron clouds of individual atoms of a crystal lattice. Each photon path from the source to the detector is indeterminant and all the possible paths are coherent[11]. These paths are determined by the collimation of the photon beam as it exits the source. The detector will measure the contributions of all possible paths of these photons. The diffraction pattern will be a result of phase difference in different paths. For a single crystal, Bragg's equation describes the angle of the maximum diffracted intensity

$$n\lambda = 2d sin\theta_B \tag{5.1}$$
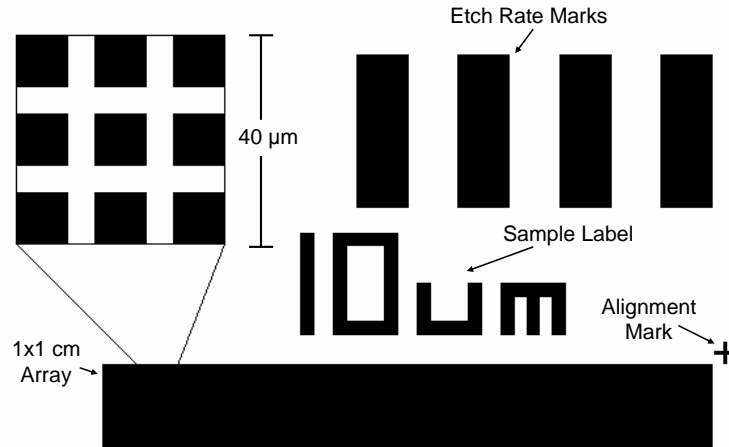
Figure 5.4: Close up of additional mask features, including sample label, alignment mark and etch rate determination pits.

where n is an integer giving the order of diffraction, λ is the wavelength, d is the interplanar spacing of the diffracting atomic planes, and, the Bragg angle, θ_B is the angle of the incident and diffracted waves relative to the reflecting plane as shown in fig. 5.5. However, Bragg's equation is an idealized case, as the electrons from which the X-rays are scattering populate a cloud around an atom, and the atoms themselves vibrate at non-zero temperatures. The contributions of atomic vibration and electron density can be accounted for by including a scattering factor[11]. Furthermore, Bragg's equation neglects several key aspects of diffraction within the crystal, such as the change in refractive index as the X-rays enter the crystal, and the possibility of photon rediffraction, in which a photon is diffracted multiple times within the crystal. Despite these issues, Bragg's law allows for the extraction of several basic properties of a crystalline layer.

5.4.1 Measured Quantities

High resolution X-ray diffraction is an important tool for the characterization of epitaxial structures in semiconductors. X-ray scans may be used to determine properties of individual layers, such as mismatch, thickness, and composition. Additionally, X-ray measurements may be used to detect defects within epitaxial layers or samples, including misorientation, mosaic spread, curvature, and strain relaxation. Rocking curve measurements are done with
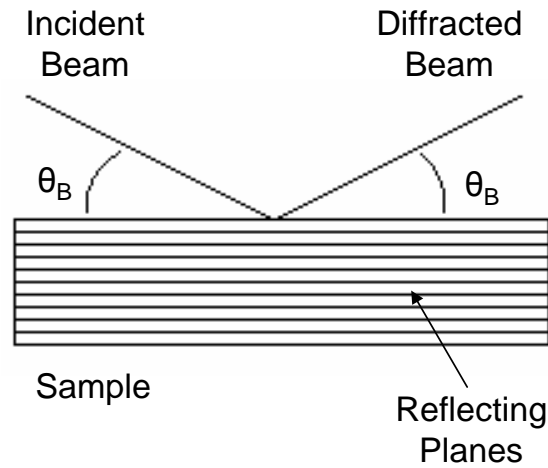
Figure 5.5: Incident and diffracted Bragg angles for reflection planes parallel to the sample surface.

a wide detector aperture such that the entire reflected beam is detected and involve adjusting the angle of the detector and sample simultaneously such that the reflections from a plane of atoms are measured over a range of incident and detector angles. In this case, the incident beam angle is defined as ω and the detector is positioned at 2θ as shown in fig. 5.6. In
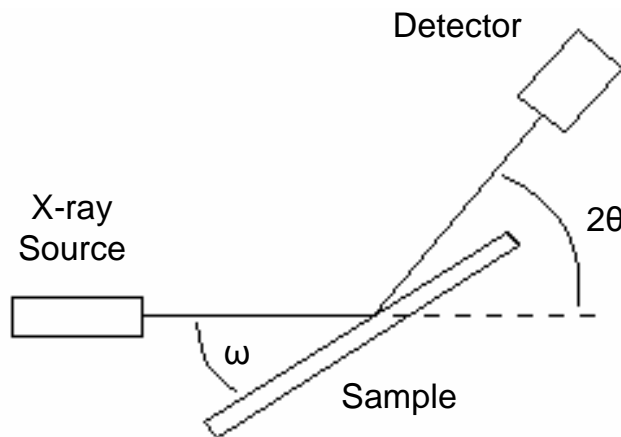
Figure 5.6: Schematic diagram of X-ray system with relevant angles defined.

this case, both angles are relative to the incident beam. Two types of rocking curve scans are used: symmetric and asymmetric. In the symmetric case, the reflecting lattice planes

are approximately parallel to the sample surface and $\omega \approx \theta(\frac{2\theta}{2})$. In the asymmetric case, the reflecting planes are at an angle with the sample surface as shown in Fig. 5.7 where $\omega = \theta_B - \phi$ for grazing incident ($\omega = \theta_B + \phi$ for grazing exit) and ϕ is the angle between the lattice planes to be measured and the sample surface.
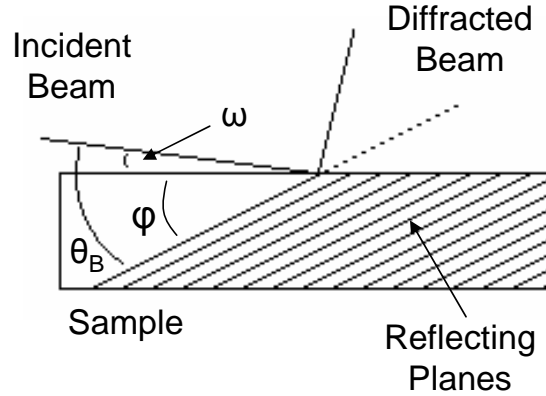
Figure 5.7: Diagram of an asymmetric grazing incident XRD measurement, planes on the left hand side of the sample are not shown for clarity.

The basic requirement to derive the layer parameters from an X-ray diffraction measurement is a recorded rocking curve. For a sample consisting of a single epitaxial layer on a substrate[4], such a scan will show two peaks, one from the substrate and one from the layer. It should be noted that while this section discusses the derivation of properties of a single layer structure, these techniques would apply to multiple peaks.

Mismatch

For the purpose of demonstration, sample analysis will be carried out on the symmetric (004) reflection scan of a sample consisting of a strained InGaAs layer on a GaAs(001) substrate shown in Fig. 5.8. In this case, the separation between the GaAs and InGaAs peaks, $\delta\omega$, is measured to be $0.388° = 0.00677$ rad. A relationship between this peak separation and the atomic layer spacing normal to the substrate can be obtained by taking the derivative of equation 5.1, and is given by

$$\frac{\delta d}{d} = -\delta\theta cot\theta_B \tag{5.2}$$
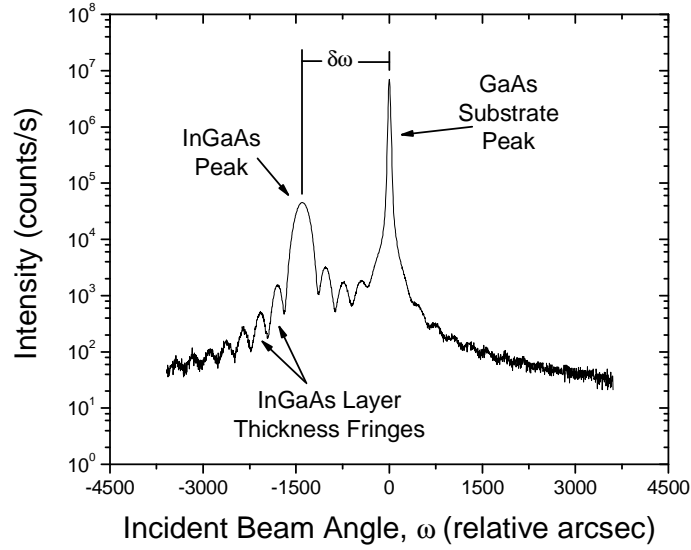
Figure 5.8: X-ray diffraction scan to demonstrate measurements of sample 5539.

where $\delta\omega = \delta\theta$ with respect to the position of the Bragg reflection of the substrate at θ_B [4]. In the case where a 004 symmetric reflection is used, then this is the out-of-plane x-ray strain

$$m^* = \frac{\delta d}{d} \tag{5.3}$$

However, m^* is not the in-plane mismatch, which relates the layer and substrate in-plane lattice parameters and is given by

$$m = \frac{a_l - a_s}{a_s} \tag{5.4}$$

where a_l is the lattice constant of a the free layer and a_s is the lattice constant of the substrate. This is related to m^* by elasticity theory[23] yielding the following relationship

$$m = m^* \frac{1 - \nu}{1 + \nu} \tag{5.5}$$

where ν is the Poisson ratio. For the above case for a GaAs substrate, where $\delta\omega = 0.00677$ rad and $\theta_B = 0.543$ rad, m was found to be 0.0057. From this mismatch, equations 5.4 and 3.1 can be used to determine the composition of any coherently strained sample. In the example case, these equations yield the result of 7.8% InAs, which closely matches the target composition of 8% InAs.

Strain Relaxation

In the case where a layer is partially relaxed, the mismatch calculated from the out of plane interatomic spacing will not provide an accurate measure of either composition or strain, unless one is known. In order to determine both quantities, the in-plane lattice constant must be measured in addition to the out of plane lattice constant. By the use of asymmetric (224) scans, two additional peak separations are measured: $\Delta\omega_i$, the separation between the layer and substrate peaks for a grazing incident scan (224), and $\Delta\omega_e$, the separation between the layer and substrate peaks for a grazing exit (-2-24) scan[4]:

$$\Delta\omega_i = \delta\omega + \delta\phi, \quad \Delta\omega_e = \delta\omega - \delta\phi \tag{5.6}$$

where $\delta\omega$ is the separation of the layer and substrate peaks for a symmetric scan of these lattice planes, and $\delta\phi$ is the additional separation of the peaks in an asymmetric scan due to tilt from elastic strain. With the assumption that in-plane strain will be equal in the two perpendicular in-plane directions, the equation for the interplanar spacing is

$$\frac{1}{d_{hkl}^2} = \frac{h^2 + k^2}{b_l^2} + \frac{l^2}{c_l^2}, \tag{5.7}$$

where b_l and c_l are the in and out of plane lattice constants, respectively and h, k, l are the Miller indices. This can be related to angles using Bragg's law (eq. 5.1) to

$$\frac{4sin^2\omega_l}{\lambda^2} = \frac{h^2 + k^2}{a_l^2} + \frac{l^2}{c_l^2}, \tag{5.8}$$

where ω_l is the Bragg peak of the layer. This may be further simplified for a (001) oriented surface by using the formula for interplanar angles in the crystal to

$$sec^2\phi_l = \frac{c_l^2}{l^2}\left(\frac{h^2 + k^2}{b_l^2} + \frac{l^2}{c_l^2}\right), \tag{5.9}$$

where ϕ_l is the angle between the reflecting planes layer and the sample surface. Then using the above relations for $\Delta\omega_i$ and $\Delta\omega_e$ provide the atomic spacing both in-plane (a_l) and out of plane[4] (c_l)

$$c_l = \frac{l\lambda}{2sin\omega_l cos\phi_l}, \quad b_l = \frac{l\lambda}{2sin\omega_l}\sqrt{\frac{h^2 + k^2}{l^2}} \tag{5.10}$$

The relaxation is then

$$R = \frac{b_l - a_s}{a_l - a_s} \times 100 \tag{5.11}$$

where a_l is the lattice parameter of the fully relaxed layer.

Thickness

The preferred method for measuring layer thickness is to use the periodic oscillations around the layer peak, labeled thickness fringes in fig. 5.8. In the single layer case, the separation, $\Delta\omega_p$ is given by[4]

$$\Delta\omega_p = \frac{\lambda\gamma_g}{t\,sin2\theta} \tag{5.12}$$

where λ is the wavelength, t is the thickness, and γ_g the cosine of the angle between the diffracted beam and the surface normal. For the case of a symmetric reflection, this simplifies to

$$t = \frac{\lambda}{2\Delta\omega_p\,cos\theta} \tag{5.13}$$

It should be noted that these equations do not contain anything about either the material or diffraction conditions besides the Bragg angle and the geometry. This independence is a result of the refractive index for X-rays being very close to unity.

It should be noted that the most reliable way to determine layer thicknesses from a multiple layer structure is by using a simulation. Using X'pert Epitaxy software from Panalytical[10], simulations were performed and then manual adjustments of the parameters, combined with use of the fitting algorithm provided in the software, were utilized to obtain a good fit. The software employs dynamical diffraction physics to obtain the simulated data[4]. Triple-axis measurements were used for the fitting of simulations. These measurements are performed with a detector aperture of 12 arcseconds, which lowers both the signal and background; however, the background is reduced more than the signal resulting in a better signal-to-noise ratio, allowing for a better fit to be obtained than for a similar rocking curve measurement.

5.5 Atomic Force Microscopy

Atomic force microscopy (AFM) is a useful tool for examining the surfaces of materials. In this experiment, an Asylum Research scanning probe microscope was used to measure the surface topography of samples and to detect the presence and density of dislocations by means of the surface steps they produce. The principal behind AFM is that of using a sharp tip to interact with the sample surface and a flexible beam to measure the resultant

force with high sensitivity[38]. An AFM tip near a sample will experience both long and short range forces as shown in Fig. 5.9[14]. The short range forces are a result of chemical
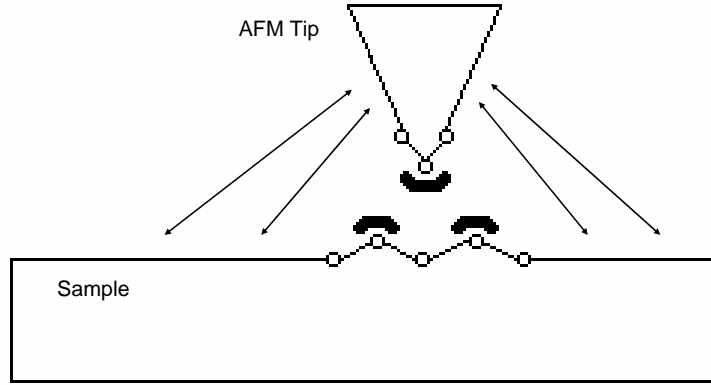
Figure 5.9: Diagram of forces experienced by an AFM tip near a surface. Short-range forces are indicated by crescents and long-range forces are indicated by arrows[14]

interactions between the tip and sample electron orbitals and they only affect the tip when these orbitals overlap. The long range forces are due to the full volume of both the tip and sample, and include van der Waals, electrostatic and magnetic forces. In AFM operation, the tip is in close contact with the sample surface, in this case, the potential energy of the tip and sample system is V_{ts}. The z component of the tip-sample force is given by $F_{ts} = -\partial V_{ts}/\partial z$, and a tip-sample spring constant $k_{ts} = -\partial F_{ts}/\partial z$.

5.5.1 Tip-Sample Forces

The contribution of the short range forces can be calculated by the Morse potential[20]

$$V_{Morse} = -E_{bond}(2e^{-\kappa(z-\sigma)} - e^{-2\kappa(z-\sigma)}) \tag{5.14}$$

which describes a chemical bond with bonding energy E_{bond}, equilibrium distance σ and decay length κ. While the Morse potential provides a good qualitative description of chemical bonds, it does not account for bond anisotropy. As this anisotropy is highly dependent on the materials involved, precise calculations must often be made from first principles.

The long range van der Waals potential for a spherical tip of radius R next to a flat

surface is given by[20]

$$V_{vdW} = -\frac{A_H R}{6z} \tag{5.15}$$

where A_H is the Hamaker constant, and depends on the type of materials of the tip and sample. It should be noted that while the van der Waals force is proportional to $1/z^2$ for spherical tips, it is proportional to $1/z$ for pyramidal or conical tips. For typical tips, the van der Waals potential is $\approx$ -30 eV, yielding a corresponding force of $\approx$ -10 nN[14]. For the measurements performed in this experiment, the samples are neither conducting nor magnetic, and consequently, the electrostatic and magnetic force contributions are negligible.

5.5.2 Force Measurement

The tip-sample forces mentioned in section 5.5.1 can vary strongly over a short distance. The sensor used to detect these fluctuations is a cantilever beam, such as is shown in Fig. 5.10[14] The spring constant of such a cantilever is given by[7]
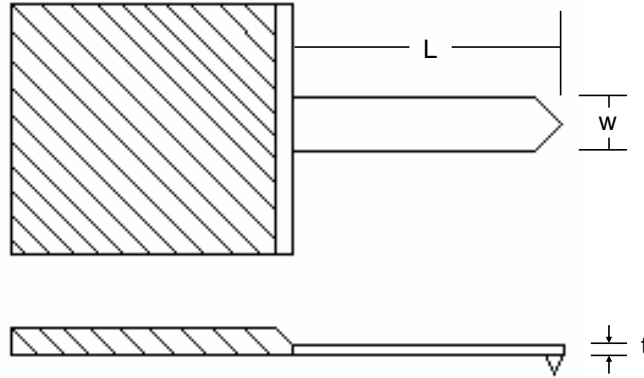
Figure 5.10: Top and side view of an AFM cantilever similar to that used for the AFM measurements performed in this experiment.[14]

$$k = \frac{Y w t^3}{4L^3} \tag{5.16}$$

where Y is Young's modulus, and w, t and L are the width, thickness and length of the cantilever respectively. The fundamental eigenfrequency for such a cantilever is given by[7]

$$f_0 = 0.162 \frac{t}{L^2} \sqrt{\frac{Y}{\rho}} \tag{5.17}$$

where ρ is the density of the cantilever.

The deflection of the cantilever is measured when a laser is reflected off the cantilever and detected by two photodiodes as shown in Fig. 5.11[38]. The resulting photocurrents
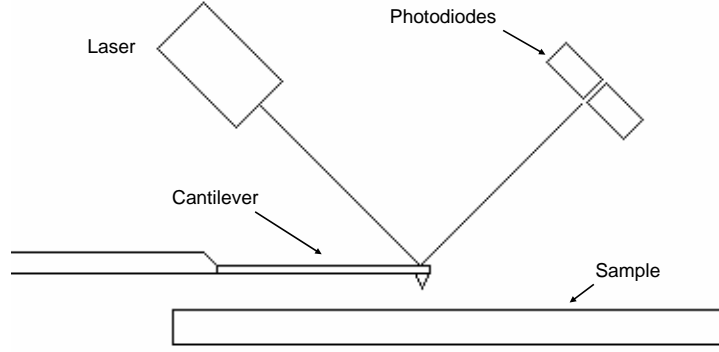
Figure 5.11: Diagram of beam bounce method of measuring cantilever deflection

from the two photodiodes are then fed into a differential amplifier, the output of which will be proportional to the deflection of the cantilever. The difference in the photocurrents is given by the following expression for a square spot approximation[38]

$$\delta i = 3\frac{\pi a}{l}\eta PA sin(\Omega t) \qquad (5.18)$$

where $2a$ is the dimension of the laser spot on the cantilever, l is the length of the cantilever, η is the quantum efficiency of the photodetector, P is the total optical power incident on the photodetectors, A is the deflection of the cantilever and Ω is the frequency of modulation.

5.5.3 Operating Mode

In this experiment, the AFM was operated in the frequency modulated-AFM (FM-AFM) dynamic mode, or "tapping" mode. In this case, the cantilever is subjected to controlled positive feedback to maintain oscillations of constant amplitude[14]. The frequency, f, is determined by the eigenfrequency f_0 of the cantilever, and the phase shift ϕ between the driving actuator and the cantilever.

The forces between the tip and sample cause the cantilever to oscillate at a new frequency $f = f_0 + \Delta f$. The eigenfrequency of a harmonic oscillator is $(k^*/m^*)^{0.5}/(2\pi)$,

where k^* is the effective spring constant, and m^* is the effective mass. If k_{ts} is constant over the whole range of the oscillating cantilever, $k^* = k + k_{ts}$. If $k_{ts} \ll k$, the square root can be expanded as a Taylor series, yielding

$$\Delta f = \frac{k_{ts}}{2k} f_0 \tag{5.19}$$

However, in cases where k_{ts} is not constant, the frequency shift when calculated by perturbation theory is

$$\Delta f = -\frac{f_0}{kA^2} < F_{ts} q' > \tag{5.20}$$

where the brackets indicate an average of one oscillation cycle and q' is the deflection of the tip of the cantilever.

From this, the shift in frequency is related to the known amplitude of oscillation, A, and the force experienced between the tip and sample, F_{ts}. By expressing this force as a combination of a van der Waals force and a Morse force[14],

$$F_{ts} = \frac{C}{z + \sigma} + 2\kappa E_{bond}(-e^{-\kappa(z-\sigma)} + e^{-2\kappa(z-\sigma)}) \tag{5.21}$$

where C depends on the tip angle and the Hamaker constants of the tip and sample. This allows for the change in frequency to be expressed in terms of the separation of the tip and sample, z, and the known amplitude of oscillations, A, allowing for the tip-sample separation to be calculated. From these measurements of surface topography, the surface roughness is determined by taking the root-mean square of the data for each scan.

5.6 Summary

An outline of the experimental fabrication procedure and techniques has been presented. The choices of both etchants and mask design were explained. The X-ray diffraction and atomic force microscopy techniques outlined above were used to fully characterize the physical properties of the samples through all stages of the experiment.

Chapter 6

Initial Sample Characterization

Samples layers were individually analyzed to determine the growth rate and composition. It was found that achieving smooth, high quality AlAs layers was necessary to obtain strained InGaAs layers that possessed good surface quality. Once the desired samples were obtained, they were characterized with XRD and AFM. Layer compositions and thicknesses were determined by means of XRD simulation.

6.1   Individual Layer Properties

Samples were grown on quarters of 2 inch diameter semi-insulating $2°$ miscut and exact GaAs(001) substrates by metal-organic chemical vapor deposition (MOCVD) in an optical showerhead reactor[15]. To determine the optimal growth conditions, and to ensure the layers in the experimental samples possessed the desired composition and thicknesses, single layers of each sample layer were grown and analyzed with XRD and AFM techniques. Initially, the growth rates of the various materials had to be determined. A single AlAs layer measured with XRD is shown in Fig. 6.1. The sample in this figure has an AlAs layer thickness of 94 nm, indicating a growth rate of 0.3 nm/s. Further measurements of this sample were not possible as the sample completely oxidized prior to additional XRD or AFM scans being performed. From this, we realized that in order to preserve the AlAs layer for measurements a $\sim$2 nm GaAs cap layer must be grown on top of the AlAs layer to prevent oxidation.

The next samples focused on determining the growth rate and critical thickness of In-
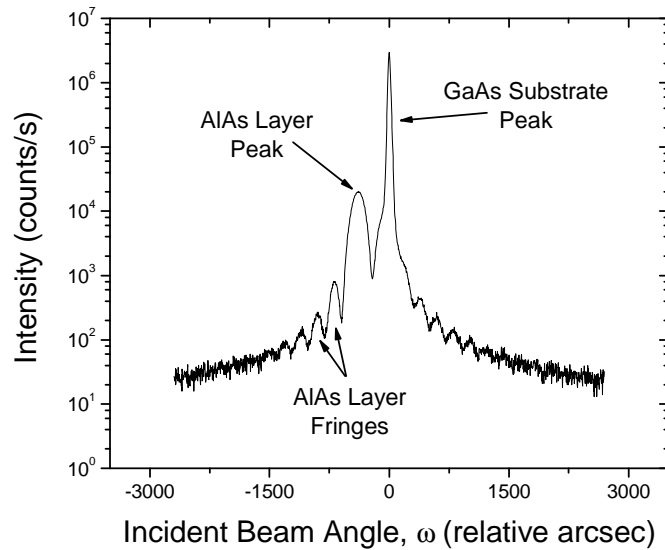
Figure 6.1: X-ray rocking curve measurement of sample 5507, an AlAs layer grown on GaAs substrate. The layer thickness of 94 nm was determined by X-ray simulation.

GaAs for the desired alloy composition. Fig. 6.2 shows an XRD scan and an AFM image of an InGaAs layer that exceeded the critical thickness. This is shown by the InGaAs layer XRD peak which has no thickness fringes, indicating that it is experiencing significant broadening caused by misfit dislocations. This sample consists of 12% InAs alloy and is 160 nm thick. Furthermore, a cross-hatch pattern is visible on the AFM scan but the density is above that which can be counted. This sample lies above the Orders-Usher experimental critical thickness shown in fig. 3.3, thus it is not surprising that a high dislocation density is present and that no fringes are visible on the XRD scans.

These initial samples appeared to be without problems, so a set of samples with the full layer structure of an AlAs layer, a GaAs layer, an InGaAs layer and a GaAs layer was grown. The AlAs layer was consistently 50 nm thick, as were the GaAs layers. The InGaAs layer was initially 100 nm thick and had an InAs alloy composition of 12%; however, this layer was reduced in both thickness and alloy composition over the course of 5 samples to attempt to obtain the desired layer quality and strain. XRD measurements of these samples consistently indicated relaxation in the InGaAs layer by dislocations as shown in Fig. 6.3a. While the thickness and composition of these InGaAs layers was believed to be below the
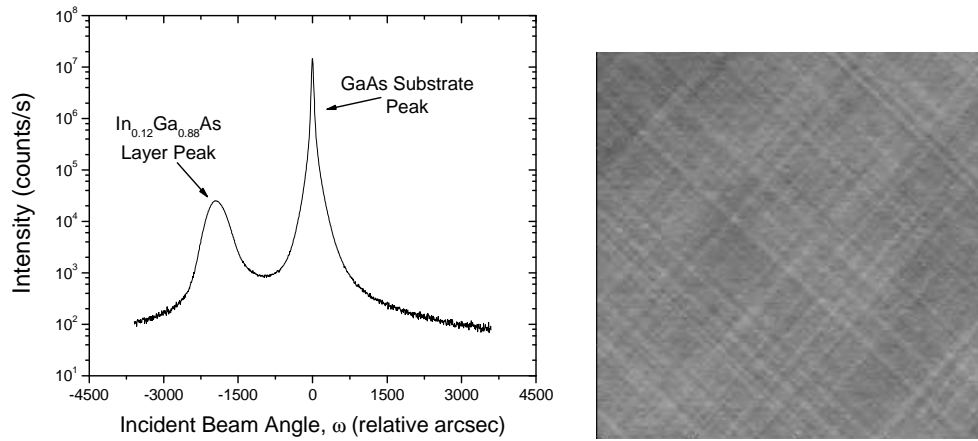
Figure 6.2: X-ray rocking curve and AFM image of a InGaAs sample (5508) which has exceeded the critical thickness and relaxed by misfit dislocations. The layer has a nominal thickness of 160 nm and is 12% InAs. The AFM image size is 20 μm and the root-mean square (RMS) surface roughness is 0.52 nm.

experimental critical thickness from XRD, it appeared that strain-relaxation was occurring during growth. AFM measurements showed extremely deep pitting as shown in Fig. 6.3b and RMS roughness of $\approx$ 1.5 nm. As single InGaAs layers showed little roughening in AFM images (fig 6.2b) when compared to the full structure samples, it was suspected that the source of the rough surface was a poor quality AlAs layer.

Consequently, a second set of samples was then grown on both exact and 2° miscut substrates to determine which type of substrate would provide the best sample quality. Initially, the focus of this set of samples was to achieve the desired surface quality for the AlAs layer, and ensure that the quality of the InGaAs layer was maintained. It was found that the surface roughness of AlAs layers was significantly greater for layers grown on miscut substrates than on exact substrates. Varying both the growth temperature and the V:III ratio over five different samples comprising a 50 nm AlAs layer and a 2 nm GaAs cap layer the RMS surface roughness of layers grown on exact substrates was improved from 0.39 nm to 0.16 nm and the quality of the surface improved immensely as shown in Fig. 6.4. The sample numbers, growth conditions, and measured roughnesses are listed in table 6.1. The RMS roughness was found to be insensitive to the V:III ratio but quite sensitive to the growth temperature. A growth temperature of 550°C with a V:III ratio of ∼12 yielded the
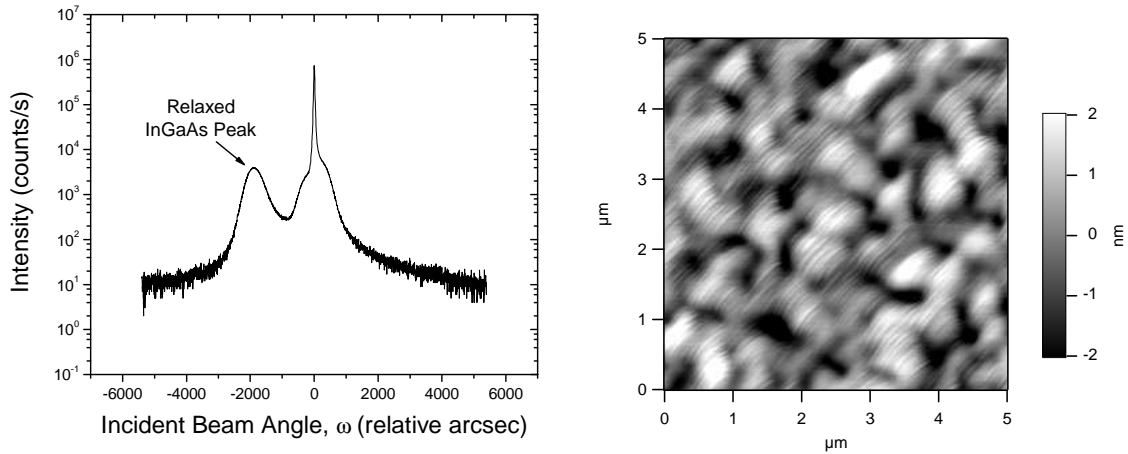
Figure 6.3: X-ray rocking curve and AFM measurements of 50/100/50 sample 5512 from the first batch of samples grown with the full layer structure. The InGaAs peak shows no thickness fringes. The InAs alloy composition was 12% and has a nominal thickness of 100 nm. RMS surface roughness measured to be 1.46 nm.

best surface quality for the AlAs layer. Under these conditions there was little difference between growth on exact and $2°$ miscut substrates.

InGaAs layers were grown on exact substrates to experimentally determine a critical thickness for 8% indium alloy composition. Figure 6.5 shows XRD and AFM data from a single strained layer of $In_{0.08}Ga_{0.92}As$. The thickness of this layer was found to be 69.8 nm by using the thickness fringes. This indicates that the layer was grown below the critical thickness in accordance with previous experimental work[35]. Furthermore, it provides an $In_{0.08}Ga_{0.92}As$ growth rate of 0.57 nm/s at these growth conditions. Note that the irregular features seen in the AFM image are individual surface steps, and the surface rms roughness of this sample was 0.15 nm, which is comparable to the value of 0.12 nm for an homo-epitaxial GaAs layer.

Table 6.1: Growth conditions & measured roughness of a 50 nm AlAs layer with a 2 nm GaAs cap.

Sample Number	Growth Temperature (°C)	V:III Ratio	Surface Roughness (nm)	
			Exact Substrate	Miscut Substrate
5533	600	5	0.39 ± 0.02	1.72 ± 0.02
5535	575	5	0.14 ± 0.02	0.72 ± 0.02
5536	600	12	0.13 ± 0.02	0.74 ± 0.02
5537	550	5	0.16 ± 0.02	0.20 ± 0.02
5538	550	12	0.16 ± 0.02	0.28 ± 0.02

(a) 5533 Exact

(b) 5533 Miscut

(c) 5538 Exact

(d) 5538 Miscut
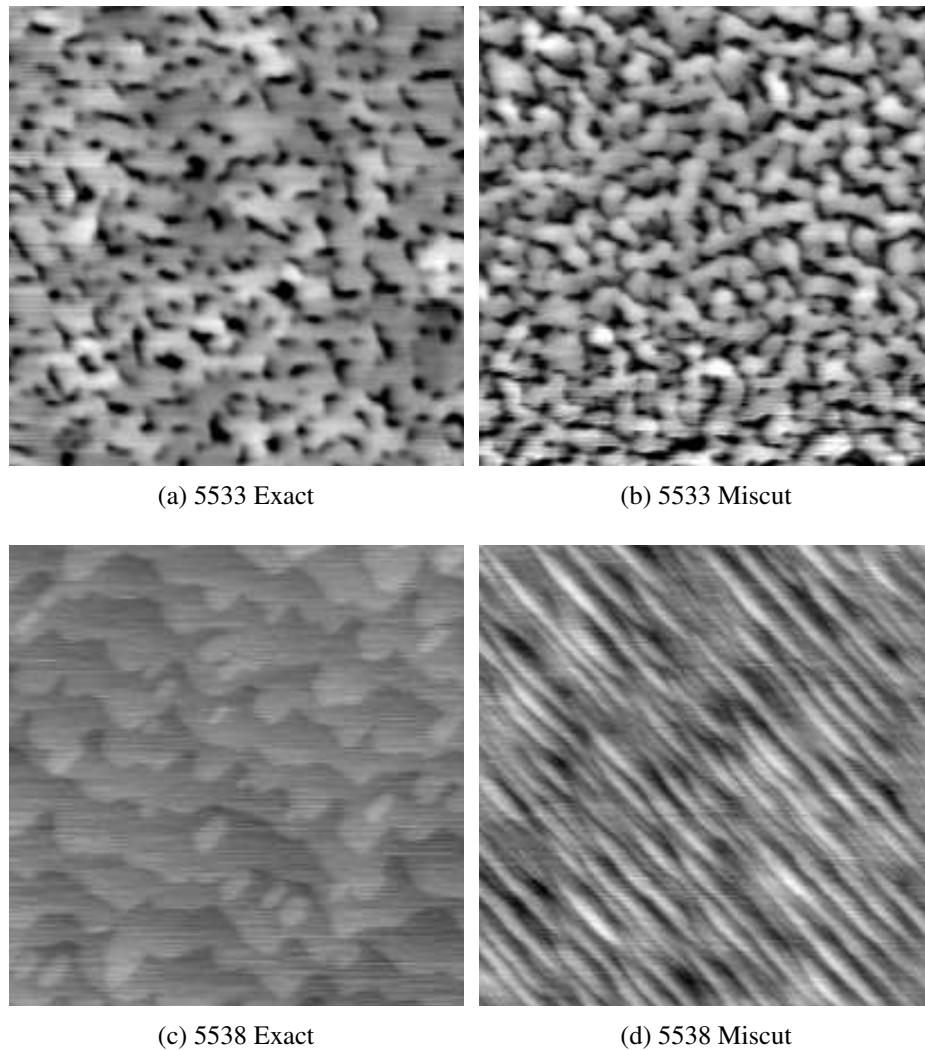
Figure 6.4: Comparison of the improvement of the AlAs layer quality on miscut and exact substrates by refinement of growth parameters. All scan dimensions are 2 μm. Vertical scan range is 2 nm. Samples (a) and (b) were grown at 600°C with a V:III ratio of 5. Samples (c) and (d) were grown at 550°C with a V:III ratio of 12. The RMS surface roughnesses are (a) 0.39 nm, (b) 1.72 nm, (c) 0.16 nm and (d) 0.28 nm.
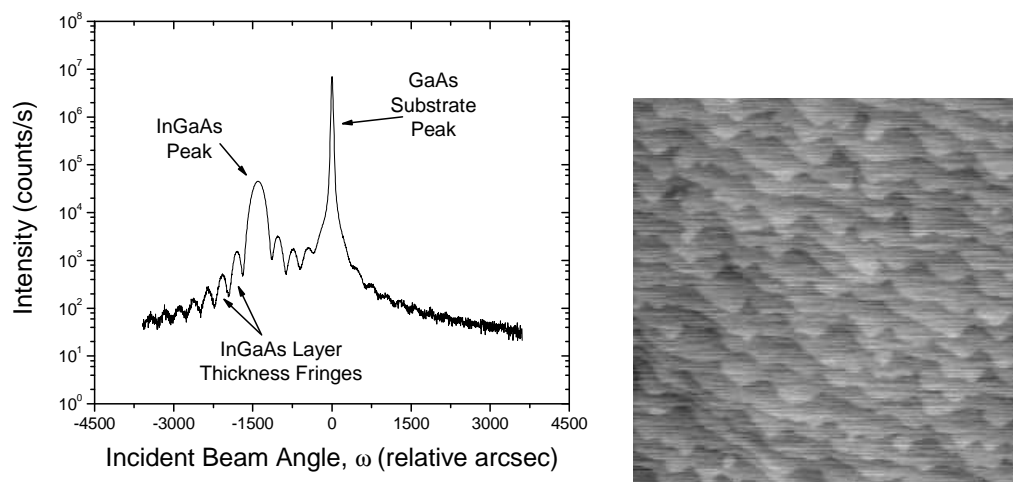
Figure 6.5: XRD and AFM data from sample 5539, a single strained $In_{0.078}Ga_{0.922}As$ layer. The layer thickness was calculated to be 69.8 nm and the RMS surface roughness to be 0.15 nm. AFM scan dimensions are 2 μm with a vertical scale of 1 nm.

6.2   Full Structure Samples

Having determined the growth conditions for each material, pseudomorphic heterostructures shown in Fig. 5.1 consisting of a 50 nm thick AlAs layer, followed by a GaAs layer, an $In_{0.08}Ga_{0.92}As$ layer and a GaAs cap layer with thickness equal to that of the first GaAs layer were grown on quarters of 2 inch diameter semi-insulating exact GaAs(001) substrates by MOCVD.

The samples were grown at 550°C and 50 Torr using triethylgallium, tertiarybutylarsine (TBAs) and trimethylindium, with hydrogen as a carrier gas. The V-III ratio was ∼13 for the GaAs layers and ∼11 for the InGaAs layers. Layers were grown at a growth rate of 2 μm/h. The InGaAs alloy composition provided a mismatch of 0.56%, as calculated by equation 3.3. The ratio of layer thickness of the InGaAs to GaAs was changed to achieve varied degrees of elastic strain relaxation of the InGaAs layer. Five different sample layer structures were grown with the GaAs/InGaAs/GaAs thicknesses in nanometers as follows: 50/100/50, 30/60/30, 20/100/20, 15/100/15 and 10/100/10. The InGaAs layer thicknesses were chosen to be below the critical thickness determined by Orders and Usher[35] and lie above the Matthews-Blakeslee critical thickness as shown in fig. 6.6. The square and circle indicate the point where the two different $In_{0.08}Ga_{0.92}As$ thicknesses used in this experiment lie relative to the Matthews-Blakeslee critical thickness (line), and previous experimental data (diamonds)[35, 29]. This indicates that while dislocations begin to move within the InGaAs layers, the density of the misfit dislocations is not high enough to cause a detectible shift in the lattice parameter.

These samples were analyzed by both XRD and AFM techniques. The X-ray rocking curve scans, shown in Fig. 6.7, exhibited thickness fringes for both 100nm- and 60nm-thick InGaAs layers. These fringes confirmed that there was negligible strain-relaxation due to the introduction of dislocations during MOCVD growth. However, the surface morphology was found to vary with the InGaAs layer thickness as shown in Fig. 6.8. A light cross-hatch pattern could be seen on the surface of the sample with the 100 nm-thick InGaAs layer indicating a minimum linear density of 0.9/μm misfit dislocations, as counted from the AFM image, assuming each visible line on the image corresponds to a single dislocation. Few dislocation-related surface steps were seen on the sample having a 60 nm-thick layer, having a density of 0.2 dislocations/μm. The strain relieved by misfit dislocations
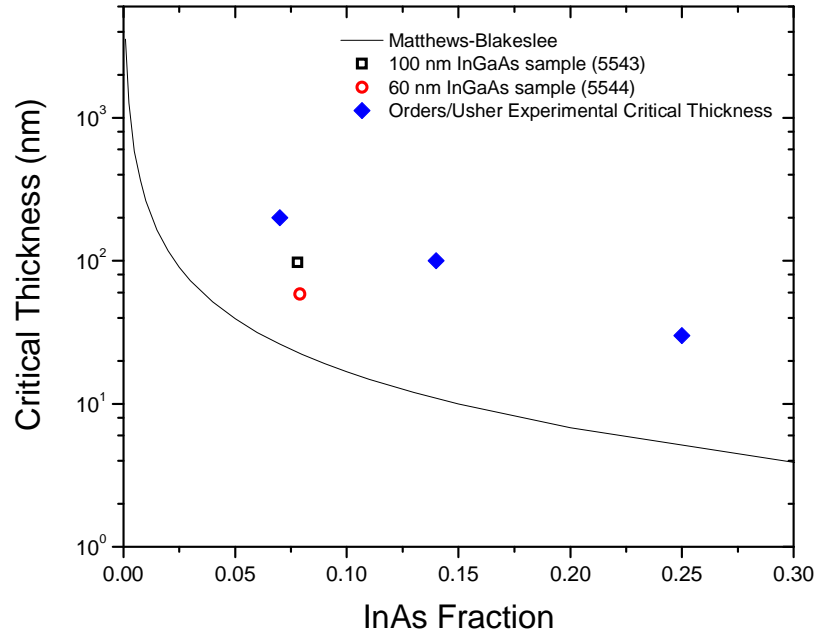
Figure 6.6: Data points for the two different thicknesses of In$_x$Ga$_{1-x}$As used in this experiment (square & circle) overlayed on Matthews-Blakeslee theory (equation 3.9) and experimental data points for the critical thickness of various InAs % samples as measured by x-ray diffraction are also shown (diamond)[35].

is $\frac{|\vec{b_\perp}|}{D}$, where D is the spacing between dislocations. For the 100 nm-thick InGaAs layer samples, this corresponds to a strain of $\approx 2 \times 10^{-5}$ being relieved by the dislocations. This corresponds to a reduction of the initial strain in the layer by 0.4%, a negligible amount, so the presence of thickness fringes on the X-ray rocking curves are not surprising. However, the RMS roughness of both samples was 0.15 nm, comparable to that of a bare GaAs substrate.
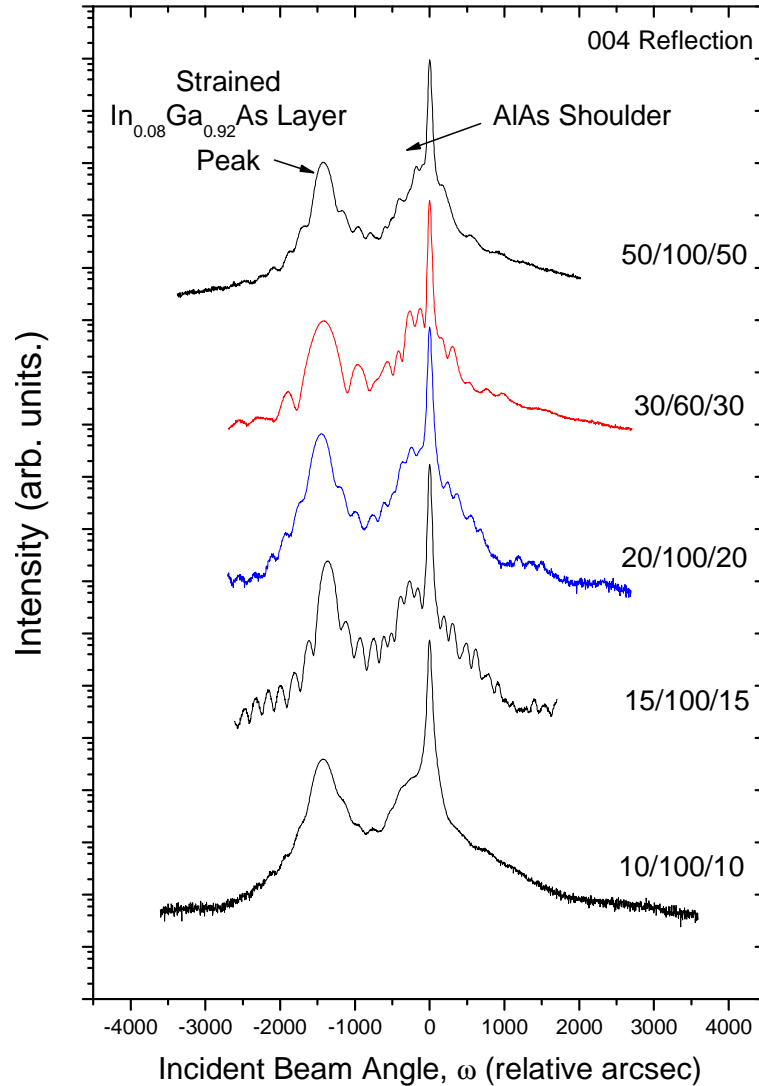
Figure 6.7: Rocking curve scans of blanket 5543 (50/100/50), 5544 (30/60/30), 5561 (10/100/10), 5562 (20/100/20) and 5633 (15/100/15) demonstrating presence of thickness fringes. These fringes indicate that the InGaAs layer is smooth and uniformally strained to within the sensitivity of X-ray diffraction.
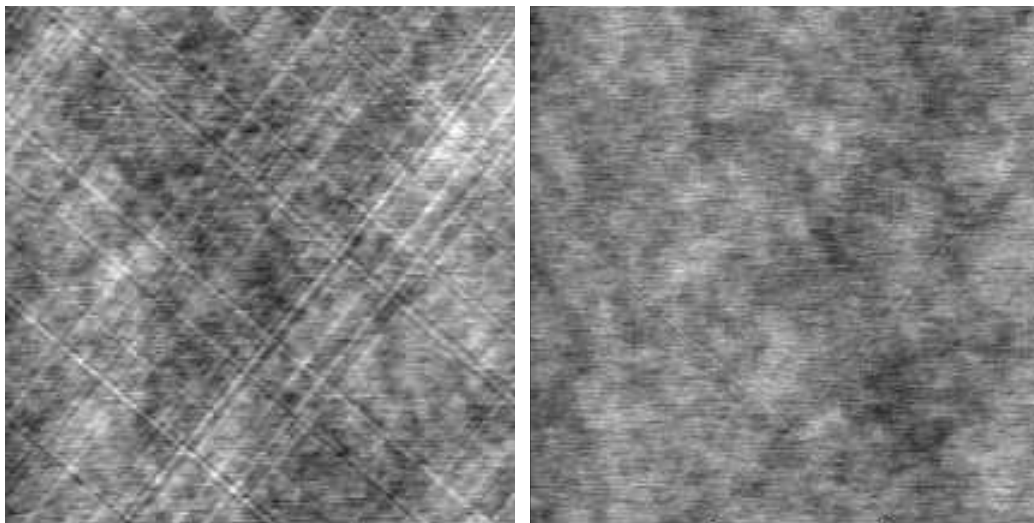
Figure 6.8: AFM scans of samples 5543 (50/100/50) (left) and 5544 (30/60/30) (right). Measured $In_{0.08}Ga_{0.92}As$ layer thickness of 97.3 nm and 58.5 nm respectively. InAs alloy composition of both samples is 8%. Scan dimensions are 30x30 μm. The cross-hatch pattern on the left hand image is from surface steps resulting from underlying misfit dislocations, the right image shows a few surface steps due to dislocations. The RMS roughness of both samples is 0.15 nm.

6.3 Determination of Sample Properties via Simulation

The sample layer thicknesses and InGaAs alloy compositions were determined from triple-axis XRD measurements taken for all samples. The triple-axis measurements were used in preference to rocking-curve measurements as they have a significantly lower background, allowing for a more accurate matching of the simulation to the measured data. Values of the thickness of each layer and InGaAs alloy composition were determined using the Panalytical X'Pert Epitaxy analysis software[10]. The fitting procedure was initiated by a simulation using the target values of layer thickness and InGaAs alloy composition with the assumption that the two GaAs layers were of equal thickness. An example of measured data and the corresponding fit are shown in Fig. 6.9. Note that the calculated scan faithfully
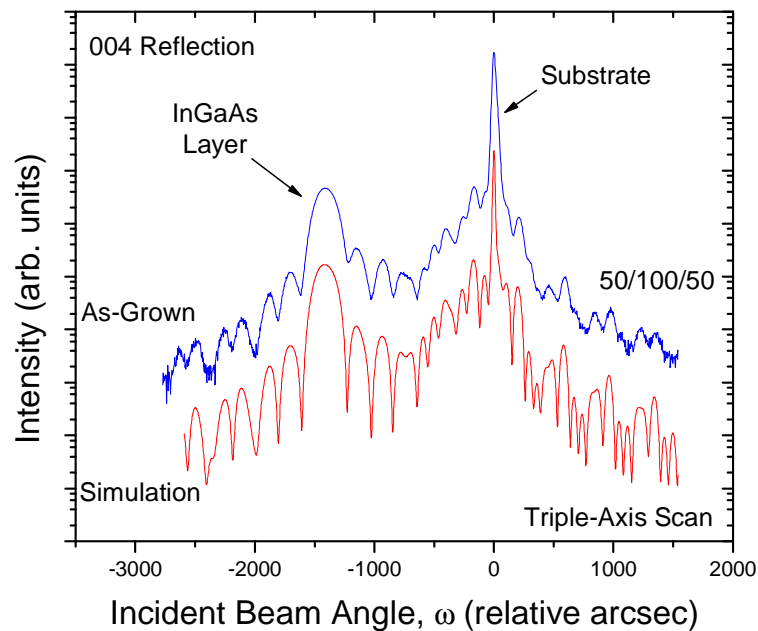
Figure 6.9: Comparison of measured and simulated scans for sample 5555 (50/100/50)

reproduced the structure of the data over six orders of magnitude of intensity.

Table 6.2 lists the samples grown for this experiment, and the layer thicknesses determined by the simulation. It also lists the surface roughness as measured by the AFM. In all cases, the target indium alloy composition was 8% and the target AlAs thickness was 50 nm. Uncertainties in thicknesses and composition were estimated from the minimum change in

Table 6.2: Initial measured sample properties.

Sample Number	Target Thickness (nm)	AlAs Thickness (nm)	GaAs Thickness (nm)	InGaAs		RMS Roughness (nm)
				InAs %	Thickness (nm)	
5543	50/100/50	44.7 ± 0.5	50.1 ± 0.5	7.8 ± 0.1	97.3 ± 0.5	0.16 ± 0.02
5544	30/60/30	46.5 ± 0.5	31.5 ± 0.5	7.9 ± 0.1	58.5 ± 0.5	0.15 ± 0.02
5552	30/60/30	46.0 ± 0.5	31.0 ± 0.5	7.8 ± 0.1	58.6 ± 0.5	0.16 ± 0.02
5555	50/100/50	47.9 ± 0.5	51.9 ± 0.5	7.8 ± 0.1	98.2 ± 0.5	0.23 ± 0.02
5556	50/100/50	42.4 ± 0.5	50.8 ± 0.5	7.8 ± 0.1	99.4 ± 0.5	0.24 ± 0.02
5558	30/60/30	44.5 ± 0.5	30.3 ± 0.5	7.9 ± 0.1	58.0 ± 0.5	0.26 ± 0.02
5559	50/100/50	46.4 ± 0.5	51.2 ± 0.5	7.9 ± 0.1	99.0 ± 0.5	0.27 ± 0.02
5560	10/100/10	39.9 ± 0.5	10.4 ± 0.5	7.8 ± 0.1	97.3 ± 0.5	0.24 ± 0.02
5561	10/100/10	42.5 ± 0.5	10.7 ± 0.5	8.0 ± 0.1	96.5 ± 0.5	0.25 ± 0.02
5562	20/100/20	43.1 ± 0.5	21.3 ± 0.5	8.0 ± 0.1	97.9 ± 0.5	0.23 ± 0.02
5633	15/100/15	50.0 ± 0.5	16.6 ± 0.5	7.6 ± 0.1	108.3 ± 0.5	0.23 ± 0.02

value that causes a visible detectible difference between the simulation and the measured data. Variation in layer composition and thickness across the sample will additionally contribute to errors in these measurements. The uncertainty in roughness was determined by examining the changes in the RMS roughness calculated from different areas of the AFM image.

Chapter 7

Sample Processing

All samples were fabricated in the cleanroom environment. The procedure involved performing conventional photolithography to apply a pattern of photoresist to the samples, the samples were then etched using two different etches according to the in-place bonding method discussed in chapter 5. A few problems occurred during the course of fabrication, discussion of these issues and their solutions is included in this chapter.

7.1   Standard Cleanroom Procedure

Figure 5.2 illustrated the process steps of the in-place bonding method. The samples were first coated with photoresist by using a standard coating process involving spinning each piece for 30 seconds at 3000 revolutions per minute. This yielded a photoresist thickness of 1.2 μm. The samples were then pre-baked at 90°C for 60 seconds to dry the photoresist and prepare it for exposure. The photoresist was then patterned to form a 10 mm by 10 mm array of nominally 10 μm or 20 μm squares by using a mask to expose desired sections to 365 nm wavelength light (i line) for 10 seconds. The sample was then hard baked at 110° for 60 seconds to set the resist prior to development. The resist was then developed in AZM Developer solution, for 60 seconds until the exposed areas of resist had been washed away. A picture taken using a microscope in the cleanroom showing a section of the photoresist on a sample to be patterned into an array of 10 μm squares is shown in Fig. 7.1(a). The 3:1 citric acid/hydrogen peroxide mixture discussed in section 5.2, page 5.2, was used to etch the GaAs and InGaAs layers at equal rates (Fig. 5.2(b)) [9]. This etch typically took

(a) Photoresist

(b) Post-citric Etch

(c) Post-HF Etch

(d) Photoresist Removed
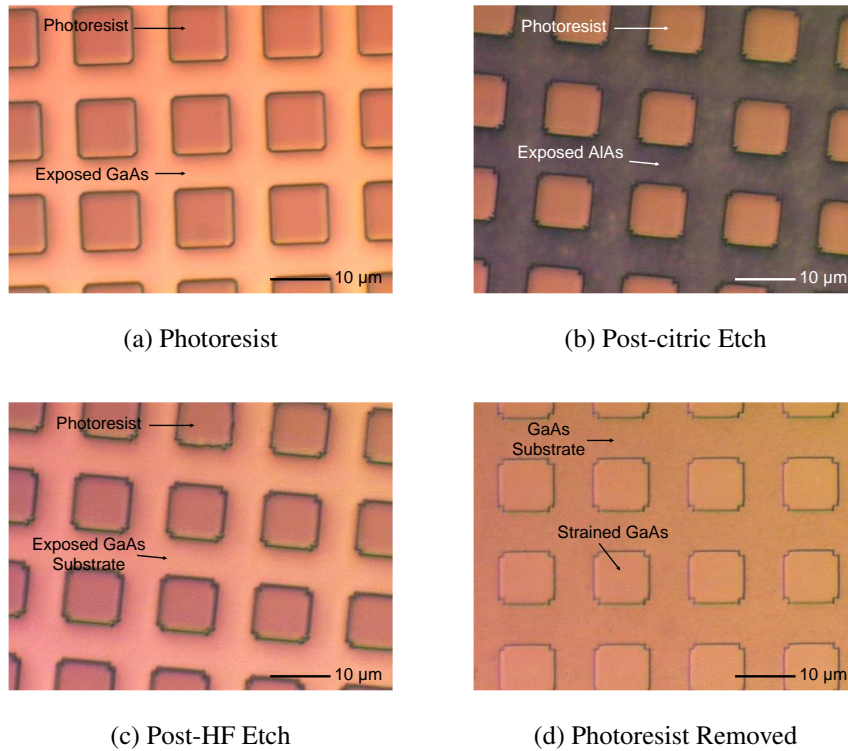
Figure 7.1: Microscope photos of a sample at various stages of cleanroom fabrication.

between 60-100 seconds, depending on the thickness of the trilayer structure. When the AlAs is exposed, it is dark in colour compared to the surrounding wafer, this provides a visible end point for the etch, as shown in Fig. 7.1(b). Because the citric/hydrogen peroxide etch does not remove the underlying AlAs layer and has a visible end point, the timing of this etch does not require precision, and can be allowed to proceed until the end point is observed. Following the etch, the sample was then rinsed in DI water for 5 minutes, dried, and examined with a microscope to look for irregularities and verify the visual end point. The photoresist layer was left in place to protect the surface of the square features, and the sacrificial AlAs layer was then removed by selective etching in 49 % hydrofluoric (HF) acid as discussed in section 5.2 (Fig. 5.2(c)). This etch process separates the GaAs/InGaAs/GaAs stack from the GaAs substrate in the GaAs layers. Etching continues until all of the AlAs layer has been removed from beneath the stack, and the stack, now with a partially relaxed InGaAs layer and strained GaAs layers, lies flat in its original place on the substrate (Fig.

5.2(e)). As this etch occurs very rapidly, it was timed for 10-15 seconds, and the sample was then immediately placed in a DI water rinse for 5 minutes. A microscope picture of the sample following HF etching is shown in Fig. 7.1(c). Notice that the dark AlAs underlayer which is visible in Fig. 7.1(b) has now been completely removed. Note also that there has been no noticeable shift in the positions of the patterned squares. The photoresist was then removed using acetone. The GaAs/InGaAs/GaAs stacks remain bonded to the substrate by van der Waal's forces after the sample is removed from the etch solution and dried, as shown in Fig. 7.1(d). Observe, in particular, that the squares show no signs of bending or bubbling, indicating that they are lying flat on the substrate.

7.2 Processing Problems

A few problems occurred during the processing stages which provided temporary setbacks or prompted design reconsiderations. These problems included irregular photoresist exposure patterns and difficulties with samples not remaining on the spinner when applying photoresist.

Initial photoresist exposure tests using whole 2 inch wafers were performed to determine optimal exposure times. These tests yielded consistent results for both 10 μm and 20 μm patterns as shown in Fig. 7.2. However, the samples to be fabricated were quar-
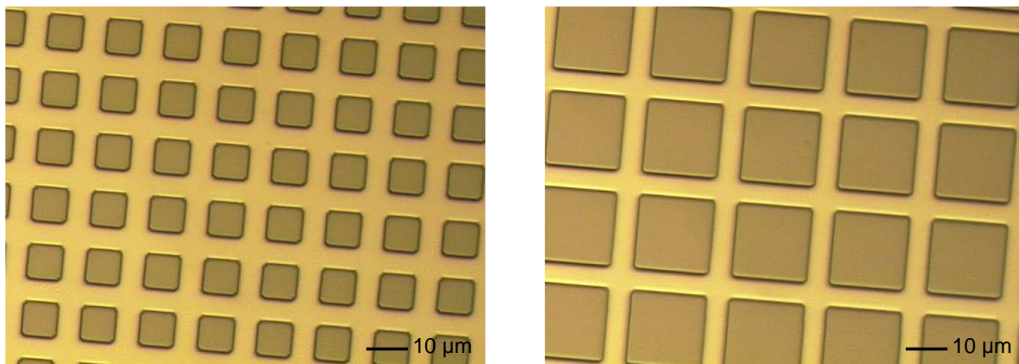

Figure 7.2: Whole wafer photo resist patterns, demonstrating both the 10 and 20 μm arrays.

ters of 2 inch wafers. These had to be mounted on whole wafers using photoresist as a

temporary adhesive to properly position them under the mask, because the mask aligner does not have sufficient range of motion to allow for a single quarter wafer to align with the desired part of the mask. Initial photoresist patterned on a sample attached to a whole wafer are shown in Fig. 7.3. Note that the edges have a spiked pattern to them; the size of the photoresist squares following development is inconsistent across the sample; and the total surface coverage of the photoresist is lower than intended. Thus, the XRD signal from the structures following processing will be lower in intensity. It was determined that this
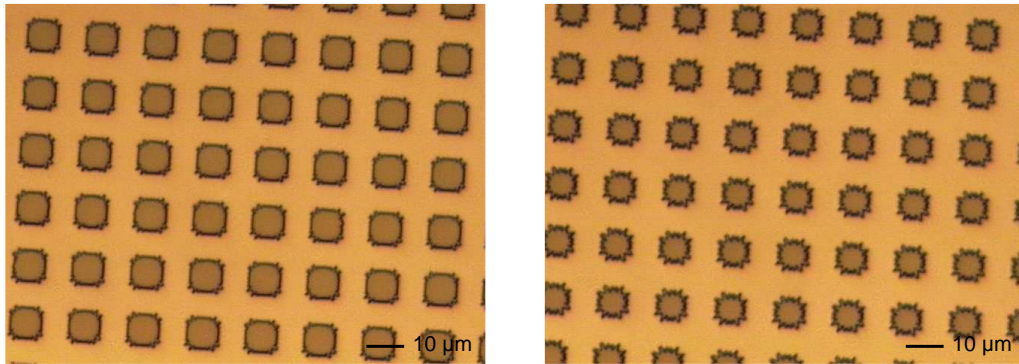
Figure 7.3: Two pictures of photoresist following development on sample 5543, note the variation in size of the squares and the spiked edges.

discrepancy between whole wafer resist patterns and quarter wafer resist patterns was in part a result of the unequal height of the sample and the underlying wafer to which the sample was attached. In particular, if only one sample was being exposed, the photoresist would be closest to the desired pattern nearest to the square corner of the quarter wafer, and would decrease in quality toward the edges of the sample. In order to offset this height difference and improve the quality of the photoresist pattern which resulted, pieces of older samples were attached to the supporting wafer to serve as spacers to provide a more consistent surface height across the wafer. This resulted in a noticeable improvement in the size and edge quality of the photoresist following development as shown in Fig. 7.4. However, there remain areas where the photoresist demonstrates spiked edges and lower coverages. These areas could not be entirely eliminated, though they did not represent a majority of the photoresist pattern on any sample processed using spacers. It should be noted that this
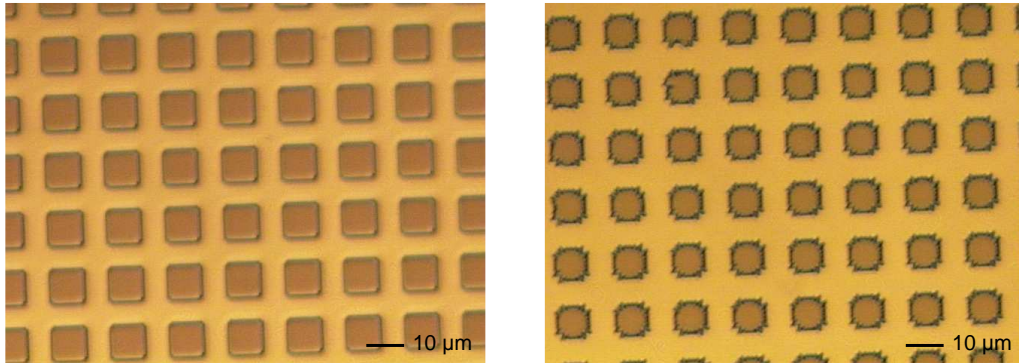
Figure 7.4: Two pictures of photoresist following development on sample 5555 where efforts were made to offset the height difference across the sample.

problem can probably be eliminated by designing a new mask with the area to be patterned in the center of the mask. However, this was unnecessary for the purposes of the proposed experiment.

Another problem that was encountered was poor sample adhesion to the spinner while applying photoresist. Photoresist is applied to a sample by placing a drop of liquid photoresist on the sample and then spinning the sample at 3000 rpm. During the spinning process, the sample is held to the spinner by a vacuum applied through a small hole in the center of the spinner (Fig. 7.5a). Due to the size of the samples, the spinner suction was not sufficient to consistently keep the quarter wafer pieces on the spinner while coating the sample with photoresist. The initial spinner piece provided only a single hole centered on the axis of rotation to provide suction. Whole wafers are coated by using no inserted piece, with the suction force distributed over the back of the wafer via channels cut within the spinner (Fig. 7.5b). A solution was achieved by designing a new insert piece which takes advantage of the existing channels to distribute the suction force in a rough square over the back of a quarter wafer piece. Figure 7.5c shows the replacement piece used to increase the suction force by increasing the surface area of a quarter wafer that is exposed to the vacuum.

Despite these difficulties, both 10 μm and 20 μm structures were successfully created in 50/100/50, 30/60/30, 20/100/20 and 10/100/10 samples using the above described cleanroom procedures. These structures, as defined by photolithographic processes, were bonded
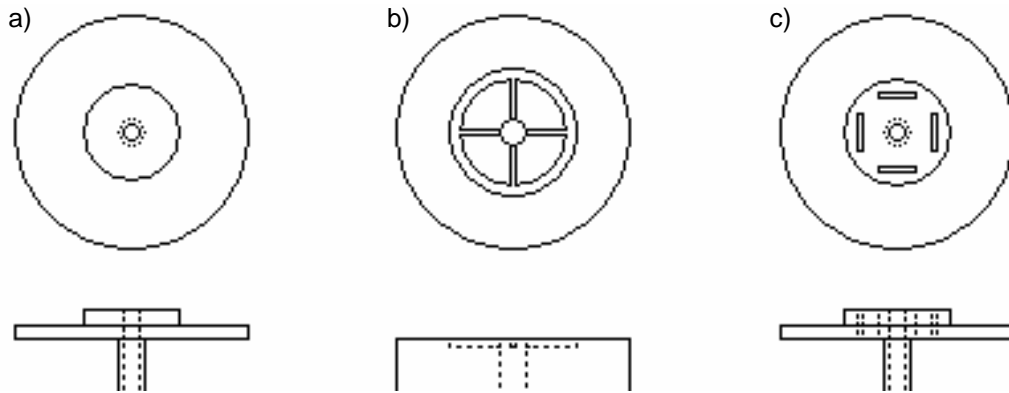
Figure 7.5: Engineering diagram of a) the spinner insert initially used for coating small wafer pieces, b) the chuck of the spinner used for whole wafer coating, which part (a) nests in, c) the piece designed to nest in (b) but makes use of the channels for additional vacuum pressure.

weakly to the substrate following fabrication. While all fabricated structures show lithographic defects at the corners, photoresist patterns created on whole wafers indicate that a slight modification in the cleanroom process will eliminate such defects.

While the 10 μm samples demonstrate flat surfaces when observed by AFM and optical microscopy as shown in fig. 7.1, the 20 μm structures show bumps when observed with optical microscopy as shown in Fig. 7.6. It appears that these bulges are a result of the edges of the square structure being unable to slide far enough to accommodate the increased structure size. This prevents the structure from lying flat on the substrate after the AlAs layer has been removed. This problem may be alleviated by increasing the AlAs layer thickness and using an etchant with a slower etch rate. Increasing the AlAs layer thickness would decrease the amount of contact area between the freed structure and the substrate during the early stages of the etch. This would decrease any friction forces, allowing the structure to continue to slide across the substrate during etching. Decreasing the etch rate would increase the amount of time during which the structure can expand by sliding before the increasing friction force between the substrate and structure prevents further expansion. Consequently, obtaining flat, large features may be possible with the use of both slower etch rates and thicker sacrificial layers.
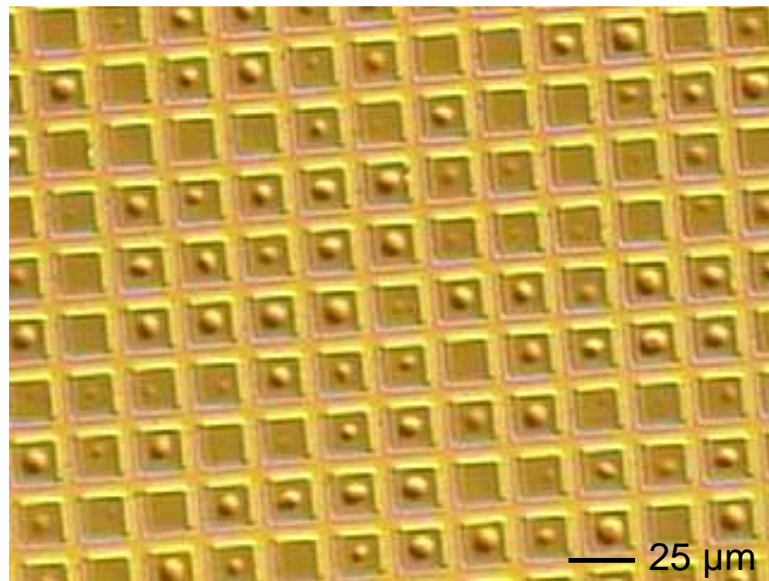
Figure 7.6: Optical microscopy image of sample 5559 patterned in a 20 μm structure array.

7.3 Summary

This chapter has discussed the cleanroom fabrication procedure applied to the samples used in this experiment. The process involves conventional photolithography, followed by two selective etches to achieve initial weak in-place bonding of the GaAs/InGaAs/GaAs heterostructure. All four structures have been successfully fabricated using this method. Additionally, two different sizes of features, 10 μm and 20 μm, were created with this method. A detailed analysis of all structures processed is presented in the following chapter.

Chapter 8

Post-Processing Analysis

The strain relaxation and surface quality of the samples was measured following processing. The strain relaxation was determined from XRD, while the surface quality was measured by AFM. The strain relaxation measured from these processed samples was compared to the expected strain relaxation calculated from the force-balance model discussed in chapter 4.

8.1   Strain Relaxation

After fabrication, the samples were again measured by XRD. As shown in fig. 8.1, it was found that the InGaAs layer peak had consistently shifted toward the substrate peak while maintaining both its shape and thickness fringes. Note that the weaker InGaAs signal is due to the smaller area of the patterned samples. This shift of the XRD peak indicates that the out-of-plane lattice constant is smaller and therefore that the compressive biaxial strain in the InGaAs layer is reduced. The shoulder on the high angle side of the substrate peak indicates that the out-of-plane lattice constant of the two thin GaAs layers is also reduced, and, therefore, that these layers are under tensile strain. The unchanged shape of the InGaAs peak and the presence of the thickness fringes indicate that the change in strain occurs elastically, since significant mosaic broadening of the XRD peak is observed when this amount of strain relaxation occurs by the introduction of misfit dislocations[32].

Using the values of the layer thicknesses and InGaAs composition determined from the XRD measurement prior to patterning the sample, the degree of strain relaxation in the In-
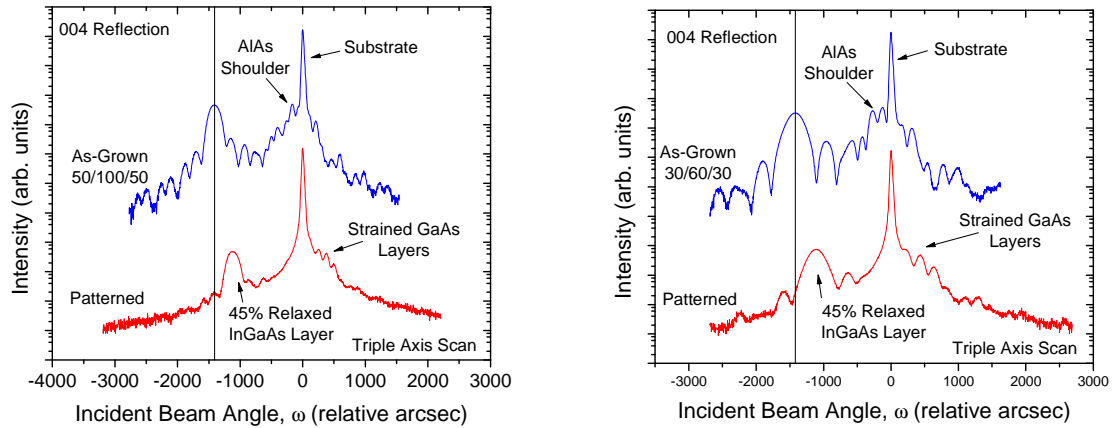
Figure 8.1: Triple axis XRD measurements of (left) sample 5555 (50/100/50), and (right) sample 5558 (30/60/30) both before and after fabrication. Note that the AlAs layer peak is absent in the patterned samples. Relaxation percentages derived from a simulation using layer thicknesses and compositions of the sample prior to processing and adjusting only the relaxation percentage of the InGaAs layer.

GaAs layer was determined by means of a simulation. Only the degree of strain relaxation was adjusted until the simulated and measured InGaAs layer peaks were aligned. Strain relaxation can be analyzed in terms of the force-balance model described in section 4.1, which models strain sharing between the layers of a free-standing structure according to their relative thickness[34, 13]. The strain relaxation experienced by samples which were successfully processed is listed in table 8.1. In particular this table shows a few notable trends. Firstly, arrays of both 10 and 20 μm structures result in similar strain relaxation. This indicates that the increased size of the square features did not interfere with the strain relaxation process. Secondly, the measured strain relaxation is, in general, slightly lower than the expected strain relaxation. This discrepancy between the theoretical and experimental strain relaxation can be accounted for by either a retarding friction force caused by contact with the substrate during relaxation, which acts against the expansion of the freed structure, or the photoresist layer which is present during relaxation, but is not considered in the model. Figure 8.2 compares the measured strain relaxation of the InGaAs layer with that calculated from the force-balance model. However, lower than expected strain relax-

Table 8.1: Measured strain relaxation of processed samples

Sample Number	Sample Array Size (μm)	Target Thickness Values	Measured Thickness Values	Expected Strain Relaxation (%)	Measured Strain Relaxation (%)
5543	10	50/100/50	50.1/97.3/50.1	49.3	45.0 ± 3
5544	10	30/60/30	31.5/58.5/31.5	48.1	48.0 ± 3
5555	10	50/100/50	51.9/98.2/51.9	48.6	45.0 ± 3
5558	20	30/60/30	30.3/58.0/30.3	48.9	45.0 ± 3
5559	20	50/100/50	51.2/99.0/51.2	49.2	45.0 ± 3
5560	10	10/100/10	10.2/97.5/10.2	82.7	79.5 ± 3
5561	10	10/100/10	10.7/96.5/10.7	81.8	79.0 ± 3
5562	10	20/100/20	21.3/97.9/21.3	69.7	67.5 ± 3
5633	10	15/100/15	16.6/108.3/16.6	76.9	75.0 ± 3

ation has been observed in compliant substrate systems involving strain sharing[44].
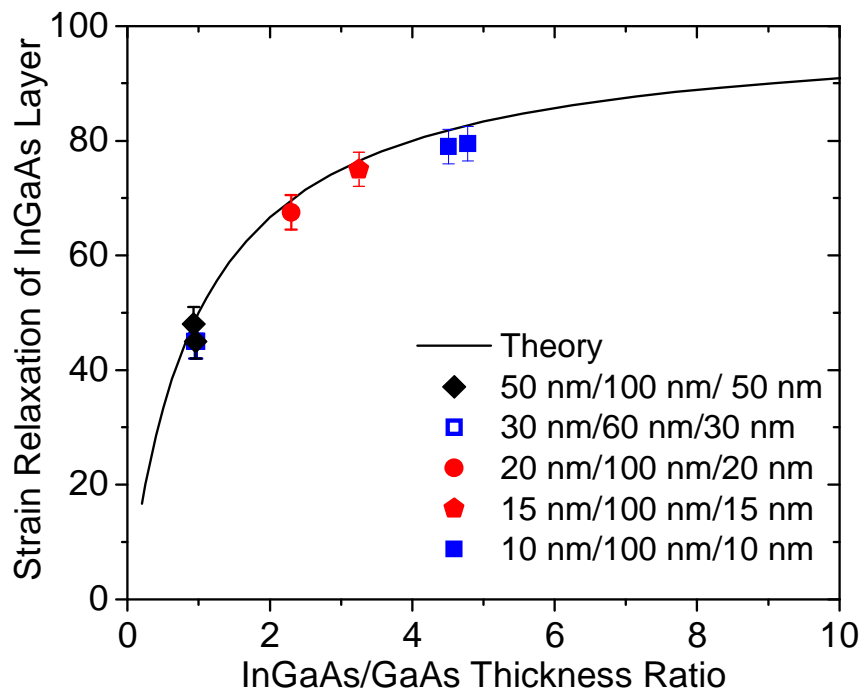
Figure 8.2: Measured strain relaxation of the $In_{0.08}Ga_{0.92}As$ layer for samples listed in table 8.1 patterned with 10 μm squares and that calculated from the force-balance model.

8.2 Surface Quality

AFM images of the surface of the square features, shown in fig. 8.3, demonstrate that the cross-hatch pattern and surface roughness are essentially unchanged after processing. In this case, the measured RMS roughness of both samples is 0.25 nm. This is further
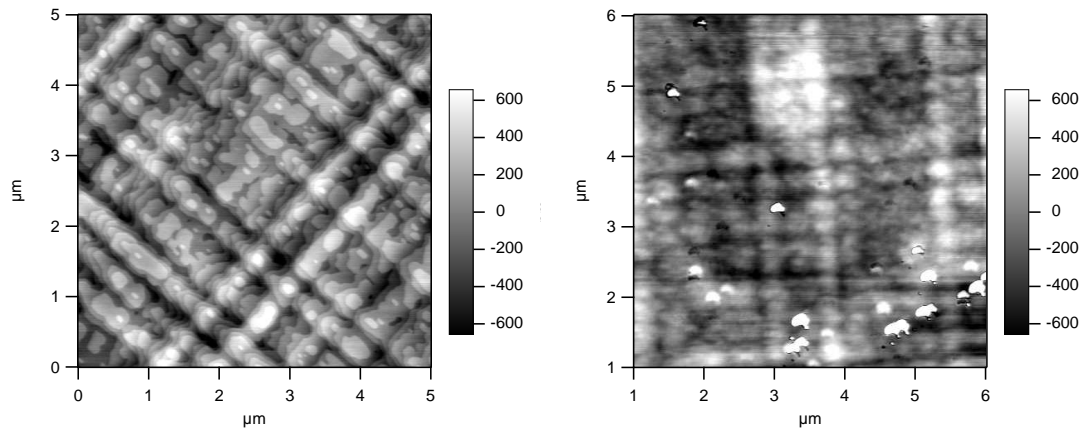
Figure 8.3: AFM measurements of sample 5555 taken before (left) and after (right) processing. The dislocation density is 0.9 /μm in both images.

evidence of elastic strain-relaxation, since epitaxial layers having a similar degree of strain relaxation via misfit dislocations typically have significantly rougher surfaces [32, 5]. The particles visible on the processed sample are most likely photoresist residue which did not completely wash away during the final stage of processing.

Optical microscope images of 10 μm structures, along with AFM images indicated that the structures are lying flat on the surface following processing as shown in fig. 8.4. The step height between the substrate and structure surface as measured by the AFM is 200 $\pm$ 5 nm, which matches the total sample layer structure thickness of 200 nm.

Figure 8.4: Microscope and AFM images of sample 5555 patterned in a 10 μm structure array.

Chapter 9

Bond Strengthening and Testing

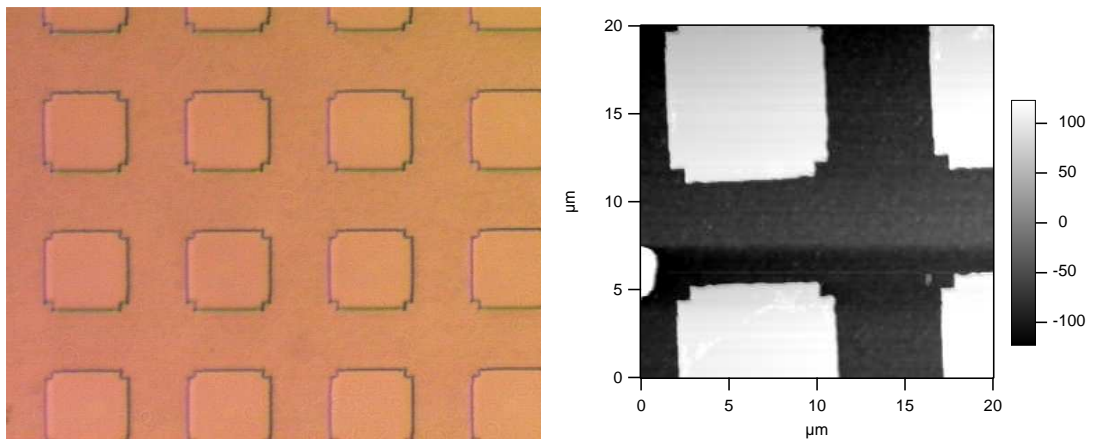Following the cleanroom processing, the structures are weakly bonded to the substrate by van der Waals forces. In order to improve the strength of the bond, an anneal must be performed to create covalent chemical bonds between the structure and substrate. To form these bonds, sample 5543 (50/100/50) was annealed at 400°C for 2 hours in the MOCVD reactor while stabilizing the surface with TBAs. This annealing time and temperature are used for whole wafer bonding of GaAs to GaAs and provided a surface bond energy of 0.7 J/m^2 in that case[18]. Due to the small size of the features, the standard method of measuring the strength of a wafer bond, described in chapter 2, cannot be used. Consequently, only one sample has been annealed awaiting a quantitative method of measuring bond strength. However, it is possible to qualitatively assess the bond strength through a cleave test and an etch test.

9.1   Cleave Test

One of the methods used to qualitatively test whether the strength of the bond between the strain-relaxed layer structure and the substrate had increased was a cleave test. This test involves cleaving a processed sample through the patterned area, structures which lie along the cleave line will either cleave or remain intact. If the structures remain intact, the bond strength between the substrate and the structure is weak compared to that of covalent bonds. However, if the structures cleaves, the substrate-structure bond strength is on the order of a covalent bond. In this case, both an annealed (5543) and an unannealed (5555) sample

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were cleaved and then the resulting cleaved edge was examined using optical microscopy as shown in fig. 9.1. The difference between the two samples was immediately apparent.
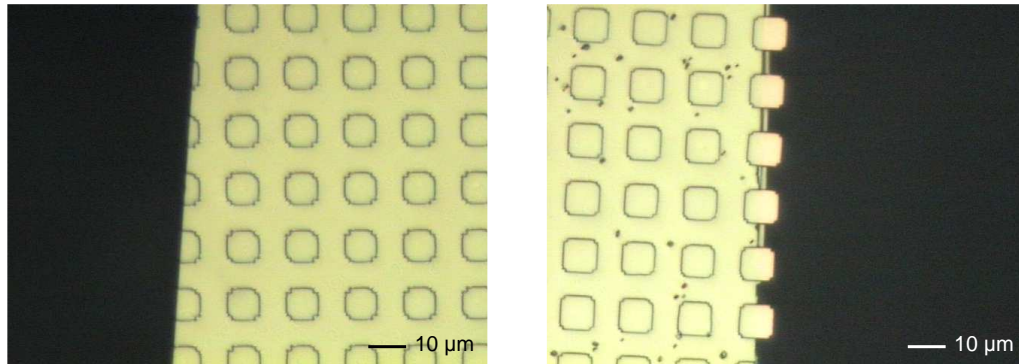

Figure 9.1: Microscope pictures of annealed sample 5543 (left) and unannealed sample 5555 (right) (50/100/50).

Structures on the annealed sample were cleaved along with the substrate, even when a very small portion of the structure remained on the examined piece. In contrast, structures on the unannealed sample remained whole and overhung the cleaved edge of the substrate or were absent entirely. This qualitatively shows that the bond strength between the structure and the substrate had increased to such a point that it was now comparable to that of covalently bonded as grown crystal. This comparison can be made as the surface area of the cleaved edge of the structure is on the order of the surface area of the structure portion remaining on the substrate. Consequently, the bond strength per unit area of the structure-substrate bond is on the order of the bond strength per unit area of the covalent structure bonds which have been cleaved, as the areas of the cleaved structure and structure-substrate bond are within an order of magnitude. In this case, the total thickness of the structure is 200 nm and fig. 9.1 the smallest of portions remaining are <1 μm wide.

9.2 Behaviour of Etched Samples

The second method of assessment involved the removal of the upper GaAs layer and part of the InGaAs layer using the citric acid etch. Optical inspection of the patterned structures indicates that they are flat, as shown in fig. 7.1(d). However, a comparison of the annealed

and unannealed samples after the additional etching, shown in fig. 9.2, reveals that while the annealed sample shows no visible change, the unannealed sample shows that some features appear to have bowed upwards at the center. This bowing occurs because once the upper
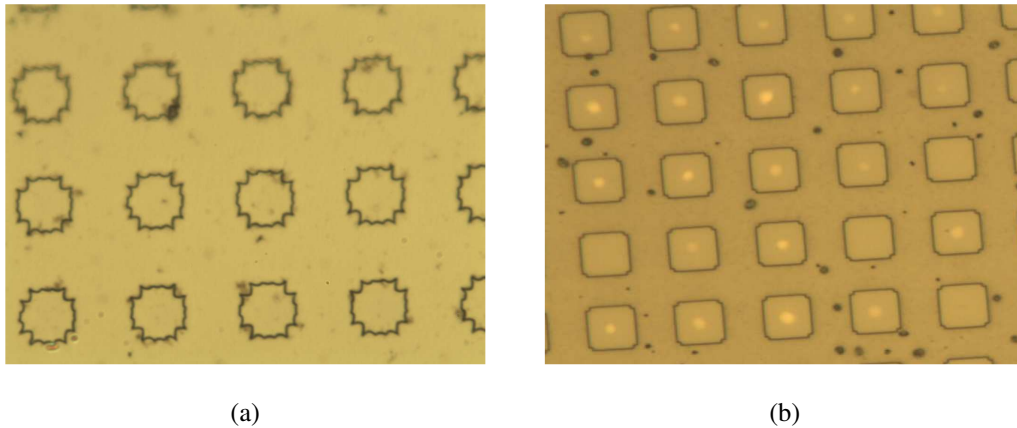

(a)   (b)

Figure 9.2: Microscope pictures of annealed sample 5543 (left) and unannealed sample 5555 (right) after removal of upper GaAs layer and part of InGaAs layer. Light patches in the right picture are due to optical interference from the air gap.

GaAs layer has been removed, the bending forces can no longer be neglected and our simple model of the strain relaxation no longer applies. A free-standing InGaAs/GaAs structure would bend, as described in section 4.1, as the InGaAs layer expands and the GaAs layer contracts in response to the lattice mismatch. An AFM line scan across a feature on the unannealed sample shows that the height of the bump is $\sim$15 nm, as shown in fig. 9.3 While a similar line scan indicated that the features remain flat in the annealed sample, the bonding forces must be strong enough to overcome the bending forces. It should be noted that the surface of the sample that was not annealed is much rougher than the sample which was annealed, however the reason for this difference is not understood. Therefore, unless post fabrication annealing is done to strengthen the bond, the bending forces seem to be stronger than the bonding forces. The combination of cleaved structures, static x-ray diffraction peak position, and lack of bowing demonstrates that the bond between the lower GaAs layer and the GaAs substrate is stronger after the 400°C anneal.

If there is a strong bond, it is expected that the strain in the InGaAs layer would be
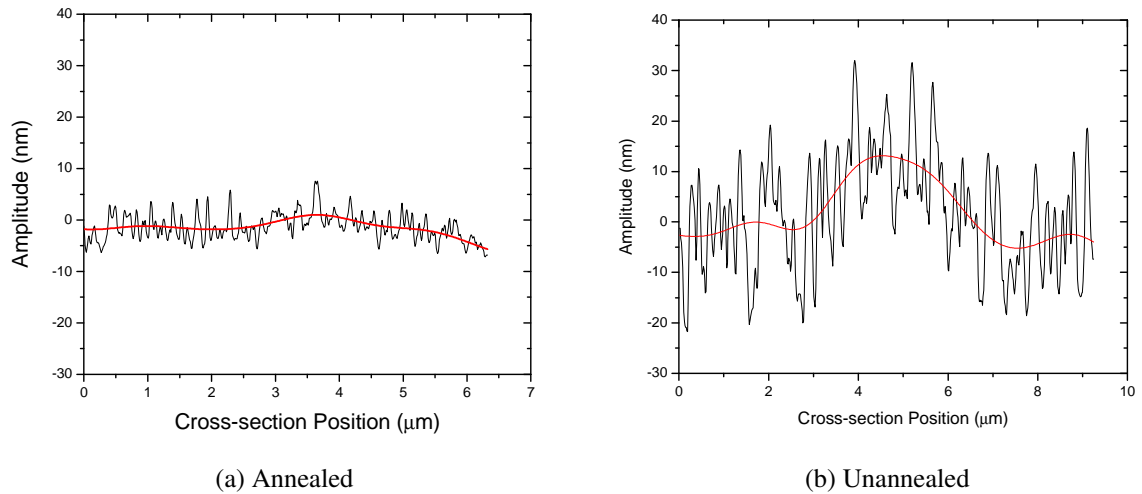
(a) Annealed

(b) Unannealed

Figure 9.3: AFM line scan across features from fig. 9.2. The scan of the annealed sample verifies that it remains flat to within $\pm$ 3 nm following etching. The height of the bump of the unannealed sample is 15 nm. Both scans were smoothed using the 75 point fast-Fourier transform algorithm in Origin 7.5.

unchanged following removal of the top GaAs layer. If the bond is weak, the strain sharing between the GaAs and InGaAs layers would change when the layer thicknesses are changed and behave as in the two layer model discussed in section 4.1. Figure 9.4 shows XRD measurements of the annealed sample before and after etching, demonstrating that the InGaAs layer peak does not shift position. The change in the fringes indicates that the InGaAs layer thickness is $\sim$80 nm after etching. As well, the interference fringes on the strained GaAs peak from the pair of GaAs layers disappear, consistent with the removal of the upper GaAs layer. Clearly the bond strength after annealing is sufficient to maintain the strain in the InGaAs and underlying GaAs layers. The unannealed sample experiences an InGaAs layer peak shift consistent 10% strain relaxation, indicating that the InGaAs layer is thinner than the lower GaAs layer.
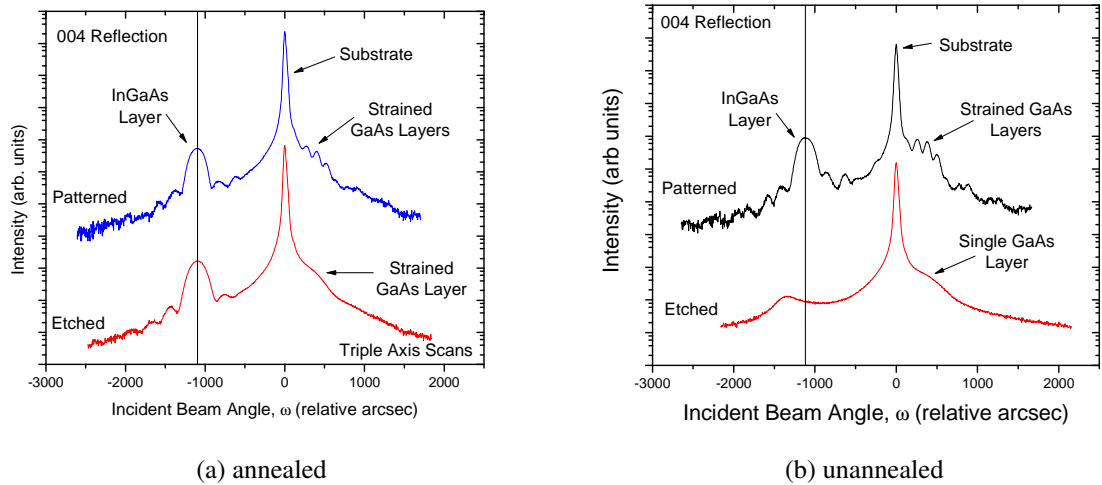
Figure 9.4: XRD measurements of annealed sample 5543 before and after etching (left) and unannealed sample 5555 before and after etching (right).

9.3 Summary

In order to improve the bond strength between the substrate and the structures, an anneal was performed on select samples under conditions similar to those used for whole wafer GaAs-GaAs bonding. A cleave test and an etch test were then performed on annealed and unannealed 50/100/50 samples. Each of these tests indicates qualitatively that the bond strength was improved following the anneal. However, neither of these methods provides a quantitative assessment of the bond strength, and consequently further experimentation is needed to determine the optimal annealing conditions to create the strongest bond.

Chapter 10

Conclusions

Bonding of elastically strain-relaxed GaAs/InGaAs/GaAs heterostructures to GaAs (001) substrates has been achieved by the in-place bonding method. When the AlAs layer is removed, the structure relaxes elastically without introducing additional dislocations. The spatial position of the squares remains unchanged since the edges of the squares bond in solution before the AlAs layer is entirely removed[8]. Subsequent annealing is needed to form a strong bond between the stack and the substrate. Both 10 μm and 20 μm structures have been fabricated with this method. The 10 μm structures lie flat on the substrate whereas the 20 μm structures have bumps in their centers. It is possible that these bumps could be eliminated by adjusting the initial AlAs layer thicknesses.

In this first implementation of the in-place bonding method for III-V semiconductors, the initial mismatch strain in the InGaAs layer was 0.56%. After bonding, the increase in the in-plane lattice parameter of the GaAs/InGaAs/GaAs structures is 0.25-0.44%, depending on layer thickness ratio of InGaAs to GaAs. Larger changes in lattice parameter would be possible by either changing the thickness ratios or growing thinner InGaAs layers with higher indium composition. An advantage of this method compared to whole wafer bonding methods may be that, as the initial bonding of the structure to the substrate occurs in HF solution, contamination of the bonded interface is reduced. This method can be applied to the wide variety of III-V semiconductor materials grown on InP and GaSb as well as on GaAs substrates so long as an appropriate sacrificial layer and selective etch can be obtained.

Future work will proceed in two directions: expansion of the engineering and fabri-

cation aspects of this project, and investigation of the properties of the bonded interface. Initially, the fabrication research will focus on obtaining larger, flat features and expanding the range of lattice parameter increase towards 0.56% by attempting to fabricate samples with no GaAs layers. The larger features will require thicker sacrificial layers and the design of an additional mask. Additionally, the sacrificial layer etch rate will be brought under control through the use of dilute HF and replacing the AlAs with AlGaAs which etches at a slower rate. Once this has been achieved, membranes supported on pedestals of $Al_{0.7}Ga_{0.3}As$ will be fabricated, and InGaAs will be regrown on top of them, initially at 8% InAs. Higher alloy compositions with higher InAs fraction should be possible, and would lead to a larger change of lattice parameter.

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