COLUMN READOUT CIRCUITRY

FOR AMORPHOUS SILICON PIXEL AMPLIFIERS

IN DIGITAL IMAGING APPLICATIONS

By

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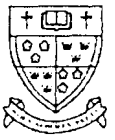

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Abstract

Amorphous silicon (a-Si:H) technology provides an opportunity to develop large area X-ray imagers with enhanced benefits over existing imaging technology. An important application of a-Si:H X-ray imagers, and the motivation of this research, is the development of diagnostic digital X-ray imagers to aid in the diagnosis of patients by medical professionals. Moreover, a diagnostic X-ray imager is desired that can provide real-time digital fluoroscopic and high exposure chest radiographic imaging applications on the same X-ray medical equipment. This research presents an architecture for a low-noise custom designed medical imaging solution designed to extend the dynamic range of pixel amplification with a current-mediated a-Si:H active pixel sensor (APS), for diagnostic X-ray imaging. The proposed circuit design permits the ability to perform both real-time fluoroscopy, and higher contrast chest radiography. The medical imaging solution was implemented and simulated in CMOS 0.18 μm technology.

Dedication

I would like to express my outmost appreciation to my fiancée Cindy, for her sacrifice and support all throughout my graduate studies. I dedicate this work to her and to my parents, Gerardina and Sabatino Ottaviani, for always being there when I needed them. I have never forgotten my family during my Master's research. Anna Rita, Giulia, and Antonio were always in my thoughts.

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1 Introduction

The introduction of amorphous silicon (a-Si:H) technology in large area X-ray digital imagers have provided the benefits of supplying a uniform deposition, low capital cost, and enhanced tolerance to X-ray radiation [1]. In addition, a-Si:H digital imagers provide on-screen diagnosis, the immediate viewing of radiographic images, convenient computer storage, and a compact imaging solution that is desired in diagnostic X-ray imaging. Currently, real-time fluoroscopy presents a challenge in X-ray imaging because of the capabilities demanded of the digital imaging electronics. Fluoroscopic imaging entails continuously exposing a patient to low doses of X-ray radiation. For instance, this occurs when a medical practitioner is scoping the artery of a patient with a catheter. Consequently, the digital imaging pixel electronics must handle reduced signal inputs for the application.

The most widely used pixel architecture is comprised of passive pixel sensors (PPS) that employ direct detection [2]. A popular amorphous selenium (a-Se) PPS architecture approach for photo-detection involves a readout circuit consisting of a thin-film-transistor (TFT), and a capacitor [3]. Charge accumulates on the capacitor during an integration interval, and the TFT acts as a switch to transfer the charge to an external charge amplifier. PPS architectures are advantageous for providing compact imagers which are practical for high-resolution applications. However, PPS structures are challenging to implement successfully for low-input, large area imaging solutions, as in fluoroscopy [3]. In general, PPS solutions require high-performance, are expensive, and may require low-noise custom charge amplification [4]. Other implementations utilize

indirect detection, such as industry standard a-Si:H switch based pixels with a signal-to-noise ratio (SNR) that produces blurry images at fluoroscopic exposure levels [2]. In contrast, current-mediated a-Si:H pixel amplifiers are able to supply a good quality SNR for low doses of X-rays required in fluoroscopy [5,6]. However, the output of the pixel amplifier becomes non-linear for increased radiation dosages, restricting the dynamic range of the pixel. This poses a dilemma when it is necessary to capture a high contrast radiographic image at a region of interest during a fluoroscopic operation.

The application and focus of this research is to present a low-noise medical imaging circuit solution designed to extend the dynamic range of pixel amplification with a current-mediated a-Si:H active pixel sensor (APS), for diagnostic X-ray imaging. The proposed design would permit the dual functionality of both real-time fluoroscopy, and higher contrast chest radiography. The medical imaging solution was implemented, simulated, and fabricated in CMOS 0.18 μm technology.

1.1 Indirect and Direct Detection

There are two types of flat panel imager approaches that differ in the method of how X-ray light is detected. The first approach is classified as indirect detection as it utilizes a phosphor layer placed in intimate contact with a flat panel array. The intensity of light produced from a location on the phosphor, translates to a measure of the intensity of the X-ray light incident on the surface of the detector, at the same relative point. Photosensitive elements on the pixels of the imager generate electric charges proportional to the intensity of light emitted from the phosphor in close proximity to each element. The process is termed indirect in that the image is transferred from X-rays to visible light photons before ultimately converted to electrical charge. In comparison, direct detection

relays X-ray interaction through photoconductors which produce charge. The process is deemed direct in that the image is transferred from X-ray light directly to electrical charge without an intermediate stage.

1.2 Pixel Architectures

1.2.1 Passive Pixel Sensors

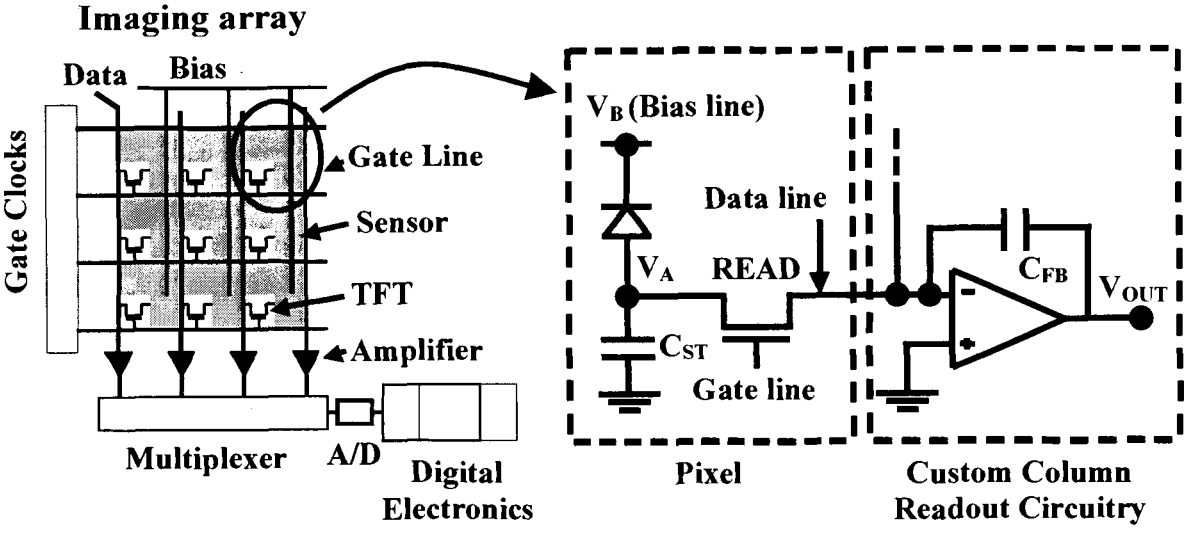

Figure 1 Passive Pixel Sensor Architecture

A commonly used passive pixel sensor resembles the one presented in Figure 1. Operation of the sensor is initiated by switching off the READ TFT such that the transistor is highly resistive. At this time the voltage across V_A is close to zero as there is no charge across the storage capacitor, C_{ST}. When X-rays are incident on the pixel, V_A moves toward V_B while C_{ST} is charged. The change in V_A during exposure is then a measure of absorption from X-ray light. In the readout phase, the READ TFT is switched on and the transistor is put in a low resistance state. A current then flows from the external circuitry to reset V_A while also being integrated across the feedback

capacitor, C_{FB}. The output voltage, V_{OUT}, then produces a measure directly related to the intensity of X-ray light detected.

The single TFT approach of the PPS allows for compact imagers and high resolution imaging. However, the PPS is vulnerable to noise emanating from the data line resistance and capacitance, as well as from the external column readout circuitry. The parasitic effects of the data bus adversely influences the readout speed and noise of the pixel, placing restrictions on the size and readout capability of a large area imager constructed with PPS elements.

1.2.2 Amorphous Silicon Active Pixel Sensors

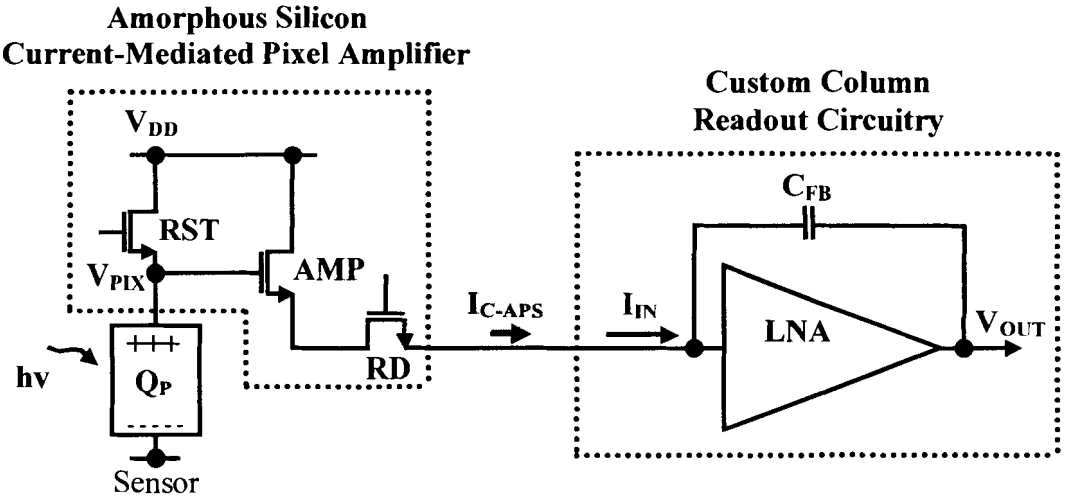

Figure 2 Current-Mediated Active Pixel Sensor Architecture

A current-mediated active pixel sensor (C-APS) is constructed as shown in Figure 2 [5]. The C-APS architecture utilizes three TFTs. Central to the C-APS is the AMP TFT that operates as a source follower which produces a current output to drive the column readout circuitry. The C-APS operates in three modes of operation: Reset, Integration, and Readout mode. In Reset mode, the RST TFT is pulsed on and the sensor

charges up to Q_P generating the voltage V_{PIX}. The integration mode occurs after reset, where both the RST and RD switches are turned off. It is during an integration period of t_{INT} that the input signal, *hv*, from the X-ray light generates photocarriers discharging an amount ΔQ_P, and as a result a proportional amount of gate voltage on the AMP TFT. The readout mode follows integration where the RD TFT is switched on and for a sampling time, T_S. In this mode, the APS becomes connected with the column readout circuitry and an output voltage, V_{OUT}, is generated across C_{FB} proportional to T_S relating the ΔV_{PIX} input change from the light-sensitive input.

A drawback of the C-APS architecture is that it requires three TFT transistors. Therefore, it occupies more space on the pixel than a PPS, and hence will have a smaller area sensitive to light input unless vertical stacking is employed [7]. The advantage of the C-APS approach is that it does not suffer from the effects of data line resistance and capacitance like the PPS and voltage-mediated active pixel sensor (V-APS) architectures. Results have shown that the C-APS architecture is capable of larger dynamic ranges for low exposure levels where the PPS arrays have produced blurry images [5,6]. The C-APS also suffers from other disadvantages to be discussed in the next section. It is the focus of this research to overcome those shortcomings while taking advantage of the improved SNR performance of the C-APS compared to well-known architectures, such as the PPS.

1.3 Large Area X-ray Medical Imaging Challenges

Several design challenges arise when developing large area X-ray imaging circuitry. The challenges to readout circuitry originate from the small-signal inputs emanating from the outputs of the current-mediated amorphous silicon pixels.

Consequently, the readout circuitry is, in part, a custom made design to best amplify the output pixel signals in the presence of these implicit design requirements. The design challenges are explained in further detail.

1.3.1 Small-Signal Inputs

X-ray sensors produce small currents that the electronics must discern and amplify to generate the required digital image. These currents can be difficult to measure. For example, an estimate of a 250 μm x 250 μm x 1 μm a-Si:H semiconductor surface produces roughly 1 nA of current in a digital fluoroscopic setting as illustrated in Table 1 [8]. Hence, a requirement for the medical imaging electronics is to be able to read signals of this magnitude.

Table 1 Small Current Calculation for a Semiconductor Pixel

Semiconductor surface dimensions: 250 μm x 250 μm x 1 μm

Min. level of illumination for digital fluoroscopy applications: 1,000 $\frac{photons}{\mu m^2 \bullet s}$

Assume a max. quantum efficiency and absorption coefficient: 0.8 and 10^6 cm^{-1}

$$\frac{1{,}000\,photons}{\mu m^2 \bullet s} \bullet \frac{10^6}{cm} \bullet \frac{1cm}{10{,}000\mu m} \bullet 250\mu m \bullet 250\mu m \bullet 1\mu m \bullet \frac{1.6x10^{-19}\,C}{s} \bullet 0.8 \approx 0.8\,\text{nA}$$

1.3.2 Low-Noise Circuitry

Since active pixel sensors can produce Pico amperes of input current, another requirement the medical imaging circuitry must have is to be able to detect and amplify these signals without contributing further noise to the process. The minimum resolvable X-ray signal that may be detected in a system is determined from the noise of the image

sensors, and from the image electronics including the amplifier. A goal in diagnostic medical imaging is to remove noise as much as possible when recovering signal input with a low noise design.

1.3.3 DC Subtraction

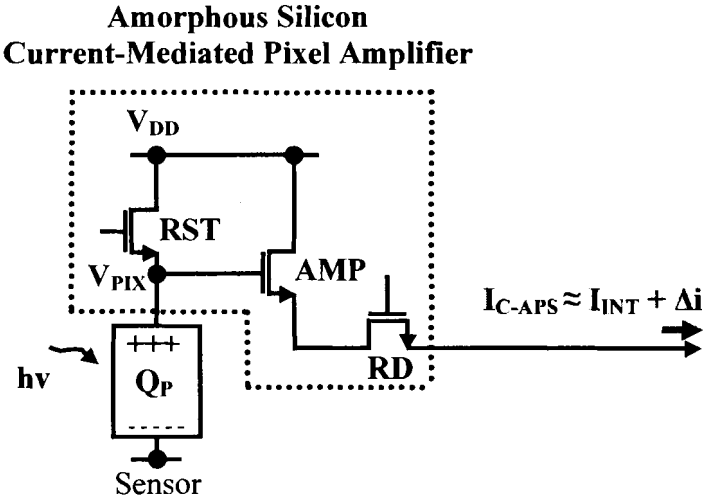

Figure 3 Current-Mediated Active Pixel Sensor With Output Current Makeup

A current-mediated a-Si:H pixel detector when connected to the imaging electronic circuitry transports a bias current together with the light-sensitive input, as illustrated in Figure 3 [5]. A further challenge for the imaging circuitry is to be able to subtract the DC bias current, Δi, leaving only the smaller DC current, I_{INT}, from the active pixel sensor to be processed further. The medical imaging circuitry detects the small current from the sensor by storing charge over a period of time. The small light-sensitive current is converted to a voltage with a capacitor after it is integrated (i.e. V = Q/C) over that time interval. The imaging architecture that performs this operation is called a charge amplifier. If the bias current is not subtracted, the output voltage of the charge amplifier will saturate much more swiftly. Furthermore, the decision for ascertaining the

output change caused solely from the light-sensitive input, will still need to be decided later in the system. Therefore, an imaging architecture that amplifies only the relevant input data is preferred.

1.3.4 Thesis Outline

Several different strategies were formulated to replace the custom column readout circuitry of Figure 2 to improve the output voltage range of the external circuitry, given the range of inputs from the C-APS. The enhanced performance of the combined system, encompassing both the C-APS and column readout circuitry, would then lead to greater resolution of a diagnostic X-ray image. It also has the consequence of exposing patients to less X-ray radiation when diagnosed. The various readout techniques were evaluated for their advantages and disadvantages, and a decision was made as to which approach would be fabricated and/or assembled on a printed circuit board (PCB). The low exposure digital fluoroscopic applications that were investigated, sought to either reduce the amount of C-APS output current before charge integration, or subtract and/or eliminate the irrelevant C-APS DC output bias current altogether. A readout architecture was then designed to extend the output voltage range of the system beyond fluoroscopic applications to include high exposure chest radiography. This architecture is designed to convey the larger X-ray C-APS inputs detected with this application for further signal processing. A comparison of the properties of each X-ray imaging system is provided in Table 2 [8]. The high exposure architecture provides a buffered output voltage from a voltage-mediated C-APS using an on-chip resistive load to process the larger sensor input signals, instead of the charge amplifier.

Table 2 Digital X-ray Imaging System Properties

Design Requirement	Chest Radiography	Fluoroscopy
Detector Size	35 x 43 cm^2	25 x 25 cm^2
Pixel Size	200 x 200 μm^2	250 x 250 μm^2
Number of Pixels	1750 x 2150	1000 x 1000
Readout Time	< 5 s	1/30 s
X-ray Spectrum	120 kVp	70 kVp
Mean Exposure	300 μR	1 μR
Exposure Range	30 – 3000 μR	0.1 – 10 μR
Noise Level	6 μR	0.1 μR

In realizing the digital X-ray imaging solutions, a low noise amplifier (LNA) and voltage buffer was designed and developed. The design methodology, component selection, and performance characteristics of each structure are documented. The results of the researched imaging solutions are also discussed, and conclusions are drawn of each design.

The most noteworthy component of this research was the uniqueness of the digital fluoroscopic readout designs in being able to subtract the unnecessary DC output component from the C-APS before charge amplification. As discussed earlier, this feature allows for the improved performance of an active pixel, with the aspiration of advancing the state-of-the-art in X-ray medical equipment for practitioners and patients. It represents one of the larger contributions of this work.

2 Medical Imaging Readout Solutions

2.1 Preliminary Design Strategies

Various strategies were contemplated to replace the custom column readout circuit of Figure 2. The benefits and negative aspects of each design were assessed, and accompany the description of each architecture below. Several designs were chosen for fabrication and/or assembled on a PCB for further investigation.

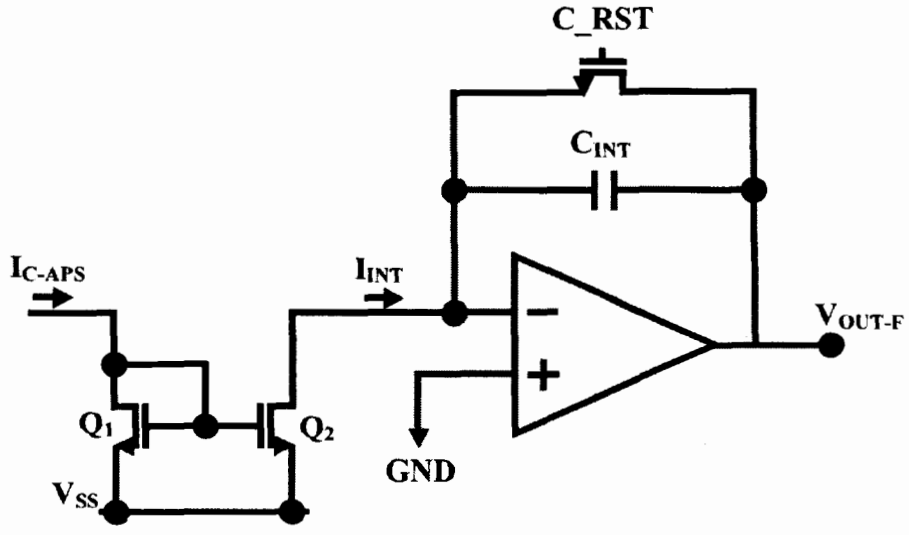

Figure 4 Current Mirror Strategy

The idea of the current mirror strategy, presented in Figure 4, is to scale back the output current from the C-APS by choosing the geometry of transistors Q_1 and Q_2 such that the current I_{INT} is a fraction of I_{C-APS}. This can be achieved by the following current mirror equation,

$$I_{INT} \approx I_{C-APS} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}.$$

By dropping the amount of current before charge amplification the amplifier will not saturate as quickly, allowing for a larger range of outputs possible for a given input. With this method the output voltage is still determined by both the large and small DC current components from the C-APS. Since it was desirable to charge amplify only the relevant DC input that was a direct product of light-sensitive input, other architectures were explored.

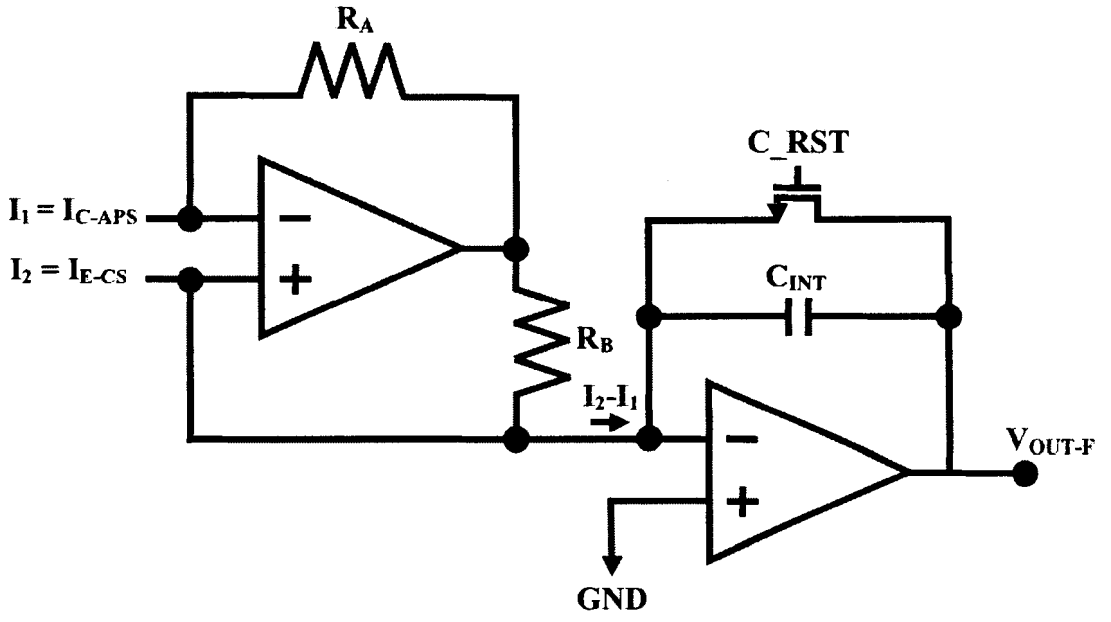

Figure 5 Subtractor-Integrator Op Amp Strategy

The subtractor-integrator op amp implementation displayed in Figure 5 was a design that intended to remove the large DC bias current from the desired C-APS output current signal before charge amplification. The circuitry takes as input the C-APS DC output current, and the DC current, $I_{E\text{-}CS}$, from an external source. The first op amp with the resistor feedback configuration subtracts the current provided by the external source from the C-APS output current. The resulting current, $I_2 - I_1$, will be the desired current

to be integrated. The external current source could be made variable to adequately tune the readout circuitry to precisely subtract the extraneous DC current.

The immediate drawback of this architecture was the added area that would be required if the solution was to be implemented in an integrated circuit solution, due to presence of the additional op amp and resistor components. In addition, performance of the subtractor would be a concern if the feedback resistors were not reasonably matched. The solution, however, would provide the benefit of integrating only the current due to pixel sensor inputs.

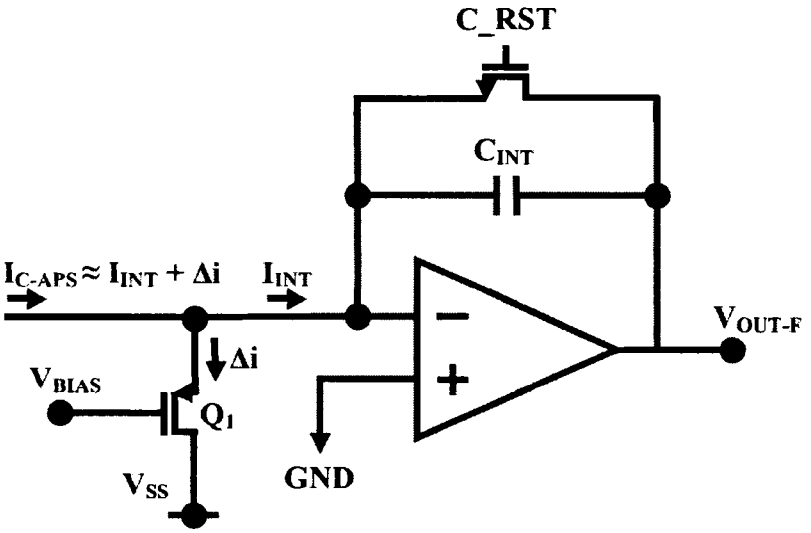

Figure 6 Bypass DC Current Strategy

The Bypass DC current strategy is presented in Figure 6. It consists of a single transistor, Q_1, to bypass the larger DC component from the C-APS output current, thus leaving the desired DC current, I_{INT}, to be charge integrated into an output voltage, $V_{OUT\text{-}F}$. A variable external bias, V_{BIAS}, is provided to the gate of Q_1 to adjust the amount of current to be subtracted from the negative input terminal of the op amp. The intention of this implementation is also to remove the superfluous DC current, Δi, before charge

integration of the remaining current, I_{INT}. A PMOS transistor should be chosen for Q_1 to minimize the amount of readout circuit noise.

Similar to the subtractor-integrator op amp strategy, the advantage of the bypass DC current strategy is to integrate only the C-APS output current generated by X-ray light. The other added benefit is the reduced complexity of this architecture relative to the other systems considered. The disadvantage of the approach is the need of a variable voltage source to tune the bypass DC current.

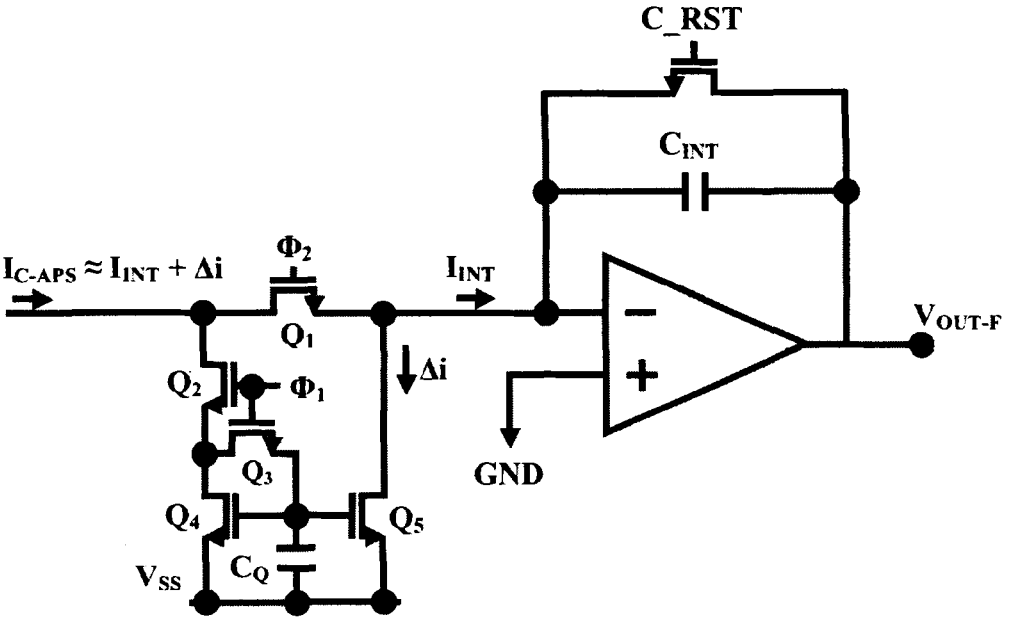

Figure 7 Switched Capacitor Subtraction Strategy

The switched-capacitor strategy in Figure 7 involves charging up capacitor, C_Q, with the current from the C-APS pixel before the photodiode has detected any photocarriers. During the storage phase of the circuit controlled by clock, Φ_1, switches Q_2 and Q_3 are closed permitting C_Q to be charged to a desired voltage level in order to bias Q_5. The value for C_Q is chosen such that the gate voltage for Q_5 will conduct a current equal to the large DC current, Δi, which is accompanied by the desired DC

current, I_{INT}, in the discharge phase. While charging, switch Q_1 is left open as controlled by the clock, Φ_2. The storage phase continues until C_Q is fully charged to its' maximum voltage whereby current can no longer conduct between Q_3, and must divert to Q_4. In the discharge phase, Φ_1 then switches off Q_2 and Q_3, as Φ_2 switches on Q_1. With the proper bias voltage and geometry for Q_5, Δi will be subtracted from the C-APS output current to advance I_{INT} to the readout circuitry for integration.

The implementation has several disadvantages. The first drawback is that the strategy requires sampling the output current from the C-APS twice. One sample is required to charge C_Q to a bias voltage, and another to bypass current through Q_5. Therefore, the architecture has a great deal of complexity associated with it. Furthermore, C_Q must be cleverly chosen so that it does not leak appreciably between the charge and discharge phases, and that it does not occupy more than a reasonable amount of area in an integrated circuit solution. Lastly, the switching of Q_3 will produce a feedthrough effect that will cause the voltage across C_Q to spike, which can potentially harm the quality of the signal being integrated. The advantage of the readout circuit solution would be that it precisely subtracts the irrelevant DC bias current, leaving only the desired C-APS output current for integration.

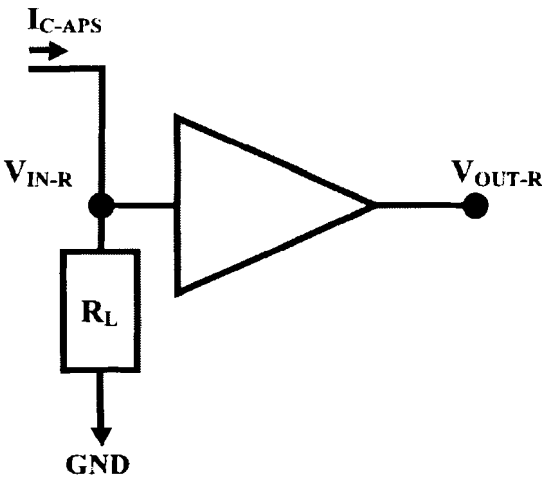

Figure 8 Attenuation Strategy for High Exposure Applications

The remaining strategy that was researched was the design in Figure 8 that was devised to accurately process high exposure C-APS inputs, advantageous for chest radiography applications. The architecture requires a large value of R_L comparable to the resistance value of the RD TFT in the C-APS. As the C-APS output current from a high exposure input flows through the circuit, both the RD TFT and R_L act as a voltage divider creating the voltage, $V_{IN\text{-}R}$, at the input of a voltage buffer. The output voltage, $V_{OUT\text{-}R}$, then produces an attenuated value of the high input dosage for further signal processing. The architecture functions owing to the linear relationship between ΔV_{PIX} of the C-APS and $\Delta V_{OUT\text{-}R}$ of the readout circuit. The downside of this approach is the size of R_L required to compare with the resistance of the RD TFT in the C-APS.

After considering the advantages and disadvantages of each approach, the decision was made to fabricate the subtractor-integrator op amp and attenuation strategies in 0.18 μm CMOS technology. This would allow an assessment of circuitry that could perform low and high exposure applications. This readout architecture is known as medical imaging readout solution I (MIRS I). In addition, both the subtractor-integrator

and bypass DC current strategies were tested with commercial IC and other discrete components on a PCB to collect further data about each architecture. The standalone bypass DC current readout strategy is also referred to as medical imaging readout solution II (MIRS II).

2.2 Medical Imaging Readout Solution I (MIRS I)

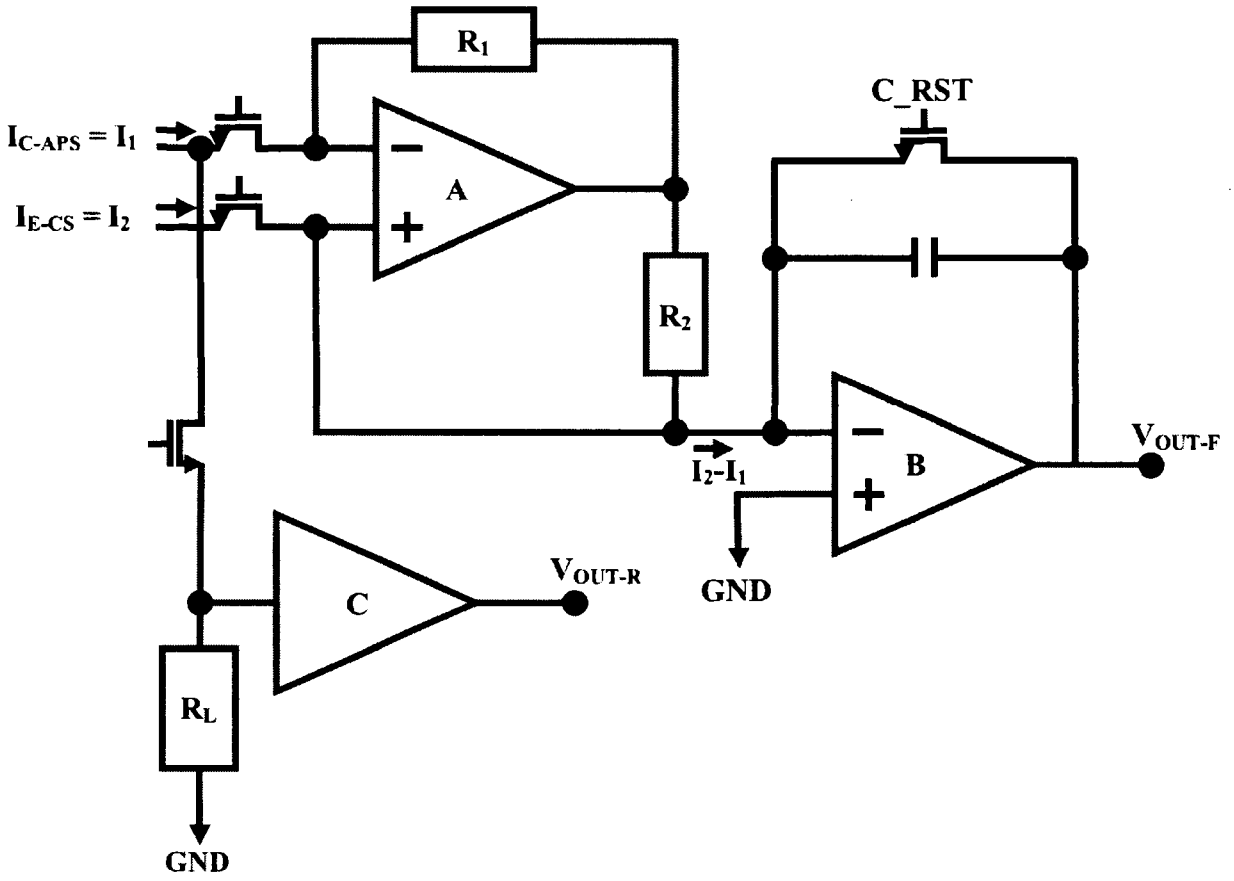

Figure 9 Medical Imaging Readout Solution I

The low-noise medical imaging circuit solution in Figure 9 was designed to extend the dynamic range of a current-mediated a-Si:H active pixel sensor (C-APS), for diagnostic X-ray imaging applications. With the addition of the attenuation strategy, this

design permits the dual functionality of both real-time fluoroscopy, and higher contrast chest radiography.

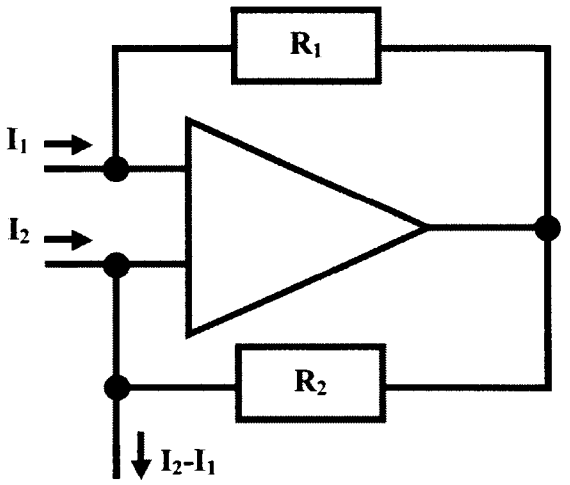

Figure 10 Feedback Implementation for Structure A

The combined design contains three low noise op amp structures and operates in two modes. In mode 1, structures ***A*** and ***B*** are identical and operational for digital fluoroscopic applications, while structure ***C*** is made inactive. Structure ***A*** serves to subtract the dc bias current from the signal input before charge amplification. Structure ***A*** is arranged in a feedback structure as pictured in Figure 10. The bias and signal DC current is transported over I_1. An external current source at I_2 serves to subtract the superfluous bias current, permitting the signal input, $I_2 - I_1$, to be amplified. Structure ***B*** operates as the charge amplifier and hence contains a capacitor in the feedback path. In mode 2, structure ***C*** functions for radiographic applications acting as a voltage buffer to increase the dynamic range for larger pixel inputs. Structures ***A*** and ***B*** are turned off while structure ***C*** buffers the input voltage sensed across the load resistor of the active pixel sensor. The digital fluoroscopic and chest radiography components of MIRS I were decoupled on the integrated solution to accurately test both parts, and to allow a greater

probability of either design module successfully operating after fabrication, should the other module not function appropriately. The digital fluoroscopic portion of the readout solution was also tested on a PCB with commercial ICs and shelf components.

2.2.1 Low Noise Amplifier (LNA)

To realize the architecture of Figure 9, a low noise amplifier was constructed for structures ***A*** and ***B***. Six different low noise amps were constructed and are labeled as LNA-1, LNA-2... and LNA-6, as presented in Figures 26 - 33 in Appendix I. Primary emphasis was placed on achieving a high slew rate of 10 V/μs or greater, and making the amplifier stable for capacitive loads of 2 - 5 pF. Structure ***A*** is estimated to observe a capacitive output load of approximately 2 pF, where Structure ***B*** is expected to have around 5 pF since it will be connected to an output pad. Since structure ***A*** and ***B*** will be realized with the same LNA, the amplifier must be stable for both figures and all values in between. The other design specifications include performance parameters that are desired but are not absolutely necessary. The desired design specifications are listed in Table 3. The imaging solution was simulated in Cadence with SpectreS and HSpiceS models.

Table 3 Desired LNA Design Specifications

Supply Voltage	**V_{DD} = 3.3 V, V_{SS} = 0 V**
Input Voltage Range	**0.0 – 3.3 V**
Power Dissipation	**≤ 1.5 mW**
Load Capacitor	**2 -5 pF**
Slew Rate	**≥ 10 V/μs**
Layout	**200 μm x 100 μm**

Primary importance was placed on achieving a high slew rate so that when integrating C-APS output currents, the output voltage from the LNA can respond quickly. In digital fluoroscopy, a 1000 x 1000 pixel flat panel array must process X-ray inputs at the frequency of 30 Hz, as seen in Table 2. Hence, each column of pixels in the array must relate the X-ray input signal to the output of the external charge amplifier with a frequency of 30 KHz. It is, therefore, advantageous to have the output voltage of the LNA swing quickly for this real-time imaging application.

As the LNA will be designed in 0.18 μm CMOS technology, V_{DD} was chosen to be 3.3 V to allow for an ample voltage drop across each branch in each LNA. It was also chosen over the 5 V rail so that it would consume less power in the system.

In order not to limit the capabilities of the LNA before construction of the amplifier has commenced, a rail-to-rail input voltage range was listed as one of the design requirements. A large input voltage range will allow for greater flexibility in biasing the LNA, if required.

Anticipating the concern of how much power the readout circuitry may consume in the digital X-ray equipment, it was desired that the medical imaging solution would use no more than 1.5 mW of power. Given a thousand columns and a readout circuit for each column, this would translate into a total of 1.5 W of power being consumed by the readout hardware.

The largest pixels used in digital X-ray medical imaging are those used in fluoroscopy. The pixel area is expected to occupy an area of 250 x 250 μm^2, as acknowledged in Table 2. Consequently, a layout requirement of 200 x 100 μm^2 for the LNA was anticipated.

2.2.2 Design Methodology

A number of architectures for the op amp were designed and simulated in investigating which design would be the most advantageous for the medical imaging solution. Various complementary folded-cascode (CFC) and two-stage amplifier designs were compared, and ultimately a topology and several test structures were submitted for fabrication. The CFC design was selected initially because it is known to be an advantageous architecture for low voltage and high frequency applications [9]. These features would be important factors in the eventual fabrication of a practical commercial product. This architecture was compared with a conventional two-stage amplifier.

2.2.2.1 Complementary Folded-Cascode (CFC)

LNA-1 and LNA-3 are low noise complementary folded-cascode amps. In general, the characteristic of a folded-cascode op amp is that it utilizes cascoding in the output stage coupled with parallel-connected n and p channel input differential pairs to obtain a respectable input common-mode range (ICMR). The folded-cascode op amp provides a reasonable gain, input common-mode range, and self-compensation. Furthermore, the power-supply rejection ratio of the folded-cascode op amp is significantly improved over that of a two-stage op amp. The CFC is an architecture based on a folded-cascode architecture. Consequently, the CFC has excellent small-signal ac response and settling time characteristics for very small capacitive loads. The CFC is a single-stage modified current steering architecture that incorporates a class AB cascode stage. The performance of the CFC configuration is superior to that of the mirrored-cascode and folded-cascoded structures [9]. The design can be used in high

frequency CMOS VLSI applications. It is capable of near rail-to-rail input and output voltage ranges.

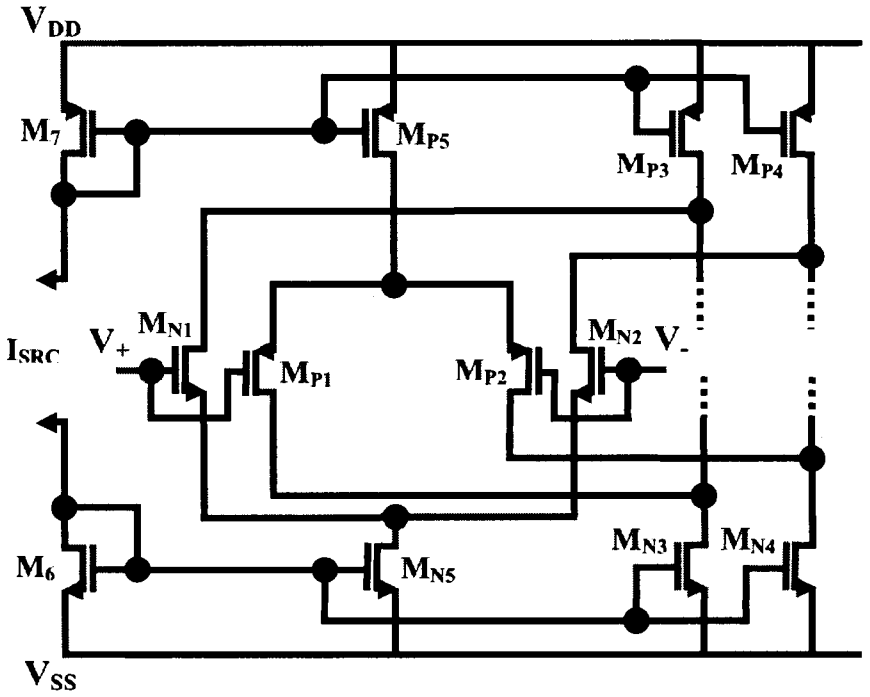

Figure 11 Parallel n and p Channel Differential Input Stage[1]

One of the best features of a CFC is the ability for the design to provide a large input common-mode range, and thus providing an excellent structure for low voltage power designs. The largest problem with reducing a power supply is the effect it has on the ICMR. The ICMR is essential for determining if the output of a stage can interface with the input of another stage. Ideally, the ICMR should be large and centered between the rail voltages. The most influential consequence of low-voltage power supplies is on the input stage of an op amp. A solution for obtaining a desirable ICMR for a low-voltage application is to use both an n-channel and p-channel differential input stage connected in parallel, as in a CFC structure that is portrayed in Figure 11.

[1] Based on P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. (New York: Oxford University Press, 2002), 418.

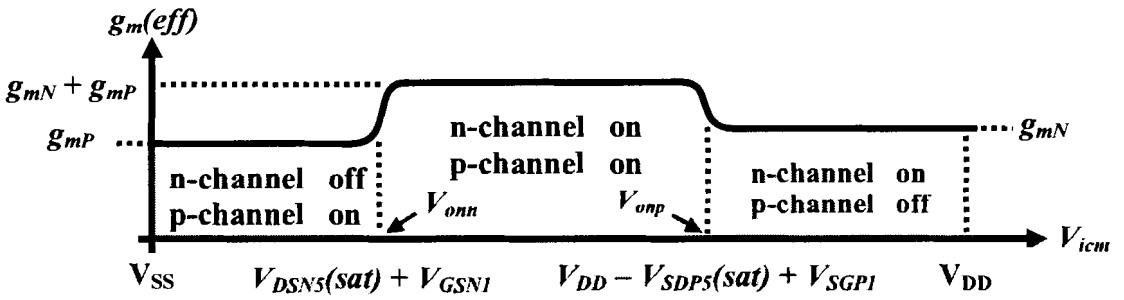

Figure 12 Effective Input Transconductance for a Parallel n and p Channel Differential Input Stage[2]

This architecture can extend the ICMR above and below the power-supply limits. The structure behaves uniquely in three regions of operation. The regions are defined as follows:

Region I: $V_{onn} > V_{icm} > 0$ (n-channel off, p-channel on)

$g_m(eq) = g_{mP}$

Region II: $V_{onp} \geq V_{icm} \geq V_{onn}$ (n-channel on, p-channel on)

$g_m(eq) = g_{mN} + g_{mP}$

Region III: $V_{DD} > V_{icm} > V_{onp}$ (n-channel on, p-channel off)

$g_m(eq) = g_{mN}$

The architecture provides a different gain in each region of operation owing to the different transconductance and output resistance generated in each mode. The effective transconductance for the input common-mode range is displayed in Figure 12.

LNA-1 and LNA-3 were designed to operate at 0.8 and 2.3 V biases, respectively, in the medical imaging readout circuit solution. This was done to match the input bias with the output voltage bias for each LNA, so that they would function appropriately in the readout architecture. Both designs utilize very wide transistor widths in the cascode

[2] Based on P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. (New York: Oxford University Press, 2002), 419.

structures. LNA-1 contains wider transistors than LNA-3, and generates an optimal noise characteristic. LNA-3 uses smaller cascode transistors establishing a slightly noisier design that uses much less area than LNA-1. LNA-1 employs an NMOS source follower, where LNA-3 uses a PMOS source follower output stage.

2.2.2.2 Two-Stage Amplifiers

LNA-2, LNA-4, and LNA-6 are low noise two-stage amplifiers. They have PMOS input differential pairs with NMOS loads in the first stage. Their second stage contains an NMOS common source amplifier and a PMOS load. Their output stage is a PMOS source follower. The designs all contain a compensating capacitor and a nulling resistor between the input and output of the second stage. The designs are identical in architecture but differ in device geometry for the compensating capacitor, null resistor, and aspect ratios for certain transistors. LNA-2 was designed to provide a low noise amplifier with a greater margin of safety, inherent by the device geometry that was chosen, that would increase the likelihood of successful operation of the design after fabrication. LNA-4 was designed to obtain the best possible gain, noise, and stability of the two-stage architecture. LNA-6 contains the same two-stage architecture, but was designed with 3.3 V tolerant devices to ensure that a voltage breakdown could not occur on any transistor. The remaining op amp designs contain 1.8 V devices but have been simulated exhaustively to ensure a voltage breakdown would never take place on any transistor in the design, even with a power supply voltage of 3.3 V.

LNA-5 is also a two-stage amplifier like the previous designs, with the exception that the input stage also contains PMOS cascode amps in the first stage. The extra PMOS

transistors are biased using the current source structure of the input differential pair. The intention of this design was to improve the bandwidth of the two-stage architecture.

2.3 Medical Imaging Readout Solution II (MIRS II)

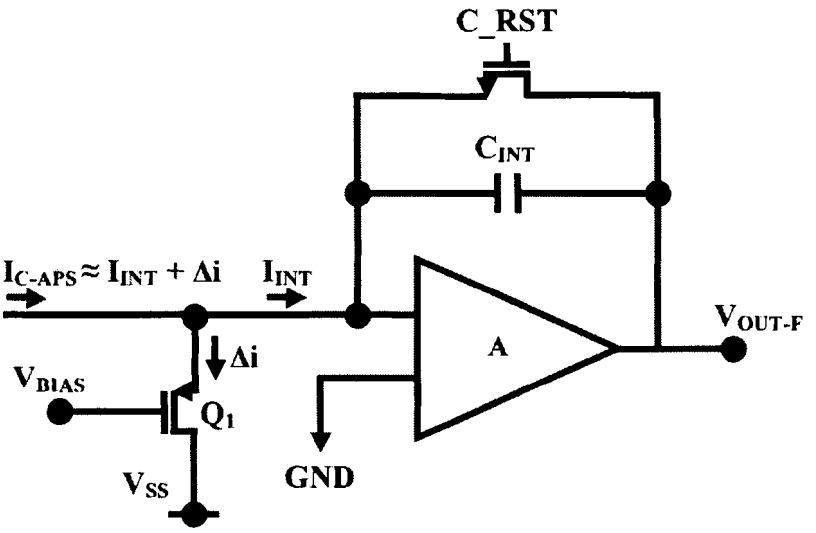

Figure 13 Medical Imaging Readout Solution II

The low-noise medical imaging readout solution in Figure 13 was also designed for diagnostic X-ray imaging applications to be used in conjunction with an active pixel sensor. The readout solution requires a low noise PMOS transistor for Q_1 in addition to an LNA, structure ***A***. An external bias controls the current through Q_1 to discard the large unwanted DC output current, Δi, from a C-APS during readout mode. The desired C-APS output current, I_{INT}, can then be integrated with the LNA. The design was constructed on a PCB with discrete components. The same IC integrator component on the PCB that was used to test MIRS I, was also used for the PCB testing of MIRS II to compare both architectures. The same LNA fabricated for MIRS I can be used for MIRS II, should MIRS II be fabricated in the future.

3 LNA Implementation

The design geometry for the amplifiers is provided in Tables 9 - 14 in Appendix IV.

3.1 Performance Results

The post-layout performance results for all the LNAs are provided in Table 4, with the exception of the output resistance and power dissipation characteristics, which were obtained from pre-layout simulations. The power supply and input bias voltages for each LNA are 3.3 and 1.65 V, respectively.

Table 4 CFC Performance Measurements

Design	LNA-1	LNA-2	LNA-3	LNA-4	LNA-5	LNA-6
ICMR (V)	-0.3 – 3.5	-0.3 – 2.6	-0.1 – 3.3	-0.3 – 2.6	0.9 – 2.5	-0.4 – 1.9
Gain (dB)	50.23	70.09	57.33	71.09	66.92	74.19
f_{-3dB} (KHz)	39.09	20.21	57.48	27.59	35.91	20.84
GB (MHz)	1.96	1.42	3.30	1.96	2.40	1.55
Unity GB (MHz)	12.74	67.51	27.55	128.9	104.0	103.4
Phase Margin @ 2, 5 pF(Φ)	84.96° 82.60°	78.70° 64.76°	74.74° 53.25°	73.50° 62.69°	74.06° 62.11°	77.07° 69.55°
Noise @ 1 KHz (nV/√Hz)	6.13	10.66	17.04	8.45	9.66	18.90
OVR (V)	0.2164 - 1.592	1.497 – 3.121	1.491 – 3.100	1.497 – 3.121	1.510 – 3.120	1.523 – 2.826
R_{OUT} (Ω)	148.66	282.02	477.16	281.26	142.60	683.72
CMRR (dB)	61.94	92.19	69.51	94.61	90.50	94.83
$PSRR^{+}$ (dB)	15.46	77.18	19.04	78.97	67.06	74.21

Design	LNA-1	LNA-2	LNA-3	LNA-4	LNA-5	LNA-6
PSRR⁻ (dB)	9.154	70.35	22.05	76.04	63.55	67.34
Slew Rate rise/fall (V/μs)	10.52 10.00	13.32 15.76	8.24 8.28	23.24 16.41	8.72 12.07	7.42 11.76
Settling Time rise/fall (ns)	681.09 1158.06	86.26 58.13	107.69 65.37	76.07 57.90	60.97 57.70	79.40 57.98
P_{diss} (mW)	80.57	8.729	18.66	8.752	11.34	6.811
Area (μm^2)	501,510	21,224	111,960	25,484	26,633	25,257

Table 5 lists the post-layout performance of amplifiers LNA-1 and LNA-3 operating under the input voltage biases of 0.8 and 2.3 V, respectively, with a power supply voltage of 3.3 V. These amplifiers will operate under these biases in the medical imaging solution.

Table 5 Performance Parameters for LNA-1 and LNA-3 at their Respective Biases in the Medical Imaging Solution

Design	LNA-1 (0.8 V Bias)	LNA-3 (2.3 V Bias)
ICMR (V)	-0.3 – 3.5	-0.1 – 3.3
Gain (dB)	49.77	57.33
f_{-3dB} (KHz)	29.17	51.51
GB (MHz)	1.45	2.95
Unity GB (MHz)	12.83	39.10
Phase Margin @ 2, 5 pF(Φ)	84.81° 83.13°	67.18° 53.02°
Noise @ 1 KHz (nV/√Hz)	6.13	17.02
OVR (V)	0.2164 - 1.580	1.493 – 3.102
R_{OUT} (Ω)	148.66	476.93
CMRR (dB)	121.3	106.4
PSRR⁺ (dB)	60.71	61.46

Design	LNA-1 (0.8 V Bias)	LNA-3 (2.3 V Bias)
PSRR⁻ (dB)	52.66	65.83
Slew Rate rise/fall (V/μs)	7.59 6.46	29.57 29.63
Settling Time rise/fall (ns)	237.35 955.87	76.82 65.61
P_{diss} (mW)	80.53	18.65
Area (μm^2)	501,510	111,960

3.1.1 Gain, f_{-3dB}, GB, Unity GB, Noise, and Phase Margin

The amplifier with the highest output voltage gain was LNA-6 with 74.19 dB. However, LNA-2 and LNA-4 were comparable with gains of 70.09 and 71.09 dB, respectively. The gains of all amplifiers are sufficiently high to ensure the closed-loop properties of an op amp with feedback.

The amplifier with the best -3 dB frequency and gain bandwidth is LNA-3 at the 1.65 V input bias. The -3 dB frequency and gain bandwidth for LNA-3 at 1.65 V is 57.48 KHz and 3.30 MHz. LNA-1 is comparable to the frequency performance of LNA-3 at the input voltage bias of 0.8 V. The CFC architectures and LNA-5 has shown to provide the best frequency results in these categories.

LNA-4 provides the best unity gain bandwidth at 128.9 MHz. LNA-4, LNA-5, and LNA-6 are better than all the other amplifiers by a significant frequency margin in this category. LNA-5 and LNA-6 also provide high unity gain frequencies, and are second and third best in providing this feature.

LNA-1 provides the best noise characteristic with 6.13 nV/√Hz at 1 KHz. However, it does so at the expense of using a lot of area. It is almost 4 ½ times larger than the next largest design. LNA-2, LNA-4, and LNA-5 also provide excellent noise

characteristics. LNA-4 and LNA-5 have noise ratings below 10 nV/√Hz at 1 KHz, while LNA-2 has only a slightly larger rating than both of those amplifiers.

LNA-1 also provides the best phase margin. This is likely because of the low gain and large area characteristic of the design. However, all the designs have substantial phase margins to ensure stability for a capacitive load of 2 - 5 pF. The lowest phase margin of any amplifier is LNA-3 at 5 pF which is still greater than 50°.

3.1.2 CMRR

LNA-1 operating at the input bias of 0.8 V provides the best CMRR. All the amplifiers produce a high CMRR. The CFC amplifiers produce the best CMRR performance at their medical imaging input biases. The remaining two-stage amplifiers also display exceptional CMRR performance ratings.

3.1.3 PSRR

$PSSR^+$ and $PSRR^-$ are best for LNA-4 with values of 78.97 and 76.04, respectively. $PSRR^+$ and $PSRR^-$ have excellent ratings for every two-stage amplifier, and for the CFC amplifiers operating at their medical imaging biases. LNA-2, LNA-4, and LNA-6 all have comparably exceptional PSRR values.

3.1.4 Settling Time and Slew Rate

The greatest slew rate characteristics were obtained with LNA-3 at the 2.3 V medical imaging input bias. LNA-4 has the second fastest slew rate characteristics. The greatest settling time characteristics were obtained with LNA-5, followed closely by LNA-4 and LNA-6. The settling time features for LNA-5 are comparable to LNA-4 and LNA-6.

3.1.5 ICMR and Output Voltage Range

The ICMR is greatest for LNA-1 and LNA-3 as was expected because they utilize the CFC architecture. They allow for a complete rail to rail input voltage range. LNA-2 and LNA-4 are next to the CFC amplifiers for providing the best ICMR with Δ 2.9 V. LNA-5 and LNA-6 have a smaller ICMR than the other amplifiers, but are able to provide Δ 1.6 and 2.3 V, respectively.

3.1.6 Dissipated Power

The dissipated power for each amplifier was obtained by summing the individual power contributions in every circuit obtained from pre-layout simulation. The power calculation for LNA-4 is provided below as an example:

LNA-4 Power Calculation

$$P = P_{M0} + P_{M1} + P_{M2} + P_{M3} + P_{M4} + P_{M5} + P_{M6} + P_{M7} + P_{M8} + P_{M9}$$

$$= (2)(206.4\mu A)(834.7mV) + (2)(103.2\mu A)(1.84V)$$

$$+ (2)(103.2\mu A)(625.2mV) + (1.76mA)(275.6mV)$$

$$+ (1.76mA)(3.024V) + (633.7\mu A)(1.655V) + (633.7\mu A)(1.645V)$$

$$= 8.75\ mW$$

3.1.7 LNA Analysis

The LNA performance results suggest that for fluoroscopic applications, the system should be implemented with LNA-4. Although the design does not score the best in every performance category, it scores extremely well in the desired categories. LNA-4 has the largest gain and slew rate than any other amplifier that has a noise rating below 10 nV/$\sqrt{Hz}$ at 1 KHz. It has one of the best overall frequency ratings of all the two-stage

amplifiers next to only LNA-5 in the f_{-3dB} and GB categories, and more than adequately meets the stability requirements for operation. It scores very well in the remaining performance categories, and provides the best comprise for consuming less power and taking less area than any other LNA. LNA-2 and LNA-6 are also very good options that can be used to implement the system. LNA-2 has the distinction of occupying the least area, while LNA-6 has the largest gain and consumes the least amount of power. However, LNA-4 is practically comparable to both designs in those categories while also achieving superior noise, slew rate, and frequency performance over those same LNAs. LNA-1 and LNA-3 are more sophisticated designs that have a higher element of risk of unsuccessful operation after fabrication. Where LNA-1 has the better noise characteristic than LNA-3, it takes up much more area, and therefore LNA-3 should be chosen ahead of LNA-1. LNA-5 was a design that attempted to enhance the frequency characteristics for the imaging solution. Where it has the best f_{-3dB} and GB frequency characteristics of any two-stage amplifier, it is not as pronounced an improvement as compared to the CFC designs. Moreover, LNA-4 surpasses LNA-5 in achieving a higher unity gain bandwidth score. LNA-5 also has more risk associated with it successfully operating after fabrication, because of the differential amplifier cascode structure in the first stage of the design. Conversely, LNA-6 is a more robust design that uses 3.3 V rated transistors with larger breakdown voltages.

The LNA post-layout simulations conclude that LNA-4, followed by LNA-6 and then LNA-2, will provide the best performance for a medical imaging readout solution.

4 Voltage Buffer

Structure *C* of Figure 9 was constructed with the same source follower architecture that was used for the two-stage amplifiers. The device geometry for the voltage buffer is provided in Table 15 in Appendix IV. The output bias of the buffer is 1.2 V. The design has an ICMR of 0 to 2.6 V. Hence, it can operate within the expected input voltage range of 0 to 1 V, which is the maximum voltage drop expected across the load resistor as it will be driven by the active pixel sensor. The design is well below 1 pV/√Hz at 1 KHz, and contributes very little noise to the system. The system bandwidth is 64.58 MHz and 105.9 KHz at the input voltage biases of 0 and 2.6 V, respectively. The noise and frequency characteristics were verified in post-layout simulations.

5 IC Layout Design for Medical Imaging Solution I

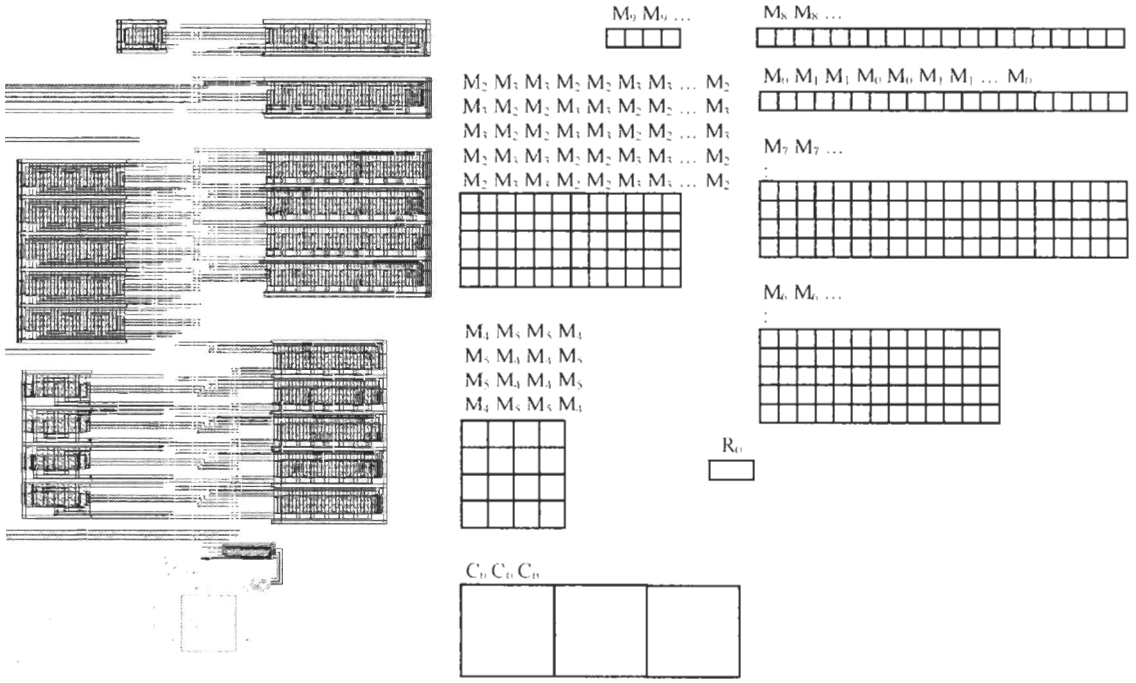

Figure 14 Layout and Floorplan of LNA-4

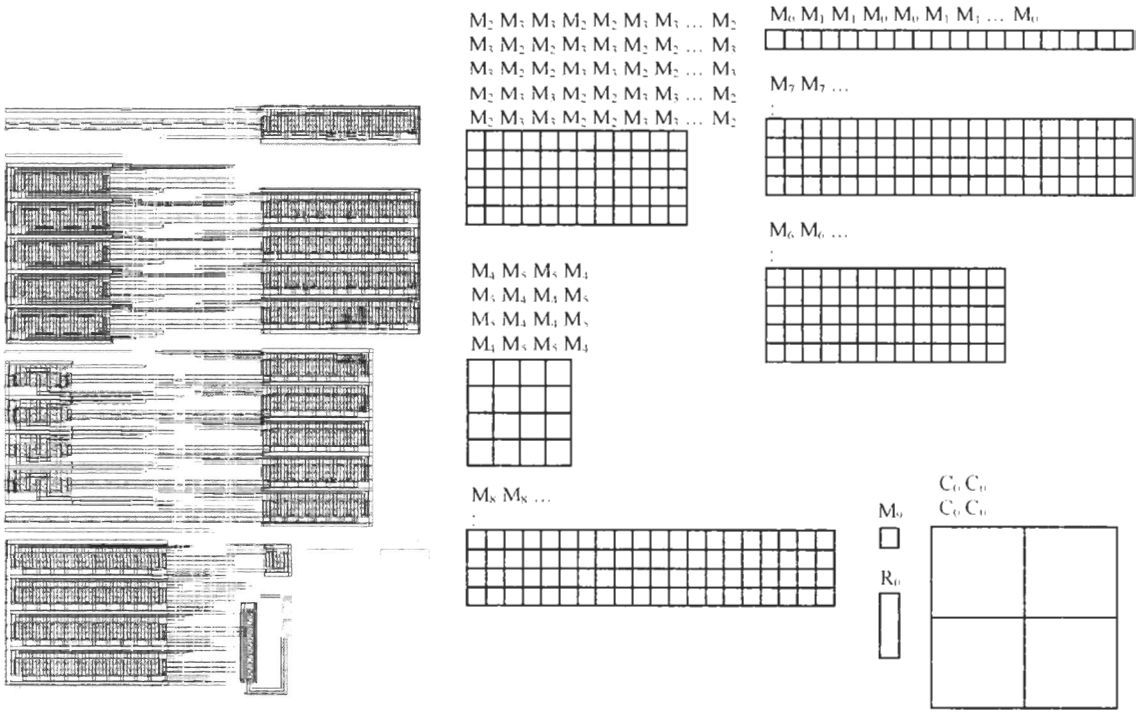

Figure 15 Layout and Floorplan of LNA-6

The channel length for all the devices was selected to be 1 μm or greater. The channel length was increased from 0.18 μm to minimize short channel effects, to lessen any negative impact on design performance from process variation, and to decrease noise in LNA-4 and LNA-6. Area was surrendered as a consequence of choosing a larger channel length. Doubling the channel length, for example, would have the effect of doubling all the device widths to maintain the same aspect ratios for the design.

The larger transistors in the design were composed of smaller transistors connected in parallel. Numerous contacts were supplied along the drain and source regions of the device in this fingering technique. This was done in order to reduce voltage drops that can occur between the junctions of relatively high resistive silicon material and metal. The smaller transistors were not made longer than 5 μm for the same reason. The multi-fingered transistors in the op amp designs made use of common-centroid and interdigitizaton techniques, as seen in the layout pictures and portrayed symbolically in the floorplans of LNA-4 and LNA-6 in Figures 14 and 15. The common-centroid and interdigitizaton techniques in these op amps can be viewed at the input PMOS and NMOS load devices in the first stage of each amplifier as highlighted by the floorplans. These layout techniques were employed to match transistors and reduce the inherent offset voltage in the op amp design.

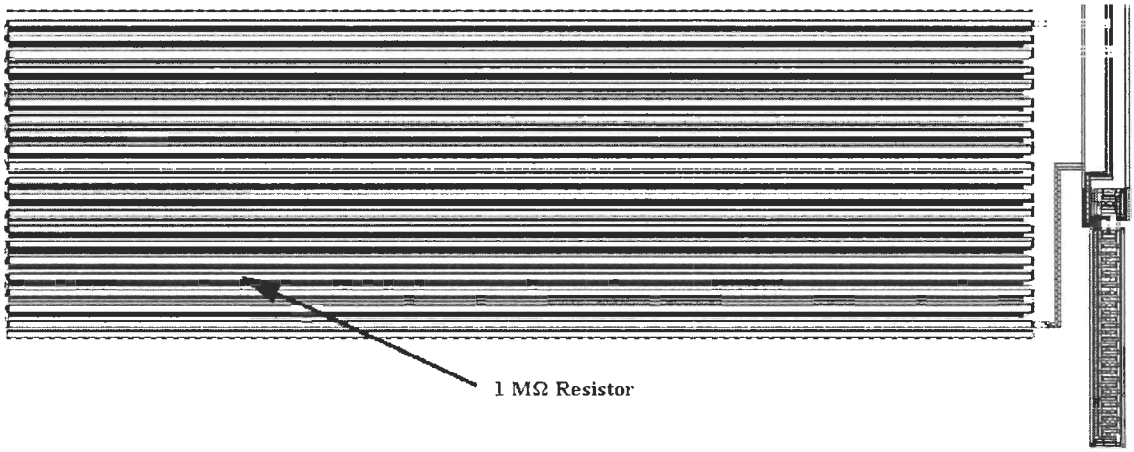

Figure 16 Layout for the Attenuation Architecture

Since MIRS I was comprised of two LNA-6 amplifiers, no other layout considerations other than increasing the size of the V_{DD} and V_{SS} traces from the pins to the pad were necessary. For the attenuation circuit in Figure 16, the 1 MΩ resistor was constructed of 20 smaller 50 KΩ resistors connected in series with a snake pattern.

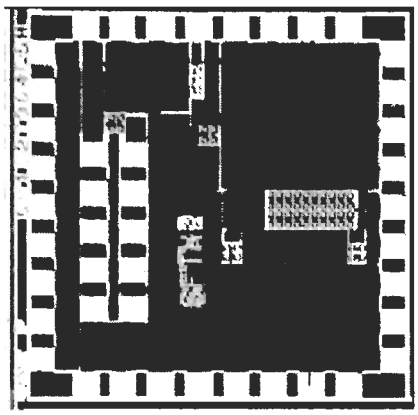

Figure 17 IC Layout

In general, the resistors on the IC were fashioned with highly resistive polysilicon in an nplus region. Capacitors were constructed with two different large metal plates connected together by vias. Every transistor, resistor, and capacitor component in the IC contained etching compensation, or dummy gates. Also, at least two vias were provided

at each metal-to-metal and metal-poly junction in the test structures to ensure that the traces were properly connected. The IC layout for all test structures is presented in Figure 17.

6 Medical Imaging Readout Results and Analysis

6.1 Medical Imaging Readout Solution I

6.1.1 Simulations

MIRS I represented in Figure 9 has been simulated with an APS Verilog-A model in Cadence. Digital fluoroscopy simulations were initially conducted with ideal amplifiers for structures ***A*** and ***B***. Digital fluoroscopy pre-layout and post-layout simulations were then conducted with each LNA taking the place of the ideal amplifier. LNA-1 and LNA-3 operate at 0.8 and 2.3 V input bias in the system. Data was collected across a small 10 mV to observe the resolution of the imaging solution possible with each LNA, and a larger 0 to 0.8 V range to study the effects of higher exposure C-APS input signals. Pre-layout simulation results show that LNA-1, LNA-2, LNA-4, and LNA-6 all closely match the simulations with the ideal amplifier under identical conditions. LNA-3 and LNA-5 also display the required linear relationship between the input and output, and show only a minor degradation between the design and ideal simulations. LNA-1, LNA-4, and LNA-6 display the best linear relationships, with LNA-4 and LNA-6 standing out among the amplifiers as providing the best digital fluoroscopy simulations with a minimum pixel gain of 2 V/V. The pixel gain was observed even with a Δ 1 mV change of V_{PIX} at the sensor input. LNA-3 allows for the greatest fluoroscopic pixel sensor input range with Δ 0.8 V before the charge amplifier will saturate. LNA-2 and LNA-4 are second best with a sensor input voltage range of Δ 0.6 V. LNA-6 was third best with a range of Δ 0.5 V.

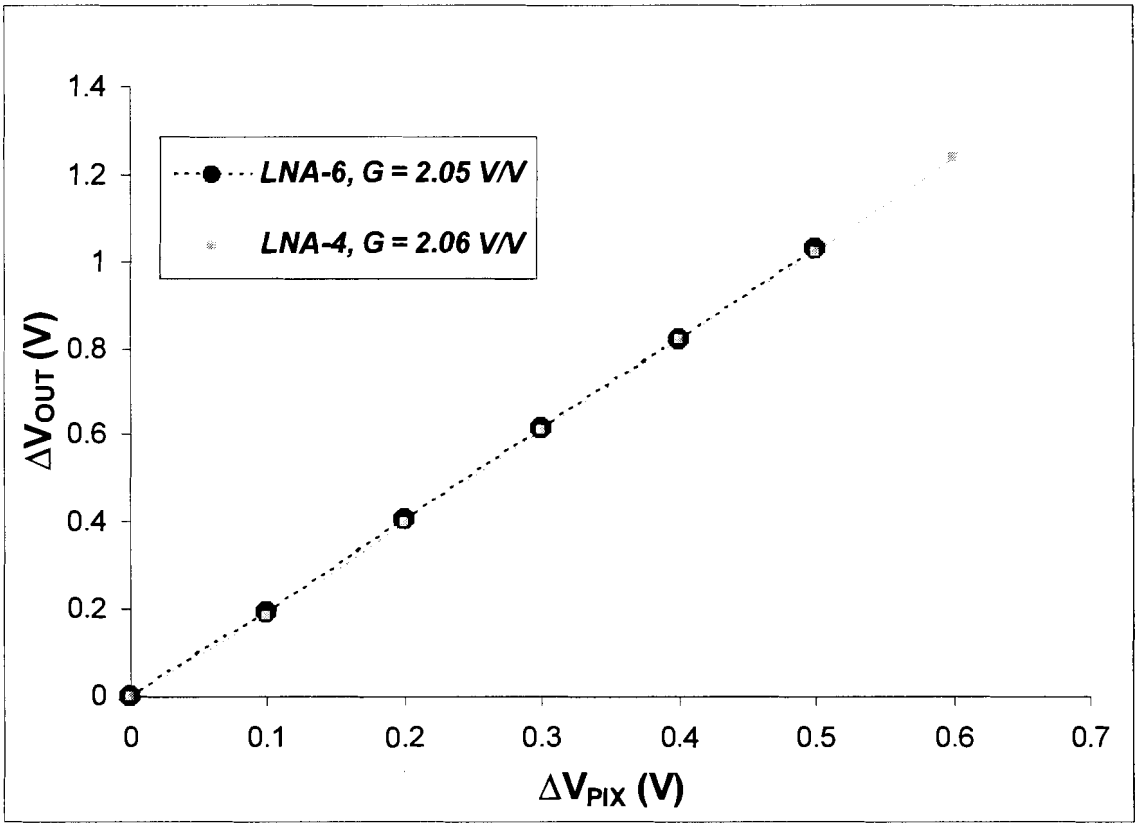

Figure 18 Post-Layout Simulations of Medical Imaging Readout Solution I with LNA-4 and LNA-6

After comparing pre-layout and post-layout solutions of each standalone LNA, and pre-layout simulations of each LNA in the entire readout solution, LNA-4 and LNA-6 were deemed the best candidates for fabrication. The CFC designs occupied more area than was desirable in the allotted area of 1 mm^2, and therefore were not chosen for fabrication. LNA-2 and LNA-5 were also not chosen for fabrication as they could not consistently achieve a pixel gain of 2 V/V in pre-layout simulations of the readout circuitry. However, any LNA could be fabricated to form the medical imaging readout solution if desired, as they each provide a respectable pixel gain when substituted for the ideal amp in the system, as shown in Table 6. Post-layout readout circuit simulations for LNA-4 and LNA-6 are presented in Figure 18. The post-layout simulation data indicates that both LNA-4 and LNA-6 are capable of achieving a pixel gain of 2.06 V/V and 2.05

V/V, respectively in MIRS I. Hence, both LNAs were implemented on the IC for fabrication. Since area restrictions allowed for only one medical imaging readout solution on the die, it was decided the readout circuit would use LNA-6 for structures ***A*** and ***B***, as the 3.3 V transistors added greater breakdown voltage protection, and hence a more robust readout architecture. Area limitations restricted implementing on-chip feedback resistors and an on-chip integrating capacitor with the overall circuit solution, and hence were not included. CMOS transmission gate switches are placed at the input of the readout solution to decouple the architecture from the C-APS output, if required[3]. A CMOS transmission gate also controls the C_RST control signal that resets charge amplification of the integrator. Inverters were used to save pins on the IC package and die, as the switches utilized them to invert the control signal from the NMOS transistor to the PMOS device in the CMOS pair.

Table 6 Pre-layout Simulations of Medical Imaging Solution I

	Pixel Gain (V/V)	
Design	**ΔV_{PIX} of 10 mV**	**ΔV_{PIX} of 1 V**
LNA-1 (0.8 V Bias)	**2.06**	**2.12**
LNA-2	**1.90**	**2.14**
LNA-3 (2.3 V Bias)	**1.90**	**1.68**
LNA-4	**2.00**	**2.11**
LNA-5	**1.90**	**2.15**
LNA-6	**2.00**	**2.03**

[3] Jan M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, 2nd ed, (New Jersey: Prentice Hall, 2003), 269-284.

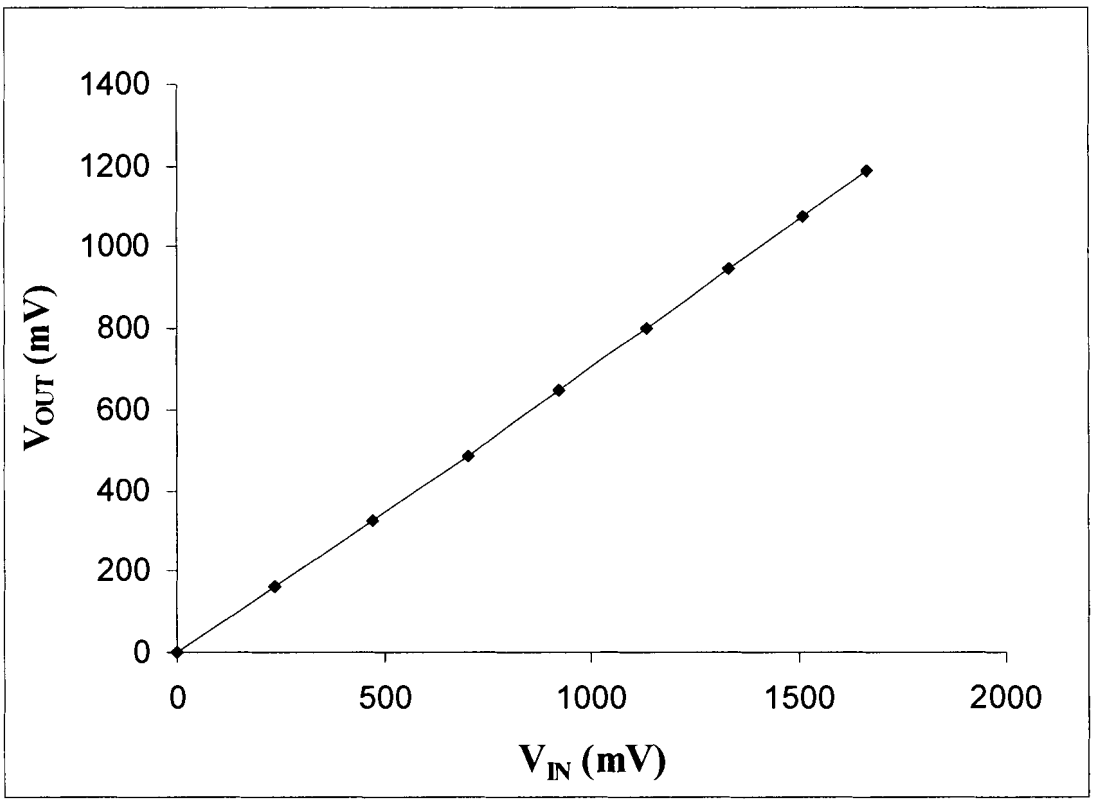

Figure 19 Post-Layout Simulations of the Attenuation Architecture

Chest radiography pre-layout simulations were conducted using the attenuation design containing the voltage buffer described as structure ***C***, and an R_L of 1 MΩ. Pre-layout and post-layout simulations indicate that the linear relationship between input and output extends for an input sensor voltage change, Δ V_{PIX}, of 9 V. The post-layout simulation for the attenuation architecture is displayed in Figure 19. The simulation data indicates the voltage buffer in the architecture provides an average gain of 0.70 V/V. The design translates a Δ V_{PIX} of 9 V into an output voltage of 1.7 V and as such attenuates the high exposure inputs to a readout circuit voltage of 0.19 V/V. The attenuation architecture was fabricated as a standalone structure on the die. However, structures ***A*** and ***B*** were replaced with LNA-4 to simulate the different loading effects of the amplifier at the pixel output should the structures eventually be combined as one on an IC solution

at some later time. The average voltage gain for the buffer and attenuation value for the radiography architecture with LNA-4 in post-layout simulations remains 0.70 and 0.19 V/V, respectively.

6.1.2 PCB Testing and Results

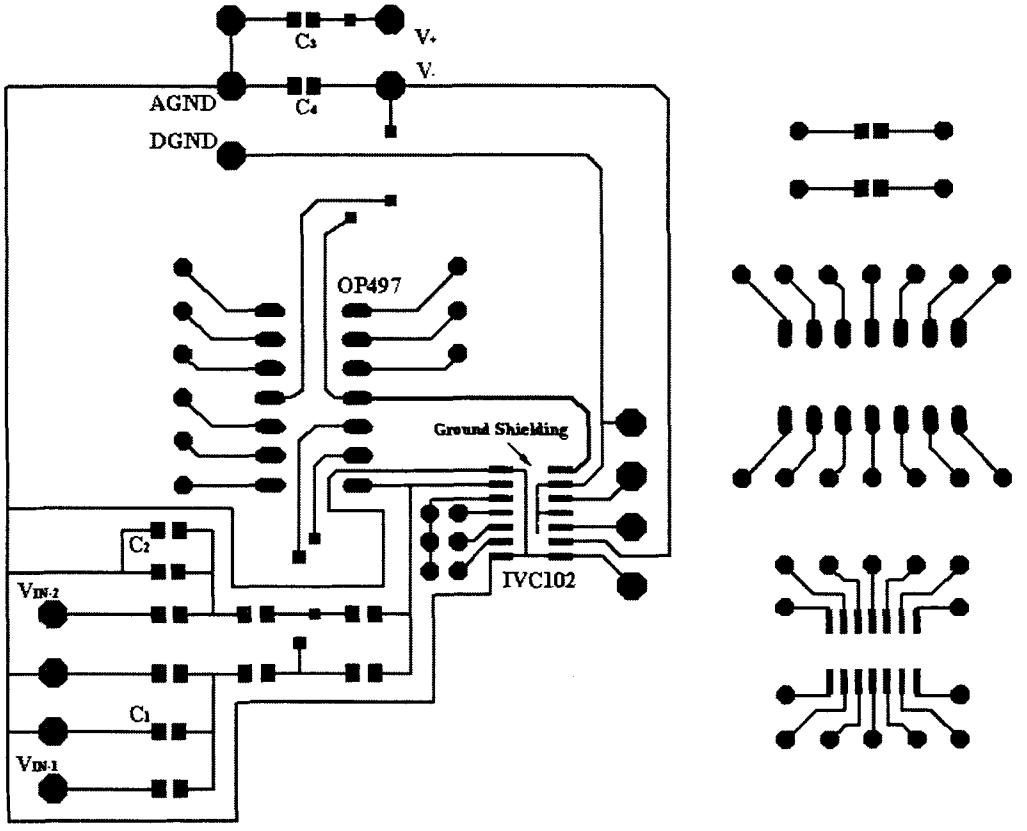

Figure 20 Layout of PCB Component Side

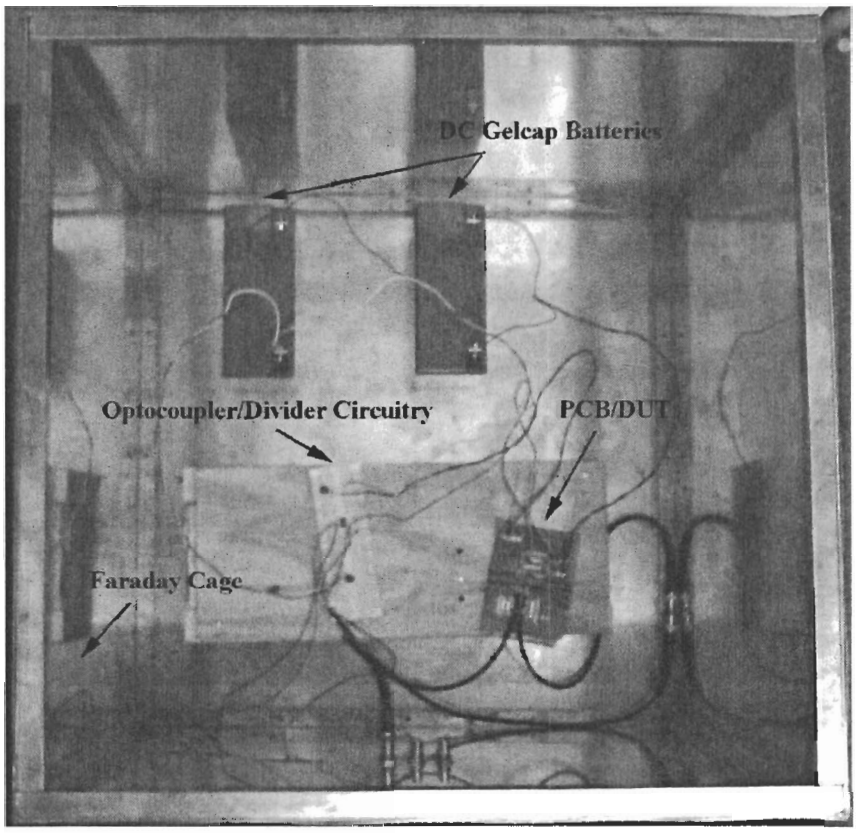

Figure 21 PCB/DUT Test Setup

The digital fluoroscopic hardware of MIRS I was constructed on a PCB comprised of IC and shelf components. The circuit results from the PCB would serve as a comparison with results obtained from the IC solution. The OP497 component from Analog Devices was used as the op amp for the subtractor, structure ***A***, in the readout solution [11]. The IVC102 device from Burr Brown was used as the integrator, structure ***B***, in the readout architecture [12]. Layout considerations for the PCB included shielding the digital traces around the integrator with ground traces. The discrete components were placed close to each other to reduce the length of connecting traces as much as possible. Capacitors at the signal and power inputs were also used to improve the output response. The layout of the PCB component side is shown in Figure 20. Noise sources were

eliminated systematically from the board to improve test results and achieve the best possible resolution from the PCB version of the readout circuitry. Low noise metal film resistors replaced thick film surface mount chip resistors to improve circuit performance. Also, DC gelcap batteries replaced the variable DC power supply in the design to reduce circuit noise. The required input voltage sources were obtained by dividing down the power source with low noise resistors arranged as dividers. An optocoupler was also used to reduce noise from the digital C_RST input signal provided by the waveform generator. The PCB was tested in a faraday cage to shield the tests from external electromagnetic interference (EMI). The test setup for the PCB is shown in Figure 21.

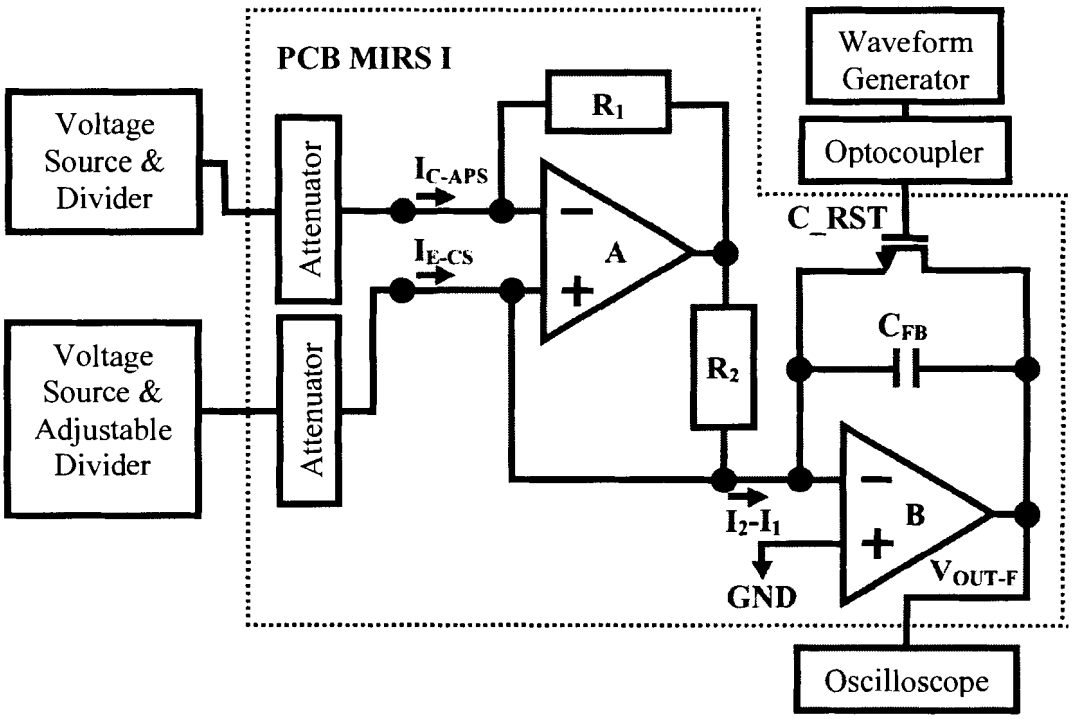

Figure 22 Test Strategy for the PCB Version of MIRS I

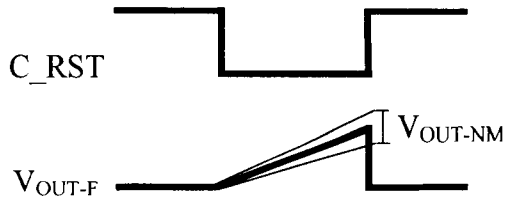

Figure 23 Transient Response of V_{OUT-F}

A battery acting as the voltage source generated a reduced voltage input through a divider, which then passed through an on-board attenuator to produce the input currents I_{C-APS} and I_{E-CS} for MIRS I, as shown in Figure 22. The voltage output of MIRS I was observed on an oscilloscope. Tests were conducted on the readout solution at frequencies comparable with the readout speeds required for digital fluoroscopy: 1, 5, 10, and 20 KHz. The tests were repeated twice for different integrating capacitances, C_{FB}, of 10 and 100 pF. For each frequency, I_{C-APS} was left fixed while I_{E-CS} was varied by tuning the adjustable voltage divider that provides the current source. I_{E-CS} was adjusted to cancel out I_{C-APS} allowing for no integration at the output signal. I_{E-CS} was then adjusted in increments to allow for both positive and negative integration, while the output voltage and output voltage variation were simultaneously recorded. It is the output noise voltage variation, V_{OUT-NM}, that was used to determine the minimum C-APS output current achievable for MIRS I, as illustrated in Figure 23. The lower the output noise margin of the readout circuit, the lower the I_{C-APS} current will be needed to discern the pertinent output voltage. The minimum C-APS output current was determined from the following equation:

$$I_{C-APS(\min)} \approx \frac{V_{OUT-NM} \times C_{FB}}{t_{INT}}, \text{ where } t_{INT} = \frac{1}{2} \cdot \frac{1}{f}.$$

Results from hardware testing indicate the minimum achievable C-APS output current that can be discerned at the digital fluoroscopic output from medical imaging readout solution I, is 1.74 nA. The results of hardware testing MIRS I are summarized in Table 7. This resolution was obtained at 1 KHz and with an integrating capacitor of 100 pF. This is not a desired result as the circuitry must be able to handle 5 KHz or better, since that is the typical readout speed that a large area flat panel array will require of the design to process X-ray inputs. Furthermore, as the design will ultimately be required to be implemented on an IC solution, the large integrating capacitance of 100 pF will take a considerable amount of area if implemented on a die. Lastly, the best possible C-APS output current obtained from hardware testing is still significantly more than 1 nA. The aspiration of the architecture would have been to integrate C-APS currents lower than 1 nA. As it is low dose X-rays that produce small currents at the output of the C-APS, a lower dosage would pose less harm to a patient when examined with fluoroscopic equipment. Therefore, the best readout architecture should be able to detect and process the smallest possible C-APS output current possible. The amount of current at the input of the readout design is limited by the noise introduced by the noise present in the C-APS itself, and from the readout circuitry. As the goal is to develop an enhanced readout solution for a C-APS approach, the attention has been to reduce the noise originating from the circuitry. Although the results of the PCB version of the readout design were not promising, the IC solution may provide better results, as traces can be shielded better and made smaller on a die than a board.

Table 7 Resolution Achievable by PCB Version of Medical Imaging Solution I

	C-APS Output Current Resolution (nA) per Frequency of C_RST Signal			
Integrating Capacitor	**1 KHz**	**5 KHz**	**10 KHz**	**20 KHz**
10 pF	**15.2**	**28.0**	**30.0**	**26.6**
100 pF	**1.74**	**4.88**	**7.20**	**11.4**

Hardware testing of the design has also shown that the SNR performance of the readout solution is extremely poor when the external current source, $I_{E\text{-}CS}$, is tuned to zero out the C-APS output current, $I_{C\text{-}APS}$, in Figure 22. That is, when the two currents were roughly made equivalent. The SNR of the system improves noticeably as the output voltage, $V_{OUT\text{-}F}$, after integration approaches either the positive or negative supply rail. The result of these observations suggests that $I_{E\text{-}CS}$ should be adjusted to allow some integration of $V_{OUT\text{-}F}$ when no light-sensitive input has been detected. The inherent bias voltage at the output will then be compared with light-sensitive output voltage responses to obtain the relevant signal for processing. In this way, small readout output voltages from low dose inputs will not be compromised by the excessive noise apparent when $V_{OUT\text{-}F}$ is in close proximity to zero.

6.1.3 IC Test Results

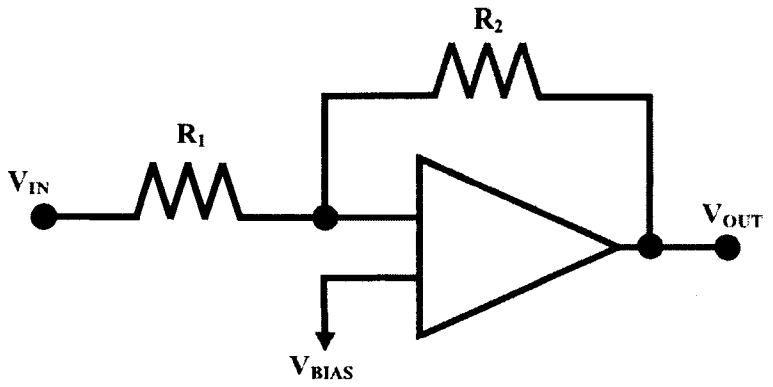

Figure 24 Inverting Closed-Loop Test Circuit for LNA-6

Preliminary test results of the IC have verified that LNA-6 is operational and functioning correctly. As this op amp serves as structures ***A*** and ***B*** in the IC version of MIRS I, it is believed the readout architecture will also function properly. LNA-6 was tested with the inverting closed-loop configuration shown in Figure 24. Using feedback resistors R_1 = 1 MΩ and R_2 = 15 MΩ, an output gain of 15.8 V/V was observed at the output as compared to the ideal gain of 15 V/V. Using feedback resistors R_1 = 0.5 MΩ and R_2 = 1 MΩ, an output gain of 2.11 V/V was observed at the output as compared to the ideal gain of 2 V/V. LNA-4 has not been verified to operate like LNA-6 at this time. However, the external bias resistor that provides the correct bias current to the first stage of the op amp was measured to be roughly the same voltage drop as that seen in post-layout simulations. This was also the case when verifying LNA-6. Moreover, it took time to place the proper bias on LNA-6 to observe correct operation of the amplifier.

Other verified components on the IC include a standalone 1 MΩ resistor that resembles the resistor used in the attenuation architecture of the readout solution. The on-chip resistor was measured to be 1.237 MΩ from the pins on the IC package.

6.1.4 Noise Discussion

The largest resistor used in the testing of MIRS I on the PCB was 100 KΩ, and that component provides an estimated noise rating of 33.1 pV^2 at 20 KHz, as determined by the noise voltage across a resistance given by the following thermal noise equation:

$$v_R^2 = 4kTBR \text{ V}^2/\text{Hz},$$

where k is the Boltzmann's constant 1.38 x 10^{-23} J/K

T is the Temperature in Kelvin

B is the frequency bandwidth in Hz

and R is the resistance of the device in Ω.

With all the resistor components utilized in the test circuit and in the feedback implementation of the subtractor, the combined resistor noise would still not add up to the noise generated by the IC op amp components. The OP497 and IVC102 devices are rated at 15 and 10 nv/√Hz at 1 KHz obtained from their published data specifications, respectively [11, 12]. Metal film resistors with a 1% tolerance rating were used for both the test circuit and design. Of the two op amps used, OP497 generates the most noise in the readout circuit.

6.2 Medical Imaging Readout Solution II

6.2.1 PCB Testing and Results

The digital fluoroscopic hardware of MIRS II was also constructed on a PCB comprised of IC and shelf components. Successful results from the PCB design of the readout solution will lead to the eventual IC implementation of the architecture. The ZVP4105A PMOS transistor from Zetex Inc. and the IVC102 served as the most

important devices in the readout solution. The IVC102 once again served as the integrator, structure *A*, in the alternative readout architecture. The ZVP4105A served to direct the DC bypass current from the integrator. The PCB designed for MIRS I was the same PCB used for MIRS II. Noise sources were similarly eliminated from board testing with low noise metal film resistors, DC gelcap batteries, placing an optocoupler between the digital C_RST input and the waveform generator, and by using a faraday cage for EMI shielding.

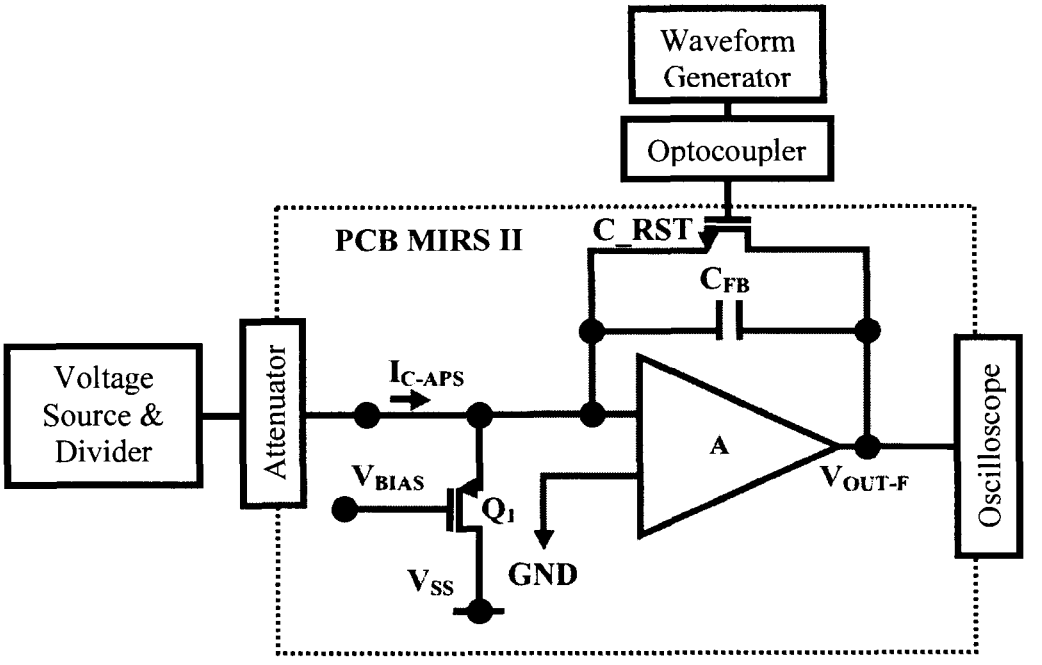

Figure 25 Test Setup for the PCB Version of MIRS II

The current I_{C-APS} for MIRS II was generated from a battery voltage source through a divider and attenuator, as shown in Figure 25. Tests were again conducted on the readout solution at the following frequencies: 1, 5, 10, and 20 KHz. The tests were also repeated for the two integrating capacitances, C_{FB}: 10 and 100 pF. For each frequency, I_{C-APS} was left fixed while the gate voltage, V_{BIAS}, on Q_1 was varied until no integration was observed at the output signal. V_{BIAS} was then adjusted in increments to

allow for both positive and negative integration, while the output voltage and output voltage variation were simultaneously recorded. The minimum C-APS output current for MIRS II was determined identically with the procedure that was used for MIRS I.

Results from hardware testing indicate the minimum achievable C-APS output current that can be discerned at the digital fluoroscopic output from MIRS II, is 0.341 nA. The results of hardware testing MIRS II are summarized in Table 8. This resolution was obtained at 1 KHz and with an integrating capacitor of 10 pF. The results are very promising as the architecture is capable of detecting and integrating C-APS output currents below 1 nA which was not attainable with MIRS I. Results also show that the readout circuitry is capable of resolving currents below 1 nA with a 10 pF integrating capacitor for the entire frequency range tested. The design can also resolve currents below 1 nA with a 100 pF integrating capacitor at 5 KHz. Hence, the data suggests several important outcomes for the readout architecture. Firstly, the architecture can resolve C-APS outputs signals significantly below 1 nA and at readout speeds required of X-ray imagers designed with C-APS structures. Secondly, the architecture can achieve this resolution with a smaller integrating capacitor than that which was seen for the previous readout solution. Therefore, the integrating capacitor if implemented with the readout solution on an IC solution will take considerably less area on a die. Furthermore, as the subtraction method consists of only one single PMOS transistor, as compared to MIRS I that uses an additional op amp with feedback resistors, MIRS II is itself a much smaller solution. Hence, MIRS II surpasses MIRS I as the preferred architecture. It is expected that if MIRS II is fabricated on an IC that even better test results may be obtained, since the lower voltage rails supplied to the CMOS components should reduce

the noise stemming from those devices in the design. The apparent success of the architecture is due to the minimum amount of extra circuitry needed by the design to subtract out the unwanted C-APS output current. As a single PMOS transistor will obviously add less noise to a design, than was seen by the subtractor circuit in MIRS I for example, the amount of readout noise introduced into the system is minimized. Therefore, MIRS II can readily resolve and process lower C-APS output currents. A notable design requirement of MIRS II is to bias Q_1 in Figure 13 such that the necessary subtraction current will be allowed to flow through the transistor. For hardware tests, the bias voltage on Q_1 placed the device in the subthreshold region where the subtraction current can be made small enough to tune the C-APS output current.

Table 8 Resolution Achievable by PCB Version of Medical Imaging Solution II

	C-APS Output Current Resolution (nA) per Frequency of C_RST Signal			
Integrating Capacitor	**1 KHz**	**5 KHz**	**10 KHz**	**20 KHz**
10 pF	**0.341**	**0.660**	**0.768**	**1.28**
100 pF	**-**	**0.464**	**4.96**	**11.7**

Despite the positive results from the architecture during hardware testing, there are some notable challenges with the PCB version of the system. The most noticeable problem encountered with the design during hardware testing, was the drift of the integration curve towards the negative rail. This phenomenon had the affect of changing the readout output voltage for a given input, set by the external current source, over a minimum period of 10 mins. The observed drift problem was pronounced for the hardware test conducted with a 100 pF integrating capacitor at 1 KHz, such that it

prevented obtaining reasonable data in that instance. The cause for the drift in the circuit is attributed to the ZVP4105A PMOS transistor which is rated as having a zero gate voltage drain current anywhere between 100 nA to 15 μA, and a gate-body leakage current of 10 nA. Ideally, Q_1 in the readout circuit should be a low noise, low leakage, PMOS transistor. As the readout circuit architecture would process signals at speeds many times faster than a minute, the problem is not deemed serious. Also, when collecting the data from the scope, the output voltage was periodically adjusted towards the positive voltage rail to conservatively obtain the resolution measurements in Table 8, in the presence of the drift problem. Measurements of the system adjusted to the negative rail have produced even better results than stated in hardware testing, and with an optimal PMOS component data can be expected to be even more impressive for the architecture. It is deemed that the results of MIRS II have been so successful that the design warrants being fabricated on a next generation IC. As LNA-6 is fully operational, it is only a formality to place an additional PMOS device at the V_- terminal and test the architecture. An additional drawback with this implementation includes providing a stable bias at the gate of Q_1 to properly subtract the necessary DC current. Also, the parasitic capacitance from Q_1 may affect signal integration. However, the parasitic capacitance is negligible in comparison to a 10 pF integrator capacitor, for instance. As the source of Q_1 is connected to ground in the PCB design, the parasitic capacitance had no affect at all on hardware tests results.

6.2.2 Noise Discussion

MIRS II consisted of the IVC102 op amp and the ZVP4105A PMOS transistor. Since the transistor operates in the subthreshold region it will be modeled for simplicity

as a resistor with a shot noise component. ZVP4105A was placed in series with a 100 Ω ± 1% metal film resistor for noise testing. The same bias used in hardware testing of MIRS I was placed at the gate of the transistor. The voltage drop across both series elements was also the same voltage drop across ZVP4105A during PCB testing. As the input voltage and the voltage across the 100 Ω resistor were both known, the source-to-drain resistance of ZVP4105A at the subthreshold gate bias was determined to be approximately 1.39 KΩ. This resistance would give a noise rating of 0.46 pV^2 at 20 KHz. The shot noise through the device is determined by the subsequent equation:

$$v^2 = 2qIBR\ V^2/Hz,$$

where q is the charge of an electron given as 1.6×10^{-19} C/e^-

I is the average current flowing through the device in A

B is the bandwidth in Hz

and R is the resistance of the device in Ω.

The shot noise for the device was estimated to be 77 fV^2/Hz for a 20 KHz bandwidth. The total noise for the transistor is approximately 0.47 pV^2 for the frequency range of operation, and is negligible in comparison to noise originating from the IVC102. This measurement verifies that MIRS II has less readout noise than MIRS I.

7 Conclusions

Two low noise medical imaging readout solutions were successfully designed to increase the dynamic capabilities of current-mediated amorphous silicon active pixel sensors, and to enhance their practicality in diagnostic X-ray imaging applications. Medical imaging readout solutions I and II permits the functionality of real-time digital fluoroscopy. Medical imaging readout solution I and the attenuation architecture was fabricated in CMOS 0.18 μm technology and post-layout simulated in Cadence with SpectreS and HSpiceS models. MIRS I and II were also hardware tested on a PCB.

The attenuation circuitry has been shown to enhance the dynamic range of the C-APS pixels for radiographic applications for a range of 9 V, where digital fluoroscopic applications can produce no more than 0.8 V of sensor input change from post-layout simulations.

Medical imaging readout solution II has been shown from hardware testing to be the better architecture over readout solution I. The architecture provides better signal processing performance, introduces less noise, and utilizes less area as a readout circuit. Both digital fluoroscopic hardware readout circuits are able to subtract the superfluous DC bias current accompanying the input signal before charge amplification during readout.

Thus far, IC testing has verified that LNA-6 is a fully functional as an op amp. This op amp is utilized on the on-chip adaptation of MIRS I, and hence will likely provide IC test results to compare with the identical PCB circuit.

MIRS II has surpassed expectations as a plausible readout circuit, and will be fabricated on an IC in a later design. The design has shown in hardware that it is capable of resolving C-APS output currents up to 0.341 nA, and possibly lower with improved lower noise hardware.

In summary, a low noise readout architecture has been designed and verified in hardware to aid in the production of a cost-effective large panel X-ray imager that will aid medical practitioners and pose less harm to patients.

8 Appendices

8.1 Appendix I: LNA Schematics

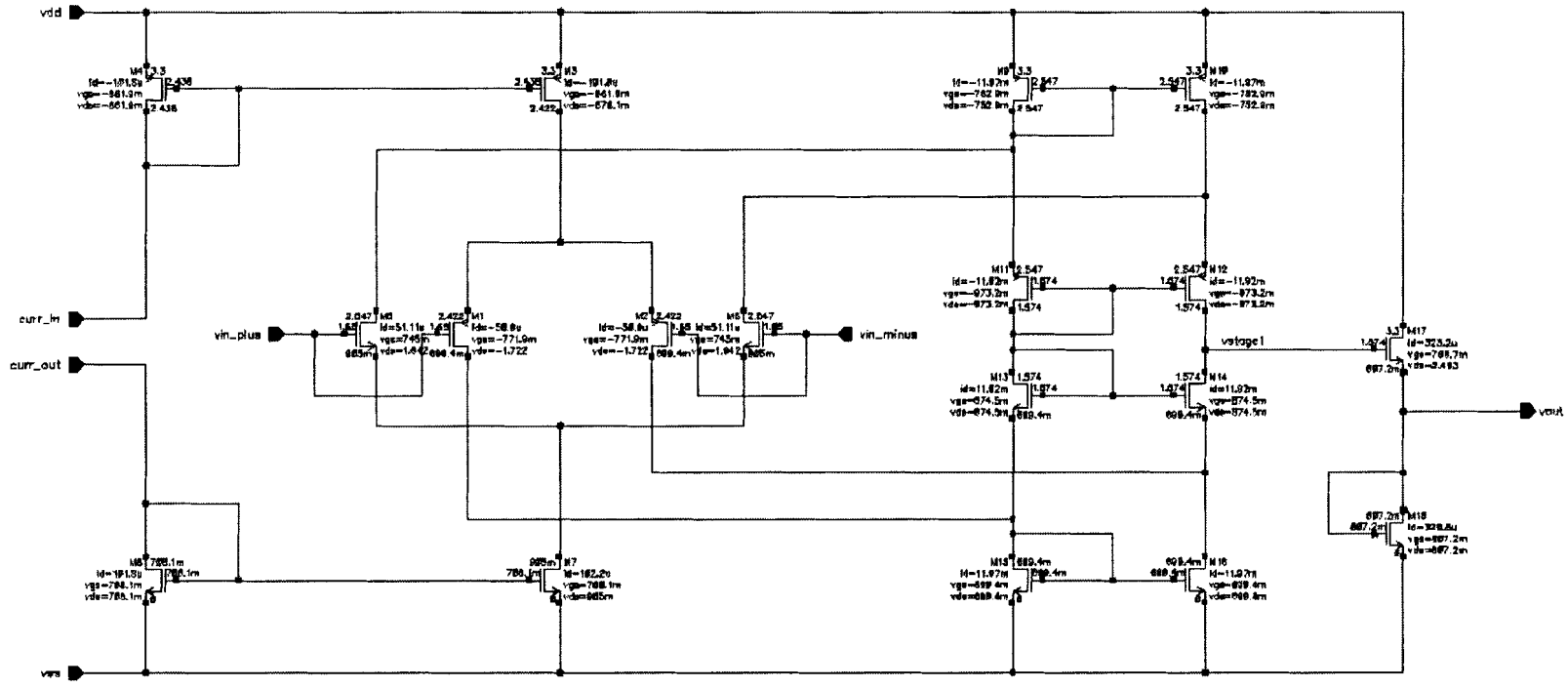

Figure 26 CFC Schematic of LNA-1

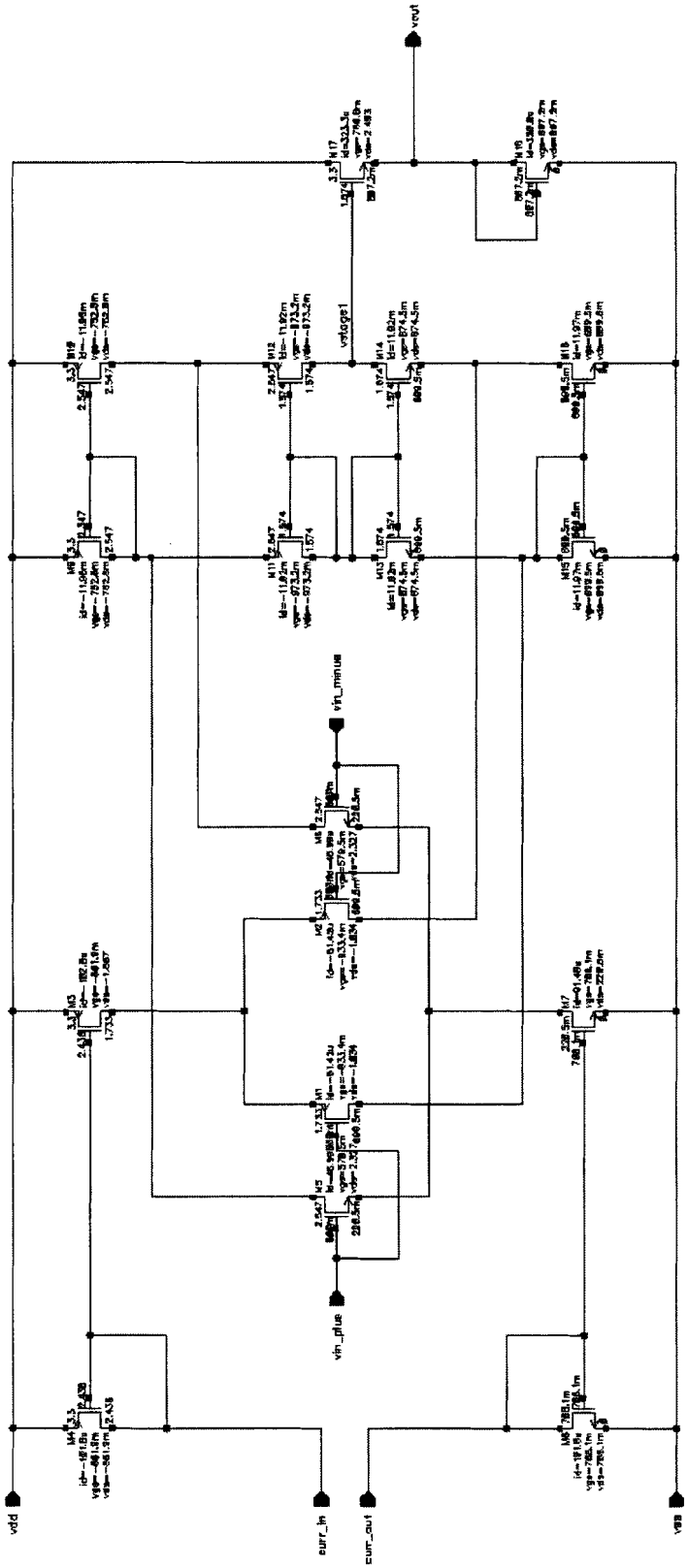

Figure 27 CFC Schematic of LNA-1 at 0.8 V Input Bias

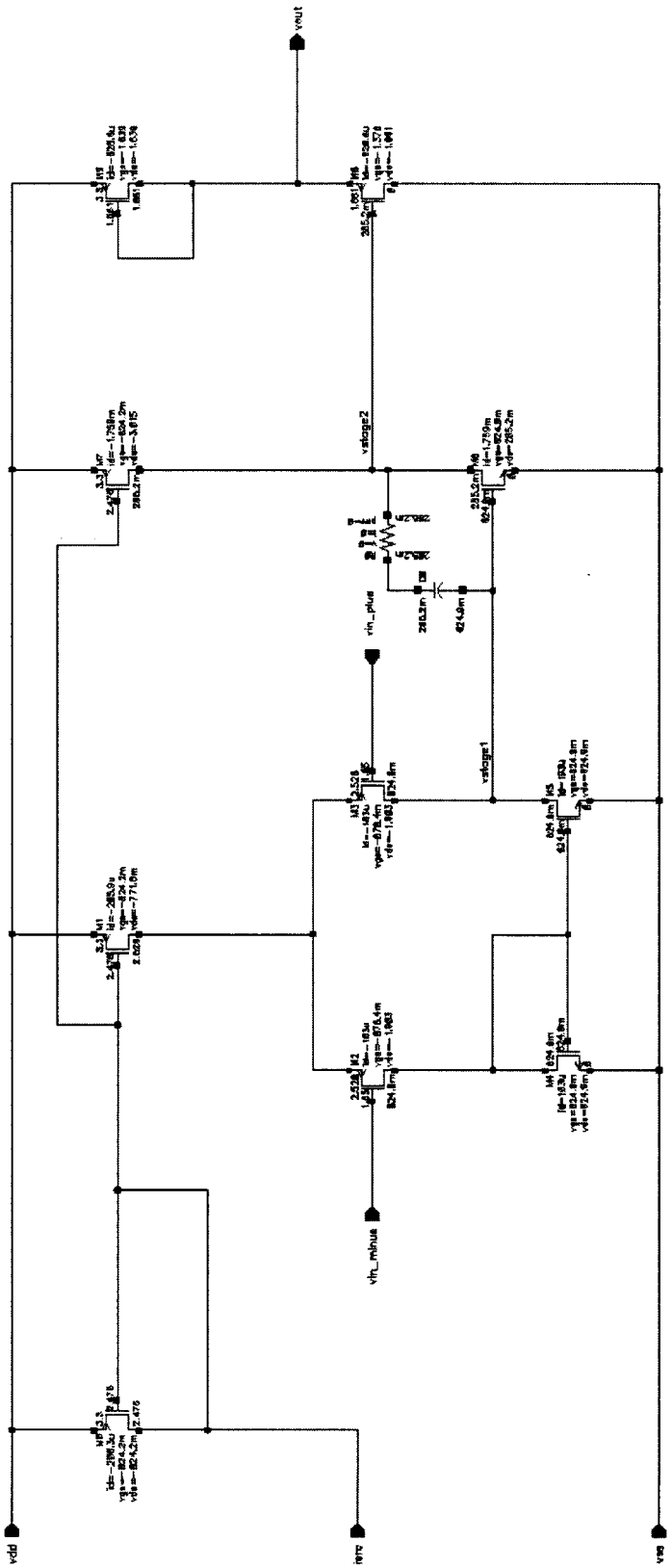

Figure 28 Two-Stage Amplifier Schematic of LNA-2

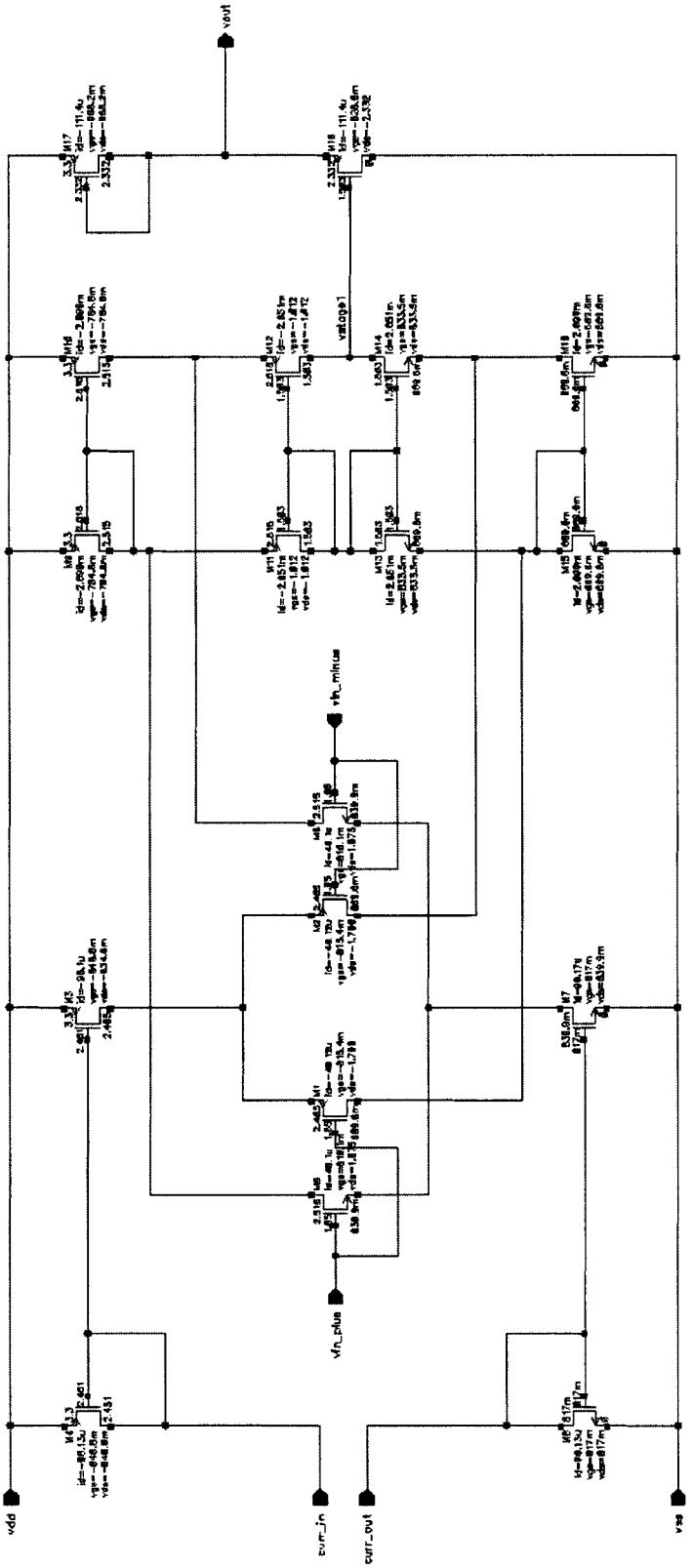

Figure 29 CFC Schematic of LNA-3

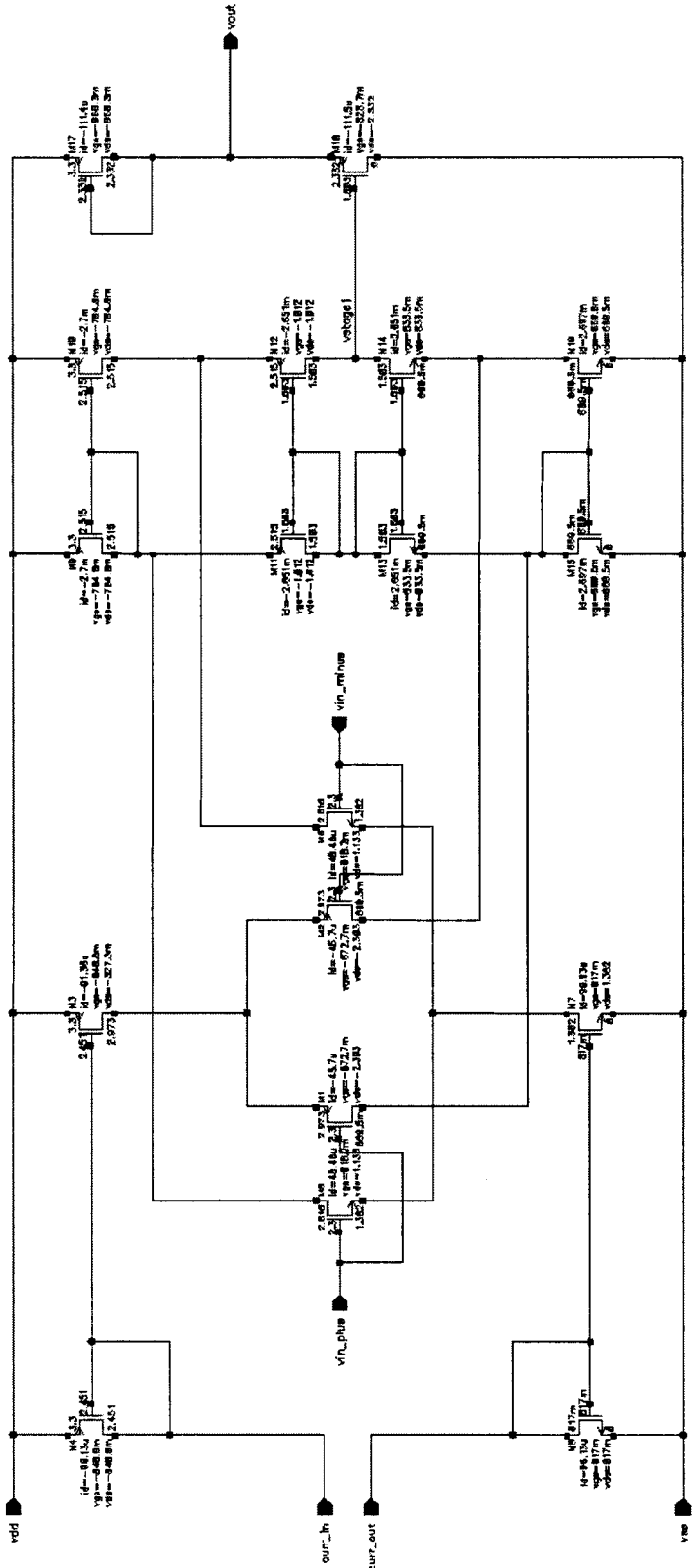

Figure 30 CFC Schematic of LNA-3 at 2.3 V Input Bias

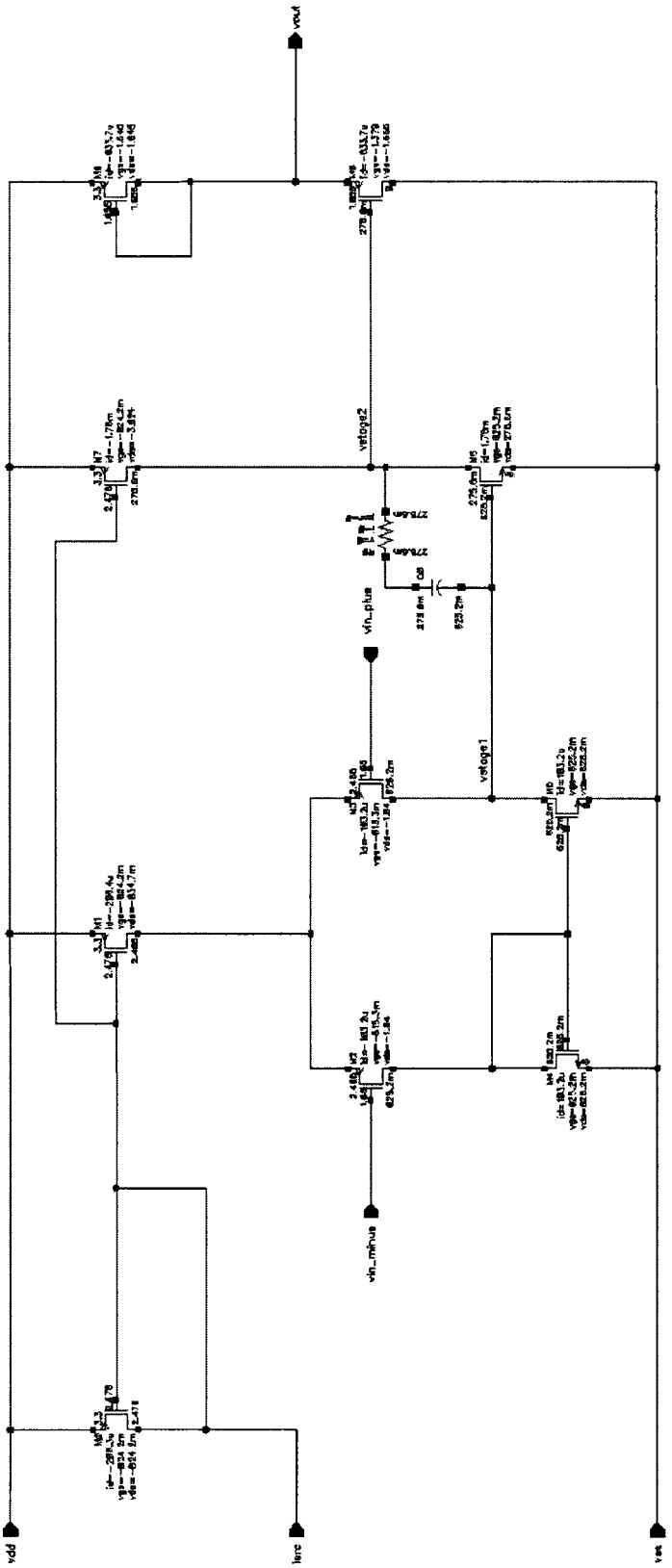

Figure 31 Two-Stage Amplifier Schematic of LNA-4

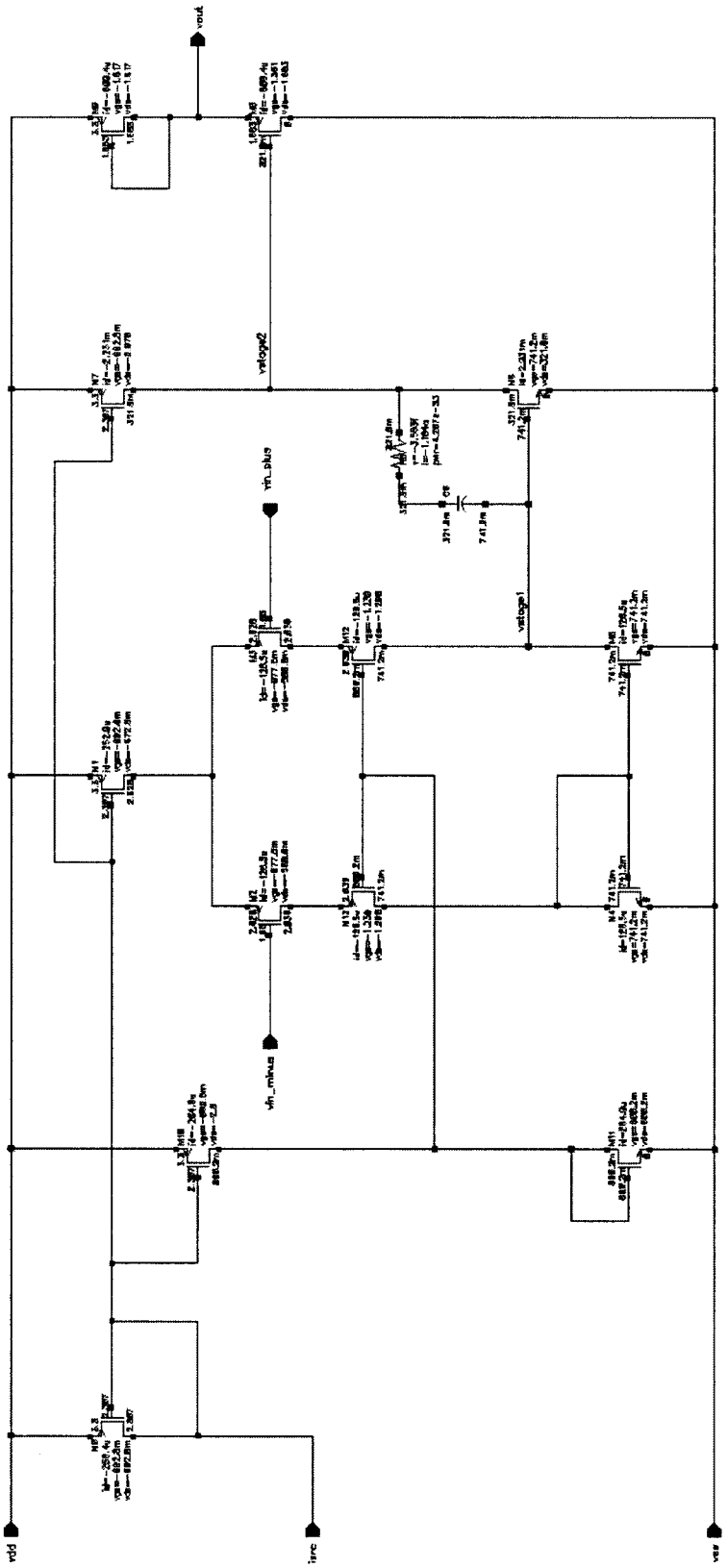

Figure 32 Two-Stage Amplifier Schematic of LNA-5

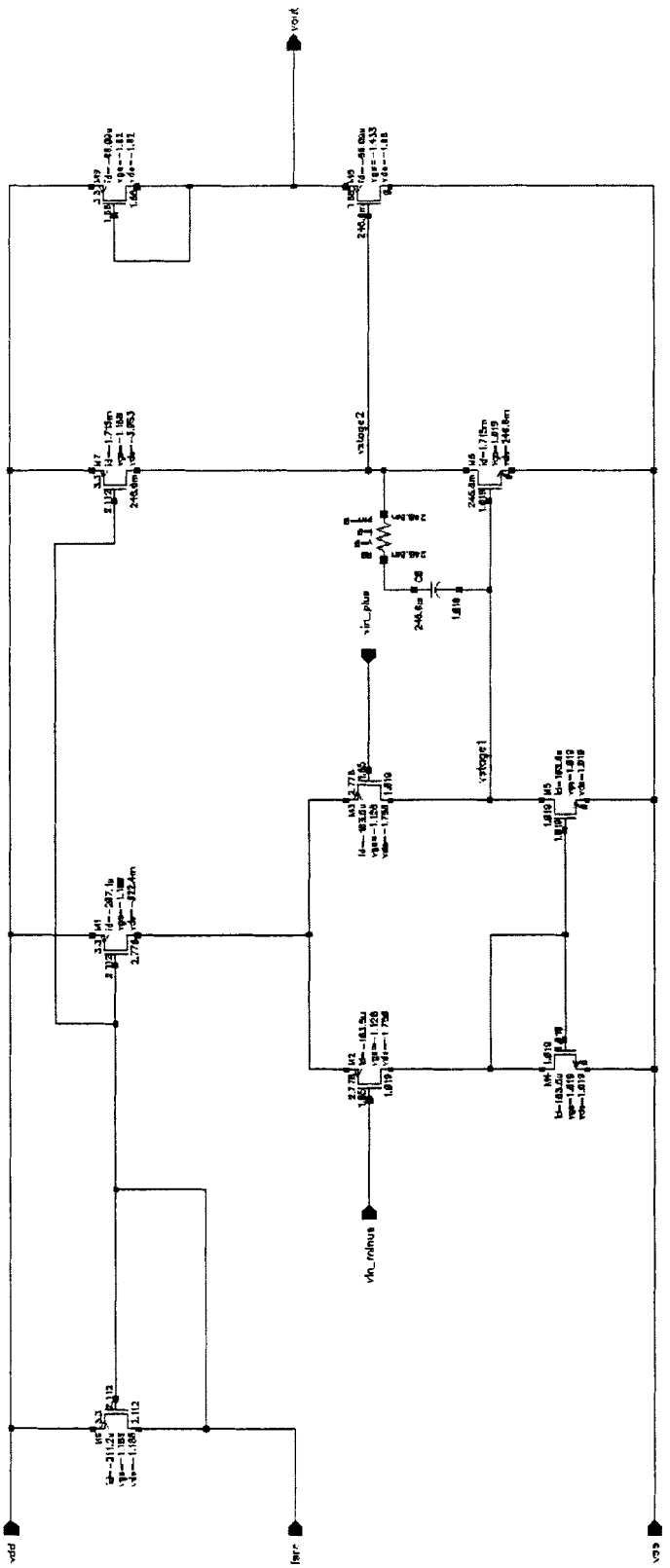

Figure 33 Two-Stage Amplifier Schematic of LNA-6

8.2 Appendix II: Small Signal AC Analysis of LNA Architectures

8.2.1 CFC

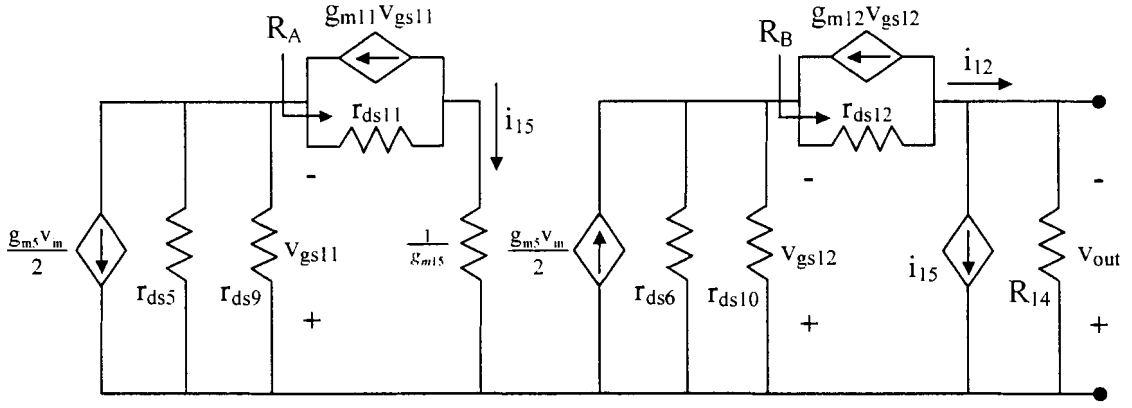

Figure 34 Small Signal Model for an n-Channel Folded-Cascode

The small signal model for an n-Channel Folded Cascode is presented in Figure 34. The ac analysis for this architecture is identical to that of the CFC in Figure 26, excluding the p-Channel input pair circuitry. The n and p channel differential input pairs can be considered independently for the CFC small signal analysis in regions I and III, and those results can be extrapolated to estimate the behavior of the design in region II.

The first step in analyzing the CFC model is to write a KVL equation at the M_6-M_{10}-M_{12} juncture in Figure 34, resulting in a circuit diagram of Figure 35.

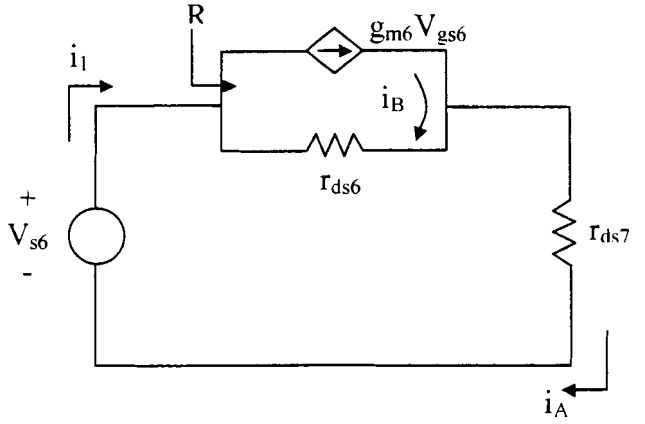

Figure 35 KVL Equation at M_6-M_{10}-M_{12} Juncture

The following equations can then be written:

$$V_{gs6} = V_{s6},\ i_A = i_1$$

$$V_{s6} = (i_1 - g_{m6}V_{gs6})r_{ds6} + i_A \cdot r_{ds7}$$

$$= (i_1 - g_{m6}V_{s6})r_{ds6} + i_1 \cdot r_{ds7}$$

$$= i_1(r_{ds6} + r_{ds7}) - g_{m6}V_{s6}r_{ds6}$$

$$V_{s6}(1 + g_{m6}r_{ds6}) = i_1(r_{ds6} + r_{ds7})$$

$$\therefore R = \frac{V_{s6}}{i_1} = \frac{(r_{ds6} + r_{ds7})}{(1 + g_{m6}r_{ds6})}$$

Consequently, $R_A = \dfrac{r_{ds11} + \dfrac{1}{g_{m13}}}{1 + g_{m11}r_{ds11}} \approx \dfrac{1}{g_{m11}}$ (since $\dfrac{1}{g_{m13}}$ is negligible).

$$R_B = \frac{r_{ds12} + R_{14}}{1 + g_{m12}r_{ds12}} = \frac{r_{ds12} + g_{m14}r_{ds14}r_{ds16}}{1 + g_{m12}r_{ds12}} \text{ (since } R_{14} \approx g_{m14}r_{ds14}r_{ds16})$$

$$\approx \frac{g_{m14}r_{ds14}r_{ds16}}{g_{m12}r_{ds12}} = \frac{R_{14}}{g_{m12}r_{ds12}} \approx r_{ds14} \text{ (assuming } g_{m12} \approx g_{m14} \text{ and } r_{ds12} \approx r_{ds16})$$

After obtaining the output resistances R_A and R_B, the small signal model of Figure 34 is redrawn to that of Figure 36, to ultimately give the small signal characterization of the CFC.

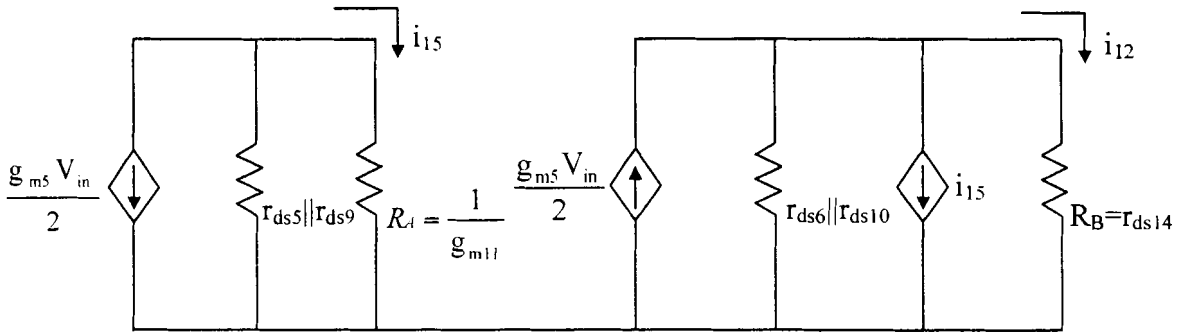

Figure 36 Redrawn Small Signal Model of Figure 34

$$i_{15} = -\frac{g_{m5}v_{in}}{2}\frac{(r_{ds5} \parallel r_{ds9})}{\frac{1}{g_{m11}} + (r_{ds5} \parallel r_{ds9})} \approx -\frac{g_{m5}v_{in}}{2}$$

$$i_{12} = \frac{g_{m6}v_{in}}{2}\frac{(r_{ds6} \parallel r_{ds10})}{\left[\frac{R_{14}}{g_{m12}r_{ds12}} + (r_{ds6} \parallel r_{ds10})\right]} = \frac{g_{m6}v_{in}}{2}\frac{1}{1 + \frac{R_{14}}{g_{m12}r_{ds12}(r_{ds6} \parallel r_{ds10})}} \text{ (where } g_{m5} = g_{m6})$$

$$= \frac{g_{m6}v_{in}}{2}\frac{1}{1 + \frac{R_{14}(g_{ds6} + g_{ds10})}{g_{m12}r_{ds12}}} = \frac{g_{m6}v_{in}}{2}\frac{1}{1+k} \text{ (where } k = \frac{R_{14}(g_{ds6} + g_{ds10})}{g_{m12}r_{ds12}})$$

Note that although transistors M_9 and M_{11} are diode connected transistors for the CFC, they will produce approximately the same result in the equations above.

Region III (n-channel Differential Input Pair)

$$\therefore A_{vn} = \frac{v_{out}}{v_{in}} = (i_{12} + i_{15})R_{II} = \left[\frac{g_{m5}}{2} + \frac{g_{m6}}{2(1+k)}\right]R_{II}$$

$$= \left[\frac{g_{ml}(1+k) + g_{ml}}{2(1+k)}\right]R_{II} \text{ (where } g_{ml} = g_{m5} = g_{m6})$$

$$= \left(\frac{2+k}{2+2k}\right)g_{ml}R_{II}$$

$R_{II} = (g_{m14}r_{ds14}r_{ds16}) \parallel [g_{m12}r_{ds12}(r_{ds6} \parallel r_{ds10})]$ (r_{out} of the n-channel folded-cascode)

$k = \frac{R_{14}(g_{ds6} + g_{ds10})}{g_{m12}r_{ds12}}$ and $R_{14} = g_{m14}r_{ds14}r_{ds16}$

Also, $p_{dom} = \frac{1}{R_{II} \cdot C_L}$ and $GB = \left(\frac{2+k}{2+2k}\right)g_{ml}R_{II}\frac{1}{R_{II} \cdot C_L} = \left(\frac{2+k}{2+2k}\right)\frac{g_{ml}}{C_L}$

Region I (p-channel Differential Input Pair)

$$\therefore A_{vn} = \frac{v_{out}}{v_{in}} = \left(\frac{2+k}{2+2k}\right) g_{m1} R_{II} \quad (\text{where } g_{m1} = g_{m1} = g_{m2})$$

$$R_{II} = \left(g_{m12} r_{ds12} r_{ds10}\right) \| \left[g_{m14} r_{ds14} \left(r_{ds2} \| r_{ds16}\right)\right] \ (r_{out} \text{ of the p-channel folded-cascode})$$

$$k = \frac{R_{12}\left(g_{ds2} + g_{ds16}\right)}{g_{m14} r_{ds14}} \text{ and } R_{12} = g_{m12} r_{ds12} r_{ds10}$$

Region II (n and p-channel Differential Input Pairs)

$$\therefore A_{vn} \approx \frac{v_{out}}{v_{in}} = \left(\frac{2+k_N}{2+2k_N}\right) g_{mN} R_N + \left(\frac{2+k_P}{2+2k_P}\right) g_{mP} R_P$$

(where $g_{mN} = g_{m5} = g_{m6}$, $g_{mP} = g_{m1} = g_{m2}$)

$$R_N = \left(g_{m14} r_{ds14} r_{ds16}\right) \| \left[g_{m12} r_{ds12} \left(r_{ds6} \| r_{ds10}\right)\right], \ k_N = \frac{R_{14}\left(g_{ds6} + g_{ds10}\right)}{g_{m12} r_{ds12}}, R_{14} = g_{m14} r_{ds14} r_{ds16}$$

$$R_P = \left(g_{m12} r_{ds12} r_{ds10}\right) \| \left[g_{m14} r_{ds14} \left(r_{ds2} \| r_{ds16}\right)\right], \ k_P = \frac{R_{12}\left(g_{ds2} + g_{ds16}\right)}{g_{m14} r_{ds14}}, R_{12} = g_{m12} r_{ds12} r_{ds10}$$

NMOS Source Follower

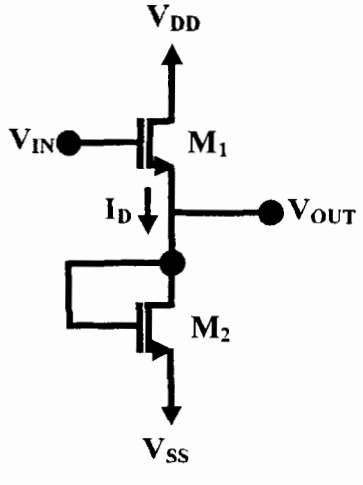

Figure 37 NMOS Source Follower with MOS Connected Diode

The CFC output stage for LNA-1 is an NMOS source follower with an NMOS connected diode as shown in Figure 37. The small signal model for the source follower is presented in Figures 38 and 39.

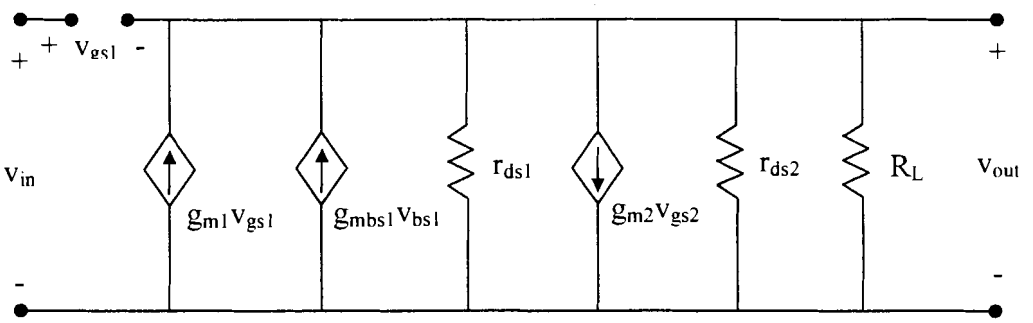

Figure 38 NMOS Source Follower with MOS Diode Load

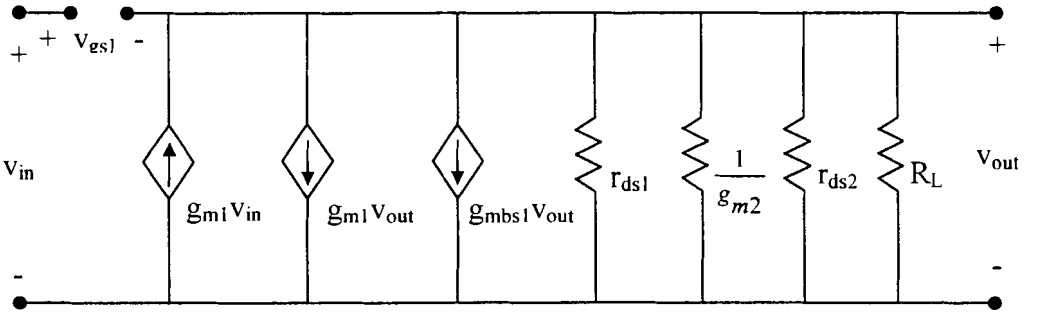

Figure 39 Simplified Small Signal Model of the NMOS Source Follower

A nodal equation at the positive output voltage rail of Figure 38 gives the following expression for the voltage gain, $A_v \approx \dfrac{g_{m1}}{g_{m1} + g_{mbs1} + g_{m2} + G_L}$. The remaining characteristics for the circuit are provided below:

$$v_{OUT}(\max) \approx V_{DD} - V_{T1},\ v_{OUT}(\min) \approx V_{SS}$$

$$R_{OUT} \approx \frac{1}{g_{m1} + g_{mbs1} + g_{m2} + g_{ds1} + g_{ds2}}.$$

8.2.2 Two-Stage Amplifier

Differential PMOS Input Stage

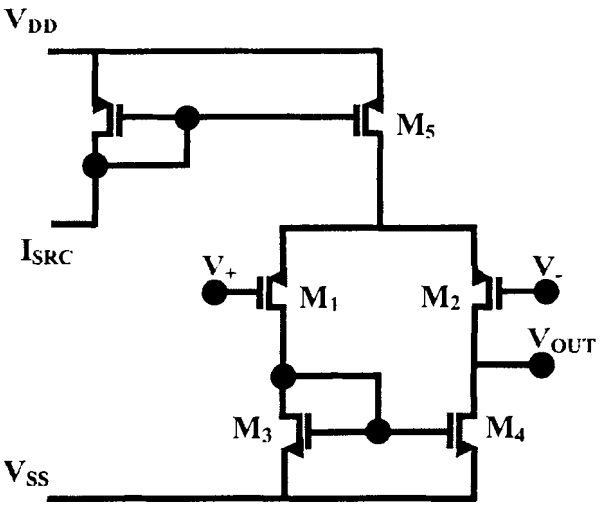

Figure 40 PMOS Input Differential Stage

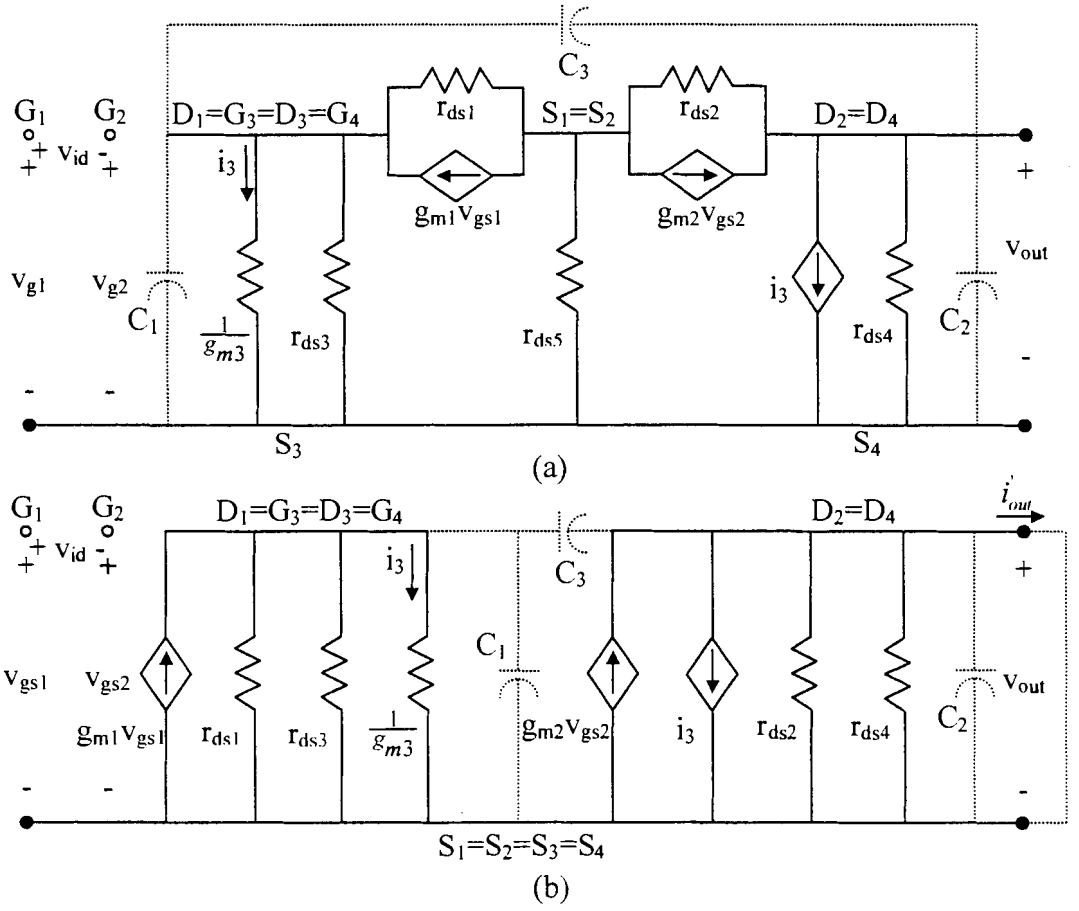

Figure 41 Small Signal Model for the Input Differential Pair

The composition of the input stage is presented in Figure 40. The small signal models for the input stage are shown in Figure 41. The sources of M_1 and M_2 can be

considered to be at ac ground, assuming both sides of the amplifier are perfectly matched simplifying Figure 41 (a) to Figure 41 (b). With the output shorted to ac ground, the current at the output can be expressed as,

$$i_{out} = \frac{g_{m1}g_{m3}(r_{ds1} \| r_{ds3})}{1 + g_{m3}(r_{ds1} \| r_{ds3})} v_{gs1} - g_{m2}v_{gs2} \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}v_{id} \text{ where } g_{m1} = g_{m2} = g_{md}.$$

The voltage gain can then be expressed as the product of g_{md} and R_{out}, where $R_{OUT} = \frac{2}{(\lambda_N + \lambda_P)I_5}$, giving $A_v \approx g_{m1}R_{OUT}$. The other characteristics of the input differential stage are provided below:

$$w_{-3dB} \approx \frac{1}{R_{OUT}C_L}$$

$$v_{ic(\max)} = V_{DD} - V_{SD5(sat)} - V_{SG1} = V_{DD} - V_{SD5(sat)} - V_{SG2}, \; v_{ic(\min)} = V_{SG3} - V_{TP1}$$

$$SR = \frac{I_5}{C_L}, \; P_{diss} = (V_{DD} + |V_{SS}|)(I_5) = (V_{DD} + |V_{SS}|)(I_3 + I_4).$$

Cascode inverters are known to have an advantage over inverting amplifiers. They provide a higher output impedance and reduce the effect of Miller capacitance on the input amplifier, providing a larger gain with improved frequency performance. For this reason, LNA-5 employed PMOS cascode devices in the differential input stage between the PMOS input and NMOS load pairs in order to obtain the same performance improvement.

Current-Source Inverter

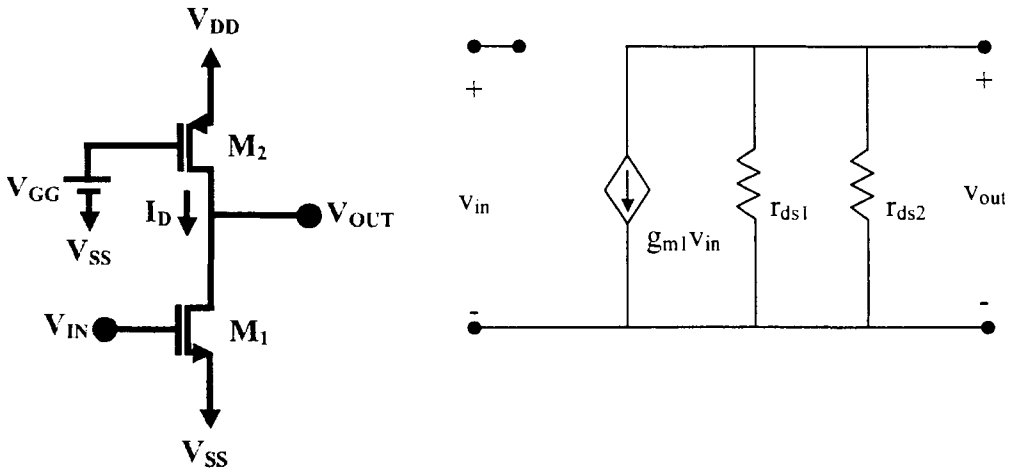

Figure 42 Current-Source Inverter Circuit and Small Signal Model

The circuit and small signal model of the current-source inverter is provided in Figure 42. Small signal analysis produces the following expressions, including the voltage gain for the circuit.

$$A_v \approx \frac{-g_{m1}}{g_{ds1}+g_{ds2}} = \left(\frac{2K_N' W_1}{L_1 I_D}\right)^{\frac{1}{2}}\left(\frac{-1}{\lambda_1+\lambda_2}\right) \propto \frac{1}{\sqrt{I_D}},\quad R_{OUT} \approx \frac{1}{I_D(\lambda_1+\lambda_2)}$$

$$v_{OUT(\max)} \approx V_{DD},\ v_{OUT(\min)} \approx (V_{DD}-V_{T1})\left\{1-\left[1-\left(\frac{\beta}{\beta_1}\right)\left(\frac{V_{SG2}-|V_{T2}|}{V_{DD}-V_{T1}}\right)^2\right]\right\}^{\frac{1}{2}}$$

PMOS Source Follower

The voltage gain and output resistance expressions for the PMOS source follower are identical to the NMOS source follower for the CFC.

$$A_v \approx \frac{g_{m1}}{g_{m1}+g_{mbs1}+g_{m2}+G_L},\quad R_{OUT} \approx \frac{1}{g_{m1}+g_{mbs1}+g_{m2}+g_{ds1}+g_{ds2}}$$

$$v_{OUT}(\max) \approx V_{DD},\quad v_{OUT}(\min) \approx V_{T1}$$

8.3 Appendix III: LNA Design Calculations

Design values were calculated as a guideline to determine the aspect ratios for the transistors, to ensure that the slew rate would be reached, and to obtain initial performance estimates. Model parameters for 0.8 μm CMOS technology obtained from Table 3.1-2 of Allan and Holberg [10], and equations obtained from the small signal AC analysis of the LNA structures in Appendix II, were used for the calculations. Design values were later altered during simulation to optimize for gain, noise, and stability. A slew rate of 100 V/ μs and a capacitive load of 1 pF was intended as a conservative target for each op amp in order to obtain the desired minimum requirement of 10 V/μs and 2 pF, respectively.

8.3.1 CFC

Preliminary design calculations for the CFC low-noise amplifiers were obtained following a similar design approach as the folded-cascode op amp described in Table 6.5-3 of Allan and Holberg [10].

Slew Rate

$I_7 = SR \cdot C_L$ = (100 V/μs)(1 pF) = 100 μA. Similarly, I_3 = 100μA.

Therefore, the bias currents and independent current source is thus determined to be 100 μA.

Bias Currents

$I_9 = I_{10}$ = 1.2 I_3 to 1.5 I_3 (To avoid zero current in the cascodes).

Hence, the target currents for the cascode branches are,

$I_9 = I_{10}$ = 1.25 (100 μA) = 125 μA.

Max. Output Voltage

$$\left(\frac{W}{L}\right)_{10} = \frac{2I_{10}}{K_P' V_{SD10}^2}, \left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10}, \left(\frac{W}{L}\right)_{12} = \frac{2I_{12}}{K_P' V_{SD12}^2}, \left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{12}.$$

$$V_{SD10(sat)} = V_{SD12(sat)} = \frac{V_{DD} - V_{OUT(\min)}}{2} = \frac{3.3 - 2.8}{2} = 0.25 \text{ V}$$

Therefore, the aspect ratios are,

$$\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{12} = \frac{2(125\mu A)}{(50\mu A/V^2)(0.25V)^2} = 80.$$

Note $V_{out(max)}$ was chosen conservatively for purposes of the calculation to be 2.8 V.

Min. Output Voltage

$$\left(\frac{W}{L}\right)_{14} = \frac{2I_{14}}{K_N' V_{DS14}^2}, \left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}, \left(\frac{W}{L}\right)_{16} = \frac{2I_{16}}{K_N' V_{DS16}^2}, \left(\frac{W}{L}\right)_{15} = \left(\frac{W}{L}\right)_{16}.$$

$$V_{DS14(sat)} = V_{DS16(sat)} = \frac{V_{OUT(\min)} - |V_{SS}|}{2} = \frac{0.5 - 0}{2} = 0.25 \text{ V}$$

Therefore, the aspect ratios are,

$$\left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14} = \left(\frac{W}{L}\right)_{15} = \left(\frac{W}{L}\right)_{16} = \frac{2(125\mu A)}{(110\mu A/V^2)(0.25V)^2} \approx 36.$$

Note $V_{out(min)}$ was chosen conservatively for purposes of the calculation to be 0.5 V.

NMOS Input Pair

$GB = \frac{g_{m5}}{C_L}$. Given the target of GB = 100 MHz, the aspect ratios for the NMOS input pair are,

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \frac{g_{m5}^2}{K_N' I_7} = \frac{GB^2 \cdot C_L^2}{K_N' I_7} = \frac{[(2\pi)(100MHz)]^2 (1pF)^2}{(110\mu A/V^2)(100\mu A)} \approx 36.$$

Min. Input CM (NMOS)

$$\left(\frac{W}{L}\right)_7 = \frac{2I_7}{K_N'\left[V_{in(min)} - V_{SS} - \sqrt{\frac{I_7}{K_N'\left(\frac{W}{L}\right)_5}} - V_{T1}\right]^2}$$

$$= \frac{2(100\mu A)}{(110\mu A/V^2)\left[0.5 - 0 - \sqrt{\frac{100\mu A}{(110\mu A/V^2)(36)}} - 0.7\right]^2} \approx 15$$

Note $V_{in(min)}$ was chosen conservatively for purposes of the calculation to be 0.5 V.

Max. Input CM (NMOS)

$$\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10} = \frac{2I_9}{K_P'(V_{DD} - V_{in(max)} + V_{T1})^2}$$

$$= \frac{2(125\mu A)}{(50\mu A/V^2)(3.3 - 2.8 + 0.7)^2} \approx 4$$

Therefore, $\left(\frac{W}{L}\right)_9$ and $\left(\frac{W}{L}\right)_{10}$ are large enough to satisfy the maximum input common-mode voltage for the NMOS input pair. Note $V_{in(max)}$ was chosen conservatively for purposes of the calculation to be 2.8 V.

Power Dissipation

$P = (V_{DD}-V_{SS})(I_7+I_{15}+I_{16}) = (3.3V)(100\mu A+125\mu A+125\mu A) = 1.2$ mW.

The estimated power for the circuit is 1.2 mW with the above design currents and power supply.

PMOS Input Pair

$GB = \frac{g_{m5}}{C_L}$. Given the target of GB = 100 MHz, the aspect ratios for the PMOS input pair are,

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}^2}{K_P' I_3} = \frac{GB^2 \cdot C_L^2}{K_P' I_3} = \frac{[(2\pi)(100MHz)]^2 (1pF)^2}{(50\mu A/V^2)(100\mu A)} \approx 80.$$

Min. Input CM (PMOS)

$$\left(\frac{W}{L}\right)_3 = \frac{2I_3}{K_P'\left[V_{in(min)} - V_{SS} - \sqrt{\frac{I_3}{K_P' S_1}} - V_{T1}\right]^2}$$

$$= \frac{2(100\mu A)}{(50\mu A/V^2)\left[0.5 - 0 - \sqrt{\frac{100\mu A}{(110\mu A/V^2)(80)}} - 0.7\right]^2} \approx 44$$

Note $V_{in(min)}$ was chosen conservatively for purposes of the calculation to be 0.5 V.

Max. Input CM (PMOS)

$$\left(\frac{W}{L}\right)_{15} = \left(\frac{W}{L}\right)_{16} = \frac{2I_{10}}{K_N'(V_{DD} - V_{in(max)} + V_{T1})^2}$$

$$= \frac{2(125\mu A)}{(110\mu A/V^2)(3.3 - 2.8 + 0.7)^2} \approx 2$$

Therefore, $\left(\frac{W}{L}\right)_{15}$ and $\left(\frac{W}{L}\right)_{16}$ are large enough to satisfy the maximum input common-mode voltage for the PMOS input pair. Note $V_{in(max)}$ was chosen conservatively for purposes of the calculation to be 2.8 V.

The gain and frequency for the operating regions were approximated. The values were determined using the small-signal model parameter equations of Table 3.3-1, the 0.8 μm CMOS technology parameters from Table 3.1-2, and the folded-cascode equations from Section 6.5 obtained from Allan and Holberg, as was verified in the CFC small signal ac analysis section [10].

$$g_m = \sqrt{2K' I_D \frac{W}{L}},\ g_{ds} = \lambda I_D$$

$\left(\frac{W}{L}\right)_9, \left(\frac{W}{L}\right)_{10}, \left(\frac{W}{L}\right)_{11}$, and $\left(\frac{W}{L}\right)_{12}$; $g_m = \sqrt{2(50\mu A/V^2)(125\mu A)(80)} = 1.00$ mA/V

$g_{ds} = (0.05V^{-1})(125\mu A) = 6.25$ μA/V

$\left(\frac{W}{L}\right)_{13}, \left(\frac{W}{L}\right)_{14}, \left(\frac{W}{L}\right)_{15}$, and $\left(\frac{W}{L}\right)_{16}$; $g_m = \sqrt{2(110\mu A/V^2)(125\mu A/)(36)} = 0.995$ mA/V

$g_{ds} = (0.04V^{-1})(125\mu A) = 5.00$ μA/V

$\left(\frac{W}{L}\right)_5$ and $\left(\frac{W}{L}\right)_6$; $g_m = \sqrt{2(110\mu A/V^2)(50\mu A)(36)} = 0.629$ mA/V

$g_{ds} = (0.04V^{-1})(50\mu A) = 2.00$ μA/V

$\left(\frac{W}{L}\right)_1$ and $\left(\frac{W}{L}\right)_2$; $g_m = \sqrt{2(50\mu A/V^2)(50\mu A)(80)} = 0.632$ mA/V

$g_{ds} = (0.05V^{-1})(50\mu A) = 2.50$ μA/V

NMOS Active (Region III)

$$R_{14} \approx g_{m14} r_{ds14} r_{ds16} = (0.995mA/V)\left(\frac{1}{5.00\mu A/V}\right)\left(\frac{1}{5.00\mu A/V}\right) = 39.8\ \text{MΩ}$$

$$R_{II} \approx g_{m14} r_{ds14} r_{ds16} \| \left[g_{m12} r_{ds12} \left(r_{ds6} \| r_{ds10} \right) \right]$$

$$= (39.8M\Omega) \| \left[(1.00mA/V) \left(\frac{1}{6.25\mu A/V} \right) \left(\frac{1}{2.00\mu A/V} \| \frac{1}{6.25\mu A/V} \right) \right] = 13.0 \text{ M}\Omega$$

$$k = R_{14} \frac{(g_{ds6} + g_{ds10})}{g_{m12} r_{ds12}} = (39.8M\Omega) \frac{(2.00\mu A/V + 6.25\mu A/V)}{(1.00mA/V) \left(\frac{1}{6.25\mu A/V} \right)} = 2.05$$

$g_{ml} = g_{m5} = 0.629$ mA/V

Voltage Gain

$$\therefore A_{vn} = \frac{v_{out}}{v_{in}} = \left(\frac{2+k}{2+2k} \right) g_{ml} R_{II} = \left(\frac{2+2.05}{2+2(2.05)} \right) (0.629mA/V)(13.0M\Omega) \approx 5440 \text{ V/V}$$

Frequency Response

$$\therefore |p_{out}| = \frac{1}{R_{II} C_{out}} = \frac{1}{(13.0M\Omega)(1pF)} \approx 76.7 \text{ KHz}$$

PMOS Active (Region I)

$$R_{12} \approx g_{m12} r_{ds12} r_{ds10} = (1.00mA/V) \left(\frac{1}{6.25\mu A/V} \right) \left(\frac{1}{6.25\mu A/V} \right) = 25.6 \text{ M}\Omega$$

$$R_{II} \approx g_{m12} r_{ds12} r_{ds10} \| \left[g_{m14} r_{ds14} \left(r_{ds2} \| r_{ds16} \right) \right]$$

$$= (25.6M\Omega) \| \left[(0.995mA/V) \left(\frac{1}{5.00\mu A/V} \right) \left(\frac{1}{2.50\mu A/V} \| \frac{1}{5.00\mu A/V} \right) \right] = 13.0 \text{ M}\Omega$$

$$k = R_{12} \frac{(g_{ds2} + g_{ds16})}{g_{m14} r_{ds14}} = (25.6M\Omega) \frac{(2.50\mu A/V + 5.00\mu A/V)}{(0.995mA/V) \left(\frac{1}{5.00\mu A/V} \right)} = 0.965$$

$g_{ml} = g_{m1} = 0.632$ mA/V

Voltage Gain

$$\therefore A_{vn} = \frac{v_{out}}{v_{in}} = \left(\frac{2+k}{2+2k} \right) g_{ml} R_{II} = \left(\frac{2+0.965}{2+2(0.965)} \right) (0.632mA/V)(13.0M\Omega) \approx 6210 \text{ V/V}$$

Frequency Response

$$\therefore |p_{out}| = \frac{1}{R_{II} C_{out}} = \frac{1}{(13.0M\Omega)(1pF)} = 76.7\ \text{KHz}$$

NMOS and PMOS Active (Region II)

$$\therefore A_{vn} \approx \frac{v_{out}}{v_{in}} = \left(\frac{2 + k_N}{2 + 2k_N}\right) g_{mN} R_N + \left(\frac{2 + k_P}{2 + 2k_P}\right) g_{mP} R_P \approx 11{,}600\ \text{V/V}$$

Output Stage

$v_{OUT}(\max) \approx V_{DD} - V_{T1} = 3.3 - 0.7 = 2.6\,\text{V}$, $v_{OUT}(\min) \approx V_{SS} = 0$

Sensible ratios for the transistors and an estimated current of 200 μA in the source follower give,

$\left(\frac{W}{L}\right)_1 = 100$ and $\left(\frac{W}{L}\right)_2 = 10$.

$$\left(\frac{W}{L}\right)_1 ; g_m = \sqrt{2(110\mu A/V^2)(200\mu A)(100)} = 2.10\ \text{mA/V}$$

$$g_{ds} = (0.04V^{-1})(200\mu A) = 8.00\ \mu\text{A/V}$$

$$\left(\frac{W}{L}\right)_2 ; g_m = \sqrt{2(110\mu A/V^2)(200\mu A)(10)} = 0.663\ \text{mA/V}$$

$$g_{ds} = (0.04V^{-1})(200\mu A) = 8.00\ \mu\text{A/V}$$

$$R_{OUT} \approx \frac{1}{g_{m1} + g_{mbs1} + g_{m2} + g_{ds1} + g_{ds2}} \approx \frac{1}{g_{m1} + g_{m2} + g_{ds1} + g_{ds2}}$$

$$= \frac{1}{2.10mA/V + 0.663mA/V + 8.00\mu A/V + 8.00\mu A/V} \approx 360\Omega$$

$$A_v \approx \frac{g_{m1}}{g_{m1} + g_{mbs1} + g_{m2} + G_L} \approx \frac{g_{m1}}{g_{m1} + g_{m2}} = \frac{2.10mA/V}{2.10mA/V + 0.663mA/V} \cong 0.760$$

Therefore, the output voltage gain at 1.65 V input bias is estimated to be 78.9 dB from the design calculations. The device geometry changed during simulation of the design to achieve the desired gain, noise, and stability performance figures required of the medical imaging application. Compromises in gain and slew rate were needed to attain the necessary low noise and stability design attributes.

8.3.2 Two-Stage Amplifier

Preliminary design calculations were obtained targeting a slew rate of 100 V/μs, a ω_{-3dB} of 500 KHz, and 1 mW of power with an estimated capacitive load of 1 pF and a gain of 250. The methodology for designing the two-stage amplifier utilizes the design procedures and equations for a differential amplifier in Table 5.2-1 and the two-stage amplifier in Table 6.3-1, as well as the current-source inverter, obtained from Allan and Holberg [10].

Slew Rate

$I_5 = SR \cdot C_L$ = (100 V/μs)(1 pF) = 100 μA and hence $I_5 \geq 100$ μA.

Power Dissipation

P = (V_{DD}+|V_{SS}|)(I_5). 1 mW = (3.3 V + 0)(I_5) and hence $I_5 \leq 303$ μA.

Therefore, the bias current and independent current source is chosen to be 200 μA, which is the approximate average of the currents calculated from the above slew rate and power constraints.

Frequency Response

$\omega_{-3dB} = \frac{1}{R_{OUT}C_L}$. Hence, $2\pi(500KHz) = \frac{1}{R_{OUT}(1pF)}$, giving

$R_{OUT} = 318\ K\Omega$. $R_{OUT} = \frac{2}{(\lambda_N + \lambda_P)I_5}$. Hence, $318K\Omega = \frac{2}{(0.01 + 0.05)I_5}$,

indicating $I_5 \geq 105\ \mu A$. Therefore, the bias current and independent current source of 200 μA will satisfy the frequency response requirement.

Voltage Gain of Input Differential Stage

$$A_v = g_{m1}R_{OUT} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{\sqrt{2K_P' I_D \left(\frac{W}{L}\right)_1}}{(\lambda_P + \lambda_N)I_D}$$

$$250 = \frac{\sqrt{2(50\mu A/V^2)(100\mu A)\left(\frac{W}{L}\right)_1}}{(0.05 + 0.01)(100\mu A)}$$

$$\therefore \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 225$$

Max. Input CM (PMOS)

$$v_{ic(\max)} = V_{DD} - V_{SD5(sat)} - V_{SG1} \quad \text{and} \quad |V_{SD1}| = |V_{SG1}| - |V_{T1}|$$

$$2.8 = 3.3 - \sqrt{\frac{2(200\mu A)}{(50\mu A/V^2)\left(\frac{W}{L}\right)_5}} - \left(\sqrt{\frac{2(100\mu A)}{(50\mu A/V^2)\left(\frac{W}{L}\right)_1}} - 0.7\right)$$

$$\therefore \left(\frac{W}{L}\right)_5 = 7.03 \approx 8$$

Note $V_{in(max)}$ was chosen conservatively for purposes of the calculation to be 2.8 V.

Min. Input CM (PMOS)

$$v_{ic(\min)} = V_{SG3} - V_{TP1}$$

$$0.5 = \sqrt{\frac{2(100\mu A)}{(110\mu A/V^2)\left(\frac{W}{L}\right)_3}} - 0.7\ ,\ \therefore \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 1.26 \approx 2$$

Note $V_{in(min)}$ was chosen conservatively for purposes of the calculation to be 0.5 V.

Inverter Stage

For the inverter stage, g_{m6} and g_{m7} refer to g_{m1} and g_{m2}, respectively, in the current-source inverter of Figure 42.

$$C_C = (0.22)C_L = 0.22(1pF) = 0.22pF \approx 0.2pF$$

$$g_{m6} = 2.2g_{m4}\left(\frac{C_L}{C_C}\right) = 2.2\sqrt{2K_N' I_D\left(\frac{W}{L}\right)_4}\left(\frac{C_L}{C_C}\right)$$

$$= 2.2\sqrt{2(110\mu A/V^2)(100\mu A)(2)}\left(\frac{1pF}{0.2pF}\right) = 2.31mA/V$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4\left(\frac{g_{m6}}{g_{m4}}\right) = 2\left(\frac{2.307mA/V}{\sqrt{2(110\mu A/V^2)(100\mu A)(2)}}\right) = 22.0 \approx 22$$

$$I_6 = \frac{g_{m6}^2}{2K_6'\left(\frac{W}{L}\right)_6} = \frac{(2.307mA/V)^2}{2(110\mu A/V^2)(22)} = 1.10mA$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5}\left(\frac{W}{L}\right)_5 = \frac{1.100mA}{200\mu A}(8) = 44$$

In order to place the null zero on top of the second pole,

$$R_Z = \frac{1}{g_{m6}}\left(\frac{C_L + C_C}{C_C}\right) = \left(\frac{C_C + C_L}{C_C}\right)\frac{1}{\sqrt{2K_N'\left(\frac{W}{L}\right)_6 I_6}}$$

$$= \left(\frac{0.2+1}{0.2}\right)\frac{1}{2.31mA/V} \approx 2600\,\Omega$$

$$g_{ds6} = (0.04V^{-1})(1.10mA) = 44.0\ \mu A/V$$

$$g_{ds7} = (0.05V^{-1})(1.10mA) = 55.0\ \mu A/V$$

$$A_v \approx \frac{-g_{m6}}{g_{ds6}+g_{ds7}} = \frac{-2.31mA/V}{44\mu A/V + 55\mu A/V} \approx -23.3\ V/V$$

Output Stage

$v_{OUT}(\max) \approx V_{DD} = 3.3\,V,\ v_{OUT}(\min) \approx V_{T1} = 0.7\,V$

Sensible ratios for the transistors and an estimated current of 200 μA in the source follower would be,

$$\left(\frac{W}{L}\right)_1 = 100 \text{ and } \left(\frac{W}{L}\right)_2 = 10.$$

S_1; $\quad g_m = \sqrt{2(50\mu A/V^2)(200\mu A)(100)} = 1.41\ mA/V$

$$g_{ds} = (0.05V^{-1})(200\mu A) = 10.0\ \mu A/V$$

S_2; $\quad g_m = \sqrt{2(50\mu A/V^2)(200\mu A)(10)} = 0.447\ mA/V$

$$g_{ds} = (0.05V^{-1})(200\mu A) = 10.0\ \mu A/V$$

$$R_{OUT} \approx \frac{1}{g_{m1}+g_{mbs1}+g_{m2}+g_{ds1}+g_{ds2}} \approx \frac{1}{g_{m1}+g_{m2}+g_{ds1}+g_{ds2}}$$

$$= \frac{1}{1.41mA/V + 0.447mA/V + 10.0\mu A/V + 10.0\mu A/V} \approx 532\Omega$$

$$A_v \approx \frac{g_{m1}}{g_{m1}+g_{mbs1}+g_{m2}+G_L} \approx \frac{g_{m1}}{g_{m1}+g_{m2}} = \frac{1.41mA/V}{1.41mA/V + 0.447mA/V} = 0.760\ V/V$$

Therefore, the output voltage gain at 1.65 V input bias is estimated to be 72.9 dB from the design calculations. The device geometry for the two-stage amplifier was also changed during simulation of the design to optimize for gain, noise, and stability performance figures required in the medical imaging application. Compromises in gain and slew rate were needed to attain the necessary low noise and stability design attributes.

8.3.3 Voltage Buffer

The voltage buffer for structure ***C*** of the medical imaging solution is the same architecture as the output stage for a two-stage amplifier with equivalent preliminary design calculations.

8.4 Appendix IV: LNA Design Geometry

Table 9 CFC Design Geometry for LNA-1

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M1	PMOS	30	5	1
M2	PMOS	30	5	1
M3	PMOS	10	4	2
M4	PMOS	10	4	2
M5	NMOS	5	5	1
M6	NMOS	5	5	1
M7	NMOS	3	4	2
M8	NMOS	3	4	2
M9	PMOS	850	5	1
M10	PMOS	850	5	1
M11	PMOS	850	5	1
M12	PMOS	850	5	1
M13	NMOS	500	4	2
M14	NMOS	500	4	2
M15	NMOS	500	4	2
M16	NMOS	500	4	2
M17	NMOS	20	5	1
M18	NMOS	3	5	1

Table 10 Design Geometry for LNA-2

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M0	PMOS	10	4	1
M1	PMOS	10	4	1
M2	PMOS	14	5	1
M3	PMOS	14	5	1
M4	NMOS	8	4	2
M5	NMOS	8	4	2
M6	NMOS	65	5	1
M7	PMOS	80	5	1
M8	PMOS	20	5	1
M9	PMOS	4	5	1

Passive Device	Value
C0	1 pF
R1	1 KΩ

Table 11 CFC Device Geometry for LNA-3

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M1	PMOS	14	5	1
M2	PMOS	14	5	1
M3	PMOS	10	4	2
M4	PMOS	10	4	2
M5	NMOS	2	5	1
M6	NMOS	2	5	1
M7	NMOS	2	4	2
M8	NMOS	2	4	2
M9	PMOS	160	5	1
M10	PMOS	160	5	1
M11	PMOS	160	5	1
M12	PMOS	160	5	1
M13	NMOS	80	4	1
M14	NMOS	80	4	1
M15	NMOS	80	4	1
M16	NMOS	80	4	1
M17	PMOS	3	5	1
M18	PMOS	40	5	1

Table 12 Device Geometry for LNA-4

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M0	PMOS	10	5	1
M1	PMOS	10	5	1
M2	PMOS	30	5	1
M3	PMOS	30	5	1
M4	NMOS	8	4	2
M5	NMOS	8	4	2
M6	NMOS	65	5	1
M7	PMOS	80	5	1
M8	PMOS	20	5	1
M9	PMOS	4	5	1

Passive Device	Value
C0	0.9 pF
R1	2 KΩ

Table 13 Design Geometry for LNA-5

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M0	PMOS	8	4	1
M1	PMOS	8	4	1
M2	PMOS	10	4	1
M3	PMOS	10	4	1
M4	NMOS	4	4	2
M5	NMOS	4	4	2
M6	NMOS	32	5	1
M7	PMOS	104	5	2
M8	PMOS	20	5	1
M9	PMOS	4	5	1
M10	PMOS	8	4	1

Passive Device	Value
C0	0.6 pF
R1	3 KΩ

Table 14 Design Geometry for LNA-6

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M0	PMOS	10	5	1
M1	PMOS	10	5	1
M2	PMOS	30	5	1
M3	PMOS	30	5	1
M4	NMOS	8	4	2
M5	NMOS	8	4	2
M6	NMOS	65	5	1
M7	PMOS	80	5	1
M8	PMOS	80	5	1
M9	PMOS	1	5	1

Passive Device	Value
C0	1 pF
R1	3 KΩ

Table 15 Device Geometry for Structure *C* of Medical Imaging Solution I

Transistor	Type	Multiplier	Width (μm)	Length (μm)
M0	PMOS	30	5	1
M1	PMOS	1	5	1

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