CMOS ACTIVE PIXEL SENSOR DESIGNS FOR FAULT TOLERANCE AND BACKGROUND ILLUMINATION SUBTRACTION

by

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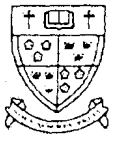

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ABSTRACT

As the CMOS active pixel sensor evolves, its weaknesses are being overcome and its strengths start to surpass that of the charge-coupled device. This thesis discusses two novel APS designs. The first novel APS design was a Fault Tolerance Active Pixel Sensor (FTAPS) to increase a pixel's tolerance to defects. By dividing a regular APS pixel into two halves, the reliability of the pixel is increased, resulting in higher fabrication yield, longer pixel life time, and reduction in cost. Photodiode-based FTAPS pixels were designed, fabricated in CMOS 0.18 micron technology, and tested. Experimental results demonstrated that the reliability of the pixel is increased and information that would have been lost without fault tolerance is recovered.

The second novel APS pixel was designed to eliminate background illumination when a detector attempts to locate a desired laser signal. This pixel design, namely the Duo-output APS (DAPS), consists of an extra output path, such that a signal can be selectively readout to one of the two paths at different time of a cycle. During one half of a given cycle while the foreground signal is turned on, the sensor detects both the background and foreground levels. During the other half of the cycle, the foreground is off, thus only the background level is detected. The difference of the two outputs is the desired foreground signal without the background noise. DAPS pixels were designed, fabricated in CMOS 0.18 micron technology, and tested. Testing results identified design changes that will improve the background subtraction.

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GLOSSARY OR LIST OF ABBREVIATIONS AND ACRONYMS

3-T APS	3-Transistor Active Pixel Sensor
4-T APS	4-Transistor Active Pixel Sensor
ADC	Analog-to-Digital Converter
APS	Active Pixel Sensor
CCD	Charge-Coupled Devices
CDS	Correlated Double Sampling
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
CTE	Charge Transfer Efficiency
DAPS	Duo-Output Active Pixel Sensor
DS	Double Sampling
DSLR	Digital Single Lens Reflex
FPN	Fixed Pattern Noise
FTAPS	Fault Tolerance Active Pixel Sensor
JFET	Junction Field Effect Transistor
LED	Light Emitting Diode
LBCAST	Lateral Buried Charge Accumulator and Sensing Transistor array
MIS	Metal-Insulator-Semiconductor
MOS	Metal-Oxide-Semiconductor
PDA	Personal Digital Assistant
PG	Photogate
PRNU	Photo Response Non-Uniformity
RPO	Resist Protection Oxide
SH	Stuck High
SL	Stuck Low
SLR	Single Lens Reflex
SOC	System-On-a-Chip
QE	Quantum Efficiency
TX	Transfer Gate

1 CHAPTER ONE – INTRODUCTION

Recent developments of Active Pixel Sensor (APS) have been focused on imaging applications such as handheld digital cameras, cellular phone cameras, video cameras, robotics, and such. These applications drive people to focus their effort to improve the sensor performance such as increasing sensitivity, reducing noise, and increasing resolution. In this thesis, we intend to explore these sensors for much wider applications by introducing new designs and concepts. The target is to modify the design of an APS to enhance fabrication yield or to detect specific signals that are not possible with regular cameras.

1.1 Active Pixel Sensor

CMOS active pixel image sensor, invented by Fossum in 1993 in the Jet Propulsion Laboratory (JPL), consists of a photodiode and three transistors – a reset transistor, a readout transistor, and a row select transistor as shown in Figure 1.

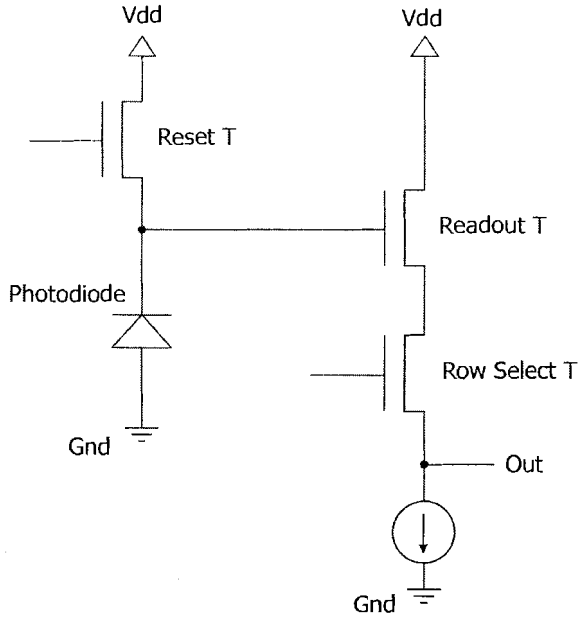


Figure 1 Schematic of an active pixel sensor

The reset transistor initializes the cathode of the photodiode to a known voltage at the beginning of an image capture to bias the device into the most linear range. Afterwards, when light hits the photodiode, photocurrent generated by the photodiode starts to integrate charges at the gate of the readout transistor, and discharging the gate. At the end of the capturing process, the row select transistor is enabled to provide a voltage output, which is dependent on the amount of charge stored at the gate of the readout transistor. This APS is also called the 3-Transistor (3-T) APS for there are 3 transistors in the pixel. In Chapter 2, a review of basic photo-detectors and image sensor will be given and the details of APS including its different varieties and advantages will be discussed in Chapter 3.

1.2 Digital Camera

Digital cameras have increasingly become more popular due to advancement in fabrication technology and microelectronics over the past 10 years. Digital cameras offer many advantages over traditional film cameras. Pictures of higher quality are achieved more easily because many features that are not possible in film cameras are available in digital cameras. For example, even low end point and shoot cameras offer instant reviewing of pictures. Moreover, control over ISO (International Standard Organization), i.e. sensitivity rating in digital cameras, and white balancing are available to digital cameras on a frame by frame basis. In film camera, ISO is either determined by the ISO of the film itself or adjusted by film labs during picture development. White balancing is either controlled by the type of film or corrected by using colour filters. Therefore, both ISO and white balancing controls are not as convenient for traditional film cameras as in digital cameras. Most importantly, the cost of digital photography is much lower because digital films, most of which are simply flash memory cards, are erasable and rewritable and permanent data storage (e.g. CD or DVD) are cheap. Photographs can be printed out selectively after previewing on computers and these can all be performed conveniently and comfortably at home rather than requiring developing and printing in film labs.

The Camera & Imaging Products Association's statistic shows that since the year 2002, the sales of digital cameras worldwide have exceeded the sales of traditional film camera [1]. The following two tables (Table 1 and Table 2) show the units sold and the total values of the shipments for both digital and traditional film cameras from 2001 to 2004.

Table 1 Sale comparison (number of units in million) of digital and traditional film cameras from 2001 to 2003

Camera type \ Year	2001	2002	2003	2004
Digital camera (units)	14.8 (35%)	24.6 (51%)	43.4 (73%)	59.8 (86%)
Film camera (units)	27.6 (65%)	23.7 (49%)	16.3 (27%)	10.1 (14%)

Table 2 Sale comparison (US dollars in billion) of digital and traditional film camera from 2001 to 2003 (Exchange rate: ¥1000 = 9.47238USD on February 6, 2004)

Camera type \ Year	2001	2002	2003	2004
Digital camera (US$)	5.17 (70%)	7.56 (80%)	11.60 (91%)	14.6 (97%)
Film camera (US$)	2.27 (30%)	1.89 (20%)	1.12 (9%)	0.52 (3%)

The number of units sold and total values of these shipments increased continually from 2001 to 2004 for the digital camera market. In contrast, both numbers for traditional film cameras show an ever more rapid decline from 2001 to 2003. In 2004, sales of digital camera reached 59.8 million pieces (up 37.7% from 2003) and this figure represents 86% of all camera units sold. In monetary figures, digital camera represents 14.6 billion US dollars of sales, which is equal to 97% of the entire camera market. Forecast suggests that in 2005 only 6.4 million pieces of traditional film camera will be sold while there will be 72.2 million digital cameras sold [1].

In recent years, APS has become a popular contender for taking over the digital imagery market by eliminating high power demands and reducing cost of production, both of which are not possible for CCD. As its name suggests, CMOS APS is CMOS compatible, where CCD is not, thus allowing circuitry to be built around the sensor on the same silicon substrate to create an

entire system, i.e. System-On-a-Chip (SOC). In the past several years, digital camera has also been incorporated into many handheld applications such as Personal Digital Assistants (PDAs), cellular phones, and MP3 players. Resolution of these miniaturized cameras is also approaching the lower end consumer digital camera. Two-mega pixel camera in cellular phone has been reported [2].

Among all digital cameras, most of the simple point and shoot types use Charge-Coupled Device (CCD) as the photo-detecting sensor. For advanced Single-Lens-Reflex (SLR) type digital cameras which are the top end of the market, however, both the CCD and the APS are used. Some predicted that APS can replace CCD only in the lower end digital camera as APS cannot compete with CCD in terms of performance [3]. However, as of 2005, a rather peculiar trend is observed from a survey on www.dpreview.com (a major digital camera review website) done by the author that APS is dominating the lowest end digital cameras and becoming dominant in the highest end digital cameras, leaving CCD cameras in the middle of the spectrum. The lowest end refers to digital camera embedded in handheld devices such as cellular phones and PDAs, which usually has resolution lower than one mega pixel. CCD systems remain dominant in the middle range, which is the point-and-shoot type digital camera.

More and more Digital SLRs (DSLRs) that use CMOS sensors are appearing in the market. All Canon and Kodak DSLRs produced in the last three years use CMOS APS. Although most Nikon DSLRs use CCD's, the newest model D2X achieves 12.2 mega pixel with APS and the model D2Hs uses a new technology similar to CMOS, called Junction Field Effect Transistor (JFET) Lateral Buried Charge Accumulator and Sensing Transistor array (LBCAST) [4]. The trend seems to drift away from the CCD technology for the top end SLR-type digital cameras. Although the performance of CCD's is better than APS' in theory, APS is the preferred technology in practice. This trend in APS can be explained as follows. First of all, with larger imagers, power consumption becomes a major drawback of the CCD because as the resolution of

the camera gets higher, the amount of power required for the CCD increases. On the other hand, the APS is famous for its low power consumption. At the same time, APS' ability to be integrated into CMOS systems on a chip makes it less costly for the low end digital cameras. Lastly, CCD imagers require specialized fabrication processes, so going to smaller pixels or larger areas requires increased development costs. APS' by comparison can draw on standard CMOS memory and logic development for smaller size devices.

This thesis investigates ways to expand APS' abilities with two novel designs of APS. First, as the resolution of imager gets larger, pixels become smaller and array sizes become larger; thus defective pixels increase in probability and the yield decreases. The first issue to be discussed is built-in redundancy within an APS pixel to increase the reliability of each pixel and therefore the reliability of the entire imaging array [5]. This built-in redundancy is not feasible in a CCD because of its serial output nature. The second objective of this thesis is to demonstrate a new APS design for novel application in background light elimination. The new APS design greatly improves the performance of the sensory system in such applications and potentially, it can be utilized as a 3-dimensional image sensor or a motion sensor. These two objectives will now be expanded upon.

1.3 Objectives

1.3.1 Sensors and Yield

The active pixel sensor's resolution approaches that of traditional film as the array size keeps increasing and pixel size decreasing. A challenge remains in lowering defects at fabrication time in order to keep yields high to minimize production costs. Moreover the increased pixel density and count causes reduced reliability over the imager's lifetime. This problem is especially important in harsh environments, such as high-radiation conditions in military or outer space, where defective imagers cannot be easily replaced. Although defect

correction by software such as interpolation and averaging from surrounding pixels are used, they are not satisfactory because, under many conditions, they give faulty information.

1.3.2 Fault Tolerant Active Pixel Sensor

Thus the concept of redundancy in APS, a Fault Tolerant APS (FTAPS), was devised by Chapman and Audet in 1999 [5]. The first objective of this thesis is to demonstrate this idea including its design and implementation of test chips, implementation of the testing environment, and experimental results. The FTAPS was simulated in 2001 by Chapman and Audet [6]. This FTAPS incorporates hardware redundancy by splitting a normal APS into two parallel operating halves with very little additional area cost. The desired yield improvement is obtained, as shown from simulations, since the probability that both pixel halves will fail over a long time of operation is low [7]. Pixels with point defect resulting in half optically stuck-low or stuck-high can be recovered by doubling the sensed output, which is a simple left shift of one in the digital domain after the output is digitized.

This thesis work involved the first design, fabrication, and tests of the fault tolerant APS concept. Chapter 3 will present the design and architecture of the fault tolerant APS. The defects that are most likely to occur for an APS will be discussed followed by a brief description of the design of the chip. The characterization of the normal and electrically-induced defective pixels will be presented in Chapter 5 and a comparison of the characterization results using optically induced defects will be made. At the end of the chapter, the testing of a small APS system by projecting images on the array is discussed.

1.3.3 Optical Scanning Detector with Background Light Elimination

The second objective of this thesis is to demonstrate a novel design of APS for optical scanning system used in 3D object profilometry. As an optical scanning system searches for a desired optical signal on an object, background illumination usually reduces the accuracy of the

scanner. This novel APS design filters out the background illumination by introducing an extra output path and by scanning any particular spot twice. Traditional scanning detectors, most of which use CCD, fail to acquire accurate results when the surface of the object is not ideal for sensing such as a dark area, a shiny surface, or a noisy background environment when background light sources such as sun light or indoor room light interfere with the optical source. The signal-to-noise ratio is significantly reduced in these situations. Increasing the optical power will not always resolve the issue in the case when a laser is the optical signal because the laser might be too strong and it alters or damages the object that is being sensed. Industrial standard also limits the power of the laser to "Laser Class 2" [8] in order to meet the safety precautions and to prevent harm to human eyes.

1.3.4 Duo-Output Active Pixel Sensor

A new active pixel sensor design is proposed to increase the detector signal-to-noise ratio in a noisy environment. Moreover, this new APS designs is capable of detecting an optical signal over a non-ideal surface, e.g. a dark defective spot on a flat surface or a shinny spot that reflects extra light. This novel APS design, called the Duo-output APS (DAPS), is a modification of the 4-Transistor (4-T) photodiode APS. An additional transistor is added to the original 3-T APS between the photodiode and the gate of the output transistor acting as a shutter. Moreover, an extra output path along with an extra shutter transistor is also added. Each of the two shutter transistors, enabled at different times within a reset cycle, allows integration on separate nodes. This mechanism permits background light to be individually readout at one node when the optical signal is off and subtracted off from the readout signal at the other node when the optical signal is on. The result is a reduction in background illumination at the output. Chapter 3 will present the current optical scanning technology as well as the design of this new APS pixel. Chapter 6 will present the experimental results for the DAPS using Light Emitting Diode (LED) and argon laser as the major light source. These results will be compared to the HSpice simulation in Chapter 7.

1.4 Overview

In this thesis, Chapter 2 reviews the basics of photo-sensing elements and several important image sensors including the charge coupled device, photodiode, and active pixel sensor. Chapter 3 discusses the design of the APS chip in a bottom-up approach, from the design of various APS pixel cells to the architecture of the whole chip. Chapter 4 presents the test setup for LEDs and for the argon laser. Chapter 5 and 6 present the two main APS designs proposed in this thesis project. The first design involves the use of redundancy within a single pixel to increase the reliability of a pixel and the entire APS array. The second design involves the use of two output nodes within a single pixel and the difference of the two outputs to eliminate the background illumination from a desired optical signal. Chapter 7 presents simulation results using HSpice in order to compare the experimental results obtained in Chapter 6 with simulations.

2 CHAPTER TWO – REVIEW OF PHOTO-DETECTORS AND IMAGE SENSORS

Before the novel active pixel sensors are presented, this chapter reviews the general concept of photo-detection using silicon. Two popular silicon photo-detectors, the charge-couple device and the photodiode, are reviewed. Since CCD's have been the major technology for imaging sensor for the past 10 years, it is important to understand the basics of CCD in order to compare them to the emerging CMOS active pixel sensor. The photodiode, being the photo-sensing component for APS, will also be explained. The last section of this chapter discusses the generic APS' that are already widely used in the market, namely the photodiode-based APS and photogate-based APS. Comparison between these two different APS' is then made. A shutter version of the photodiode based APS, namely the 4-Transistor (4-T) APS follows.

2.1 Silicon Photo-Detector for Visible Light

Semiconductor photo-detector refers to the device used for detection of optical signals of different wavelengths using semiconductor material. It is widely used ranging from application in daily life to scientific research such as industrial measurement, security systems, medical radiology, digital camera systems, space mission, and astronomical equipment. Detection of wavelength within the optical range, as shown in Figure 2, varies from ultraviolet of wavelength longer than 10nm to infrared of wavelength shorter than 1mm, through specific detectors. Although there are detectors for gamma-ray [9] and radio waves, they are not classified within the optical range.

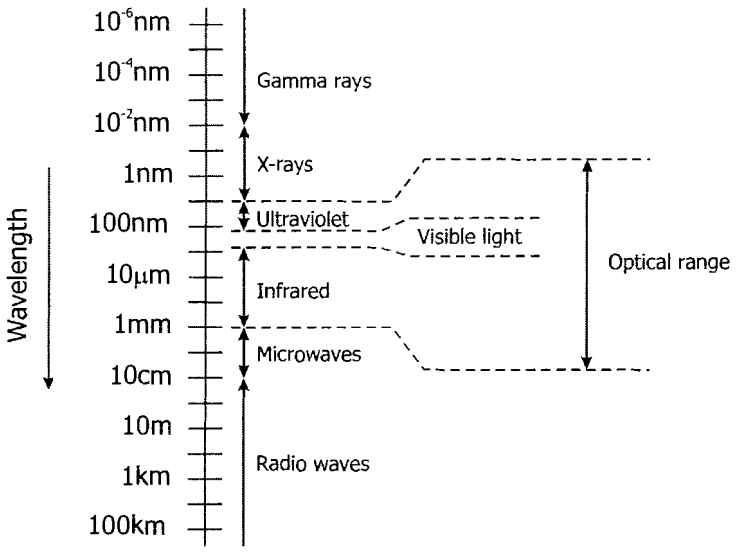


Figure 2 Optical electromagnetic spectrum after Kaufmann [10]

Examples of semiconductors used in photo-detector are Silicon (Si), Cadmium Zinc Telluride (CdZnTe) [9], and Gallium Nitride (GaN) [11]. This thesis concentrates on the basic mechanism of photo-detection using silicon for the visible light spectrum, i.e. from 400nm to 700nm. For each material, different wavelengths of optical signal are absorbed over different penetration depths. Thus different types of detector materials respond to specific spectral ranges.

2.1.1 Absorption of Optical Signal by Silicon

When incident light impinges on a piece of silicon, some portion of the original optical power is reflected due to the index of refraction change at the surface. The remaining light enters the silicon piece and gets absorbed by the material such that the amount of power decays exponentially from the surface. If *P(x)* represents the power of the optical signal at depth x from the surface, *P(0)* is the power level that enter the silicon surface. *P(x)* is related to *P(0)* by the Beer-Lambert law [12]:

$$P(x) = P(0) \cdot e^{-\alpha x} \tag{1}$$

α, of unit m^{-1}, is called the absorption coefficient and is a function of the wavelength of the optical signal. α decreases as wavelength increases but in general α cannot be mathematically computed easily. Scientific measurement of the absorption coefficient is shown in Table 3 [13].

Table 3 Relationship between absorption coefficient and wavelength for silicon based photo-detector

Wavelength (nm)	400	430	480	500	530	590	620	696
Absorption Coefficient (μm^{-1})	8.98	3.51	1.13	0.889	0.681	0.413	0.323	0.167

From equation (1) and Table 3 above, the optical power level at depth x is weaker for a shorter wavelength than for a longer wavelength. A shorter wavelength signal at the blue end of the visible spectrum in fact might be more difficult for a photo-detector to sense depending on the design and architecture of the detector.

2.1.2 Electron-Hole Pair Generation

As mentioned above, energy is absorbed by the silicon when an optical signal enters the material. This energy is in the form of photons and these photons play the major role for photo-detection. By Planck's Law, the photon energy contained in a photon of wavelength λ is:

$$E = \frac{hc}{\lambda} = \frac{1.24\times10^{-6} eV}{\lambda} \tag{2}$$

h is Planck's constant and has a value of 6.626×10^{-34}J·s or 4.136×10^{-15}eV·s, c is speed of light and has a value of 2.998×10^8 m/s. These photons may excite electrons from the valence band to the conduction band, called intrinsic photoexcitation [14]. The amount of electrons excited to the conduction band depends on the energy of photons. The energy band gap, i.e. energy between the valence and conduction bands, is 1.124eV for silicon at room temperature. Any photon with energy greater than this band gap energy might get absorbed by the silicon and is able to excite an electron to the conduction band.

For the red visible light of wavelength 650nm, the energy is 1.91eV or 3.056×10^{-19}Joule. For green (510nm) and blue (475nm), the energies are 2.43eV and 2.610eV respectively. The longest wavelength that provides sufficient energy to excite electrons to the conduction band is 1103nm. Therefore, the entire visible light spectrum has high enough energy to excite electrons in silicon from the valence band to the conduction band.

When a photon from the visible light spectrum excites an electron to the conduction band, one electron-hole pair is generated. The role of a photo detector is to convert the electron-hole pair generated into photocurrent. The effectiveness of generating electron-hole pairs is measured by Quantum Efficiency (QE). Quantum efficiency refers to "the number of electron-hole pairs generated per incident photon" [14] and it can be formulated as [12]:

$$\eta = \frac{J/q}{P_p/h\omega} \tag{3}$$

J represents the optically induced current density, P_p represents the power of the optical signal per unit area and ω is the angular frequency of the incident light. Since only a single electron hold pair is created by each photon, wavelengths shorter than 1.1μm show lower quantum efficiency.

After an electron-hole pair is generated, the electron and hole tend to recombine to restore to equilibrium. This recombination of electron and hole (recombination process) represents an electron falling from the conduction band back to the valence band, resulting in an emission of a photon or transfer of energy to another electron [14]. Figure 3 shows both the generation of electron-hole pair when a photon with enough energy is incident on the silicon and the recombination of electron (e^-) with hole. E_c and E_v represent the conduction and valence bands respectively.

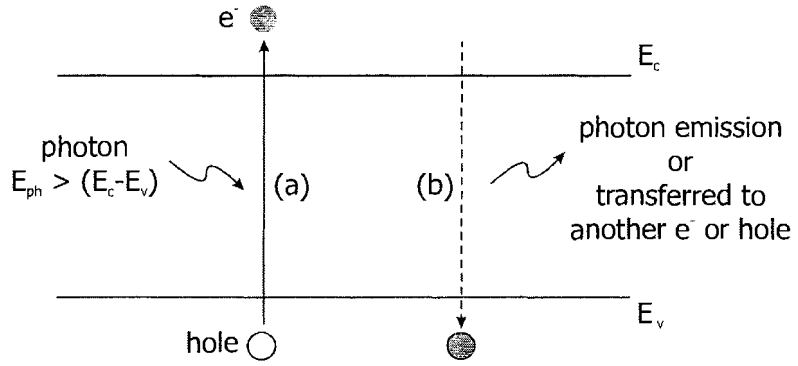


Figure 3 Generation and recombination processes: (a) generation of an electron-hole pair by a photon and (b) recombination of electron and hole emits a photon or transfers energy to another electron or hole

Therefore it is important to collect the photo-generated electron-hole pair before they recombine and it is usually carried out by separating them. The next two sections in charge-couple devices and photodiode will present the way each of them uses to separate the generated pair.

2.1.3 Measurement of Photo-Generated Charges

Now, after the electron and hole are separated apart, how does the photo-detector measure the number of electrons or holes? In most detectors, only the number of electrons will be measured as the number of holes generated should be identical. The unit often used for a measure of visible light is "lux", or lumens per meter square (lm/m^2), and one lux is equal to $1.464\times10^{-3}W/m^2$ at 555nm (green-yellow) [15], which is the wavelength of maximum responsivity of human beings.

Let us assume that the photo-detector is exposed in a typical indoor office light of 200lux [16], and that 50% of the photon energy is effectively transferred to electrical energy. The total number of photons effectively detected can be calculated as follows:

$$\begin{aligned}\text{Power of } 200\,\text{lux} &= 50\%\times200\times1.464\times10^{-3}W/m^2 \\ &= 146.4\times10^{-15}W/\mu m^2 \ (\text{or } J/s/\mu m^2)\end{aligned} \tag{4}$$

$$\text{Energy of a photon (555nm)} = \frac{hc}{\lambda}$$
$$= \frac{(6.626\times10^{-34}\,J\cdot s)(2.998\times10^{8}\,m/s)}{555\times10^{-9}\,m} \quad (5)$$
$$= 3.579\times10^{-19}\,J/photon$$

$$\text{Total number of photons (per second per area)}$$
$$= \frac{146.4\times10^{-15}\,J/s/\mu m^2}{3.579\times10^{-19}\,J/photon} \quad (6)$$
$$= 0.409\times10^{6}\,photons/s/\mu m^2$$

The total number of electron-hole pairs effectively created by the photons is 4.09×10^5 per second per μm^2. The current generated by the photons, or photocurrent, is therefore 4.09×10^5 e^- /sec/μm^2 or $(4.09\times10^5) \times (1.6022\times10^{-19})$ C/s = 65.53fA/μm^2. For 18% efficiency from photons to detected electron-hole pair, a relatively high value for silicon, the photocurrent is only 23.59fA/μm^2. This extremely small current, which is very difficult to detect, is the main reason why charge accumulation, that is integrating the charge over a period of time, is necessary. The most successful imagers to use this concept were the CCD and the APS. The following two sections discuss two methods often employed to integrate photocurrent within a single photo-site, namely the charge-coupled device and photodiode.

2.2 Charge-Coupled Device

The Charge-Coupled Device (CCD) was invented by Boyle and Smith back in 1969 at Bell Laboratories [17]. By utilizing the Metal-Insulator-Semiconductor (MIS) device, a new type of memory storage for computers called the CCD was invented [18] [19]. In 1973, an image sensor was fabricated for commercial low resolution television, which has two 64x106 arrays or 13,000 CCD elements [20]. In 1974, Fairchild Electronics produced the first astronomical CCD

image using a commercial 100x100 pixel CCD array and an 8-inch telescope [21] [22]. Subsequently, the concept of a replacement for the traditional camera film has been investigated.

The earliest metal-insulator-semiconductor on a charge-coupled device was constructed with a thin insulating film sandwiched between a top metal layer and a bottom semiconductor substrate [23]. The first CCD used Cr-Au as the metal layer and n-type silicon as the semiconductor layer [24]. The insulating layer is usually silicon dioxide (SiO_2), thus forming a Metal-Oxide-Semiconductor (MOS) capacitor as in Figure 4 below.

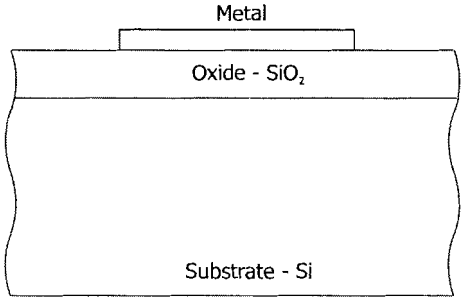


Figure 4 Metal-oxide-semiconductor capacitor

Besides using metal, polysilicon was also used as the top layer (also known as the gate) due to the semi-transparent property of polysilicon [25] [26]. As mentioned in the last section, light with shorter wavelength has a shallow penetration depth, leading to poorer detection by the CCD because much of the power might get absorbed by the gate material. The polysilicon is partially opaque and its thickness adds to the depth which the light signal has to penetrate before being picked up by the silicon underneath. Table 4 below presents a list of the depth at which 90% of incident photons are absorbed by a typical CCD.

Table 4 Depth at which 90% of incident photons are absorbed by a typical CCD [27]

Wavelength (nm)	400	450	500	550	600	650	700
Penetration Depth (μm)	0.19	1	2.3	3.3	5	7.6	8.5

2.2.1 Operation of CCD

When a positive voltage is applied to the metal or polysilicon gate of the MOS capacitor, a depletion region, i.e. a region absent of carriers, is formed under the silicon dioxide layer on the silicon substrate. In effect, surface potential (ψ_s) under this gate is increased, thus creating a potential well for charge storage. This is illustrated in Figure 5 below.

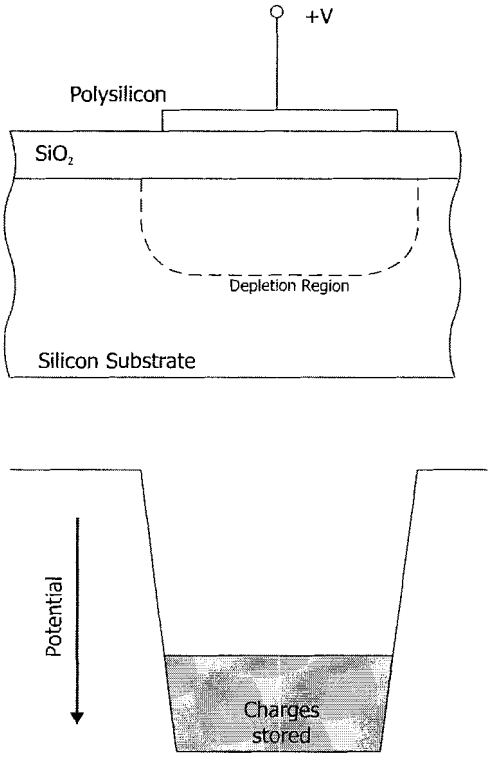


Figure 5 Potential well of a MOS capacitor when positive voltage is applied to the gate

This potential well allows charge to be stored under the gate and the amount of charge that the well is capable of storing depends on the voltage applied to the gate. When incident light (i.e. photon) excites the silicon either by front-illumination or back-illumination, photo-generated electron-hole pairs are created. Electrons are collected by this potential well while the substrate connection collects the holes, thus separating them to prevent recombination.

A CCD imaging array is basically an array of MOS capacitors closely spaced together. Each MOS capacitor represents a pixel of a CCD imaging array. By carefully controlling the

voltages of the gates of this array of MOS capacitors, charges can be transferred from one location under a gate to another location under another gate. Three different techniques for this operation are possible: two-phase, three-phase, and four-phase.

The first type of charge-coupled device in the early 1970s uses a three-phase transfer scheme [28]. Figure 6 below shows the cross section of the basic three-phase CCD.

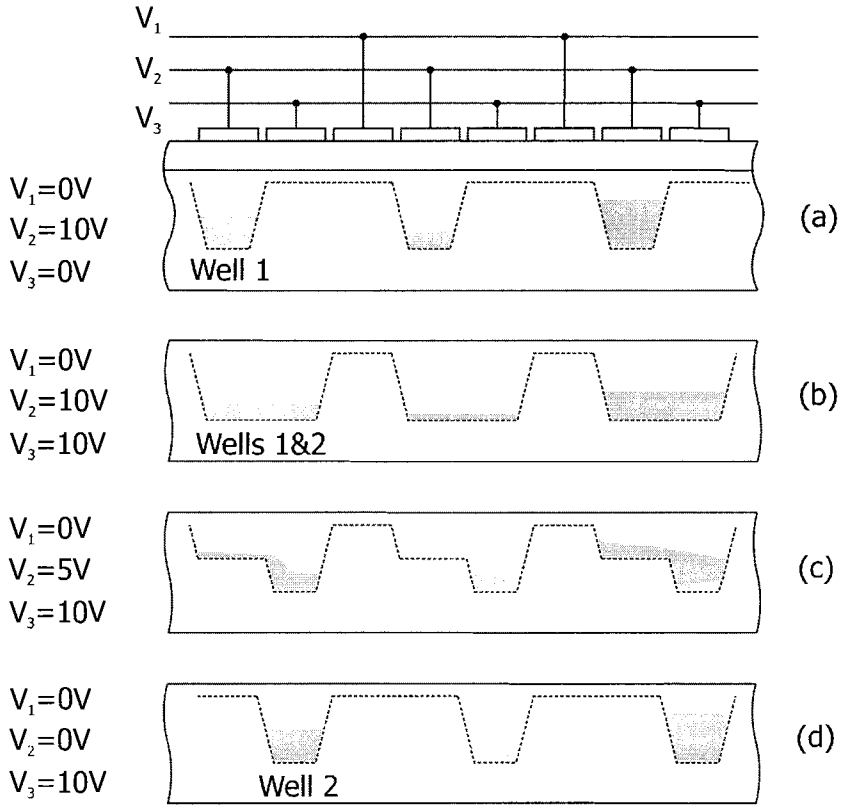


Figure 6 Cross section of the earliest three-phase charge-coupled device after Boyle and Smith [29]

Every third gate is connected together to a single input voltage. Assume that charge exists within potential well 1 when the V_1 is 10V while both V_2 and V_3 are 0V (a). Now V_2 is increased to 10V while V_3 remains at 0V (b). The charge would spread out across potential wells 1 and 2. As V_1 is reduced to 5V, the charge stored under potential well 1 would flow to well 2 due to thermal diffusion, self-induced drift, and the fringing field effect (c) [14]. By pulsing V_1 off to 0V and keeping V_2 at 10V, the charge originally in potential well 1 in effect has been

transferred to potential well 2. Repeating the above procedure to V_2 and V_3 would transfer the charge to potential well 3 (d). This practice of moving charge is called the bit bucket technique. Using this, the information in each pixel can be shifted to the end of the CCD, allowing it to be readout.

2.2.2 Figures of Merit for CCD

Let us take a 1000×1000 (1 mega pixel) CCD array. Since the charge under a gate represents the value of a particular pixel, it is very important that this signal is read out properly. This means the amount of charge in any pixel should be nearly perfectly transferred to the last pixel on the row for output. Figure 7 below shows a 1 mega pixel CCD array with output buffer on the right end of the array.

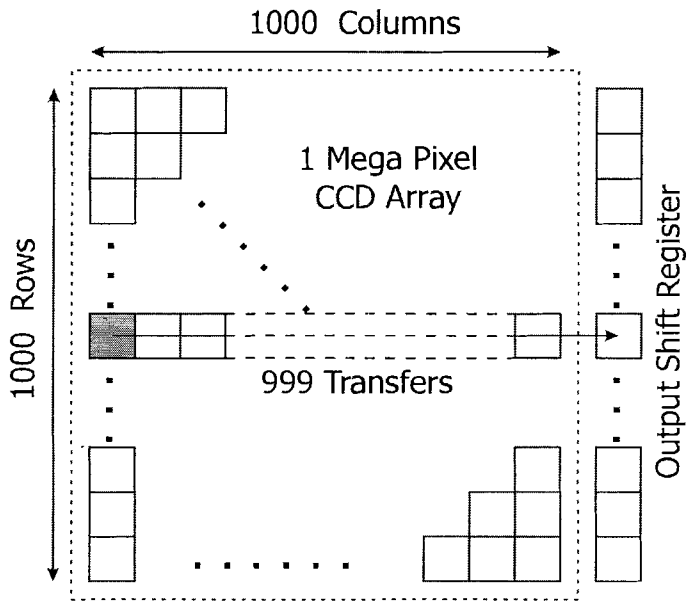


Figure 7 Charge transfer of a 1 mega pixel CCD array

Unfortunately, it is impossible to have 100% transfer efficiency from pixel to pixel, thus Charge Transfer Efficiency (CTE) is used to measure the percentile of the charge transferred effectively. Some charge might get trapped and left behind in a pixel, resulting in pixel information lost when a signal is being transferred to an adjacent pixel with less than 100%

transfer efficiency. In order to obtain 90% of the original signal transferred from one end of the CCD array to the other end at the output shift register, it requires a CTE of 99.9895% in this case. Obtaining 99% of the original signal requires a CTE of 99.9990%. Therefore, the geometry of the pixel, the fabrication process parameters, and the voltages used are all crucial to achieving high CTE. As the resolution of imaging arrays approaches 10MPixel, pixel count on each row easily reaches several thousand. Therefore, the CTE requirement is much higher for several thousand transfers in a single row. Note that the charge left behind alters the information in the previous pixel, smearing the image and this accumulates with each transfer.

A second important figure for charge-coupled device is operating speed. For a signal to be read out from one end of the array to the other end for readout, it takes 1000 transfers. Apparently, the operating speed of the CCD very much depends on the time it takes for the transfer and this is one of the drawbacks of the CCD. The time it takes for each transfer from one potential well to the adjacent one would affect the charge transfer efficiency. The longer the charge is allowed to transfer, the higher proportion of the total charge can be transferred, and thus the higher the transfer efficiency. Therefore, the time that is allowed for charge transfer needs to be carefully controlled to obtain a balance of charge transfer efficiency and operating speed.

Power consumption is another major drawback of CCD. Continuous pulsing of the CCD gates, usually at 5V or more, to transfer charge from one end of the array to the other end requires significant power consumption. It makes CCD difficult to be utilized in battery-powered consumer electronics such as cell phones, personal digital assistants, and digital cameras. Moreover, note that CCD requires multiple voltages for the transfer operation.

Of all the factors for digital cameras, resolution is probably the parameter a general consumer pays the foremost attention to. Resolution of both consumer and professional digital cameras has been increasing at a fast pace in recent years. As fabrication technology approaches smaller than 100 nanometer scale, larger imaging arrays with high resolution are made possible.

The limitation, however, is primarily its fabrication yield rate, i.e. the percentage of functional dice among all fabricated chips. Fabrication defects dictate the yield rate and low yield rate implies high production cost. In memory chips, defects are minimized or overcome by using fault tolerance built into the memory array. The yield rate can be increased and cost can be lowered if defects are minimized and defective cells within the array can be fixed easily. Unfortunately, fault tolerance is not possible for CCD. In fact, failure of one pixel (MOS capacitor) could result in an entire dead row because no charge can be transferred through this dead pixel. For the above reasons, it is difficult to achieve high resolution and yield rate of large format CCD tends to be low thus resulting in high cost.

Fill factor refers to the portion of area sensitive to light, in percentage, among the entire pixel area (Figure 8). Since most of a CCD pixel area is dedicated to light sensing while minimal area is used as control lines, the CCD can achieve a fill factor as high as 100% effectively by the use of a micro lens that is placed on top of a pixel to focus incident light onto the pixel.

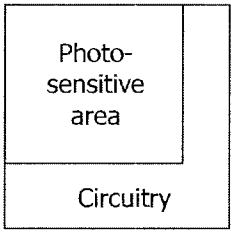


Figure 8 Fill factor of a pixel

The last but not least figure of merit is noise, which plays an important role in determining the performance of an image sensor. There are many types of noise such as temporal noise, reset noise, dark current, Fixed-Pattern Noise (FPN), Photo-Response Non-Uniformity (PRNU) noise, shot noise, flicker (1/f) noise, and quantization noise in an Analog-to-Digital Converter (ADC). Each of the aforementioned noise is a complicated topic and will not be discussed in detail here. Since CCD technology has matured over a span of 30 years, noise issues have been drastically minimized.

2.2.3 Future of CCD

After more than 30 years of development, CCD fabrication process has evolved into a high speed, low-noise [30], high resolution, and high fill factor technology. Blooming, one of the problems of CCD, has been improved by anti-blooming schemes [31]. Recent advancement of CCD includes Fujifilm's superCCD, superCCD HR, and superCCD SR [32]. SuperCCD reduces the pixel pitch, increases the sensitivity, dynamic range, and signal-to-noise ratio by rotating the pixels by 45°. SuperCCD HR achieves high resolution while its counterpart, superCCD SR, increases the dynamic range of the pixel by introducing a smaller sub-pixel photo-sensing element to avoid saturation and detect high intensity level.

Presently, as of 2005, CCD's dominate the point-and-shoot-type digital camera. As CCD technology has been well-established over the years, production of reasonably sized CCD has high yield and is cost effective. However, it reached a point where making ever larger CCD arrays is not cost effective. Therefore, CCD's seem to lag behind to the CMOS APS for the high-end professional digital SLR. On the other hand, as CCD's are not CMOS compatible, integrating system-on-a-chip is not feasible and therefore CCD's do not contribute much to the embedded camera system in low end handheld devices such as PDAs and cell phones. Moreover, power consumption becomes a major issue for these devices; thus a large share of the lower end consumer market requiring low power consumption is captured by APS [33] [34].

2.3 Photodiode

A silicon photodiode is simply an interfacing of p-type silicon and n-type silicon to form a p-n junction diode that is used for photon detection. A vertical p-n junction photodiode is shown in Figure 9 below.

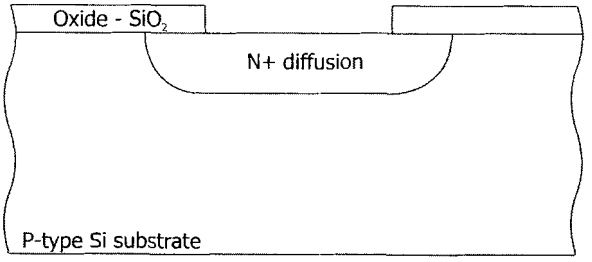


Figure 9 Illustration of p-n junction photodiode on a silicon substrate

When a p-n junction is formed, a depletion region is created in which mobile carriers are depleted from the region. The concentration difference of p-carriers (holes) would cause holes to diffuse from the p-region of higher hole concentration to the n-region. This diffusion results in depletion of holes on the p-side near the p-n junction. For the same reason for the n-carriers (electrons), a region depleted of electrons appears near the p-n junction on the n-side. The actions of both the electrons and holes above, called diffusion current, is shown in Figure 10 below.

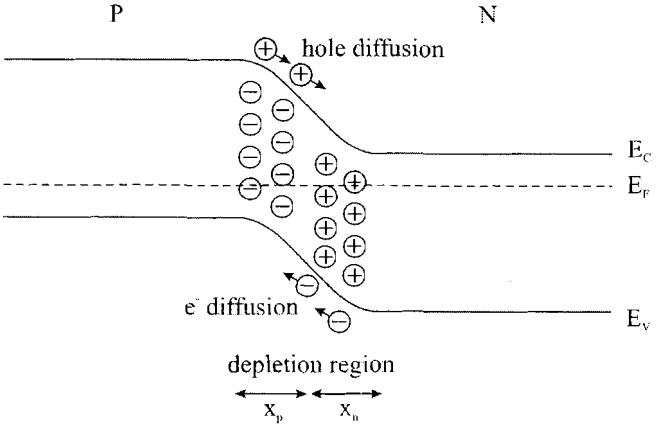


Figure 10 Diffusion and depletion region of a p-n junction diode

The depleted region has a width of x_p on the p-side and a width of x_n on the n-side; thus the total depletion width is $x_p + x_n$. This depletion region results in a net charge of un-neutralized silicon ions, negative on the p-side and positive on the n-side. The net charge, by Gauss Law, implies there is an electric field in the direction from right to the left in Figure 11 below. This

electric field in turn causes another current, called the drift current, with direction as shown in Figure 11.

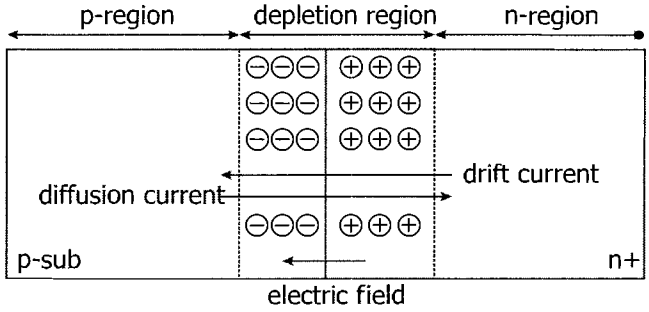


Figure 11 Thermal equilibrium of p-n junction photodiode

The maximum electric field at the junction is given by the following equation [14]:

$$E = -\frac{q}{\varepsilon} N_d x_n \tag{7}$$

q is the electronic charge, N_d is the concentration of n-carriers, and x_n is the penetration of the depletion region into the n material. In thermal equilibrium, i.e. no external voltage, no photo-excitation, and uniform temperature, drift current and diffusion current counteract each other to provide a net zero current.

2.3.1 Operation of Photodiode

When electron-hole pairs are generated within the depletion region as mentioned in Section 2.1.2, the electric field will separate the electrons and holes. Holes will be attracted to the p-side of the p-n junction, which is negatively charged due to depletion of holes, while electrons will be attracted to the n-side. The combination of these two actions makes up the photocurrent.

If photons hit the bulk region of the p-n junction with no electric field, photo-generated electron-hole pairs will not be separated and will eventually recombine, as shown in Figure 12. The light signal will not be detected in this region and is then lost, reducing quantum efficiency.

Therefore, if the depletion region can be carefully controlled, it would seem wise to increase the width of the depletion region, thus widening the electric field, for photo-detection purposes.

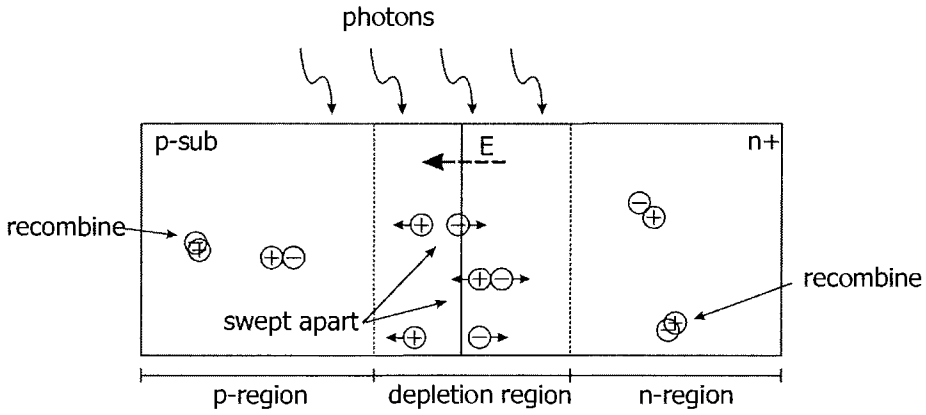


Figure 12 Electron-hole pair generation in photodiode

When a voltage is applied across the p-n junction, the characteristics of the diode change. A positive voltage applied to the n-side of the p-n junction relative to the p-side, called reverse-biasing the diode, increases the width of the depletion region. The detail of the characteristics will not be discussed in this thesis but readers are referred to [35] [36] and [37]. Increasing the width of the depletion region is one of the most important changes for image sensing. However, increasing the depletion region increases the transit time of carriers and the response of the photodiode is slower. Therefore, tradeoffs exist between response time and quantum efficiency.

In standard CMOS technology, p-n junction is formed vertically as shown in Figure 9 above. Therefore, the depth of the p-n junction is extremely important in a photo-detector. The standard CMOS p-n junction depth however is usually not ideal for photo-sensing as it is optimized for standard analog/digital CMOS operation. This is especially true for smaller technologies (e.g. 0.18μm) as the junction depth decreases as the technology size shrinks.

2.3.2 Photodiode Model

A simulation model for the photodiode is proposed by Swe and Yeo in [38]. The noise components of the photodiode model are omitted for simplicity sake. The model is shown in Figure 13 below.

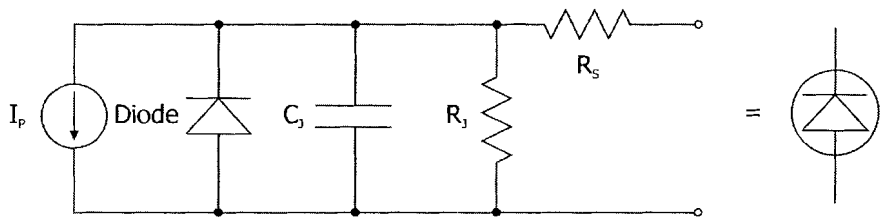


Figure 13 Photodiode model

I_P is photocurrent generated by the photodiode, C_J is the junction capacitance, R_J is the junction resistance, and R_S is the series resistance. The photocurrent per area is calculated by the following equation [14]:

$$I_p = \frac{q\eta P_{opt}}{h\nu} = \frac{q\eta P_{opt}}{hc/\lambda} \tag{8}$$

where,

I_p = photo current per area
q = electronic charge = $1.602\times10^{-19}\,C$
η = quantum efficiency
P_{opt} = optical power
h = Planck's constant = $6.6262\times10^{-34}\,Js$
ν = frequency
c = speed of light = $3\times10^{8}\,m/s$
λ = wavelength

The junction capacitance, C_J, is the parasitic capacitance of the photodiode. This depletion capacitance changes as the voltage at the cathode changes during the integration period. From [39], the depletion capacitance of a photodiode is:

$$C_{jdep} = \frac{cj \cdot A_D}{\left(1+\frac{V_{DB}}{pb}\right)^{mj}} + \frac{cjsw \cdot P_D}{\left(1+\frac{V_{DB}}{pbsw}\right)^{mjsw}} \tag{9}$$

where,

cj = zero - bias depletion capacitance
$cjsw$ = sidewall zero - bias depletion capacitance
A_D = Area of diode
P_D = Periphery of diode
V_{DB} = Voltage across diode
pb = built - in potential
mj = grading coefficient
$pbsw$ = built - in potential of the sidewall
$mjsw$ = grading coefficient of the sidewall

Typical capacitance value of a photodiode of size 10μm × 10μm in CMOS 0.18 micron technology is approximately 7×10^{-15}F or 7fF (femto Farads). The series resistance, R_S, consists of the resistance of the non-depleted silicon and contacts resistance [40] and it is:

$$R_S = \frac{(W_S - W_d)\rho}{A} + R_C \tag{10}$$

The junction resistance, R_J, varies with the current of the photodiode [14]:

$$R_J = \frac{nkT}{qJA_J} = \frac{nkT}{qI} \tag{11}$$

2.3.3 Figures of Merit for Photodiode

The operating speed of the photodiode depends on the width of the depletion region [14]. If a photodiode is required to operate in high speed, the width of the depletion region needs to be small to reduce the transit time for the charge. However, the photodiode in the APS is used to integrate charge, as it will be shown later. Therefore, the dependence of the depletion width for

the operating speed is not much of an issue. It would only be important when the photodiode is used by itself as the photo-detector.

Apparently with narrow depletion region, the quantum efficiency will be reduced. Moreover, the spectral response will also be different because the depth of the depletion region is changed. Since one of the most important concerns for photodiode is quantum efficiency, in most cases, the photodiode is reverse-biased to create a thick depletion region, thus enhancing quantum efficiency.

With all said, it should be noted that a photodiode is only the input stage of an image sensor. The output portion of the sensor can be implemented with many different approaches. Therefore, merely the operating speed of the photodiode does not dictate the entire operating speed of an image sensing array. Due to the same reason, the power consumption, resolution, fill factor, and noise of a photodiode will not be compared to that of the CCD here. The competition for CCD comes from the active pixel sensor, in which one of the several possible light sensing methods is by using a photodiode. Thus we will compare the photodiode-based APS in the next section.

2.4 Active Pixel Sensor

In searching for a faster, cheaper, more robust, and less power consuming image sensing solution as a successor for the charge-coupled device, Eric Fossum from NASA's Jet Propulsion Laboratory developed the Active Pixel Sensor (APS) in 1993. An active pixel sensor is defined as an imaging sensor "with one or more active transistors located within each pixel" [41]. It is also widely known as CMOS imaging sensor due to its CMOS compatibility. It opens the door to a whole new dimension in digital imagery as APS promises to provide a lot of advantages over CCD. Since then, an enormous amount of effort has been put into the research and studies of the APS and several examples are in [42], [43], [44], [45], and [46]. While APS retains some of the advantages of CCD such as high sensitivity and large array formats [41], some of the advantages

claimed by APS over CCD are higher operating speed, lower power consumption, lower cost, ability to integrate System-On-a-Chip (SOC), and random pixel access.

The photo-detecting element for the APS can be either a photodiode or a photogate. While the detail of a photodiode has been discussed in last section, the photogate actually borrows the idea from CCD technology as the light sensing element. The following sections will discuss each of the two types of APS, photodiode and photogate, including their architectures, operations, characteristics, differences, and performance.

2.4.1 Photodiode-Based APS

A photodiode APS consists of a photodiode and three transistors, namely the reset transistor (M_{RST}), the readout transistor (M_{OUT}), and the row select transistor (M_{ROW}), usually referred as the 3-transistor (3-T) photodiode APS. Figure 14 below illustrates the schematic of a 3-T photodiode active pixel sensor.

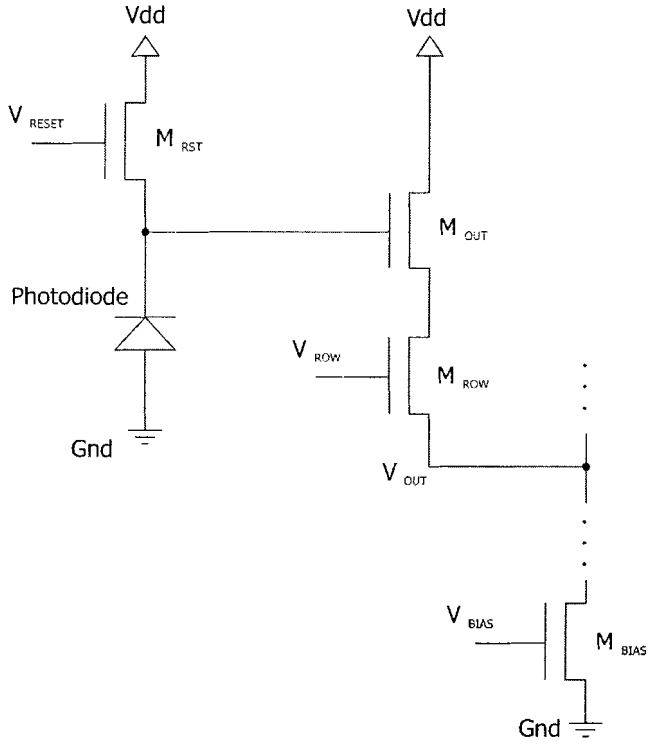


Figure 14 3-T Photodiode active pixel sensor schematic

The readout transistor M_{OUT}, when being sunk with a constant current, acts as a source follower. The bias transistor M_{BIAS} is not part of the pixel itself, but is shared by all pixels in the array on the same column. M_{BIAS} provides a constant current sink to the readout transistor M_{OUT} by applying a bias voltage V_{BIAS} to the gate and keeps it operating in the saturation region. Ideally, M_{BIAS} provides a constant current sink, therefore it would be important to design this transistor to maximize the range where the current being sunk is consistent. An ideal transistor supplies a constant current when V_{GS} is fixed and less than $V_{DS}+V_t$. In reality, the channel length modulation comes into play, increasing the current as V_{DS} increases. Therefore, the bias transistor should have a long channel to minimize channel length modulation. The effect of this issue will be shown in simulation of the simple photodiode-type APS in Chapter 7.

An APS operating cycle has three phases: reset phase, integration phase, and readout phase. At the beginning of a cycle is the reset phase. The reset transistor (M_{RST}) is turned on by applying VDD to the gate of M_{RST}, thus resetting the photodiode and the gate of the output transistor to approximately VDD-Vth (M_{RST}). In CMOS 0.18 micron technology, where the power supply voltage is 1.8V and the threshold voltage is about 0.5V, the readout transistor's gate is reset to about 1.3V.

Integration follows the reset phase. Photo-generated charge is created when incident light (i.e. photon) hits the surface of the photodiode. As it is noted in Section 2.3, since the photodiode is reversed-biased, electrons and holes generated will be swept apart. Electrons will be swept to the cathode of the photodiode and holes to the anode. Since this photocurrent is extremely small, in the pico ampere range, all the charge generated by the photocurrent is required to be integrated during a period of time in order for it to be sensed by the gate of the readout transistor. Integration of charges essentially happens on the gate capacitance of the readout transistor as well as the parasitic capacitance of the photodiode.

It can be noted that the controls required for the pixel are only the reset signal and the row select signal. This is relatively simple compared to CCD and the photogate APS, as it will be shown in the next subsection. Figure 15 below shows a typical operating cycle of a photodiode APS and the output.

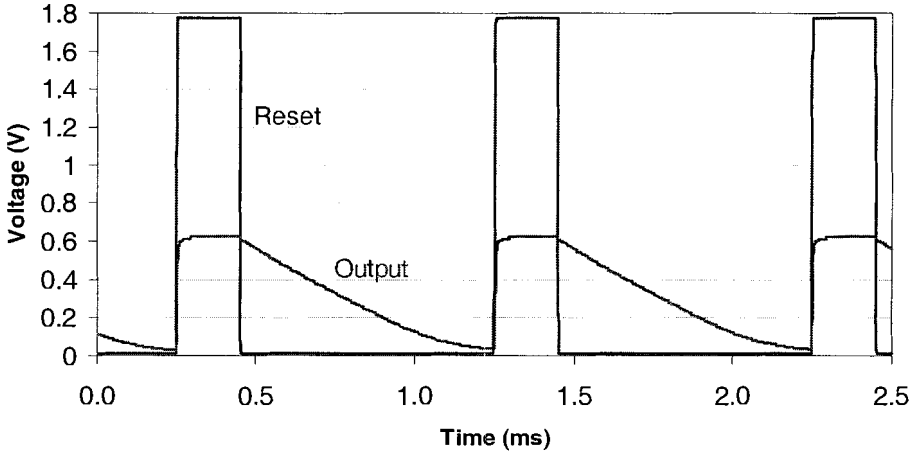


Figure 15 Typical operating cycle of a photodiode APS

During integration, the photo-generated charge basically discharges the gate of the readout transistor. It can be seen that the output voltage drops during integration. At the beginning, the APS operates in the linear region. As the readout gate further discharges, the APS will eventually enter a non-linear region. The dynamic range of the APS, i.e. the range of the output, depends on the bias voltage. For saturation of M_{BIAS},

$$\begin{aligned} V_{DS} &\geq V_{GS} - V_t \\ V_D &\geq V_G - V_t \\ V_{out} &\geq V_{bias} - V_{t-b} \end{aligned} \tag{12}$$

At t=0, immediately after reset (ignoring the voltage drop across the row select transistor)

$$V_{out}(\max) = V_{G-M1} - V_{GS-M1} \tag{13}$$

Minimum value of output voltage:

$$V_{out}(\min) = V_{bias} - V_{t-Mbias} \tag{14}$$

To minimize V_{out}(min), we choose the bias voltage to be slightly larger than $V_{t\text{-}Mbias}$

$$V_{bias} = V_{t-Mbias} + 0.05V \tag{15}$$

$V_{G\text{-}M1}$ is $VDD\text{-}V_{t\text{-}MReset}$ during reset and $V_{GS\text{-}M1}$ is approximately $V_{t\text{-}M1}$. Thus the maximum dynamic range is ($V_{bias} - V_t$) or 0.05V to ($VDD\text{-}2V_t$), assuming threshold voltage is fixed.

The output response of the photodiode APS depends on two main factors, namely the charge-to-voltage conversion gain and the voltage swing. The charge-to-voltage conversion gain of the photodiode APS, ΔV_{gain} is inversely proportional to the total capacitance of the readout node and is equal to the charge of electron q divided by the capacitance of the readout node [12], i.e.

$$\Delta V_{gain} = \frac{q}{C_{total}} \tag{16}$$

The total capacitance, C_{total}, is equal to the sum of the photodiode capacitance and the capacitance at the gate of the readout transistor, i.e. $C_{total} \approx C_{photodiode} + C_{gate}$. However, it is dominated by the photodiode. As mentioned before, typically values for the capacitance of the photodiode is in the fF range (~7fF) while the capacitance of the gate of the readout transistor is approximately one tenth of the photodiode capacitance (~0.4fF) for a minimum gate geometry. Other parasitic capacitances from the drain, source, and metal line are much smaller. In Section 2.3.2, it was seen that the capacitance of the photodiode is approximately directly proportional to the area of the photodiode. Therefore, a larger photodiode area results in lower conversion gain.

On the other hand, the voltage swing at the APS output is determined from the photo-generated charge, which in turn is determined by the size of the photodiode. Larger photodiode implies more photo-generated charge and therefore a larger voltage swing. This relationship can be characterized by the equation below:

$$V = \frac{Q}{C} \tag{17}$$

where Q is the total photo-generated charge collected and C is the total capacitance at the readout node

For a large photodiode area (>5μm×5μm), the capacitance of the photodiode is mainly contributed by the area of the photodiode. Thus an increase in area results in an increase in capacitance and photocurrent (thus photo-generated charge), and the voltage swing (or sensitivity) is nearly unchanged. However, as the photodiode gets smaller, the sidewall capacitance of the photodiode plays a more important role. As the photodiode area is decreased, the rate of decrease of the capacitance is slower than the rate at which the photodiode area is decreased because the sidewall capacitance starts to have a significant impact. For example, consider reducing a square photodiode of size L×Lμm^2 to L/2×L/2μm^2. The area is decreased by 75% while the total length of the sidewall is only reduced by 50%. Therefore, to the first order, the total photo-generated charge is reduced by 75% but the capacitance is only reduced by half. Thus the voltage swing of the APS is halved.

Therefore, a trade-off between the charge-to-voltage conversion gain and the voltage swing is needed but it requires a more extensive study out of the scope of this thesis.

2.4.2 Photogate-Based APS

While this thesis concentrates on the photodiode APS, some photogate APS work was also investigated. The photogate APS, also invented by Fossum [41], is identical to the photodiode version except for the light sensing element. The light detection in a photogate borrows the idea from the charge-coupled device. Instead of a photodiode, a single CCD unit (or photogate, PG) is used to detect light. Photo-generated charges are trapped under this gate if a voltage is applied. With single poly layer, a transfer gate (TX), essentially a transistor, is built between the photogate and the gate of the readout transistor. This transfer gate can act as a

smaller CCD but it will not be used for light detection and only for the control of the photo-generated charge flow. Figure 16 below shows the schematic of the photogate APS.

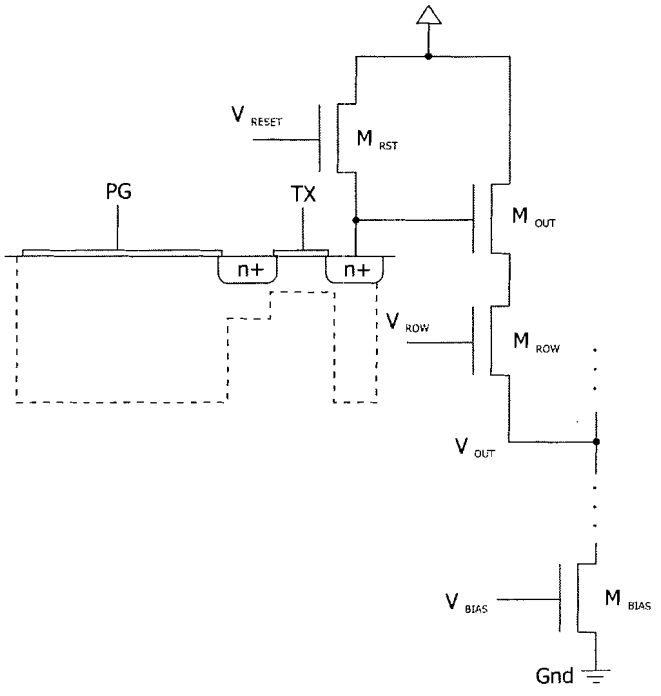


Figure 16 Photogate active pixel sensor schematic

For the salicided (Self-Aligned silicided) CMOS 0.18 micron process, the polysilicon layer is covered with silicide, which is opaque. A special mask called the RPO layer, however, is available to mask out the area where silicide is undesired. The gate of the photogate, now a very thin layer of non-silicided polysilicon, is transparent to visible light so incident light can transmit through the gate and falls on the silicon bulk. Penetration depth of incident light in PG is similar to that of the CCD as their structures are essentially the same and it was discussed in Section 2.2. Electron-hole pairs are generated under the photogate and trap in the potential well when a positive voltage is applied to the gate, as in the CCD.

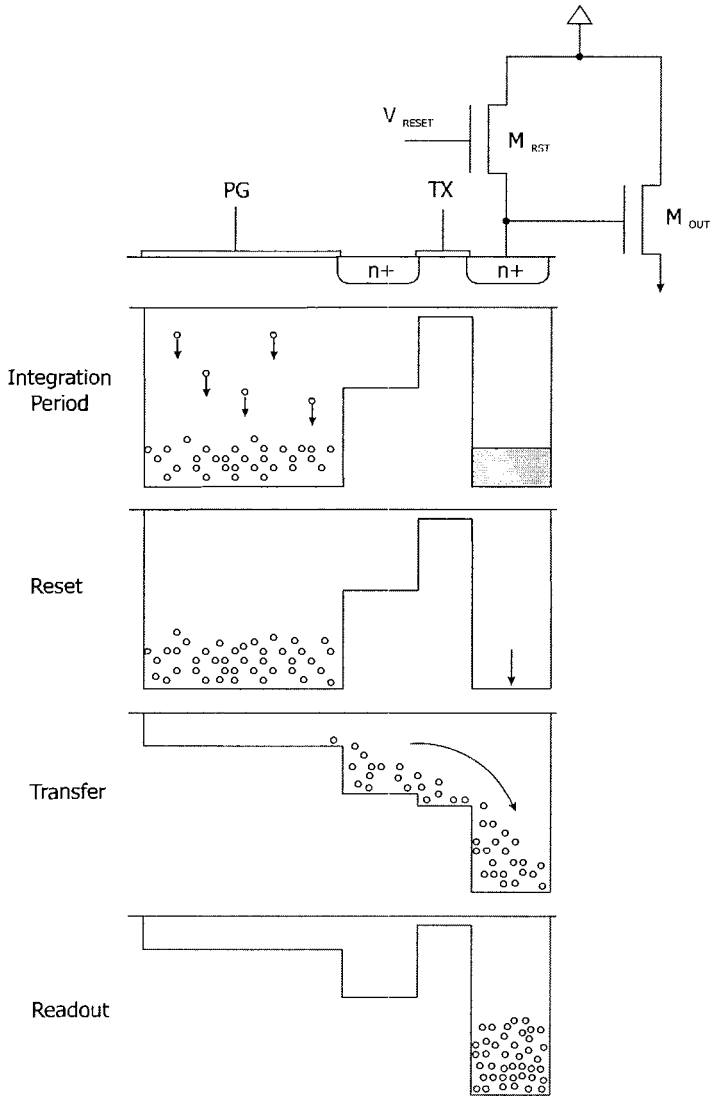


Figure 17 Typical operation cycle of a photogate APS

The transfer gate (TX) and the photogate (PG) together act similar to two CCD units. When the appropriate voltages are applied at appropriate times, charge can be transferred from under the photogate to the gate of the readout transistor via the transfer gate. The charge transfer is illustrated in Figure 17 above, showing the operation cycle of a photogate APS.

A photogate active pixel sensor, similar to its photodiode counterpart, has four phases of operation, three of which are identical: reset phase, integration phase, and readout phase. The extra phase is the transfer phase, and therefore, more control signals are required and the timing

control is more complex compared to the photodiode, which requires only one reset control. Besides reset, the photogate APS also requires a photogate signal (PG), and a transfer gate signal (TX).

At the beginning of an integration cycle, the photogate (PG) is turned on and, similar to the CCD, a potential well is created for charge accumulation. Electron-hole pairs are generated by incident photons and integration of charges occurs under the photogate. At the end of the integration, the reset transistor (M_{RST}) is turned on and the readout node (gate of M_{OUT}) is reset to a pre-defined voltage. This clears out all the charges from the previous integration cycle and prepares for the readout of a new integrated signal.

All the charges are then transferred from under the photogate to the readout node by first lowering the potential barrier of the transfer gate (TX) to about ½ VDD. The potential of the PG is then lowered, essentially raising the potential well, to force all the charges to flow from a high potential well to a low potential well. This is similar to the transfer of charges from one CCD pixel to the next CCD pixel; thus the charge transfer efficiency is very important for the photogate APS. At last, after TX is turned off to prevent further charge transfer from PG and after the row select transistor (M_{ROW}) is enabled, the signal is read out from the readout transistor.

2.4.3 Differences between Photodiode-Based and Photogate-Based APS'

Several differences between the photodiode APS and the photogate APS can be observed from the fact that the structure of the photo-sensing elements are different. First of all, the polysilicon layer of the photogate reduces the response of blue light because the shorter wavelength will be absorbed by the gate. A photogate APS fabricated in a standard 0.18 micron CMOS technology has been reported with less than 5% quantum efficiency for wavelength under 450nm [47]. This behaviour of light with different wavelengths in silicon is exploited when Foveon Inc. invented the X3 active pixel sensor, which detects red, green, and blue lights at different depth of the pixel [48]. However, the sensitivity of the photodiode APS in general does

get hampered by the fact that the sensing node is shared by the gate of the readout transistor and the photodiode capacitance [49]. As a whole, the photodiode APS is still more sensitive than the photogate APS in general imaging work due to its better blue response.

Second, since the photogate has more devices, essentially 5 transistors, the fill factor of the pixel is decreased. Otherwise, the pixel area needs to increase to maintain the same fill factor.

The extra requirements of control signal for the photogate make the timing circuitry much more complex compared to the photodiode. As it is illustrated above in the operation cycle, the timing of all signals is very critical and has to be carefully synchronized. This complication slightly increases the power consumption of a photogate APS as well.

The photodiode APS integrates charge at both the photodiode capacitance as well as the gate capacitance of the readout transistor. These two nodes essentially form one photo-site for charge integration with $C_{total} \approx C_{photodiode} + C_{gate}$. Compared to that of the photogate APS, the integration node, being the photogate only, is separated by the transfer gate from the readout node, which is the gate of the readout transistor, shown as M_{OUT} in Figure 16. Since the sense node (gate of the readout transistor) is separated from the photogate by the transfer, all the charge is transferred to the gate with $C_{total} \approx C_{gate}$. Therefore, the conversion gain, $\Delta V_{gain} = q / C_{total}$ of the photogate APS is higher. Moreover, the transfer mechanism of the photogate APS allows "multiple integration", in which charge integrated under the photogate can be transferred to the readout node multiple times before the signal is eventually readout through the row select transistor, shown as M_{ROW} in Figure 16.

For the active pixel sensor, one of the major challenges so far is the reduction in noise, such as reset noise (or kTC noise), 1/f noise, shot noise, and thermal noise. These noises comes from various sources including threshold voltage variation along the pixel array on the substrate, power supply voltage fluctuation, photodiode's dark current, and variation of reset voltage from frame to frame. Each type of noise deserves its own thesis work and is not within the scope of

this thesis. However, one simple method often used to reduce reset noise is Correlated Double Sampling (CDS). CDS records and compares the output signals from the pixel before and after integration in order to subtract the noise out from the pixel. This procedure is carried out by a sample and hold circuit, positioned at the bottom of each column of the APS array [50]. While CDS can be carried out in photogate APS, CDS is generally more difficult to implement for the photodiode APS but Double Sampling (DS) is easier. Figure 18 below illustrates the difference between DS and CDS in a timing diagram.

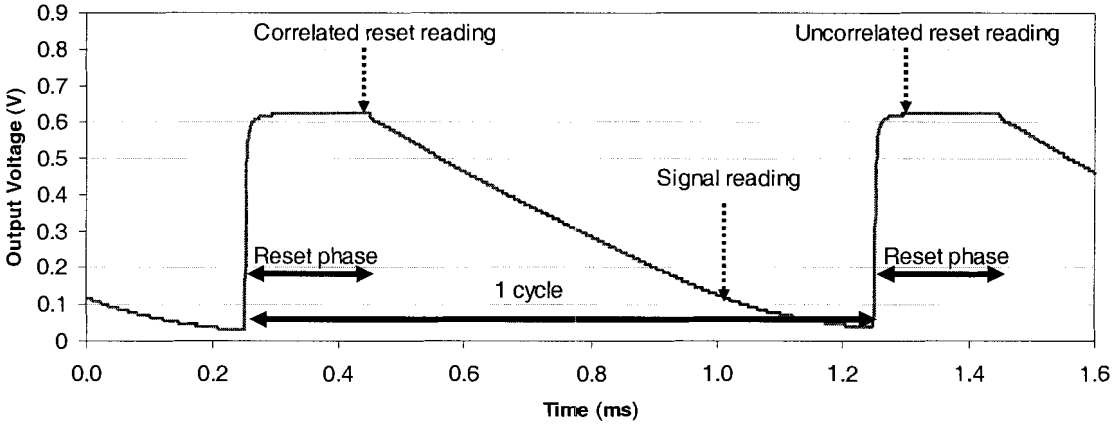


Figure 18 Comparison of correlated double sampling and double sampling

The reset noise is correlated, thus the term correlated double sampling, if the reset value is taken and compared to the integrated signal within the same integration cycle. If the reset value is subtracted from the light signal that comes from the next integration cycle, it is referred to as double sampling.

Therefore, one of the main advantages of using the photogate APS is the ability to remove reset noise [51]. Table 5 below summarizes the differences between the photodiode and photogate APS'.

Table 5 Summary of differences between photodiode APS and photogate APS

	Photodiode APS	Photogate APS
Responsivity	Better blue response	Poorer blue response
Overall Sensitivity	Higher	Lower
Fill factor	Higher	Lower
Control signals	Simple	Complicated
Power consumption	Low	Slightly higher
Total capacitance at output node	Cphotodiode + Cgate	Cgate
Charge integration	On same photo-site	On separate photo-site
Multiple integration	Not possible	Possible
Correlated Double Sampling (CDS)	Possible	Double Sampling (DS) only

While each of the two light sensing elements, the photodiode and the photogate, has their own advantages and disadvantages, choosing the better one for the APS depends greatly on the application in which it is being used.

2.4.4 4-T Photodiode APS

The photodiode APS with four transistors (4-T APS) is the shuttered version of the regular photodiode APS. An extra transistor is inserted between the photodiode and the gate of the readout transistor in order to separate the photo-site and the output node, similar to the photogate version of the APS. When the shutter is off, the photodiode is isolated from the readout transistor node, thus the integration of the photo-generated charge happens at the parasitic capacitance of the photodiode as opposed to both the parasitic capacitance of the photodiode and the gate capacitance of the output transistor. However, as the shutter is opened (turned on), the charge is redistributed to the photodiode capacitance and the readout gate capacitance, which is similar to the 3-T photodiode APS case without the shutter.

The additional transistor requires an extra control line for the shutter for manipulating the readout timing, i.e. when the integrated charges are transferred to the readout transistor for

readout. With the shutter transistor separating the photodiode and the output transistor, two possible schematics of this APS are illustrated below in Figure 19.

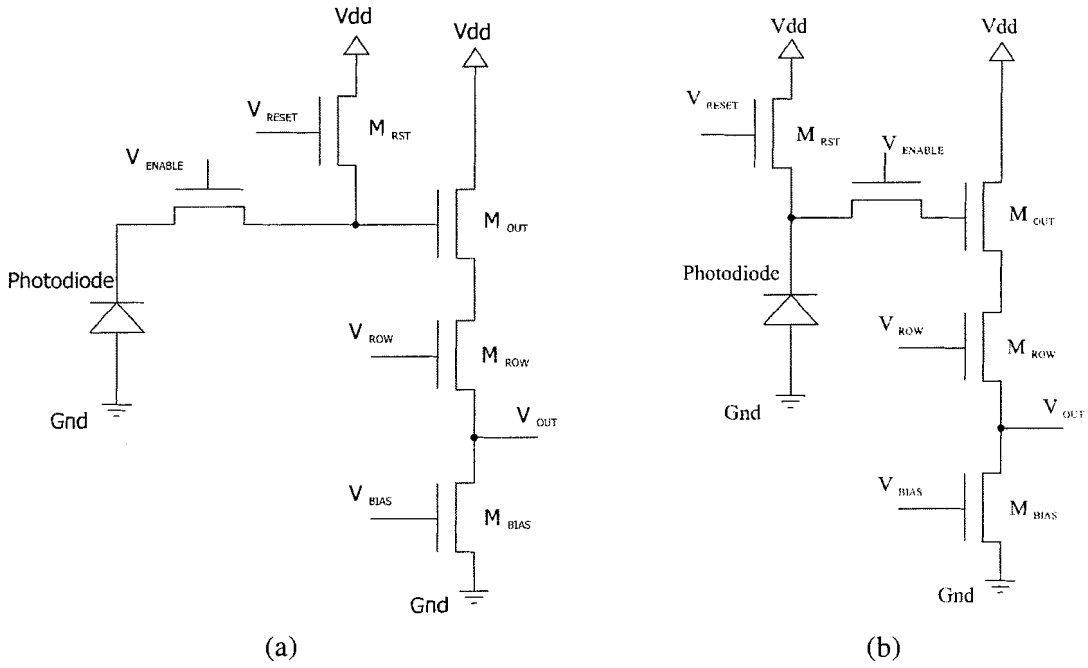


Figure 19 Photodiode Active Pixel Sensor with shutter (4-T APS)

The reset transistor can be positioned on either side of the shutter, Figure 19 (a) at the gate of the readout transistor (source follower) or Figure 19 (b) at the cathode of the photodiode. The two 4-T APS designs differ significantly in terms of their clocking schemes and usability. In all the designs the author submitted, the second design, as shown in Figure 19 (b), is used. However, it was discovered that it might be of advantageous to use the first schematic, as shown in Figure 19 (a), for the purpose of the proposed novel APS design. The advantage of using this schematic will be discussed in Chapter 7 when simulations are presented.

Although a shutter is present, multiple integrations are not possible. Unlike the photogate, in which all the charges are dumped to the readout node at the end of integration, when the enable transistor is turned on in this 4-T APS, charges are divided between the capacitance of the photodiode and that of the gate of the readout transistor. The photodiode relies

on the reset transistor to reset its voltage while the photogate basically resets itself and is ready immediately for another integration.

2.4.5 Advantages of APS over CCD

As it was shown in the section involving CCD, each signal in a CCD cell is shifted to one end for readout. This readout scheme results in slower operating speed compared to APS, in which no shifting of signal is necessary and any pixel in any row or column can be readout immediately, i.e. random pixel access.

Higher power consumption of the CCD is due to the constant pulsing of gates for integration and the shifting of signals from one end to the other and these gate voltages are usually higher in the order of 5V to 10V. Multiple voltages are also required which results in more complex circuits. In contrast, voltage pulsing occurs in APS only during global reset, global transfer (for photogate APS only) and when a row is selected. These voltages are usually the supplied voltage of the technology, e.g. 1.8V for CMOS 0.18 micron technology. Current is drained only for a small period of time when a row is selected.

Cost, which is usually one of the most important driving forces of a product, is lower for making APS because of its CMOS compatibility. Would-be-obsolete CMOS fabrication plants that used to fabricate larger geometry semiconductors can be utilized to produce APS, which does not require the most advanced transistor technology. For example, APS' using CMOS 0.5 micron or larger technology outperforms APS' using CMOS 0.18 micron technology without technology optimization [52]. However, at the time of design, only 0.18 micron technology was available to the author. Moreover, sensors and other circuitry can be combined on the same silicon area because of the sensor's CMOS compatibility, i.e. System-On-a-Chip or SOC. In contrary, CCD requires special process steps that make it non-CMOS compatible; thus resulting in higher production cost and SOC is infeasible.

Comparison has been made between the APS and the traditional charge-coupled device. At the time this study is being pursued, APS has already captured a larger portion of the market and is sharing the profit with CCD [53]. The author believes that APS will eventually catch up with CCD's performance and secure an even larger portion of the market once more imaging processing circuitries are embedded within the same chip with the sensor.

2.5 Summary

In this chapter, we have reviewed the concept of silicon photo-detection, along with three major silicon photo-detectors in the digital imagery market – the charge-coupled device, the photodiode, and the active pixel sensor. Operations of these sensors were discussed and different aspects of the sensors were compared such as operating speed, power consumption and CMOS compatibility. Three different types of APS' were presented and they are the photodiode-type, photogate-type, and the 4-transistor photodiode-type. In the next chapter, the designs of the basic photodiode-type and the 4-T photodiode-type APS' are shown. Two novel active pixel sensors that are a modified from the basic photodiode-type and 4-T photodiode-type APS' will be presented.

3 CHAPTER THREE – EXPERIMENTAL ACTIVE PIXEL SENSOR CHIPS

Architectures of the active pixel sensor chips produced for this thesis are presented in this chapter, starting from the design of individual pixels and then going to the overview of the entire chip. The design and implementation of standard APS', including simple photodiode APS, photogate APS, and 4-T photodiode APS are discussed. Afterwards, the two new APS' will be introduced: the fault tolerant APS and the duo-output APS. Current technological obstacles related to APS will be discussed which lead to the motivation behind these two novel APS pixels. The details of the proposed pixel designs will then follow. In the last section, the fabricated chips will be presented.

3.1 Simple Active Pixel Sensor Designs

3.1.1 Design and Implementation of Simple Photodiode APS Pixel

A number of simple photodiode active pixel sensors were designed and fabricated with TSMC CMOS 0.18 micron technology in order to have a standard to compare the operation and behaviour of APS' built in this technology to that discussed in the literatures. These basic APS designs also serve as a basis for comparison with the results from the novel APS designs, which will be discussed in Chapter 5 and 6. The 0.18 micron CMOS technology is provided by Canadian Microelectronics Corporation (CMC) and the design tools, including Cadence and HSpice along with the Sun Workstations, are also provided by CMC. TSMC CMOS 0.18 micron technology is a single silicided poly, 6 metal-layer CMOS process. Operating supply voltage can be 1.8V or 3.3V. 1.8V is used for all designs described in this thesis.

Figure 20 shows the layout view of the simple 3-T photodiode APS (the circuit of Figure 14) and Figure 21 shows the microphotograph of this fabricated design in a 3x4 array.

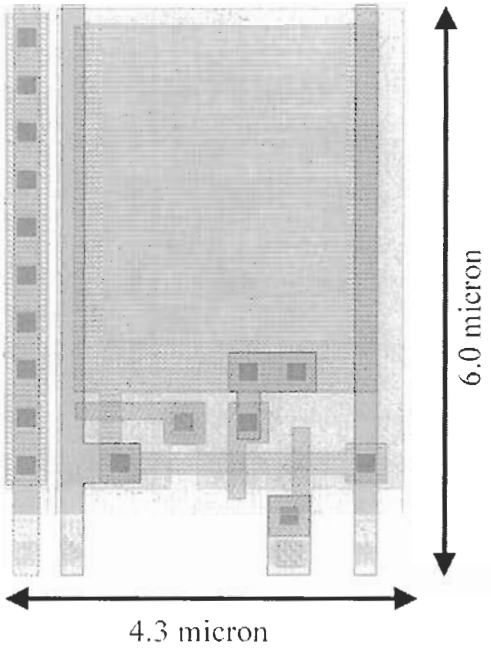


Figure 20 Simple photodiode APS layout

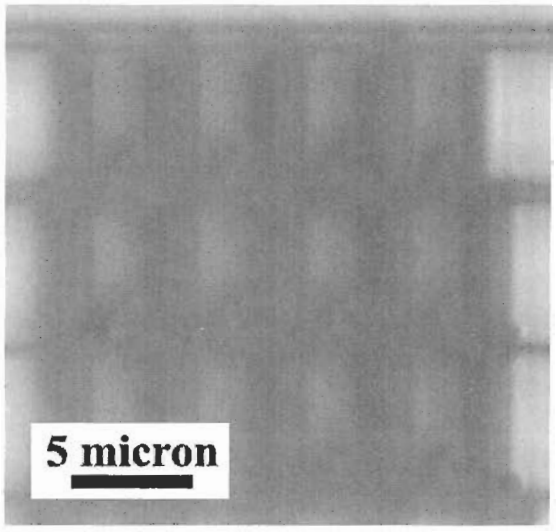


Figure 21 Microphotograph of an array of simple photodiode APS'

The photodiode APS above is designed with minimum geometry in mind, thus transistors and metal lines are minimized whenever possible. The result is a pixel with dimension 4.3μm by 6.0μm and its fill factor, i.e. the fraction of photosensitive area over the entire pixel area, is 41%. The photodiode is formed by an n-diffusion/p-sub p-n junction. A total of three APS chips were designed and fabricated. Variations of the above pixel with larger components were also made to increase yield and reliability and the size of the photodiode APS' ranges between $4\times7\mu m^2$ and $5\times5\mu m^2$.

Although the 0.18 micron technology has 6 layers of metal, only two metal layers are used for this APS pixel. The remaining higher metal layers can be used for shielding on area outside the photo-sensing element, i.e. the photodiode in this case, to reduce noise. It will be shown later that shielding is actually essential for one of the novel APS'.

3.1.2 Design and Implementation of Simple Photogate APS Pixel

An overall aim of this project was to compare these new APS designs proposed in both photogate and photodiode APS'. As this APS project was a cooperative effort with another graduate student, Sunjaya Djaja, discussion and measurements of the photogate-based APS designs can be found in his thesis, which is expected to be completed by the end of 2005. The rest of this section presents a brief discussion of the simple photogate APS.

Simple photogate APS' were designed and fabricated using TSMC CMOS 0.18 micron technology. It is important to note that the silicide on the polysilicon in standard CMOS is used to increase the conductivity of polysilicon [54]. In an image sensor, the optical response of the pixel will be drastically reduced if the silicided polysilicon is present due to its opaque property. Silicide also needs to be removed from the polysilicon for poly resistors and in this case, the same design rules allow it to be removed for higher transparency on the photogate. Therefore, the silicide is masked out from the polysilicon layer by creating a layer called resist protection oxide, or RPO layer. Figure 22 shows the layout of a photogate APS using the Figure 16 circuit and Figure 23 shows the microphotograph of this fabricated design in a 3x4 array.

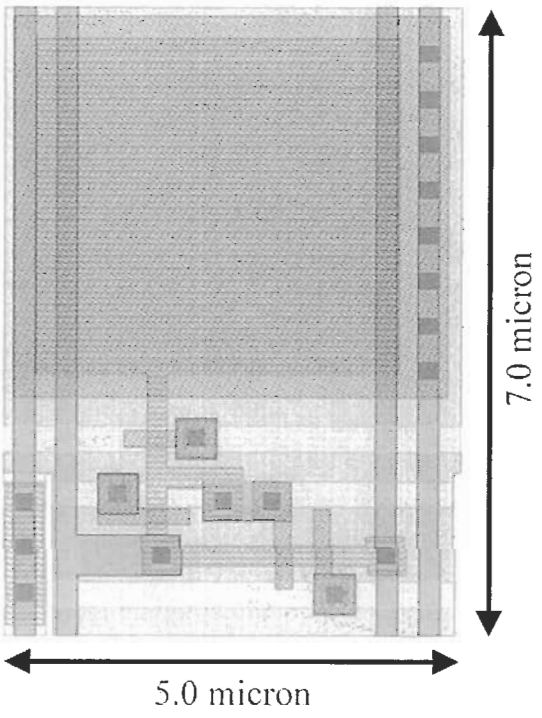


Figure 22 Layout of a simple photogate APS

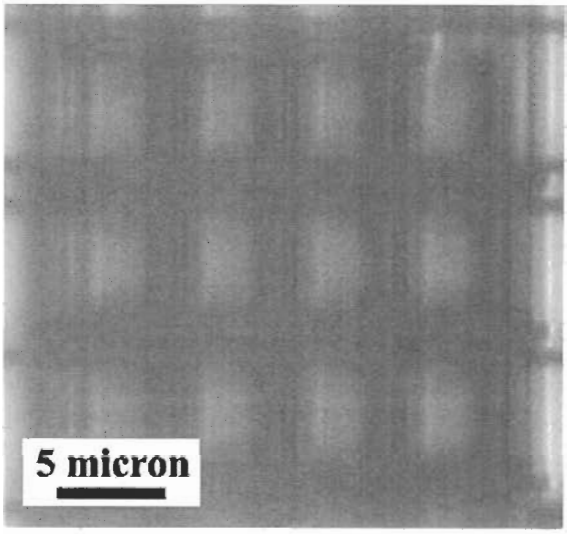


Figure 23 Microphotograph of an array of simple photogate APS'

The TSMC CMOS 0.18 micron technology is a single poly process, thus the transfer gate TX of the photogate APS is created by essentially a transistor as discussed in Chapter 2. The cross section of the photogate and transfer gate is shown in Figure 16 in Chapter 2.4.2. In case of a double poly layer process, the transfer gate overlaps the photogate area and the n-diffusion area between PG and TX would not be necessary.

The above photogate APS pixel is 5.0μm by 7.0μm and has a fill factor of only 30.6%. The relatively low fill factor is due to the design rules limiting the RPO layer, which is not shown in the layout, to be smaller than the active area. Although the simple photogate APS' and other photogate-based APS' were fabricated the rest of this paper only discusses photodiode-based APS designs.

3.2 Fault Tolerant APS

3.2.1 Defects in APS Pixel Array

As APS approaches the resolution of traditional film, the array size keeps increasing and pixel size decreasing. Thus lowering defects at fabrication time in order to keep yields high to minimize production costs becomes one of the primary concerns in digital imaging. Moreover, the increased pixel density and pixel count reduces reliability over the imager's lifetime. This problem is especially important in harsh environments such as high-radiation conditions (e.g. outer space or in military application), where replacing a sensor is difficult or impossible.

Defects in the APS are an extension of those in traditional microelectronics circuits. First, there are the expected electrical defects in circuits such as opens or shorts within the pixel. In addition, an electrically defect-free APS can also be defective due to optical problems such as metal blobs covering the photo-detectors or packaging defects. Furthermore, defects in APS can be caused by wafer imperfection, cleanroom contamination, and numerous flaws during fabrication and degradation over time (e.g. radiation induced charges). In general, defects in APS with respect to the output are categorized into three groups: optically Stuck Low (SL), optically Stuck High (SH), and low sensitivity.

Optically stuck low refers to the pixel that always has a low output, i.e. a dark spot (very low in detected signal value). Electrically, as an example, this is equivalent to the gate of the readout transistor shorted to VDD. Stuck lows could also be due to the photodiode area being blocked by a particle, the photodiode or readout transistor gate connected to VDD, the reset transistor always on, or source and drain of readout transistor shorted.

Optically stuck high refers to the pixel always reading a high signal, i.e. a bright spot (near saturation light intensity). This is electrically equivalent to the gate of the readout transistor shorted to ground. Stuck high could be due to photodiode malfunctioning or not fully formed, a

readout transistor gate shorted to ground, reset transistor always off, or source and drain of readout transistor opened.

A pixel with low sensitivity produces a less than expected signal for a given light level. This can be caused, for example, by a leaky diode, the photodiode partially blocked by a particle or remnant from other layers during fabrication. Figure 24 below illustrates effects of different optical defects on a sample picture.

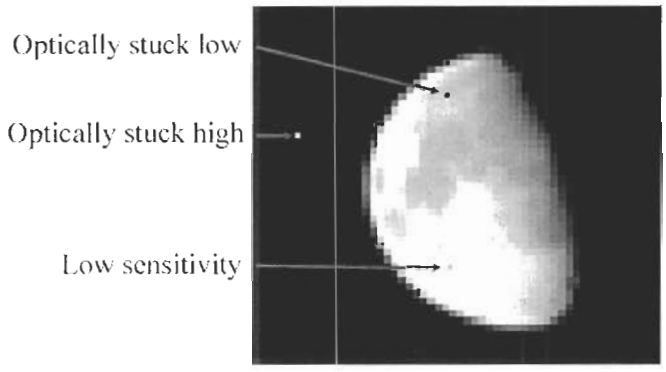


Figure 24 Results of optical defects in pixels

Although defect correction by software such as interpolation and averaging from surrounding pixels have been used [55], they are not satisfactory because, under many conditions, they give faulty information. To overcome this, a fault tolerant APS was devised by Chapman and Audet in 1999 [5] and simulated in 2001 [6]. It incorporates hardware redundancy by splitting a normal APS into two parallel operating halves with very little additional area cost. The desired yield improvement is obtained, as shown from simulations, since the probability that both pixel halves will fail over a long time of operation is low [7].

It is important to note that in the rest of this thesis, stuck low and stuck high refer to the optical behavior, stuck low being no optical signal being detected and stuck high being optical signal saturating the pixel. If correlated double sampling is performed to find the difference between the output during reset and that at the end of the integration, both a stuck-low pixel and a

stuck-high pixel would see a dark spot as the output signals are not modulated by the light intensity.

3.2.2 Yield Analysis and Pixels

One of the main advantages of the fault tolerant APS is to increase the die yield of image sensor chips, i.e. the number of fabricated dice on a wafer that successfully meet the minimum test requirements. Yield of any particular chip design is closely related to the cost of production. Cost drops when the yield of a design increases because the cost does not vary with yield. The most common defect on imaging arrays are point-like defects, i.e. error of size that is comparable to the minimum feature dimension (e.g. broken lines, via failing, etc). Assuming a single die area is A. In a simple yield model using a Poisson distribution, the number of defects per unit area is give by λ. The yield, Y, can be formulated by [56]:

$$Y = e^{-\lambda A} \tag{18}$$

For a given technology, as the pixel count in an imager increases A increases. Thus the yield decreases rapidly. As technology scales down, the pixel count can be increased with A held unchanged but λ is generally higher. The value of λ depends on the maturity of the technology and the defect density and thus λ usually higher at the early stage of the technology and therefore yield is lower. As the technology matures, fabrication processes can be controlled more precisely, thus λ is decreased and yield is higher.

3.2.3 Design and Architecture of Fault Tolerant APS

A fault tolerant APS introduces redundancy by dividing a normal APS, as shown in Figure 14 in Chapter 2, into two halves operating in parallel. Each component can be split into two, including the photo-sensing area, reset transistor (M1), output transistor (source follower, M2), and row select transistor (M3). Figure 25 shows a schematic diagram of a fault tolerant APS that has two photodiodes PD.a and PD.b, two reset transistors M1.a and M1.b, and two

readout transistors M2.a and M2.b. In this particular design, the row select transistor is not split into two although it can be done as well.

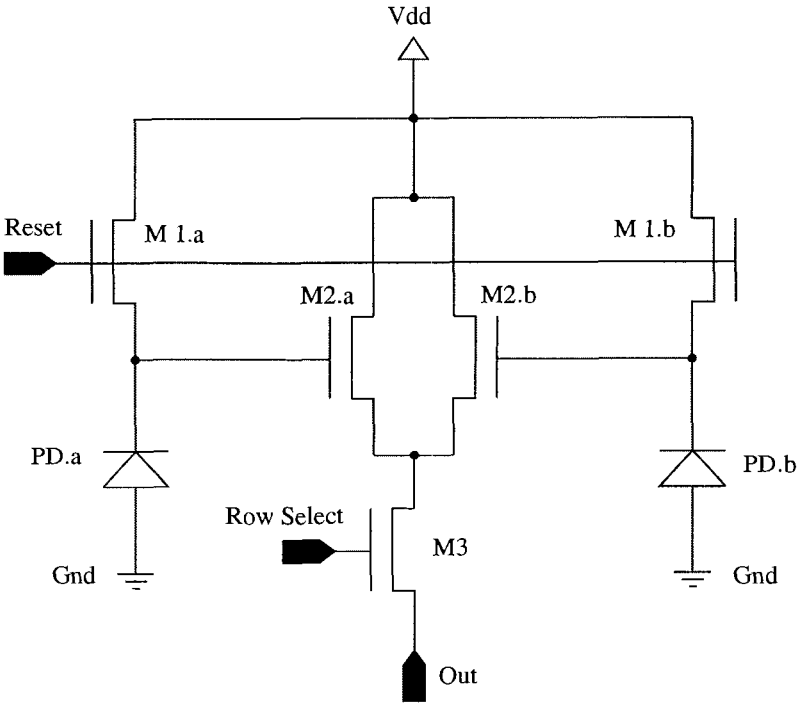


Figure 25 Fault tolerant APS schematic

As a result, PD.a, M1.a, and M2.a form one half of the APS while PD.b, M1.b, and M2.b form the other half. The row select transistor is not split and it is shared between the two halves. Each side behaves as a sub-pixel and operates in parallel but independent of each other. When there is no defect, the parallel operation results in the APS behaving, in principal, the same as an unsplit APS. The reliability of the pixel is increased because if one of the two sub-pixels fails, the other half is still functional and it is less likely that both will fail simultaneously [7]. This is half sensitive because it is able to detect half of the pixel illumination. The original signal can then be recovered by calibrating the output value, a multiplication of two. This multiplication of two is easily accomplished in digital systems as it is a simple left shift by one.

It is important to point out that this FTAPS operates in a slightly different way than regular APS'. Instead of a load at the output created by a bias transistor, both halves of the

FTAPS operate in current mode, in which the currents of the two APS halves are combined at the output. The total current is output to a current-to-voltage converter (I-V converter) off chip and the voltage can be recorded. The total change of current before and after integration indicates the light signal level. If one of the two halves is stuck at high or low, the total change of current will be halved. This is the reason why a multiplication of two of the output value can retrieve the signal and therefore a bias transistor, shown in M_{BIAS} in Figure 14, is not necessary for this design.

Comparing this FTAPS to a simple APS, many point defects in a simple APS would destroy the entire pixel. By comparison for a single defect, the FTAPS is functional with recoverable state thus resulting in a more reliable pixel design. However, this is obtained at the cost of extra transistors hence reducing fill factor. Figure 26 and Figure 27 below show the layouts and microphotographs of the fault tolerant APS, which have been designed and fabricated in TSMC CMOS 0.18 micron salicide technology.

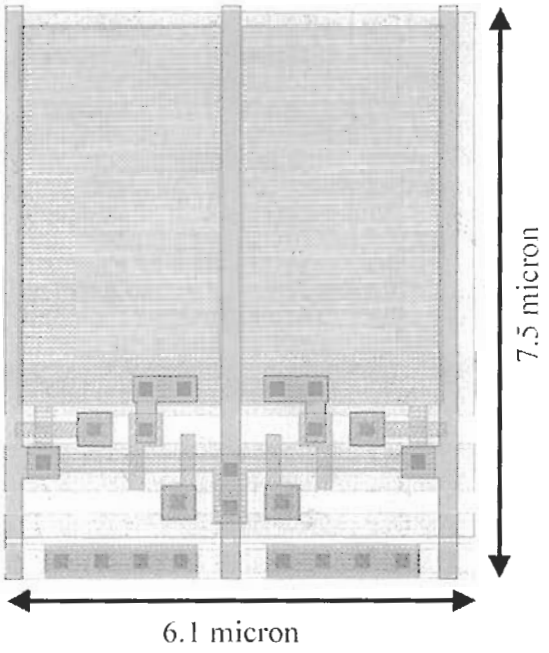


Figure 26 Fault tolerant APS layout

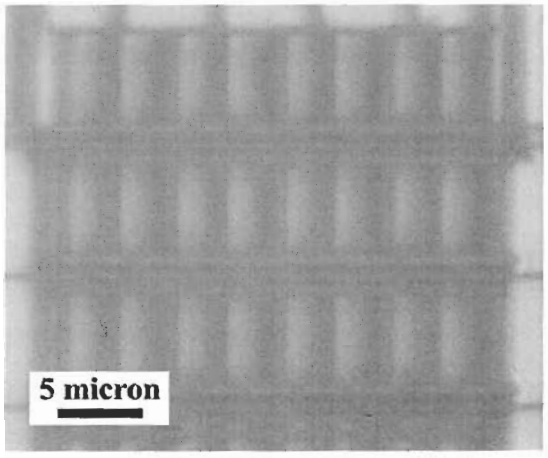


Figure 27 Microphotograph of an array of fault tolerant APS'

Although the fill factor of the fault tolerant APS is 44.2%, which is larger than that of the simple photodiode APS, it should be noted that the increase in fill factor for the fault tolerant APS comes from the increase in total pixel area in this particular design but not from the introduction of redundancy. Moreover, in this design, we did not try to minimize the pixel size, which might reduce the fill factor. Previous study has shown that the expected reduction in photo-sensing area for the fault tolerant APS is only approximately 6% [7].

Previous simulation, implementation, and experimentation of fault tolerant APS have also been investigated by Djaja and Chapman [45]. The emphasis on that investigation was at the pixel level, whereas the operation at a system level is the focus here.

3.2.4 Defects in Fault Tolerant APS

The concept behind the fault tolerant APS is that as defects are commonly quite small, they will only affect one half of the parallel operating pixel, resulting in half the pixel still being sensitive. Since the probability of defects is low to begin with (e.g. less than 1 or 2 pixels in a million currently), standard wafer yield calculations show that the chances of both halves failing are extremely small [57]. For example, if simple binomial probability was employed, the probability of one half failing is p, and then the probability of both halves failing is approximately p^2. As noted, a pixel's signal can be recovered from the operating half, after compensating for the changes created by the defective half. For example, if the probability of defective pixel in an array without fault tolerance is five in a million (i.e. 5 defects per mega-pixel or 5×10^{-6}), the probability is reduced to 25×10^{-12} with fault tolerance, which implies no defect in most chips.

In order to identify all the defects described above in a fault-tolerant APS array, dark field illumination and light field illumination calibration images are used [57]. Identical to the ideas shown in Figure 24, exposing the entire APS array to no illumination will identify the completely stuck high pixels that output a high value as if they are detecting bright light. Half optically stuck high pixels will output a medium value (grey spot), again easily seen against the

black image. Similarly, by exposing the entire APS array to a uniform high light illumination, every pixel is nearly saturated and should output a high value (bright spot). Any pixels that output near zero values (dark spot) are completely stuck low and malfunctioning. Pixels that output medium value (grey spot) are half optically stuck low or have low sensitivity.

In this thesis, small arrays of FTAPS were fabricated and tested so that they can be compared to the simple photodiode APS. While some FTAPS pixels are designed to operate normally, some were designed with defects added including stuck-high and stuck-low defects. With injected defects, the behaviour of defective pixels could be measured, corrections (i.e. multiplication of two of the output signal) could be made and the results compared to the non-defective FTAPS outputs. Besides electrically injected defects, optically induced defects were also created using a laser and microscope light source (see Chapter 5). Characterization of these different defective FTAPS' as well as the non-defective FTAPS were carried out. Chapter 5 will present the experimental results for the FTAPS from the fabricated sensors and Chapter 7 will compare the results with simulations.

3.3 Duo-Output Photodiode-Based APS

Integrated scanning systems are utilized in many industries to detect optical signals. These applications include 3-dimensional profile scanning, food or material processing, animation or movie production, and more. 3D profile scanning usually involves the use of laser(s), a linear optical detector array, an optical lens system, and signal processing to map out the profile of an object. The detection is based on optical triangulation shown in Figure 28 below.

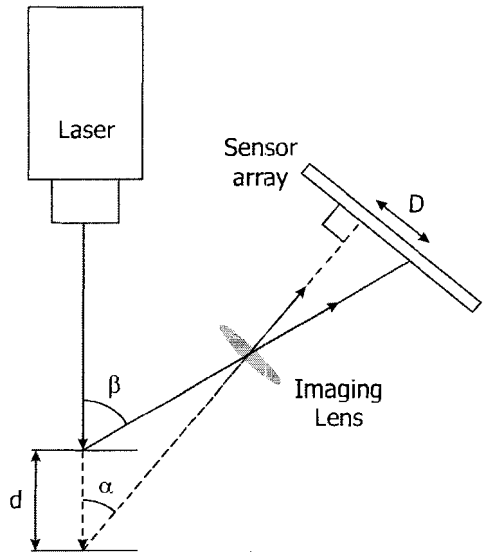


Figure 28 Optical triangulation after Oh et al. [58]

The laser signal is projected on an object, which reflects the laser source to an optical detector array through an imaging lens. As the distance of the object changes relative to the light source, the reflected beam lands on different locations of the sensor array, as it is shown in Figure 28. By identifying the relationship between the distance and the position of the spot position, the location of the lighted spot can be identified. As the object to be scanned is moved progressively relative to the laser source, the profile of the object can be obtained.

Another example used in movie or animation production, involves the use of a camera to detect the natural movement of real human beings or animals. The sequences of the movement are then used to form the artificial beings such as robots in movies or human beings in animations. The detection is usually carried out by sensing and recording the movement of coloured dots that are attached to the major joints of a human being or an animal. The acquired data is then processed by computers to yield positions with time. Robots can then be created and special effects or computer graphics can also be generated to mimic the reality as closely as possible.

3.3.1 Current Optical Scanning Technology

One of the major problems of optical sensing in the above applications is the background illumination and variation in object surfaces, causing noise. Since optical sensing relies on reflected light from a surface that is being sensed by optical detectors, disturbance arises from the illumination changes in the environment where the operation takes place. Background light sources exist unless the operation takes place in an absolutely dark area tightly shielded from any light or in an area where light is well controlled, both of which are usually impractical or inconvenient. Noise could also be due to the intrinsic characteristics of the object being scanned. For example, a shiny spot on a surface with high reflectivity can reflect more background light than the rest of the area and is falsely picked up by the optical detector as an optical signal. An example of false detection in laser profile scanning is illustrated in Figure 29 below.

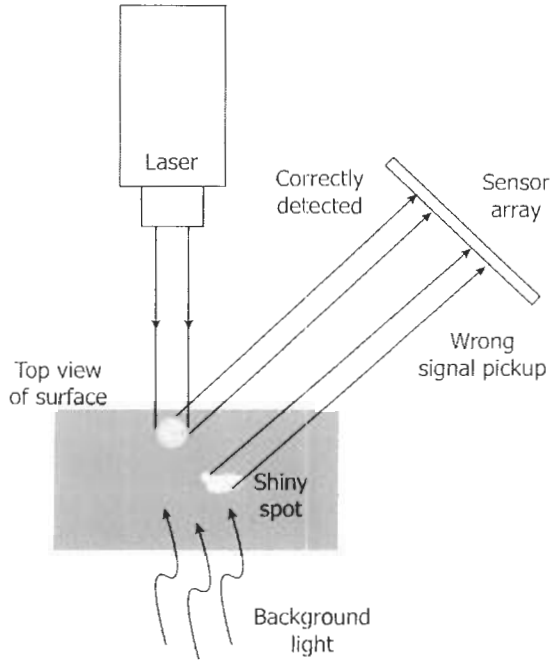


Figure 29 Incorrect recognition of laser spot on a shiny surface

On the other hand, a defective area on a surface, such as a dark spot or hole with low reflectivity, could absorb most of the light illumination on the spot. The optical detector would then have difficulty registering the spot even if a laser is present, as shown in Figure 30 below.

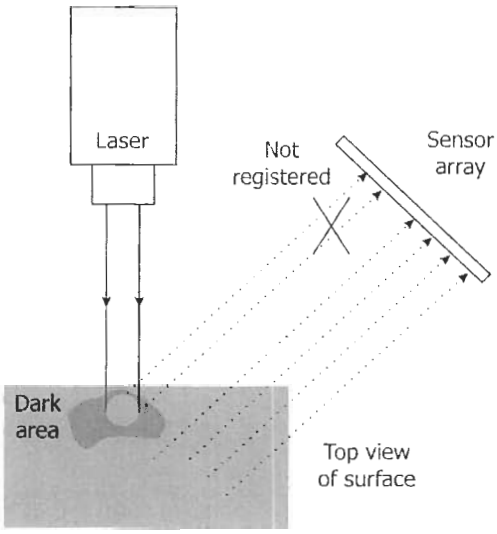


Figure 30 Laser signal lost due to a dark area

In some cases, increasing the optical power will increase the signal-to-noise ratio but it is not always feasible. In the case of a laser, there is a maximum allowed limit on the power for safety reasons, which is only 0.5mW or about sunlight level. Moreover, a high power laser could possibly alter or damage the object being detected. Typically assuming background light levels were of a constant power level, the sensor array detects rising and falling edges of light intensity to locate the laser spot. However, there are many errors if the surface of the sensed object is not of constant reflectivity or if the background light level is constantly changing.

Charge-coupled device has been the major technology used for the detector in these integrated scanning systems and the above mentioned problems have yet to be solved in CCD. Active pixel sensor has been investigated recently as a possible solution to the problems faced by CCD but by far, APS has not shown an advantage over CCD. APS does show an advantage of higher operating speed but the relatively small linear array required in some applications suggests that speed is of secondary importance compared to the accuracy advantage in CCD.

3.3.2 Background Elimination Concept

In the hope of solving the above problems, this chapter proposes a novel active pixel sensor design that introduces an extra output path to the original shuttered (or 4-T) photodiode APS, as shown in Figure 19 in Chapter 2.4.4. Except the photo-sensing element (photodiode), every transistor in the original 4-T APS, i.e. reset transistor, enable transistor, readout transistor and row select transistor, is replicated to provide an extra output path. The result is the Duo-output APS (DAPS), an APS that has two output paths. This additional output node, along with the additional shutter, allows charge to be integrated separately on different sides during different phases of an integration cycle. When the laser is synchronized with the shutters, background light alone can be separately integrated and readout on one side of the DAPS when the laser is off, the "OFF phase". This signal is then subtracted off from the readout signal on the other side integrated over the other phase of the integration cycle when the laser is on, the "ON phase". This discrepancy results in an elimination of background illumination at the output. Figure 31 illustrates the concept of background elimination, showing the timing diagram of the reflected light intensity from an object for both the ON phase and OFF phase of a cycle.

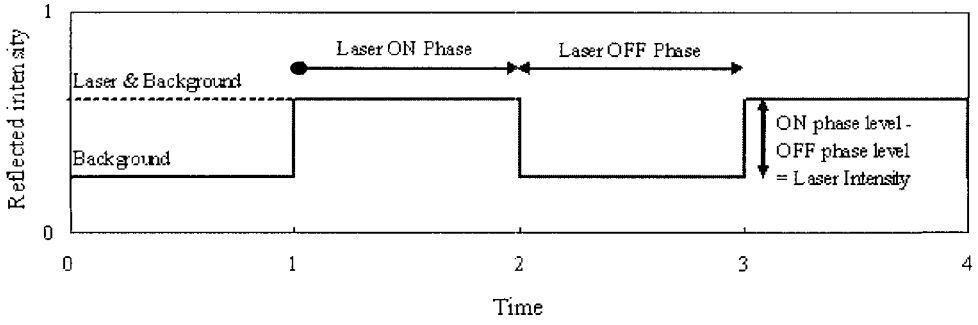


Figure 31 Timing diagram illustrating the reflected light level from an object during the ON phase and OFF phase of a cycle

The important point to note is that, with standard APS, it is possible to carry out an ON phase reading and store the output temporarily and then carry out an OFF phase reading before the difference is computed. However, since the reflected background light signal changes rapidly,

it is critical to read the foreground and background signals with minimal time separation. This can be achieved easily with two sides on a pixel but it would be much more difficult if one pixel were to perform an entire readout twice.

3.3.3 Design and Implementation of 4-T Photodiode APS

The only difference between a 4-Transistor (4-T) photodiode APS and a simple photodiode APS is the extra enable transistor added between the photodiode and readout transistor. As it was described in the previous chapter, this enable transistor acts as a shutter to control the transfer of charges stored in the photodiode to the readout transistor. The schematic of the 4-T PD APS is shown in Figure 19 in Chapter 2.4.4. Figure 32 below shows the layout of a 4-T photodiode APS pixel design.

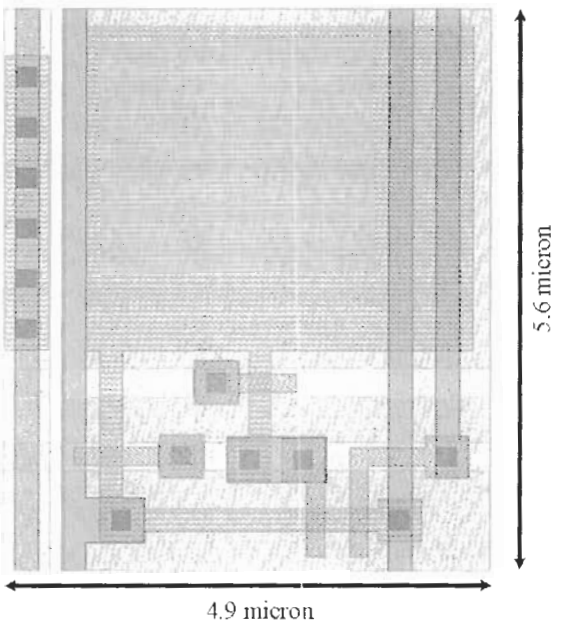


Figure 32 Layout of a 4-T photodiode APS

The above 4-T photodiode APS has a dimension of 4.9μm by 5.6μm and a fill factor of 36%. It can be seen near the center of the pixel that an extra transistor acts as the transfer path between the photodiode and the output transistor. The area of the pixel is larger than the simple

photodiode APS, thus it is difficult to calculate the area cost of the extra enable transistor in the 4-T transistor. An estimate is a reduction in fill factor by 7-10%, which is in fact unimportant because the APS is arranged as a 1-D sensor array.

This 4-T APS serves as a basis for the duo-output APS because it is simply the single output version of the DAPS. Since the 4-T APS is a standard shuttered pixel, this pixel will be used to compare to the design and testing of the DAPS. In fact, the DAPS can operate as a simple 4-T APS when one of the two shutters is disabled. In Chapter 6, the DAPS will be first tested with only one side enabled before both sides are enabled for background elimination.

3.3.4 Design and Architecture of Duo-Output APS

Duo-output APS utilizes the shutter mechanism of the 4-T photodiode APS discussed in Chapter 3. The concept of the DAPS is to use two shutters to control the readout of a single photodiode to two output nodes. In any given operating cycle, there are two phases and each of them is dedicated to integrating the signal for one of the two nodes. In the first phase of a cycle, the signal from the photodiode is read and stored in the first node. In the second phase of the cycle, the signal is read and stored in the second node. If a synchronized light source is turned on during only the first phase while there is only background illumination during phase two, there will be a difference in the two outputs at the end of a cycle. The differential output subtracts the background illumination from the sum of the desired signal and the illumination in phase one, thus background illumination elimination is achieved. Subtraction of one signal from the other can be done with a difference amplifier. Figure 33 shows when the two sides of the DAPS are enabled during different phases of an integration cycle. The remainder of this section discusses the design and architecture of this duo-output APS.

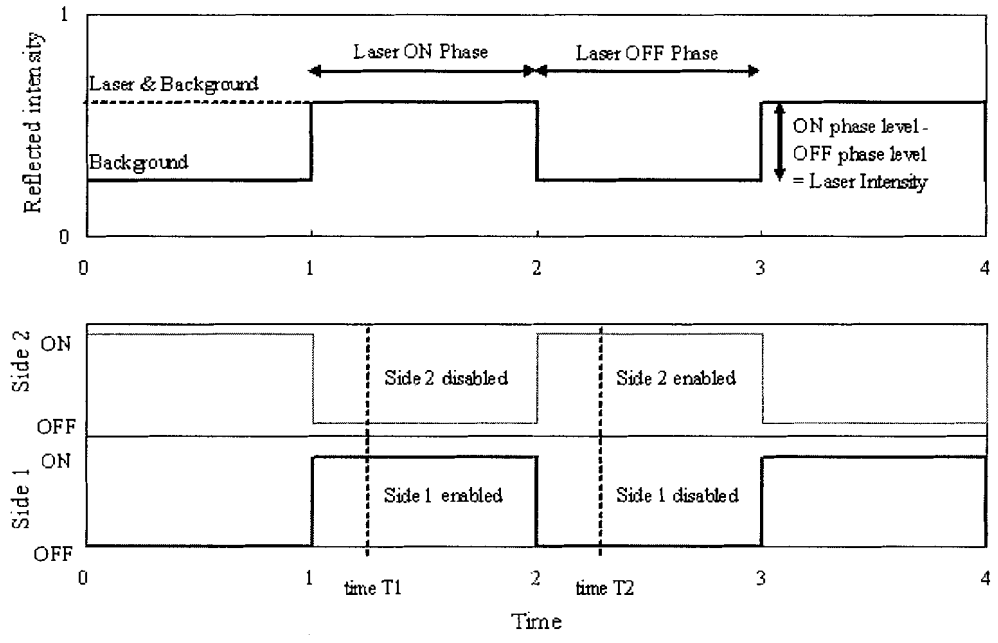


Figure 33 Timing diagram illustrating side 1 and side two of the DAPS enabled at different time to read signal at different phase for background elimination

By duplicating everything except the photodiode of the shutter 4-T photodiode APS, we create a duo-output APS, in which the two shutters (or enable transistors) control the output direction of the photodiode signal. Figure 34 below shows the schematic of such APS.

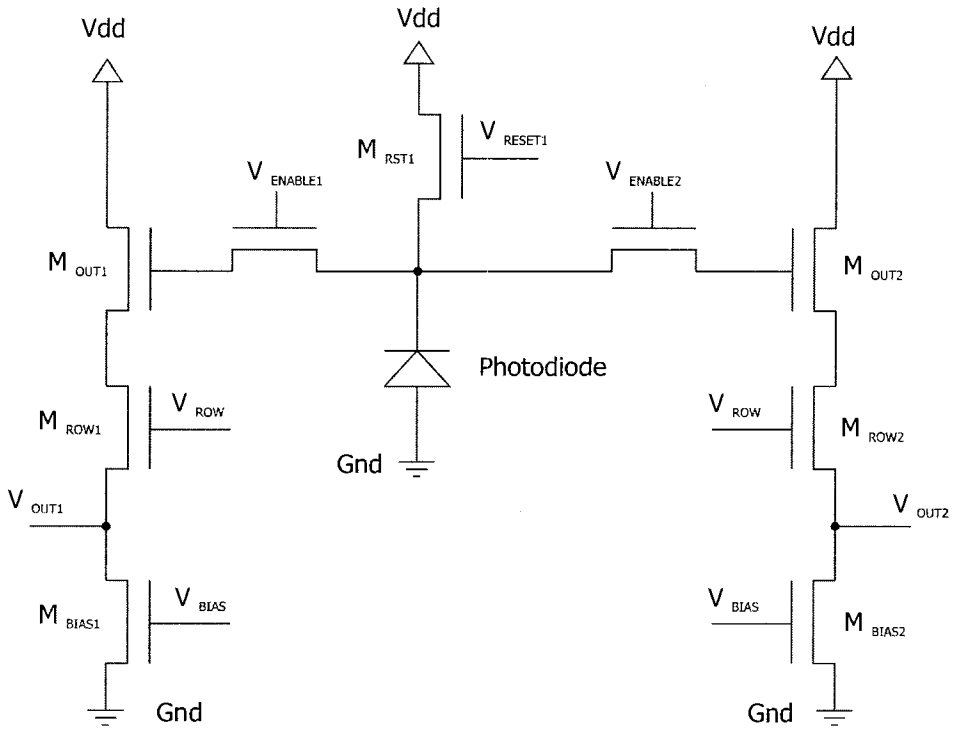


Figure 34 Schematic of a duo-output APS

This schematic is similar to the schematic of the fault-tolerant APS. Instead of splitting every component of the APS including the photodiode, only the transistors M_{OUT}, M_{ROW}, M_{BIAS}, and M_{ENABLE} are duplicated to form M_{OUT1}, M_{ROW1}, M_{BIAS1}, and $M_{ENABLE1}$ on one side of the photodiode and M_{OUT2}, M_{ROW2}, M_{BIAS2}, and $M_{ENABLE2}$ on the other side. Each side behaves as an independent output source follower with the photo-sensing element shared between the two sides.

Only one of the two shutters is turned on at any instant such that only unidirectional integration of photo-generated charges is allowed, either to the left or to the right. The shutters and the optical source can be synchronized as they both belong to a single system unit. Figure 33 has already illustrated conceptually when side 1 (i.e. enable 1) and side 2 (i.e. enable 2) are turned on during an integration cycle. Figure 35 and Figure 36 below show the layouts and microphotographs of a duo-output APS, which have been designed and fabricated in TSMC CMOS 0.18 micron salicide technology.

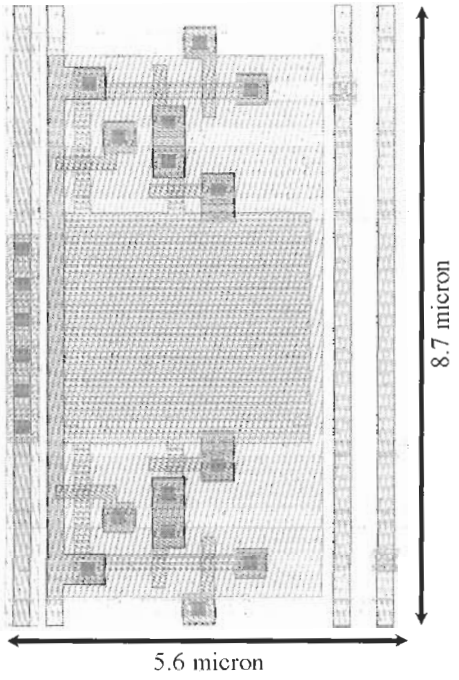


Figure 35 Layout of a duo-output APS

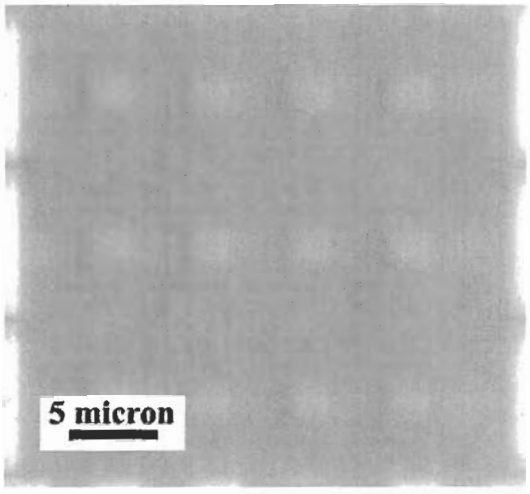


Figure 36 Micrograph of an array of duo-output APS

It can be seen that the lower half of the DAPS pixel is identical to the 4-T APS with an enable transistor (shutter) at the mid-bottom of the photodiode. The circuit above the photodiode is simply a mirror image of the bottom half. The pixel has a dimension of 5.8μm by 8.7μm and a fill factor of 14%. Although the fill factor is low compared to other normal APS', the intended application of this sensor is typically arranged in a linear array and does not require high resolution. Several variations were designed and fabricated. Some have a larger total area with higher fill factor and some have larger transistors.

Small DAPS pixel arrays were fabricated but only individual pixels were tested. Both a laser and LEDs are used as the light input to the pixel and these input signals will be synchronized to the DAPS pixel. LEDs allow flood illuminating of the entire pixel area while a focused laser beam allows the input signal to be confined to only a small area on the pixel. One side of the DAPS will be disabled so that the other side will operate identical to a 4-T APS. The

ultimate objective of this thesis is to use the DAPS to eliminate background signal and utilize this pixel in different applications such as profile detection using laser. Therefore, eventually a larger linear array will be fabricated and tested with laser to demonstrate the application of this sensor in various ways.

Chapter 6 will present the experimental results for the DAPS from the fabricated chips and Chapter 7 will compare the experimental results to simulations.

3.4 Design and Implementation of APS Chips

Since the objective of the project is to test and characterize the behaviour of several novel APS test structures; only 1-dimension or small 2-dimension arrays are fabricated. Each chip has a number of different designs including those discussed in the last several sections and they are arranged in columns, thus each row has identical APS design. Figure 37 below shows the layout of the entire chip area.

Three chips have been fabricated using TSMC CMOS 0.18 micron salicide technology provided by CMC. All three chips are 1.5mm by 1.5mm in size (see Figure 37), which includes bonding pads, the necessary I/O support ring, decoders, analog multiplexers, and standalone test structures. The bonding pads allow bonding wires to be bonded to the package. The I/O ring provides power supply and ground to the core of the chip and to other I/O cells forming the ring itself.

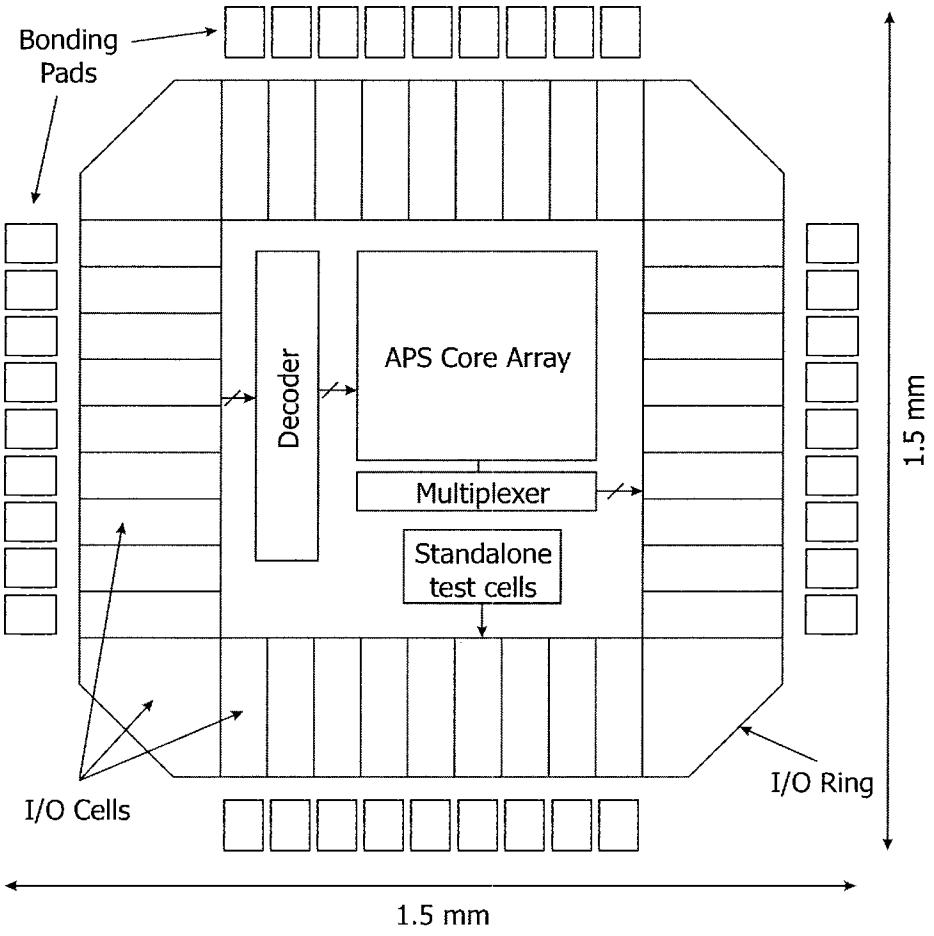


Figure 37 Overview of a 1.5mm by 1.5mm APS chip

Two decoders are implemented within the decoder block. The 6-input-64-output decoder is used to select one of the 64 rows of pixels at a time by turning on the row select transistor of an entire row of APS cells. The 3-input-8-output decoder provides the input to the multiplexer to select a subset of columns to be output to the output pads.

Within the APS core array, test structures of many different active pixel sensor designs are arranged such that each row consists of the same design and each design has several rows. The output of each column goes directly to the multiplexer. Besides the core array, an extra small array of standalone APS cells is included in all three designs so that if any of the decoder, multiplexer, or the core APS array fails to operate, a small array can serve as the backup to be

tested. Figure 38 and Figure 39 show an example of one of the three Cadence chip layout and the microphotograph of this fabricated chip.

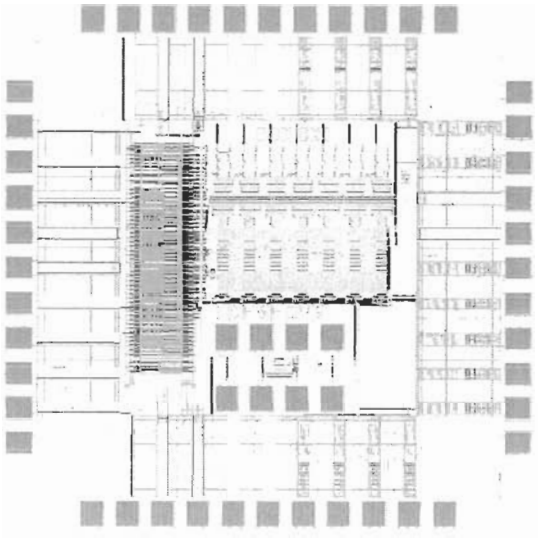


Figure 38 An APS chip layout view

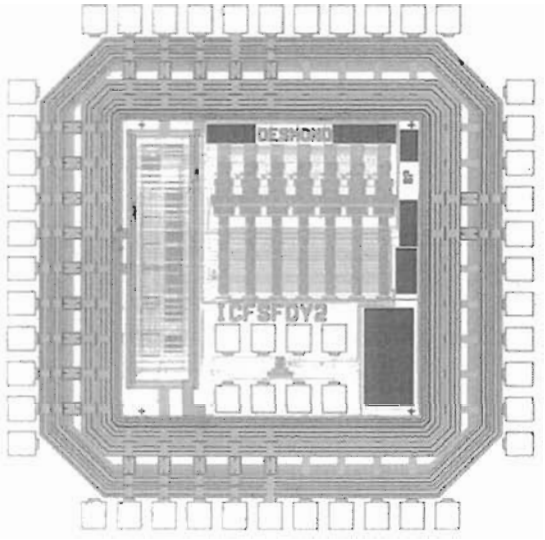


Figure 39 Microphotograph of a fabricated APS chip

It can be seen from the fabricated view that the IO cells form a ring around the peripheral of the chip area. Blocks of black area in the fabricated view are dummy metal fills that are added on the empty area to meet the minimum required amount of metal or polysilicon present on the chip area. This requirement ensures that the topographical thickness variation of the chip area is minimized during chemical mechanical polishing in the fabrication process.

Among the three chips designs, most of the tests discussed in this thesis were mainly performed on the third chip and one of the other chips designed by another graduate student, Mr. Sunjaya Djaja. The first chip was used for some other APS tests, which are not discussed in this thesis. Design errors in the second chip prevented us from extensive testing. Improved APS designs were made and submitted by other graduate students but these chips are not available in time for testing.

3.5 Summary

This chapter has discussed the designs of simple APS' and has introduced two novel APS'. One of the two novel APS', the fault tolerant APS (FTAPS), demonstrates a way of increasing fabrication yield by splitting a normal photodiode APS into two sub-pixels. The reliability of the pixel thus increases because if one of the two halves fails, the optical signal can be retrieved by the doubling the output from the second half of the pixel that remains working. The second novel APS introduces a method of eliminating background illumination from a foreground optical signal by using a duo-output APS (DAPS). A DAPS consists of two output paths, one that outputs the detected signal when both the desired signal and background illumination is present and another one that outputs the signal when only the background illumination is present. The active pixel sensor chips that were designed and fabricated using CMOS 0.18 micron salicide technology were also illustrated. In order to test both of the novel APS' on the chips, LEDs and an argon laser are used. The following chapter will discuss the setup for testing the fabricated sensor chips using LEDs and the laser.

4 CHAPTER FOUR – EXPERIMANTAL SETUP

Testing of our APS chips is different from the generic methods as we are interested in the behaviour and performance of individual pixels. Testing image sensors usually involves using a lens system to focus structured images on the APS array. After capturing the picture, an image signal processor manages the raw information and outputs the results for easy interpretation. The objective there is to see how well the sensor reproduces the image. However, this thesis looks at a couple ways of injecting faults into APS cells or differentiating pulsed illuminations from the background lighting. In our experiments, focused laser or pulsed light emitting diodes are used as the major light sources. The outputs from only several pixels and their behaviour during the whole illumination cycle are of interest. Processing of the raw data is performed with spreadsheets so that the output signal level can be monitored at any given time.

This chapter discusses the experimental setup for the active pixel sensor chips. This includes how the APS chips are connected to the computer which in turn generates the control signals. It also includes the experimental setup for two different optical signals that are used as the optical inputs to the sensors – a laser and light emitted diodes.

4.1 APS Chip Electrical Setup

Fabricated active pixel sensor chips were received from CMC, packaged in 40-pin DIPs. During testing, packaged sensor chips are mounted on breadboard in the laser or LED illumination setup, as shown in Figure 40. A computer with LabVIEW® program written by a post-doc researcher Dr. Chenheng Choo with two signal acquisition/controller boards (PCI-6024E and PCI-6713) supplies the power, row/column addressing, and the timing control signals to the APS chip. The output of the APS chip is captured by a digital storage oscilloscope as shown in Figure 40 below.

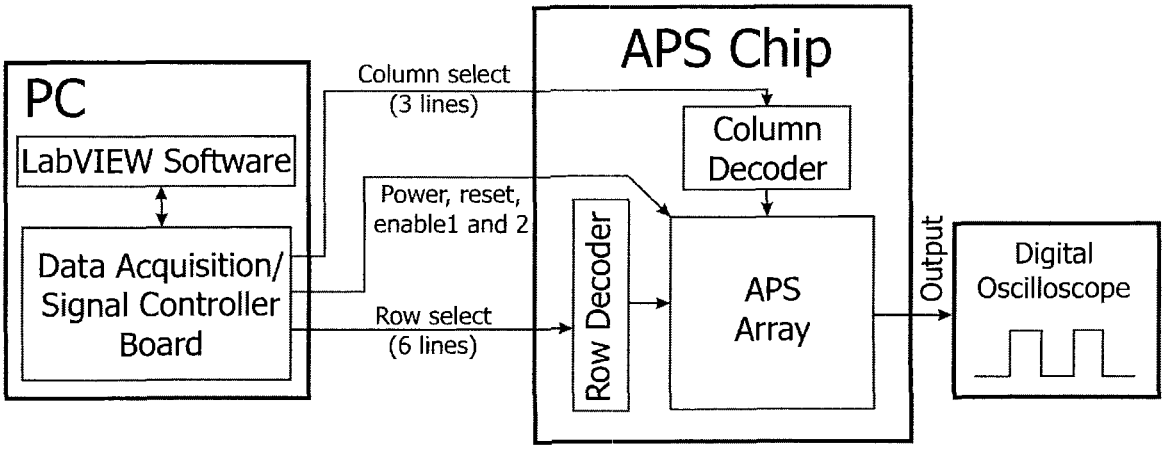


Figure 40 Test setup for APS chips

There are a fixed number of analog and digital control signals on the two controller boards. The LabVIEW program dictates how these output signals behave. Since all APS chips that are under test require a 1.8 supply voltage, the 5V TTL digital signals from the boards need to be voltage divided to provide sufficient input controls to the chips. Voltage dividers are arranged on breadboards.

4.1.1 LabVIEW program

Figure 41 shows an example of the LabVIEW main control window for the testing of the APS chips. Different panels from the program are dedicated to different functions. In this main control panel, the graphical user interface allows the main power supply and the reset signal to the chip to be separately controlled so that they can be manually switched on or off at various times. From experience, we found that the order of the signals being switched on and off is important to the lifetime of the chip. To prevent power related damage, a green light on the power supply button indicates when the power is turned on, as shown in Figure 41.

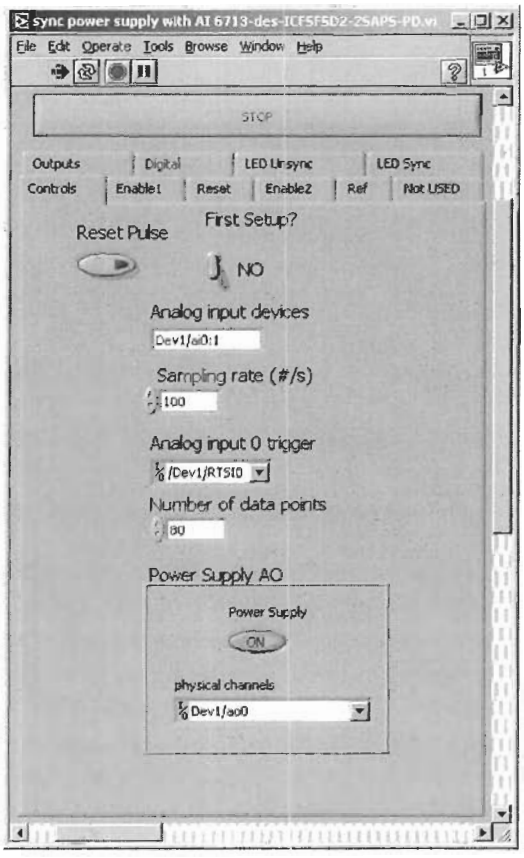


Figure 41 Screen capture of the LabVIEW main control window for APS experiments

Since the APS chips are mixed-signal designs with everything analog except the two digital decoders, all the inputs to the decoders on the sensor chip use the digital outputs from the data acquisition boards (8 from PCI-6024E and 8 from PCI-6713) while the remaining signals, i.e. the enable gates (TX1 and TX2) and reset, uses the analog outputs (2 from PCI-6024E and 8 from PCI-6713). During testing, once the reset signal is turned on, it triggers both the enable gates. LabVIEW then generates these signals to the chip continuously until it is notified to stop. The column and row selects are controlled manually and they can be changed on the fly while the program is running. In some of the APS chip designs, the decoders can be totally disabled such that they do not output any high signal regardless of what the inputs are. Figure 42 below illustrates the LabVIEW window where the decoder inputs can be changed and the enable buttons to the two decoders.

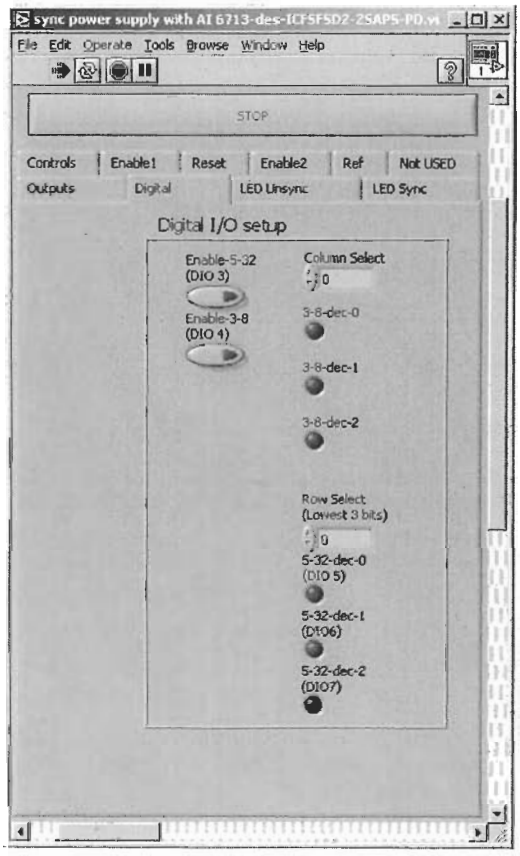


Figure 42 Screen capture of the digital controls for the row and column address decoders and their enable buttons

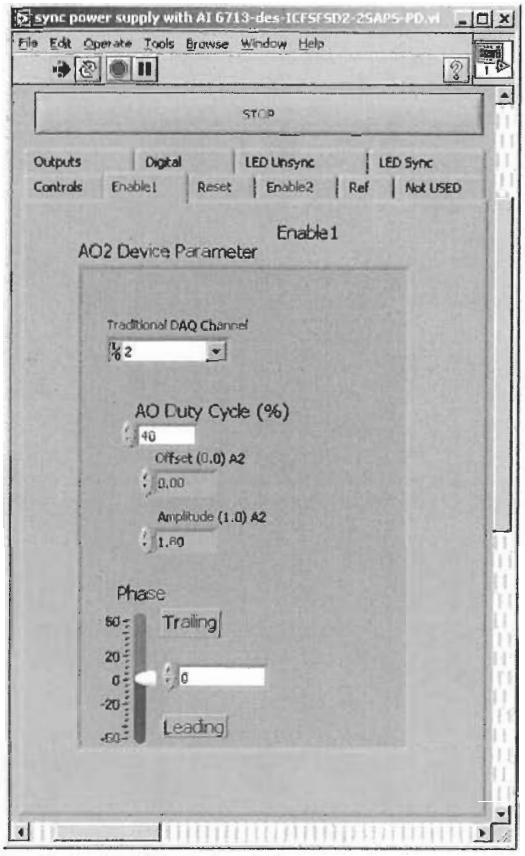


Figure 43 Screen capture of the control for an analog output showing the different parameters that can be adjusted

Figure 43 shows one of the controls to the analog lines, the enable 1 in this case. The duty cycle (%), amplitude (Volt), offset voltage (Volt), as well as the phase of the signal can be adjusted. The values of the row and column decoders can be modified on the fly while the program is running. Since the analog signal involves a much more complicated procedure, the program needs to be stopped and restarted every time when one or more parameters of the analog control is changed. The chip must be powered down during changes, otherwise it can be damaged.

4.1.2 Data Capture with the Digital Oscilloscope

Due to the need to capture detailed response from various signals, the outputs of the APS chip are connected to a 4-channel digital oscilloscope (Tektronix TDS2014). Figure 44 below shows a screen capture of the oscilloscope displaying the reset signal and the outputs of two APS pixels. The top curve is the reset signal while the two curves at the bottom almost overlapping each other are the outputs from two APS pixels. It can be seen that during each of the two periods of the integration cycle, the reset goes high to reset the output node and then goes back to low to allow integration of light, leading to a voltage drop at the outputs.

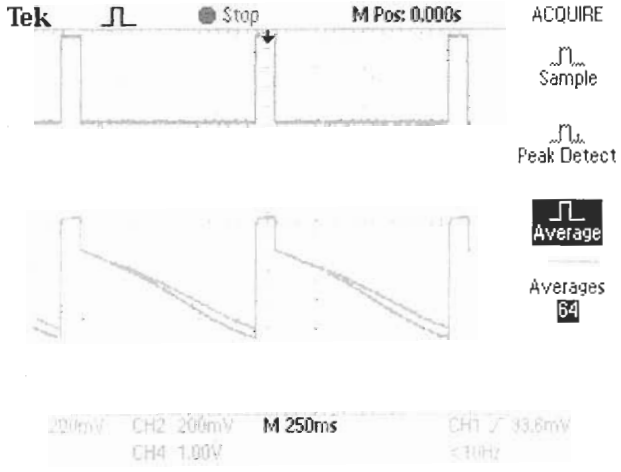


Figure 44 Example of the screen capture on the digital oscilloscope

The digital oscilloscope has a bandwidth of 100MHz and a sample rate of 1.0GS/s. In each channel, 2500 points are being recorded. The digital oscilloscope also includes an add-on to the Microsoft Excel® that allows data to be transferred from the oscilloscope and automatically plotted in Excel.

4.1.3 Wiring

Initially, connections between the chip and the PC were done by a bundle of 35 to 40 messy long wires. Since there is more than one sensor chip, switching between testing one chip

to the other was time consuming and was prone to errors. Figure 45 below shows a diagram depicting the setup.

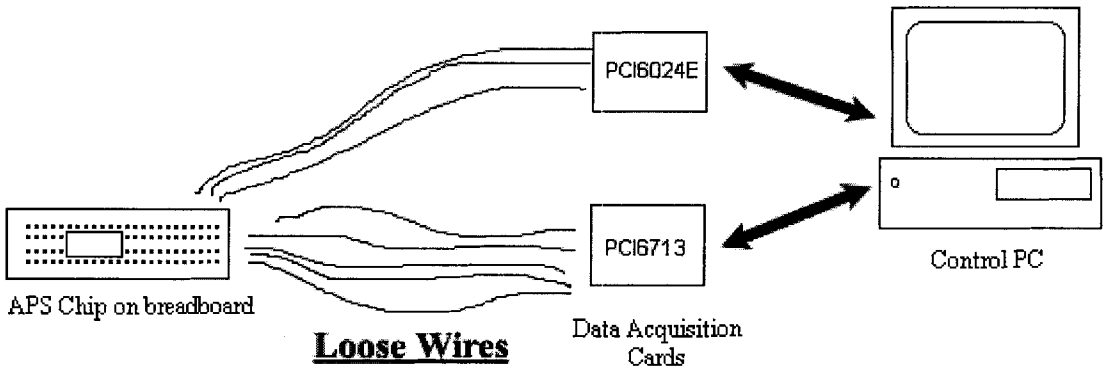


Figure 45 Loose wires connecting APS chip to data acquisition boards after Wang and Liaw [59]

Realizing the inconvenience and inefficiency, a universal connector was proposed and implemented by two undergraduate students, Benjamin Wang and Gary Liaw, who assisted this project [59]. A universal connector is used to connect the breadboard and the data acquisition card, which provides a cleaner and more convenient solution, as shown in Figure 46 below.

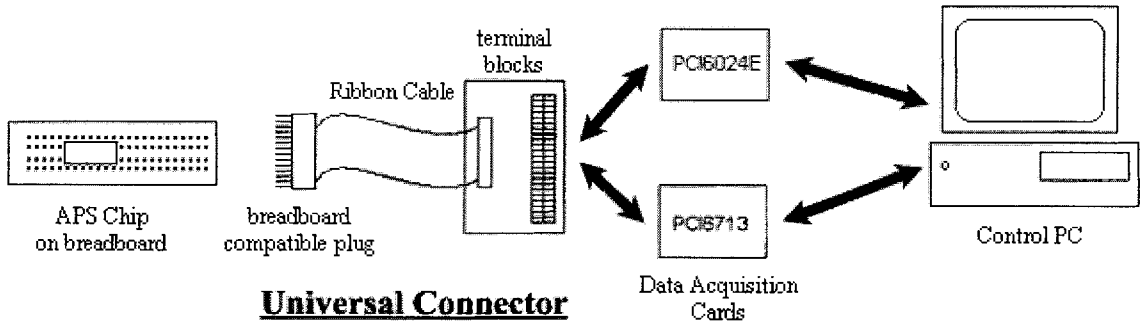


Figure 46 Universal connection increases efficiency in switching between experiments after Wang and Liaw [59]

Since the ribbon cable can be detached from either side of the breadboard-compatible plug or the terminal blocks, switching between experiments with different sensor chips requires simply disconnecting the ribbon cable on the breadboard and reconnecting it to another breadboard with a different APS chip.

4.2 Argon Laser APS Illumination

To separately control the illumination on a single pixel on the APS chip to selectively test individual pixels, one of the test setups of the APS chips involves the use of a focused argon (Ar) laser, using a wavelength of 514nm (bluish green line). By placing the APS chip on a computer-controlled x-y-z positioning table with 0.05μm positioning accuracy and vibration isolation [60], a focus laser beam can be positioned within a given APS. Using objective lenses ranging from 1x to 50x, a laser spot can be focused to a range of sizes, from 2μm to 100μm to cover a single pixel to an array of pixels. Aligning the laser beam is done manually by observing the pixel using the TV camera system on a microscope. Figure 47 below shows the entire setup of the laser table, while Figure 48 is a photograph of the system.

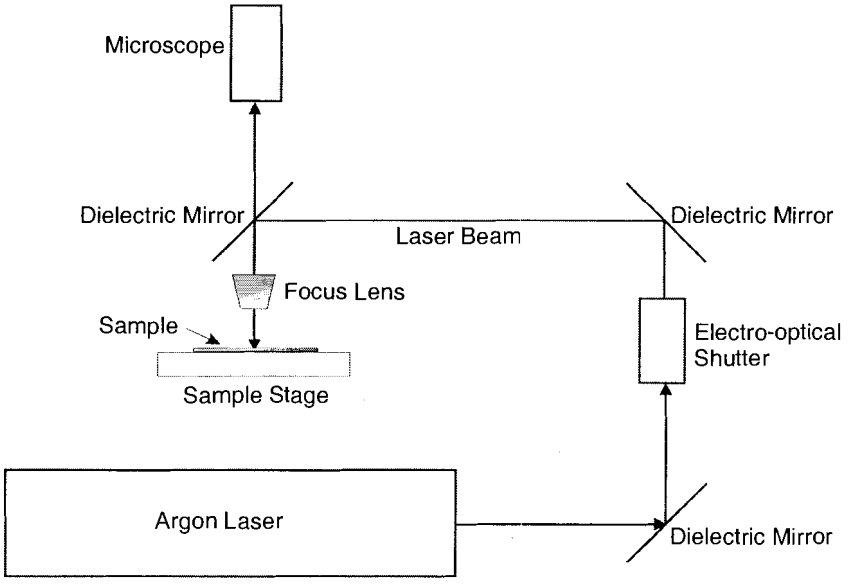


Figure 47 Laser table setup shows argon laser is focused on a sample after Tu [61]

A dielectric mirror reflects the continuous (CW) argon laser beam towards an electro-optical shutter, which is controlled by a computer and a function generator, allowing the signal laser timing and the amount of laser power going through the shutter be rapidly and carefully controlled. With the shutter off, the minimal amount of laser allowed to pass through is less than

1% while over 85% is allowed when the shutter is on. The switching of the shutter can be operated at a high speed (~1μsec) such that a laser pulse stream can be generated.

After the shutter, the laser beam is deflected by another two dielectric mirrors into an objective lens, which determines the size of the laser beam illuminating the sample. Since the laser table is located in an enclosed room, background illumination is minimized when room light is off. Figure 48 and Figure 49 below displays a photograph of the laser table setup which include the argon laser, x-y-z table, microscope, the light control for the microscope and the APS chip.

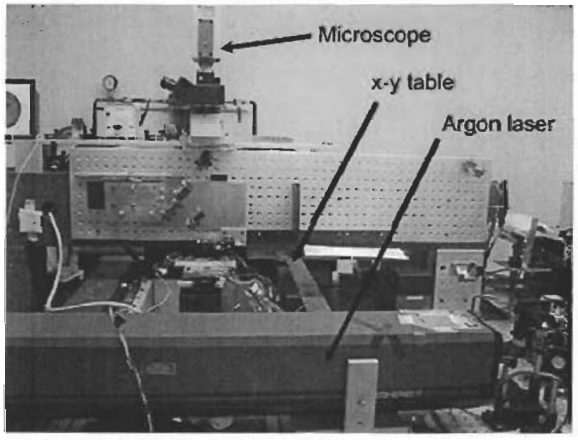


Figure 48 Photograph of the entire laser table setup

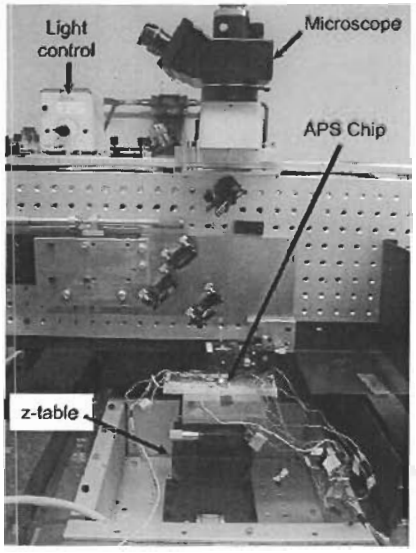


Figure 49 Photograph of the detail of the chip under test

Besides the argon laser, the microscope is also used as another light source to flood illuminate a pixel or a pixel array. This microscope light is supplied by a high-powered incandescent bulb and filtered to give a broad band radish light source. Unfortunately, neither the power nor the timing of the microscope light can be controlled easily. Therefore, LEDs were also used to create an intensity and time controllable light source.

4.3 LED Broad Area Illumination

Since the laser setup is designed to illuminate only part of a pixel, there is a need to create a setup that gives a timed flood illumination. Furthermore, as the laser table and the argon laser are shared with other researchers and students, access is limited. Therefore light emitting diodes are used for some testing when the position of the light signal does not have to be accurately controlled. In the experimental setup, LEDs were mounted on a piece of wooden block, which can be positioned on top of a packaged APS sensor chip. The wooden block keeps the sensor in the dark while the LED provides the only light source. A cavity is created at the bottom of the wooden block as shown in Figure 50 below such that the LED can be mounted at a reasonable distance away from the chip to ensure the sensor chip under the wooden block is flood illuminated by the LED. Different colours of LEDs (red and blue) are used in some testing and changing the LED is convenient by simply switching the LED in the wooden block with another one.

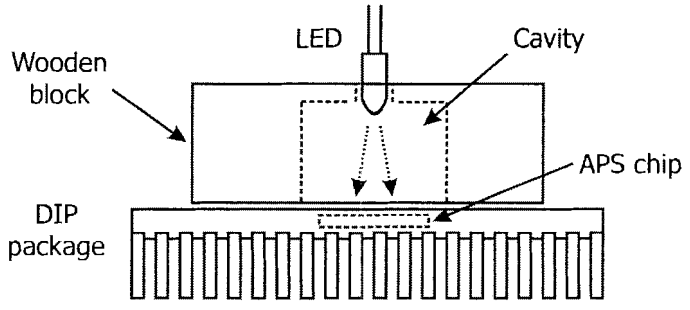


Figure 50 Setup of test using LED as main light source

The red LED that was used has a wavelength centered at 665nm and the blue LED has a wavelength centered at 470nm. The intensity of both LEDs was controlled by one of the analog control lines from the LabVIEW program connected in series with a resistor.

4.4 Summary

This chapter has explained the experimental setup for testing the APS chips and the way the sensors are arranged in the optical systems. In the next two chapters, details of the experimental results for the two novel APS will be presented. Chapter 5 will present the results for the fault-tolerant APS when the argon laser is used for the testing. Chapter 6 will present the results for the duo-output APS when the LEDs and the argon laser are used.

5 CHAPTER FIVE – FAULT TOLERANT APS EXPERIMAENTAL RESULTS

Experimental results of the Fault Tolerant Active Pixel Sensor (FTAPS) are presented in this chapter. The FTAPS will be characterized both when operating without faults and when faults are inserted into the pixel. The first section shows the characterization of the FTAPS with optically induced defects and the second section shows the characterization of the FTAPS with electrically induced defects. Afterwards, the testing result of a small APS system by projecting images on an array is shown.

5.1 Methods of Measurement for Fault Tolerant APS

Prior to this thesis, the fault tolerant APS was simulated but measurement of real devices has not been made. The concept of FTAPS was proposed by Chapman and Audet in 1999 [5]. In 2000, the idea of combining fault tolerant method and traditional software correction method for imagers was studied by Chapman and Koren [7]. Later in 2001, FTAPS was modelled and was simulated with HSpice to give a convincing prove of concept [6]. This chapter carries on with the project to provide experimental prove of the FTAPS.

Two different methods were employed to inject faults into the FTAPS so that the pixel can be characterized when faults are present. The first method uses optical techniques to induce faults into the normal FTAPS pixels. The second method uses special pixels with faults built into the pixels during the design stage, and it is called the electrically induced method.

Optically induced defects are used first as it can be tested on any normal FTAPS pixel within the array. The same pixel can be tested both with and without defects. In order to discover how reliable the optical method is, electrically induced faults are also used. As electrically induced defects are created during the design stage, they are less flexible and more

difficult to test. For example, the same pixel cannot be tested with and without defects. Nevertheless, electrically injected defects also represent some of the real situations when metal lines are shorted or opened.

5.2 Optically Induced Defect Measurements on Fault Tolerant APS

The first method of testing the redundant photodiode APS is to inject defects optically by separately controlling the illumination on one sub-pixel of the redundant APS relative to the other sub-pixel. In this way, it is possible to create the effect of optically stuck low and optically stuck high conditions on any pixel, without the need of creating the fault combining pixels during the design. This is accomplished by using a combination of a focused argon laser source and a field illumination light source. The computer-controlled submicron x-y-z positioning table (Chapter 4) and microscope lens system directs the laser beam to focus onto the correct APS. The microscope light itself provides a controllable uniform illumination across the sub-pixels. This combination of laser and microscope light allows for the generation of any illumination from dark to saturating light levels separately on each sub-pixel.

The initial experiment tested the normal operation of the redundant APS by focusing a laser spot of size 2μm in diameter on the center of the correct sensor, creating equal amounts of illumination on each sub-pixel, and measurements were taken for about two decades of light intensity. As the spot is in the center, both half pixels are activated. The illumination levels are kept within the APS' linear operation region. Figure 51 below shows the laser spot location with respect to the redundant APS pixel for the normal operation.

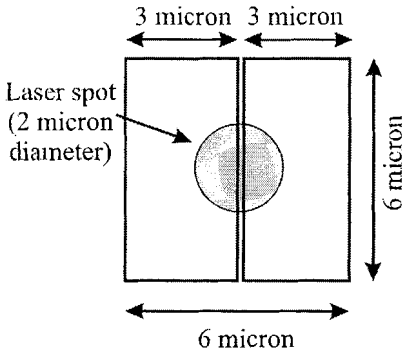


Figure 51 FTAPS with laser simulating normal operation

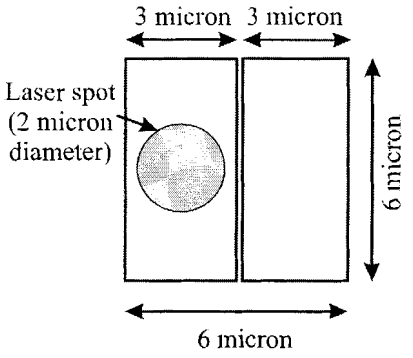


Figure 52 FTAPS with laser simulating stuck low operation

To create pixel that is optically stuck low, only one-half of the redundant APS is illuminated with the laser spot over a range of powers while the other side is in the dark. Figure 52 shows location of the laser spot for optically stuck low operation. This is possible because the photodiode size of each sub-pixel is approximately 3μm×6μm, whereas the laser spot (power within $1/e^2$ of the peak value) is approximately 2μm in diameter. Very little signal was observed on adjacent APS' even at saturation conditions on the illuminated pixel showing little crosstalk among the APS. This also confirms the laser light is well confined to a single pixel.

To create an optically stuck high condition, one-half of the redundant APS is illuminated with laser at an intensity that just saturates that sub-pixel, while the entire pixel is uniformly illuminated with the microscope light, as shown in Figure 53 below. This creates the same effect as if one of the gates of the output transistor was grounded (or the transistor is not functioning).

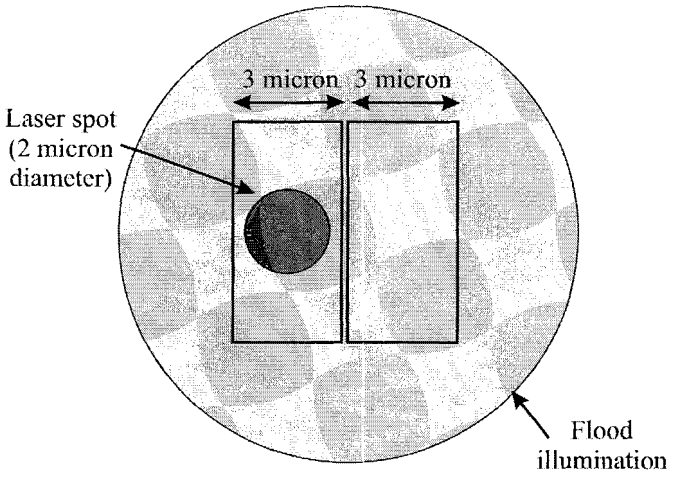


Figure 53 FTAPS with microscope light flood illuminating entire pixel and laser spot saturating one half

The first experimental results of this method were obtained from an earlier study [45], which was carried out in cooperation with Mr. Sunjaya Djaja. Only the major results are presented here and will be compared to the data obtained from using electrically injected faults in the next section. Figure 54 shows the characteristic plot, i.e. the output voltage against illumination intensity of the laser, for the normal, stuck high and stuck low APS when optically induced faults are used.

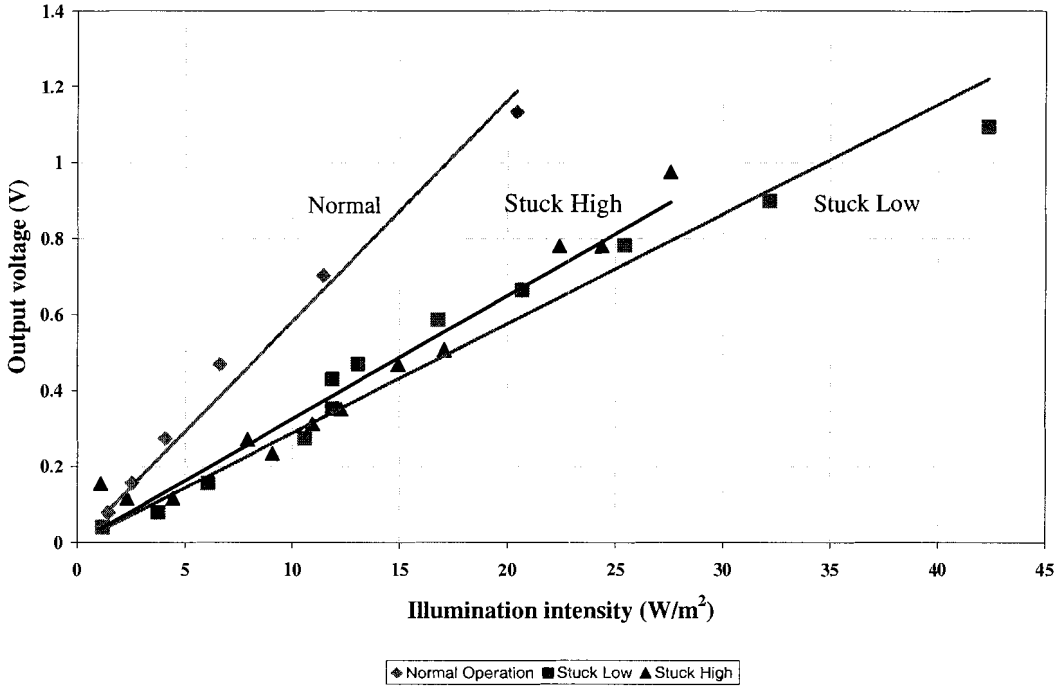


Figure 54 First study of sensitivity of fault tolerant APS versus illumination levels

It can be seen from Figure 54 that the curves for stuck high and stuck low are very similar and they both have approximately half the slope of the normal curve. Table 6 summarizes the sensitivities of the FTAPS in different operating modes, which are obtained from the slope of characterization curves in Figure 54 by regression fits to the data.

Table 6 Summary of sensitivity of fault tolerant APS from first study

Fault tolerant APS operating modes	Sensitivity (V/W/m2)			
Non-Defective (Normal)	0.0582 ± 0.00204	Sensitivity ratio of non-defective to single defect	Difference from expected value of 2	Expected error
Single Defect – Stuck Low	0.0288 ± 0.00100	2.02	0.02	0.141
Single Defect – Stuck High	0.0325 ± 0.00105	1.79	0.21	0.121
Difference between SH and SL Ratio		0.23	N/A	0.262

Comparing to the expected sensitivity ratio of 2, the sensitivity ratio for the single-defect stuck-low agrees within 1% (absolute value of 0.02) while the sensitivity ratio for the stuck-high agrees within 10.5% (absolute value of 0.21). The difference in the sensitivity values themselves is possibly due to greater uncertainties in the experimental setup. The stuck low case is simulated by simply focusing a laser spot in one half of the pixel. The stuck high case requires a second light source, i.e. the microscope light, which introduces another degree of uncertainty in order to saturate another half. Although the microscope light flood illuminates an entire pixel, the intensity of this light source cannot be controlled very accurately. Nevertheless, the difference between sensitivity ratios of the stuck-high and the stuck-low is 0.23, which is within the expected error of ±0.262. This implies that both the stuck-low and stuck-high cases behave statistically the same.

5.3 Electrically Induced Defect Measurements on Fault Tolerant APS

The second test characterizes the fault tolerant active pixel sensors by creating special designs – normally operating pixels, half optically stuck low pixels, and half optically stuck high pixels. By means of electrically induced shorts in the photodiode area, since electrical test corresponds directly to several defects, they allow us to compare the electrical to the optical defects. While no changes have to be made to the normally operating pixel, as shown in Figure 25, the latter two scenarios have been intentionally created on-chip. Since a half stuck low pixel in the optical sense refers to electrically stuck high, we shorted the output node (gate of the output transistor) to VDD. Similarly in a half optically stuck high pixel, it is equivalent to electrically stuck low and the output node is tied to VSS. Figure 55 and Figure 56 below illustrates the ideas in layout.

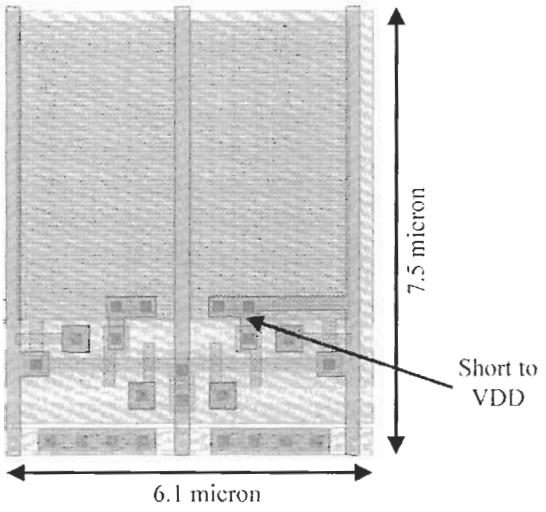


Figure 55 Half-stuck-low FTAPS layout

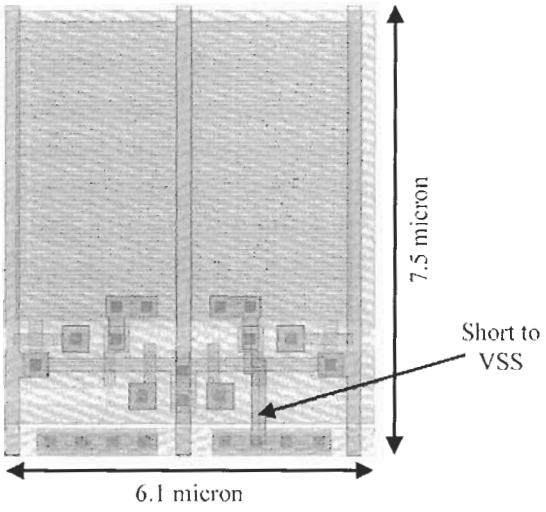


Figure 56 Half-stuck-high FTAPS layout

The characterization of a pixel involves varying the laser power on the individual pixel under test and plotting the output response as a function of laser intensity. A typical pixel response curve over time with varying light intensities is shown below in Figure 57.

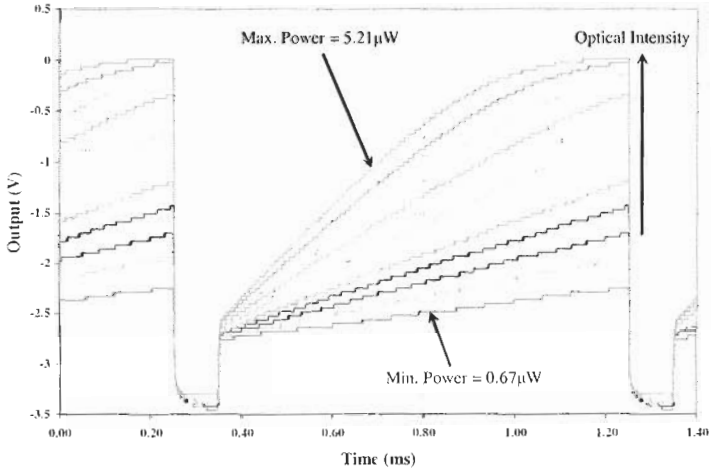


Figure 57 Typical pixel responses over time with varying light intensities (see Figure 58 for intensities)

First of all, it should be noted that the output increases during integration because the FTAPS output is a current and it is converted to voltage with a current-to-voltage converter. As

the intensity of the light increases, it can be seen that the slope of the output curve increases. The sensitivity of a pixel (output voltage against light intensity) is obtained by finding the difference between two values on the response curve over a range of intensities, the first value at the beginning of the integration right after reset, and the second value at the end of the integration. It is very similar to correlated double sampling in which the output during reset is stored and subtracted from the stored output at the end of the integration. For each of the normal and stuck low cases, three separate pixels were tested and plotted in Figure 58. Similarly for the stuck high case, three separate pixels were tested and plotted in and Figure 59 along with three pixels from the normal case for comparison.

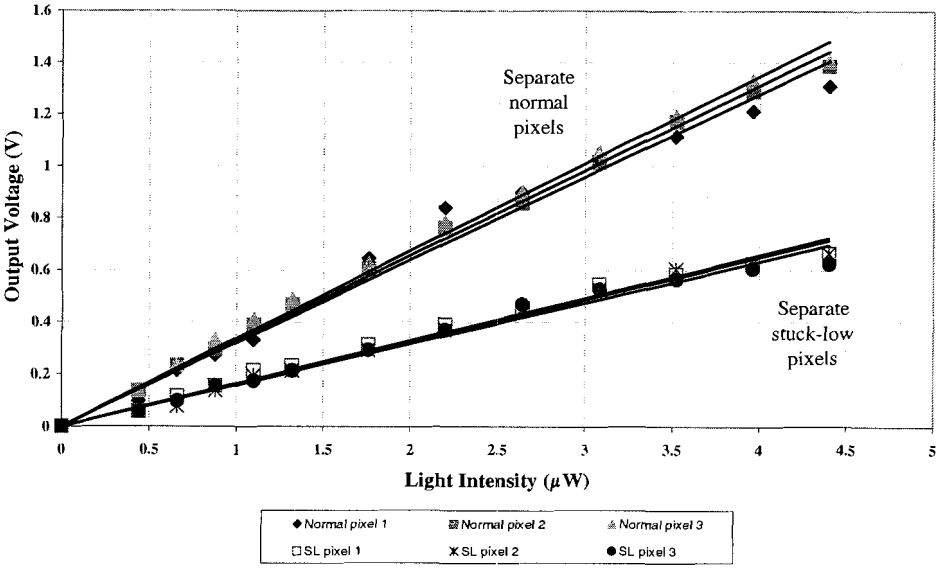


Figure 58 FTAPS pixel output voltage as a function of total pixel illumination for 2 separate cases: normal operation and half stuck-low

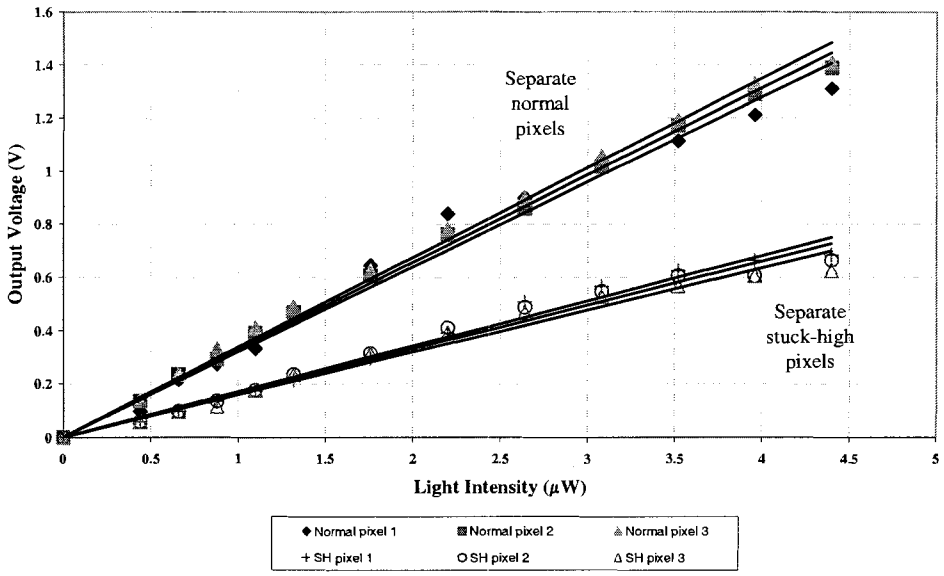


Figure 59 Pixel output voltage as a function of total pixel illumination for 2 separate cases: normal operation and half stuck-high

Figure 58 and Figure 59 plot the output voltage of the APS as a function of the entire pixel illumination for defect free, stuck low and stuck high pixels. Three pixels of each type are tested. The sensitivities of these pixels as measured by the slope of Figure 58 were obtained by linear regression analysis. Table 7 summarizes the slopes of the sensitivities of the nine pixels, the average sensitivities, as well as the discrepancies from the averages.

Table 7 Summary of Figure 56 showing the slopes of the 3 separate pixels for each case (normal, stuck low, and stuck high)

Fault Tolerant APS Operating Modes	Sensitivity (V/μW)	Average Sensitivity (V/μW)	Difference from Average (V/μW)
Normal (Defect Free)	0.3195 ± 0.00702	0.3282 ± 0.00466	-0.0087 ± 0.01168
	0.3280 ± 0.00307		-0.0002 ± 0.00773
	0.3371 ± 0.00390		0.0089 ± 0.00856
Stuck Low	0.1705 ± 0.00353	0.1649 ± 0.00381	0.0056 ± 0.00734
	0.1653 ± 0.00397		0.0004 ± 0.00778
	0.1589 ± 0.00392		-0.0060 ± 0.00773
Stuck High	0.1644 ± 0.00320	0.1616 ± 0.00313	0.0028 ± 0.00633
	0.1623 ± 0.00272		0.0007 ± 0.00585
	0.1580 ± 0.00348		-0.0036 ± 0.00661

In order to characterize the response of the three cases (normal, stuck-low, and stuck high) and to compare between the stuck-low/stuck-high and normal cases, the above results from the three pixels for each design is averaged out to give the results in Table 8 below.

Table 8 Summary of sensitivity of fault tolerant APS under normal and stuck conditions

Fault Tolerant APS Operating Modes	Sensitivity (V/μW)	Sensitivity Ratio of Non-Defective to Single Defect
Non-Defective (Normal)	0.3285 ± 0.00429	
Single Defect – Stuck Low	0.1616 ± 0.00294	2.03 ± 0.063
Single Defect – Stuck High	0.1649 ± 0.00365	1.99 ± 0.070
Difference between Stuck-High and Stuck-Low Sensitivity Ratios		0.04 ± 0.133

Table 8 above summarizes the sensitivity of the three different cases for the FTAPS. It shows that both the sensitivity of the half-stuck-high and the half-stuck-low FTAPS are very close to the expected ratio of 2 when compared to the non-defective case.

As can be seen from Table 8, the stuck low and stuck high sensitivity ratios are within the error of the expected 2 ratio. The percentage differences comparing the half-stuck-high or the half-stuck-low and the expected ratio of 2 are 0.5% (absolute value of 0.03) and 1.5% (absolute

value of 0.01) respectively. Comparing the difference of the sensitivity ratios of the stuck-high and the stuck-low, the absolute value is 0.04, which is within the expected error of 0.133. This result reinforces the confidence in the experiment undertaken for this thesis as it proves that the difference in the results is statistically insignificant.

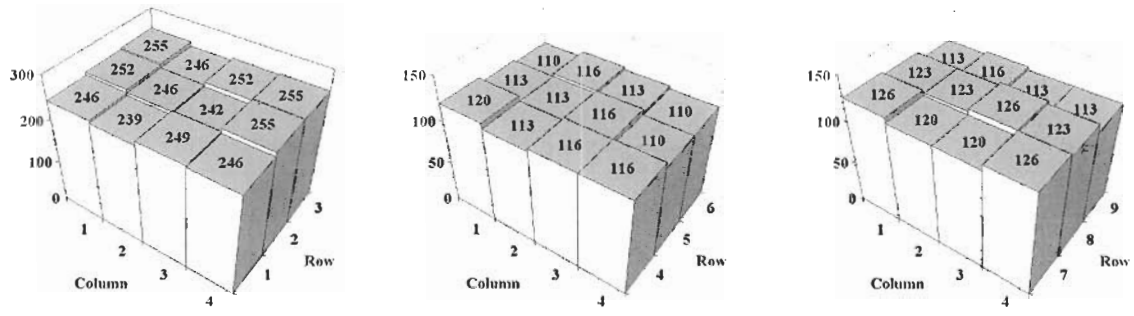
It is important to note that both the stuck low and stuck high cases showed this ratio of two. By comparison in the optical tests, the stuck low gave very good results but the stuck high had a much larger error. This built-in defective design for testing confirms that the difference with optically created stuck high is due to errors from light sources.

5.3.1 Uniform Illumination of Small Pixel Arrays with Electrically Injected Faults

In order to find the variance in sensitivity of the image sensor array, uniform light illumination was done on a 3 by 4 pixel array of each type. The readout data has been converted to 8-bit grayscale shown in Table 9 below. This table and Figure 60 below show the sensitivity distribution of the array, which demonstrate that the pixel variations are indeed small.

Table 9 Variance of image sensor with uniform light illumination shown by grayscale values

Operating Modes	Average	Std. Dev.		
Defect Free	248.44	5.28		
Stuck Low	114.12	3.04	Difference from Defect Free	Expected Error of Difference
Stuck High	120.15	4.99		
Stuck Low after × 2 Calibration	228.24	6.08	-20.2	± 11.36
Stuck High after × 2 Calibration	240.31	9.99	-8.13	± 15.27



(a) (b) (c)

Figure 60 Variation of response to uniform light illumination for fault tolerant APS (a) operating normally (b) stuck low and (c) stuck high scaled to an 8-bit grayscale value

The average grayscale value of the defect free case is shown in the table above. The average values of both the stuck low and stuck high cases are doubled and compared to that of the defect free. Several observations can be made from the numbers. First of all, the noise or errors from the stuck-low and stuck-high cases are higher, as would be expected from the smaller signal. The reason is twofold. First of all, both of their outputs are half of the defect free pixels because they are half as sensitive. The second reason is that the noise or errors would be doubled after calibration of multiplication by two.

The second observation that can be made is that the difference between the average of the stuck-high pixel and that of the defect free pixel is 8.13, which is less than the expected error of 15.27. The difference is 20.2 for the stuck-low case, which is less than two times the expected error of 11.36. This implies that the difference of the results is statistically insignificant.

Both results using two different experimental methods agree with each other within expected errors; therefore, showing that a simple multiplication by 2 is sufficient to correct a single defect within a fault tolerant APS.

5.4 Capture of Simple Bitmap Images

The previous experiments were done on individual pixels. In this section, an image will be taken with small arrays of the redundant pixels, and compared to the same image recovered from the stuck low and stuck high arrays. The first order test involves projecting simple bitmap patterns on a small pixel array and comparing the results for the normal fault tolerant APS and the two defective modes. The results would be used to test the validity of the fault-tolerant concept when the APS is defective. The 9×4 pixel array consists of three rows of fully operational fault tolerant APS' followed by three rows of optically stuck low and three rows of optically stuck high pixels. The patterns are projected using an argon laser and a mask pattern combined with various lens systems. The mask pattern size is larger than the size of the laser beam, which is 2.5mm; therefore, a beam expander is necessary to expand the beam to illuminate the entire mask. After the pattern is formed by the mask, a beam shrinker is used to reduce the size of the pattern to the appropriate size for the APS pixel array. Figure 61 shows the entire setup of the optics.

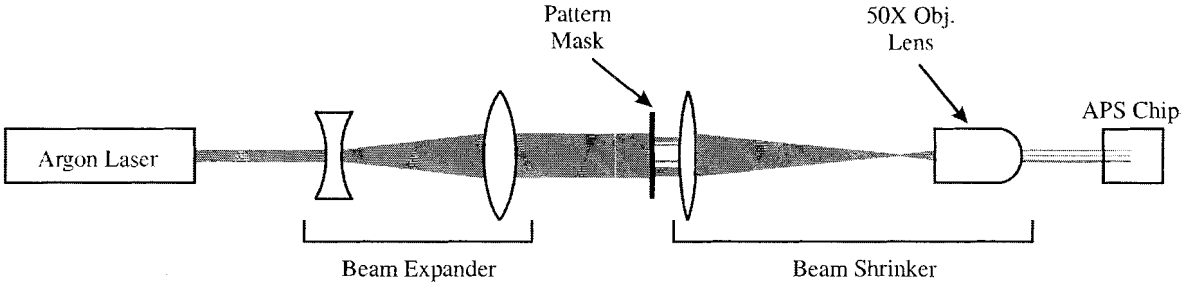


Figure 61 Setup for projection of pattern on APS using the laser

A simple pattern is captured by a 9×4 fault tolerant APS pixel array. Each row of pixel is moved to a reference position so that each row is exposed to consistent lighting conditions. Figure 62 below shows the capture from the APS array when the right half of the array is blocked by the mask.

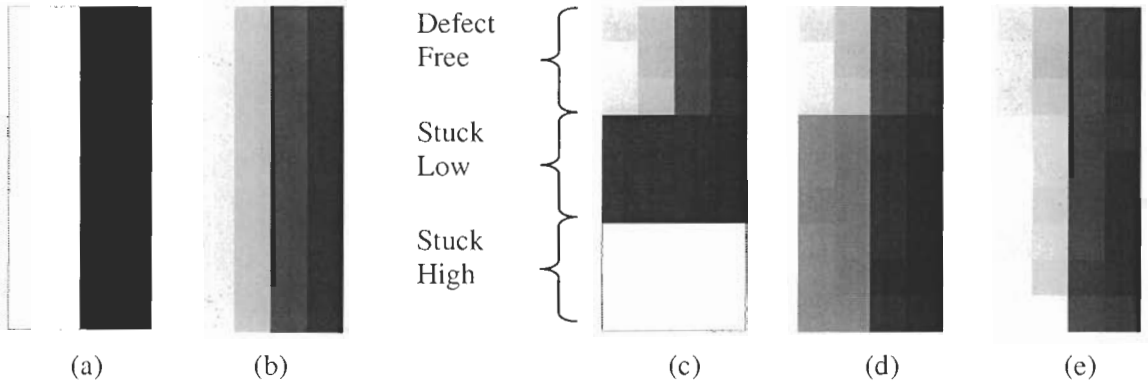


Figure 62 (a) Mask for projection, (b) expected image using defect-free fault tolerant APS array, (c) capture of half-blocked image if no fault tolerance is presence, (d) image captured with fault tolerance before any calibration, (e) final image with fault tolerance after compensation of 2 and individual correction for each pixel

Figure 62 (a) shows the mask used to project the image. Figure 62 (b) shows what a defect-free fault tolerant APS would obtain, in which the left half is not perfectly white while the right half not perfectly black. This uncertainty at the edge between two columns could come from diffraction or the projection mask not being perfectly aligned with the pixel boundaries. Figure 62 (c) shows what the images would look like when the middle three are optically stuck low pixels and the last three are optically stuck high pixels without using redundant pixels. Figure 62 (d) shows the intermediate images captured data when the pixels have redundancy and defects but before calibrations are made to the half-stuck pixels. Figure 62 (e) shows the final image using fault tolerant pixels after compensation of 2 and correction for each individual pixel corresponding to their variance in Table 9 and Figure 60.

It can be seen from Figure 62 (c) that the image with no fault tolerance has large amounts of missing information relative to those with redundancy. The images captured from the fault tolerant APS after calibration in Figure 62 (e) appears to have a sharper contrast between the bright and the dim spots compared to that before calibration in Figure 62 (d). Although there is some recovery in the non-corrected pixels, the resulting image is much enhanced after compensation.

It is valuable to look at the grayscale values resulting from the captures above so comparisons can be made on the same column between the fully operational pixel array and both the stuck low and stuck high pixel array after compensation by multiplication of 2. Table 10 below shows the grayscale values for these three cases and the absolute errors compared to the average of the defect-free (normal) pixels.

Table 10 Grayscale values and absolute error with respective to averages of the normal case for a small bitmap captured using three cases of the fault tolerant APS after compensation of 2

Operating Modes	Row\Col	Col 1			Col 2			Col 3			Col4		
		Value	Abs. Diff	Exp. Error	Value	Abs. Diff	Exp. Error	Value	Abs. Diff	Exp. Error	Value	Abs. Diff	Exp. Error
Defect Free	Row 1	219	-7.1	6.2	187	-3.6	11.1	43	-1.8	3.1	21	-1.8	3.1
	Row 2	230	3.6	6.2	182	-8.9	11.1	43	-1.8	3.1	21	-1.8	3.1
	Row 3	230	3.6	6.2	203	12.5	11.1	48	3.6	3.1	27	3.6	3.1
Average (Std. Dev.)		226.5 (6.2)			190.8 (11.1)			44.6 (3.1)			23.2 (3.1)		
Stuck Low	Row 1	225	-1.8	12.4	203	12.5	11.1	43	-1.8	3.1	32	8.9	9.3
	Row 2	225	-1.8	12.4	203	12.5	11.1	43	-1.8	3.1	21	-1.8	9.3
	Row 3	214	-12.5	12.4	203	12.5	11.1	43	-1.8	3.1	21	-1.8	9.3
Average (Std. Dev.)		221 (6.2)			203 (0.0)			43 (0.0)			25 (6.2)		
Diff. from Defect Free		-5.3			12.5			-1.8			1.8		
Expected Error from Difference		12.4			11.1			3.1			9.3		
Stuck High	Row 1	235	8.9	6.2	214	23.2	17.3	43	-1.8	9.3	21	-1.8	9.3
	Row 2	235	8.9	6.2	214	23.2	17.3	32	-12.5	9.3	21	-1.8	9.3
	Row 3	235	8.9	6.2	225	33.9	17.3	43	-1.8	9.3	32	8.9	9.3
Average (Std. Dev.)		235 (0.0)			218 (6.2)			39 (6.2)			25 (6.2)		
Diff. from Defect Free		8.9			26.7			-5.3			1.8		
Expected Error from Difference		6.2			17.3			9.3			9.3		

The differences between the averages of the defect free pixel and that of the corrected stuck low and stuck high pixels on the same column are shown in the highlighted boxes in Table 10. These values are then compared to the expected error for the differences, shown in the second rows of the highlighted boxes. It can be seen that the differences for the stuck-low case are less than or slightly greater than the expected error. While two of the four differences for the stuck-high case are more than the expected error, they are within the statistically acceptable range of two times the expected error. This strongly suggests that a multiplication by two is sufficient to correct for single-defect problems, thus images can be recovered in the presence of stuck-low and stuck-high defects, within the expected pixel variation.

5.5 Summary

Fault tolerant active pixel sensors (FTAPS') have been fabricated using CMOS 0.18 micron technology. This specially designed image sensor tolerates common defects that are formed during fabrication or degradation over the lifetime of the pixel array. The FTAPS is structured by splitting a traditional APS into two operating halves. Their independent but parallel operations increase the reliability of the pixel as well as the fabrication yield, thus decreasing the production cost. In this chapter, characterization of the FTAPS illustrated that the compensation required for a half stuck low pixel or a half stuck high pixel is a multiplication by two. Simple bitmap images were captured on a small array using different operating modes and the results show the significance of the FTAPS. Lost information in defective pixels can be recovered well unless both halves are defective, which has a very low probability. Future works involve the testing of the photogate FTAPS, which has already been fabricated, as well as capturing larger images using large arrays for both the photogate and photodiode FTAPS.

In the next chapter another novel APS, duo-output APS, will be discussed. This special APS eliminates background illumination when an optical scanning system scans for a particular optical signal and therefore the signal can be detected more accurately. An additional output path

is created by utilizing the concept of the 4-transistor APS to allow signal integration at different out paths at different phases within a readout cycle.

6 CHAPTER SIX – DUO-OUTPUT APS EXPERIMENTAL RESULTS

In Chapter 3, the implementation of the duo-output APS (DAPS) was discussed and Figure 34 showed the schematic of the design. Test cells of this DAPS were fabricated using TSMC CMOS 0.18 micron technology. This chapter presents the experimental results of this pixel design. Light emitting diodes and an argon laser were used as the major optical input signal to the sensor. The first section of this chapter presents initial experimental results using LEDs, suggesting some undesired output characteristics from the pixel output. The second section shows the results of the DAPS if LEDs are replaced by a focused argon laser beam. Better results from using the laser identify the problems with the current design and the direction needed for improvement.

6.1 Experimental Results Using Light Emitting Diodes

This section presents the experimental results from testing the duo-output APS using red light emitting diodes of wavelength centered on 665nm. Tests of the DAPS with LEDs use the setup described in Chapter 4.3. As it was explained in Chapter 3.3, one of the two sides of the DAPS integrates one phase while the other side integrates the other phase. If an optical source is encoded and synchronized with the DAPS such that it is turned on only during the first phase, one of the two sides will integrate the optical signal along with the background illumination. On the other hand, the other side of the pixel will integrate only the background signal during the second phase. Subtracting the second reading from the first removes the background illumination.

Experiments are performed in several stages, starting with simplified operation using simple input signals. Unless otherwise specified, red LED with a peak wavelength of 665nm was used. The stages and the order that these tests are discussed are as follows. In the first test, one

of the two enable gates of the DAPS pixel is always kept off to disable one side while the other side operates as a 4-T APS. This test is to show that the DAPS would operate identical to a 4-T APS when one side is disabled. In the second test, both sides of the DAPS operate sequentially as described in Chapter 3.3 and a constant light source is used. This test allows comparison to be made between the outputs from the two sides of the DAPS when the input is constant. In the third test, both sides operate sequentially and a synchronized LED is pulsed such that it is turned on only during the first of the two integration phases. This is the ideal environment for the operation of DAPS because there is no background illumination. The result of this test serves as a basis for comparison with the next test. In the forth test, a more realistic situation is tested with both sides operating sequentially and in additional to the cycled light source, a constant background light signal is added as the background illumination.

6.1.1 Single Side Operation

In the first stage, one of the two enable gates is always kept off to disable one side while the other side operates by itself as a 4-T APS. The result is similar to a simple 4-T photodiode APS configuration as discussed in Chapter 2.4.4. The test is to check for isolation on one side while we get proper collection on the other side. In the first experiment, the LED full area illumination was used and the LED intensity is kept constant throughout the entire APS cycle. Figure 63 below shows the two input signals, *reset* and *enable*, along with the pixel output when LED is fixed at three different intensities. The intensities are represented by the power of the LED measured with a light meter (Coherent FieldMaster-GS) when the LED is placed in proximity to the meter's sensor. The numbers can only be used as references and they do not represent the exact amount of power shining on the pixel because the sensor is flood illuminated. Unless otherwise stated, numbers representing the power of the LED in the remaining of this thesis are served as references.

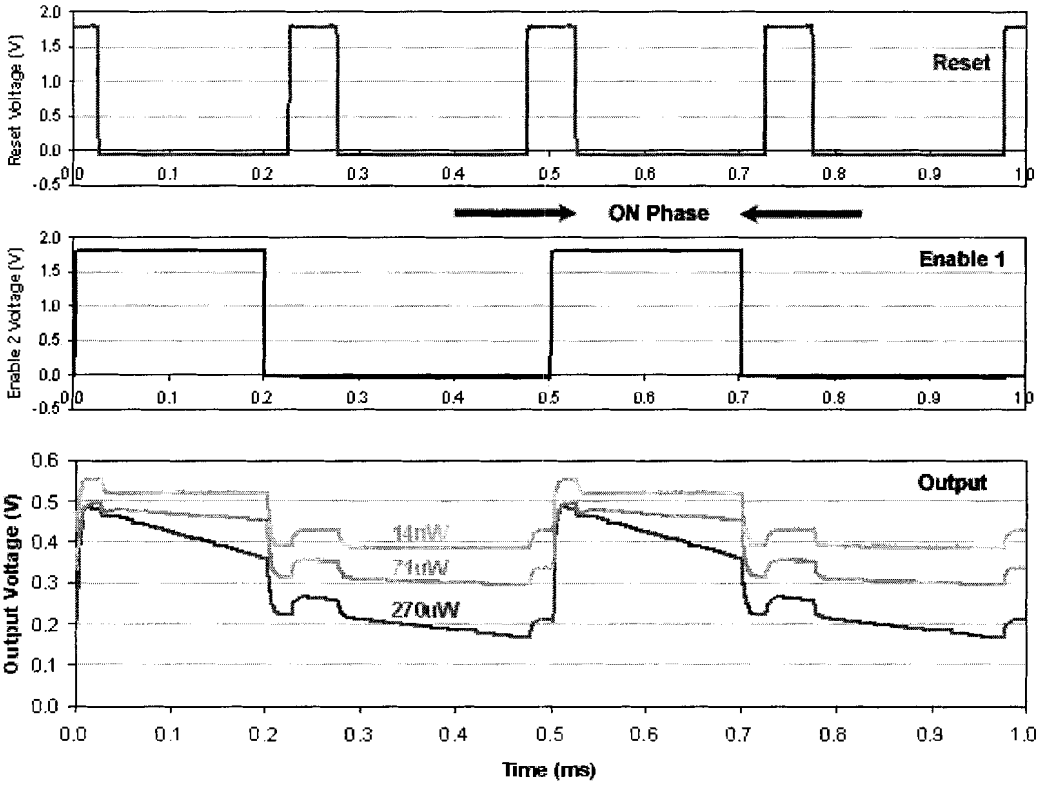


Figure 63 Input signals and output plots of a DAPS with single side operating (LED constantly on)

As it was explained in Chapter 3, for a fully functional DAPS operation, the integration period when the LED is ON is referred to as the "ON phase". In this case, we assign the integration period where enable 1 is high and after reset goes low as the "ON phase". The "OFF phase" is the second integration when enable 2 is high and right after reset goes low with LED off.

Figure 63 above shows that the pixel behaves normally during the ON phase integration. Higher LED intensity results in larger voltage drop. However, during the OFF phase, the voltage output continues to drop and the amount of voltage drop also depends on the LED intensity, with higher LED intensity resulting in larger voltage drop. In order to compare the results from both phases, Table 11 below shows the slopes of the above output at both the ON phase and OFF phase of the integration cycle.

Table 11 DAPS slope comparison of ON and OFF phase for single side operation

Constant LED power	Slope during ON phase (± 31 V/s)	Slope during OFF phase (± 31 V/s)	Ratio (ON / OFF)
14 nW	0.0 V/s	30.8 V/s	0
71.1 μW	184.6 V/s	92.3 V/s	2.0
270 μW	676.9 V/s	246.2 V/s	2.75

Ideally, we would expect to see that regardless of what the light signal is, the slope of the output curve during OFF phase is zero, i.e. no voltage drop. The ratio of the slope during the ON phase to that during the OFF phase should be very large and ideally close to infinity. The above experiment shows that the voltage drop during the OFF phase corrupts the signal stored during the ON phase. Since the amount of drop depends on the light intensity, it is suspected that the light is disturbing the pixel output in some way during the OFF phase.

Another observation made from Figure 63 is that whenever the enable gate is turned off, the output voltage jumps simultaneously. This phenomenon is called charge injection. When a transistor acting as a switch is connected to the gate of the readout transistor, charge injection occurs when the transistor is switched off. The issue of charge injection will be addressed in more detail in Chapter 7, and methods of cancelling this undesired property will be suggested as well. Similar effect occurs when the reset transistor is switched off. Since the reset transistor is located on the photodiode node but it is located close to the readout transistor, the output voltage jumps are most likely due to coupling noise through the substrate and are therefore much smaller.

When an LED pulse is synchronized with the ON phase, i.e. LED is on only during the ON phase integration cycle, the output plot in Figure 64 below is obtained.

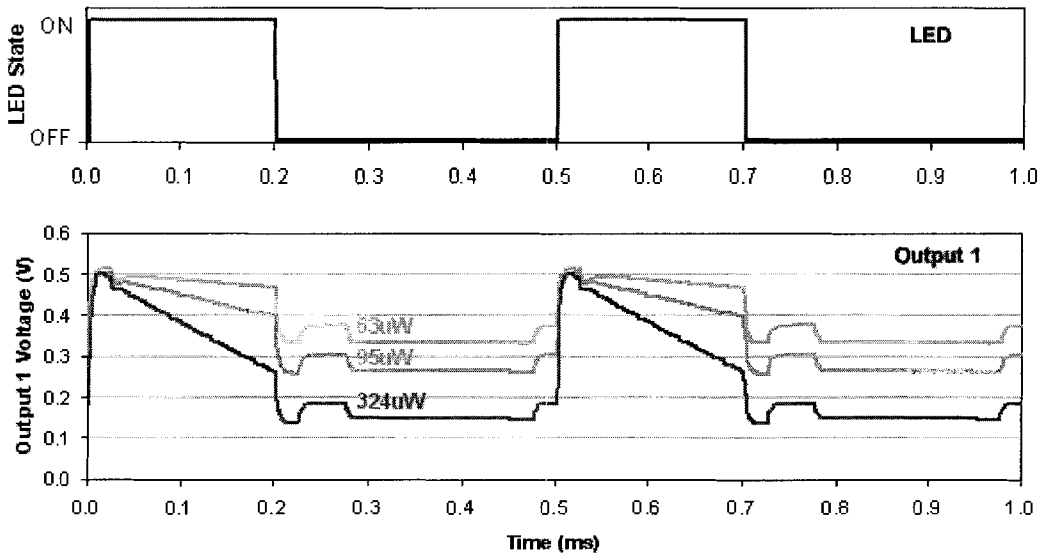


Figure 64 Input signals and output plots of DAPS with single side operating and synchronized LED of different intensities (see Figure 63 for Reset and Enable 1 signals)

Figure 64 above shows that when LED is off during the OFF phase of the cycle, the output voltage does not drop regardless of what the LED intensity is during the ON phase of the cycle. This independency on the ON phase confirms that the voltage drop is due to the light signal disturbing a certain part of the APS pixel during the OFF phase. This result also shows that the charge at the gate of the readout transistor can be kept constant during the OFF phase without significant RC time decay or leakage to the substrate.

Therefore, the OFF phase voltage drop suggests that while the enable is shut off, light is affecting the device in some way. It could be due to several possibilities: 1) enable gate does not provide a good enough isolation between its source and drain resulting in leakage, 2) penetration depth of the light source is too deep such that the photo-generated electrons diffuse across the enable gate within the substrate, and 3) light is affecting other portion of the pixel out of the photo-sensing area such as the enable gate or output transistors. Further investigation will follow in the remaining of this chapter.

6.1.2 Double Side DAPS Operation

After a set of simplified experiments with only one side operating, experimental results when both sides of the DAPS operate are presented in this section. In the first experiment, the LED intensity is kept constant. With two sides operating, there are three input signals – reset, enable 1 and enable 2. Figure 65 below shows input signals and the output plots of both output 1 and output 2 when three different LED intensities are used.

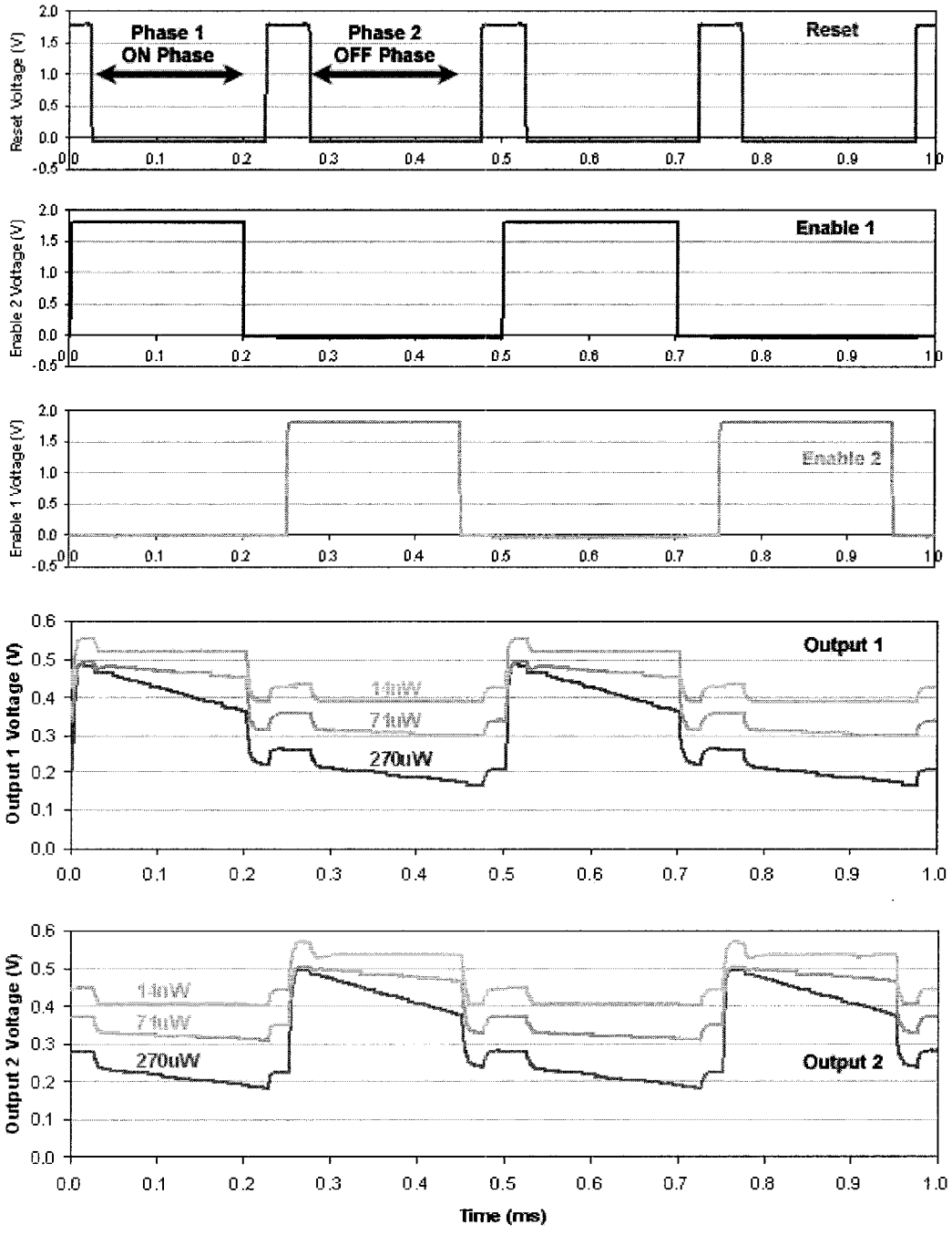


Figure 65 Input signals and output plots of a DAPS with both sides operating (constant LED of different intensities)

Note that side 1 is ON when side 2 is OFF and vice versa. Table 12 below shows the slopes of both side 1 and side 2 in the first and second phase. In the first phase, side 1 is ON while side 2 is OFF and in the second phase, side 1 is OFF while side 2 is ON. The ratio in the

last column shows the ratio of the slope of side 1 to that of side 2 in the first phase, and the ratio of the slope of side 2 to that of side 1 in the second phase.

Table 12 DAPS slope comparison of ON and OFF phase for both sides with constant LED intensity

Constant LED power	Slope in the 1st phase (± 31 V/s)		Slope in the 2nd phase (± 31 V/s)		Ratio(ON phase / OFF phase)	
	Side 1	Side 2	Side 1	Side 2	1st phase	2nd phase
14 nW	0	0	0	0	0	0
71.1 μW	184.6	61.5	61.5	184.6	3.00	3.00
270 μW	646.2	276.9	246.2	615.4	2.33	2.33

The figures in Table 12 above show that the results are very similar to the results in Table 11 for single side operation. The slopes of the ON phase or the OFF phase are almost identical to that of the single sided operation, suggesting that the operation of one side does not affect the operation of the other side. The ratios also show very similar figures to those presented in Table 11, with the slope of the ON phase only 2 to 3 times that of the OFF phase. Thus, the difference between output 1 and output 2 would not provide an enough distinction for background rejection.

In an ideal environment for optical scanning, there is only one main light source and no background illumination. In this case, the only light source is the encoded LED that is synchronized with one of the two sides. In the next experiment, the DAPS operates with LED synchronized to side 1 of the pixel such that during the first phase of the cycle, only side 1 is enabled and the LED is on. The LED is off in the second phase when side 2 alone is enabled. Figure 66 below shows the plots of output 1 and output 2.

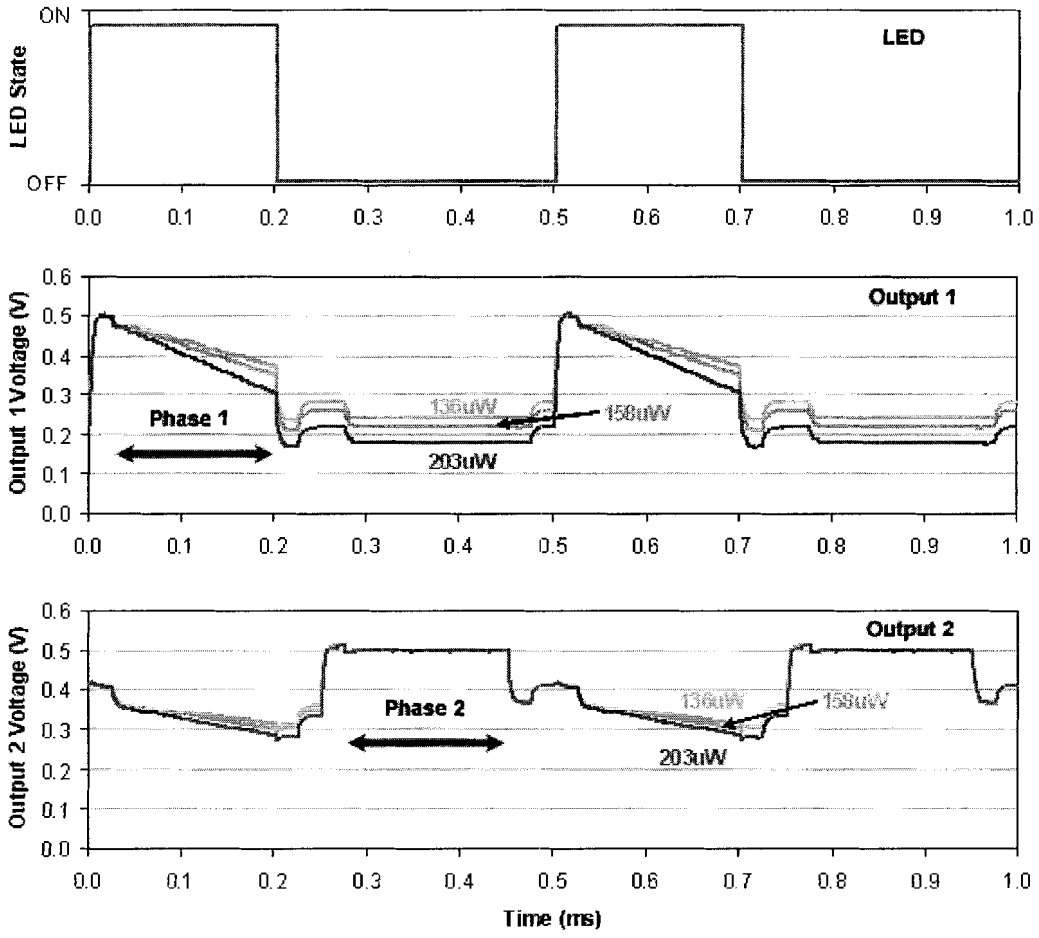


Figure 66 DAPS output plots of side 1 and side 2 with LED synchronized to side 1 and no background offset (see Figure 65 for Reset, Enable 1 and Enable 2 signals)

Output 1 plot shows that during phase 1, different LED intensities result in different slopes. During phase 2, since the LED is off, output 1 remains constant. For output 2 during phase 2, the LED is off, thus no integration occurs. During phase 1 however, output 2 drops depending on the intensity of the LED, again suggesting the LED affects the side that is disabled. Table 13 below summarizes the slopes of the two plots, showing the ON phase to OFF phase ratio is again between 2 and 3.

Table 13 DAPS with LED synchronized to side 1 slope comparison of two outputs

LED ON phase power	Slope in the 1st phase (± 31 V/s)		Slope in the 2nd phase (± 31 V/s)		Ratio(ON phase / OFF phase)	
	Side 1	Side 2	Side 1	Side 2	1st phase	2nd phase
136 μW	646.2	307.7	0	0	2.10	N/A
158 μW	800.0	307.7	0	0	2.60	N/A
203 μW	1015.4	430.8	0	0	2.36	N/A

It would be important to see if the integration of the first phase would affect that of the second phase. Previously, it was shown that with constant LED integration, the slope of the signal output during the second phase depends on the intensity. However, it is possible that the slope of the output in the second phase also depends on the final output value at the end of the first phase. In order to eliminate this uncertainty, the following experiment was performed.

If a background light signal is added to the above experiment by offsetting the LED intensity during its off phase, the slopes of both side 1 and side 2 would be greater than 0. Figure 67 shows the plots of output 1 and output 2. Table 14 shows the slopes with different ON phase LED intensities (measured LED power from 114μW to 203μW) and a fixed OFF phase background light intensity (measured LED power of 91.8μW).

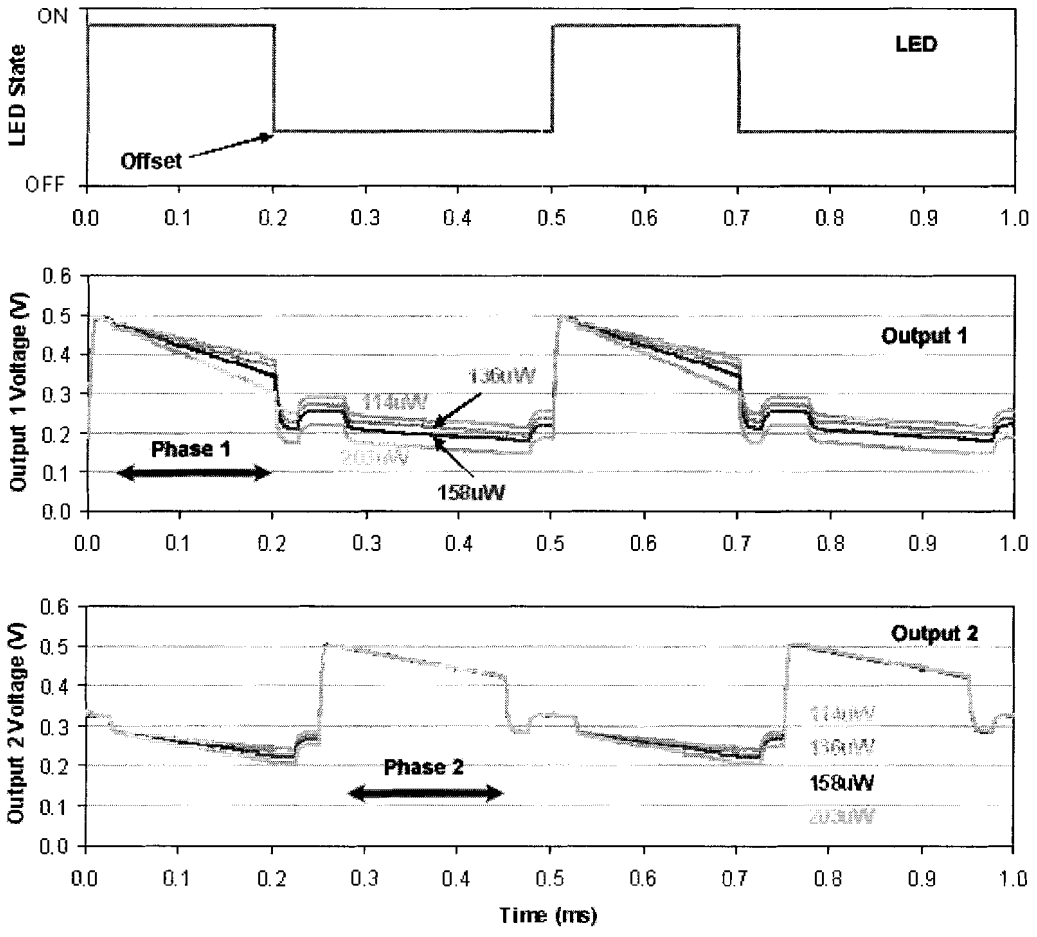


Figure 67 DAPS output plots of side 1 and side 2 with LED synchronized to side 1 and background offset (see Figure 65 for Reset, Enable 1 and Enable 2 signals)

Table 14 DAPS output slope comparison of ON and OFF phase with LED synchronized side 1 and background light offset (LED measured power of 91.8μW)

LED ON phase power	Slope in the 1st phase (± 31 V/s)		Slope in the 2nd phase (± 31 V/s)		Ratio(ON phase / OFF phase)	
	Side 1	Side 2	Side 1	Side 2	1st phase	2nd phase
114 μW	523.1	215.4	184.6	430.8	2.43	2.33
136 μW	646.2	276.9	184.6	430.8	2.33	2.33
158 μW	769.2	307.7	153.9	430.8	2.50	2.80
203 μW	953.9	400.0	184.6	400.0	2.38	2.17

The above table shows that the slopes of all four outputs in the second phase, i.e. offset background illumination from LED with power 91.8μW, are consistent, independent on the LED intensity during the first phase, implying the integration of the second phase is independent of the first phase.

6.1.3 DAPS Illumination with Shorter LED Wavelength

It was found from previous sections that the output voltage drops even when the enable gate is off. Experiments show that it is not due to insufficient isolation from the enable gate. Nor it is due to leakage or RC time constant decay because the voltage can be kept constant when there is no light during the OFF phase (Figure 64). This section continues to investigate to see if the voltage drop is caused by the deep penetration capability of the red LED. Photo-generated electron deep in the substrate may diffuse across the enable transistor indirectly to the output node.

By using a signal with shorter wavelength at the blue end of the visible light spectrum, the voltage drop might be reduced because the light has a shallower penetration depth and diffusion is less. Table 15 below shows the experimental result when a blue LED of wavelength 470nm is used. Both sides of the DAPS operates normally and the LED is synchronized with phase 1 and no background light is assumed.

Table 15 DAPS with constant blue LED signal slope comparison of two outputs

Constant blue LED power	Slope in the 1st phase (± 31 V/s)		Slope in the 2nd phase (± 31 V/s)		Ratio(ON phase / OFF phase)	
	Side 1	Side 2	Side 1	Side 2	1st phase	2nd phase
133 μW	553.9	215.4	-30.8	0	2.57	N/A
162 μW	707.7	276.9	0	0	2.56	N/A
219 μW	923.1	369.2	0	0	2.50	N/A

The slopes of the output curves in Table 15 cannot be compared directly to those obtained previously when red LED was used because the light intensities of the LEDs are not accurately controlled. Nevertheless, the ratios of the slope in the ON phase to that of the OFF phase are all around 2.5, suggesting that there is no significant improvement with the use of blue LED over red LED. Therefore, penetration depth of different light wavelength does not contribute to the output voltage drop during a pixel's OFF phase.

6.2 Spot Illumination of DAPS

If the effect of the optical signal on other part of the pixel (transistors, metal contacts, etc) causes the voltage to drop during the OFF phase, confining the light source only to the photo-sensing area should remove the undesired output. Design of the pixel can limit a light source to only the photo-sensing area if higher metal layers are used to cover everything except the photodiode. None of the current pixel design has metal shielding but the identical result can be achieved experimentally with the use of a focused laser beam. In this section, an argon laser will be used as the only light source to confine the light source to a 2μm diameter spot.

To avoid any light signal affecting other parts of the APS chip other than the photo-sensitive area, an argon laser with spot size of about 2μm diameter was focused on the photodiode center (see Figure 68). The wavelength of the argon laser is 514nm, which is bluish green. This section presents experimental results of testing DAPS using the laser to focus the signal at the middle of the photodiode as well as different segments within the photodiode. The experimental setup discussed in Chapter 4.2 was used. Note that as the laser spot is a Gaussian distribution, there will still be some illumination outside of the photodiode.

Figure 68 below shows the layout of a duo-output APS that is being tested and the relative size of the laser spot in the middle of the photodiode area. This particular pixel is designed by another graduate student Sunjaya Djaja but the measurements were done by this author.

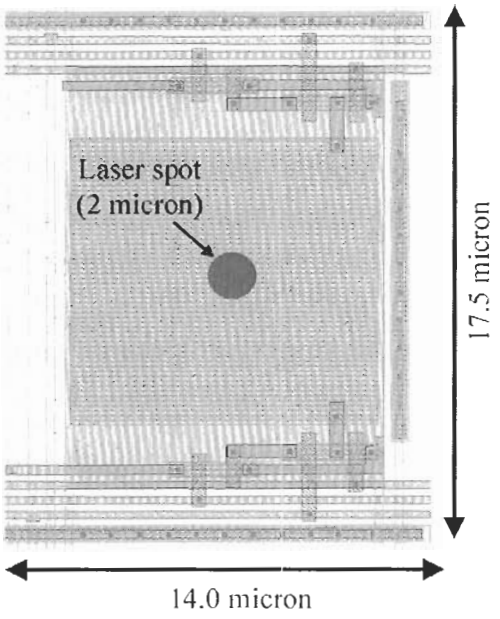


Figure 68 Layout of a DAPS and laser spot in the middle of the photodiode

6.2.1 Constant Laser Illuminated DAPS

In the first experiment, a constant laser beam is focused at the middle of the photodiode of a duo-output APS. Both sides of the DAPS operate sequentially, with one side enabled in phase one and the other side in phase two. Example plots of output 1 and output 2 with three different laser powers are shown in Figure 69 below.

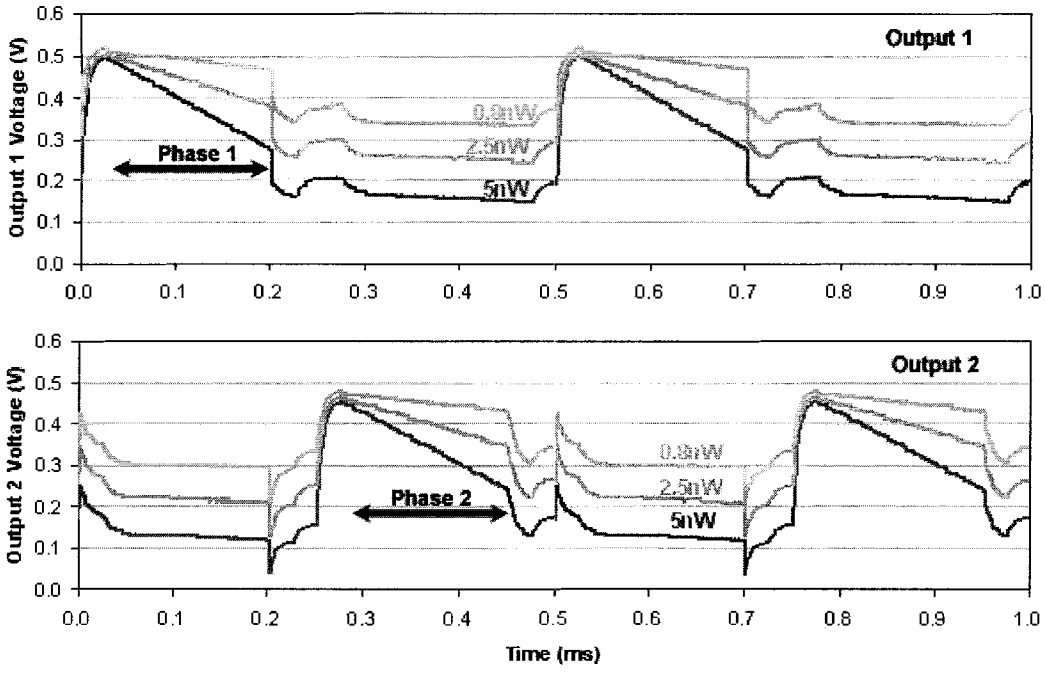


Figure 69 Output of DAPS of side 1 and side 2 (laser spot is focused to the middle of the photodiode with different power levels)

Three different pixels were tested and their average slopes are illustrated below in Table 16. Note that the positive and negative slopes on the first row are within the experimental error of ± 28.6V/s.

Table 16 Average slopes of three DAPS pixels with a focused argon laser beam at constant intensities

Constant laser power	Slope in the 1st phase (± 28.6 V/s)		Slope in the 2nd phase (± 28.6 V/s)		Ratio(ON phase / OFF phase)	
	Side 1	Side 2	Side 1	Side 2	1st phase	2nd phase
0.00 nW	-28.6	0.0	28.6	0.0	N/A	0
0.83 nW	228.6	28.6	28.6	238.1	8.00	8.33
1.42 nW	409.5	38.1	57.1	409.5	10.75	7.17
2.54 nW	685.7	76.2	85.7	676.2	9.00	7.89
3.87 nW	1047.6	95.2	104.8	981.0	11.00	9.36
4.80 nW	1238.1	104.8	95.2	1181.0	11.82	12.40
5.01 nW	1285.7	114.3	114.3	1238.1	11.25	10.83

Table 16 shows that the side that is disabled, i.e. side 2 during the 1st phase or side 1 during the 2nd phase, has a much smaller slope than the side that is enabled. The OFF side is not affected by light as much as before when LEDs were used and voltage can be maintained relatively constant. The ratio of the slope during the ON phase to that during the OFF phase ranges from 7.17 to 12.40, except in the case of no illumination where the slope is zero. Comparing these ratios to those obtained when LEDs were used, which range from 2 to 3, confining the light source to only the photo-sensing area gives much better results in terms of isolating one side while the other side integrates.

Figure 70 below plots the slopes from the above table to illustrate that the output of the side that is disabled is nearly independent on the power of the laser spot being focused on the photodiode. The slight increase in slopes when laser power is increased is due to the Gaussian distribution of the laser as mentioned before, affecting the APS circuitry outside the photodiode.

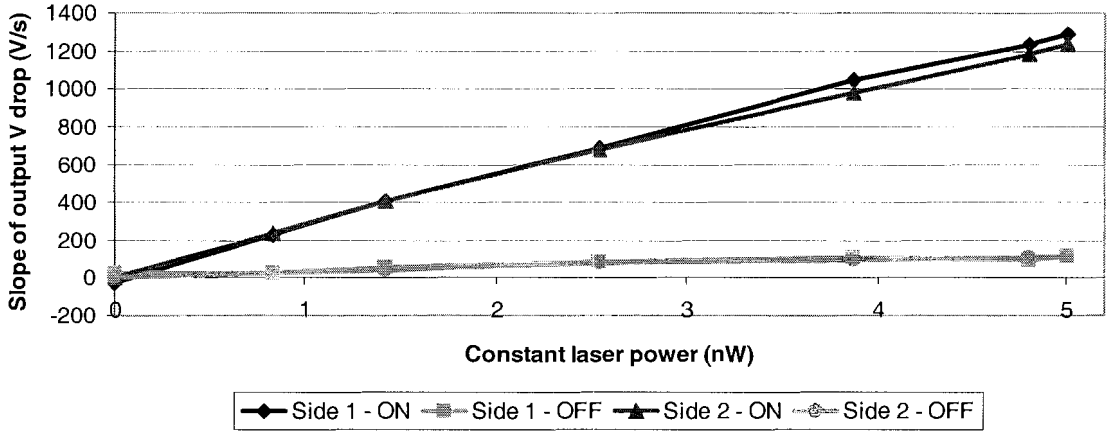


Figure 70 Average slopes of output curves for both sides of the DAPS during different phases against laser power when constant light source is used

This significant difference allows synchronized optical signal to be integrated on one side, while only the background light signal alone integrated on the other side. The next section shows the data for operating the DAPS with a laser spot centered in the photodiode area and synchronized with side 1 along with background light illumination.

6.2.2 Synchronized Laser Illuminated DAPS

Pulsed laser signal can be created with the electro-optical shutter mentioned in Section 4.2. By turning on and off the shutter, optical pulses with controllable power can be formed. In this experiment, the laser signal is synchronized with side 1 of the DAPS, i.e. the shutter is opened to create a higher laser signal only when side 1 is enabled. When side 1 is disabled, the shutter is closed down to allow a smaller signal to go through (1.90nW). This smaller signal acts as a background light signal. Figure 71 below shows the output plots for both side 1 and side 2 when a synchronized laser at different power levels is used.

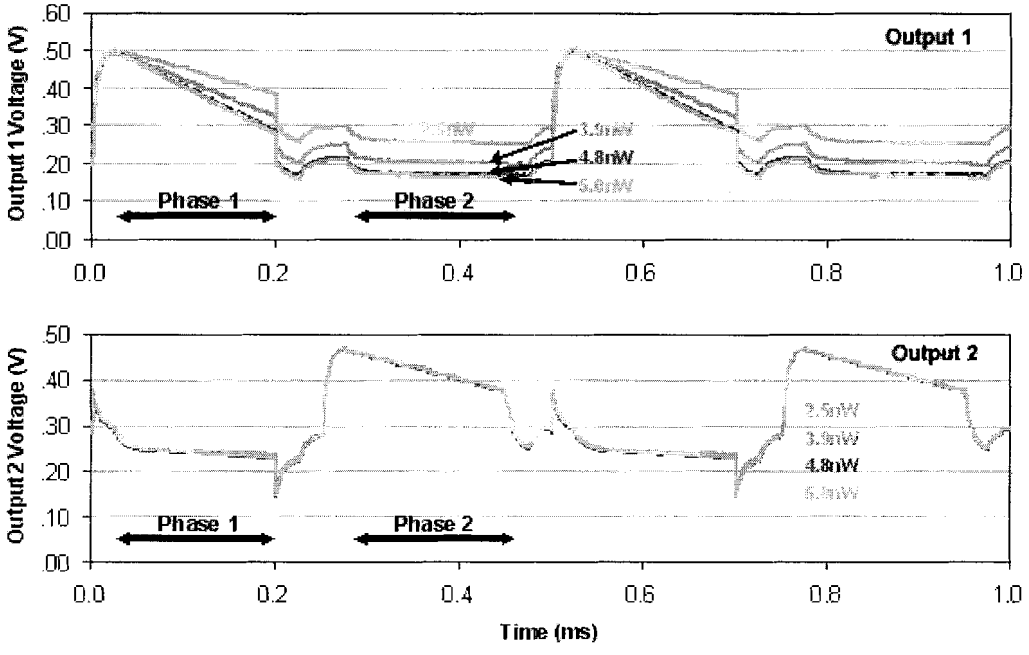


Figure 71 DAPS output plot of both side 1 and side 2 (with a synchronized laser at different power levels)

It can be seen that the charge injection when the enable gates are turned off alters the original output voltage at the end of integration. Section 7.3 presents a possible solution to the charge injection and shows the proposed solution with HSpice simulation. With the electro-optical shutter closed, a minimum laser power of 1.9nW goes through, serving as the background signal and it can be seen that the background level detection (by Output 2) remains constant while

the foreground laser power is varied. With this background signal and foreground power ranging from 2.5nW to 5nw, Table 17 below shows the average results when three different DAPS pixels are tested.

Table 17 Average slopes and their ratios for three DAPS pixels when a synchronized Ar laser signal is focused on the center of the photodiode

ON phase laser power	Slope in the 1st phase (± 28.6 V/s)		Slope in the 2nd phase (± 28.6 V/s)		Ratio(ON phase / OFF phase)	
	Side 1	Side 2	Side 1	Side 2	1st phase	2nd phase
2.54 nW	685.7	76.2	76.2	533.3	9.00	7.00
3.87 nW	1028.6	104.8	57.1	523.8	9.82	9.17
4.80 nW	1247.6	114.3	76.2	523.8	10.92	6.88
5.01 nW	1247.6	133.3	57.1	533.3	9.36	9.33

During phase 1 when the laser power is high, side 2 (OFF side) has a much smaller slope than side 1 (ON side). The voltage drop is higher with higher laser power on side 1 while the light signal is not affecting much the side that is disabled, i.e. side 2. Similarly in phase 2 when the electro-optical shutter is off and the light signal is only 1.90nW, side 1 also has a much smaller slope than side 2. The consistent slopes of side 2 in phase 2 demonstrate the constant light signal during its OFF phase. The ratios between the slope of the ON side to that of the OFF side in phase 1 and phase 2 range between 7 and 10.92, which are much higher than what we obtained when flood illumination is done by LED. Figure 72 below shows the plot of output slopes against laser power for both sides of the DAPS in both phase 1 and 2.

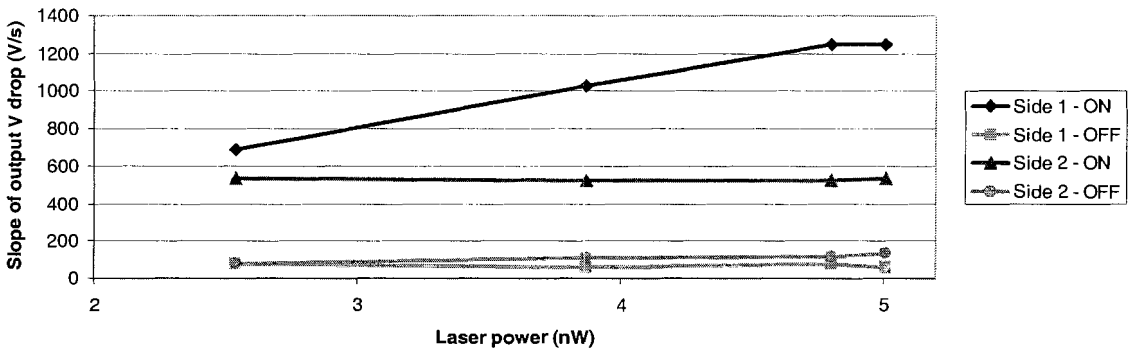


Figure 72 DAPS slope of output curve vs. laser power when light is synchronized with light source

It can be seen from Figure 72 that as the laser power increases, only the slope of side 1 during the ON phase increases. The amount of voltage drop during phase two for both side 1 and 2 is relatively constant regardless of the laser power in the first phase. Side 1 has close to zero slopes because enable gate 1 is off and side 2 has consistent slopes of about 500V/s because it integrates a constant background illumination of 1.90nW.

We can conclude from this experiment that, when a light signal is confined to the photodiode of the duo-output APS, background light elimination is feasible. In an environment where background illumination is present, a laser-APS-system can distinguish a bright spot produced by a shiny area reflecting the background signal from one produced by the reflection of the laser. When a DAPS detects a surface with constant high signal, i.e. a shiny bright area, the output from phase 1 (output1) and phase 2 (output 2) will be identical. The difference of these two outputs will be zero.

On the other hand, when another area is illuminated by the encoded laser, regardless of the reflectivity of the surface, the two sides of the DAPS will have different outputs. In the first phase where the laser signal and the background are present, the output from side 1 would be higher than the output from side 2 after phase two, where there is only the background

illumination. Thus the laser signal can be identified independent on the surface of the area being detected and the background illumination level.

Further investigations are carried out to find the response of the pixels with respect to the location of the light spot on the photodiode area of the duo-output APS.

6.3 Pixel Response on Different Part of Photodiode

Given the results of section 6.2, the question is where, on the pixel, does illumination cause this crosstalk effect. Since the laser spot is quite confined, we can use changes in its location to identify the areas causing problems. The response of the pixel with respect to the location of the laser spot is obtained by moving a laser spot with constant power on the photodiode area. With the help of the x-y table, a 2μm-diameter laser spot is positioned accurately and is moved on the photodiode area with steps of 1μm. Figure 73 below shows the laser spot movement relative to the photodiode on a DAPS. The following sections discuss the response of the pixel with respect to the following movement of the laser: (a) moving horizontally along the center of the photodiode, (b) moving vertically along the center of the photodiode, (c) laser moving horizontally near the output circuit of side 1, and (d) laser moving horizontally near the output circuit of side 2.

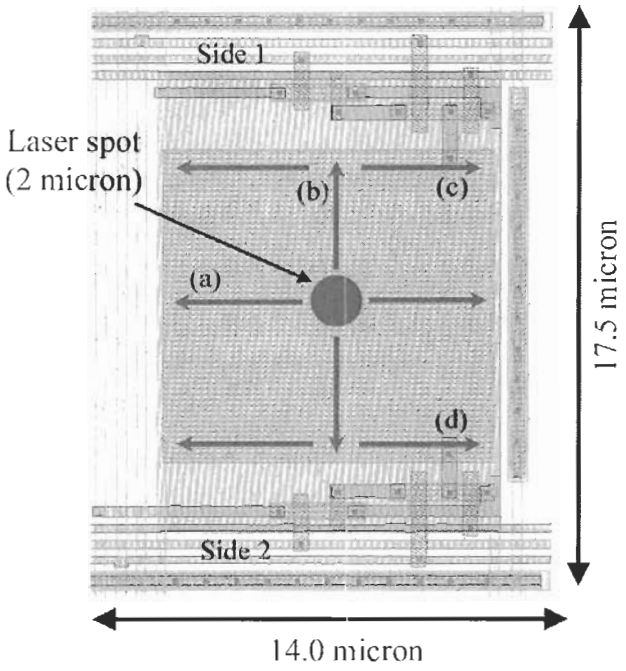


Figure 73 DAPS pixel response with respect to different locations of the argon laser spot on the photodiode area

6.3.1 DAPS Pixel Horizontal Spot Movement at the Photodiode Center

Figure 74 below shows the output plots of side 1 and 2 for both phases averaged over two independent DAPS pixels when a laser spot with constant power is moved horizontally along the middle of the DAPS with a 1μm step, as in (a) in Figure 73. The output voltage (V) is plotted here instead of the slope but they are identical because the slope is simply the output voltage divided by the integration time, which is constant for all the results shown throughout this thesis.

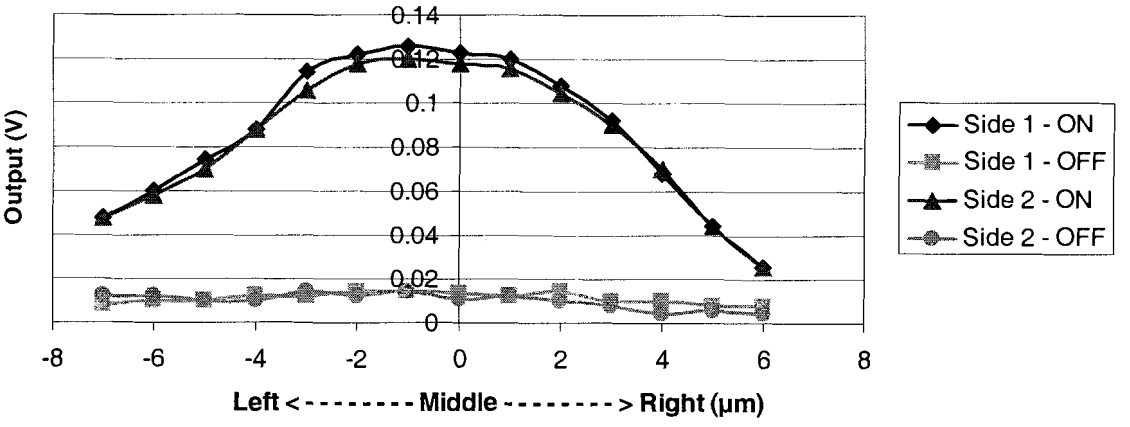


Figure 74 Output plot of a DAPS when a laser spot is moved from left to right along the middle part of the pixel – (a) in Figure 73

It can be observed that during the OFF phase (side 2 in the 1st phase and side 1 in the 2nd phase), the output is relatively low and independent of the location of the laser spot. This is expected as it was shown in the last section that the side that is disabled does not pick up light signal. However, it does show the problem must occur along the top or bottom photodiode edge.

On the other hand, during the ON phase for both side 1 and 2, the pixel output is maximum when the laser spot is right at the middle of the pixel. Since a laser spot has a Gaussian shape, as the laser move away from the center horizontally, we can see from the layout in Figure 73 that some of the laser power is lost to the metal lines on either side of the DAPS pixel. Therefore, the response of the pixel should be highest when the laser spot is in the dead center of the photodiode.

6.3.2 DAPS Pixel Vertical Spot Movement at the Photodiode Center

Figure 75 below plots the average output of two independent DAPS pixels when the laser spot with constant power is moved vertically along the center of the photo-sensing area with a 1µm step, shown in (b) in Figure 73.

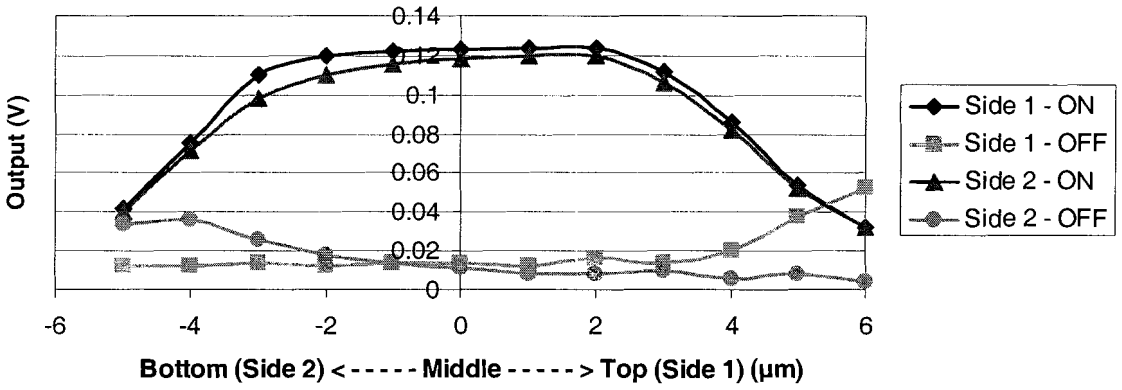


Figure 75 Output plot of a DAPS when a laser spot is moved from top to bottom along the center of the pixel – (b) in Figure 73

During the ON phase, i.e. side 1 in the 1st phase and side 2 in the 2nd phase, the output is at maximum when the laser spot is in the middle. Similar to the case when the laser spot is moved horizontally, the output falls when the laser spot moves away from the center.

During the OFF phase, unlike in the case when the laser is moved horizontally, the outputs change depending on the location of the laser spot. The output of side 1 during its OFF phase (i.e. 2nd phase) is steady when the laser spot is moved from the bottom to the center of the pixel.

However, when the laser gets closer to the top part of the pixel, where the output circuitry for side 1 is, output 1 increases even when the enable gate is off. Similarly, during output 2's OFF phase (i.e. 1st phase), the output remains steady until the laser spot gets closer to the bottom part of the pixel, which is where the circuitry for output 2 is. These two observations suggest that the laser light is affecting the output circuitry for either the top or the bottom part of the pixel. This is consistent with our previous observation that when we have an LED flood illuminating the entire APS sensor chip, one side of the duo-output APS cannot be isolated even the enable gate is

turned off. It confirms that it would be necessary to use metal shielding to cover the area other than the photo-sensing area for the DAPS to operate properly.

6.3.3 Pixel Response near Output Circuitry of the Pixel

It was observed in the last section that if the optical signal is close to the output circuit, the ON phase output of that side is reduced while the OFF phase output is increased. In order to study how the outputs are affected, a laser spot with constant power is moved horizontally along the top and bottom part of the photodiode very close to the output circuit, shown in (c) and (d) in Figure 73. The average result of two independent pixels is shown in Figure 76 below when the laser spot is at proximity to the output circuit of side 1, i.e. the top part of the photodiode.

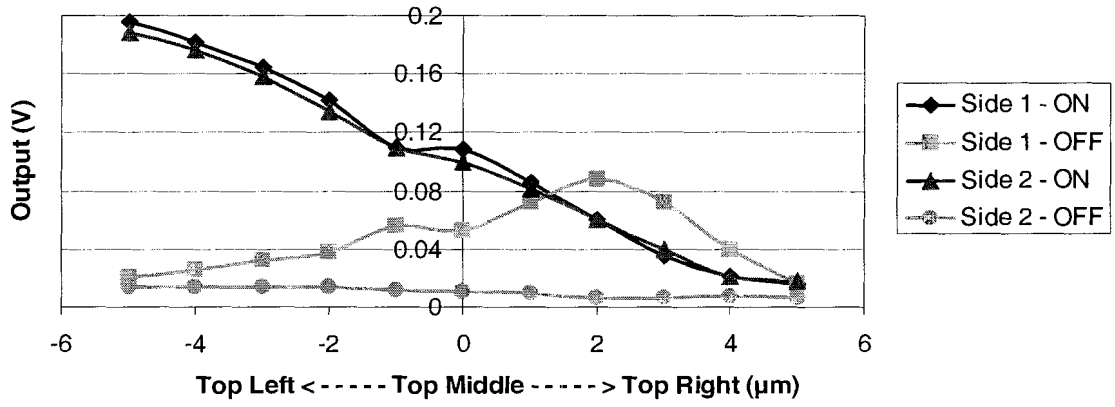


Figure 76 Output plot of DAPS when the laser spot is moved horizontally along the top part of the pixel

During the ON phase for either side, as the laser spot moves from the center to the right, the output signals drop. This is consistent with the results observed before as more laser signal is lost to the metal lines. However, as the laser is moved to the left, the outputs increase and these outputs are even greater than that when the laser is at the dead center of the photodiode. It is suspected that some of the laser power is affecting a sensitive region of the output circuits.

For the OFF phase, side 2 is not affected by the location of the laser spot because the laser is close to the output of side 1. On the other hand, the output of side 1 fluctuates greatly because the laser signal disturbs the output circuit. Therefore the laser is affecting the side 1 output even when the enable gate is off.

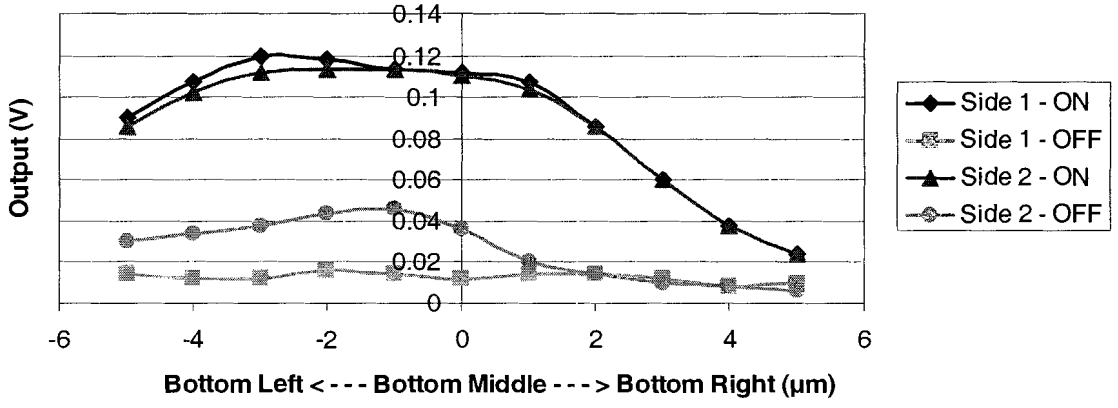


Figure 77 Output plot of DAPS when the laser spot is moved horizontally along the bottom part of the pixel

When the laser spot is close to side 2 (bottom of pixel), Figure 77 shows the results below. For the ON phase, both outputs drops as the laser spot is moved away from the center to either the left or the right and this is consistent with our previous observation. For the OFF phase, side 1 is not affected by the location of the laser because the laser is at proximity to the output 2 circuit. Therefore, we can see a fluctuation on side 2 output. Although the extent to which the laser affects the side 2 output is less than that when the laser is near the top of the photodiode, it can be due to experimental discrepancy.

Due to the complication of the carriers moving within the semiconductor, it is difficult to gain a full understanding of how the location of the laser spot affects the response when it is close to either output 1 or output 2. However, it is important to realize the implication of the experimental results that optical shielding of the enable/output circuitry of the pixel is necessary.

It might also be helpful to put a guard ring type of protection (diffusion area grounded) around the pixel to reduce noise from undesired sources.

6.4 Summary

Duo-output active pixel sensors have been designed and fabricated using CMOS 0.18 micron technology. The specially designed pixel eliminates background illumination from the environment to enhance foreground signal detection by the sensor. In a non-ideal environment or on a non-ideal object surface, an optical scanning system could either detect an undesired signal or miss a desired signal. The duo-output APS, having two output paths, first integrates a desired optical signal along with the background to one path in the 1st phase, and then integrates the background alone to another path in another phase. When the integrated signal in phase 2 is subtracted from that in phase 1, the foreground optical is obtained free from the background illumination. When the difference of the two outputs is zero, it indicates no optical signal present.

This chapter has presented the experimental results from using light emitting diodes and an argon laser as the major optical sources. Results from the LED testing suggest that, because the output circuitries are not shielded, the ability of the foreground-background subtraction was greatly degraded. By using a focused laser beam, on the other hand, the results were significantly improved because the laser signal is not affecting the output circuitries when it is focused only on the photodiode area. Further investigations of the pixel response with respect to the location of the laser spot within the photodiode were shown. A focused laser beam is moved within the photodiode area and the outputs are recorded. Results affirm the necessary shielding outside the photodiode area to improve performance of the DAPS. More precise experiments are necessary to study the effect of laser on different section on the photodiode. Future works include improving the DAPS design, creating a fully functional array of DAPS, and testing of the fully functional DAPS array in a real world situation for an industrial application.

7 CHAPTER SEVEN – SIMULATION

This chapter presents the simulation results of the photodiode and photodiode-type APS' using HSpice provided by the Canadian Microelectronics Corporation. Simulation provides a useful basis for the design of the APS' and a comparison to experimental results in Chapter 6. The geometries of various pixel components are decided based on the simulation results. A simulation model for the simple photodiode has already been discussed in Chapter 2. In the first section of this chapter, the photodiode model is combined with the output circuit of a simple photodiode APS and the simulation of this simple pixel will be illustrated. Section 7.2 compares the simulation results between the simple photodiode APS and the 4-T photodiode APS. Section 7.3 presents some preliminary simulation results of the duo-output APS in order to verify several important observations made in Chapter 6. The last section of this chapter proposes a method along with the simulated results to eliminate charge injection for future DAPS pixel designs.

It should be emphasized at the beginning that simulation of photo-sensors is different from simulation of traditional electronics circuits. Many photoelectric effects cannot be simulated by HSpice. The simulation model of the APS is not perfect and it can only provide a first order approximation. Hence, the simulation results do not reflect the reality precisely quantitatively or qualitatively. Simulation tools that have the ability of simulating photo-response, such as Monte Carlo, might provide more reliable simulation results but it was not available to the author.

7.1 Simulation of Simple Photodiode APS

Combining the photodiode model presented in Chapter 2.3.2 with the active pixel sensor circuit, we obtain the following schematic in Figure 78 for simulation.

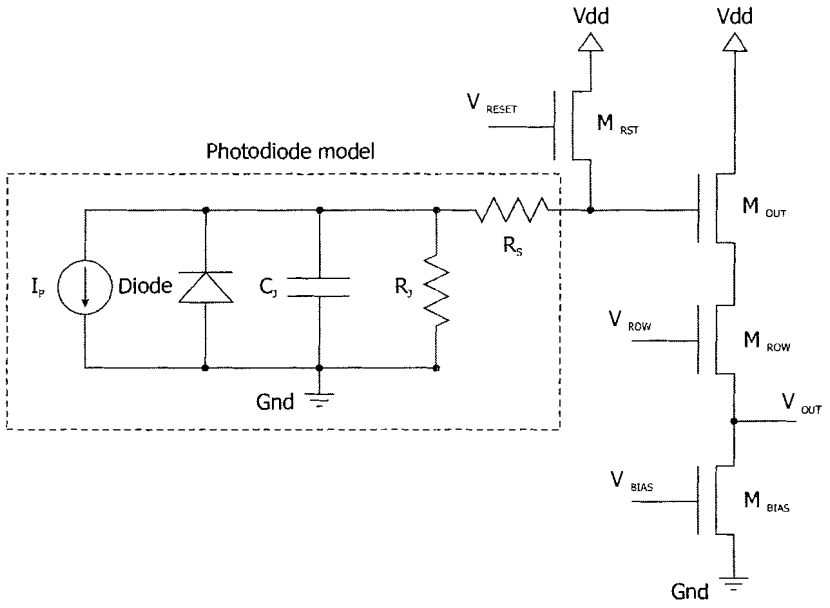


Figure 78 Photodiode APS schematic for simulation

From Chapter 2, we know that the photocurrent I_p can be calculated by:

$$I_p = \frac{q\eta P_{opt}}{h\nu} = \frac{q\eta P_{opt}}{hc/\lambda} \tag{9}$$

where,

I_p = photo current per area

q = electronic charge = $1.602\times10^{-19}\,C$

η = quantum efficiency

P_{opt} = optical power

h = Planck's constant = $6.6262\times10^{-34}\,Js$

ν = frequency

c = speed of light = $3\times10^{8}\,m/s$

λ = wavelength

If we take λ = 550nm near the middle of the visible spectrum, from [13], the absorption coefficient α is approximately $0.38\mu m^{-1}$. If the depth of the pn-junction is assumed to be z, from

equation (1) in Chapter 2.1.1, we know that the power of an optical signal is reduced to $e^{-\alpha z}$ of the original. Therefore, the power of the light is reduced to 37% of the original at a depth of 1/0.38μm, i.e. 2.63μm. In other words, 63% of the light power gets absorbed at a depth of 2.63μm. In a vertical pn-junction arrangement, however, the situation is more complicated because the collection of photo-generated charges happens within the depletion region, which extends above and below the junction. Moreover, in reality, other factors would also play a role, such as the reflectivity of the diode. This uncertainty is an example of the non-ideal APS model, which can only provide a first order approximation to the photocurrent, I_p.

The argon laser has a wavelength of 488nm for power under 1W and a wavelength of 514nm for power over 1W. Their absorption coefficients are approximately $1.02\mu m^{-1}$ and $0.78\mu m^{-1}$ respectively [13].

The junction capacitance, C_J, is the parasitic capacitance of the photodiode. From equation (9) in Chapter 2.3.2, we know that the junction capacitance changes during the integration as the voltage across the diode, V_{DB}, changes. V_{DB} ranges from the reset voltage VDD-V_{TH}, to a minimum of $V_{BIAS}+V_{GS}$ for an APS to remain in the linear operating region [62]. V_{TH} is the threshold of the reset transistor and V_{GS} is the gate-source voltage of the readout transistor. A Maple plot shows the junction capacitance variance with V_{DB} in Figure 79.

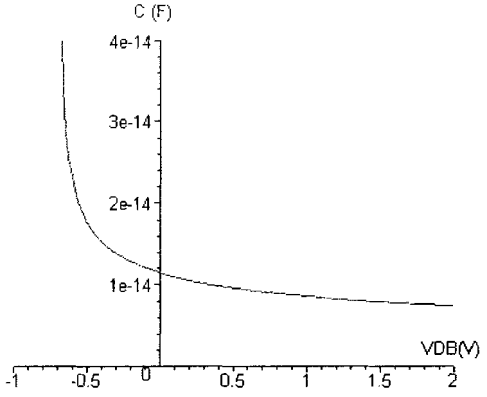


Figure 79 Maple plot of photodiode junction capacitance against voltage across the photodiode

It is shown that the junction capacitance does not vary drastically within the linear operating region. Thus a constant junction capacitance is chosen for the photodiode model described in Figure 78. The series resistance, R_S, and the junction resistance, R_J, were discussed in Chapter 2.3.2.

7.1.1 Size of Bias Transistor

The bias transistor plays an important role in the APS as it governs the amount of current that is being sunk (which in turn determines the power consumption) and it also determines the range of the output voltage as mentioned in Chapter 2.4.1. Moreover, the linearity of the APS is dependent on the size of the bias transistor because channel length modulation would be significant for a bias transistor with a short channel.

With all the above parameters, the model in Figure 78 is simulated using HSpice. Similar to the way a pixel is monitored during experiments, the row select of the pixel is kept on to monitor the pixel output during the entire cycle. The gate of the bias transistor is biased at 0.55V. A sample of the HSpice file can be found in Appendix A. The pixel is reset at a frequency of 1 kHz and two pixels with two different bias transistor sizes are simulated with result shown in Figure 80 below.

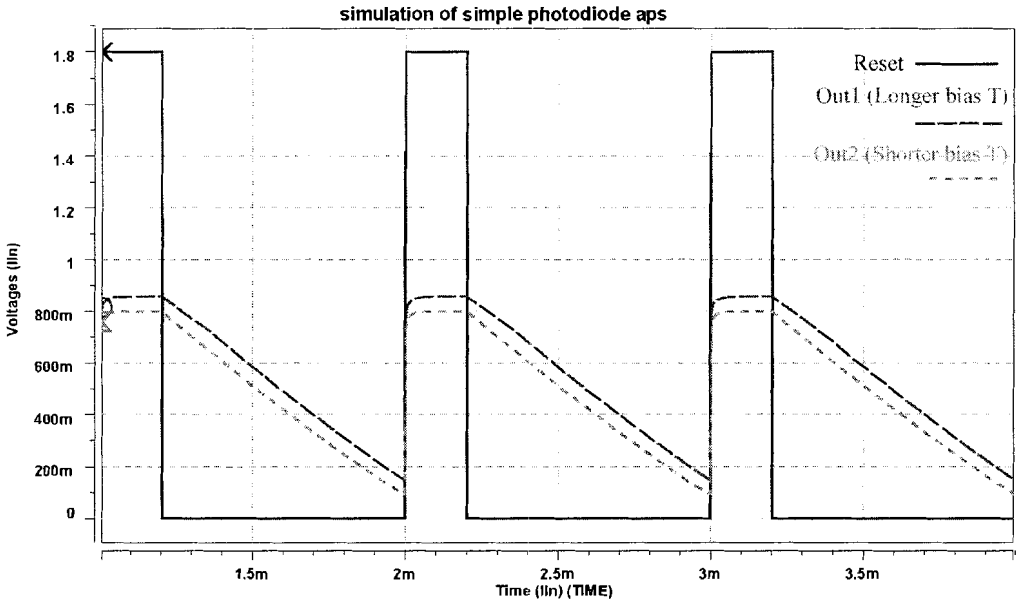


Figure 80 Simulation of photodiode APS at 1 kHz reset rate

The above figure illustrates the reset signal and two outputs for two APS' that have different bias transistor sizes. When the reset signal is high, both outputs are maintained at a fixed reset level. When reset is turned off, integration starts and both outputs drop at the same rate because the photocurrent is identical. The APS that outputs *Output 1* has a bias transistor with longer channel length (4.0μm) than that of the APS that outputs *Output 2* (0.5μm), thus sinking a smaller current. Figure 81 below shows the current going through the two different bias transistors.

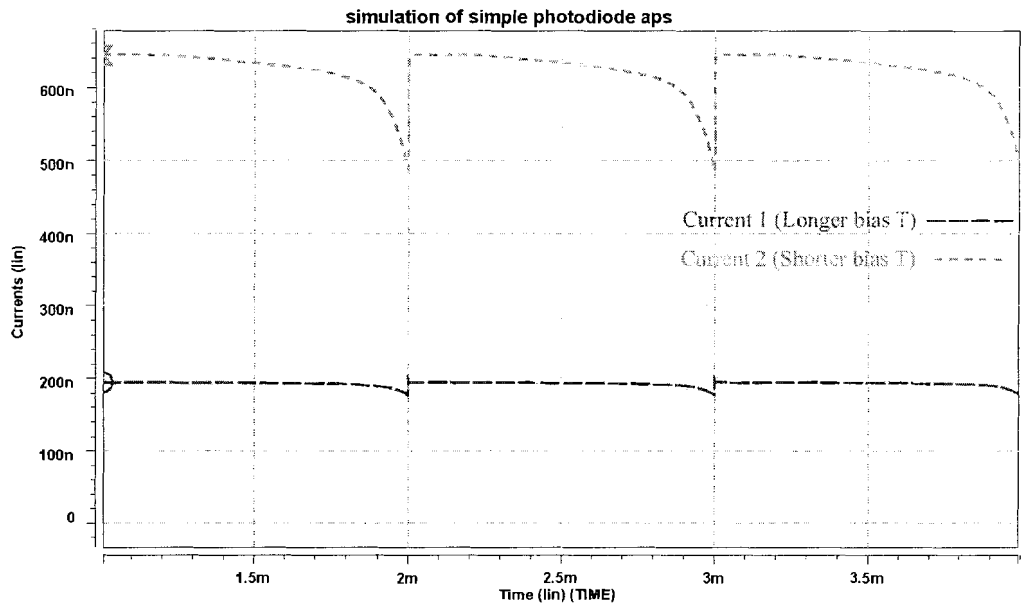


Figure 81 Bias current of two APS' with different bias transistors

The bias transistor with shorter channel sinks a larger current, *Current 2* above. At the very beginning of the integration, both currents are relatively constant but *Current 2* starts to decrease after approximately a quarter of the phase. *Current 1* remains constant until near the end of integration as it enters a non-linear region. Thus, the region where the current is constant is shorter for *Current 2* than for *Current 1*. This is due to the effect of channel length modulation for shorter transistor channel length of the bias transistor. Thus dynamic range is reduced because the region where the transistor operates linearly is reduced. It should be kept in mind that simulation does not give a very accurate representation of how real devices behave, especially when simulating photonics devices that are not entirely electrical. Certain parameters in photonics devices are not simulated, such as penetration depth of the optical signals, cross talk from pixel to pixel, and the effect of the optical signals on other parts besides the photo-sensing area. Nevertheless, simulation does give a general outlook of how the APS device operates.

7.2 Simulations of Simple PD APS vs. 4-T Photodiode APS

As mentioned in Chapter 2 for the 4-T photodiode APS, an extra timing control is required for the additional shutter transistor. Two arrangements are possible to implement this additional transistor and the timing control of the reset transistor depends on where the reset transistor is located. If the reset transistor is connected to the gate of the output transistor, as shown in Figure 82 (a), the enable transistor separates the photodiode and the readout gate; therefore the reset transistor can remain on during the integration. On the other hand, if the enable transistor is connected to the photodiode, as shown in Figure 82 (b), the reset transistor must be off during the integration.

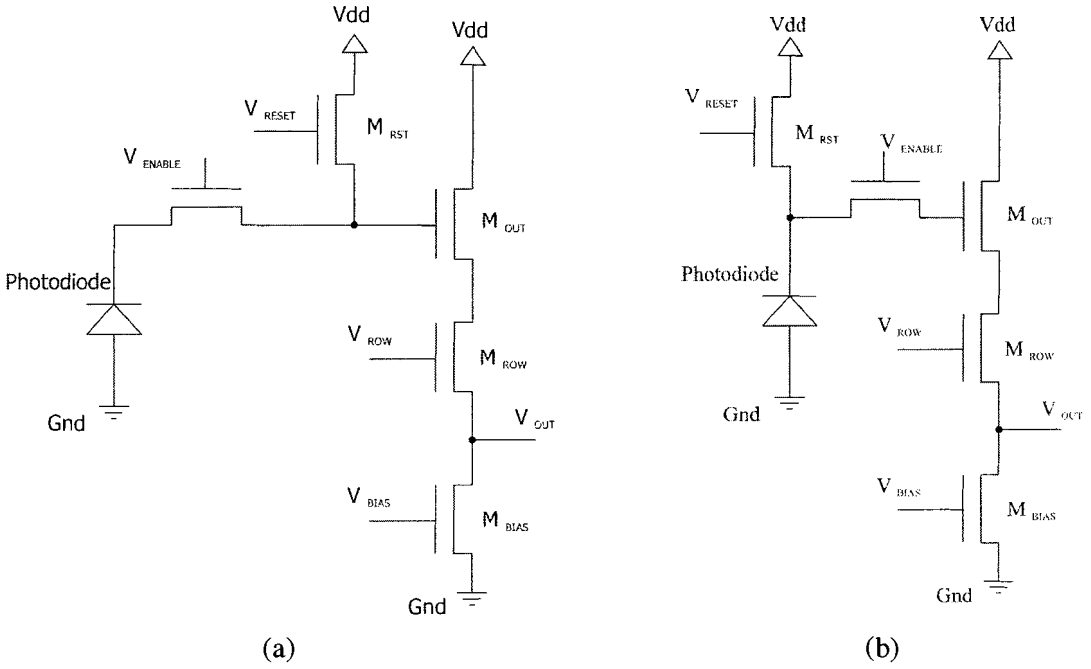


Figure 82 Photodiode Active Pixel Sensor with shutter (4-T APS) – (a) reset transistor located at the gate of the readout transistor and (b) reset transistor located at the photodiode

As a result, the voltage of the readout node in schematic (a) above can be kept constant at the reset level until immediately before readout at the end of the integration. This minimizes any effect on the readout transistor, such as time-constant decay or effect of light on the readout transistor if there is any of these two.

Moreover, it was suggested that since the source of the reset transistor introduces an extra parasitic capacitance to the readout node, sensitivity is increased [63]. Thus the scheme where the reset transistor is at the gate of the readout transistor, i.e. Figure 82 (a), is preferable. Figure 83 below shows the timing diagram for this 4-T PD APS.

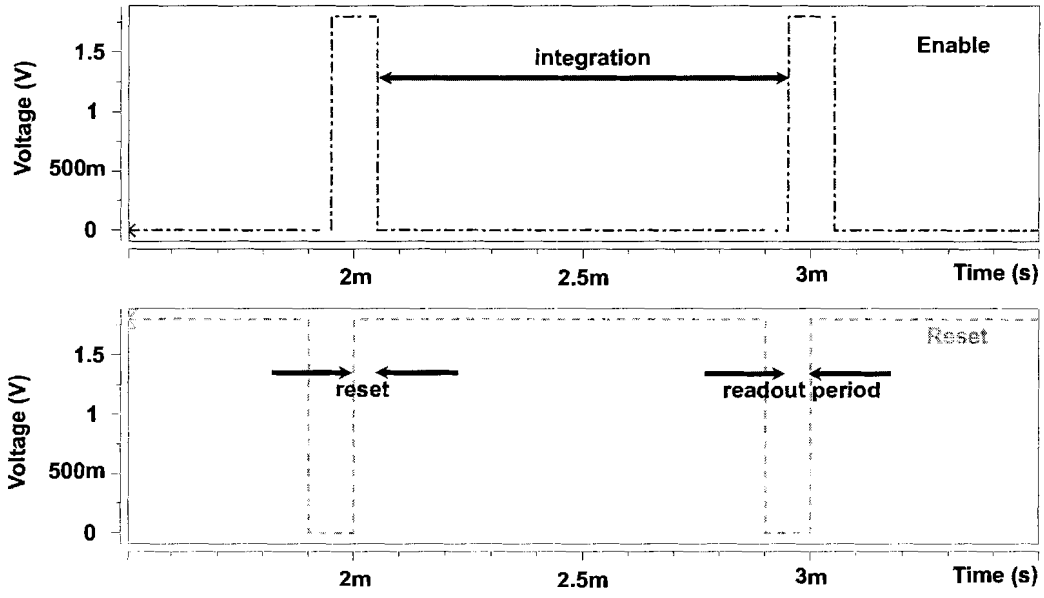


Figure 83 Timing diagram for the first version of 4-T PD APS in Figure 82 (a)

At the beginning of the integration, both the reset and enable transistors are turned on to reset both the photodiode and readout transistor gate. The enable transistor is then turned off and the integration starts at the photodiode while the reset remains on during the integration to maintain a fixed reset voltage at the output node. This is achieved by the shutter transistor isolating the integration node from the output node. At the end of the integration, i.e. right before the readout, the reset transistor is turned off and the enable transistor is turned on to output the signal.

The timing signal illustrated in Section 2.4.1 for the simple photodiode APS is plotted in Figure 84 below one more time. It simply has one reset timing control and is identical to the 4-T APS reset signal.

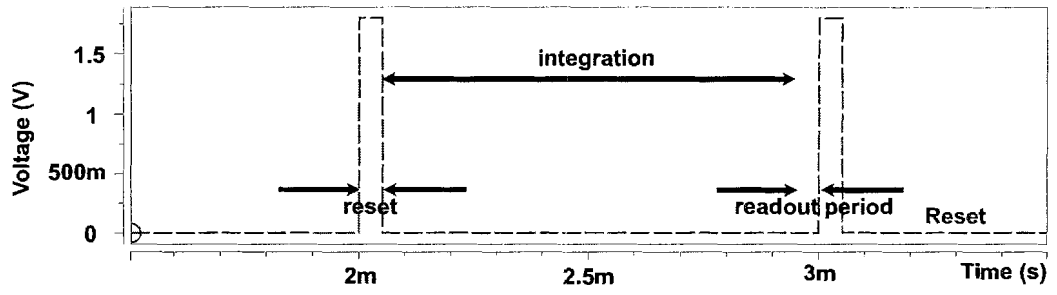


Figure 84 Timing diagram for simple PD APS

Integration for this APS happens between two reset pulse and readout is performed at the end of the integration before reset is performed for the next cycle. Figure 85 below shows the simulation results of the voltages at the photodiode node and at the output node on a simple PD APS and a 4-T PD APS.

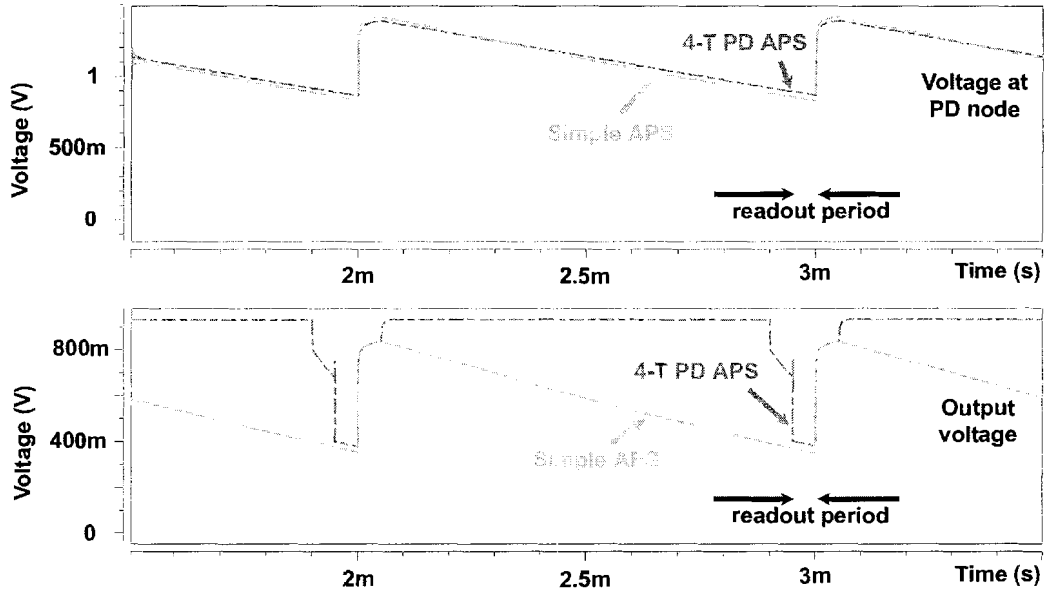


Figure 85 Simulation of simple PD APS and 4-T PD APS showing (a) voltages at photodiode node and (b) output voltages

It can be observed that the final outputs are virtually identical. The slightly smaller drop of the 4-T photodiode APS is due to a small extra capacitance from the source of the shutter transistor.

Since the reset transistor for the 4-T PD APS remains on and shutter remains off until the end of the integration, the gate of the output transistor remains at a reset voltage until reset is turned off and shutter is turned on for readout. The most important result here is that during the readout period, the output of the 4-T PD APS behaves almost identical to the output of simple PD APS, with a slight difference which has already been addressed. This simulation result proves the concepts of the shutter performing correctly as anticipated and establishes a solid background for the development of the duo-output APS.

7.3 Simulation of Duo-Output APS

The duo-output APS in Figure 34 from Chapter 3.3.4 is simulated using HSpice with the photodiode model identical to that in Figure 78. The purpose of the simulation in this section is to verify several observations made from experiments in Chapter 6. The DAPS will be simulated with only single side operating as it gives us sufficient information for important issues that need to be addressed.

In the first set of simulation, one of the two enable gates remains off for the entire cycle while the other is turned on normally during phase 1. This setup is similar to the simple 4-T photodiode APS discussed in Section 7.2. The photocurrent is kept constant to represent a constant light signal throughout the entire cycle. Figure 86 below shows the timing diagram of the input signals and three simulated output plots of side 1, resulted from three different photocurrents, which are equivalent to different light intensities in simulation. The output on side 2 is not shown as *Enable 2* is kept at low, thus side 2 is disabled.

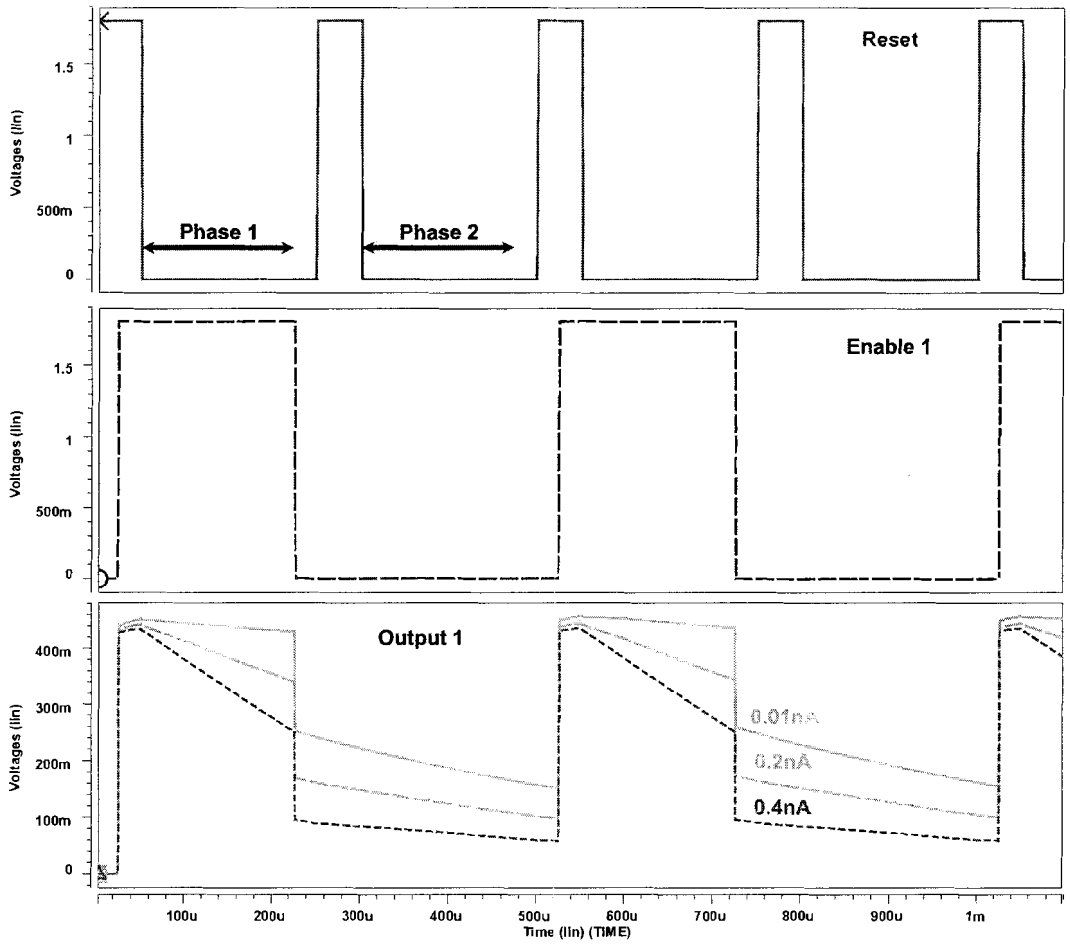


Figure 86 Input and simulated output signals of a duo-output APS when only one side operates and photocurrent is constant throughout the integration cycle

The reset signal goes high before the integration for the first phase. Afterwards, *Enable 1* goes high. Similar to the 4-T APS, once *Enable 1* goes high, the gate of the readout transistor and the photodiode node is reset. When *Reset* is off, integration of phase 1 starts and the output signal starts to drop at a rate according to the light intensity. It shows that the side being enabled during phase 1 operates similar to the simple 4-T photodiode APS. It is not shown in the figure but enable 2 stays at 0V in order to disable one side of the duo-output APS.

One important observation in the above result is that charge injection occurs whenever *Enable 1* is switched off. In a given technology and transistor geometry, the amount of charge injection mainly depends on the voltage at the photodiode node when the enable gate is turned off

[64]. Therefore the charge injected in turns depends on the light intensity during the integration. This observation agrees with our experimental results from Chapter 6. Omission of charge injection can be done by adding one extra transistor [64] to the APS. The next section will discuss the simulation results with charge injection cancellation. In Chapter 6, we also saw an output voltage jump when the reset transistor is turned on or off but it does not happen at all in simulation. It confirms our suggestion in Chapter 6 that the voltage jump is due to noise coupling through the substrate when reset and readout transistors are close together.

Another important observation here is that the output signal continues to drop even after the enable gate is shut off, which is also consistent to our experimental results. It is undesired because we would like to keep the signal until the end of the second phase and perform a differencing operation. However, slightly different results were obtained from experiments. The voltage drop during the OFF phase in experimental data shows a strong dependency on the optical signal present. A stronger optical signal results in more voltage drop. In simulation, a reverse of this scenario is observed.

In Chapter 6, it was concluded that the voltage continues to drop during the OFF phase because the optical signal is affecting other parts of the pixel. In the simulation however, photonics effects are not taken into consideration for the optical signal affecting area outside of the photo-sensitive area. In order to investigate further for the voltage drop in the last simulation, another simulation is performed, where the light source is turned off during phase 2. Figure 87 below superimposes the outputs of three different light intensities for the two cases – constant light signal throughout the entire cycle and synchronized light signal where the light is only on during phase 1.

All the three outputs with different synchronized light intensities show virtually no difference compared to those outputs with constant light intensities. This is contradictory to our experimental results that when the optical signal is off during the OFF phase, the voltage remains

constant. It can be argued that the voltage drop during the OFF phase in the simulation is due to RC constant decay. In fact, by increasing the capacitance at the gate of the readout transistor, it was found that the voltage drop is reduced. Although RC constant decay was not observed in experimental results, it is emphasized again that simulation of photo-detector as a pure electrical device only provides a first order approximation of the behaviour of a real photonics device.

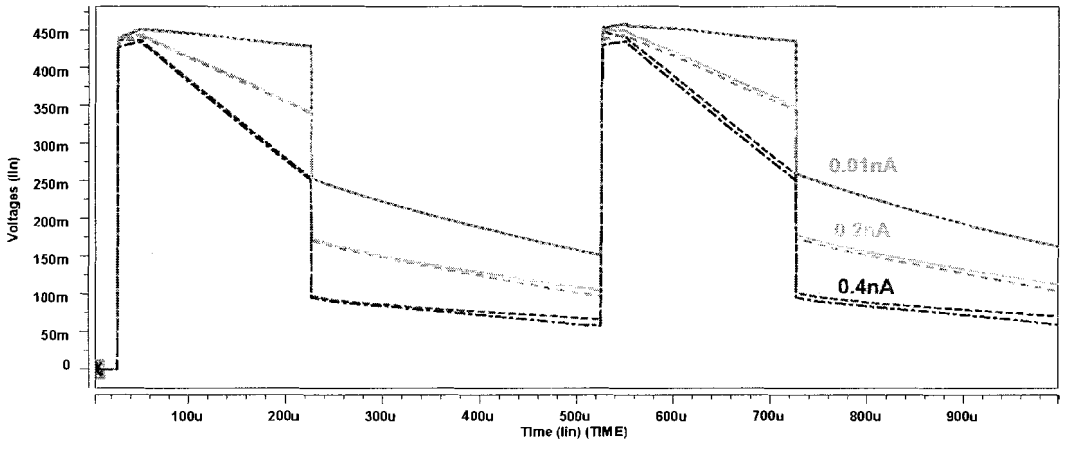


Figure 87 Output signals of a duo-output APS when one side is kept turned OFF showing virtually no difference between two light signals: a) constant light source and b) synchronized light source

From the above results, since the optical signal does not affect the voltage drop when the enable gate is off, it re-confirms one of our conclusions that the voltage drop is not due to the leakage through the enable gate to the photodiode and that the enable gate does isolate the photodiode node from the gate of the readout transistor.

7.4 Charge Injection Cancellation

As it was seen in this chapter and in Chapter 6, charge injection from the enable transistor potentially inhibits the functionality of the duo-output APS. When the enable gate is on and the V_{DS} across the enable gate is small, a charge Q in the inverted channel exists under the gate oxide. When the enable gate is turned off, half of this charge is injected into the photodiode while half of it is injected to the gate capacitance of the readout transistor. This creates a sudden jump in the

output voltage whenever the enable transistor is switched off and therefore corrupting the signal stored at the output node [64].

Cancellation of charge injection can be achieved by placing a dummy switch between the enable transistor and the readout node, i.e. the gate of the readout transistor [64]. Figure 88 below shows the concept.

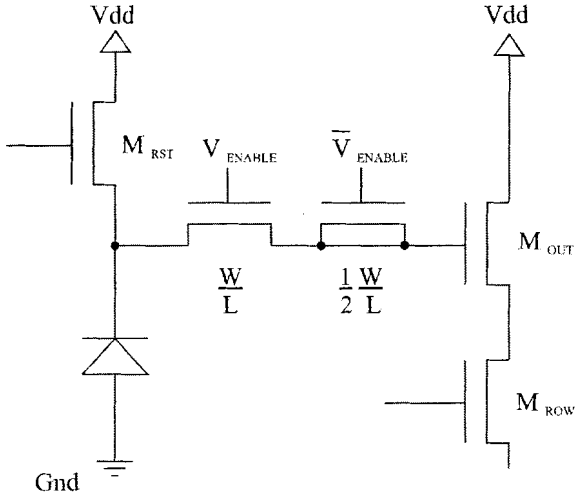


Figure 88 A dummy switch is inserted between the enable transistor and the gate of the readout transistor of a 4-T APS to reduce charge injection

The dummy switch has the drain and source shorted and is one-half the size of the original enable transistor, which has a size of more than two times the minimum geometry. The input signal to the dummy is a complement of the input to the enable transistor and it is slightly delayed. This dummy transistor's role is to offset the effect of charge injection. As it was mentioned before, when the enable transistor is turned off, half of the charge in the channel is injected to each side (source and drain). The dummy transistor only requires half the size of the enable transistor to generate a total charge equal to that injected by the enable transistor because the drain and the source of the dummy transistor is shorted.

The cancellation of charge injection was simulated using a duo-output APS with single side operation. A 1μs delay for the complement input to dummy switch was used and the results

of the operating side are plotted below in Figure 89. Three different light intensities, i.e. photocurrents, were used with intensities shown in the figure.

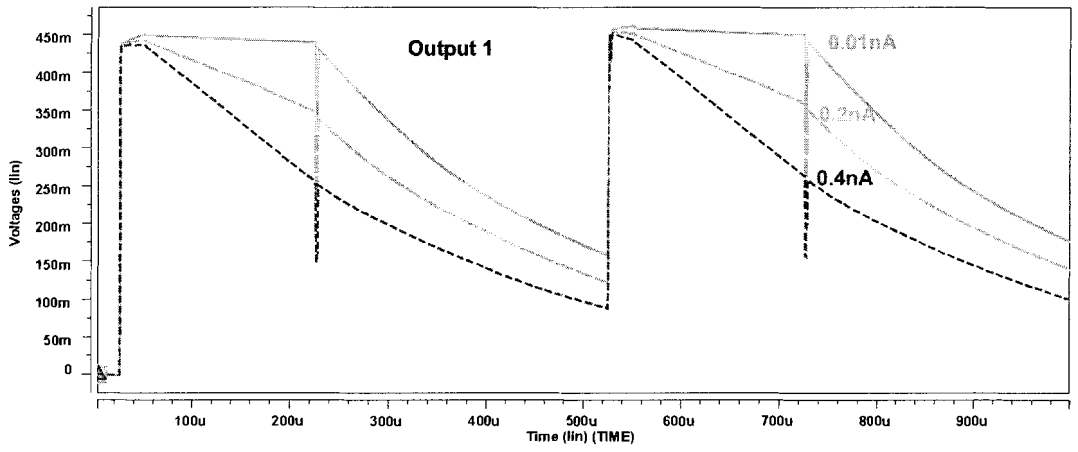


Figure 89 Output after charge injection elimination

Figure 89 above is compared to the simulation results for the DAPS with single side operation but without charge injection reduction in Figure 86. Figure 89 shows that a spike occurs whenever the enable gates switches state. However, at the end of the spike, the output returns to its original value. This spike suggests that, despite of the effect of charge injection from the enable transistor, the charge injection from the dummy transistor offsets this effect.

Therefore, charge injection can be cancelled with the cost of an additional transistor and signal line, meaning a reduction in fill factor and more complex circuit. However, in a 1-dimensional array, fill factor is not of major importance for a lot of the profile scanning application mentioned before. Therefore this implementation is valuable to specialized sensors. Charge injection cancellation was not implemented in any of the pixel design but the above simulation results suggest that it should be considered in future designs. In fact, another group of graduate students have already submitted the improved APS designs with charge injection cancellation for fabrication.

Another method mentioned in [64] involves the use of a CMOS transmission gate, i.e. an NMOS transistor in parallel with a PMOS transistor, to replace the enable gate transistor. The PMOS transistor complements the NMOS transistor so that the voltage change is cancelled out. However, this method requires an n-well for the PMOS transistor, which requires a much larger area. Moreover, it requires a very precise control of the clock signals that both the transistors are switched at exactly the same time [64]. Nevertheless, it might be worthwhile to implement this to future DAPS' because, once again, the area of the linear array is not an important issue.

7.5 Summary

This chapter has presented HSpice simulation to verify various experimental results obtained mainly in Chapter 6. Simulation of a simple photodiode APS was first presented to illustrate how the size of the bias transistor was decided. Two different ways of implementing the 4-transistor APS were then simulated and compared to the simple PD APS. It is preferred that the reset transistor is placed at the gate of the readout transistor instead of the photodiode node. Simulations showed that this 4-T APS behaves very similarly to the simple PD APS.

The duo-output APS was also simulated to verify some of the experimental results obtained from Chapter 6. It was observed that the enable gate does provide a good isolation between the photodiode and the gate of the readout transistor. Charge injection was also observed in both simulation and experiments, thus possibly corrupting the output signal. Therefore, a method of eliminating charge injection was presented and simulated with the APS. It was recommended that charge injection cancellation should be implemented in future DAPS designs.

8 CHAPTER EIGHT – CONCLUSION

This thesis investigates two novel designs of active pixel sensor: the fault tolerant active pixel sensor (FTAPS) and the duo-output active pixel sensor (DAPS). Both designs attempt to address problems faced by the current image sensor technologies, either the traditional charge-coupled devices or the state-of-the-art active pixel sensor. These two novel pixel designs were designed and fabricated using CMOS 0.18 micron technology and experimental results were shown.

8.1 Fault Tolerant Active Pixel Sensor

As the pixel count of image sensors keep increasing and pixel size decreasing, the resolution of image sensors, be it the CCD or the APS, is approaching to that of the traditional film. Because of the same reasons, the reliability of imagers over their lifetimes is reduced. This problem is especially important in harsh environments such as high-radiation conditions in the military or the outer space. Moreover, lowering defects at fabrication time in order to keep yields high to minimize production costs becomes one of the primary concerns in digital imaging.

Besides regular electrical defects and degradation over time, defects in APS can be caused by optical problems such as covered photo-detectors or packaging defects. In general, defects in APS with respect to the output are categorized into three groups: optically stuck low (SL), optically stuck high (SH), and low sensitivity.

Software correction such as interpolation and averaging from surrounding pixels are used but the results are not satisfactory. Under many conditions, they give faulty information. Thus a fault tolerant APS was devised and simulated by Chapman and Audet to correct this problem. It incorporates hardware redundancy by splitting a normal APS into two parallel operating halves

with very little additional area cost. If one of the two halves fails to operate due to any reasons, the other half remains functional and the reading of the pixel can rely on this operating half. Multiplying the output by two retrieves the full pixel reading as if a normal operating APS. FTAPS prevents the loss of the entire pixel reading in a traditional APS without fault tolerance when a point defect can destroy the entire pixel. Therefore, the reliability and fabrication yield rate are significantly increased.

In this thesis, the experimental results for the photodiode-based FTAPS were presented. Optically induced defects were generated by using a focused argon laser beam. Characteristics of the FTAPS pixel were recorded in three different scenarios: fully functional pixel, half stuck low pixel, and half stuck high pixel. Results showed that the sensitivities of the half defective pixels, i.e. half stuck low or half stuck high, are half of the sensitivity of a fully functional pixel. These results agreed with our hypothesis that after splitting a normal pixel to two halves, if only half of a pixel is sensitive to light, the sensitivity of this pixel is half of that of a non-defective pixel. Therefore, by multiplying the result of a half-stuck pixel by two, the original optical signal can be retrieved.

Electrically induced defects were also employed by intentionally shorting certain signal lines to either VSS or VDD to create the half stuck low or half stuck high effects. Characteristics of these pixels were measured. Results were compared to that from the optically induced method and they agreed with each other within the expected experimental errors. The sensitivity of the fully functional pixel is two times the sensitivities of the half stuck low or half stuck high pixels.

A simple bitmap image was projected on a small array of FTAPS which contains non-defective pixels, half stuck low pixels and half stuck high pixels. The captured result illustrated the difference between the output images with and without fault tolerance.

8.2 Duo-output Active Pixel Sensor

The duo-output APS (DAPS) was designed to target applications where the background illumination is desired to be subtracted from the laser signal on an object. These applications include but not limited to 3-D profile scanning using laser and food or material processing. The signal to noise ratio of these applications can be greatly increased if the background illumination can be eliminated from the sensor reading. Current technologies of detecting laser spots are sensitive to changes in surface reflectivity.

The duo-output APS addresses the above obstacles by incorporating an additional output path to the traditional 4-T APS pixel, resulting in two output paths within a pixel. For any given integration cycle, there is two phases. One output path integrates and stores a signal during the first phase while the other path integrates and stores a signal during the second phase. When the pixel is synchronized with the optical source such that the optical source is only on during the first phase, the first integration can then read the optical level of both the background and the illuminated spot while the second phase reads the background illumination alone. At the end of a cycle, the output from the second integration (background illumination only) can then be subtracted off from the first output to eliminate the background level, resulting in an output containing only the desired signal.

Designs of the DAPS were fabricated using CMOS 0.18 micron technology and experiments were carried out. Simple experiments involved the use of a pulsed LED to flood illuminate the entire pixel area with only one side operating or with both sides operating. Results suggested that since the pixel was flood illuminated and the circuitry of the pixel other than the photo-detecting region was not optically shielded by higher metal layers, the pixel output was disturbed by the optical signal. Therefore the output of a given side cannot be kept constant even when this side is not integrating.

To investigate the above problem, the LED was replaced by a focused argon laser beam so that light is confined only to the photo-sensitive area. The argon laser is synchronized to the laser by using an electro-optical shutter that controls the amount of laser power that passes through. Significant improvement was observed that when one of the two sides is not integrating, its stored signal can be maintained at a constant level. Results were obtained with and without background illumination and they demonstrated a clear difference between the two outputs from a DAPS pixel, suggesting that background illumination can be eliminated with a simple differencing circuitry.

Further study was done to investigate the response of a pixel with respect to the location of the focused laser spot. It once again confirmed our results using LED that a pixel output is affected if light is illuminated on the output circuitry.

HSpice simulations were carried out specifically for the simple photodiode APS, 4-transistor APS, and the duo-output APS. It was shown from simulation and experimental results that all of these APS' experience charge injection. Thus a method of cancelling charge injection was proposed with APS by adding an additional transistor between the shutter transistor and the gate of the readout transistor. Simulation showed that the effect of charge injection can be cancelled by the extra transistor implemented in a 4-T APS.

8.3 Suggested Future Work

With the satisfactory results from the photodiode version of the fault tolerant APS, the photogate version should be tested. In fact, experiments for the photogate version of the FTAPS have already been carried out by a group of new graduate students who will be taking over the APS project in the next couple years. Report of these results will be presented in conference paper as well as their thesis in the future.

For the duo-output APS, experimental results indicated that improvements should be made to the current DAPS pixel design. Necessary modifications include moving the reset transistor from the photodiode node to the gate of the readout transistor, adding metal shielding to the area outside the photo-sensitive region, and inserting an extra transistor(s) to the pixel to achieve charge injection cancellation. With these modifications, further experiments can be carried out. Indeed, two new graduate students, Ms. Michelle La Haye and Cory Jung, have already submitted improved APS designs for fabrication but these chips did not arrive in time to be tested for this thesis.

Besides improvements made to the pixel designs, more can be implemented to the sensor array. Larger 2-D pixel arrays can be created for the FTAPS and with the help of the argon laser, half-pixel-defects or even full-pixel-defects can be created after fabrication. Capturing an image using the defective FTAPS illustrates the effect of combining hardware correction and software correction.

More on-chip circuitries can also be gradually tested and added to the APS sensor chip. More timing controls, such as the reset and enable signals, can be used instead of relying mostly on the timing signals generated by LabVIEW. Instead of using static row decoders to output only one row at a time, digital timing control can be implemented to output the a selected section or the entire pixel array automatically by sequentially shifting output signals through a shift register. Simple circuitry can also be implemented to the DAPS to output the difference between the two outputs at the end of an integration cycle.

8.4 Summary

At the beginning of the thesis, we aimed at two major studies related to the active pixel sensor. The first objective was to design, implement, and test the fault-tolerance APS proposed and simulated by Chapman et. al. The second objective was to actualize the idea of eliminating background illumination by using a duo-output APS. This involves design, implementation, and

testing the DAPS pixel. The photodiode fault-tolerance APS was tested and results showed that fault tolerance is feasible to recover would-be-lost information, leading to increased reliability, fabrication yield, and lifetime. DAPS pixels were also designed and tested. Although experiments were still in early stage and more studies are needed, preliminary results showed that the idea of eliminating background illumination is plausible.

9 APPENDIX A

```
Simulation of Simple Photodiode APS
*
* Supply volt: 1.8V
* TSMC CMOS 0.18 micron technology
*
*------ Transistor model -------------
.lib '/CMC/kits/cmosp18/models/hspice/mm018.l' TT
.lib '/CMC/kits/cmosp18/models/hspice/mm018.l' DIO

*------ Voltage/Current sources ------
.global VDD! VSS! rst! row! gate! bias! out!
V1 VDD 0 1.8
V2 VSS 0 0V
V3 rst 0 PULSE (0V 1.8V 0ms 1us 1us 0.2ms 1ms)
V4 bias 0 0.55V
Ip 1 VSS 0.2nA

*------ MOSFET -----------------
*   d    g    s    b
M1  VDD gate 2    VSS nch L=0.18u W=0.22u
Mr  VDD rst  gate VSS nch L=0.18u W=0.22u
Mrs 2   VDD  out  VSS nch L=0.18u W=0.22u
Mb  out bias VSS  VSS nch L=4.0u  W=0.22u

*------ Setup resistors/capacitors/diodes -----
Rj VSS 1 1.00E13
Cj VSS 1 2.00E-15
Dp VSS 1 ndio AREA=6.06955E-12
Rs 1 gate 1.70E-18

.TEMP=25
.TRAN 1us 5ms

.OPTION POST=2 nomod
.PROBE TRAN

.END
```

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