Multi-band Fourth Order Continuous-Time Bandpass Sigma-Delta Modulation

by

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Abstract

Since the mid-1990's, semiconductor processes have increased in speed to the point that it has become possible to implement gigahertz-speed modulators. Bandpass Sigma-Delta Modulators (BPΣΔMs) with high resolution and oversampled noise shaping properties have gained widespread use in current radio systems. Much attention has been focused on continuous-time (CT) BPΣΔMs in cellular radio applications. CT BPΣΔMs can operate at higher sampling frequencies and with lower thermal noise as compared to discrete-time (DT) BPΣΔMs.

In the near future, third generation cellular systems will be deployed. Meanwhile, there is an existing second-generation network infrastructure, which will remain in use for a number of years. As a result, mobile phones will need support multiple standards.

A multi-band, f_s/x, fourth order BPΣΔM topology, with a single bit quantizer, is proposed. This architecture can work at different carrier frequencies instead of only at one quarter of the sampling frequency. ΣΔMs are also known as "noise shaping converters", which can shape noise away from the interested band. We can simply tune the four pulse feedback coefficients and the resonator frequency to implement different noise transfer functions without changing the hardware structure. Meanwhile, one can maximize the dynamic range of the modulator and improve the system performance by tuning the coefficients.

Important BPΣΔMs impairments such as sampling jitter, excess loop delay, comparator hysteresis and amplifier parameters are modelled and analysed at the system level. With these models, it is straightforward to predict the entire system performance.

An ideal switching mode power amplifier (PA) in an H Bridge-configuration driven by a multi-band programmable CT BPΣΔM is described. In order to reduce the noise power introduced by the PA, the behaviour of the PA embedded within the CT BPΣΔM loop is studied. Finally, a multi-channel wideband CDMA signal is fed into the system and the results are investigated.

In memory of my beloved father

Acknowledgements

This thesis would not have been completed without the assistance of a number of individuals. First, I would like to express my extreme gratitude to Professor Shawn Stapleton, my senior supervisor, not only for introducing me to the area of sigma-delta modulation, but also for his insightful advice, his patience, generous financial support and the provision of the resources necessary to carry out the tasks required for this thesis.

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List of Abbreviations and Acronyms

A/D	Analog-to-digital
ADC	Analog-to-digital converter; analog-to-digital conversion
AWN	Additive white noise
BPF	Bandpass filter
BPΣΔM	Bandpass sigma-delta modulation; bandpass sigma-delta modulator
CDMA	Code division multiple access
CT	Continuous-time
DAC	Digital-to-analog converter; digital-to-analog conversion
DBPF	Differential bandpass filter
DC	Direct current
DR	Dynamic range
DSP	Digital signal processing
DT	Discrete-time
EMI	Electromagnetic interference
FFT	Fast Fourier Transform
GBW	Gain bandwidth
HRZ	Half-delay return-to-zero
i.i.d.	Independent and identically distributed
IMD	Intermodulation distortion
LNA	Low-noise amplifier
LPΣΔM	Lowpass sigma-delta modulation; lowpass sigma-delta modulator
NRZ	Non-return-to-zero
NTF	Noise transfer function
Op-Amp	Operational amplifier

OSR	Oversampling ratio
PA	Power Amplifier
PDF	Probability density function
PCM	Pulse code modulation
PSB	Power System Blockset
PWM	Pulse-width modulated
RF	Radio frequency
RZ	Return-to-zero
SC	Switched capacitor
ΣΔM	Sigma-delta modulation; sigma-delta modulator
SFDR	Spurious-free dynamic range
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
SR	Slew rate
STF	Signal transfer function
3G	Third generation
VCO	Voltage-controlled oscillator
VLSI	Very large scale integration
WCDMA	Wideband code division multiple access
ZOH	Zero-order-hold

Chapter 1

Introduction

The growth of information and communication technology has exploded in recent years. Advances in VLSI technology have made it feasible to create high speed densely packed digital circuits, which provide the opportunity to implement radio frequency (RF) functions with digital signal processing (DSP). Various RF front-end conversion architectures are proposed as alternatives to the conventional super heterodyne scheme, which, traditionally, requires a significant number of discrete components. One of the architectures that has received a great deal of attention is the direct conversion scheme, where the RF signal is mixed down to baseband by setting the sampling clock frequency equal to the RF carrier frequency [23].

1.1 Motivation

The heterodyne topology is the most widely used receiver architecture and is shown in a simplified form in Figure1-1.

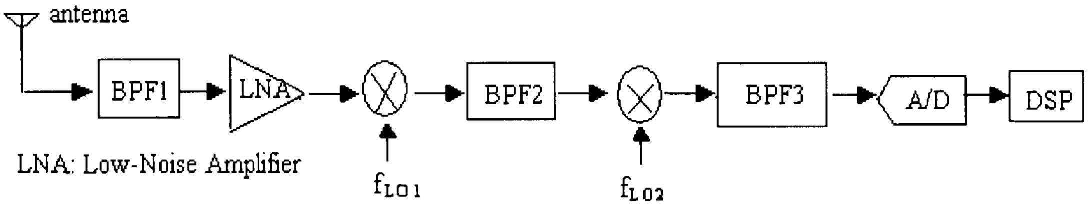


Figure 1-1 Traditional heterodyne receiver with baseband ADC

As shown in Figure 1-1, off-chip, expensive, and bulky filters make it difficult to implement the entire receiver on a single integrated circuit. Placing the bandpass A/D converter following an RF bandpass filter (BPF) and a low noise amplifier (LNA), as shown in Figure 1-2, and performing the analog signal processing (frequency translation, channel filtering and signal demodulation) in one digital chip has become today's challenge.

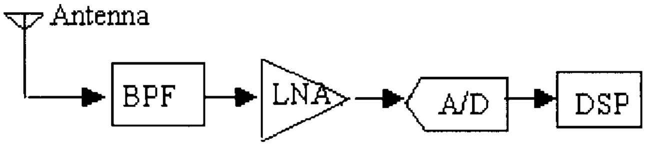


Figure 1-2 Receiver with RF A/D Conversion

Requirements for the RF A/D Converter in the architecture shown in Figure 1-2 are extremely challenging, as the converter must handle the full antenna receiving power. To meet this challenge the converter must have high dynamic range, high linearity and large bandwidth at high (RF) frequencies [22]. Attempts have been made to explore the boundaries of RF analog-to-digital conversion (ADC) by using BPΣΔMs, since it has inherent linearity and high resolution [11, 13, 14, 24].

The existence of various wireless standards within North America and around the world has created a demand for transceivers that operate in more than one mode. In the simplest case, two different receive and transmit frequency bands must be supported, while other properties of the system remain unchanged. Accommodating two or more standards in one transceiver generally requires substantial added complexity in both the RF section and the base band section of the radio, and leads to a higher cost. Thus, the best system must be designed so as to minimize the physical size, manufacturing cost and maximize the shared hardware.

So far, most BPΣΔM architectures have been based on an $f_s/4$ structure [4, 6, 10, 13,14]. This implies that the carrier frequency, f_c, is one quarter of the sampling frequency, f_s. It is the intention of this thesis to present a simple structure that can cater to a variety of centre frequencies overcoming the restriction of the popular $f_s/4$ architecture.

Using a lowpass to bandpass transformation, a fourth order multi-band discrete-time BPΣΔM with a single-bit quantizer is derived in this thesis. A single-bit CT BPΣΔM with inherent anti-aliasing filtering and linearity performance is attractive for use in RF communications because it can be operated at high frequency without a significant performance penalty. A fourth order multi-feedback CT BPΣΔM that is suitable for multiple standards is developed in Chapter 3. By tuning the related feedback pulse coefficients, the continuous-time domain transfer function can be equated to the discrete-time domain transfer function. Meanwhile, this architecture can operate at different carrier frequencies, not only $f_s/4$, without changing the hardware.

Since the third generation UMTS (WCDMA) and second-generation IS-95 (CDMA) cellular systems will coexist in the near future. We will primarily focus on two different fourth order continuous-time modulator prototypes, $f_s/4$ and $f_s/10$, where the carrier frequencies are 2100MHz and 840MHz, respectively.

Nonideal characteristics adversely affect the performance of ΣΔMs. To investigate the impact of the impairments on system performance, system level behavioural models based on the analytical expressions were implemented and simulated.

The main challenge in using a ΣΔM in the transmitter, is the design of the output power amplifier. The transmitter can control the power of the baseband signal to improve noise performance, but severe trade-offs remain among efficiency, linearity and supply voltage in the design of a good power amplifier [31]. Nevertheless, simulations suggest that efficient operation at higher frequencies is possible [3, 4, 5, 27]. Researchers have used a convenient 2-level binary signal generated by a RF BPΣΔM to drive a switching mode RF power amplifier (class D, class E or class S). The transistors are either fully on or fully off during as much of the RF cycle as possible. Because the internal power dissipation is minimized, high efficiency is attained. The architecture is shown in Figure 1-3.

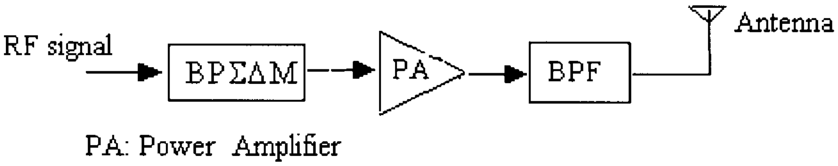


Figure 1-3 Schematic of a transmitter

A switching mode power amplifier (PA) in an H Bridge-configuration driven by a multi-band programmable BPΣΔM is described in the latter part of this thesis. The noise shaping property of the ΣΔM is exploited to decrease the noise introduced by the PA by embedding the power amplifier within the BPΣΔM loop.

1.2 System Level Simulation

The analysis of $\Sigma\Delta$Ms is difficult because of the presence of a nonlinear element, the quantizer, inside the loop. If conventional electrical simulators are used for simulation, the simulation times are very long because transient analysis is required.

Several intermediate approaches have appeared in the last few years, usually in the form of specialized simulation programs like MIDAS [20], TOSCA [21] and ADS [65]. In this thesis, MATLAB/SIMULINK is employed for all system level simulations. Simulation at the system level is a powerful method to quickly predict and validate the performance of a $\Sigma\Delta$M. System level simulation allows various configurations to be readily implemented, and can further verify some design decisions [22].

Based on vector and matrix manipulations MATLAB is a widely used software tool that provides a comprehensive set of system level tools and an environment that accelerates the design process. SIMULINK, as an extension to MATLAB, is a dynamic system simulation tool that offers a graphical modelling environment enabling the user to operate on complex systems [1].

Behavioural models of BP $\Sigma\Delta$M impairments were developed at the system level. These models can be integrated into a system to investigate their impact on the overall performance in a matter of minutes, without the need to go through the entire design process.

1.3 Power System Simulation

The MATLAB Power System Blockset (PSB) is used to simulate the ideal switching-mode PA. The development of design automation tools, for power electronic circuit analysis and design applications, has received a great deal of attention in the last three decades. A number of fundamental methods have been proposed for the formulation and solution of the network equations. A comprehensive survey on simulation methods for power electronics has been presented in [70, 71]. The main analysis techniques for power electronics simulation include state-variable analysis, nodal analysis, and modified model analysis. These techniques have been applied to the development of different simulation packages [72].

The PSB is a convenient tool for the simulation of electronic circuits containing power electronic devices. The PSB is based upon the use of the state-variable and can accurately detect the instant at which discontinuities and switching occur. A power system (Figure 1-4) is represented in two parts when using the PSB [69]: a state-space model for linear circuit elements and a feedback model between voltage outputs and current inputs for the nonlinear elements.

The differential equations of a linear electrical circuit can be written in the form of two state equations:

$$\dot{x} = Ax + Bu \tag{1.1}$$

$$y = Cx + Du \tag{1.2}$$

where, x is the vector of state-space variables (inductor currents and capacitor voltages), u is the vector of voltage and current inputs, and y is the vector of voltage and current outputs. This state-space model can be computed by the command *circ2ss*.

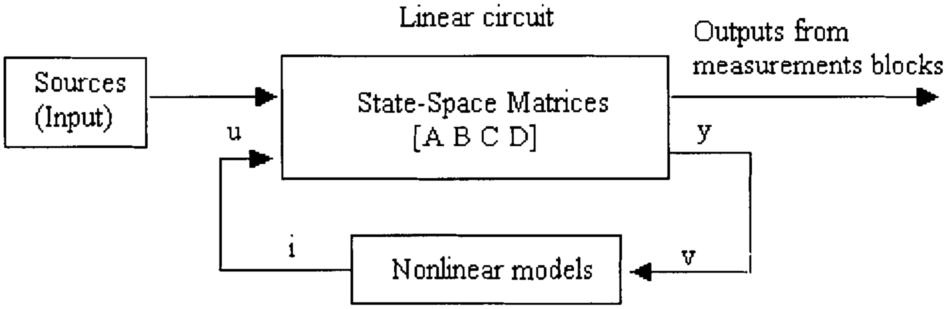


Figure 1-4 A power system model

State variable formulation allows the use of fixed time step and variable time step algorithms. The variable time step method is usually faster for small and medium size systems because it requires fewer steps than the fixed-time step algorithm. However, the variable-step method will reduce the computation step size significantly for high-frequency circuits and, consequently, the simulation time becomes very long. Nonlinear elements, such as transformer saturation branches, switches and electric machines are simulated by using nonlinear V-I relationships [72].

The PSB is entirely compatible with MATLAB and SIMULINK due to its graphical interface. The user can easily integrate control systems implemented with SIMULINK blocks directly into a diagram built with the PSB. In addition, the powerful processing ability of MATLAB allows the user to perform complex post-processing on simulation results.

Simulation results can be visualized with the use of SIMULINK scopes that are connected to the measurement block outputs. These measurement blocks act as an interface between the electrical blocks and SIMULINK blocks.

1.4 Performance Definitions

The performance measurement of interest for a $\Sigma\Delta M$ is its resolution in bits, or equivalently, the maximum obtainable SNR.

Signal to noise ratio (SNR): Determined by calculating the ratio of the signal power to the integrated in-band noise power in the output spectrum. The "noise" consists of system noise such as thermal and 1/f noise, as well as quantization noise.

Peak SNR: The ratio between the maximum signal power and in-band noise power.

Signal to noise and distortion ratio (SNDR): The ratio between the signal power and total in-band noise, including the harmonic distortion power.

Dynamic range (DR): The ratio between the maximum input signal power allowable before the modulator becomes unstable and the minimum detectable signal power.

Spurious free dynamic range (SFDR): The ratio between the maximum signal carrier power and the maximum distortion component.

Intermodulation distortion (IMD): When multiple signal tones are modulated and passed through a non-linearity system, the resulting distortion is found at combinations of the input signal frequencies [22]. Intermodulation distortion is the combination of the various products of two tones (ω_1 and ω_2). These products are found at ($m\omega_1 \pm n\omega_2$), where $n,m \in \{0, \pm1, \pm2, \ldots\}$. The order of the IMD is given by $|n| + |m|$. As an example, consider two-tone input signal:

$$x(t)=A_1 \sin\omega_1 t + A_2 \sin\omega_2 t$$

that is applied to a nonlinear system whose output, y(t) can be described by the expansion:

$$y(t)=k_1 x(t)+k_2[x(t)]^2+k_3[x(t)]^3$$

The quadratic term produces second-order IMDs at $(\omega_2 \pm \omega_1)$. The cubic term produces third-order IMDs at $2\omega_2 \pm \omega_1$ and $2\omega_1 \pm \omega_2$. The most troublesome IMDs are $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$, since they can fall within the signal band.

In order to explore the application of a ΣΔM in a 3G system, a 20 MHz bandwidth is employed. Since it is standard practice to use sinusoids to quantify the quality of an ADC [56], we apply high frequency sinusoids to the system and investigate how the rate of change of the input affects the output and the intermodulation products.

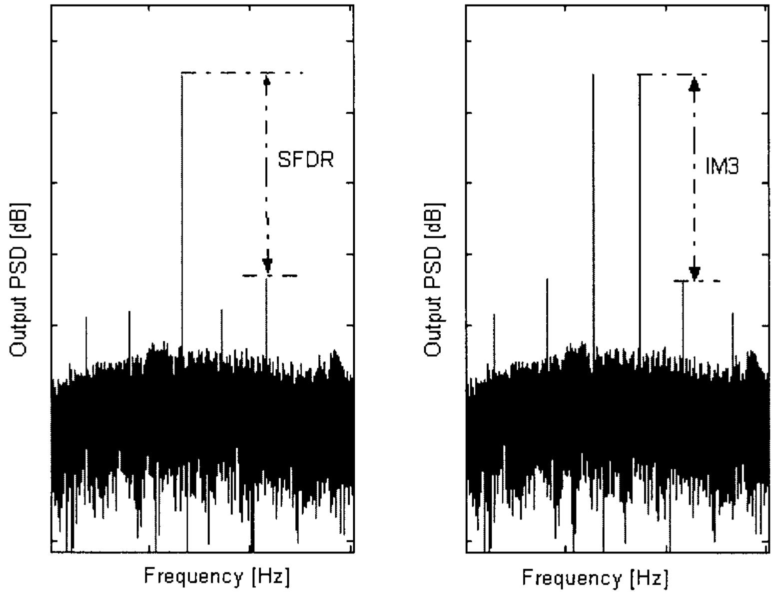


Figure 1-5 **SFDR and IMD definition**

1.5 Organization

This thesis is organized into six chapters, including this introduction. The next chapter briefly reviews the fundamental theory of ΣΔM. The design of DT BPΣΔMs based upon their lowpass counterparts is demonstrated. The design of a fourth-order, f_s/x DT BPΣΔM with a single bit quantizer is presented.

Chapter 3 describes a multi-feedback CT BPΣΔM design. A CT ΣΔM can be perfectly matched to its discrete-time equivalent by tuning the feedback pulse coefficients. Directly implementing the desired noise shaping specifications with the required stability is described. Architecture for operating under different standards is proposed and simulations of a fourth order CT BPΣΔM operating at a centre frequency of 2.1 GHz and 840MHz are discussed. Finally, a non-linear quantizer model is presented for the purpose of stability analysis.

Chapter 4 describes the significant impairments of BPΣΔMs such as sampling jitter, excess loop delay and comparator hysteresis, and sets out system level models for these impairments. It provides a good starting point for future implementations of the modulator with these models.

Chapter 5 is devoted to the ideal switching-mode amplifier in an H Bridge-configuration. The ideal power amplifier is embedded within the ΣΔM loop to observe whether EMI thermal noise is reduced. Even-order distortion, especially arising from second-order non-linearities, can degrade the system's performance significantly. The differential bandpass filter (DBPF) provides inherent cancellation of even-order distortion and is less sensitivity to substrate noise and other interference sources [78] and is used to filter the amplifier output signal. Chapter 5 concludes with the description of a system amplifying a WCDMA signal.

A summary of this work, as well as suggestions for future research topics, is presented in Chapter 6.

Chapter 2

Multi-band 4^{th}-order DT BPΣΔM

Analog-to-digital (A/D) converters based on ΣΔM provide high resolution by combining a sampling rate higher than the Nyquist rate with negative feedback and a digital filter. Furthermore, ΣΔM is able to provide a high degree of linearity without requiring precisely matched components.

In this chapter, the basic concepts of ΣΔM are reviewed. This review includes a discussion of oversampling and noise shaping, as well as the linearized white and uniformly distributed quantization noise model, that is used to estimate the performance of a ΣΔM. The theoretical estimated performance can subsequently be compared to the results of behavioural simulations.

The conventional second-order discrete-time lowpass sigma-delta modulator (LPΣΔM) with a two-level quantizer is described, along with simulation result. Using a lowpass to bandpass transformation for resonators, a fourth order DT BPΣΔM is derived. The general structure of an f_s/x DT BPΣΔM for multiple communication standards is presented at the end of the chapter.

2.1 Overview of the Sigma-delta Modulation

In 1962, a base-band sigma-delta modulator was proposed by Inose, Yasuda and Murakami [29], who added a filter in the forward path and in the front of a delta modulator. It is this filter, in the feedback loop, that is the characteristic of today's ΣΔMs.

A basic ΣΔM consists of *a loop filter*, a *quantizer*, and *a feedback loop*. Since the system includes a delta modulator and an integrator, it is named a ΣΔM, where the "sigma" denotes the summation performed by the integrator. Today, the term sigma-delta is more popular and has also become almost synonymous with noise shaping ADCs [9].

An ADC produces a digital representation of the analog input signal by uniform sampling in discrete time and quantization in discrete amplitudes.

Sampling of a signal at the Nyquist rate (the sampling rate is equal to twice the bandwidth of interest) has the advantage of a minimum sampling rate. However, it includes the need for high-accuracy analog antialiasing circuits to filter the signal before sampling.

Quantization is a non-invertible process; although, the accuracy of the ADC can be improved by increasing the number of quantization levels. Increasing the number of quantization levels, however, will result in instability. Furthermore, due to the number of quantization levels, the quantization process itself can introduce additional errors. To alleviate these problems associated with quantization, a two-level quantizer with high linearity is employed in our system.

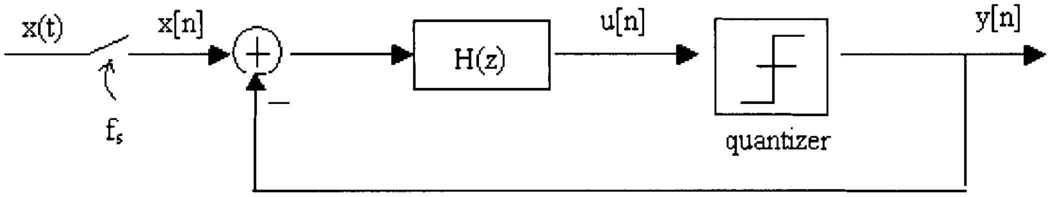


Figure 2-1 General model of a DT ΣΔM

The diagram of a general discrete-time single-loop ΣΔM is shown in Figure 2-1, where x[n] is the discrete time input to the ΣΔM, u[n] is the output of the loop filter H(z) and y[n] is the output of the system. Before moving to a detailed description of the specifications of ΣΔMs, some basic concepts of ΣΔMs are introduced below.

A quantizer with Q output levels is said to have N bits of resolution, where $N=\log_2(Q)$ when Q is even, and $N= \log_2(Q-1) + 1$ when Q is odd. Letting the maximum and minimum quantized output values be V and –V, respectively, (see Figure 2-2), for an ADC with Q quantization levels, the least significant bit (LSB), which is the difference between the binary digital word for two adjacent output levels, is defined as Δ and is equal to 2V/(Q-1). If the quantization error $e[n] = y[n] - u[n]$ does not exceed half a LSB, i.e., $|e[n]| \leq \Delta/2$, the quantizer or ADC is said to be not overloaded; otherwise, for $|e[n]|>\Delta/2$, the ADC is said to be overloaded or saturated [30].

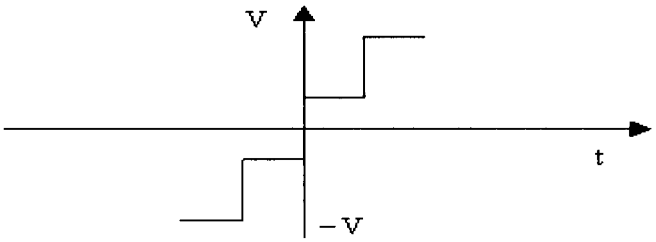


Figure 2-2 A uniform multilevel quantization characteristic

2.1.1 Linear Model

The quantizer is the heart of a ΣΔ modulator and its inherent nonlinearity makes the analysis of even the simplest system difficult. To overcome this difficulty, various methods based on approximations have been widely used which are usually implicitly or explicitly built on either the asymptotic results of Bennett [32] or the exact results of Sripad and Snyder [34] (which is the extension of Widrow [33]). However, many of the original results and insights into the behaviour of quantization error are due to Bennett's [32] approximation, which modelled the quantization error, e[n], as input-independent additive white noise (AWN). However, this approximation is valid if the following conditions are satisfied [9]:

a) The input is never in the overloaded region of the quantizer.

b) The quantizer has asymptotically large number of quantization levels.

c) The quantization step size Δ is asymptotically small.

d) The joint probability density function of the input signal at different sample times is smooth.

Under these conditions, the quantization error is distributed uniformly in [-Δ/2, Δ/2]. The variance, or power of the quantization error is given by:

$$e_{rms}^{2} = \int_{-\Delta/2}^{\Delta/2} e^{2}\frac{1}{\Delta}de = \frac{1}{\Delta}\frac{e^{3}}{3}\Bigg|_{-\Delta/2}^{\Delta/2} = \frac{2}{\Delta}\frac{1}{3}\left(\frac{\Delta}{2}\right)^{3} = \frac{\Delta^{2}}{12} \qquad (2.1)$$

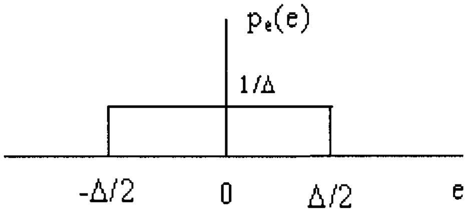


Figure 2-3 **Probability density function (PDF) of quantization error in the linear model**

The AWN approximation enables the system to be linearized, which means that the output of the modulator is the sum of the filtered input signal and the filtered quantization noise as shown in Figure 2-4.

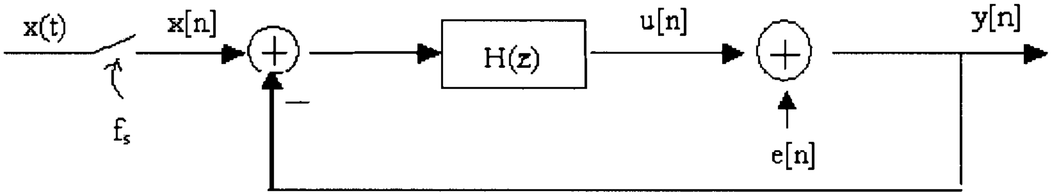


Figure 2-4 **General linear model of a discrete-time ΣΔM**

Using the general linear model of a DTΣΔM shown in Figure 2-4, the single bit digital output, y[n], is given by:

$$y[n]=\{x[n]-y[n]\}*h[n]+e[n]$$

where $*$ denotes convolution, and Y(z) in the z domain is given by:

$$Y(z)=[X(z)-Y(z)]\cdot H(z)+E(z)$$

$$Y(z)=\frac{H(z)}{1+H(z)}X(z)+\frac{1}{1+H(z)}E(z) \tag{2.2}$$

or

$$Y(z)= STF(z)X(z)+ NTF(z)E(z) \tag{2.3}$$

where

$$STF(z)=\frac{H(z)}{1+H(z)}$$

$$NTF(z)=\frac{1}{1+H(z)}$$

H(z) is the loop filter transfer function, which has a very large magnitude in the desired (signal) band. The signal transfer function, *STF(z)*, has approximately unity gain in the desired band, while the noise transfer function, *NTF(z),* is designed to be zero in the desired band. The NTF attenuates the quantization noise within the desired signal band.

This simple linear model, also called an AWN model, is good for the initial design and is sufficient to explain the most basic characteristics of a ΣΔM, such as quantization noise shaping. It is also sufficiently accurate to estimate the performance of a wide variety of ΣΔM architectures [9]. Later, in chapter 3, a less tractable nonlinear model will be addressed which is necessary for verifying stability and correcting linear estimates.

2.1.2 Oversampling and Noise Shaping

The critical specifications of a ΣΔM are its oversampling ratio and its noise shaping characteristic. In this section, the principles of oversampling and noise shaping are reviewed.

Oversampling means that sampling of the analog input signal is carried out at a sampling rate higher than the minimum required Nyquist frequency (twice the signal bandwidth). The immediate advantage of oversampling is that it relaxes the requirement of the sharp transition band of the antialiasing filter. The oversampling ratio (OSR) is defined as:

$$OSR=\frac{f_s}{2\,f_b}=\frac{Sampling\ Frequency}{Nyquist\ Frequency}$$

Where f_b is the signal bandwidth. Typical values of OSRs are in the range 32-256 [14], though circuits with OSRs outside this range have been fabricated [90,91].

If we assume that all of the error power is within the positive range of frequencies, when a quantized signal is sampled at f_s ($=1/T_s$), all of its power folds into the frequency band: $0 \le f \le f_s/2$. Therefore, the power spectral density of the sampled quantization error is [9]:

$$P_e(f)=\frac{e_{rms}^2}{\frac{f_s}{2}}=\frac{2e_{rms}^2}{f_s},\quad 0\le f\le\frac{f_s}{2} \tag{2.4}$$

Equation 2.4 shows that the higher the sampling frequency, the lower the noise power density - this is the principle of oversampling. If we assume $|NTF(f)|$ is equal to 1 for any frequency, the total in-band quantization noise is given by:

$$\sigma_{ey}^2 = \int_0^{f_b} P_e(f)\,|NTF(f)|^2\,df = \frac{e_{rms}^2\, 2f_b}{f_s} = \frac{e_{rms}^2}{OSR} \qquad (2.5)$$

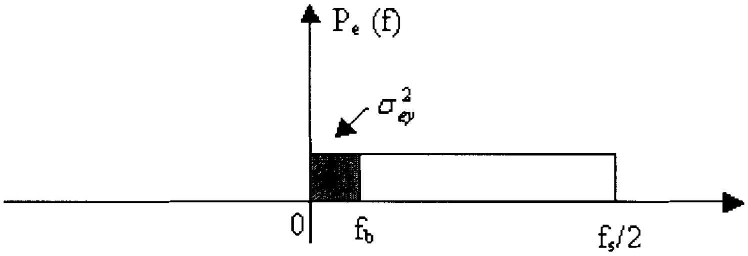


Figure 2-3 **Oversampled quantization noise power spectral density**

From Equation (2.5), we have the well-known result that oversampling reduces the in-band noise power by spreading a fixed quantization noise power over a bandwidth much larger than the signal band. The maximum achievable in-band signal-to-noise-ratio (SNR) in dB is then:

$$SNR = 10\log_{10}\left(\frac{\sigma_x^2}{\sigma_{ey}^2}\right) = 10\log_{10}\left(\sigma_x^2\right) - 10\log_{10}\left(e_{rms}^2\right) + 10\log_{10}\left(OSR\right)\ (dB) \qquad (2.6)$$

Where σ_x^2 is the signal power, which is assumed to be confined to the signal band only, and the in-band signal gain is 1.

Consider a sinusoidal input whose signal power is $V^2/2$, and an N bit quantizer (2^N quantization levels), i.e. $\Delta = 2V/(2^N - 1)$. Thus from Equation (2.6) and Equation (2.1), we have:

$$SNR = 10\log_{10}\left(\frac{V^2}{2}\right) - 10\log_{10}\left(\frac{4V^2}{12\left(2^N - 1\right)^2}\right) + 10\log_{10}\left(OSR\right).$$

If N is large, $(2^N - 1)^2 \approx 2^{2N}$, and we can write:

$$\begin{aligned} SNR &= 10\log_{10}(2N-1)^2 + 10\log_{10}\frac{3}{2} + 10\log_{10}\left(OSR\right) \\ &= 6.02N + 1.76 + 10\log_{10}\left(OSR\right) \qquad (dB) \end{aligned} \qquad (2.7)$$

Note that for an increase in N by one, i.e. for each doubling of the number of quantization levels, the SNR increases approximately by 6 dB. Alternatively, for every doubling of the OSR, the SNR increases by about 3 dB, or, equivalently, the resolution is improved by half a bit.

The use of a multi-bit quantizer in a sigma-delta modulator will result in higher resolution and alleviate the quantization noise expressed by Equation (2.1). Additionally, a multi-bit quantizer will tend to increase the stability of higher order modulators since the modulator gain will be relatively close to one for most input signals. However, a multi-bit quantizer cannot be easily fabricated in VLSI with sufficient linearity needed for high-resolution conversion [30].

Noise shaping in the context of ΣΔMs refers to the filtering of the quantization error and the suppression of the error within the signal band, while the noise outside of the signal band is amplified. The noise can be removed by a digital filter that follows the modulator.

The NTF in Equation (2.3) is responsible for shaping and suppressing the noise within the signal band. Spreading the NTF zeros throughout the desired signal band can improve the SNR [7, 8] and an optimizer can help with the zero placement [42]. A detailed discussion of the placement of the NTF zeros is provided in section 3.1.

2.2 The Second-order DT LPΣΔM

In a LPΣΔM, the loop filter uses integrators to push noise away from DC. Consequently, the NTF is a high pass filter, which suppresses the noise at DC. The STF is a lowpass filter with a constant (approximately unity) magnitude response around DC.

We start our analysis with the conventional 2^{nd}-order LPΣΔM [9, 30, 39]. The quantizer has only two levels (±1), which eliminates the harmonic distortion that may be generated by step-size mismatch in a multi-bit quantizer [92]. The performance and dynamic range of the LPΣΔM will be estimated through the use of a behavioural simulation [87]. Figure 2-6 shows the schematic of the ideal second-order LPΣΔM. An equivalent LPΣΔM that employs integrators is depicted in Figure 2-7.

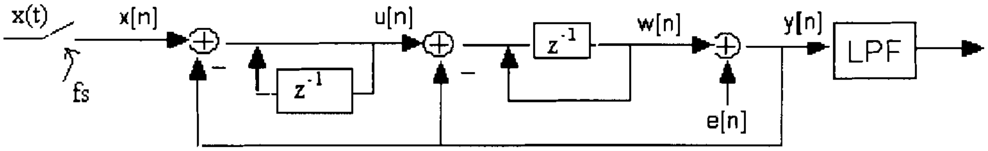


Figure 2-4 The ideal 2nd-order DT LPΣΔM

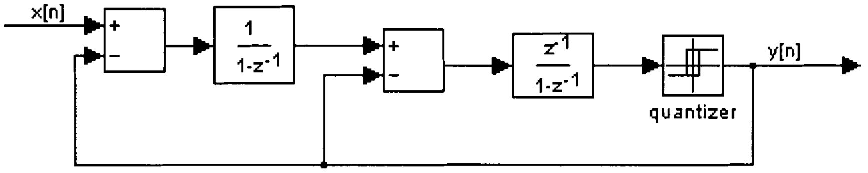


Figure 2-5 The equivalent 2nd-order DT LPΣΔM

From Figure 2-6, we have:

$$u[n]=x[n]-y[n]+u[n-1]$$
$$w[n]=u[n-1]-y[n-1]+w[n-1]$$
$$y[n]=w[n]+e[n]$$

Equivalently, in the z-domain:

$$U(z)=\frac{X(z)-Y(z)}{1-z^{-1}} \tag{2.8}$$

$$W(z)=z^{-1}\frac{U(z)-Y(z)}{1-z^{-1}} \tag{2.9}$$

$$Y(z)=W(z)+E(z) \tag{2.10}$$

Substituting Equations (2.8) and (2.9) into Equation (2.10) gives:

$$Y(z)=z^{-1}X(z)+(1-z^{-1})^{2}E(z) \tag{2.11}$$

The corresponding output in the time domain is:

$$y[n]=x[n-1]+e[n]-2e[n-1]+e[n-2] \tag{2.12}$$

It is observed that, the output is a delayed version of the input. The quantization noise has been shaped by a second order differentiator or a high pass filter. In Equation (2.11), the NTF is:

$$NTF(z)=(1-z^{-1})^{2} \tag{2.13}$$

The signal transfer function is:

$$STF(z)=z^{-1} \tag{2.14}$$

Applying Equation (2.13) in Equation (2.3), the loop filter transfer function is:

$$H(z)=\frac{2z^{-1}-z^{-2}}{\left(1-z^{-1}\right)^{2}} \tag{2.15}$$

The magnitude response of *NTF(z)*, *STF(z)* and *H(z)* of the second-order LPΣΔM is shown in Figure 2-8. From Equation (2.15), we see that the integrators (*H(z)*) have poles at DC, and that *NTF(z)* has zeros at DC which will shape noise away from DC.

The power spectrum of the linearized white quantization noise is:

$$P_{ey}(f)=P_{e}(f)\left|NTF(f)\right|^{2} \tag{2.16}$$

Substituting Equations (2.4) and (2.13) into Equation (2.16) yields:

$$\begin{aligned}
P_{ey}(f)&=\frac{2e_{rms}^{2}}{f_{s}}\left|\left(1-z^{-1}\right)^{2}\right|^{2}\Big|_{z=e^{j2\pi f/f_{s}}}\\
&=\frac{2e_{rms}^{2}}{f_{s}}\left|1+e^{-j4\pi f/f_{s}}-2e^{-j2\pi f/f_{s}}\right|^{2}\\
&=\frac{2e_{rms}^{2}}{f_{s}}\left[\left(1-2\cos\alpha+\cos 2\alpha\right)^{2}+\left(\sin 2\alpha-2\sin\alpha\right)^{2}\right]\Big|_{\alpha=2\pi f/f_{s}}\\
&=\frac{2e_{rms}^{2}}{f_{s}}\left[\left[2\cos\alpha(\cos\alpha-1)\right]^{2}+\left[2\sin\alpha(\cos\alpha-1)\right]^{2}\right]\Big|_{\alpha=2\pi f/f_{s}}\\
&=\frac{32e_{rms}^{2}}{f_{s}}(\cos^{2}\frac{\alpha}{2}-1)^{2}\\
&=\frac{32e_{rms}^{2}}{f_{s}}\sin^{4}\left(\frac{\pi f}{f_{s}}\right)
\end{aligned} \tag{2.17}$$

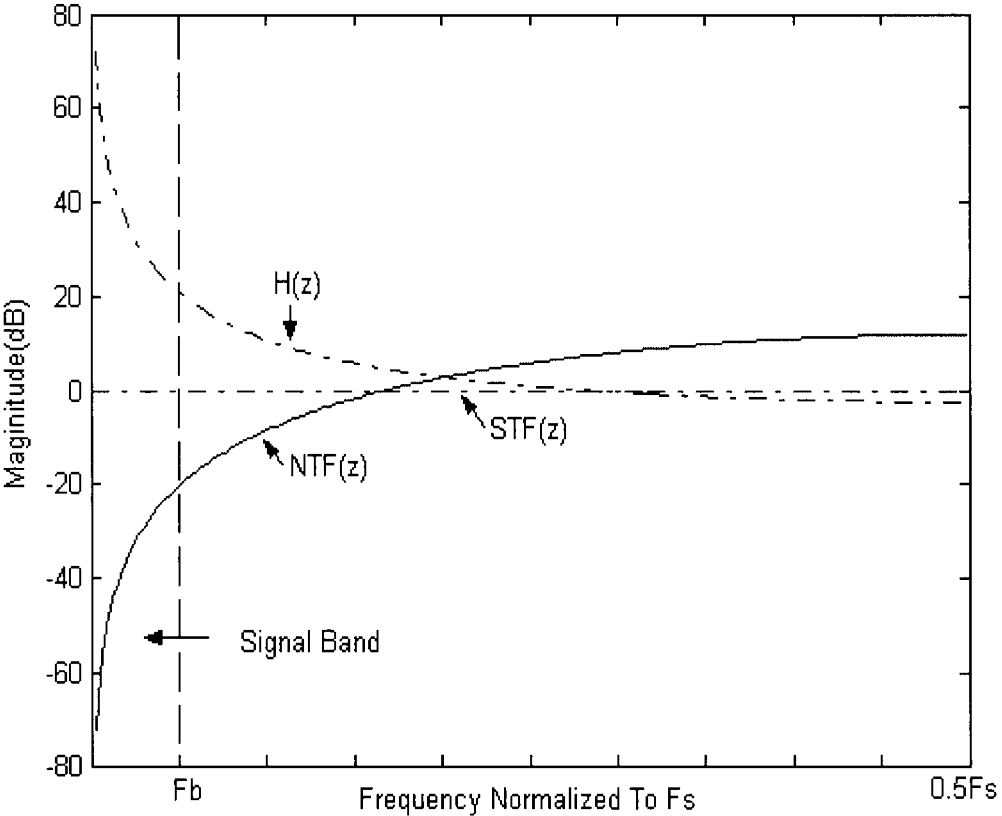


Figure 2-6 The signal and noise transfer function for a 2nd-order LPΣΔM

The in-band quantization noise power (σ_{ey}^2) is given by:

$$\begin{aligned}\sigma_{ey}^2 &= \int_0^{f_b} P_{ey}(f)\,df \\ &= \frac{32e_{rms}^2}{f_s}\int_0^{f_b}\sin^4\left(\frac{\pi f}{f_s}\right)df \\ &= \frac{32e_{rms}^2 f_s}{f_s\pi}\int_0^{f_b\pi/f_s}\left[\frac{3}{8}+\frac{1}{8}\cos(4F)-\frac{1}{2}\cos(2F)\right]dF\Bigg|_{F=\frac{\pi f}{f_s}} \\ &= \frac{32e_{rms}^2}{\pi}\left[\frac{3}{8}\frac{f_b}{f_s}\pi+\frac{1}{32}\sin\left(4\frac{f_b}{f_s}\pi\right)-\frac{1}{4}\sin\left(2\frac{f_b}{f_s}\pi\right)\right]\end{aligned} \tag{2.18}$$

For $f_b << f_s$, we can use the Taylor series expansion:

$$\begin{aligned}\sin x &= x-\frac{x^3}{3!}+\frac{x^5}{5!}+O\left(x^7\right) \\ &\cong x-\frac{x^3}{3!}+\frac{x^5}{5!}\end{aligned} \tag{2.19}$$

Thus:

$$\begin{aligned}\sigma_{ey}^2 &= \frac{32e_{rms}^2}{f_s}\left\{\frac{3}{8}F+\frac{1}{32}\left[4F-\frac{(4F)^3}{3!}+\frac{(4F)^5}{5!}\right]-\frac{1}{4}\left[2F-\frac{(2F)^3}{3!}+\frac{(2F)^5}{5!}\right]\right\}\Bigg|_{F=\frac{f_b\pi}{f_s}} \\ &= \frac{32e_{rms}^2}{f_s}\frac{f_s}{\pi}\frac{1}{5}\left(\frac{f_b}{f_s}\pi\right)^5 = \frac{\pi^4}{5}e_{rms}^2\,OSR^{-5}\end{aligned} \tag{2.20}$$

Therefore, the SNR in dB for the second order LPΣΔM is expressed as:

$$\begin{aligned}SNR_2 &= 10\log_{10}\left(\frac{\sigma_x^2}{\sigma_{ey}^2}\right) \\ &= 10\log_{10}(\sigma_x^2)-10\log_{10}(e_{rms}^2)-10\log_{10}\left(\frac{\pi^4}{5}\right)+50\log_{10}(OSR)\end{aligned} \tag{2.21}$$

Equation (2.21) reveals that for every doubling of the OSR, the SNR increases by 15 dB (2.5 bits). Using a 65536-sample simulation of a second order LPΣΔM, the dynamic range for two different OSRs and a single tone input is depicted in Figure 2-9. Theoretical results are also shown in Figure 2-9. The difference between the theoretical and simulation results may be explained by the use of a Hanning window. Windowing the data prior to applying the FFT may introduce approximately 4.26dB loss in tone power [14]. On the other hand, the discrepancy may be due to the theoretical result being based on the linear model assumption. In fact, the quantizer is nonlinear, particularly for large input signals. As the input signal power is increased, the second integrator will overload and the in-band noise will increase. This increase in the in-band noise will eventually cause the system to become unstable and the performance will deteriorate dramatically.

The spectrum of the output of the LPΣΔM at an input power of –15 dB and an OSR of 210 is shown in Figure 2-10. Figure 2-11 shows the occurrences of the first and second integrator output.

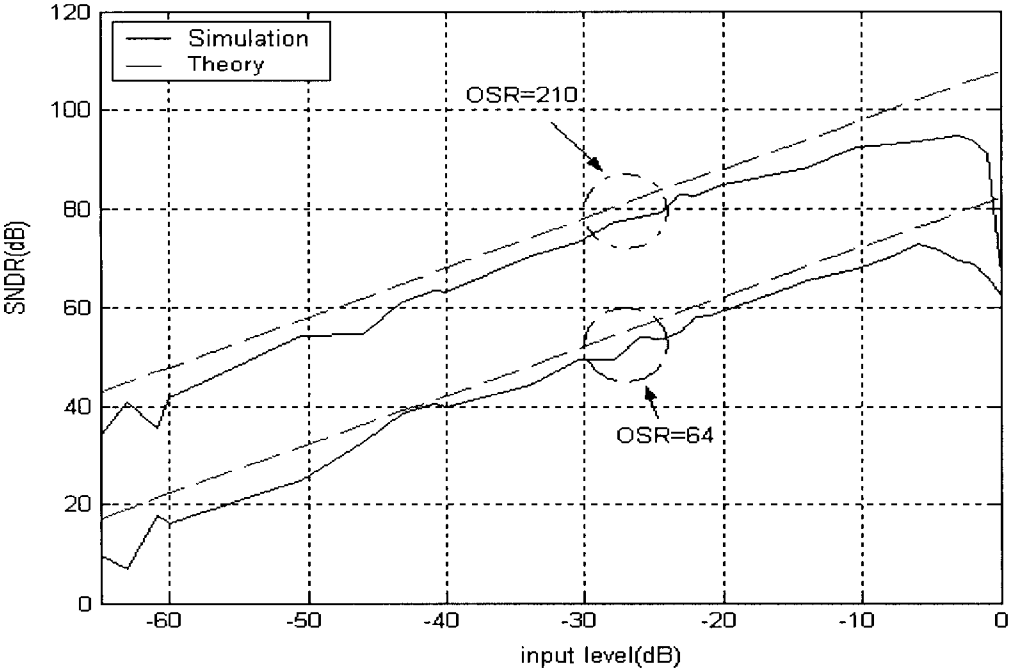


Figure 2-7 SNDR vs. input signal for the 2nd-order DT LPΣΔM

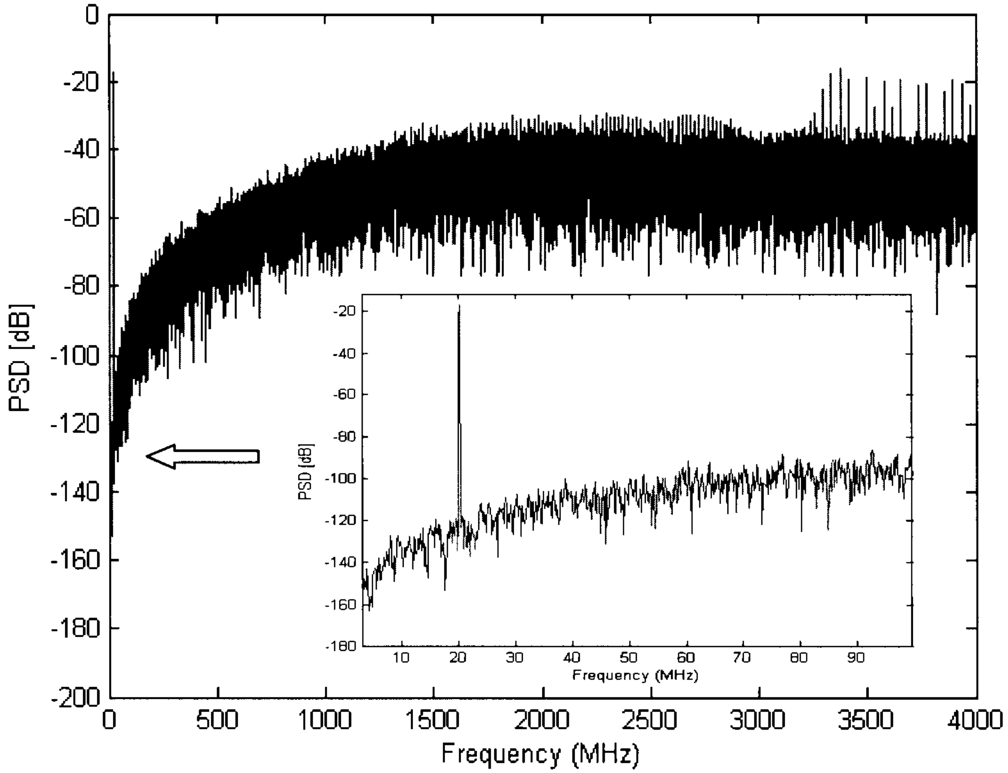
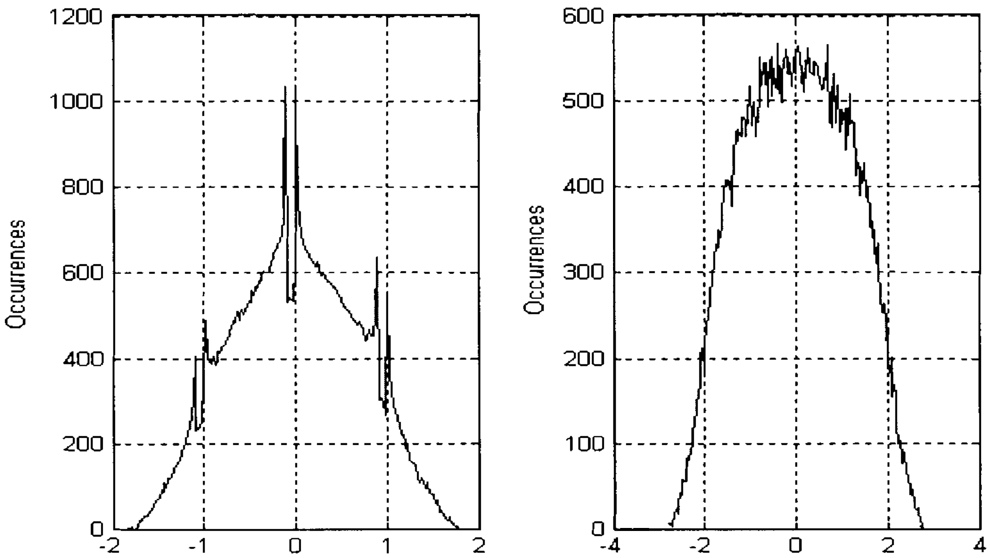
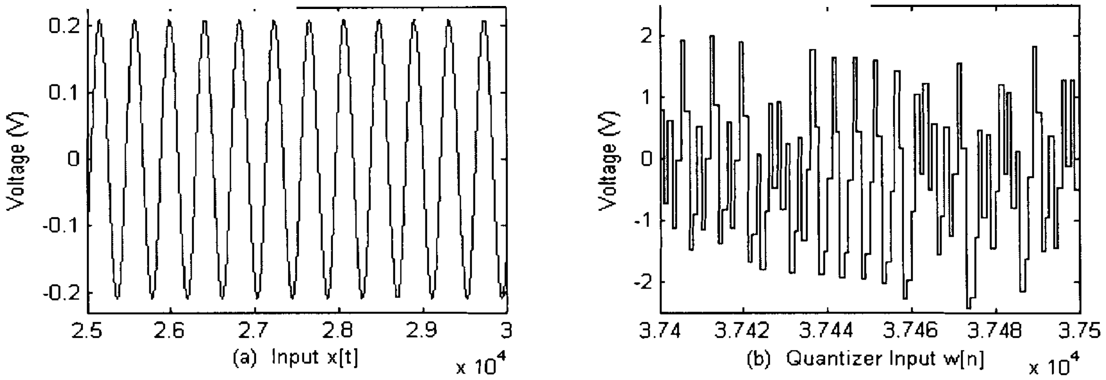


Figure 2-8 The undecimated single tone spectrum of the 2nd-order DT LPΣΔM

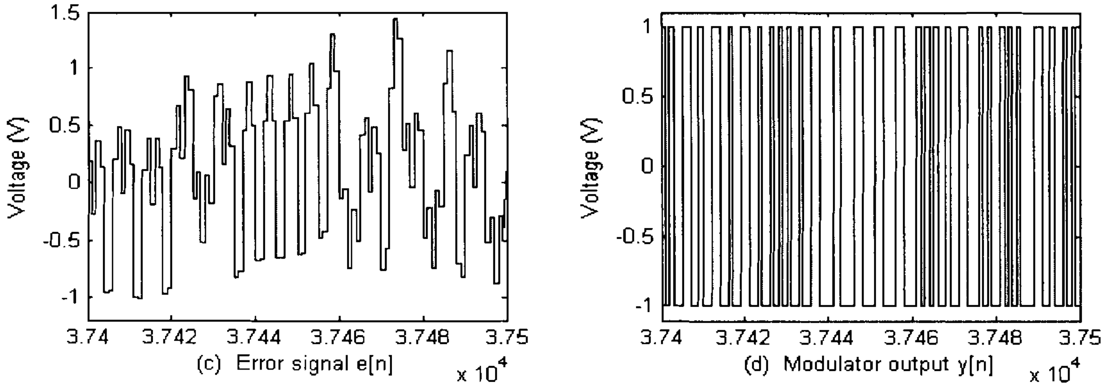


(a) First Integrator Output [V] (b) Second Integrator Output [V]

Figure 2-9 The 1^{st} and 2^{nd} integrator output of the 2^{nd}-order LPΣΔM



(a) Input x[t] (b) Quantizer Input w[n]



(c) Error signal e[n] (d) Modulator output y[n]

Figure 2-10 The 2^{nd} order LPΣΔM responding to a sinusoidal input

For an nth order LPΣΔM (n integrators in the loop), the noise transfer function is [30]:

$$NTF(z)=(1-z^{-1})^{n} \tag{2.22}$$

Transforming Equation (2.22) to the frequency domain gives:

$$NTF\ (f)=NTF\ (z)\Big|_{z=e^{j2\pi f/f_s}}=(1-e^{-j2\pi f/f_s})^{n}$$

Substituting this equation into Equation (2.16) gives the power spectrum of the output quantization noise, $P_{ey}(f)$:

$$\begin{aligned}
P_{ey}(f) &= \frac{2e_{rms}^{2}}{f_s}\left|(1-e^{-j2\pi f/f_s})^{n}\right|^{2} \\
&= \frac{2e_{rms}^{2}}{f_s}\left[\left|1-\cos\alpha+j\sin\alpha\right|^{2n}\right]\Big|_{\alpha=2\pi f/f_s} \\
&= \frac{2e_{rms}^{2}}{f_s}\left|2\sin\frac{\alpha}{2}\right|^{2n}\Big|_{\alpha=2\pi f/f_s} \\
&= \frac{2^{2n+1}e_{rms}^{2}}{f_s}\left|\sin\frac{\alpha}{2}\right|^{2n}\Big|_{\alpha=2\pi f/f_s}
\end{aligned}$$

The in-band quantization noise power, σ_{ey}^{2}, is then:

$$\begin{aligned}
\sigma_{ey}^{2} &= \int_{0}^{f_b} P_{ey}(f)\,df \\
&= \frac{2^{2n+1}e_{rms}^{2}}{f_s}\int_{0}^{f_b}\sin^{2n}\left(\frac{\pi f}{f_s}\right)df
\end{aligned}$$

For $f_b << f_s$, we can use a Taylor series expansion, see Equation (2.19), so that:

$$\begin{aligned}
\sigma_{ey}^{2} &\approx \frac{2^{2n+1}e_{rms}^{2}}{f_s}\int_{0}^{f_b}\left(\frac{\pi f}{f_s}\right)^{2n}df \\
&= \frac{2^{2n+1}e_{rms}^{2}}{f_s}\,\frac{f_s}{\pi}\,\frac{\left(\frac{\pi f_b}{f_s}\right)^{2n+1}}{2n+1}=\frac{\pi^{2n}e_{rms}^{2}}{2n+1}\left(\frac{2f_b}{f_s}\right)^{2n+1}
\end{aligned}$$

And therefore, the ideal in-band *SNR* for an nth order LPΣΔM can be written as:

$$\begin{aligned}
SNRn=&10\log_{10}(\sigma_{x}^{2})-10\log_{10}(e_{rms}^{2})-10\log_{10}\left(\frac{\pi^{2n}}{2n+1}\right) \\
&+(20n+10)\log_{10}(OSR)
\end{aligned} \tag{2.23}$$

The magnitude response of the NTF of a 1st, 2nd and 3rd order LP$\Sigma\Delta$M is shown in Figure 2-13. Although the higher order NTF provides more attenuation over the low frequency signal band, the out of band high frequency gain increases. Unfortunately, modulators with a one-bit quantizer and filters of order higher than 2 are only conditionally stable [36, 37]. Many methods and topologies have been suggested to overcome the instability of the $\Sigma\Delta$Ms [36, 37, 55, 86], for instance, careful choice of loop coefficients, limiting of the input signal range, or using a multi-stage structure [88, 89].

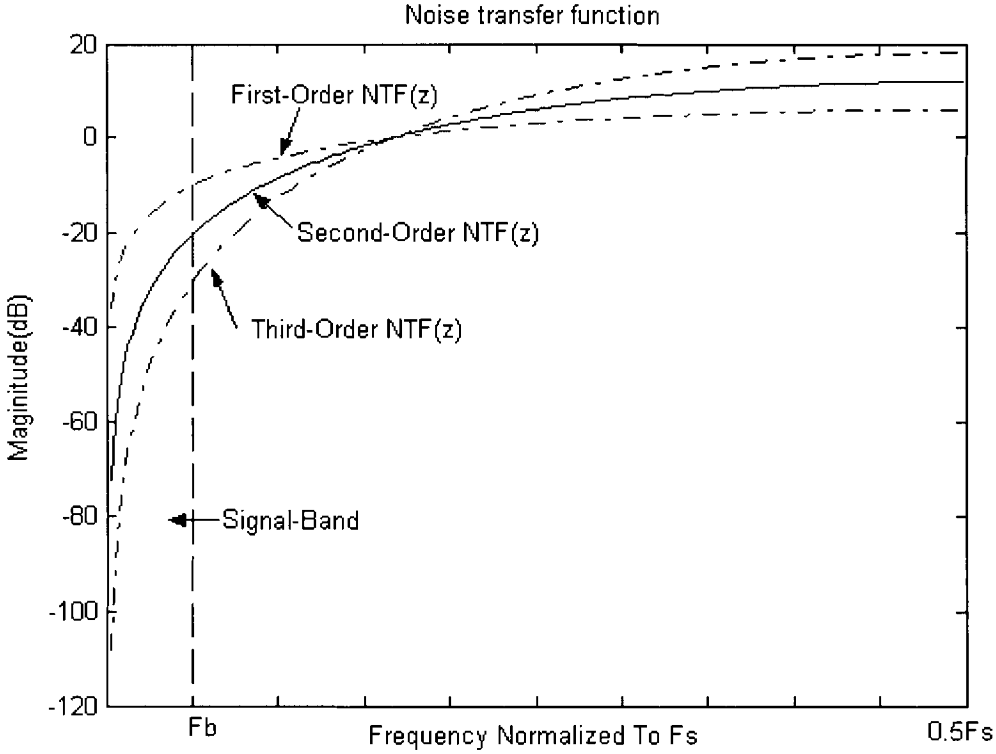


Figure 2-11 Magnitude responses of the 1st, 2nd and 3rd order NTF

2.3 The 4th-order, fs/4 DT BPΣΔM

The bandpass ΣΔM operates in much the same manner as a conventional lowpass modulator and retain many of the advantages that LPΣΔMs have over Nyquist-rate converters. A simple bandpass ΣΔM can be constructed by using the resonators to replace the integrators in the lowpass prototype.

Essentially, the BPΣΔM moves the noise notch from DC to an intended nonzero centre frequency. Figure 2-14 depicts the structure of a BPΣΔM. Here, the loop filter, H(z), is a bandpass filter and the noise transfer function, NTF (z), is a band-stop filter. This structure introduces nulls in the noise response within the pass-band and as a result, significantly increases the SNR within the pass-band.

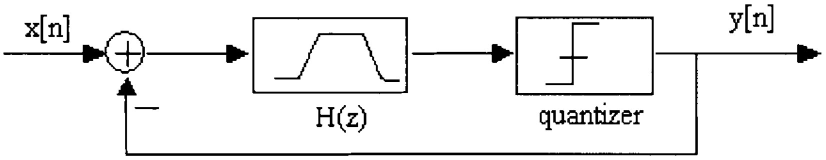


Figure 2-12 Schematic of a DT BPΣΔM

The typical approach to designing bandpass ΣΔMs is to start with a lowpass loop filter and perform a lowpass to bandpass mathematical transformation [38,50]. The transformation requires the substitution of z^{-1} with a second order system, i.e.:

$$z^{-1} \rightarrow -\frac{z^{-2} - a_1 z^{-1} + a_2}{a_2 z^{-2} - a_1 z^{-1} + 1} \tag{2.24}$$

where

$$a_1 = \frac{2\alpha k}{k+1} \tag{2.25}$$

$$a_2 = \frac{k-1}{k+1} \tag{2.26}$$

$$k = \cot\frac{\omega_{c2} - \omega_{c1}}{2}\tan\frac{\omega_{lp}}{2} \tag{2.27}$$

$$\alpha = \frac{\cos\frac{\omega_{c1} + \omega_{c2}}{2}}{\cos\frac{\omega_{c2} - \omega_{c1}}{2}} \tag{2.28}$$

ω_{c1} and ω_{c2} are the lower and the upper cutoff frequencies of the bandpass filter and ω_{LP} is the cutoff frequency of the lowpass filter. The frequency variables namely, ω_{LP}, ω_{c1} and

ω_{c2}, are all normalized such that the frequency range from DC to $f_s/2$ corresponds to 0 to π. The lowpass filter cutoff frequency ω_{LP} can be arbitrarily chosen to be equal to the bandwidth, ω_B, of the BPF, resulting in k in Equation (2.27) being unity. The cutoff frequencies, ω_{c1} and ω_{c2}, can be set equal to the desired resonator frequency, ω_c, when ω_B approach to zero for the ideal resonator [87]. Setting ω_{c1} and ω_{c2} in this manner results in α being equal to cos (ω_c) and k being equal to 1 as well:

$$k = \lim_{\omega_B \to 0} (\cot \omega_B \tan \frac{\omega_B}{2}) = 1$$

Therefore, Equations (2.24) through (2.28) become:

$$a_1 = \alpha \tag{2.29}$$

$$a_2 = 0 \tag{2.30}$$

$$k = 1 \tag{2.31}$$

$$\alpha = \cos \omega_c \tag{2.32}$$

Substituting these results into Equation (2.24), the lowpass to bandpass transformation for ideal resonators, becomes [52,87]:

$$z^{-1} \to \frac{\cos \omega_c \, z^{-1} - z^{-2}}{1 - \cos \omega_c \, z^{-1}} \;, \; where \quad \omega_c = 2\pi \frac{f_c}{f_s} \tag{2.33}$$

Based on Equation (2.33), a good choice for ω_c is $\pi/2$, which corresponds to the $f_s/4$ architecture. The reason that this is a good choice is that the loop filter design is simplified, since half of the coefficients are zero [52]. The discrete-time loop filter transfer function can be obtained using the following transformation:

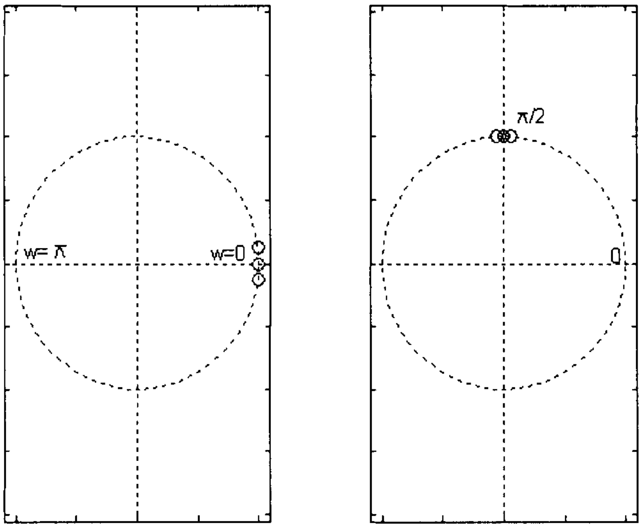
$$z_{lp}^{-1} \to -z_{bp}^{-2} \tag{2.34}$$

In the frequency domain, Equation (2.34) implies:

$$e^{-j\omega_{lp}} \to e^{\pm j\omega_s/2} \cdot e^{-j2\omega_{bp}}$$

$$\Rightarrow \qquad \omega_{bp} = \pm \frac{\omega_s}{4} + \frac{\omega_{lp}}{2} \tag{2.35}$$

Where ω_s is the sampling frequency, ω_{bp} is the mapped bandpass frequency and ω_{lp} is the original lowpass frequency. From Equation (2.35), it is observed that the null in the quantization noise that appears at DC in the lowpass ΣΔM is moved to $\pm\omega_s/4$ in the bandpass ΣΔM. Figure 2-15 depicts the transformation of the NTF zeros.



(a) 2^{nd}-order LPΣΔM, (b) 4^{th}–order BPΣΔM.

Figure 2-13 The frequency transformation of NTF zeros

When performing the transformation of Equation (2.34), a canonical bandpass resonator is produced from a delayed, discrete-time integrator [67]:

$$H_{reso}(z) = \left.\frac{z^{-1}_{inte}}{1 - z^{-1}_{inte}}\right|_{z^{-1}_{inte} = -z^{-2}} = \frac{-z^{-2}}{1 + z^{-2}} \tag{2.36}$$

In the same manner, the loop transfer function of the discrete-time BPΣΔM can be obtained from its lowpass equivalent given in Equation (2.15):

$$H_{bp}(z) = \left.\frac{2z_{lp}^{-1} - z_{lp}^{-2}}{\left(1 - z_{lp}^{-1}\right)^2}\right|_{z_{lp}^{-1} = -z^{-2}} = \frac{-2z^{-2} - z^{-4}}{\left(1 + z^{-2}\right)^2} \tag{2.37}$$

Substituting Equation (2.37) into Equations (2.2) and (2.3) gives the NTF (z) of the BPΣΔM:

$$NTF_{bp}(z) = \frac{1}{1 + H_{bp}(z)} = (1 + z^{-2})^2 \tag{2.38}$$

From these equations, the canonical 4th-order BPΣΔM is obtained. The order of the BPΣΔM is twice the order of the lowpass ΣΔM. The order of the bandpass modulator refers to the number of poles in the NTF.

There are many filter structures to implement a given loop filter, H (z), and with an ideal realization of the filter, all of them would result in modulators with identical behaviour. However, different filter structures have different sensitivities to component errors, op-amp performance and noise.

By directly replacing z^{-1} with $-z^{-2}$ in the structure shown in Figure 2-7, the structure of Figure 2-16a results.

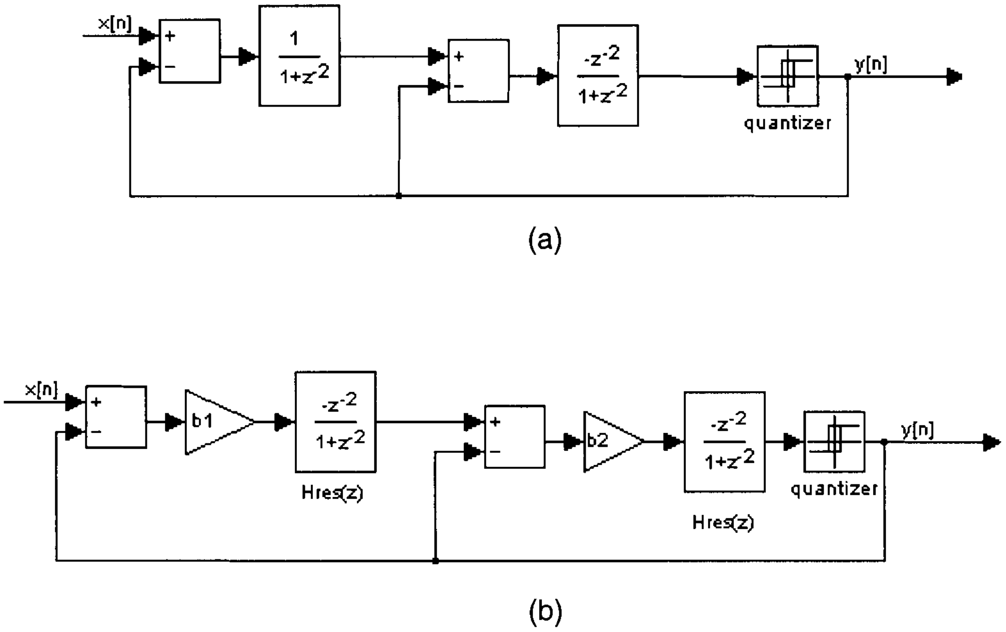


Figure 2-14 (a) The 4th-order DTBPΣΔM directly from the 2nd-order LPΣΔM
(b) The 4th-order DT BPΣΔM with double resonators

The cascade-of-resonators structure, depicted in Figure 2-16b, is frequently used because large capacitor errors contribute less than one LSB to the quantization error [6]. In order to generate the same loop filter response given in Equation (2.37), two-gain blocks, b_1 and b_2, need to be added to the structure as shown in Figure 2-16b.

The transfer function of Figure 2-16b is:

$$H_{bp}(z)=b_2 H_{res}(z)+b_1 b_2 H_{res}(z)^2 \tag{2.39}$$

Substituting Equation (2.37) into Equation (2.39), and solving for coefficients b_1 and b_2 yields:

$$b_1 = 0.5 \qquad\qquad b_2 = 2 \tag{2.40}$$

Under the linear model assumption we discussed in section 2.1.1, the quantization noise power spectrum of the 4th-order bandpass sigma-delta modulation is:

$$P_{ey}(f)=\frac{2e_{rms}^2}{f_s}\left|(1+z^{-2})^2\right|^2\Big|_{z=e^{j2\pi f/f_s}}=\frac{32e_{rms}^2}{f_s}\cos^4\left(\frac{2\pi f}{f_s}\right) \tag{2.41}$$

Since $f_b << f_s$, the Taylor series expansion of Equation (2.19) can be used to find the in-band noise power, σ_{ey}^2:

$$\begin{aligned}\sigma_{ey}^2 &= \int_{f_s/4-f_b/2}^{f_s/4+f_b/2} P_{ey}(f)\,df \\ &= \frac{32e_{rms}^2}{f_s}\int_{f_s/4-f_b/2}^{f_s/4+f_b/2}\cos^4\left(\frac{\pi f}{f_s}\right)df \\ &\cong \frac{\pi^4 e_{rms}^2}{5}(OSR)^{-5}\end{aligned} \tag{2.42}$$

Equation (2.42) is the same as that obtained for the second-order LPΣΔM given by Equation (2.20). Thus, the SNR for the 4th-order BPΣΔM is:

$$SNR=10\log_{10}(\sigma_x^2)-10\log_{10}(e_{rms}^2)-10\log_{10}\left(\frac{\pi^4}{5}\right)+50\log_{10}(OSR) \tag{2.43}$$

As we can see, the transformation of $z^{-1} \rightarrow -z^{-2}$ does not change the SNR of the system. The dynamic range of the BPΣΔM is shown in Figure 2-17 for two different OSRs. These curves are nearly identical to the lowpass curves shown in Figure 2-9.

Using the circuit in Figure 2-16b with $b_1 = 0.5$ and $b_2 = 2$, as well as an input tone at 2100MHz, yields the SNDR plot shown in Figure 2-17. The SNDR is 96.7dB with an OSR of 210. The theoretical result of Equation (2.43) is approximately 102 dB. The reason for the 4 to 5 dB discrepancy was discussed in section 2.2.

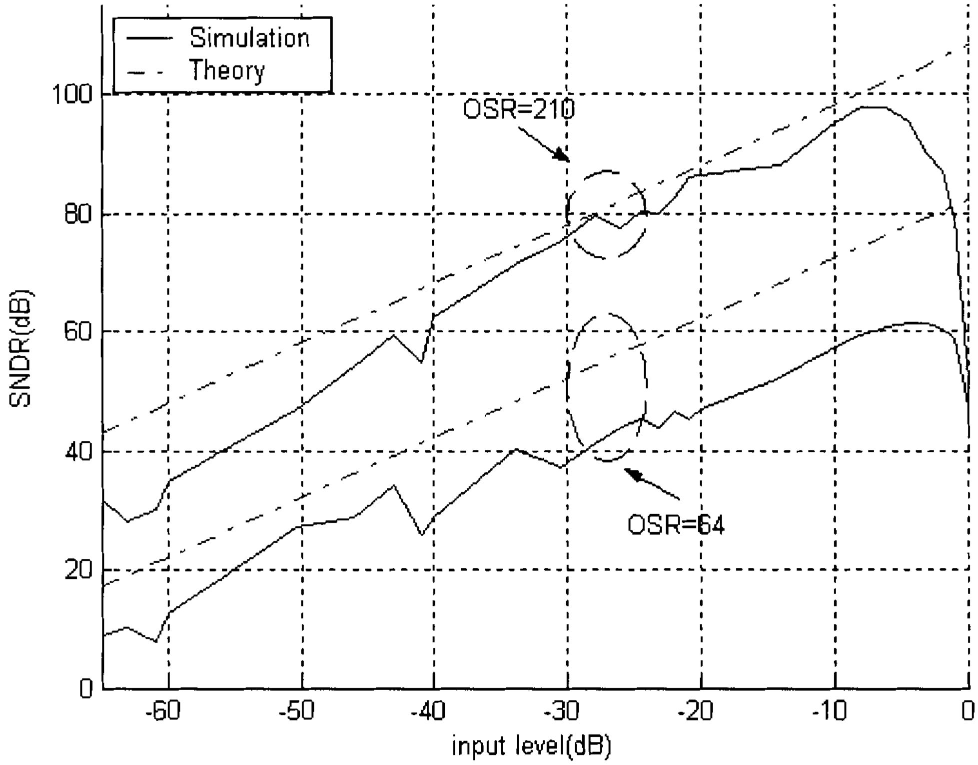


Figure 2-15 **SNDR vs. input signal level for the 4th-order, fs/4 DT BPΣΔM**

Simulation results for the 4th-order BPΣΔM are shown in Figure 2-18. Theses results show that there are some strong tones near DC, $f_s/2$, $f_s/8$, $3f_s/8$ for the $f_s/4$ structure. Similar results were found in [43]. Although these tones lie in the stop band region, they can potentially degrade the noise and distortion characteristics of the bandpass modulator by mixing with the input signal and falling into the pass band. This problem can be partially mitigated by centring the resonator frequency away from $f_s/4$ (see Figure 2-19), especially for the low-level input signal, or by adding a dithering signal before the quantizer. Centring the resonator frequency away from $f_s/4$ allows us to change the notch position and zeros of the NTF. Because the quantization error is typically not white and contains components harmonically related to the input frequency and amplitude, the dither signal can whiten the quantization error and decorrelate the quantizer input signal, and hence reduce or even eliminate the spurious tones and modulated noise [9].

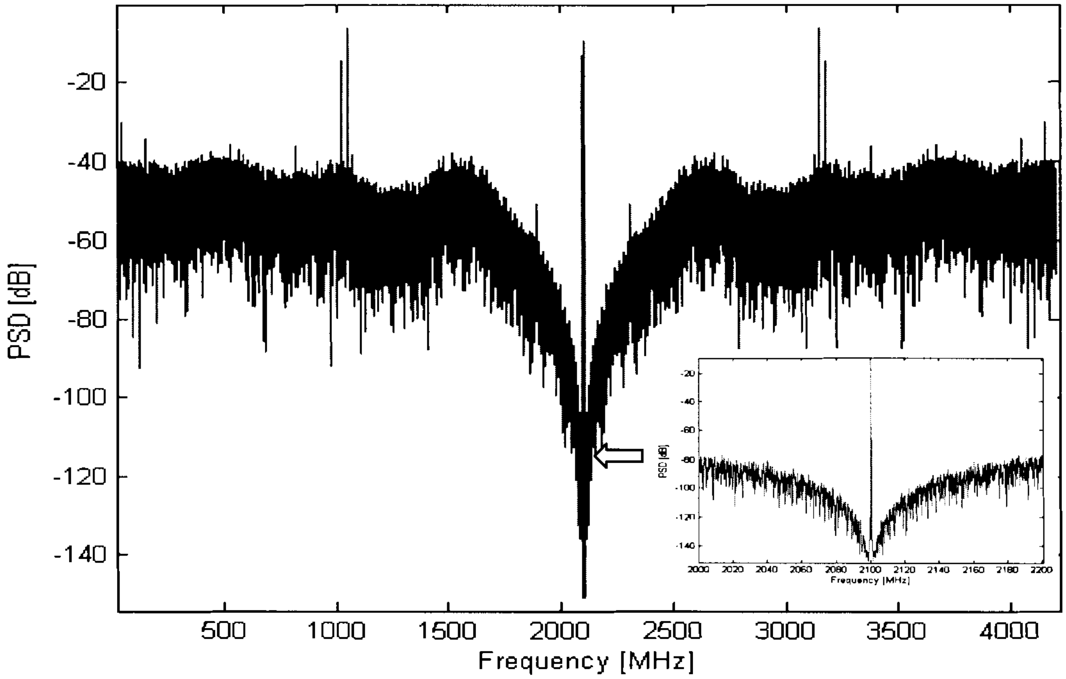


Figure 2-16 The undecimated spectrum of the 4th-order, $f_s/4$ DT BPΣΔM

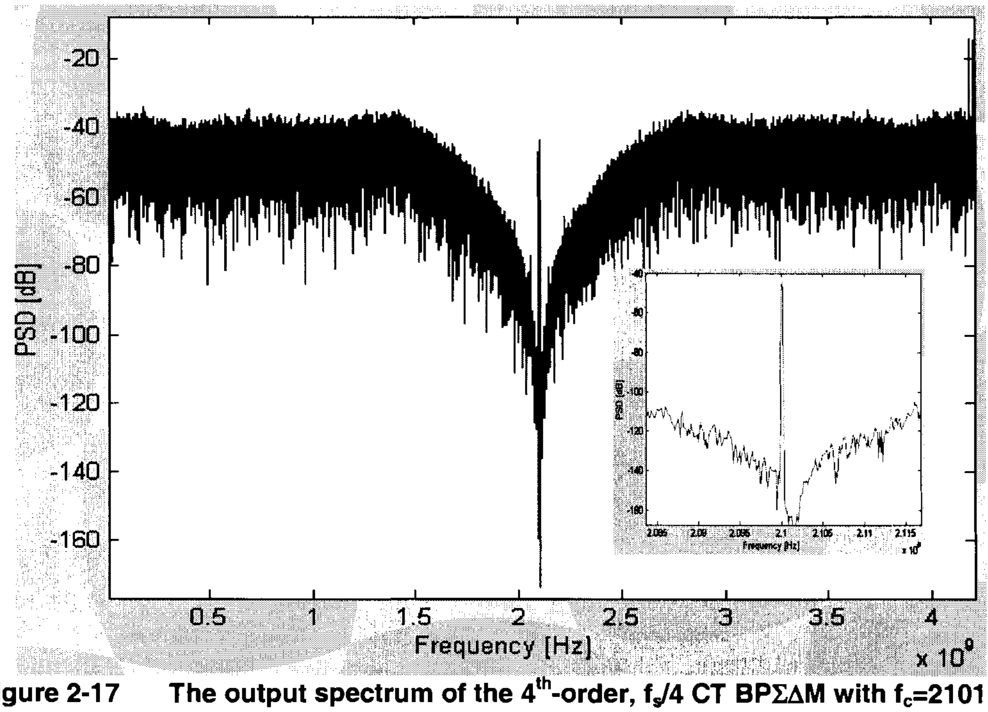


Figure 2-17 The output spectrum of the 4th-order, $f_s/4$ CT BPΣΔM with f_c=2101MHz

2.4 The 4^{th}-order, f_s/x DT BPΣΔM

Since multiple mobile communication standards are in use today, a multi-standard system that can serve people more efficiently, and save resources at the same time, is worthy of attention. In this section, we will use the lowpass to bandpass transformation to develop an architecture that can be employed in a multi-standard environment by adjusting relevant system parameters.

Using the transformation, which is illustrated in Equation (2.33), the fourth order bandpass loop filter can be derived as follow:

$$\begin{aligned} H_{bp}(z) &= \left.\frac{2z_{lp}^{-1} - z_{lp}^{-2}}{\left(1 - z_{lp}^{-1}\right)^2}\right|_{z_{lp}^{-1} = \frac{\cos\omega_c z^{-1} - z^{-2}}{1 - \cos\omega_c z^{-1}}} \quad where\ \omega_c = 2\pi\frac{f_c}{f_s} \\ &= \frac{(\cos\omega_c z^{-1} - z^{-2})\left(2 - 3\cos\omega_c z^{-1} + z^{-2}\right)}{(1 - 2\cos\omega_c z^{-1} + z^{-2})^2} \end{aligned} \tag{2.44}$$

$H_{bp}(z)$ can be implemented by two second order loop filters, $H_1(z)$ and $H_2(z)$, as shown in Figure 2-20a.

The output y [n] of Figure 2-20a in the z domain is:

$$\begin{aligned} Y(z) &= [(X(z) - Y(z))H_1(z) - Y(z)]H_2(z) + E(z) \\ Y(z) &= \frac{H_1(z)H_2(z)}{1 + H_2(z) + H_1(z)H_2(z)}X(z) + \frac{1}{1 + H_2(z) + H_1(z)H_2(z)}E(z) \end{aligned} \tag{2.45}$$

As was discussed in section 2.1, the magnitude of the STF within the signal band should be close to unity and the NTF must be carefully designed to achieve the desired noise shaping. From Equation (2.3), the NTF (z), in term of $H_{bp}(z)$, is given by:

$$NTF(z) = \frac{1}{1 + H_{bp}(z)} \tag{2.46}$$

By equating Equation (2.46) and the NTF of Equation (2.45), it is evident that:

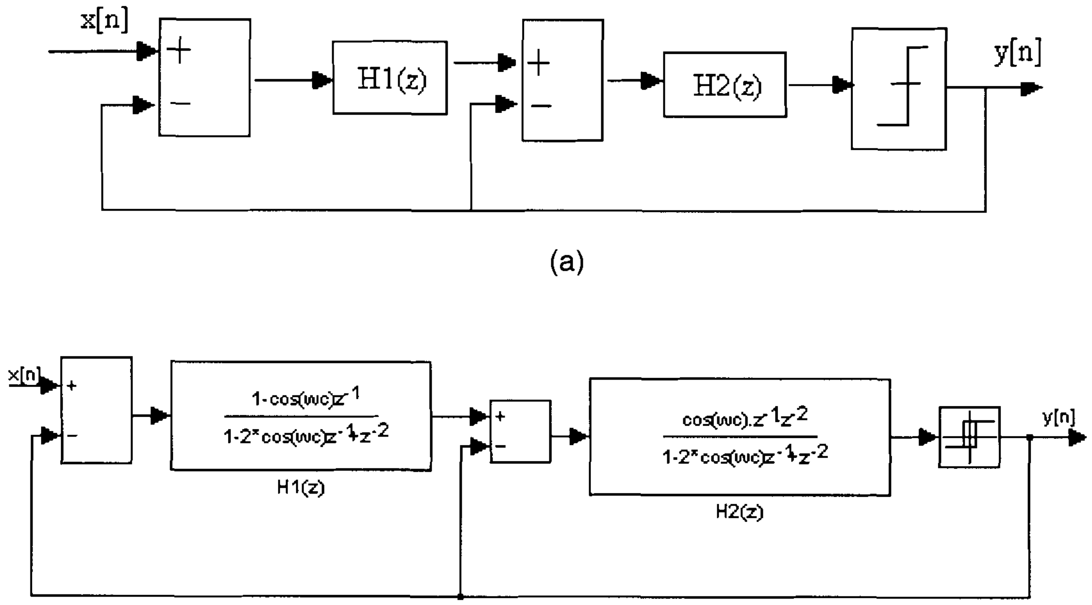
$$H_{bp}(z) = H_2(z) + H_1(z)H_2(z) \tag{2.47}$$

Furthermore, by substituting Equation (2.44) into Equation (2.47), after some simplification, we obtain:

$$H_1(z)=\frac{1-\cos(\omega_c)z^{-1}}{1-2\cos(\omega_c)z^{-1}+z^{-2}} \qquad (2.48)$$

$$H_2(z)=\frac{\cos(\omega_c)z^{-1}-z^{-2}}{1-2\cos(\omega_c)z^{-1}+z^{-2}} \qquad (2.49)$$

Thus, Figure 2-20a can be modified by substituting for $H_1(z)$ and $H_2(z)$, as shown in Figure 2-20b.



(a)

(b)

Figure 2-18 (a) Schematic of the 4th-order, f_s/x DT BPΣΔM
(b) The 4th-order, f_s/x DT BPΣΔM

From Equations (2.44) and (2.46), the noise transfer function is:

$$NTF_{bp}(z)=\frac{(1-2\cos\omega_c\, z^{-1}+z^{-2})^2}{(1-\cos\omega_c\, z^{-1})^2} \qquad (2.50)$$

The zeros of the $NTF_{bp}(z)$ can be positioned anywhere between DC and $f_s/2$. In addition, the centre frequency, f_c, of the resonator can be at any arbitrary frequency, f_s/x, where $2 < x < \infty$. Nevertheless, constraining x to be an integer can simplify the design of the decimation filters that follow the sigma-delta modulator [6].

The dynamic range of the system shown in Figure 2-20b was investigated for different values of f_c. Specifically, results were compiled for f_c equal to $f_s/10$, $f_s/7$ and for reference, $f_s/4$. These results are shown in Figure 2-21. In the case of the $f_s/10$ and $f_s/7$ systems, despite the fact that they have a different NTF, the dynamic range results of each are nearly identical.

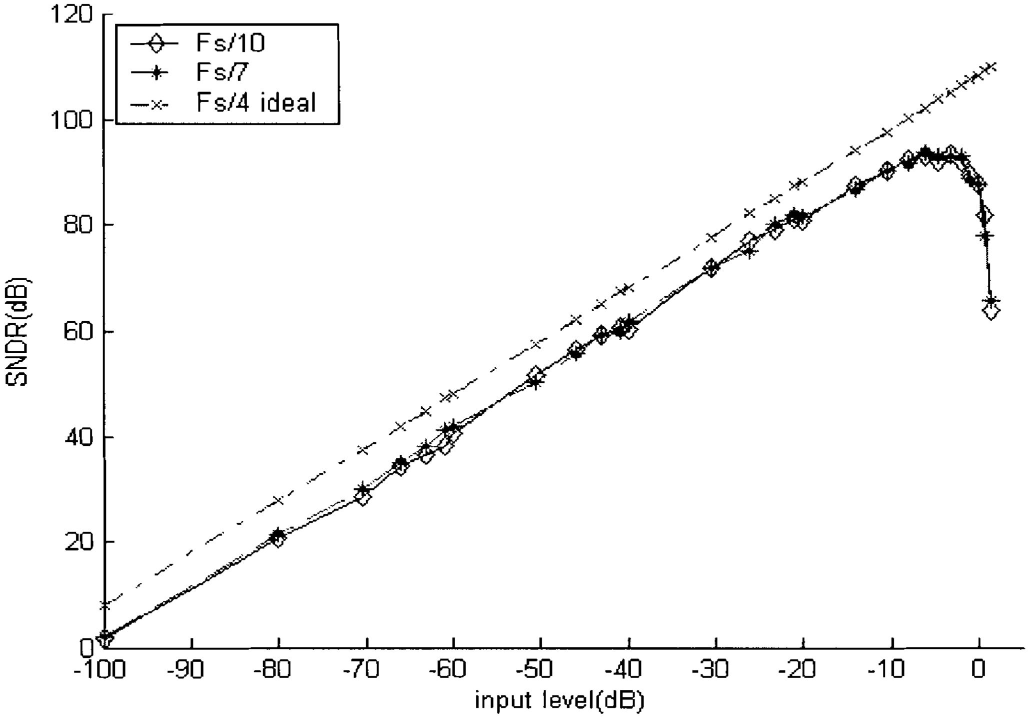


Figure 2-19 The dynamic range of 4th-order, $f_s/10$, $f_s/7$ DT BPΣΔMs

Since the focus here is mainly on the IS-95 (840MHz) and UMTS (2100MHz) standards, the $f_s/4$ and $f_s/10$ structures, respectively, can be used to implement a ΣΔM for the standards if the modulator's sampling frequency is 8400MHz. In this section the $f_s/10$ ΣΔM is discussed.

The magnitude response of the NTF of the $f_s/10$ ΣΔM is illustrated in Figure 2-22. The maximum out-of-band gain is 4. In Figure 2-23, the output spectrum of $f_s/10$ ΣΔM with an input tone at 840MHz and having a power of 6dB is shown. The in-band SNDR is 92.4dB and we observe that there are no tones near DC or $f_s/2$. Even for input signals of low amplitude, there are not many tones out of band like the $f_s/4$ structure. These are advantages of the $f_s/10$ structure, although its structure is more complex than the $f_s/4$ structure [87].

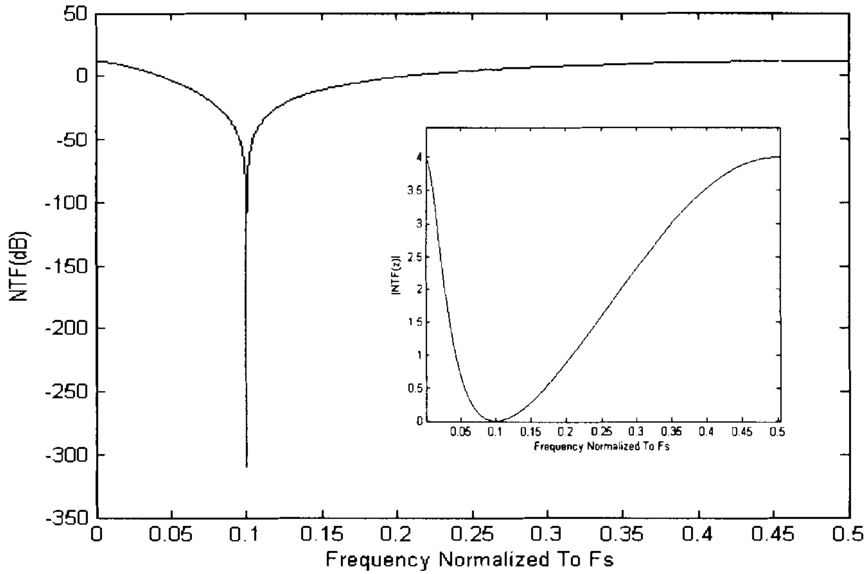


Figure 2-20 The magnitude response of the NTF in the 4^{th}-order BPΣΔM

A multi-band f_s/x fourth order BPΣΔM based upon a lowpass to bandpass transformation is shown in Figure 2-20b. Since the stability or the peak signal-to-noise ratio is correlated to the out-of-band gain of the NTF [2,7,8], this structure can be augmented to enhance its stability and/or peak SNDR by adjusting the out of band gain of its NTF [9]. The out of band gain of the NTF can be adjusted by adding two gain blocks before the resonators as shown in Figure 2-24.

The gain blocks, g_1 and g_2, before the first resonator and the second resonator, can be used to tune the out of band gain of the NTF to obtain the desired SNR or increase the maximum stable input signal amplitude. Changing the value of g_1 and g_2 leaves the zeros of the NTF unchanged, however, the poles change. Note that, the second gain block, g_2, does not affect the behaviour of the ideal modulator because the second resonator is followed immediately by a single threshold quantizer. The magnitude of g_2 can be adjusted arbitrarily without impairing the performance of the modulator [5]. However, variation of g_1 can alter the noise shaping of the BPΣΔM and, consequently can change the performance of the A/D converter.

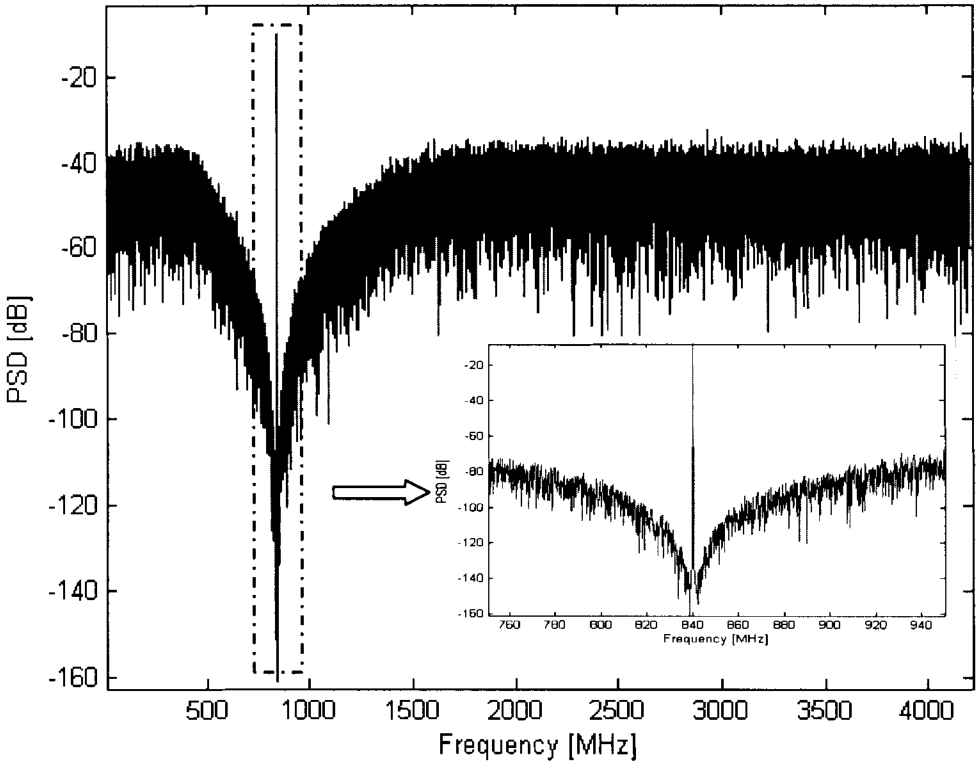


Figure 2-21 The output spectrum of the 4th-order, $f_s/10$ DT BPΣΔM

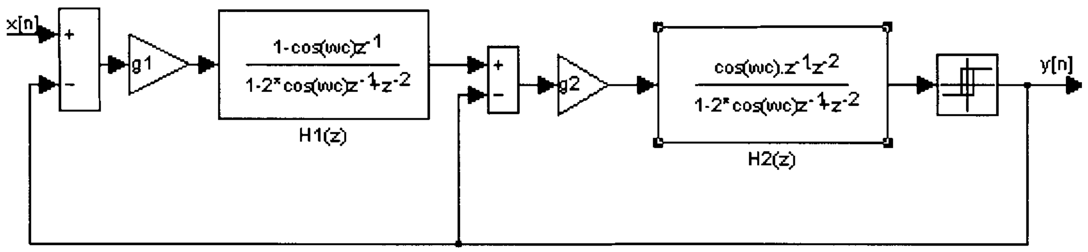


Figure 2-22 The 4th-order, f_s/x DT BPΣΔM with the tuneable NTF

The architecture derived by direct synthesis of NTF (z) has more flexibility than those derived by transforming a lowpass prototype. For discrete-time ΣΔMs, one can use an optimization algorithm [8,9, 49, 93] or some computer filter approximator [42,94] to design an arbitrary band-reject NTF (z) at a desired centre frequency considering some modulator stability, bandwidths and/or variant OSR constraints. Increasing the out-of-band gain of NTF will increase the Peak SNDR, however, the penalty is the decreased stable input range. The detailed discussion will be presented in Chapter 3.

In this chapter the effects of oversampling and noise shaping were discussed. The requirements for which the quantization error can be assumed to be white and uniformly distributed were presented. The BPΣΔM derived from a lowpass prototype was discussed. Simulation results show: a) that the bandpass modulator is stable, if and only if, the lowpass modulator is stable, and b) that the SNR curves of the modulators are identical. In particular, a fourth-order, f_s /4 modulator designed in this manner can be proven to be stable because the prototype lowpass second-order modulator is known to be stable [40].

In addition, the flexible f_s/x architecture derived from the lowpass architecture was discussed and analysed. The output spectrum of the f_s/x ($x \neq 4$) ΣΔM is smoother than the $f_s/4$ ΣΔM, without tones located at $f_s/2$, nor at DC.

A direct implementation of a specific noise-shaping function without relying on the transformation from the lowpass domain will be discussed in the next chapter.

Chapter 3

Multi-band 4^{th}-order CT BPΣΔM

As was outlined in Chapter 1, the goal is to implement a BPΣΔM that operates at RF frequencies. DT BPΣΔMs that employ switched-capacitor or switched current circuits are impractical for this purpose. Switched-capacitor and switched current circuits suffer from: 1) a clock rate that is limited both by the op amp gain bandwidth and by the fact that circuit waveforms require several time constants (i.e., clock periods) to settle [14]; 2) power dissipation that is an order of magnitude higher than continuous-time filters [44,45]; not being readily transferable to other high-speed technologies, such as silicon bipolar or other III-V technology [11]. Unlike switched-capacitor and switched current circuits, continuous-time filters can be operated at high frequencies without a performance penalty and generate less switching noise. Furthermore, in a CT BPΣΔM, sampling occurs at the output of the CT loop filter. As a result, the loop filter operates as an anti-aliasing filter, hence, discarding the need for an anti-aliasing filter in front of the CT ΣΔM (which is required in a system using a DT BPΣΔM).

Since the clocked quantizer is inside the CT loop, an ideal CT modulator can be derived from a DT ΣΔM by mapping the z-domain description to the s-domain. Conveniently, analysis of the stability of the modulator, the theoretical limit of the achievable signal to noise ratio and the distortion-free dynamic range, can all be done in the z-domain. In fact, the noise-shaping behaviour of a CT ΣΔM can be designed entirely in the discrete-time domain [52].

The CT BPΣΔM architecture, designed by directly implementing the desired noise shaping specification and having the required stability, is presented in this chapter. The aim is to build an architecture that can operate over multiple-bands with the minimum number of hardware components. In this chapter, the $f_s/4$ multi-feedback architecture built in [14,16] is used as a starting point. This $f_s/4$ architecture is then extended to an f_s/x continuous-time fourth order BPΣΔM, by tuning the feedback pulse coefficients and the resonator centre frequency.

Again, since the primarily focus is on the IS-95 (CDMA) and UMTS (WCDMA) standards, the centre frequencies are chosen to be 840MHz and 2100MHz, respectively. The modulators sampling rate is chosen to be 8400 MHz, thus, the $f_s/4$ and $f_s/10$ architectures are principally investigated and simulated.

3.1 The Noise Transfer Function

ΣΔMs are also known as "Noise Shaping Converters." The NTF minimizes the quantization noise in a given band and maximizes the overall in-band signal to noise ratio of the converter. There are two constraints on NTF design [6]: causality and stability.

To satisfy **causality**, the loop around the quantizer cannot be delay free; otherwise, the modulator would represent an inconsistent, unrealisable system. Causality is satisfied by setting the leading coefficients (those multiplying z^n) of the numerator and denominator polynomials of NTF(z) to 1 [9]. In terms of the transfer function, this constraint forces:

$$\lim_{z \to \infty} NTF(z) = 1$$

A consequence of the causality constraint is that one cannot force the magnitude of the NTF to zero in every instance.

Stability is a difficult problem in the realm of ΣΔMs. The stability of a ΣΔM is limited. A practical definition of stability is that a modulator is stable if it "works". An unstable modulator means that the modulator exhibits large, and possibly unbounded states that remain even after removing the input signal and the output SNR is poor in comparison to that predicted by the linear model. In general terms, if the out-of-band noise gain is too high, the overall internal filter states will run away [2]. As a guideline, Lee [7] proposed that for a 1-bit quantizer the modulator is stable if the peak magnitude gain of the NTF at every frequency is less than 2. However, this constraint is neither necessary nor sufficient to guarantee stability [2]. For a higher-order NTF, which corresponds to more aggressive noise shaping, the maximum out-of-band-gain may be smaller.

Using the above two constraints, the NTF filter of the BPΣΔM can be implemented by a band-stop filter where the stop band edge is the edge of the desired signal pass band. The zeros of *NTF(z)* must be positioned at the desired noise null and they must be placed exactly on the unit circle, ("infinite Q"), as this will result in a very deep modulator noise notch. If the zero radius is reduced, this "over stability" may generate "dead bands" [2,3], which can cause intermodulation distortion. For normalization purposes we put complex zeros at $e^{\pm j\theta}$ where θ is equal to $2\pi f_c/f_s$. The numerator of *NTF(z)* is

$$NTF_{num}(z) = \left[\left(z^{-1} - e^{j\theta}\right)\left(z^{-1} - e^{-j\theta}\right)\right]^2 = \left(1 - 2\cos\theta\, z^{-1} + z^{-2}\right)^2 \qquad (3.1)$$

By adjusting the complex zero location of the NTF, an improvement of several decibels in SNR may be possible. The NTF denominator, NTF_{den} is introduced because the correct noise shaping does not guarantee stability when a 1-bit quantizer cannot track the input closely enough and accumulates a large error. With the correct choice of NTF_{den}, a maximally flat out-of-band NTF response can be obtained. For optimum performance, we want the poles to be far away from zero, but not so far as to cause the modulator to be unstable or nearly so [8]. The Butterworth pole alignment of the NTF is often a good choice and is commonly used in commercial products. One reason for this is that the relatively low Q poles can reduce the potential instability, and therefore the Butterworth alignment tends to be less susceptible to oscillation caused by input signals that are at the same frequency as the poles [9].

Given the two constraints stated, one can use the ΣΔ design toolbox [49] to calculate the desired NTF (z).

The MATLAB command line is:

$$\text{NTF} = \text{synthesizeNTF (order, Ngain, } f_0) \qquad (3.2)$$

Where *order* is the order of the BPΣΔM; Ngain is the maximum out-of-band-gain of NTF(z); f_0 is the ratio between the centre frequency, f_c, and the sampling frequency, f_s. In this case the order is chosen to be equal to 4, Ngain to be 1.8 and f_0 to be 0.1. For these parameters the NTF is:

$$NTF(z)=\frac{1-3.2361z^{-1}+4.618z^{-2}-3.2361z^{-3}+z^{-4}}{1-2.2666z^{-1}-2.3995z^{-2}-1.2977z^{-3}+0.3086z^{-4}} \tag{3.3}$$

The numerator of NTF (z) is equal to:

$$NTF(z)_{num}=(1-2\cos\frac{\pi}{5}z^{-1}+z^{-2})^2 \tag{3.4}$$

For Equation (3.4), the noise notch is located at $0.1f_S$, as expected. Specifically, the zeros are located at ± π/5, and are shown in Figure 3-1 along with the poles of NTF(z). The poles of NTF(z) guarantee the maximum out-of-band gain of the NTF and hence, ensure the stability.

We can adjust the order and the out-of-band gain of the NTF to design a stable system by using Schreier's toolbox [49]. The relation between the out-of-band gain of the NTF and the modulator's SNDR will be illustrated in section 3.4. Once we have the NTF, the loop filter transfer function can be determined, and hence the coefficients of the CT BPΣΔM can be calculated.

Figure 3-1 shows the poles and zeros of the NTF of a fourth-order $f_s/10$ BPΣΔM with an out-of-band gain equal to 1.8. The magnitude response of the NTF is shown in Figure 3-2.

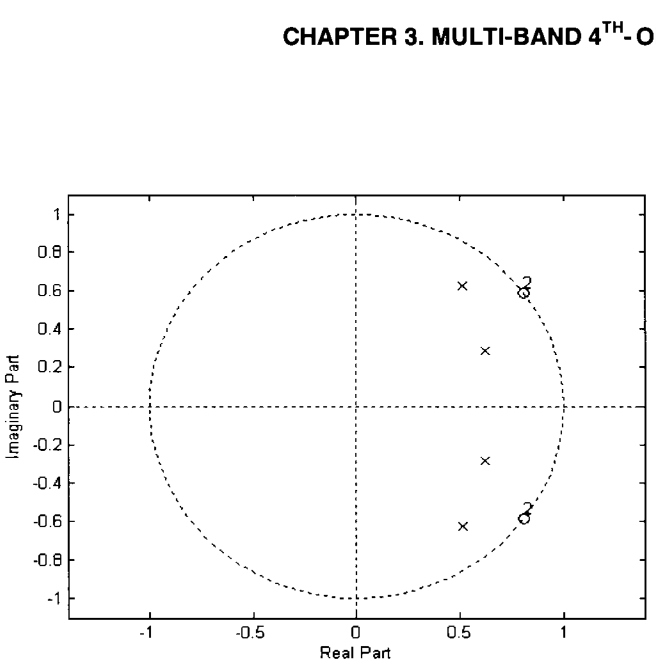


Figure 3-1 Poles and zeros constellation of the NTF of the 4th-order $f_s/10$ BPΣΔM

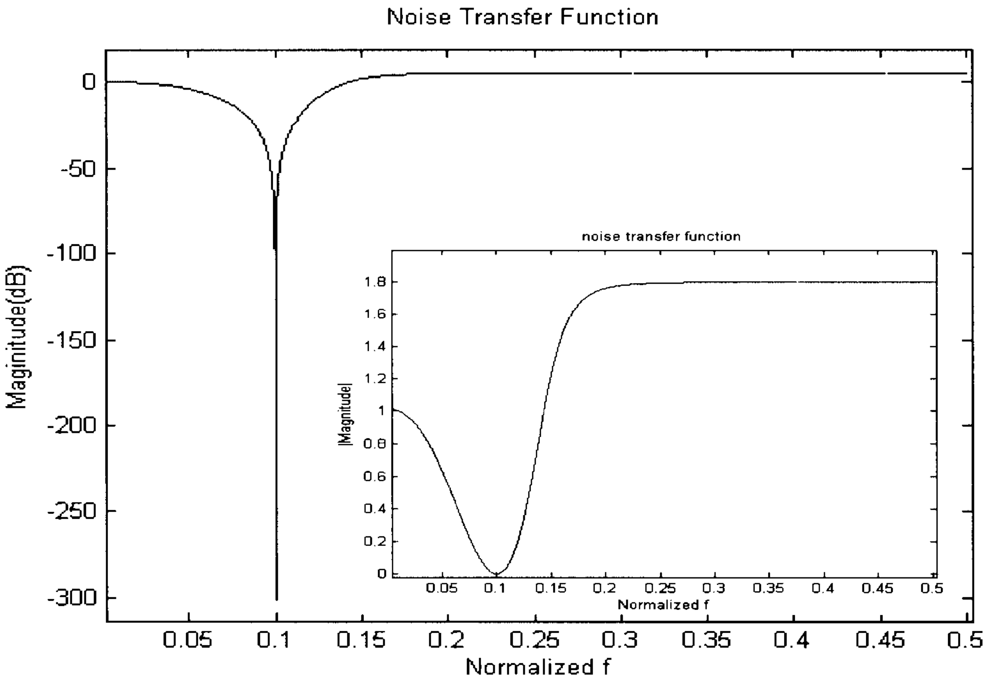
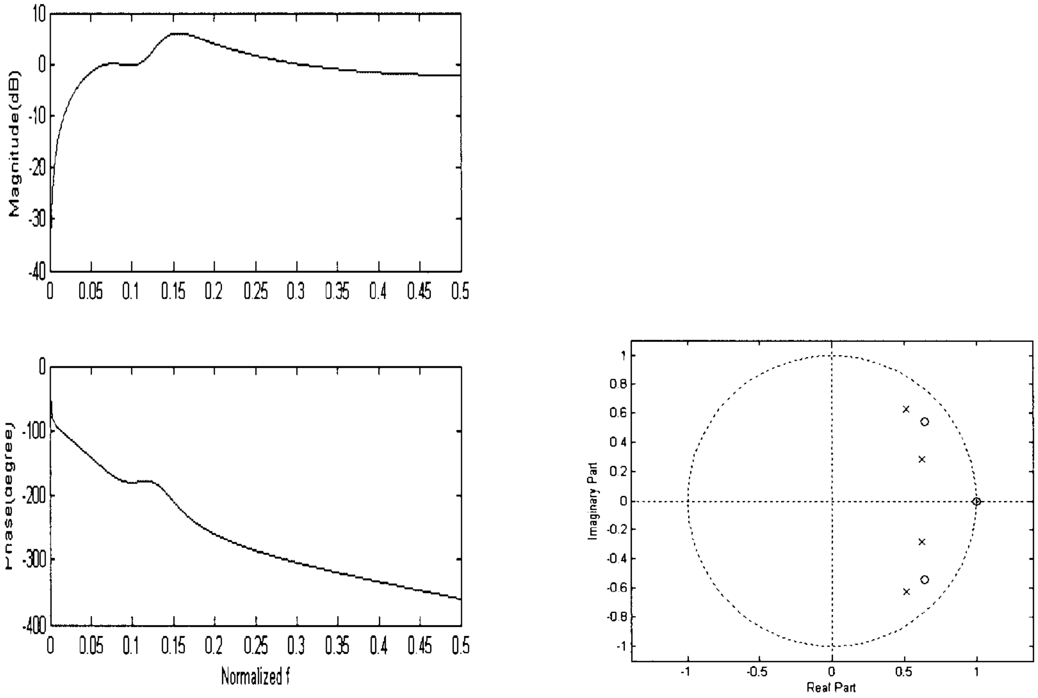


Figure 3-2 The magnitude response of the NTF in the 4th-order $f_s/10$ BPΣΔM with the out-of-band gain of 1.8

3.2 The Signal Transfer Function

The modulator's input-output STF spectrally shapes the input signal. Depending on the chosen architecture, it may or may not be possible to independently specify the STF from the NTF. Normally, the desired STF is flat over the band of interest, and is typically designed for unity gain and linear phase [35]. Some out-of-band attenuation is acceptable to reduce the total signal power and enhance stability. With the correct choice of zeros, the adjacent radio channels can be rejected [17]. The magnitude and phase response of *STF(z)* is shown in Figure 3-3. The poles of *STF(z)* are the same as that of *NTF(z)*.



a) Magnitude and phase response **b) pole-zero constellation**

Figure 3-3 The STF of the 4^{th}order, $f_s/10$ BPΣΔM

3.3 Design Methodology of CT BPΣΔMs

Single-bit continuous-time sigma-delta modulation is a good technique for analog-to-digital conversion (ADC), as it incorporates inherent anti-aliasing filtering, has excellent linearity performance, and can consume little power. All of these performance factors are particularly important in a battery-powered transceiver.

A general diagram of a continuous-time modulator is depicted in Figure 3-4. The continuous-time input, $x(t)$, is applied to a modulator with a CT loop filter, H(s), whose output is indicated as $u(t)$. The quantizer samples $u(t)$ at frequency f_s and yields a DT output signal, $y[n]$, which is fed back through a DAC (digital-to-analog converter). Compared to the discrete-time ΣΔM shown in Figure 2-1, reproduced in Figure 3-5, if the output sequence, $y[n]$ of both modulators is the same, we can say they are equivalent. In other words, if the input, $u[n]$, to the quantizer is the same at the sampling instants of both modulators, their output bit sequence, $y[n]$, is the same.

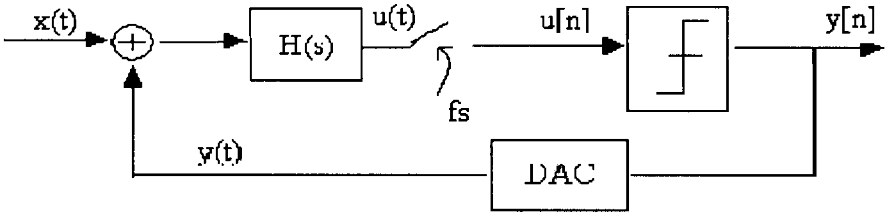


Figure 3-4 A general model of a continuous-time ΣΔM

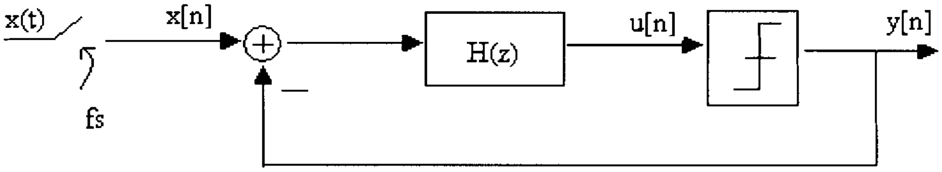


Figure 3-5 A general model of a discrete-time ΣΔM

Figure 3-6a shows the loop transfer function from the output of the quantizer back to its input. This loop transfer function must be equivalent to the discrete-time ΣΔM transfer function shown in Figure 3-6b. Therefore, the loop transfer function can be equated according to [48]:

$$Z^{-1}\left[-H(z)\right]=L^{-1}\left[R_{DAC}(s)H(s)\right]\Big|_{t=nT_s} \tag{3.5}$$

Where Z^{-1} is the inverse z-transform and L^{-1} is the inverse Laplace transform. Equation (3.5) can be expressed in the time domain [52] by:

$$h[n]=\left[r_{DAC}(t)*h(t)\right]\Big|_{t=nT_s}=\left[\int_{-\infty}^{\infty}r_{DAC}(\tau)h(t-\tau)\,d\tau\right]\Big|_{t=nT_s} \tag{3.6}$$

Where r_{DAC} (t) is the impulse response of a zero-order-hold (*ZOH*) pulse.

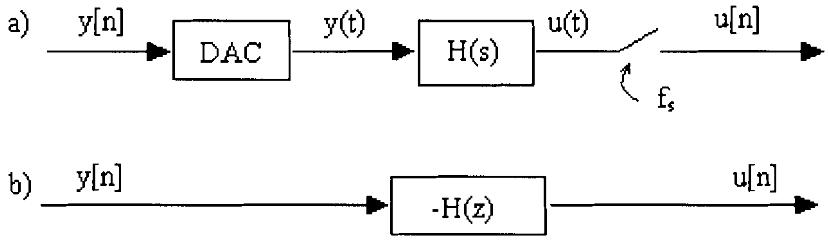


Figure 3-6 ΣΔM open loop block diagrams
a) continuous-time,
b) discrete-time

There are three important possible DAC pulses, namely, non-return-to-zero (*NRZ*), return-to-zero (*RZ*) and half-delay return-to-zero (*HRZ*). The impulse responses of all three pulses are shown in Figure 3-7.

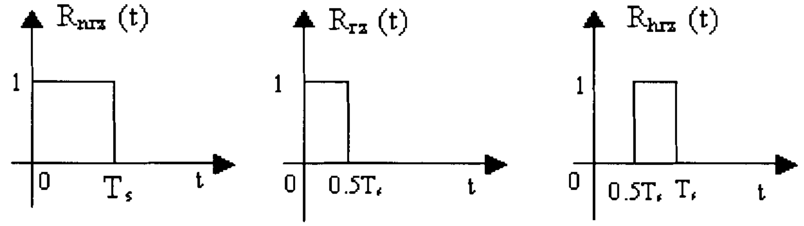


Figure 3-7 NRZ, RZ, HRZ DAC pulse types

The Laplace transforms and time domain equation for the three pulses are:

$$R_{nrz}(s)=\frac{1-e^{-sT_s}}{s}\;;\; r_{nrz}=\begin{cases}1,\ 0\leq t\leq T_s\\ 0, otherwise\end{cases}$$

$$R_{rz}(s)=\frac{1-e^{-sT_s/2}}{s}\ ;\ r_{rz}=\begin{cases}1,\ 0\le t\le \frac{T_s}{2}\\ 0, otherwise\end{cases}$$

$$R_{hrz}(s)=e^{\frac{-sT_s}{2}}\ \frac{1-e^{-sT_s/2}}{s};r_{hrz}=\begin{cases}1,\ \frac{T_s}{2}\le t\le T_s\\ 0, otherwise\end{cases}$$

Early designs of continuous-time ΣΔ modulators [48,53,54] assumed that if the ΣΔ loop filter poles are selected properly, one could expect to have the desired band stop noise shaping at a frequency band close to the loop filter pole frequencies. However, as illustrated in section 3.1, noise shaping does not guarantee system stability. In other words, the ΣΔ modulator dynamics are determined by the overall ΣΔ loop transfer function. To make the bandpass modulator stable, designers had to reduce the Q of the resonators [52], which reduced the effectiveness of the noise shaping.

To obtain the maximum SNR for a given modulator order, without sacrificing the noise shaping, the multi-feedback architecture was proposed in [16]. This method is based upon pulse shaping of the DAC output to realize a desired loop transfer function. However, none of the simple NRZ, RZ or HRZ DAC pulse shapes alone can implement the fourth order transfer function directly. Nevertheless, with any combination of two pulse shapes, for instance, RZ and HRZ, it is possible to build an ideal fourth order loop transfer function [52].

The fourth order bandpass ΣΔM is shown in Figure 3-8. Two identical resonators ($\omega s/(\omega^2 + s^2)$), and two different types of feedback DACs, HRZ and RZ are employed. Four tuneable parameters are used to generate the equivalent loop transfer function.

The open loop diagram of the multi-feedback CT BPΣΔM is shown in Figure 3-9. As was stated earlier, the path from the output of the quantizer to its input must be equivalent to the DTΣΔM transfer function shown in Figure 3-6a. Using superposition on the four feedback paths, we have:

$$\begin{aligned}Z[C_{2r}\,r_{rz}(t)*h_2(t)+C_{2h}\,r_{hrz}(t)*h_2(t)+C_{4r}\,r_{rz}(t)*h_4(t)\\ +C_{4h}\,r_{hrz}(t)*h_4(t)]\Big|_{t=nT_s}\qquad =-H_{bp}(z)\end{aligned} \tag{3.7}$$

where * denotes convolution. The inverse Laplace transforms of the resonator and the resonator cascade are:

$$h_2(t)=L^{-1}[H_2(s)]=L^{-1}(\frac{\omega s}{\omega^2+s^2})=\omega\cos\omega t \tag{3.8}$$

$$h_4(t)=L^{-1}[H_1(s)H_2(s)]=L^{-1}[(\frac{\omega s}{\omega^2+s^2})^2]=0.5\omega^2(t\cos\omega t+\frac{\sin\omega t}{\omega}) \tag{3.9}$$

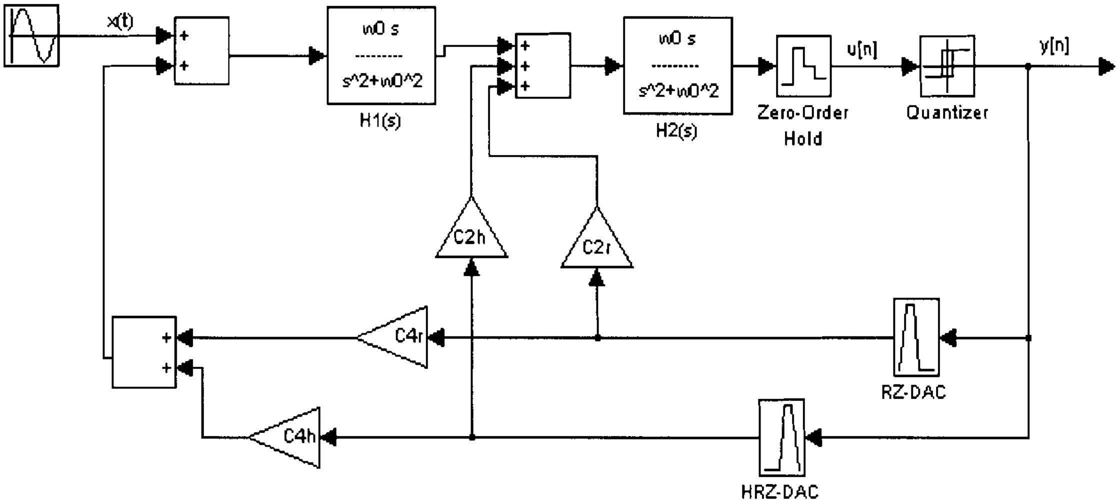


Figure 3-8 The 4th-order multi-feedback CT BPΣΔM

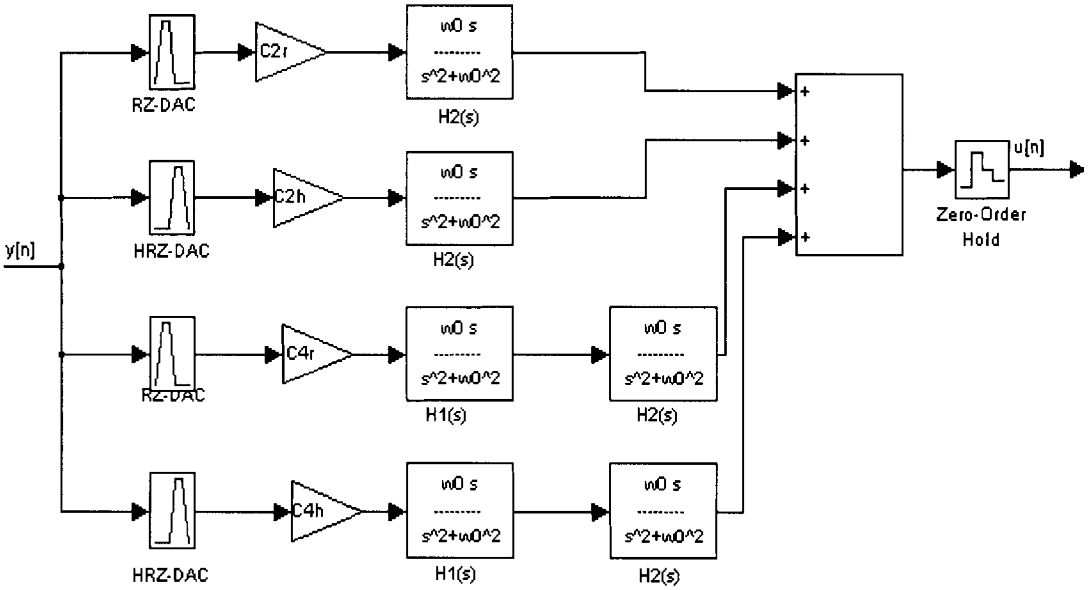


Figure 3-9 The open-loop diagram of the 4th-order multi-feedback CT BPΣΔM

3.4 The 4th-order, f_s/x CT BPΣΔM Architecture

The loop filter transfer function of the fourth order multi-band DT BPΣΔM derived in section 2.4 is reproduced here:

$$
\begin{aligned}
H_{bp}(z) &= \frac{(\cos\omega_c z^{-1} - z^{-2})\left(2 - 3\cos\omega_c z^{-1} + z^{-2}\right)}{(1 - 2\cos\omega_c z^{-1} + z^{-2})^2} \\
&= \frac{2\cos\omega_c z^3 - (2 + 3\cos^2\omega_c) z^2 + 4\cos\omega_c z - 1}{(1 - 2\cos\omega_c z + z^2)^2} \quad \Bigg|\, \omega_c = 2\pi\frac{f_c}{f_s}
\end{aligned}
\tag{3.10}
$$

As discussed in section 3.1, Equation (3.2) may be used to obtain the loop filter transfer function by directly implementing the NTF. To implement a continuous-time domain transfer function that is equal to discrete-time domain transfer function in Equation (3.7), MATLAB's *c2d* function can be used to transfer a continuous-time function convolved with a NRZ DAC pulse to an equivalent discrete-time function [14]. This is done as follows:

$$
c2d[\mathit{state-space}\ \mathrm{mod}\mathit{el\ of}\ h_2(t)] = Z[r_{hrz}(t) * h_2(t)] \tag{3.11}
$$

where Z is the z-transform. We can use state-space matrices and vectors [14] for general rectangular DAC pulses whose width of the magnitude 1 is over an interval [α β]. For different DAC pulses, only the *B* state-space matrix changes [9]. Thus, the discrete-time *B* matrix for non-NRZ DAC pulses is [14]:

$$
B_{(\alpha,\beta)} = A_{NRZ}^{-1} \cdot \left(e^{A_{NRZ}(1-\alpha)} - e^{A_{NRZ}(1-\beta)}\right) \cdot B_{NRZ} \tag{3.12}
$$

Using *c2d* and Equation (3.12), the equivalent discrete time functions for the four paths of Figure 3-9 are:

$$
H_{2r}(z) = Z[C_{2r} \cdot r_{rz}(t) * h_2(t)] = C_{2r} \frac{h1_{2r} z + h0_{2r}}{z^2 - 2\cos\omega_c z + 1} \tag{3.13}
$$

$$
H_{2h}(z) = Z[C_{2h} \cdot r_{hrz}(t) * h_2(t)] = C_{2h} \frac{h1_{2h} z + h0_{2h}}{z^2 - 2\cos\omega_c z + 1} \tag{3.14}
$$

$$
H_{4r}(z) = Z[C_{4r} \cdot r_{rz}(t) * h_4(t)] = C_{4r} \frac{h3_{4r} z^3 + h2_{4r} z^2 + h1_{4r} z + h0_{4r}}{(z^2 - 2\cos\omega_c z + 1)^2} \tag{3.15}
$$

$$H_{4h}(z)=Z[C_{4h}\cdot r_{hrz}(t)*h_4(t)]=C_{4h}\frac{h3_{4h}z^3+h2_{4h}z^2+h1_{4h}z+h0_{4h}}{(z^2-2\cos\omega_c z+1)^2} \tag{3.16}$$

In Equations (3.13) through (3.16), $h1_{2r}$, $h0_{2r}$, $h1_{2h}$, $h0_{2h}$, $h3_{4r}$, $h2_{4r}$ ... $h0_{4h}$ are coefficients for which numerical results can be obtained by running the MATLAB code listed in Appendix A. Applying Equations (3.10) and (3.13) to (3.16) to Equation (3.7) yields:

$$H_{2r}(z)+H_{2h}(z)+H_{4r}(z)+H_{4h}(z)=-\frac{2\cos\omega_c z^3-(2+3\cos^2\omega_c)z^2+4\cos\omega_c z-1}{(1-2\cos\omega_c z+z^2)^2} \tag{3.17}$$

Equivalently, Equation (3.17) can be written as:

$$\begin{aligned}&(H_{2r}(z)+H_{2h}(z))\frac{1-2\cos\omega_c z+z^2}{1-2\cos\omega_c z+z^2}+H_{4r}(z)+H_{4h}(z)\\&=-\frac{2\cos\omega_c z^3-(2+3\cos^2\omega_c)z^2+4\cos\omega_c z-1}{(1-2\cos\omega_c z+z^2)^2}\end{aligned} \tag{3.18}$$

The coefficients C_{2r}, C_{2h}, C_{4r}, C_{4h} can be solved by using Equation (3.13) through (3.16) and Equation (3.18).

3.4.1 The 4th-order, f_s/4 CT BPΣΔM

First, let us examine the $f_s/4$, 4th-order CT BP ΣΔM. Instead of feeding the output of the quantizer directly into RZ and HRZ DACs, a unit delay can be inserted after the quantizer without a penalty in performance {14, 16]. This structure having the added unit delay is shown in Figure 3-10. Although this structure requires an additional flip-flop, the modulator is less sensitive to extra nonideal loop delays, such as propagation delay time introduced by the comparator and DACs [52].

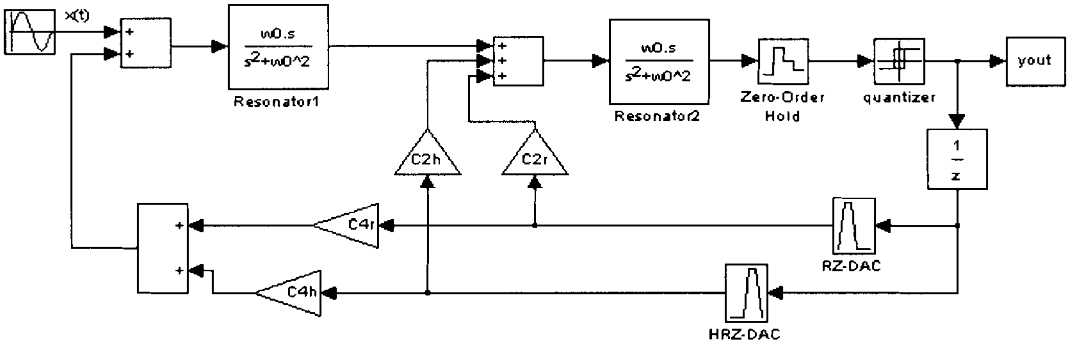


Figure 3-10 The 4th-order f_s /4 CT BPΣΔM with a unit delay,

The related discrete-time loop filter, $H_{bp}'(z)$, must be altered to reflect the introduction of the unit delay:

$$H_{bp}'(z)=\frac{-2z^3-z}{\left(z^2+1\right)^2} \tag{3.19}$$

For the CT BPΣΔM shown in Figure 3-10, Equations (3.13) to (3.16) become:

$$H_{2r}(z)=Z[C_{2r}\cdot r_{rz}(t)*h_2(t)]=C_{2r}\frac{0.2929z-0.7071}{z^2+1} \tag{3.20}$$

$$H_{2h}(z)=Z[C_{2h}\cdot r_{hrz}(t)*h_2(t)]=C_{2h}\frac{0.7071z-0.2929}{z^2+1} \tag{3.21}$$

$$H_{4r}(z)=Z[C_{4r}\cdot r_{rz}(t)*h_4(t)]=C_{4r}\frac{0.5077z^3-0.833z^2+0.0476z+0.2777}{(z^2+1)^2} \tag{3.22}$$

$$H_{4h}(z)=Z[C_{4h}\cdot r_{hrz}(t)*h_4(t)]=C_{4h}\frac{0.2777z^3+0.04764z^2-0.833z+0.5077}{(z^2+1)^2} \tag{3.23}$$

Applying Equations (3.19) and (3.20) through (3.23) to Equation (3.7) and simplifying yields:

$$(H_{2r}(z)+H_{2h}(z))\frac{z^2+1}{z^2+1}+H_{4r}(z)+H_{4h}(z)=\frac{2z^3+z}{\left(z^2+1\right)^2} \tag{3.24}$$

Using the MATLAB program set out in Appendix A, the feedback coefficients, C_{2r}, C_{2h}, C_{4r}, C_{4h} are found to be:

$\{C_{2r}, C_{2h}, C_{4r}, C_{4h}\} = \{-0.633883, 2.987437, -0.450158, 1.0867779\}$

Alternatively, instead of using LP to BP transformation to determine $H_{bp}'(z)$, the MATLAB function synthesizeNTF and the noise shaping described in section 3.1 can be utilized to determine $H_{bp}'(z)$. For a ΣΔM having an order of 4, a carrier frequency that is one quarter the modulator's sampling frequency and an out of band gain of 1.8, plus an additional delay of one sample following the quantizer, synthesizeNTF results in:

$$NTF(z)=\frac{z^4+2z^2+1}{z^4+0.922476z^2+0.299746} \tag{3.25}$$

$$H_{bp}(z)=\frac{1.0775239z^2+0.700254z}{z^4+2z^2+1} \tag{3.26}$$

Substituting Equation (3.26) and Equation (3.20) to Equation (3.23) in Equation (3.7), and using the MATLAB program listed in Appendix A, the feedback coefficients for the alternative design are:

$\{C_{2r}, C_{2h}, C_{4r}, C_{4h}\} = [-0.4675, 1.6784, -0.1698, 0.4100\}$

Figure 3-11(a) and (c) show the magnitude response of the NTF Equation (2.38) and the STF of the $f_s/4$ CT BPΣΔM based upon the lowpass to bandpass transformation ("transformed CT BPΣΔM"). From Figure 3-11(c), it is evident that the maximum out-of-band gain of the transformed CT BPΣΔM is around 4. The magnitude response of the NTF and STF of the $f_s/4$ CT BPΣΔM derived directly from the optimized NTF Equation (3.25) ("optimized CT BPΣΔM") are shown in Figure 3-11 (b) and (d). The notch in the NTF of the optimised CT BPΣΔM is deeper than that of the transformed CT BPΣΔM because its poles have moved away from the origin (see Figure 3-12). Similarly, the SNDR of the optimized CT BPΣΔM $|NTF|_{max}=1.8$ is higher than that of the transformed

CT BPΣΔM, however, the maximum stable input amplitude of the optimised CT BPΣΔM is degraded, consistent with our discussion in section 3.1. In Figure 3-13, the dynamic range of the transformed CT BPΣΔM and optimised CT BPΣΔM, both with an OSR of 210, is observed to be very close to the theoretical result. The theoretical result is for the linear model of the $f_s/4$, fourth order DT BPΣΔM given in Equation (2.43). The output spectrum of the transformed CT BPΣΔM having a two tone input signal at -13dB is shown in Figure 3-15. Note that there are strong tones near DC and $f_s/2$, which is similar to the DT BPΣΔM that was discussed in section 2.3.

The inclusion of a unit delay between the quantizer and DACs, as shown in Figure 3-10, is particular to f_s /4 bandpass modulators because of the causality principle. Later, a structure different from that in Figure 3-10 where the numerator of the loop filter has a non-zero z^{-1} term will be presented. If we factor out the z^{-1} term, the loop filter would be non-causal.

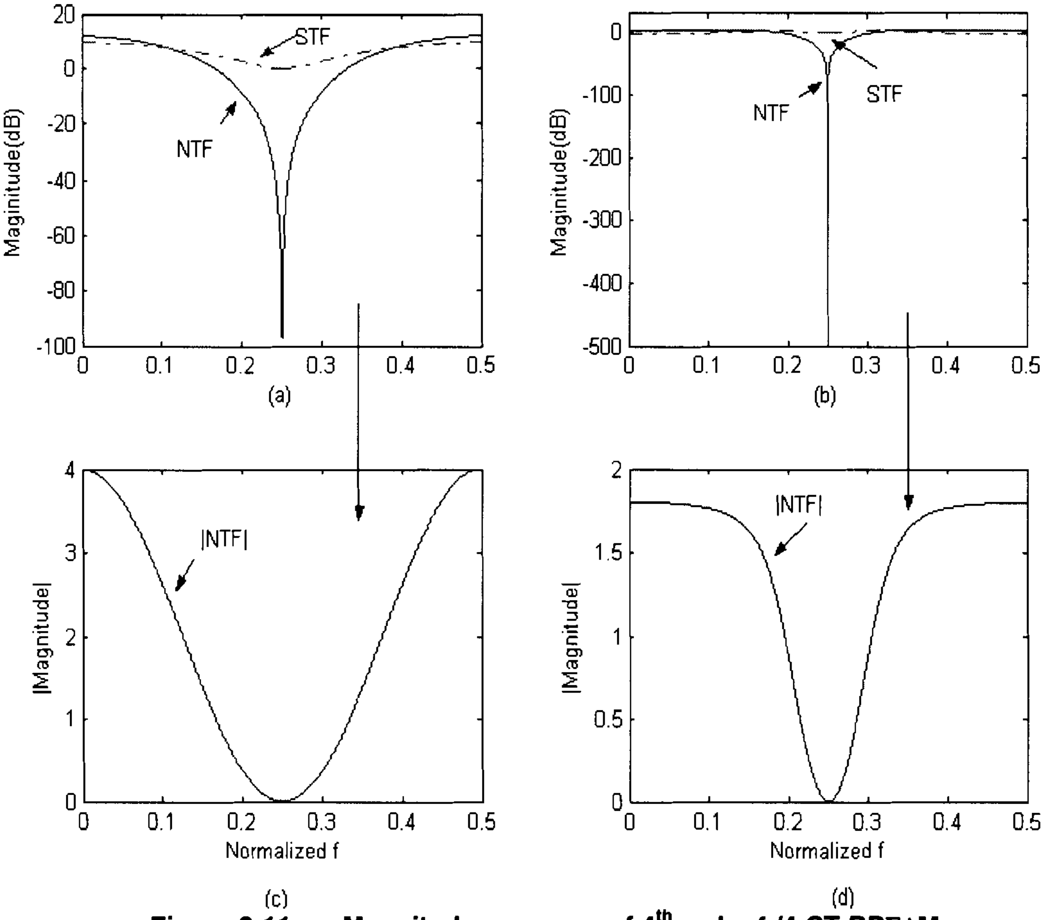


Figure 3-11 **Magnitude response of 4^{th}-order $f_s/4$ CT BPΣΔMs**
(a) STF and NTF for $|NTF(f)|_{max}=4$,
(b) STF and NTF for $|NTF(f)|_{max}=1.8$,
(c) |NTF| for $|NTF(f)|_{max}=4$,
(d) |NTF| for $|NTF(f)|_{max}=1.8$

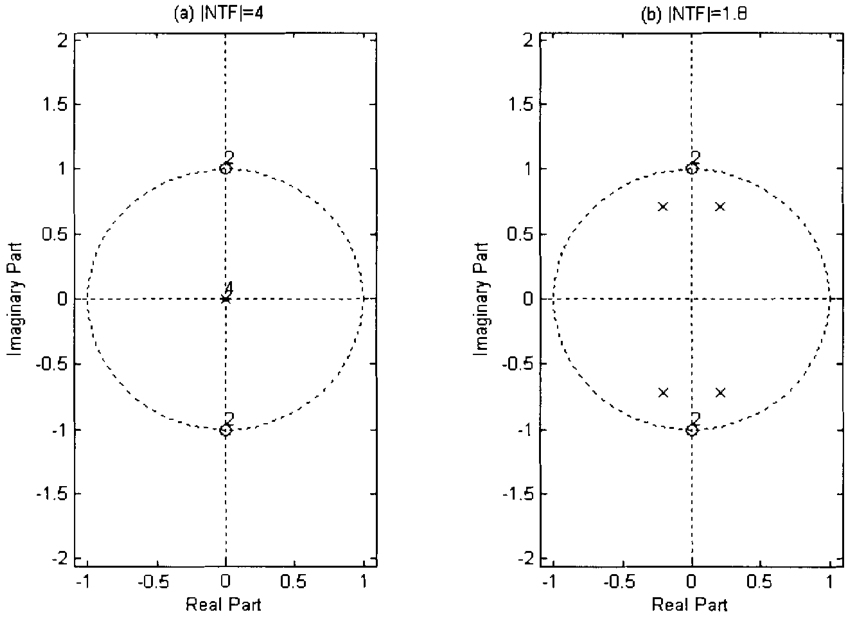


Figure 3-12 Poles and zeros constellation of the NTF of the 4th-order, $f_s/4$ BPΣΔM

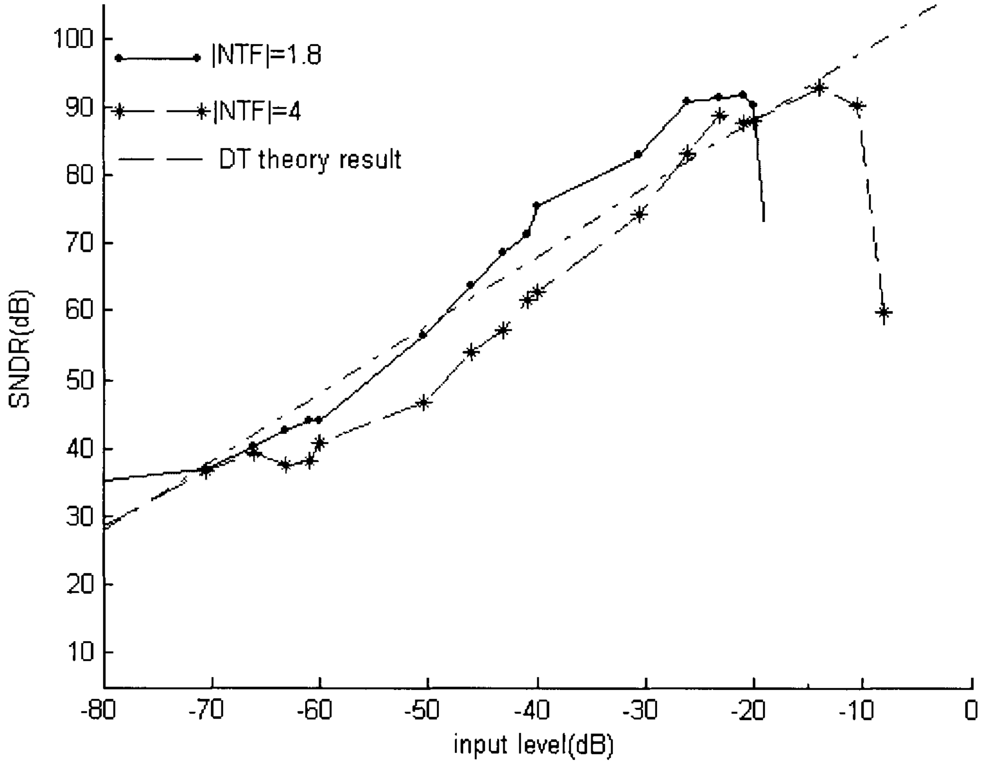


Figure 3-13 The dynamic range of the 4th-order, $f_s/4$ CT BPΣΔM

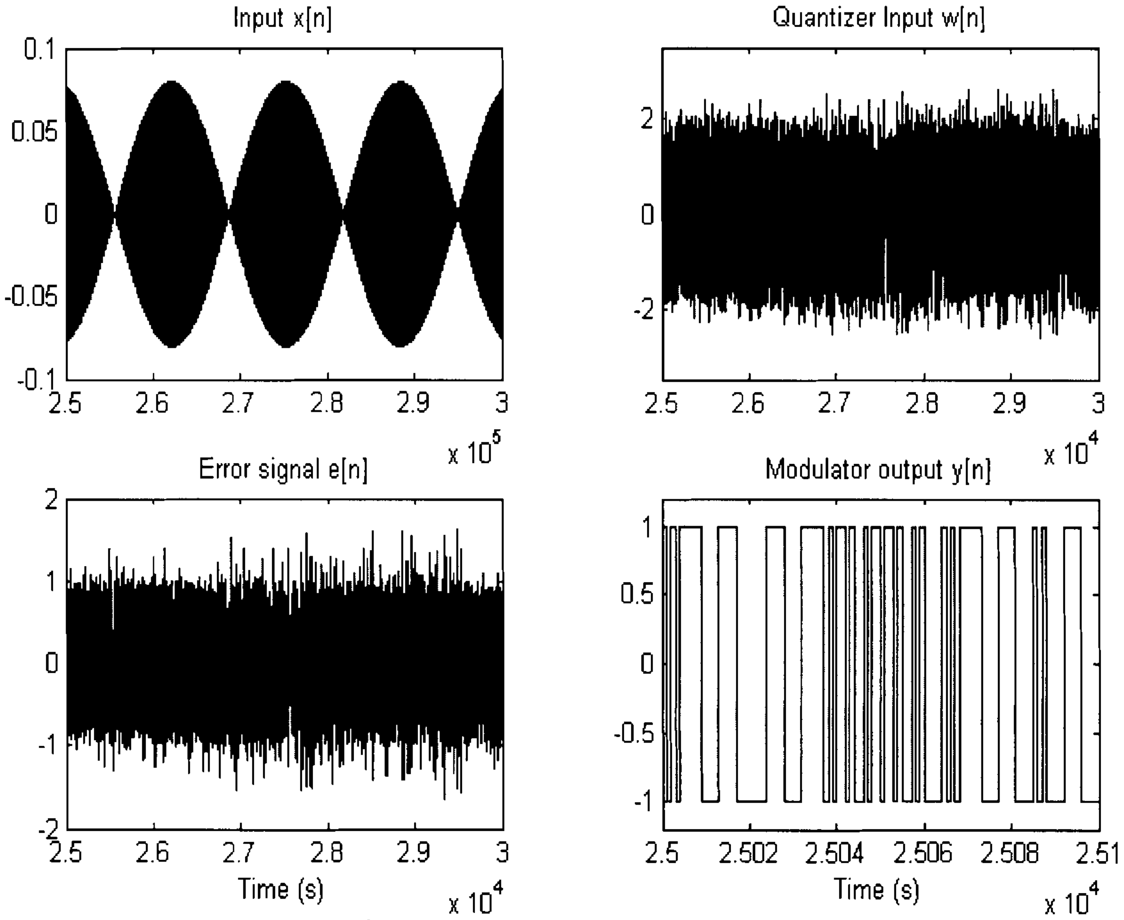
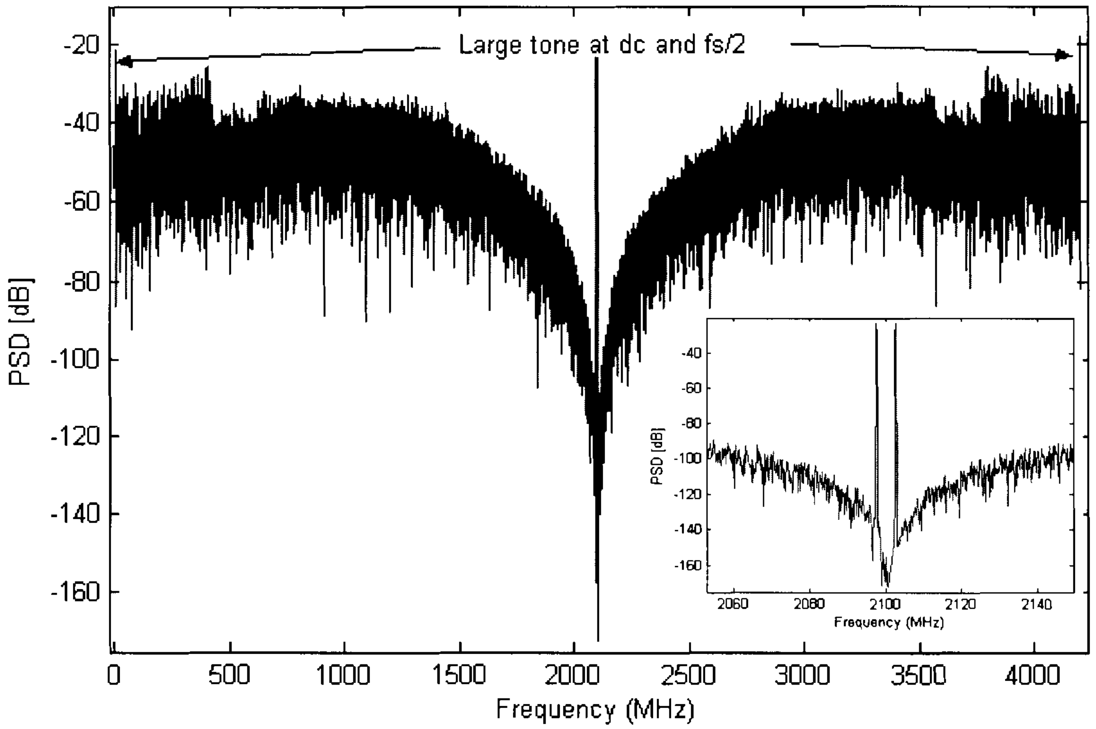


Figure 3-14 The 4th-order, $f_s/4$ CT BPΣΔM responding to two tones input



(b) Around DC

(c) Around fs/2

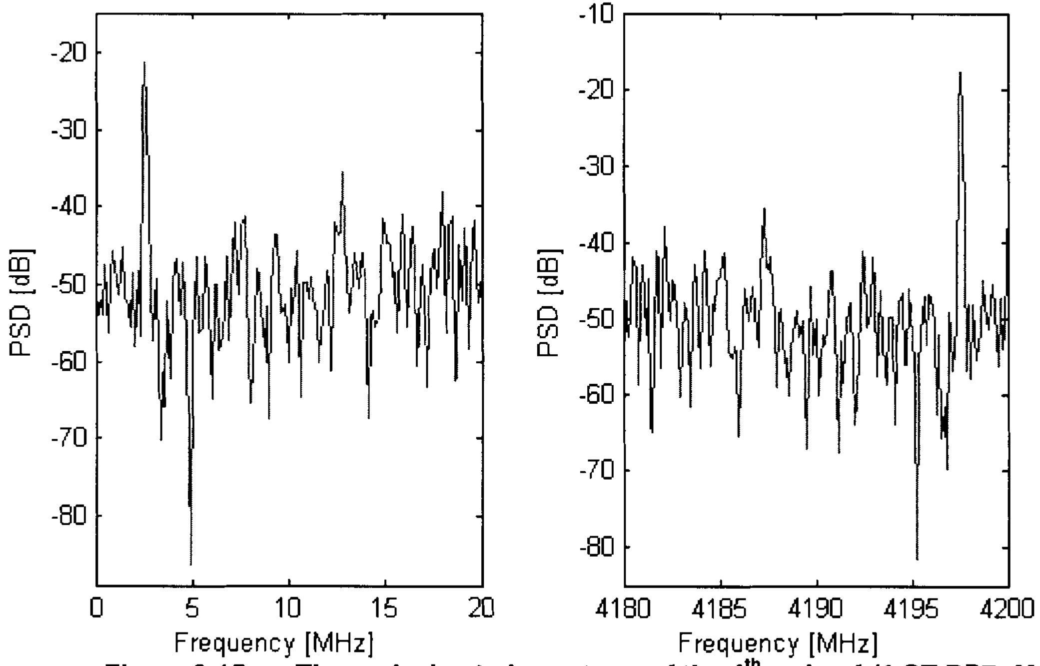


Figure 3-15 The undecimated spectrum of the 4th-order, $f_s/4$ CT BPΣΔM

3.4.2 The 4th-order, f_s /10 CT BPΣΔM

In the case of the f_s /10 CT BPΣΔM architecture, the same steps used in section 3.4.1 to obtain the CT domain system function can be employed. First, the **c2d** function is utilized to derive the discrete-time loop transfer function.

$$H_{2r}(z)=Z[C_{2r}\cdot r_{rz}(t)*h_2(t)]=C_{2r}\frac{0.2788\,z-0.309}{z^2-1.618\,z+1} \tag{3.27}$$

$$H_{2h}(z)=Z[C_{2h}\cdot r_{hrz}(t)*h_2(t)]=C_{2h}\frac{0.309\,z-0.2788}{z^2-1.618z+1} \tag{3.28}$$

$$H_{4r}(z)=Z[C_{4r}\cdot r_{rz}(t)*h_4(t)]=C_{4r}\frac{0.1361\,z^3-0.2242\,z^2+0.0395\,z+0.04854}{(z^2-1.618z+1)^2} \tag{3.29}$$

$$H_{4h}(z)=Z[C_{4h}\cdot r_{hrz}(t)*h_4(t)]=C_{4h}\frac{0.04854\,z^3+0.0395\,z^2-0.2242\,z+0.1361}{(z^2-1.618z+1)^2} \tag{3.30}$$

Second, the loop filter is found using the lowpass to bandpass transformation:

$$\begin{aligned}H_{bp}(z)&=\frac{2\cos\frac{\pi}{5}z^3-(2+3\cos^2\frac{\pi}{5})z^2+4\cos\frac{\pi}{5}z-1}{(1-2\cos\frac{\pi}{5}z+z^2)^2}\\&=\frac{1.618z^3-3.9635z^2+3.2361z-1}{(1-1.618z+z^2)^2}\end{aligned} \tag{3.31}$$

Hence, for the f_s /10 fourth-order CT ΣΔM, Equation (3.18) can be written as:

$$(H_{2r}(z)+H_{2h}(z))\frac{z^2-1.618z+1}{z^2-1.618z+1}+H_{4r}(z)+H_{4h}(z)=-H_{bp}(z) \tag{3.32}$$

Third, using the MATLAB program, the four feedback coefficients are obtained:

$\{C_{2r}, C_{2h}, C_{4r}, C_{4h}\} = \{-6.2137, 3.2569, -7.4735, 2.5752\}$.

As in section 3.4.1, the feedback coefficients can also be derived using the optimization algorithm given in Equation (3.2). For a 4th-order BPΣΔM having an out-of-band gain of 1.8 and a carrier frequency of f_s/10 (f_0 =0.1) we obtain:

$$NTF(z)=\frac{(z^2-1.618z+1)^2}{z^4-2.2666z^3+2.3995z^2-1.2977z+0.3085} \tag{3.33}$$

$$H_{bp}(z)=\frac{-0.9695z^3+2.2185z^2-1.9384z+0.6914}{(z^2-1.618z+1)^2} \tag{3.34}$$

The four feedback coefficients are found to be:

$\{C_{2r}, C_{2h}, C_{4r}, C_{4h}\} = \{-1.9189, -1.7359, 2.0147, -3.5502\}$

The dynamic range of the $f_s/10$ transformed CT BPΣΔM and the optimized CT BPΣΔM are illustrated in Figure 3-16. From Figure 3-16, it is evident that higher out-of-band gain lowers the SNDR, however, increases the dynamic range. By tuning the four feedback coefficients, the SNDR of the CT BPΣΔM is nearly identical to that of the equivalent DT BPΣΔM.

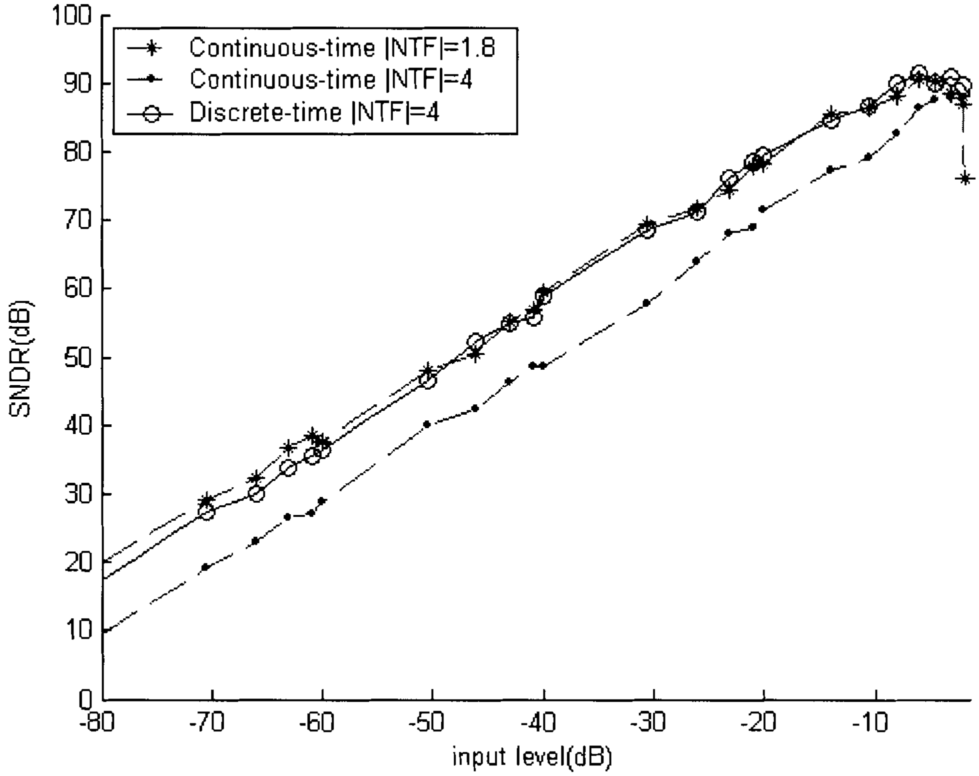


Figure 3-16 The dynamic range of the 4th-order, $f_s/10$ CT BPΣΔM

Figures 3-17(a) to (d) show the magnitude response of the NTF and the STF of the $f_s/10$ transformed CT BPΣΔM and the optimized CT BPΣΔM. As with the $f_s/4$ CT BPΣΔM, the noise shaping response of the $f_s/10$ optimized CT BPΣΔM is superior to that of the transformed CT BPΣΔM. Furthermore, the optimised CT BPΣΔM has a higher

SNDR than the transformed CT BPΣΔM, but suffer from a degraded maximum stable input amplitude. Figure 3-19 shows the occurrence of the 1st and 2nd resonator output voltage with a power of 13dB. Under the stable status, the 2nd resonator output voltage, i.e. the quantizer input is limited in a small range. When the system is going to be unstable, the quantizer input will be unbounded. We will discuss the stability in the next section. Figure 3-20 shows the output spectrum of the 4th-order $f_s/10$ CT BPΣΔM. There is no tone near DC and $f_s/2$.

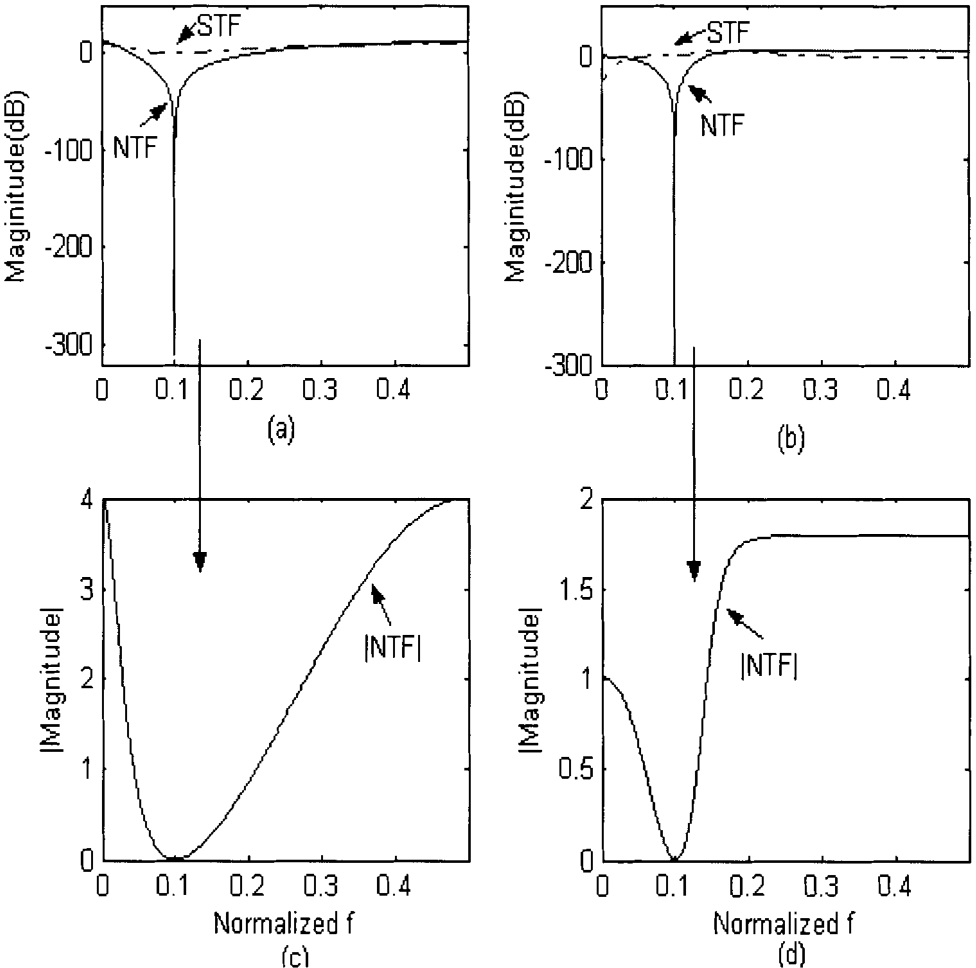


Figure 3-17 **Magnitude responses of the 4th-order, $f_s/10$ CT BPΣΔM**
(a) STF and NTF for $|NTF(f)|_{max}=4$,
(b) STF and NTF for $|NTF(f)|_{max}=1.8$,
(c) |NTF| for $|NTF(f)|_{max}=4$,
(d) |NTF| for $|NTF(f)|_{max}=1.8$

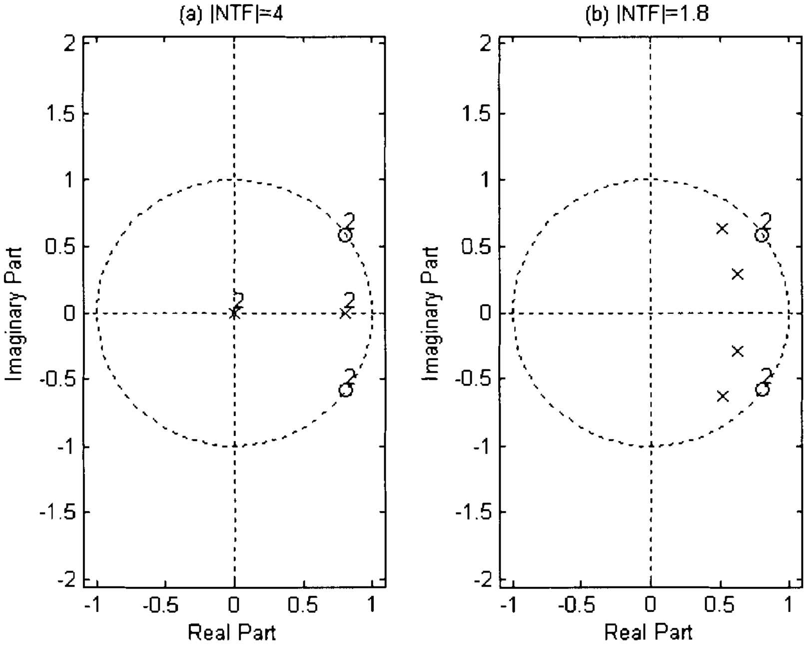


Figure 3-18 **Poles and zeros constellation of the NTF of the 4th-order, f_s/10 BPΣΔM**

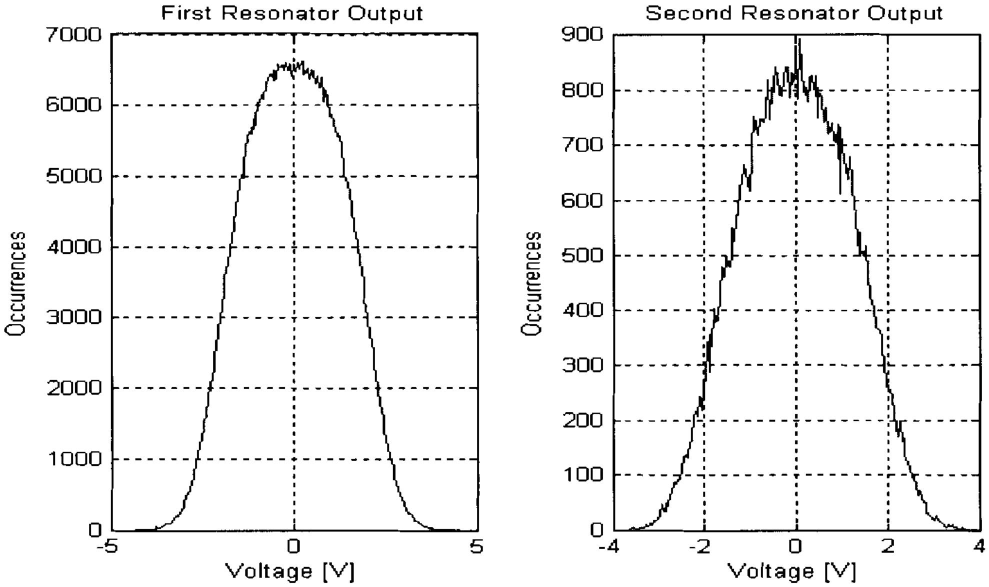


Figure 3-19 **The 1st and 2nd resonator output of the 4th order, f_s/10 CT BPΣΔM**

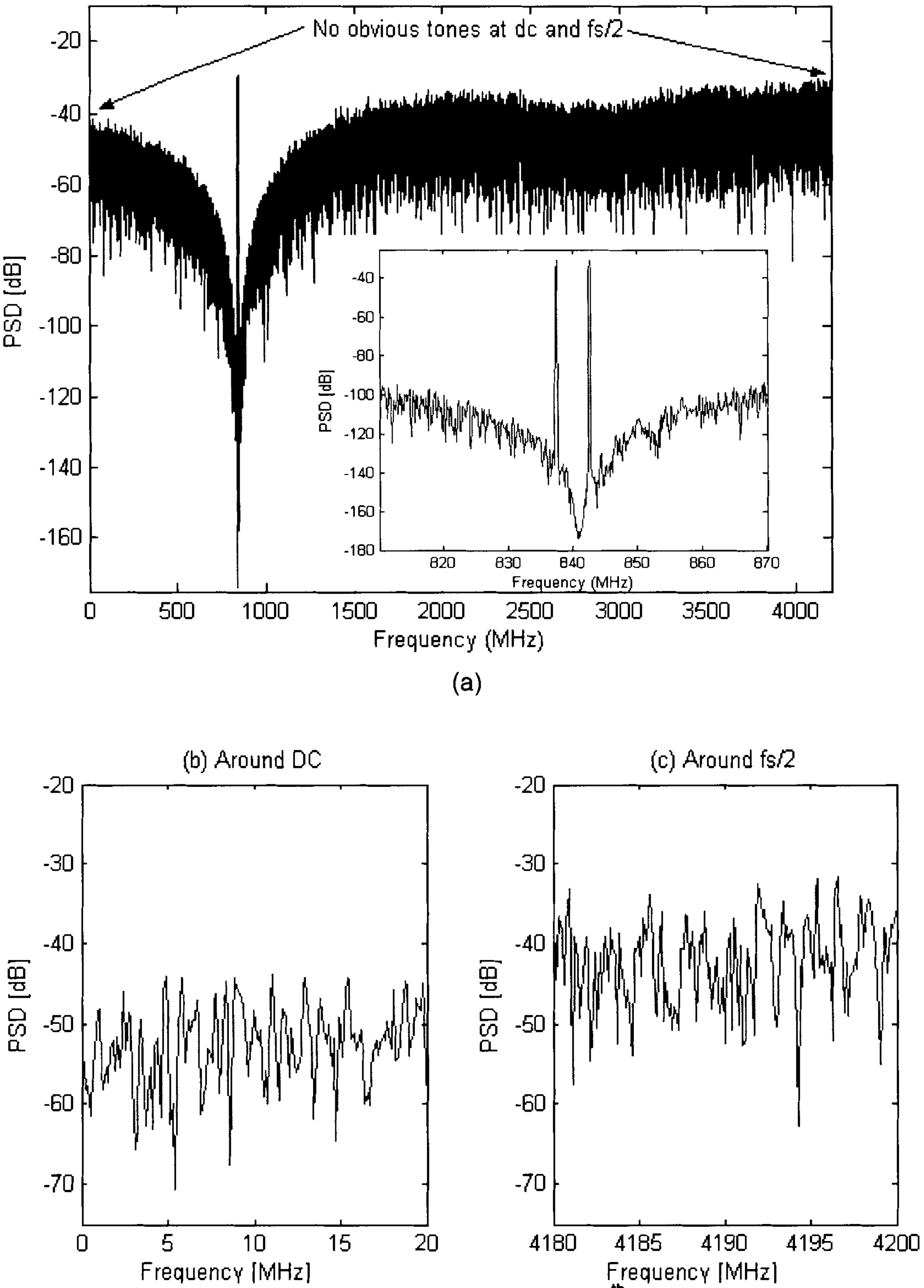
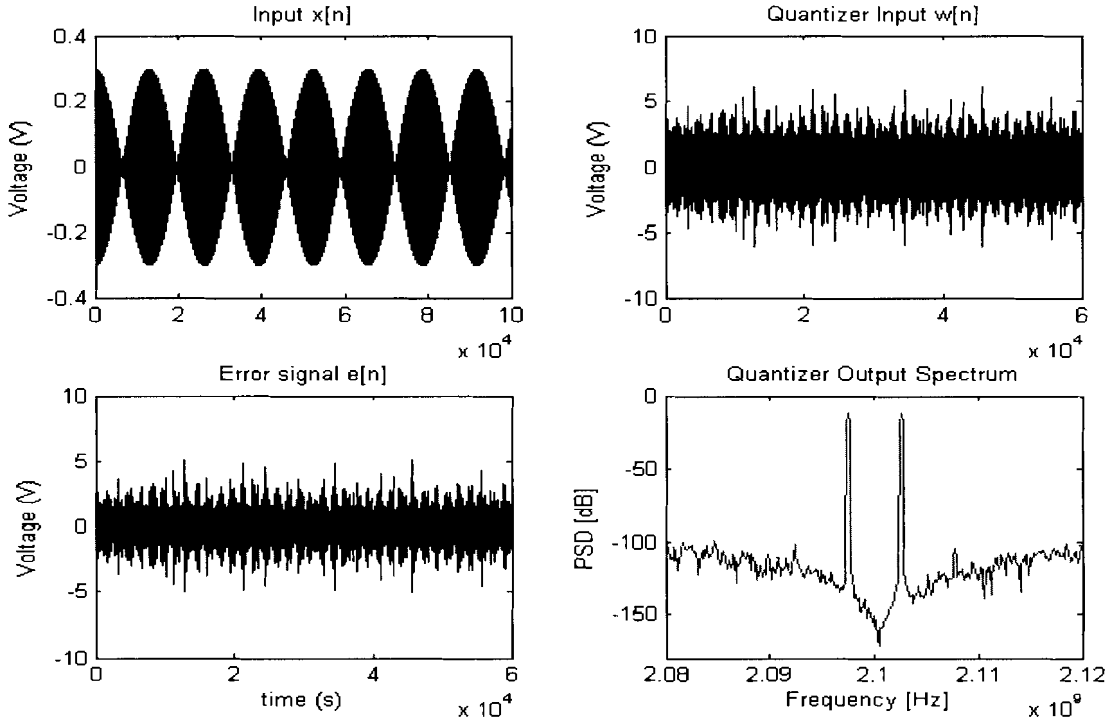


Figure 3-20 **The undecimated spectrum of the 4th-order, f_s/10 CT BPΣΔM**

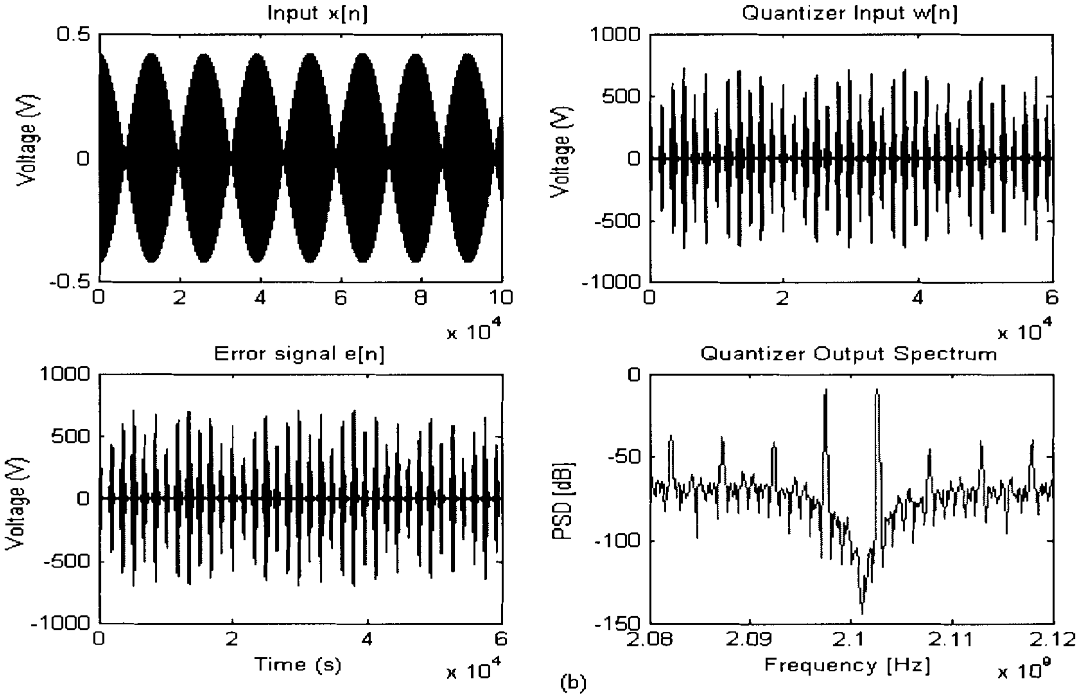
3.5 Stability

As was discussed in Section 3.1, when the amplitude of the input signal to a ΣΔM is increased, a threshold level will be reached after which the SNR will dramatically drop off. The reasons for this are as follows: the quantizer input signal grows out of bounds and oscillates with large amplitude, the quantizer is overloaded and the quantizer error is unbounded. Moreover, the system is unstable and the output signal no longer resembles the input signal. At this point, the quantizer stops behaving like a linear additive noise source and the independence assumption described in section 2.1.1 is no longer valid. Instead, the quantizer input signal is highly correlated with the input signal to the modulation. Figure 3-21 shows how the system becomes unstable when the input signal amplitude is increased.

Simulation shows that even though the modulator may become unstable in a linear sense, it can remain stable due to the nonlinear feedback. The output of the loop filter has exponentially diverging trajectories that are kept within certain bounds by the nonlinear feedback [96]. Large input signals eventually overwhelm the linearity of the input stage, and any nonlinearity in the input stage appears directly in the modulator output spectrum [11]. The nonlinear model of the quantizer must be used to analyse the stability of the ΣΔM instead of the linear model.


Input x[n]
Voltage (V)
0.4
0.2
0
-0.2
-0.4
0 2 4 6 8 10
x 10^4
Quantizer Input w[n]
Voltage (V)
10
5
0
-5
-10
0 2 4 6
x 10^4
Error signal e[n]
Voltage (V)
10
5
0
-5
-10
0 2 4 6
time (s)
x 10^4
Quantizer Output Spectrum
PSD [dB]
0
-50
-100
-150
2.08 2.09 2.1 2.11 2.12
Frequency [Hz]
x 10^9

(a)


Input x[n]
Voltage (V)
0.5
0
-0.5
0 2 4 6 8 10
x 10^4
Quantizer Input w[n]
Voltage (V)
1000
500
0
-500
-1000
0 2 4 6
x 10^4
Error signal e[n]
Voltage (V)
1000
500
0
-500
-1000
0 2 4 6
Time (s)
x 10^4
Quantizer Output Spectrum
PSD [dB]
0
-50
-100
-150
2.08 2.09 2.1 2.11 2.12
Frequency [Hz]
x 10^9

(b)

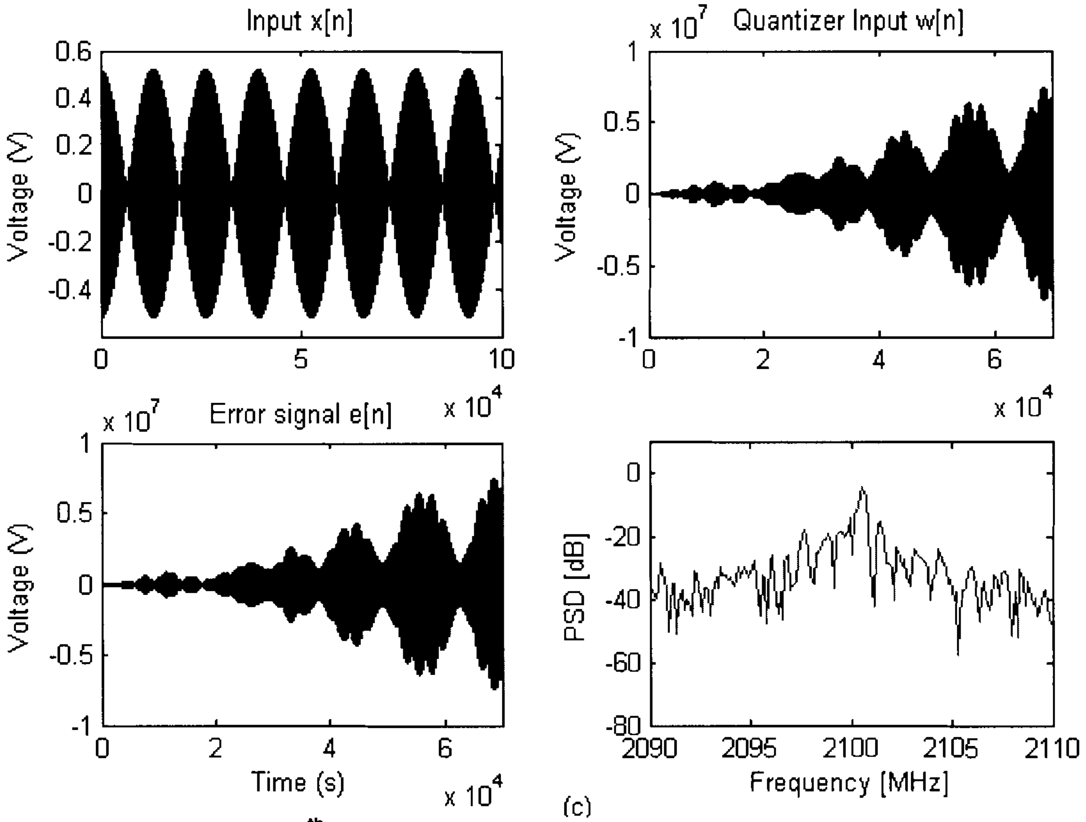


Figure 3-21 The 4^{th}-order, $f_s/4$ CT BPΣΔM responding to two tone inputs with the maximum input amplitude is a) 300mV, b) 420mV, c) 520mV

In order to accommodate the inaccuracy of the linear model, many sophisticated models of the quantizer have been developed [97, 98, 99, 100]. Typically, the quantizer is modelled as a time variable gain element, k, whose gain depends on the input to the modulator. The gain, k, is defined as the ratio of the quantizer' s output and input voltages. For a single-bit quantizer, k can have any value larger than zero. For multi-bit quantizers, the value of k will be near unity. A block diagram is depicted in Figure 3-22.

For the structure shown in Figure 3-22, the NTF and the STF are:

$$NTF(k,z)=\frac{1}{1+k\,H(z)} \tag{3.35}$$

$$STF(k,z)=\frac{k\,H(z)}{1+k\,H(z)} \tag{3.36}$$

Since k is a function of the input signal, the NTF depends on the input signal. The poles of the STF determine the stability of the system.

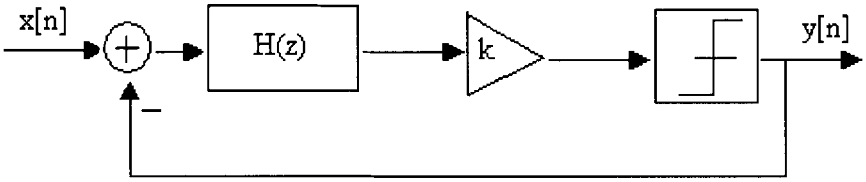


Figure 3-22 The diagram of the stability model of the ΣΔ modulator

By applying root locus or Nyquist plot [7] techniques, a linear stable operating range for the quantizer input can be obtained. A low input amplitude corresponds to a high quantizer gain and the poles of STF (z) are inside or on the unit circle. But increasing the input amplitude would reduce the quantizer's gain. When the gain k is smaller than a certain value k_0, the poles of STF (z) go outside the unit circle and the modulator becomes unstable.

Using the root locus search method to find a certain minimum value k_0, we can predict the maximum quantizer input amplitude [96]. In order to guarantee the stability of the ΣΔM, Van Engelen *et. al.* [96] suggests placing a limiter between the loop filter output and the quantizer input or monitoring the amplitude of the signal at the quantizer input to control the input signal or reset the loop filter states when it appears to be unstable. However, placing a limiter would introduce harmonic and periodic resets and the continuous overload of the modulator must be avoided under normal operating conditions. Furthermore, the accurate boundary prediction for stability is not currently available for the BPΣΔM.

Several authors have proposed stability criteria for ΣΔMs. Lee's rule of thumb [7] is to limit the gain of the NTF to be less than 2. Agrawal and Shenoi [68] argue that the total power gain of the NTF must not exceed a factor of 3 to validate the white noise assumption. An overview of these methods are summarized in [101] and they show that both Lee's Rule and the Power Gain Rule are overly conservative and neither necessary nor sufficient to guarantee stability. To ensure a robust stability providing the desired performance, simulations are the most reliable method.

3.6 Summary

By using a multi-feedback CT BPΣΔM with the appropriate DAC pulses, the loop filter can match that of the discrete time ΣΔM, and hence the behaviour of both DT and CT ΣΔM are identical. The four tuneable coefficients make it easy to design the desired architecture.

Multi-band f_s/x continuous-time sigma-delta modulation is investigated. With the correct choice of NTF, including poles, zeros and the maximum out-of-band gain, we may obtain the desired performance. If this level of performance were unsatisfactory, we may consider using the higher order ΣΔM, the multi-bit quantizer or the higher over-sampling ratio.

Maintaining the same structure and sample frequency, tuning the four coefficients C_{2r}, C_{2h}, C_{4r}, C_{4h} and changing the resonating frequency of the resonators, the system can be tuned to different centre frequencies. The NTF derived from the lowpass to bandpass transformation and directly from the noise shaping with the out-of-band gain is simulated individually. The behavioural simulation shows that in changing the out-of-band gain of the NTF, we can change the signal-to-noise ratio. The penalty for this is the dynamic range. Figure 3-23 shows that increasing the out-of-band gain of the NTF causes the poles to move to the origin, which leads to the shallower notch and immediately poor noise shaping [4].

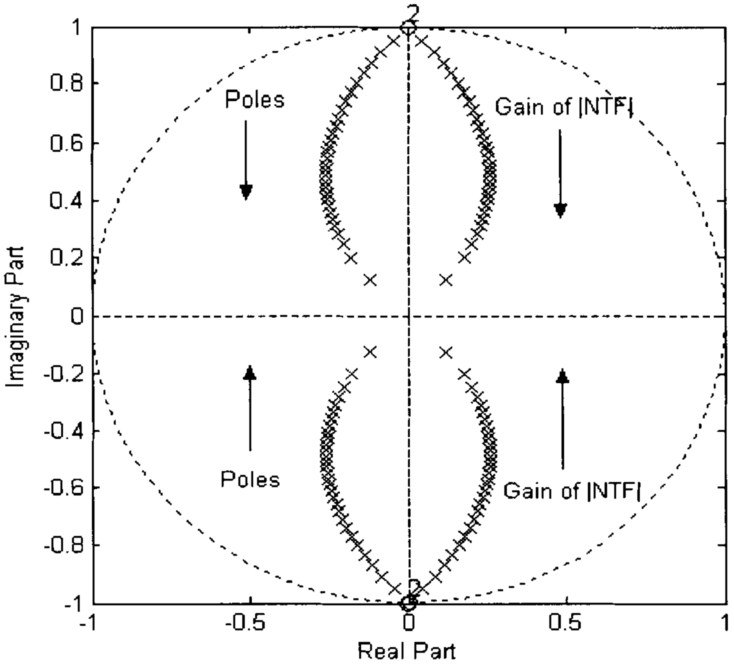
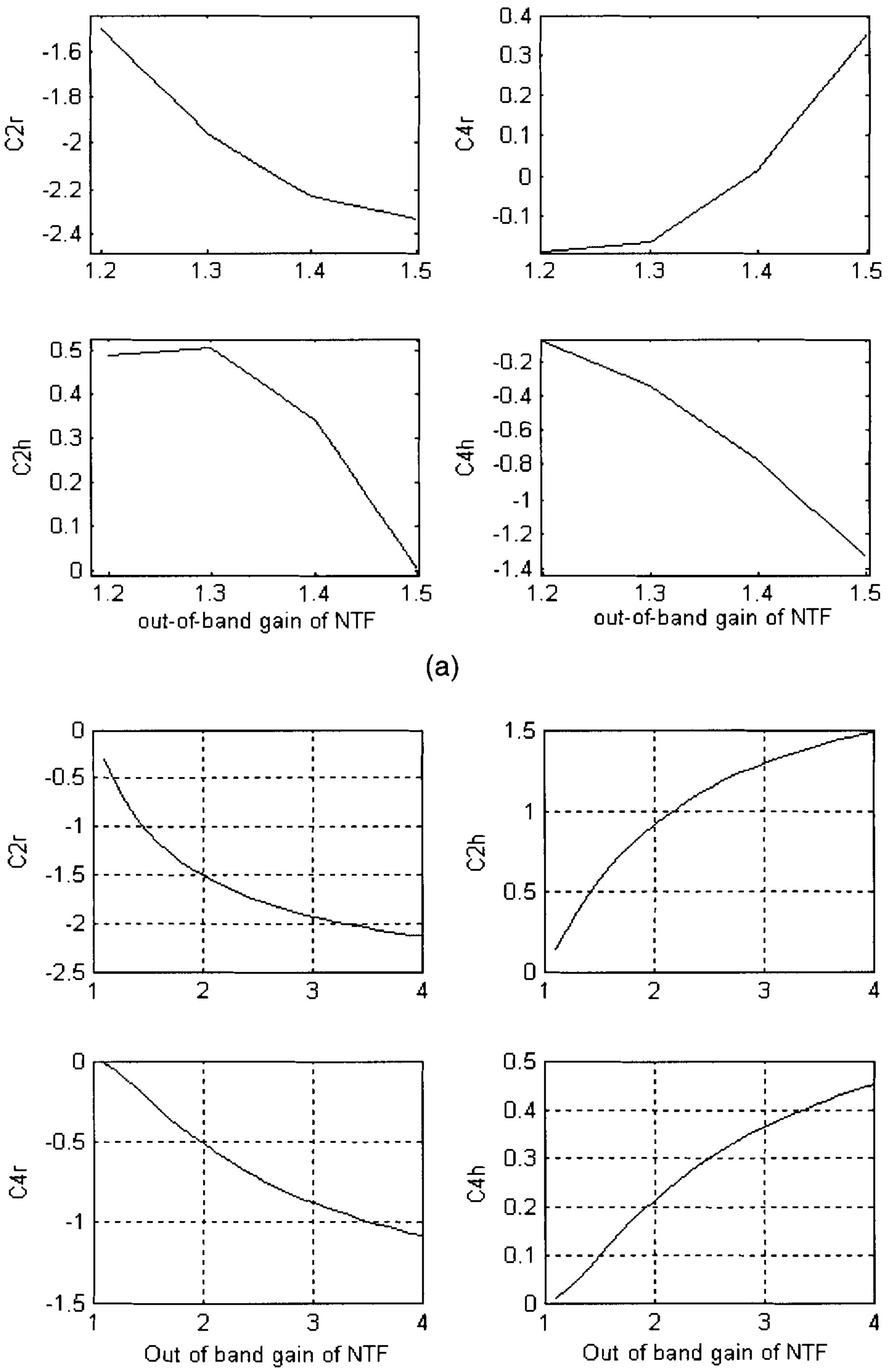


Figure 3-23 **Poles of NTF of $f_s/4$ vs. the gain of NTF**

The simulation in Figure 3-24, illustrates that the fourth order CT BP system is not sensitive to the exact values of the four coefficients, which suggests the possibility that the design may be suitable for VLSI implementation.

In the next chapter, the nonideal behaviour model will be gradually added to the system to observe the impairment to performance.



(a)

(b)

Figure 3-24 Four coefficients vs. the out-of-band gain of the NTF for the 4th-order (a) $f_s/10$ CT BPΣΔM, (b) $f_s/4$ CT BPΣΔM

Chapter 4

Nonideal Characteristics in CT BPΣΔMs

The system level design of an ideal fourth-order BP ΣΔM has been discussed in the previous chapters. In practical designs, there are a number of nonideal characteristics that adversely affect the performance of ΣΔMs. These non-ideal characteristics are similar in CT ΣΔMs and DT ΣΔMs. In CT designs, the characteristics of the quantizer and feedback DAC pulses are of particular concern, being especially sensitive at high clock rates.

Nonideal models are usually derived in two ways. One method is to derive the analytical expressions for each nonideal characteristic. However, this is not always straightforward because of nonlinear transfer characteristics and op-amp noise. As a consequence, certain assumptions must be made or constraints defined in order to validate the nonideal models. The second approach is to use a transfer function to define the nonideality (e.g. finite gain in the z-domain) and fully simulate the behaviour at a high level.

An overview of the CT ΣΔM nonideal characteristics including sampling jitter, excess loop delay, comparator hysteresis and operational amplifier parameters such as intrinsic noise, finite gain, finite bandwidth, slew-rate and saturation voltage is presented in this chapter. The error mechanisms are discussed along with a system level model. With the proposed models, we can perform exhaustive behavioural simulations of any ΣΔ modulator and trade off different topologies given a set of specifications. Hence, we can more precisely predict the impact of nonideal characteristics on the system performance within a short simulation time.

4.1 Sampling Jitter

Sampling of a signal is a memoryless, linear operation in which a continuous time signal is sampled at discrete moments in time. Commonly, the sample moments are spaced equidistantly with an interval T_s, resulting in uniform sampling. Any deviation or uncertainty in the sampling interval will introduce distortion if the samples are treated as if they were spaced equidistantly.

Random deviations in the zero crossing of a (sampling) clock signal, called *jitter*, can cause a reduction of the effective quantizer resolution and result in non-uniform sampling.

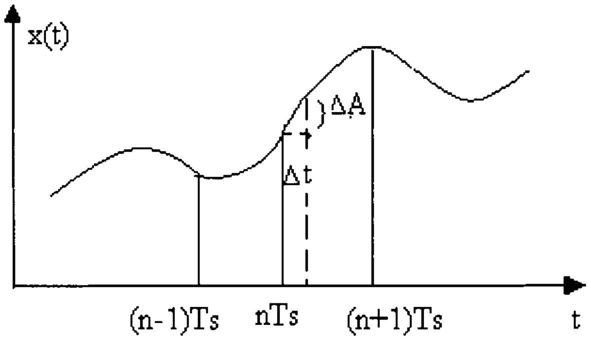


Figure 4-1 Sampling jitter

From Figure 4-1, it is shown that a deviation of Δt at a certain sample instant will result in an amplitude error ΔA. In order to avoid a significant loss of quantizer resolution, the amplitude error must not exceed the quantization step size, Δ; otherwise, the quantizer will become overloaded. The maximum amplitude error, ΔA_{max}, will occur when the rate of change of the sampled signal is at a maximum [106]. For a sine wave with amplitude A and frequency f_{in}, the maximum rate of change occurs around the zero crossings and equals:

$$\frac{dA\sin(2\pi f_{in}t)}{dt}\Big|_{\max} = 2A\pi f_{in} \qquad (4.1)$$

For $\Delta t \ll 1/f_{in}$, the rate of change of the sine wave can be considered constant within Δt [96], and the maximum deviation in amplitude can be calculated as:

$$\Delta A_{\max} = 2A\,\pi\, f_{in}\,\Delta t < \Delta \tag{4.2}$$

Thus, for an N bit quantizer, having full-scale amplitude of $A_{\max} \cong 2^{N-1}\,\Delta$, the maximum sampling time error is:

$$\Delta t_{\max} = \frac{2^{-N}}{\pi\, f_{in}} \tag{4.3}$$

The result in Equation (4.3) is believed to be overly conservative [52], since a clock corrupted by a random Gaussian jitter will have a peak timing error that cannot be defined exactly. Using the standard deviation however, one can predict the probability of an occurrence of a certain peak timing error of the jitter [52].

There is a number of jitter in the current literature, such as period, accumulated, and long-term jitter. Unfortunately, there has been no clear indication which of these is the “correct” specification for A/D converters [53].

The spectrum of the output noise due to clock jitter in a CT ΣΔM is often presumed to be white [51]. The quantizer clock jitter is a serious problem, as it can cause the noise notch to be filled with white noise, which further limits the minimum convertible input signal amplitude. Clock sources having random Gaussian distributed jitter with an assigned standard deviation, σ, have been generated in MATLAB [40] and then used for ELDO [107] simulations.

The deviation of Δt we named as $\delta_j(t)$, *the jitter*, is considered to be a discrete time random process with time step T_s having zero mean and being independent from the analog input signal, x (t). The former assumption is without loss of generality, the latter is well verified in most of the real systems [53]. $\delta_j(t)$ models the perturbation of the actual sampling instant from the ideal kT_s. The error that results from jittered sampling, $e_j(kT_s)$ is defined as:

$$e_j(kT_s) = x(kT_s + \delta_j(t)) - x(kT_s) \tag{4.4}$$

Usually, the input signal is assumed to be smooth enough, so that the jitter $\delta_j(t)$ is much smaller than the sampling period T_s, which is usually very well satisfied in practical applications [53], with this linear approximation, x $(kT_s + \delta_j(t))$ can be approximated as a first-order Taylor series expansion as:

$$\begin{aligned} e_j(kT_s) &\cong x(kT_s) + \delta_j(t)\cdot\frac{d}{dt}x(t)\Big|_{t=kT_s} - x(kT_s) \\ &= \delta_j(kT_s)\cdot x'(kT_s) \end{aligned} \tag{4.5}$$

The autocorrelation of Equation (4.2) is:

$$\begin{aligned} r_{ej}(mT_s) &= E\left[e_j(kT_s+mT_s)\cdot e_j(kT_s)\right] \\ &= E\left[\delta_j(kT_s+mT_s)\cdot\delta_j(kT_s)\,x'(kT_s+mT_s)\cdot x'(kT_s)\right] \\ &= r_j(mT_s)\,r_{x'}(mT_s) \end{aligned} \tag{4.6}$$

Knowing that the power is the value of the autocorrelation at zero, the magnitude of the clock error is a function of both the statistical properties of the sampling jitter and the input to the ΣΔ modulator. The ratio between the signal power to the jitter error power is calculated as [53]:

$$SNR_j = 10\log_{10}\left(\frac{r_x(0)}{r_j(0)\,r_{x'}(0)}\right)\ dB \tag{4.7}$$

This expression is a very powerful equation for communication system design. Within the linear approximation, the sampling jitter error depends on the variance of the sampling jitter $\delta_j(t)$ (for zero mean jitter, $r_j(0) = \sigma_j^2$). We assume that the jitter is a Gaussian random process with standard deviation $\delta_j(t)$. Then, we can implement the behavior model to the jitter error [40], as is depicted in Figure 4-2.

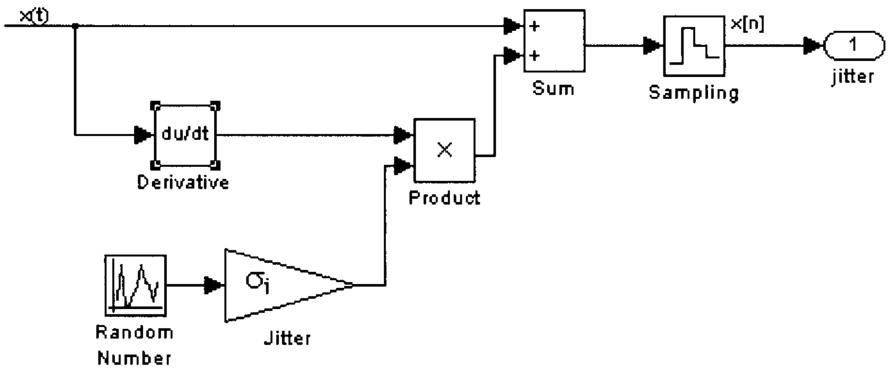


Figure 4-2 A random sampling jitter model

For two tone input signals, Equation (4.5) can be reproduced as:

$$x(t) = A(\sin\omega_1 t + \sin\omega_2 t)$$

$$x'(t)=A(\omega_1\cos\omega_1 t+\omega_2\cos\omega_2 t)$$

$$r_x(mT_s)=\frac{A^2}{2}\left[\cos(\omega_1 mT_s)+\cos(\omega_2 mT_s)\right] \tag{4.8}$$

$$r_{x'}(mT_s)=\frac{A^2}{2}\left[\omega_1^2\cos(\omega_1 mT_s)+\omega_2^2\cos(\omega_2 mT_s)\right] \tag{4.9}$$

$$e_j(kT_s)=\delta_j(kT_s)\,A\left[\omega_1\cos(\omega_1 kT_s)+\omega_2\cos(\omega_2 kT_s)\right] \tag{4.10}$$

Substituting Equations (4.9) and (4.10) into Equation (4.6):

$$r_{ej}(0)=r_j(0)\cdot\frac{A^2}{2}\left(\omega_1^2+\omega_2^2\right) \tag{4.11}$$

From Equation (4.8), we have: $r_x(0)=A^2$ (4.12)

Substituting Equations (4.11) and (4.12) into Equation (4.7):

$$SNR_j=10\log_{10}\left(\frac{2}{r_j(0)(\omega_1^2+\omega_2^2)}\right) \tag{4.13}$$

Assuming the sampling jitter is a white noise process while the sampling errors are uncorrelated from one sampling instance to another, the power of the jitter $r_j(0)$ is equal to the variance σ_j^2. Hence,

$$SNR_j=10\log_{10}\left(\frac{2}{\sigma_j^2(\omega_1^2+\omega_2^2)}\right) \tag{4.14}$$

So the performance is related to the variance of jitter and the frequency of the input signal. Higher input frequency means larger clock jitter error. Since the ΣΔ modulator has the oversampling property as we mentioned in chapter 2, the in-band clock jitter error is also related to the OSR.

In [104], Cherry indicated that the accumulated jitter whitens the in-band spectrum in much the same way as independent jitter, since any clock spectral impurities will randomly modulate the out-of-band noise into the signal band.

In a CTΣΔM the quantizer is the unique element that introduces clock jitter to the system. Clock jitter influences both the input signal sampling instants and the feedback pulse characteristics which means the jitter affects a signal with considerably more power than the input alone [102]. Therefore, a CTΣΔM is more sensitive to clock jitter than DT designs [39].

Two tones with 5MHz interval and the same amplitude are used as input signals. Fourth-order, CT BPΣΔM (Figure 3-10), DT BPΣΔM (Figure 2-16) architectures and the jitter model (Figure 4-2) are simulated.

Figure 4-3 shows the spectrum of a fourth-order, $f_s/4$ CT BPΣΔM with 21% clock jitter in which the in-band noise is increased.

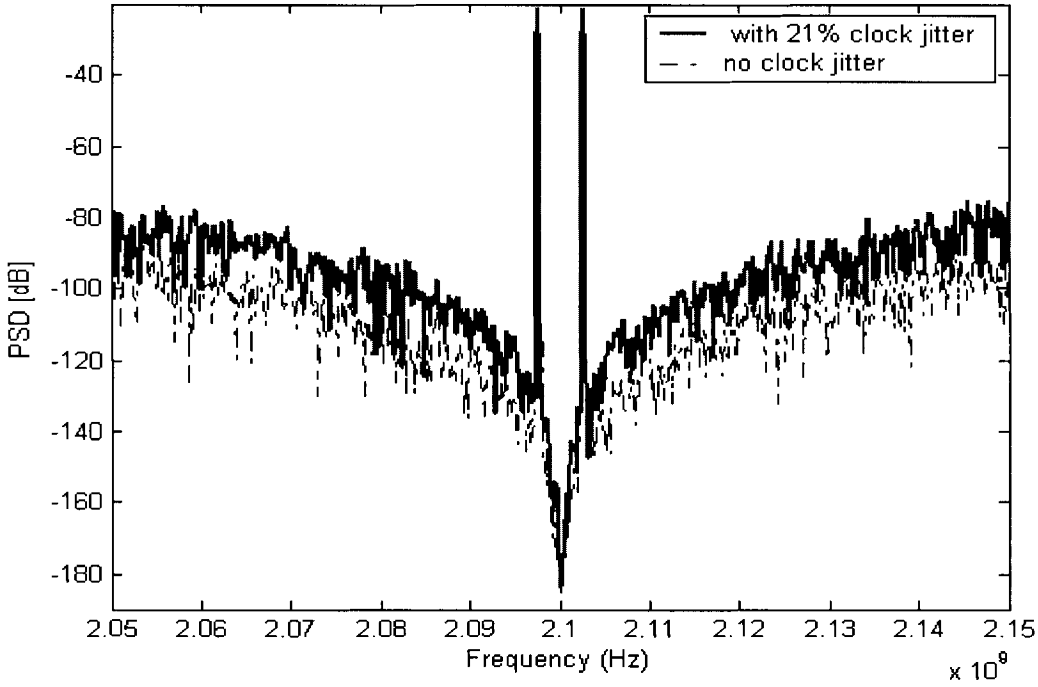


Figure 4-3 **The spectra of the $f_s/4$, CT BPΣΔM output with/without the clock jitter**

Simulation results (Figure 4-4) show that the jitter–induced noise for CT modulators is virtually independent of the input-signal amplitude. The pass band noise floor has a flat spectral density due to the white jitter, which whiten the quantization noise and reduced the harmonic distortion.

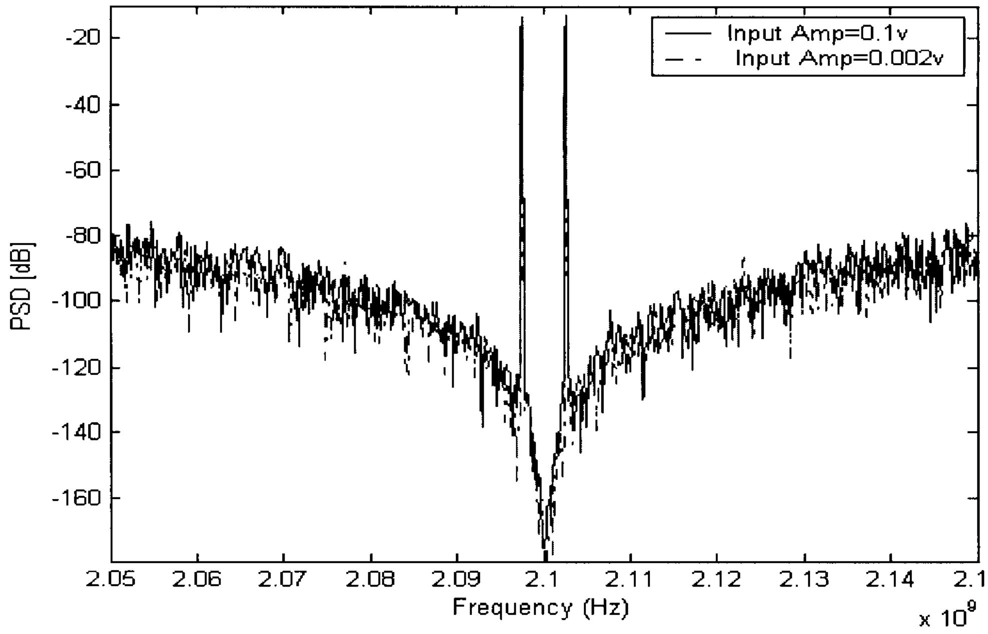


Figure 4-4 **The spectra of the $f_s/4$, CT BPΣΔM output with different input amplitudes having a 21% clock jitter**

In a CT ΣΔM design, the sampling occurs at the quantizer rather than the input, which shares the noise shaping with the quantization noise. Meanwhile, this white noise model works like the dither signal, which whites the quantization error. Hence for a smaller jitter, it will not affect CT BPΣΔMs much more than DT BPΣΔMs. Simulation results of the equivalent $f_s/10$ CT BPΣΔM and the DT BPΣΔM for a 10% clock jitter are shown in Figure 4-5 and Figure 4-6. The effect of the sampling jitter is more noticeable in DT BPΣΔM than in CT BPΣΔM. However, when we increase the jitter, CT BPΣΔMs are more sensitive than DT BPΣΔMs with $f_s/10$ architecture. The results are shown in Figure 4-7. Around 30% clock jitter, CT BPΣΔMs will become unstable and the performance is considerably degraded. The reason for this seems to be the jitter of CT BPΣΔMs affects the sum of the input plus the quantization noise – a signal with considerably more power than the input only. The quantization noise mixing with the jitter spectrum and the out-of-band quantization noise will fold into the pass band. Hence, this jitter model in CT ΣΔMs is more sensitive to high clock jitter than DT designs [51].

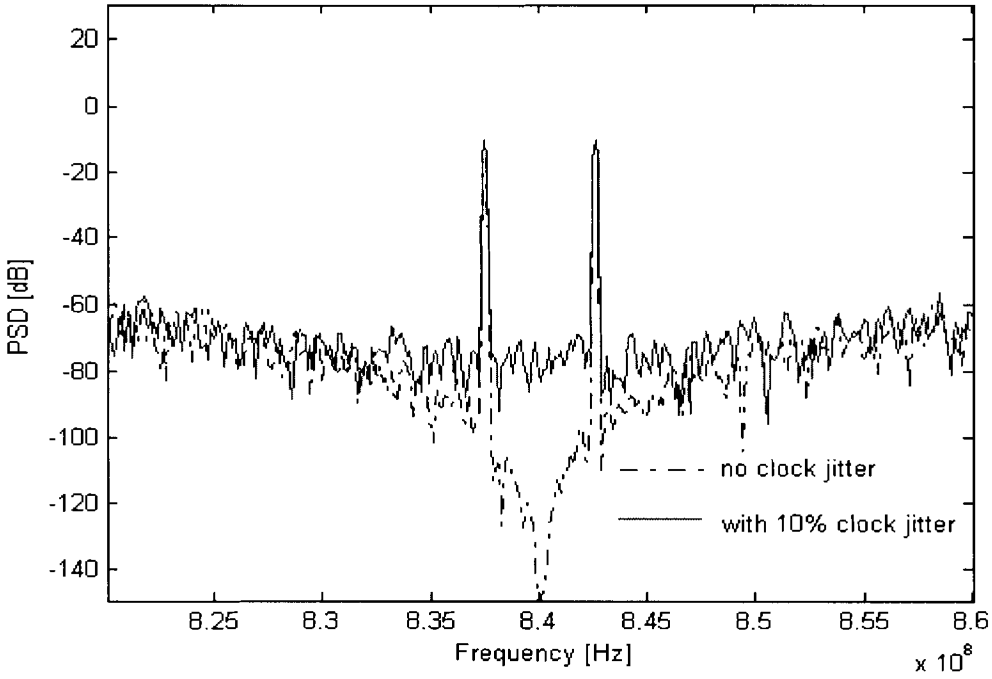


Figure 4-5 **The spectra of the $f_s/10$ DT BPΣΔM output with/without the clock jitter**

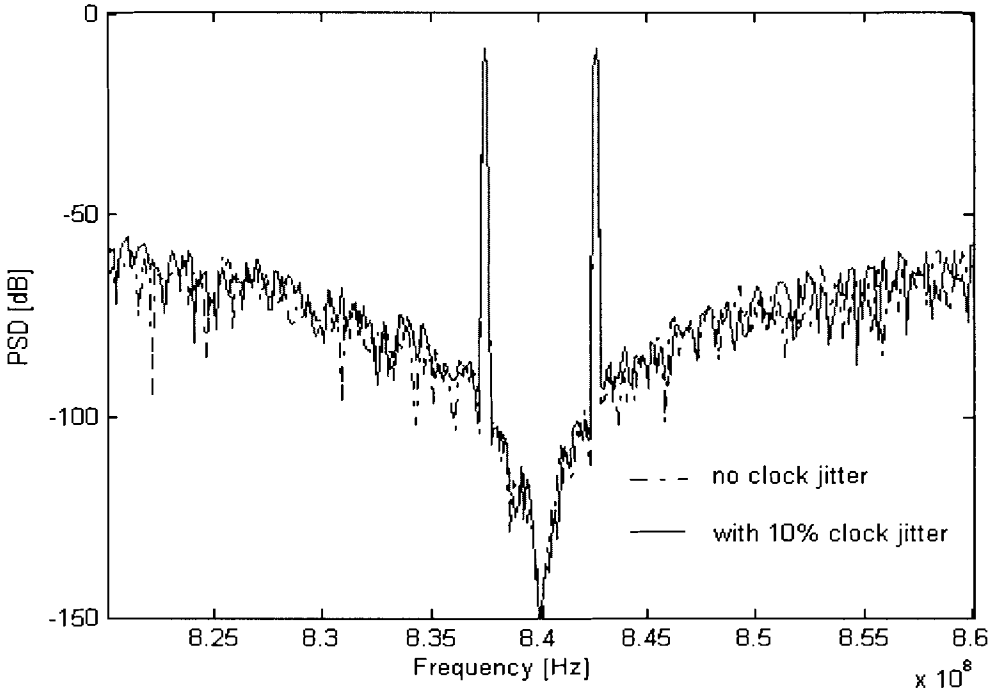


Figure 4-6 **The spectra of the $f_s/10$ CT BPΣΔM output with/without the clock jitter**

Figure 4-7 illustrates the signal-to-noise ratio of a CT BPΣΔM, which rapidly degrades for a sampling clock jitter increment beyond 25%. In earlier discussions we have seen that the larger the jitter, the more amplitude errors, and more quantization error is resulted. So far, there is not an obvious way to adjust the sampling jitter in high-speed circuits. The only way to guarantee that clock jitter does not alter the performance significantly is to use low-jitter crystal oscillators or low phase-noise VCOs and careful layout techniques to avoid substrate coupling [108]. Therefore, to satisfy the required specifications, the effect of the clock jitter on the SNR of a ΣΔM must be estimated for a given clock jitter system.

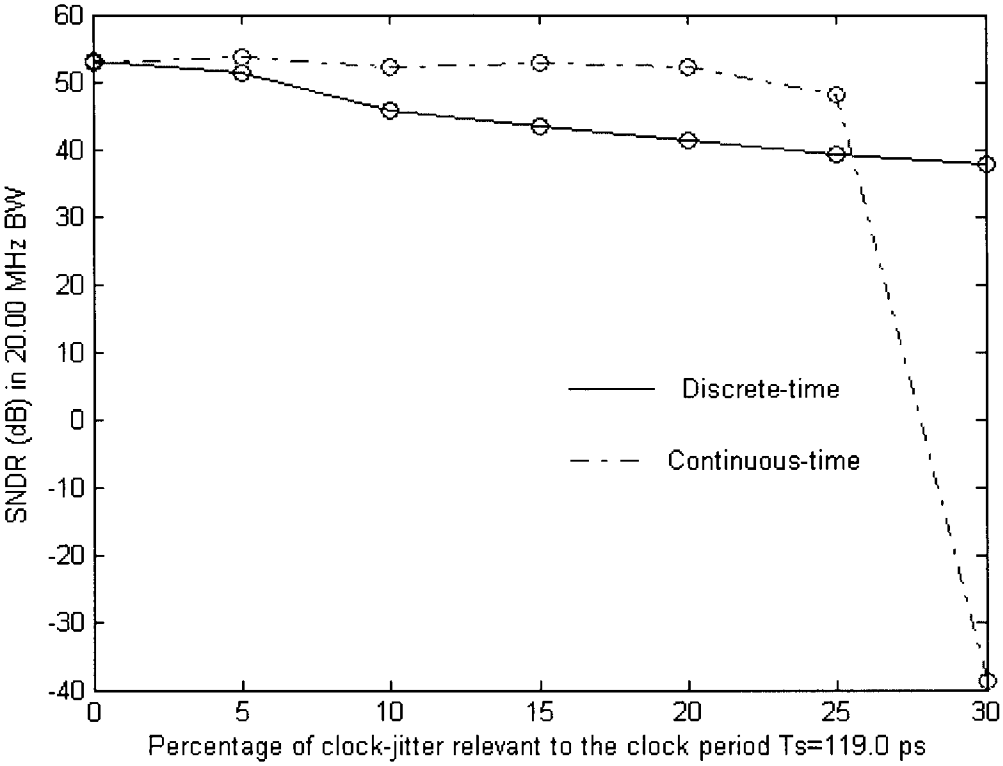


Figure 4-7 **Performance of the $f_s/10$ BPΣΔM with/without the clock jitter**

4.2 Excess Loop Delay

Ideally, the DAC currents respond immediately to the quantizer clock edge, but in practice, the quantizer is a latched comparator with a finite regeneration gain; a small quantizer input leads to a longer quantizer regeneration time. Furthermore, there is a delay in the DAC pulse. A non-zero delay exists between the quantizer clock and the DAC current pulse, which makes the edge of the DAC pulse begin after the sampling clock edge [14]. This delay is called *excess loop delay*, or simply *excess delay* or *loop delay* which results in higher in-band quantization noise and degraded modulator stability, although its effect can be mitigated by tuning the feedback coefficients.

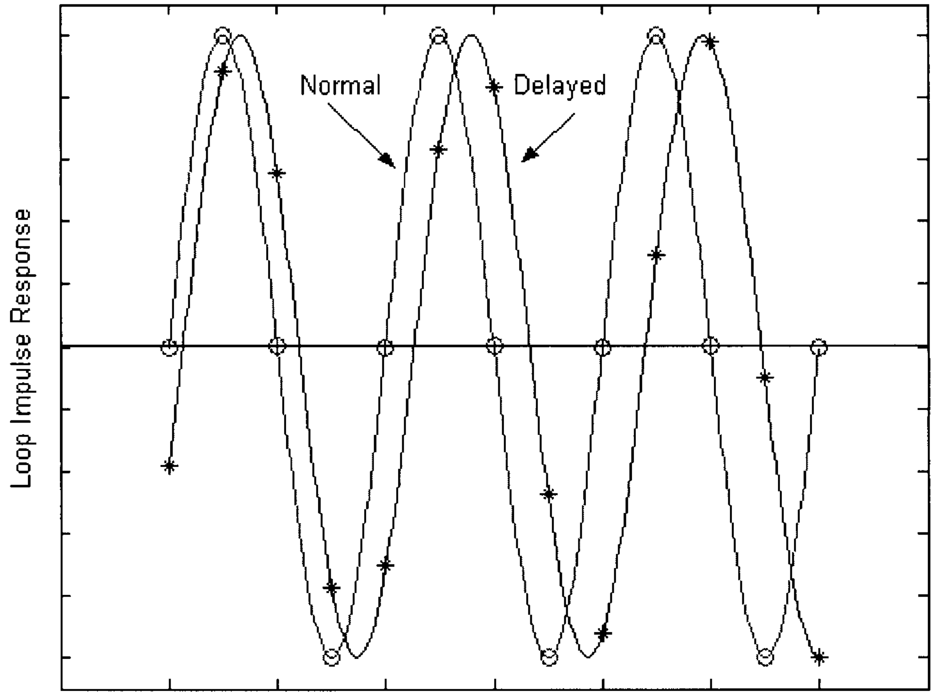


Figure 4-8 The effect of an excess loop delay on the loop samples

Excess loop delay has been studied extensively. Gosslau and Gottwald found that excess delay of 25% actually improves the DR of a 1st-order CT LP$\Sigma\Delta$M, compared to no excess delay [109,110]. Horbach confirmed this and extended the results to higher order LP modulators, showing that excess delay degrades their performance [111]. Chan found that a full sample of feedback delay in his 2nd-order LP modulator resulted in 10 dB loss of SNR [63]. Shoaei [52] found loop delays higher than 20% reduced SNR rapidly, and at 25%, the 4th-order BP $\Sigma\Delta M$ becomes completely unstable. Gao *et al.* [57] proposed the modified Z-transform to study the excess delay and demonstrated that tuning feedback coefficients can be implemented to alleviate delay problems in a 4th-order BP $CT\Sigma\Delta M$. In [103], Cherry and Snelgrove discussed the effects of the excess loop delay in a higher order LP and BP $\Sigma\Delta M$.

As shown in Figure 4-8 an extra loop delay can cause the samples to move from their original values represented by "circle" to some incorrect values represented by "*". The sampling times are assumed fixed (no clock jitter) but the open loop (Figure 3-6a) impulse response is changed at sampling moments 0, T_s, $2T_s$, ...

Thus, the excess loop delay can be assumed as [14]:

$$\tau_d = \rho_d T_s \tag{4.15}$$

The value of τ_d depends on the switching speed of the transistors f_T, the quantizer clock frequency f_s, the number of transistors in the feedback path n_t, and the loading on each transistor. As a rough approximation, we may assume all transistors switch fully after time $1/f_T$, in which case we could write [14]:

$$\rho_d \approx \frac{n_t f_s}{f_T} \tag{4.16}$$

τ_d could end up being a significant fraction of T_s depending on the parameters in (4.16).

For a return-to-zero (RZ) DAC pulse, the delayed pulse is shown in Figure 4-9. In the time domain, the delayed RZ pulse is described as:

$$\hat{r}_{rz}(t) = \begin{cases} 1, & \tau_d \le t \le \tau_d + \dfrac{T_s}{2} \\ 0, & otherwise \end{cases} \tag{4.17}$$

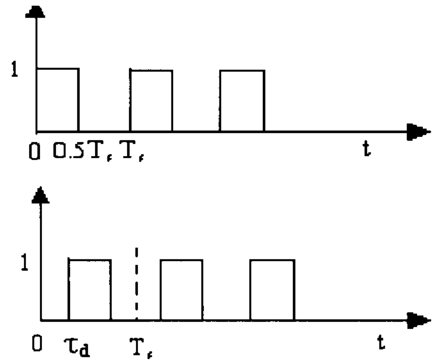


Figure 4-9 Illustration of the excess loop delay on a RZ DAC pulse

For a HRZ DAC pulse, the delayed HRZ pulse is

$$\hat{r}_{hrz}(t)=\begin{cases}1, & 0\le t\le \tau_{d},\ \ \tau_d \le t \le \tau_d+\dfrac{T_s}{2}\\ 0, & otherwise\end{cases} \tag{4.18}$$

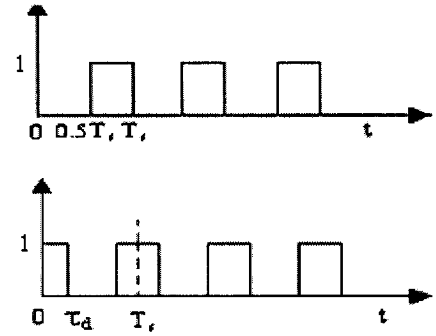


Figure 4-10 Illustration of the excess loop delay on an HRZ DAC pulse

Now, for a RZ DAC pulse, the period of the magnitude of 1 is changed from (0, $T_s/2$) to (τ_d, $\tau_d+T_s/2$); for an HRZ DAC pulse the duration of the magnitude of 1 is changed to (0, τ_d) plus ($\tau_d+T_s/2$, T_s). Applying the delayed pulse to the system shown in Figure 3-10, if the four coefficients are not changed, one could see that the new system is not equivalent to its discrete-time counterpart and Equation (3.5) is no longer valid.

With the loop delay, an extra term, $e^{-s\tau_d}$, appears in the s-domain of DAC pulse. In the Z-domain the loop filter H (z) will have some extra terms in the numerator. The order of the numerator of H (z) would be increased [14, 57]. The related denominator of NTF is also changed. The poles of NTF will approach the unit circle and the system will become unstable. Since the quantizer is input signal dependent, the quantizer gain is not always 1. Increasing the delay τ_d to a certain point will degrade the system performance. Simulation shows in Figure 4-11 that smaller input would make the system more stable in the presence of a large delay [108].

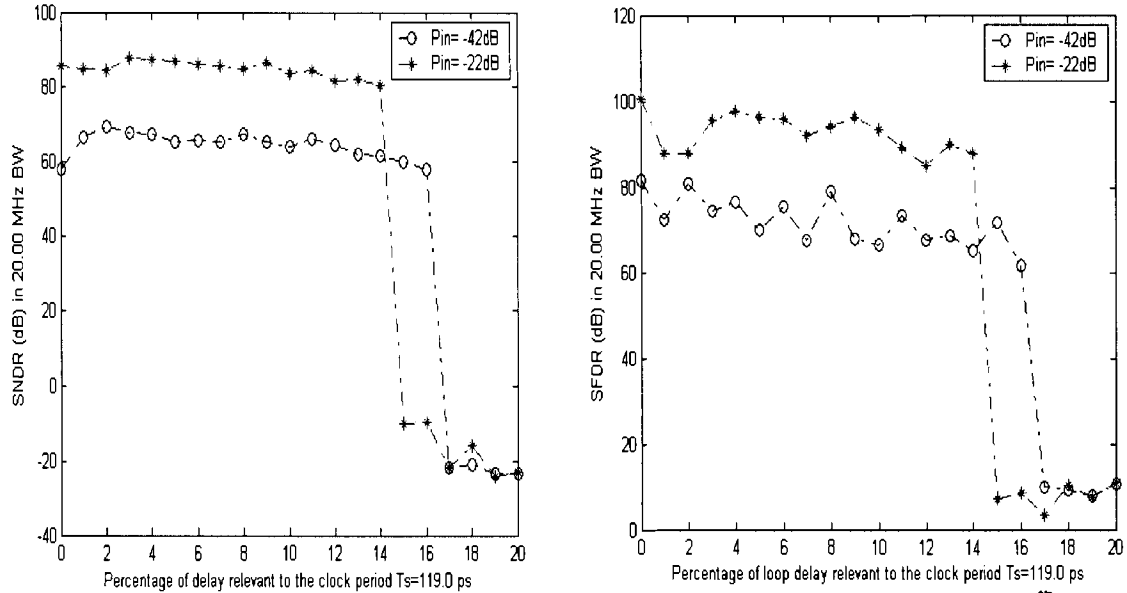


Figure 4-11 **SNDR and SFDR vs. loop delay with different input powers for the 4^{th}-order, f_s/10 CT BPΣΔM**

As we illustrated in Chapter 3, varying the out-of-band gain of NTF can change the system dynamic range and the maximum stable input amplitude. The simulation illustrated in Figure 4-12 shows that it is possible to make a modulator immune to the excess loop delay by choosing the appropriate out-of-band gain of NTF. The same result is presented in [103] particularly for higher order modulators that are implemented directly from the NTF.

The nonzero switching time of the transistors in the feedback path results in asymmetry in the DAC feedback pulse and causes signal imbalance and even intersymbol interference [58]. The return-to-zero (RZ) or the half-delay-return-to-delay (HRZ) technique improves matching of the waveforms. As a result, it greatly reduces signal dependence of the mismatch. If we know exact the delay τ_d, then with the right DAC pulses we could tune the feedback pulse coefficients C_s to match the equivalent *H(z)* form.

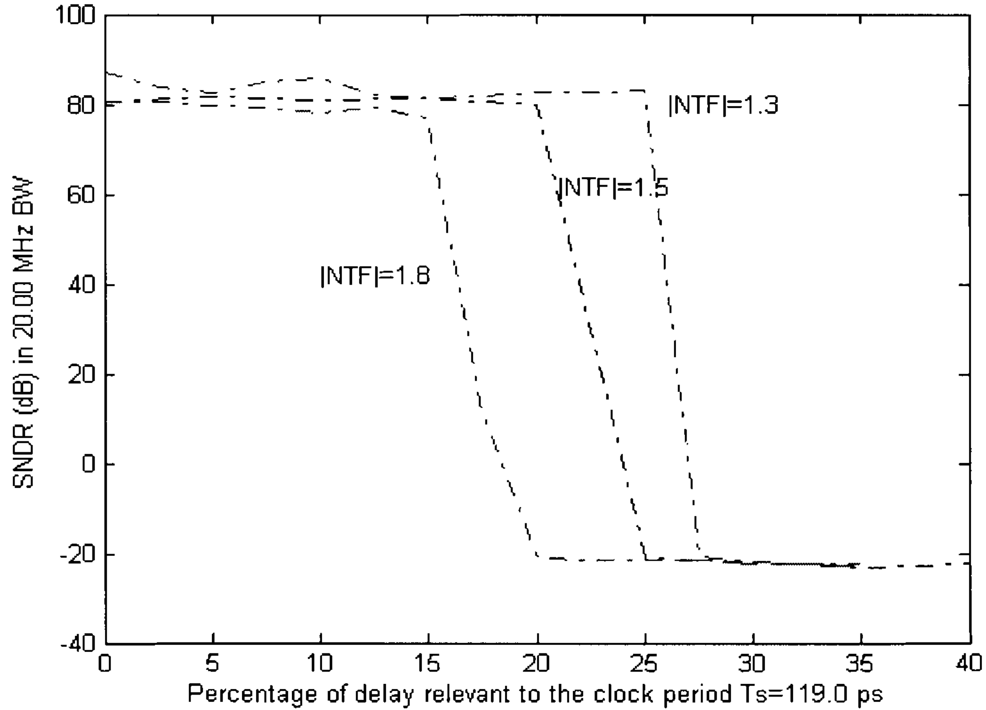


Figure 4-12 **SNDR/NTF gain vs. τ_d for the 4^{th}-order, $f_s/4$ BP CTΣΔM**

Following the procedure in section 3.4, we can match the CT BPΣΔM to its DT BPΣΔM. With the loop delay, the duration (α,β) of the magnitude 1 of the RZ DAC pulse is changed from (0, $T_s/2$) to (τ_d, $\tau_d+T_s/2$). For a HRZ DAC pulse, (α,β) is the linear combination of (0, τ_d) and ($\tau_d+T_s/2$, T_s). For simplicity, we will assume the sampling frequency f_s is 1. Thus the discrete-time *B* matrix (3.12) for the delayed HRZ DAC pulse (Figure 4-10) is changed to:

$$B_{(\alpha,\beta)} = A_{NRZ}^{-1}\cdot\left(e^{A_{NRZ}} - e^{A_{NRZ}(1-\tau_d)}\right)\cdot B_{NRZ} + A_{NRZ}^{-1}\cdot\left(e^{A_{NRZ}(1-\tau_d-0.5)} - 1\right)\cdot B_{NRZ} \qquad (4.19)$$

One can use MATLAB to tune the coefficients, which is demonstrated in Appendix A. For instance, if τ_d is equal to 20% of T_s with an $f_s/4$ architecture, |NTF|=1.8, tuning C_s to

{ C2r, C4r , C2h , C4h } = { -6.3948, -1.4224, 6.8837, 1.4058}

The performance is shown in Figure 4-13.

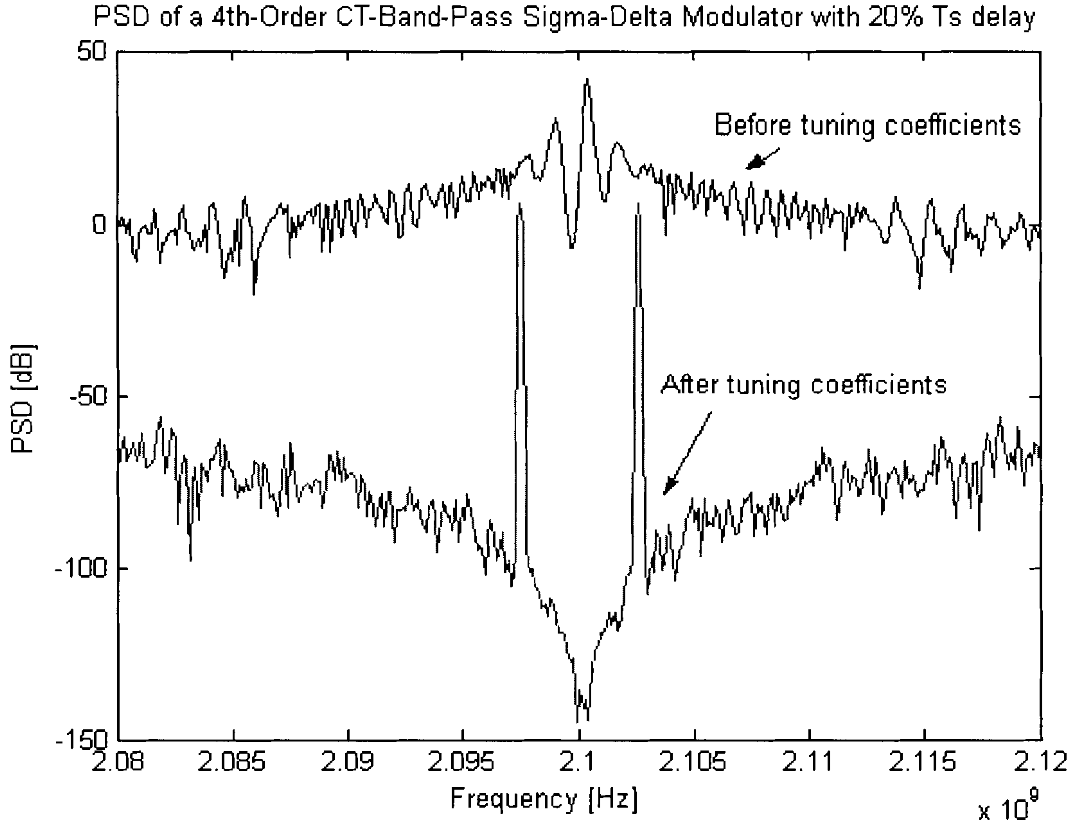


Figure 4-13 Two-tone spectrums at a certain input level before and after tuning

A way to mitigate excess loop delay is to find a way to provide a full degree of freedom to make the equivalent discrete-time domain loop transfer function match the desired transfer function. An extra DAC feedback loop can be added to the front-end building block and is applied to degrade the loop delay effects [24, 52, 112]. A multi-bit quantizer can be used in the multi-feedback loop [103] and attempts to improve the immunity to the loop delay. However, the technique is very hard to implement in a high-speed CT ΣΔM and an additional excess delay is added.

From the simulation results and paper [57,103], with the proper DAC pulses and tuning the feedback parameters, the performance loss due to delay can be greatly mitigated. How to design a tuning algorithm to maximize DR that works on-chip, perhaps even while the modulator is operating, is an interesting topic for future research.

4.3 Hysteresis

In a ΣΔM there is a comparator, which quantizes a signal in the loop and generates the output of the modulator. Although the comparator characteristics can be suppressed by the noise shaping property of the feedback loop of the modulator, there are still important circuit design parameters to be considered. Hysteresis is one of them.

Consider two thresholds, V_{TL} and V_{TH}, shown in Figure 4-14. When the input voltage is in the range $V_{TL}<V_{in}<V_{TH}$ (assume V_R, the reference threshold, is zero), the output can be either L_+ or L_-, depending on the state that the circuit is already in. Thus, for this input range, the output is determined by the previous value of the trigger signal that causes the circuit to be in the current state. The width of the hysteresis is the difference between the high threshold V_{TH} and the low threshold V_{TL} [85].

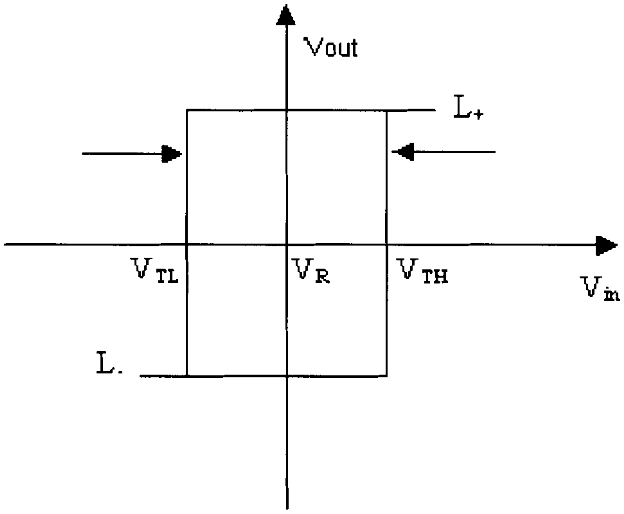


Figure 4-14 Comparator characteristic with hysteresis

The output of the comparator with hysteresis can be expressed as:

Case1: $V_{pre\_out} = L-$

$V_{in} \leq (V_R + V_{hys}/2)$, $V_{out}=L-$

$V_{in} > (V_R + V_{hys}/2)$, $V_{out}=L_+$

Case2: $V_{pre\_out} = L_+$

$V_{in} \leq (V_R - V_{hys}/2)$, $V_{out}=L-$

$V_{in} > (V_R - V_{hys}/2)$, $V_{out}=L_+$

Combining these two cases yields the following equations:

$$V_{in} \leq (V_R - \text{sign}(V_{pre\_out}) \times V_{hys}/2) , \quad V_{out}=L- \tag{4.20}$$

$$V_{in} > (V_R - \text{sign}(V_{pre\_out}) \times V_{hys}/2) , \quad V_{out}=L_+ \tag{4.21}$$

where sign(.) is the sign function whose value equals unity for positive V_{pre_out} and −1 otherwise. "Memory" exists in the comparator that can create unwanted system poles, which may cause errors in the signal and the NTF [9]. Nevertheless, by introducing hysteresis of appropriate width, it can reject interference since the two thresholds V_{TH} and V_{TL} can reduce the potential error click due to the interference superimposed on the input signal, and hence provide another form of filtering [85].

Although hysteresis means that the quantizer sometimes does not make a decision to change the output bit when it should, the performance of a ΣΔM does not suffer much because of hysteresis [14,39]. In [39], the researchers illustrated that hysteresis may be as severe as 0.1Δ with negligible performance loss in a SC circuit. In our simulation, shown in Figure 4-15, when the hysterisis is 0.1Δ, the in-band noise is unchanged and is close to the analytical result [39], which is the sum of quantization noise N_q and the hysteresis:

$$N_{noise} = \frac{\pi^{2n}}{2n+1} \frac{\Delta^2}{OSR^{2n+1}} \left(\frac{1}{12} + 4h^2 \right) \quad OSR >> 1 \tag{4.22}$$

N is the order of the modulator, Δ is the quantization step size and h is the magnitude of the comparator hysteresis relative to Δ. The factor 4 reflects the adjustment of the scalar preceding the second resonator from 2 to 0.5. The researchers model the comparator hysteresis with AWN with power $(h\Delta/2)^2$.

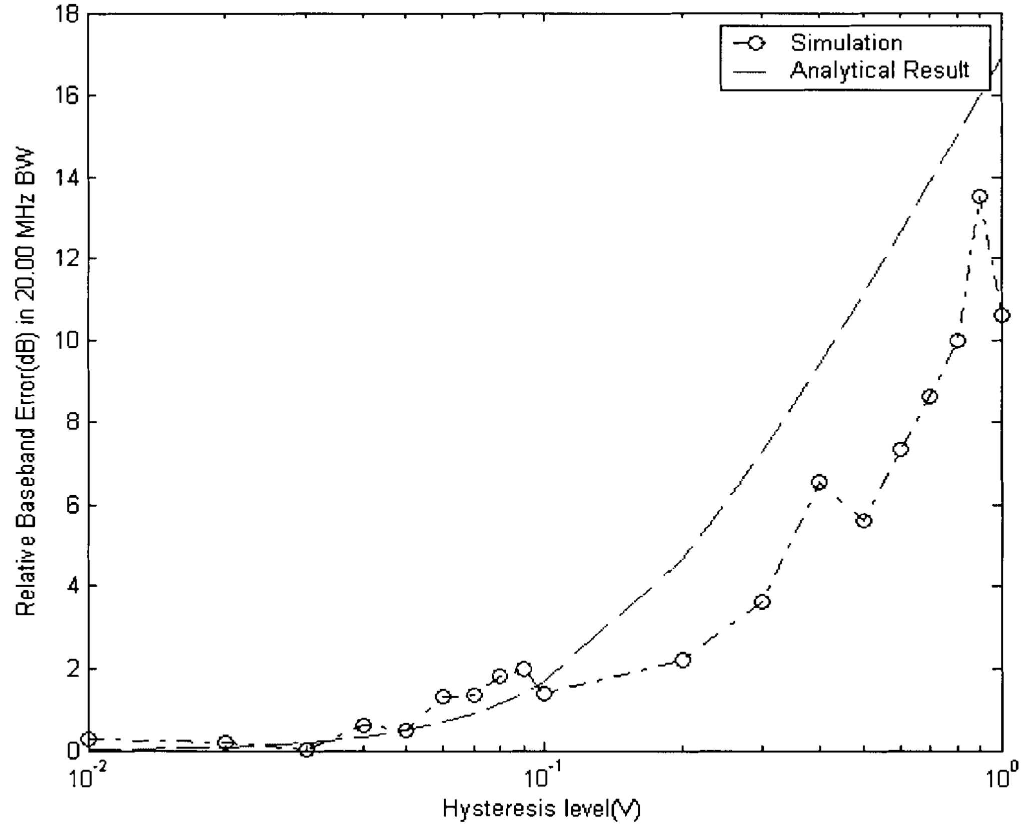


Figure 4-15 **The 4th-order, $f_s/4$ CT BP CTΣΔM with hysteresis (Pin=-26dB)**

In Figure 4-16, we see the PDF of the quantizer becoming wider with hysteresis. This is expected, as long as the quantizer output bit remains the same, the circuit inside the loop will continue integrating in the same direction, enlarging the signal swings [14].

Hysteresis introduces harmonic distortion, moreover too large an internal signal excursion range results in gradual instability and hence DR loss [14]. In Figure 4-17, performance loss is very small even for large hysteresis that is attributable to the presence of the noise-shaping property of the feedback loop.

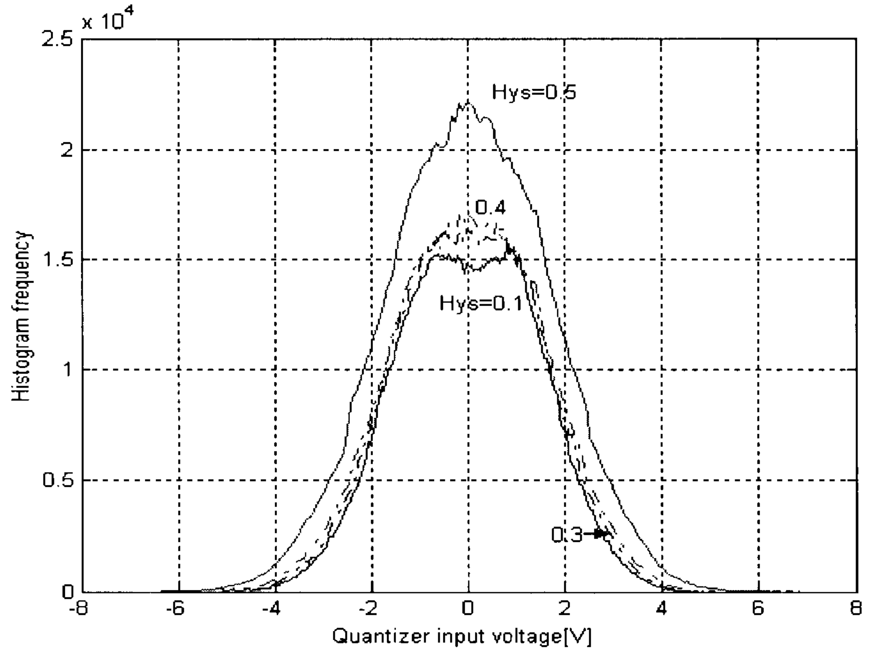


Figure 4-16 Histogram frequency vs. quantizer input voltage with Pin=-34dB

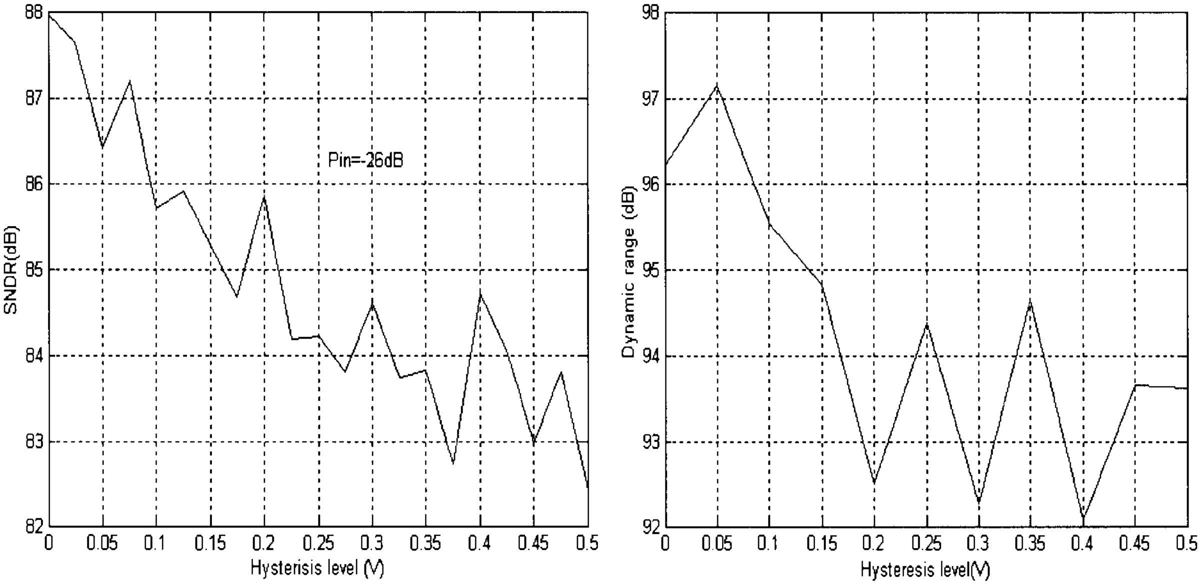


Figure 4-17 a) SNDR vs. hysteresis level, b) Dynamic range vs. hysteresis

4.4 Nonlinearity of the Input Transconductor

Linearity is imperative in circuit design because the input signal frequency can be very close to saturation at the input. As a result, even a weak nonlinearity can produce distortion. In this section, a simple nonlinear model is proposed.

Because of noise shaping, nonlinear effects are most important at the input. The input transconductor uses a differential pair degenerated with an emitter resistor g_m in the CT ΣΔM [11]. The linearity of this transconductor is the key to the linearity of the whole circuit [14].

It has been assumed that the modulator is constructed with fully differential circuits. The result is the cancellation of all even-order distortion terms (harmonic and intermodulation), regardless of the cause of the distortion. It has also been assumed, to simplify the analysis, that the power of a harmonic decreases with increasing harmonic order. Therefore, only third order nonlinear terms are considered [9].

Hence, the nonlinearity can be modelled at the input along with a weak cubic nonlinearity.

$$V_{in'} = V_{in} + \beta V_{in}^3 \tag{4.23}$$

where β is the nonlinearity coefficient of the input transconductor.

Simulation results (Figure 4-18) illustrate that the nonlinearity limits the peak SNDR achievable at large signal levels, which agrees with [39]. Figure 4-19 shows the spectrum of the 4th-order $f_s/4$ CT BPΣΔM with and without nonlinearity. After plugging in nonlinear components, the third order IMD is very noticeable.

Nonlinear effects are difficult to handle analytically. The best approach in dealing with nonlinearity is to have a good qualitative understanding of their causes and effects. The computer simulation can get quantitative results on modulator performance due to nonlinearity, but it may be very inaccurate because of the inherent difficulty of modelling these very small effects [9].

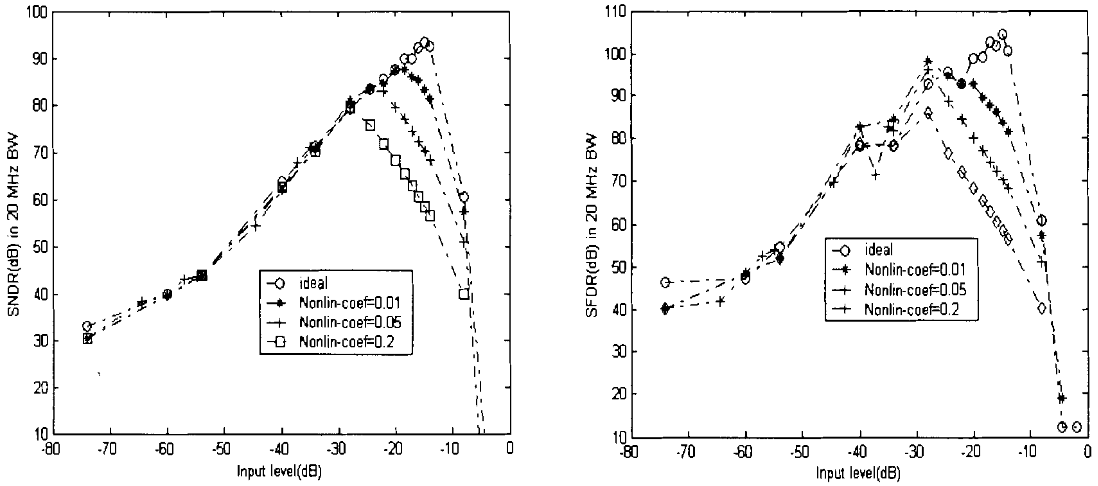
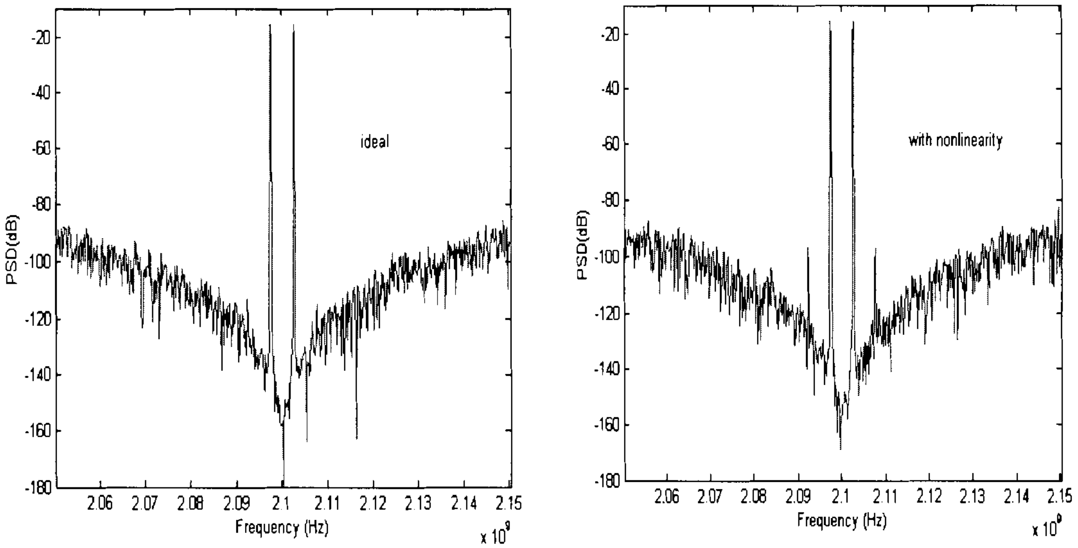


Figure 4-18 Influence of transconductor nonlinearity on the performance of the 4th-order, $f_s/4$ CT BPΣΔM



a) ideal **b) β =0.01**

Figure 4-19 Spectrums on the 4th-order, $f_s/4$ CT BPΣΔM with Pin=-14dB

4.5 *Finite Gain*

The resonator we addressed previously is assumed to be ideal in the sense that the gain of the centre frequency is infinite (Figure 4-20).

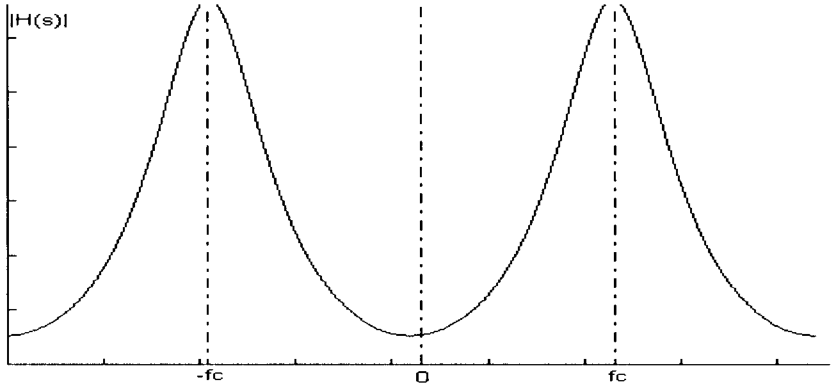


Figure 4-20 Frequency response for the ideal resonator

In practice, the op-amp gain is limited by the finite Q of the resonator as well as the circuit constraints. These produce finite gain of the loop filter at the pole frequencies and finite loss of the NTF at the corresponding frequencies. The resulting frequency response of the resonator is given by:

$$H(s)=\frac{\omega_c s}{s^2+(1-\beta_l)\omega_c s+\omega_c^2} \tag{4.24}$$

The consequence of this "resonator leakage" is that a fraction of β_l of the previous output of the resonator is added to each new input sample.

The factor β_l limits the height of the peak in the magnitude response and shifts the peak away from the centre frequency. The limited gain increases the in-band quantization noise shown in Figure 4-22. As shown in Equation (4.24), the poles of the loop filter are changed due to the leakage. The pole error causes a leakage of unshaped quantization noise to the output of the converter. Finite gain decreases the notch in a manner similar to capacitors mismatch. It also reduces the resonator's peak gain, thus decreasing pole radius. Decreased pole radius is a more serious concern than a shift in centre frequency because it corresponds to a familiar problem in LPΣΔMs. stable limit cycles that result in increased distortion and "dead-band" behaviour [2, 26].

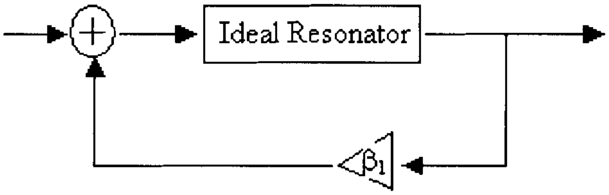


Figure 4-21 Resonator with finite gain

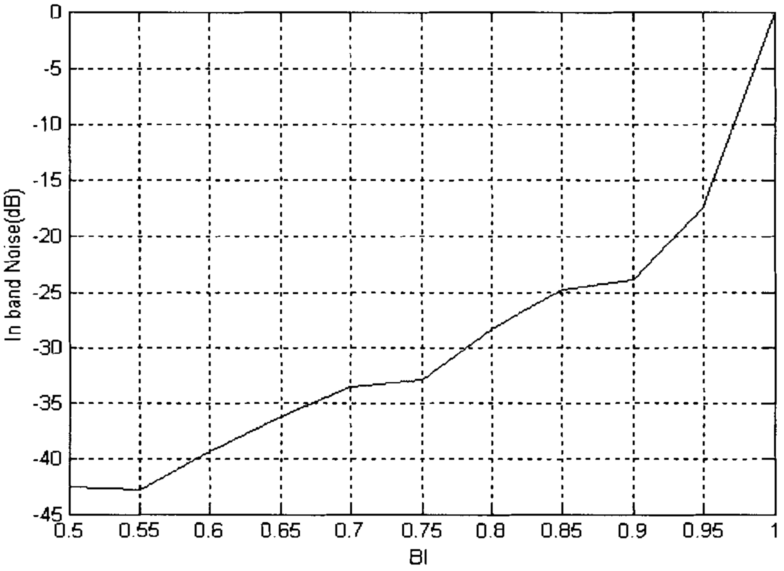


Figure 4-22 In-band-noise vs. β_l

4.6 Intrinsic Noise

Frequency domain based noise analysis techniques for linear time-invariant systems are well known. Many studies of noise analysis for periodically switched linear circuits can also be found in literature since the launch of switched-capacitor techniques in the 1970s. Noise analysis for nonlinear circuits, however, is always a difficult problem.

In an analog implementation of ΣΔMs, the signal is corrupted not only by quantization error, but also by electronic noise generated in the device itself. We refer to it as intrinsic noise (or op-amp noise). Since it is a property of the device, intrinsic noise cannot be eliminated by shielding, filtering or circuit layout, but its value can be altered by choice of circuit topology and component size. The two most important noise mechanisms in MOS devices are thermal noise and 1/f—flicker noise [9].

Thermal noise and 1/f noise are caused by the random fluctuation of carriers due to thermal energy, which are present even at equilibrium. The intrinsic noise is conventionally modelled as an ergodic stationary process [9]. We assume the intrinsic noise has a white spectrum with variance V_n^2.

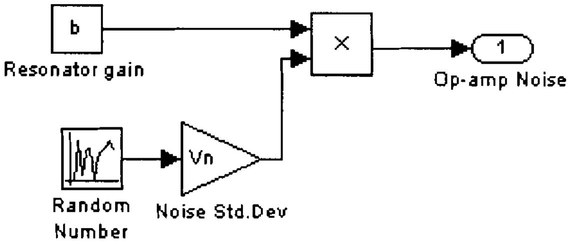


Figure 4-23 Intrinsic noise model

The total input-referred noise power V_n^2 (V_n represents the total rms noise voltage referred to in the op-amp input) includes 1/f noise, wide-band thermal noise and DC offset. DC offset is only a minor concern in signal acquisition systems when the quantization is uniform. Power supply, substrate and clock feed through noise depend heavily on layout and circuit topology. Thermal noise generated by the resistors and amplifiers is a fundamental constraint. Accurate calculation of electrical noise is important to predict the circuit performance characteristics.

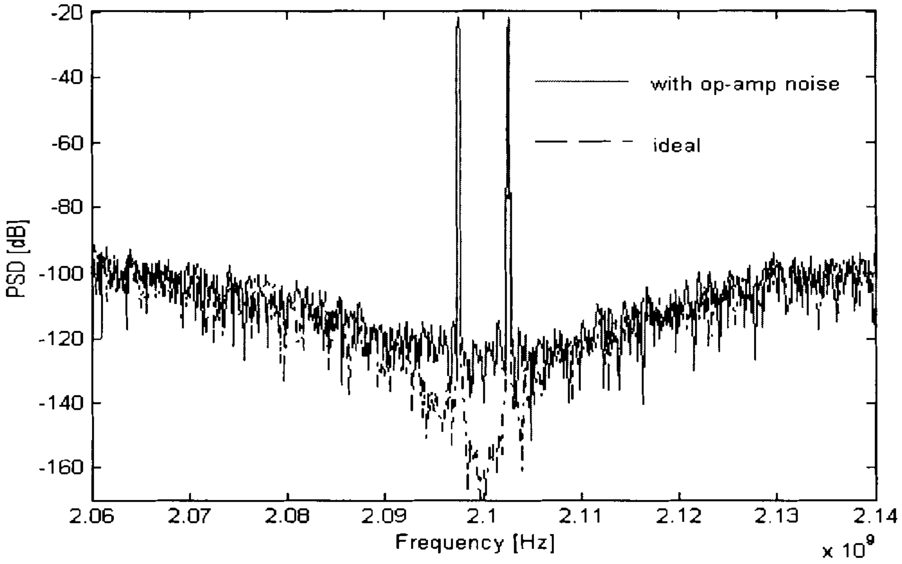


Figure 4-24 Spectrums with intrinsic noise (Vn=90uV$_{rms}$)

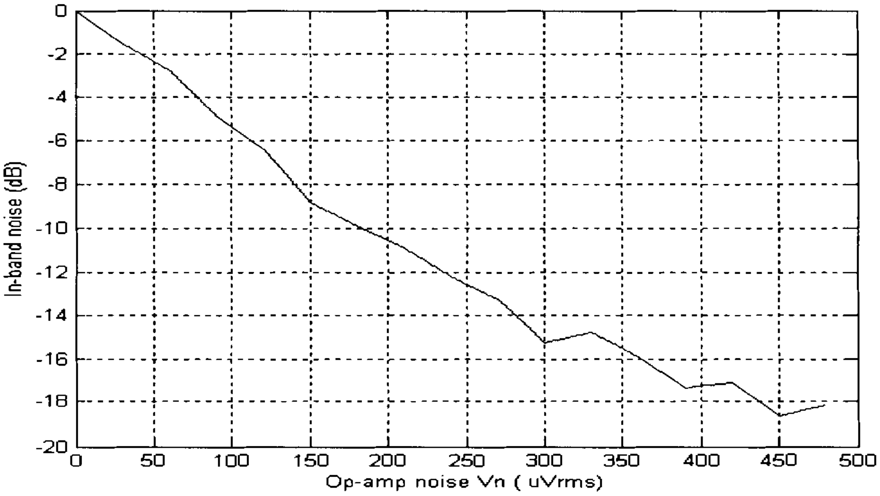


Figure 4-25 In-band noise caused by intrinsic noise

4.7 Finite Bandwidth and Slew-rate

Ideally, the output of a sampled-data analog filter settles completely during each sampling period, but in reality this is not possible. First, the output of the op amp usually approaches its desired value with a form of decaying exponential. Second, the finite slew rate of the op amp limits the maximum rate at which the output can change [55].

An op amp has some limitations in frequency due to poles that limit the speed of the settling process. Usually, it is assumed an op amp can be modelled as a single-pole system with time constant τ [36, 39, 60, 64] that implies the op-amp unity-gain bandwidth (GBW) should be on or above the order of the modulator sampling rate. However, simulations indicate that the op-amp unity-gain bandwidth can be considerably lower than this; and with correspondingly inaccurate settling, it will not impair the $\Sigma\Delta$ modulator performance. The settling process is a linear phenomenon and does not result in a change in the shape of an input sinusoid. That is, it does not lead to nonlinear distortion [39, 63, 64].

The slew-rate (SR) limitation refers to the fact that there is a specific maximum rate of change possible at the output of a real op-amp, which is defined as

$$SR = \frac{dv_0}{dt}\Big|_{\max} \tag{4.25}$$

It is usually specified on the op-amp data sheet in the units of V/µs [85]. The slew-rate limitation can cause nonlinear distortion to an input sinusoidal signal when its frequency and amplitude are such that the corresponding ideal output would require v_0 to change at a rate greater than SR. This introduces input signal harmonics in the output spectrum that degrades the SNDR [63, 64].

The effects of finite bandwidth and slew-rate of the operational amplifier are related to each other and are interpreted as a nonlinear gain. The exact settling characteristics will depend on the details of the resonator and amplifier implementations. In essence, the settling behaviour of the op-amp has been subdivided into three distinct cases: linear settling only, a combination of linear settling and nonlinear slewing, and nonlinear slewing. A good first-order model of the settling response of the generic op amp has been incorporated into the discrete time simulator and is defined as [55]:

$$v_{out}((n+1)T_0) = v_{out}(nT_0) + g(\beta_l\, v_{in}(nT_0)) \tag{4.26}$$

where

$$g(x) = \begin{cases} x[1 - e^{-\frac{T_0}{\tau}}], & |x| \le SR\,\tau \\ x - sign(x)\,SR\,\tau\, e^{-\frac{1}{\tau}[T_0 + \tau - \frac{|x|}{SR}]}, & SR\tau < |x| < SR(T_0 + \tau) \\ sign(x)\,SR\,T_0, & |x| \ge SR\,(T_0 + \tau) \end{cases} \tag{4.27}$$

sign(.) denotes the sign function, whose value equals unity for positive x and –1 otherwise. τ is the settling time constant, which is inversely related to the amplifier bandwidth GBW and the β_l is the resonator leakage. The T_0 represents the available settling time (approximately half a clock cycle) [61]. In this model, the output of the integrator is assumed to approach its final value with a single exponential time constant τ and the maximum rate of change is limited to SR.

4.8 Saturation

Practically speaking, the amplifier transfer characteristic remains linear over a limited range of input and output voltages. For an amplifier operated from two power supplies, the output voltage cannot exceed a specified positive limit and cannot decrease below a specified negative limit. If the input signal swings out of the limits, it will be clipped because of amplifier saturation. Clipping will result in severe baseband noise penalties [36, 39, 64]. To avoid clipping the peaks of the output waveform, and the resulting waveform distortion, the input signal must be kept correspondingly small.

We can use a saturation block or MATLAB function "tanh" to implement this characteristic.

$$if\ |V_o| > V_{sat}\ then\ V_o = V_{sat} \times sign(V_o) \tag{4.28}$$

4.9 Simulation Results of Two Tone Inputs

These nonideal characteristics and the estimated impact on the performance at the system level can help us in selecting a circuit topology. The SIMULINK model we implemented is shown in Figure 4-26. Only the nonideal characteristics of the first resonator are considered as their effects are not attenuated by the noise shaping.

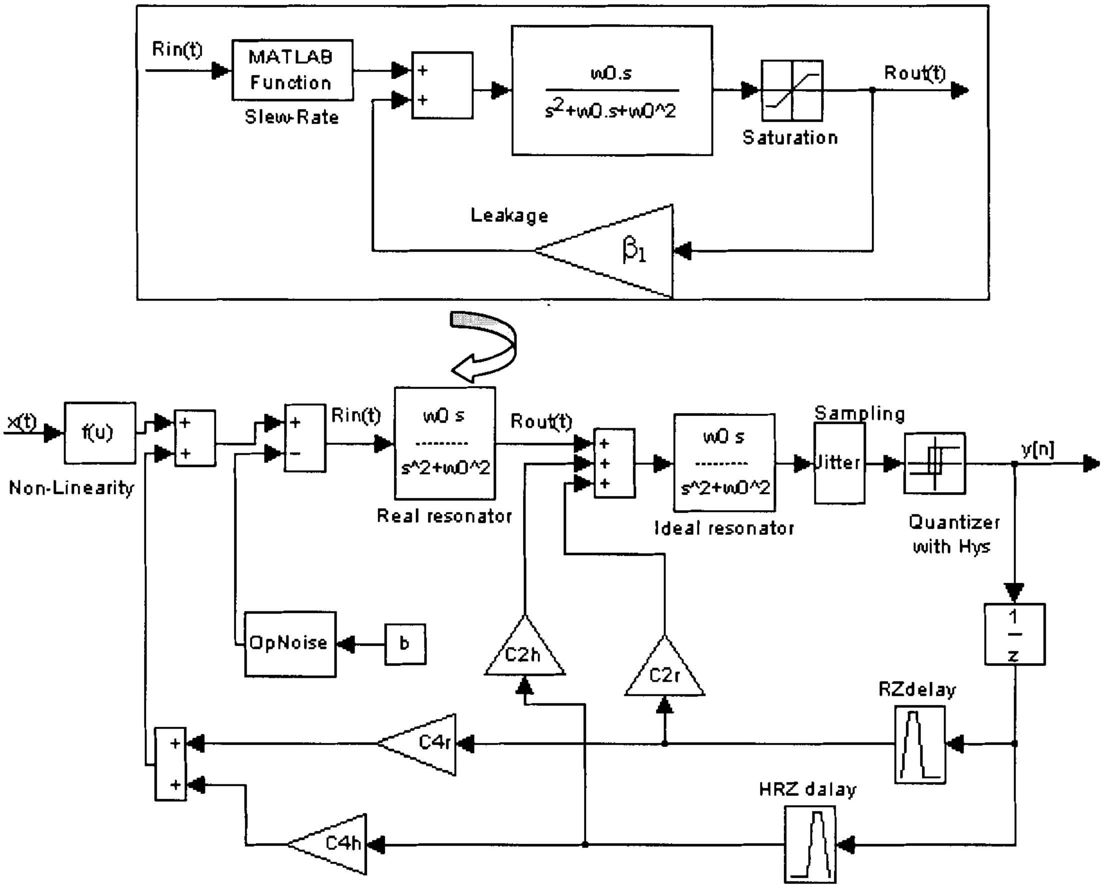


Figure 4-26 The 4^{th}-order CT BPΣΔM with nonideal components

Using two sinusoids at the input and then feeding them into an $f_s/4$ 4th-order CT BPΣΔM structure, the simulation parameters are shown in Table 4-1.

Parameters	Value
Center Frequency	2100MHz
Frequency Interval	5MHz
Signal Bandwidth	20MHz
Sampling Frequency	8400MHz
Input amplitude	30mV

Table 4-1 Simulation parameters

Table 4-2 compares the total SNDR and the total SFDR of the ideal modulator with those achieved with the same architecture, when one single limitation at a time is introduced. The spectrum is shown in Figure 4-27.

Resonator Nonideal Characteristics	SNDR (dB)	SFDR (dB)
Ideal modulator	83.8	96.9
Sampling jitter (δ_j =11.905ps)	77.9	90.6
Excess Loop-delay (τ_d = 11.905ps)	83.2	94.3
Hysterisis (0.1V)	82.9	94.6
Non-linearity (β = 0.1)	79.5	81.5
Op-amp noise (V_n=90μV_{rms})	79.7	93.2
Finite gain (|$H(f_c)$|=100)	81.4	93.2
Saturation voltage (1.55V)	81.3	96.8
Finite bandwidth(GBW=15.75GHz, SR=33.6V/ns)	82.9	92.2
All nonideal characteristics	73.6	79.0

Table 4-2 Simulation results

Simulation results show some nonideal characteristics affecting each other. When the sampling jitter or excess-loop delay becomes large, the system performance is degraded. However, for a small deviation, it seems to whiten the spectrum and increase the SNDR. Since the system is nonlinear, we need to be aware of the input power, as increasing power will cause the system to become unstable.

So far, we have presented the major macro-models of nonideal component characteristics. In practice, there are other nonideal factors that are unknown or are difficult to derive equivalent analytical models. This reminds us that when we design a circuit, we must take into account those nonideal elements and be aware of the layout and circuit topology in order to avoid unnecessary loss of performance.

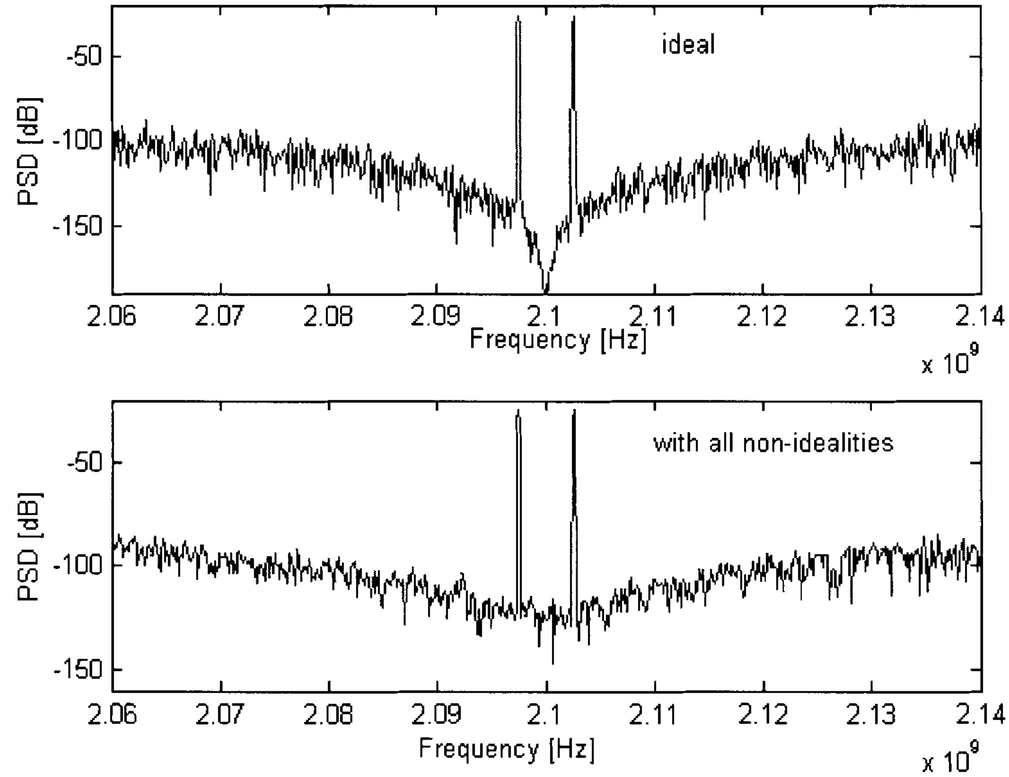


Figure 4-27 PSD of the 4th-order, $f_s/4$ CT BPΣΔM with all nonideal characteristics

Chapter 5

Class S Amplifier with H-bridge Configuration in the CT BPΣΔM

In the previous chapters, we discussed the design of the BPΣΔM and the influence of nonideal characteristics. One of the main challenges in the high-frequency transmitter system is the design of high-efficiency linear power amplifiers. In this chapter we will briefly review an ideal high-efficiency switching-mode power amplifier (PA) design using the Class S amplifier with an H-bridge configuration. The H-bridge configuration is also known as an H-bridge power converter or a full-bridge converter [75, 76] in disciplines such as power electronics and we will use both of these terms interchangeably.

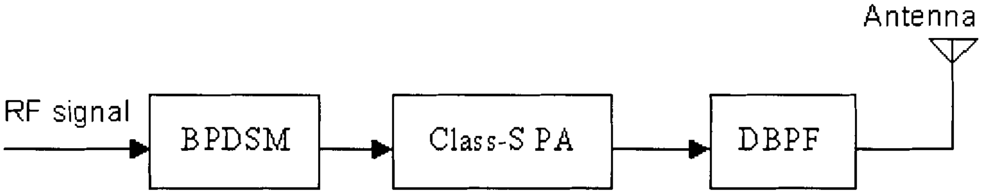


Figure 5-1 Schematic of a transmitter

Figures 1-3 and 5-1 illustrate the path of the RF signal through the transmitter system. The BPΣΔM encodes the RF input signal into a relatively low noise binary level square wave signal, which drives a switching-mode PA. The amplified signal then passes through the DBPF to remove the unwanted spectral components and converts the digital signal into an analog output signal. Finally, the signal is sent to the antenna. In this chapter, the PA is embedded within the BPΣΔM feedback loop to gauge the noise impacts of power supply noise on the system performance. The performance of the modelled system is then evaluated with a wide-band CDMA (WCDMA) signal.

5.1 Principle of the Class S PA with H Bridge-configuration

Amplifier circuits have traditionally been organized into "classes" in order to provide an easy way to describe their basic operation. Terms such as "class A" and "class AB" are well known and have been used for at least 50 years. The primary amplifier characteristics defining the "class" are the linearity and the efficiency. One type of amplifiers operates its output devices in its linear range. Another type of amplifiers uses its output devices as high-efficiency switches (saturation or pinch-off) rather than current sources. Class D, E and Class S are switching-mode power amplifiers. Class D and Class S amplifiers are often reversed or used interchangeably by some authors [73].

Switching-mode power amplifiers are also described as " digital power amplifiers" since they are operated in two-state: on and off, depending on the amplitude of the input pulse train. Thus they can amplify binary input signals.

Switching-mode power amplifiers are often used in circuits where linearity can be sacrificed for efficiency. Fortunately, the linearity can be improved by feeding a pulse-width modulated (PWM) signal and filtering after the switching-mode PA [73]. Meanwhile, for a bandpass sigma-delta input signal, the switching-mode PA is a linear stage for digital signals; the linearity of the filtered output is determined by the linearity of the BPΣΔM signal [3,4].

Figure 5-2 shows the ideal class S amplifier in an H Bridge-configuration, which consists of two half-bridge converters. With the same DC input voltage, the maximum output voltage of the H-bridge (full-bridge) converter is double that of the half-bridge converter. This implies that for the same power, the full-bridge carries half as much current as the half-bridge. Hence, at high power levels, it may be advantageous to select a full-bridge converter over a half-bridge converter to reduce the number of paralleled devices in the switch [76].

In Figure 5-2, the power supply is a fixed-magnitude DC voltage Vcc. The output of the PA is v_{AB} which can be controlled in magnitude as well as polarity. Similarly, the magnitude and the direction of the output current i_0 can be controlled. Therefore, this H Bridge-configuration PA can operate in all four quadrants of the i_0—v_{AB} plane [76] and the power flow through the converter can be in either direction.

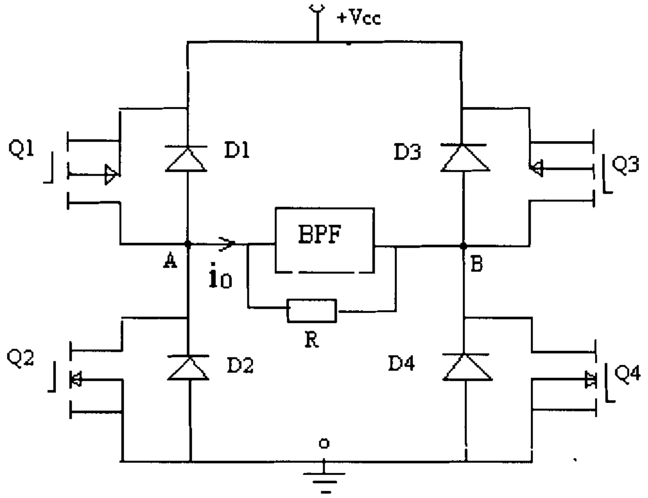


Figure 5-2 **Class S Amplifier with H Bridge-configuration**

The four diodes, D_1, D_2, D_3 and D_4, which are shunted with the switches Q_1, Q_2, Q_3 and Q_4, can provide a reverse current flow from spikes generated by charges accumulated in the output filter's capacitor and hence protect the switches.

When the binary signal is applied to Q_1 and Q_4 and has the proper polarity and amplitude, switches Q_1 and Q_4 conduct and act like low resistance switches allowing the drain current to flow into the filter and the load. The diodes D_1 and D_4 may or may not conduct a current depending on the direction of the output current i_0. In the mean time, the switches Q_2 and Q_3 are in the opposite status and in the off state. For ideal switches, when Q_1 and Q_4 are in the OFF state, Q_2 and Q_3 will be in the ON state. They are not off simultaneously in order for the output current i_0 to flow continuously.

Consider the output voltage v_{A0} in Figure 5-2. When Q_1 is on, the output current will flow through Q_1 to the load if i_0 is positive or it will flow through D_1 if i_0 is negative. In both cases the point A in Figure 5-2 is at the same potential which is equal to the positive DC input, and therefore

$$v_{AO} = V_{cc} \qquad (if\ Q_1\ is\ on\ and\ Q_2\ is\ off) \tag{5.1}$$

Similarly, when Q_2 is on, a negative i_0 will flow through Q_2 (since D_1 is reverse biased) and a positive i_0 will flow through D_2. Therefore

$$v_{AO} = 0 \qquad (if\ Q_2\ is\ on\ and\ Q_1\ is\ off) \tag{5.2}$$

Equations (5.1) and (5.2) show that v_{AO} depends only on the switch status and is independent of the direction of i_0. Hence, the average output voltage of V_{AO} over one switching period T_s, depends on the input voltage and the duty cycle of Q_1 (d_1):

$$V_{AO} = \frac{V_{cc}\,t_{ON} + 0 \cdot t_{OFF}}{T_s} = V_{CC} \cdot duty\ cycle\ of\ Q_1 = V_{CC} \cdot d_1 \tag{5.3}$$

Similarly applied to V_{BO}:

$$V_{BO} = V_{CC} \cdot duty\ cycle\ of\ Q_2 = V_{CC} \cdot (1 - d_1) = V_{CC}\, d_2 \tag{5.4}$$

Therefore, the output $\qquad V_{AB} = V_{AO} - V_{BO} = V_{cc}\,(2d_1 - 1) \qquad (5.5)$

The PA average output V_{AB} can be controlled by controlling the switch duty cycle and is independent of the magnitude and the direction of i_0. The waveforms are shown in Figure 5-3.

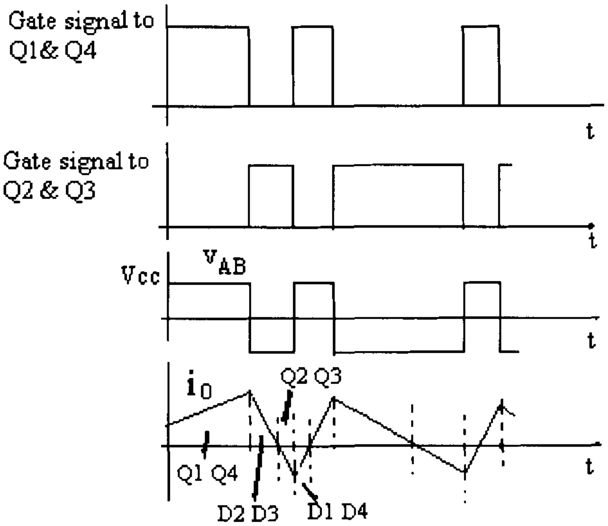


Figure 5-3 **Ideal voltage and current waveforms for an H-Bridge converter**

5.2 *Design of Differential Bandpass Filters (DBPF)*

A complete DBPF design is beyond the scope of this thesis, however, the simplest design procedure for our simulation is presented here as a reference.

Filtering the unwanted interference is required with virtually all solid-state RF PAs and especially those intended for radio communications. For WCDMA mode, a fifth order Chebyshev filter with 0.01dB ripple in the passband was applied in [79]. For GSM mode, a 5th-order Butterworth filter was found to meet the system requirement [80]. In this section, these two filter design procedures are given. As we known, BPF design is almost exclusively done with lowpass filters. We start our design with the conventional lowpass filter using the so-called normalized tables.

5.2.1 Lowpass Filter

There are two basic types of lowpass filters commonly used to suppress harmonics of the desired frequency in the RF output: the Butterworth and the Chebyshev filters.

The Butterworth filter is a medium-Q filter that exhibits a monotonic attenuation profile that is generally easy to implement. The frequency response of the Butterworth is the flattest passband response with no ripple. To achieve a steep attenuation transition from pass- to stop-band, a large number of components are needed. The Chebyshev filter is a high-Q filter that allows ripple in the passband. As more ripples are introduced, the initial slope at the beginning of the stopband is increased and produces a more rectangular attenuation curve when compared to the smoother Butterworth response [77].

The design of lowpass filters using tables of normalized element values and the attenuation curve provided in [77] is relatively straightforward. There are four steps involved.

1. To select the type of filter, one must define the desired responses such as passband ripple, attenuation slope, linear phase etc. Based on [79], we want 0.01dB in

the passband and thus we choose the Chebyshev filter.

2. Normalize the frequency f_i of interest by dividing it by the cutoff frequency f_c of the filter, based on the attenuation required at the desired frequency. Next, check the attenuation curves in [77] to find the filter order. Note that the 3dB point is when f_i/f_c is equal to 1. Step 1 and 2 can be processed at the same time.

3. Calculate the ratio between the source and the load impedance to find the related lowpass prototype normalized values in the table.

4. Scale all elements to the cutoff frequency and load impedance of the final design using the following formulas:

$$C=\frac{C_n}{2\pi f_c R_L} \tag{5.6}$$

$$L=\frac{L_n R_L}{2\pi f_c} \tag{5.7}$$

where C_n, L_n is the lowpass normalized capacitance, the inductance value in the table; f_c is the cutoff frequency; R_L is the load impedance value; C, L are the final capacitance, inductance values, respectively.

5.2.2 Bandpass Filter

BPF design is performed through a simple transformation process from the lowpass filter design.

In the lowpass filter design, the ratio of f_i/f_c is the horizontal axis of the attenuation curve. In the BPF design, the horizontal axis is the ratio of the bandwidth between the desired bandwidth BW and the 3dB bandwidth, BW_c, rather than the frequency ratio. Thus we have:

$$\frac{BW}{BWc}=\frac{fi}{fc} \tag{5.8}$$

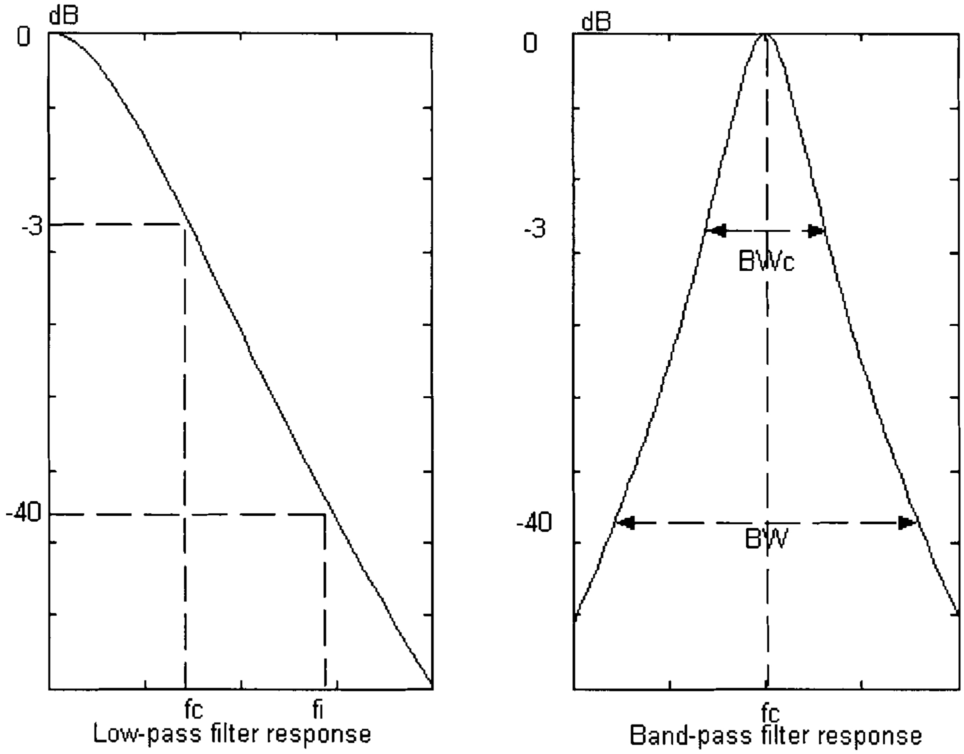


Figure 5-4 **Lowpass to bandpass filter transformation bandwidths**

We use the bandwidth ratio as the frequency ratio to find the related lowpass filter prototype. Then we resonate each lowpass element with the same value, that is all shunt elements of the lowpass filter become parallel-resonant elements, and all series elements become series-resonant elements. This procedure is illustrated in Figure 5-5.

Finally, we scale the normalized values to the real values using the following equations:

1. For the parallel-resonant branches 1and 3:

$$C=\frac{C_n}{2\pi R_L\, BW_c} \tag{5.9}$$

$$L=\frac{R_L\, BW_c}{2\pi f_c^2\, L_n} \tag{5.10}$$

2. For the series-resonant branch 2:

$$C = \frac{BW_c}{2\pi f_c^2 C_n R_L} \tag{5.11}$$

$$L = \frac{R_L L_n}{2\pi BW_c} \tag{5.12}$$

where, BW_c is the 3dB bandwidth of the BPF; R_L is the load impedance, f_c is the geometric center frequency of the BPF; L_n, C_n is the normalized inductance and capacitance bandpass element values.

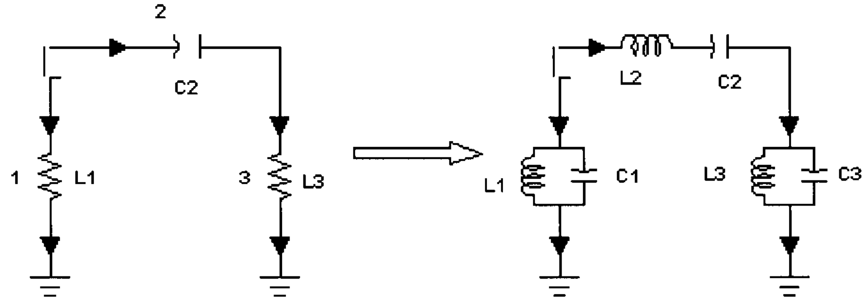


Figure 5-5 **Lowpass to bandpass circuit transformation**

5.2.3 Differential bandpass filter (DBPF)

In the previous section, we described the design of the single-ended BPF. Because the output of the H Bridge-configuration PA that we selected was a differential signal, we will implement a DBPF in the simulation. We have selected this filter because of its larger dynamic range and its ability to reject power-supply noise and clock feedthrough. It will, however, increase power and area requirements [84].

Based on the prototype in section 5.2.2, we can convert the unbalanced structure to the balanced structure implementing the following rules:

1) Divide the series inductor by 2 and multiply the series capacitor by 2, and, place the same value in the lower part, which is the ground return in the single-ended filter.

2) Keep the shunt element values unchanged.

The procedure is illustrated in Figure 5-6.

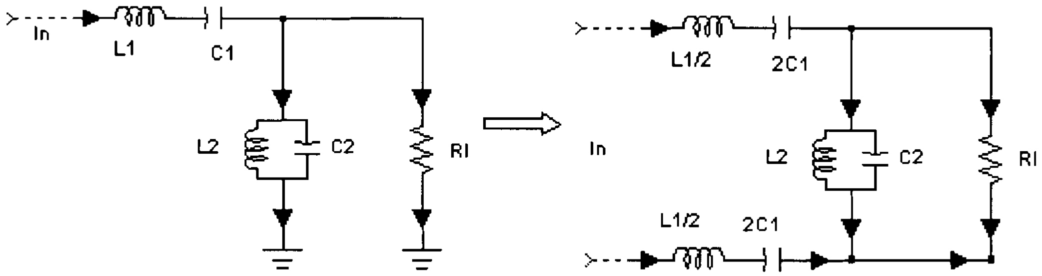


Figure 5-6 **The conversion from the single-ended to the differential filter**

5.2.3.1 Chebyshev Differential Bandpass Filter

Our target is the fifth-order Chebyshev filter with 0.01dB ripple in the passband, with the centre frequency being 2100MHz and the 3dB bandwidth being 20MHz. We have assumed the load impedance to be 10 ohms, and the source impedance is approaching zero. Thus the ratio between the source impedance and the load impedance is zero. We can directly check the lowpass normalized values table to yield the prototype circuit of Figure 5-7a, which is transformed into the bandpass prototype circuit of Figure 5-7b. Finally using Equation (5.9) through Equation (5.12), we obtain the final BPF that is shown in Figure 5-8 and the DBPF that is illustrated in Figure 5-9. The frequency response of the DBPF is plotted in Figure 5-10. The calculation is as follow:

$$L_1 = \frac{10\times 1.547}{2\pi\times 20\times 10^6} = 0.123uH \qquad C_1 = \frac{20\times 10^6}{2\pi\times\left(2100\times 10^6\right)^2\times 1.547\times 10} = 0.0467pF$$

$$L_2 = \frac{10\times 20\times 10^6}{2\pi\times\left(2100\times 10^6\right)^2\times 1.795} = 4.02\,pH \qquad C_2 = \frac{1.795}{2\pi\times 10\times 20\times 10^6} = 1.428nF$$

$$L_3 = \frac{10\times 1.645}{2\pi\times 20\times 10^6} = 0.262uH \qquad C_3 = \frac{20\times 10^6}{2\pi\times\left(2100\times 10^6\right)^2\times 1.645\times 10} = 0.0439pF$$

$$L_4 = \frac{10\times 20\times 10^6}{2\pi\times\left(2100\times 10^6\right)^2\times 1.237} = 5.84\,pH \qquad C_4 = \frac{1.237}{2\pi\times 10\times 20\times 10^6} = 0.98nF$$

$$L_5 = \frac{10\times 0.488}{2\pi\times 20\times 10^6} = 0.039uH \qquad C_5 = \frac{20\times 10^6}{2\pi\times\left(2100\times 10^6\right)^2\times 0.488\times 10} = 0.148pF$$

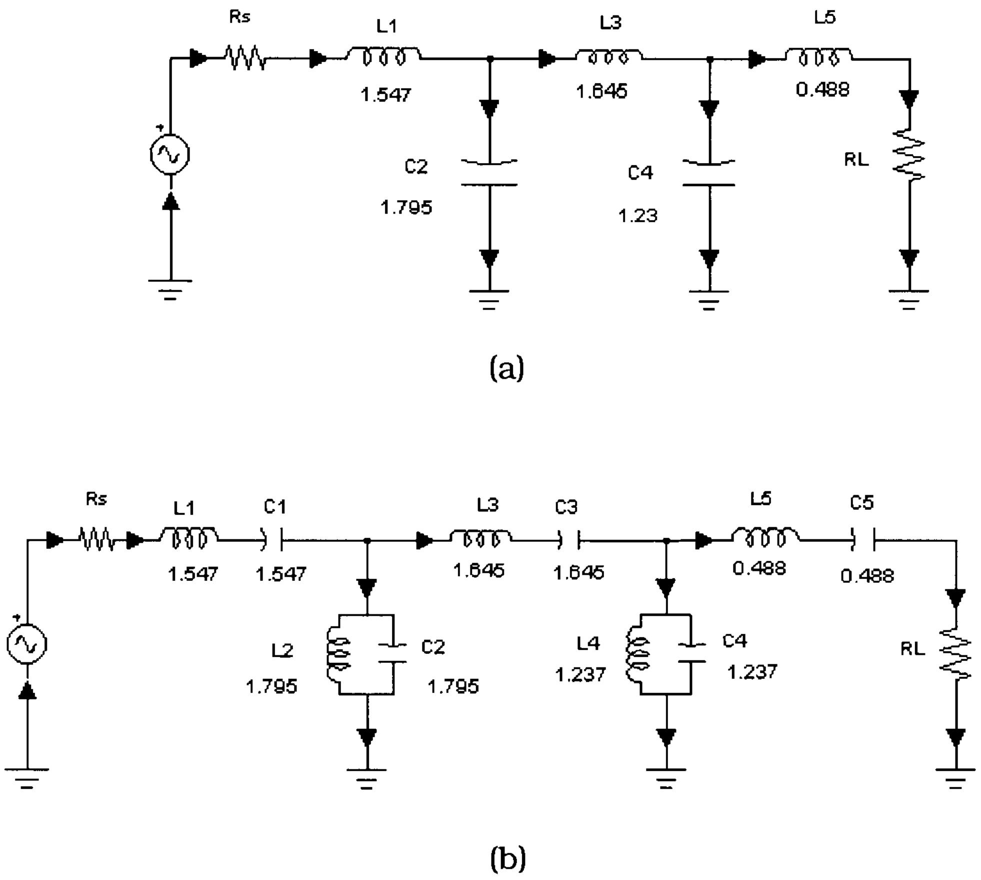


Figure 5-7 **(a)** **Normalized Chebyshev lowpass prototype circuit**
(b) **Normalized Chebyshev bandpass prototype circuit**

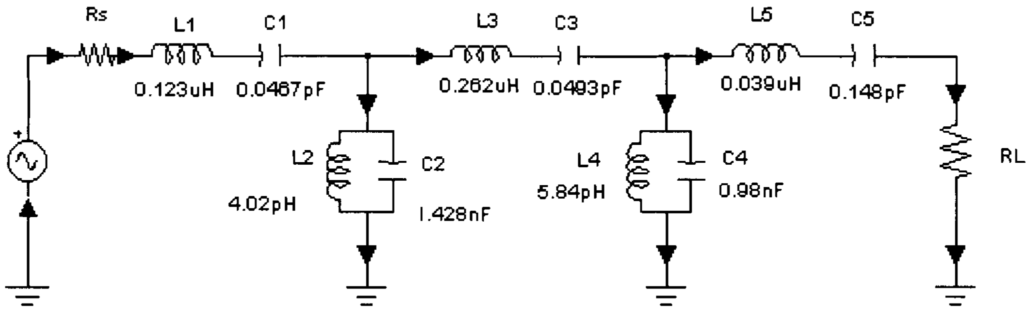


Figure 5-8 Final Chebyshev BPF circuit

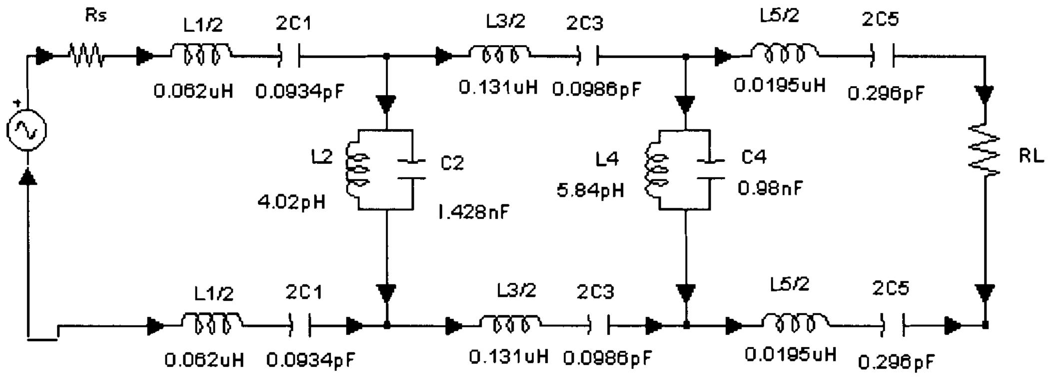


Figure 5-9 Chebyshev DBPF

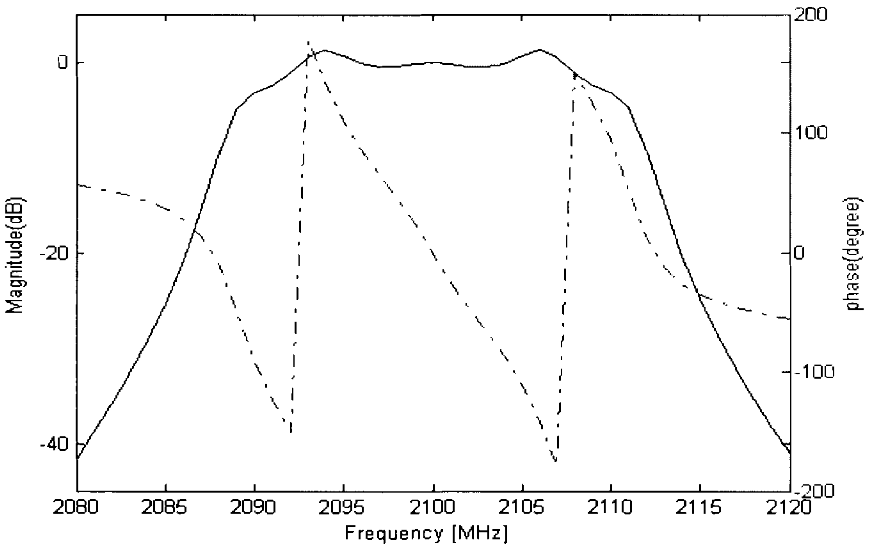


Figure 5-10 Frequency response of the Chebyshev DBPF

5.2.3.2 Butterworth Differential Bandpass Filter

Similarly, we can use the same procedure as the Chebyshev DBPF to design the fifth-order Butterworth DBPF where the center frequency is 840MHz and 3dB bandwidth is 20MHz. We use the Butterworth lowpass filter normalized values from a table to obtain the five normalized values as follow:

$\{ L_1 , C_2 , L_3 , C_4 , L_5 \} = \{ 1.545, 1.694, 1.382, 0.894, 0.309 \}$.

Transforming the lowpass to the bandpass filter and scaling to the final values, we obtain the following values:

$$L_1 = \frac{10\times 1.545}{2\pi\times 20\times 10^6} = 0.123uH \qquad C_1 = \frac{20\times 10^6}{2\pi\times\left(840\times 10^6\right)^2\times 1.545\times 10} = 0.292pF$$

$$L_2 = \frac{10\times 20\times 10^6}{2\pi\times\left(840\times 10^6\right)^2\times 1.694} = 26.63\,pH \qquad C_2 = \frac{1.694}{2\pi\times 10\times 20\times 10^6} = 1.348nF$$

$$L_3 = \frac{10\times 1.382}{2\pi\times 20\times 10^6} = 0.11uH \qquad C_3 = \frac{20\times 10^6}{2\pi\times\left(840\times 10^6\right)^2\times 1.382\times 10} = 0.326pF$$

$$L_4 = \frac{10\times 20\times 10^6}{2\pi\times\left(840\times 10^6\right)^2\times 0.894} = 50.46\,pH \qquad C_4 = \frac{0.894}{2\pi\times 10\times 20\times 10^6} = 0.71nF$$

$$L_5 = \frac{10\times 0.309}{2\pi\times 20\times 10^6} = 0.025uH \qquad C_5 = \frac{20\times 10^6}{2\pi\times\left(840\times 10^6\right)^2\times 0.309\times 10} = 1.46pF$$

The final differential Butterworth BPF is illustrated in Figure 5-11. The frequency response is show in Figure 5-12.

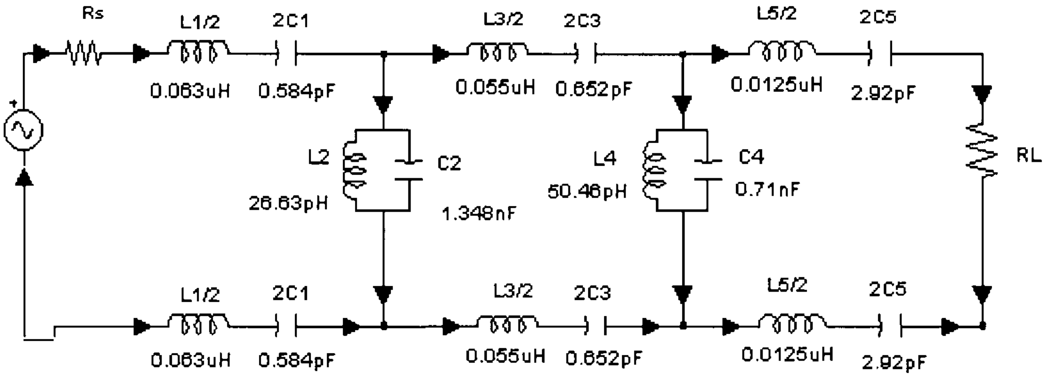


Figure 5-11 Butterworth DBPF

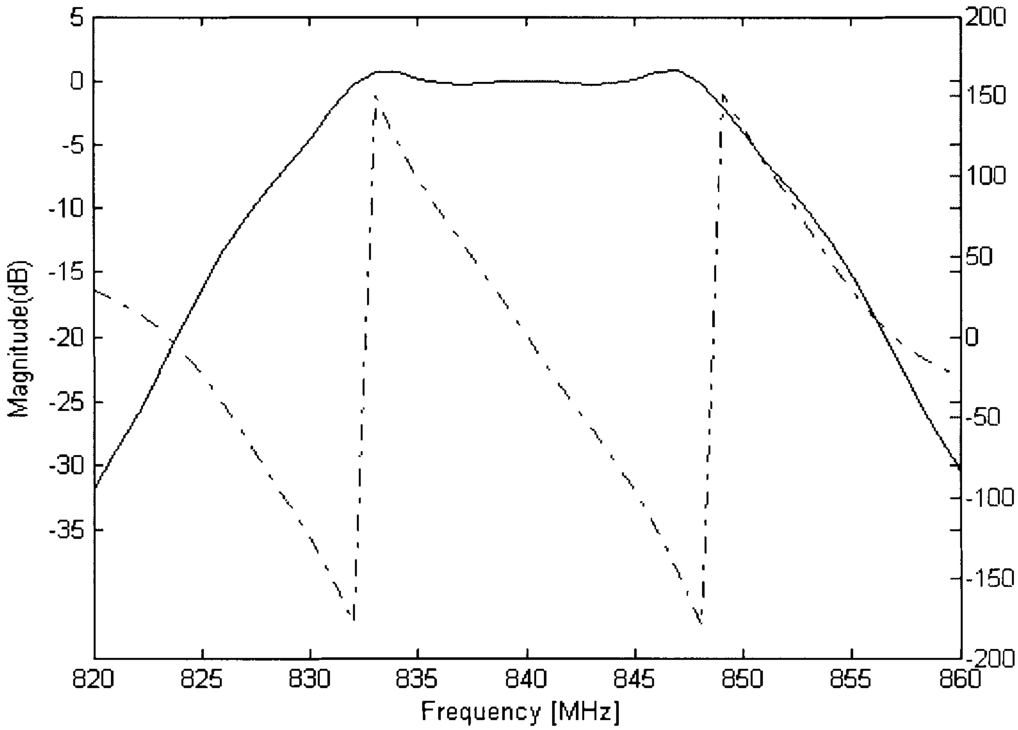


Figure 5-12 Frequency response of the Butterworth DBPF

5.3 Simulation Results of the CT BPΣΔM with the PA and DBPF

5.3.1 The Ideal Case

The ideal case is illustrated in Figure 5-13. This case is shown by feeding two tones with 5MHz spacing and a 2100 MHz centre frequency into the ideal $f_s/4$ CTBPΣΔM (using the coefficients of Equation (3.24)) with a Class S amplifier in a H Bridge-configuration and a DBPF.

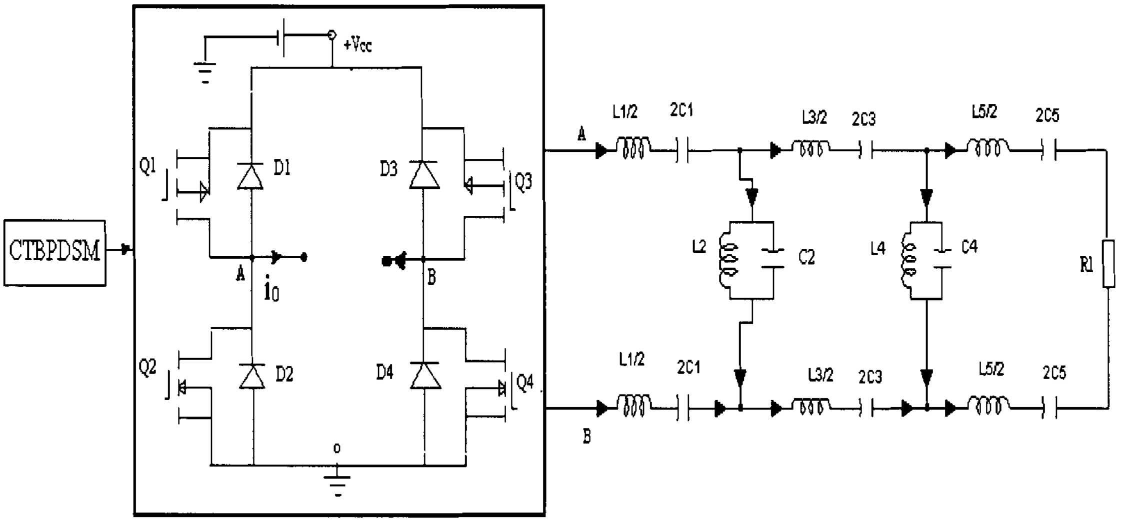


Figure 5-13 The system schema of a CTBPΣΔM with the PA and DBPF

In the ideal switch, we assume the on-resistance is 0.01ohm. Using the scheme shown in Figure 5-13, the highest efficiency is obtained when the load resistance is approximately 10 ohms, which is shown in Figure 5-14.

The input and output waveforms and spectrums for an $f_s/4$ structure are illustrated in Figure 5-15. For the $f_s/10$ architecture, we chose 1.8 as the gain of NTF and the optimized coefficients shown in Equation (3.22). The simulation result is illustrated in Figure 5-16. The comparison of the performance of the two architectures is listed in Table 5-1. The two configurations have similar performance.

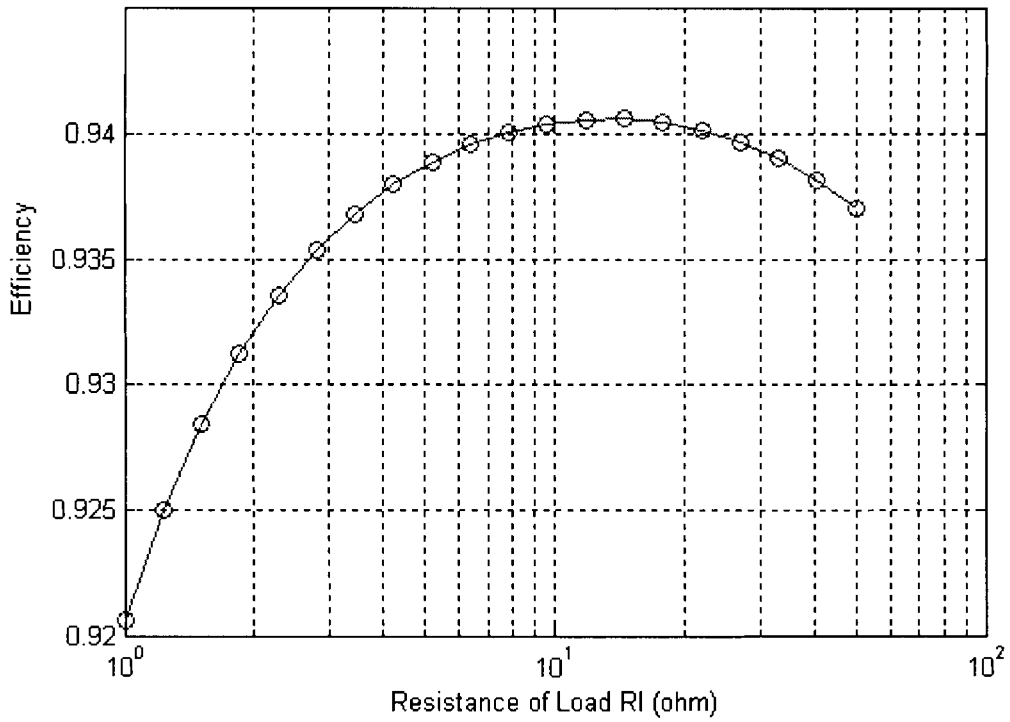


Figure 5-14 **Efficiency vs. Resistance of the load**

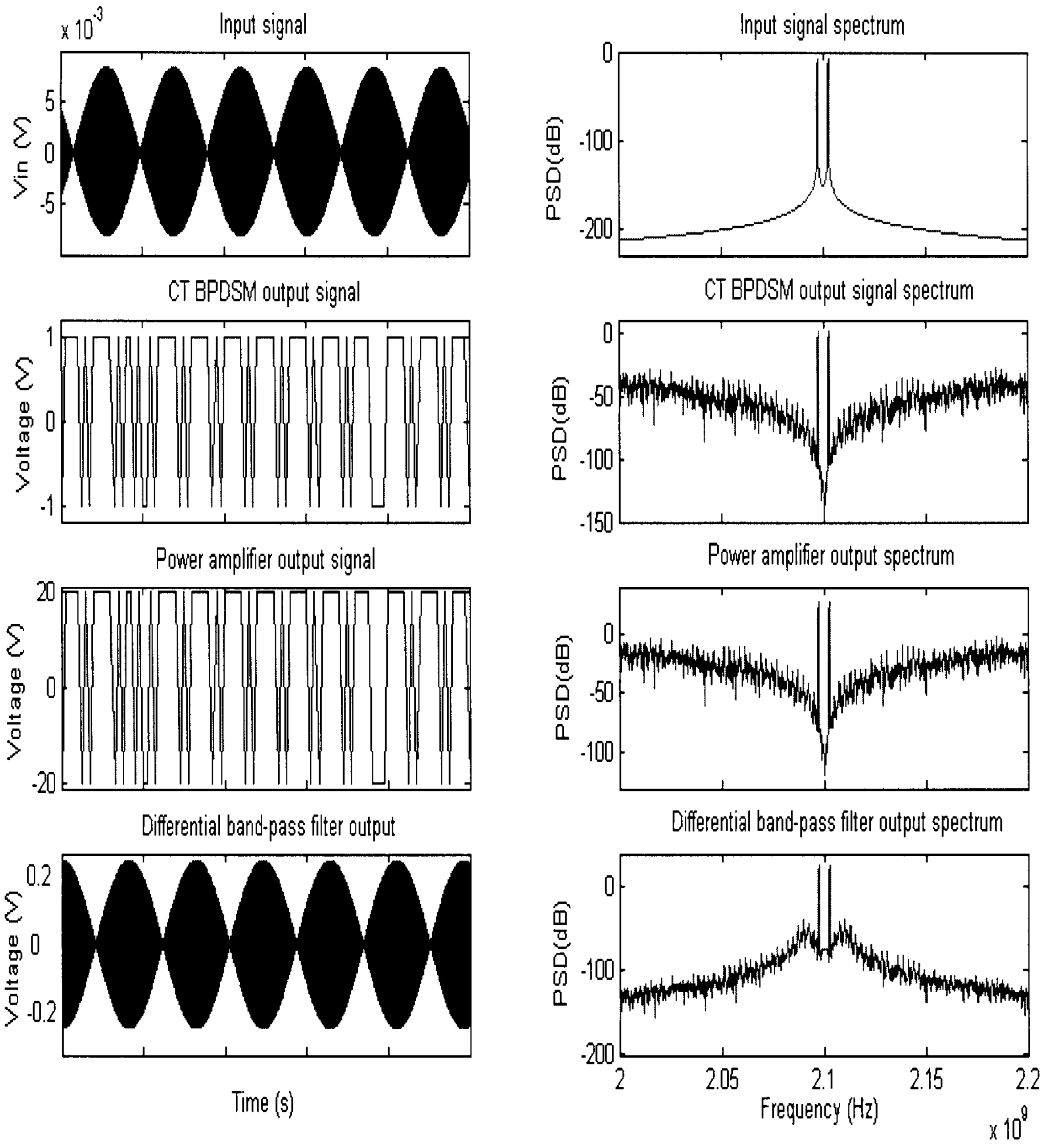


Figure 5-15 Simulation results for an $f_s/4$ CTBPΣΔM with the PA and DBPF

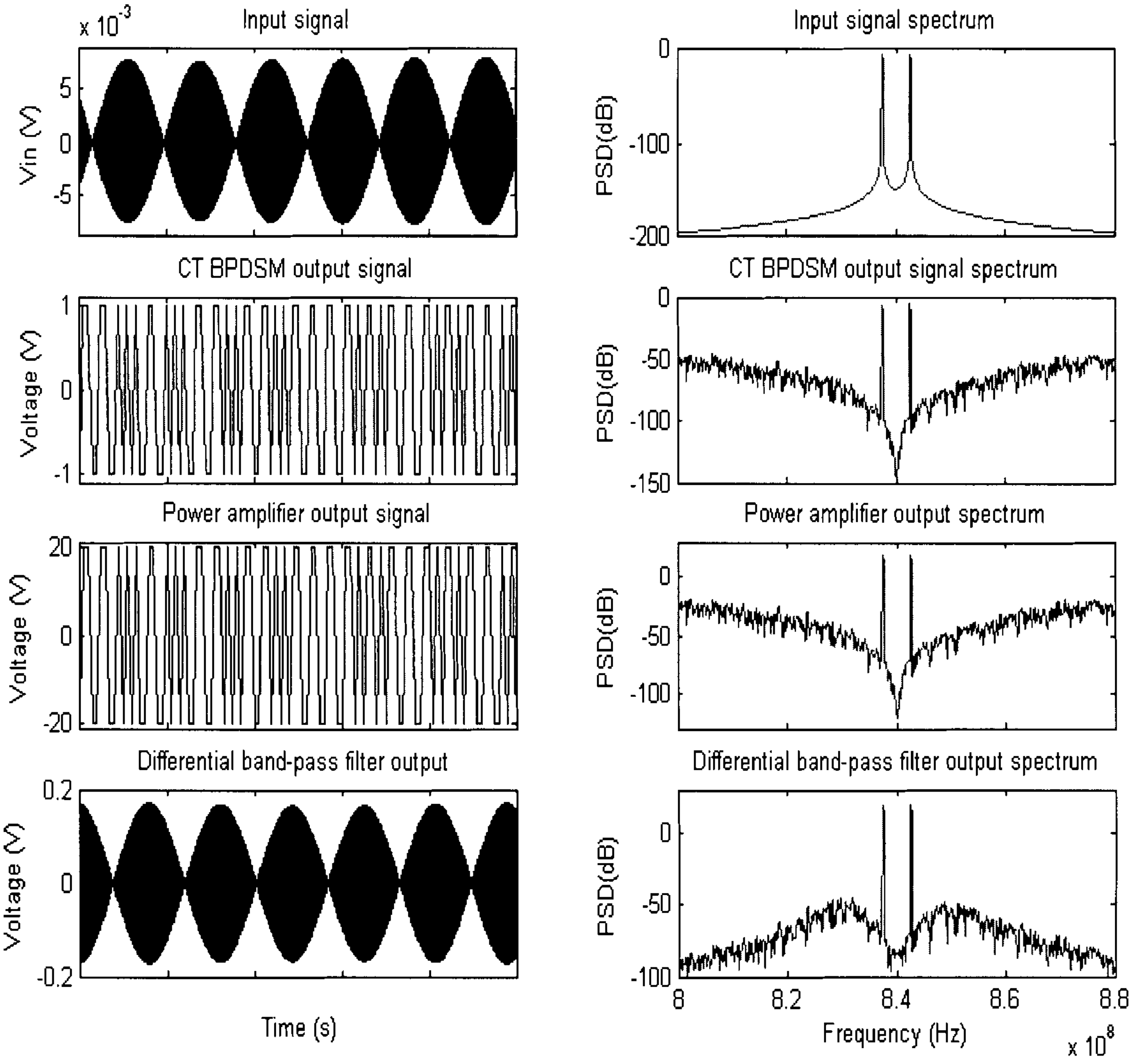


Figure 5-16 **Simulation results for an $f_s/10$ CTBPΣΔM with the PA and DBPF**

Output	**$f_s/4$, Chebyshev DBPF**		**$f_s/10$, Butterworth DPPF**	
	SNDR(dB)	**SFDR(dB)**	**SNDR(dB)**	**SFDR(dB)**
CTBPΣΔM Output	59.52	66.29	57.70	70.51
DBPF Output	60.72	66.13	58.52	69.92

Table 5-1 **Performance of $f_s/4$ and $f_s/10$ CT BPΣΔMs**

5.3.2 EMI Noise in the Power Amplifier

In the high-speed switch, the EMI noise generated by the voltage fluctuations is very critical to the signal to noise ratio. Using sigma-delta modulation this kind of noise will be attenuated more compared to the conventional pulse-width modulation (PWM). Due to the property of sigma-delta, the shortest pulse can last T_s seconds, the largest pulse train can be several times T_S. This means the output signal can not change between a sample and the next sample, thus the switching operation is not necessary. This implies that the switching number is less than the fixed time conventional PWM signal.

The simplest model of the EMI is built in this section as a random Gaussian noise with zero mean, which is added to the DC power supply. Suppressing the EMI noise with noise cancellers, filter circuits and packaging methods, is a popular topic and these methods were applied in [81, 82, 83]. Placing the PA after the quantizer, yet inside the BPΣΔM loop is investigated in this section. For consistency, we have placed a constant block between the PA and the BPΣΔM. The constant is the reciprocal of the PA gain. Based on the concept of the linear model we discussed in Chapter 2, the noise, which is independent of the signal after the quantizer, can be shaped away by the sigma-delta loop structure. Figure 5-17 is the original model we used in this simulation. The modified model is shown in Figure 5-18 where PA is placed inside the CT BPΣΔM loop.

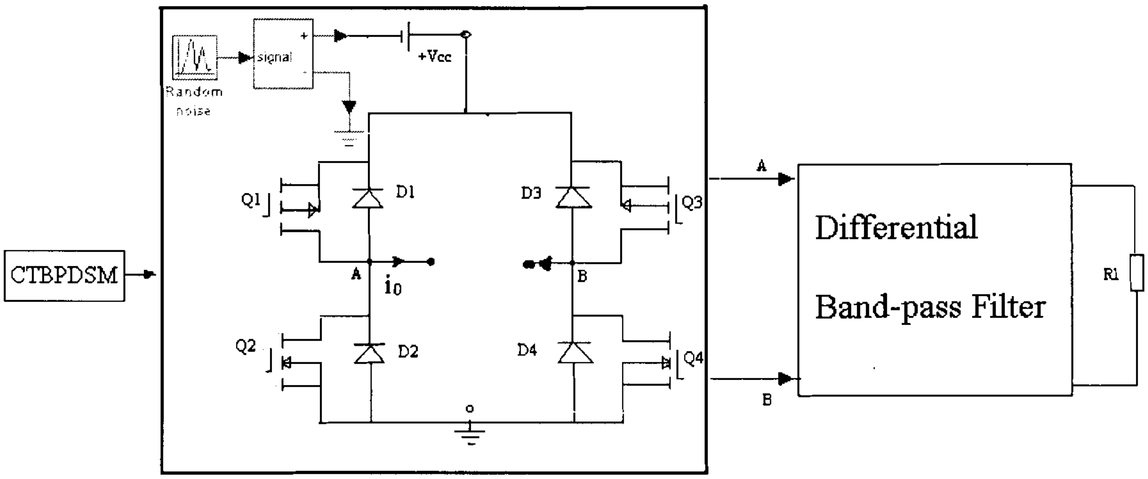


Figure 5-17 EMI noise model

The simulation results are listed in Table 5-2 for the $f_s/4$ structure with 2100 MHz centre frequency and a fifth-order, 0.01dB ripple Chebyshev BPF. From the results, we have found that putting the PA inside the BPΣΔM loop will slightly improve the signal to noise ratio and reduce the intermodulation distortion. The reason for this is that the random noise is independent of the input signal. We can consider it as a dither signal which can break up tone structures including overload and idle channel tones, therefore producing a whiten power spectrum output, a more linear dependence of the SNR versus the signal power, and an improvement in the dynamic range [9]. However, this analysis does not apply to the $f_s/10$ structure at 840 MHz. In Table 5-3, the result is different. Placing the PA inside the loop degrades the system performance. The reason for this is that the spectrum of $f_s/10$ is not symmetrical. Thus the quantization noise cannot be whitened and degrades further.

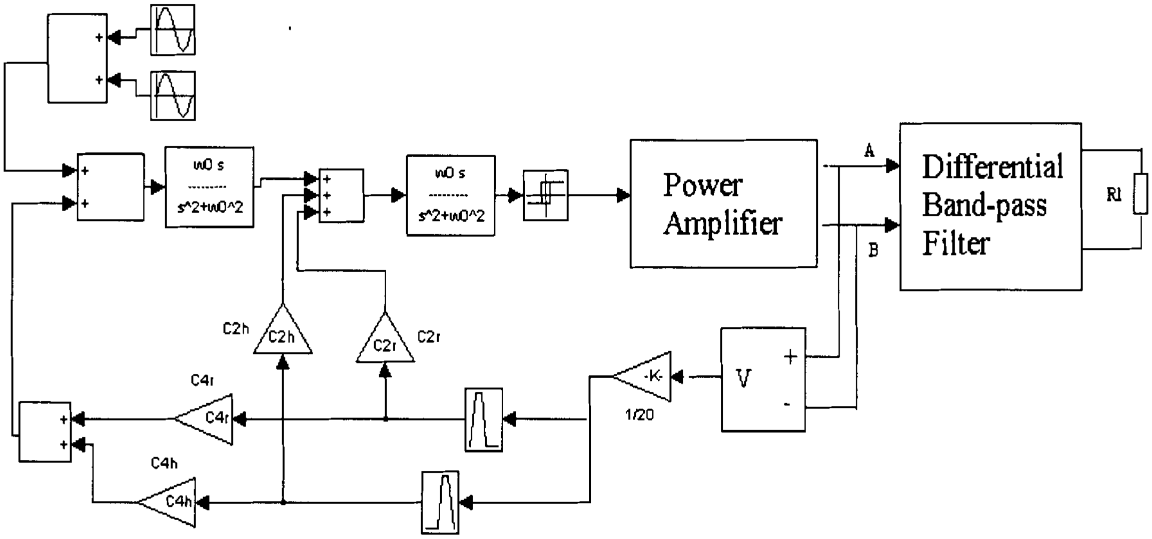


Figure 5-18 PA inside the BPΣΔM loop

EMI noise variance	Regular design		PA inside the loop	
	SNDR(dB)	SFDR(dB)	SNDR(dB)	SFDR(dB)
0.5e-5	59.31	65.60	60.74	72.73
0.5e-4	53.61	63.23	54.28	67.13
0.5e-3	44.04	59.15	44.71	61.20

Table 5-2 Performance of the $f_s/4$ CTBPΣΔM with EMI noise

EMI noise variance	Regular design		PA inside the loop	
	SNDR(dB)	SFDR(dB)	SNDR(dB)	SFDR(dB)
0.5e-5	55.68	66.45	47.36	63.85
0.5e-4	48.41	61.58	38.63	50.80
0.5e-3	38.87	50.95	28.73	41.07

Table 5-3 Performance of the $f_s/10$ CTBPΣΔM with EMI noise

5.3.3 Simulation Results of WCDMA Signals

In the third generation cellular standards, there is a significantly wider channel bandwidth required than with the previous systems. The input of the $\Sigma\Delta M$ is typically narrowband, but in this section we will feed a single-carrier and a four-carrier wideband CDMA signal with a channel bandwidth of 5MHz into the $f_s/4$ ideal system. The simulation results are show in Figure 5-19, 5-20 respectively.

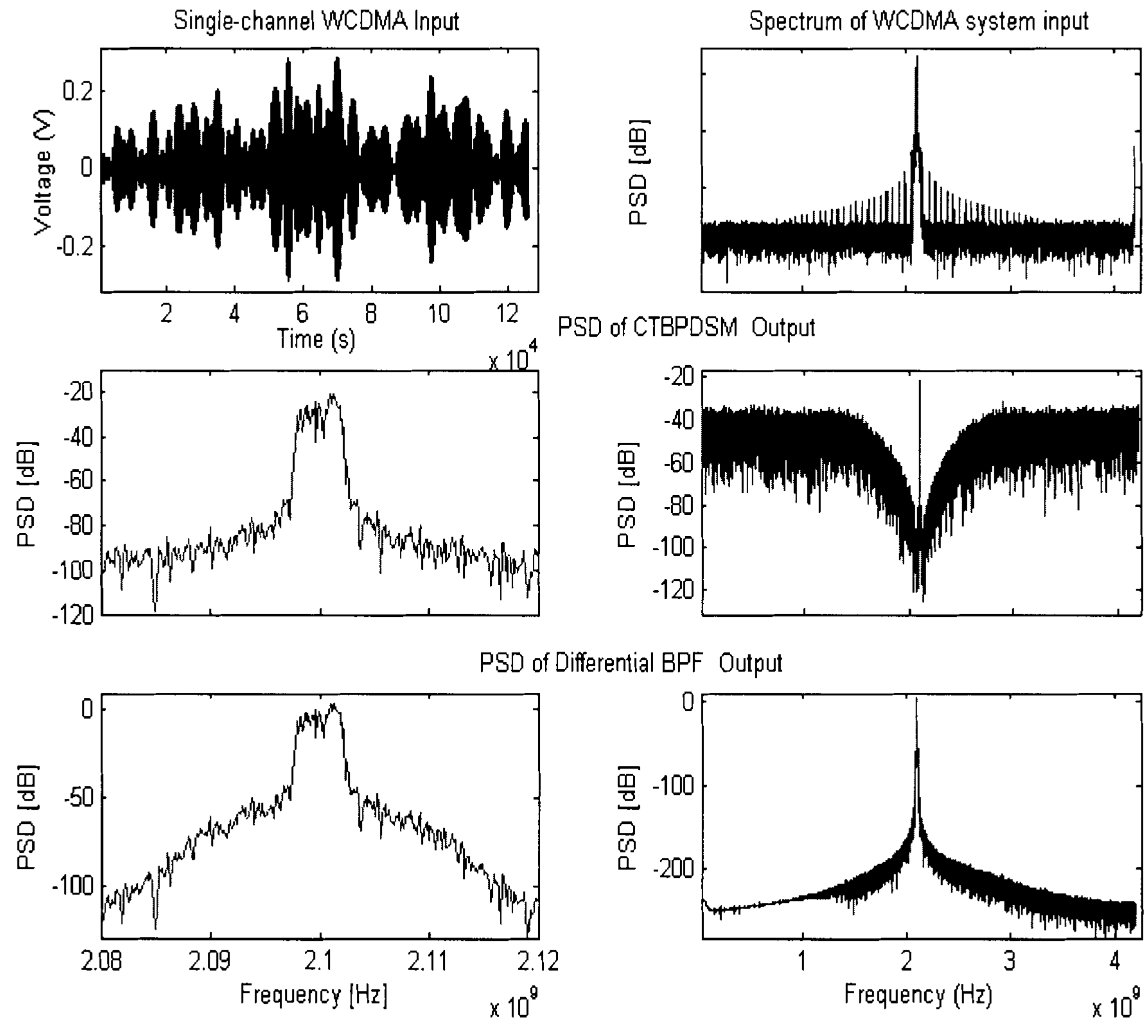


Figure 5-19 Simulation results for a single-channel WCDMA signal

From the simulation results, the ΣΔM is shown to be capable of modulating wideband signals. With the noise shaping and suitable bandpass channel filter, the distortion can be suppressed and the performance can be improved.

In this chapter, the ideal Class S amplifier in a H Bridge-configuration was described. The DBPF was simulated. The simple EMI model was developed and the modified structure where the PA was embedded within the BPΣΔM loop for improving the system performance was built. The wideband CDMA signal being fed into the system was investigated.

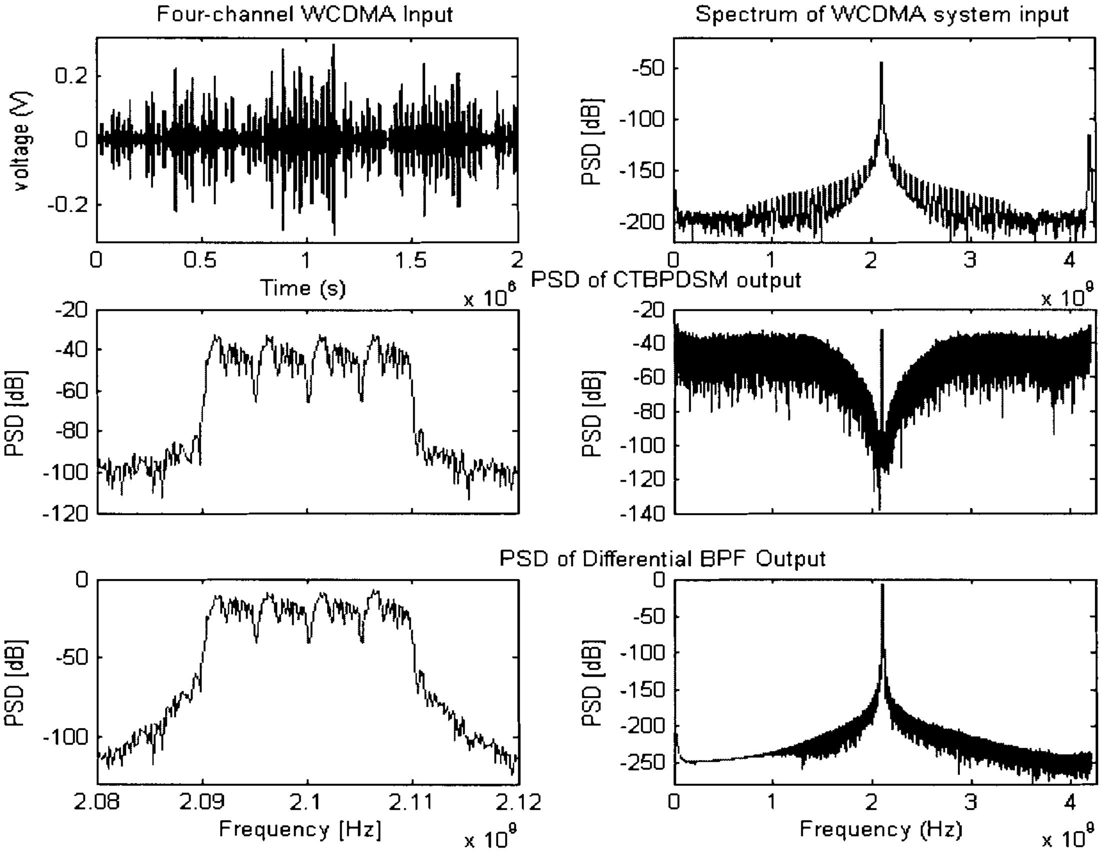


Figure 5-20 Simulation results for a four-channel WCDMA signal

Chapter 6

Conclusions

6.1 Summary

Sigma-delta modulation has proven to be an effective means of implementing high-resolution ADCs. In this thesis, the ideal behavioural model built in MATLAB SIMULINK was demonstrated. It was shown that one could make a continuous-time sigma-delta loop filter, such that the behaviour of both discrete-time equivalent and continuous-time sigma-delta loops, would be identical. With the combination of two pulses, return-to-zero (RZ) and half-to-return-to-zero (HRZ), the ideal continuous-time fourth order bandpass loop transfer function is provided. The four pulse feedback coefficients guarantee a sufficient number of parameters for implementing any arbitrary loop transfer function. With this multi-feedback structure, the methodology for designing the multi-band fourth order CT BPΣΔM was proposed. This architecture has the potential for integration with the circuitry associated with an RF transmitter into a single DSP based IC and it can be used together with a switching mode amplifier such as Class S PA and an analog filter.

Nonideal elements associated with the implementations of CT BPΣΔM were investigated. A non-linearity analysis framework was developed to accommodate a wide range of non-linear effects that occur in modulators. To avoid unnecessary nonideal characteristics, a careful layout and good circuit topology is recommended.

Using the oversampled noise shaping property of ΣΔM to overcome the noise presented in the PA was discussed by embedding the PA within the feedback loop.

6.2 Future Research Topics

As in the case of nearly all research studies, certain aspects of this research topic remain unexplored and many questions remain unanswered. Further discussion and research can be explored on topics such as designing an optimized loop-filter for a $\Sigma\Delta$M to improve its noise factor, dynamic-range, linearity, power consumption, reliability and higher frequency operation.

Higher order $\Sigma\Delta$Ms, alleviating the high-speed clock requirement, offer the potential of increased resolution and enhanced suppression of both in-band noise and in-band tones since this allows a higher attainable in-band loop gain. However, modulators with more than two integrators suffer from potential instability owing to the accumulation of large signals in the integrators [66,67]. Also, higher loop gain will leads to high non-linearity.

Using a multi-bit quantizer, the feedback and input signals cancel each other better than in the case of a single-bit feedback signal. However, due to mismatch between the quantization step-size, a multi-bit quantizer is non-linear and introduces harmonic distortion itself. In the transmitter system, using a multi-bit quantizer will require high-efficiency power amplifier that can amplify the multi-level signal instead of the simple on and off signal, which will increase the complexity of the PA.

To date, most analysis is based on the linear model of quantizer, which gives an estimate of the SNR that is sufficient for use with a first design iteration and makes it convenient to use a filter approximation for the basic design. However, the linear model neither guarantees stability nor allows an exact prediction of the input signal level that achieves the maximum SNR. Therefore, stability analysis continues to be a central research issue for these modulators.

How to design a tuning algorithm for a high speed CT $\Sigma\Delta$M to maximize DR that works on-chip, perhaps while the modulator is operating, is an interesting topic for future research.

Appendix A

MATLAB Codes for Calculating Four Coefficients of the Fourth Order CT BPΣM

```matlab
function [c2r,c4r,c2h,c4h]= CT4ordercoef(Fcsratio, Hnum, delay)

% According to the structure of fc/fs, and the excess-loop delay
to obtain four coefficients of the CT BPΣΔM.

%Fcsratio is the ratio between the centre frequency fc and the
sampling frequency fs.

%Hnum is the numerator of the loop filter transferfunction

%delay is the excess-loop delay

        alfa=delay;

        beta=delay+0.5;

%       zeros of the NTF

        Zntf=2*pi* Fcsratio;

%       Make second-order NRZ system

        [a2, b2, c2,d2]=tf2ss([0 Zntf 0],[1 0 Zntf*Zntf]);

%       Build the continuous time state-space model

        sysc2=ss(a2,b2,c2,d2);

%       Transfer to discrete domain state-space model, Ts=1

        sysd2n=c2d(sysc2,1);

%       Find a RZ system in the discrete domain

        sysd2r=sysd2n;

%       Calculate the Matrix B using Equation (3.12)

        sysd2r.b=inv(sysc2.a)*(expm(sysc2.a*(1-alfa))-
expm(sysc2.a*(1-beta)))*sysc2.b;

%       Find an HRZ system in the discrete domain
```

```
     sysd2h=sysd2n;

     sysd2h.b=inv(sysc2.a)*(expm(sysc2.a*(1-beta))-
eye(size(sysc2.a)))*sysc2.b + inv(sysc2.a)*(expm(sysc2.a)-
expm(sysc2.a*(1-alfa)))*sysc2.b   ;

%    Common denominator

     z1coef=2*cos(Zntf);

     tf2=tf([1 -z1coef 1],[1 -z1coef 1],1);% Ts=1

     tfd2r=tf(sysd2r)*tf2;

     tfd2h=tf(sysd2h)*tf2;

%    Make the 4th-order NRZ system

     [a4, b4, c4,d4]=tf2ss([0 0 Zntf^2 0 0],[1 0 2*Zntf*Zntf 0
Zntf^4]);

%    Build continuous time state-space model

     sysc4=ss(a4,b4,c4,d4);

%    Transfer to discrete domain state-space model, Ts=1

     sysd4n=c2d(sysc4,1);

%    Find RZ system in the discrete domain

     sysd4r=sysd4n;

     sysd4r.b=inv(sysc4.a)*(expm(sysc4.a*(1-alfa))-
expm(sysc4.a*(1-beta)))*sysc4.b;

%    Find an HRZ system in the discrete domain

     sysd4h=sysd4n;

     sysd4h.b=inv(sysc4.a)*(expm(sysc4.a*(1-beta))-
eye(size(sysc4.a)))*sysc4.b + inv(sysc4.a)*(expm(sysc4.a)-
expm(sysc4.a*(1-alfa)))*sysc4.b

%    Find the 4th-order transfer functions

     tfd4r=tf(sysd4r);

     tfd4h=tf(sysd4h);

%    Extract the numerator of the loop filter

     Hcoef=Hnum(2:5)';

     nummatrix=zeros(4,4);
```

```
%      Building the numerator matrix

       nums=tfd2r.num{:};    nummatrix(:,1)=nums(2:5)';

       nums=tfd2h.num{:};    nummatrix(:,2)=nums(2:5)';

       nums=tfd4r.num{:};    nummatrix(:,3)=nums(2:5)';

       nums=tfd4h.num{:};    nummatrix(:,4)=nums(2:5)';

%      Solve for four feedback coefficients

       feedcoefs=nummatrix\Hcoef

       c2r= feedcoefs (1);

       c2h= feedcoefs (2);

       c4r= feedcoefs (3);

       c4h= feedcoefs (4);
```

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