Hardware Platform Design for Validation of PMC-Sierra S/UNI® MULTI-48™

By:
Arash Haidari-Khabbaz

PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF ENGINEERING
in the School
of
Engineering Science

SIMON FRASER UNIVERSITY

Spring 2005

APPROVAL

Name:	Arash Haidari-Khabbaz
Degree:	Master of Engineering
Title of Project:	Hardware Platform Design for Validation of PMC-Sierra S/UNI® MULTI-48™

Examining Committee:

Chair:	Dr. Andrew Rawicz Professor of the School of Engineering Science Faculty of Applied Science Simon Fraser University
Senior Supervisor	Dr. Ash M. Parameswaran Professor of the School of Engineering Science Faculty of Applied Science Simon Fraser University
Supervisor	Randy Hughes Manager, System Validation Design PMC-Sierra Inc.

Date Defended/Approved: January 26, 2005

SIMON FRASER UNIVERSITY

PARTIAL COPYRIGHT LICENCE

ABSTRACT

This document is a report on the design of hardware platform for the validation of PMC-Sierra's S/UNI® MULTI-48™. The purpose of the engineering validation hardware system design is to provide a platform upon which to evaluate the quality and functionality of the device under test. The general platform requirements are:

- Support the execution the S/UNI® MULTI-48™ feature test plan.
- Fulfill product validation requirements for all points controllable and accessible.
- Furnish the power-supply requirements of the S/UNI® MULTI-48™ device by segregate power planes, and providing low-noise and quite supply where required.
- Permit independent external control of all device power rails. Support product engineering's requirements for power-supply noise injection
- System clock domains must be capable of being driven synchronous as well as asynchronously from both on and off-board sources.
- Support high quality signal integrity for multi Gigahertz signals.

This report describes the design of a hardware platform that supports the above mentioned requirements for the validation of PMC Sierra's S/UNI® MULTI-48™ device. It describes the challenges and the techniques that are used to overcome those challenges.

ACKNOWLEDGEMENTS

I would like to thank the following people for their support and contributions on this project:

- Dr. Ash M. Parameswaran
- Randy Hughes
- Tianyu Zhang
- Richard Stewart
- Mounir Youssef
- Mike Zieglmeier
- Rod Zavari
- David Garau

TABLE OF CONTENT

Approval ii

Abstract iii

Acknowledgements iv

Table of Content v

List of Figures vii

List of Tables ix

Abbreviation x

Introduction 1

Device Features and Application 3

Device Application Examples 6

Device Block Diagram and Various Loopback Modes 9

Hardware Platform 13

Compact PCI *18*

Single Board Computer (SBC) *18*

Clock Distribution 20

SONET Line Interface 25

1X2488 ..... *26*

4x622 ..... *26*

4x155 ..... *27*

Mix of 622 and 155 ..... *27*

Automatic Protect Switching (APS) LVDS serial interface 28

System Side Interface 29

FPGA (XILINX XCV1000E) for SONET overhead insertion/extraction 31

EVB Board Support 32

Power Supply and Decoupling *32*

Reset Circuit *37*

CPLD (XILINX XC95288XLPQ208) *38*

LEDs *38*

JTAG *39*

Adapters, Interface Cards, Backplanes *39*

SIGNAL Integrity 42

Serial High-Speed Line Interface *42*

Clock Termination Circuits *44*

Project Contributions and Schedule 49

Conclusion 50

References 51

LIST OF FIGURES

Figure 1: Multi-rate ATM Switch Port Application [1] 6

Figure 2 Multi-Rate IP Switch Port Application [1] 7

Figure 3 APS Protection Application [1] 8

Figure 4 Block Diagram [1] 9

Figure 5 Serial Diagnostic Loopback [1] 10

Figure 6 Parallel Diagnostic Loopback [1] 10

Figure 7 Line Loopback [1] 11

Figure 8 APS Protection Configuration [1] 11

Figure 9 APS Working Configuration [1] 12

Figure 10 Cell/Packet Loopback [1] 12

Figure 11 S/UNI® MULTI-48™ EVB Placement Diagram 15

Figure 12 S/UNI® MULTI-48™ EVB Block Diagram 16

Figure 13 Finished S/UNI® MULTI-48™ Evaluation Board 17

Figure 14 nanoEngine from Bright Star Engineering 19

Figure 15 PMC-Sierra MIPS processor based Single Board Computer 19

Figure 16 155.52/77.76 REFCLK Clock Distributions 22

Figure 17 77.76 MHz SYSCLK Clock Distributions 23

Figure 18 UL3/PL3 Interface Clock Distributions 24

Figure 19 Single Form Factor Pluggable (SFP) Optical Module 25

Figure 20 Layout of S/UNI® MULTI-48™ to SFP optical modules 26

Figure 21 60 position HS3 Backplane Connector used for APS port 28

Figure 22 Transmit and Receive PL3 and UL3 HS3 connectors 29

Figure 23 3.3V and 1.8V Power Distribution Circuit 35

Figure 24 Recommended Analog Power Filtering 36

Figure 25 Recommended APS Analog Power Filtering 37

Figure 26 Looptime PLL Board Block Diagram 40

Figure 27 Assembled Looptime PLL Board 41

Figure 28 Layout of the Top Layer High-Speed Line Interface Traces 43

Figure 29 Waveforms of Differential PECL Signal 44

Figure 30 Thevenin Equivalent Transformation 46

Figure 31 AC Coupling Termination without V_{BB} Pin 48

Figure 32 AC Coupling Termination with VBB Pin 48

LIST OF TABLES

Table 1 Clock Domains 20

Table 2 Transmit PL3 and UL3 HS3 connectors 29

Table 3 Receive PL3 and UL3 HS3 connectors 30

Table 4 Power Consumption and Decoupling Worksheet 32

Table 5 S/UNI® MULTI-48™ Analog Power-Supply Filtering Recommendations 34

ABBREVIATION

DUT	Device Under Test
SONET	Synchronous Optical Network
SDH	Synchronous Digital Hierarchy
PL3	POS PHY™ Level 3
UL3	Utopia Level 3
APS	Automatic Protect Switch
S/UNI®	SATURN User Network
EVB	Engineering Validation Board
FTP	Feature Test Plan describing the tests and expected results for verifying a device
SBC	Single Board Computer
SEEPROM	Serial Electronically Erasable Programmable Read Only Memory
PECL	Positive-referenced Emitter Coupled Logic
SFP	Single Form Factor Pluggable
IBIS	I/O Buffer Information Specification
PLL	Phase Lock Loop

INTRODUCTION

The high level of competition in today's telecommunication market has led the equipment manufacturers to redesign their systems in order to decrease power, reduce cost, increase efficiency while providing more flexibility and supporting higher bandwidth. To achieve these objectives the equipment manufacturers demand the silicon and chipmaker companies to walk down the same path. Consequently, companies like PMC-Sierra continuously develop new devices that include a subset of previous generation devices and a set of new requirements for their target market. This trend has resulted in an increase of device gate count from thousands of gates to millions of gates during the past 7 years.

A multi million-gate device is a device that supports many modes of operation and is fit for numerous applications. There can be hundreds of features that are supported by such a device and it can have thousands of registers for configuration and monitoring. The challenge for chipmakers is to ensure that such complex devices function properly and error free in all these modes of operations, fit all the intended application, and support all the advertised features. This necessitates the existence of a department whose sole function is to face this challenge and to validate all the functions, features, modes of operations, and applications of the devices. System Validation Design (also known as Product Validation) department in PMC-Sierra is tasked to validate all PMC-Sierra devices, to record, and to report all the issues that are found with a particular device. Product validation acts as the first customer for device and is a key gate before the product is released to market.

There are two phases that a product validation team assigned to a chip will go through. The first phase is the preparation phase and the second phase is the execution phase. The preparation phase (which is the most complex and challenging phase) includes all the tasks that are carried out until the day that the packaged silicon arrives in the production validation laboratory. A validation team is assigned to a device a few months before the arrival date of a device. At the beginning the members of the team will familiarize themselves with the device and will develop a high-level plan and schedule for the validation of the device. When the plan is approved, the team will have two major objectives during the preparation phase. The first objective is to provide a detailed test plan known as the device Feature Test Plan (FTP). The second objective is to design and to prepare a fully functional

hardware and software platform for the validation of the device. These two objectives must be met before the arrival date of the device and are usually carried out in parallel.

The execution phase involves the execution of the feature test plan and the reporting and recording of all the test results and device issues. This phase will start from the arrival time of the packaged silicon.

This document describes the design and preparation of the hardware platform for the S/UNI® MULTI-48™ device which is one of the key objectives of the preparation phase. It also describes the challenges existed in meeting this objective.

DEVICE FEATURES AND APPLICATION

"The PM5360 S/UNI® MULTI-48™ SATURN User Network Interface is a monolithic integrated circuit that implements SONET/SDH processing, ATM mapping and Packet over SONET mapping functions for a channelized[1] STS-48 (STM-16) 2488.32 Mbit/s stream, up to four channelized STS-12 (STM-4) 622.08 Mbit/s streams, and up to four STS-3 (STM-1) 155.52 Mbit/s streams. The S/UNI® MULTI-48™ may be configured as a single 2488.32 Mbit/s stream aggregating one STS-48c(STM-16/AU-4-16c) or a combination of STS-12c(STM-4/AU-4-4c) and STS-3c(STM-1/AU-4)/STM-1streams. It can also be configured as a combination of four 622.08 Mbit/s and 155.52 Mbit/s streams aggregating STS-12c(STM-4/AU-4-4c) and STS-3c(STM-1/AU-4.

The S/UNI® MULTI-48™ receives SONET/SDH streams using bit serial interfaces, recovers the clock and data and processes section, line, and path overhead. The S/UNI® MULTI-48™ performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The S/UNI® MULTI-48™ interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cells or POS frames.

When used to implement an ATM UNI or NNI, the S/UNI® MULTI-48™ frames to the ATM payload using cell delineation. Idle/unassigned cells may be optionally dropped. Cells are also dropped upon detection of a header check sequence error. The ATM cell payloads are descrambled and are written to a scalable FIFO buffer (programmable FIFO depth). The received cells are read from the FIFO using a 32-bit wide UTOPIA Level 3 or POS-PHY Level (clocked up to 104 MHz) datapath interface. Counts of received ATM cell headers that are erroneous are accumulated independently for performance monitoring purposes.

When used to implement packet transmission over a SONET/SDH link, the S/UNI® MULTI-48™ extracts Packet over SONET (POS) frames from the SONET/SDH

[1] channelized downto STS-3c (STM-1/AU-4)

synchronous payload envelope. Frames are verified for correct construction and size. The control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive scalable FIFO (programmable FIFO depth – all packets are 16 byte block aligned). The received packets are read from the FIFO through a 32-bit POS-PHY Level 3 (clocked up to 104 MHz) system side interface. Valid and FCS erroneous packet counts are provided for performance monitoring. The S/UNI® MULTI-48™ Packet over SONET implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

The S/UNI® MULTI-48™ transmits SONET/SDH streams using bit serial interface(s). When in STS-48(STM-16) mode, the S/UNI® MULTI-48™ synthesizes the transmit clock from a 155.52 MHz frequency reference. When in STS-12(STM-4) and STS-3(STM-1) modes, the S/UNI® MULTI-48™ synthesizes the transmit clock from a 77.76 MHz frequency reference. The S/UNI® MULTI-48™ performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI® MULTI-48™ generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the ATM or POS frames. The S/UNI® MULTI-48™ also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications. Any of the transmit streams can be loop-timed to its corresponding receive link.

When used to implement an ATM UNI or NNI, ATM cells are written to an internal scalable FIFO (programmable FIFO depth) using a 32-bit wide UTOPIA Level 3 or POS-PHY Level 3 (clocked up to 104 MHz) datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI® MULTI-48™ provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement a Packet over SONET/SDH link, the S/UNI® MULTI-48™ inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to

be transmitted are written into a scalable FIFO (programmable FIFO depth – all packets are 16 byte block aligned) through a 32-bit SATURN POS-PHY Level 3™ (clocked up to 104 MHz) system side interface. POS frames are built by inserting the flags, control escape characters and the FCS fields. Either the CRC-CCITT or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

All transport overhead bytes can be inserted from or extracted to an external device through specialized I/O pins.

The S/UNI® MULTI-48™ provides an APS port to connect to a mate working or protection device. The APS interface is based upon a specialized 8B/10B encoded LVDS interface which encodes the framing position, the path overhead position, marks the AIS state, and guarantees transition density on the descrambled SONET/SDH payload. This APS functionality is performed on the system side of the path overhead processors, which, on both the working and protection devices, is timed with a common clock.

No line rate clocks are required directly by the S/UNI® MULTI-48™ as it synthesizes the transmit clock and recovers the receive clock using a 155.52 MHz reference clock (for STS-48/STM-16 mode) or a 77.76 MHz reference clock (for STS-12/STM-4 and STS-3/STM-1 modes). The S/UNI® MULTI-48™ outputs differential CML line data (TXD_P[4:1]/ TXD_N[4:1]). The S/UNI® MULTI-48™ is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The S/UNI® MULTI-48™ also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI® MULTI-48™ is implemented in low power, +1.8 Volt, CMOS technology. It has LVTTL/CMOS compatible digital inputs and LVTTL/CMOS compatible digital outputs. High-speed inputs and outputs support 3.3V compatible pseudo-ECL (PECL).

This device is in a 500-ball UBGA package. PCB layout provisions are provided for a custom 500-ball UBGA socket adapter." [1]

Figure 1: Multi-rate ATM Switch Port Application [1]

shows how the S/UNI MULTI-48 device can be used in a multi-rate ATM switch port application. In this example, the SYSCLK oscillator is optional.

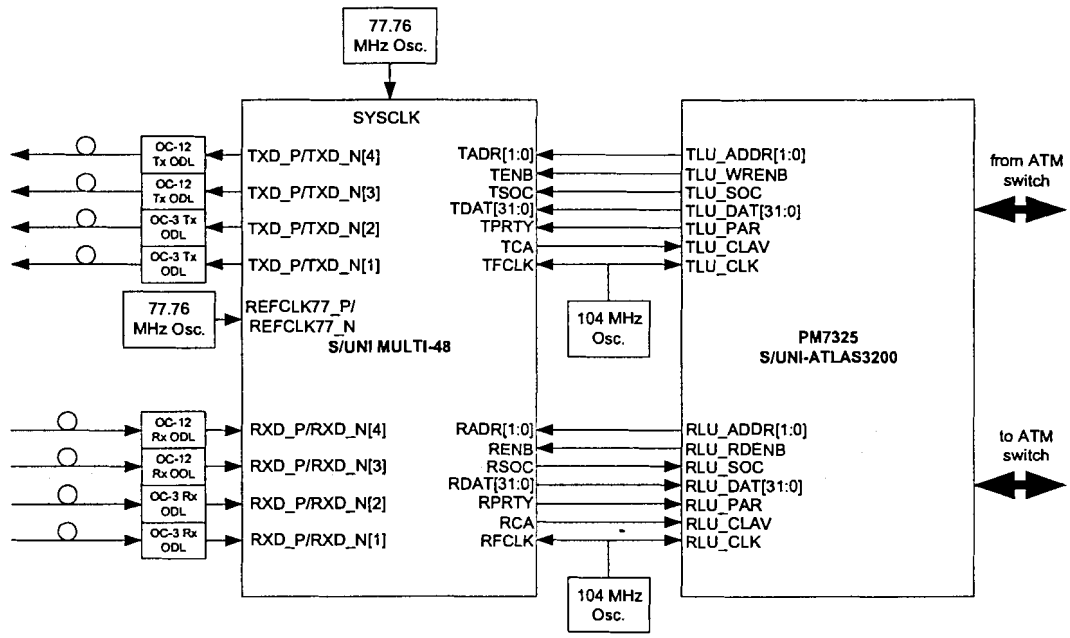

Figure 1: Multi-rate ATM Switch Port Application [1]

Figure 2 shows how the S/UNI MULTI-48 device can be used in a multi-rate IP switch port application. In this example, the SYSCLK oscillator is optional.

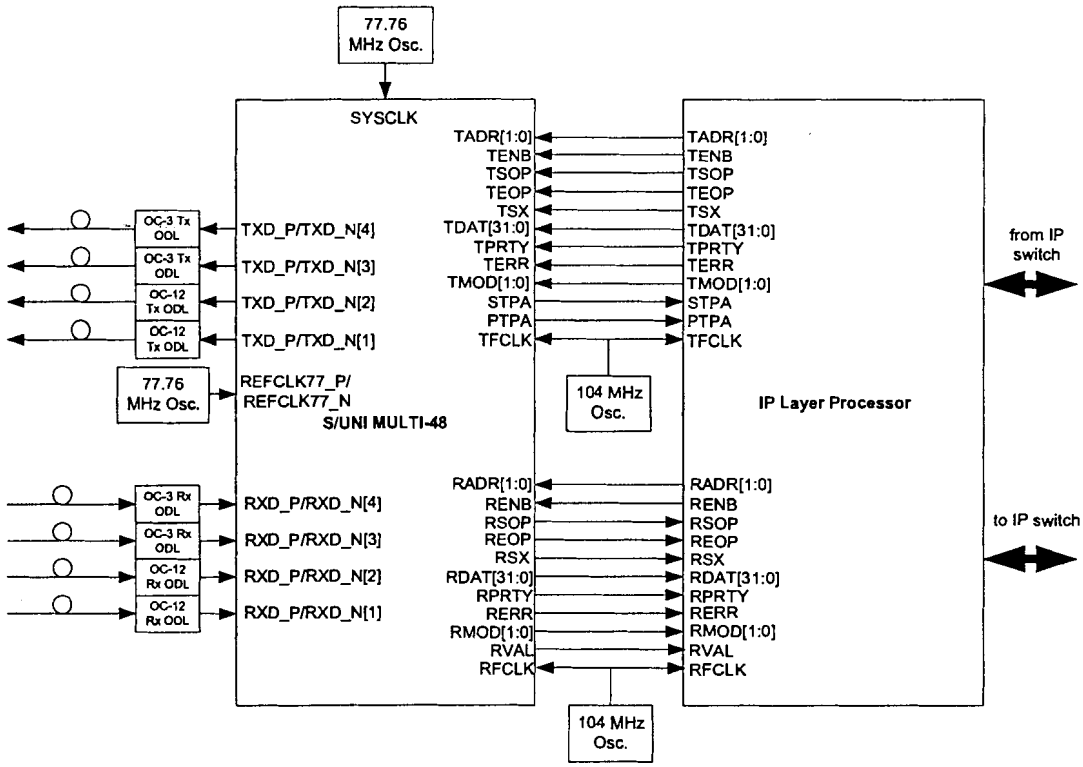

Figure 2 Multi-Rate IP Switch Port Application [1]

Figure 3 shows how two S/UNI MULTI-48 devices can be used in a 1:1 protection scheme. In this example, the SYSCLK oscillator and 8 kHz reference are optional.

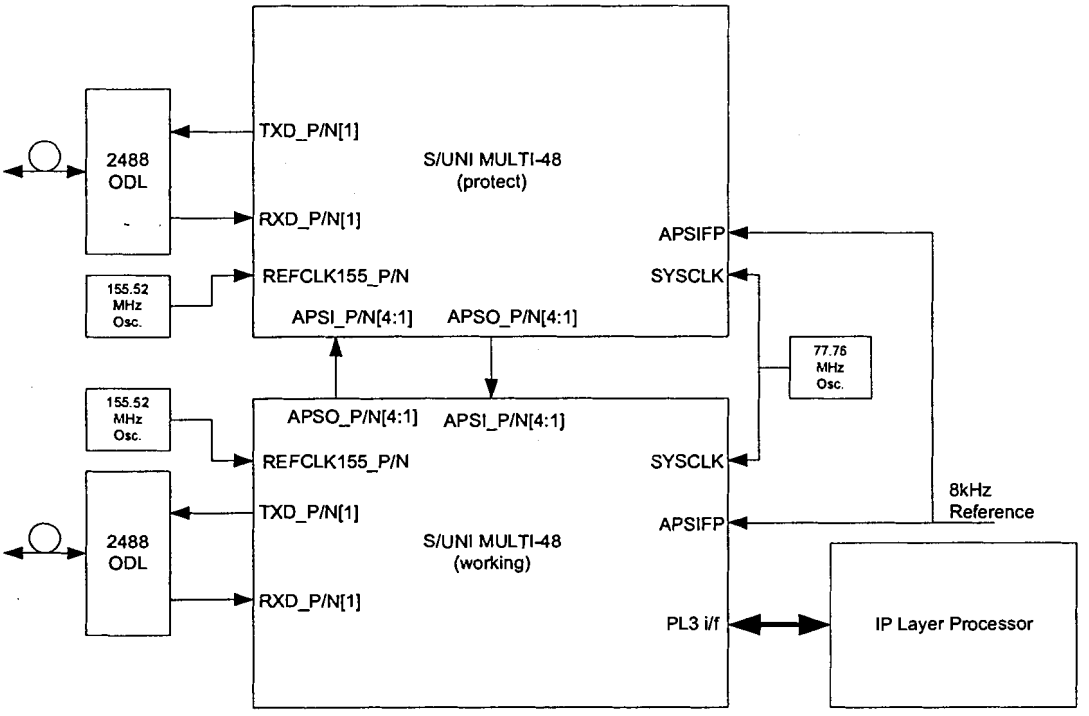

Figure 3 APS Protection Application [1]

DEVICE BLOCK DIAGRAM AND VARIOUS LOOPBACK MODES

The S/UNI® MULTI-48™ functional block diagram and various loopback modes are given below. These diagrams are very significant and they provide maps for testing various data paths within the device.

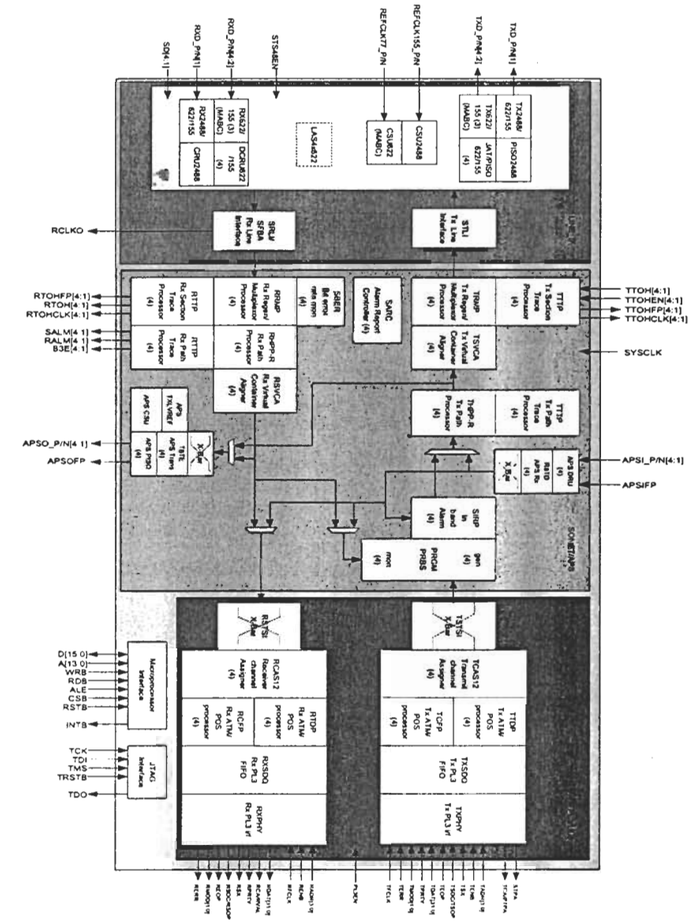

Figure 4 Block Diagram [1]

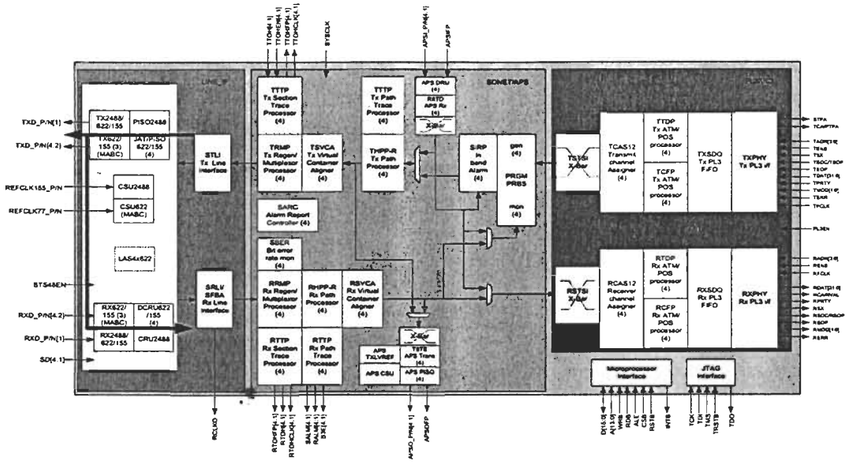

Figure 5 Serial Diagnostic Loopback [1]

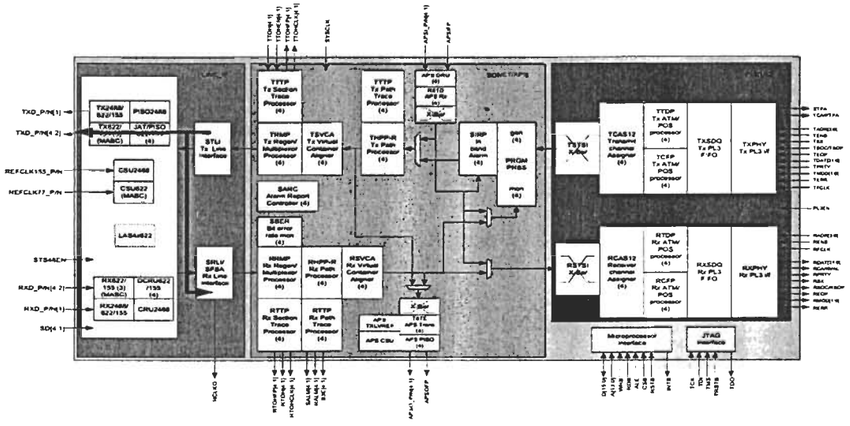

Figure 6 Parallel Diagnostic Loopback [1]

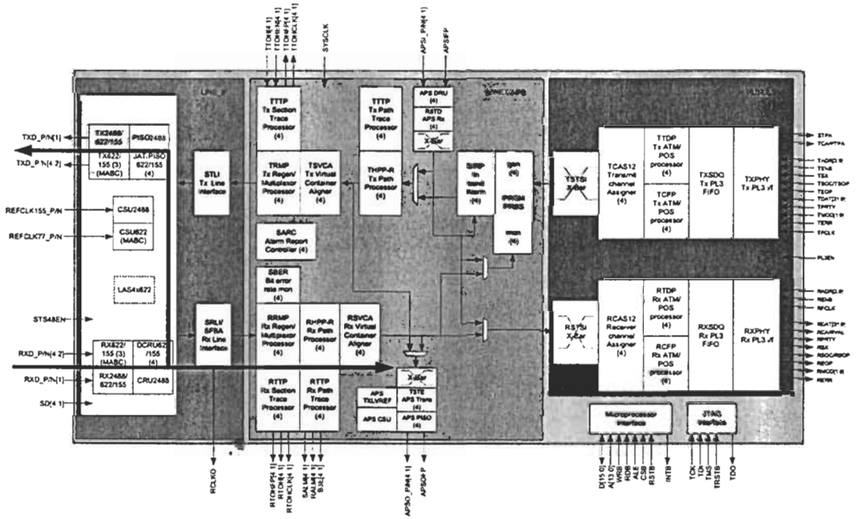

Figure 7 Line Loopback [1]

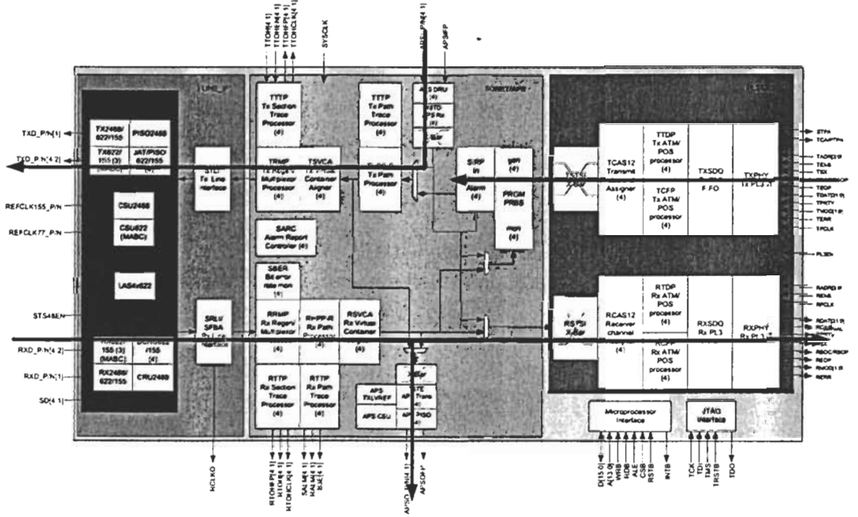

Figure 8 APS Protection Configuration [1]

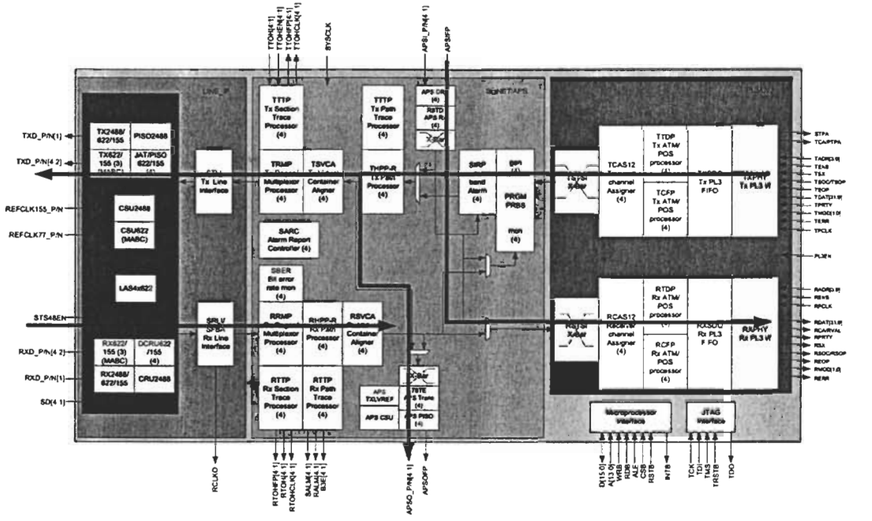

Figure 9 APS Working Configuration [1]

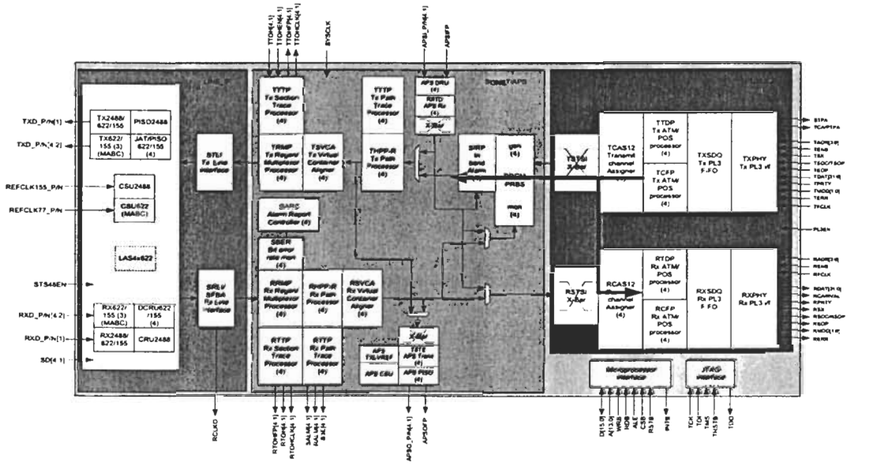

Figure 10 Cell/Packet Loopback [1]

HARDWARE PLATFORM

Among the product validation engineers, the hardware platform is commonly referred to as the Engineering Validation Board (EVB). The purpose of the engineering validation board is to provide a platform upon which to evaluate the quality and functionality of the device under test. The general EVB requirements are:

- Support the execution the feature test plan.
- Fulfill product validation requirements for all points controllable and accessible.
- Furnish the power-supply requirements of the device under test by segregate power planes, and providing low-noise and quite supply where required.
- Permit independent external control of all device power rails. Support product engineering's requirements for power-supply noise injection
- System clock domains must be capable of being driven synchronous as well as asynchronously from both on and off-board sources.
- Support interoperability requirements with other members of the system architecture.
- Furnish the required device under test densities with which to conduct system testing.

Additionally, this board is designed such that it can be used as a reference design for customers. A reference design is a design that is passed on to PMC customers as a reference for their own designs. Customer reference designs must provide general guidelines as to the design major circuits for the device such as high-speed serial interface design, parallel interface design, power supply design, clock distribution circuit, etc. Some main application requirements for the PMC S/UNI® MULTI-48™ customer reference design are listed below:

- The board should be as simple as possible. The customer should just need to connect the power and the Ethernet. They should not need to do anything else hardware wise.

- The width of the board should be 6U. The standard depth for a 6U board is 160mm.
- Keep the number of jumpers as low as possible.
- The customer should be able to use a nano-engine as the processor on board.
- An FPGA is required on the UL3/PL3 bus.
- A single 3.3V power source should be able to power up the entire board.

The following block diagrams outline the major elements and bus structures of the S/UNI® MULTI-48™ EVB design.

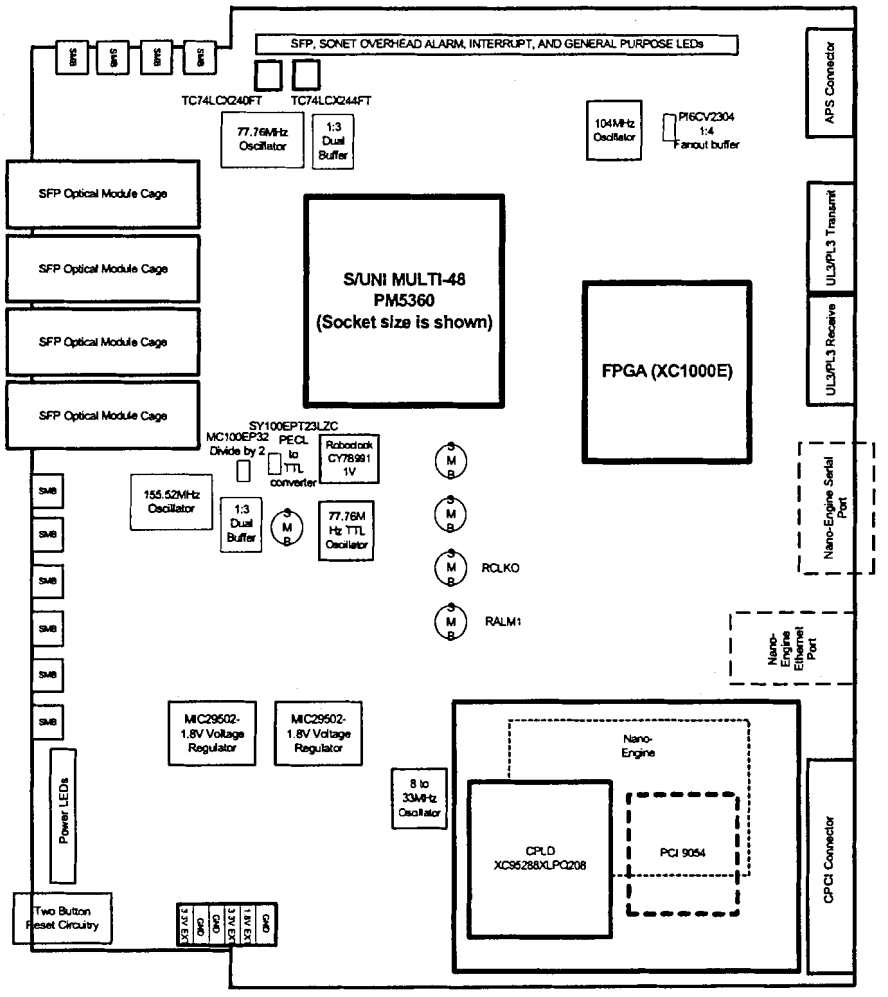

Figure 11 S/UNI® MULTI-48™ EVB Placement Diagram

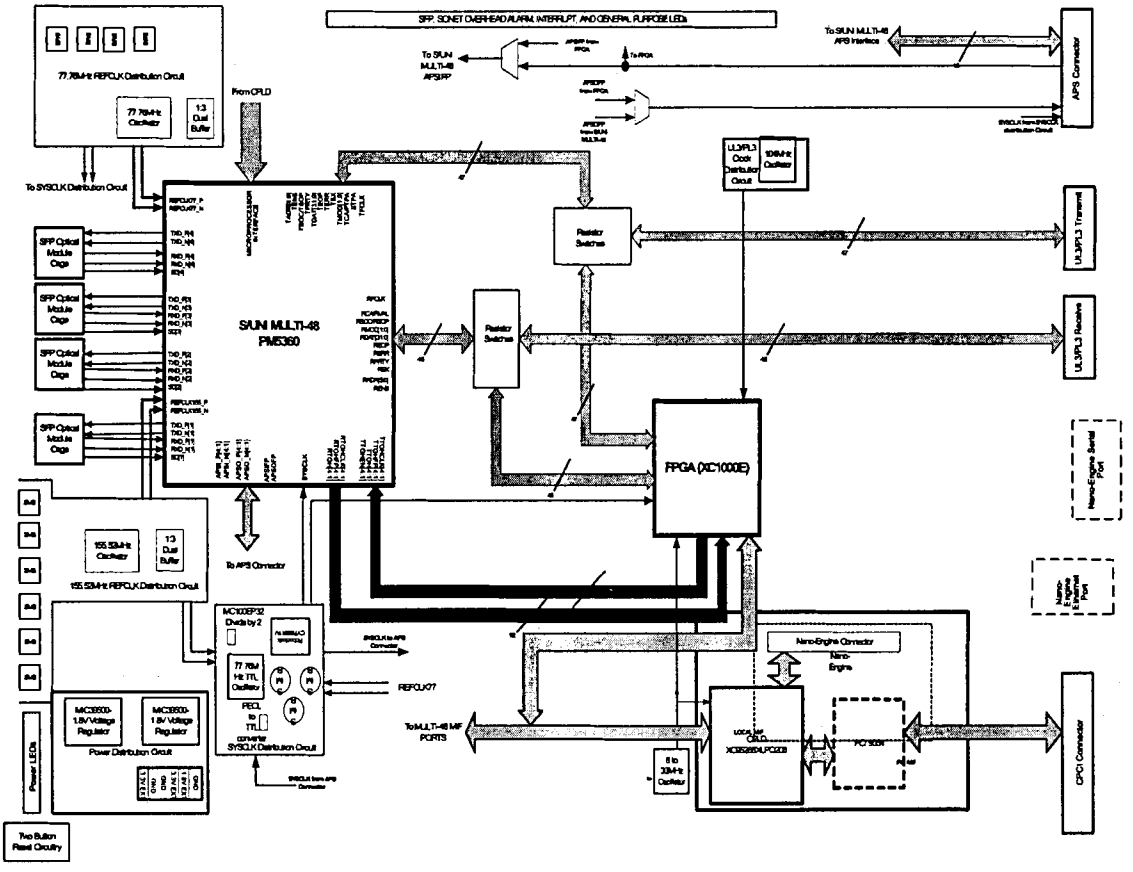

Figure 12 S/UNI® MULTI-48™ EVB Block Diagram

Figure 13 shows the finished assembled board as used by the product validation group for the validation of the S/UNI® MULTI-48™ device.

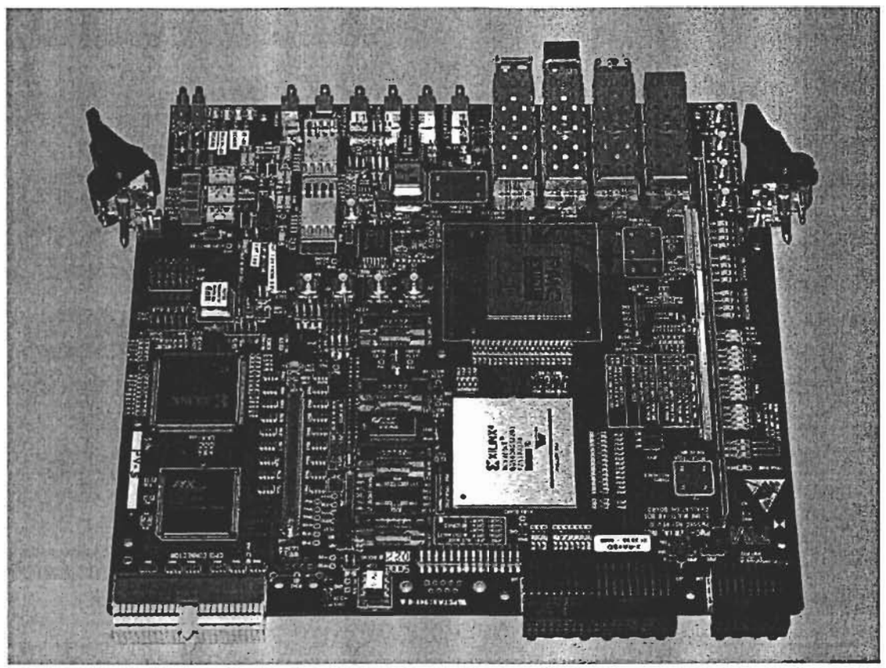

Figure 13 Finished S/UNI® MULTI-48™ Evaluation Board

The design of major blocks of the S/UNI® MULTI-48™ EVB are described in the following sections.

PROCESSOR INTERFACE

The S/UNI® MULTI-48™ EVB local processor interface can be provided by a variety of processor modules.

COMPACT PCI

The PCI bridge device, PLX-9054, comes in a 176-pin QFP package. This device is highly configurable and supports many different local bus interface configurations.

The PLX-9054 will be set in 16-bit non-multiplexed mode to accommodate the following devices:

- XILINX XC95288XLPQ208 CPLD: 8-bit, non-multiplexed mode
- S/UNI® MULTI-48™: 16-bit, non-multiplexed mode
- XILINX XCV1000E FPGA: 8-bit, non-multiplexed mode

The PLX may also be set in 16 bit multiplexed mode to support the above devices. In this mode, the CPLD will demultiplex the address and data and will provide them to the down stream devices.

The PCI port on the bridge device is connected directly to the cPCI connector, a 22 x 5 Type A shielded female RA connector (AMP 352068-1). The 20MHz local bus clock and PCI clock are routed to the PCI bridge device.

The configuration SEEPROM is used to configure the PCI bridge after power-up. The SEEPROM used is a National/Fairchild NM93CS66 8-pin DIP. To facilitate validation board control, the SEEPROM also records a copy of the EVB serial number.

SINGLE BOARD COMPUTER (SBC)

The S/UNI® MULTI-48™ EVB Microprocessor interface adopts the processor-per-card architecture utilizing the nanoEngine from Bright Star Engineering (Figure 14) or the PMC-Sierra MIPS processor based Single Board Computer (SBC) (Figure 15) as distributed controller and 10/100 Base-T Ethernet for the control plane. The distributed processor architecture is no longer limited by the 8-slot CompactPCI backplane.

Figure 14 nanoEngine from Bright Star Engineering

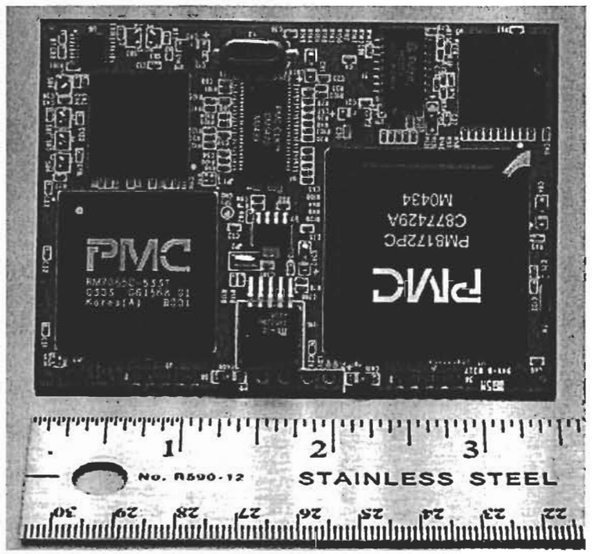

Figure 15 PMC-Sierra MIPS processor based Single Board Computer

CLOCK DISTRIBUTION

There are 5 clock domains on the S/UNI® MULTI-48™ EVB driven by 5 on-board oscillators and the PCI backplane.

Each of the cell and system clocks can be derived either from its respective oscillator, or from an alternate external clock source. This allows the testing of both synchronous and asynchronous clock domains. The SYSCLK can be skewed using Cypress ROBO clock.

Table 1 Clock Domains

Name	Frequency	Logic	Impedance	Description
BCLK	20MHz	LV-CMOS	50 Ω	Local Bus Clock: The processor bus clock is distributed to the PLX-9054, the CPLD, and a Mictor header.
REFCLK_155	155.52MHz	3.3V PECL	50 Ω	Used for REFCLK_155 input to the device. It is distributed to SMBs.
REFCLK_77	77.76 MHz	3.3V PECL	50 Ω	Used for REFCLK_77 input to the device. It is distributed to SMBs.
SYSCLK	77.76 MHz	3.3V TTL	50 Ω	Used for device SYSCLK (which is used for APS). Distributed to SMB and APS connector as well as the device SYSCLK pin.
TFCLK/RFCLK	104 MHz	3.3V TTL	50 Ω	This oscillator is mainly for reference design usage and will not be used for PV testing. The user has the option of choosing to drive the RFCLK and TFCLK from UL3/PL3 receive and transmit clocks, or this oscillator.

A 155.52 MHz differential PECL reference clock is required to drive the 155.52MHz reference clock for both clock recovery and clock synthesis circuits (REFCLK155) of the S/UNI® MULTI-48™. A distribution scheme is required for distribution of the REFCLK155 to the S/UNI® MULTI-48™ and an off board connector for jitter testing.

A 77.76 MHz differential PECL reference clock is required to drive the 77.76MHz reference clock for both clock recovery and clock synthesis circuits (REFCLK77) of the S/UNI® MULTI-48™. A distribution scheme is required for distribution of the REFCLK77 to the S/UNI® MULTI-48™ and an off board connector for jitter testing.

Clock generation at each frequency (155.52MHz or 77.76MHz) is provided by one of either a socketed oscillator, or an external clock. REFCLK155 configuration is selected by jumpers. The reference clock monitor brings out the clock for observation.

At each frequency, (155.52MHz or 77.76MHz) an additional oscillator and additional SMB inputs have been added to allow REFCLK to be directly connected without buffering to the S/UNI® MULTI-48™. This feature is required for jitter testing.

Optionally, the 77.76MHz clock or a divide by 2 version of the 155.52MHz clock can be converted to TTL and used as a source for SYSCLK. This is required for applications where the SYSCLK is not used and/or SYSCLK may require being frequency locked to the REFCLK.

Also for each frequency, the two SMBs at the input of the buffer may be connected directly to the device REFCLK balls. This is done for jitter testing purposes and the idea is to have a function generator generate a clock and connect it directly to the device balls without any buffering.

A block diagram of the REFCLK155 and REFCLK77 distribution is given in figure 16.

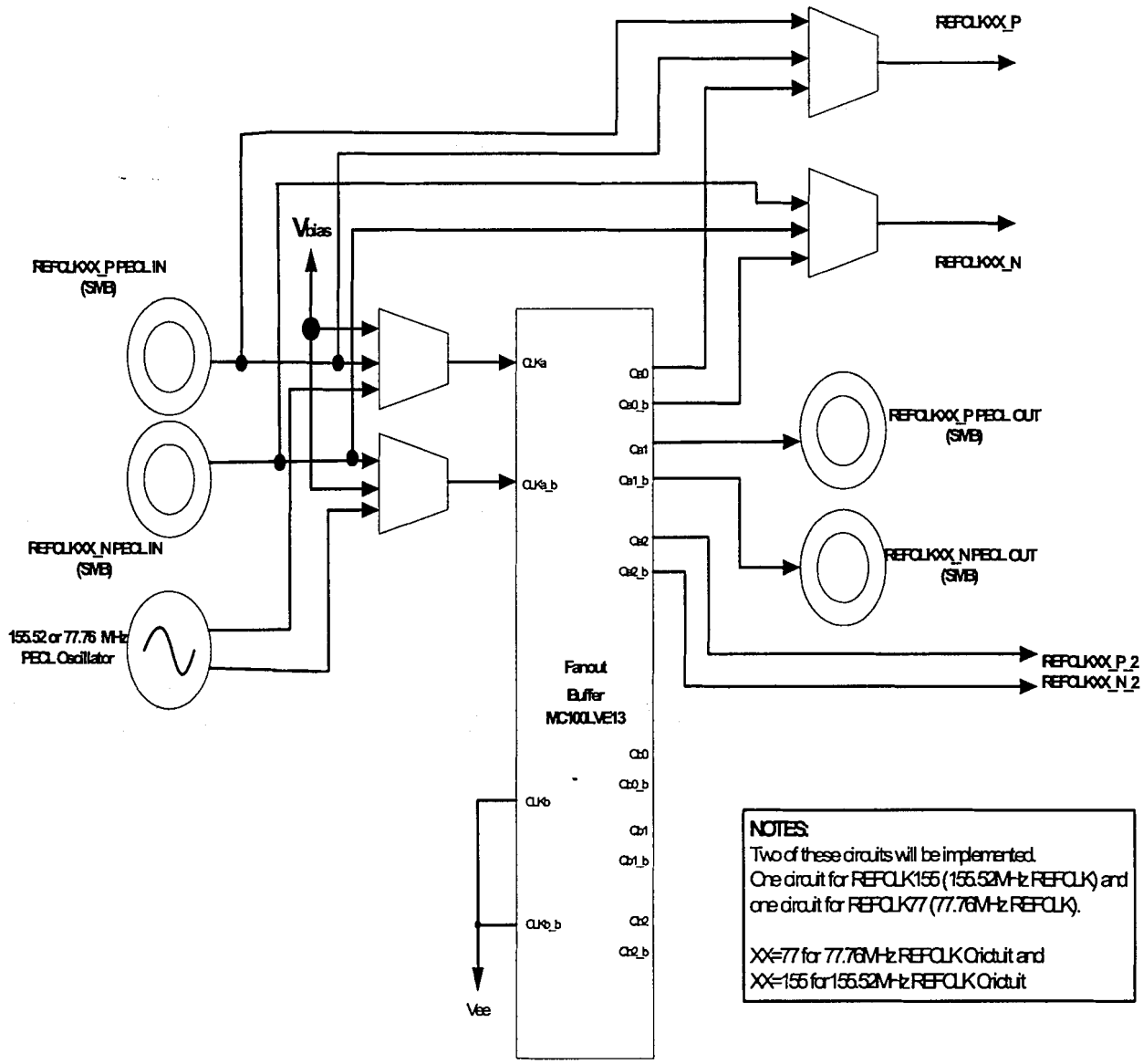

Figure 16 155.52/77.76 REFCLK Clock Distributions

The SYSCLK when not grounded can be provided from a 77.76MHz TTL, a single ended PECL SMB input, another board through the APS connector, or from the REFCLK clock distribution circuit. When the clock is provided by an external source through the SMB input, it must be converted to TTL. A ROBOCLOCK is used to change the skew of the SYSCLK if deemed necessary. The circuit also outputs the clock to an SMB for measurement and monitoring purposes. Also a clock is generated for the SYSCLK of

another port. This clock is routed to the other board through the APS connector. A direct SMB input to the device SYSCLK pin is also provided. A block diagram of the SYSCLK distribution is given in figure 17.

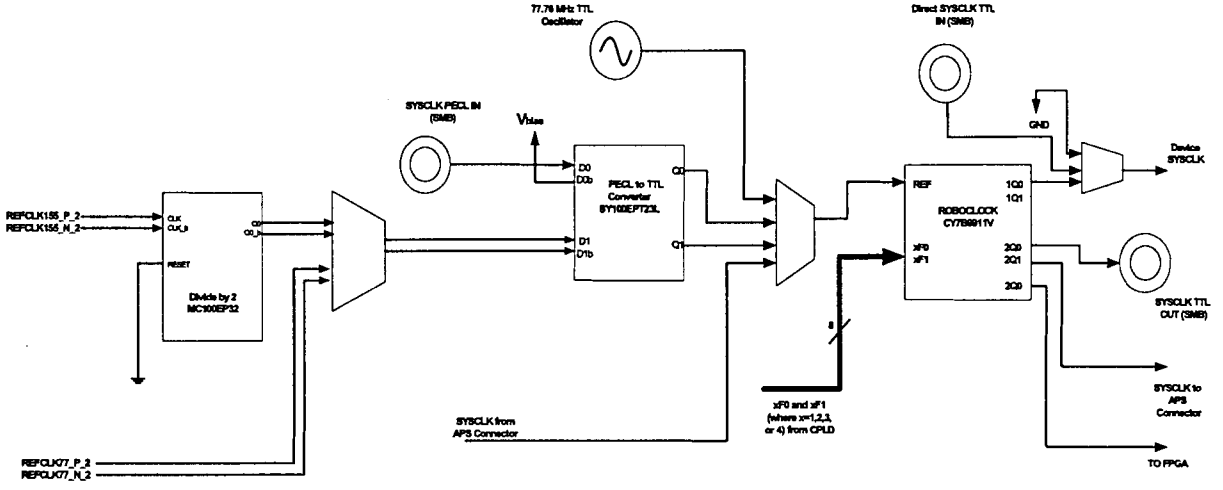

Figure 17 77.76 MHz SYSCLK Clock Distributions

The UL3/PL3 device interface requires two clocks (RFCLK and TFCLK). A 104MHz TTL oscillators is provided on the board. This oscillator is mainly for reference design usage and will not be used for product validation testing. The user has the option of choosing to drive the RFCLK and TFCLK from UL3/PL3 receive and transmit clocks, a single 104MHz oscillator. Product validation will mainly use the clocks provided from the tester board over the UL3/PL3 backplane connectors. The clock generated by the oscillator will also be passed to the FPGA. A block diagram of the RFCLK and TFCLK distributions is given in figure 18.

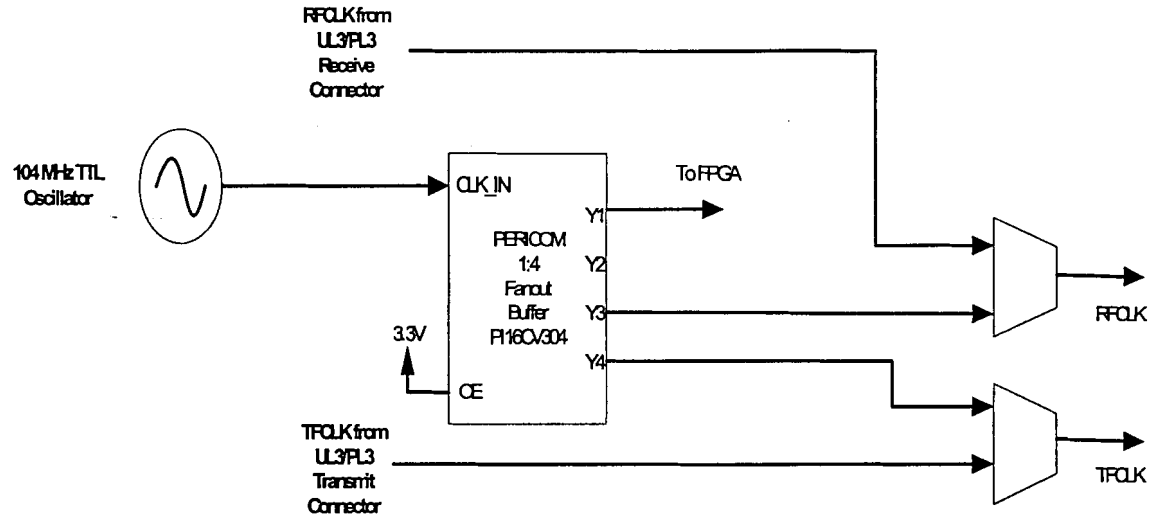

Figure 18 UL3/PL3 Interface Clock Distributions

SONET LINE INTERFACE

The Line side of the S/UNI® MULTI-48™ allows Single Form Factor Pluggable (SFP) optical modules to be connected directly to the device without the need for additional external terminations. Figure 19 is a picture of an SFP optical module.

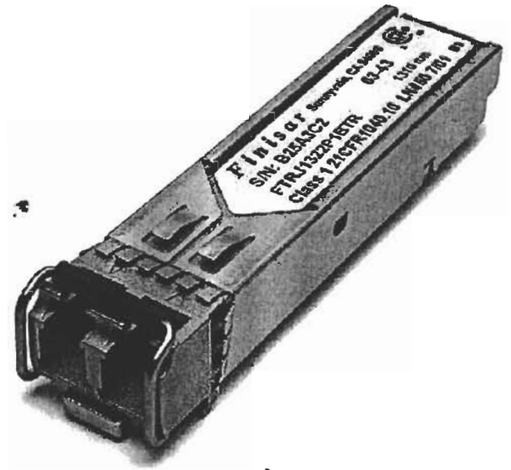

Figure 19 Single Form Factor Pluggable (SFP) Optical Module

The S/UNI® MULTI-48™ has been designed to interface directly to Small Form Factor Pluggable (SFP) Optical Modules. Figure 20 shows the layout of the S/UNI® MULTI-48™ serial interface to SFP optics on the S/UNI® MULTI-48™ EVB.

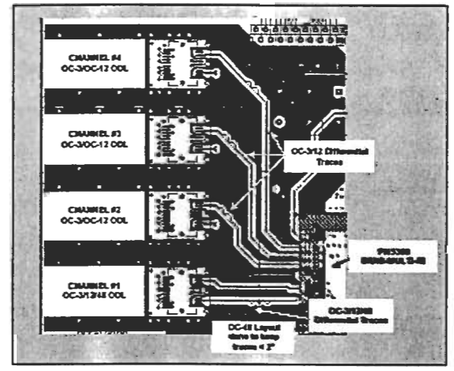

Figure 20 Layout of S/UNI® MULTI-48™ to SFP optical modules

The S/UNI® MULTI-48™ device can operate in three different modes:

1X2488

In this mode the device receives/transmits OC48 rate data from/to its RXD[1]/TXD[1] ports. The SONET OC-48 frame is serialized and transmitted/received over a small form factor pluggable (SFP) optical transceiver on the front panel of the card. A TTL level Signal Detect (SD) is also provided to the S/UNI® MULTI-48™ analog interface. Note that since the optical module is pluggable, modules from various vendors may be used. This is extremely useful since it allows us to find and recommend the module that has the best jitter performance.

4X622

In this mode the device receives/transmits OC12 rate data from/to its RXD[4:1]/TXD[4:1] ports. The SONET OC-12 frame is serialized and transmitted/received a small form factor pluggable (SFP) optical transceiver on the front panel of the card. A TTL level Signal Detect (SD) is also provided to the S/UNI® MULTI-48™ analog interface. The device has four ports and can thus handle four OC12c channels. Note that since the optical module is pluggable, modules from various vendors may be used. This is extremely useful since it allows us to find and recommend the module that has the best jitter performance. Optionally various pluggable paddle boards may be designed such that they can plug into the SFP on board connector while the paddle board itself is populated with a different optical module (SFF or 1x9).

4X155

In this mode the device receives/transmits OC3 rate data from/to its RXD[4:1]/TXD[4:1] ports. The SONET OC-3 frame is serialized and transmitted/received a small form factor pluggable (SFP) optical transceiver on the front panel of the card. A TTL level Signal Detect (SD) is also provided to the S/UNI® MULTI-48™ analog interface. The device has four ports and can thus handle four OC3c channels. Note that since the optical module is pluggable, modules from various vendors may be used. This is extremely useful since it allows us to find and recommend the module that has the best jitter performance. Optionally various pluggable paddle boards may be designed such that they can plug into the SFP on board connector while the paddle board itself is populated with a different optical module (SFF or 1x9).

MIX OF 622 AND 155

In this mode the device receives/transmits a mix of OC3 and OC12 rate data from/to its RXD[4:1]/TXD[4:1] ports. The optical modules used in this mode are exactly the same as the modules used for 4X622 and 4x155 modes.

The line interface design with the Single Form Factor Pluggable Optical modules, enables the board to support all the modes of operation for the S/UNI® MULTI-48™ device.

AUTOMATIC PROTECT SWITCHING (APS) LVDS SERIAL INTERFACE

The Automatic Protect Switching (APS) LVDS serial interface carries eight differential signals to the backplane on a 60 position connector (figure 21). An interface to the backplane allows connectivity to another APS interface in another slot of the compact PCI chassis. Four differential transmit and four differential receive signals carry the encoded data and optionally two framing pulses and a system clock at 77.76 MHz may be used for synchronizing over a full system. The S/UNI® MULTI-48™ EVB can be used as the clock slave to the other board (for example, the TSE EVB) or can be used as the clock master to the other board.

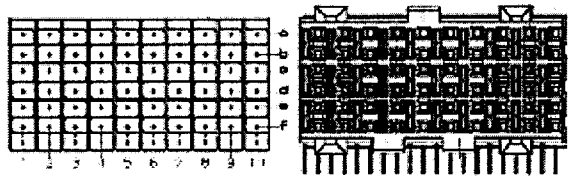

Figure 21 60 position HS3 Backplane Connector used for APS port

The board is designed such that when APS differential inputs are not used, the _P side of each unused link can be shorted to ground, and the _N side of each unused link can be tied to 3.3V using a 4.7KΩ resistor. This is the required for the device to operate error free when APS is not used.

SYSTEM SIDE INTERFACE

The S/UNI® MULTI-48™ can use Utopia Level 3 (UL3) or POS PHY Level 3 (PL3) to communicate to a higher level device over its system interface. An HS3 connector is provided to test the system interface of the device. The pin out of the transmit and receive connectors are described below:

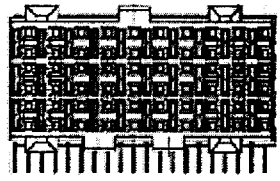

Figure 22 Transmit and Receive PL3 and UL3 HS3 connectors

Table 2 Transmit PL3 and UL3 HS3 connectors

Pin	A	B	C	D	E	F
10	TDAT[31]	TDAT[30]	TSYSCLK	TDAT[29]	TDAT[28]	TFCLK
9	TDAT[27]	TDAT[26]	TDAT[25]	TDAT[24]	TDAT[23]	N.C.
8	TDAT[22]	TDAT[21]	TDAT[20]	TDAT[19]	TDAT[18]	N.C.
7	TDAT[17]	TDAT[16]	TDAT[15]	TDAT[14]	TDAT[13]	N.C.
6	TDAT[12]	TDAT[11]	TDAT[10]	TDAT[9]	TDAT[8]	N.C.
5	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	N.C.
4	TDAT[2]	TDAT[1]	TDAT[0]	TPRTY	TERR	N.C.
3	TSX	TS0C/TSOP	TEOP	STPA	TCA/TPA	N.C.
2	TMOD[0]	TMOD[1]	TENB	N.C.	N.C.	N.C.
1	N.C.	TADR[3]	TADR[2]	TADR[1]	TADR[0]	N.C.

Table 3 Receive PL3 and UL3 HS3 connectors

Pin	A	B	C	D	E	F
10	RDAT[31]	RDAT[30]	RDAT[29]	RDAT[28]	RDAT[27]	N.C.
9	RDAT[26]	RDAT[25]	RDAT[24]	RDAT[23]	RDAT[22]	N.C.
8	RDAT[21]	RDAT[20]	RDAT[19]	RDAT[18]	RDAT[17]	N.C.
7	RDAT[16]	RDAT[15]	RDAT[14]	RDAT[13]	RDAT[12]	N.C.
6	RDAT[11]	RDAT[10]	RDAT[9]	RDAT[8]	RDAT[7]	N.C.
5	RDAT[6]	RDAT[5]	RDAT[4]	RDAT[3]	RDAT[2]	N.C.
4	RDAT[1]	RDAT[0]	RERR	RSOC/RSOP	REOP	N.C.
3	RPRTY	RCA/RVAL	RMOD[0]	RMOD[1]	RSX	N.C.
2	RADR[0]	RADR[1]	RADR[2]	RADR[3]	N.C.	N.C.
1	N.C.	N.C.	RSYSCLK	N.C.	RENB	RFCLK

The UL3/PL3 data and control buses may be routed to the backplane HS3 connectors or be routed to the onboard FPGA. Resistor switches are used to accommodate this.

FPGA (XILINX XCV1000E) FOR SONET OVERHEAD INSERTION/EXTRACTION

The S/UNI® MULTI-48™ SONET overhead port allows the extraction of SONET overhead bits through a clock and data interface. At the same time, it allows the insertion of overhead bits through the same clock and data interface. A Xilinx XCV1000E device is used to insert data into the SONET overhead as well as verify the integrity of this data when it is extracted on the other side. This device can be programmed for PRBS data and user defined patterns. Note that the XCV1000E is also used for frame pulse generation in the APS and cross connect configurations.

For the customer reference design board, this FPGA is also used to interface to the system side interface of the S/UNI® MULTI-48™ device and to support UL3/PL3 packet insertion, extraction and processing.

EVB BOARD SUPPORT

POWER SUPPLY AND DECOUPLING

The S/UNI® MULTI-48™ device can be powered via an external power supply. The S/UNI® MULTI-48™ EVB has two separate power planes: the +3.3V plane and the +1.8V plane.

The following table provides a rough estimate of the power required for each plane. Each plane is segregated and summarized at the bottom of the table. This table reveals a number of parameters:

total board power consumption,

sizing of regulators,

required number of power planes,

estimated decoupling story.

a sanity check for the total number of device under test power and ground pins.

Table 4 Power Consumption and Decoupling Worksheet

voltage	plane	device	qty	current	power	pins	mA/pin	# 0.1uF	#bulk
3.3V	VDDO	DUT	1	167 mA	551 mW	39-pins	4.281 mA	39-caps	0-caps
3.3V	AVDH	DUT	1	244 mA	806 mW	12-pins	20.354 mA	14-caps	2-caps
3.3V	QAVD	DUT	1	0 mA	0 mW	4-pins	0.000 mA	4-caps	0-caps
1.8V	AVDL	DUT	1	866 mA	1558 mW	13-pins	66.598 mA	11-caps	3-caps
1.8V	VDDI_A	DUT	1	275 mA	495 mW	5-pins	55.000 mA	6-caps	2-caps
1.8V	VDDI and VDDI_JAT	DUT	1	3084 mA	5552 mW	45-pins	68.543 mA	45-caps	0-caps
	VSS	DUT	1	0 mA	0 mW	125-pins	0.000 mA	0-caps	0-caps
sub-total				4636 mA	8962 mW	243-pins		119-caps	7-caps

voltage	plane	device	qty	current	power	pins	mA/pin	# 0.1uF	#bulk
3.3V		FPGA XILINX XCV1000E	1	5000 mA	16500 mW	40-pins	125 mA	40-caps	0-caps
		Optical Module (SFP)	4	280 mA	3696 mW	2-pins	140 mA	12-caps	8-caps
		XTAL	5	135 mA	2228 mW	1-pins	135 mA	7-caps	7-caps
		ROBOCLOCK Cypress CY7B9911V	1	480 mA	1584 mW	2-pins	240 mA	6-caps	0-caps

LEDs	34	20 mA	2244 mW	1-pins	20 mA	0-caps	0-caps
CPLD 95288	1	85 mA	281 mW	17-pins	5 mA	9-caps	2-caps
PCI9050 Bridge	1	250 mA	825 mW	15-pins	17 mA	13-caps	0-caps
4096 BIT SERIAL EEPROM	1	1 mA	3 mW	1-pins	1 mA	1-caps	0-caps
IDT74FCT3807AQ 1 to 10 Clock Driver	1	23 mA	75 mW	4-pins	6 mA	4-caps	0-caps
DS1834AS DUAL ECONO RESET WITH PUSHBUTTON	2	0 mA	0 mW	1-pins	0 mA	0-caps	0-caps
PI74LPT16244V 16-BIT BUFFER/LINE DRIVER	1	3 mA	11 mW	4-pins	1 mA	4-caps	0-caps
PI74LPT16245A 16-BIT BIDIRECTIONAL TRANSLATOR	1	3 mA	11 mW	4-pins	1 mA	4-caps	0-caps
SY100EPT22VZC DUAL LVTTL/LVCMOS-TO-DIFF LVPECL TRANSLATOR	1	25 mA	83 mW	1-pins	25 mA	2-caps	0-caps
MC100LVEL13DW ECL DUAL 1:3 FANOUT BUFFER	2	40 mA	264 mW	3-pins	13 mA	4-caps	2-caps
SY100EP32VZI /2 DIVIDER	1	37 mA	122 mW	1-pins	37 mA	2-caps	0-caps
SY100EPT23LZC DUAL DIFFERENTIAL LVPECL TO LVTTL TRANSLATOR	1	30 mA	99 mW	1-pins	30 mA	2-caps	1-caps
TC74LCX244FT OCTAL BUS BUFFER	1	4 mA	13 mW	1-pins	4 mA	2-caps	0-caps
TC74LCX240FT OCTAL BUS BUFFER INVERTED	1	4 mA	13 mW	1-pins	4 mA	2-caps	0-caps
nanoEngine	1	1555 mA	5132 mW	16-pins	97 mA	2-caps	2-caps
PI6CV2304W 160MHZ CLK BUFFER	1	34 mA	112 mW	1-pins	34 mA	2-caps	0-caps
Sub-		8009 mA	33295 mW			118-caps	22-caps

voltage	plane	device	qty	current	power	pins	mA/pin	# uF	# bulk
1.8V		FPGA XILINX XCV1000E	1	1000 mA	3300 mW	36-pins	28 mA	36-caps	4-caps
sub total				1000 mA	3300 mW			36-caps	4-caps
total					6595 mW			154-caps	26-caps

Table 5 S/UNI® MULTI-48™ Analog Power-Supply Filtering Recommendations

Name	Ball Location	Function	Filtering
AVDH	Ah26, AJ21, AK21, AJ19, AG23, AD4, AC5, AA5, Y5, V5, U5, G5	3.3V analog core power	Refer to figures 30 & 31
AVDL	AG24, AF24, AJ25, AJ23, T4, T5, R5, N5, L5, H5, F5, E3, J5	1.8V analog core power	Refer to figures 30 & 31
QAVD	AF23, AD5, U4, E4	3.3V quite analog power for the core	Refer to figures 30 & 31
VDDI_A	AE5, AE3, AC4, AA4, V4	Not defined yet.	Refer to figures 30 & 31

Figure 23 shows the 3.3V and 1.8V power distribution circuits for both the S/UNI® MULTI-48™ device and the EVB.

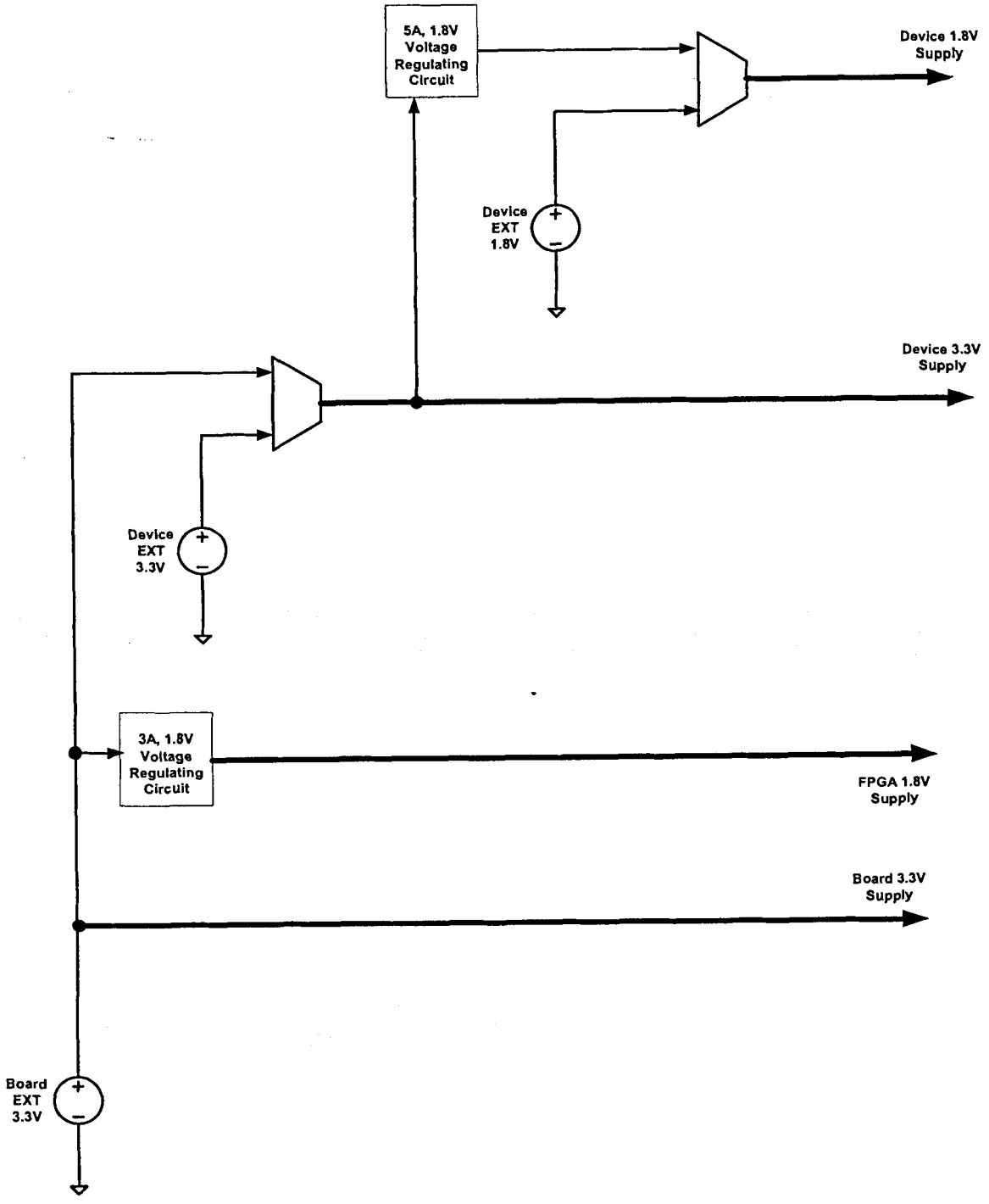

Figure 23 3.3V and 1.8V Power Distribution Circuit

Figure 24 indicates the recommended filtering for analog power balls as per the datasheet of the PMC S/UNI® MULTI-48™ device.

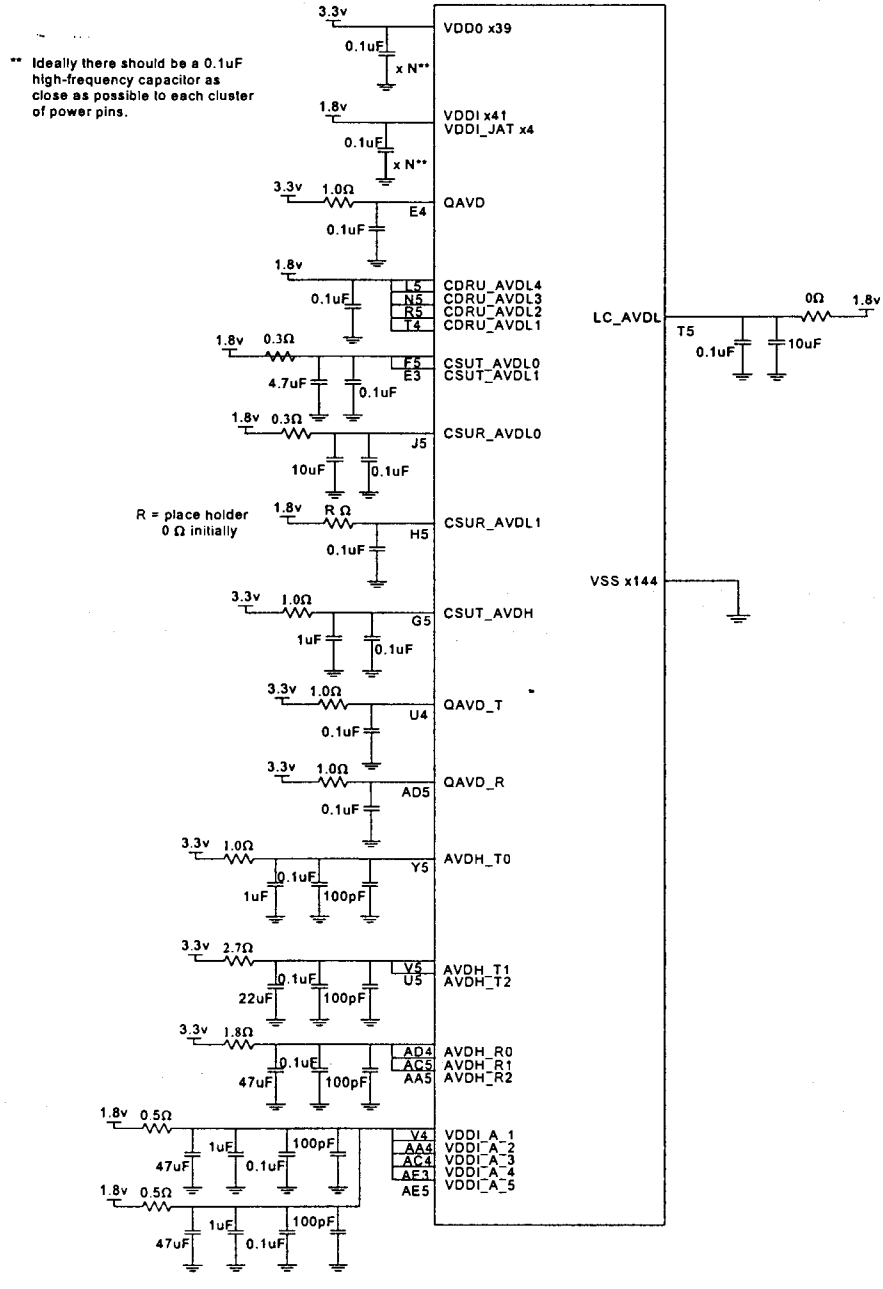

Figure 24 Recommended Analog Power Filtering

Figure 25 indicates the recommended filtering for APS analog power balls.

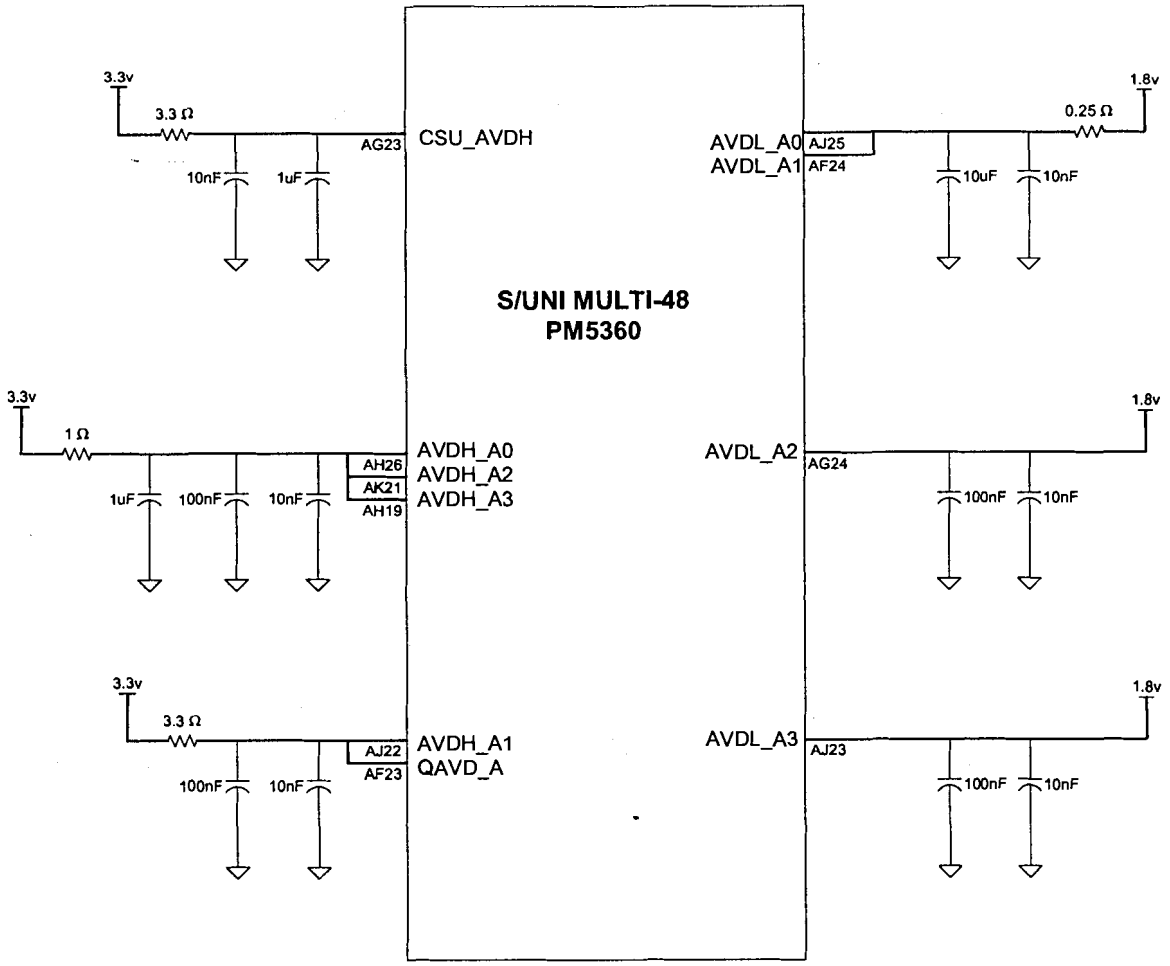

Figure 25 Recommended APS Analog Power Filtering

RESET CIRCUIT

The reset logic formed by the Dallas reset circuitry directly controls the PCI bridge, and the CPLD by monitoring either local power, or external reset switch or host generated CompactPCI reset. The S/UNI® MULTI-48™ device can be reset under software control via the CPLD interface.

There are two reset buttons on the board. The S1 button is used to reset the entire board except for the S/UNI® MULTI-48™ device. The S2 button is used to only reset the S/UNI® MULTI-48™ device.

CPLD (XILINX XC95288XLPQ208)

The XILINX XC95288XLPQ208 CPLD contains the glue logic necessary to interface the S/UNI® MULTI-48™ device and provides the following functions:

S/UNI® MULTI-48™ to CPCI bridge interface logic

Support network configuration FPGA

General purpose I/O

Address decode logic

LED and ROBO Clock Control

Reset Control

UL3/PL3 Bus switch select

UL3 or PL3 system interface select

OC48 or OC12/OC3 line interface select.

The CPLD shall provide a number of uncommitted input and outputs with which to signal and detect events. A Xilinx 9-pin JTAG header is provided for programming the CPLD.

LEDS

LEDs are provided to display the status of the power rails and device specific conditions. The single colour and tri-colour board status LEDs (DS[20:1]) are used to convey the following board conditions:

Single colour LEDs:

1. DUT 3.3V power supply status => 1 LED
2. DUT 1.8V power supply status => 1 LED
3. Board 3.3V power supply status => 1 LED
4. FPGA 1.8V power supply status => 1 LED
5. DUT Interrupt Indicator => 1 LED
6. FPGA Interrupt Indicator => 1 LED

7. Section Alarm Indicator (SALM[4:1]) => 4 LEDs
8. Receive Alarm Indicator (RALM[4:1]) => 4 LEDs
9. Bit Interleaved Parity Indicator (B3E[4:1]) => 4 LEDs
10. FPGA Program Done Indicator => 1 LED
11. Ethernet connectivity/activity Indicator (ETH_LED[2:0]) => 3 LEDs
12. General purpose => 2 LEDs.

Tri-colour LEDs

1. SFP transmitter fault indicator (SFP_TXFAULT[4:1]) => 4 LEDs
2. SFP LOS of receive signal indicator (SFP_LOS[4:1]) => 4 LEDs
3. General purpose => 4 LEDs.

JTAG

1. A 6-pin header is provided for the JTAG interface to the S/UNI® MULTI-48™ device.
2. A Xilinx 6-pin JTAG header is provided for programming the CPLD.
3. A Xilinx 6-pin JTAG header is provided for programming the FPGA.
4. A 7-pin JTAG header is provided for programming the nanoEngine.

ADAPTERS, INTERFACE CARDS, BACKPLANES

The following Adapters, Interface Cards, and/or Backplanes were developed for the validation effort:

1. PM1524-BD2 HS3 to HS3 paddle board is used to connect the EVB to PM1505 UL3/PL3 FPGA tester board.
2. PM1576A electrical adapter board is used to bring the line side electrical interface to SMA connectors to facilitate jitter tests.
3. A holder stand is used to support the electrical adapter boards. The holder stand will screw to the EVB and may also be supported by two vertical poles.

The electrical adapter boards are then screwed to the holder stand. The stand is made of Aluminum.

4. PM5560_BD2 LVDS Link Access Board is used to extend the S/UNI® MULTI-48™'s APS port LVDS signals to SMB connectors for LVDS analog performance tests. The board has a connector and eight pairs of SMBs on it. The access board connects to the EVB APS connector and provides access to the APS ports of the device through the SMBs.

5. PM5560_BD3 PLL board is used to clean the recovered RCLKO and feed it back into the REFCLK77 or REFCLK155 pins. This board provides the means of performing external looptiming on the device. Also two of these boards connected using SMB cables may be used for two devices talking over the APS ports in working and protect configuration. The block diagram for the board is given in figure 26.

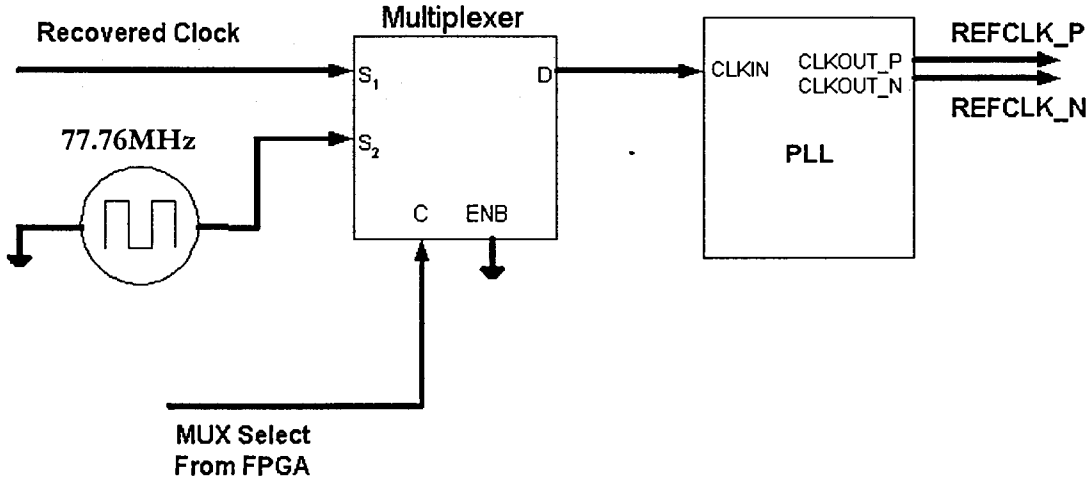

Figure 26 Looptime PLL Board Block Diagram

Figure 27 shows the finished assembled looptime PLL board.

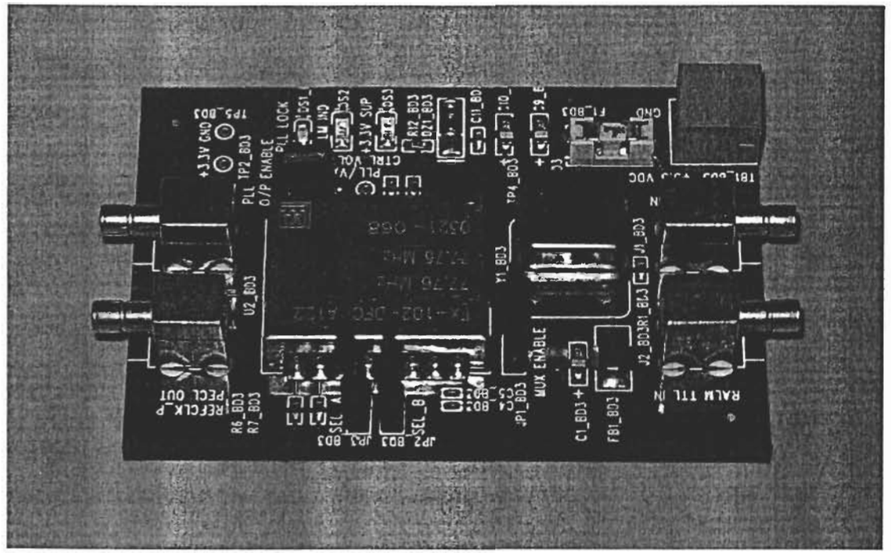

Figure 27 Assembled Looptime PLL Board

SIGNAL INTEGRITY

Signal integrity is a major issue when designing with high-speed devices and signals. There are numerous issues to consider such as impedance matching, reflections, return loss, electromagnetic interference (EMI), terminations, etc. The following describes the various signal integrity issues that were dealt with during this project.

SERIAL HIGH-SPEED LINE INTERFACE

The serial line interface of the S/UNI® MULTI-48™ device runs data rates up to 2.488Gbps. When designing at such rates, one most consider the effects of EMI, cross talk, noise, and loss.

S/UNI® MULTI-48™ has four channels and each channel has its own line interface. Channel 0, is the only channel that runs at 2.488Gbps rate. The other three channels will only run at rates up to 622Mbps. As a results, the board was designed such that channel 0 has the shortest traces to minimize the loss of the 2.488Gbps lines.

In many cases signals cannot be routed on the top layer and have to be routed on the inner layers or the bottom layers. The traces can be routed from one layer to another layer using vias. The disadvantage of vias is the added discontinuity and intrinsic inductance and capacitance to the data path. As a result, designers must try to reduce the number of vias used on the high-speed traces. For this reason the package of the S/UNI® MULTI-48™ device is designed such that the transmit and the receive pairs of channel 0 (i.e. the 2.488Gbps channel) can be routed to an SFP optical module of the top layer. Consequently, when designing the board, we routed the traces differentially on the top layer, separating them by ground pour to ensure minimum EMI effects.

For all the other serial channels, we routed the transmit signals on the top layer. Since reflections are the major issue on transmitters, added discontinuity due to vias is avoided. Also to minimize the EMI effects on the top layer, a ground pour is placed in between all the top layer high-speed traces. This ground pour is stitched to the board ground plane through numerous vias to ensure that the voltage at the plane is kept at zero and there are no localized charge-ups. Figure 28 indicates the routing of the signals on the top layer.

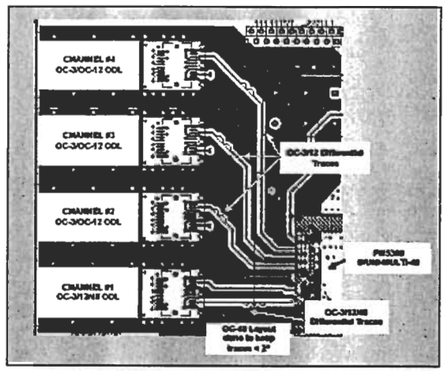

Figure 28 Layout of the Top Layer High-Speed Line Interface Traces

At the same time, the receive signals have to be routed on a different layer due to the restrictions caused by the chip ball-out. Vias usually go through the entire board stack-up. For example, for a 10 layer board, the via will go through all 10 layers. If a signal is routed from the top layer through the via to layer 4 and then after a distance is routed back up through a second via to the top layer, in addition to the discontinuity, there exists two via stubs each 6 layers deep. The added attenuation and reflections cause by the via is something that should be avoided at all costs. To get around this issue, the high-speed signals that have to be routed to a different layer through vias, must be routed as close to the bottom layer as possible. This would keep the via stubs to a minimum length and will not have significant signal integrity impacts. The best option is to route the traces on the signal layer above the bottom layer. This way, the high-speed signals are buried on a signal layer in between two ground/power planes, which gives them maximum EMI protection. The second best option is to route them on the bottom layer. In this case they will not the get maximum EMI protection, but there will be no via stubs. In case of the S/UNI® MULTI-48™ EVB, the receivers for channel 1, 2, and 3 are routed on the signal layer above the bottom layer.

Using the above techniques, we ensure that the best signal integrity is kept for the high-speed traces to guarantee best performance.

CLOCK TERMINATION CIRCUITS

PECL (Positive-referenced Emitter Coupled Logic) clocks are commonly used in today's circuits. The S/UNI® MULTI-48™ device has two PECL clock inputs. These clocks can be sourced from PECL oscillators or an external PECL source. PECL devices are widely used in our design and should always be properly terminated.

PECL (Positive-referenced Emitter-Coupled Logic) originates from ECL but uses a positive power supply. Points to remember about PECL:

1. The DC midpoint voltage is VCC – 1.3V
2. Typical signal peak-to-peak swing is VPP = 800mV
3. Output impedance is 6-8Ω□ in both LOW and HIGH states. An average value of 7Ω□ is used when doing any calculation
4. PECL can drive 50Ω transmission lines directly
5. PECL signal only sources current and never sinks current. It needs an external resistive path be provided from the output pin to VEE

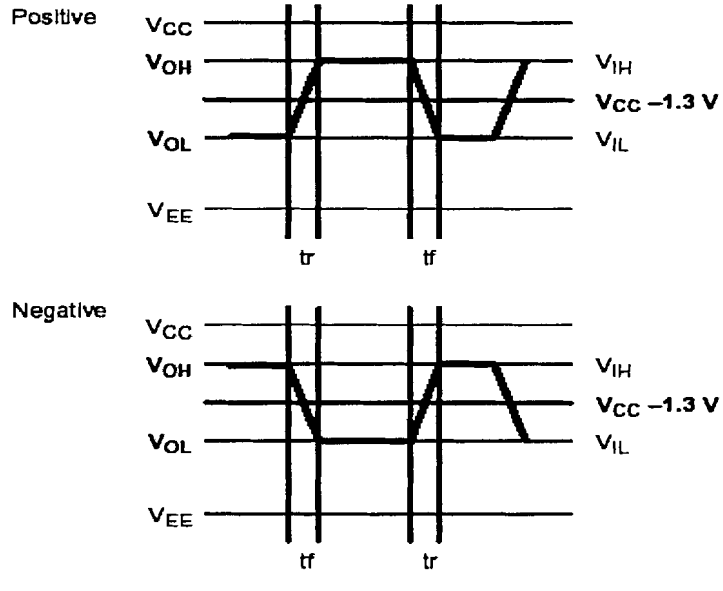

Figure 29 Waveforms of Differential PECL Signal

There are two types of PECL termination schemes:

1. DC-Coupling:

End Parallel Termination

The PECL output is designed to drive a 50Ω load to (VCC – 2V). Note that not 50Ω to ground like CMOS/TTL. The most common termination way is to put 50Ω resistors at the inputs of the receiver assuming the transmission line characteristic impedance (Z0) is 50Ω.

End Thevenin Termination

Because the potential of (VCC – 2V) power supply is usually not available for termination networks, it is often preferable to find a parallel combination of resistors that result in a Thevenin equivalent circuit. Figure 30 shows the result of the Thevenin transformation. This method eliminates the need for a (VCC −2V) supply.

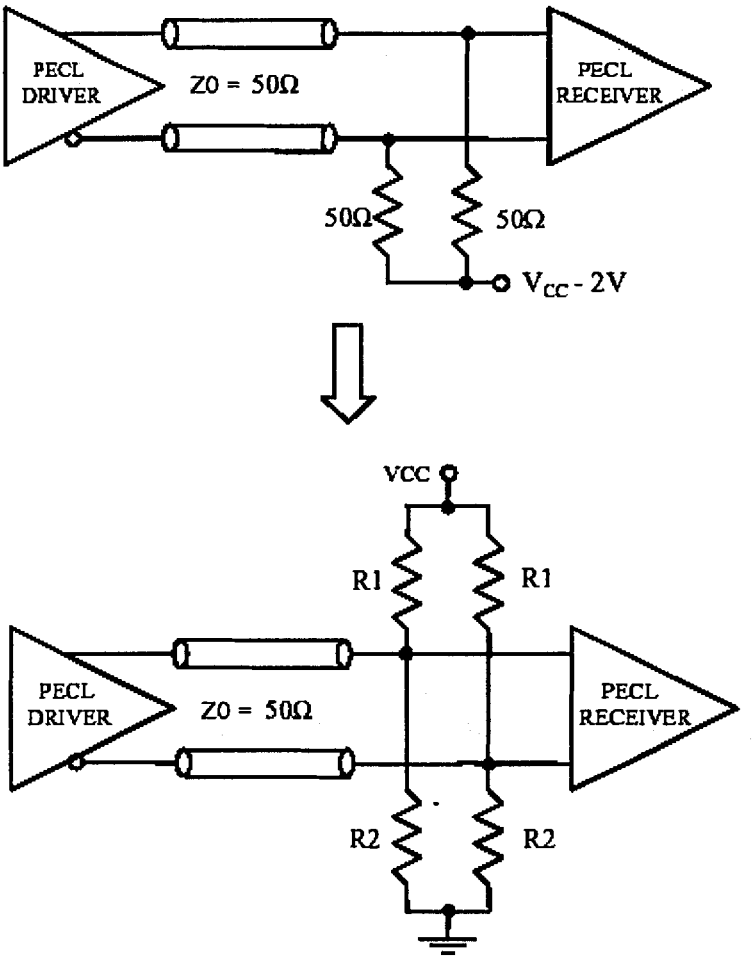

Figure 30 Thevenin Equivalent Transformation

The termination requirement of 50Ω to (VCC – 2V) impose the condition of

$$(VCC - 2V) = \frac{Vcc \times R2}{R1 + R2} \text{ and } (R1 \mid\mid R2) = 50\Omega.$$

Solving for R1 and R2 yields the following

$$R1 = \frac{50 \times Vcc}{Vcc - 2V} \text{ and } R2 = 25 \times Vcc\,.$$

Recommended values of R1 and R2 are:

- R1 = 127Ω and R2 = 82.5Ω for VCC = 3.3V

• R1 = 125Ω and R2 = 83Ω for VCC = 5.0V

2. AC Coupling

Some design applications require the PECL signals to be AC coupled due to nonstandard PECL signal levels coming from a source. One application for product validation is that they want to use a PECL clock distribution device to be interfaced to different clock sources including non-PECL compatible outputs. PECL receiver supports such applications, but there is one criteria that the amplitude of the clock input not exceed the upper or lower end of the CMR range when centered on the VBB reference.

When PECL outputs need to be AC-coupled to a 50Ω termination, a resistor from the PECL driver output to ground should be used to provide DC current return path before AC-coupling to the transmission line.

Examples below show some of the suggested solutions for the AC coupled PECL signals. When the destination device does not provide a VBB output pin for proper biasing when its inputs are AC coupled, the following scheme shown in Figure 40 can be used. For a PECL input termination R3 and R4 should be selected by the considering the following:

1. PECL input DC bias voltage should be set at (VCC - 1.3V);

2. matching the characteristic impedance of the transmission line.

$$(\text{VCC} - 1.3\text{V}) = \frac{Vcc \times R4}{R3 + R4}, \text{ and R3 } || \text{ R4} = 50\ \Omega$$

Recommended values are:

• Rt =140Ω for VCC = 3.3V and 270Ω for VCC = 5.0V

• R3 = 82Ω and R4 = 130Ω for VCC = 3.3V

• R3 = 68.5Ω and R4 = 185Ω for VCC = 5.0V

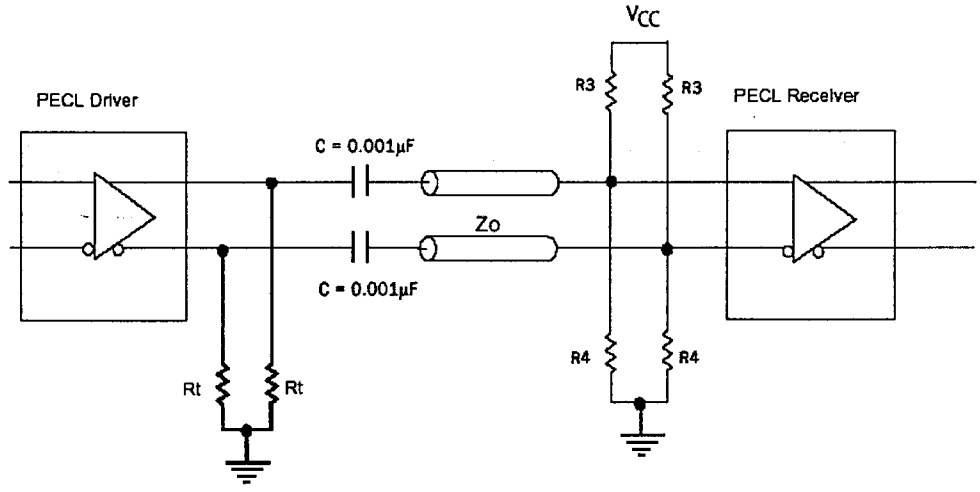

Figure 31 AC Coupling Termination without VBB Pin

When the destination device does provide a VBB output for proper biasing of its inputs in capacitive coupling mode, the solution in Figure 32 should be used for proper signal interface.

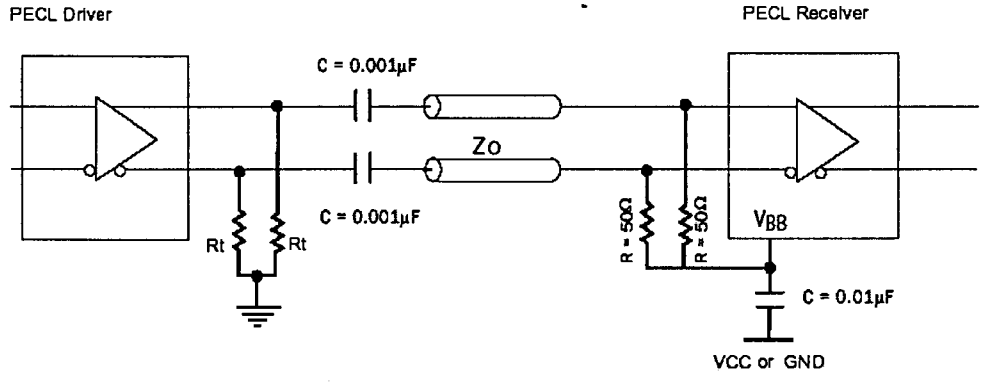

Figure 32 AC Coupling Termination with VBB Pin

PROJECT CONTRIBUTIONS AND SCHEDULE

There were two people working full time on the S/UNI® MULTI-48™ validation project. During the preparation phase I was responsible for designing the board, oversee its layout, manufacturing, and assembly processes as well as developing the software platform under the control of which the board would operate. The entire board design phase took four months to complete and the boards were ready one week before the devices were in house. Contributions from other members of product validation group, the product validation layout group, the mixed signal group, the signal integrity group, the applications group, and the product development group were key factors during the board development phase.

CONCLUSION

The hardware platform developed for the validation of S/UNI® MULTI-48™ became operational ahead of schedule and did not delay the validation efforts for the S/UNI® MULTI-48™ device. During the design phase, we had to deal with signal integrity issues, power supply design, clock circuit design, and high-speed serial interface design. All the design challenges were overcome during the development phase and the project was a success. The board served well in validating the device and the device was released to production on schedule.

REFERENCES

[1] PMC-2020735 S/UNI MULTI-48 ASSP Telecom Standard Product Data Sheet, Issue 1, September 29, 2003.

[2] PMC-2021191 S/UNI® MULTI-48™ (Multi-Rate SATURN® User Network Interface for 1x2488, 4x622, and 4x155) ASSP Telecom Standard Product Engineering Validation Board Document (EVB), Issue 3, August 5, 2003.

[3] PECL Termination Technical Documet, Tianyu Zhang, September 3, 2002.

[4] PMC-2030399 PM5360 S/UNI MULTI-48 Hardware Design Guide, Richard Stewart, Issue 1, June 2003.