DEVELOPMENT OF VTECH MINI 5.8GHZ WDCT CORDLESS TELEPHONE

by

Raymond Yuen
B.A.Sc., Simon Fraser University, 2001

PROJECT SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF ENGINEERING

In the
School
of
Engineering Science

SIMON FRASER UNIVERSITY

Spring 2005

APPROVAL

Name:	**Raymond Yuen**
Degree:	**Master of Engineering**
Title of Project:	**DEVELOPMENT OF VTECH MINI 5.8GHZ WDCT CORDLESS TELEPHONE**
Examining Committee:	
Chair:	**Paul Ho** Professor School of Engineering Science, SFU
Senior Supervisor:	**Ash Parameswaran** Professor School of Engineering Science, SFU
Senior Supervisor:	**James Cao** Baseband Development Manager VTech Engineering Canada
Date Defended/Approved:	March 23, 2005

SIMON FRASER UNIVERSITY

PARTIAL COPYRIGHT LICENCE

ABSTRACT

The VTech Mini 5.8 Ghz cordless phone is the next generation cordless phone product, which is a full featured and low cost model with small form factor. The objectives are to design and develop the product based on a reference design and begin product mass production within an eight-month time frame.

The scope of the project includes designing and verifying the product baseband circuitry and integrating the baseband circuitry with the radio frequency modules, mechanical structures, and software of the product. Within the baseband section, there are many areas covered including digital and analog circuit design, audio gain plan and acoustic design, ESD protection design, power management design, and ASIC system integration. Compliance with various industrial standards is also part of the project. The product specifically complies with FCC Part 15, Part 68, and UL and cUL standards.

ACKNOWLEDGEMENTS

I would like to express my gratitude to VTech Engineering Canada for providing me the opportunity to work on this exciting project. I would like to thank James Cao for supervising this project and also the baseband team members Hai Nguyen and Titus Cheung for working together to make this a successful project. I also would like to express my appreciation to other project members including Edwin Lange, Jose Fung, John Sharpe, and Wenkai Zhong for providing support on software, mechanical, and RF issues.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND ACRONYMS

ADC - Analog Digital Converter
ADPCM - Adaptive Differential Pulse Code Modulation
ASIC - Application Specific Integrated Circuit
ATE - Automated Testing Equipment
CID - Caller Identification
DSP - Digital Signal Processor
DSS - Digital Spread Spectrum
EEPROM - Electronic Erasable Programmable Read Only Memory
ESD - ElectroStatic Discharge
FCC – Federal Communications Commission
FFT - Fast Fourier Transform
FSK - Frequency Shift Keying
GND - Ground
HSF - Handsfree
ITAD - integrated Telephone Answering Machine
LED - Light Emitting Diode
PCB - Printed Circuit Board
ROLR - Receiver Objective Loudness Rating
RX - Receive
SINAD – Signal to Noise Ratio And Distortion
SMD - Surface Mount Device
SOLR - Sidetone
SPI - Serial Peripheral Interface
STH - Silver ThroughHole
TDD - Time
TDMA - Time Division Multiple Access
TOLR - Transmit Objective Loudness Rating
TX – Transmit
UL – Underwriters Laboratories
WDCT – Worldwide Digital Cordless Telecommunications

1 INTRODUCTION

VTech Engineering Canada Limited is one of the world's leaders in the cordless telephone industry. It is also a key player in the electronic learning product market and the electronic toy market. VTech Engineering Canada Ltd. is a subsidiary of VTech Telecommunications, which has a design center in Richmond to design 2.4GHz and 5.8 GHz cordless telephones.

The project is to develop a new WDCT cordless phone system using hybrid 5.8 Ghz/2.4 GHz technology. The Mini product emphasizes on the small form factor, system expandability, and cost effective bill of materials. The product design stages include designing the rendering, mechanical structures, radio module for establishing air link, baseband circuitry to support audio and user features, software including design MMI, and ATE setup for testing the products during mass production

The products are designated with the model numbers shown in Table 1.

Table 1 : Model Designation

	MI6821	MI6861	MI6820
Base Unit	1 Basic Base	1 Base with Integrated Telephone Answering Device (ITAD)	NA
Handset	1 Handset	1 Handset	1 Handset

The Mi6821 is the basic model which comes with a base unit and a handset. The Mi6861 model comes with a base with integrated ITAD and a handset. The Mi6820 is the optional accessory handset for linking to any Mi6821 or Mi6861 system. Both the Mi6821 and Mi6861 systems can have 4 handsets registered simultaneously.

The focus on this report is on the baseband design portion and will have limited exposure to the other aspects of project. The objectives are to develop the complete baseband circuitry based on a reference design to fit in the cosmetic rendering designed by the industrial designer. Full design verification was performed to ensure compliance with FCC and UL safety standards which is mandatory. Finally, the design has to be robust to have high manufacturability and cost effective since high volume production is expected for this product line.

Within the baseband section, there are many areas covered including all digital and analog circuit, audio gain plan and acoustic design, ESD protection design, power management, and ASIC system integration.

1.1 WDCT Technology

WDCT technology is the North American wireless communication standards for cordless phones. WDCT employs Time Division Multiple Access (TDMA) and Digital Spread Spectrum (DSS) technologies. The TDMA system allows sharing of the radio channel by dividing the channel into time slots. In WDCT, there are 4 TX slots and 4 RX slots within each cycle to allow 4 handsets to be used at the same time or time diversity of data transfer. The time diversity is to ensure the data integrity during poor radiation environment or extended range. The DSS

technology is used to divide the radio transmission and reception to different frequencies channels. The technique used in the product is referred as frequency hoping. The frequency channel used at any given time is different since the system is hoping between different frequency channels within the band limit for data transfers. A specific hoping pattern is specified on different WDCT systems to minimize the chances for interference.

The hybrid 5.8 Ghz/2.4 Ghz technology offers advantage of the low power consumption of the 2.4 Ghz technology and the range advantage of the 5.8Ghz technology. The transmitting frequency on the base uses the 5.8 Ghz band where the transmitting frequency on the handset uses the 2.4 Ghz for lower power consumption on the handset, which is running on battery packs. The hybrid technology allows the talk time of the handset to increase compared to a conventional 5.8 Ghz technology.

2 BASE UNIT

The base unit is a wall-powered unit that interfaces with the public telephone line. It consists of a radio module used to communicate with the handsets. There are also visual indicators on the base to signal the status of the base. A charging cradle is incorporated to the base to provide battery charging capability when the handset is cradled. For the model equipped with digital answering machines (ITAD), the ITAD user interface, microphone, and speaker are located on the base.

2.1 Cosmetic Renderings

The cosmetic renderings for both models emphasize on the compact and slim shape and lines. On The Mi6861, the base also provides access to all the features of the ITAD through the keypad. The cosmetic rendering for the MI6821 base is shown in Figure 1.

Figure 1: MI6821 Rendering

The cosmetic rendering of the MI6861 base is shown in Figure 2

Figure 2: MI6861 Rendering

2.2 High Level Block Diagram

The high-level block diagram of the base is shown in Figure 3. Each functional block will be discussed in this chapter.

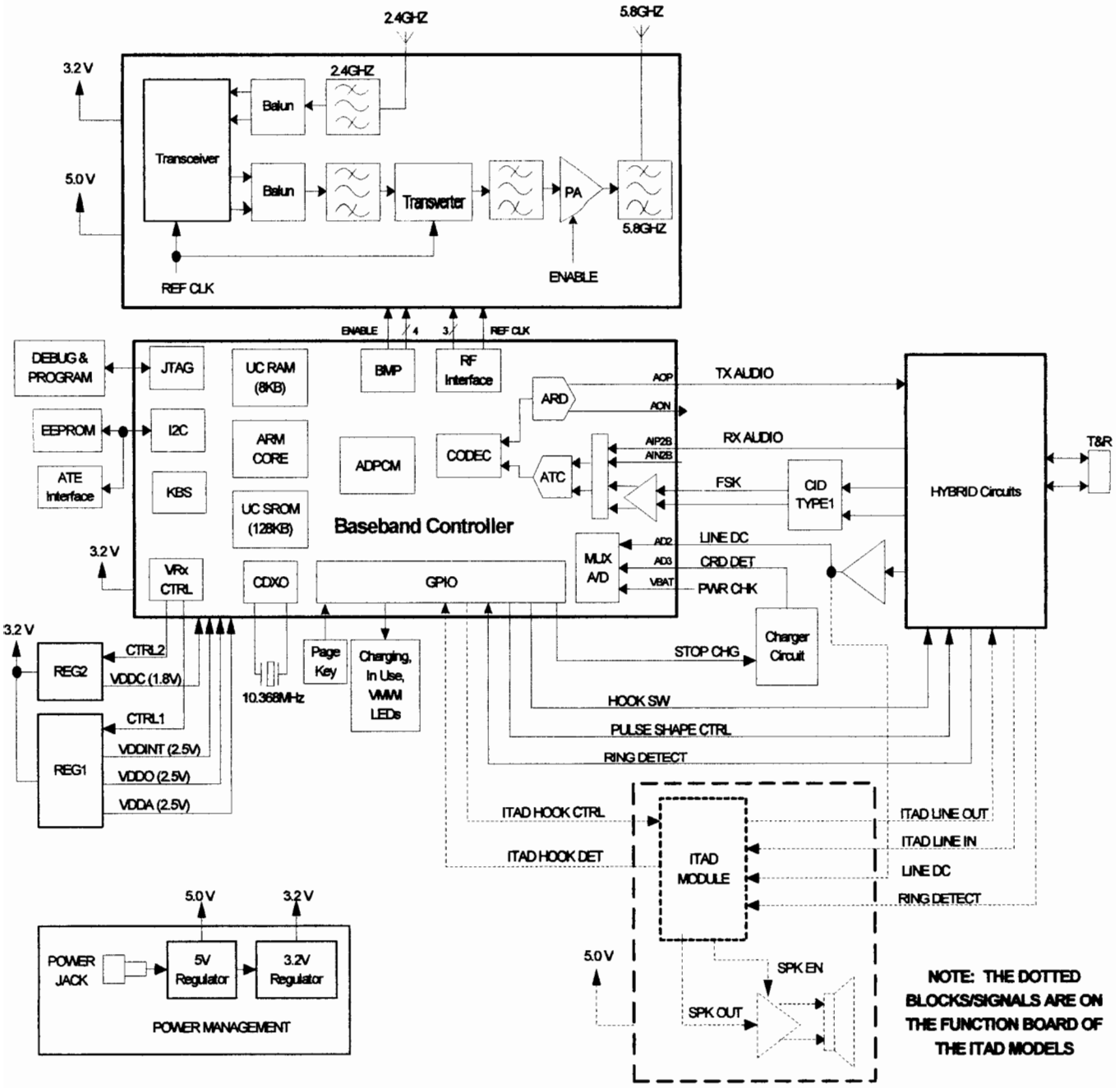


Figure 3: High Level Block Diagram For Base

2.2.1 Power Management

The general overview of the power management scheme on the base is shown in Figure 4.

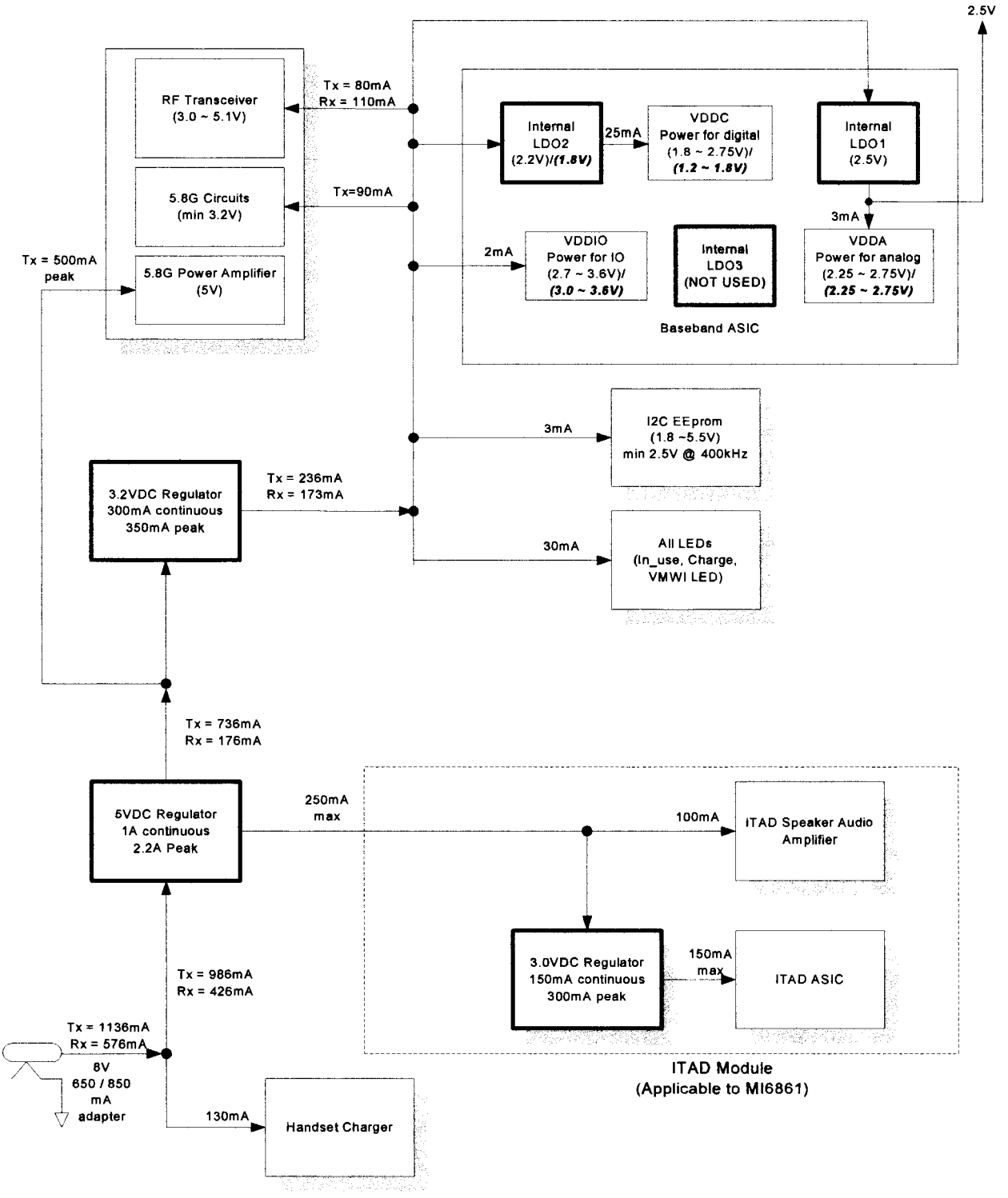


Figure 4: Power Management Scheme for Base

2.2.1.1 VDD - 5V

A high current rated 5V voltage regulator is used to supply power to the RF Power Amplifier and the function board to power the ITAD circuitry on Mi6861. This regulator is also providing power to other regulators in the system. The 5V regulator for the basic model is rated at 1A and the one for ITAD model is rated for 1.5A to support the additional current draw from the ITAD circuitry. The input to the regulator is connected to the 8V DC adapter. The regulator has to maintain the output voltage with input voltage below 7V during peak current consumption period. Another key concern on this regulator is the heat dissipation on the regulator during high current draw time and causes the surface temperature on the base to rise. Heatsink on PCB and external heatsink provision are implemented to control the heat dissipated to the enclosure.

2.2.1.2 VDDIO – 3.2V

The 3.2V regulator is an adjustable voltage regulator that can provide 300mA max current continuously. The output voltage is controlled by the two resistors, R1 and R2, on the reference voltage pin. The output voltage can be calculated by the equation:

$$Vo = Vref\,(R1 + R2) / R1 \qquad \text{where } Vref = 1.235V$$

There is about 2% of tolerance on the voltage output when the input voltage is at least higher than the output voltage. This voltage is fed to VDDIO pins of the ASIC to supply for all I/O ports, EEPROM, LEDs, and circuitry inside the RF module.

2.2.1.3 VDDA, VDDINT and VDDO -2.5V

These voltages are regulated from 3.2V supply by the internal regulator control inside the ASIC. All of these voltages have its nominal voltage of ~2.5V. VDDA is used to supply the analog domain inside the ASIC, EEPROM, all LEDs, and audio amplifiers. VDDINT is to supply the internal flash memory and VDDO is the supply to the on-chip oscillator of the ASIC.

2.2.1.4 VDDC - 1.8V

The voltage is regulated from 3.2V supply by the internal regulator control inside the ASIC. This voltage is used to supply the digital core in the ASIC.

2.2.1.5 DC Power Adapter -8V

The DC power adapter used for the Mi6821 base is rated at 8V with 650mA current. The Mi6861 base power adapter is rated at 8V and 850 mA of average current. The extra current capacity in the Mi6861 model supports the operation of the ITAD, user interface and speaker and microphone. These adapters rating will provide operation of the unit from 100VAC up to 125VAC.

2.2.1.6 Battery Charging Circuit

The battery charging circuit on the base is powered directly from the 8V adapter. The circuit is a constant current source delivery about 130mA to the handset through the cradle contacts. The circuit is basically a current mirror consisting of high current 2 NPN bipolar transistors and the circuit is also controlled by the baseband ASIC. When a power

dropout is detected, the charging circuit will be disabled by the ASIC to prevent further loading of the power source. Special precaution was also made to prevent the circuit from oscillation since prior experience showed that the circuit could become unstable during certain conditions and emit excessive digital emissions.

2.2.1.7 PCB Power and Ground Connections layout

The power and ground connections are separated using the scheme shown in Figure 5. The grounding scheme of the system can be divided in into AGND, DGND, RFGND, HGND, PWRGND (5VGND and 3V2 GND) and ITADGND. Different grounds are all summed at the DC adapter source ground. AGND is the reference ground for all the audio circuitry and it is critical to be isolated from other grounds. DGND is the ground for all the digital circuitry in the system including the ASIC digital core, EEPROM and it is a ground pour on the PCB. RFGND is the reference ground for the RF module which is routed directly to the source ground since it is the current return path of the high current RF power amplifier. HGND is the reference ground for the hybrid circuitry which interfaces with the telephone line. ITADGND is the reference ground for the ITAD module in Mi6861 model and should be routed separately to the source ground since it is the current return path for the speaker amplifier circuit. PWRGND is the reference for all the regulators on the system and should have solid connection to the source ground.

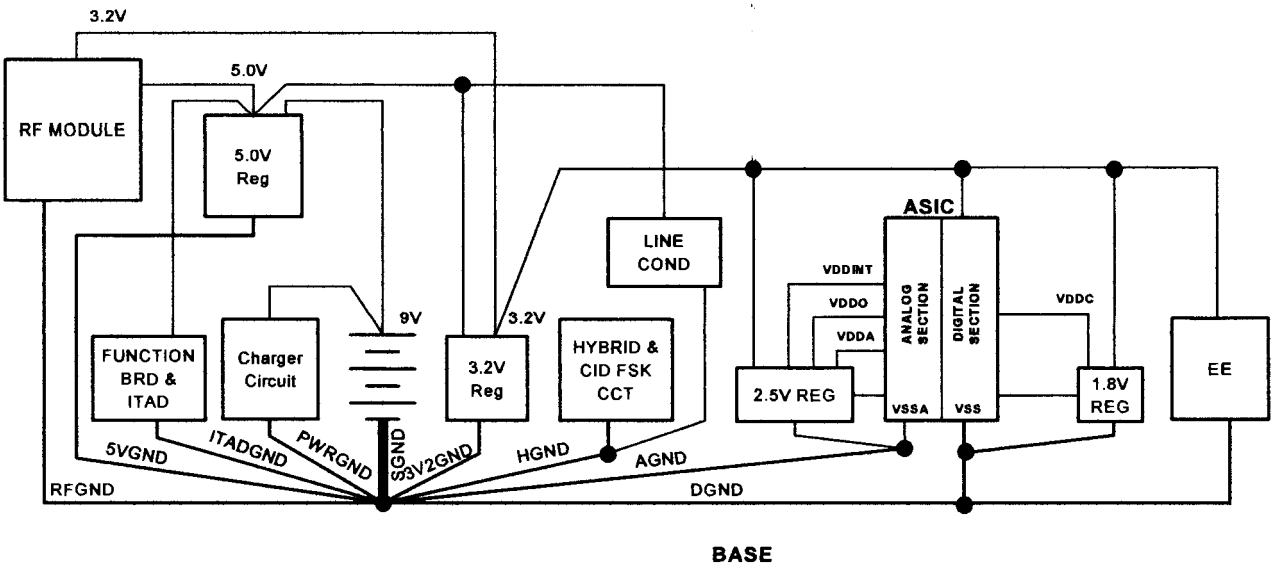


Figure 5: Power and Ground Connections for Base

The grounding of the system is a major factor of the noise induced in the audio path and will also greatly affect the ESD performance. By using the grounding scheme, a low noise electrical environment can be achieved to provide a stable noise-free platform.

2.2.2 System Controller - Baseband ASIC

The baseband ASIC is integrated to provide all the features required for WDCT wireless device which otherwise have to be implemented using discrete solutions. The baseband ASIC consists of a ARM cored microcontroller, ADPCM codec engine, audio and FSK interfaces, internal voltage regulators, GPIO and serial interfaces, Burst mode controller and RF interfaces dedicated for WDCT.

The ASIC has the following hardware features:

- Embedded 32-bit microprocessor
- ARM7TDMI RISC controller featuring extremely low mW/MHz,
- 69 MHz core clock speed guaranteed over full specification range
- Program memory
- 128 KB ROM
- Data memory
- 8 KB SRAM
- Microprocessor interfaces:
- 19 general purpose I/O-pins
- Keyboard scanner (KBS) interface
- IIC interface (up to 400 kbaud)
- SPI interface
- Buzzer interface
- Embedded digital signal processor (DSP) subsystem
- Embedded flexible burst mode processor
- RF Interface
- Embedded ADPCM Codec

2.2.3 Drop Out Detect Circuit

The purpose of this circuit is to reserve power while a power dropout event occurs. The way to achieve this is using a voltage level detector to monitor the adapter voltage. Once the adapter voltage drops to a predefine threshold, the /DROPOUT_DET signal goes low to the ASIC. Upon receiving a logic low, the ASIC will disable all LEDs and the charging circuit immediately to minimize current draw on the adapter. There is also an enable bit in EEPROM to disable the whole software detection algorithm. Because of software implementation, if the /DROPOUT_DET signal is held low while inserting the adapter, the Base will not power up properly. Therefore a pull-up resistor must be connected to this signal to provide the proper logic state for startup.

2.2.4 Hybrid

The hybrid circuit is the interface between the public telephone line and the audio circuitry in the base. The design of this hybrid is taken from IP5825 series model. A simplified diagram shown in Figure 6 illustrates the design of hybrid TX circuit. The TX gain is set to +10dB and can be roughly calculated as:

$$\text{Gain (dB)} = 20_{\log} (900//600)/110$$

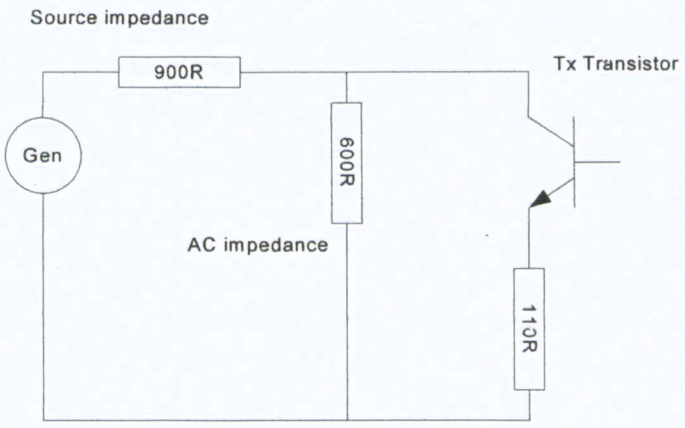


Figure 6: Simplified Illustration of Hybrid RX

The frequency response of the transmit path in the hybrid is shown in Figure 7.

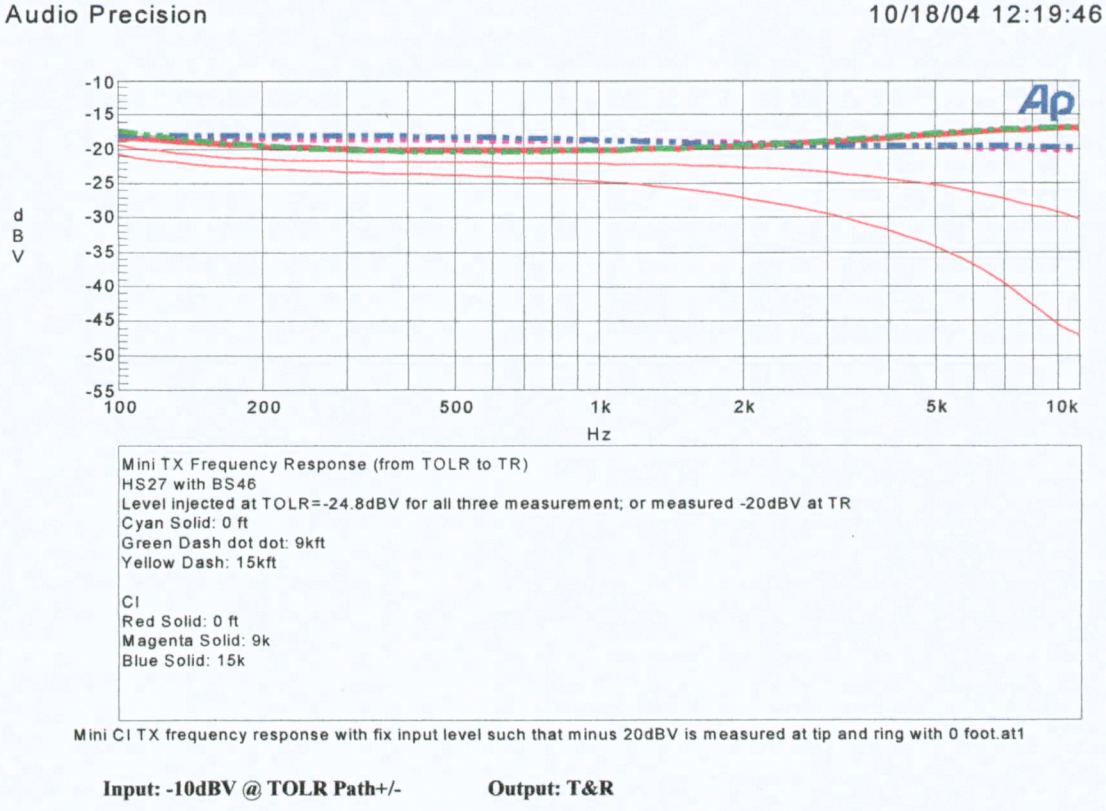


Figure 7: Hybrid TX Frequency Response

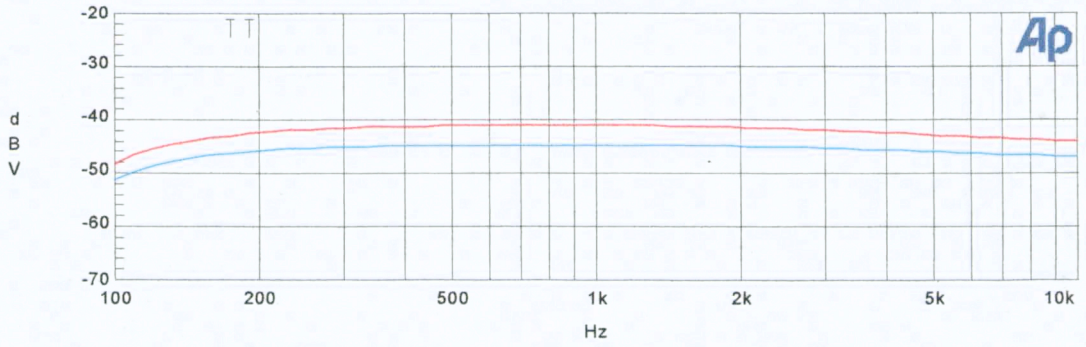
As shown in the diagram, the TX frequency response is flat for Mi6821. For Mi6861, the frequency response starts to roll off at around 2K- 3KHz due to the loading of the ITAD module on the line. Different line lengths also have an effect on the frequency response of the hybrid. The three line lengths tested are 0KFt, 9KFt and 15 KFt.

The AC impedance of the base is determined by 600R load on the line. When the phone goes off-hook, most of the loop current will flow through 600R load. Therefore the power rating of resistive load must be high enough to dissipate the power.

The Rx chain is simply a resistor divider consisted on a 10k and a 470R resistor. The gain in Rx direction is therefore calculated to be:

$$\text{Rx Gain (dB)} = 20 \log .47 / 10.47 = -27\text{dB}$$

The actual gain is measured to be about -21dB because there is some resistance in parallel with the 470R resistor. The overall Rx gain from the line to ASIC inputs is shown in Figure 8. The hybrid RX frequency response is flat across the frequency range for both Mi6821 and Mi6861 models



Color	Line Style	Thick	Data	Axis
Cyan	Solid	1	Anlr.Ampl	Left
Red	Solid	1	Anlr.Ampl	Left

Mini RX freq response with TR measurement = -20dBV when offhook
Measured at ROLR_PATH_P
CI
0: Cyan Solid
9k: Green Solid
15k: Yellow Solid

C
0 Red Solid
9k Magenta Solid
15k Blue Solid

CI sidetone and RX.at2

Input: -20dBV @ T&R **Output ROLR Path+/-**

Figure 8: Hybrid RX Frequency Response

The sidetone comes from the feedback to the RX from the TX within the hybrid.

The net sidetone gain is measured to be at least –10dB across the frequency band. The sidetone frequency response is also known as the transhybrid response. A transhybrid response is crucial to provide a good echo free hybrid on a telephone system. The transhybrid frequency response is shown in Figure 9.

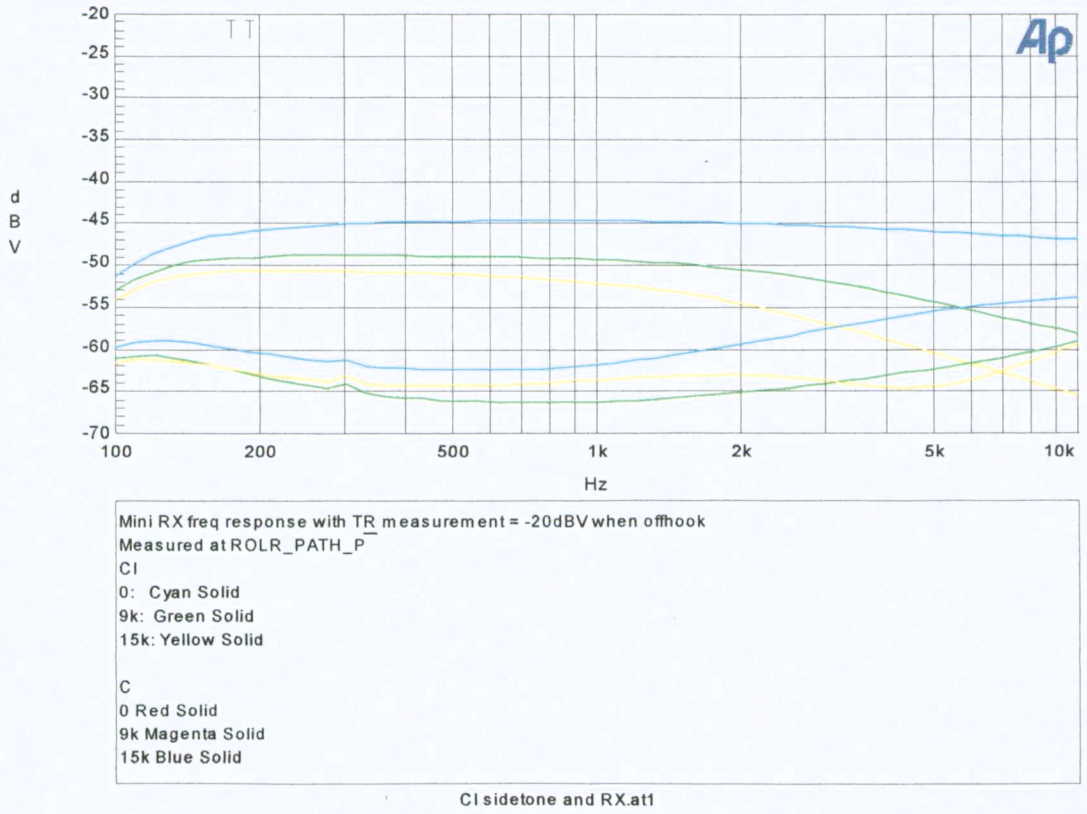


Figure 9: Transhybrid Response

In the hybrid circuit, the hook switch is implemented by a high voltage/current transistor circuit. The hook switch is controlled by the ASIC. When the phone is off hook, the circuit provides 600 Ohm impedance to ground. When the phone is onhook, the circuit provides greater than 15 Mohm impedance to ground. This is used to control the onhook and offhook impedance to the network.

A pulse shaping circuit is implemented to the hybrid to provide pulse-dialling capability for compatibility with older telephone systems. This is done by introducing a load to the signal line and creates the desired pulse response. The ASIC has control on this circuit to allow user to select between tone and pulse dialling via the handset user interface.

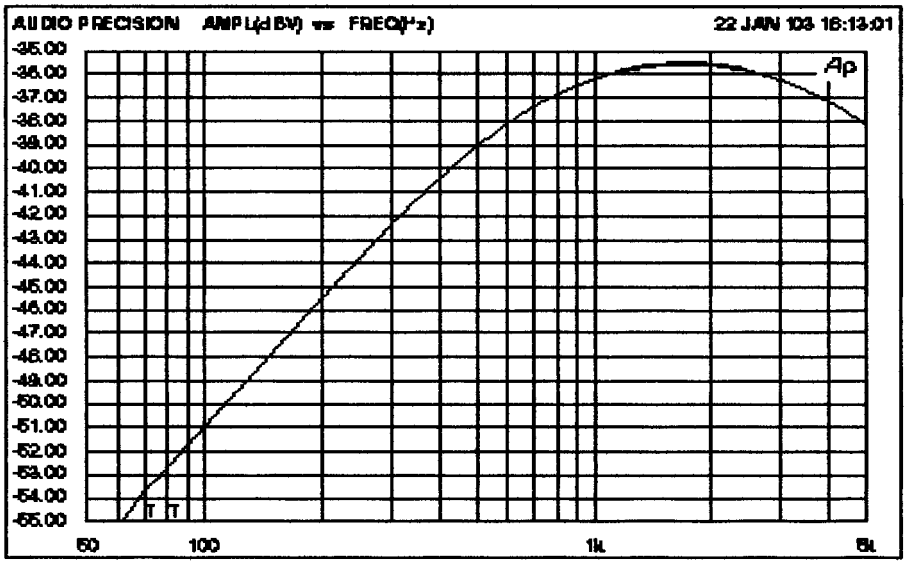
2.2.5 Ring Detect Circuit

The ring detect circuit only looks at the positive peak of the ring signal. The ringing voltage threshold is set by a voltage divider then fed to a transistor switch. The output of the amplifier is connected to an ASIC GPIO. The software will measure the signal and calculate the ringing frequency if it is between 15 and 68Hz.

2.2.6 FSK Circuit

CID information is sent present on the telephone line after the first ring. The information is modulated using Frequency Shift Keying (FSK). FSK uses 2 frequency ranges to signal a logic 0 and a logic 1. The 1188Hz—1212Hz is known as the Mark frequency which signals a logic 0 and 2178Hz—2222Hz is known as the Space frequency which signals a logic 1. The mark and space level are between -12 dBm and -36 dBm.

The FSK circuit uses the op-amp inside the codec2 inputs and some discrete components to form a differential-to-single op-amp design. The specific circuit also acts as a filter to only let the FSK frequencies to pass through and provide a gain of –26dB with 0dB twist. The twist is defined as the difference in level between the mark and space. The frequency of the FSK circuit is shown in Figure 10.



Input = -10dBV @ T&R Output = CID_In+ or CID_In-

Figure 10: FSK Circuit Frequency Response

It also provides more than 40dB attenuation @ 60Hz to avoid the codec being saturated with high 60Hz noise on the telephone line.

2.2.7 Line DC Circuit

The line DC circuit is a single-ended input op-amp with input-output ratio of 10:1. It is powered from 5V through a resistor divider to provide 3.9V at the op-amp. Since the op-amp maximum output is around Vcc – 0.8 V to Vcc –1 V, the maximum output level will be 3.1V which is below the maximum input level on the ADC. The input high frequency cut-off is 14.5Hz so it is basically a dc attenuator and will filter out any ac signal. The input impedance must be greater than 15M ohm to meet the DC on hook impedance spec. The output voltage is fed to an ADC input to determine the line status from the 4 different states: on-hook, off-hook, no line and parallel set off-

hook. Table 2 shows the threshold for the line status detection that the ASIC uses to decide the current line status. These parameters are stored in EEPROM and can be optimized if needed for different networks.

Table 2: Line Voltages and Conditions

Line Status	DC Voltage
On Hook	> 13V
No Line	< 1.5V
Off hook	>1.5V and < 13V
Parallel Set	0.5V change on line voltage when phone is off hook
Extension in Use	0.5V change in line voltage when phone is on hook

2.2.8 VDDC Delay Start-Up Circuit

In order for the ASIC to power up reliably, the VDDC voltage must be at least 0.8ms after VDDA. The following plot shows the power up profile of VDDA and VDDC. VDDC is about 1ms delay after VDDA is stable. A simple RC transistor switch circuit is designed to buffer the voltage regulation in order to provide the required delay. Figure 11 shows the VDDC startup characteristics. The startup delay for VDDC measures to be about 2ms after VDDA is stable.

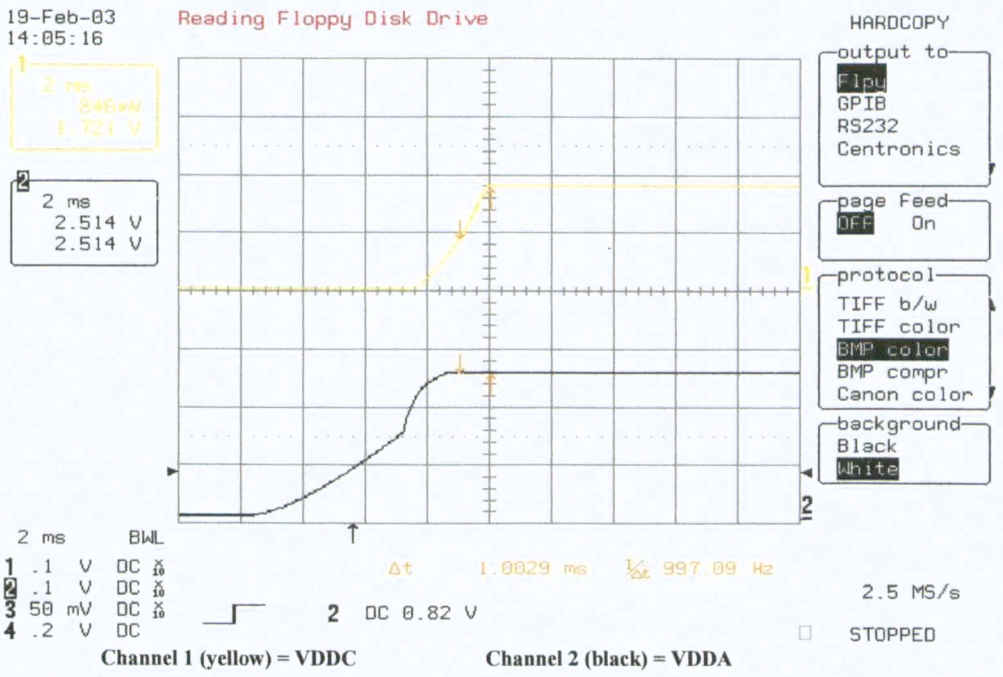


Figure 11: VDDC Startup Characteristic

2.2.9 EEPROM

The base consists of a 64 Kbit EEPROM to store various data requiring non volatile storage. Data include calibration and registration data, tuning parameters, frequencies hoping tables, audio gain plan parameters, battery charging parameters, and phone book and CID log data. All the data stored in the EEPORM can be accessed through the 2-wire I2C interface by the ASIC. The access protocol to the EEPROM is careful design to prevent data corruption during sudden power loss.

2.2.10 Crystal Oscillator

The crystal oscillator used on the handset runs at 10.368MHz. For the crystal oscillator to run at the correct frequency, the oscillator circuit must load the crystal with the correct capacitive load. If the capacitive load is less than what the crystal was designed for, the oscillator runs faster and vice versa. On the other hand, the higher capacitive load will have more current consumption.

The loading capacitance of 15pF was chosen for the design to intentionally make the crystal runs slightly faster than the desired frequency. The reason is to provide a tuning capability for the handset when it runs through Automated Testing Equipment. The ATE tunes the crystal frequency by adjusting the internal loading capacitor banks in the ASIC to adjust the frequency to the desired value.

2.2.11 Cradle Detection

Cradle detection is done by a resistor divider attached to the cradle contact to derive a voltage level to an ASIC ADC input. The ASIC ADC has 8 bit resolution and has a 2.5 V dynamic range. The ASIC will compare this voltage with the thresholds set in EEPROM to determine the status of the cradle. When an On-cradle event is detected, the ASIC will turn on the 'CHARGE' LED by toggling a GPIO port. When the cradle contacts are disconnected, the ASIC will turn off the 'CHARGE' LED after a preset debounced time of 3 seconds.

2.3 ESD Protection

ESD protection is a major focus on handheld products since they are more susceptible to ESD damage than other electronic products. VTech ESD specification is to pass +/- 15kV air discharge to any part of the unit and will not cause any damage or reset/lockup conditions. Furthermore, the unit also has to meet +/- 8kV contact discharge and will not cause any damage or reset/lockup conditions. In order to meet the ESD requirement, various circuits are used in both the base and handset to channel ESD energy efficiently to prevent damage or reset/lockup conditions.

ESD protection can be done in combinations of electrical and mechanical protection. In mechanical protection, the opening of the chassis should be at least 10mm away from any electrical components including the PCB. If sufficient clearance cannot be provided, a plastic wall should be added and yield the same effective travel distance of 10mm. In keypad or LED area, the components or PCB should be fully encapsulated with the rubber keypad or the LED lens to prevent any discharge to any component.

Electrically, ESD energy is diverted to the telephone line or a solid ground plane to maintain the stability of the baseband circuits. There are only few locations on the base that would attract ESD discharge. They are the cradle contacts, telephone line jack and power line jack. On the Mi6861, the discharge location also includes the speaker. In order to protect these locations from ESD discharges, different design techniques are used. The cradle contacts are connected to the telephone line through a high voltage capacitor to couple the ESD charge directly to the telephone line. On the telephone line, there are inductors placed in series to provide impedance. The speaker is connected to the speaker

amplifier on the function board. To prevent ESD energy to damage the speaker amplifier, a pair of zenor diodes is placed on the speaker lines to ground. Also, series inductors are used to provide impedance to dissipate the ESD energy.

Since ESD energies can be dissipated to the ground of the system, it will create a momentary potential difference between different grounds in the system and caused the ASIC to have different potential reference at different pins. This will cause the ASIC to reset or lockup. In order to resolve this issue, a 10N cap is placed between the AGND and DGND of the system to couple the ESD energy such that the ground will bounce at the same rate during an ESD discharge.

2.4 UL/FCC Requirement

Since the base is connected to the public telephone line and the AC power line, it has to meet the safety standard of UL and FCC Part68. Furthermore, the system also has to comply with FCC Part 15 as a wireless device.

2.5 ATE Testing

ATE testing is important to ensure all products from the production line are fully tested and verified before shipping. Thorough testing of the system is time and manpower consuming. Therefore ATE testing is implemented to increase efficiency of testing the units. Various test points are implemented on the PCB to provide access for ATE station to measure different parameters of the system. Main tests for ATE testing include all voltage levels and current consumption, all audio path levels, frequency responses,

distortions and SINADs, RF power levels, and functionality of all other circuits. Clock frequency tuning and RF deviation tuning are also done in ATE testing stations. The ATE station communicates with the unit under testing through an I2C interface and generates specific testing commands to the unit. The unit under test will execute the specific command under test mode.

2.6 PCB Layout

The PCB layout on the base is designed using a FR1 double sided Silver TroughHole (STH) technology. The main advantage of the technology is the low cost structure and process. The drawback includes the moderate via size and non plate through process which is challenging for high density PCB design. To overcome the space concern on the base motherboard using STH technology, components have to be placed on both sides in order to provide enough placement area. The placement is carefully designed in a modular approach to meet all the mechanical constraints and electrical requirement.

All the surface mount devices (SMD) are placed on the top side and all the throughhole components are placed on the bottom side. With this configuration, only 1 process is needed to assemble all the components onto the PCB. The process used is a 2-step wave soldering technique where the PCB with components glued in place is placed through a wave soldering machine. The first step in the process is for soldering all the SMD components and second step is for soldering all the throughhole components.

As discussed in the power management section, the different ground and power flows are also implemented on to the layout. They are implemented with the appropriate trace width and via numbers to allow sufficient current capacity.

Another important design rule used is that all the audio traces and high speed clock signals are shielded with their respective ground which will minimize noise and crosstalk induced from other signals.

3 CORDLESS HANDSET UNIT

The wireless handset provides a text based user interface through the LCD to access all the handset features. Aside from the normal audio receiver, it also features a speakerphone mode to let the user stay on a call in handsfree operation. A 2.5mm headset jack is provided for using a wired headset. The unit also features a 50-entry phone book and a 30-entry call log. The handset is capable of providing 10-hour talk time and 4.5 days standby time with a 3.6V 600 mAH battery pack.

3.1 Cosmetic Rendering

The rendering of the handset is shown in Figure 12. The handset small form factor is also a new feature across the VTech product offerings.

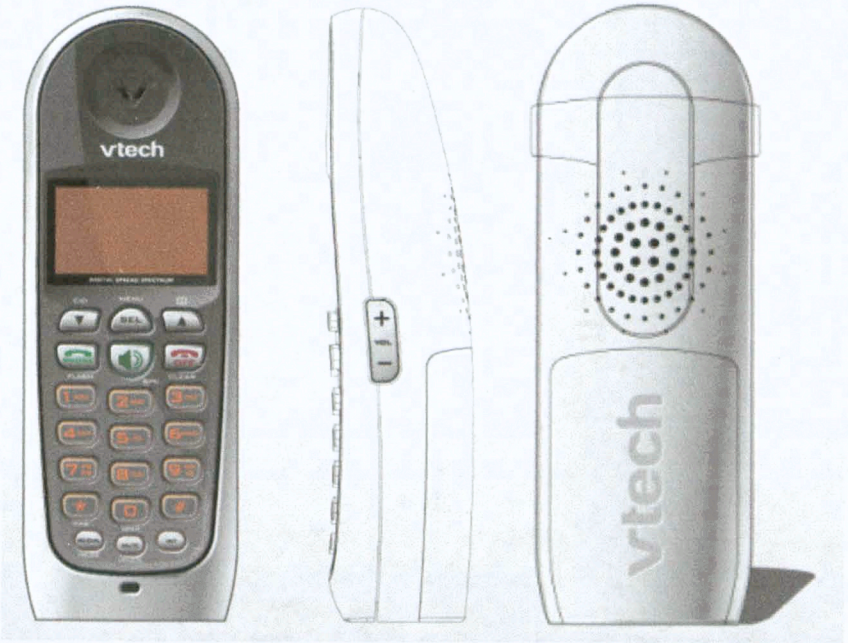


Figure 12: Mi6820 Rendering

3.2 High Level Block Diagram of the Handset

The high level block diagram for the handset is shown in Figure 13.

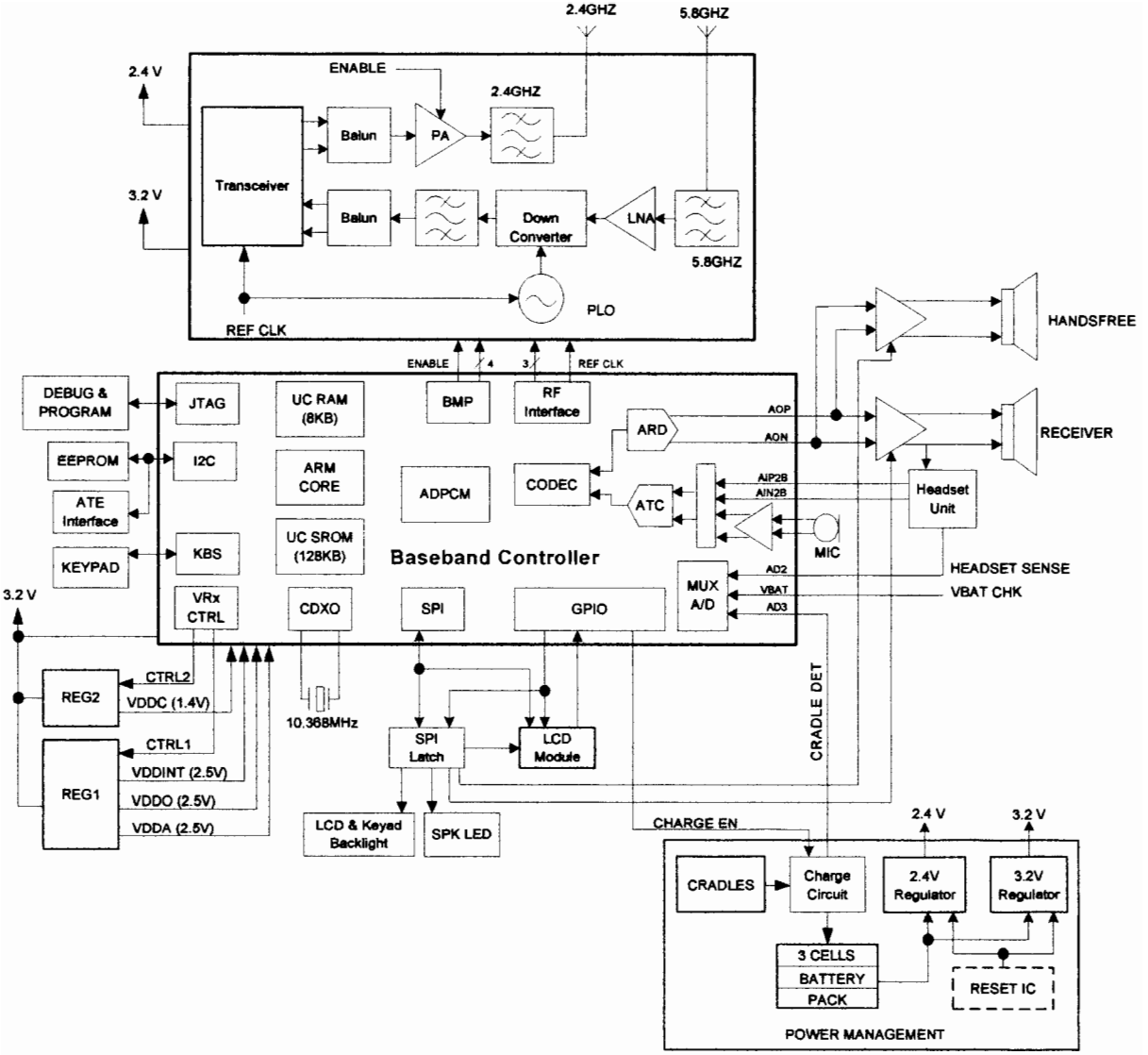


Figure 13: High Level Block Diagram for Handset

3.2.1 Power Management

The power management on the handset is carefully designed to yield the required talk time and standby time. Figure 14 shows the power management scheme of the handset

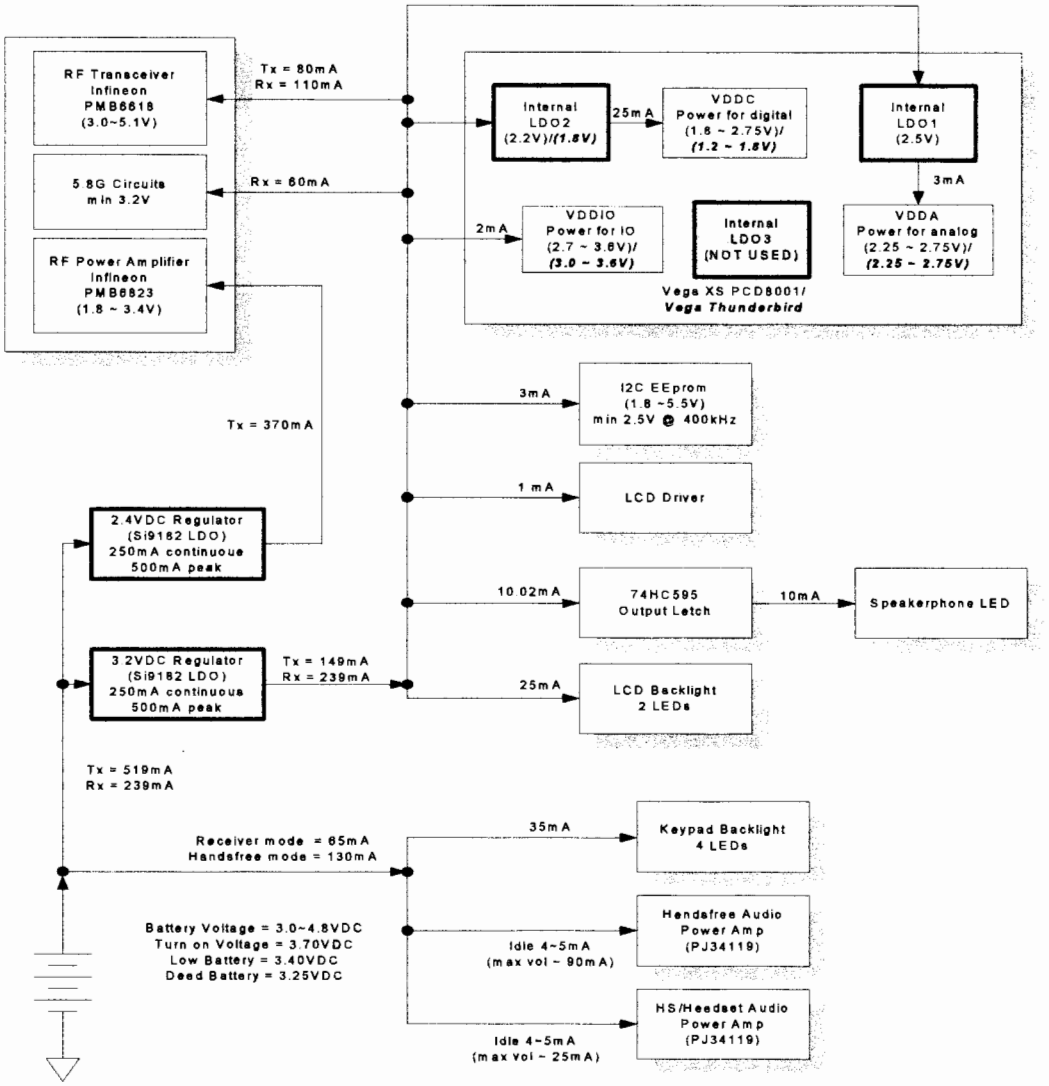


Figure 14: Power Management Scheme For Handset

3.2.1.1 VDDIO – 3.2V

The VDDIO – 3.2V regulator is an adjustable voltage regulator. It can provide up to 500mA peak and 300mA of current continuously. The output voltage is controlled by two feedback resistors, R1 and R2. The output voltage can be calculated as follows:

$Vo = (R1 * Vref) / R2 + Vref$ where $Vref = 1.215V$

The output voltage of this regulator is fed to VDDIO and VDDC pins of the ASIC to supply all the analog and digital circuitry. It also supplies the LCD module, EEPROM, 74HC595 latch, LCD Backlight, speakerphone LED, and the RF module's transceiver and 5.8 Ghz circuitry.

3.2.1.2 RFVDD - 2.4V

The RFVDD – 2.4V regulator is an adjustable voltage regulator. It can provide up to 500mA peak and 300mA of current continuously. The output voltage is controlled by two feedback resistors (R3 and R4). The output voltage can be calculated as follows:

$Vo = (R3 * Vref) / R4 + Vref$ where $Vref = 1.215V$

This regulator is dedicated to supply only the RF Module's Power Amplifier.

3.2.1.3 VDDA, VDDINT, and VDDO

These three voltage rails branch from the 2.5V rail, which is regulated from the 3.2V supply. This 2.5V supply rail is controlled by an internal regulator control 1 in the ASIC,

VDDA (VDD Analog) supplies the analog circuitry of the ASIC. VDDO (VDD Oscillator) supplies on-chip oscillator of the ASIC. VDDINT supplies the internal flash memory

3.2.1.4 VDDIO

This VDDIO (VDD Input/Output) rail is directly connected to the 3.2V regulator's output. This VDDIO rail mainly supplies the digital I/O pins of the ASIC.

3.2.1.5 VDDC (1.8V)

The VDDC (VDD Core) voltage is regulated from 3.2V supply by the internal regulator control 2 (VR2). This voltage is used to supply the digital part (ARM & DSP) of the ASIC.

3.2.1.6 Power and Ground Connections

Similar to the base, the power and ground connections are carefully layout for optimum noise performance. Figure 15 shows the power and ground connections on the handset

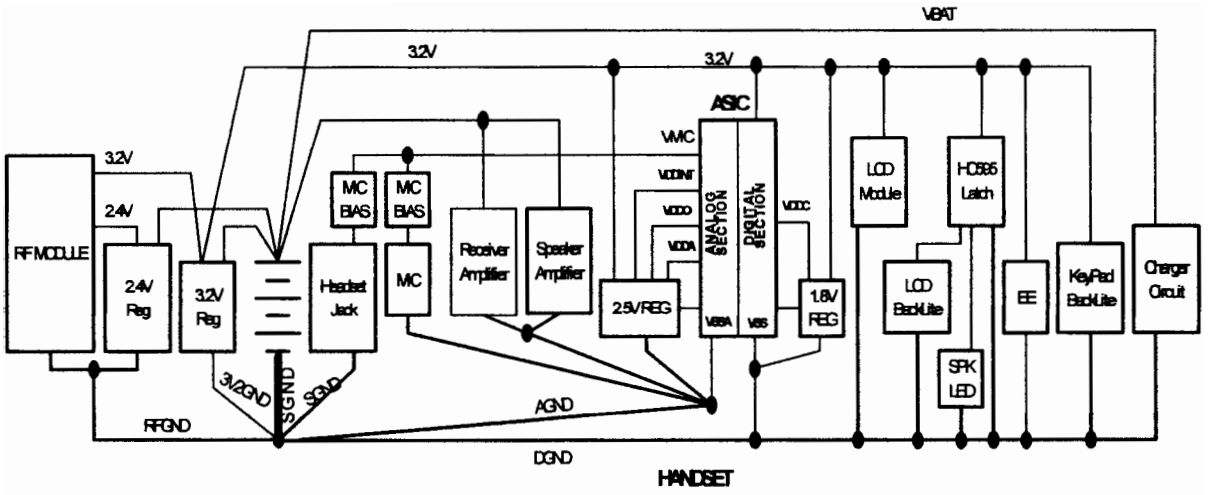


Figure 15: Power and Ground Connections For Handset

3.2.2 Batteries

The main supply of the handset is a three-cell AAA 600mAH NiMH battery pack. The battery pack contains a fuse to prevent damages from short circuit. The battery voltage powers all the regulators and supplies keypad backlight, Handsfree speaker, and earpiece receiver.

3.2.3 Baseband ASIC

The handset shares the same baseband controller ASIC with the base. The only difference is the software running in it. The handset ASIC is configured to run at a higher clock rate to provide the power needed to support the handset operations. Please refer to Section 2.2.2 for more information on the Baseband ASIC.

3.2.4 Shift Register (74HC595)

Due to limited I/O pins available on the ASIC, an external SPI shift register, 74HC595 is required to provide more outputs. The 74HC595 shift register IC controls the keypad backlight, LCD backlight, speaker LED indicator, LCD reset signal, receiver amplifier enable, and handsfree speaker amplifier enable signal.

The serial peripheral interface (SPI) control signals for the shift register IC are shared with the LCD module. In order to multiplex and SPI bus between the register and LCD, a GPIO (LCD/Latch_Sel signal) is used to select the bus master. The shift register IC accepts the serial data when the "LCD/Latch_Sel" signal goes from low to high and the LCD accepts the serial data while this signal is held high. In order words, the register is edge triggered by the LCD/Latch_Sel signal and the LCD is level triggered by the same signal.

3.2.5 LCD Module

The LCD module on the handset is a COG module with SPI interface. It uses a low-cost character-based LCD driver. The LCD can display two rows of 16 characters wide and one additional row, which contains date, time, and some special icons. The LCD module is powered from the 3.2V power rail.

3.2.6 LCD Backlight

The LCD backlight is required to light up during any key press. These LEDs are powered are driven directly from two of the shift register's outputs through series current

limiting resistors. Because the shift register IC can have different manufacturers, the driving current can vary. It is very important to pay attention to the luminous intensity of the LEDs if the shift register IC were to change.

3.2.7 Keypad

Due to the small size of the handset, it was not possible to integrate the keypad into the handset main board. A separate keypad board was designed and it uses STH technology to minimize material cost. They keypad is made of rubber with carbon pills. All keys will be coated with a metal paint and laser etched.

Because the keypad is arranged in a triangle matrix configuration, eight I/O pins can support up to 28 keys. The major advantage for this configuration is that it can support a lot more keys than the conventional keypad configuration (4x4 = 16 keys). A drawback is that the key information is only evaluated if exactly one key is pressed at a time. If several keys are pressed simultaneously, none of them will be recognized until only one key remains pressed. A 220-ohm resistor is added in series with each signal lines to prevent the I/O pins from being damaged from ESD discharge.

The key mapping can be changed and it is an EEPROM setting. For instance, if the function of the "On" and "Off" keys has to be swapped, it can be done by changing contents of EEPROM without a software change.

3.3 Crystal Oscillator

The crystal oscillator used on the handset runs at 10.368MHz. The circuit is identical to the base oscillator except it uses a SMD crystal instead due to the limited area on the handset. Please refer to Section 2.2.10 for more information of the crystal oscillator circuit.

3.3.1 EEPROM

The handset uses a 16Kbit EEPROM which uses I2C protocol. The EEPROM is used to store configurable parameters such as RF parameters, volume controls, ring tones, audio gains, battery charging parameters, etc.

3.3.2 Audio Circuitry

The handset audio circuitry is an integration of microphone, receiver, headset and handsfree speakerphone. The microphone circuit for the handset is biased by VMIC supply and it is driven differentially into the ASIC's Microphone Amplifier (AIP2 and AIN2). This signal level is then adjusted appropriately and routed to the audio paths inside the ASIC. When the headset jack is plugged in, the audio path to the handset's receiver is disconnected and the headset's receiver is then connected. The headset's microphone circuit is biased in a similar fashion as the handset's microphone. The VMIC supply voltage for the microphones (2.0V) is supplied by the ASIC's VMIC pin.

The handsfree speakerphone circuit uses differential audio outputs from the ASIC's AOP & AON pins. It is amplified and filtered by a high power speaker driver before passing

the audio signal to the speaker. The speaker amplifier can output up to 3dBV with 3.2V supply.

The receiver circuit uses the same differential audio outputs as the speakerphone circuit. It is amplified and filtered separately a different speaker amplifier with less power compared to the handsfree speaker driver. The audio signal is then drive the receiver on the handset or on the headset. The receiver amplifier can output up to -2dBV with 3.2V supply.

Since both amplifiers have the Chip Disable control, software has the ability to enable and disable the drivers depending on the user's selection. When the handsfree speaker is in use, the handset receiver is disabled and vice versa. Only one amplifier will be enabled at a time.

3.3.3 Ringer and Key Beeps

The handset uses the handsfree speaker to produce the ringer tones and key beeps. Upon detecting a ring signal, a ringer tone is sent to the speaker through the handsfree audio path. The speaker amplifier IC is enabled and the ring signal is amplified and filtered. The key beep is done the same way, only replacing the ring tone with the key beep.

3.4 Battery Charging Algorithm

The charging algorithm can be summarized in the block diagram in Figure 16. The basic algorithm is that when a handset is placed on cradle, it will first estimate the battery

capacity based on the battery voltage and then it selects the appropriate charge time and duty cycle (called charge zone). The battery voltage is divided into 6 zones. In each voltage zone, a charge time and charge duty cycle is specified. While previous models uses pulse charging technique to charge the battery, we generally feel that this is not a good way to charge the battery because the test results show that it does not effectively charge the battery. It was decided to use continuous charging with specific charge duration based on the battery voltage. The current charge setting is as follows:

Zone 1: If battery voltage < 3.50V, charge continuously for 10 hours.

Zone 2: If 3.50V <= battery voltage < 3.70V, charge continuously for 9 hours.

Zone 3: If 3.70V <= battery voltage < 3.82V, charge continuously for 7 hours.

Zone 4: If 3.82V <= battery voltage < 3.95V, charge continuously for 5 hours.

Zone 5: If 3.95V <= battery voltage < 4.25V, charge continuously for 3 hours.

Zone 6: If 3battery voltage > 4.25V, trickle charge at 23% duty cycle forever.

The settings above are optimized based on experimental data. Zone 6 is set to 23% duty cycle trickle charge to supply just enough current needed for the handset in standby mode and compensate for the self-discharge problem of the battery.

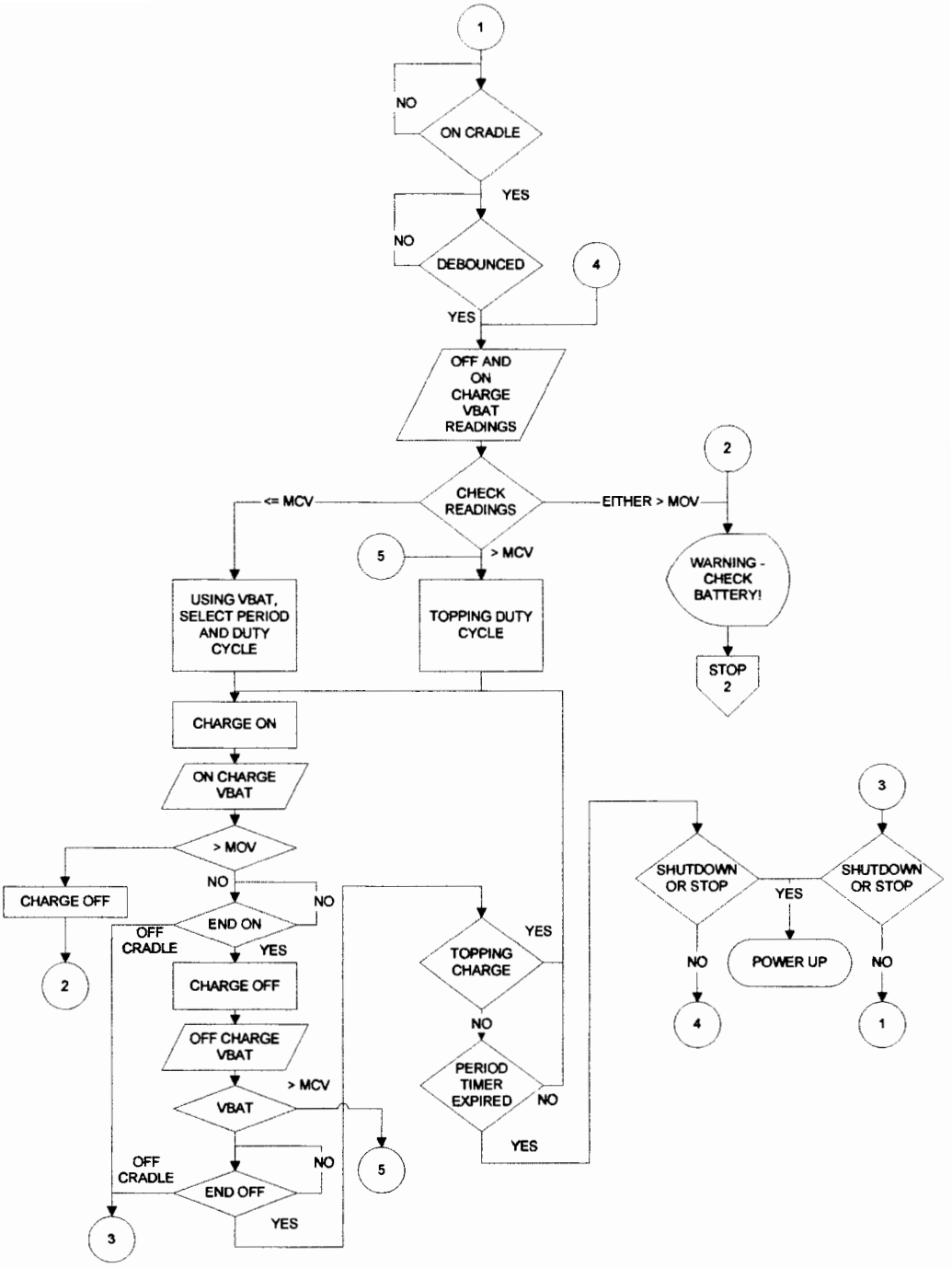


Figure 16: Battery Charging Algorithm

3.4.1 Battery Charger Circuit and Control

The handset senses the on-cradle event by checking the cradle voltage by an ADC port through a voltage divider circuit. This circuit is used to scale down to cradle voltage to ensure that it does not exceed the maximum allowable range of the ADC. Similarly, the handset monitors the battery voltage by an ADC port through a voltage divider circuit, which connects to the battery terminals. This battery voltage information is used to determine the charging behaviour of the handset.

When the handset is placed on cradle, a constant current of approximately 150mA is supplied from the base (or from the standalone charger, if it's placed on the standalone charger) to charge the battery pack. Out of this 130mA, the handset's charger circuit consumes approximately 5mA and the handset itself consumes an additional 20mA. So the net current which charges the battery is only about 100mA. To fully charge the battery, approximately 9 hours is needed.

This battery charger circuit is controlled by the ASIC's GPIO port. In the case where the battery voltage is very low (below 2V), the state of this pin can be at any logic. If it happens that this pin is at logic low when the battery is low, the charger circuit will be disabled and the battery won't be able to charge up. To prevent this dead-lock situation, a bypass mechanism is employed. The charger circuit uses the "Error" pin of the RF PWR regulator to force it to turn on regardless of the ASIC control pin's state. This error pin will turn on the handset charger circuit when the battery voltage is below 2.3V. Once the handset powers up, it will enable the charge control, start the charge timer, and select

the appropriate duty cycle. The handset continuously monitors the battery voltage and determines when to switch to the trickle charge.

3.4.2 No Battery Detection

If there is no battery inside a handset or the battery connection is not properly made, the handset could still power up when it is placed on cradle. This is because when the charge circuit is turned on, the voltage at the cradle contacts is transferred to the battery voltage rail. This voltage can be enough to turn on the handset and it be as high as 5.6V. A protection zenor diode is used to clamp the battery voltage down to 5.6V in case there is no battery installed.

Operating at this voltage is undesirable because the components that are connected to the battery voltage rail can be damaged due to high voltage. To prevent the components from damaging, a safety feature is implemented. As soon as the handset powers up, it will immediately check for the battery voltage. If the battery voltage is above the "Maximum Operating Voltage", the handset will display "Warning – Check Battery!" on the LCD, disable the charge circuit, and halt all operation. The idea here is to prevent drawing current from the components that are connected to the high battery voltage rail. In this condition, the handset will keep recycling the power until either the handset is taken off cradle or the batteries are installed.

3.4.3 Overcharge and Undercharge Conditions

The battery charging algorithm estimates the battery capacity based on the battery voltage level. This estimation can be totally wrong because the battery voltage level does not always represent the real battery capacity. A clear example of this is in charging an old battery. Because the internal resistance of old battery can be a lot higher than new battery, when it is being charged, its voltage increases very rapidly and could rise very high, but its capacity is low. This section discusses the situations where the handset could over/under estimates the battery capacity, resulting in under/over charge the battery.

It is important to note that in charging mode, the battery voltage does not rise up linearly for the duration of the charge time. It is rises up very quickly in the first hour of the charge time, after which it settles and rises up slowly for the rest of the charge time. The same can be said for discharging mode (whether in talk or standby mode). The discharge voltage is non-linear and is most pronounced right after charge when the battery holds full capacity.

Because of the characteristics above, overcharge or undercharge conditions occur when the handset under/over estimates the battery capacity. The parameter settings for the charging time and duty cycle for each battery voltage zones are described in section 3.4 above.

For undercharge condition, it can happen when users charge a handset with dead batteries for one hour then re-cradle the handset. Because of the fast voltage rise, after one hour of charge time, the battery voltage can be as high as 4.1V. When the handset is re-cradled,

Zone 5 will be selected because the battery voltage falls within Zone 5 and so the battery will be charged for only 3 hours. For some handsets, trickle charge (Zone 6) will be selected after Zone 5 is completed because the battery voltage is within Zone 6.

For overcharge condition, it can happen when a user uses a handset with fully charged battery for 30 minutes, then re-cradle the handset. Because of the fast voltage drop, the battery voltage can be as low as 4.2V after 30 minutes. When the handset is re-cradled, Zone 5 will be selected and the battery will be overcharged for about 2.5 hours.

To illustrate the charging characteristics, a charging curve is shown in Figure 17.

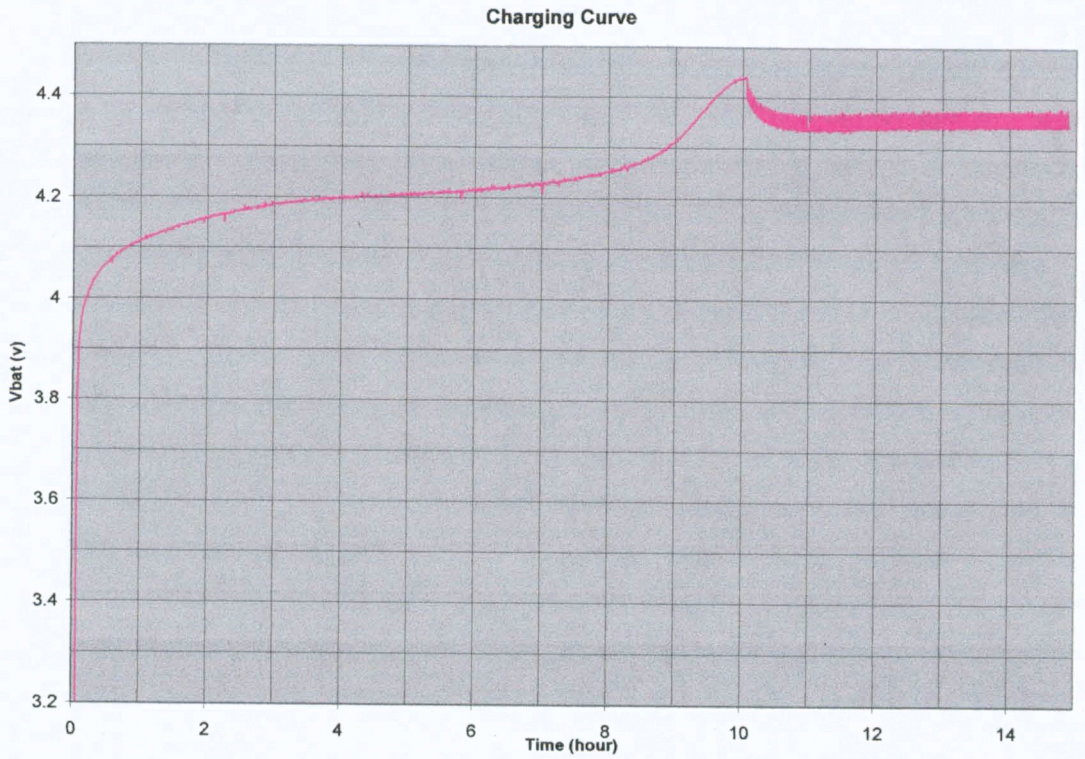


Figure 17: Battery Charging Curves

3.4.4 Talk mode, and standby mode

An important performance figure for handheld battery devices are standby and talk time. The actual talk and standby times depend on the condition of the battery as well as the current consumption of the handset. In general, 10 hours of continuous talk time and 4.5 days of standby time can be archived with the power management scheme of the handset.

Figure 18 shows the discharging curve of the battery during talk mode. As observed from the graph, the calls were terminated when the voltages dropped below 3.3V and the talk time ranges between 9- 10.5 hrs

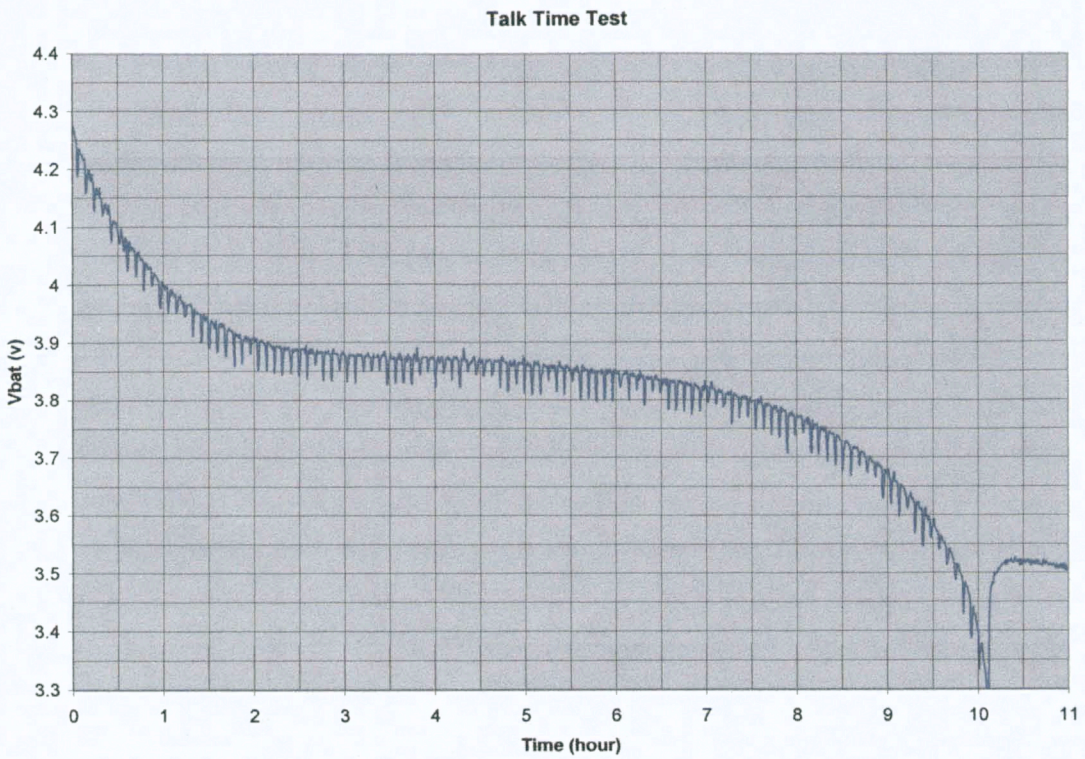


Figure 18: Battery Discharge Curve - Talk Mode

Figure 19 shows the discharging curves of the batteries during standby mode. The handset will enter low battery mode when the voltages dropped below 3.2V and the standby times range from 4 – 5 days.

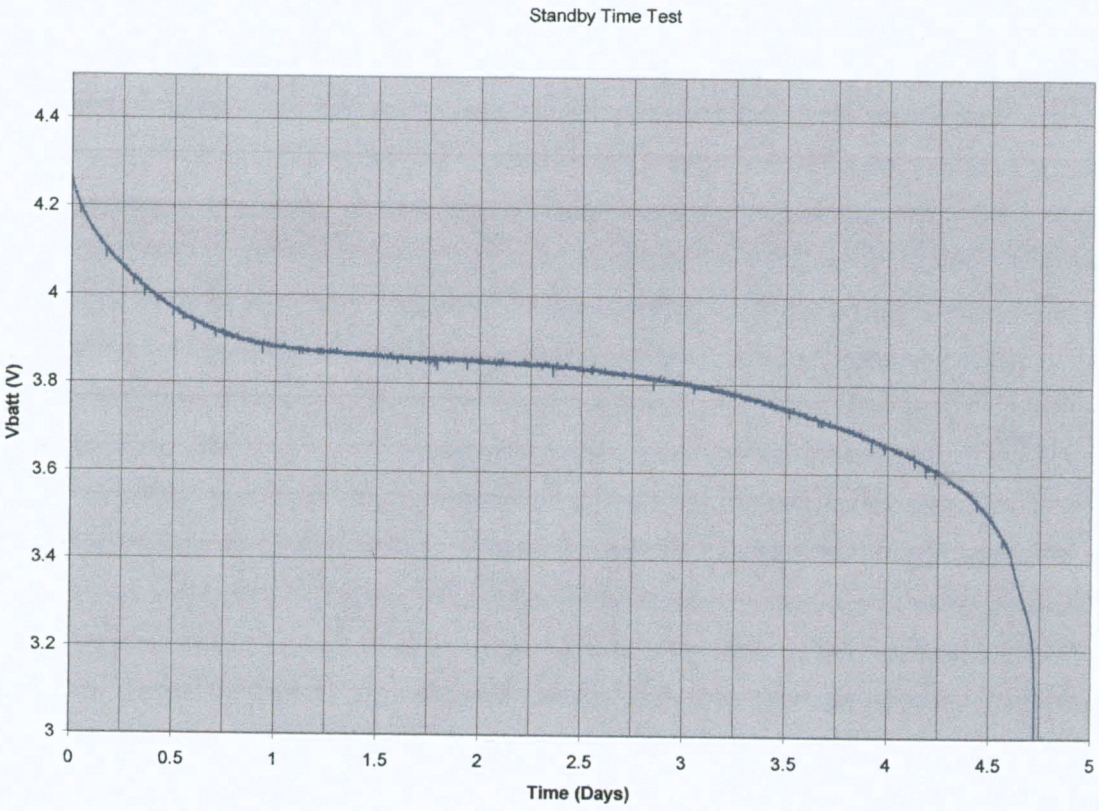


Figure 19: Battery Discharge Curve - Standby Mode

3.5 ESD Protection

For the handset, ESD is a major concern since the ESD energy cannot be channelled to the telephone line power line like on the base. Instead the ESD energy is dissipated to the system ground, the energy is often dissipated to the battery or the ground of the circuit.

There are many ESD protection techniques implemented in the design to prevent component damages and system reset and lockup. Using caps to couple ESD energy to GND, zenor diodes and ferrite beads are also used to minimize the voltage potential seen by the ASIC during an ESD hit. Alternatively, a small series resistor on signals can be used to dissipate ESD energy delivered to IC.

ESD rings are layout on the edges of PCBs to attract ESD discharge since ESD ring are connected to GND and lower impedance to GND than other signal traces and ESD energy will be divert to a lower potential destination through the least impedance path. An example of the ESD ring on the handset is shown in Figure 20.

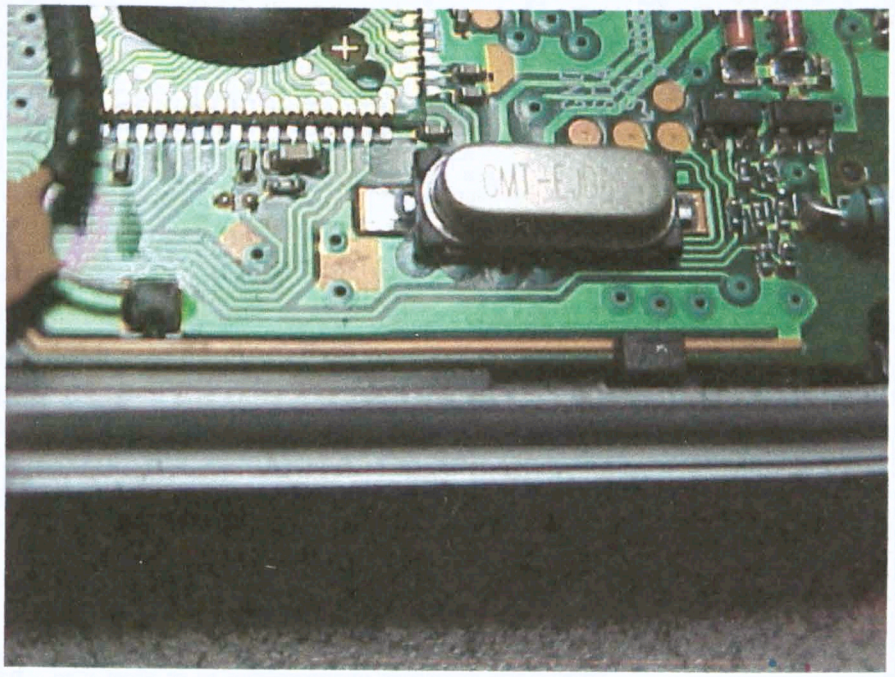


Figure 20: ESD Ring on Handset

During an ESD hit to the system GND, the ground plan bounces to an absolute higher potential due to the excessive energy. However, the ground bounce might not be at the same rate at different ground of the system and hence caused the ASIC to see difference reference grounds to cause a reset.

3.6 PCB Layout

The handset PCB layout uses the FR2 STH technology similar to the base PCB. Since the handset is smaller in form factor compared to the base, all SMD components are used to utilize the PCB area effectively. A separate keypad PCB is used for the key decals in order to provide a double sided placement of components for the motherboard. The

keypad PCB is connected to the motherboard using flat flex cable. Otherwise, the general techniques used in the layout are similar to the base motherboard.

4 ACOUSTIC AND AUDIO GAIN PLAN

Acoustic and audio gain plan design is a main portion of the project design. There are 3 modes supported in the handset. They are the normal handset mode with receive audio from the receiver and transmit audio through the microphone, headset mode with receive and transmit audio through the headset, and handsfree speakerphone mode where the receive audio is from the speaker and transmit audio still shares the normal microphone. With 3 different audio profiles, different gain plan has to be designed to accommodate different operating conditions.

4.1 DSP Audio Features

Within the DSP core of the ASIC, different functional blocks are available for processing the audio data and provide the phone features.

A pair of ADPCM, ITU-U G.711 CODEC engine is built in to the ASIC DSP. Basically, they are hardware blocks adjacent to the analog to digital converter on the audio path that performs compression and decompression of the data. The compression/decompression algorithms uses 8 bit A-law or u-law PCM data format to compress/decompress the audio at 32kbps.

An automatic volume/gain control block is used to adjust the gain on the audio signal automatically to ensure the output audio is at a non-clipping level when the input varies

dramatically. The ACV basically takes PCM audio data and analyze the level. The level estimation is aligned to the active speech by eliminating noise that might appear on the audio signal. Base on this estimation, the ACV will increase or decrease the gain on the signal to maintain the overall nominal level of the signal.

The half-duplex handsfree block is used when the handset is in speakerphone mode. The half-duplex handsfree block switches the direction of the audio and ensure the smoothness of the audio is maintained., The switching is decided based on the comparing level of the RX audio and TX audio and will switch to the direction with higher level. Based on the switching mechanism, the AGC TX AGC will ramp up during TX and ramp down during RX and vice versa for the RX AGC.

A local echo canceller (LEC) is used to eliminate the echo at the near end when the transmitted audio is reflected by the hybrid circuit due to the mismatch to the network. The LEC basically compares the received signal with the transmitted audio and cancel the part of receive audio that is determined to be echo. The LEC is a running dynamically to adapt to different audio signals and conditions.

A network echo suppresser (NES) is used to suppress or minimize the far end echo observed on the other end of the telephone line. The NES is a fixed parameter echo suppresser with the attenuation and echo delay set at 9/12 dB and up to 10ms. The NES operates by taking the receive audio as input and selectively suppress transmit audio to minimize echo.

Various filters in the DSP block are also available for fine tuning the audio response.

4.2 Normal handset Mode

In the normal headset mode, audio is full duplex which means audio is simultaneously transmitted and received. The receive audio is driven to the receiver enclosed in an acoustic chamber. The acoustic chamber design is modelled using a Helmholtz resonator approach. The Helmholtz resonator design is based on a defined resonant frequency decided from the form factor of the acoustic chamber. The resonant frequency and the frequency response of the receiver will yield the actual frequency response of the receive audio. Figure 21 shows the receiver frequency response for various line lengths, 0kFt, 9kFt, 15kFt. The line length simulates the effect of the unit being at a distance away from the CO. This acoustic response is measured in a sealed environment that means the receiver and chamber of the unit is sealed to the microphone of the test equipment. This sealing is critical to obtain the actual acoustic response.

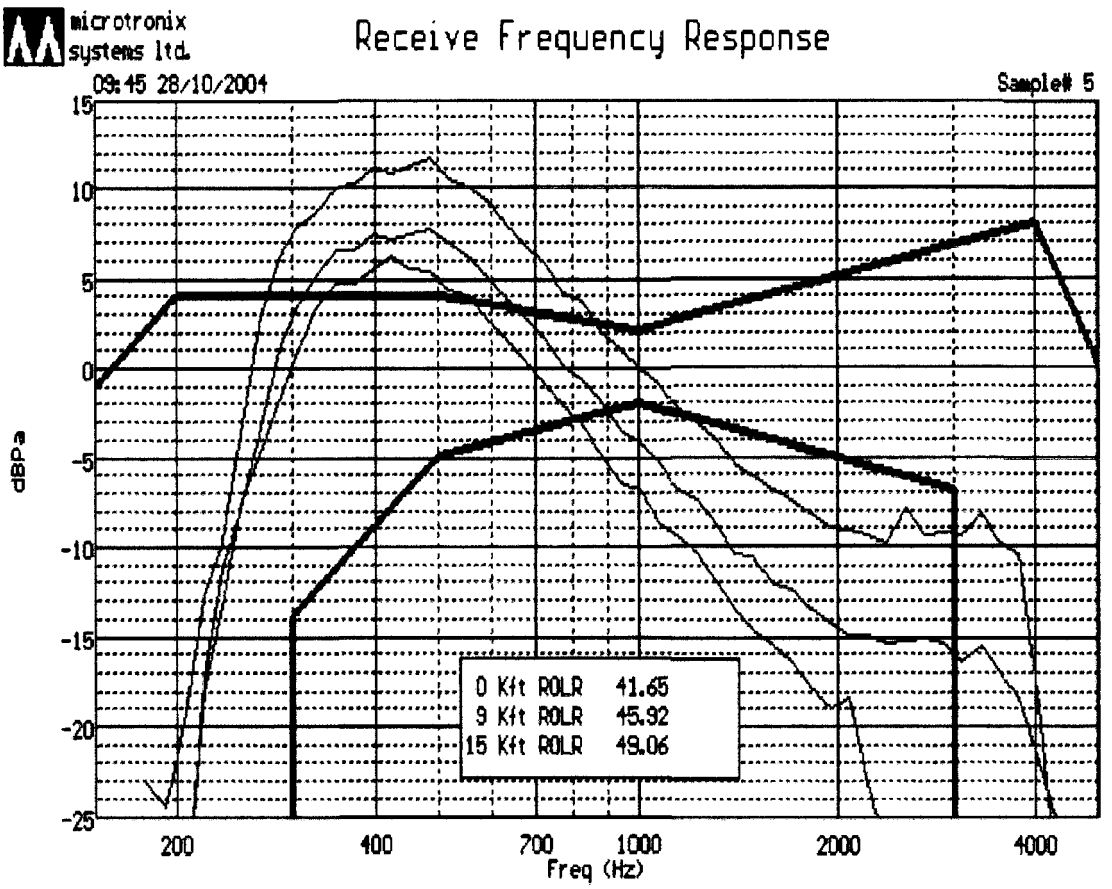


Figure 21: ROLR Graph

The ROLR number is calculated from the frequency content of the response to give a overall subjective loudness. From TIA spec, the range for ROLR at nominal volume setting is -41dB to –51dB and the dynamic range of the volume adjustment is between 12dB to 21 dB. From the receive frequency response, the base frequency (300-500Hz) of the audio is boosted and the high frequency has a sharp cut-off is at about 3.5KHz. The majority of the audio content is concentrated at 1KHz to 2 KHz and the low frequency content will add a perceptive quality audio factor.

On the transmit side, the frequency response is shown in Figure 22. The TOLR number is calculated from the frequency contents to give an objective loudness the far end. Different line lengths TOLR are provided to simulate the actual user scenario.

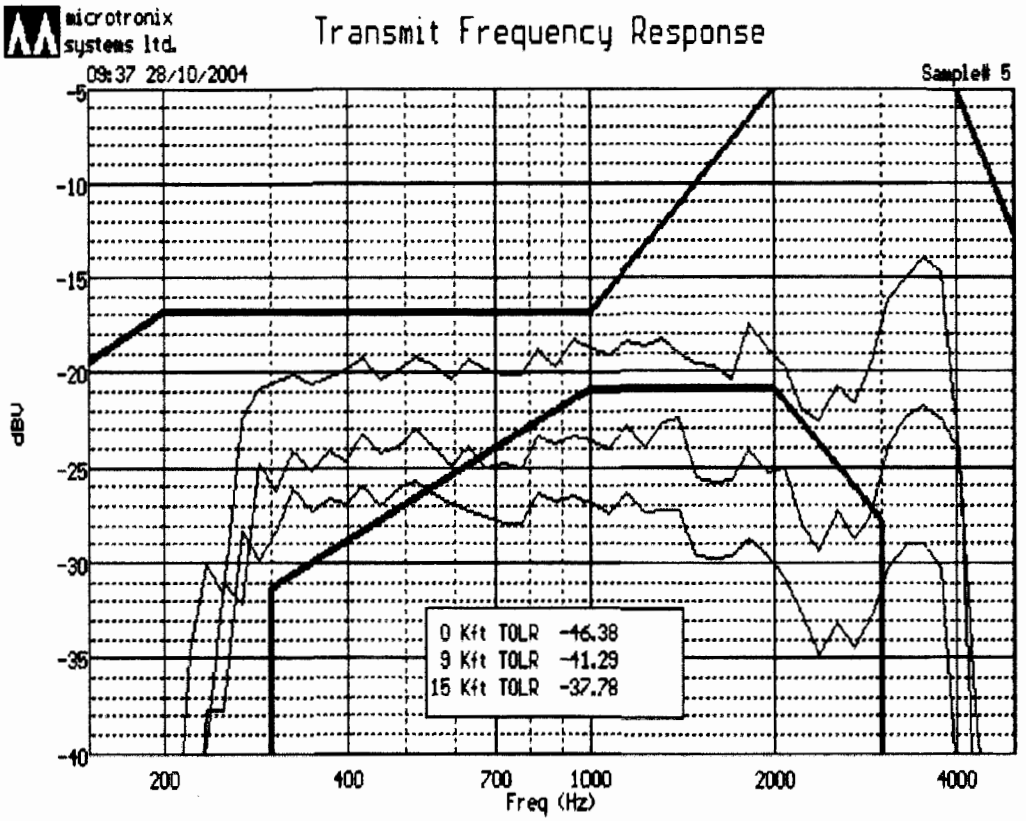


Figure 22: TOLR Graph

The sidetone is the amount of audio feedback from the transmit path to the receive path. In other words, the audio from the user is feedback to the receiver to give a comfortable feedback. The sidetone frequency response is shown in Figure 23.

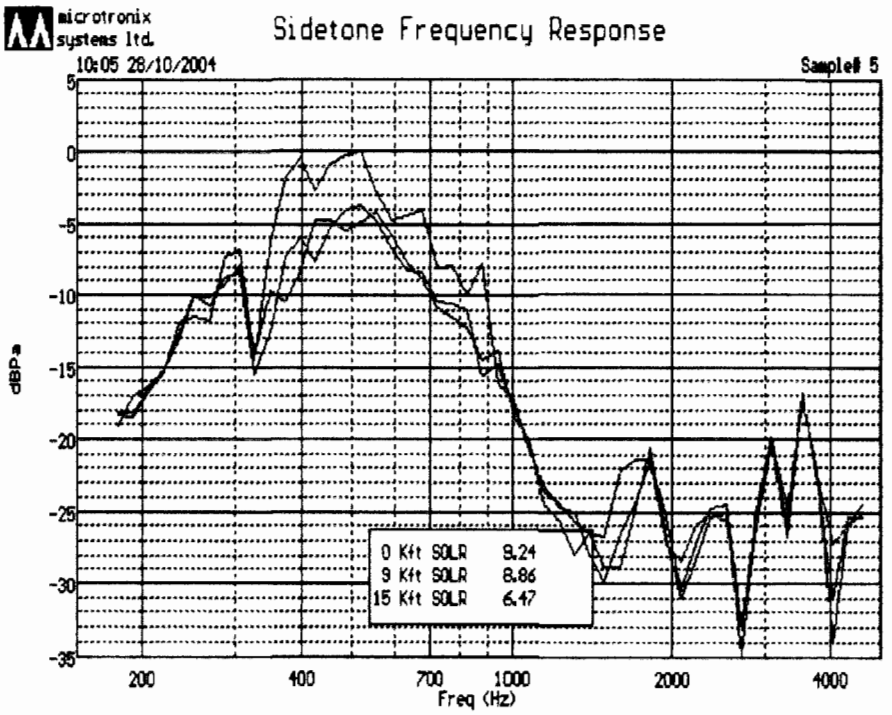


Figure 23: SOLR Graph

TDD noise is another key factor for good audio quality. Low frequency noise is induced from the either from RF signal or from power/ground to the audio path which is referred to as TDD noise. To prevent radiated TDD noise, audio components must be placed with sufficient distance to the antennas. All the differential audio signals should be routed closed to each other on the PCB to reject common mode TDD noise. In addition, small value capacity is also used to filter TDD noise when they are present on audio path.

To prevent conducted TDD noise, good ground and power flow is very important. Avoid sharing the GND and power between audio circuits and RF circuits. Since the current draw from the Power Amplifier of the RF at TDD interval can cause noise on the power or ground.

Figure 24 shows a FFT noise measurement on the receiver. The unit of measurement is in dBR which is referenced to 94 dBSPL. As seen on the graph, there are peaks starting from 300HZ repeating every 100Hz until 1 KHz. These are the TDD noise induced on the audio path by the RF. When the peaks are less than –60 dBR, there are not audible in normal environment. The plot also shows the different noise curve for minimum and maximum volume settings. The difference in gain between the two volume settings is roughly 13 dB.

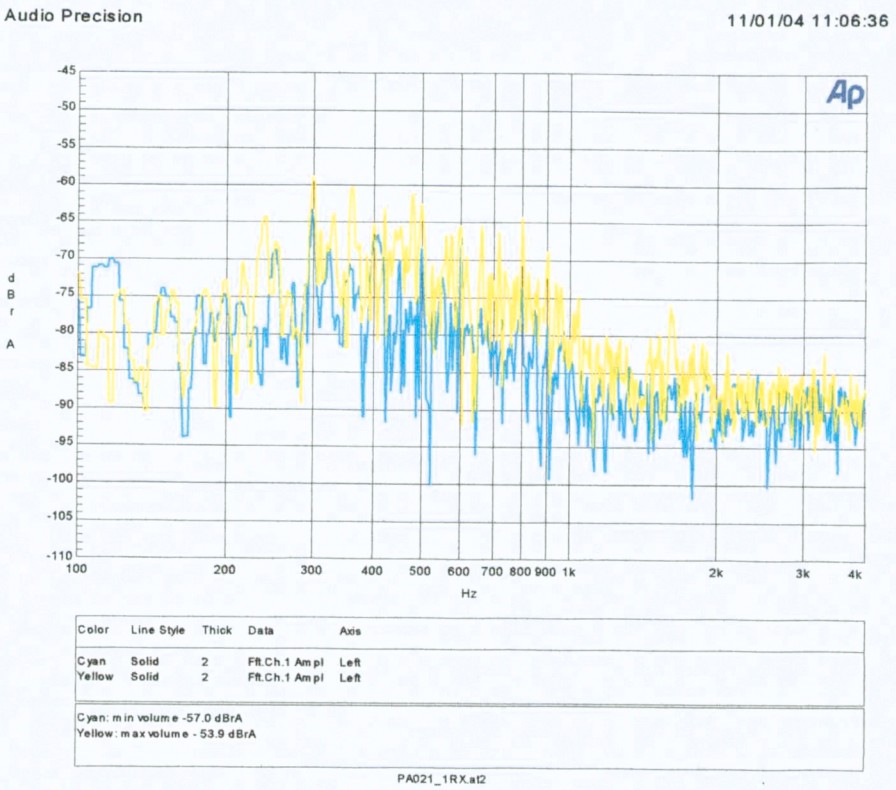


Figure 24: FFT RX Noise Measurement

On the transmit side, the noise is measured at the telephone line by taking a FFT sweep. As shown in Figure 25, the noise level is measured in dBV. Again, the 100Hz peaks also appeared on the transmit side but they are relatively low and are not audible on the far

end. If noise peaks exceed -70dBV, a hum will be observed on the far end. The plot consists of the noise curve when the microphone is enabled and also when it is disabled.

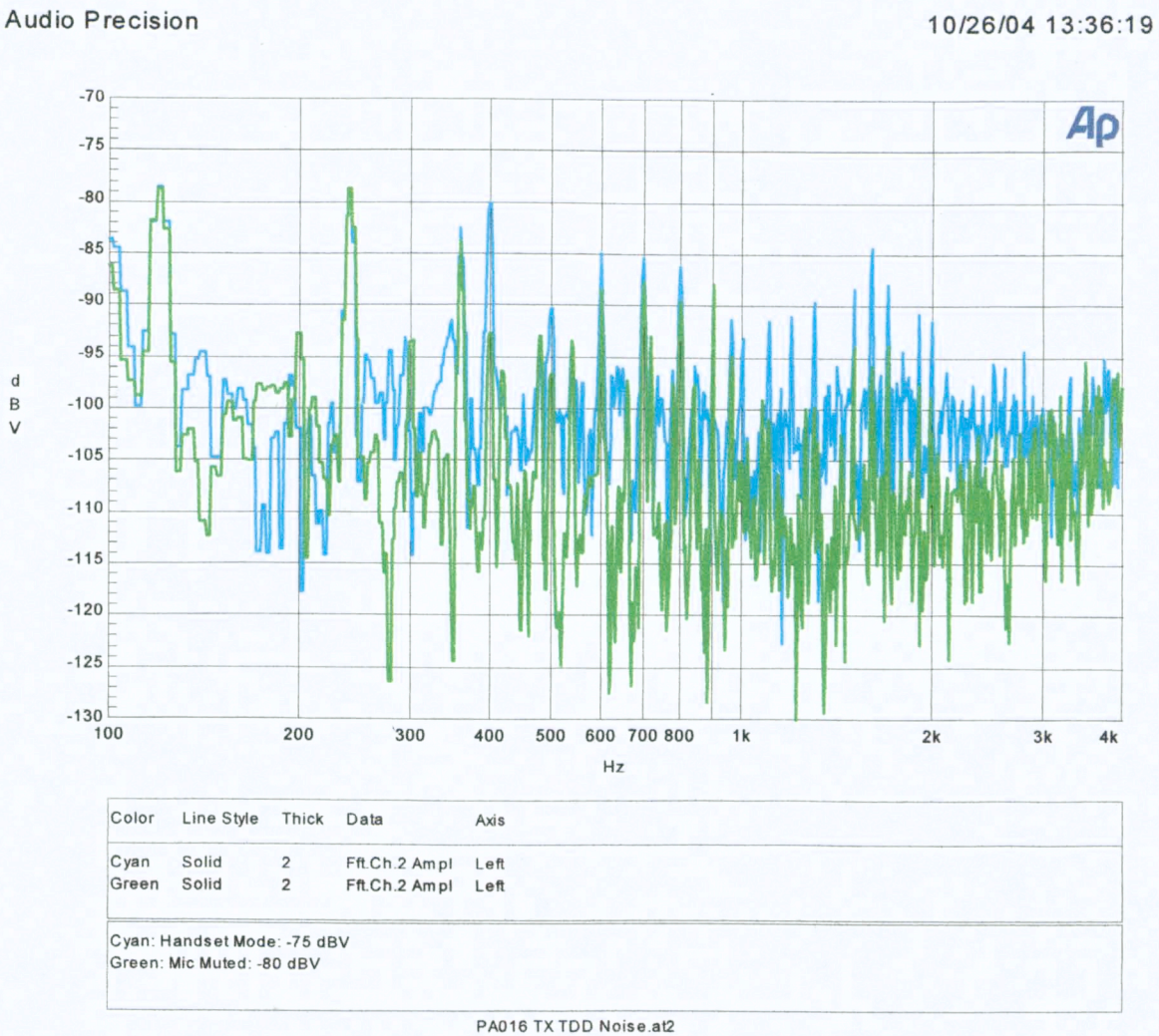


Figure 25: FFT TX Noise Measurement

4.3 Headset Mode

In headset mode, the audio is routed to the individual headset microphone and receiver. A different gain setting is used for the headset. In handset mode, the headset is plugged in to

the headset jack of the handset which connects the receiver amplifier and microphone bias circuit to the headset.

4.4 Handsfree Speaker Phone Mode

In handsfree speakerphone mode, the gain plan is different from the normal audio mode. The operation of the handsfree speakerphone is half-duplex, which means the audio can only be in one direction at a given time. The speakerphone algorithm is provided by the DSP processor in the ASIC. The tuning of the speaker phone switching module is to yield the best subjective performance for normal conversation. Figure 26 shows the RX frequency response of the HSF with the ROLR level.

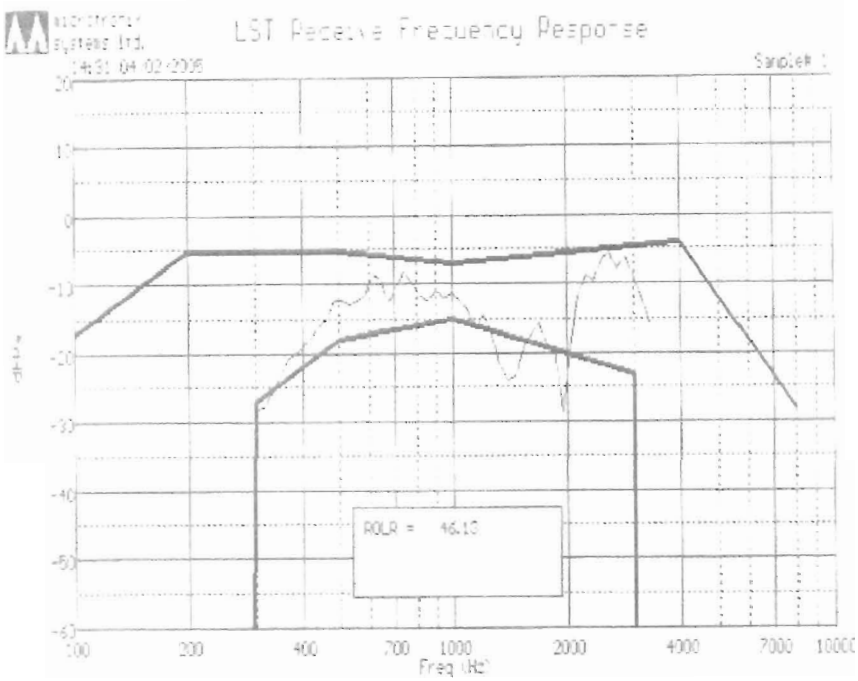


Figure 26: HSF ROLR Graph

Figure 27 shows the TX frequency response of the HSF with the TOLR level.

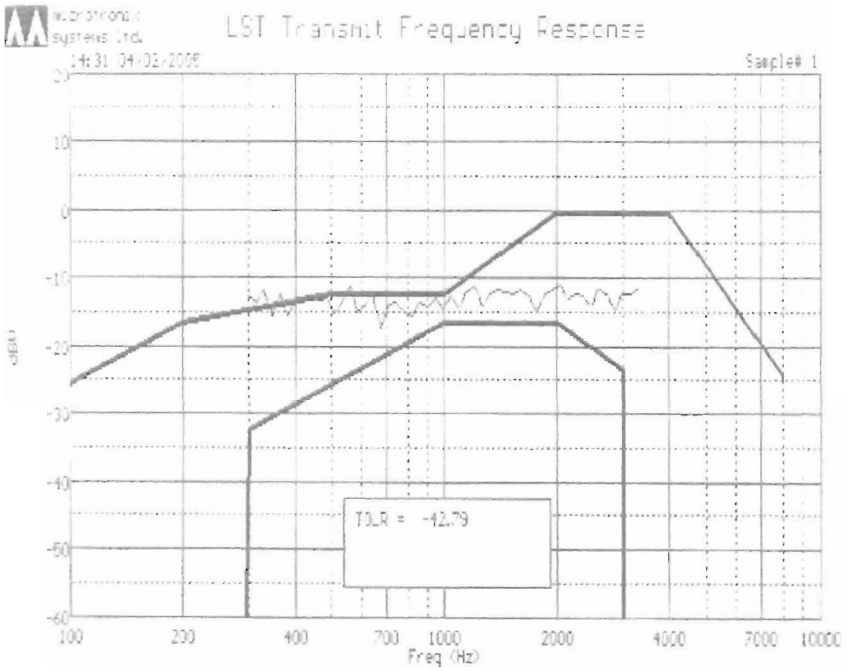


Figure 27: HSF TOLR Graph

5 ITAD MODULE

The ITAD module is a common part used in different products of the company. The module is a standalone component and will function separately from the integration target. In other words, there is no direct data exchange existed between base MCU and ITAD module. To integrate the ITAD module to the cordless base, only certain signals need to be connected.

ITAD functions including:

- Playback, Repeat, skip, delete messages in 3 different mailboxes
- Outgoing Message and memo record/review
- Answer on/off setting
- Voice help menu and user interface with mailboxes LEDs, 2-digit 7-segment LED display.
- Flash technology with Compression rate 3.2kbps 5.2kbps 16kbps to accommodate 17 minutes, 12 minutes, and 3 minutes of recording time respectively.
- Voice day and time stamping of memos and incoming messages
- Remote Access with programmable two-digit security code for remote control
- Automatically update real time clock from CID

To interface the ITAD module with the base unit, only few signals have to be connected to the ASIC and hybrid circuit to allow the ITAD module to detect ringing from the line, line status, control the hook switch, and the TX and RX audio lines. The ITAD module also contains a FSK demodulator to decode CID data to update the real time clock.

The ITAD module is equipped with microphone bias circuit for connecting microphone to record outgoing message and memo. The module also provide a single-ended or differential audio output to drive a speaker amplifier playback of messages.

5.1.1 Interconnect from ASIC to ITAD

MI6861 uses a standalone ITAD module to facilitate all the ITAD functions. Traditionally there is no direct communication between ASIC and the ITAD module. In this design, however, there are two interconnections between ASIC and ITAD module. They are the ITAD_HOOK_CTRL and /ITAD_HOOK_DET. The ITAD_HOOK_CTRL signal is an active high signal from ASIC to ITAD module. This signal is high when ASIC goes OFF-HOOK for itself so ITAD module must go on-hook immediately to avoid conflict. When ITAD module detects ASIC is off-hook, ITAD module will change the \ITAD_HOOK_DET signal output to HIGH. ITAD_HOOK_DET is an active low signal from ITAD module to ASIC. If this signal is low, the ITAD module wants to go off-hook. Therefore the ASIC must go off-hook and mute its own codec inputs immediately.

6 MULITPLE HANDSET OPERATIONS

The expandability of the firmware is designed to accommodate 4 handsets in the system.

With multi-handset capability, the system can provide enhanced features such as,

- Conference and intercom mode
- Call transfer between handsets
- Phonebook and CID log sharing

The registering process is based on an unique 15 digits ID for the base. This ID is stored in the base EEPROM during in the last ATE testing station. The base also stores all the handsets ID in the EEPROM to identify all the handsets registered in the system.

When there are 2 or more handsets registered to a base, conference call can be established. The maximum number of handset in conference with an outside line is two. Meanwhile, other handsets in the system can be in intercom mode simultaneously.

In the WDCT standard, 4 time slots are available in the TDMA system to allow data multiplexing. In conference call mode, 2 slots will be occupied for the 2 handsets in conference and 1 slot is reserved to maintain link to the other idle handsets in the system. In an environment with interference, one of the handsets in the conference call can go into enhanced mode which uses two slots to implement redundancy. This technique is also known as time diversity. Calls can also be transferred between two handsets when desired.

All phone book and CID log information are stored in the base EEPROM to offer a common storage for all handsets. Handsets can retrieve data from the base through the RF interface when necessary. The data transfer is done independent with the audio data traffic to provide data access capability during a call.

7 DISCUSSION AND CONCLUSION

The VTech 5.8 Mini cordless phone was designed to provide a full featured system with a small form factor. The project begins with designing the baseband circuitry and integrating it with the RF module, mechanical structures and software and performance system level validation. At the system level design, acoustic and audio gain plan are optimized to ensure good audio quality in all audio modes.

High level block diagrams were presented to outline the functional blocks in the baseband section for both the base and handset. Power management design is a key area on both the handset and base baseband sections. On the base, the line interface circuit (hybrid) was designed to interface the public telephone line with the baseband ASIC. The rest of the circuit on the base was to integrate the baseband ASIC with the system. On the model equipped with ITAD, the ITAD module is interfaced to the hybrid and ASIC to provide the answering machine capability. The ITAD model also features a microphone and speaker on the base for audio recording and playback. An user interface consists of buttons and LED display was provided to access the ITAD features as well. On the handset, a backlit character based LCD and keypad are used to provide the use interface to access various phone features. The handset also shares the same baseband ASIC with the base but running on different software. The handset is equipped with two audio amplifiers, one for the handset receiver and one for the speaker. They are used to supply audio or tones in different audio modes.

Acoustic and audio design was a major focus of the design. All audio modes are optimized by tuning various parameters in the ASIC DSP. The audio modes include normal handset audio mode, handsfree speakerphone mode, and headset mode. Optimized areas include far end and near end echo, TX and RX frequency and levels, distortion and dynamic ranges, and TDD noises.

The design was fully validated to be compliant with FCC and UL requirement. Furthermore, the products also met the VTech ESD criteria. Manufacturability was optimized at the end of the project to ensure high yield can be achieved in the production line. Automated testing equipment was setup to assist verification of the products at the factory. All the design work and validation process were completed before the start of mass production in roughly 6 months.

After mass production begins, further enhancement activities are in progress to improve in areas where performance might not been optimized. The areas include TDD noise in headset TX mode, surface temperature of handset during charging, ESD performance while handset on base cradle, and etc. Cost reduction activities are performed to further lower the cost of the product. Different areas are studied to reduce cost such as low cost discrete components to replace ICs.

8 REFERENCE

[1] Hai Nguyen, 2005, Theory of Operation - Handset, VTech Engineering Canada

[2] Raymond Yuen, 2005, Theory of Operation - Base, VTech Engineering Canada