FIELD EFFECT INVESTIGATIONS IN THIN CADMIUM SULFIDE FILMS

by

JOHN FRANCIS O'HANLON

B.S.E.E., The University of Arizona, 1962
M.S., The University of Arizona, 1963

A DISSERTATION SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

In the Department
of
Physics

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SIMON FRASER UNIVERSITY
October 1967

EXAMINING COMMITTEE APPROVAL

R. R. Haering
Senior Supervisor

J. F. Cochran
Examining Committee

R. F. Frindt
Examining Committee

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ABSTRACT

Field effect investigations on thin cadmium sulfide films have yielded a method of controlling the surface potential. The control of the surface potential is achieved by the successive evaporation of two dielectrics, CaF_2 and SiO. The SiO produces donor-like surface states at the CdS surface, while CaF_2 produces acceptor-like surface states. By evaporating a thin layer of CaF_2 between the CdS and SiO, the effect of the donor-like surface states on the surface conduction of CdS may be reduced. Thus, by proper choice of the CaF_2 thickness, any surface potential between the limits of SiO and CaF_2 may be obtained.

The analysis, construction, and performance of a new evaporated thin-film transistor capable of withstanding over 300 V is described. This thin-film transistor will switch a current of 100μa with a gate voltage of less than 50 V, and is particularly suited as a transistor controlled switch. The large increase in operating voltage is achieved by changes in the device geometry, material characteristics, and through careful control of the CdS surface potential by the method described above.

Devices were constructed with an incremental saturation resistance of 200MΩ, and a maximum operating voltage in excess of 350 V. These transistors were used to switch electro-

luminescent lamps with gate voltages of 50 V in less than 0.2 msec. The transistors with semiconducting layers of CdS, utilizing CaF_2, SiO, and GeO_2 insulators and Al electrodes, were fabricated on glass substrates by vacuum evaporation.

In related experiment it was found that an evaporated CaF_2 layer could be used to vary the surface potential of germanium, and the effects of controlling the surface potential of a Ge(Li) p-i-n diode were observed. A thickness of 150 to 200 Å of CaF_2 appeared to restore the surface potential in the intrinsic region to the bulk value, and thus resulted in a lower surface leakage current.

TABLE OF CONTENTS

Page

LIST OF TABLES vii

LIST OF ILLUSTRATIONS viii

ACKNOWLEDGMENTS xii

1. INTRODUCTION 1

1.1 Historical Review 1

1.2 Description of the TFT 2

1.3 Physical Requirements of the Materials used in a TFT 3

1.4 Materials and Methods used in TFT Fabrication. 4

1.5 Scope of this Work 5

2. REVIEW OF THE THEORY OF THE INSULATED-GATE THIN-FILM TRANSISTOR 7

2.1 Introduction 7

2.2 The Gradual Approximation 7

2.3 The SCL Current Model 13

2.4 The Static Theory of the Insulated-Gate Thin-Film Transistor 14

2.5 Low Frequency Characteristics 20

2.6 The A.C. Transconductance 25

2.7 Comparison of TFT Theory with Experiments 28

2.7.1 Static Characteristics 28

2.7.2 Dynamic Characteristics 29

3. APPARATUS AND MATERIALS FOR THE FABRICATION OF EVAPORATED THIN-FILM TRANSISTORS 31

3.1 Introduction 31

3.2 The Vacuum System 31

3.3 Control of the Substrate Temperature 31

3.3.1 The Conduction Heater 34

3.3.2 The Directly Heated Substrate 37

3.4 Evaporation Sources, Materials and Techniques. 41

3.4.1 Cadmium Sulfide 41

3.4.2 Silicon Monoxide 41

3.4.3 Germanium Dioxide 47

3.4.4 Aluminum 48

3.4.5 Calcium Fluoride 49

3.5 Mask Design and Construction 49

3.6 Film Thickness Monitor 50

4. THE VACUUM EVAPORATION OF CADMIUM SULFIDE 53

4.1 Introduction 53

4.2 Mechanisms of Evaporation 53

4.3 Techniques of Producing Evaporated CdS Films . 55

4.4 Electrical Properties 58

4.5 Crystalline Structure 60

4.6 Recrystallized Layers 61

5. CONTROL OF THE SURFACE POTENTIAL OF EVAPORATED CdS LAYERS 64

5.1 Introduction 64

5.2 Principles of the Method 64

5.3 Experimental Procedure 67

5.4 Experimental Results 67

6. CONTROL OF THE SURFACE POTENTIAL OF OTHER SEMICONDUCTORS 73

6.1 Introduction 73

6.2 Application to Lithium-Drifted Germanium Diodes 73

6.3 Experimental Procedure 74

6.4 Results 76

6.5 Conclusion 77

7. THE HIGH VOLTAGE TFT - THEORY OF OPERATION AND DESIGN 81

7.1 Introduction 81

7.2 Design Consideration for the High Voltage TFT. 82

7.3 Device Fabrication 87

8. THE HIGH VOLTAGE TFT - EXPERIMENTAL RESULTS 94

8.1 Device I-V Characteristics 94

8.2 Transconductance and Mobility 97

8.3 Output Conductance 101

8.4 Switching Speed 102

8.5 High Voltage Limitations 107

8.6 The High Voltage TFT as an EL Lamp Switch 109

8.7 The Effects of Rectifying Contacts 113

8.8 Device Stability 115

8.9 Suggestions for Improvement of the Characteristics 120

9. CONCLUSION 123

APPENDIX A. CALCULATION OF THE SMALL SIGNAL A.C. TRANSCONDUCTANCE AND OUTPUT CONDUCTANCE OF A TFT 125

A.1 Introduction 125

A.2 Calculation of the Transconductance 125

A.3 Calculation of the Output Conductance 127

APPENDIX B. APPARATUS FOR THE MEASUREMENT OF THE RESISTIVITY AND HALL COEFFICIENT IN HIGH RESISTIVITY SEMICONDUCTORS 129

B.1 Introduction 129

B.2 Theory of Operation 129

B.3 Measurement Techniques 131

APPENDIX C. THE FILM THICKNESS MONITOR 136

APPENDIX D. THE ELECTROLUMINESCENT LAMP 143

REFERENCES 146

LIST OF TABLES

Table		Page
3-1	Calibration Factors for Some Materials Evaporated in this System	52
4-1	Resistivity, Hall Mobility and Free Electron Concentration of Typical Evaporated CdS Films	58
7-1	Dimensions of the High Voltage and Conventional TFT	87
8-1	Measured Effective Mobility in Several TFT's.	98

LIST OF ILLUSTRATIONS

Figure		Page
2-1	TFT Geometry	8
2-2	Typical Static Characteristics for TFT's Operating in the Enhancement and Depletion Modes ...	12
2-3	Longitudinal Cross-Section of Transistor Model .	15
2-4	Static TFT Characteristic for h/L = 1/50	21
2-5	Static TFT Characteristic for h/L = 1/25	21
2-6	Variation of Transconductance of Silicon TFT with Gate and Drain Voltage	22
2-7	Variation of Output Conductance of Silicon TFT with Gate Voltage	22
2-8	Hall Mobility in an Evaporated CdS TFT Plotted as a Function of Gate Voltage	24
2-9	Gate Capacitance of a CdS TFT Plotted as a Function of Gate and Drain Voltage	24
2-10	Variation of $\lvert g_m(\omega)\rvert$ with Frequency	27
3-1	Mask Changing Apparatus	32
3-2	Conduction Substrate Heater	36
3-3	Transient Response and Calibration of the Conduction Heater	39
3-4	The Directly Heated Substrate	40
3-5	Temperature Distribution on Substrate in Regions used for Evaporation of CdS in the High Voltage TFT	42
3-6	Power Input to Substrate vs Front Surface Temperature of Substrate	43
3-7	Front Surface Temperature of Substrate vs Reference Temperature	43

3-8	Tantalum Sources for the Evaporation of SiO and CdS	45
3-9	Interference Fringes for a 2,000 Å CdS Film ...	52
4-1	Mass Spectrum Before and During the Evaporation of CdS from a Ta Crucible	57
4-2	Electron Micrograph and Transmission Pattern of Thin CdS Film	62
5-1	Energy Band Structure of a CdS Film with Equally Depleted Surfaces	66
5-2	Cross-Section of the Evaporated Semiconductor-Insulator Structure	66
5-3	The Completed Resistivity Sample Showing Twelve Devices, Each Containing Hall and Resistivity Contacts	69
5-4	Conductance per Square for Two Sets of Symmetrically Coated CdS Films	70
5-5	Measured Depletion Depth of CdS Coated with CaF_2 Followed by 2,000 Å of SiO_x	71
6-1	Energy Band Diagram of P-I-N Diode	75
6-2	Effects of CaF_2 Evaporation on Edges of Ge(Li) Detectors	78
6-3	Spectrum of Cs^{137} Gamma Ray Taken with Ge(Li) Diode Before and After Coating with 150 Å of CaF_2	79
6-4	Cs^{137} Gamma Ray Detected with Ge(Li) Diode after Coating with 150 Å CaF_2 Followed by an FET Preamp	80
7-1	Calculated Static Characteristics of the High Voltage TFT	89
7-2	Geometry of the High Voltage TFT	90
7-3	Energy Band Structure of and Electron Concentration in the High Voltage TFT	93
8-1	Dark Characteristics of two TFT's as Displayed on the Tektronix 575 Curve Tracer	95

8-2	TFT Static Dark Characteristic	96
8-3	TFT Transconductance vs. Gate Voltage	99
8-4	TFT Showing High Mobility and Transconductance .	100
8-5	Frequency Dependence of the Transconductance of Two TFT's showing the Effect of Slow Traps	103
8-6	TFT with High Saturation Resistance	104
8-7	TFT Output Resistance vs. Gate Voltage	106
8-8	Switching Speed Analysis of a TFT with a Parllel RC Load Operating in the Saturation Region	108
8-9	Switching Time for a Transistor with Various RC Loads	110
8-10	TFT Operating with V_{SD} = 350 Volts	111
8-11	TFT Switching of EL Lamp	112
8-12	EL Lamp Power vs. Gate Voltage for a 0.25 cm^2 Lamp as Detected by a Silicon Solar Cell	114
8-13	Effect of Rectifying Drain Contacts on TFT Characteristics	116
8-14	Effect of Reversing Source-Drain Connection on a TFT with Rectifying Contacts	118
8-15	Illustration of Ion Drift in an Insulator	119
8-16	Instability in TFT Characteristics	121
8-17	TFT Connected as a Diode Showing Shift in Characteristic due to Moisture in the Insulator.	121
B-1	Basic Measuring Circuit	130
B-2	Modified Measuring Circuit	130
B-3	Block Diagram of the Bridge	132
B-4	Circuit of Potentiometer P_1	133
B-5	Circuit of Potentiometers P_2 and P_3	134

C-1	Block Diagram of the Film Thickness Monitor	137
C-2	Circuit Diagram of the 5 mc. Oscillator	142
C-3	Geometry used in Calculating the Resonant Frequency of a Coated Quartz Crystal	142
D-1	Emission Characteristic for Green Phosphor used in this Study	144
D-2	Impedance Characteristic of EL Lamp	144

ACKNOWLEDGMENTS

The author is indebted to Dr. R. R. Haering for suggesting this topic and for his help and guidance throughout the course of the investigation. Grateful acknowledgment is also given to Drs. J. F. Cochran and R. F. Frindt for reading the manuscript and for their many helpful suggestions.

The author is grateful to Dr. L. Young of the Department of Electrical Engineering at U.B.C. for use of the Hitachi Electron Microscope, photo-etching facilities, and for reading the manuscript, to Dr. J. Coburn for permission to use his unpublished mass spectra of CdS, and to Dr. B. D. Pate and Mr. A. Sher of the S.F.U. Department of Chemistry for the fabrication of and gamma ray spectra on Ge(Li) detectors, to Mr. J. Mercier for technical help and drafting, to the Science Workshop for construction of apparatus, and to Mrs. S. Ginetz for typing the thesis.

The work described in this thesis was supported by the Defence Research Board and the National Research Council.

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I. INTRODUCTION

1.1 Historical Review

When an electric field is applied in a direction normal to the surface of a conductor, a surface charge is produced. This charge, which is drawn into the conductor via the contact electrode, alters the conductivity of the surface region. In metals, the density of electrons available for conduction is large -- even in the absence of a transverse electric field -- and the additional electrons which constitute the surface charge are almost negligible. It is possible to observe a very small field effect in metals using a ferroelectric.(1) However, in semiconducting materials, the applied field should in principle be able to alter the conductivity of the surface region by many orders of magnitude. The applied field may therefore be used to control a current flowing in the semiconductor, and field effect modulation of conductivity is of practical as well as of theoretical interest.

The first records of conductivity modulation by a transverse electric field are contained in patents by Lilienfield(2) in 1930. In 1935 Heil(3) observed the effect in a thin-film structure. These early devices were limited by the low sensitivity of the semiconductor to the applied field. In 1948 Shockley and Pearson(4) modulated the conductivity of

germanium films and used Bardeen's[5] theory of surface states to show that these states were responsible for the poor conductivity modulation. In 1960 Bockemuehl[6] constructed a device which operated on this principle of surface conductivity modulation by a transverse electric field. This device, which is referred to as an insulated-gate field-effect transistor, was constructed by evaporation of the electrodes and insulation on single crystal CdS. In 1962 Weimer[7], using CdS, constructed the first evaporated field-effect device. He observed that the type of surface states on the semiconductor were dependent upon the nature of the evaporated insulating material, and his efforts are largely responsible for the current work on surface states employing the thin-film transistor structure.

1.2 Description of the Thin-Film Transistor

The thin-film transistor is a unipolar device in which the density of free majority carriers available to carry current in the conducting region is controlled by the application of an electric field to the surface of a thin, semiconducting film. In the TFT electrons flow from an ohmic contact, called the source, through a conducting surface channel to another ohmic contact, called the drain. The conductivity of the channel may be modulated by the transverse electric field produced by the gate electrode. The gate is one plate of a capacitor which is separated from the other plate, the semiconducting surface, by a thin insulating layer.

1.3 Physical Requirements of the Materials used in a TFT

Although the insulation and contact materials used are important, the characteristics of a TFT are largely dependent upon the properties of the semiconductor. The question is, then, how does one choose a semiconductor for this application?

One important criterion is majority carrier mobility. A high mobility assures that the source-drain transit time of the injected carriers will be small; the device will then have a high frequency response. Although the higher mobility of single crystals is desirable, the mobility of many polycrystalline films is acceptable. To some extent a lower mobility can be compensated for by a smaller source-drain spacing, but here practical limits of about 5μ are encountered. A second criterion is free carrier density. The free carrier density of the semiconductor must not be too large because the amount of charge which can be modulated is limited by the insulator dielectric constant and electric field breakdown strength. For example, consider a silicon dioxide film with a dielectric constant of 2.5 and a dielectric breakdown field of 5×10^6 V/cm. This electric field terminates on a surface electron charge layer of 7×10^{12} electrons/cm^2. If the free carrier density is greater than about 10^{19}/cc the resulting surface conductivity change will be insignificant.

Two requirements of the insulator material are now apparent: a high dielectric constant, and a high dielectric breakdown strength. Since high electric fields are impressed

on the insulator, it should also be free of mobile ions and molecules whose polarization effects result in instability of the surface conductivity.

1.4 Materials and Methods used in TFT Fabrication

TFT's have been constructed by vacuum evaporation of a large number of semiconductors. Among these are silicon[8], tellurium[9], cadmium sulfide[7], cadmium selenide[10], cadmium telluride[11], lead sulfide[12], gallium arsenide[13], indium antimonide[14], zinc oxide[11], tin oxide[15], and indium oxide[15]. In addition Wright[16] has proposed aluminum antimonide and gallium phosphide.

The details of the deposition and processing techniques of each of these films are as significant as the choice of the material. Of these materials, films of CdSe and CdS are among the easiest to form by vacuum evaporation. In part, the CdSe films are formed more easily than those of CdS because of the relative closeness of the vapor pressure curves of Cd and Se. Both CdSe and CdS films were used in this study. However, the bulk of the data were taken using CdS films; largely because of our greater experience with this material.

The techniques used to construct the TFT must be such that the density of surface trapping states at the semiconductor-insulator interface is small compared with the charge density that can be induced by the transverse electric field.

McWhorter[17] has observed that the 1/f noise associated with these devices is due to the transfer of carriers in and out of surface states, and a reduction of this noise necessitates an even further reduction of the surface state density. To this end, vacuum evaporation of the entire device in one chamber seems most desirable in order to minimize surface states arising from uncontrolled changes of ambient conditions.

1.5 Scope of this Work

This thesis describes a method of controlling the surface potential of CdS by the successive evaporation of a fluoride and an oxide insulation layer. This work on control of the surface potential has lead to the development of a new high voltage thin-film transistor. The technique was also applied to germanium and was found to reduce the surface leakage current in germanium p-i-n diodes.

Section 2 reviews the theory of the insulated gate thin-film transistor, which provides a framework for the understanding of conductivity modulation by a transverse electric field. Section 3 describes a high vacuum system for the production of the multilayer thin film structures; the techniques and materials for deposition and measurement of the evaporated films are discussed. A review of the deposition techniques and properties of CdS films is given in Section 4. Section 5 discusses the method used to control the surface potential of CdS. In Section 6

it is demonstrated that this technique can be used to reduce the surface leakage currents in germanium p-i-n diodes used as gamma ray detectors. Section 7 presents the theory of operation and fabrication techniques of the high voltage thin-film transistor; Section 8 describes the performance characteristics of typical units fabricated. Appendices dealing with related topics are also included.

2. REVIEW OF THE THEORY OF THE INSULATED-GATE THIN-FILM TRANSISTOR

2.1 Introduction

A review of the physical theory of the insulated-gate thin-film transistor is given here. The static characteristics are first analyzed for a simplified model and then for the general case. The small-signal parameters derived from the static characteristics are discussed and their deviations from observed characteristics are explained in terms of changes in carrier mobility and trapping effects.

2.2 The Gradual Approximation

An analysis of the TFT based upon the work of Many, as published by Borkan and Weimer[18], and usually referred to as the gradual approximation is given here. The idealized structure of the TFT is illustrated in Fig. 2.1.

The semiconducting film has thickness, t, width, w, and length, L. It is separated from the gate electrode by an insulator of thickness, h. In this analysis the following assumptions are made:

1. The semiconducting layer is homogeneous and thin compared to the insulating layer.

2. The mobility, μ, of the semiconductor is a constant.

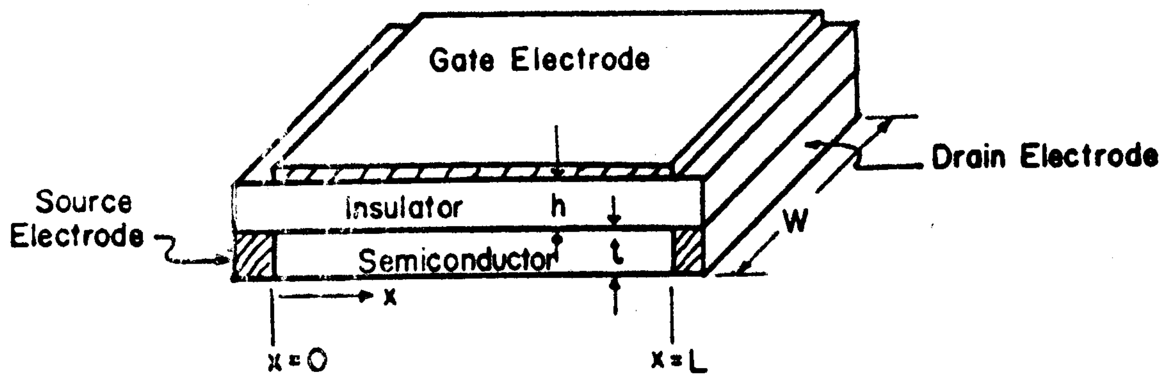


Figure 2-1. TFT Geometry

3. Only majority carriers are considered to exist in the semiconductor. This approximation is expected to be good for a material such as CdS, although it may fail in the depletion mode for very large voltages.

4. The gate-semiconductor capacitance, C_G, is assumed constant.

5. Trapping effects are neglected.

6. The metal-semiconductor work function difference is neglected.

7. The gradual-channel approximation is assumed to hold. This approximation states that the rate of change of the potential along the channel is very small compared to the rate of change of the gate potential normal to the channel.

The charge induced per unit area on the gate electrode is given by

$$q\,\Delta N(x) = \frac{C_G}{wL}\,(V_G - V(x)), \qquad (2\text{-}1)$$

where $V(x)$ is the potential of the semiconductor relative to the source measured at a distance x from the source, and $\Delta N(x)$ is the number of charges per unit area induced on the gate electrode. The drain current, I_D, in the semiconductor may then be expressed as

$$I_D = tw\mu q\,\left(\frac{N_o}{twL} + \frac{\Delta N(x)}{t}\right) E_x. \qquad (2\text{-}2)$$

N_o is the total number of initial charges in the semiconductor, q is the electronic charge, and E_x is the electric field in the x-direction. With the aid of equation (2-1) one may integrate equation (2-2)

$$I_D \int_o^L dx = \frac{\mu C_G}{L} \int_o^{V_D} \left(\frac{N_o q}{C_G} + V_G - V \right) dV \qquad (2\text{-}3)$$

which gives

$$I_D = \frac{\mu C_G}{L^2} \left[\left(\frac{N_o q}{C_G} + V_G \right) V_D - \frac{V_D^2}{2} \right] \qquad (2\text{-}4)$$

where V_D is the potential at the drain. The term $\frac{N_o q}{C_G}$ has the dimensions of voltage and is conventionally replaced by a voltage $-V_o$, where $+V_o$ is the minimum gate voltage which has an effect on I_D. A positive value of N_o implies the presence of free electrons in the conducting channel at zero gate voltage, while a negative value of N_o implies the presence of unfilled traps.

Equation (2-4) is valid up to the point $V_D \leq (V_G - V_o)$. For larger source-drain voltages a small region of the channel at the drain becomes completely depleted of carriers and the current is strictly space-charge-limited; nearly all of the source-drain voltage increase will appear across this region. If it is assumed that this region is small and its length constant, then the drain current will be approximately saturated

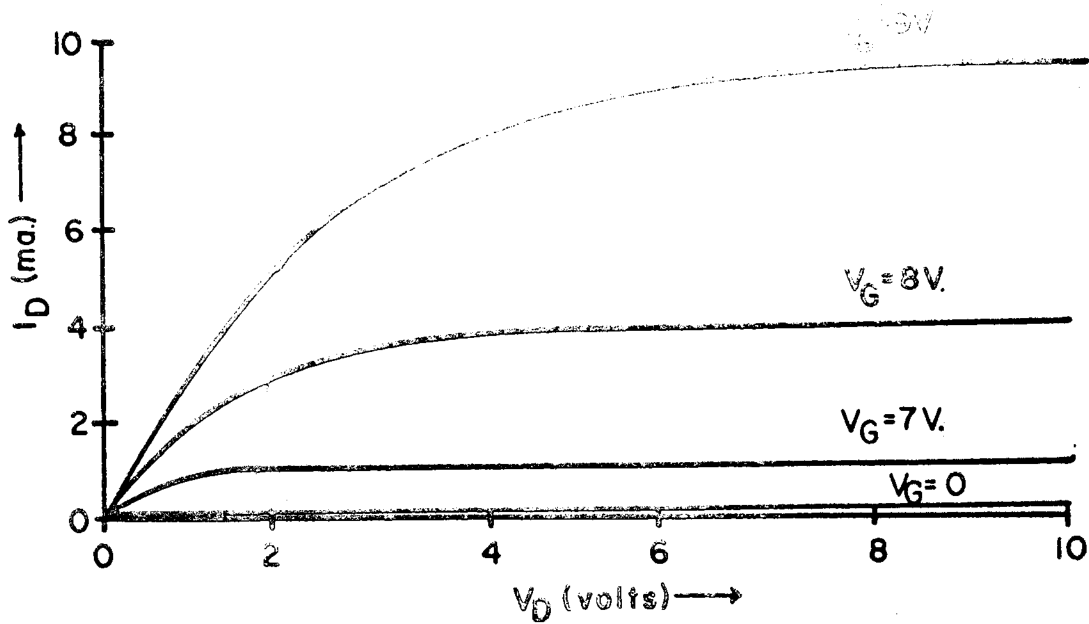
so that,

$$I_D = \frac{\mu C_G}{2L^2}(V_G - V_o)^2 \quad \text{if} \quad V_D > (V_G - V_o). \qquad (2\text{-}5)$$

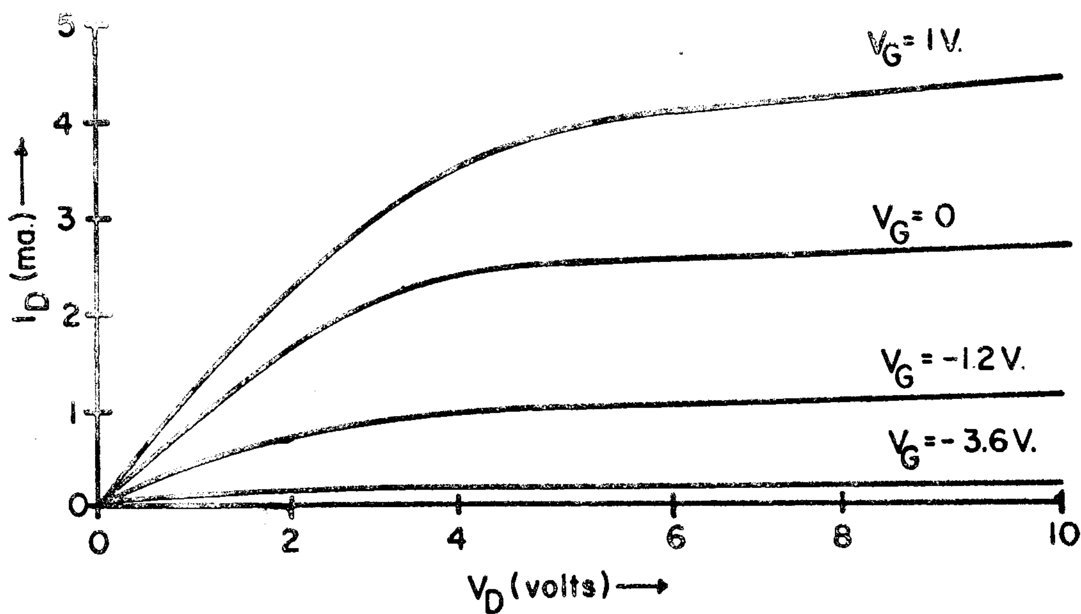
This zero output conductance or perfect saturation of the characteristics has never been observed in actual units.

Depending on the value of V_o, two modes of device operation are possible. If V_o is made positive the device is "turned off" at zero gate bias; the device is said to be operating in the "enhancement mode" because application of a positive gate potential will enhance source-drain charge flow. If V_o is negative, the device is "turned on" at zero gate potential; the device is now said to be operating in the "depletion mode" because application of a negative bias will cause the source-drain current to decrease. Fig. 2-2 illustrates typical static characteristics of a depletion and an enhancement mode device.[7]

Typically, the value of V_o obtained depends upon the choice of insulation material and its method of deposition in addition to the previous history of the semiconducting surface. For example, evaporation of SiO on a CdS layer previously exposed to oxygen results in an enhancement unit, while evaporation of SiO on a freshly deposited CdS film results in a depletion unit. It is also known that CdS devices with CaF_2 insulation are "turned off" at zero gate bias.[19] Thus the surface potential of the semiconductor may be altered somewhat



(a) Enhancement Mode



(b) Depletion Mode

Figure 2-2. Typical Static Characteristics for TFT's Operating in the Enhancement and Depletion Modes.

by proper choice of techniques and materials. In Section 5 a new method of continuous control of the surface potential utilizing compound layers of insulation is discussed.

2.3 The Space-Charge-Limited (SCL) Current Model

Physical mechanisims have been put forward by several authors[20, 21] to account for the observed non-ideal saturation. The model by Wright[22] distinguishes a source region where the gradual approximation is valid, and a drain region through which a space-charge-limited current flows in the presence of a longitudinally-directed electric field. The point at which the semiconductor potential equals the gate potential divides the source and drain regions. Despite a mathematical difficulty in matching the two solutions at the junction of the source region and drain region, Wright is able to calculate current-voltage relations for a TFT with $V_o = 0$ (i.e. no surface or bulk trapping states) which agree with experiment. This model shows that the finite output conductance is related to the increase in size of the drain region in which SCL current flows as the source-drain voltage is increased beyond the limits of the gradual approximation. Since the effective channel length (source region) decreases slowly with increasing drain voltage, the calculated I-V characteristics show a slope beyond the limits of the gradual approximation.

2.4 The Static Theory of the Insulated-Gate Field-Effect Transistor

It is of interest to compare the analysis given in the preceding section with the theory by Geurst[23]. This analysis, which is valid only for the static case, is the only theoretical treatment to date that does not make use of the gradual approximation. It does, however, make the unphysical assumption that the semiconducting layer is infinitely thin. Geurst's analysis makes use of conformal mapping techniques to solve a boundary value problem for the electric field everywhere in the insulator. With this information the static characteristics are calculated.

In this model the mobility is assumed constant and the occurrence of partially ionized donors and hot electrons is not considered. The assumption is made that the thickness of the semiconducting channel is infinitely thin compared to the thickness of the insulation layer. A two-dimensional model is then introduced in which the electrode configuration is assumed symmetric in the sense that the semiconducting channel is flanked by gate electrodes at both sides. This symmetry has been introduced for mathematical convenience. Fig. 2-3 illustrates the geometry of the model.

It is reasonable to expect that the overlap of gate and source-drain electrodes and the extension of the electrodes to infinity will not seriously affect the results obtained for the static case.

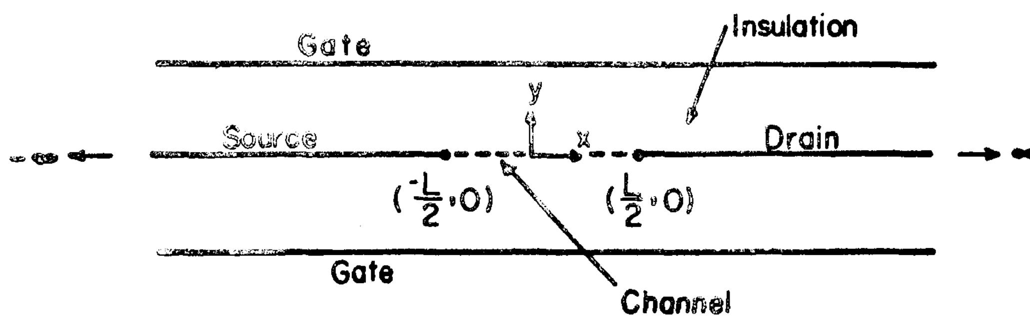


Figure 2-3. Longitudinal Cross-Section of Transistor Model.

The current, I, traversing the semiconducting channel from the source (-L/2, 0) to the drain (+L/2, 0) per unit width of the channel is given by

$$I = \sigma v \qquad (2\text{-}8)$$

where σ denotes the mobile charge per unit surface area in the channel and v represents the drift velocity of the charge carriers. The mobile surface charge density may be expressed as

$$\sigma = D_y^+ - D_y^- - \frac{qN_o}{L} \qquad (2\text{-}9)$$

where $D_y^\pm$ represent the y-components of the displacement vector at the upper and lower sides of the channel. The number of electrons/unit width originally present in the channel may be expressed as a voltage by the relation

$$\frac{2\epsilon_o\epsilon_r V_o}{h} = -\frac{qN_o}{L} . \qquad (2\text{-}10)$$

Where ϵ_r is the relative dielectric constant of the insulator. A positive value of V_o corresponds to empty traps in the channel and a negative value of V_o corresponds to the mobile charge present at zero gate bias. The drift velocity, v, (for electrons) is given by

$$v = -\mu E_x . \qquad (2\text{-}11)$$

Upon noting that the longitudinal component E_x is continuous

across the channel one may substitute equations (2-9), (2-10), and (2-11) in (2-8) to obtain

$$I = -2\mu\varepsilon_o\varepsilon_r \left[\left(E_y + \frac{V_o}{h}\right) E_x\right]^+ \qquad (2\text{-}12)$$

where the superscript denotes the limiting value at the upper side of the channel. Equation (2-12) is a non-linear boundary condition for the electric field in the insulating region bounded by the upper half of the semiconducting channel. The remaining boundary condition at the metal electrodes is given by

$$E_x = 0. \qquad (2\text{-}13)$$

Thus the boundary condition around the entire insulating region is known. The detailed steps of this derivation have been omitted since the work is not original.

Before examining the solution to this problem it is of interest to examine equation (2-12) for the case where the electric field between the gate electrode and the channel is parallel to the y-axis (i.e. $E_x \ll E_y$ at the channel). Equation (2-12) may now be written as

$$I = -\frac{2\mu\varepsilon_o\varepsilon_r}{h} \left[V_G - V(x) - V_o\right] \frac{dV}{dx} \qquad (2\text{-}14)$$

which, apart from the factor of 2 introduced by symmetry, is identical to equation (2-3). The statement $E_x \ll E_y$ is the

gradual approximation in the theory given by Borkan and Weimer[16] Note, however, that equation (2-12) retains its validity when E_x does not satisfy the gradual approximation.

The similarity between the theories of Geurst and Wright become apparent when Equation (2-12) is examined for the case $V_o = 0$. For this case it may be considered as a particular form of the general formula for space-charge-limited currents in solids given by

$$J_\iota = -\mu(\mathrm{div}\bar{D})E_\iota \qquad (2\text{-}15)$$

for electrons in an infinitely thin semiconductor. The one-dimensional case of equation (2-15) with all the field lines parallel to the direction of charge flow assumed by Wright for the drain region in his model is

$$J_x = -\mu\varepsilon_o\varepsilon_r \left(\frac{\partial E_x}{\partial x}\right) E_x \; . \qquad (2\text{-}16)$$

This differs from Equation (2-15) only by the term in $\frac{\partial E_y}{\partial y}$. For the case of a reasonably thick semiconducting channel this approximation is valid. Thus it is seen that the theory of Geurst gives results similar to those obtained by Wright.

Equations (2-12) and (2-13) are the non-linear boundary condition for the electric field in the insulator region. By use of a complex transformation the transcendental equation relating the source-drain current, I_D, to the source-drain

voltage, V_D, and the gate voltage, V_G, was found to be

$$\log \left[\frac{\frac{\pi L}{h} [1 - \frac{(1 - \eta^2)}{d}]}{(1 - e^{-\pi L/h})} \right] + 1 - \frac{\frac{\pi L}{h} [1 - \frac{(1 - \eta^2)}{d}]}{(1 - e^{-\pi L/h})} + \frac{\pi L}{h} \frac{\eta^2}{j} = 0 \qquad (2-17)$$

where the dimensionless current, j, and the dimensionless voltage, η, are defined by

$$j = - \frac{I}{\frac{\mu \varepsilon_o \varepsilon_r}{hL} (V_G - V_o)^2} \qquad (2-18)$$

$$\eta = \frac{V_D}{(V_G - V_o)} - 1 \qquad (2-19)$$

This equation has been solved numerically in terms of the geometric ratio h/L, which is the ratio of the insulation thickness to source-drain gap. The model shows that the amount of saturation expected is related in a non-linear manner to the ratio h/L, and that for smaller values of h/L it becomes asymptotic to the gradual approximation with perfect saturation for $V_D \geq (V_G - V_o)$.

To illustrate this behavior Geurst's model has been solved for two values of h/L for a conventional evaporated TFT. The ratios h/L = 1/50 and h/L = 1/25 correspond to insulation thickness of 1,500 Å and 3,000 Å for L = 7.5μ. The results of

these calculations are displayed in Figures 2-4 and 2-5. It can be seen that the device with the thinner insulation (Fig. 2-4) has a higher saturation resistance as well as a larger transconductance. This is due to the increased screening and capacitance of the more closely spaced gate electrode.

2.5 Low Frequency Characteristics

The small-signal transconductance, g_m, and output conductance, g_{Do}, obtained from the gradual approximation (equation 2-4) are given by

$$g_m \equiv \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D} = \frac{\mu C_G V_D}{L^2} \text{ for } V_D \leq (V_G - V_o)$$

$$= \frac{\mu C_G}{L^2}(V_G - V_o) \text{ for } V_D \geq (V_G - V_o) \qquad (2\text{-}20)$$

$$g_{Do} \equiv \left(\frac{\partial I_D}{\partial V_D}\right)_{V_G} = \frac{\mu C_G}{L^2}(V_G - V_o - V_D) \text{ for } V_D \leq (V_G - V_o)$$

$$= 0 \text{ for } V_D \geq (V_G - V_o) \qquad (2\text{-}21)$$

Experimentally, one finds poor agreement with these expressions. Typical results for a silicon evaporated TFT[24] are compared with this theory in Figures 2-6 and 2-7.

In deriving equations (2-20) and (2-21) an extremely simplified model was used. In particular, trapping effects,

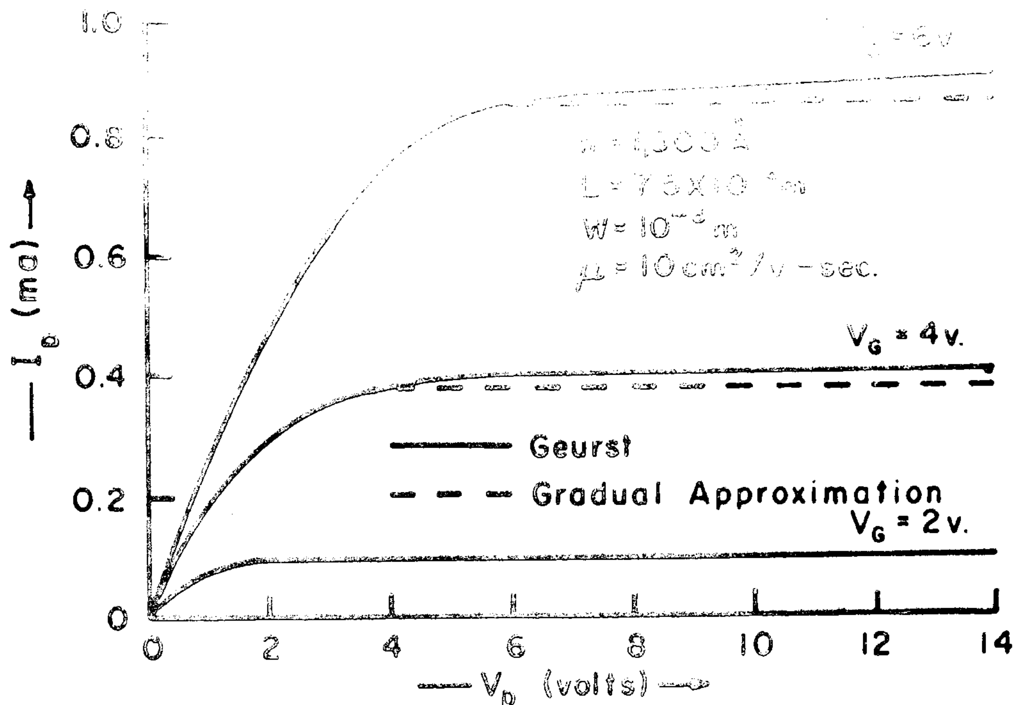


Figure 2-4. Static TFT Characteristic for h/L = 1/50.

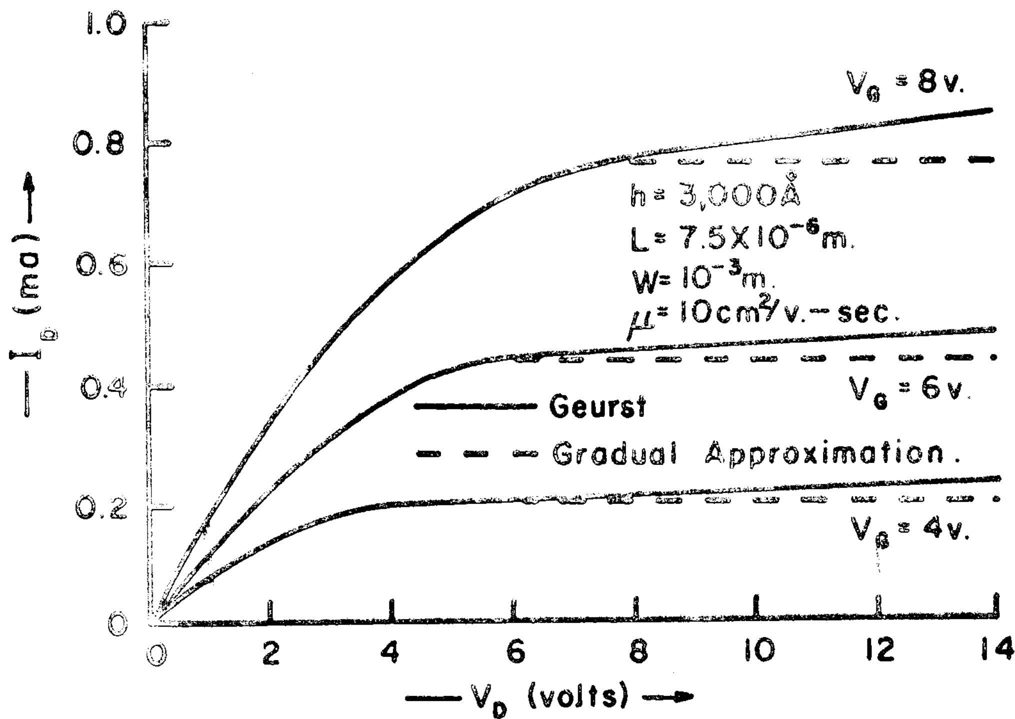


Figure 2-5. Static TFT Characteristic for h/L = 1/25.

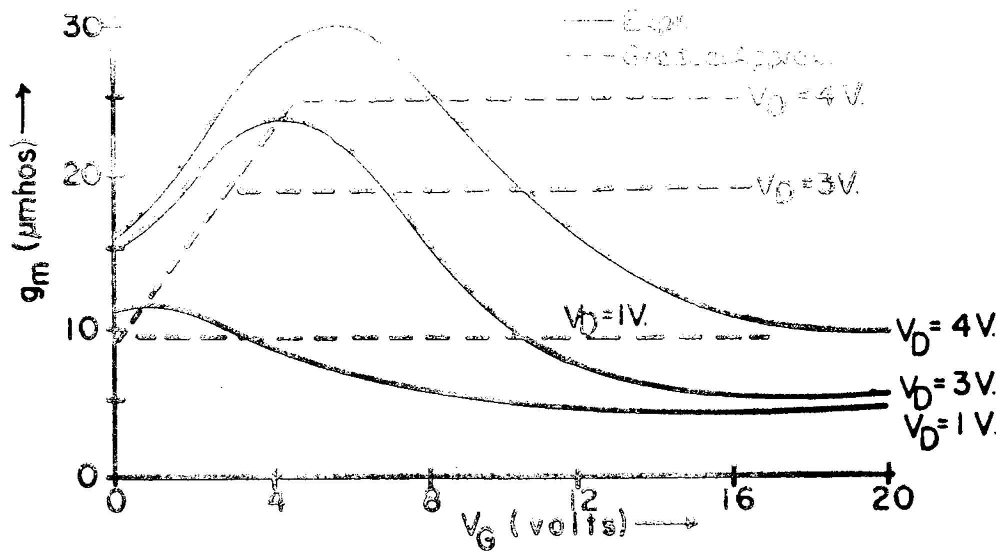


Figure 2-6. Variation of Transconductance of Silicon TFT with Gate and Drain Voltage.

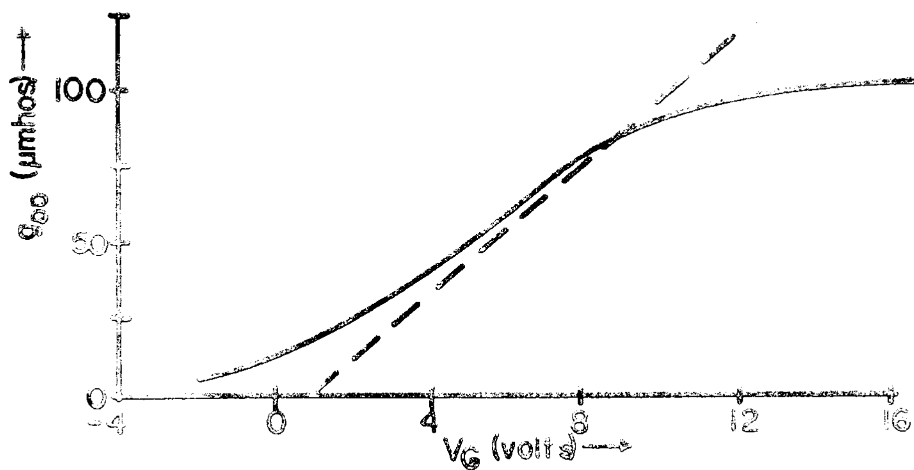


Figure 2-7. Variation of Output Conductance of Silicon TFT with Gate Voltage.

mobility variations and gate capacitance variations were ignored. Waxman et al.[25] have measured the Hall mobility vs. gate voltage in a modified CdS TFT and have obtained the results shown in Fig. 2-8. The increase in mobility at low gate potentials is thought to be due to the filling of traps at intercrystalline barriers,[26, 27] while at high gate voltages the mobility will vary as $1/E_G$ as predicted by Schrieffer[28] for non-degenerate surface scattering.

The measured dependence of gate capacitance on gate voltage[19] for a typical TFT is shown in Fig. 2-9. The total gate capacitance corresponds to a series combination of the oxide and semiconductor surface capacitance.

$$C_G = \frac{C_{ox} C_s}{C_{ox} + C_s} \qquad (2\text{-}22)$$

Equation (2-22) is a very instructive way of expressing the gate capacitance because the total capacitance will deviate from the oxide capacitance only to the extent that the surface potential can follow the applied signal.

In evaporated polycrystalline CdS films the transconductance as well as the mobility will be dependent upon the filling of traps located at grain boundaries and scattering from ionized impurities. Since a time constant is associated with the filling and emptying of these traps, their presence may be observed most easily by examining the frequency dependence of the transconductance.

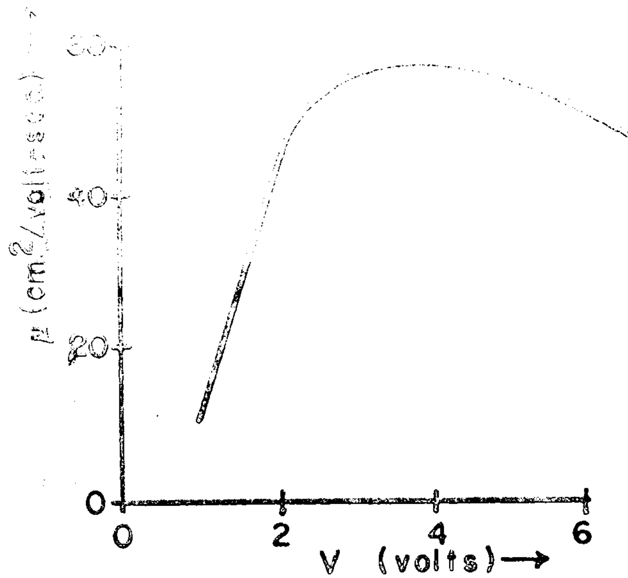


Figure 2-8. Hall Mobility in an Evaporated CdS TFT Plotted as a Function of Gate Voltage.

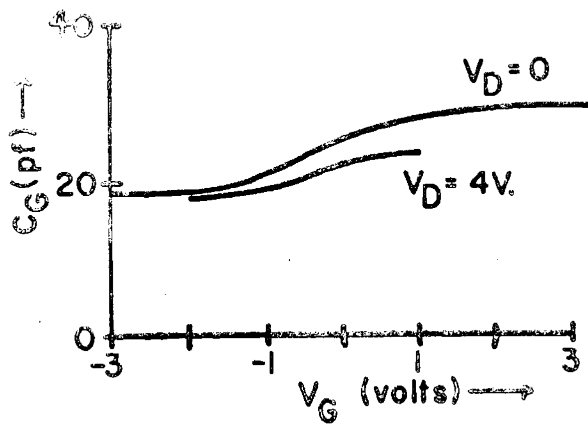


Figure 2-9. Gate Capacitance of a CdS TFT Plotted as a Function of Gate and Drain Voltage.

In the next section a model by Haering is discussed which shows that the magnitude and phase of the small-signal a.c. transconductance allows one to infer which physical mechanism is responsible for the conductivity modulation.

2.6 The A.C. Transconductance

Haering[29] has discussed a model of the TFT in which the mobility as well as the electron concentration is allowed to vary with the gate voltage. Thus the differential conductance, $d\sigma$, of the channel becomes

$$d\sigma = \Delta n q \mu + n q \Delta\mu. \qquad (2\text{-}23)$$

where q is the electronic charge and n is the electron concentration. This model postulates that the mobility variations depend upon the occupancy of impurities or trap states; the dependence of mobility on channel narrowing is neglected although the model could be extended to include this case. Waxman et al.[25] have also postulated and observed this variation in mobility with surface potential, but did not use this information to calculate the frequency dependence of the transconductance. In addition to the assumptions stated in Section 2.2 this model assumes a single set of traps or impurity states which obey the Boltzmann distribution.

Using this model it is possible to calculate the frequency dependence of the small signal transconductance, g_m, in terms of the variation of mobility with the density of trapped

electrons. The transconductance has been shown to be

$$g_m = \frac{\mu V_D}{L^2} C_G \left(\frac{dn_c}{dn} + \beta \frac{dn_t}{dn}\right) , \qquad (2\text{-}24)$$

where $\beta = (nc/\mu)\ (d\mu/dn_t)$, and dn denotes the change in total electron concentration as a result of a change, dV_G, in gate voltage. By assuming that the a.c. quantities in equation (2-24) are small, one may obtain the frequency dependence of the transconductance shown in Fig. 2-10. The importance of mobility variations is included in the parameter β. For the case $\beta = 0$ (constant mobility) the transconductance is always an increasing function of frequency. That is, for frequencies lower than those characterizing the traps, a fraction of the electrons induced will be trapped resulting in a lower transconductance than at high frequencies, where the traps are unable to follow the induced carrier variations.

For the case of large mobility variations ($\beta > 1$), the transconductance is a decreasing function of frequency. The transconductance will be large at low frequencies due to the modulation of the density of trapped electrons. Since the traps cannot follow the gate voltage at high frequencies, the transconductance is a decreasing function of frequency.

Experimental studies[30] of TFT's with slow surface traps are in accord with the principle of carrier mobility variation as well as carrier concentration variation with applied gate voltage.

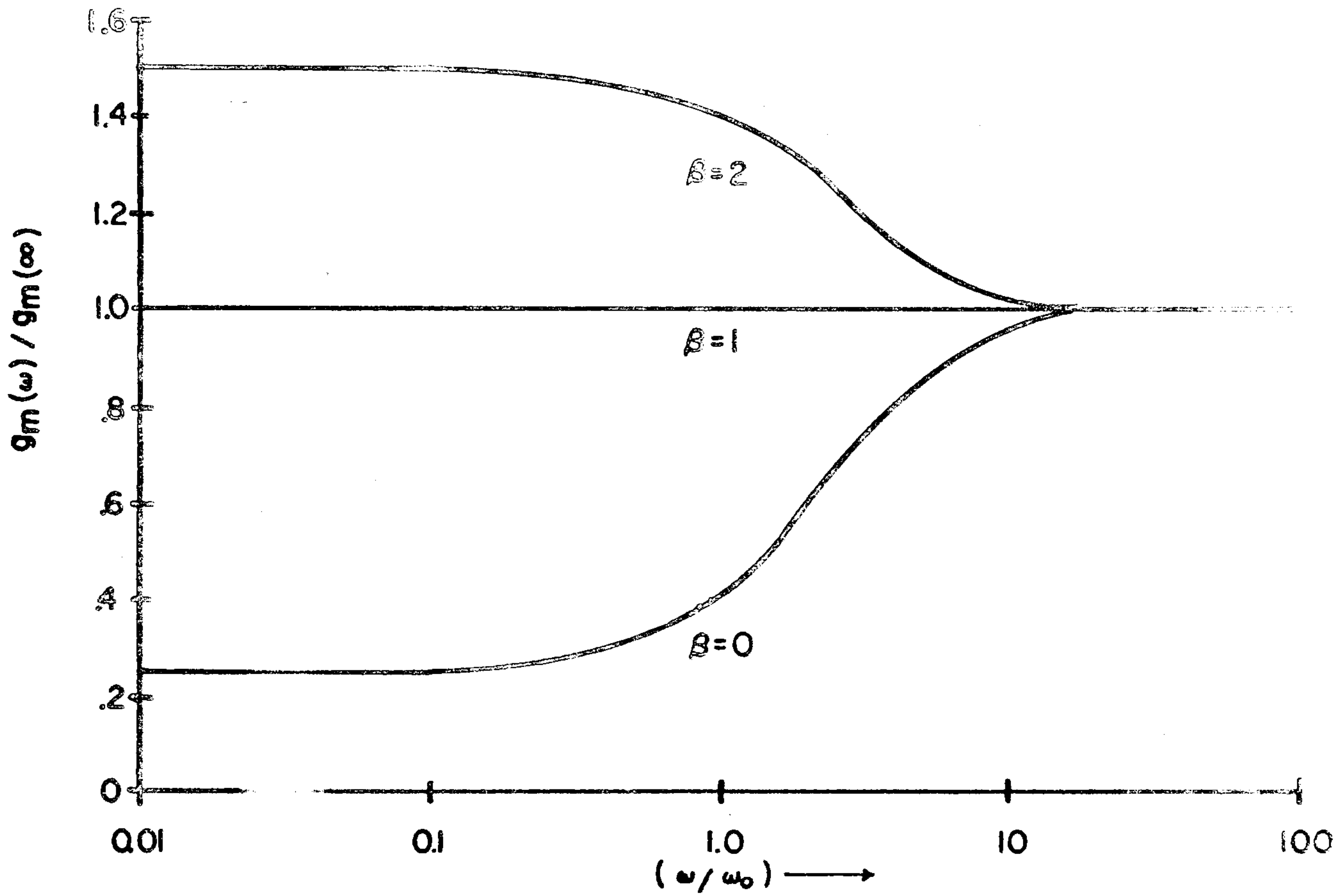


Figure 2-10. Variation of $|g_m(\omega)|$ with frequency. The parameter β measures the importance of mobility variations.

2.7 Comparison of TFT Theory with Experiment

2.7.1 Static Characteristics

The static characteristics of a TFT may be adequately described by equation (2-4) in the region $V_D < (V_G - V_o)$. Within this region the models of Wright and Geurst reduce to the gradual approximation of Many.

In the saturation region, the models of Wright and Geurst both postulate a finite saturation resistance. However, the two theories are based on entirely different physical assumptions. Wright has assumed that the current is carried in a high resistivity material by space charge, and that operation occurs under space-charge-limited conditions. Geurst has related the finite saturation resistance to the geometry of the transistor, specifically to the geometric configuration of its electrodes. His model, however, assumes an infinitely thin semiconducting layer.

The above models are inadequate to describe the non-saturated behavior often observed. For the case of the semiconducting insulated gate field-effect transistor, Hofstein and Heiman(21) have related the output resistance in saturation to the excess charge carriers induced in the channel by the drain electrode at the substrate side of the semiconductor. The output resistance calculated by these authors gives rise to a voltage amplification of the same order of magnitude as that measured on real transistors.

A different explanation of the finite output resistance at saturation has been put forward by Johnson[20]. He assumes that the donors present in the semiconducting layer are only partially ionized. The saturation region of the I-V characteristics would then correspond to ionizing the donors in the deeper-lying levels. Complete saturation would occur only at drain voltages greater than the transistor could withstand.

None of the above models take trapping states or mobility variations into account, thereby making a comparison with the real transistor difficult.

2.7.2 Dynamic Characteristics

The measured transconductance and output conductance do not agree well with the gradual approximation as shown in Figures 2-6 and 2-7, because the derivation neglects the effects of traps, mobility variations and gate capacitance variations.

The model of the a.c. transconductance of the TFT by Haering[29] discussed in Section 2.6 has been used by Miksic et-al.[30] to analyze the frequency dependent transconductance of TFT's in the range 1 to 1,000 cps. The observations can be understood in terms of the model which postulates gate voltage induced mobility variations in addition to trapping effects. Although this model is unable to explain the high effective mobility

obtained by Weimer[7], the postulate of gate voltage induced mobility variations is confirmed by the work of Waxman et al.[25] displayed in Fig. 2-8.

3. APPARATUS AND MATERIALS FOR THE FABRICATION OF EVAPORATED THIN-FILM TRANSISTORS

3.1 Introduction

The thin-film devices necessary for this work were fabricated by vacuum evaporation techniques. This section describes the equipment, materials and methods used to fabricate the structures, and the apparatus for measuring the thickness of the deposited films.

3.2 The Vacuum System

The evaporation system consists of an NRC Model 3176+ vacuum coater equipped with an 18" diameter glass bell jar and a 7" diffusion pump which is capable of pumping the system to 10^{-7} Torr. A vacuum collar with 16 two inch ports was installed between the bell jar and the base plate for greater flexibility. The mask changer, which is mounted on the collar, is capable of registering any one of 6 masks adjacent to the substrate to within 0.001 in. and shuttering the evaporant from any one of 5 resistance heated sources. Fig. 3-1 illustrates the mask changing apparatus.

3.3 Control of the Substrate Temperature

In the deposition of thin layers by vacuum evaporation, knowledge of the substrate temperature is important. For example,

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\+ NRC Equipment Corp., Newton, Massachusetts.

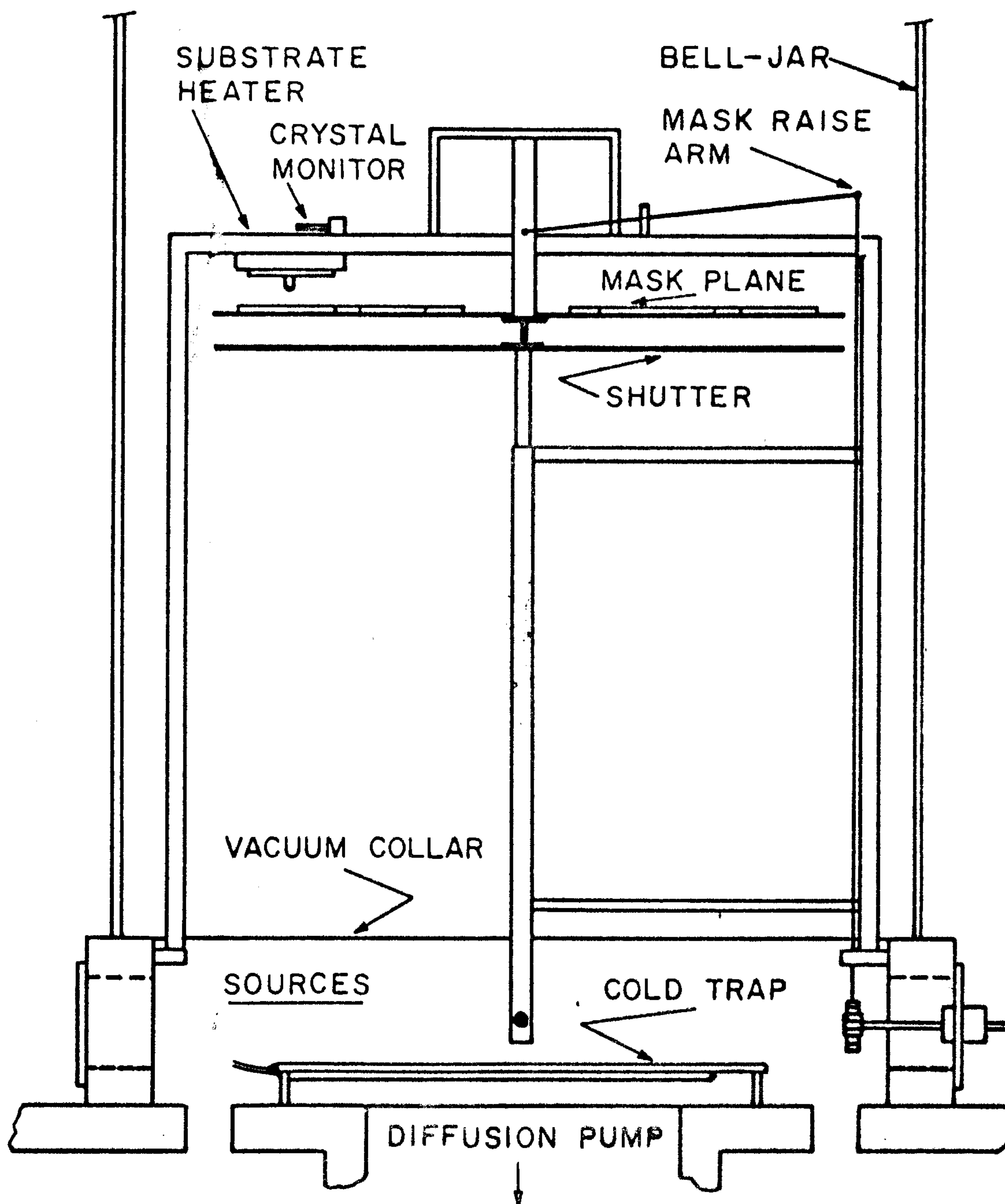


Figure 3-1. Mask Changing Apparatus

the resistivity of CdS, and the dielectric constant and optical properties of SiO and GeO_2 are determined in part by the substrate temperature. The two main problems in the control of the substrate temperature are the inability to heat the substrate unifromly and the difficulty in measuring the temperature of the substrate surface facing the evaporant. The most common material used as a substrate is glass; which, because of its low thermal conductivity makes the problems of temperature control and measurement more difficult.

One common technique used is to heat the substrate by means of radiation. A black box heater or a line source placed at the focus of a parabolic, reflecting cylinder has been used.(31, 32, 33) Another commonly used heater is constructed by pressing the substrate against a heated copper block.(30) Unless the substrate makes reproducibly uniform contact to the heater, the temperature of the front surface will not be accurately known. Since the spectral transmittance of most glass shows a distinct cutoff near 25,000 Å, any radiation whose wavelength is greater than this will be absorbed by the glass. Hanson(34) has shown that a heater whose temperature is less than 500° C will have $> 99\%$ of its energy in the region $\lambda \geq 25{,}000$ Å. Thus a large-area, low-temperature heater which will distribute energy evenly over the surface of the substrate appears most desirable.

If extremely accurate temperature control over a large substrate for a long period of time is desired, then one may

use an elaborate method developed by Hanson[34], in which the entire bell jar is heated in an oven. Such a system has been able to maintain a temperature stability of 250°C ± 2°C.

When using radiation heaters one conventionally presses a thermocouple to the side of the substrate facing the heater[32, 33] or evaporates a thermocouple (for example, Ni - Fe) on the side of the substrate facing the evaporant.[34, 35] Both are subject to error because of temperature gradients in the substrate. Also, neither thermocouple absorbs the same energy per unit area from a radiation heater. Conduction heaters are usually monitored by a thermocouple attached to the heater block. In such cases the temperature of the front surface is not known unless the heater is first calibrated.

Two methods of heating were chosen by the author: the conventional conduction heater, where the substrate was clamped to a heated copper block, and the directly heated substrate where current is passed through the sintered tin oxide film on the reverse side of the substrate.

3.3.1 The Conduction Heater

The conduction heater used is illustrated in Fig. 3-2. The substrate is clamped to the lower surface of the copper heat sink. Imbedded in the copper block are lengths of $\frac{1}{4}$" copper tubing through which cryogenic liquids or heated air may

be passed. This heater was chosen because of the wide temperature range that is so easily available. The temperature of the copper heater was monitored by a copper-constantan thermocouple. The mask and shutter planes lie 1 and 2 inches below the substrate respectively before evaporation. During evaporation the mask plane is moved to within a few thousandths of an inch from the substrate. The substrate material used was Corning 0211 glass. The substrates were 2" x 2" x .024" and coated on one side with a sintered tin oxide film with a resistivity of 100Ω/square. The SnO surface was placed adjacent to the heater to help achieve a uniform temperature distribution on the substrate. Details of substrate cleaning procedures may be found elsewhere.[36, 37, 38]

The temperature of the front surface was measured by use of an evaporated gold resistance thermometer. This thermometer was calibrated by means of a copper-constantan thermocouple. Annealing effects were observed during the first heat-up of the gold film; the resistance was then linearly proportional to the temperature.

The steady-state temperature of the substrate surface was then measured as a function of the heater temperature with a TFT mask held in evaporation position. The time required for the system to come to equilibrium was 45 minutes. Fig. 3-3 shows the resulting calibration curve and transient response of the system. Several gold thermometers were constructed. All

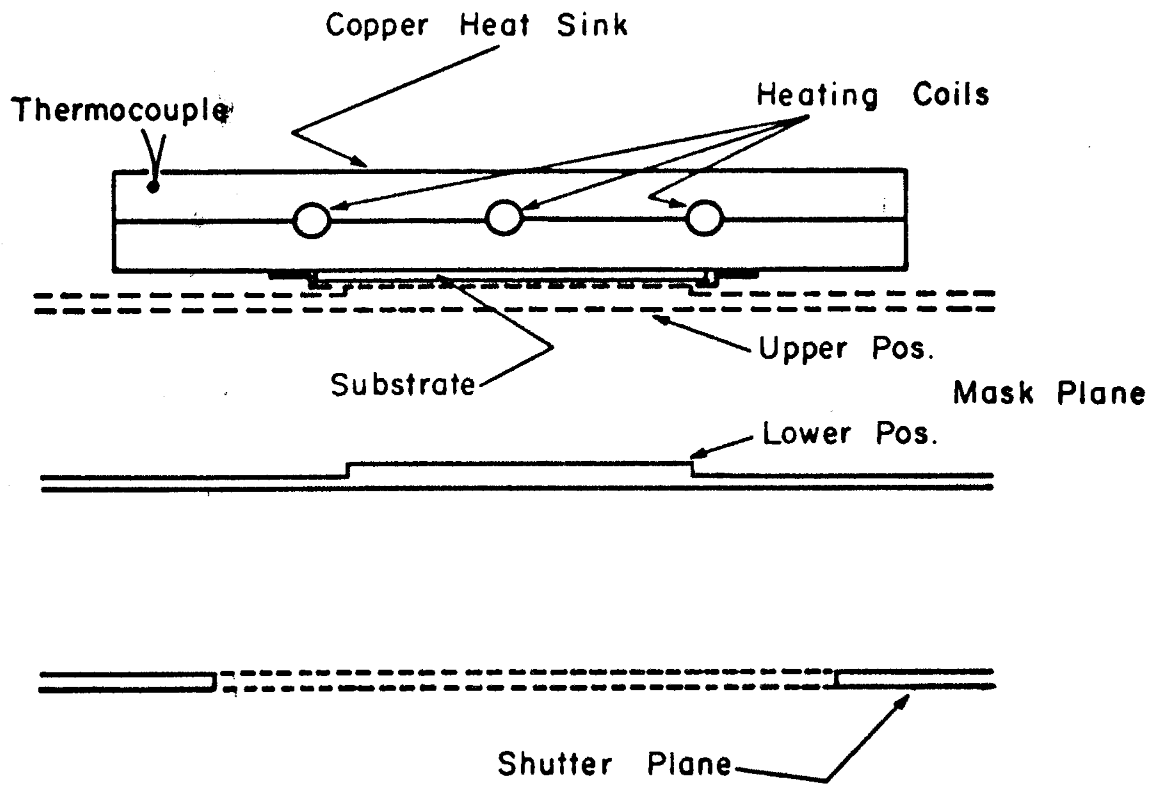


Figure 3-2. Conduction Substrate Heater.

gave results within a few degrees. The evaporation of a silver film or the use of silver paint on the side of the glass in contact with the heater failed to improve the good thermal contact between the heater and substrate already obtained with the sintered tin oxide film. Insulating layers evaporated on the Au thermometer through masks resulted in a temperature rise of only 3°C. This temperature rise is due to radiant heating of the substrate by the source and is small because of the distance (16") between them.

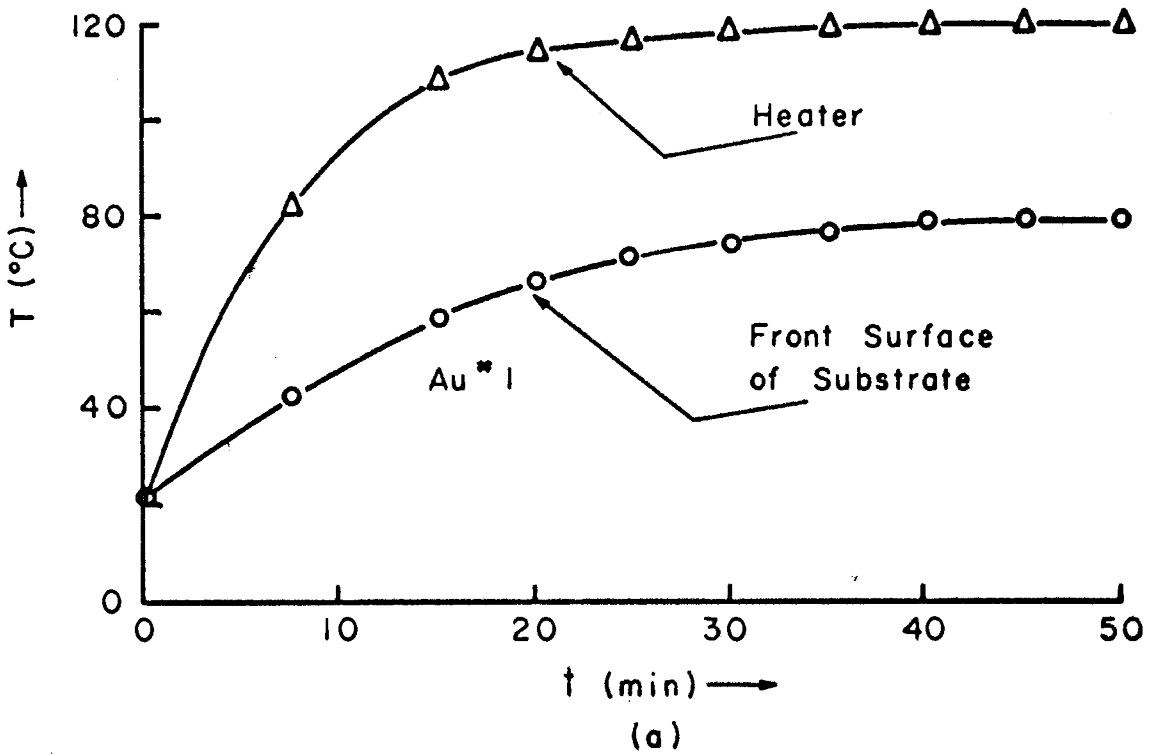
Although this system has a very long time constant, it is reasonably accurate (±20°C) and can be used in the temperature range -180°C to +100°C.

3.3.2 The Directly Heated Substrate

A new heating method developed by the author makes use of the conductive properties of the sintered tin oxide film on the Corning 0211 glass. Such glass has been employed for some time in heating aircraft windows. A uniform current distribution was obtained by baking silver paint strips across opposite ends of the glass. Fig. 3-4 describes the substrate heater. The front surface mirror located behind the substrate is used to reduce the radiation loss. A reference thermocouple was installed so that it makes contact with the conducting side of the glass by means of a small drop of mercury-gallium-indium alloy. The reference thermocouple was placed near the

edge of the film so that it will not adversely affect the temperature distribution in the region where the TFT will be deposited. Although spacial variations in temperature are anticipated, it was expected that the central region would be uniform enough for the evaporation of CdS, SiO_x, and GeO_2. A check was made as follows: the temperature in the central region of the surface facing the evaporant source was measured with a small Pt/Pt-10 Rh thermocouple which was wetted with the alloy described above. The mask used for the deposition of CdS in the high voltage TFT contains four 1/8" holes spaced 0.2" apart in its central region; this mask was placed as during evaporation, and the thermocouple consecutively placed in each hole. The temperature at each position was recorded for a constant reference temperature while the system was pumped below 10^{-6} Torr. Fig. 3-5 shows the results obtained. The variation observed is insignificant for the materials evaporated in this study.

One obvious advantage of this heater is its small power requirement; only the glass itself is being heated directly and it has a small mass. Fig. 3-6 shows that less than 4 W. is necessary to achieve the highest temperature of interest. This system will come to thermal equilibrium in 10 min. because of the small heat capacity of the substrate. Fig. 3-7 shows a calibration curve for the heater designed in this study. It relates the temperature of the reference thermocouple located on the reverse side of the substrate to the front surface temperature in the central region where the



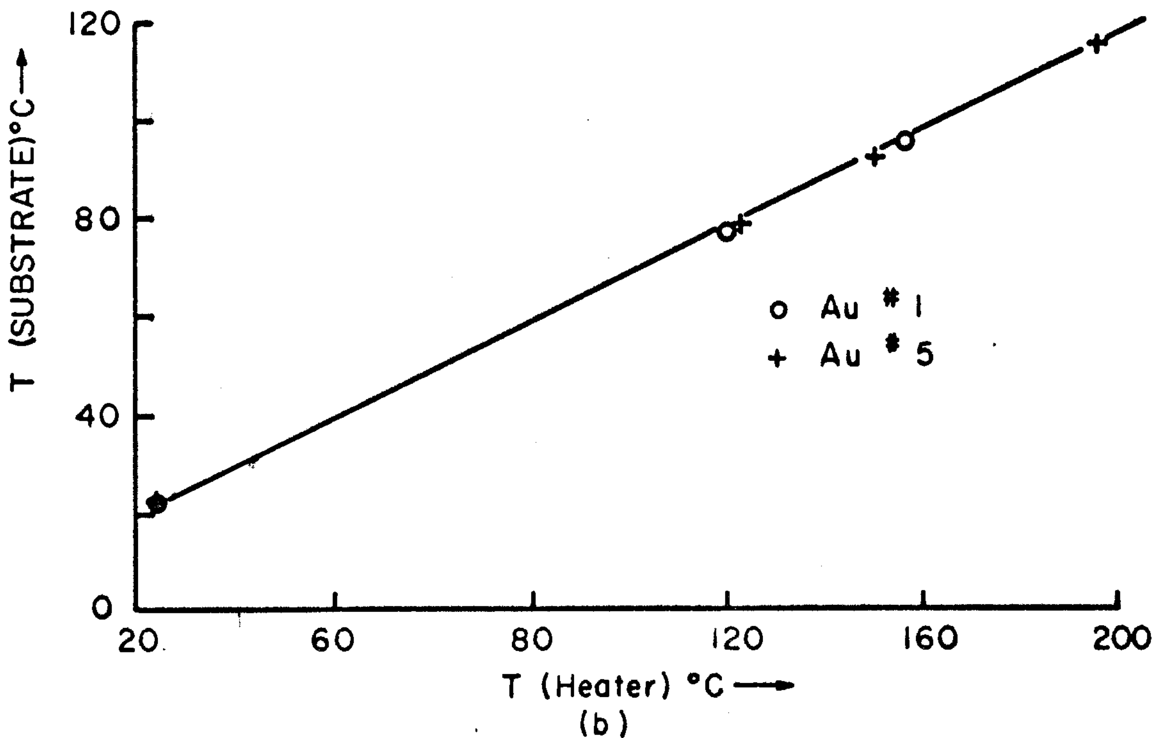


Figure 3-3. (a) Transient response of heater and substrate.
(b) Correspondence between substrate surface temperature and heater temperature.

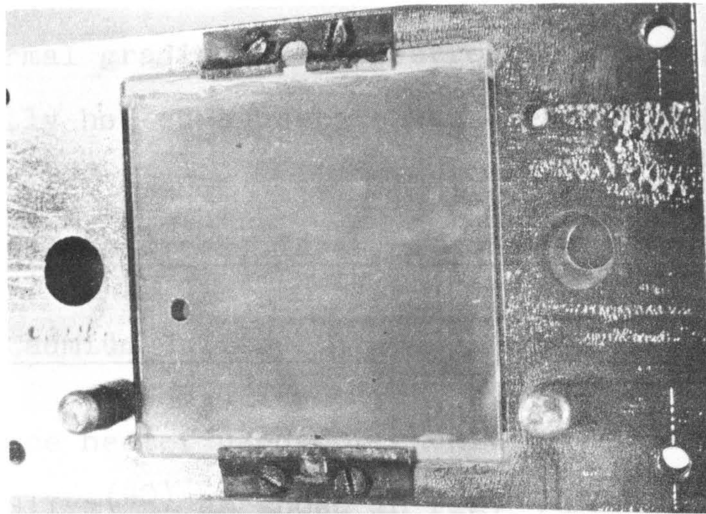


Figure 3-4. Directly heated substrate. A front surface mirror is located 1/16" behind the substrate. The silver strips and hole for the reference thermocouple are visible.

active devices were deposited. Although temperature gradients larger than those shown in Fig. 3-5 may exist elsewhere on the substrate, it is seen that this heater is useful for experiments where only the central portion of the substrate is used for devices where tolerances of a few degrees centigrade are allowed. Low power requirements and a short time constant are its main advantages. This substrate may not be heated much in excess of 250°C or thermal gradients may destroy the glass. A description of the directly heated substrate has been published.[39]

3.4 Evaporation Sources, Materials and Techniques

3.4.1 Cadmium Sulfide

The source heater used for cadmium sulfide follows a design by DaSilva[40] as shown in Fig. 3-8. The CdS films were prepared from Eagle-Picher "High Purity Grade A" CdS which was packed around the central core and covered with a baffle to prevent "splitting". A detailed discussion of the evaporation of CdS is given in Section 4.

3.4.2. Silicon Monoxide

The properties of SiO films are quite sensitive to the evaporation conditions; the evaporation rate, source temperature, substrate temperature and ambient oxygen pressure influence the electrical, physical and optical properties of the deposited films. In this subsection a brief summary of the conditions known to influence the nature of the SiO films is given, followed

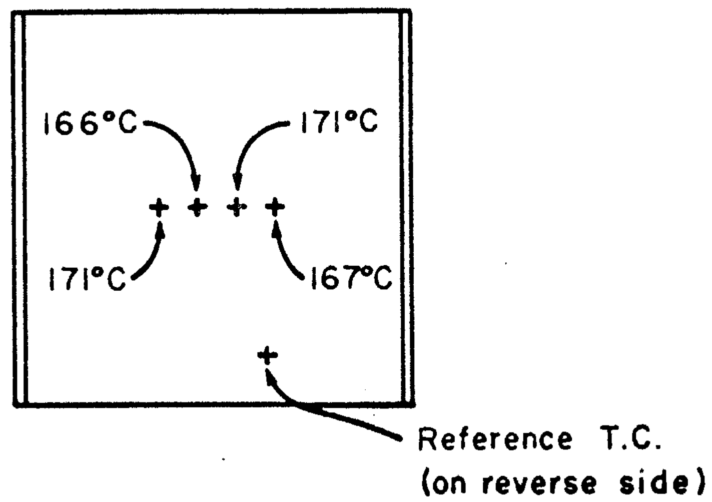


Figure 3-5. Temperature distribution on substrate in regions used for evaporation of CdS in the high voltage TFT.

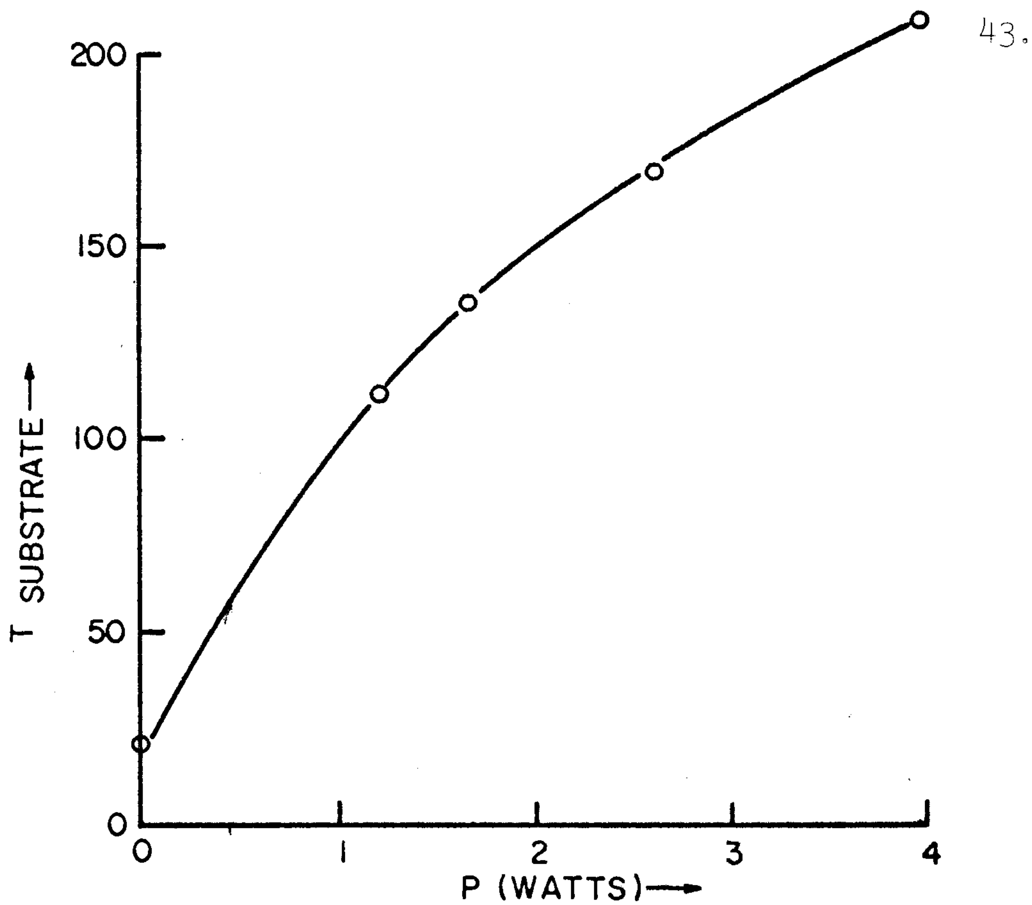


Figure 3-6. Power Input to Substrate vs Front Surface Temperature of Substrate

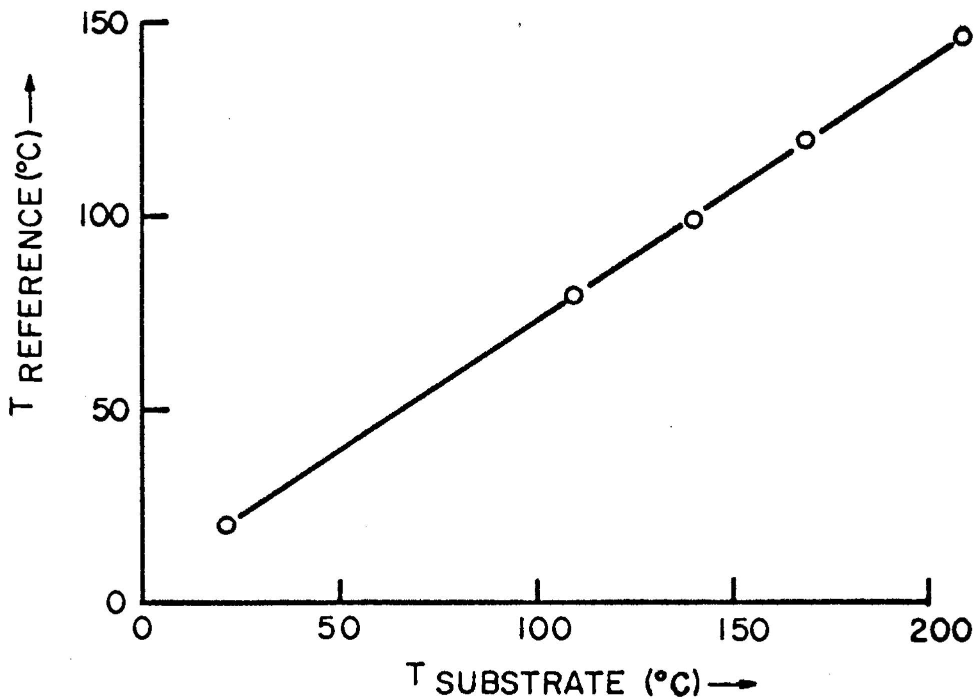


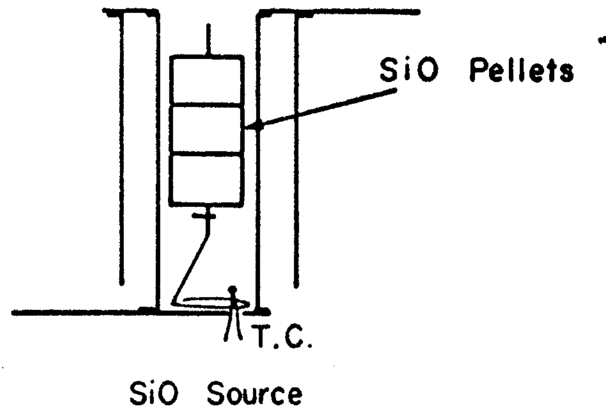
Figure 3-7. Front Surface Temperature of Substrate vs Reference Temperature

by the technique employed in this study.

Schwartz and Berry[41] have reported that for SiO evaporated at pressures of < 10^{-5} Torr the film composition depends upon the deposition rate. For rates of 1-5 Å/sec. porous low-density films were obtained which oxidized quickly in air to colorless films with an ultraviolet transmission characteristic of SiO_2. At intermediate deposition rates of 6-12 Å/sec. the films had a density comparable to bulk SiO and an amber color. At high deposition rates (25 - 30 Å/sec.), the film density exceeded that of bulk SiO, and electron diffraction indicated a solid solution of Si and SiO_2. They also observed peeling when films were exposed to moisture. This peeling was caused by excessive compressional stress, and could be eliminated by heating the substrate during deposition.

The color change of films evaporated in 10^{-4} Torr of oxygen is attributed to oxidation of the SiO to higher phases. It was thought that this phase was predominantly SiO_2 but recent work by Ritter[42] has shown the existance of an intermediate phase Si_2O_3.

Anastasio[43] has shown that the dielectric constant and dielectric loss are a function of the ratio of molecular impingement rates of O_2 and SiO on the substrate independent of the absolute values of pressure or rate within the ranges studied (2×10^{-5} - 2×10^{-4} Torr, and 10 - 110 Å/sec.).



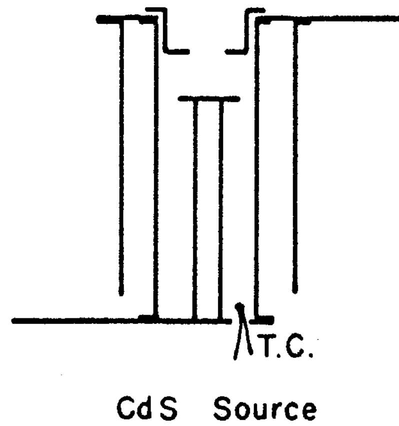


Figure 3-8. Tantalum Sources for the Evaporation of SiO and CdS

When this ratio, α, is less than 1 (excess SiO), it was observed that the dielectric loss sharply increased; for all values of α studied the dielectric constant was a decreasing function of α.

Thus films formed at high rates or low O_2 pressures ($\alpha < 1$) are unsuitable for insulation layers, because of the high dielectric loss due to the free silicon content. Films formed at low rates and high O_2 pressures ($\alpha > 1$) contain a larger fraction of SiO_2 and Si_2O_3, which have lower dielectric constants than SiO, and are more stable because they contain fewer O_2 vacancies.

In addition to the arrival rates of O_2 and SiO at the substrate, the concentration of higher oxides is affected by the substrate temperature, which determines the surface mobility of the deposited material, and by gas phase reactions[41].

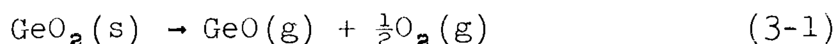
In this study SiO was typically evaporated from a source held at 1300°C at a rate of 5 - 10 Å/sec. in the presence of 10^{-4} Torr of O_2 onto a substrate held at 200°C. The resulting film is transparent and is referred to in this work as SiO_x. If the O_2 pressure is kept below 10^{-5} Torr, the resulting film is amber and more closely resembles SiO.

The source heater used for the evaporation of silicon monoxide shown in Fig. 3-8 is identical to that used for CdS

except for the method of supporting the charge. The SiO used in this study was Union Carbide "select grade", in the form of 1/4" x 3/8" pellets or in the form of #10 mesh lumps. As shown in Fig. 3-8, the pellets were drilled and suspended on a tantalum wire located in the center of the cylindrical heater. The lumps were evaporated from a boron nitride crucible placed in the cylindrical tantalum heater, and covered by a baffle. It is important that the SiO does not come into contact with the heated Ta walls as the resulting films were found to have a high dielectric loss factor. This is most likely due to the decomposition of SiO into free silicon and tantalum pentoxide; free silicon is known to cause a high dielectric loss,[44] and in these cases the SiO residue was coated with a purple tantalum oxide deposit. Decomposition of the SiO due to a reaction with the source can be eliminated by use of an electron beam source.

3.4.3 Germanium Dioxide

Germanium dioxide films were evaporated from a flat platinum boat at a temperature of 1,300°C and a rate of ~ 4 Å/sec. in the presence of 10^{-4} Torr of oxygen onto a substrate held at 200°C. During the initial operation of a fresh GeO_2 charge, the total system pressure may reach 2 x 10^{-4} Torr. This is in agreement with Drowart[45] who has shown that GeO_2 evaporates according to the reaction



$$GeO_2(s) \rightarrow GeO(g) + \tfrac{1}{2}O_2(g) \qquad (3\text{-}1)$$

The films deposited are probably a mixture of lower and higher oxides of germanium as was the case for silicon monoxide. Schwartz and Berry[41] have shown that multiple dielectrics composed of 5,000 Å of SiO and 1,000 Å of MgF_2, SiO_2 or Al_2O_3 show even lower leakages than SiO alone. GeO_2 was also used for this purpose.

3.4.4 Aluminum

Aluminum was evaporated from both tantalum coils and resistance-heated refractory crucibles constructed from boron nitride and boron nitride/titanium diboride. However, tantalum forms an alloy with aluminum, as does molybdenum and tungsten, and only the first 1,000 Å or so are pure enough to make ohmic contact to CdS. This type of source is useful in CdS device fabrication where only one aluminum evaporation is needed or where the CdS ohmic contacts are made with the first of the aluminum evaporations. In all other cases a more elaborate aluminum evaporation technique must be chosen.

Crucibles made from carbon or alumina are unsatisfactory because of the formation of aluminum carbide and aluminum oxide. Crucibles made from boron nitride, titanium diboride, were found to be satisfactory. These materials may be r.f. heated or resistance heated by a tantalum cylinder. Because aluminum wets and creeps on these materials, the top of the crucible should project sufficiently above the heater as to be below the melting point of aluminum. The crucibles should be thoroughly

vacuum out gassed before use after they have been exposed to atmospheric pressure. This may be done by heating slowly to the evaporation temperature of 1,000°C and waiting until a bright aluminum film is deposited. When heated, boron nitride may be decomposed by water vapor; the ammonia which is formed will then combine with the aluminum to form aluminum nitride.(46) If one does not properly outgas the crucible, the first aluminum layer evaporated will contain a large amount of the nitride and will be tinted brown. A summary of aluminum evaporation techniques is given by Holland(47); however, this book was published before the advent of the electron beam heater or of the boron nitride type crucible.

3.4.5 Calcium Fluoride

Calcium fluoride was evaporated from a simple tantalum boat at a temperature of 1,250°C onto a room temperature substrate at rates of 10 - 100 Å/sec. CaF_2 vaporizes according to the reaction(45)

$$CaF_2(s) \rightarrow CaF_2(g) \qquad (3\text{-}2)$$

however, CaF^+ is also formed by dissociative ionization of $CaF_2(g)$.(48)

3.5 Mask Design and Construction

The masks used to deliniate the pattern for each evaporation

were constructed from 0.005" beryllium-copper foil. A master drawing of each mask was first constructed 23 times the actual size. The drawings were then photographed on 35 mm. direct positive film. This image was then contact printed on the beryllium-copper coated with a thin layer of Kodak-Photo-Resist.[49] Subsequent etching of the exposed film in ferric chloride produced the final mask.

With the aid of registration marks, the masks were spot welded to stainless steel frames for proper location in the mask holder. Each one of the 6 masks could be aligned to within .001" of its ideal position, thus allowing the construction of intricate multi-layer structures.

3.6 Film Thickness Monitor

A quartz crystal monitor technique was used in this study. This method requires that a quartz crystal be located in the vapor stream near the substrate. The deposited film lowers the resonant frequency of the crystal. For small changes in resonant frequency the change in resonant frequency is a linear function of the deposited mass. The monitor system is discussed in detail in Appendix C.

Some experimentally determined frequency constants for the system used in this study are listed in Table 3-1. It should be noted, however, that due to the system geometry, each source coated only a fraction of the crystal area. Also,

some materials have sticking coefficients which vary with temperature and material, and thus it is necessary that the system be calibrated by evaporating a test film from each source. The test film was covered with a totally reflecting layer of silver or aluminum, and the Fizeau fringe shifts are measured by means of an optical interferometer[+] to an accuracy of ~ 100 Å. Fig. 3-9 illustrates the interference fringes obtained from a 2,000 Å CdS film. A calibration factor is then obtained which linearly relates the frequency shift of the crystal to the thickness of the film obtained.

+ Sloan Angstrometer, Sloan Instrument Company, Santa Barbara, California.

Material	Calibration Factor
Cadmium Sulfide	0.43 Å/cps. @ $T_{substrate}$=100°C
Silicon Monoxide	1.47 Å/cps.
Calcium Fluoride	3.46 Å/cps.
Germanium Dioxide	6.95 Å/cps.
Gold	0.15 Å/cps.

Table 3-1. Calibration Factors for Some Materials Evaporated in this System.

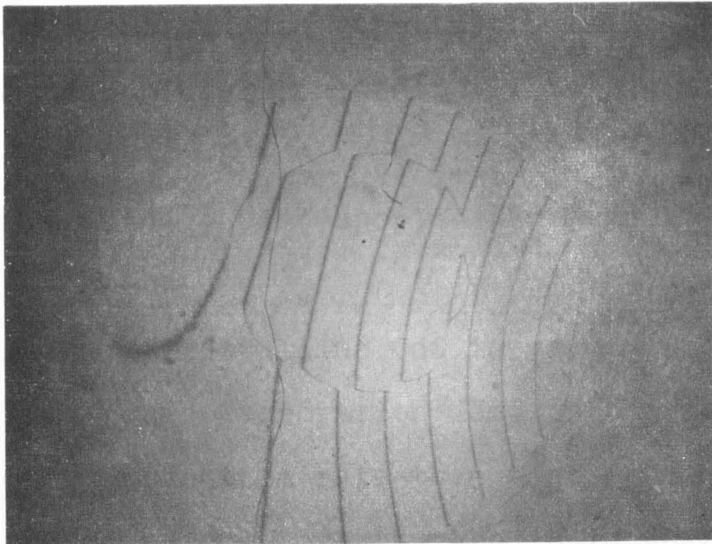


Figure 3-9 Interference fringes for a 2,000Å CdS film. The line spacing corresponds to the half wavelength of the sodium line λ = 5,890Å.

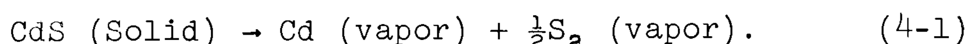
4. THE VACUUM EVAPORATION OF CADMIUM SULFIDE

4.1 Introduction

This section describes the mechanisms of vacuum evaporation and condensation of CdS. In addition the physical and electrical properties of the resulting films are described in terms of the techniques and procedures used.

4.2 Mechanisms of Evaporation

Cadmium sulfide is a member of a group of polyatomic solids which dissociate upon vaporization. It vaporizes according to the dominant reaction[50]



$$CdS\ (Solid) \rightarrow Cd\ (vapor) + \tfrac{1}{2}S_2\ (vapor). \qquad (4\text{-}1)$$

The vaporization of crystalline CdS in vacuum from an open source is called "free evaporation" and is characterized by a markedly slower evaporation rate than that obtained from equilibrium vaporization where the gas is in thermodynamic equilibrium with the solid. Experimentally, equilibrium evaporation is obtained from an effusion cell. In an effusion cell the molecular vapors do not stick to the heated walls, and thus come to thermodynamic equilibrium with the solid before emanating from the small exit hole.

Experiments have been carried out by Somorjai[50] on single crystal CdS to determine the mechanism of evaporation and

why the free evaporation rate is an order of magnitude less than the equilibrium rate. Somorjai has postulated that the evaporation of single crystal CdS is characterized by the following steps:

1. Formation of cadmium and sulfur surface atoms at their lattice positions.

2. The diffusion of Cd and S atoms on the surface.

3. Recombination of S atoms to form S_2 molecules.

4. Evaporation of Cd atoms from the surface into vacuum.

5. Evaporation of S_2 molecules from the surface into vacuum.

The rate limiting step in the free evaporation of an undoped CdS single crystal has been shown to be a charge transfer surface reaction which takes place prior to the desorption of neutral cadmium atoms and sulfur molecules from the surface.(51) For Cd or S doped CdS single crystals, Somorjai has shown that the charge transfer process leads to a condition in which the evaporation is controlled by the outdiffusion of excess sulfur or cadmium from the lattice. As the excess surface Cd or S_2 evaporates, it is replenished from the bulk by diffusion. Thus, bulk diffusion, which in turn controls the surface concentration of the excess element is the rate limiting step in this case.

For polycrystalline CdS powder the situation is not so clear. The observed rates are faster than free evaporation but

slower than equilibrium evaporation because a large percentage of the interior surface of the powder sample faces small crevices in which the vapor may be in thermodynamic equilibrium with the solid.

In the following sub-section evaporation techniques will be discussed in the light of this model of evaporation.

4.3 Techniques of Producing Evaporated CdS Films

CdS films are typically evaporated onto a heated glass slide from a freely vaporizing or equilibrium source. Böer[38] and Terry[52] have evaporated CdS from freely vaporizing quartz or tantalum sources onto substrates with temperatures in the range 23°C to 150°C. At temperatures over 150°C virtually no CdS will stick to the glass, while at room temperatures the films are gray to black, indicating a great excess of cadmium. Addis[53] has evaporated CdS from an equilibrium source. The region between the source and the heated substrate is enclosed by a chamber whose walls are heated to a temperature near that of the source. The impinging vapor stream thus bounces off the chamber walls but sticks to the substrate. The rate of condensation on the substrate is thus equal to the rate of vaporization from the CdS in equilibrium. In this manner good quality films were evaporated at much higher temperatures (up to 350°C).

Mass spectrometric analysis by Drowart[45] of the non-condensible gases evolved upon heating of the source material

in a platinum effusion cell at 1,000°K showed that the main constituents were Cd, S, S_2, S_3, S_4, while Addis[53] has shown that H_2S and CS_2 exist in a similar cell in addition to SO_2 for samples previously exposed to air.

For a freely vaporizing charge of CdS Coburn[54] has shown that Cd and S_2 are predominant vaporization products. Fig. 4-1 shows portions of the mass spectrum before and during heating of the CdS charge. The sensitivity of the spectrometer is not constant over the mass range shown; thus one should examine only the relative changes of a particular mass peak. The S_2 peak increased by a factor of 300, while the mass 32 peak (O_2, S) increased only by a factor of 2. In addition, mass peaks at 65 (S^{32} S^{33}), and 66 (S^{32} S^{34}) were clearly visible. All eight cadmium isotopes were present.

In this study CdS was evaporated from the cylindrical, baffled tantalum source discussed in Section 3.4 with a source to substrate distance of 16". Substrate temperatures from 77°K to 180°C were used. Above 120°C no deposits were observed on the substrate. In the range 90 to 110°C bright yellow films approximately 2,000 Å thick were deposited which had resistivities in the range 50 to 1,000 Ω-cm. Films of the same thickness deposited on room temperature substrates were black, indicating a heavy cadmium concentration, while those deposited at 77°K were dark orange, which is the characteristic color of amorphous CdS.

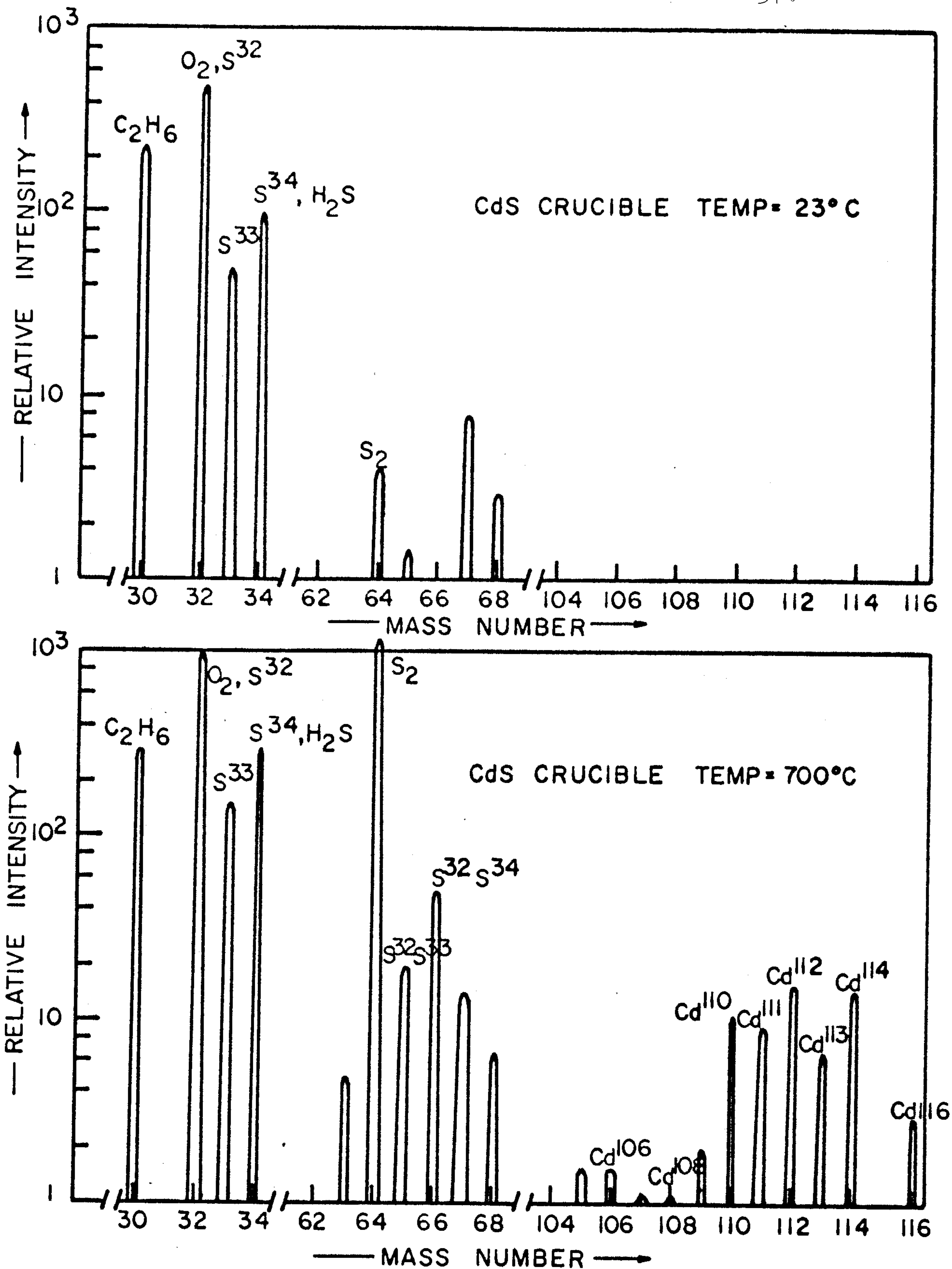


Figure 4-1. Mass spectrum before and during the evaporation of CdS from a Ta crucible.

4.4 Electrical Properties

The resistivity and Hall mobility of evaporated CdS films are functions of the substrate temperature and condensation rate of the film. In general, both quantities increase with higher substrate temperatures and decrease with higher condensation rates. A resistivity range of 10 to 10^5 Ω-cm and a mobility range of 5 to 40 cm^2/V-sec. have been reported.[48] The resistivity, Hall mobility, and free carrier concentration of typical films evaporated in this study are shown in Table 4-1.

Sample	Resistivity (Ω-cm)	Hall Mobility cm^2/V-sec.	Electron Concentration cm^{-3}
H-3	60	2.8	3.7×10^{16}
H-4	36	3.1	5.5×10^{16}
H-6	125	4.4	1.1×10^{16}
H-7	280	4.9	4.6×10^{15}

Table 4-1. Resistivity, Hall mobility, and free electron concentration of typical 2,000 Å to 7,000 Å thick CdS films evaporated on a glass substrate and measured at room temperature.

One must take care in comparing resistivity and Hall mobility data for thin films, as ambient surface conditions can enhance or deplete the surface layers giving rise to order of magnitude errors due to free-carrier concentration and mobility variations across the thickness of the film. For very thin films ($<$ 2,000 Å) it is possible for the surface condition to mask out almost

entirely the variations due to substrate temperature and condensation rate. This is discussed in detail in Section 5.

Addis[53] has made the following model to account for the variations in resistivity of CdS films with substrate temperature. Since Cd and S_2 exist in vapor, their condensation coefficients may be considered separately. At sufficiently low temperatures the cadmium condensation coefficient is quite high, while for sulfur it is quite low (the sulfur vapor pressure is about four orders of magnitude greater than the cadmium vapor pressure). The sulfur condenses effectively only when it arrives at appropriate sites for reforming CdS. Thus films with a large excess of cadmium and a consequent low resistivity are formed. At higher temperatures the cadmium condensation coefficient is decreased, and films are formed with a smaller excess of cadmium. At sufficiently high temperatures the cadmium condensation coefficient becomes negligibly small, and no film forms on the substrate.

The condensation coefficient of cadmium is also a function of the substrate material as well as the temperature. CdS films evaporated over ohmic contacts of aluminum or indium show a thickness gradient extending $\sim$ 1 mm. on to the glass; the film deposited immediately over the metallic contact was thicker and darker in color indicating cadmium enrichment. Weimer[19] has shown that gold, which normally makes a rectifying contact to CdS, makes ohmic contact in this manner

because of an initial layer that is very cadmium rich. Good film uniformity near contacts was obtained by depositing the CdS prior to the ohmic contacts.

The increase in mobility is due to the increase in crystallite size with hotter substrate temperatures; intercrystalline barriers and trapping states are thought to be the dominant scattering mechanism.[25]

4.5 Crystalline Structure

CdS has two phases, hexagonal (wurtzite) and cubic (zincblende). Addis[53] has deposited thin films (less than 1,000 Å) of CdS from an effusion cell onto glass and noted that the films consisted of an agglomeration of small hexagonal crystallites about 800 - 900 Å across. He concludes that the films were randomly oriented as all the allowed Bragg reflections at about the right intensities were observed. These results are in agreement with Böer[38] and Terry.[52] Thin films deposited in this study showed similar characteristics. The CdS films were removed from the glass by etching away the glass with HF. The films then floated to the surface where they were placed on a microscope screen. Fig. 4-2 (a) shows a transmission electron micrograph of a 700 Å film evaporated onto a glass substrate at 100°C. The observed crystallite sizes of about 300 - 500 Å across show that thin films deposited onto glass from a freely evaporating source are essentially the same as those obtained from an effusion cell by Addis. Fig. 4-2 (b)

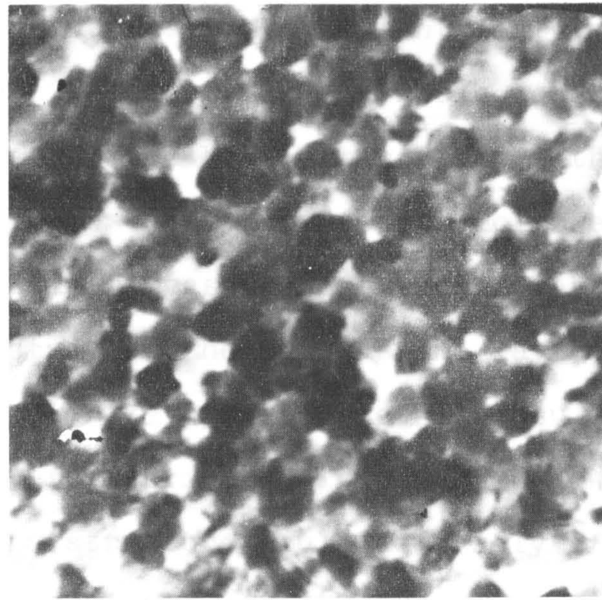
shows a selected area transmission diffraction pattern of the 700 Å film; the area selected is approximately 0.25μ. The more intense (h,k,l = 0) reflections show that there is some preference for the c-axis to be oriented perpendicular to the substrate. If all of the crystallites were oriented in this manner, only (h,k,l = 0) reflections would be present. No a-axis orientation was observed. These results are in agreement with those of Terry(52) and Foster.(55)

For thicker films ($\sim$ 1μ) the crystallites continue to grow predominantly in the hexagonal phase with the c-axis preferentially oriented perpendicular to the substrate. Crystallite sizes of 1μ have been observed by Addis and Terry. The hexagonal phase was observed to be the most predominant even in the thinnest films.(52) No evidence of the cubic phase was found in this work.

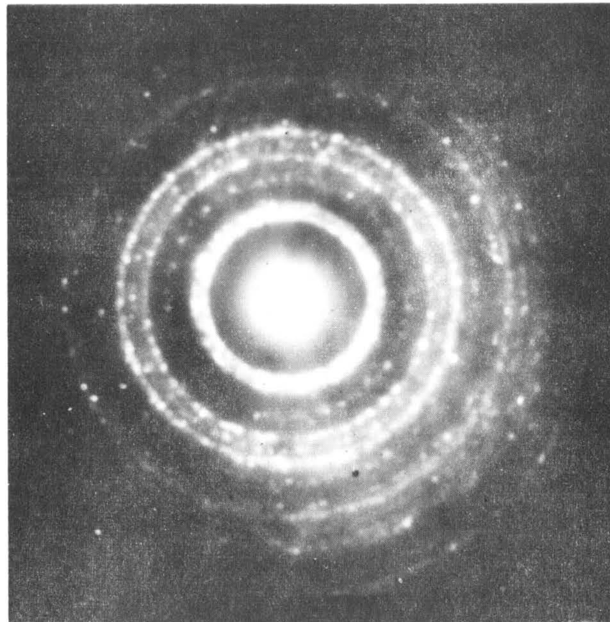
The lack of preferential orientation in addition to the small crystallite size in thin films observed by transmission electron microscopy apparently contradicts the results obtained on thicker films using X-ray and reflection electron diffraction techniques. This apparent discrepancy is explained by the small randomly oriented crystallites in the initial (< 1,000 Å) layer of the film.

4.6 Recrystallized Layers

Recrystallization is a post deposition treatment given to an evaporated film in order to increase the grain size and



(a)



(b)

Figure 4-2. (a) Electron Micrograph of thin CdS film (700Å thick);
(b) Electron transmission pattern for this film.

improve crystal boundaries to the extent that the effective mobilities approach values observed in single crystals. A CdS film may be recrystallized by first coating with a thin film of an activator such as silver or copper followed by treatment in vacuum or in an inert gas. These techniques were not employed in this study as the CdS was one layer of a structure composed of up to eight evaporated metal, insulator, and semiconducting layers fabricated in one pump down. Heat treatment of such a structure would adversely affect the resistivity of the CdS film as the aluminum used for contacts becomes a donor impurity upon diffusion into the CdS; removing the device from the vacuum system for post CdS deposition treatment introduces an unknown amount of surface contamination. For a complete treatment of recrystallization one may consult papers by van Cakenberghe[56], Böer[39, 57], and Addis.[53]

5. CONTROL OF THE SURFACE POTENTIAL OF EVAPORATED CdS LAYERS

5.1 Introduction

The conductance of evaporated films is strongly affected by the changes in the film surface. Weimer(19) has reported that depletion or enhancement surface layers may be produced on CdS films by a suitable choice of the insulating material and deposition conditions. These methods, however, do not allow continuous control of the surface potential and electron concentration. It is the purpose of this section to describe a simple method of controlling the surface potential and measuring the depletion depth in evaporated CdS films.

5.2 Principles of the Method

It has been shown that evaporation of SiO_x in a good vacuum produces an enhancement layer on the CdS surface while CaF_2 produces a depletion layer.(19) By evaporating a thin CaF_2 layer between the CdS and SiO, the author has shown that the enhancement effect of the SiO on the CdS surface is reduced. As the thickness of the CaF_2 layer is increased, the surface electron concentration is reduced and eventually the surface is completely depleted. Thus, by proper choice of CaF_2 thickness, any surface potential between the limiting potentials of pure SiO_x and CaF_2 is possible. The limiting potential of SiO_x is not fixed in that it depends upon the oxygen pressure and substrate temperature during evaporation.

The energy band structure of a CdS film with equally depleted surfaces is shown in Fig. 5-1. If $|\Phi_s - \Phi_b| >> \frac{KT}{q}$, the surface will be completely depleted of electrons. Φ_s and Φ_b are the surface and bulk potentials respectively measured from the fermi level. One may then analyze the problem with the total exhaustion approximation. In this approximation the free carrier density is zero within a distance d_o from each surface, and has the value n_b in the remainder of the film; provided the film thickness, t, is greater than $2d_o$. For a film of uniform electron concentration ($\Phi_s = \Phi_b$) the conductance per square will be

$$\frac{Gl}{w} = \sigma t, \qquad (5\text{-}1)$$

where G is the film conductance, l is the length of the film, w is the width and σ is the conductivity. The conductance between opposite edges of a square sheet of any size is the same and is called the "conductance per square". If, however, the films are depleted of carriers within a distance d_o from each side, the conductance/square may be expressed by

$$\frac{Gl}{w} = \sigma(t - 2d_o). \qquad (5\text{-}2)$$

Hence, a plot of G versus t yields both the "bulk" conductivity of the film as well as d_o. A negative value of d_o implies that the surface concentration is greater than the bulk concentration.

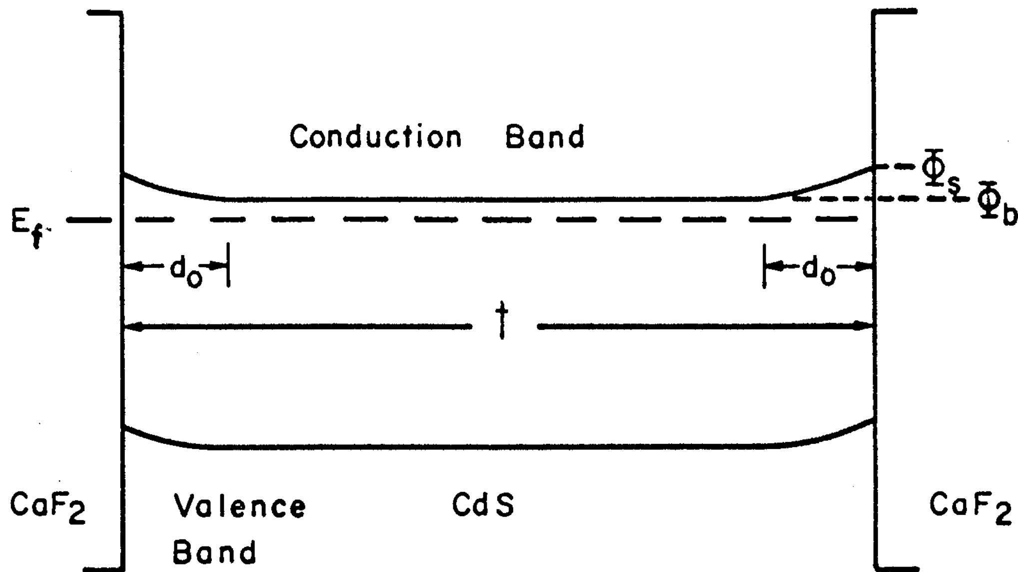


Figure 5-1. Energy Band Structure of a CdS Film With Equally Depleted Surfaces.

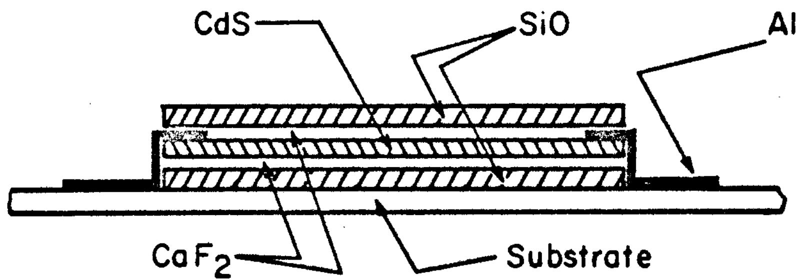


Figure 5-2. Cross-Section of the Evaporated Semiconductor-Insulator Structure.

5.3 Experimental Procedure

To demonstrate the control of the surface potential, CdS films of several thicknesses and with symmetrical surface coatings were evaporated having the geometry shown in Fig. 5-2. In addition to the ohmic contacts shown at the ends of the rectangular film, Hall probes were evaporated at the midpoint. The entire structure was fabricated in one pump-down. Fig. 5-3 shows a photograph of the resulting structures. Each of the samples is 0.22 cm wide and 0.55 cm long. The thickness changes were obtained by successively masking off three samples at a time as the CdS deposition proceeded. The conductances of 3 identical films were then averaged in the interpretation of the data.

5.4 Experimental Results

Fig. 5-4 shows the results of two typical evaporations. One set of films (A) was coated with 2,000 Å of CaF_2 on both sides and has a depletion depth of $d_o = 1{,}050$ Å and an electron concentration of $n_b = 3.7 \times 10^{16}$ cm^{-3}. If it is assumed that there is one free electron for each ionized donor, then the total exhaustion approximation gives a surface potential of $|\Phi_s - \Phi_b| = 0.32$ V. The second set of films (B) was coated with 50 Å of CaF_2 followed by 2,000 Å of SiO_x. The apparent negative depletion layer simply means that the surface conductivity is greater than the bulk conductivity. In such polycrystalline CdS films, the surface mobility may differ from the bulk

mobility, so that Hall measurements on such structures are difficult to interpret.[58]

In Fig. 5-5 the measured dependence of the depletion depth of CaF_2 thickness is shown for films coated with 2,000 Å of SiO_x and various thicknesses of CaF_2 between the CdS and SiO_x. From Fig. 5-5 it may be noted that for CaF_2 thicknesses of order 1,000 Å or larger the effect of the SiO surface states on the CdS is negligible. For thin CaF_2 layers a negative depletion layer or surface excess is observed. Films coated with approximately 150 Å of CaF_2 followed by SiO_x show zero depletion depth which implies that $\Phi_s = \Phi_b$.

The present results indicate that the electrostatic potential at the insulator surface is determined by both surface states and states distributed in the insulation region due to impurities or vacancies. In particular, this study has shown that these states are distributed over (or screened after) a distance of 1,000 to 2,000 Å in the insulating material. Young[59] and Seraphim[60] have shown that the bulk states in SiO_2 are caused by oxygen vacancies. The nature of the states of the CaF_2 - CdS system has not been determined, however some speculation may be made. Surface states from chemisorbed oxygen ions are known to cause a depletion layer on CdS[61]; chemisorbed fluorine ions may behave in a similar manner.

The results indicate a simple and effective method for controlling the surface potential continuously between the values

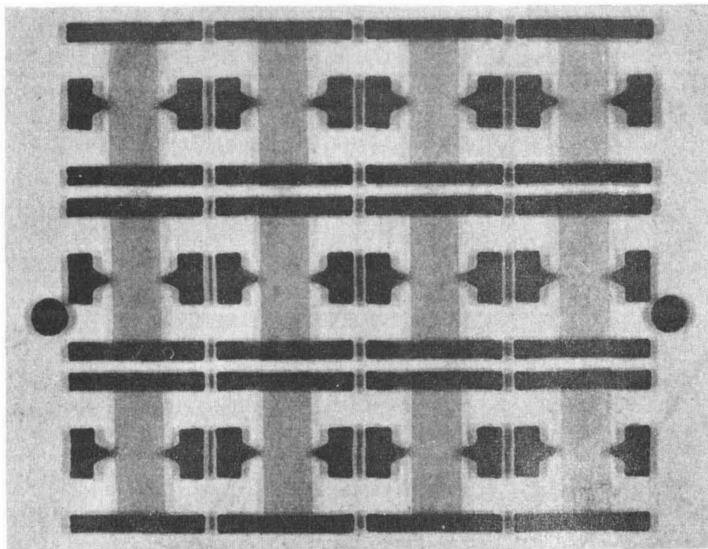


Figure 5-3. The completed resistivity sample showing twelve devices, each containing Hall and resistivity contacts.

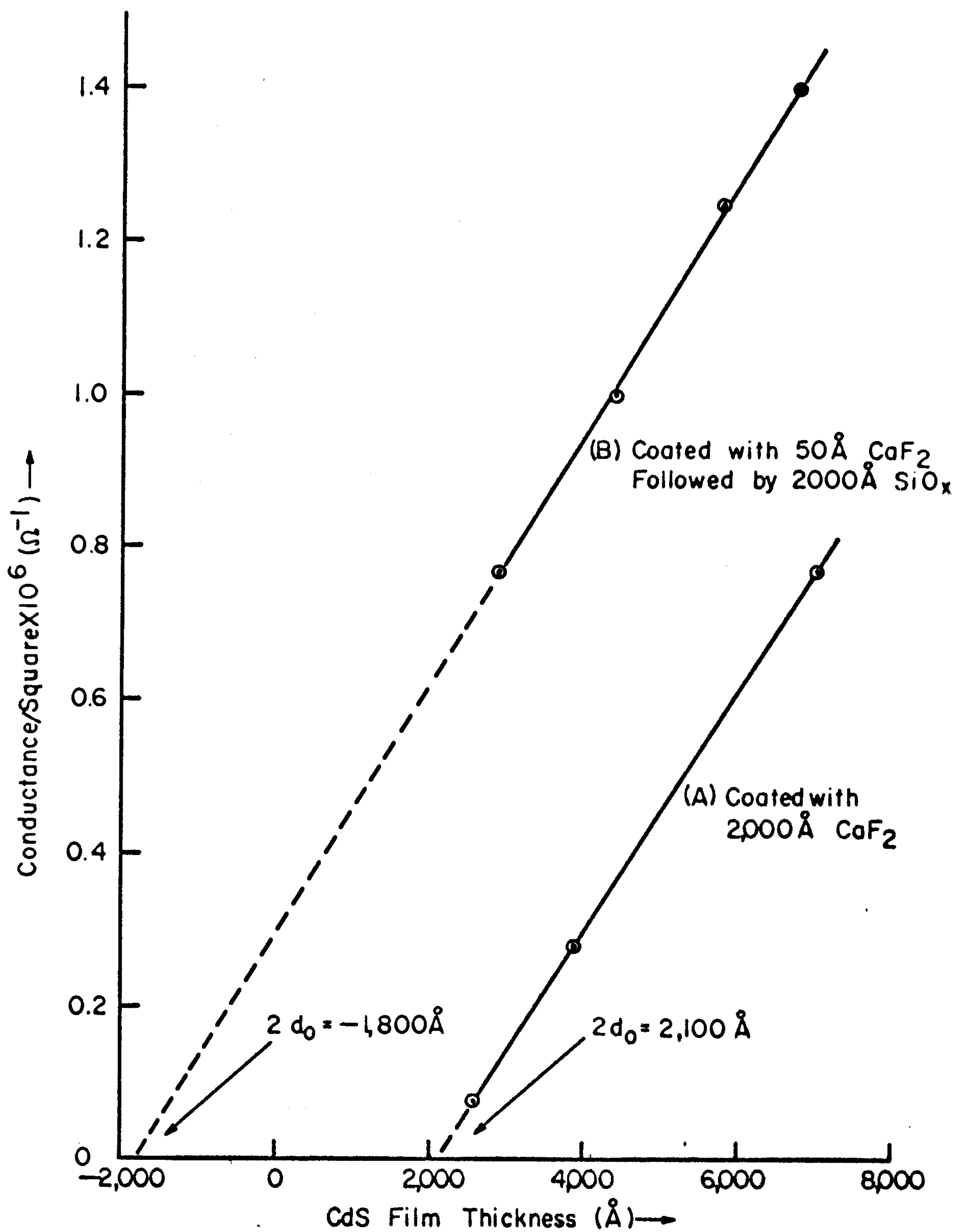


Figure 5-4. Conductance per square for two sets of symmetrically coated CdS films.

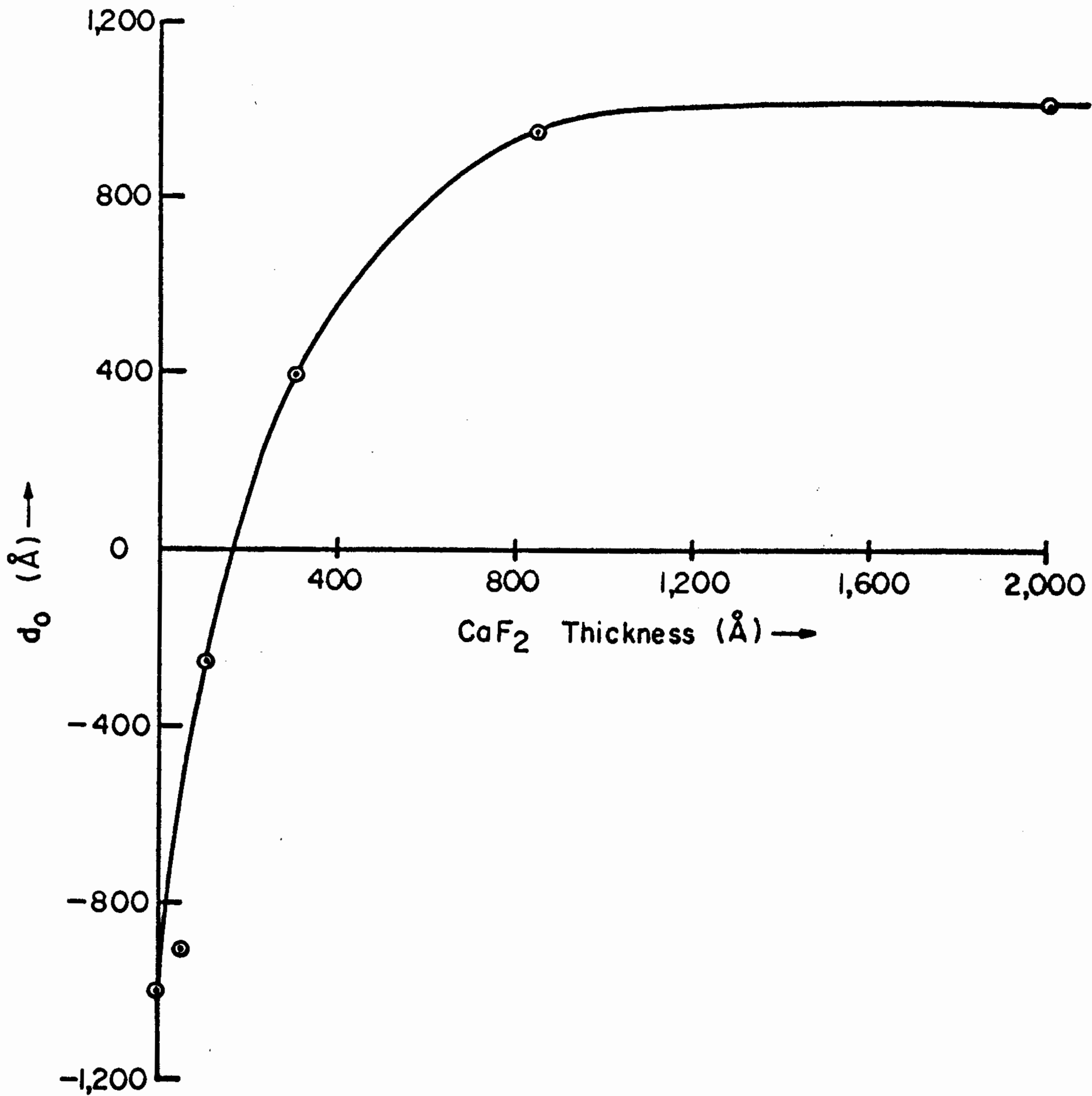


Figure 5-5. Measured depletion depth of CdS coated with CaF_2 followed by 2,000Å of SiO_x.

corresponding to SiO_x and CaF_2 insulation. The possiblity of extending this technique to other semiconductors is discussed in the next section. A summary of the above results has been published[62].

6. CONTROL OF THE SURFACE POTENTIAL OF OTHER SEMICONDUCTORS

6.1 Introduction

The results obtained in the previous section indicate that the evaporated layers of inorganic oxides and fluorides may be used to control the surface potential of CdS films. One may speculate that this technique may also be applicable to other semiconductors. This section describes an application of the results of Section 5 to the control of the surface potential on a lithium-drifted germanium p-i-n diode used as a detector in gamma-ray spectroscopy.

6.2 Application to Lithium-Drifted Germanium Diodes

The sensitivity of exposed surfaces of germanium to ambient conditions and the effects of the surface states on the properties of germanium-lithium p-i-n particle detectors (Ge(Li) diodes) have been studied in some detail.[63-67] Charges trapped in surface states can cause the formation of either n or p-type inversion layers near the surface, and the model proposed by Llacer[68, 69] provides a good explanation of the role of these surface states and resulting inversion layers in determining noise and excess leakage current in p-i-n diodes. As shown in Fig. 6-1, an n-type surface layer extending across the intrinsic region can give rise to a region of high electric field near the i-p boundary. This conduction

layer causes the excess noise.[68, 69]

In the course of Ge(Li) detector fabrication and mounting, and n-type inversion layer may be formed from an etch and water wash, and exposure to room environments.[70, 71] In order to remove this inversion layer chemical dips such as H_2O_2 and HNO_3 are commonly used. These treatments lack control and do not protect the surface from future exposure to room environments.[63]

The results of Section 5 on controlling the surface potential of CdS with evaporated CaF_2 and SiO_X layers suggest that the evaporation of a thin CaF_2 layer on the edges of a Ge(Li) diode may remove the n-type inversion layer. The evaporation of a critical thickness (yet to be determined) of CaF_2 on the four exposed edges of a Ge(Li) diode should therefore restore the surface potential in the intrinsic region to the bulk value, and thus result in a lower surface leakage current, making the diode surface less sensitive to exposure to ambient conditions. The results obtained here should be qualitatively applicable to silicon diodes as well.

6.3 Experimental Procedure

The detector fabrication process used in this work has been presented in some detail elsewhere[72] and thus only the final step in preparing the p-i-n diode will be outlined.

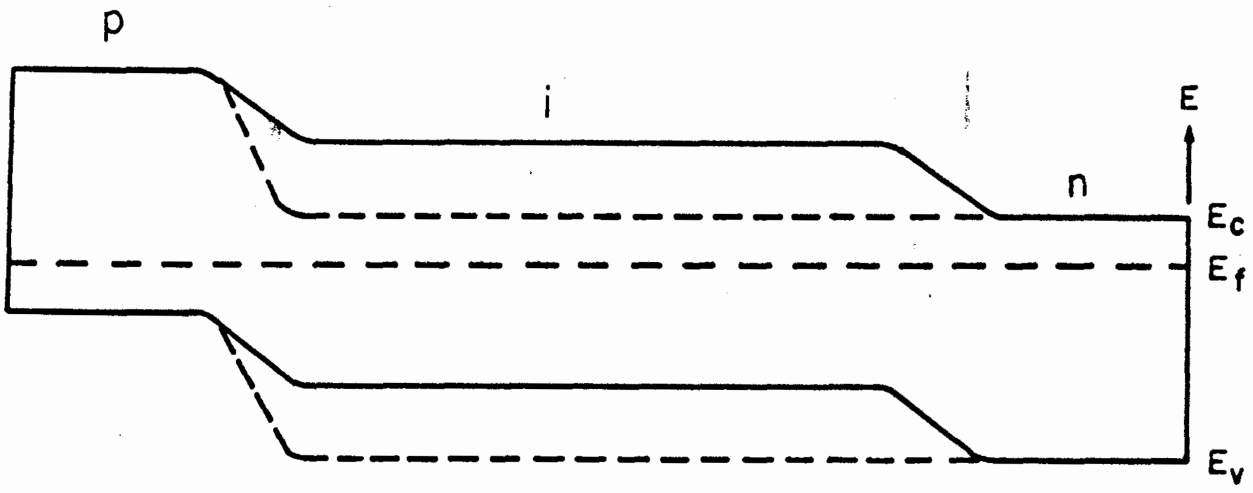


Figure 6-1. Energy band diagram of p-i-n diode. Solid lines show position of energy bands in the bulk material while dotted lines show energy bands on an n-type surface.

After a long lithium drift in an electric field at room temperature, a two-stage etch consisting of 3 minutes in a 2:1 volume mixture of HNO_3 and HF and 15 seconds in a 5:1 mixture is carried out followed by washing in deionized, distilled water and drying in nitrogen gas. After mounting in the cryostat and reducing the pressure to 10^{-6} Torr, the diode is cooled to -72°C and a reverse bias of 500 - 1,000 V is applied until no further leakage current reduction is noted; typically the time required is 72 to 96 hours. The diode is then cooled to 77°K, its reverse leakage measured, and test spectra run.

The diode is then brought to room temperature over a period of several hours under vacuum, transferred to the evaporator and coated with CaF_2. The cooling procedure is then repeated with a shorter cleanup drift at -72°C, and the reverse leakage and test spectra remeasured. All test spectra were taken on the 662 KeV gamma ray of Cs^{137}.

6.4 Results

Fig. 6-2 shows the resulting reverse bias characteristics at 77°K for four diodes coated with various amounts of CaF_2 on their etched surfaces. In 6-2 (a) it is seen that 50 Å of CaF_2 gave no measurable difference in reverse characteristic; the 7KeV resolution of the 662 KeV gamma ray of Cs^{137} at -90 volts bias was also unchanged. In 6-2 (b) it is seen that 150 Å of CaF_2 gave a significant reduction in the reverse leakage current. Fig. 6-3 shows that its resolution improved from 5.04 KeV to 4.1 KeV at the same bias. The actual increase in resolution

is greater than the apparent increase observed in Fig. 6-3 because of the pre-amplifier noise. When the spectrum in Fig. 6-3 (after coating) was retaken using a low-noise field-effect transistor pre-amplifier, the resolution was found to be 2.37 KeV (Fig. 6-4). Fig. 6-2 (c) shows the improvement in bias characteristic for a 200 Å CaF_2 film. At -50 V bias the resolution was improved from 15 KeV to 8 KeV. Finally, Fig. 6-2 (d) shows the results of a 2,000 Å coating. Apparently a strong p-type inversion layer now exists at the surface; the resulting diode is unusable as a detector.

6.5 Conclusion

These results indicate that CaF_2 coatings alter the surface potential of germanium significantly; in particular, 150-200 Å of CaF_2 may provide enough "surface states" to compensate the states produced by the etch procedure and thus leave the surface potential of this germanium approximately equal to the bulk potential.

It is also likely that CaF_2 is only one of a class of inorganic, oxygen-free insulators (e.g. MgF_2) which will have the same effect on certain semiconductors. Moreover, such coatings should be rugged and provide some protection against absorption of water vapor. A summary of these results has been published.[73]

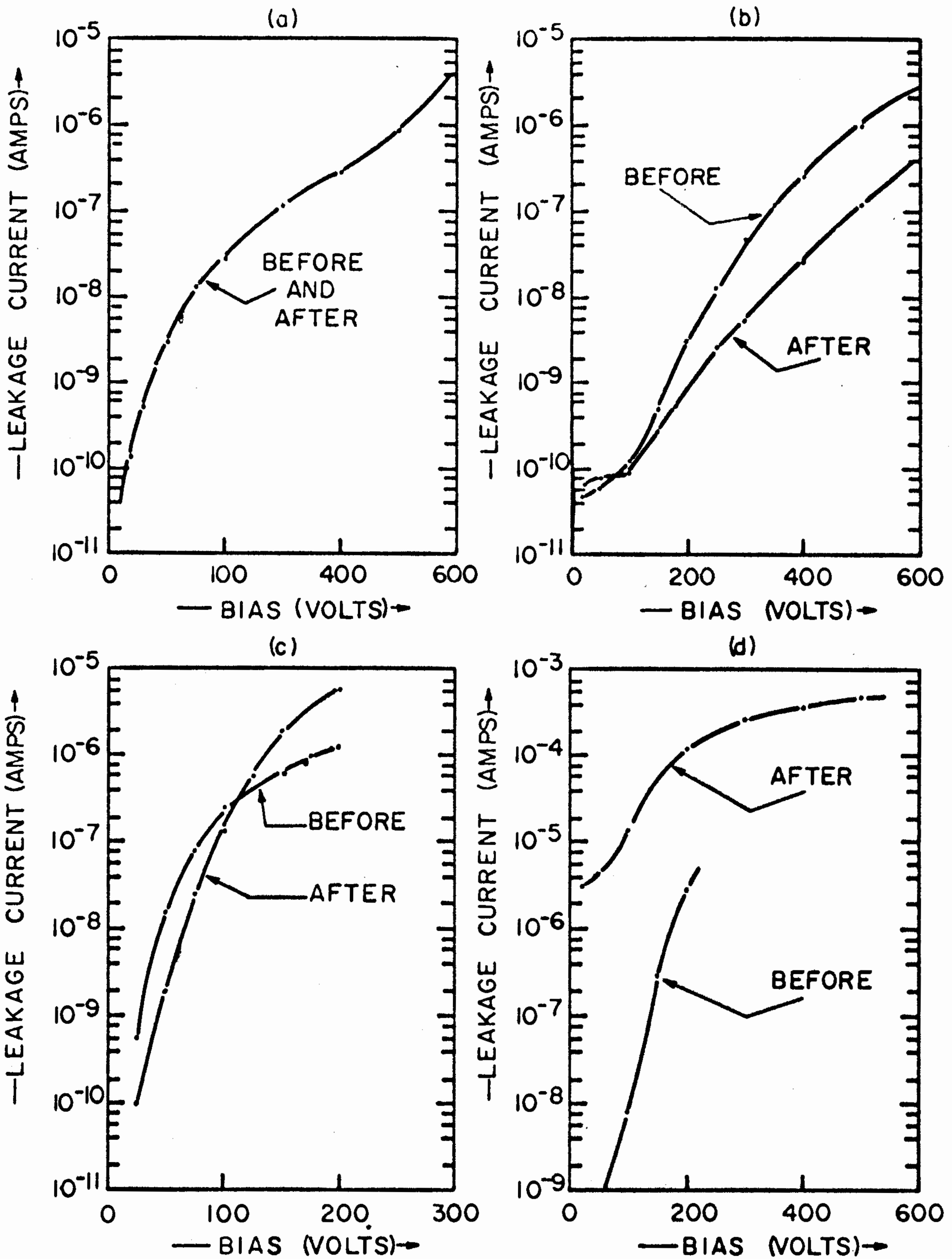
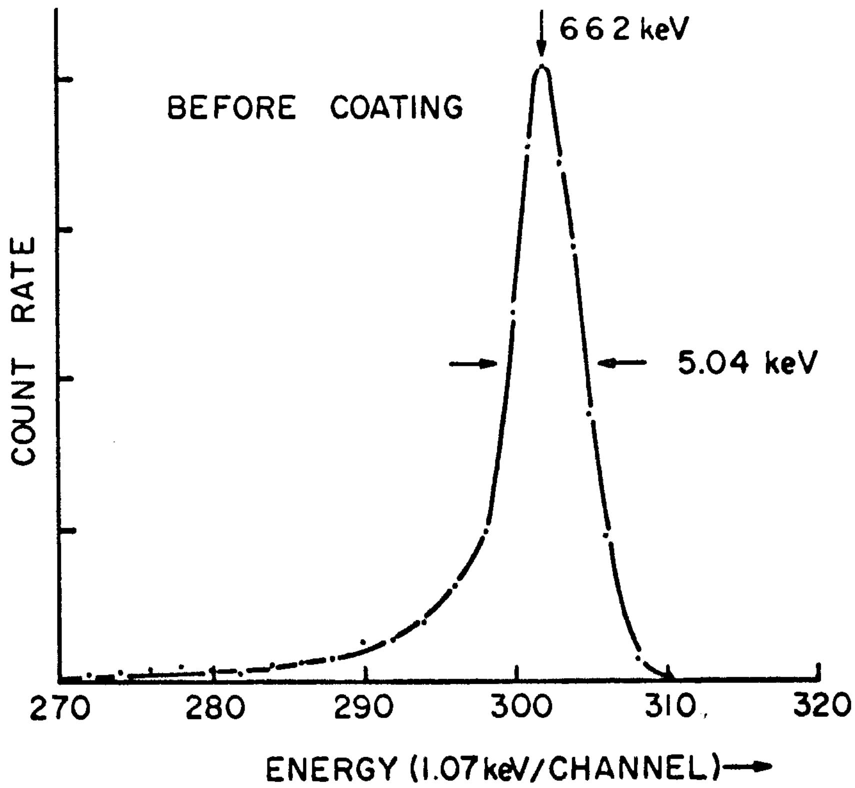


Figure 6-2. Effects of CaF_2 evaporation on edges of Ge (Li) detectors (a) 50Å, (b) 150Å, (c) 200Å, (d) 2,000Å.



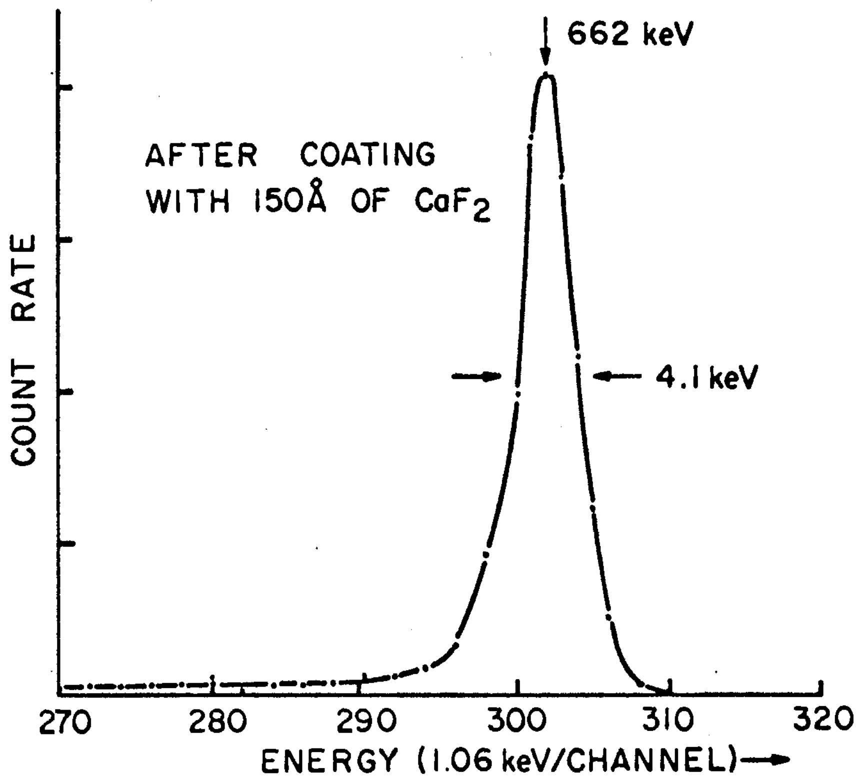


Figure 6-3. Spectrum of C_s^{137} Gamma Ray Taken with Ge(Li) Diode before and after Coating with 150Å of CaF_2.

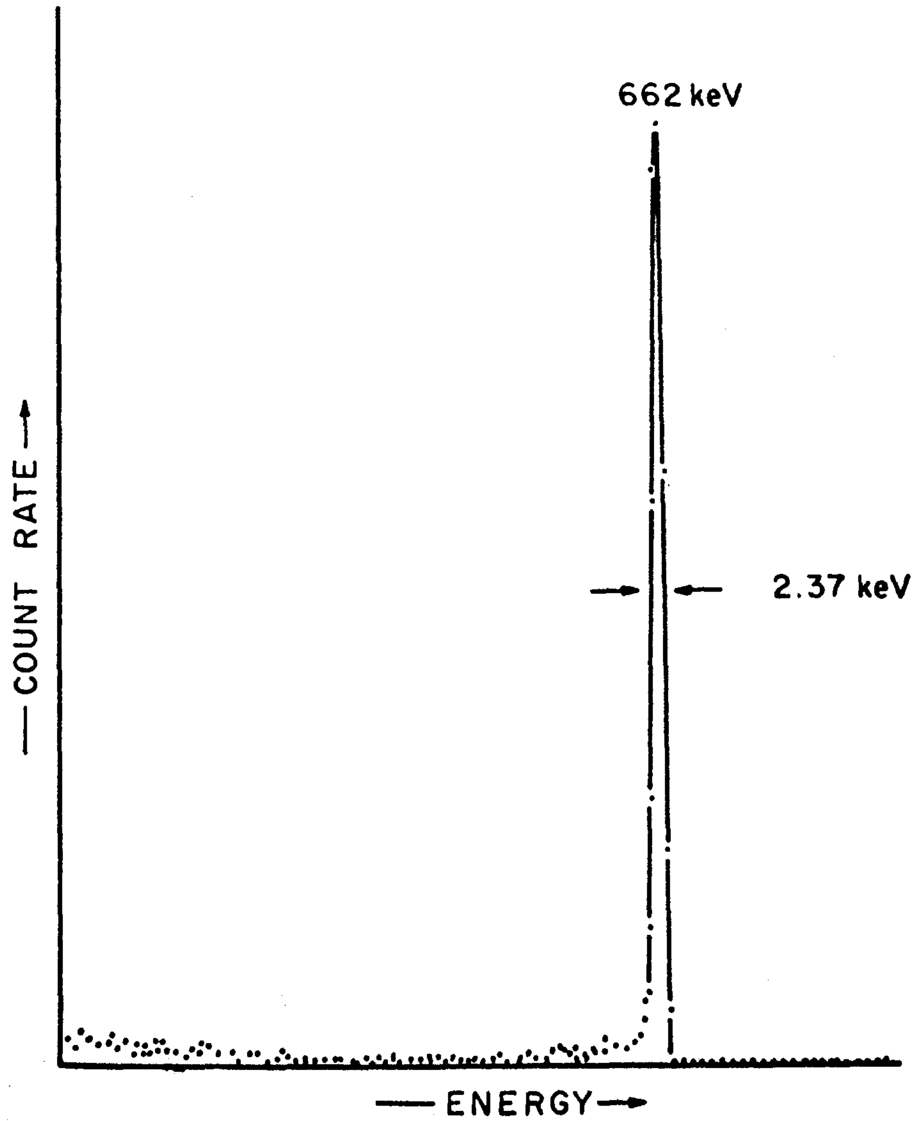


Figure 6-4. Cs^{137} Gamma Ray Detected with Ge(Li) Diode Coated with 150Å CaF_2 Followed by FET Preamp.

7. THE HIGH VOLTAGE THIN-FILM TRANSISTOR

7.1 Introduction

The results of Section 5 may be applied to the thin-film transistor where control of the surface potential is necessary to predict the device characteristics. This section describes the design of a new thin-film transistor capable of withstanding over 300 V. This transistor will switch a current of 100μa with a control voltage of 50 V. The new device, which we shall refer to as a high voltage thin-film transistor, is basically an extension of the thin-film transistor originally proposed by Weimer(7) .

Conventional TFT's have source-drain breakdown voltages of approximately 20 V. The increased operating range is achieved through careful control of the surface potential of the active layer and through appropriate changes in the device geometry and material constants.

The geometry and material constants of a TFT with the necessary characteristics have been calculated using the gradual approximation and verified by the theory of Geurst(23). The following subsections discuss the modifications required to achieve high voltage operation, and describe the device fabrication.

7.2 Design Considerations for the High Voltage TFT

The static characteristics of a typical low voltage TFT are sketched in Fig. 2-2. Several characteristics of the conventional TFT should be reviewed here. The static source-drain characteristics tend to saturate, but the saturation slopes are ~ 10KΩ (i.e. saturation is not perfect). Also note that the impedance corresponding to $V_G = 0$ is comparable in magnitude to the saturation impedance. The source-drain curves in Fig. 2-2 cannot be extended to arbitrarily large source-drain voltages. In typical units either the CdS or the gate insulation will break down at source-drain voltages exceeding 15 - 20 V.

As discussed in Section 2.2 the idealized theory predicts the following dependence of the source-drain current, I_D, on gate voltage, V_G, and source-drain voltage, V_D.

$$I_D = \frac{\mu C}{L^2} \{(V_G - V_o) V_D - \frac{V^2_D}{2}\} \quad \text{if } V_D < (V_G - V_o) \text{ and } V_G > V_o \qquad (7\text{-}1)$$

Equation (7-1) is valid only up to the "knee" of the curves in Fig. 2-2. This knee occurs when $V_D = (V_G - V_o)$. For larger source-drain voltages the idealized model predicts perfect saturation, so that:

$$I_D = \frac{\mu C}{2L^2} (V_G - V_o)^2 \quad \text{if } V_D > (V_G - V_o) \text{ and } V_G > V_o \qquad (7\text{-}2)$$

Desirable characteristics of a high voltage TFT would be pentode-like characteristics with a saturated source-drain current of ~ 5μa with no applied gate voltage, and a source-drain current of ~ 100μa with a gate voltage of, say, 20 V. In addition, the device should be able to withstand source-drain voltages of ~ 300 V. Thus, the mode of operation envisaged for the high voltage TFT implies operation in the extreme saturation region (gate voltage << source-drain voltage).

Three basic changes in the conventional TFT are required to fabricate a high voltage device with the desired characteristics.

(1) The source-drain gap must be increased so that the active layer will not break down when potentials of several hundred volts are applied between the source and the drain.

(2) The gate insulation thickness must be increased in order to withstand voltages of several hundred volts, since the source-drain voltage effectively also appears between drain and gate.

(3) The impedance of the device corresponding to $V_G = 0$ V must be increased from a typical value of 10KΩ to a value high compared with the impedance of a typical load. For example, an electroluminescent cell has an impedance of 10 to 100 MΩ. Part of this increase in impedance will

be obtained automatically because of the wider source-drain gap, if the lateral dimension is kept constant.

An estimate of the source-drain gap may be made by noting that conventional units with a source-drain gap of 7.5×10^{-4} cm. are able to withstand a source-drain voltage of 15 to 20 V before breaking down. If we make the reasonable assumption that breakdown occurs at a critical field (not at a critical voltage) this implies a gap of 2×10^{-2} cm. for source-drain voltages of 400 V. Hence the modified TFT requires a source-drain gap which is about 25 times larger than that of conventional units. In a similar manner the gate insulation thickness may be calculated. The breakdown field strength of this insulation is about 4×10^6 V/cm. Thus, a gate insulation thickness of 10,000 Å will withstand 400 V.

Assuming that the lateral width of the modified TFT is the same as that of conventional units (approximately 2 mm) the 1,000 to 10,000 fold increase in the required device impedance will require an increase in the layer resistivity by a factor of 40 to 400. Since conventional TFT's use active layers with $\rho \simeq 10 \rightarrow 100\Omega$-cm, the modified TFT's will require an effective resistivity of $10^3 \rightarrow 10^5\Omega$-cm.

These changes in the device geometry will have a profound effect on the device performance. Values of important parameters such as on current, off current, voltage gain, and the gain-bandwidth product may easily be calculated from the geometrical changes. For example, the expression for the gain-bandwidth

product is[7]

$$GBP \sim \frac{1}{2\pi} \frac{\mu(V_G - V_o)}{L^2} . \tag{7-3}$$

However, $L_{new} = 25L$, and assuming $(V_g - V_o)_{new} = 10\ (V_g - V_o)$, the new GBP will be

$$GBP_{new} \rightarrow GBP \frac{10}{(25)^2} . \tag{7-4}$$

Since conventional units have a GBP $\approx 10^7$, this implies that the high voltage TFT will have a GBP $\approx 10^5$. For the expected voltage gain ($\approx$10) this implies a switching time of 0.2 msec.

It is of interest to examine the relative surface state densities of the two structures. In Section 2.2 the total number of traps or electrons, N_o, in the channel at zero gate potential was expressed as

$$V_o = \frac{qN_o}{C_G} = \frac{qn_o}{\epsilon/h} = \frac{qn_o h}{\epsilon} \tag{7-5}$$

where n_o is the surface density. In the conventional TFT, values of $V_o \approx 5$ V are obtained; values of $V_o = 5 \rightarrow 15$ V are acceptable for the high voltage device. Thus the density of surface traps must be 3 - 10 times smaller than acceptable in conventional units. This implies a density equal to the

smallest obtained in conventional structures ($\approx 3 \times 10^{11}/cm^2$).

The above considerations of the device design are based on what seem like reasonable assumptions. At this point one may use the theory of the insulated gate field effect transistor by Geurst[23] to verify the above assumptions and conclusions about the static device characteristics. In his model, Geurst assumes the thickness of the semiconducting channel to be infinitely small compared to the thickness of the insulating layer. In these devices the gate insulation is 10,000 Å, and thus is large compared to the active material thickness of ~ 1,500 Å. It therefore seems reasonable to analyze this structure in terms of Geurst's model.

This analysis has been carried out assuming a ratio of insulator thickness to source-drain spacing of 1/250 and a carrier mobility of 10 cm^2/V-sec. To obtain the required zero gate bias characteristic ($I_D = 5\mu a$, $V_D = 300V$) the model predicts a surface carrier density of 3×10^{11} electrons/cm^2. (Note that it is not possible from this surface carrier density to calculate the material resistivity explicitly because Geurst has assumed an infinitely thin or two-dimensional semiconducting layer. Thus, the original assumption regarding the active layer resistivity must be checked experimentally.) To obtain the desired source-drain current of ~ 100μa at saturation the model predicts a gate voltage of 17 V. The value of gate

voltage required to produce this current will depend upon the free-carrier mobility. For example, if the mobility is assumed to be 1 cm^2/V-sec., a gate voltage of 60 V is required to produce the same current.

Fig. 7-1 illustrates the static electrical characteristics of this structure as calculated from Geurst's model. Note that complete saturation is predicted. This is consistent with the model which shows that the amount of saturation expected is related in a non-linear manner to the ratio of insulator thickness to source-drain spacing as well as the free carrier mobility and initial density of surface charges.

In Table 7-1 the dimensions of the high voltage TFT are summarized and compared to the conventional TFT.

	High Voltage TFT	Conventional TFT
Active Material	CdS	CdS
Active Material Thickness	~1,500 Å	~2,000 Å
Source-Drain Gap	0.025 cm	7.5×10^{-4} cm
Insulation Thickness	10,000 Å	1,000 Å
Electrode Width	0.2 cm	0.2 cm

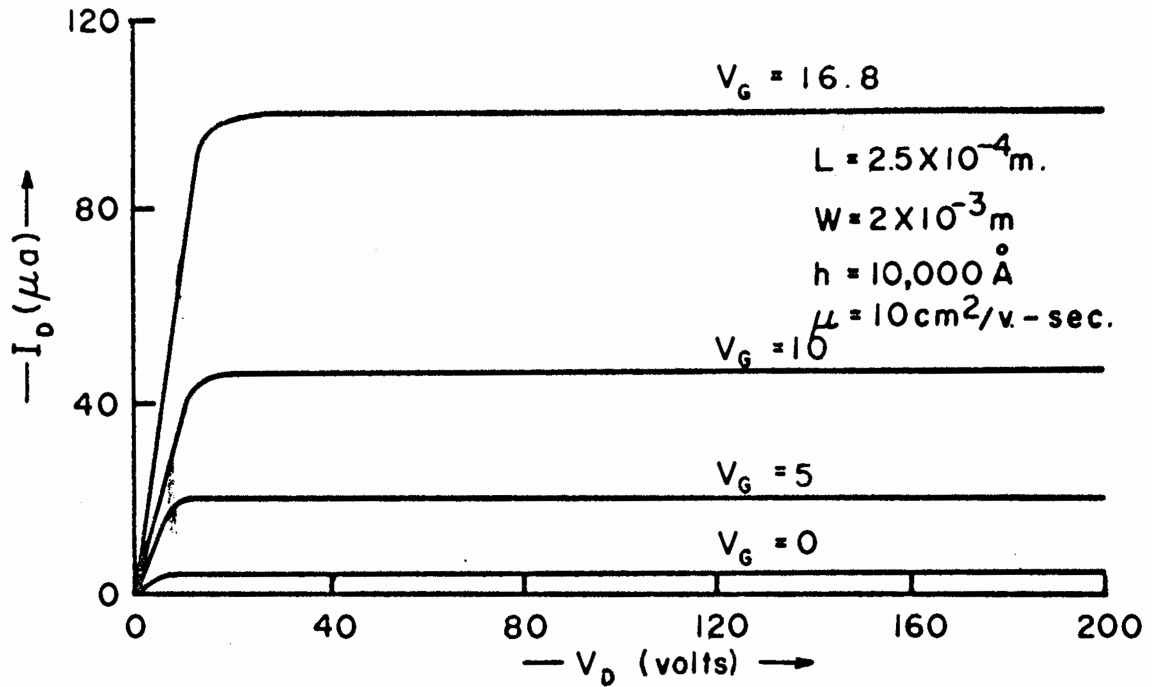
Table 7-1. Dimensions of the High Voltage and Conventional TFT.

7.3 Device Fabrication

Fig. 7-2 illustrates two forms of the high voltage TFT constructed with the dimensions given in Table 7-1. The geometry illustrated in Fig. 7-2 (a) is simpler to construct

than that illustrated in Fig. 7-2(b), but it has two disadvantages. The first one is that the CdS characteristics may be unpredictably altered by the high substrate temperature required for the ensuing insulation evaporation; and since CdS vapor diffuses during evaporation, all other sources in the system which are to be subsequently used may be contaminated with CdS. The form of the high voltage TFT illustrated in Fig. 7-2 (b) surmounts these difficulties by evaporating the insulation layer first. Two source-drain electrodes have been made in this form -- above and below the CdS. Weimer[18] has reported that aluminum electrodes evaporated under CdS do not make good ohmic contacts, however, electrodes evaporated above the CdS are unsatisfactory because of solid state electrolysis effects. The high fields existing between the gate and drain electrodes cause oxygen ions in the insulation to migrate to the drain electrode with the result that a blocking contact is formed at the semiconductor-drain interface. By placing a source-drain electrode above and below the CdS, mobile ions may be screened from the semiconductor-drain interface and good ohmic contact assured.

This more complicated structure means that three high quality aluminum layers must be fabricated in one pump down - a feat that cannot be done from a simple Mo, Ta, or W coil because of source contamination. Thus, a more sophisticated aluminum source such as a boron nitride crucible, or an electron beam heater must be used.



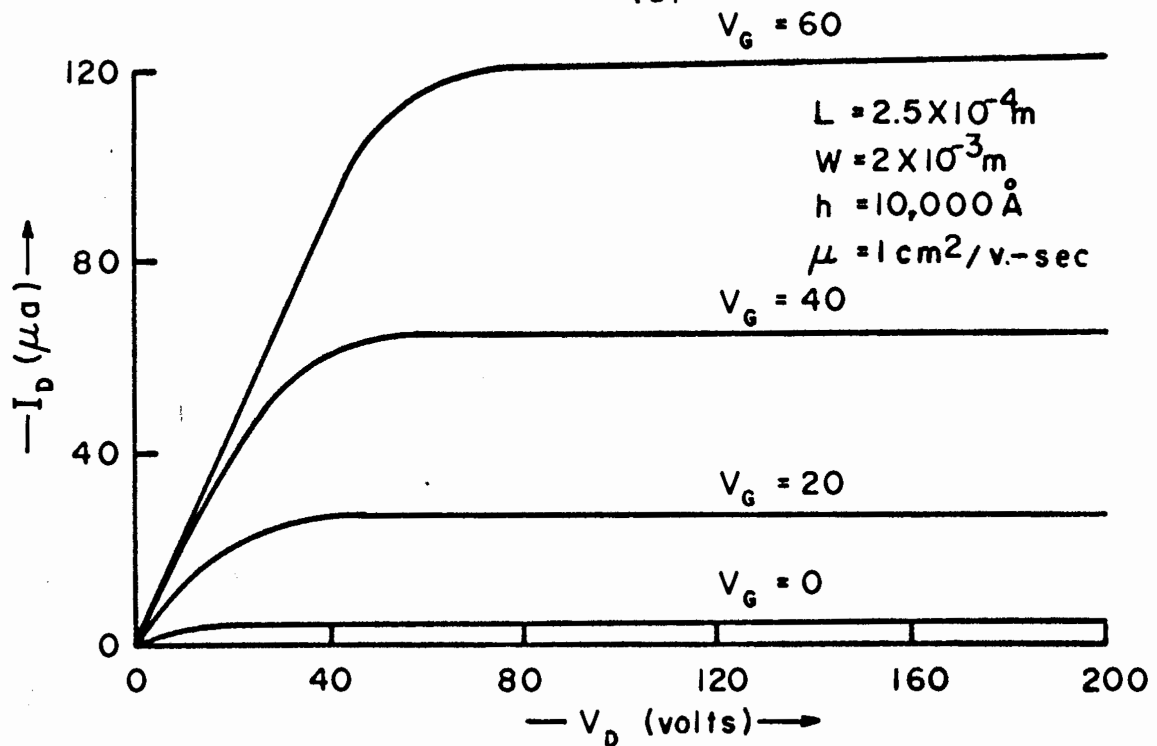
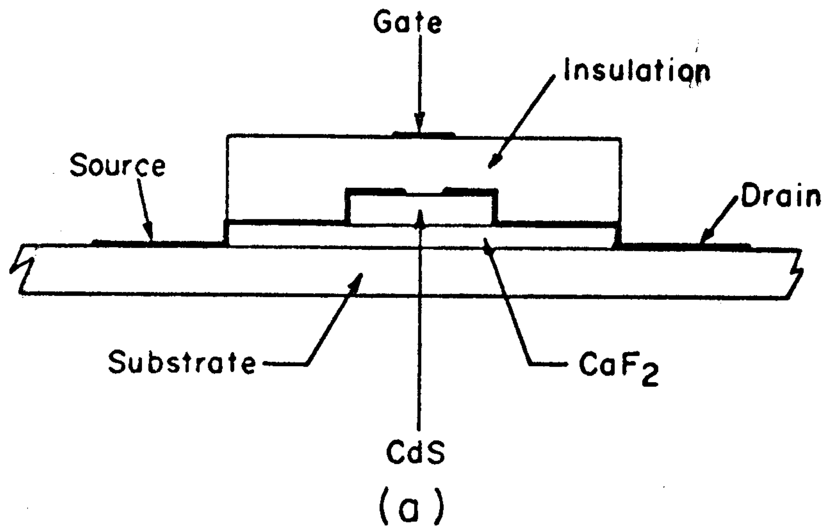


Figure 7-1. Calculated Static Characteristics of the High Voltage TFT (a) μ = 10 cm^2/v.sec. (b) μ = 1 cm^2/v.sec.



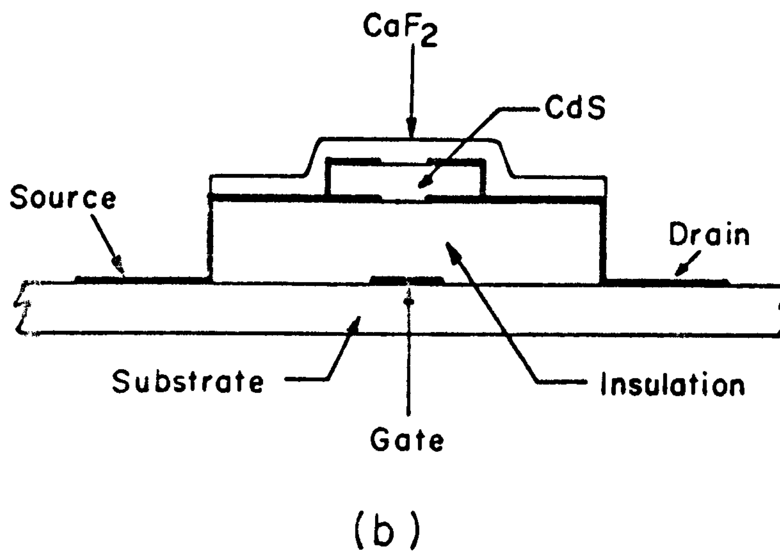


Figure 7-2. Geometry of the High Voltage TFT.

The devices constructed with SiO_x insulation were not satisfactory because the zero bias drain current at $V_D = 200$ V was ~ 500μa. Devices constructed with CaF_2 insulation were also unsatisfactory because the drain current under similar conditions was < 1μa with little gate control observable. The SiO_x insulation produces an enhancement layer (excess surface conductivity) on CdS. The degree of enhancement depends critically on the oxygen pressure and the substrate temperature during the SiO_x evaporation. CaF_2 produces acceptor-like surface states at the CdS interface which cause the CdS to be depleted of free carriers near the surface. For the applications envisaged these insulators produced devices which were too enhanced or too depleted of surface carriers.

In Section 5 it was demonstrated that a thin CaF_2 layer evaporated between the CdS and SiO_x reduced the enhancement effect of the SiO_x on the CdS surface. As the thickness of the CaF_2 layer is increased, the surface becomes completely depleted. In particular, it was shown for the films deposited in this laboratory that ~ 150 Å of CaF_2 evaporated adjacent to the CdS followed by an SiO_x layer > 2,000 Å resulted in an approximately flat band structure (Φ surface = Φ bulk). For this device the CaF_2 film was placed adjacent to 10,000 Å of SiO_x.

In addition to adjusting the potential of the front CdS surface to the desired value, one must consider the shunting

effect of a leakage current along opposite surface of the CdS (the surface opposite to the gate electrode). This current may be eliminated easily by evaporating a film of CaF_2 over this surface. The effect of CaF_2 on the depletion depth in evaporated CdS films has been measured as a function of thickness, and it has been shown that 1,000 Å of CaF_2 will deplete the CdS of free carriers to a depth of 1,000 Å. The shift in the surface potential in this case is about 0.3 eV.

Fig. 7-3 illustrates the energy band diagram and electron concentration of the CdS in a typical structure. With these insulation techniques, devices with acceptable static characteristics have been produced and will be discussed in the next section. This device is particularly suited as a transistor controlled switch for applications involving high impedance loads, such as the electroluminescent lamp (EL lamp) described in Appendix D.

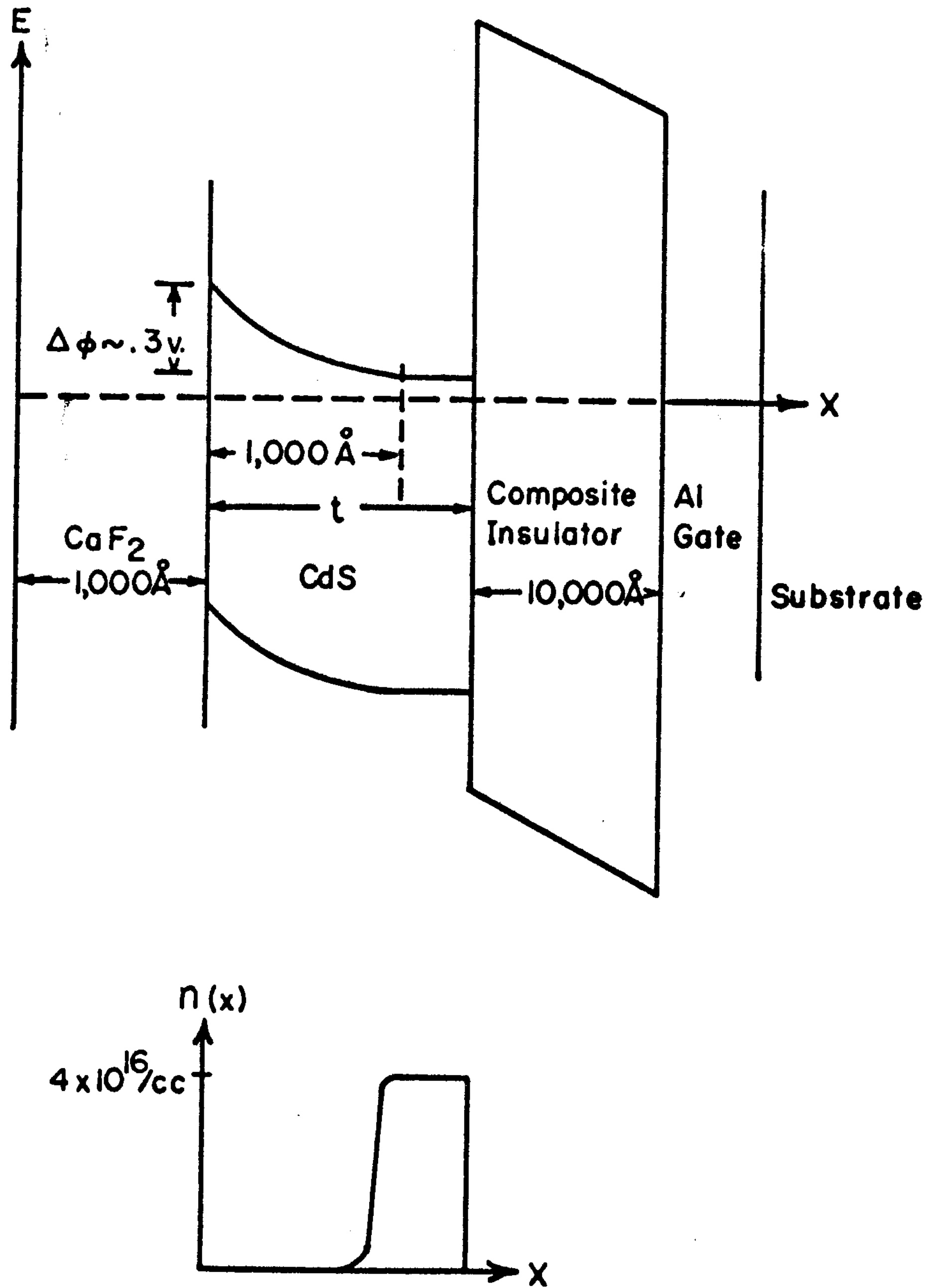
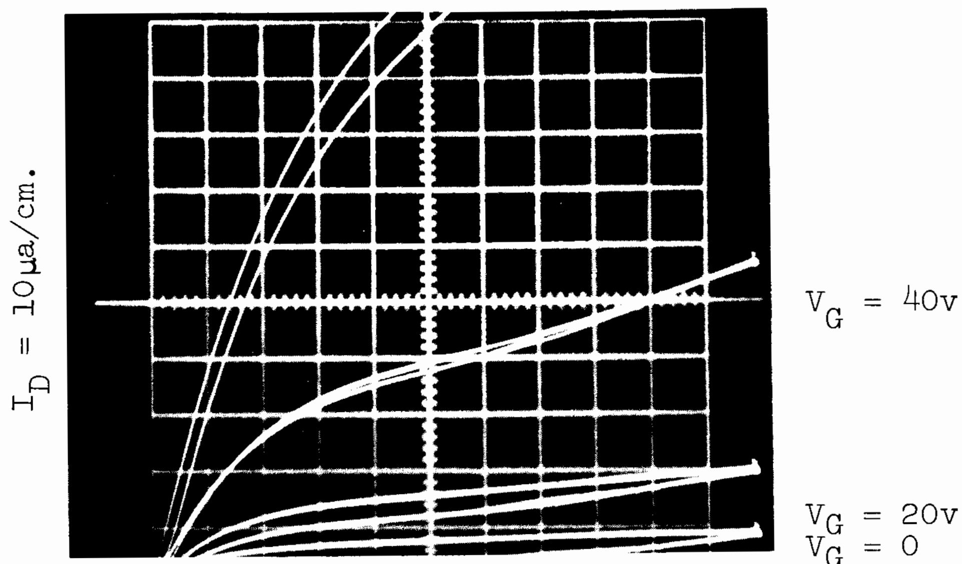


Figure 7-3. Energy-band structure of and electron concentration in the High Voltage TFT. Drawing not to scale.

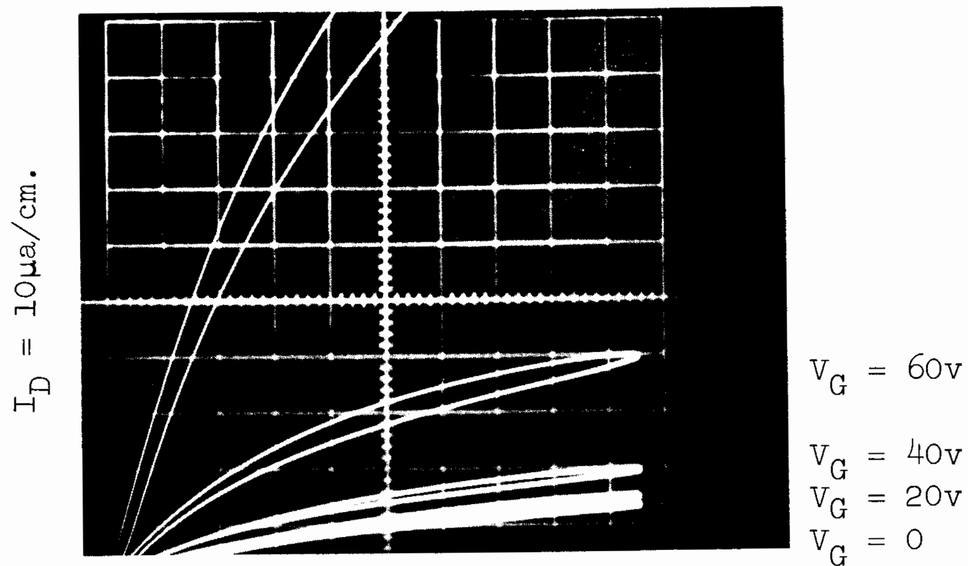
8. THE HIGH VOLTAGE TFT -- EXPERIMENTAL RESULTS

8.1 Device I-V Characteristics

Plots of the drain current vs. drain voltage for various values of positive gate bias for two devices constructed with the geometry given in Table 7-1 are shown in Fig's. 8-1 and 8-2. The characteristics displayed in Fig. 8-1 were taken with a Tektronix type 575 curve tracer where the source-drain voltage was swept at a rate of 120 cps; a constant gate voltage was supplied by an external source. The lower trace of the hysteresis loop is for increasing gate voltage. The drain voltage is limited by the curve tracer to a maximum value of 200 V. A curve tracer with a limiting voltage of 350 V was constructed to demonstrate the extremely high voltage capability of these devices. A typical result is shown in Fig. 8-10. The I-V characteristics displayed in Fig. 8-2 were taken on an X-Y recorder and are thus "static" characteristics. The insulation layer in these devices consisted of 150 Å of CaF_2 adjacent to the substrate and followed, in most cases, by 8,000 Å of SiO and 2,000 Å of GeO_2. The following subsections describe the performance characteristics of the high voltage TFT and its ability to operate as a switch for an electroluminescent lamp. In order to illustrate the various physical mechanisms which are relevant, we purposely display TFT's with a wide range of characteristics -- including effects which are detrimental to device operation.

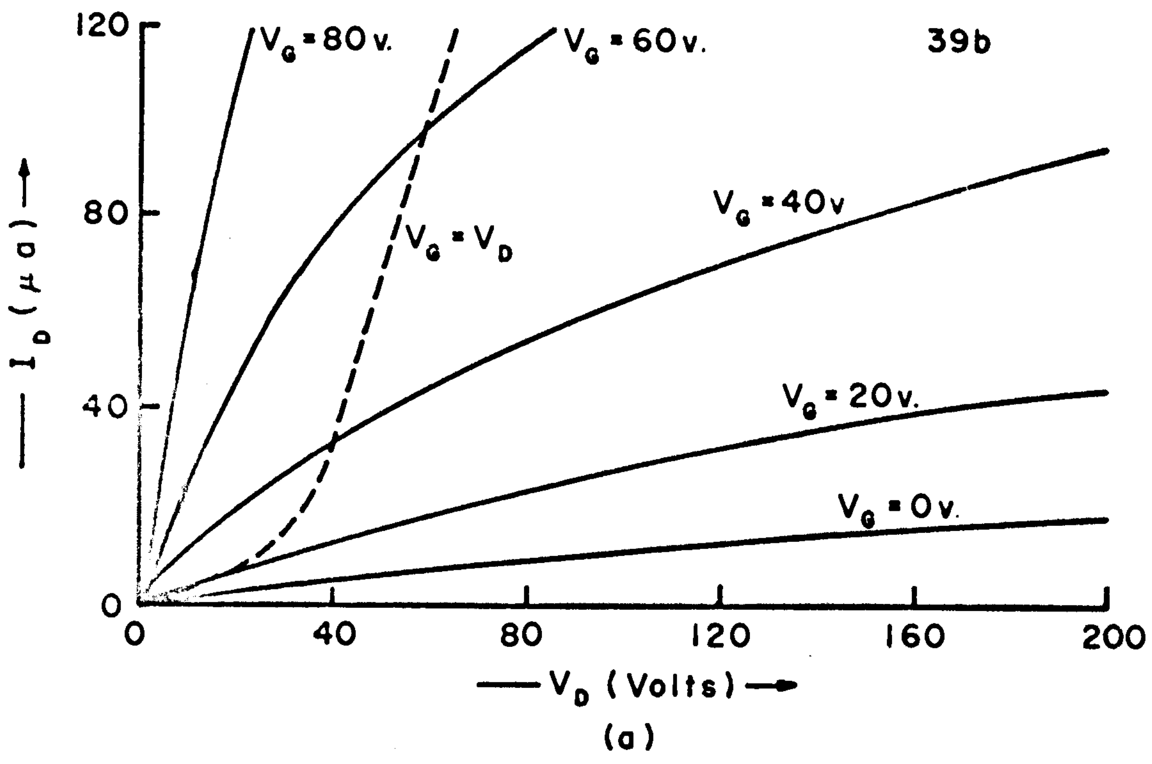


(a)



(b)

Figure 8-1. Dark Characteristics of two TFT's as Displayed on the Tektronix 575 Curve Tracer.



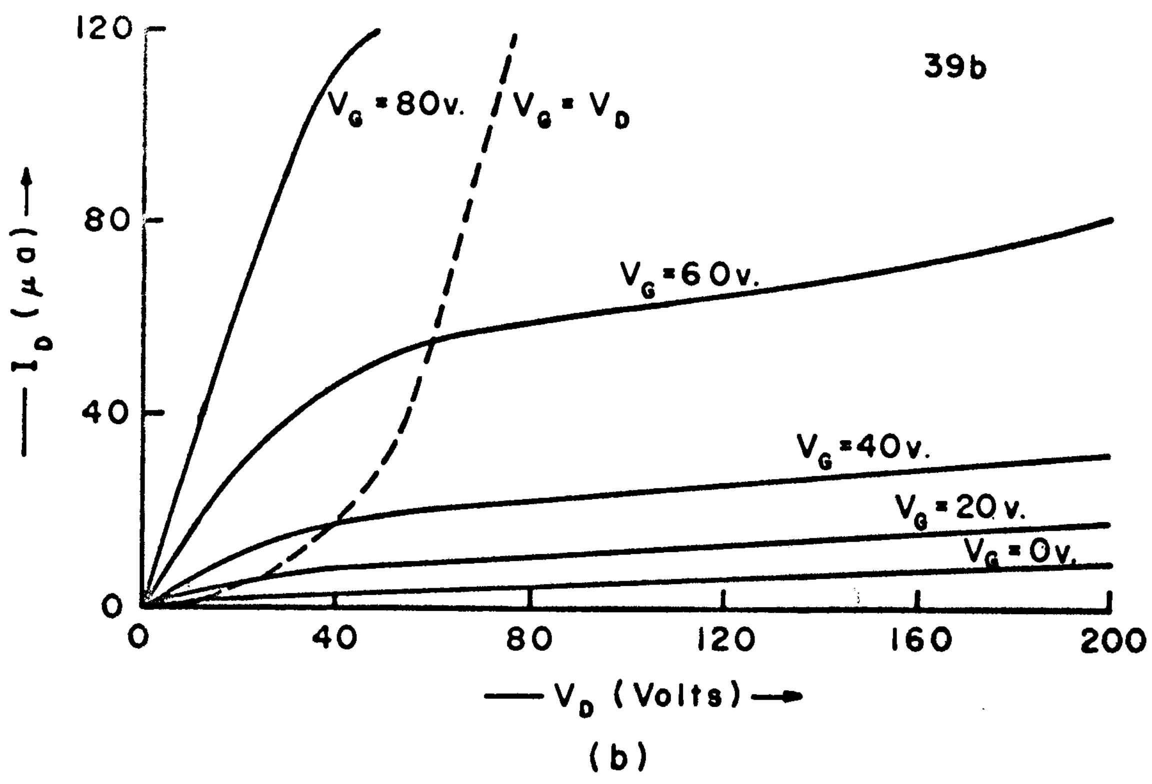


Figure 8-2. TFT Static Dark Characteristic in (a) Dry N_2; (b) Room Humidity.

8.2 Transconductance and Mobility

From Section 2.5 the relation between mobility and transconductance is seen to be

$$\frac{g_m}{\mu} = \frac{C_G V_D}{L^2} \text{ for } V_D \leq (V_G - V_o) \qquad (8\text{-}1)$$

$$(V_G - V_o) > 0$$

$$\frac{g_m}{\mu} = \frac{C_G}{L^2}(V_G - V_o) \quad \text{for} \quad V_D \geq (V_G - V_o) \qquad (8\text{-}2)$$

$$(V_G - V_o) > 0$$

One obvious requirement for high transconductance is high mobility.

The mobility of the CdS is in turn a function of the deposition conditions. It was noted in Section 4.4 that the mobility increases with substrate temperature, but at temperatures in excess of 120°C little CdS condensed on the substrate. The CdS films studied here were evaporated at substrate temperatures of 100 - 115°C, with a small improvement noted at the higher temperature. By use of equation (8-1) the effective mobility of several TFT's was determined and is presented in Table 8-1.

Unit	V_D	V_G	μ_{eff}
39b	33V	50V	1.5 cm^2/V-sec.
53d	33	70	1.75
54a	33	130	1.5
30b	33	17.5	12

Table 8-1. Measured Effective Mobility in Several TFT's

The field effect mobility is also dependent upon the gate potential. For increasing positive gate bias, trapping states near the insulator-semiconductor interface and between crystallites are being filled causing a reduction in electron scattering, and an increase in mobility.

For the extreme saturation region, equation (8-2) predicts that g_m will be linearly proportional to V_G for $(V_G - V_o) > 0$ and will be zero for $(V_G - V_o) < 0$. Since a positive value of V_o implies unfilled surface states, this is another way of saying V_o is the minimum value of gate voltage which has an effect on the drain current. Fig. 8-3 shows the transconductance vs. gate voltage for 3 devices. Unit 30b, whose I-V characteristics are shown in Fig. 8-4 along with those of unit 30C, had one of the highest transconductances and lowest values of V_o measured. Unfortunately, due to insulation breakdown, the drain voltage could not be increased beyond 80V. The S-shape of the I-V characteristics of Unit 30c is indicative of rectifying contacts as explained in Section 8.7. Unit 54a, whose I-V characteristics are shown in Fig. 8-6, showed a higher value of $V_o \sim 100V$. Unit 39b has an acceptable value of V_o, but a low mobility. These large variations in V_o are due in part to

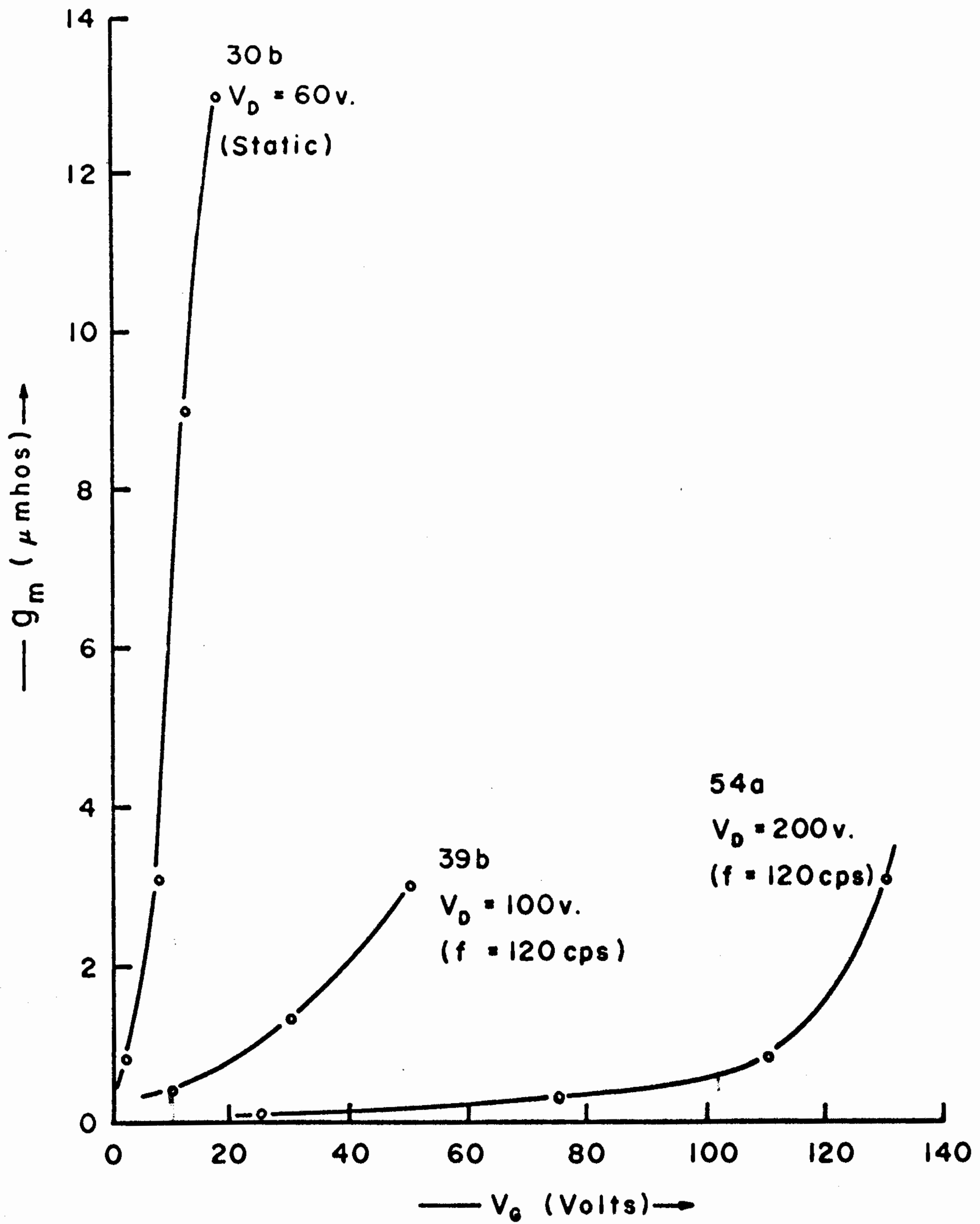
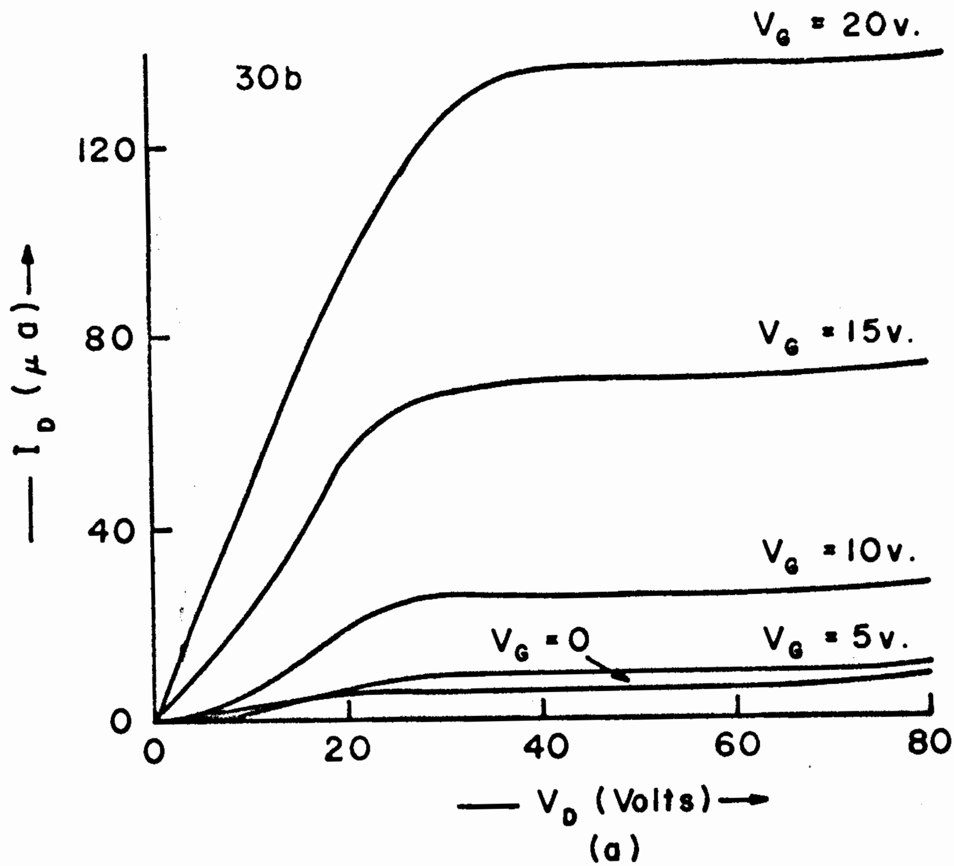


Figure 8-3. TFT Transconductance *vs.* Gate Voltage.



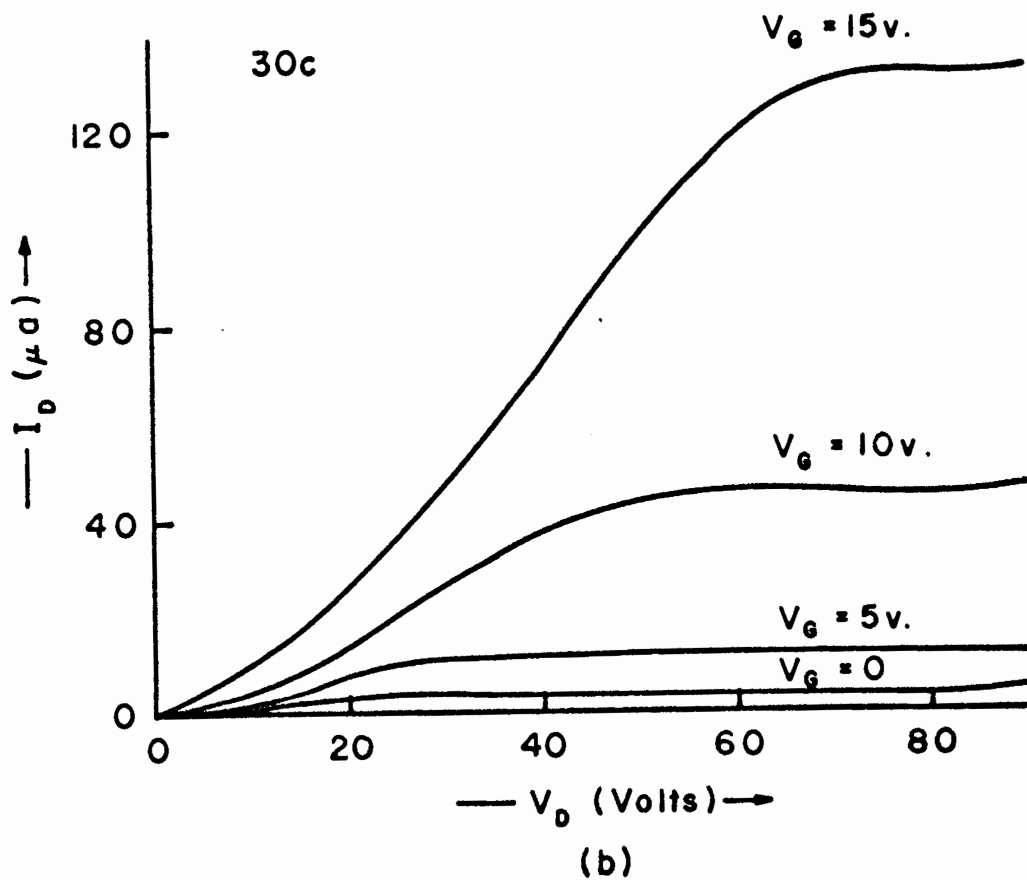


Figure 8-4. TFT Showing High Mobility and Transconductance.

the methods used in evaporating the SiO insulation, and will be discussed in more detail in Section 8.8.

The model from which equations (8-1) and (8-2) are derived is frequency independent and ignores the effect of electron traps. In reality the CdS film contains a large number of such traps. For the case of constant mobility it was shown in Section 2.6 that the transconductance is an increasing function of frequency. For frequencies lower than those characterizing the traps, a fraction of the electrons induced will be trapped resulting in a lower transconductance than at higher frequencies, where the traps are unable to follow the induced carrier variations. Fig. 8-5 displays the range of the frequency dependence of the transconductance observed in these devices.

8.3 Output Conductance

In the ideal device described in Section 2, the drain current is saturated for $V_D > (V_G - V_o)$. The model by Geurst has shown that the incremental output resistance is not, in general, infinite for $(V_G - V_o) < V_D$ but dependent upon the carrier mobility and on the electrostatic shielding of the drain electrode by the gate electrode. However, for the conditions appropriate to our present structures these effects are inadequate to account for the observed finite saturation and alternative mechanisms must be present.

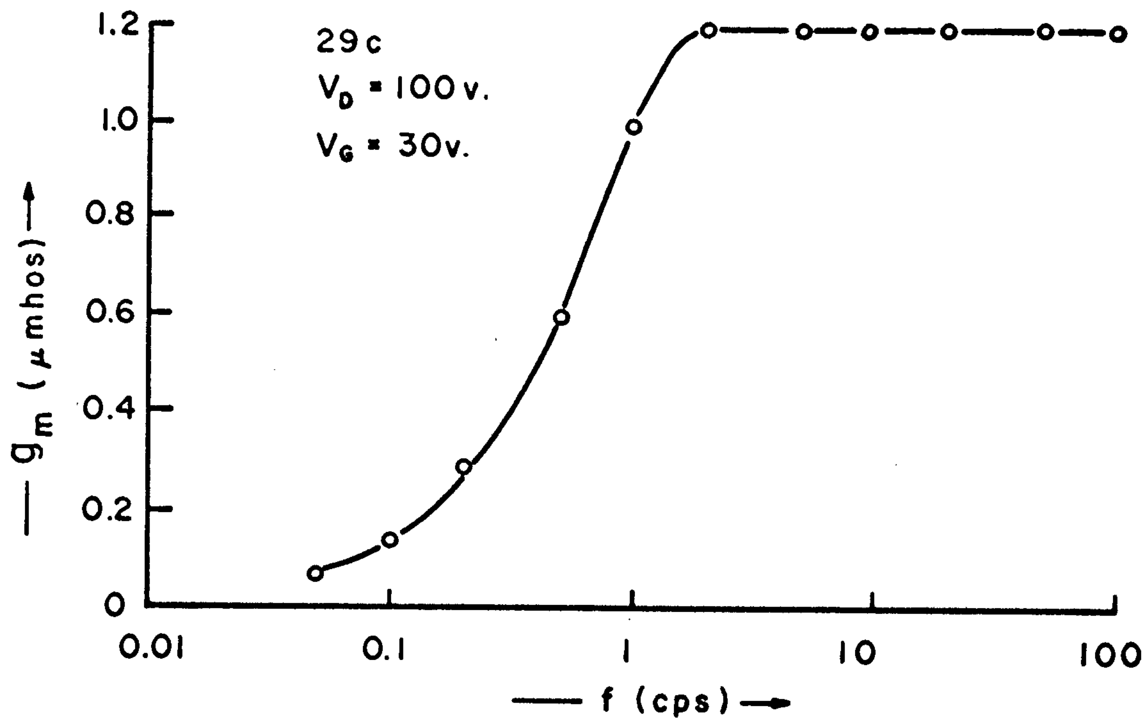
The dominant effects in reducing the incremental output

resistance are the filling of traps and mobility variations. Also, an unmodulated parallel conduction path between the source and the drain resulting from donor surface states on the reverse side of the film or too thick a semiconducting film could reduce the output resistance. The shunt conductance along the reverse side has been eliminated by the techniques described in Section 7.3. Fig. 8-6 shows in the I-V characteristics of a TFT with a very high saturation resistance. The incremental output resistance of two devices is plotted in Fig. 8-7. Saturation resistances of $> 10^8 \Omega$ are desirable at zero gate bias if the device is used to drive EL lamps.

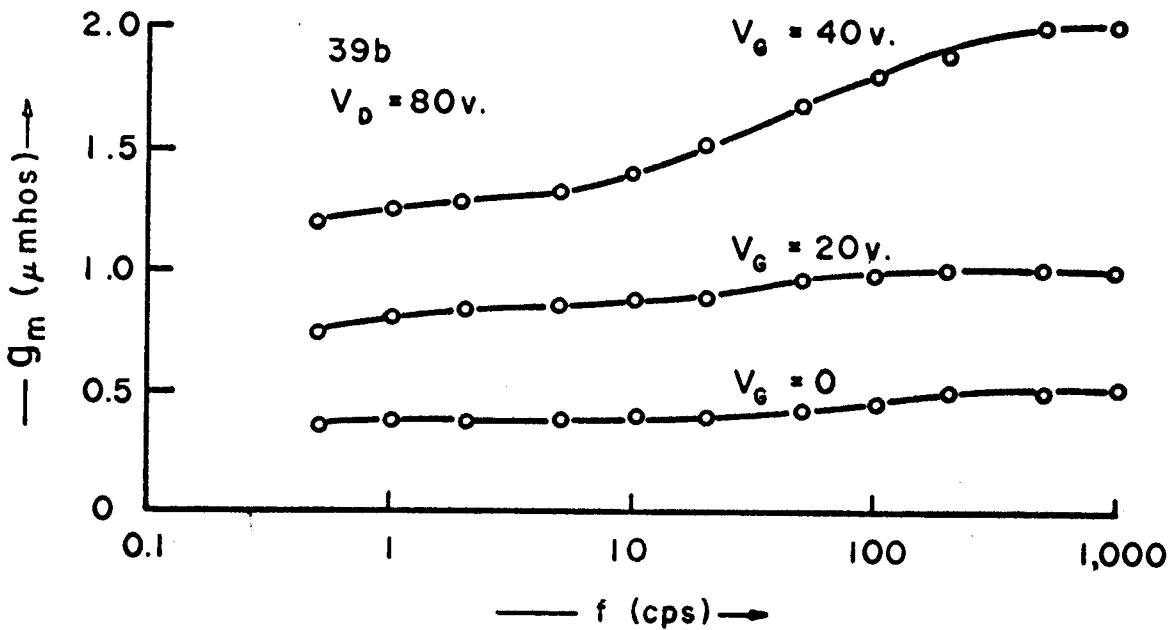
8.4 Switching Speed

The switching speed analysis of a TFT operating in the saturation region is given in Fig. 8-8. The circuit under consideration is illustrated in Fig. 8-8(a). The total capacitance between the source and drain is made up of the load, stray, and source-drain capacitances. Fig. 8-8(b) shows the device characteristics under consideration. When a step gate voltage is applied, the operating point instantly switches from point 1 to 2, as the voltage across the total source drain capacitance cannot change instantly. The operating point then relaxes to point 3 with time constant, τ, given by

$$\tau = \frac{r_{SD} R_L}{r_{SD} + R_L} (C_L + C_{SD} + C_{STRAY}) \qquad (8\text{-}3)$$



(a)



(b)

Figure 8-5. Frequency Dependence of the Transconductance of two TFT's showing the Effect of Slow Traps.

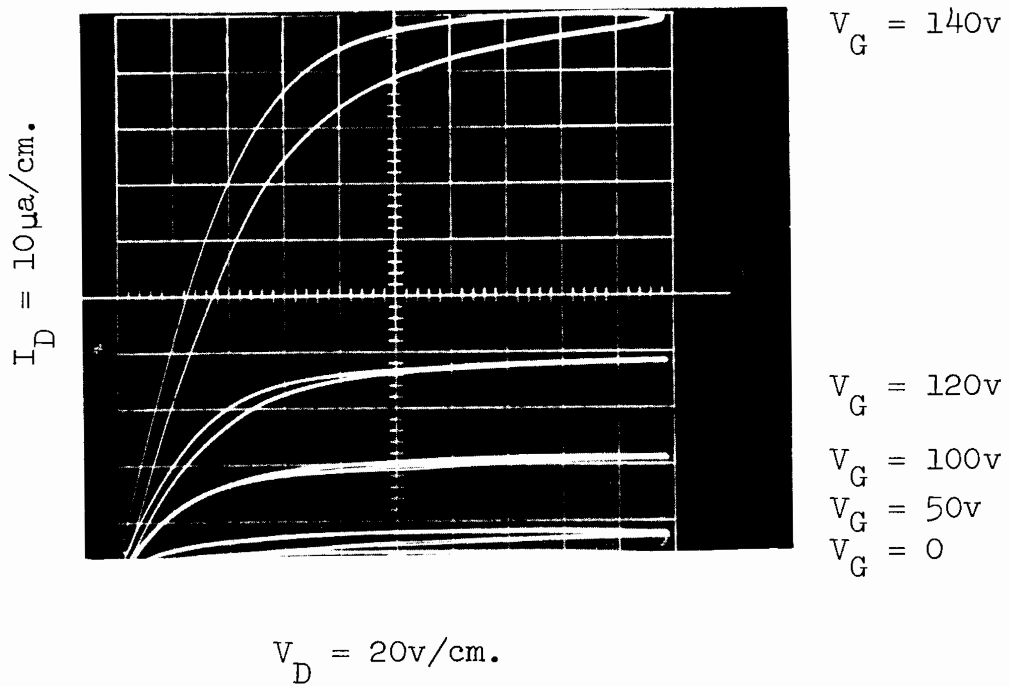


Figure 8-6. TFT With High Saturation Resistance.

where r_{SD} is the incremental output resistance defined by

$$r_{SD} = \left(\frac{\partial I_D}{\partial V_D}\right)^{-1} \qquad (8\text{-}4)$$

the turn off time is seen to be identical provided r_{SD} does not change with gate voltage.

The gate-drain capacitance, which has been neglected allows a fraction of the gate voltage to appear across the load with a polarity opposite to the drain signal. The initial magnitude of this signal is seen to be

$$V_D' = \frac{C_{GD}}{C_{GD} + C_T} V_G \qquad (8\text{-}5)$$

Measurement of the switching time of a high-voltage TFT is shown in Fig. 8-9(a) and Fig. 8-9(c) for two values of load resistance. For a load resistance of $10^7 \Omega$, the switching time is 0.2 msec., and for a load resistance of $10^6 \Omega$, the switching time is 0.1 msec.

The equivalent circuit of a typical load, an EL lamp, (see Appendix D) is a parallel resistance and capacitance. For a lamp with an area of 0.25 cm^2 this is approximately $10^6 \Omega$ in parallel with 100 pf. The switching speed of this RC load is shown in Fig. 8-9(b) to be 0.2 msec. A lamp with an area of 0.1 cm^2 is equivalent to $10^7 \Omega$ in parallel with 33 pf. Fig. 8-9(d)

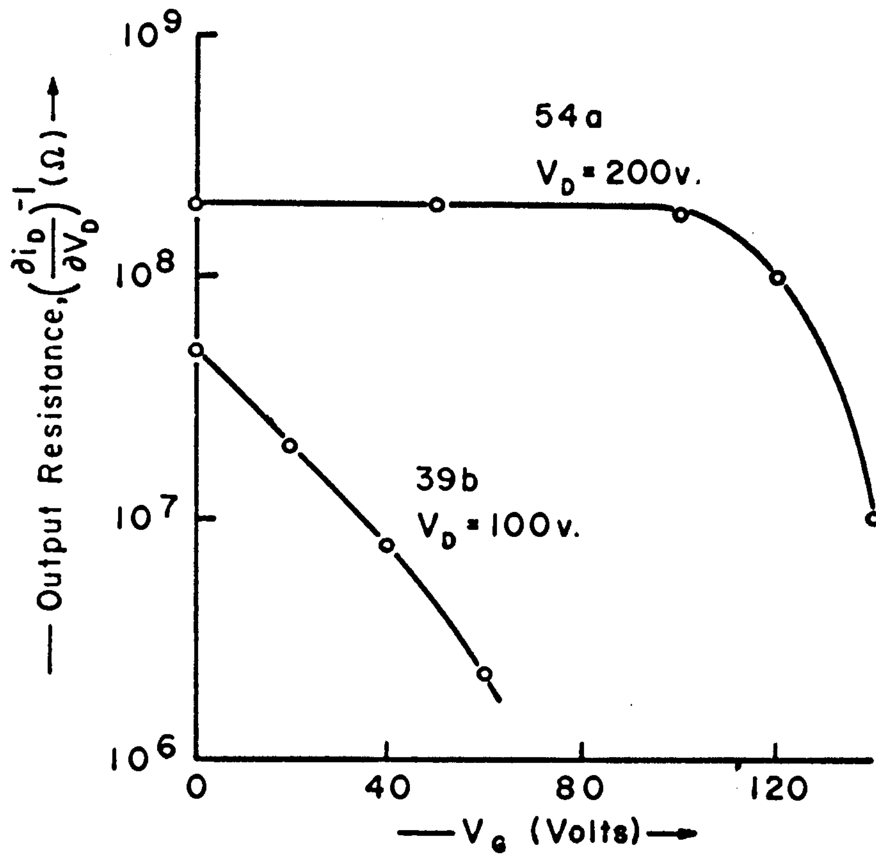


Figure 8-7. TFT Output Resistance vs. Gate Voltage.

shows that such a lamp can be switched in 0.5 msec. From this measurement one can determine the maximum size lamp that can be switched in the required time with a high voltage TFT. The actual switching times will be somewhat smaller as about 25 pf. of the total source-drain capacitance is due to the test circuit. A properly encapsulated circuit would have a stray capacitance of ~ 5 pf. Equation (8-5) shows that the capacitive feed-through signal is reduced for larger load capacitances. This is verified in Fig. 8-9.

8.5 Voltage Limitations

The high voltage TFT described in Section 7.2 was designed to withstand a source-drain voltage of 400 V for a dielectric breakdown strength of 4×10^6 V/cm. Measured dielectric breakdown strengths were in excess of 4.4×10^6 V/cm. and as high as 6×10^6 V/cm. implying $V_{SD} = 440 \rightarrow 600$ V as an upper limit for an insulation spacing of 10,000 Å. In most cases the I-V curves were plotted on a curve tracer with a maximum available voltage of 200 V, and this capability was not apparent. A curve tracer with a higher voltage capability was constructed, and Fig. 8-10 shows the I-V characteristics of a device for which the source-drain voltage was swept to 350 V. The high breakdown voltage of this unit is typical of the great majority of units constructed in this study.

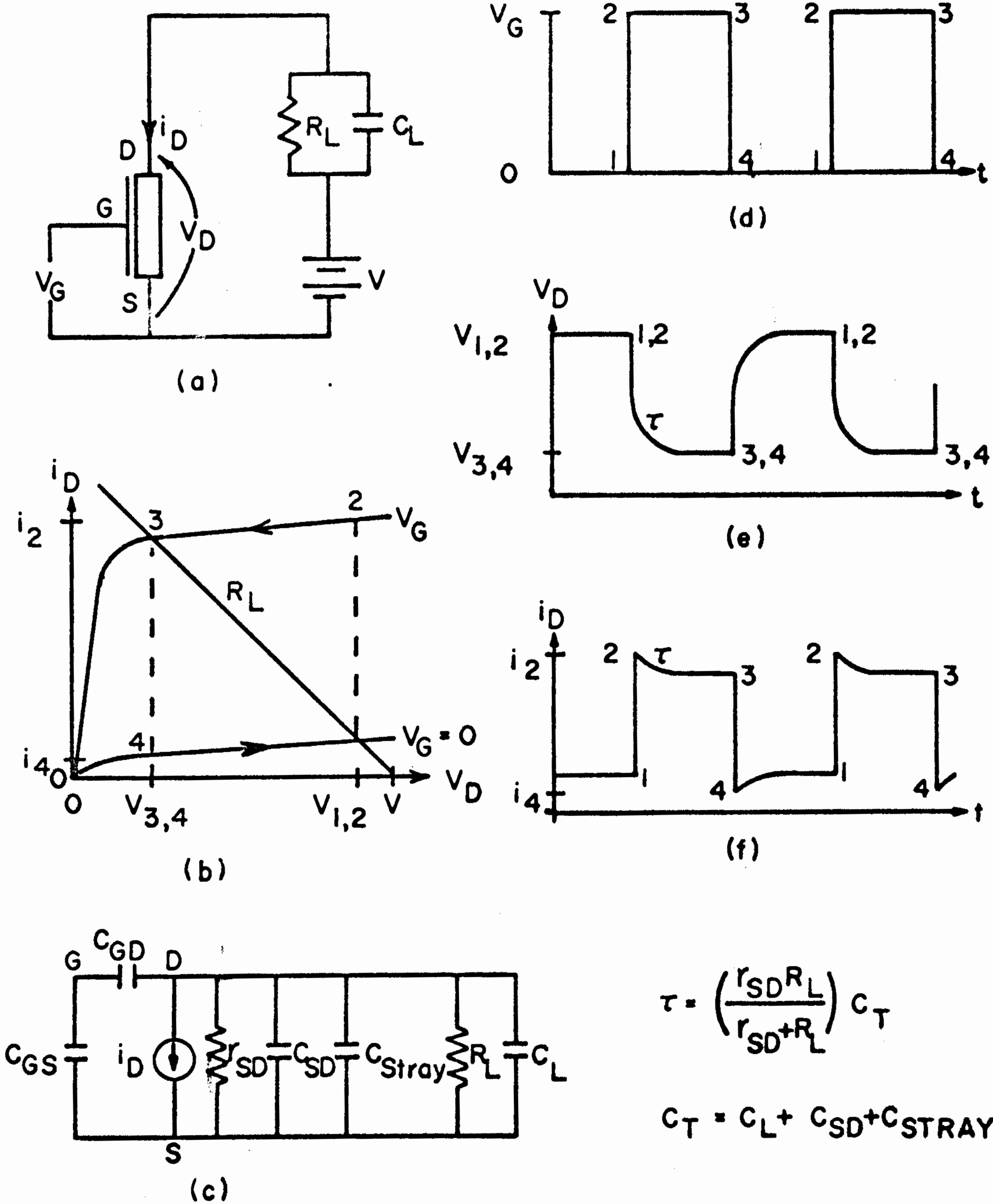
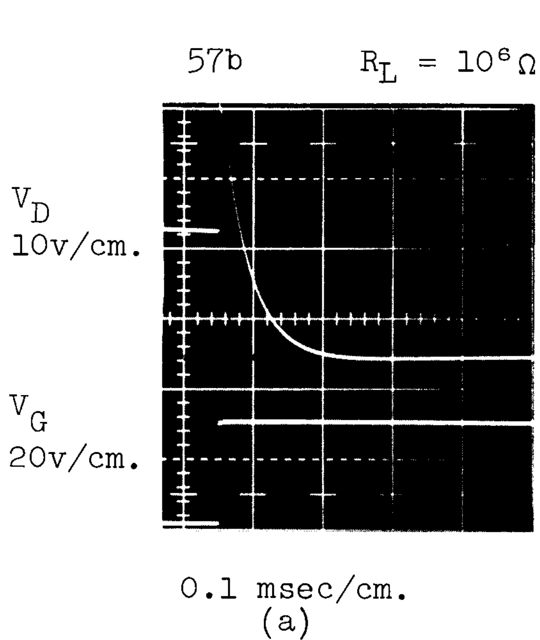


Figure 8-8. Switching Speed Analysis of a TFT with a Parallel RC Load Operating in the Saturation Region. (Direct coupling of gate voltage is neglected).

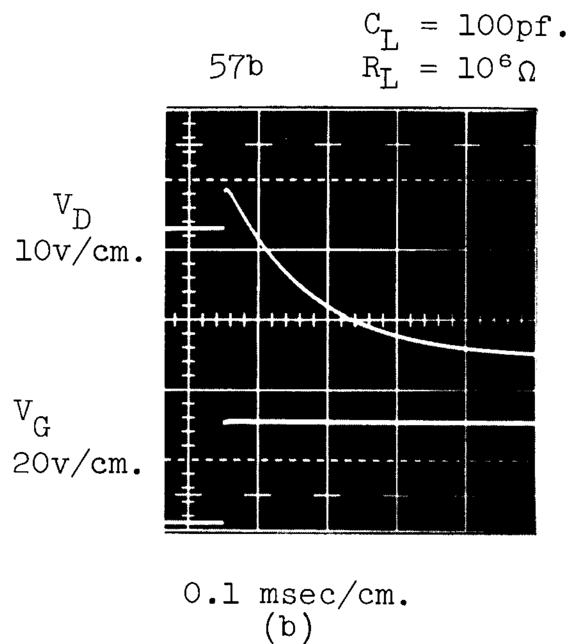
8.6 The High Voltage TFT as an EL Lamp Switch

Most EL lamps operate on a.c., however, the TFT drain must always be positive with respect to the source. One convenient supply for the lamp and TFT is a full-wave rectified sine wave as shown in Fig. 8-11. Alternatively the circuit could be supplied by a voltage $V + 2V \sin(\omega t)$. With zero gate voltage the extremely high output resistance of the TFT is sufficient to hold the lamp off. The lamp may be switched on with the application of a positive gate voltage. Lamps have been operated in this laboratory, in the extreme saturation region with a drain supply voltage of 350 V peak and switched with a gate voltage as low as 50 V. A further reduction in the gate voltage necessary may be achieved by increasing the mobility of the film and stabilizing the insulator. Typical lamp sizes used were 0.1 to 0.25 cm². Since the brightness of the lamps is approximately linear with frequency, it is desirable to use as high a frequency as is practical in the drain supply. The maximum useable frequency is then determined by the shunting effect of the source drain capacitance, and is about 2Kc for these transistors. As discussed in Section 8.4, the switching time is a function of the load and the transistor; a switching time of several milliseconds is adequate for visial displays.

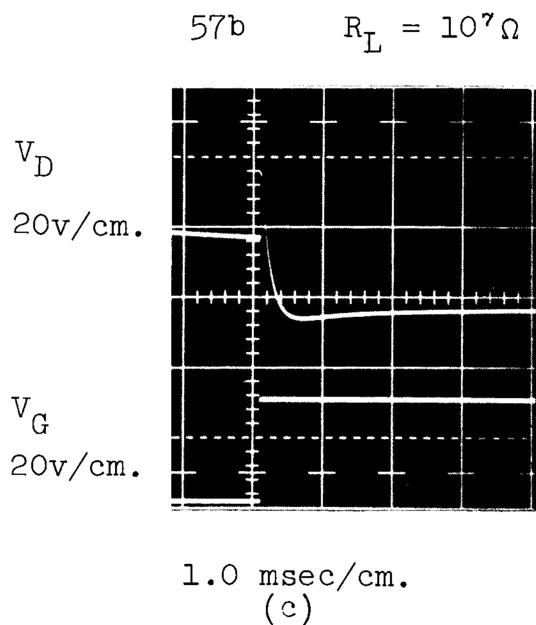
The output light intensity for a typical TFT driving a 0.25 cm² lamp is shown in Fig. 8-12. At a gate voltage of 60 volts, the lamp produces sufficient brightness. When V_G is



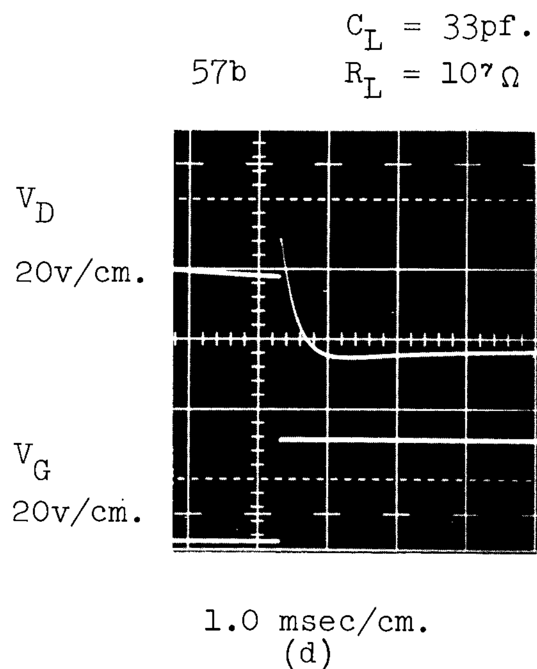
(a)



(b)



(c)



(d)

Figure 8-9. Switching Time for a Transistor with Various RC Loads.

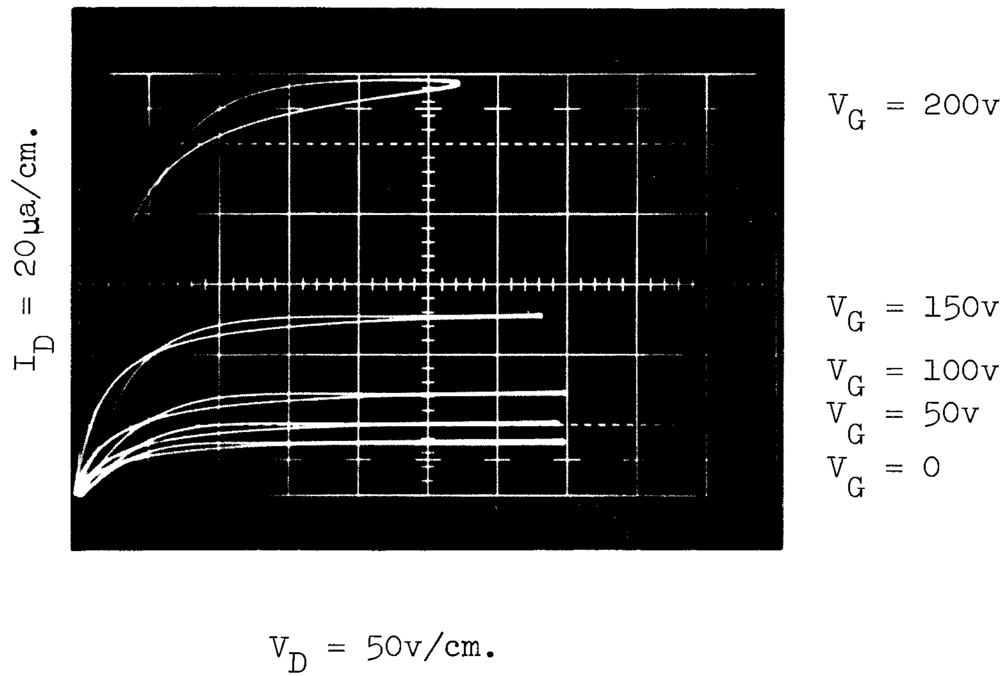


Figure 8-10. TFT Operating with V_{SD} = 350 volts.

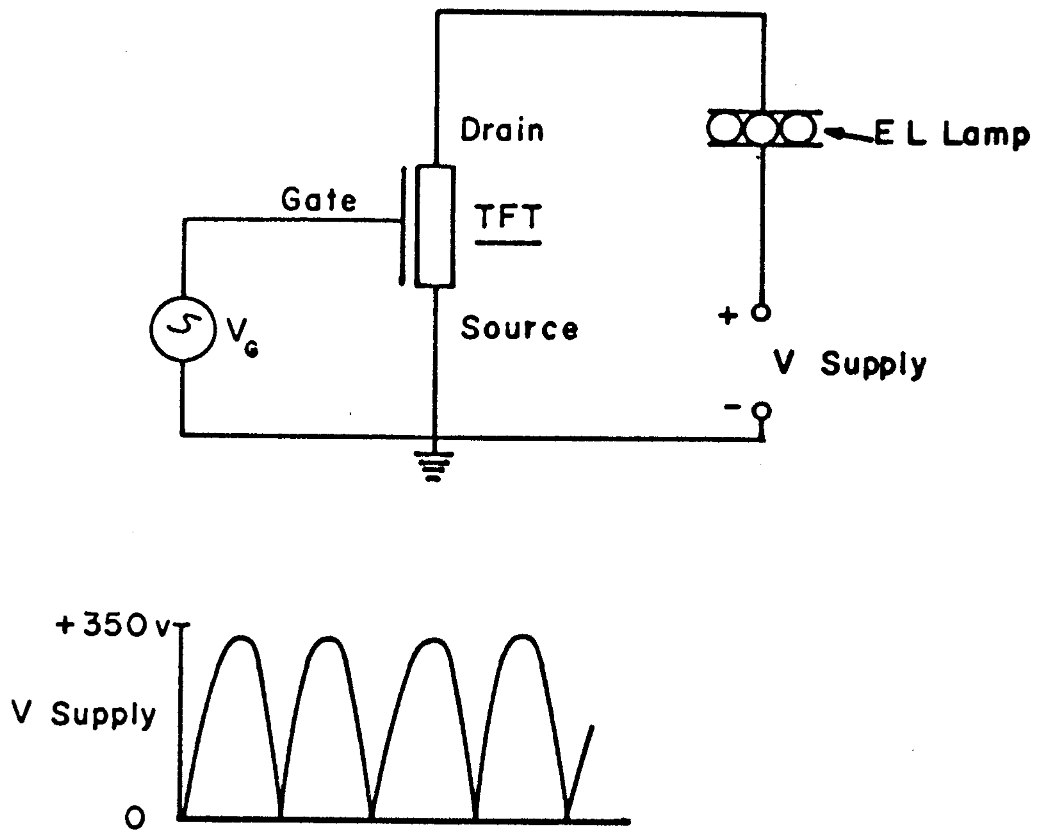


Figure 8-11. TFT Switching of EL Lamp.

increased beyond 80 volts, the light intensity saturates. The maximum brightness obtained was comparable to that obtained by the direct application of a.c. to the lamp. The data in Fig. 8-12 were taken with a silicon solar cell mounted adjacent to the TFT and were computed using the sensitivity of the solar cell at the peak (520 mμ) intensity of the EL lamp.

The high voltage TFT's and interconnections necessary to switch an array of lamps may all be deposited on the same substrate and mounted adjacent to the lamps resulting in a compact, compatible structure.

8.7 The Effects of Rectifying Contacts

Ohmic contacts with CdS films may be made with aluminum, gallium and indium. However, indium and gallium melt at the high substrate temperatures used in device fabrication. Great care is required with the aluminum evaporation if ohmic contacts are desired. If evaporated too slowly, a semi-insulating barrier will be formed under the electrode. Rectifying contacts may also be formed when the aluminum reacts with the source producing an alloy which will not make ohmic contact. Rectifying contacts were formed when a tantalum filament was used more than once to evaporate aluminum contacts.

The effects of rectifying contacts may be seen by examining the I-V characteristics of a TFT. A rectifying source contact

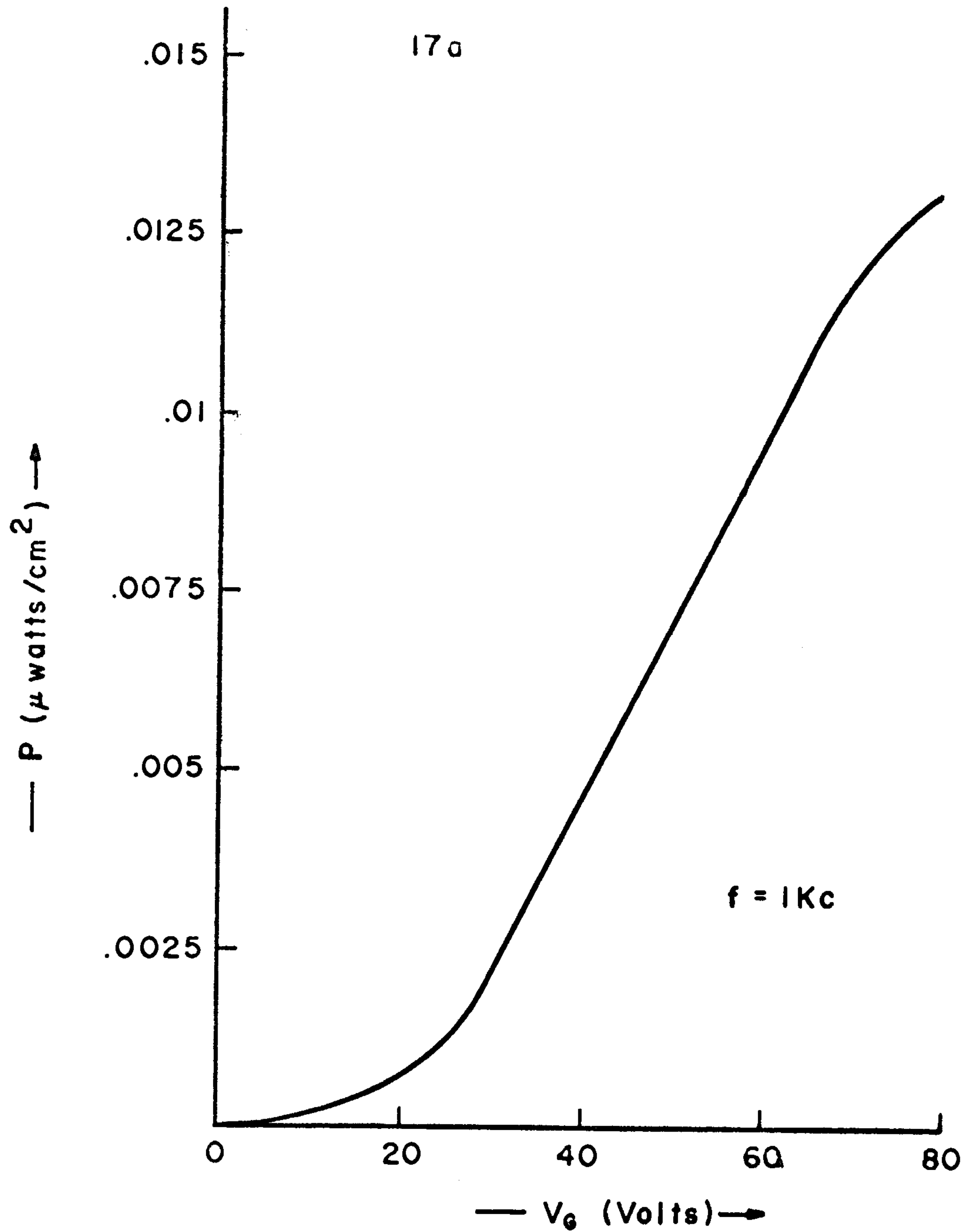


Figure 8-12. EL Lamp Power vs. Gate Voltage for a 0.25 cm² Lamp as Detected by a Silicon Solar Cell.

produces a crowding of the characteristics at high gate voltages. The rectifying Al-CdS contact at the source is a reversed biased diode which limits the amount of current that may be drawn in from the source electrode. A rectifying CdS-Al drain contact produces an S-shaped I-V characteristic near the origin; this diode will be forward biased and will not limit the maximum drain current. Fig. 8-13 shows the effect of a rectifying drain contact on the I-V characteristic of a TFT.

One then wonders why one contact is rectifying when both were fabricated at the same time. In these two devices the lower aluminum source-drain contact (Fig. 7-2(b)) between the CdS and SiO was missing. The high gate-drain field produced solid state electrolysis effects; it was thought that oxygen ions diffused through the insulation and CdS and made a semi-insulating barrier on the drain electrode. This is illustrated in Fig. 8-14. Where the I-V curves in Fig. 8-14(a) were taken first, and a rectifying drain electrode has been formed. The source and drain electrodes were reversed and the I-V curves of Fig. 8-14(b) taken; the saturation of the new source electrode is apparent. To avoid this type of behavior, a source-drain electrode should be placed between the CdS and SiO, as indicated in Fig. 7-2.

8.8 Device Stability

In a stable device the drain current should be uniquely defined by the gate voltage and the drain voltage. In many

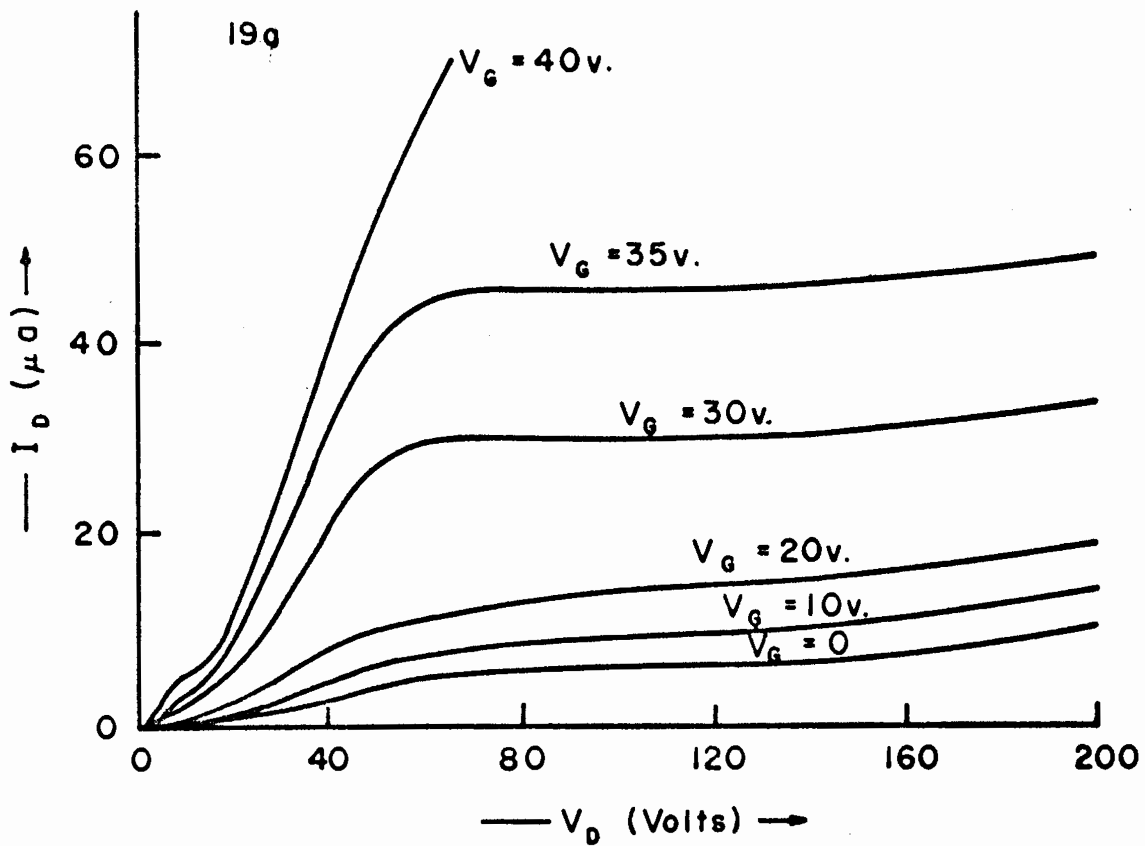
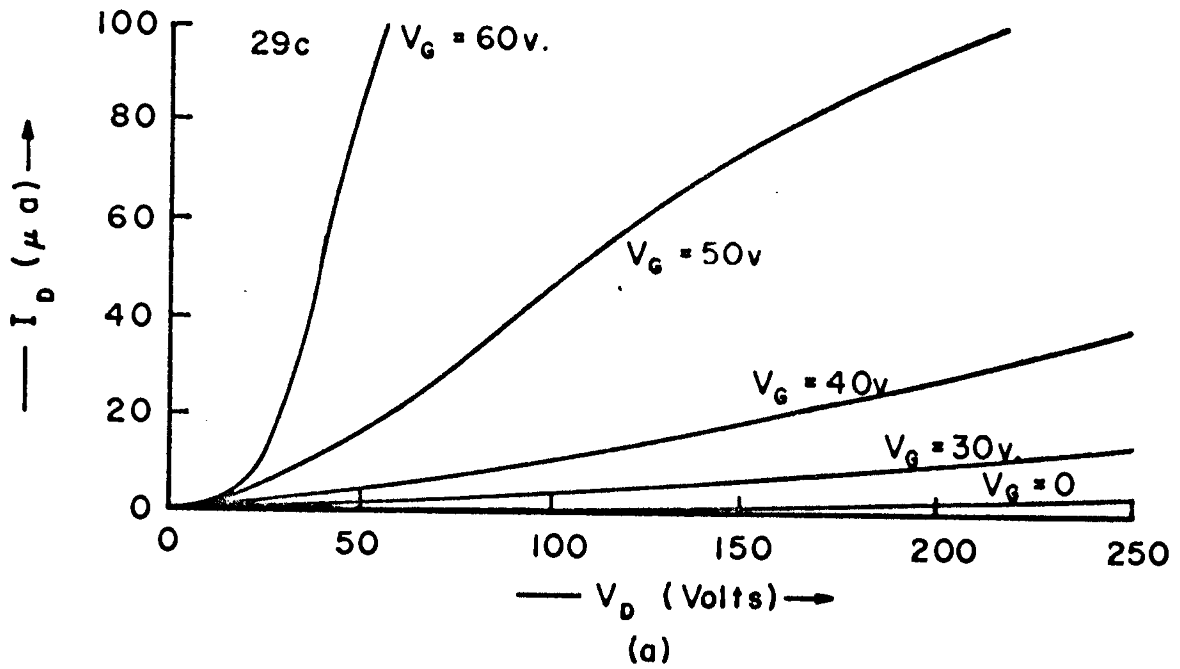


Figure 6-13. Effect of Rectifying Drain Contacts on TFT Characteristics.

devices instability of some form is evident. The most troublesome form of instability in insulators may be the motion of ions due to the high applied electric field. The oxide contains mobile, polyatomic molecules which may be easily dissociated.[74] The application of a positive voltage to the gate causes the migration of negative ions toward the gate electrode and positive ions toward the CdS. The slow migration of ions causes the electric field at the CdS surface to slowly increase with time, as illustrated in Fig. 8-15. This slow drift of characteristics of a very unstable device is demonstrated in Fig. 8-16.

When the gate voltage is removed, the transistor does not return to its previous "off" condition for some time. The change in "off" characteristic can be interpreted as a change in the electron or trap concentration. Heiman[74] has reported changes in unpassivated thermally grown SiO_2 on Si as high as $\Delta n = 5 \times 10^{11}/cm^2$, while after passivation with phosphorous this change is reduced to $\Delta n = 5 \times 10^{10}/cm^2$. In this study similar changes of $\Delta n = 5 \times 10^{11}/cm^2$ for evaporated SiO_X in a dry N_2 atmosphere were observed. The ion mobilities in the insulator determine the speed with which the drain current drifts after application of a gate bias.

Humidity also affects the value of V_O, the pinch off voltage. Absorption of water vapor in the insulation has an effect which is the same as creation of acceptor-like states at the CdS interface. By connecting the transistor as a diode



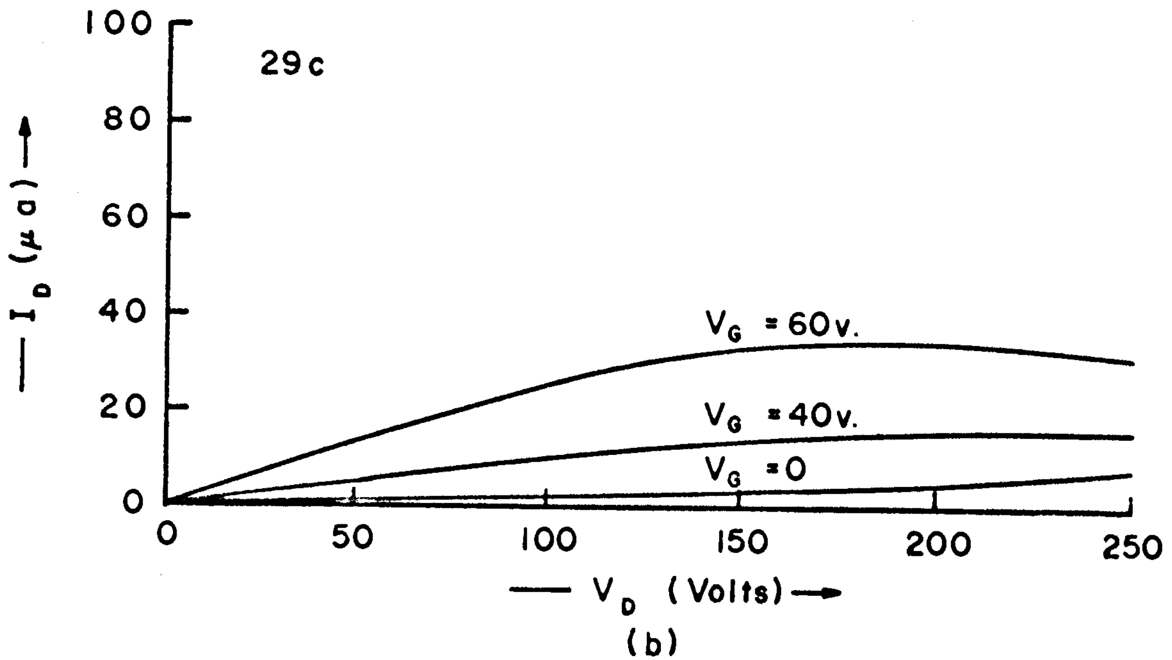


Figure 8-34. Effect of Reversing the Source Drain Connection [illegible] with Rectifying Contacts. First (a) was plotted, the source and drain connections reversed, then (b) was plotted.

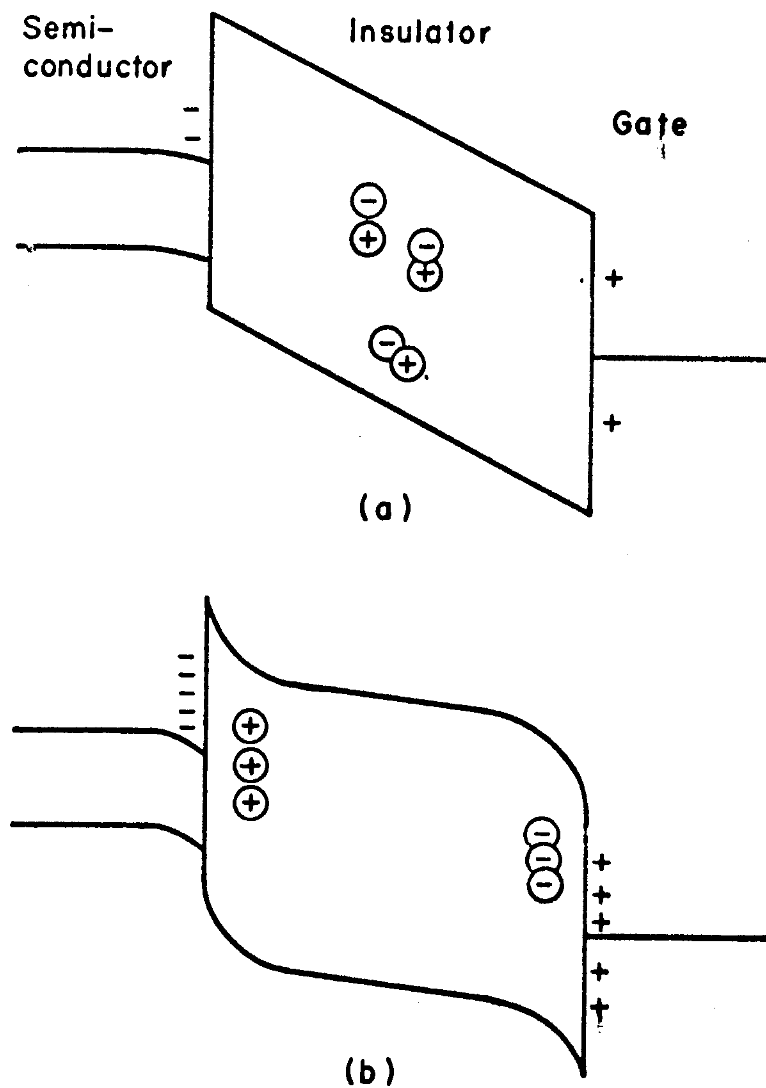


Figure 8-15. Illustration of Ion Drift in an Insulator. (a) Initial application of positive gate voltage followed by (b) slow ion migration.

($V_G = V_D$) one may see the effect of humidity on V_o. Fig. 8-17 shows the diode characteristic of a very unstable TFT in dry N_2 and in room humidity; V_o has changed by about 100 V indicating that $\Delta n = 1.3 \times 10^{12}/cm^2$. In a more stable unit such as 39b, (see Fig. 8-2) $\Delta V_o \sim 15$ V which corresponds to $\Delta n = 2 \times 10^{11}/cm^2$. This shows that the effect of ion drift in the insulator is greater than the effect of humidity. The relative humidity in the laboratory was typically 50 - 70%. Instability effects due to humidity were eliminated by potting the TFT in Silicone rubber.

The degree of instability was found to vary considerably with the technique used for evaporating the SiO layers. The most stable films were deposited from SiO pellets suspended on a tantalum wire as described in Section 3.4.2. SiO films depositied from a tantalum crucible proved to be very unstable. Free silicon, which is formed from decomposition of SiO, forms a eutectic with platinum at 830°C[75] also making films deposited from platinum boats unstable. Boron nitride seems somewhat better, but an electron beam source should probably be used for best results.

8.9 Suggestions for Improvement of the Characteristics

Improvement in device performance may be realized by improving the stability of the oxide layer and increasing the film mobility. One avenue of approach to this problem may be the selection of a semiconductor such as CdSe with a

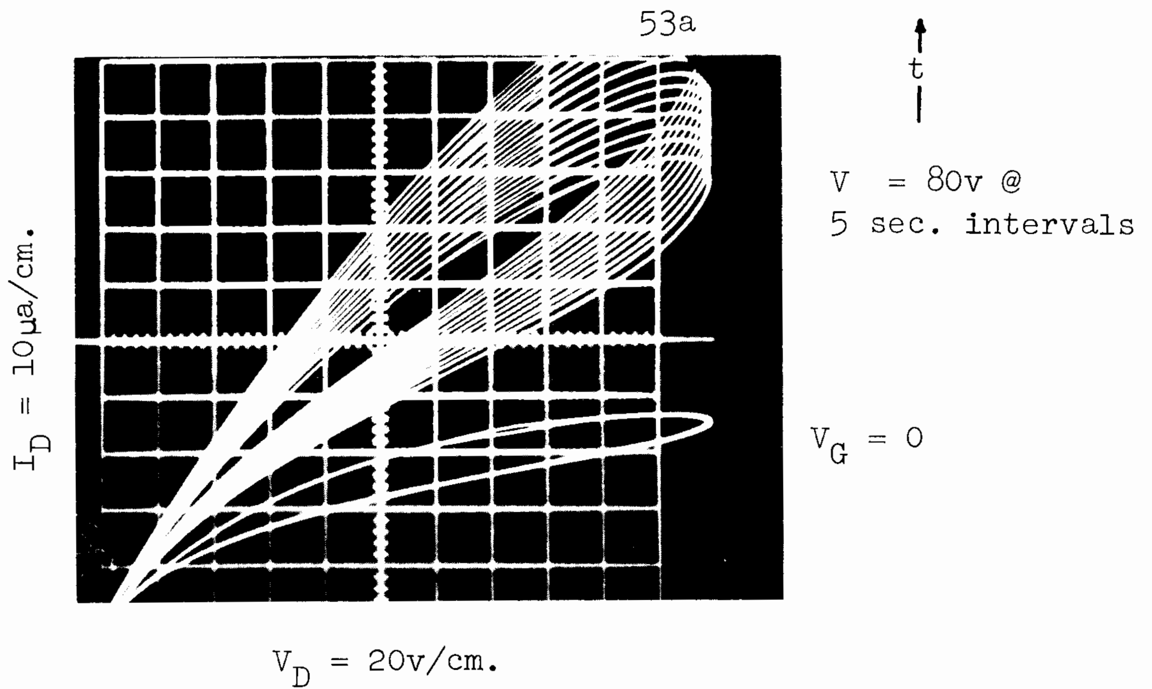


Figure 8-16. Instability in TFT Characteristics.

Dark, Dry

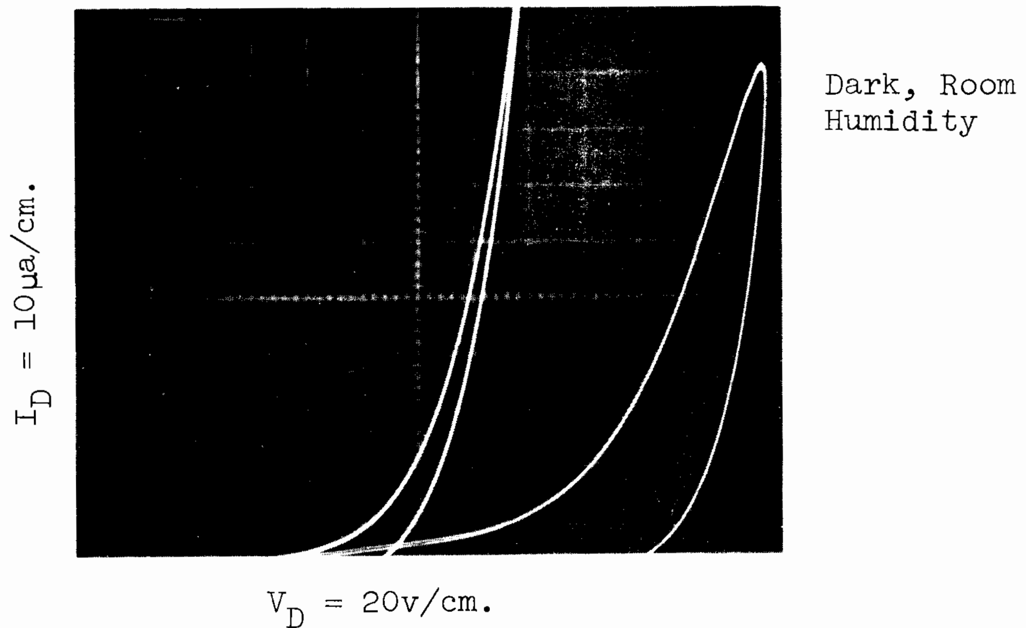


Figure 8-17. TFT Connected as a Diode ($V_G = V_D$) Showing Shift in Characteristic due to Moisture in the Insulator.

higher mobility. The single crystal mobility of CdSe is 600 cm^2/V-sec. compared with 300 cm^2/V-sec. for CdS. One CdSe transistor was constructed in this study. Although the resistivity was too low for use as an EL switch, the effective mobility was 2.5 cm^2/V-sec. There is every reason to expect that a higher value of mobility is attainable. The selection of an insulator with a closer lattice structure than SiO will aslo help to reduce ion migration.

Additional improvement in device gain at the expense of band width may be obtained by using a symmetrical double gate TFT. The double gate TFT has an insulated gate on each side of the semiconductor and has been extensively analyzed(76, 77). For the case when the two gates are at the same potential the equations which describe the double gate TFT are the same as the single gate TFT except

$$C_G \rightarrow 2\ C_G\ . \qquad (8\text{-}5)$$

The gate voltage required to supply the same drain current in saturation is given by

$$(V_G - V_o)_{\substack{\text{Double}\\\text{Gate}}} = \frac{1}{\sqrt{2}}\,(V_G - V_o)_{\substack{\text{Single}\\\text{Gate}}} \qquad (8\text{-}6)$$

This increase in gain is at the expense of bandwidth; the double gate TFT would still have adequate bandwidth to drive an EL lamp.

9. CONCLUSION

This investigation of field effects in cadmium sulfide films has yielded a new high voltage thin-film transistor constructed entirely by vacuum evaporation. This TFT, which is capable of withstanding over 300 V, will switch a current of 100μa with a gate voltage of less than 50 V, and is particularly suited as a transistor controlled switch for applications involving a high impedance load.

Devices were constructed with an incremental saturation resistance of 200 MΩ and a maximum operating voltage of 350 V. Rise times of 0.2 msec. for a $10^7 \Omega$ load were observed. The transconductance ranged from 3 to 13 μmhos. The large gate voltage required and the low transconductance observed were attributed to the low electron mobility (0.5 $\rightarrow$ 2.5 cm^2/V-sec.) of the polycrystalline films, and the high density of electron traps (up to 10^{12}/cm^2) at the CdS surface. The variation of the pinch off voltage, V_O, and the instability in the characteristics were attributed to the insulation evaporation techniques. The density of mobile ions, which affect the device stability, is a function of the insulation evaporation technique and environment; devices with SiO insulation were observed to be unstable unless operated in a nitrogen atmosphere. There are no extensive data yet on the reproducibility of the high voltage TFT, but based on the limited number of devices constructed it appears that reproducible devices will not be difficult to make.

Resistivity and Hall mobility measurements on CaF_2/SiO coated CdS films showed that control of the CdS surface potential was possible. By evaporating a thin layer of CaF_2 between the CdS and SiO, the effect of the donor-like surface states of SiO was reduced by the effect of the acceptor-like surface states of CaF_2. By proper choice of CaF_2 thickness, any surface potential between the limits appropriate to SiO and CaF_2 could be obtained.

It was found that an evaporated CaF_2 layer could be used to control the surface potential of germanium, and the effect of adjusting the surface potential of a Ge(Li) gamma-ray detector was seen to be an increase in the resolution of over 20% on the 662KeV gamma-ray of Cs^{137}. Application of 150 - 200 Å of CaF_2 to the exposed edges of the detector appeared to restore the surface potential in the intrinsic region to the bulk value, and thus result in a lower surface leakage current, and increased resolution.

Further study may improve the performance of the high voltage TFT by stabilizing the oxide layer and increasing the film mobility. Increased mobility may be obtained by improving the CdS deposition techniques, or by choosing another semiconductor such as CdSe. The selection of an insulator with a closer lattice structure than SiO should help to reduce ion migration in the insulator.

APPENDIX A. CALCULATION OF THE SMALL SIGNAL A.C. TRANSCONDUCTANCE AND OUTPUT CONDUCTANCE OF A TFT.

A.1 Introduction

In the usual derivation of TFT characteristics, the mobility and gate capacitance are considered to be constant. It is instructive to re-derive the expressions for the transconductance and output conductance of a TFT while allowing these quantities to vary with source drain voltage, V_D, and gate voltage, V_G. This derivation will show the functional dependence of the transconductance and output conductance on the mobility and gate capacitance variations. No attempt will be made here to relate these variations to the physical processes involved. This model will be valid in the gradual approximation as discussed in Section 2.2.

A.2 Calculation of the Transconductance

The transconductance is defined as

$$g_m \equiv \left(\frac{dI_D}{dV_G}\right)_{V_D} \qquad \text{(A-1)}$$

the variation in drain current may be written as

$$dI_D = \frac{WL_D}{L} V_D \, d\sigma \qquad \text{(A-2)}$$

for the sample geometry shown in Fig. 2-1. The Debye length,

L_D, is the depth to which conduction electrons are distributed in the semiconductor in the enhancement region. To solve for $d\sigma$, one allows both n_c, the density of conduction electrons, and μ, the mobility to change with gate voltage.

$$\frac{d\sigma}{dV_G} = \frac{dn_c}{dV_G} e\mu + n_c e \frac{d\mu}{dV_G} \qquad \text{(A-3)}$$

where the average n_c may be expressed as

$$n_c = \frac{C_G\ (V_G - V_D/2)}{eL_D WL} + \frac{N_o}{L_D WL} \qquad \text{(A-4)}$$

$N_o/L_D WL$ is the density of electrons on the semiconducting surface at $V_G = V_D = 0$ if N_o is positive, or the density of unfilled traps at $V_G = V_D = 0$ if N_o is negative. N_o may be expressed as a voltage in the following way:

$$N_o = \frac{-V_o C_o}{e} \qquad \text{(A-5)}$$

where C_o is the oxide capacitance of the gate insulation. Thus:

$$n_c = \frac{C_G\ (V_G - V_D/2)}{eL_D WL} - \frac{V_o\ C_o}{eL_D WL}\ . \qquad \text{(A-6)}$$

The variation of gate capacitance with gate voltage is contained in the term

$$\frac{dn_c}{dV_G} = \frac{\partial n_c}{\partial C_G}\frac{dC_G}{dV_G} + \frac{\partial n_c}{\partial V_G} \qquad \text{(A-7)}$$

upon substituting one obtains

$$g_m = \frac{V_D C_G \mu}{L^2} + (V_G - \frac{V_D}{2} - \frac{C_o}{C_G} V_o) \frac{C_G V_D}{L^2} (\frac{d\mu}{dV_G}) \qquad \text{(A-8)}$$

$$+ (V_G - \frac{V_D}{2}) \frac{V_D \mu}{L^2} (\frac{dC_G}{dV_G}) \; .$$

The first term is identical to the term obtained by Borkan and Weimer[18] for the case of constant mobility and gate capacitance. Equation (A-8) shows that if $d\mu/dV_G \sim \mu$, then mobility variations cannot be neglected. Fig. 2-8 shows that this is indeed the case for low gate voltages. The smaller magnitude of the gate capacitance variation (Fig. 2-9) would imply that this term is not as important as the mobility variation term.

A.3 Calculation of the Output Conductance

The output conductance is defined by

$$g_{DO} \equiv (\frac{dI_D}{dV_D})_{V_G} \; . \qquad \text{(A-9)}$$

The source-drain current, I_D, may be written as:

$$I_D = \frac{WL_D}{L} V_D \, \sigma \qquad \text{(A-10)}$$

from which one obtains

$$g_{DO} = \frac{WL_D}{L} \left(\sigma + V_D \frac{d\sigma}{dV_D}\right) . \qquad \text{(A-11)}$$

Upon substituting, one obtains in an analogous manner the expression for the output conductance.

$$g_{DO} = \left(V_G - V_D - \frac{C_o}{C_G} V_o\right) \frac{C_G \mu}{L^2} + \left(V_G - \frac{V_D}{2} - \frac{C_o}{C_G} V_o\right) \frac{V_D C_G}{L^2} \left(\frac{d\mu}{dV_D}\right)$$

$$+ \left(V_G - \frac{V_D}{2}\right) \frac{V_D \mu}{L^2} \left(\frac{dC_G}{dV_D}\right) \qquad \text{(A-12)}$$

Again, the first term agrees with the model of constant and gate capacitance.

APPENDIX B. APPARATUS FOR THE MEASUREMENT OF THE RESISTIVITY AND HALL COEFFICIENT IN HIGH RESISTIVITY SEMICONDUCTORS

B.1 Introduction

The apparatus used was designed by Fischer, Grieg, and Mooser.[78] It differs from previous instruments in that it will permit measurement of sample resistivities for sample resistances in the range $10 \rightarrow 10^{12}\Omega$ and determination of the Hall coefficient for samples with a mobility as low as 1 cm^2/V-sec. Such a range is necessary for measurement of high resistivity-low mobility evaporated CdS films. In addition to the 6 terminal standard Hall sample, this apparatus will permit measurements with the van der Pauw geometry[79, 80, 81] and other techniques designed for high resistivity evaporated thin films such as the one described by Gobrecht, et. al.[82]

B.2 Theory of Operation

The simplest circuit permitting independent measurement of V and I is shown in Fig. B-1. This circuit can only be grounded at one terminal, A or B; thus, shielding of the ungrounded circuit becomes difficult for high impedance samples. The significant change made by the designers is the addition of another electrometer and potentiometer as shown in Fig. B-2. By nulling electrometer E_3 with potentiometer P_2, the current supply is connected to the voltage measuring circuit by a low resistance path (P_2) and only shielding of the sample is

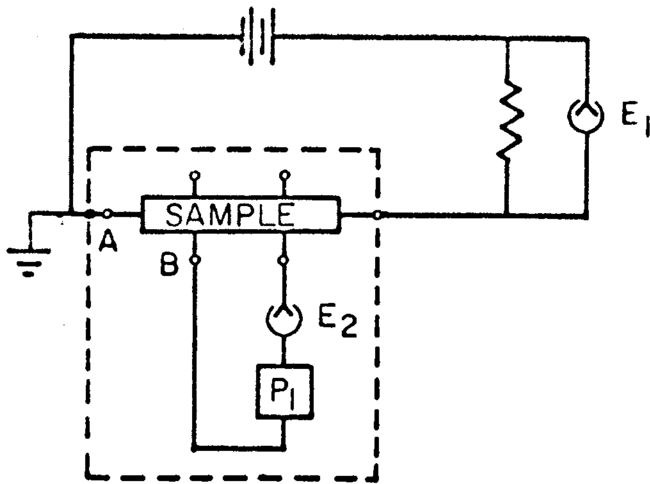


Figure B-1. Basic Measuring Circuit

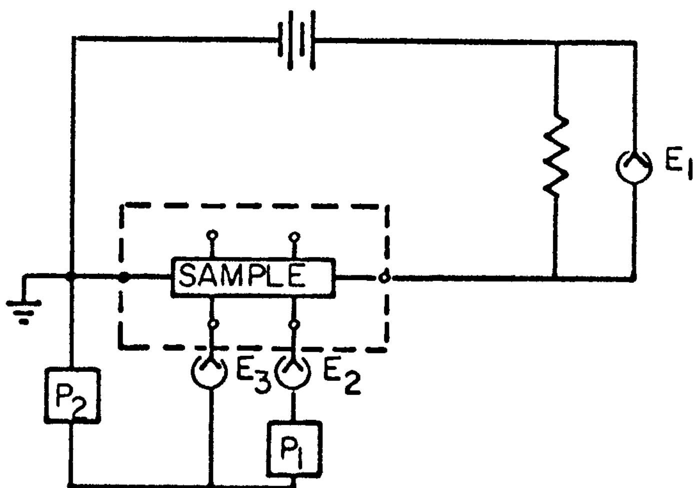


Figure B-2. Modified Measuring Circuit

necessary. Two electrometers must now be nulled to make a voltage measurement; however, this is offset by simpler shielding.

B.3 Measurement Techniques

The complete bridge is described in the block diagram of Fig. B-3. The sample current is determined by electrometer E_1 and its decade shunt. Potentiometer P_2 serves to connect the primary or current supply circuit to the secondary or voltage measurement circuit. This potentiometer need not be calibrated; but stable drift free operation is essential. Potentiometer P_1 alone is used to measure the sample voltage for the four terminal resistivity measurement. For Hall measurements the voltage is measured by the series combination of P_1 and P_3 in the following manner.

With the forward magnetic field (or zero field) on, potentiometer P_3 is used to null out electrometer E_2; then the magnetic field is reversed (or turned on) and potentiometer P_1 is switched in series with P_3. The signal corresponding to $2V_H$ (or V_H) may now be read on P_1 which is calibrated from $1\mu V$ to 1V. The purpose of P_3 is to null out the signal at the Hall terminals corresponding to contact misalignment. Thus the bridge consists of two very stable uncalibrated potentiometers (P_2, P_3) and one stable calibrated potentiometer (P_1). The potentiometers shown in the accompanying figures (B-4 and B-5)

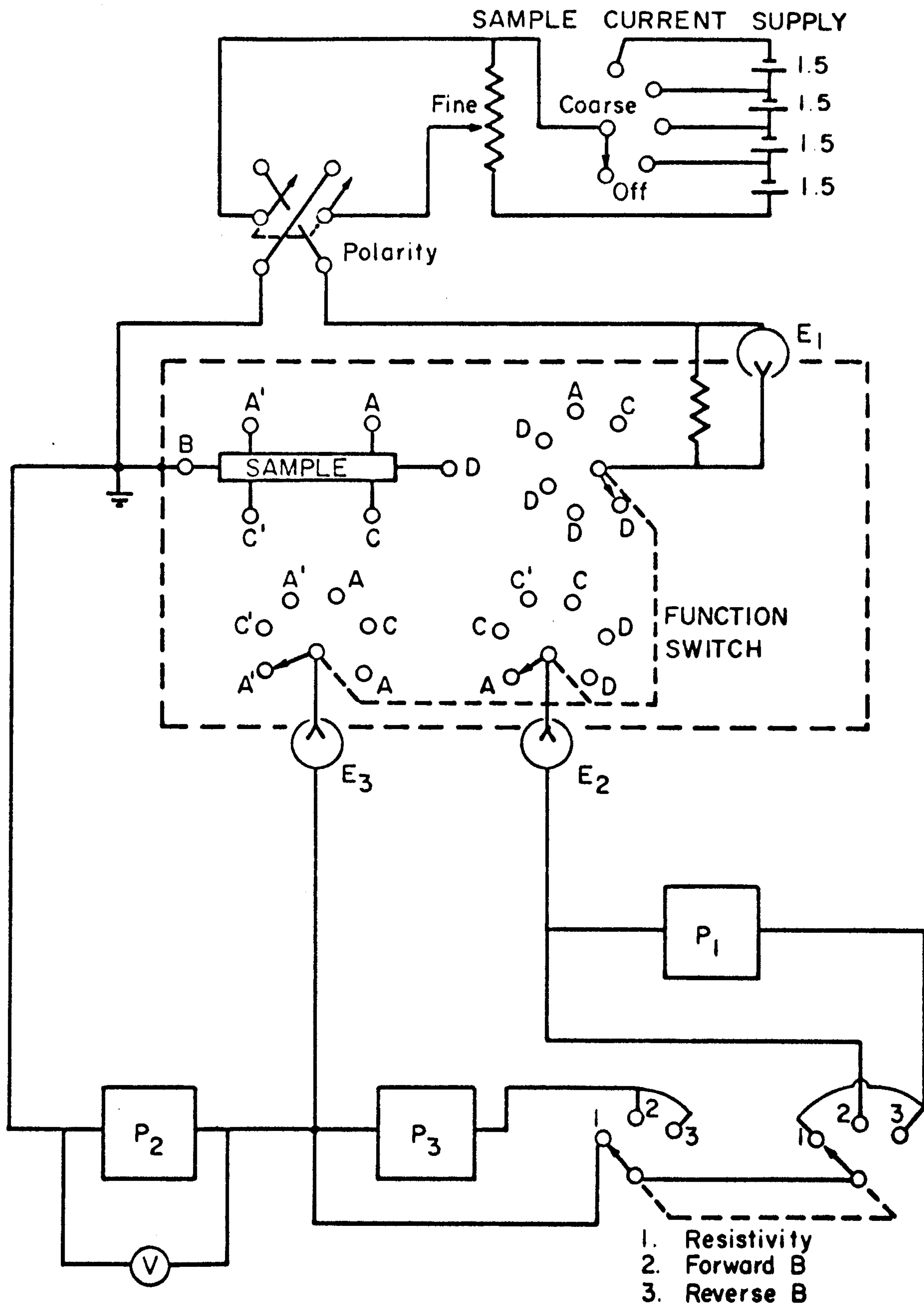


Figure B-3. Block Diagram of the Bridge

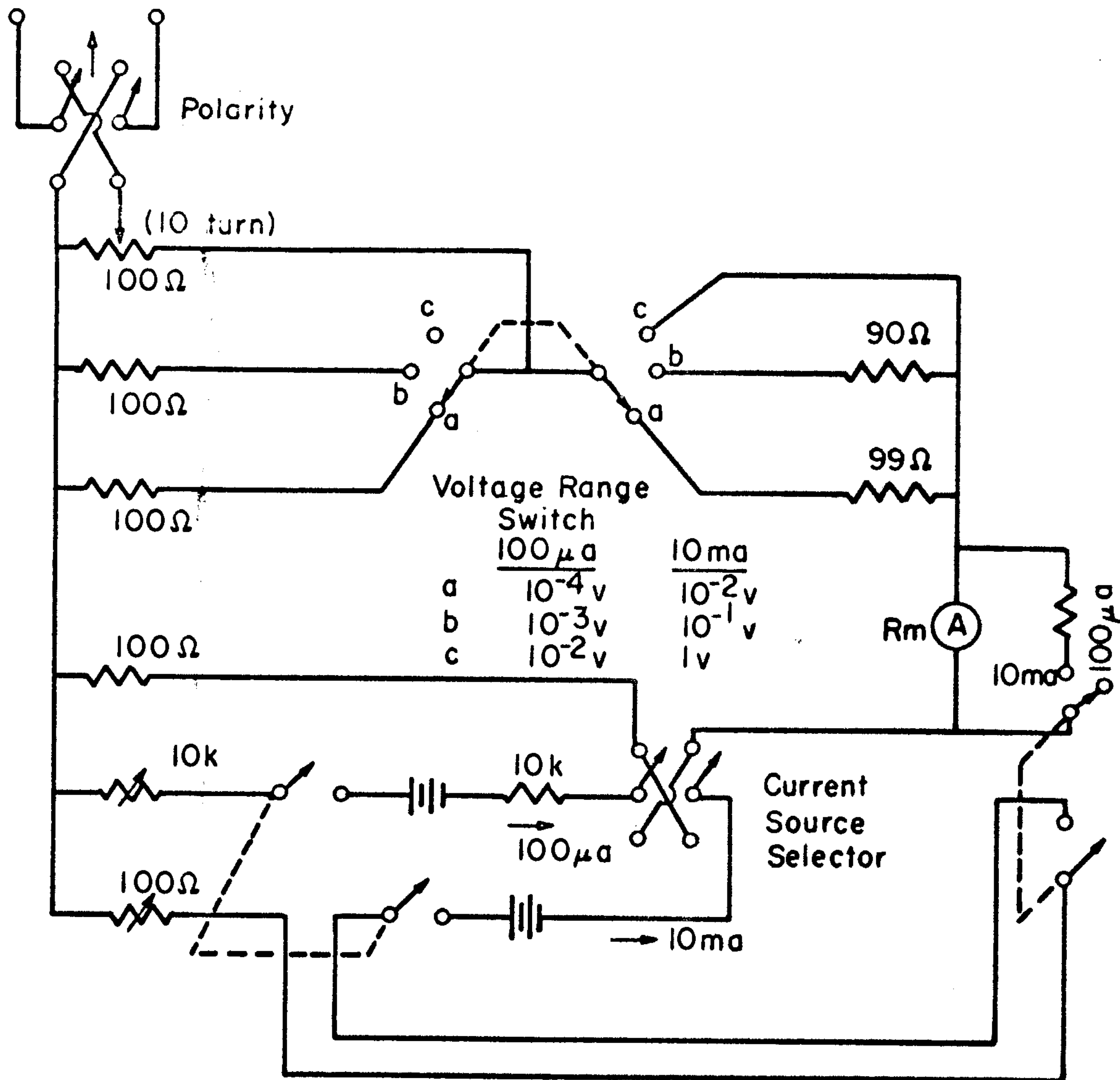


Figure B-4. Circuit of Potentiometer P_1

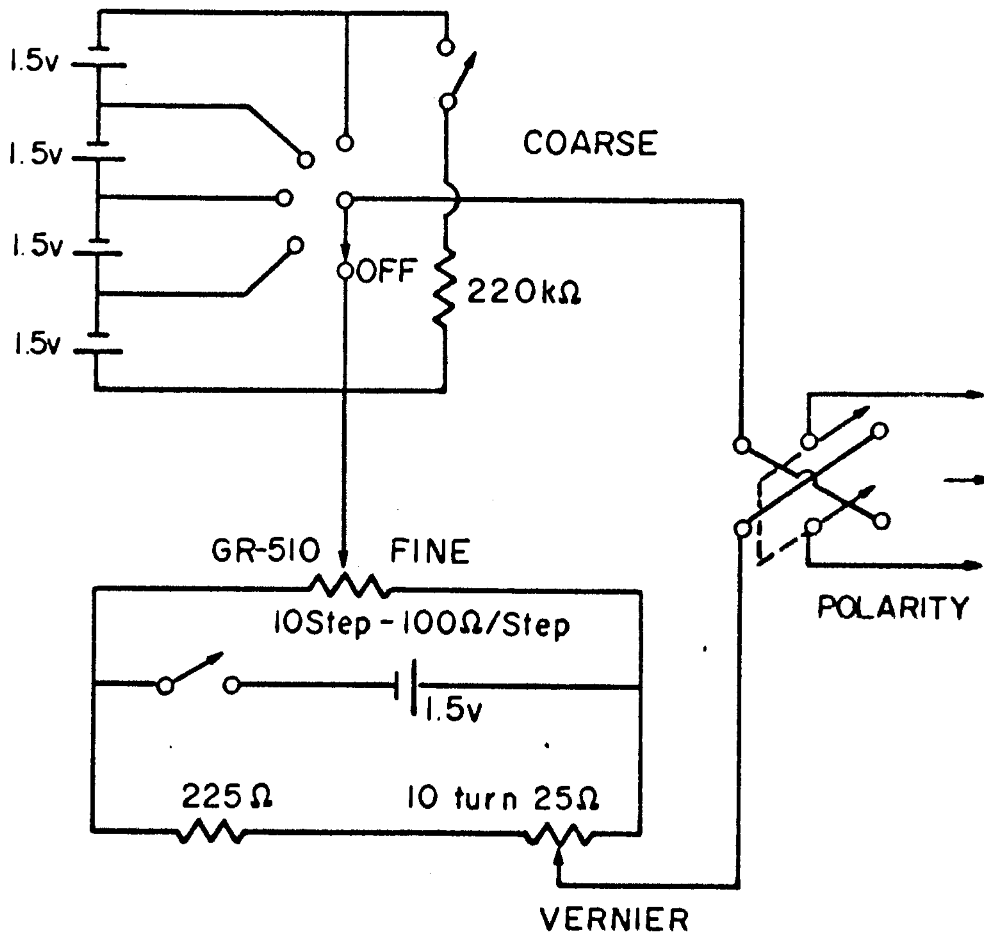


Figure B-5. Circuit of Potentiometers P_2 and P_3.

are powered by the 1.5 volt cells, and not the 100 V sources described in the reference.[78] All potentiometers were found to be stable after a 3 hour warm up.

In addition to the standard geometry, this bridge is designed for convenient operation with samples of the van der Pauw geometry.[79] This geometry is very useful for thin films of high resistivity and uniform thickness, and for thin anisotropic crystals of uniform thickness.[80, 81]

APPENDIX C. THE FILM THICKNESS MONITOR

The quartz crystal used for monitoring the film thickness is mounted in the vapor stream near the substrate. The deposited mass lowers the resonant frequency of the crystal linearly provided that the total change in mass is very small. Two derivations of the constant of proportionality are given below.

Consider the thin quartz plate, whose lateral dimensions are large compared to its thickness, shown in Fig. C-1. The 5Mc. crystals used here support a thickness mode shear wave. The equation of motion of a shear wave in an isotropic solid is given by

$$\rho \frac{\partial^2 v}{\partial t^2} = \mu \frac{\partial^2 v}{\partial z^2} \qquad \text{(C-1)}$$

where v is the particle displacement perpendicular to z, ρ is the mass density, and μ is the shear modulus. A proper solution of equation (C-1) is

$$v\ (z,\ t) = (Ae^{-jkz} + Be^{jkz})e^{j\omega t} \qquad \text{(C-2)}$$

where k is the propagation constant defined by

$$k = \omega/v_s\ , \qquad \text{(C-3)}$$

and the shear velocity, v_s, is given by

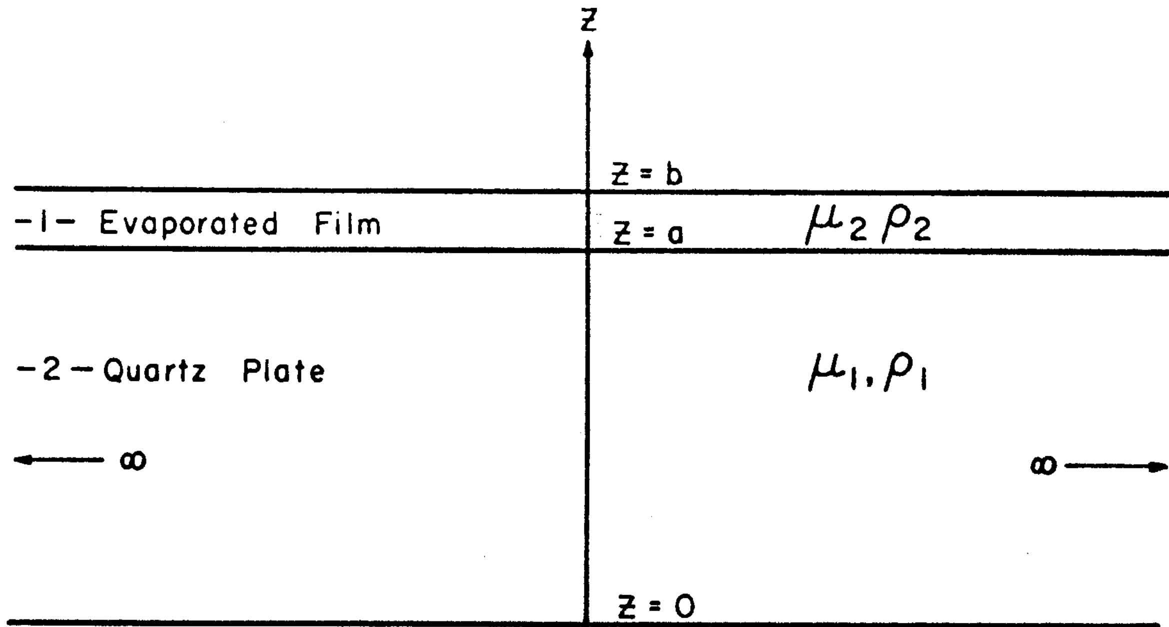


Figure C-1. Geometry used in calculating the resonant frequency of a coated quartz crystal.

$$v_s^2 = \frac{\mu}{\rho} . \tag{C-4}$$

The boundary conditions for such a system are discussed by Mason.(83) At the interface z = a, the stress component, T_4,+ and the displacement, v, must be continuous

$$T_4^1 \ (a) = T_4^2 \ (a)$$

$$\mu_1 \frac{\partial v_1}{\partial Z} \bigg|_{z=a} = \mu_2 \frac{\partial v_2}{\partial Z} \bigg|_{z=a} \tag{C-5}$$

$$v_1 \ (a) = v_2 \ (a) \quad . \tag{C-6}$$

At the free sides of the plate the stress $T_4 = 0$

$$T_4^1 \ (0) = T_4^2 \ (b) = 0$$

$$\mu_1 \frac{\partial v_1}{\partial Z} \bigg|_{z=o} = \mu_2 \frac{\partial v_2}{\partial Z} \bigg|_{z=b} = 0 \tag{C-7}$$

The resonant frequencies of this cavity are dependent upon the nature of the boundary conditions. The boundary conditions for the compound cavity with free surfaces are assumed to be ideal in the sense that any stresses at the free surfaces have been neglected along with any slip at the quartz crystal-evaporated film interface.

\+ T_4 is the only non-zero component of the stress tensor for this geometry, mode, and direction of propagation.

After applying these boundary conditions to solutions of the form given in equation (C-2), one obtains the following relation:

$$j \frac{k_1 \mu_1}{k_2 \mu_2} \tan (k_1 a) = \frac{1 - e^{2jk_2(b - a)}}{1 + e^{2jk_2(b - a)}} \quad , \qquad \text{(C-8)}$$

where it is recalled that $k_1 = \omega/V_{S1}$, $k_2 = \omega/V_{S2}$. Equation (C-8) is an exact solution for the allowed frequencies of oscillation of the compound cavity as a function of the film thickness, (b - a). The right hand side of equation (C-8) may be simplified by noting that $k_2 (b - a) = k_2 z' << 1$; i.e., the deposited film thickness is much smaller than the crystal thickness. The new frequencies of oscillation will therefore be only slightly perturbed from the natural resonant frequencies, ω_n, of the quartz plate. The natural resonant frequencies of the uncoated quartz plate may be calculated in a straightforward manner and are found to be

$$\omega_n = \frac{n\pi V_{S1}}{a} \quad (n = 1, 2 \ldots .) \qquad \text{(C-9)}$$

For the lowest allowed mode the left hand side of equation (C-8) may be expanded as

$$\begin{aligned} \tan (k_1 a) &= \tan \left(\frac{\omega_1 a}{V_{S1}} + \frac{\Delta\omega a}{V_{S1}}\right) = \\ &= \tan \left(\pi + \frac{\Delta\omega a}{V_{S1}}\right) \simeq \frac{\Delta\omega a}{V_{S1}} \end{aligned} \qquad \text{(C-10)}$$

Hence, equation (C-8) becomes

$$j \frac{k_1 \mu_1}{k_2 \mu_2} \frac{\Delta\omega a}{V_{S1}} = - jk_2 z' \qquad \text{(C-11)}$$

and the resulting frequency constant is seen to be

$$\Delta f = - f \frac{\rho_2 z'}{\rho_1 a} = - \frac{f}{a} \frac{dm_2}{\rho_1 A} \qquad \text{(C-12)}$$

where dm_2 is the amount of mass added, and A is the crystal area. The proportionality constants ($f\rho_2/\rho_1 a$) measured in this study for those sources which deposited films on equal areas of the crystal fit this dependence qualitatively; that is the constants are linearly proportional to the mass density of the deposited film. The result is also valid for crystals vibrating in the thickness-longitudinal mode.

This result agrees with that obtained by Behrndt[84] based on a more elementary derivation. If the crystal is excited in the thickness shear mode, the thickness corresponds to a half-wavelength of the fundamental frequency; equation (C-9). Differentiation of this equation with respect to the crystal thickness, a, and introduction of

$$da = \frac{dm}{\rho_1 A} \qquad \text{(C-13)}$$

yields

$$df = -\frac{f}{d} \frac{dm}{\rho_1 A} \qquad (C-14)$$

Since an antinode is formed in thickness-shear oscillations on the surface of the quartz plate, only the weight of the material deposited will affect the frequency provided that dm is sufficiently small. This means that a thin film of any material will result in the same frequency shift as the equivalent mass of quartz. This argument holds only for films which are sufficiently thin compared with the thickness of the quartz plate, and agrees with the result obtained by considering the film and quartz plate as a compound acoustical cavity. Behrndt[84] has calculated the maximum permissible df for 1% deviation from linearity to be

$$(df)_{max} = 5 \times 10^{-3} f_o \text{ (cps)} \qquad (C-15)$$

where f_o is the natural resonant frequency of the quartz plate.

The most dominant undesirable frequency shift in this method is caused by changes in temperature of the quartz crystal. These changes can usually be minimized by mounting the crystal on a cooled holder.

The block diagram of the complete film thickness monitor is illustrated in Fig. C-2 and the circuit diagram for the 5 Mc. oscillator used is shown in Fig. C-3.

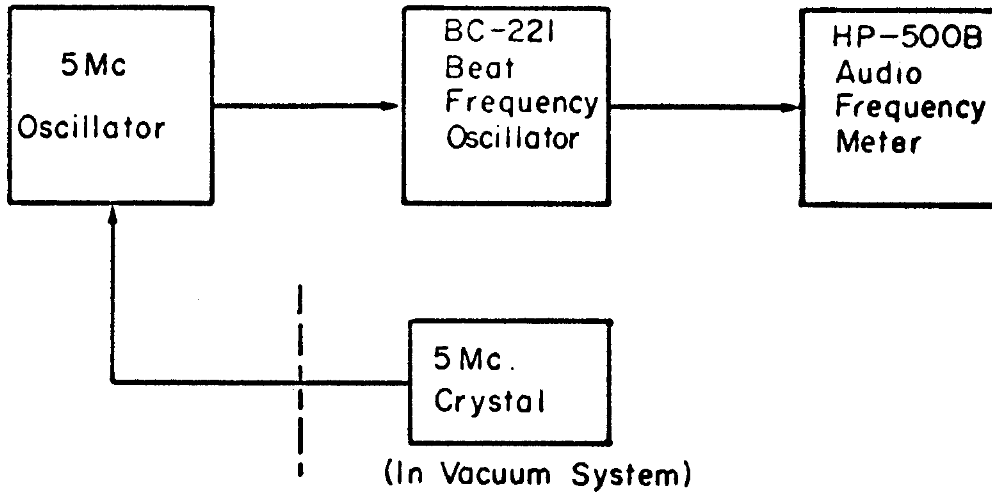


Figure C-2. Block Diagram of the Film Thickness Monitor

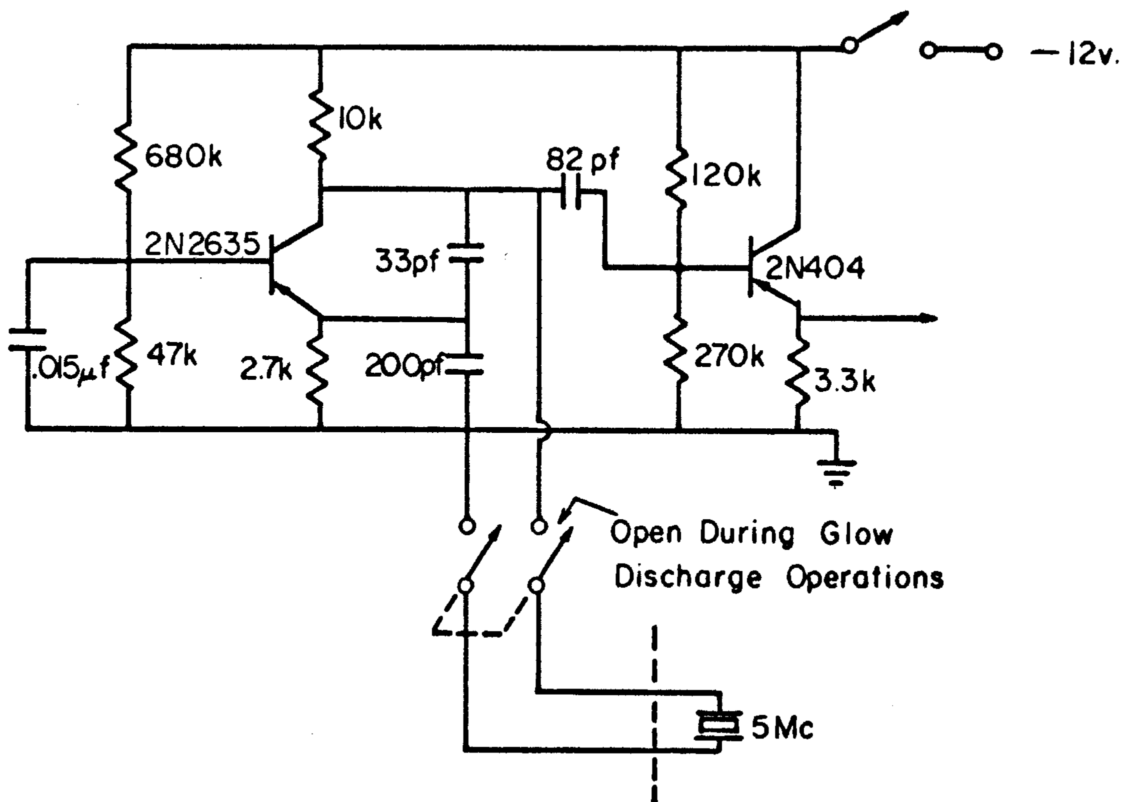


Figure C-3. Circuit Diagram of 5Mc. Oscillator

APPENDIX D. THE ELECTROLUMINESCENT LAMP

Electroluminescent light production is achieved by applying a high alternating electric field to a suitable phosphor. Typically, lamps are constructed by depositing a thin (.003 to .006 in.) layer of phosphor in a dielectric between two conducting surfaces, one of which must be transparent to the emitted light. A phosphor, such as ZnS, is deposited on a conducting glass substrate, and covered with an evaporated aluminum electrode. Fig. D-1 illustrates the measured emission spectrum of a green ZnS phosphor; the intensity of the emission is approximately linear with the frequency of the applied electric field.

At present EL lamps are of lower brightness than fluorescent lamps and therefore find a more restricted field of use where space is limited, and where low to medium brightness is needed, such as instrument panels. They will withstand intense vibration and temperature variation without failure. In these applications many small segments (0.05 - 0.25 cm^2) are used to make up alpha-numeric or bar-graph displays. Logic circuitry must be provided to switch each segment independently. To switch the EL lamp off, a higher impedance must be placed in series. The impedance characteristic of a 0.1 cm^2 lamp operating at 1Kc is shown in Fig. D-2. The lamp impedance may be varied considerably by suitable choice of frequency and area. The switch must be capable of withstanding the high voltage

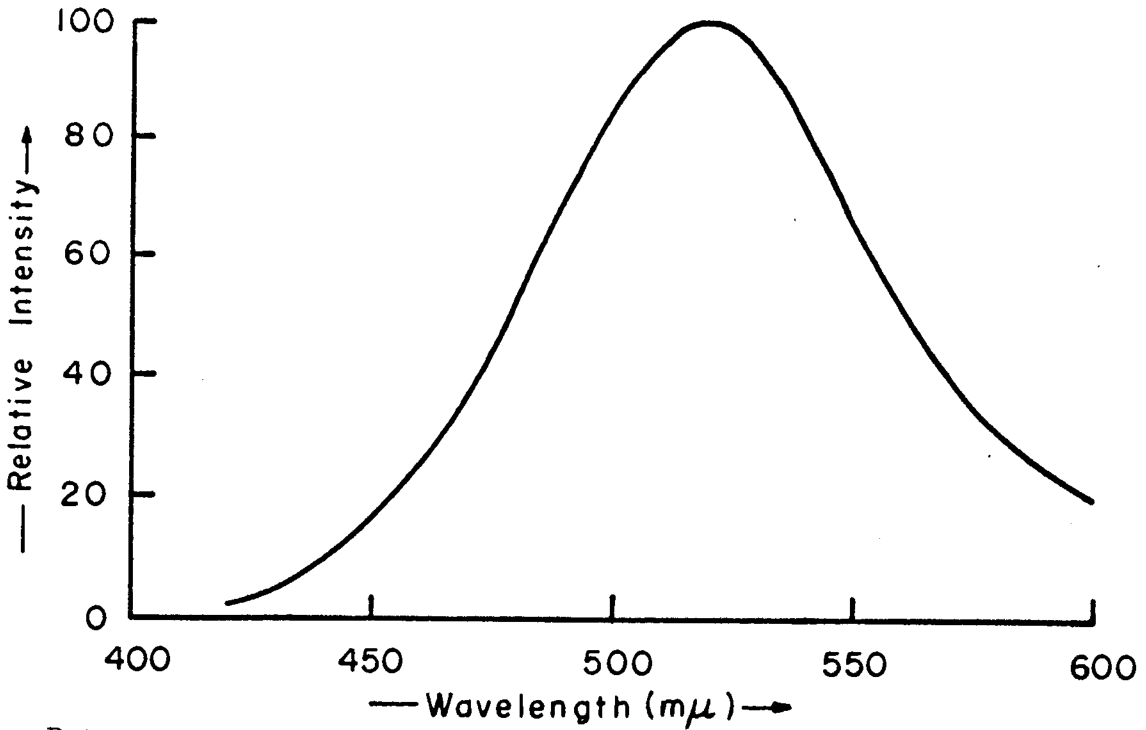


Figure D-1. Emission Characteristic for Green Phosphor used in This Study.

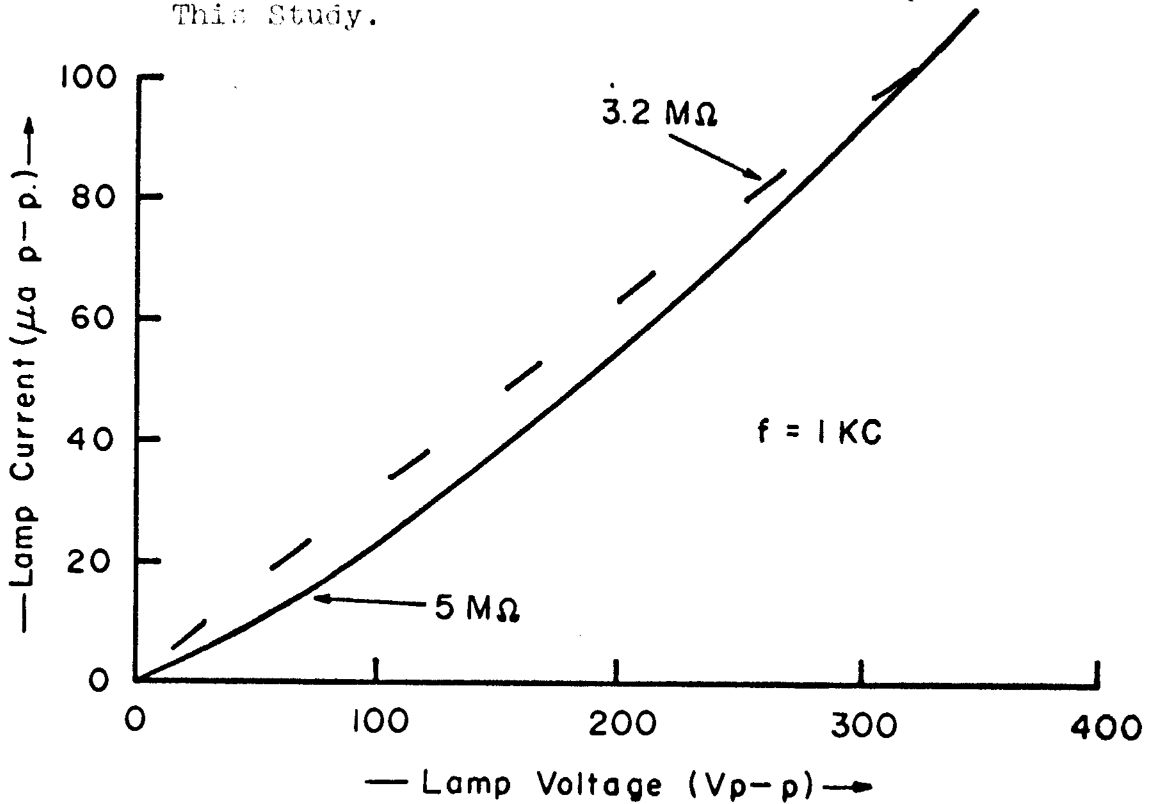


Figure D-2. Impedance Characteristic of EL Lamp. (Lamp area = 0.1 cm^2, c = 36 pf.)

(120 - 350 V) required; so that conventional transistors are unsuitable. Switching devices that have been used[85] are the silicon controlled rectifier, the incandescent-photo conductive gate, and the magnetic gate. All of these devices are large in size compared with the EL lamps and in contrast to the proposed high voltage TFT, are incompatible with its method of manufacture.

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