A MAGNETIC FIELD SENSOR ARRAY USING REDUNDANCY SCHEMES FOR DEFECT AVOIDANCE

by

Yves Audet

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M.Sc., University of Sherbrooke, 1992

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Name: Yves Audet

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Examining Committee:

Chairman: R.H. Stephen Hardy

Glenn H. Chapman
Senior Supervisor
Associate Professor

Richard F. Hobson
Associate Professor, School of Computing Science

Marek Syrzycki
Associate Professor

Ash Parameswaran
Internal External Examiner
Associate Professor

Stuart K. Tewksbury
External Examiner
Professor, Department of Computer Science and Electrical Engineering
West Virginia University

Date Approved: December 23rd, 1997

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ABSTRACT

Fabrication defects inherently present in any microelectronic process prevent the production of defect free integrated circuits larger than 5 cm^2 at reasonable cost due to the resulting low yield. For applications involving integrated sensor arrays, measurements of macroscopic size stimulus are often involved, requiring devices larger than conventional chip sizes. This thesis describes the design of a first prototype of a large area integrated magnetic field sensor array with built-in defect avoidance. The device employs a unique combination of redundancy schemes and restructuring strategies to avoid faulty circuit blocks originated by processing defects.

Two redundant design approaches are employed. Local redundancy schemes are used for the sensor grid, where the physical position of the spare sensor cell is important, whereas global redundancy schemes assumes the defect avoidance strategy of the readout circuits. A Monte-Carlo simulation algorithm, first compared to analytical calculations to verify its preciseness, was used to determine the resulting yield improvement of different local and global redundancy schemes.

A 3 mm by 6 mm prototype of the magnetic field sensor array was fabricated with the Mitel CMOS 1.5 μm process. To implement the redundancy schemes, the laser link technology was selected as the restructuring tool. In order to evaluate the effect of the restructuring on the device performance, a comparison software algorithm was developed. Aided with this algorithm, the difference between the sensor array responses of a working device measured before and after performing the laser restructuring is quantified. Finally, this new concept of redundancy, for the special case of yield improvement of sensor arrays, was proven successful even for restructuring schemes involving critical analog circuit blocks. As a result, a yield improvement of 56% was achieved on the prototype.

For my parents

Where we are ignorant, we withhold belief. Whatever annoyance the uncertainty engenders serves a higher purpose: It drives us to accumulate better data. This attitude is the difference between science and so much else. Science offers little in the way of cheap thrills. The standards of evidence are strict. But when followed they allow us to see far, illuminating even a great darkness.

- CARL SAGAN, *PALE BLUE DOT* (1994)

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LIST OF ABBREVIATIONS AND SYMBOLS

ABM	Automatic Banking Machine
Ain0	Differential analog input of the A/D multifunction board
Aout0	Programmable analog output of the A/D multifunction board
APS	Active Pixel Sensor
CCD	Charge Couple Device
Clk_c	Column shift register clock input
Clk_r	Row shift register clock input
CM	Current Mirror
CSC	Column Scanning Circuit
CSR	Column Shift Register
Da, Db	LAMSA reading lines
Da_sp, Db_sp	LAMSA spare reading lines
DD-DS	Double Drain/Double Source
Dout[0-3]	Digital output channels of the A/D multifunction board
D0_c	Column shift register serial input
D0_r	Row shift register serial input
D1, D2	MAGFET drains
L	MOSFET length
LAMSA	Large Area Magnetic field Sensor Array
LCD	Liquid Crystal Display
MAGFET	Magnetic Field Effect Transistor
MFL	Magnetic Flux Leakage
MSC	Magnetic Sensor Cell
Q74_c	Column shift register output of the 74^{th} flip-flop
Q26_r	Row shift register output of the 26^{th} flip-flop
Qb25_r	Row shift register inverted output of the 25^{th} flip-flop
Qb75_r	Row shift register inverted output of the 75^{th} flip-flop
R1, R2	LAMSA output load resistors
Res_c	Column shift register reset
Res_r	Row shift register reset
RSR	Row Shift Register
RSB	Row Scanning Circuit
RVLSI	Restructurable Very Large Scale Integration
S1,S2	MAGFET sources

SMU	Source Measurement Unit	
SPDT	Single-Pole Double-Throw switch	
SR	Shift Register	
WSI	Wafer Scale Integration	
W	MOSFET Width	
A	defect sensitive area	[μm^2]
Alpha	constant	
σ_r	standard deviation of the sensor grid response	[V]
α, α_{se}, α_{sl}	clustering parameter	
α_{grid}	sensor grid clustering parameter	
α_{cell}	sensor cell clustering parameter	
B	magnetic field amplitude	[Gauss]
B	matrix of coefficients	[Gauss/V]
$\vec{B}$	magnetic field vector	[Gauss]
B_x	magnetic field amplitude along the x axis	[Gauss]
C	number of columns in the sensor grid	
c	speed of light	[2.98 x 10^{10} m/s]
C_o	capacitance of the minimum size driver of a chain	[F]
C_l	load capacitance	[F]
Ce	fault density matrix	
D_{pix}	number of defective pixel	[%]
D_{cell}	number of defective cell	[%]
Δ	comparison parameter	[%]
δ	current imbalance	
δ_r	realtive current imbalance	
$\vec{F}$	Lorentz force vector	[N]
f	driver sizes ratio	
FaultTh	threshold value	
gr	number of circuit modules in a grouping	
$\Gamma(x)$	gamma function	
H_x	primary magnetic field amplitude along the x axis	[Gauss]
I	coil current	[A]
I_{D1}, I_{D2}	MAFGFET drain currents	[A]
Idn	NMOS drain current matching parameter	[%]
I_{ij}	Integral of the response of sensor cell[i,j]	[V-Gauss]

Ir_{ij}	Integral of the response of sensor cell[i,j] after restructuring	[V-Gauss]
I_{out}	current mirror output current	[A]
I_{ref}	current mirror reference current	[A]
λ	defect density per unit area	[μm^{-2}]
$\hat{\lambda}_{cell}$	average fault density per sensor cell	
$\hat{\lambda}_{grid}$	average fault density per sensor grid	
λ_{se}	sensor element fault density per sensor cell	
λ_{sl}	signal line fault density per sensor cell	
μ	magnetic permeability	
μ_p	hole mobility	[cm^2-V/s]
μ_n	electron mobility	[cm^2-V/s]
N	number of wire turns in a coil	
n	number of drivers, number of MSCs	
$Ngrid$	number of faults per sensor grid	
$P(x)$	defect probability distribution	
$P_{se}(x_{se})$	sensor element fault probability distribution	
$P_{sl}(x_{sl})$	signal line fault probability distribution	
$Prob$	probability number	
q	electron charge	[1.6 x 10^{-19} coulomb]
R	number of rows in the sensor grid	
R	coil radius	[m]
Ran	random number	
R_{cm}	current mirror output resistance	[Ω]
R_{load}	LAMSA output load resistance	[Ω]
R_{meas}	A/D multifunction board input resistance	[1 GΩ]
R_{msc}	MSC output resistance	[Ω]
r	MSC voltage response to a magnetic field	[V]
$\hat{r}$	average of the sensor grid response	[V]
r_o	MSC output voltage without magnetic field	[V]
t_d	reading bus discharging time	[s]
t_p	MSC response stable time	[s]
V	variance of a fault distribution	
V_D	drain voltage	[V]
V_{DS}	drain source voltage	[V]
$V_{Da,Db}$	LAMSA output voltage	[V]

V_G	applied gate voltage	[V]
VGref	external gate reference voltage	[V]
V_{GS}	gate source voltage	[V]
V_{in}	driver input voltage	[V]
V_{out}	current mirror output voltage	[V]
V_{ref}	current mirror reference voltage	[V]
V_T	MOS threshold voltage	[V]
Vtn	NMOS threshold voltage matching parameter	[%]
$\vec{v}$	charge velocity vector	[m/s]
X	matrix of the magnetic field values	[Gauss]
x	number of defects	
x_{se}	number of sensor element faults	
x_{sl}	number of signal line faults	
Y	matrix of the measured responses	[V]
Y_{cell}	yield of the MSCs	
Y_{cm}	yield of the current mirrors	
Y_{col}	yield of the column scanning circuits	
Y_{row}	yield of the row scanning circuits	
Y_{pix}	yield of the pixels	

Chapter 1

Introduction

1.1 The Increasing Complexity of Integrated Circuits

Over the past twenty years, the industry of microelectronics has experienced an unprecedented level of growth unparalleled by any other field of commercial activities. Forecasts for the year 2000 predict that the world market of microelectronics will surpass the automobile, chemical, and steel industries in sales volume. Refinements in techniques and tools of microelectronic processes, from the seventies to the nineties, have permitted an increase in the level of integration from 10^3 transistors/chip to 10^6 transistors/chip[1], allowing for the fabrication of circuits of increasing complexity at reduced costs. Today, at the dawn of the information age, when the computer industry is merging with electronic media to form cyberspace, demand for more powerful integrated circuit systems of various uses has never been so imminent.

Microelectronic systems are now found in a myriad of industrial and consumer products: calculators, computers, automobiles, household appliances, robotics, biomedical equipment, etc. They gather, process, transmit and store data; with the recent event of integrated microsensors they can now "feel" the physical environment and interact with it through microactuators. The integration of these newly developed sensors and actuators onto conventional chips has created a new class of microelectronic systems. One field of interest representing a great potential of applications is sensor systems for imaging. Among the most popular mediums for imaging are: infrared[2], visible, X-ray[3] radiations and magnetic fields[4]. This particular class of sensor systems requires an array of identical microsensors to form an image: since the application usually involves images of macroscopic sources, integrated sensor arrays of more than 5 cm^2 are often needed, representing chip sizes larger than those conventionally produced. Also, in the case of high sensitivity photonic imaging sensors, the pixel element requires an optimal size in order to produce a detectable signal, resulting in a fairly large chip, especially when higher spatial resolution and on-chip processing are needed. Fabrication of large chips always represents risks for the industry. It is well known that as the chip size increases, its yield decreases almost exponentially[5], due to the occurrence of defects inherent in any microelectronic process, resulting in reduction in the profit margin of the fabrication run.

1.2 Wafer Scale Integration for Large Area Sensor Arrays

In the seventies, researchers started to explore the possibilities of expanding the size of chips to integrate more powerful and complex microelectronic systems. No limit in chip size were foreseen, and attempts of using the whole wafer as a single chip were even made[6]. A new field of research, called Wafer Scale Integration (WSI), was born. Since

that time, investigations have been carried out dealing with new design techniques involving redundant architecture approaches and restructuring tools to overcome faulty circuits generated by process defects. Most of the research done in the WSI field is aimed at CMOS digital systems, these being the major class of circuits benefiting from chip size increases, resulting in more processing capabilities and more memories on one chip. Due to its low power consumption, the CMOS technology is also the logical choice for large chips, since heat dissipation can easily become an issue for integrated systems comprised of a million transistors.

In the case of large area sensor and actuator arrays, actual successful products like CCD (Charge Coupled Device) and APS (Active Pixel Sensor) arrays[3][7] for photonic imaging, the digital micromirror device for projection display[8] and the capacitor array device for finger print scanning[9] are fabricated at low yield without any redundant aspect for yield improvement. Moreover, past magnetic sensor arrays of the size of conventional chips (9.2 by 7.8mm) have been fabricated without defect avoidance schemes[12]. Even at this moderate size, these arrays lose columns and rows due to single point defects. For these integrated systems, profits are based on limited special application niches where prices are very high. Also, in the case of CCD arrays, the number of microsensors within the array is high enough that even chips having complete rows or columns of defective pixels find buyers, since compensation of dead lines is achieved by image processing. However, many types of large area sensor and transducer arrays would find a market or increase their sales volumes by reducing their production costs through post-processing yield improvement. This thesis will explore the application of redundancy schemes to a large area magnetic field sensor array.

1.3 Thesis Objectives

The work presented in this thesis deals with all the aspects related to the design and the post-processing yield improvement of a Large Area Magnetic field Sensor Array (LAMSA). Two important aspects are investigated in detail. First, the most effective redundant design strategies are determined through yield simulation. Second, effects of the restructuring schemes on the electrical characteristics of the LAMSA are experimentally evaluated. From the simulation and the experimental results, the feasibility of a LAMSA product is assessed.

Some of the restructuring techniques and tools developed for the WSI field are used or readapted here for this particular case of sensor array system. Especially, the laser link technology[10] which is the key tool to restructure circuit blocks or elements for defect avoidance. To avoid being too general without proposing any practical solutions for such an applied problem, it has been chosen to explore the fundamental aspect of the redundant design and restructuring of sensor arrays on a real device. Hence, implementation problems are readily discovered and fed back at the design level. Nevertheless, fundamental architecture and design approaches will remain valid for other types of sensor arrays at the expense of a few technical modifications.

Experimental sensor arrays with redundancy have been build in the past, mostly by the Simon Fraser University microelectronic research group. This thesis extends that work into two main areas. First, yield modeling of mixed signal designs such as sensor arrays has never been done in the past. This particular device relies on two types of redundancy for yield improvement. Local redundancy for the sensing elements since the position of the spare is critical for the device specification, and global redundancy for the peripheral

circuitry where the positioning of the spares is less critical. Second, the effect of the laser link restructuring technology on analog circuit cell has never been studied. This thesis tackles this issue on the particular case of a sensor array by comparing the magnetic field response and the maximum frequency of operation of the device before and after laser link restructuring. To realize this comparison, the laser link tool is employed to discard initial functioning blocks and connect corresponding spares. The design allows for the full operation of the sensor array without requiring post-processing laser linking steps. In a production environment, laser linking would only be used for defect avoidance.

1.4 Organization of the Work

Chapter 2 begins with a review of the history of the WSI field of research and presents the previous work realized on wafer scale transducer arrays. Next, the physics of the magnetic field sensing mechanisms are introduced along with a description of the basic principles of operation of the LAMSA. Since redundancy plays a major role in the feasibility of this sensor system, the two types of redundancy employed for the LAMSA design, local and global, are described. Redundancy is obviously useless without the capability of redirecting the signal lines to the spare circuit blocks. Therefore, the restructuring tool selected for the LAMSA, the laser link technology, is presented with emphasis on the parameters employed for the Mitel CMOS 1.5μm process, the technology chosen to fabricate this device. In chapter 3, a novel double drain/double source Mosfet, developed exclusively to improve the defect immunity of the LAMSA, is characterized. Also, the design of every circuit block of the sensor system is described and, aided by SPICE simulations, the complete electrical analyses of the circuits are performed.

Chapter 4 introduces the basic concepts of wafer defect statistics, followed by a description of an analytical calculation method of the sensor grid yield as a function of its defect density, for different redundant design schemes. Since the analytical method is limited to calculation on identical circuit cells, a Monte-Carlo simulation algorithm is developed to determine the overall LAMSA yield improvement of various redundancy schemes and restructuring strategies. This algorithm is first compared to analytical calculations, in order to verify its preciseness.

In chapter 5, The LAMSA functionality is experimentally verified and the sensor grid response is measured. From the calibration algorithm of the sensor grid response, a comparison parameter is defined and is first employed to evaluate the repeatability of the sensor grid measurements. Using this comparison parameter, the effects of the LAMSA restructuring schemes on the sensor grid response and the maximum frequency of operation are quantified in chapter 6.

The LAMSA has many potential applications such as magnetic field mapping for detecting fringing fields in electric motors and defects in steel piping[11], as well as acting as a sensing medium in compliant tactile sensor arrays[4]. Chapter 7 focuses on some of these applications and illustrates their concepts from magnetic field mappings measured experimentally.

Chapter 8 summarizes the contribution of this thesis and, from the simulation results, describes the important features of a fault tolerant design of large area sensor array systems. Also, design modifications that would readily improve the performance of the LAMSA are discussed. Finally, given the microelectronics state of the art and the new

market requirements at the end of this century, the possible impacts of the techniques developed in this thesis are forecast.

Chapter 2

Use of Redundancy in the LAMSA Design

The Large Area Magnetic field Sensor Array (LAMSA) uses a combination of magnetic field sensor cells, readout circuits and a laser link interconnection technique to build a fault tolerant sensor device. Similar to wafer scale integrated circuits, this design also requires levels of redundancy to restructure faulty cells or circuit blocks after fabrication, thus increasing the production yield of the sensor system. This chapter first summarizes the early efforts in the field of wafer scale integration leading to the development of redundancy strategies and restructuring tools. Then, the LAMSA basic principle of operation, its redundant design features and the restructuring tool employed, the laser link technology, are presented. Exhaustive simulations of the readout and sensor grid circuits and the experimental characterization of the magnetic field sensor cell are covered in chapter 3.

2.1 Overview of the Redundant Design Strategy

2.1.1 History

Large integrated circuits were introduced in the mid 1960s in an effort to increase chip performance and functionality with the available processes. The first prototypes used a full wafer, hence the name Wafer Scale Integration (WSI) was given to this field of research and development. An example of early work in the field is the 8 by 8 parallel multiplier implemented on a 1.5 inch TTL wafer[13]. The circuit was designed at Hughes Aircraft Company and fabricated by Texas Instrument in 1970. Hughes early WSI effort resulted in a total of 30 different wafer designs fabricated in a variety of technologies and wafer sizes, TTL and ECL on 1.5, 2.25 and 3 inch wafers. Problems encountered in the fabrication of three layers of metallization, in packaging and in the design phase due to immature computerized tools, led Hughes to abandon its WSI projects.

Trilogy Systems Corporation[14] in the early 1980s conducted a largely publicized WSI effort. Their ambitious project was aimed at implementing a mainframe computer on a few wafers using ECL circuits. New approaches to wafer yield, heat management, circuit connection, circuit and system design, testing and CAD tools were required, representing an important development investment. In mid 1984, the project was no longer economically viable and was abandoned.

An alternative approach used VLSI circuits and CMOS process, providing circuits of relatively high speed with low power consumption, allowed the WSI concept to regain in popularity by easing the inherent problems of interconnection delays and power consumption. Meanwhile, pursuing a project launched at the end of the 1970s, the MIT Lincoln Laboratories successfully designed and fabricated different complex WSI CMOS

processor circuits[15]. They introduced a concept called restructurable VLSI (RVLSI), which employed the laser link technology to connect and/or disconnect multilevel metal patterns on a wafer. Extensive computer tools were developed to support the design and the fabrication of RVLSI circuits.

Inova Microelectronics Corporation[16] was the first to commercially exploit WSI concepts and the CMOS process. In 1988, they began the fabrication of 1 Megabit CMOS static RAM devices using laser cutting to restructure circuits. Two years before, Westinghouse Electric launched a WSI program for the development of complete signal and data processors. The project made use of, and expanded the Inova technology base. It included a new packaging scheme and was not committed to just one device manufacturing strategy.

2.1.2 The legacy of the WSI era

Today, in this wave of submicron CMOS processes fabricated on six, eight, ten and twelve inch wafers, the term WSI becomes less appropriate given the technical difficulties that would arise from designing, processing, packaging, handling and cooling such a giant microelectronic system. However, most of the redundancy techniques and restructuring tools evolved from the WSI efforts are still valid for the fabrication of large area systems[1] such as in the particular case of transducer arrays presented in this thesis.

The possible success of the LAMSA design relies on its capacity to overcome defects inherent in any fabrication processes. Therefore, a redundant design is required. The redundant schemes of the LAMSA design must fulfill two specific tasks. They must

1. The term large area system refers to a complete microelectronic device occupying a die size of more than 5 cm^2.

ensure that the sensor grid conserves a minimum spatial resolving power throughout the entire sensing area, and replacement blocks must be provided for the readout circuitry. Thus, two redundancy techniques evolved from the WSI efforts are utilized for the LAMSA redundancy strategy. One, referred to as local redundancy, is employed where the physical position of the replacement element is important, such as the spare pixels of the sensor grid. The other, termed global redundancy, defines a scheme where entire circuit blocks are duplicated at least once to allow their replacement. The physical position of the spare blocks is generally not important. This scheme was the one employed in the successful RVLSI systems built at MIT Lincoln Laboratories and is used for the readout circuitry of the LAMSA.

These redundancy schemes define the location and the amount of spare circuits and also determine the routing of the metal interconnection lines. However, to physically implement the schemes by disconnecting the defective circuits and connecting the spares, a restructuring tool is required. Following the successful path opened by MIT RVLSI work, the laser link technology is employed in this thesis to restructure the LAMSA circuits.

2.1.3 Previous works on wafer scale transducer array

Among the previous works exploring this field, Chapman, Parameswaran and Syrzycki[17] laid out the basis of a design effort aiming at wafer scale transducer arrays involving a micromachining step in the transducer fabrication. They reported on the designs of a wafer scale thermal scene generator[18] and a wafer scale visual to thermal converter[19][20]. They opted for the laser link technology as the restructuring tool. Although the redundancy aspect and the restructuring issues of the designs were described,

no experimental data were presented on the effects of the redundant architectures and the restructuring schemes on the device performance. Later the same team reported experimental results on a test vehicle for a wafer scale thermal pixel scene generator[2]. The test chip comprised eight transducers and their corresponding control and latching circuitry. They employed the laser link technology to interconnect the transducer and its corresponding circuits one at a time for test purposes. The approach taken in this thesis does not require any laser interconnection to initially operate and test the full sensor system. Laser links and cuts are only performed to isolate defective circuits and connect the spares. Hence, the effects of laser restructring of different circuits on the response and the functionality of the LAMSA can be determined by characterizing the device when operating with its initial circuits, and when operating with the laser restructured spare circuits.

2.2 LAMSA Principles of Operation

2.2.1 Physics of the magnetic field sensor

The physics principles ruling the magnetic field sensors comprising the sensor grid of the LAMSA are illustrated in Figure 2.1. In the presence of drain-source voltage, when sufficient biasing is applied to the gate of the double drain MOSFET (MAGFET)[21], carriers of the inversion layer generated in the *x-y* plane are deviated by a magnetic field component in the z direction according to the Lorentz force:

$$\vec{F} = q\vec{v} \times \vec{B} \tag{2.1}$$

where q is the carrier charge, $\vec{v}$ its velocity and $\vec{B}$ the magnetic field. This effect results in a lateral deflection of the carriers traveling from the source to the drains, which in turn gives rise to a Hall voltage in the x direction, perpendicular to the current flow. At

equilibrium, the Hall voltage balances the Lorentz force and annihilates the carrier deflection. However, in the vicinity of the drains, the Hall voltage vanishes due to the short circuit effect, allowing the Lorentz force to establish the carrier deflection mechanism. As a result, the current collected by one drain, I_{D1}, increases at the expense of a reduction in the current collected by the other drain, I_{D2}, since the total MAGFET current is independent of the magnetic field. Experimentally, this effect is quantified by defining the current imbalance parameter, δ, as follows:

$$\delta = \frac{I_{D1} - I_{D2}}{I_{D1} + I_{D2}} \tag{2.2}$$

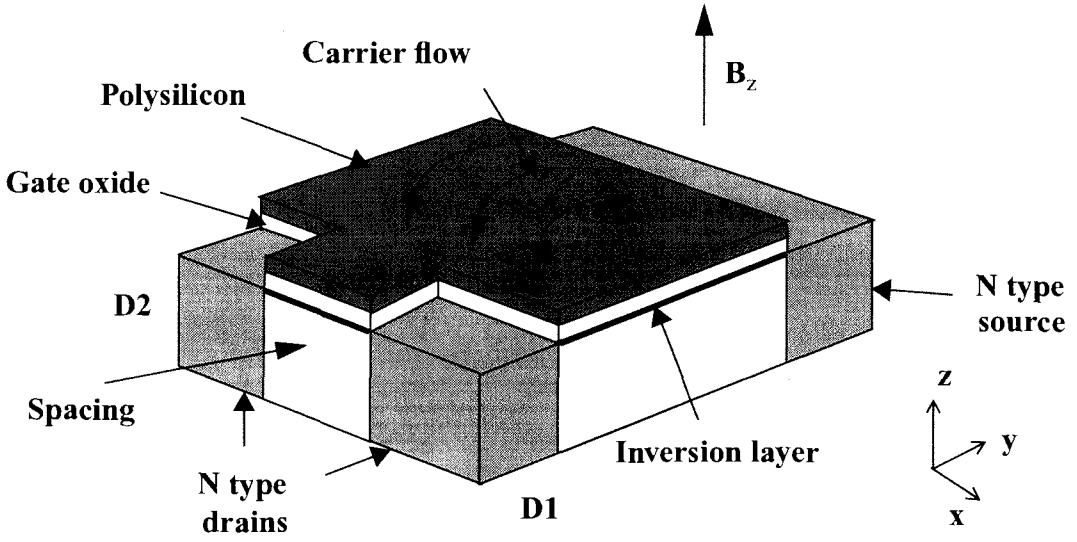

Figure 2.1 Schematic view of a N type MAGFET.

Due to the short circuit effect in the vicinity of the drain diffusions, it is impossible to deduce an accurate analytical relation expressing the current imbalance as a function of the magnetic field strength. Numerical modeling is required to obtain information on the electrical equipotential lines and the current line trajectories of the inversion layer as a function of the magnetic field strength and the geometrical aspect of the devices[22]. Combining simulation results to analytical expressions, the sensor can be characterized with good accuracy. A recent model developed by Lau et al[23], attributes the sensitivity

of the MAGFET in the linear region to an increase of the drift velocity due to the roll-off of the Hall voltage and a shift of the drain saturation voltages in the saturation region. In the latter case, experimental data indicated a shift of roughly 2%/Tesla on each drain.

It will be shown in chapter 3 that from a design point of view, there are advantages in modifying the MAGFET to have both the source and the drain split. It allows the merging of several MAGFETs together as presented below in the inset of Figure 2.2. Experimental results in section 3.1.3 show that the double drain/double source merged MAGFET acts similarly as the regular single source MAGFET.

2.2.2 Basic functional description of the sensor array

Figure 2.2 shows the floor plan of the LAMSA. The magnetic field sensor grid is comprised of a matrix of rows and columns of double drain/double source N MOSFET, of square geometry. Two or more double drain/double source MOSFETs can be merged together and share the same drains and gate as shown in the inset of Figure 2.2. Therefore, the number of drain and gate contacts required is reduced, resulting in a denser sensor array and a reduced probability of bad contact occurrence. This novel double drain/double source MAGFET with merging capability, has been developed expressly for the LAMSA applications. It will be presented and characterized in chapter 3.

The magnetic field response of each MSC is read in a raster scan fashion, synchronized by column and row shift registers. Signal lines directing each MSC to the cascode current mirror (CM), used as an active load, are activated by Single-Pole Double-Throw analog switches (SPDTs) which are controlled by the column shift register. A differential amplifier (amp.) is used to amplify MSCs' responses.

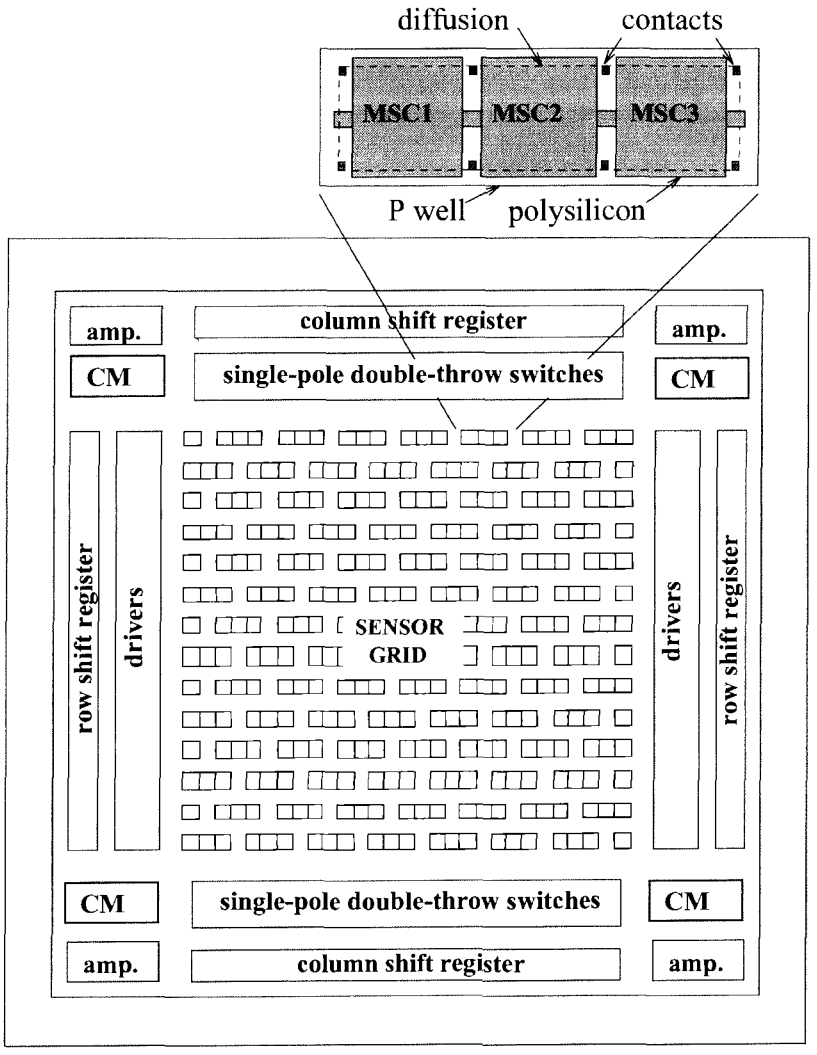

Figure 2.2 Floor plan of the LAMSA. Inset: a merged triple sensor cell subarray.

Figure 2.3 shows current paths commanded by the column shift register, which enables the reading of the magnetic field response of the sensor MSC2. MSC2 is the middle sensor cell of a merged triple sensor cell subarray. Note that this subarray can be located anywhere in the grid as illustrated in Figure 2.2. A maximum subarray length of three sensor cells avoids the occurrence of large dead areas in the grid due to gate oxide shorts, which can cause the loss of an entire subarray. The proper row to be read is selected by the outputs of the row shift register which turns "on", via a driver, the gates of all the MSCs in the entire row. By propagating a "0" at the outputs of the column shift register

which are initially set to "1", the current flowing from the active load is directed by the SPDT switches to only one MSC at a time, thus performing a sequential reading of the sensor grid. In the case of Figure 2.3, the presence of a magnetic field will produce a difference between the amplitude of currents I_{D1} and I_{D2} flowing through drains D1 and D2 of MSC2, creating a voltage difference at the outputs of the active load. This voltage is accessible through lines Da and Db feeding the inputs of a differential amplifier.

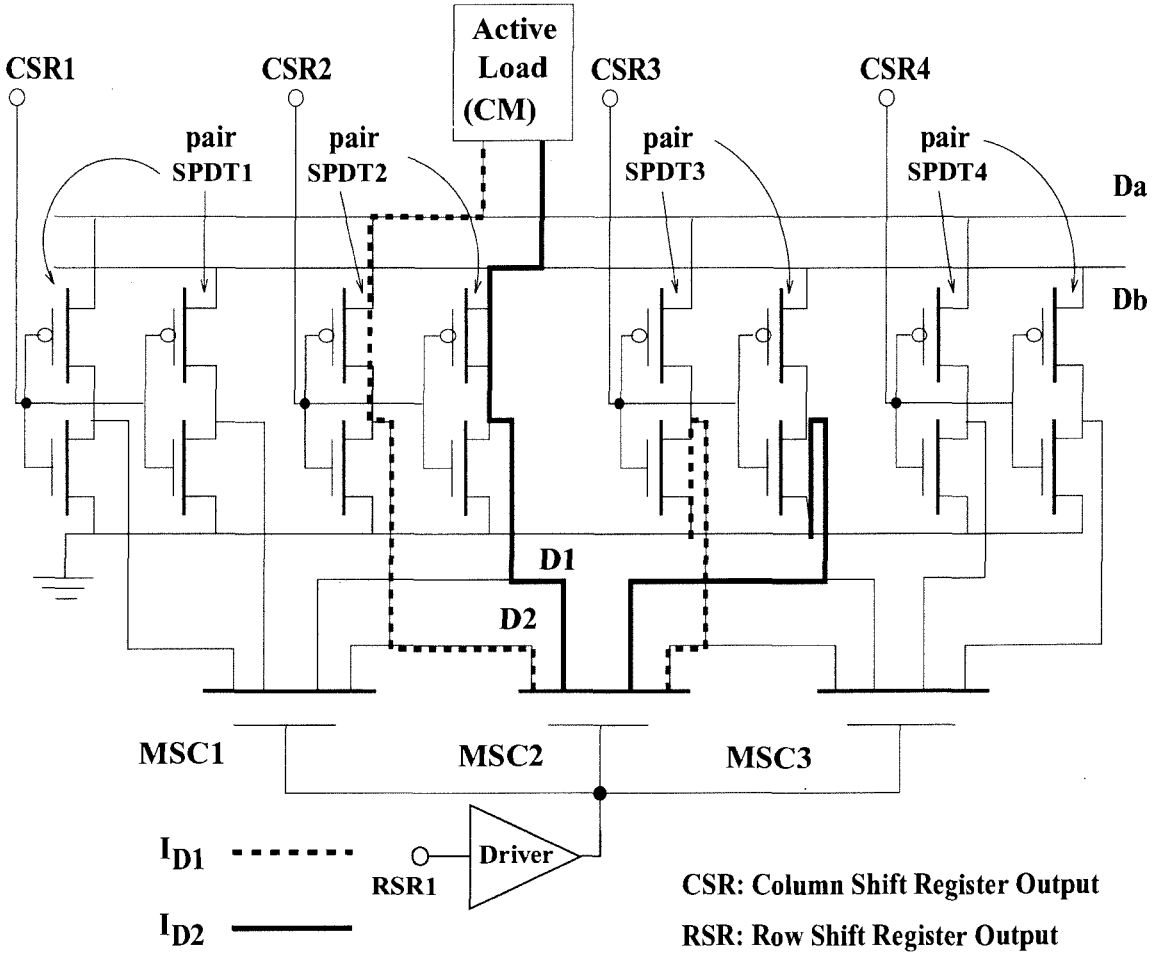

Figure 2.3 Current paths involved in the reading of the sensor cell MSC2. CSR1 and CSR2 are set to "0" while CSR3, CSR4 and RSR1 are set to "1".

2.3 Redundancy Levels

The philosophy of defect avoidance of the LAMSA is to create a design targeting the maintenance of a specified sensor resolution at all points throughout the grid. The design will allow for some local failures; however, it must be resistant to defects that could eliminate large areas of the sensor grid or disable the surrounding readout circuit.

2.3.1 Control circuits global redundancy

As mentioned in section 2.1.2, the term global redundancy refers to redundant circuit blocks of the same type where one or many of them can be connected to form parts of a working system without any dependence on the physical position of the selected blocks on the chip. As shown in the floor plan of Figure 2.2, column and row shift registers, buffers and SPDT switches surrounding the sensor grid are duplicated once, providing a global redundancy of 2:1. A previous study on a magnetic field sensor array of 7.9 by 9.2 mm fabricated without redundancy has reported a yield of 90 to 95% on a current mirror used as active load[12]. Indeed the active load is a critical part of the sensor system and small variations in its parameters can inhibit the response of the entire sensor grid. Based on these results, the active load used in our system is duplicated three times, providing a global redundancy of 4:1. The same amount of spare circuits is employed for the differential amplifier.

2.3.2 Sensor grid local redundancy

Conversely, the sensor grid redundancy strategy can not be global, since each physical region of the grid needs a certain number of working cells. Figure 2.4 presents an enlargement of the sensor grid. Here, at the pixel level, a local redundancy of 3:1 is

defined, meaning that at least one MSC out of three in the same pixel block has to be non-defective in order to consider the pixel functional. For a given application, MSCs are fabricated at twice the linear minimum resolution of the final system target. With yields of individual MSCs easily being 99%, it follows that most of the grid will have more resolving power than the minimum amount required. Although defect clustering may lead to a few sites with no resolution, this can be overcome by image processing.

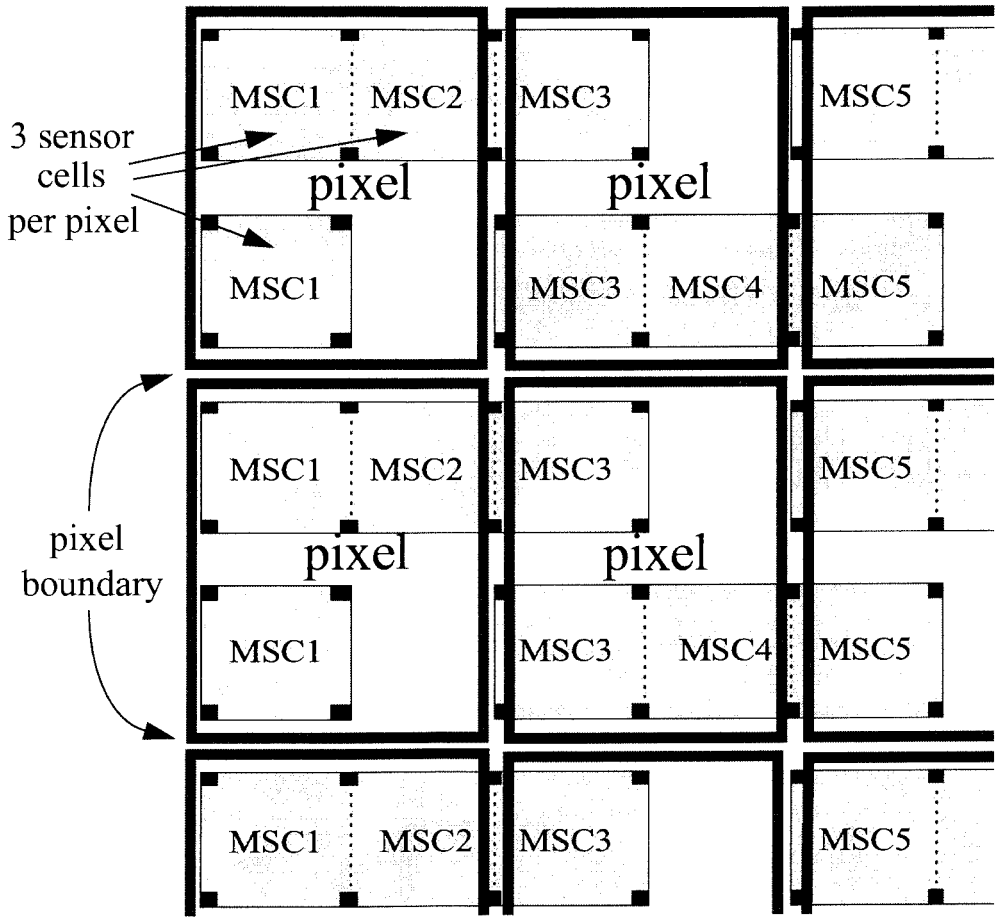

Figure 2.4 Detail of the pixel definition.[1]

1. Open spaces of the same size as the sensor pitch are inserted between the sensor subarrays of a same row, to provide a uniform pixel pitch across the grid in the case of small sensor geometries. For instance, from the design rules of the Mitel CMOS 1.5 µm process, the smallest achievable sensor pitch is 6 µm while the minimum space required between two adjacent subarrays is 5 µm.

To increase the sensor grid yield, another local redundancy scheme is added at the sensor cell level. Figure 2.5 shows the signal line redundancy pattern for the sensor grid. Here, for each MSC, the redundancy scheme allows for one spare drain line for a pair of drains and one spare gate line. In the event of open and shorted signal lines, through a combination of laser links and cuts, it is possible to reroute a drain line or a gate line to its spare, thus preventing any signal line failure from eliminating a whole column or row of sensors. Also, bad contacts on a signal line can be avoided by laser linking the spare signal line. Detail of the rerouting method will be given in chapter 6.

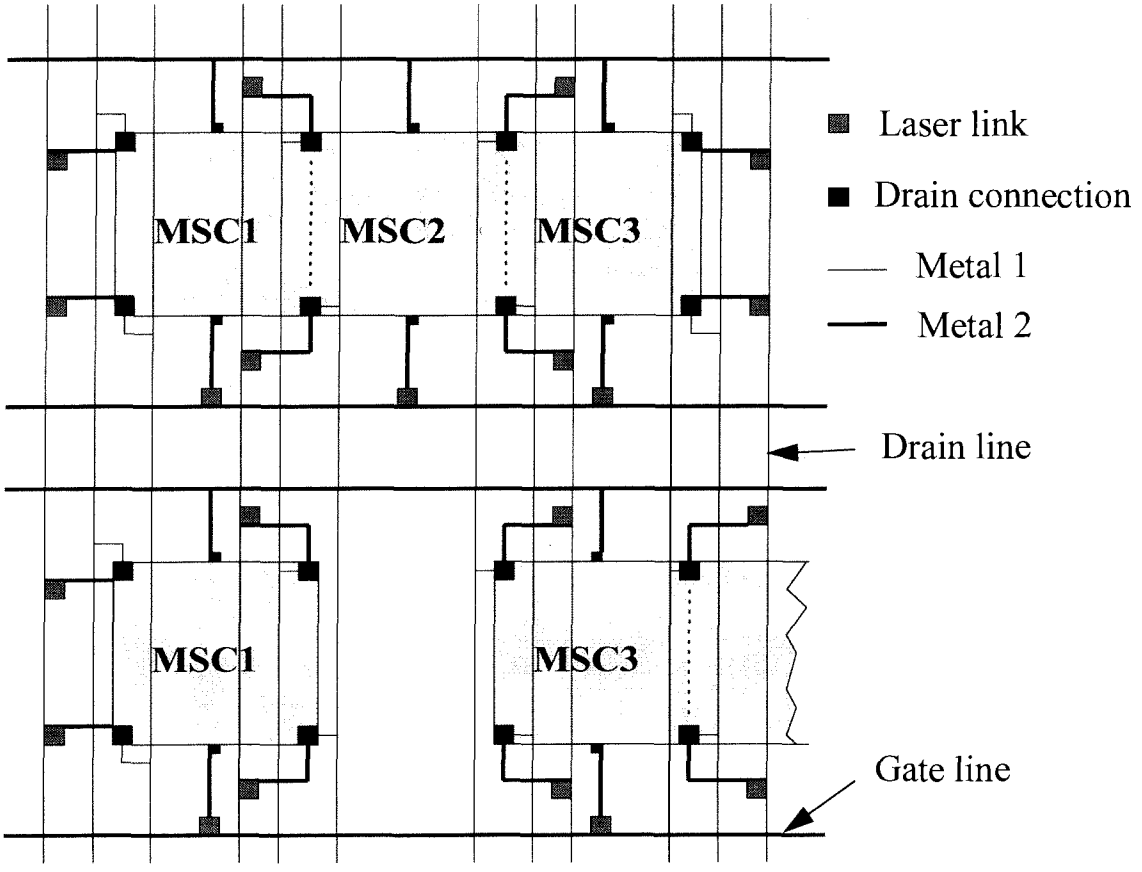

Figure 2.5 Detail of the signal line redundancy scheme for sensor grid.

2.4 The Laser link Technology as a Restructuring Tool

Although active switches are often used in experimental design, compared to laser link structures, they have the disadvantage of being more resistive by a factor of 10 to 40[26] and requiring gate connections, thus introducing delays, larger impedances and extra control circuitry. In many digital applications, these drawbacks do not prevent the restructuring of working circuits. However, in mixed signal systems, such as sensor arrays, highly resistive links can severely degrade the device's analog circuit performance. Moreover, for a targeted array size, the switch area overhead forces an increase in the chip size, reducing the yield and increasing the production costs. For all of these reasons, the laser link technology has been selected as the only restructuring tool employed for the LAMSA. The laser link apparatus used at Simon Fraser University has been extensively described in previous theses[24], [25]. Therefore, to avoid repetition of this well documented technology, only a brief survey of the technique follows, with emphasis placed on the important parameters employed for the LAMSA chip.

2.4.1 Mitel 1.5 μm links and cuts

The heart of the laser link system consists of an argon laser of variable power, 0 to 5 W. On the laser beam path, an electro-optic shutter sets the pulse duration. The chip positioning is assumed by an x-y table using linear induction motors, where the position is monitored by laser interferometry to an accuracy of 0.1 μm. A z-axis micropositioner allows the chip to be remotely focused. The whole laser link system can be controlled manually via a Windows based software tool or automatically via a script file.

To link two metal lines, the laser link technology requires a special structure

consisting essentially of a gateless NMOS transistor as shown in Figure 2.6. When the laser beam is focused midway between the two diffusion regions, a "zap" generates a melting pool, enabling dopants of the N+ regions to diffuse across the gap and create a low resistivity connection. To lower the resistivity, more zaps can be performed on longer link structures. The structure of Figure 2.6 is the basic two contact long laser link used for restructuring the signal lines of the LAMSA device..

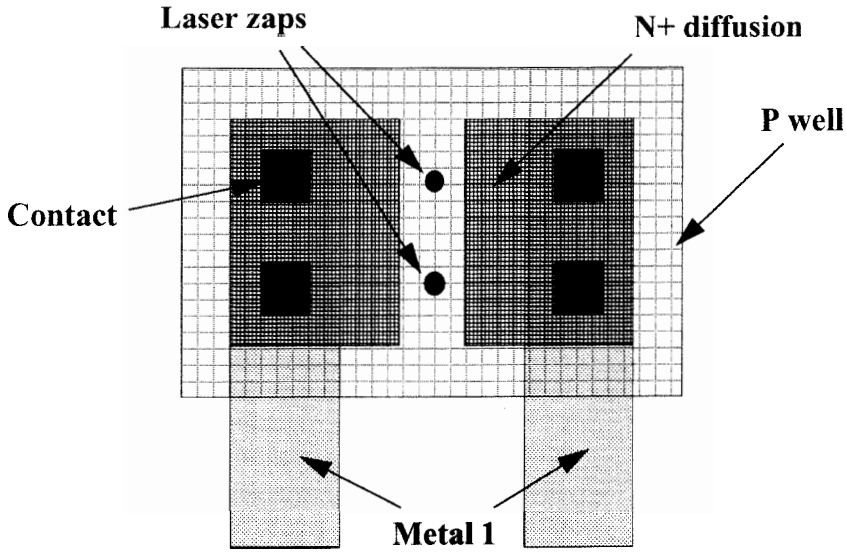

Figure 2.6 Laser link structure.

A laser cut is performed by shining the laser beam on a metal line in order to melt the focused region and generate an opening. For metal line widths smaller than 3.3 μm, only one zap is required to make the cut. Link and cut parameters are listed in Table 2.1.

	Power (W)	Pulse Duration (μs)	Number of zaps	R open (Ω)	R link Average (Ω)	R link Std. dev. (Ω)
Link	2.0	100	2	> 20 M	78.0	7.39
Cut	1.5	100	1	> 20 M	----	

Table 2.1 Laser link parameters for the Mitel 1.5 μm process.

2.4.2 The testable laser link

One of the important problems encountered in wafer scale design is the occurrence of Vdd-ground short circuits within a circuit block. In this situation, no further testing can be performed on the system since the power supply is constantly shorted. A counter solution consists of having every circuit block initially disconnected from the ground bus and connecting each one at a time. In this case, circuit blocks having power shortage can be located by monitoring the supply current after each connection. Past wafer scale design employed transistors to perform this duty[26]. This method has the advantage of being simple, however, the transistor resistance can generate a large voltage drop when large currents are drawn, reducing the effective voltage supply of the circuit block. To reduce the voltage drop, larger transistors can be implemented at the expense of taking up more silicon space.

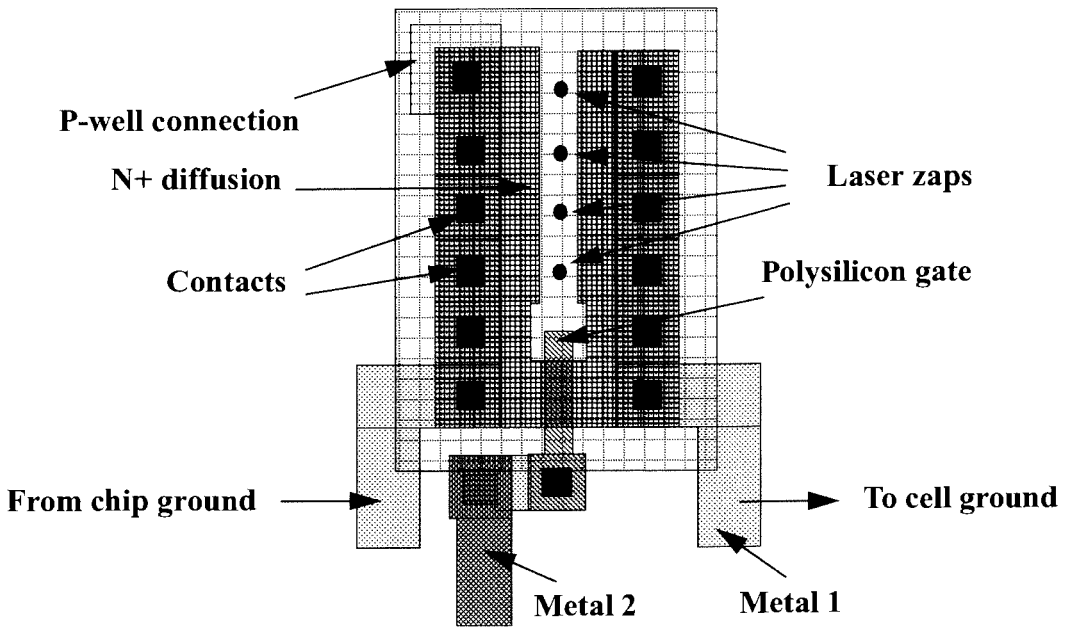

Figure 2.7 The testable laser link.

To fulfill the particular task of connecting a circuit block to the ground through a low resistive switch without consuming too much silicon space, a new structure has been

developed at SFU, called the testable laser link[24]. As shown in Figure 2.7, the structure combines a laser link with a NMOS transistor at one end. By turning the transistor "on", the power consumption of the circuit block undergoing tests can be measured; in the event of no power short being detected, the laser link is zapped, forming a permanent low resistive connection. By virtue of this added transistor, faulty circuit blocks can be quickly discarded without performing a time consuming linking sequence. The testable laser link uses a longer diffusion structure, requiring three laser zaps, which results in a lower gap resistance. Adding this resistance to the lower contact chain resistance reduces the overall link resistance to about 50Ω . Contrary to the normal laser link structure, the testable laser link requires a P-well connection, permitting the NMOS transistor to function normally.

2.5 Summary

A brief history of the evolution of the WSI field of research leading to the refinement of design methodology for defect avoidance and the creation of restructuring tools was presented. Exploiting successful design strategies and a restructuring tool issued from the WSI era, the LAMSA design is described with emphasis on its basic principle of operation and its different redundancy aspects. The redundancy schemes of section 2.3 were shown as examples. In chapter 4, the robustness of various redundant sensor grid patterns and readout circuits will be investigated through simulations. Finally, the laser link technology used for restructuring the LAMSA circuits was reviewed and the link and cut parameters were optimized for the Mitel 1.5 μm CMOS process chosen to fabricate the LAMSA prototype.

Chapter 3

Analysis and Design of the LAMSA Circuits

This chapter focuses on the details of the large area magnetic field sensor array design. In addition to having many useful applications, as seen in section 1.3, the magnetic field sensor array system presented in this thesis has the advantage of using a simple MOSFET structure as a basic sensor cell. This simplifies the circuit design complexity and facilitates the implementation of built-in redundancy. Section 3.1 details the Magnetic field Sensor Cell (MSC), a novel double drain/double MOSFET designed especially for applications in sensor arrays.

Attempts to include the magnetic field effect in SPICE simulation was made using the lumped discrete approach to model arrays of merged MSC. Reference [31] compares simulated and experimental results. A large discrepancy was observed leading to the abandonment of this method. In addition to this, the poor matching of the SPICE transistor parameters observed on the first runs of the Mitel CMOS 1.5 μm offered by the Canadian Microelectronic Corporation, rendered useless the SPICE simulation results of the MSC

arrays. As a result, an experimental approach was taken to determine the MSC geometry that would give the highest sensitivity.

The complete circuit analysis of every circuit block comprising the LAMSA along with a brief description of the restructuring features of the spare blocks is discussed in the following sections. To facilitate the reading of this chapter, figures of circuit layouts are grouped in appendix A. It should be noted that experimental results obtained with the sensor grid, having the cascode current mirror as an active load, have shown a good sensitivity without using a differential amplifier. Thus, in an effort to ease the testing stage of the LAMSA, the differential amplifier has not been designed for the first complete prototype and is therefore not mentioned in the remainder of the thesis.

3.1 A Double Drain/Double Source MOSFET for Magnetic Field Sensor Arrays

In the past, several examples of highly functional integrated magnetic field sensors have been successfully achieved for useful applications such as contactless keyboards, brushless motors and proximity sensors. Most of these applications involve silicon process technology where the basic sensing elements employed are the conventional bipolar epitaxial Hall plate, the MOS Hall plate, magneto resistive structures and bipolar magnetotransistors[27]. Although the double drain and triple drain MOSFETs are among the most investigated of the fully compatible CMOS magnetic field sensors, they still have not found any practical applications, due mainly to their low intrinsic sensitivity. Nevertheless, a simple double drain MAGFET used with a current mirror as active load and a simple amplifier buffer on the same chip has shown a sensitivity as high as 1 to 5 mV/Gauss[12]. These active load and amplifier circuits are part of a magnetic field sensor

array which uses a grid of double drain MAGFETs as their basic sensing elements.

Inspired by these results, the MAGFET sensor has been selected as the sensing element for the LAMSA. However, the single source of the conventional MAGFET structure of Figure 2.1 has been transformed to a double source similar to the drain side. The first step in building the new merged device is to transform the single source of the MAGFET into a double source. As a result, two double drain/double source MAGFETs can be put side by side and merged by sharing a pair of drain or a pair of source diffusions. By doing so, the total area taken by the two MAGFETs is reduced by about 16%. Figure 3.1 shows the layout views of a) a double drain/single source (DD-SS) MAGFET, b) a double drain/double source (DD-DS) MAGFET and c) two merged DD-DS MAGFETs.

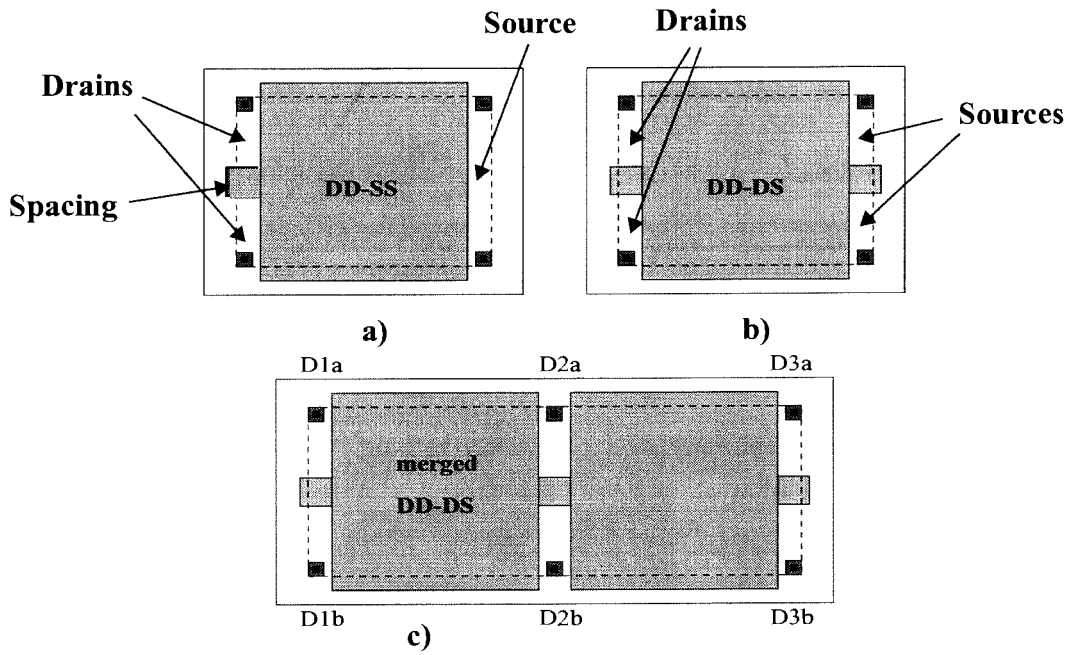

Figure 3.1 Layout views of a) a double drain/single source b) a double drain/double source and c) a merged double drain/double source MAGFETs.

The merging of two or more sensors side by side reduces the amount of contacts and signal lines required to address the sensor grid. Keeping in mind the targeted large die

size of the LAMSA, the reduction of contacts and signal lines will increase the robustness of the sensor grid to fabrication defects. The sensitivity of this novel double drain/double source merged MAGFET has been experimentally optimized using different layout geometries. The results are presented in section 3.1.2 and 3.1.3, while section 3.1.1 describes the magnetic field source employed for the sensitivity measurements.

3.1.1 Magnetic field source

The technique employed to generate the magnetic field is based on the Helmhotz coils principle[28]. The magnetic field generated by two coils positioned face to back on the same axis, as shown in Figure 3.2, is approximately uniform within the space delimited by the coils' diameter, if the distance between them equals the length of their radius. The magnitude of the constant field, in Gauss, inside the space along the x axis, H_x is then given by:

$$H_x = \frac{32\pi NI}{5^{3/2}cR} \tag{3.1}$$

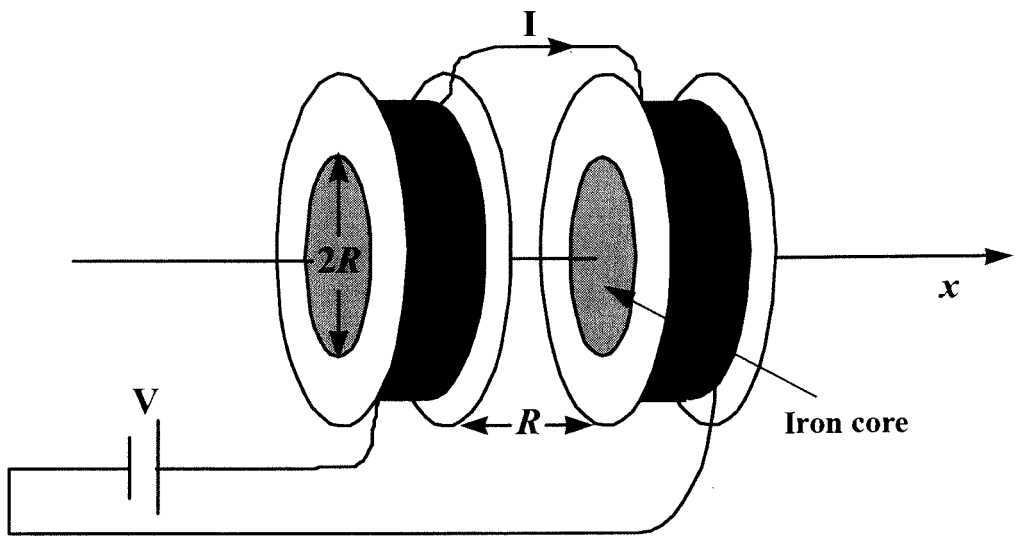

Figure 3.2 Helmholtz coils used to create the magnetic field.

where I is the current flowing in the coils, N the number of turns in each coil, c the speed of light and R the coils' radius. By filling the core of the coils with a material having a high magnetic permeability, μ, the resulting magnetic field in the gap, B_x, is raised to:

$$B_x = \mu H_x \tag{3.2}$$

For instance, in our case, soft iron cylinders have been used to boost the field magnitude by a factor of about 200.

A monolithic Hall effect sensor (UGN-3501UA), based on the Hall plate principle as the magnetic field sensing mechanism, was used to calibrate the coils. This Hall sensor provides an accurate magnetic field measurement within a range of -3000 to 3000 Gauss with a sensitivity of 700 mV/1000 Gauss. Initially, the Hall effect sensor output was calibrated using a Nuclear Magnetic Resonator (NMR) and the coil system of the Physics department at Simon Fraser University. The NMR is a precise magnetic field sensor, capable of a resolution in the order of one tenth of a Gauss. The Hall plate sensor was calibrated from -3000 to 3000 Gauss with a reading occurring at every 200 Gauss. A curve fitting of the Hall plate output voltage as a function of the magnetic field was then performed in order to extrapolate the magnetic field value corresponding to any output voltage. The Hall plate reading is valid, provided the field magnitude is included within the calibration limit of -3000 to 3000 Gauss. Figure 3.3 shows the calibration curves obtained for the Helmhotz coils pair. The arrows indicate the proper axis for each curve. The DC current injected into the coils creates a magnetic field which is measured by the Hall plate and converted into magnetic field values. Hence, the coil current can be directly linked to the magnetic field magnitude between the coils.

The coils are driven by a Xantrex regulated DC variable voltage source capable of

delivering 300 V at 10 A. The power supply can be remotely controlled by an external 0 to 5V DC voltage source or 0 to 5 mA DC current source. The total coil resistance is 30 Ω. Before each measurement, a settling time of five seconds is allowed to reduce the hysteresis effect of the iron core.

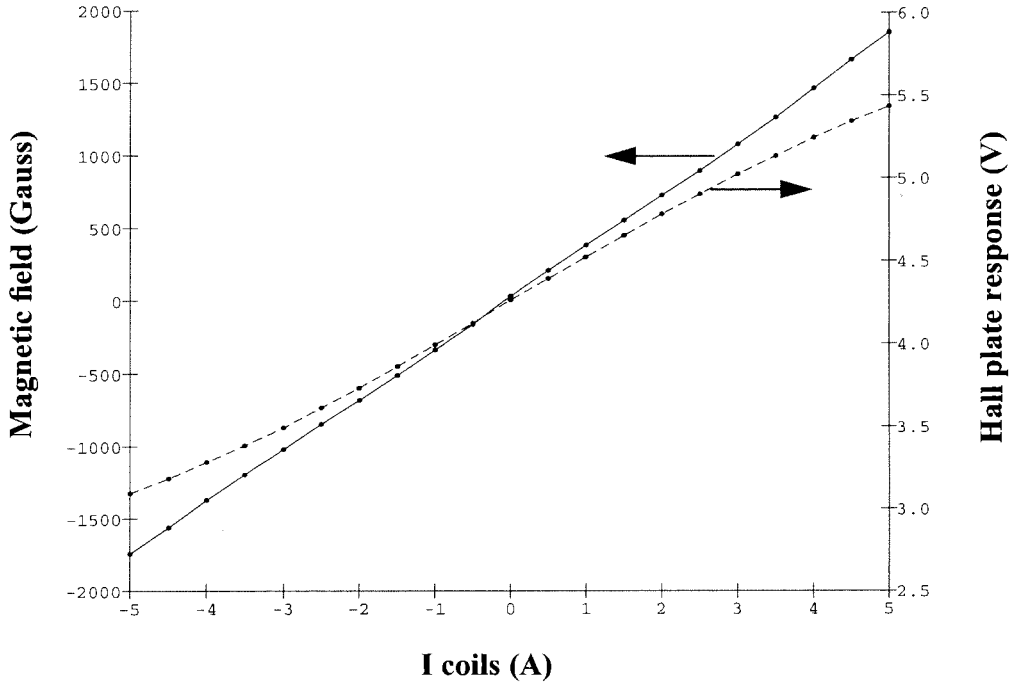

Figure 3.3 Helmhotz coils calibration curves.

3.1.2 Sensitivity optimization of the double drain/double source merged MAGFET

When subjected to magnetic fields, as described in section 2.2.1, MAGFETs display a change in the current imbalance parameter δ of equation 2.2. Previous studies have demonstrated that the maximum sensitivity (current imbalance) is reached for MAGFETs working in the saturation region[29] and having a square geometry, i.e. channel length equalling the width. In order to determine the dependence of the current imbalance as a function of the total MAGFET current in saturation mode, measurements on a NMOS MAGFET of length and width of 18 μm, fabricated with the Northern Telecom CMOS 3μm process, have been performed. The graph of Figure 3.4 shows I_{D1},

I_{D2} and the current imbalances as a function of the gate voltage, V_G, taken with and without magnetic field, B, for a constant drains-source voltage, V_{DS}, of 5 V. The data were gathered with an HP semiconductor analyser (model 4145A) where one variable voltage source was used as V_G, and two SMU channels were connected to the drains as current monitor, i.e. constant voltage sources V_D[30].

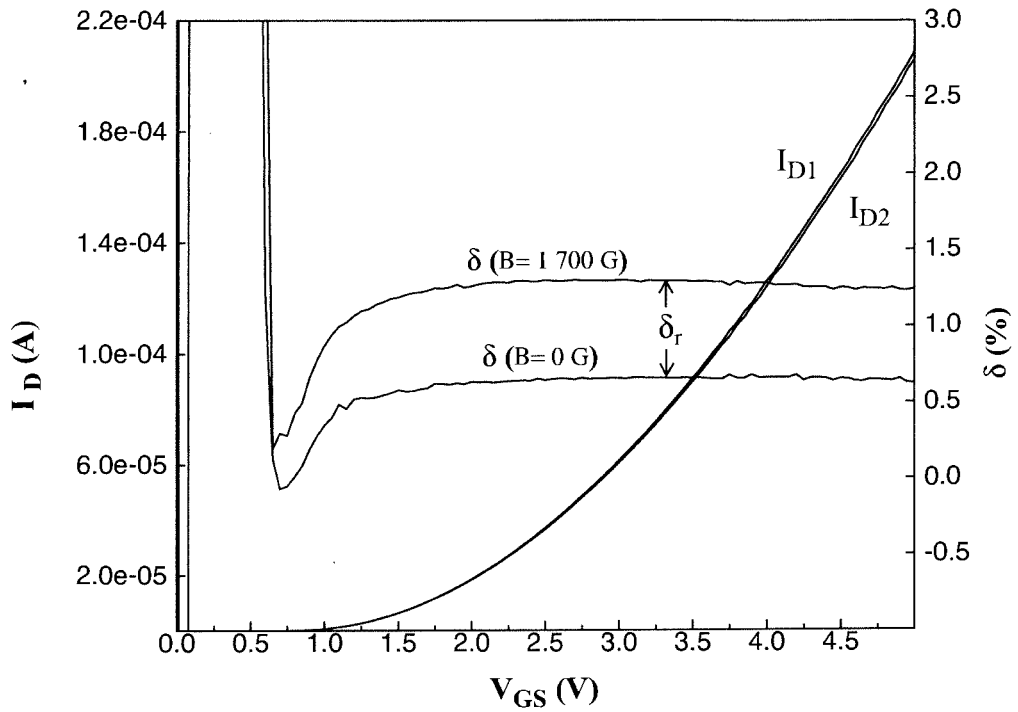

Figure 3.4 Effect of a magnetic field of 1700 G on the drain currents and comparison of the current imbalances for B= 0 G and B= 1700 G.

The current curves present a typical quadratic behaviour of a transistor in saturation, since $V_{GS} - V_T < V_{DS}$, where V_T, the threshold voltage, is about 0.8 V for this technology. The intrinsic current imbalance obtained when no magnetic field is applied (B= 0 G) is due to geometrical differences of the drain diffusion regions and is specific to each MAGFET. For $V_{GS} < V_T$, δ exhibits an unusual high value due to the large discrepancy between the drain currents in subthreshold. Once V_{GS} exceeds the threshold voltage of about 1 V, δ reaches a plateau. The same behaviour is observed for δ obtained

with B equal to 1700 G, with the exception that the magnetic field provokes a shift in the plateau level. The occurrence of this plateau shows that in the saturation region, the current imbalance, hence the sensitivity, is independent of the total current. The relative current imbalance, δ_r, used to quantify the sensor sensitivity, is given by the difference between the current imbalances obtained with and without the magnetic field as shown in Figure 3.4.

3.1.3 Experimental results of the double drain/double source merged MAGFET

In order to optimize the sensitivity of the merged MAGFET, six special structures have been designed and fabricated with the Nothern Telecom CMOS 3 μm process. They consist of two sets of three arrays of three different square MAGFET sizes: 40, 80 and 160μm. Based on the high discrepancy obtained between experimental results and SPICE simulations of MAGFET arrays using the lumped discrete approach, as reported in reference [31], no simulation could be usefully performed on those structures. The study relied solely on experimental results. Figure 3.5a) shows the first set of arrays. Each array is made up of five MAGFETs in which six sensitivity measurement patterns can be configured. In Figure 3.5a), from top to bottom, the patterns are:

1) Single source - double drain, with maximum spacing between drains.

2) Double source (maximum spacing) - double drain (maximum spacing).

3) Double source (maximum spacing) - double drain (minimum spacing).

4) Situation 3 inverted using the same MAGFET.

5) Double source (minimum spacing) - double drain (minimum spacing).

6) Single source - double drain, with minimum spacing between drains.

The second set of arrays of Figure 3.5b) presents the same measurement patterns as Figure 3.5a) except that no active region is defined underneath the polysilicon spacing

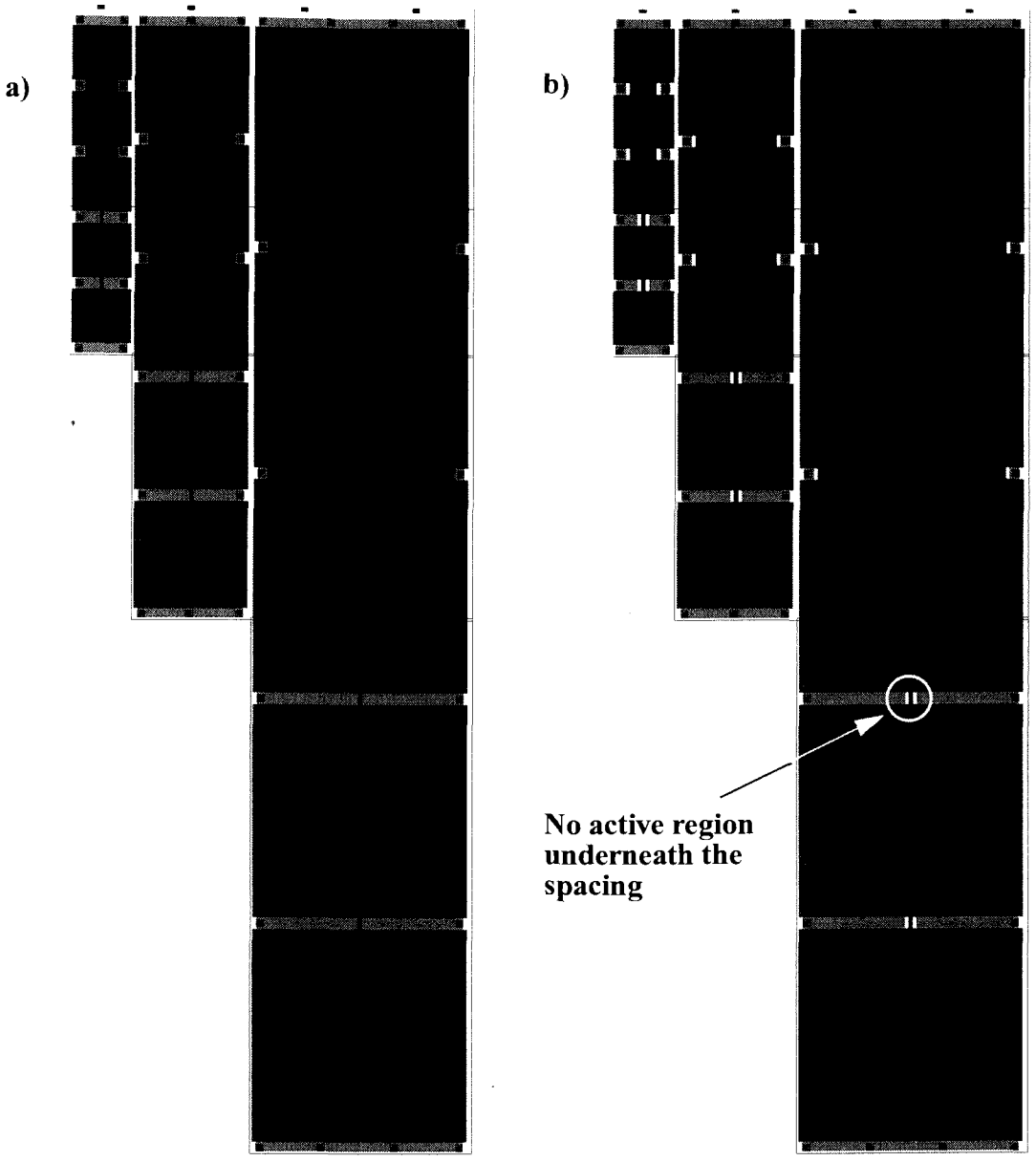

Figure 3.5 Array structures for sensitivity optimization with a) no conduction barrier and b) conduction barrier between MAGFETs.

separating the drain diffusions.[1] The effect desired is to remove the inversion layer underneath the spacing, creating a conduction barrier between adjacent MAGFETs within the array. Measurements were done, using once again, the plateau technique in saturation mode as described in section 3.1.2. Special care must be taken when measuring the

1. In the case of MAGFET arrays, since the drain side can be interchanged with the source side, only the term drain is employed to name the diffusion regions.

sensitivity of the merged DD-DS device, i.e no diffusion regions must be left floating. For instance, in Figure 3.1c), when the left side MAGFET is measured, contacts D1a and D1b are connected to separate drain voltage sources while contacts D2a, D2b, D3a and D3b are connected to ground, minimizing the current draw by the right side MAGFET. Similarly, the right side MAGFET is measured by connecting D1a, D2a and D1b, D2b to separate drain voltage sources and D3a and D3b to the ground.

Table 3.1 compiles the relative current imbalances obtained for a magnetic field of 1700G. Two chips including the test structures of Figure 3.5 were measured. Similar results were obtained on both, hence, only one set of measurements is presented in Table 3.1. Results obtained on the set of arrays without conduction barriers demonstrate that none of the MAGFET structures gives a higher sensitivity. This suggests that the size of the inversion layer between adjacent drains does not affect the equipotential line distribution in the vicinity of the drains, which is responsible for the sensitivity in saturation mode. Conversely, the set of arrays with a conduction barrier underneath the spacing shows a sensitivity reduction for the measurement pattern 1, 2 and 3. These patterns correspond to MAGFETs having the maximum spacing between drains, thus, reducing the short-circuit effect. As mentioned in chapter 2, section 2.2.1, an equilibrium is achieved in the channel when the Lorentz force is balanced by the Hall voltage, disabling the current deflection. However, in the vicinity of the drains, the diffusion regions short-circuit the Hall voltage, permitting the deflection of charge carriers. Hence, by reducing the short-circuit effect around the drain diffusions, the sensitivity is altered. The measurement patterns 4, 5 and 6, which have the least spacing between drains, and thus longer diffusion regions, give approximately the same current imbalances as the arrays with no conduction barrier.

Pattern #	Experimental Sensitivity (Relative Current Imbalance δ_r(%))					
	Arrays Without Barriers MAGFET Size (μm)			Arrays With Barriers MAGFET Size (μm)		
	40x40	80x80	160x160	40x40	80x80	160x160
1	.758	.748	.747	.403	.287	.275
2	.773	.774	.769	.441	.298	unstable
3	.770	.731	.730	.455	.296	.233
4	.759	.760	.802	.650	.730	.704
5	.690	.733	.727	.651	.698	.728
6	.750	.716	.791	.779	.705	.756

Table 3.1 Measured relative current imbalances for the array structures of Figure 3.5 for B=1700 G.

As a comparison, for a magnetic field of 1700 G, Lau et al[23] measured on double drain/single source single MAGFETs of ratio W/L of 50/50 and 100/100 a sensitivity of 0.544 and 0.646 respectively. Both devices operated in the saturation region and their spacing between the drains was 4 μm. These results suggests that no loss of sensitivity arises from the merging of MAGFETs.

From the results of Table 3.1, the characteristics of the merged DD-DS MAGFET, used as the basic Magnetic Sensor Cell (MSC) for the LAMSA, can now be defined. MSCs should be of square geometry with no special requirement on the spacing size, provided that the active layer lies under it. It must be an N type MOSFET to achieve a better sensitivity, since the mobility of electrons is higher than that of holes. A triple drain/ triple source merged MAGFET has also been investigated[31]. Although the use of a middle drain connection increases the sensitivity by about 45%, the added requirements of

extra contacts, signal lines, SPDT switches and restructuring overhead would complicate the design, the tests, and also reduce the yield of the LAMSA. Thus for this first attempt of circuit fabrication of a sensor array system with redundancy, a more conservative design using DD-DS MAGFETs has been chosen in order to concentrate the study on the redundancy and the restructuring aspects.

3.1.4 MSC arrays with drain line redundancy

In order to implement the drain signal line redundancy scheme, the laser link structures are merged to the MSC drain contacts. Since the laser link consists of a gateless NMOS transistor, the easiest and more compact way to attach a link structure to a drain is to simply use the N-type doped drain as one of the diffusion regions of the laser link. Figure 3.6 shows the layout of a three MSCs subarray designed with one spare drain line for each pair of drains. Also, three laser link structures are designed to connect the spare gate line.

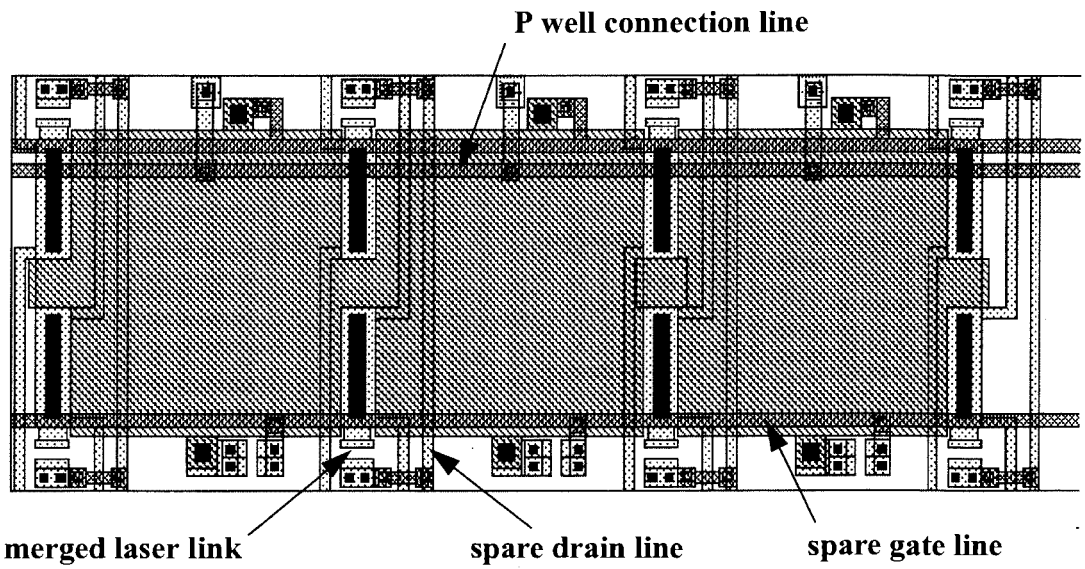

Figure 3.6 MSC subarray with merged laser link structure.

Special care must be taken in the design to leave the gap zapping space free of metal lines which would obstruct the laser beam. In the case of the subarray made of three $54\mu m^2$ merged MSC of Figure 3.6, used in the LAMSA prototype, the combined laser link structures increase the total subarray area by approximately 33%.

3.2 Active Load and Single-Pole Double-Throw Switches

The cascode Current Mirror (CM) acts as an active load for the MSCs. It is the key element transforming the MSC's current imbalances, generated by the magnetic field, into voltage[32]. The Single-Pole Double-Throw switches (SPDTs) are used to direct the currents of the CM to one sensor cell at a time. They also affect the sensitivity of the sensor array, since the current coming from the CM flows through them before reaching a sensor cell. This section describes these two circuit blocks separately and then, aided by the SPICE simulation program, find the best operating condition of the whole CM-SPDTs-MSC subcircuit.

3.2.1 The cascode current mirror (CM)

Compared to a simple current mirror using two transistors, the two extra transistors of the cascode CM, M3 and M4, as shown in Figure 3.7, increase its output resistance and desensitize the effect of the output voltage variation on the output current[33]. In order to obtain a good uniformity of the MSC responses throughout the grid, only one CM is used for the entire sensor array.

Since MSCs are essentially MOSFETs of type N, the CM, acting as an active load, is made up of four P MOSFETs of the same dimension. Considering that in order to obtain the highest sensitivity MSCs must operate in saturation mode, and that transistors of the

CM in normal operation are always in saturation mode, the ratio width(W)/length(L) assigned to the CM transistors would simply be half that of the MSC, namely 0.5. However, taking into account the difference between the P type and N type carrier mobility of the Mitel 1.5 μm CMOS process, where the mobility ratio μ_n/μ_p equals about 4.0, the width and the length are set to 8 μm and 4 μm respectively. To minimize the error of aspect ratios among the transistors, gate sizes larger than the minimum size geometry are employed.

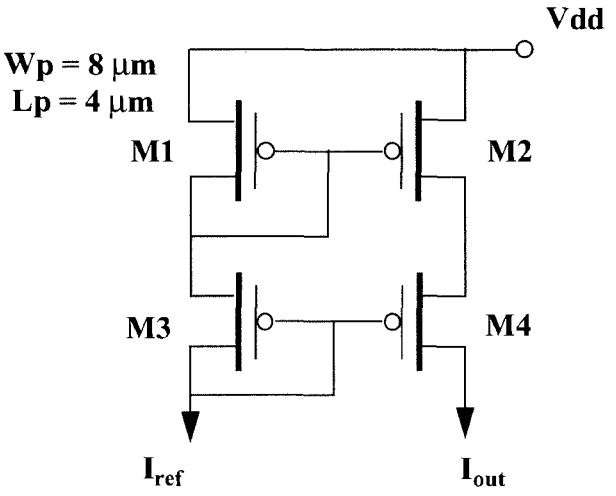

Figure 3.7 Schematic diagram of the cascode current mirror.

Layout of the CM is depicted in appendix A, Figure A.1a). Figure A.1b) presents the same cell with restructuring overhead, consisting of simply two laser links, allowing a spare CM to be hooked to the reading bus, lines Da and Db (Figure 2.3).

3.2.2 Single-pole double-throw switches (SPDTs)

The single-pole double-throw switch is merely an inverter having the source of the P MOSFET connected to one of the reading lines. They work in tandem, directing the pair of drains either to the ground or to the reading bus, as shown in Figure 3.8. Since they transmit a current instead of a voltage, the usually full transmission gate type comprised of

two MOSFETs of type N and P in parallel is not required. The voltage controlling the SPDT comes from the shift register output and is either near 0 V or 5 V. In normal operating conditions, transistors in an "on" state are in linear mode. Hence, the resistivity added by the SPDT transistors in the current path is negligible compared to that of the MSC and the CM, both working in the saturation region. For compactness, transistors W/L ratios have been set to one for the NMOS, and four for the PMOS.

Figure A.2 shows the layouts of a) a pair of SPDTs and b) a spare pair. Since the signal line redundancy schemes selected for the sensor array consist of one spare signal line per pair of drains, as shown in Figure 3.6, both SPDT cells require a laser link structure allowing the connection of the spare line to one SPDT switch of the pair. In the case of the spare SPDT twin, Figure A.2b), two extra laser link structures are needed to connect the normal drain lines dl_1 and dl_2. P-guard and N-guard rings have been designed around the NMOS and PMOS transistors respectively, to protect the SPDT switches against latchup.

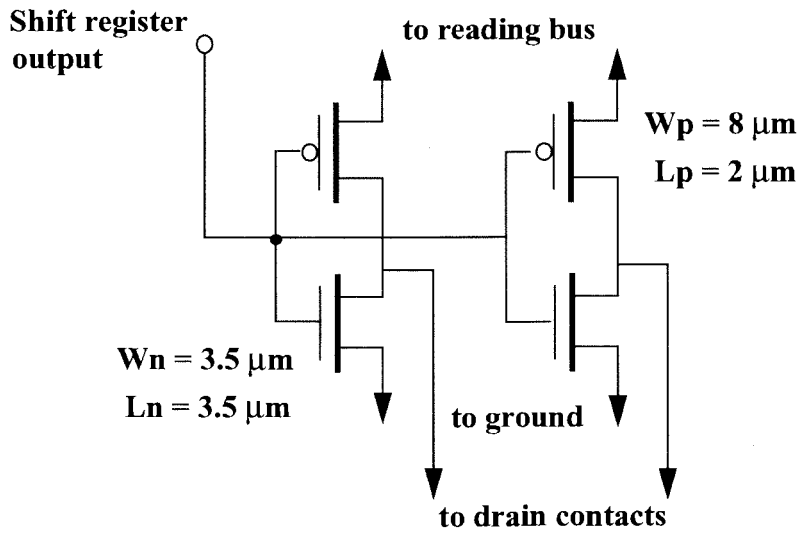

Figure 3.8 Schematic diagram of a pair of single-pole double-throw switches.

3.2.3 DC simulation of the MSC readout circuit

In order to evaluate the best biasing voltage V_G of the MSCs, a simple DC analysis using the simulation program SPICE was performed. In the reading situation of Figure 2.3, where a current flows through MSC2, the gate voltage, V_G, is swept from 0 V to 3 V. Figure 3.9 summarizes the equivalent circuit obtained in these conditions when no magnetic field is applied. To simulate the MSC with SPICE, simply two N MOSFETs of ratios W/L of 0.5 are employed with their gates connected together. No magnetic field effect is taken into account in this simulation.

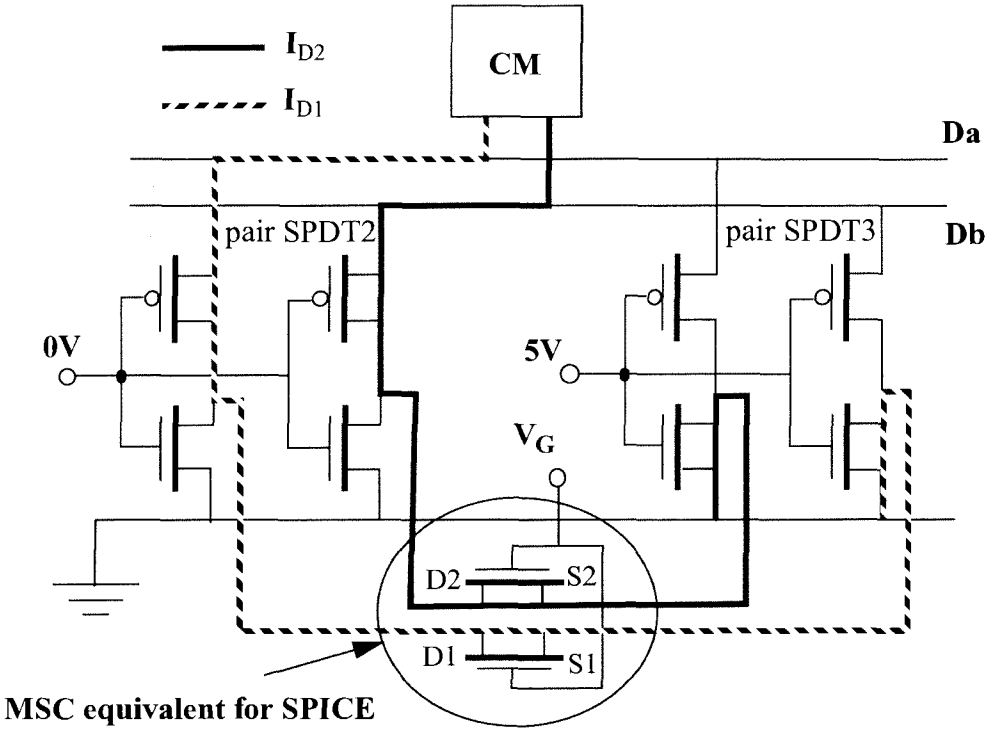

Figure 3.9 Schematic diagram of the circuit involved in the reading of a sensor cell.

Results of the simulation are sketched in Figure 3.10. In Figure 3.10a), the drain current I_{D1} rises for a gate voltage V_G of 0.9 V, which is approximately the NMOS threshold voltage, V_T = 0.84 V. Then, the increase in current follows a second order behaviour, characteristic of the saturation mode, until it reaches a plateau at about

V_G=1.57 V. Figure 3.10b) shows the voltages at three nodes: the reading bus Da and the drain and the source of one half of the MSC, D1 and S1. The voltage at the S1 node remains small for the whole simulation, showing that N MOSFETs of the pair SPDT3 are in linear mode and have little effect on the total load. As I_{D1} increases, the voltage across the diode-biased PMOS of the current mirror increases linearly, causing the voltages at

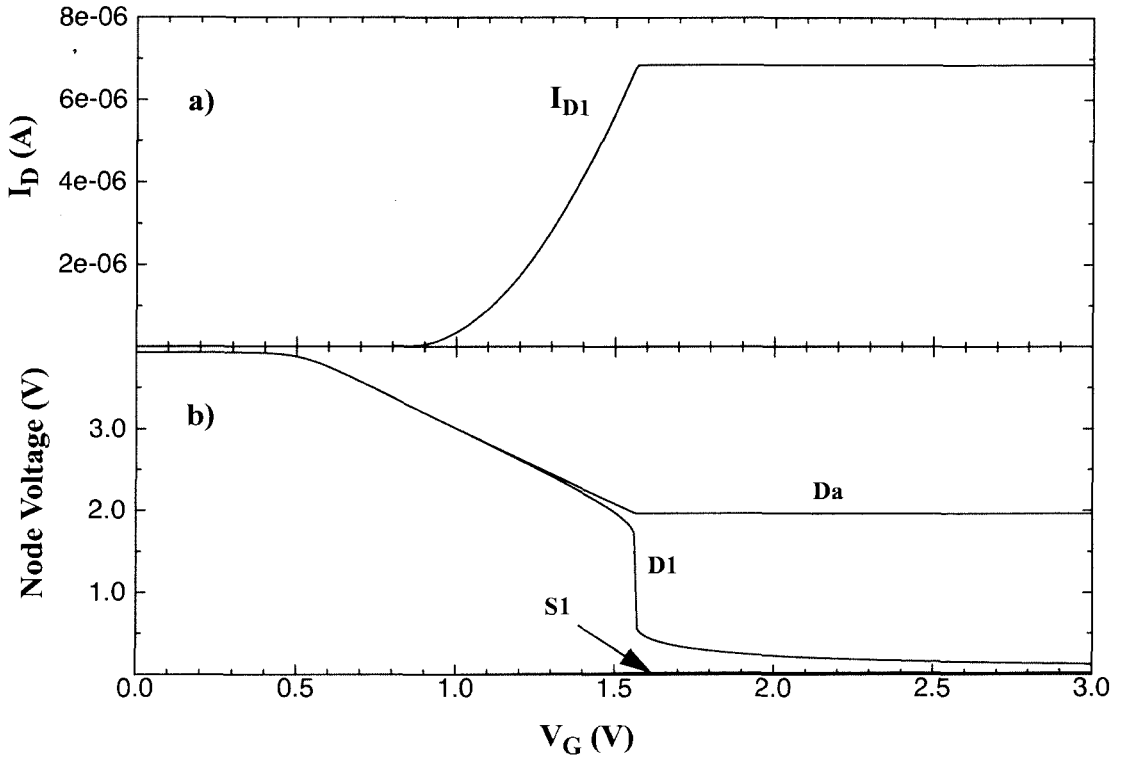

Figure 3.10 SPICE simulation results of the MSC's biasing circuit a) drain current and b) node voltages.

nodes Da and D1 to decrease, also linearly. This trend stops once the gate-source voltage, V_{Da}, of the PMOS transistor of the pair SPDT2 becomes small enough that $V_{Da,D1} > V_{D1} - V_T$(pmos), indicating that the PMOS shifts in operating mode from linear to saturation. From this point on, any further increment in the current I_{D1} is prohibited since it would imply the conflicting requirement of an increase of the voltage at the node Da for the

PMOS, and at the same time a drop of V_{Da} for the cascode current mirror. Consequently, as V_G keeps increasing, the sensor is driven in linear mode, in which the sensitivity to the magnetic field is weak. Similar behaviour is observed for the current branch I_{D2}. From these results, one could expect a good MSC's sensitivity for V_G ranging from 0.9 V to 1.6V, where the sensor is operating in saturation mode. The SPICE program of this simulation is presented in appendix B.

3.3 The Voltage Response to a Magnetic Field

As mention in the chapter introduction, two factors rendered useless any simulations of the circuit comprising the CM, SPDT switches and the MSC array in presence of a magnetic field. The failure of the lumped discrete approach in simulating accurately the MSC arrays, and the poor matching of the SPICE transistor parameters observed on the first runs of the Mitel CMOS 1.5 μm process.

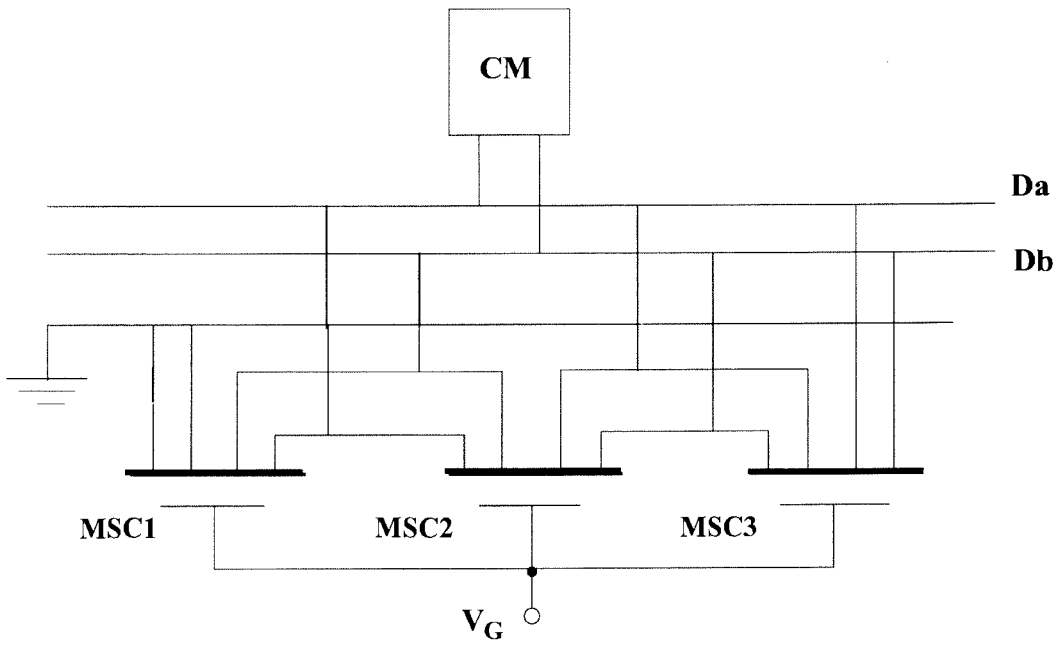

Figure 3.11 Circuit diagram for the measurement of the sensor voltage response to a magnetic field.

Alternatively, the CM and a subarray of three MSCs were fabricated separately on a test chip. They were used to evaluate experimentally the efficiency of the current mirror, acting as active load, in transforming the magnetic field generated current imbalance of the MAGFET into a voltage difference $V_{Da,Db}$, at the output of the reading bus. Figure 3.11 shows the interconnections between the CM and the MSC subarray in the case were the output voltage $V_{Da,Db}$ of MSC1 to a magnetic field is measured. The interconnections were wired externally and two voltmeter channels of the SPA 4145B were used to measure the voltages of the lines Da and Db. Since in normal operating condition the transistors of the SPDT switches directing the current paths are in linear mode, their effect on the magnetic field response is weak. As a result, they were not included on the test chip.

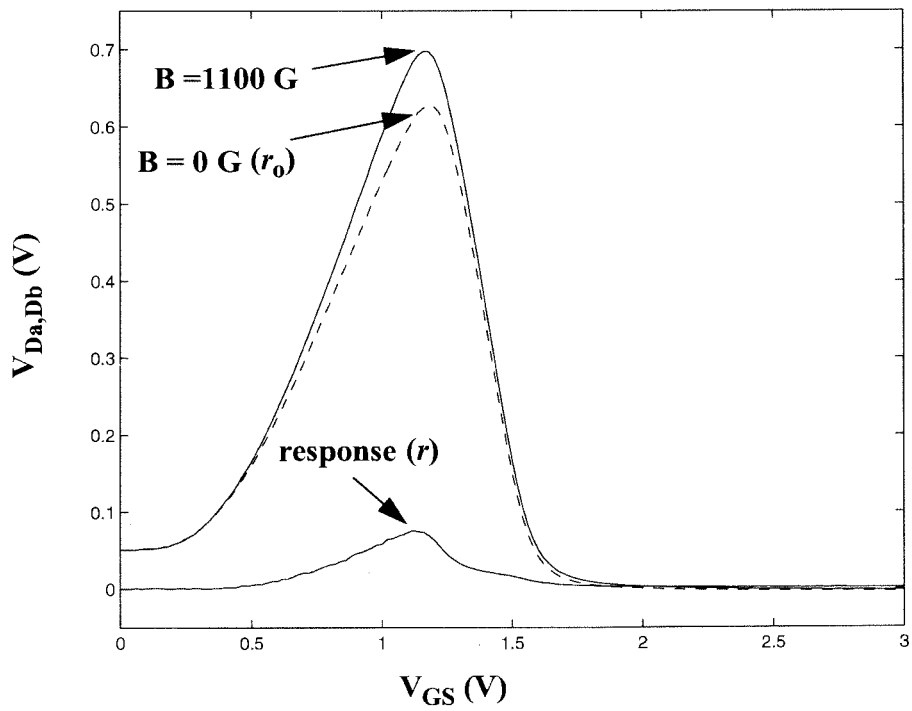

Figure 3.12 Voltage readouts and the resulting magnetic field response of the test circuit of Figure 3.11.

The curves of Figure 3.12 show the measured voltage readouts $V_{Da,Db}$ of the circuit of Figure 3.11 with and without magnetic field and the resulting magnetic field response obtained from the subtraction of these two curves, as a function of the sensor gate voltage. A maximum response of 74.9 mV for 1100 Gauss was obtained at a gate voltage of 1.12 V, well within the gate voltage range predicted by the simulation results of Figure 3.10. As can be seen, without a magnetic field, the intrinsic current imbalance of the sensor and the mismatch of the current mirror transistors produces an important offset readout r_o, that is required to be subtracted from the measurement with magnetic field in order to obtain the true response r. For an entire array of sensor cells, r_o varies from sensor to sensor and produces a fixed pattern noise[1] that must be removed from the raw data to obtaine the sensed image. Also, the value of this offset voltage depends on the active load resistance.

Analytically, the voltage response with offset removed, r as in Figure 3.12, can be related to the current imbalance created by the magnetic field through the equation:

$$r = \delta(I_{D1} + I_{D2})(R_{cm}^{-1} + R_{msc}^{-1})^{-1} - r_o \tag{3.3}$$

$I_{D1} + I_{D2}$ is total current flowing in the MSC, δ is the current imbalance including the intrinsic component, R_{cm} and R_{msc} are the output resistances of one branch of the current mirror and the sensor cell respectively, seen as being in parallel by the sensor, and r_o is $V_{Da,Db}$ without magnetic field, as shown in Figure 3.12. In the case where δ_r, the relative current imbalance, is known, equation (3.3) simply becomes:

$$r = \delta_r(I_{D1} + I_{D2})(R_{cm}^{-1} + R_{msc}^{-1})^{-1} \tag{3.4}$$

Keeping the gate voltage at 1.12 V, the response of the sensor cell MSC1 was then

1. The term "fixed pattern noise" comes from the image sensor field, where it represents the variation in pixel currents at uniform illumination, measured at the output of the sensor array[34].

measured as a function of low magnetic field strength, in order to evaluate its sensitivity. Figure 3.13 shows the measured curve obtained. For this range of magnetic field, the response is monotonic and approximately linear at 66.7 μV/Gauss, with a minimum resolution of 40 Gauss. Similar behaviours were observed on the curves of MSC2 and MSC3. In chapter 5, comparison between calculated and measured responses are performed.

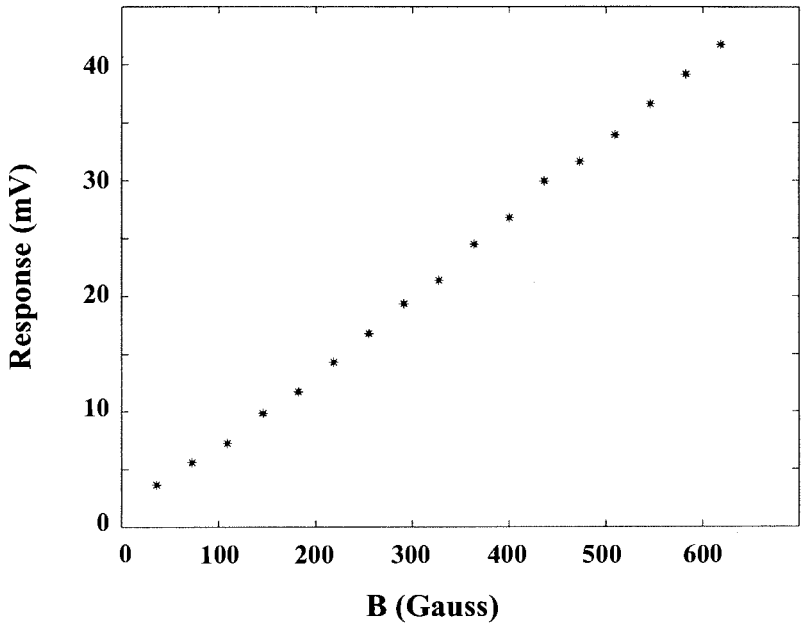

Figure 3.13 Magnetic field response of the sensor cell MSC1 of the test circuit of Figure 3.11.

3.4 The Driver

All MSCs on a row are activated at the same time by applying a voltage on the gate line connecting the sensor cell gates together. For large MSCs and long rows, the capacitive load can attain values in the order of hundreds of picofarads. To charge such a large capacitive load, a driver is required between the output of the row shift register and the gate line. Cascaded drivers are found to be very effective in reducing the delay when driving large capacitive loads[35]. They consist of a chain of drivers gradually increasing

in size. Given a capacitive load, C_l, the optimum number of drivers, n, required to minimize the delay can be calculated from[35]:

$$n = ln\left(\frac{C_l}{C_o}\right) \tag{3.5}$$

where C_0 is the capacitance of the minimum size driver of the chain, in this instance, the gate capacitance of the output stage of the D flip-flop. Rounding "n" to the nearest integer, the size ratio, f, of the chain is given by:

$$f = \left(\frac{C_l}{C_o}\right)^{\frac{1}{n}} \tag{3.6}$$

For a row comprising 57 sensor cells of 54 μm x 54 μm plus 76 spacings of 7 μm x 9 μm and C_0 of 100 μm^2, the nearest integer given by the equation (3.5) is eight; from equation (3.6) a size ratio of 2.65 is then obtained.

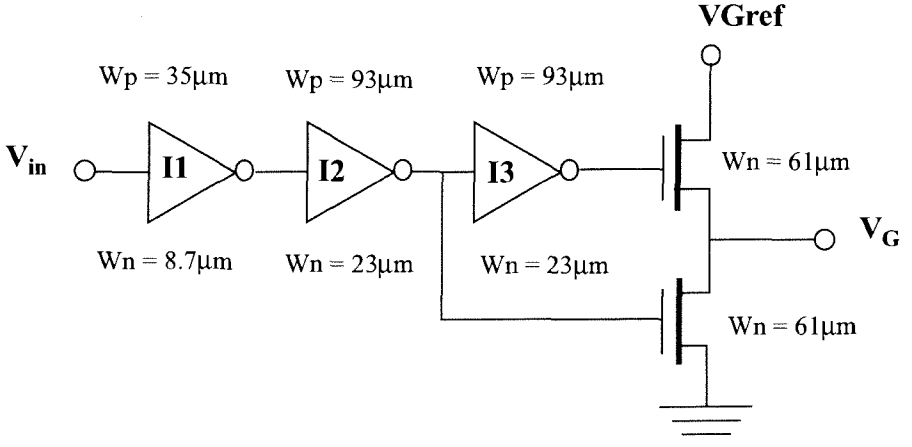

Figure 3.14 Schematic diagram of the row driver.

Figure 3.14 presents the schematic diagram of the driver. A special output stage has been designed in order to obtain an adjustable output level. The gate voltage represented by V_G in Figure 3.14 can be adjusted via the external voltage reference input VGref to a precise value producing the maximum sensitivity. A row of MSCs becomes active when V_G reaches VGref, which must be adjusted in the vicinity of 1 V according to the results of

the previous section. Therefore, to avoid any saturation effect slowing down the charge of the row capacitance, a N MOSFET has been implemented as a pull-up transistor of the last stage of the driver. Driver stages I1, I2 and the output stage N MOSFETs are scaled up to the ratio calculated previously, 2.65. I3 has the same size as I2 and acts as an inverter to drive the pull-up N MOSFET of the output stage. Constrained by the limited chip size available for the LAMSA design, only the first three driver stages were implemented instead of eight stages, in accordance with the calculation of equation (3.6). Even though the charging delay increases, reasonable performance is still achieved since the required output swing is low, in the vicinity of 1 V. No SPICE simulations were performed to optimize the transistor geometries for minimum delay of the three stages. Since only three stages are used, SPICE optimizations would have led to large sizes, not practical in the case of the LAMSA prototype, given the limited silicon die size available.

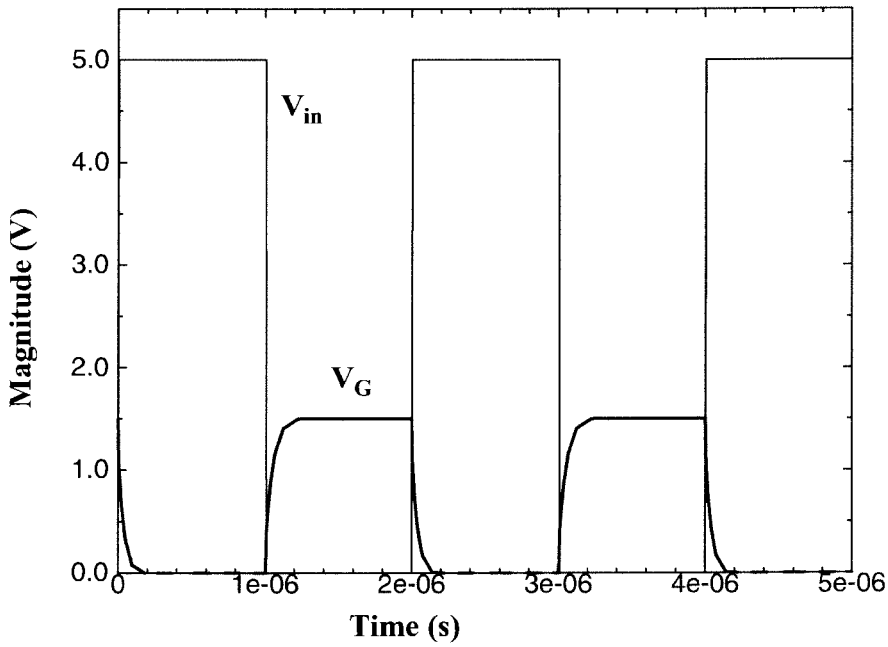

Figure 3.15 SPICE simulation results of the driver.

SPICE results of a transient analysis are plotted in Figure 3.15. VGref was set to 1.5 V and a square wave of magnitude 5 V at a frequency of 500 kHz was fed at the input.

To simulate the effect of the polysilicon gates contained on one row, a row capacitance of 330 pf in series with a row resistor of 11 Ω was connected at the output of the driver. The plot shows that the operating frequency is limited by the charge cycle. After 200 nsec, the output reaches a voltage equal to VGref. Figure A.3 shows the layouts of a) the driver and b) the spare driver with restructuring laser links.

3.5 Row and Column Shift Registers

The shift registers (SR) employed to synchronize the reading sequences of the sensor grid are composed of a simple positive edge-triggered D flip-flop with synchronous reset. Figure 3.16 presents the schematic diagram of its circuit. Two static latches with a clocked feedback ensure the master and slave functions. The full transmission gates used in the feedback loop avoid the need for ratioed design, and the output inverters isolate the storage nodes, preventing any charge sharing problems with a connected circuit. The latch inverter of the master side has been replaced by a NAND gate in order to provide a synchronous reset. Figure A.4, in appendix A, shows the layout of the D flip-flop cell.

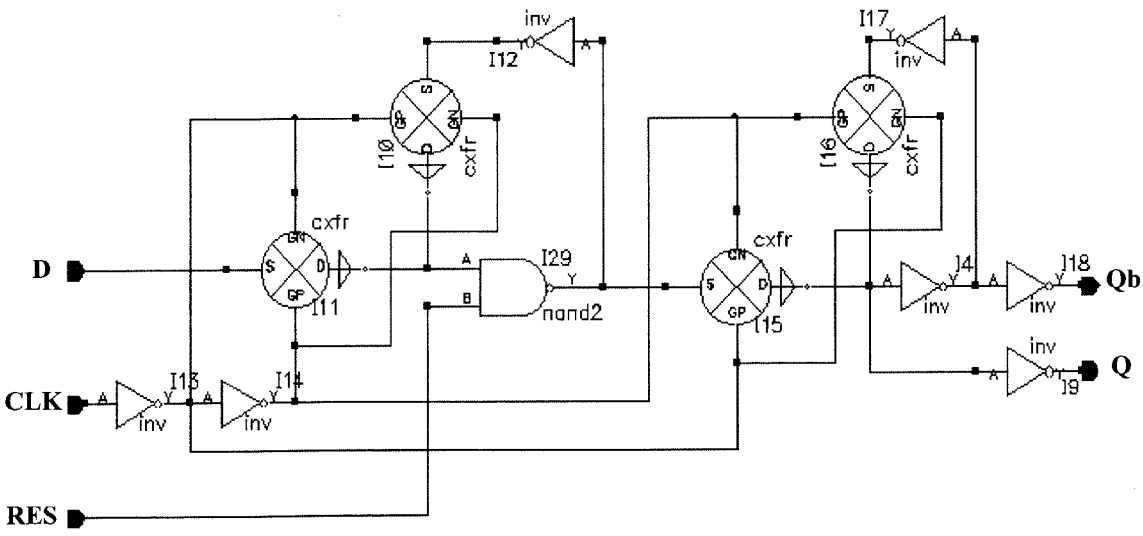

Figure 3.16 Schematic diagram of a positive edge-triggered D flip-flop with synchronous reset.

3.5.1 The column shift register

The block diagram of Figure 3.17a) shows a serial load shift register comprised of four D flip-flops, interconnected to realize a raster scan reading of a row. SPICE simulation results of a transient analysis of the shift register are plotted in Figure 3.17b).

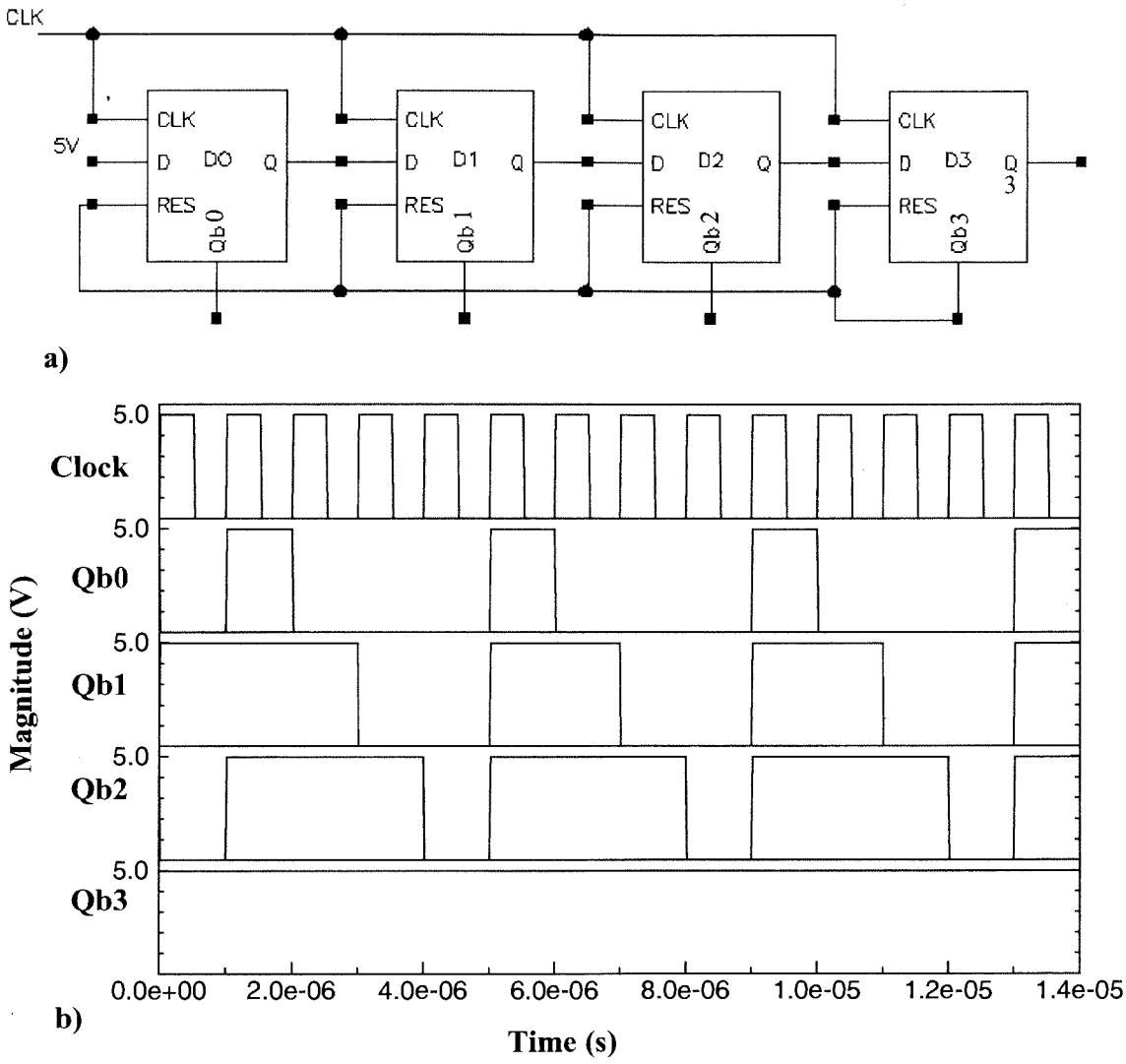

Figure 3.17 a) Block diagram of the column shift register, b) SPICE simulation of the reading sequence.

In continuous reading mode[1], at the beginning of a reading sequence, the inverted output of the D flip-flops are set to a logic level "1". With the input D0 being permanently hooked to "1", the clock propagates a chain of "0s" on the inverted output, connecting, through the SPDT switches, one pair of drains at a time to the CM, thus allowing a current flow in one sensor cell at a time. Once the propagating chain reaches the last flip-flop output of the row, Q3, the whole shift register is automatically cleared and the sequence can start again for the next row.

3.5.2 The row shift register

Essentially, the same serial load shift register is used to control the reading sequence of the rows, the only difference being that only one logic level "1" is propagated instead of a chain, since only one row is active at a time. To realize the continuous reading mode, two extra D flip-flops are added at the end of the shift register, as seen in Figure 3.18a). Once a stray "1" hits the flip-flop D4, outputs of D0 to D3 are cleared, while D4 saves the "1" and feeds it to D5, ensuring that the reset node of D0 to D3 is back to "1" before the saved "1" is applied to input of D0. This results in a first valid reading sequence with only one "1" propagating throughout the shift register. The plot of Figure 3.18b) depicts the row SR reading sequence simulated with SPICE. The inverted ouputs "Qb" feed the driver charging the row gates. In continuous reading mode, since the row SR changes its output state after each reading cycle of the column SR, its clock signal is taken from the non-inverted output of the D flip-flop located before the last one on the column SR.

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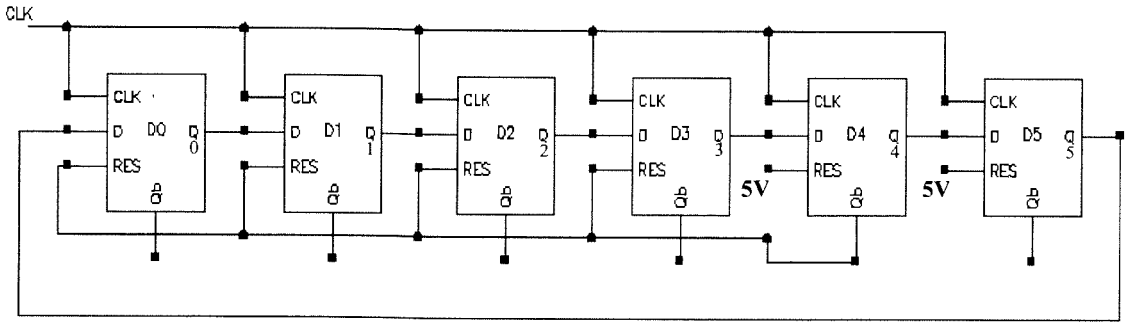
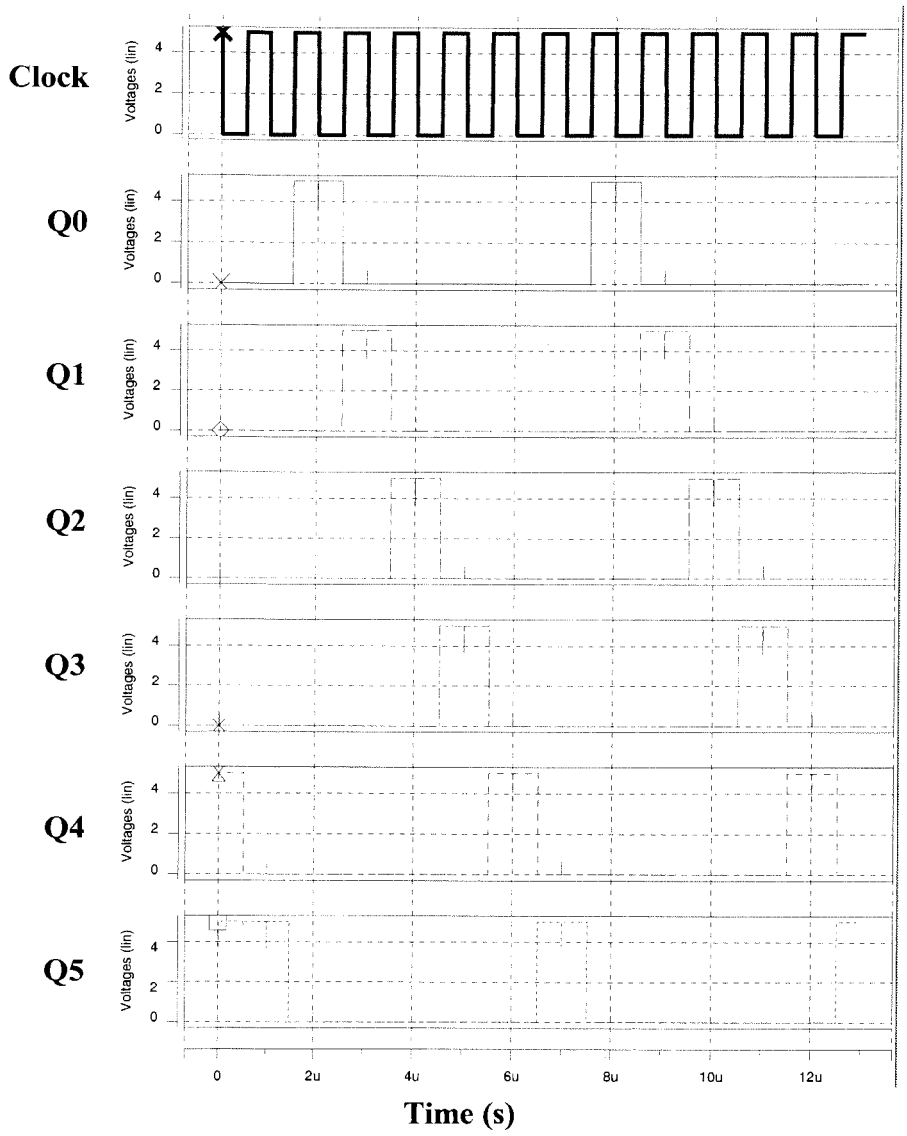
1. The continuous reading mode refers to an interconnection pattern of the column and row shift registers allowing a continuous scanning of the sensor grid. Except for the clock, no external control signal is required. For instance, this mode is employed when visualizing the grid responses through an oscilloscope.



a)



b)

Figure 3.18 a) Block diagram of the row shift register, b) SPICE simulation of the reading sequence.

3.5.3 Column and row shift register restructuring

To every D flip-flop of the column SR (row SR) is attached a pair of SPDTs (a driver). Once either the flip-flop and/or the corresponding pair of SPDTs or driver is faulty, the whole module has to be replaced by its twin located on the other side of the chip. In this case, the signal lines connecting the driver or the SPDTs to the MSCs are cut, and a new module is connected through laser linking. Details of the shift registers restructuring steps will be presented in chapter 6.

3.5.4 Clock skew

In any large integrated system, special care must be taken in routing the clock lines. The clock skew[35] introduced by long clock lines can disturb the cycling sequence of a circuit block and thus generates faults that are not due to wafer processing defects. In order to prevent any problems in the case of the long shift registers of the LAMSA, the clock signal must propagate in the opposite direction as the serial data chain. Thus, we ensure that the input of the flip-flop D(n) is captured before the output of D(n-1) changes.

3.6 Summary

A novel merged double drain/double source MOSFET especially designed for large sensor array applications has been presented. Aided with SPICE simulations, the description of the electrical behaviour of every circuit block composing the LAMSA has been reviewed. Figure A.5 of appendix A presents the layout of the first prototype of the fully restructurable LAMSA chip, including the spare row and column scanning circuit blocks and the spare active loads. Details of the restructuring strategy using the laser link technology will be gradually introduced as needed in the following chapters. Finally, important aspects of the design of the circuit cell layouts have been addressed.

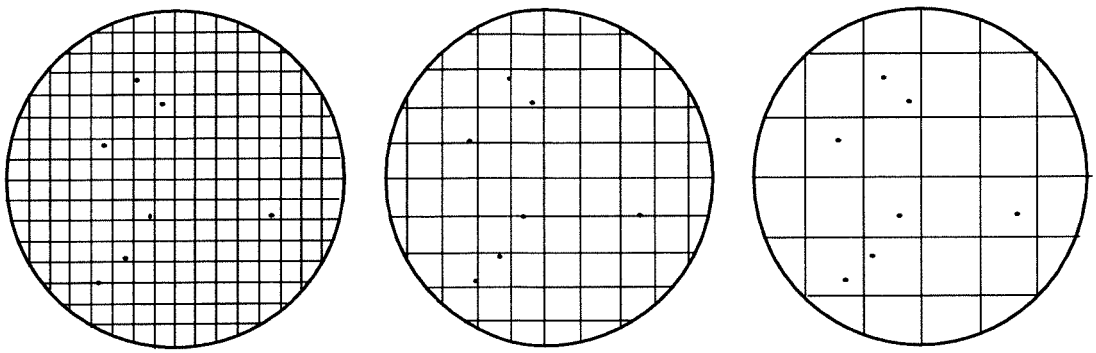
Chapter 4

Yield Improvement

Taking into account the redundancy schemes of chapter 2 and the restructurable capabilities of chapter 3, the yield performance of the LAMSA design can now be evaluated. Specifically, impacts on the yield of different redundancy schemes and restructuring strategies are investigated in this chapter. To accomplish this task, the method consists of determining the yield of the sensor grid and the surrounding control circuits separately. First, an overview of fabrication defect occurrence mechanism and defect distributions in the microelectronic industry is presented, followed by the deduction of an analytical expression used to calculate the yield of the sensor grid. Given the limitations of the method, a Monte-Carlo simulator is developed in the following section. In order to validate the simulation results, simulated and analytically calculated yields are compared for simple cases. Next, yield simulations are performed to evaluate different types of redundancy schemes of the sensor grid and the control circuits. Finally, the best restructuring approach is deduced by considering the yield results and the restructuring technical limitations.

4.1 Fabrication Defects

In the microelectronic industry, the chip yield is limited by defects, a consequence of long fabrication steps where extreme care must be taken to avoid contaminating the wafers with dust or unwanted chemicals. Nevertheless, defects always occur, causing electronic failures on chips that must then be discarded. Figure 4.1 shows three wafers of the same size having the same defect locations (represented with black dots) and three different die sizes. As can be seen from left to right, as the die size increases, the yield decreases markedly. In fact, in today's state of the art microelectronic industry, the situation is not that dramatic, due to a tendency for defects to gather together. This effect, called clustering, is responsible for the higher yield, observed on large chips, than that predicted by simple yield models using random defect distributions[36]. Intuitively, clustering can be easily understood, since in the case of dust, particles rarely travel alone, they usually originate from one source and they scatter in a cloud. Moreover, in the case of thin film defects, it is likely that a defect in a layer will affect the subsequent layers to be deposited on top. Hence, there is a high probability that the region of the original defect will become clustered with defects.



Yield = 95% **Yield = 86%** **Yield = 62%**

Figure 4.1 Effect of the die size on the yield.

To date, the defect distribution best representing the yield trend observed in the industry is the following negative-binomial distribution[37]:

$$P(x) = \frac{\Gamma(\alpha + x)}{x!\Gamma(\alpha)} \frac{(A\lambda/\alpha)^x}{(1 + A\lambda/\alpha)^{x+\alpha}} \tag{4.1}$$

where $P(x)$ is the probability of having x defects in a defect sensitive area A; $\Gamma()$ is the gamma function; λ is the defect density per chip area A; and α, the clustering parameter. In order to obtain an accurate yield prediction with equation (4.1), a distribution must be evaluated for each type of fabrication defect; then, the final yield is obtained by multiplying the probabilities given for x equals 0 defects[38]. Unfortunately, this method is not easy to access since extensive statistical data over several wafer lots of a dedicated process are required. Moreover, such data are often proprietary information and of limited access. However, according to the results of Stapper and Rosner obtained on Read Only Store chips[39], it is possible to achieve reasonably good fits with a simple yield model using equation (4.1), where λ expresses the number of electric faults per cell. This technique is employed specifically for designs made of mainly one type of cell such as memory circuits and sensor arrays. By doing so, the fault distribution modeled encompasses the effect of all defect distributions.

4.2 Analytical Yield Expression for the Sensor Grid

In order to evaluate the robustness of the sensor grid redundancy schemes, two types of faults are defined, each having their respective probability represented by the negative binomial distribution. The first encompasses faults due to defects affecting the **sensor element**, being defined as a sensor cell without the connecting drain and gate signal lines. Examples of such faults include:

- Shorts between the polysilicon gate and the P-well.

- Shorts between the polysilicon gate and drain diffusions.

- Shorts between drains.

The second fault distribution deals with defects affecting drain and gate **signal lines** connecting the sensors to the surrounding control circuits. These faults are generally produced by:

- Metal 1 and metal 2 line shorts and opens.

- Via and contact failures.

Both fault densities, λ_{se} (sensor element) and λ_{sl} (signal line), are expressed in terms of the number of faults per sensor cell. Hence their respective probabilities are given by:

$$P_{se}(n, x_{se}) = \frac{\Gamma(\alpha_{se} + x_{se})}{x_{se}!\Gamma(\alpha_{se})} \frac{(n\lambda_{se}/\alpha_{se})^{x_{se}}}{(1 + n\lambda_{se}/\alpha_{se})^{x_{se}+\alpha_{se}}} \tag{4.2}$$

$$P_{sl}(n, x_{sl}) = \frac{\Gamma(\alpha_{sl} + x_{sl})}{x_{sl}!\Gamma(\alpha_{sl})} \frac{(n\lambda_{sl}/\alpha_{sl})^{x_{sl}}}{(1 + n\lambda_{sl}/\alpha_{sl})^{x_{sl}+\alpha_{sl}}} \tag{4.3}$$

where x_{se} and x_{sl} represent the number of faults, and n the number of sensor cells included in the calculation.

The yield expression of a pixel for the signal line type of fault is now deduced, under the redundancy scheme conditions presented in Figure 2.4 and Figure 2.5. Figure 4.2 depicts the redundancy schemes at the sensor cell and the pixel levels. First, the yield of one sensor cell is evaluated. A sensor cell defines an area including one sensor element and both gate and drain signal lines located on top or beside this element. In the case of Figure 4.2, each sensor cell (MSC) comprises three possible drain line connections for each left and right drain pair, and two possible connections to the gate lines, meaning that

up to three signal line faults can occur within one sensor cell without disabling it.[1] The sensor cell yield, Y_{cell} is then given by:

$$Y_{cell}(n) = \sum_{\binom{allfixable}{patterns}} P_{sl}(n, x_{sl}) \tag{4.4}$$

Hence equation (4.4) becomes:

$$Y_{cell}(1) = P_{sl}(1,0) + P_{sl}(1,1) + \frac{21}{28}P_{sl}(1,2) + \frac{18}{56}P_{sl}(1,3) \tag{4.5}$$

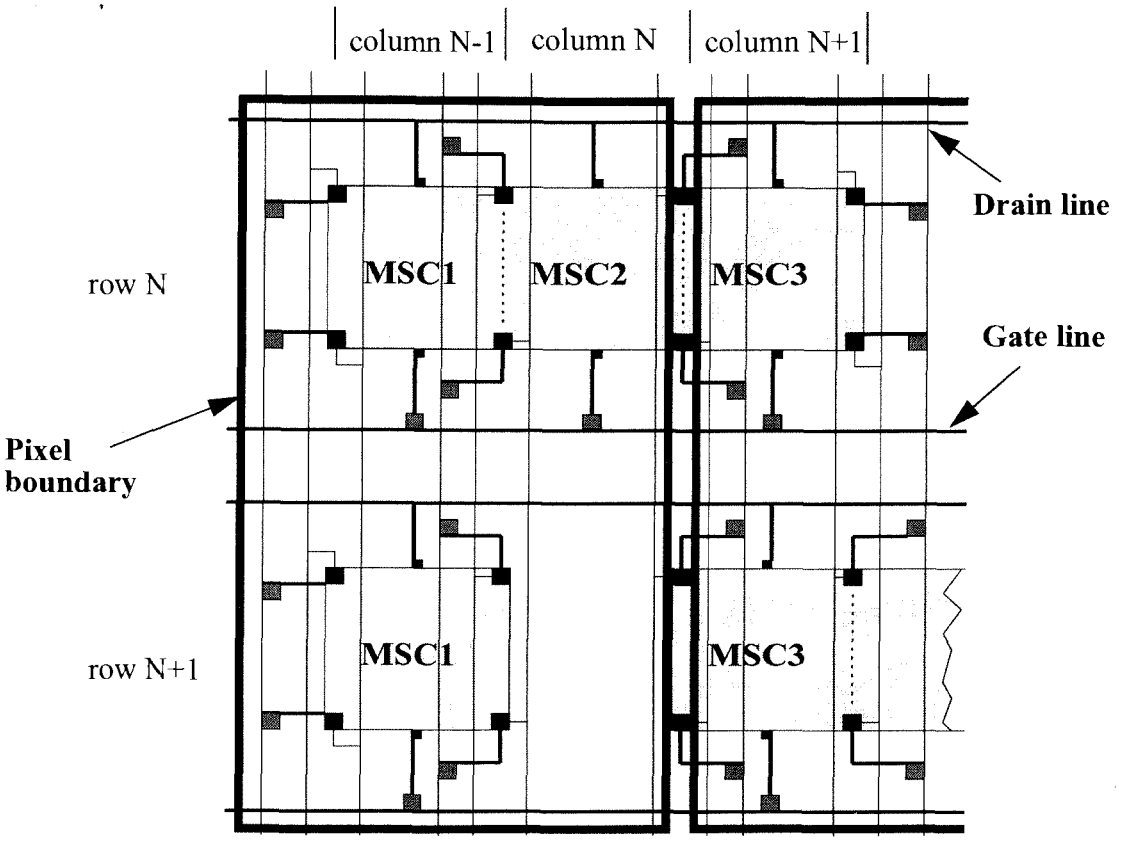


Figure 4.2 Detail of the sensor grid redundancy.

Factors before P_{sl} terms are ratios of fixable fault patterns over the total number of available patterns depending on the number of faults, x. The pixel yield can now be

1. It should be noted that for MSCs sharing a subarray of three sensor cells, two gate signal lines can be disabled without disabling the sensor cell, as long as the gate line of the MSCs sharing the same subarray is not defective. This case is not taken into account in this analysis and may lead to a slight underestimation of the yield.

deduced. Referring to Figure 4.2, it has been defined that one sensor cell out of three must be working in order to consider the pixel functional. Since the faults occurring in adjacent sensor cells are dependent, the Inclusion Exclusion principle[40] must be applied, giving:

$$Y_{pix} = Y_{cell}(3) - 3Y_{cell}(2) + 3Y_{cell}(1) \tag{4.6}$$

This relation is valid only if the clustering parameter, α_{sl}, is constant throughout the pixel area. Table 4.1 summarizes the ratios of the fixable fault patterns with respect to the P_{sl} terms required to evaluate equation (4.6).

Number of faults (x)	Fixable patterns / Total patterns		
	$P_{sl}(1,x)$	$P_{sl}(2,x)$	$P_{sl}(3,x)$
0	1	1	1
1	1	1	1
2	$\frac{21}{28}$	$\frac{69}{78}$	$\frac{194}{210}$
3	$\frac{18}{56}$	$\frac{193}{286}$	$\frac{1036}{1330}$
4	-	$\frac{306}{715}$	$\frac{3503}{5985}$
5	-	$\frac{270}{1287}$	$\frac{8013}{20349}$
6	-	$\frac{108}{1716}$	$\frac{12168}{54264}$
7	-	-	$\frac{12042}{116280}$
8	-	-	$\frac{7128}{203490}$
9	-	-	$\frac{1944}{293930}$

Table 4.1 Ratios of fixable fault patterns of P_{sl} terms.

This analysis is valid by virtue of the restructuring capabilities of the laser link technology. Indeed, with a combination of laser links and cuts, it is possible to swap from a drain line to a spare, or from a gate line to a spare within a sensor cell, thus discarding open or shorted lines in the routing. Remaining defect free segments of defective lines can still be employed for rerouting in other sensor cells.

4.3 Monte-Carlo Simulation

This section proposes another approach to finding the yield of the sensor grid by using Monte-Carlo simulations. Monte-Carlo simulations were introduced fifty years ago as a calculation tool to evaluate the outcome of any process evolving by random events. For our specific problem of yield determination, the randomness occurs in the spatial distribution of faults and their amount per cell throughout the entire circuit, specifically among the sensor cells, in the case of our sensor grid.

4.3.1 Generation of the fault distribution

It has been proven mathematically by Koren et al[41] that a negative-binomial distribution is generated when the probability of having a fault in a cell during a time interval Δt is linearly proportional to the number of faults already on the chip. In computation terms, this type of distribution is generated by calculating, for each cell *Ce*[i,j], a probability number, *Prob*, equal to a random number, *Ran*, and a term proportional to the number of faults already included in that cell and its four nearest neighbours[42]:

$$Prob = Ran + Alpha(Ce[i,j] + Ce[i-1,j] + Ce[i+1,j] + Ce[i,j-1] + Ce[i,j+1]) \qquad (4.7)$$

where *Alpha* is a constant. The number *Prob* is then compared to a threshold value, *FaultTh,* between 0 and 1, which *Prob* must be greater than (*Prob* > *FaultTh*) in order to add a fault to the cell *Ce*[i,j]. The algorithm continues until the total number of faults specified for the circuit map is reached.

In order to obtain a good statistical sample, our sensor grid yield model defines a cell map of a hundred sensor grids, each comprising "R" rows and "C" columns of sensor

cells, as shown in Figure 4.3.[1] The simulation program requires, as input, the number of faults per sensor grid, *Ngrid*, the constant *Alpha* and *FaultTh*. Once the program has assigned the 100**Ngrid* faults to the cell map, parameters of the resulting negative-binomial distribution are computed, namely: average fault density per sensor grid, $\hat{\lambda}_{grid}$ [2], and per cell, $\hat{\lambda}_{cell}$, and the corresponding clustering parameters, α_{grid} and α_{cell}. The clustering parameters are obtained from the respective variances, V, and averages of the fault densities[41]:

$$\alpha = \frac{\hat{\lambda}^2}{V - \hat{\lambda}} \tag{4.8}$$

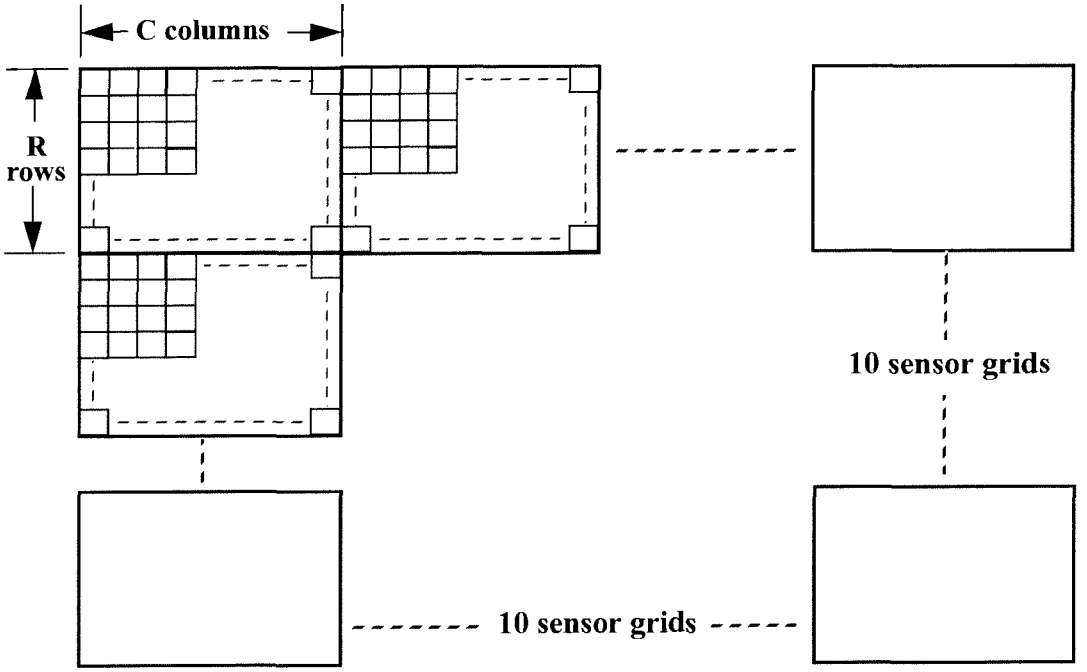
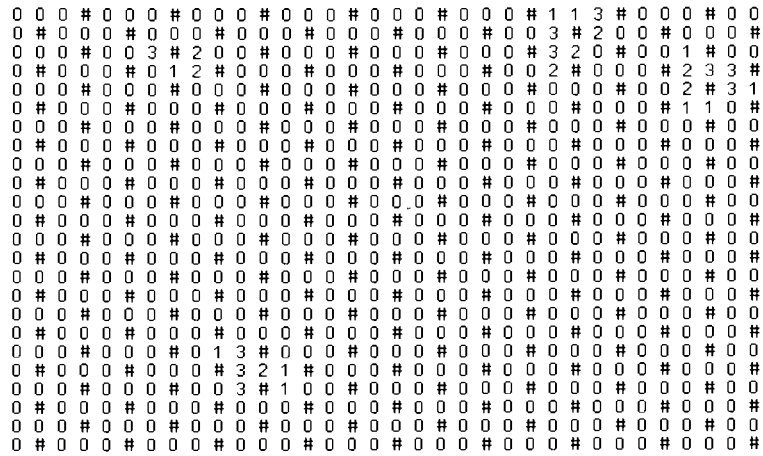


Figure 4.3 Detail of the cell map comprising 100 sensor grids.

Figure 4.4 shows two sensor grid fault patterns, each selected among the one hundred generated from their respective cell maps. The number of faults in each cell is displayed and the symbol "#" stands for blank cells located between the sensor cell

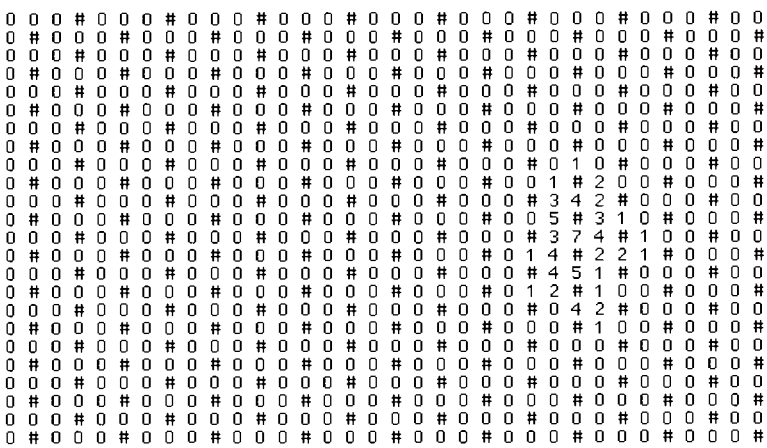
1. For cells located on the edge of the cell map, four neighbours are also included in the calculation of equation (4.7). However, for the four corner cells, only three neighbours are considered.
2. It should be noted that most of the time $\hat{\lambda}_{grid}$ exceeds the input parameter, *Ngrid*, since the faults are distributed through a loop of the type "while{}" where the stopping condition is verified after each complete scanning of the cell map.

subarrays as shown in the pixel redundancy scheme definition of Figure 2.4. Figure 4.4a) represents a pattern with medium clustering, $\alpha_{grid} = 0.986$, whereas Figure 4.4b) reveals a pattern having a stronger tendency for the faults to gather in a group, resulting in high clustering, $\alpha_{grid} = 0.203$. A fault pattern with $\alpha_{grid} \cong \infty$ is characteristic of a Poisson distribution[40], where there is no statistical dependence within numbers of faults of neighbouring cells. The grids are made up of 24 rows and 74 columns comprising 1356 sensor cells and 452 pixels.



a) **Inputs:** $Ngrid = 70$, $Alpha = 0.03$, $FaultTh = 0.99995$

Outputs: $\hat{\lambda}_{grid} = 79.92$, $\hat{\lambda}_{cell} = 0.098$, $\alpha_{grid} = 0.986$ $\alpha_{cell} = 0.021$



b) **Inputs:** $Ngrid = 70$, $Alpha = 0.1$, $FaultTh = 0.999989$

Outputs: $\hat{\lambda}_{grid} = 75.03$, $\hat{\lambda}_{cell} = 0.092$, $\alpha_{grid} = 0.203$ $\alpha_{cell} = 0.064$

Figure 4.4 Sensor grid fault patterns.

4.3.2 Yield computation

Once the fault distribution has been assigned to the cell map, faults of each cell are dispatched randomly. According to the signal line redundancy pattern of Figure 4.2, a fault has a 2/8 chance of affecting the gate signal line due to the two possible gate line connections per sensor cell, and a 3/8 chance of affecting both right and left pair of drains due to the three possible drain line connections per pair of drains. This implies that there is a probability that up to four signal line faults can affect a sensor cell without disabling it, provided that the gate connection of the adjacent sensor cells sharing the same subarray are not faulty. In the case of a single subarray cell of the first column of the even numbered rows, up to three signal line faults can be found without disabling it. Once the dispatching step is executed, the percentage of defective sensor cells and pixels is computed for each of the one hundred sensor grids, and the average results, D_{cell} and D_{pix}, for the whole cell map, are calculated.

In order to compare the Monte-Carlo sensor grid yield model to the analytical yield expression deduced in the previous section, curves of D_{cell} *and* D_{pix} are simulated as a function of the number of faults per sensor grid for a constant grid clustering parameter, α_{grid}[1]. For each point of the curve, the corresponding $\hat{\lambda}_{cell}$ and α_{cell} extracted from the cell map are fed in to the equations (4.5) and (4.6) to calculate Y_{cell} and Y_{pix}, since these expressions are developed at the cell level. Then, the calculated percentage of defective sensor cells and pixels for a grid is simply given by:

$$Dcell(\%) = 100(1 - Y_{cell}) \tag{4.9}$$

$$Dpix(\%) = 100(1 - Y_{pix}) \tag{4.10}$$

1. During the simulation, all distributions giving a value, α_{grid}, outside the limit [desired value] ± 5%, are discarded. Distributions with $\alpha_{grid} = \infty$ are generated by setting the input parameter *Alpha* to zero.

Simulated and calculated D_{cell} and D_{pix} for three sensor grid clustering parameters appear in Figure 4.5. For the graphs representing low a) and medium b) clustering, simulated and

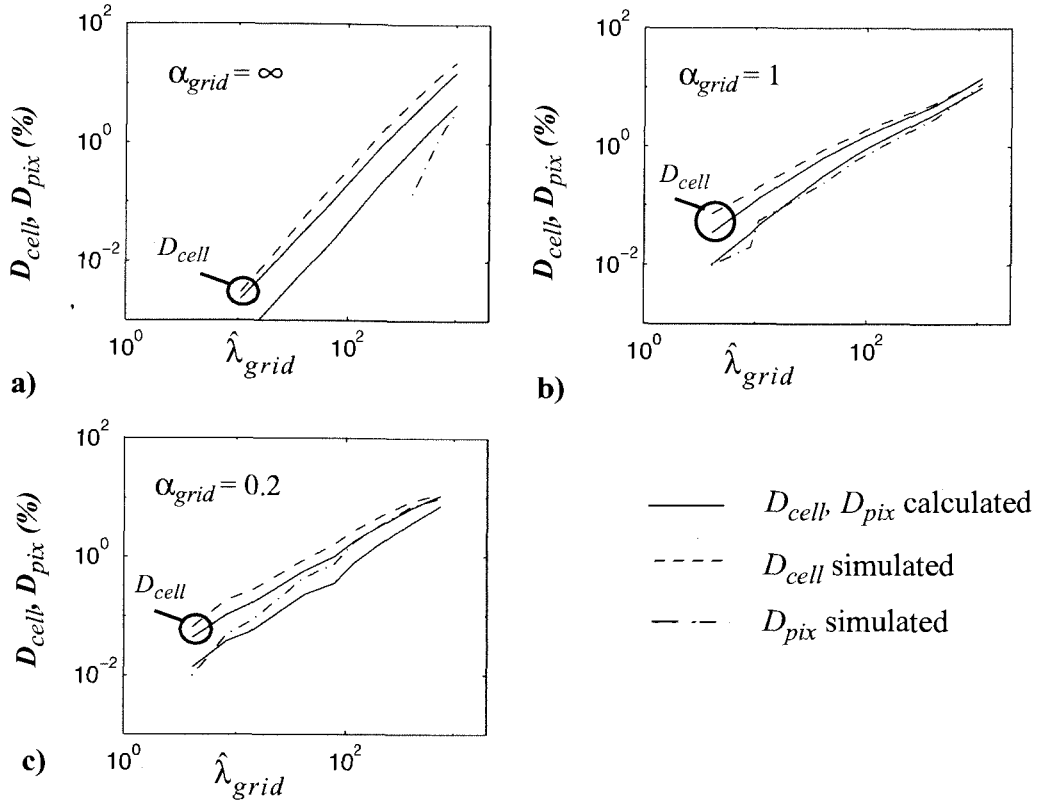


Figure 4.5 Comparison of calculated and simulated yields for three values of clustering.

calculated results follow the same trend, except for D_{pix} at low clustering where the simulated curve is misleading. Since the simulation program can only give integer values of defective pixels for each sensor grid, by omitting partially defective pixels, the true mathematical result is underestimated. Conversely, for medium and high clustering, even at low fault density, chances are that few sensor grids per cell map will have at least one defective pixel, resulting in a more accurate averaging. In the case of high clustering, contrary to the cases a) and b), D_{pix} values calculated and simulated present a high discrepancy for $\hat{\lambda}_{grid} > 10$ faults/grid. This result suggests that α_{cell} is no longer constant throughout the pixel area at high clustering, misleading the analytical results. The slightly

lower D_{cell} observed on the calculated curves for all three cases originates from the fact that some fault patterns disabling one sensor cell will also disable the adjacent sensor cell, in the case where a common pair of drains is defective. This fact is not taken into account in the analytical expression giving Y_{cell}.

Overall, except in some extreme cases, the model is in good agreement with the analysis, validating its utilization as a tool for the following sensor grid and control circuit redundancy scheme investigations of following sections.

The main advantage of using Monte-Carlo simulations resides in the fact that the yield of each circuit block of the LAMSA can be evaluated from fault patterns covering the entire chip. As a result, yields of different circuit blocks under various redundancy schemes can be compared for the same fault distribution parameters per chip. Analytically, yields of each circuit block need to be calculated separately, disabling the dependency relationship between adjacent circuit blocks of different types, shapes and sizes, especially when clustering is taken into account. To meet these modeling demands, the sensor grid map of the previous section is now expanded to include the whole LAMSA system. The simulation output parameters $\hat{\lambda}_{grid}$ and α_{grid} become $\hat{\lambda}_{chip}$ and α_{chip}.

4.3.3 Chip grid definition

In order to form a chip grid with the entire sensor system circuit, a basic cell of size 78 μm by 73 μm has been defined, corresponding approximately to the size of one sensor cell of the final LAMSA prototype. This basic cell includes one and a half pair of drains, as shown in Figure 4.6. Other circuits of the system are defined in term of this basic cell according to their sizes given in appendix A. Table 4.2 summarizes the number of basic

cells assigned for each circuit element. Since the size difference between a given circuit element and its corresponding spare (including the restructuring structures) is small compared to the size of the basic cell, the same amount of basic cells is assigned to each circuit element and its spare.

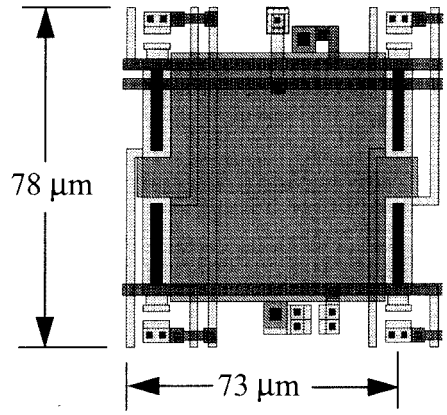


Figure 4.6 Layout of one sensor cell defining the basic cell.

Circuit elements	Dimension (μm^2)	Number of basic cells
Sensor cell	78 x 73	1
CCM	33 x 29	1
pair of SPDTs	54 x 49	1
Driver	216 x 78	3 x 1
D flip-flop	160 x 61	2 x 1

Table 4.2 Number of basic cells assigned to each circuit element.

According to Table 4.2 and the floor plan of Figure 2.2, the chip grid of a LAMSA comprising a sensor grid of 24 rows and 74 columns is defined in Figure 4.7. Since 75 columns of drain pairs are required to access every sensor cell, 75 D flip-flop-SPDT modules are required. Also, the two extra D flip-flops at the end of the row SR are required to operate the LAMSA in continuous reading mode as explained in section 3.4.2. Analogous to the simulation of the cell and pixel yield of the previous section, yields are

computed from maps of one hundred chip grids generated in the same fashion as detailed in Figure 4.3.

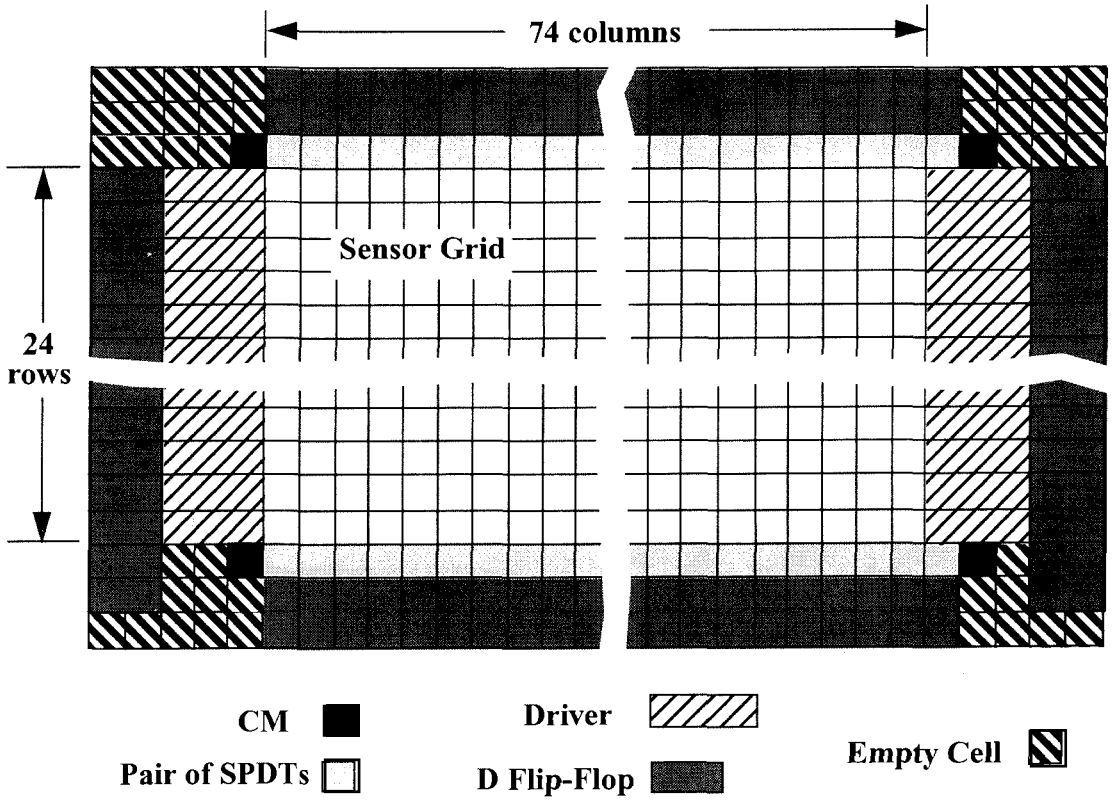


Figure 4.7 Chip grid definition.

4.4 Sensor Grid Redundancy Scheme Comparison

To investigate the effect of the signal line and the sensor element types of faults on the sensor grid redundancy scheme, three patterns of sensor grids are defined. Figure 4.8 depicts the three patterns (1), (2) and (3), made up of subarrays of one, two and three combined sensor cells respectively. For a sensor grid of 24 rows and 74 columns, patterns (1), (2) and (3) include 888, 1188 and 1332 sensor cells respectively, each with the same number of pixels, namely 444. The grid pattern (3) corresponds to the one presented and simulated in the previous section. For each of these sensor grid patterns, Monte-Carlo simulations are performed to investigate separately the effect of signal line and sensor

element fault densities per chip, λ_{chip}, for three values of the chip clustering parameter, $\alpha_{chip} = \infty$, 1 and 0.2.

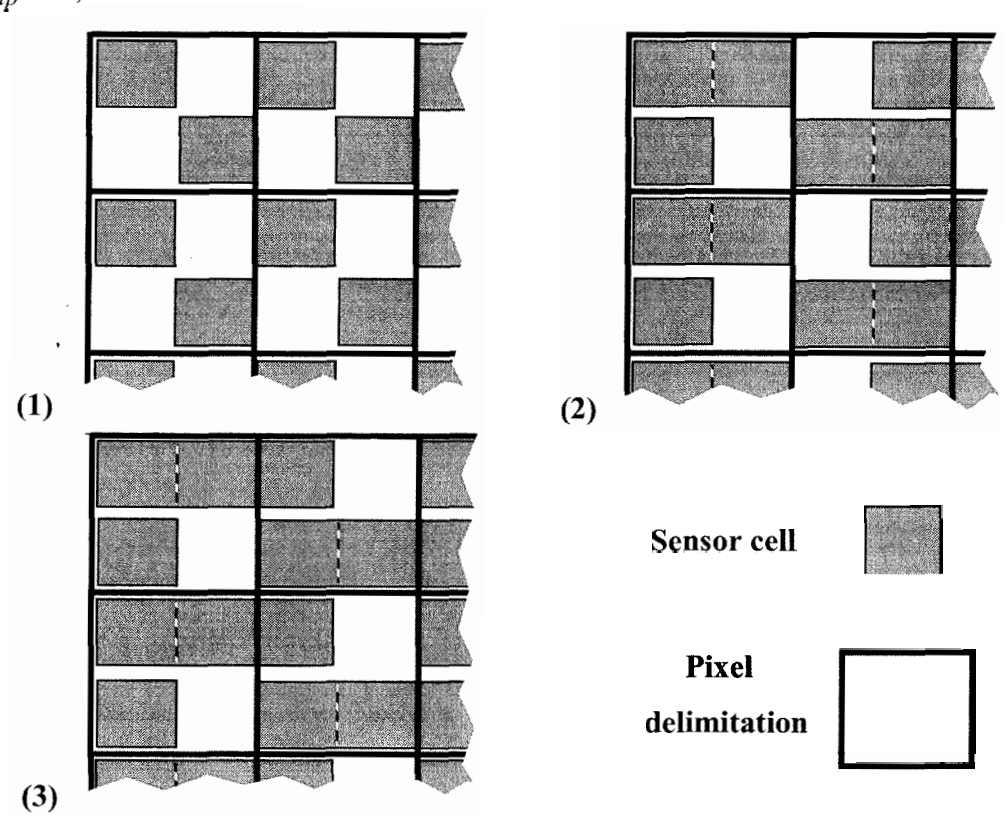


Figure 4.8 Sensor grid patterns comprising subarrays of (1), (2) and (3) sensor cells.

4.4.1 Results for the signal line type of faults

Figure 4.9, Figure 4.10 and Figure 4.11 present the results obtained on the sensor cell and pixel yield simulations for the three grid patterns (1), (2) and (3) respectively. For each grid pattern, simulations were performed on sensor grids having no redundancy and the grids following the redundancy scheme of Figure 4.2 (two spare drain lines and one spare gate line per sensor cell). All three figures present the same trend. Without redundancy schemes, as the clustering increases (i.e. α_{chip} decreases), D_{cell} and D_{pix} increase and converge towards similar values, especially at high fault density. This effect is a direct consequence of the clustering, since as more faults gather in groups, the probability of disabling a pixel increases. The same effect is observed on the curves with

redundancy, although at lower percentages of D_{cell} and D_{pix}. However, a reduction in the yield gain, due to the redundancy scheme, appears as the fault density and the clustering increase. From these results, all three grid patterns exhibit nearly the same robustness towards the signal line type of faults. This suggests that the greater amount of sensor cells per pixel of pattern (2) and (3) is offset by their vulnerability to faults occurring on drain pairs shared by two adjacent sensor cells. Hence, the design robustness at the pixel level remains the same for all three patterns. In the case where applications require a spatial resolution lower than the pixel definition, the grid pattern (1) would suffer from a greater amount of dead spots.

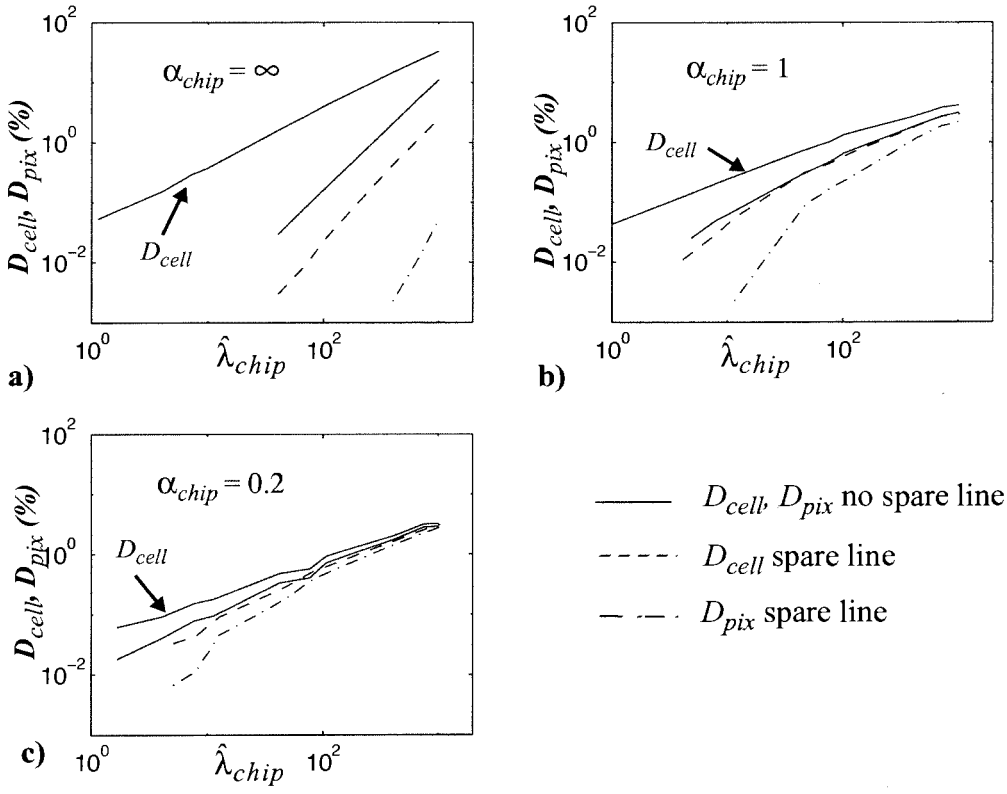


Figure 4.9 Yields comparison for sensor grid pattern (1).

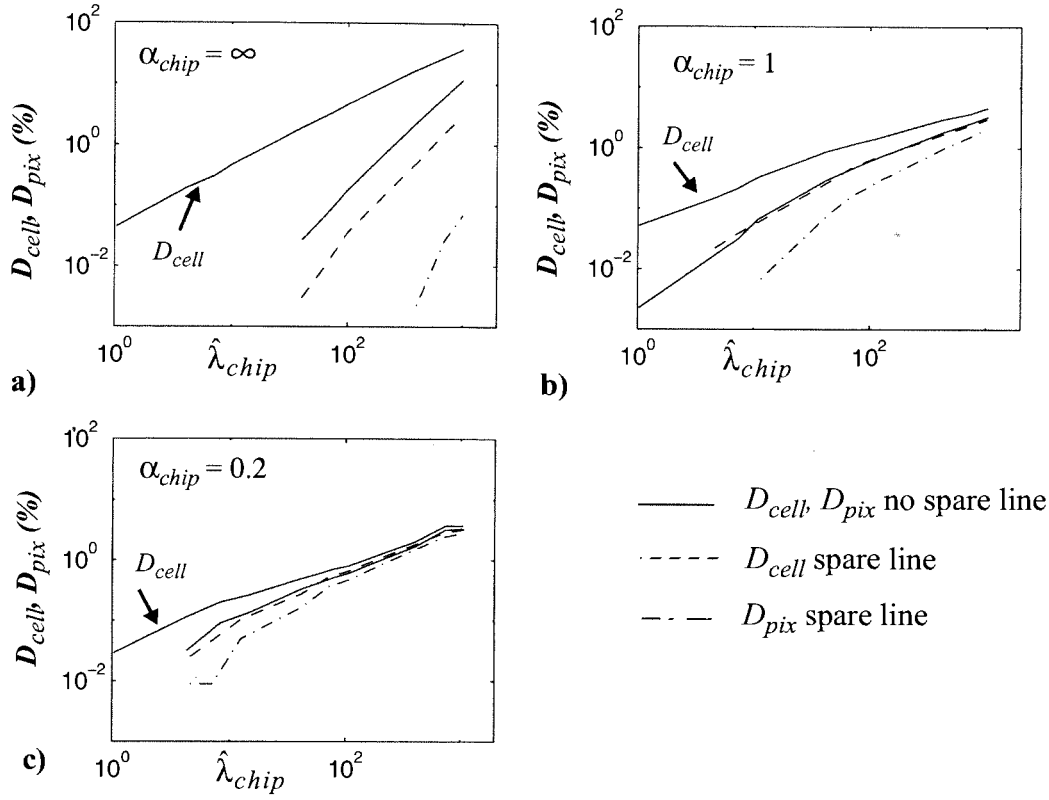


Figure 4.10 Yields comparison for sensor grid pattern (2).

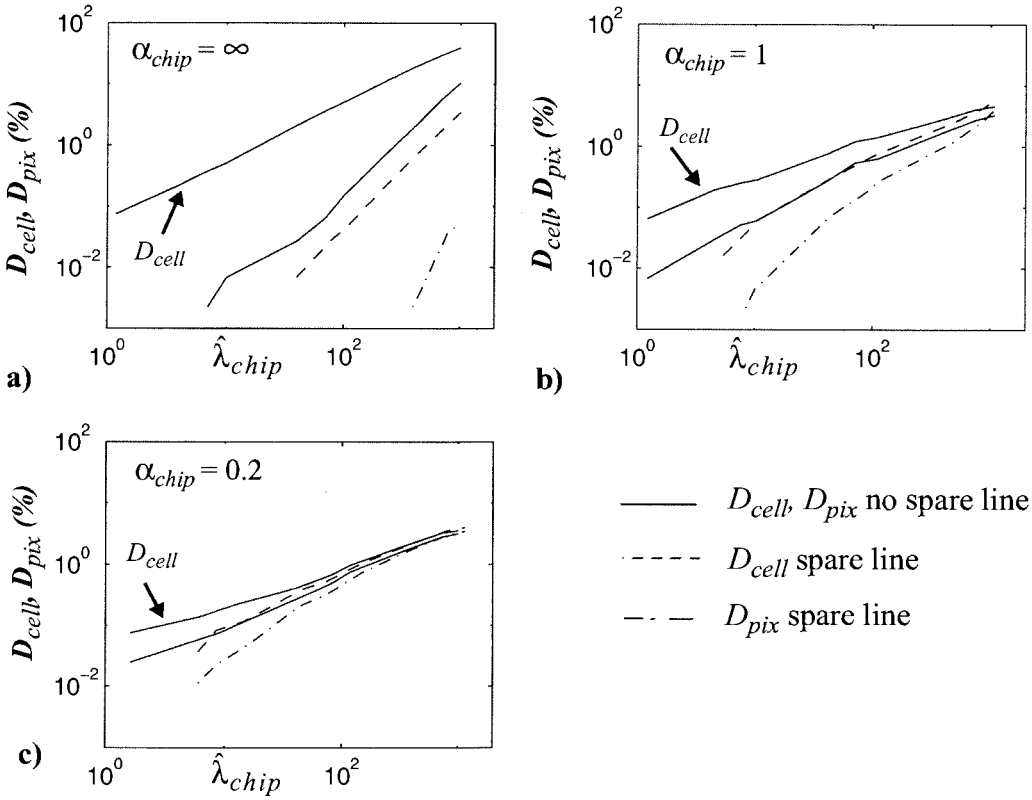


Figure 4.11 Yields comparison for sensor grid pattern (3).

4.4.2 Results for the sensor element type of faults

For this simulation, only faults short-circuiting the gate to a drain or the gate to the P-well are considered. Hence these faults will disable all the sensor cells sharing a common gate.[1]

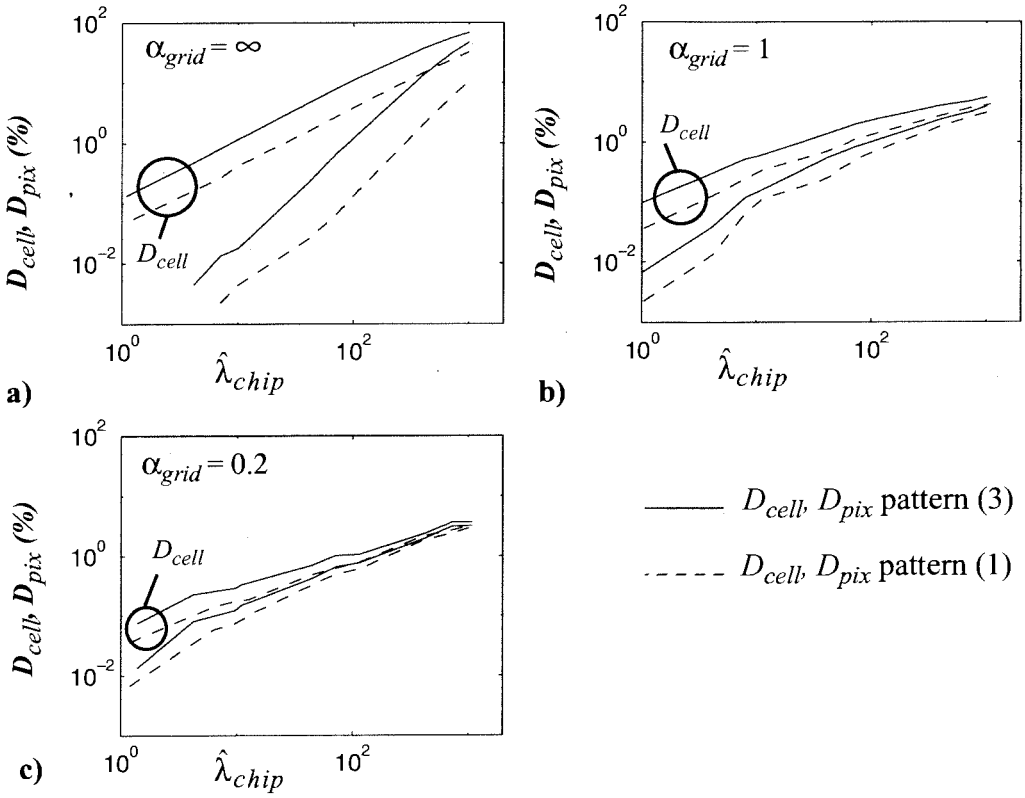


Figure 4.12 Yields comparison of sensor grid patterns (3) and (1).

Figure 4.12 compares the results obtained for sensor grid patterns (3) and (1). Once again for both patterns, convergence of D_{cell} and D_{pix} is observed at high fault density and high clustering. Grid pattern (1) achieves the best yield, although the yield gain decreases as the fault density and the clustering increase, displaying the advantage of having two sensor cells per pixel not sharing the same gate. This yield gain is, however, quickly lost for the pattern having two sensor cells per subarray, as plotted in Figure 4.13. Except for

1. Given the size of the notch (9 μm) separating adjacent drains on the MSCs of our prototype implemented in CMOS 1.5 μm technology, faults short-circuiting two adjacent drains are not likely to happen.

graph a) with no clustering, where pattern (2) exhibits slightly better yield, curves D_{cell} and curves D_{pix} follow nearly the same trend. These results demonstrate that fewer sensor cells per subarray provide better robustness against the sensor element type of faults, especially at low clustering.

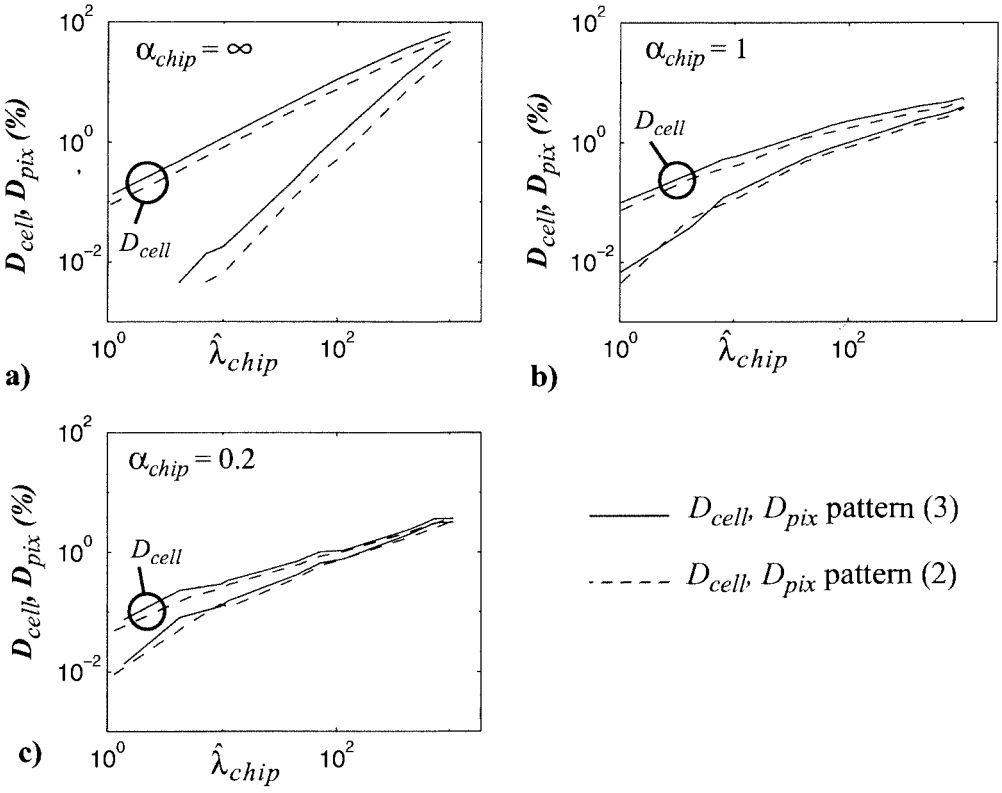


Figure 4.13 Yields comparison of sensor grid patterns (3) and (2).

4.4.3 Summary of the sensor grid redundancy scheme comparison

Overall, the three sensor grid patterns present very similar robust behavior towards the signal line type of fault. The addition of a spare signal line per pair of drains and a spare gate line improves the robustness for any fault density scenario. However, patterns where fewer adjacent sensor cells share the same gate have been proved more robust to sensor element type of faults. Enlightened by these results, in the case of a large sensor system, the designer choice of a sensor grid pattern with or without redundancy schemes

should consider not only the spacial resolution and the design performance required for a specific application, but also the robustness of the design to fabrication process defects.

4.5 Readout Circuits Redundancy Schemes Comparison

The Monte-Carlo generated fault maps are now used to evaluate the robustness of different redundancy schemes of the readout circuits. Figure 4.14 shows three restructuring schemes devised to overcome a faulty cascode current mirror a), a faulty segment in the row shift register b) and a faulty segment in the column shift register c). In the case of Figure 4.14a), the faulty current mirror is simply replaced by a spare by cutting its connections to the reading bus with the laser, and connecting the spare through laser links. As shown in the chip grid definition of Figure 4.7, to each pair of SPDTs is combined a bit segment of the shift register, made up of a D flip-flop. The combined D flip-flop-SPDTs is then called a column scanning module. Similarly, to each bit segment of the row shift register is attached a driver to form a row scanning module. To achieve better robustness of the scanning circuits, the whole column scanning circuit is segmented in groups of modules fully restructurable with spare twin groups located on the opposite side of the sensor grid. Thus, the serial scanning signal can alternate from one working segment to another on either side of the sensor grid, as illustrated in Figure 4.14b). A similar tactic is employed for the restructuring scheme of the row scanning circuit, as shown in Figure 4.14c). Details of the restructuring sequence using the laser link apparatus will be given in chapter 6.

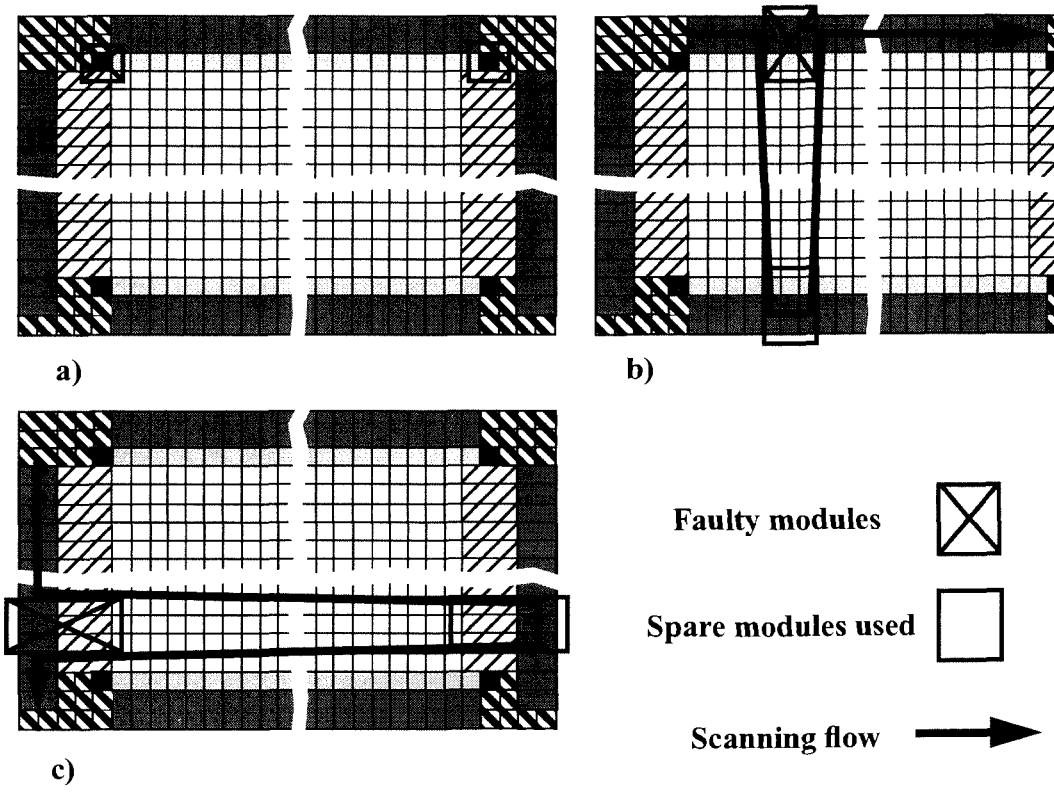


Figure 4.14 Restructuring examples of active load and scanning modules.

4.5.1 Yield computation

From the one hundred chip grid fault maps generated with the Monte-Carlo algorithm, the yield of the three control circuits (the current mirror, the column scanning circuit and the row scanning circuit) are computed as follows. For each chip grid fault map, the CM is considered faulty when all four redundant CM cells are hit by a fault. The CM yield is then given by subtracting the number of chip grids having four CM cells faulty from one hundred, the total number of generated chip grid fault maps.

In the case of the column scanning circuit, the yield is computed in two steps. First, when a fault hits a basic cell which either has the control bus or the reading bus travelling through it, an algorithm determines whether the fault affects the bus or the rest of the circuit associated with the basic cell. The fault dispatching is based on the ratio of

the cell area taken by the bus. Figure 4.15 illustrates the details of the fault mapping. For the LAMSA prototype, the cell area ratio taken by the reading bus travelling through the pair of SPDTs' basic cell is 0.077, and the cell area taken by the clock and reset lines on the basic cell making the lower half of the D flip-flop is 0.051. Secondly, in order to have a working column scanning circuit, each scanning module or its corresponding spare on the opposite side of the sensor grid has to be non-faulty, as shown in Figure 4.14b). In addition, reading and control buses have to access every scanning module forming the complete scanning circuit.

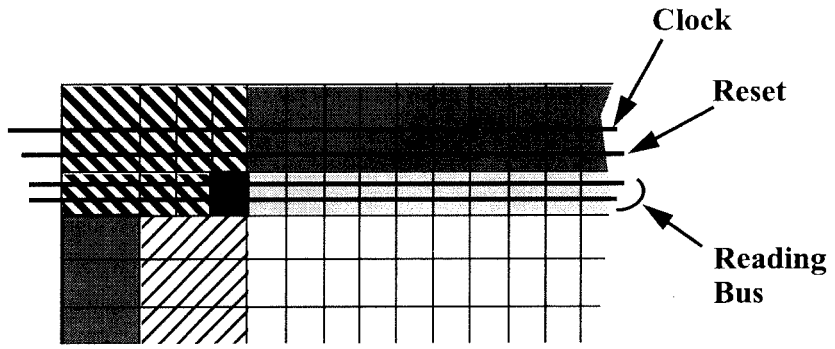


Figure 4.15 Details of the column scanning circuit used for yield computation.

The same approach is employed in the case of the row scanning circuit, except that only the clock and the reset lines are taken into account in the fault dispatching, as seen in Figure 4.16.

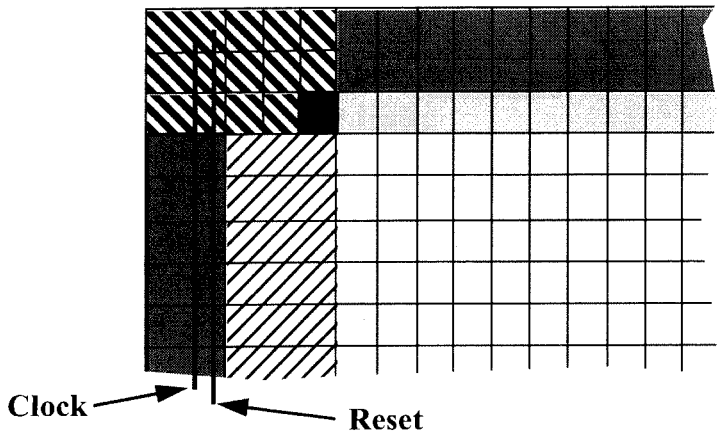


Figure 4.16 Details of the row scanning circuit used for yield computation.

4.5.2 Simulation Results

Analogous to section 4.4, where the robustness of different sensor grid redundancy schemes are evaluated, Monte-Carlo simulations are performed here to verify the robustness of the redundancy schemes of the CM, the column scanning circuit and the row scanning circuit versus the fault density and the clustering level of the fault distribution. In addition to these parameters, in the case of the column and row scanning circuits, a parameter called "grouping" is taken into account in the evaluation of the circuit robustness. The grouping is defined as the number of column or row scanning modules grouped together to form restructurable segments. The goal of these segments is to reduce the number of rerouting lines that allow the scanning flow to propagate from one side of the sensor grid to the other. Hence, the grouping fixes the minimum number of scanning modules that have to be restructured whenever a fault on either scanning circuit is discovered. For instance, the restructuring schemes of Figure 4.14b) and c) show a column and a row grouping of three modules.

The simulated yield of the CM, Y_{cm}, was 100% for fault densities lower than approximately 700 faults/chip, and for the three clustering parameter values 0.2, 1 and ∞. For fault densities higher than 700 faults/chip and the same three values of clustering, Y_{cm} was oscillating between 99% and 100%. These results prove the effectiveness of the CM redundancy strategy in terms of functionality. However, parametric shifts of the CM characteristic could render a functioning cell useless and hence decrease the overall Y_{cm}.

Figure 4.17 presents the results of the product of the column and the row scanning circuit yields, $Y_{col}*Y_{row}$, for three values of clustering, α_{chip} = 0.2, 1 and ∞, and three values of grouping gr = *1, 4* and *8*. A major trend observed is the reduction of the

robustness of any redundancy scheme at low clustering. Due to the large area covered by the scanning circuits located in the periphery of the chip, faults distributed uniformly throughout the chip have a higher probability of defeating the redundancy scheme. This effect is also observed on the grouping strategy where higher values of grouping, meaning larger scanning segments, are more vulnerable to faults, especially at low clustering.

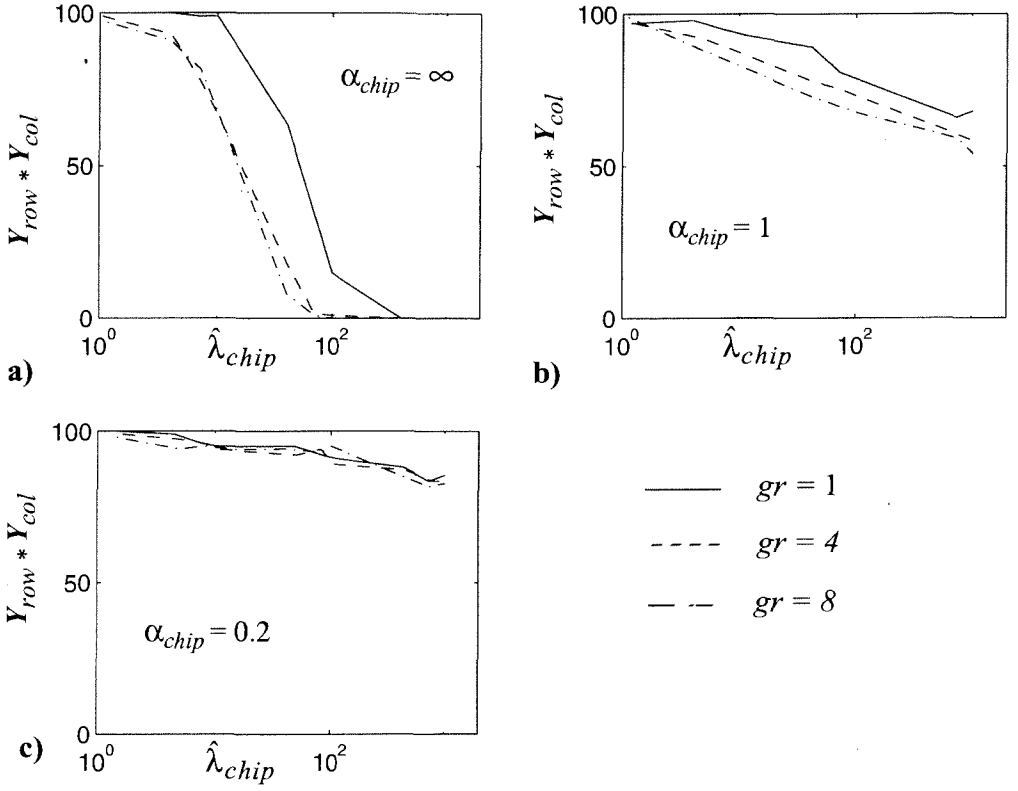


Figure 4.17 Comparison of the product of the column and the row scanning circuit yields.

Figure 4.18 distinguishes between the column and the row scanning circuit yields for the same values of clustering and grouping than Figure 4.17. A similar trend is observed for both circuits as a function of the clustering. However, Y_{row} is slightly lower than Y_{col} except for the graph at no clustering for $gr = 1$. This effect is caused by the larger size of the row scanning modules. Due to the size of the driver, the row scanning modules

are two basic cells wider than the column scanning modules, making each row module more vulnerable to faults. This tendency, however, is reversed when the most robust redundancy scheme *(gr* = 1) is employed at no clustering, where the longer length of the column scanning circuit is an easier target for faults distributed uniformly across the chip.

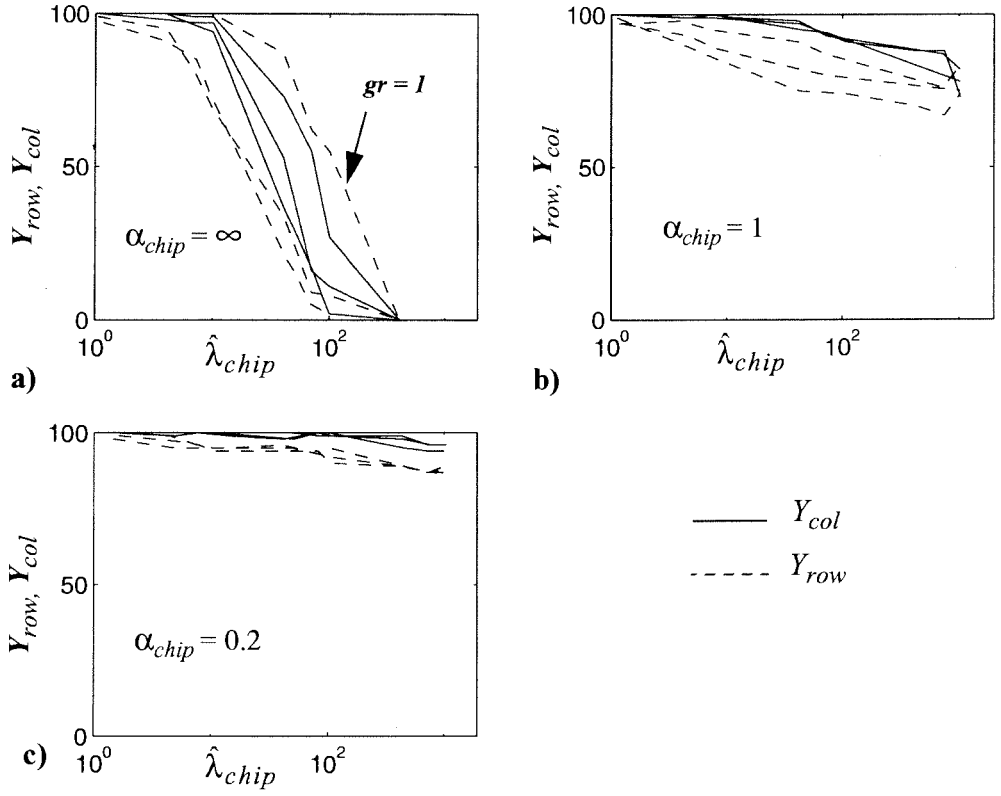


Figure 4.18 Separation of the column and the row scanning circuit yields.

4.5.3 Summary of readout circuits redundancy schemes comparison

The redundancy scheme of the CM has been proven effective for faults destroying the functionality. With this circuit being a key component affecting the sensitivity of the whole sensor system, test results will give valuable information about the uniformity of its parameters from spare to spare across the same chip. Thereafter, the overall robustness of this redundancy strategy, including parameter shifts, will be evaluated. A scanning module grouping number of one has been proven to be the most robust redundancy scheme for the

row and the column scanning circuits. However, this scheme requires one rerouting line connecting each twin scanning modules, which can be realized only in the case of CMOS processes having three metal layers. For the first LAMSA prototype, fabricated in a double metal process, a more conservative grouping strategy is used since the rerouting has to be made off-chip through a limited number of output pads. Results have shown that clustering, which occurs in VLSI CMOS processes[36], narrows the yield difference among the groupings. Hence, slightly lower yields would be obtained by using a more conservative grouping strategy.

4.6 Summary

In this chapter, integrated circuit yield demeanors have been presented in conjunction with their mathematical expressions. The negative-binomial distribution, proved to be the best analytic function relating defect density to yield in the microelectronic industry, has been selected as the fault distribution for the yield study of this chapter. Since analytic yield calculations are not suitable for chips made of different types of cells, a Monte-Carlo simulation algorithm has been developed. Analytic yield results obtained from calculations made solely on the most symmetric part of the LAMSA, the sensor grid, have been found in good agreement with Monte-Carlo simulated yield results performed on that same circuit part. These results have proven the capability of the Monte-Carlo algorithm to generate fault distribution following the negative binomial distribution. Subsequent simulations involving the whole LAMSA system, broken down in basic mapping cells, have enabled the evaluation of the robustness of proposed redundancy schemes for the sensor grid and the readout circuits. Results have demonstrated that spare signal lines on the sensor cell increase the yield independently of

the sensor grid pattern. Also, patterns having fewer adjacent sensor cells sharing the same gate have been proven more robust to faults affecting the sensor element only, excluding the signal lines. The redundancy scheme of 4 to 1 employed for the CM has been very effective when applied to a simulated scenario; however, its true robustness will depend upon the range of variation of its parameters from spare to spare on a real device. The most effective row and column scanning circuit redundancy scheme has been obtained for module groupings of one. However, due to the large amount of rerouting lines that such a scheme implies, for designs made with double metal processes, a feasible approach would be achieved by using larger groupings. According to the simulation results, larger groupings decrease the yield only slightly when the defect distribution presents clustering.

The objective of this chapter is to develop a simulation tool to help finding a robust redundancy strategy against a variety of fault distributions. Some potential yield problems are not covered by the model, such as power shorts. Although the redundancy scheme for control circuits could overcome this type of fault, cases may occur where it can not be avoided due to its location or due to faults in the restructuring path. Also, in the case of the current mirror, parametric shifts causing chip failure are not taken into account in this purely defect oriented model. For all these reasons, and especially for the absence of defect distribution parameters from the Mitel 1.5 μm process, such as defect densities and clusterings, it is impossible to effectively compare the yield simulations to experimental yield results obtained on the LAMSA.

Chapter 5

Sensor Grid Parameters Extraction

Keeping in mind that the main objective of the thesis is to prove experimentally that the redundancy schemes employed for the LAMSA system enhance its final yield and do not alter its performance, chapter 5 introduces the hardware and software tools used to measure, optimize and evaluate the performance of the LAMSA chips. First, the test methodology is presented with a description of the software tools conceived to process the raw data. The sensor grid raw response distribution is explained using the analytical calculation developed in chapter 3 along with some measured parameters. Finally, a calibration method for the sensor grid response is developed and employed to evaluate the repeatability of the test apparatus and the sensor system.

5.1 Measurement Apparatus

At the heart of the measurement system is the multifunction analog/digital board

for PCs, AT-MIO-16D, designed by National Instruments Corporation. The board is comprised of 16 digital input/output channels, eight single input analog channels and two analog output channels. The eight single analog input channels can be modified into four differential input channels. The test programs were written in C^{++} using the input/output subroutines provided with the board. Digital output channels 0 to 3, analog differential input 0 and analog output channels 0 and 1 were used for the three test programs developed to verify the LAMSA functionality. Details of the specific functions of the input/output channels will be given in the next section. From the PC, a flat ribbon cable is linked to a connection box, dispatching the signals to a circuit board including a 68 Pin Grid Array zero insertion force socket to insert the device undergoing testing. The circuit board is suspended between the coils, with the socket positioned in the centre of the constant magnetic field region, perpendicular to the field direction. The magnetic field was generated and measured with the equipment described in section 3.1.1.

5.2 Measurements

5.2.1 Verification with an oscilloscope

The first step performed in the testing of the LAMSA consisted of merely verifying its basic functionality with an oscilloscope. By connecting the device in continuous reading mode, as mentioned in section 3.5.1, the output Da and Db can be visualized through the oscilloscope. Dead sensor cells, a faulty current mirror and faulty row and column scanning circuits are immediately discovered through the waveform display. Figure 5.1 summarizes the output/input connections required to set the chip in continuous reading mode. Figure 5.2 illustrates a typical signal waveform produced during the scanning of the sensor grid. It represents the signal obtained during the scanning of a

subarray of three sensor cells delimited by two blank cells. Since a blank cell is only a gap between two pairs of drains where no MAGFET has been drawn, no current can flow from the current mirror to the ground during this sequence. This enables the charge of the reading line Da to reach 4.5 V, beyond which the current mirror ceases delivering currents. Once the reading sequence reaches the left most sensor cell of the subarray, Da drops to about 1.9 V, as identified in the SPICE simulation of Figure 3.10, when VGref equals 5V. The voltage level decreases slightly for each of the two following sensor cells due to the added parallel current paths, when the subsequent pairs of drains are pulled to the current mirror. Due to the decrease in resistivity of the current path, a slight shift in the voltage at the output Da is produced. This shift is in the order of 20 mV for each added cell. The shape of the voltage peak associated with the reading of a blank cell is strongly dependent on the device clock frequency, setting the charge time duration of the reading lines. The frequency corresponding to the waveform drawing of Figure 5.2 is about 1 kHz. Without a magnetic field, Da and Db outputs have similar voltage swings.

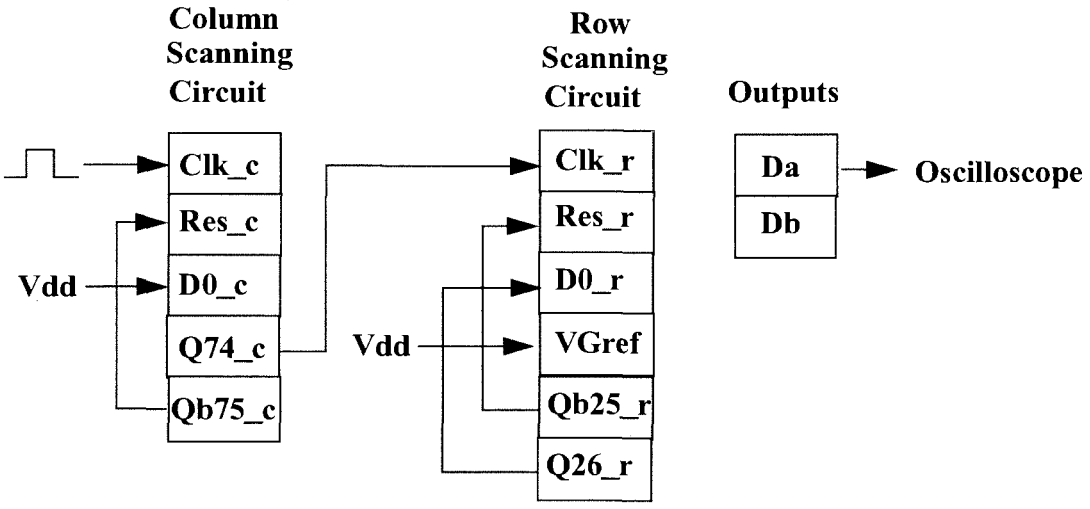


Figure 5.1 Input/output interconnections for reading with an oscilloscope.

By increasing the oscilloscope time base, a few rows and different sections of the

sensor grid can be visualized on the screen. Also, by externally triggering the oscilloscope time base sweep with the output signal Q26_r and adjusting the trigger delay, the voltage waveform produced by specific rows or group of sensors within a row can be displayed.

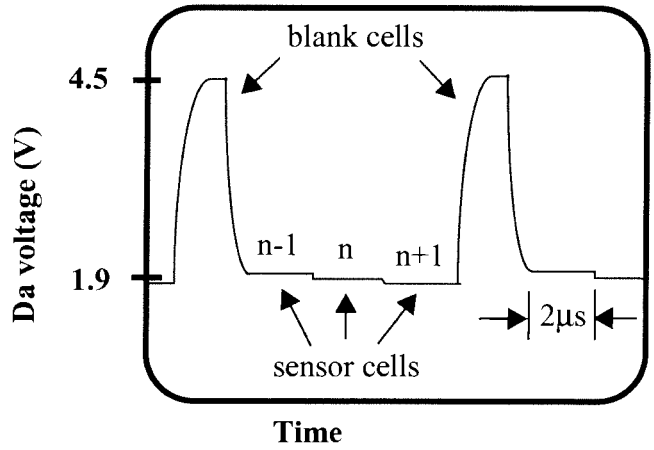


Figure 5.2 Oscilloscope reading at the output Da.

5.2.2 Determination of the biasing voltage for the maximum sensitivity

The multifunction A/D board is now used to find the optimum biasing voltage, VGref, that will allow the sensor grid to be the most sensitive.

Figure 5.3 illustrates the input/output interconnections involved in the measurement of the optimum VGref. Connections Dout0 to Dout3 corresponds to the digital output channels of the A/D board. Aout0 and Ain0 are an analog output and a differential analog input of the A/D board respectively. R1 and R2 are two resistors used to reduce the discrepancy among the sensor cell responses. Details on how the values of those resistors have been determined are given in the next section.

Figure 5.4 plots the 4 sequences generated by a C^{++} algorithm in order to read the responses of the sensor cells of a specific row, submitted to a voltage sweep at the input VGref. Sequence (1) resets all the row gates to 0V. It is repeated 24 times within a "*for*"

loop statement, to enable the "0" level fed in the serial input, D0_r, of the row shift register, to reach every row gate. Next, sequence (2) resets the column shift register outputs and activates the first row of sensors by feeding in a "1" in the serial input D0_r. The following sequence, (3), propagates the level "1" of the row shift register, stopped at the first row, to the selected row to be measured. It is repeated a number of times (N-1), where N is the specific row number to be measured. The last sequence, (4), sweeps the voltage VGref in order to find the optimum value producing the highest sensitivity. The voltage ramp varies from 0.7 V to 1.7 V, covering the sensor high sensitivity region as expected from the SPICE simulation results of Figure 3.10. The sweeping step is 0.02 V and the measured value at the differential outputs Da minus Db, is taken from the averaging of four readings at each step. The total sweeping time is about 500 ms while the period of the digital sequencing signals is approximately 10 μs. This sequence is repeated 74 times for the 74 columns of sensors. In order to remove the fixed pattern noise from the response, as mentioned in section 3.3, two sets of measurements, one with a magnetic field of 1800 G and another without magnetic field, are taken and subtracted from each other. Hence, the resulted set represents the response due solely to the magnetic field effect.

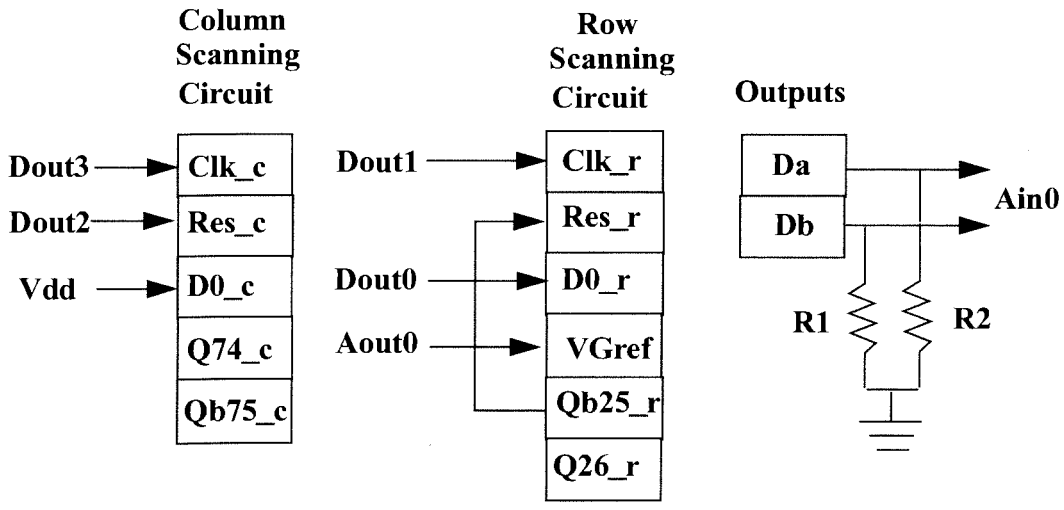


Figure 5.3 Input/output interconnections for biasing voltage determination.

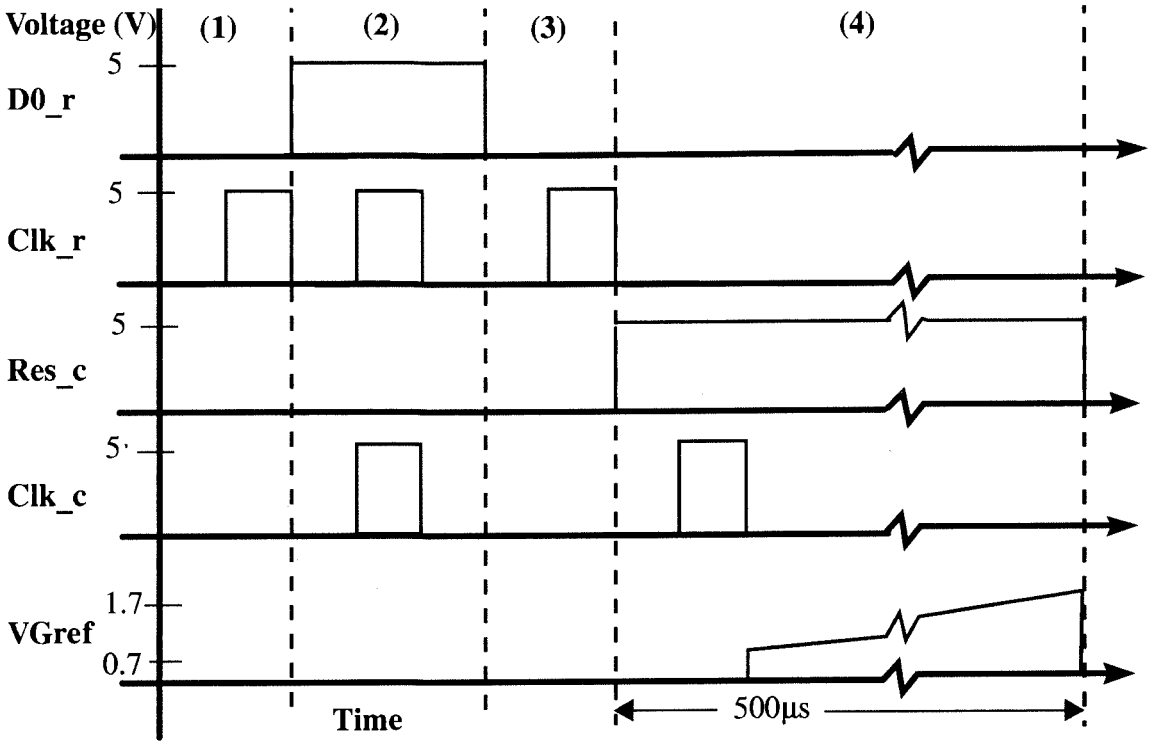


Figure 5.4 Timing sequence employed to determine the optimal biasing voltage.

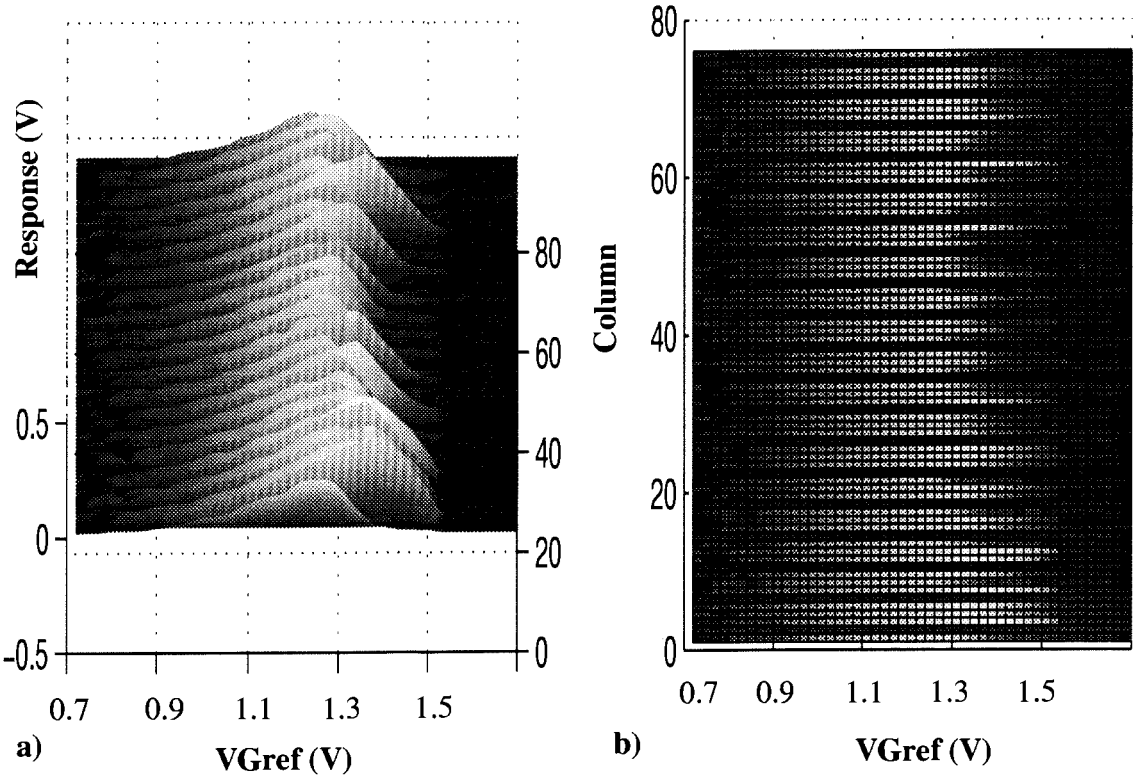


Figure 5.5 a) Three dimensional plot of the sensor cell responses of row number 12 of chip CA8-5 as a function of the voltage (VGref). b) Bird's-eye view of a).

Figure 5.5 presents two mesh diagrams of the magnetic field response as a function of the biasing voltage VGref, for the 74 sensor cells of row number 12 of chip CA8-5. Axes x, y and z represent VGref, the column number and the voltage response respectively. Figure 5.5a) presents a perspective view of the response, whereas Figure 5.5b) shows a brird's-eye view of the same three dimensional diagram. The brighter cells correspond to the zone of higher sensitivity. From several VGref sweeps made on different sensors and different rows, row number 12 has been proven to be the one representing the best average row sensor response of the entire grid. For this measurement, R1 and R2 of Figure 5.3 were set to 10 MΩ . These three dimensional diagrams were generated using the data processing capabilities of Matlab[43] software. From the ASCII data file generated by the multifunction acquisition board, the data are transferred to a Unix platform and are entered into the Unix Matlab environment in a matrix format. According to Figure 5.5b), the response of the entire row is maximum with a good uniformity when VGref equal to 1.24V[1]. Beyond this voltage, the response of the sensor cell located on row number 45 starts decreasing, meaning that the double drain/double source MOSFET falls into the linear operating region and loses its sensitivity as explained in section 3.2.3. As VGref keeps increasing, the sensitivity of the sensor cells eventually decreases to null.

5.2.3 The response distribution for the entire sensor grid

Once the proper biasing voltage VGref has been determined, the response distribution of the entire sensor grid can be measured. In order to simplify the testing process, the same input/output interconnections of Figure 5.3 are employed, only the

1. During the test process, the data were analysed with a colour monitor on a SUN Sparc station using a coloured map scale. Hence, better mapping resolutions than the one of Figure 5.5 were obtained. The gray scale mapping is employed here solely to improve the quality of the figure printed with a black and white laser printer.

timing sequence is modified and the input VGref is kept constant at the maximum sensitivity voltage previously found, namely 1.24 V.

By submerging the chip in a constant magnetic field of 1800 Gauss, the timing sequence of Figure 5.6 allows for the reading of the sensor cell responses for the entire grid. Analogous to the timing sequence of Figure 5.4, sequence (1) resets the row shift register and sequence (2) resets the column shift register and activates the row number 1. Sequence (3) is divided into two parts, first, sequence (3a) is cycled 74 times, for the 74 columns of the sensor grid. After each cycle, four measurements of the response are taken and the average is stored in the data file. Once the entire row is scanned, sequence (3b) is cycled once to reset the column shift register and activate the following row. In order to read the 24 rows of the sensor grid, sequence (3) must be repeated 24 times. Here again, in order to eliminate the fixed pattern noise, two sets of data, one with the magnetic field and one without the magnetic field are taken and subtracted from each other.

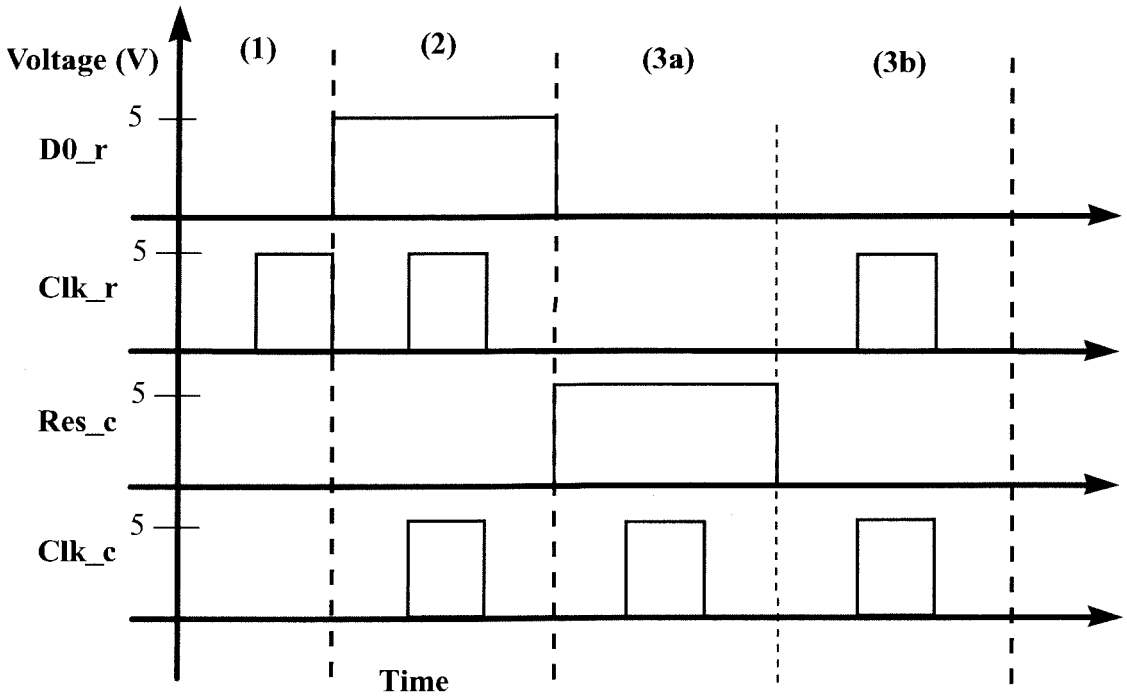


Figure 5.6 Timing sequence employed to measure the sensor grid response.

In order to evaluate the optimum resistor value of R1 and R2 that will reduce the sensor response discrepancy without significantly decreasing the sensitivity, the sensor grid responses for four values of R1 and R2 have been measured. For each value, the optimum biasing voltage VGref is determined using the method employed in section 5.2.2. Figure 5.7 presents histograms of the sensor grid response of the sample chip CA8-5 for R1 and R2 equal to a) ∞, b) 40 MΩ, c) 20 MΩ and d) 10 MΩ, submitted to a constant magnetic field of 1800 Gauss. Case a) corresponds to a measurement taken without output resistors. In this case, the output load value is then 1 GΩ, the input impedance of the analog input channel. This high value has a negligible effect on the total output impedance for the cases b), c) and d) since it is located in parallel with R1 and R2.

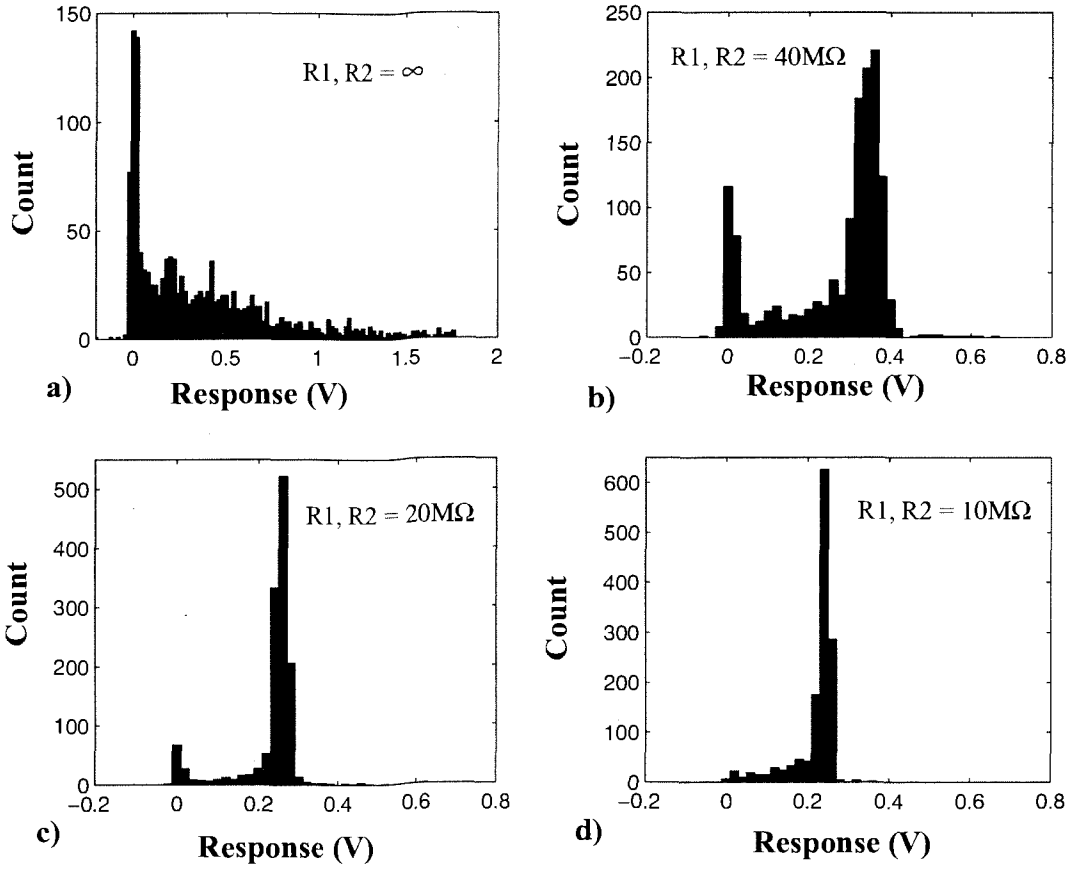


Figure 5.7 Sensor grid responses of chip CA8-5 for four values of output load at B = 1800 Gauss.

Table 5.1 summarizes the response distribution parameters of Figure 5.7. The cascode current mirror acting as an active load for the sensor cells provides a high differential gain to the sensor readout circuit. By adding an output load, the output resistance of the sensor readout circuit is reduced, hence decreasing the gain. As seen in column 2 of Table 5.1, as the output load decreases, the average response decreases. However, the standard deviation of the distributions is greatly reduced, meaning a better response uniformity. Column 4 confirms the response uniformity improvement by expressing the ratio of the standard deviation of the distribution over its average. Also, as depicted in Figure 5.7, low values of the output resistors greatly reduce the number of sensor cells having no sensitivity, and this number almost disappears for R1 and R2 equal to 10 MΩ . Given these results, output resistors of 10 MΩ will be used for every measurement performed on any chip for the remainder of the thesis.

R1, R2 (MΩ)	VGref (V)	Average Response ($\hat{r}$) (V)	Standard Deviation (σ_r) (V)	$\frac{\sigma_r}{\hat{r}}$ (%)
∞	0.92	0.364	0.400	110
40	1.06	0.263	0.134	50.8
20	1.10	0.231	0.077	33.4
10	1.22	0.222	0.055	24.7

Table 5.1 Experimental results of the response distribution of Figure 5.7.

To verify the effect of the load resistors R1 and R2 on the average response, the analytical expression linking the response to the current imbalance (equation (3.4) of chapter 3) is adapted for the present case. It simply requires adding in parallel to the output load, the value of the resistors R1 or R2 denoted R_{load}, and the value of the input impedance of the A/D board, R_{meas}. Equation (3.4) then becomes:

$$r = \delta_r(I_{D1} + I_{D2})(R_{cm}^{-1} + R_{msc}^{-1} + R_{load}^{-1} + R_{meas}^{-1})^{-1} \quad (5.1)$$

To obtain r, the evaluation of the right hand side of equation (5.1) is carried out. R_{load}, is taken from Table 5.1 and R_{meas}, given by the A/D board user manual, is 1 GΩ . I_{D1} and I_{D2} are assumed to be equal and are found from the simulation results of Figure 3.10 for the values of VGref listed in Table 5.1. δ_r is extrapolated from the experimental results of Table 3.1. In the case of arrays without conduction barriers, the average relative current imbalance is 0.75% for a magnetic field of 1700 G. Assuming a linear progression, δ_r is approximately 0.79% for a magnetic field of 1800 G, the value employed in the experiment giving the results of Table 5.1 and Figure 5.7.

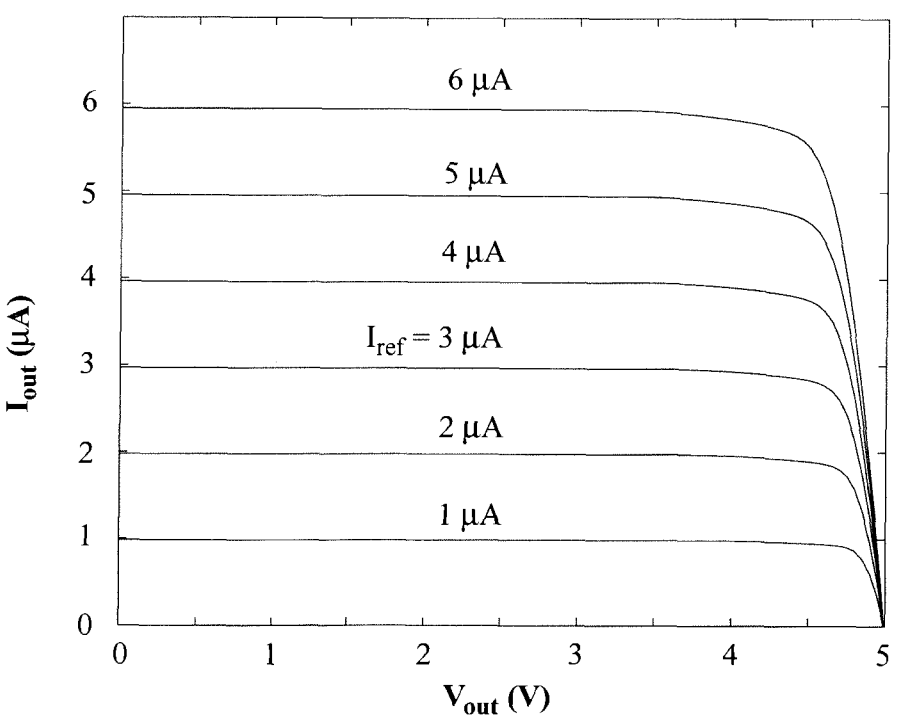


Figure 5.8 Experimental input-output characteristics of the cascode current mirror.

R_{cm} is evaluated from the measured input-output characteristics of a spare CM. The measurement was made with the SPA HP4145A from the bottom unused spare

reading bus of a chip, on which the left CM is permanently connected (see Figure A.5: the spare active load located on the bottom left of the layout). Figure 5.8 shows the experimental input-output characteristics of the CM. The values of R_{cm} are calculated from the slope of the curves, knowing the operating current and voltage of the LAMSA readout circuit.

Given the length of the sensor cell, 54 μm, the output resistance of one drain of the MSC operating in the saturation region, R_{msc}, could easily reach several giga ohms. Since no measured output characteristics are available for the MSC, the values of R_{msc} are approximate evaluations from SPICE simulations of the output characteristics of a N MOSFET. The N MOSFET is 54 μm in length and 27 μm in width, corresponding to one half MSC having one drain and one source. For such a large transistor, It should be noted that the effect of the poor matching of SPICE parameters is less critical in the evaluation of R_{msc}. Figure 5.9 shows the result of the simulation.

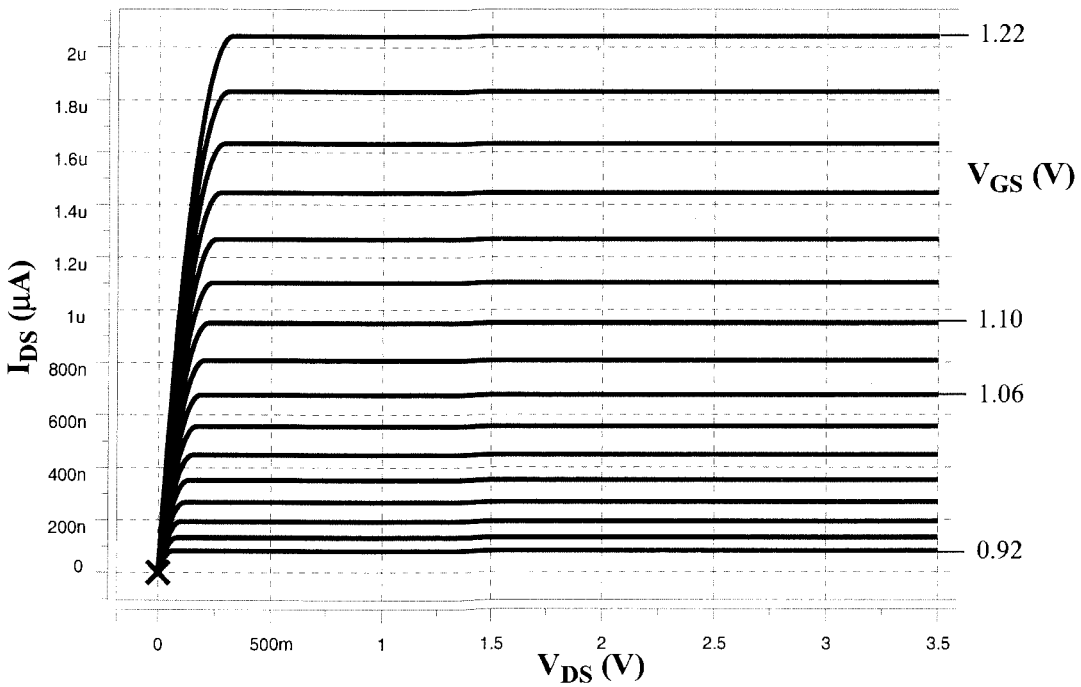


Figure 5.9 SPICE simulation of the output characteristics of half sensor cell.

Having the input-output characteristics of the current mirror and the magnetic sensor cell, R_{cm} and R_{msc} can now be obtained and the analytical expression of the response, equation (5.1), can be evaluated. For each value of the load resistors, the proper operating points (I_{D1},V_{Da}) and (I_{D1},V_{D1}) must be found to derive R_{cm} and R_{msc}. To extract these operating points, SPICE simulations of Figure 3.10 are rerun with R_{load}, and I_{D1}, V_{Da} and V_{D1} are extracted for the VGref voltages listed in Table 5.1.

Table 5.2 summarizes the results obtained from the analytical response calculation of equation (5.1). From the measured curves of Figure 5.8, only two values of R_{cm} were evaluated; namely for I_{ref} equals 2 μA and 1 μA, corresponding approximately to the situation were I_{D1}equals 1.95 μA and 0.92 μA respectively. For lower values of I_{D1}, R_{cm} increases and becomes negligible compared to R_{meas} of 1 GΩ . The values of R_{msc} derived from the SPICE simulations give, as expected, very high resistivity and are also negligible compared to R_{meas}. Except for the case where no R_{load} was employed, i.e. R_{load} equals infinity, the values of R_{load} set the equivalent value of the parallel resistors in the equation (5.1). The 5% tolerance of R_{load} employed in the experiment, is taken into account when calculating the response. Translated in the equation (5.1), it implies a variation of ±10% considering the extreme case where one branch resistor is at the nominal value plus 5% and the other at the nominal value minus 5% and vice-versa.

R_{load} (MΩ)	VGref (V)	I_{D1} (μA)	V_{Da} (V)	R_{cm} (GΩ)	R_{msc} (GΩ)	Response (r) (V)
∞	0.92	0.08	3.15	-	435	1.22
40 ±5%	1.06	0.66	2.86	-	274	0.401 ±.038
20 ±5 %	1.10	0.92	2.78	16.7	272	0.285 ±.028
10 ±5%	1.22	1.95	2.53	1.96	184	0.304 ±.028

Table 5.2 Results of the analytical response calculation of equation (5.1)

Looking at the experimental results of Figure 5.7, the peaks of the response distributions follow the same trend as the calculated responses of Table 5.2, except for R_{load} equals infinity. For instance, in the case where R_{load} equals 10 MΩ and 20 MΩ, both peaks are located at similar voltage values, and increases of 0.1 V for R_{load} set to 40 MΩ, as predicted in Table 5.2. However, for R_{load} equals infinity, the peak is located at zero.

Physical variations of device structures due to process limitation are responsible for the spread distribution of the sensor cell responses for each value of R_{load}. A careful investigation of some of the electrical tests used during the process characterization could help in explaining the global sensor grid response behaviour.

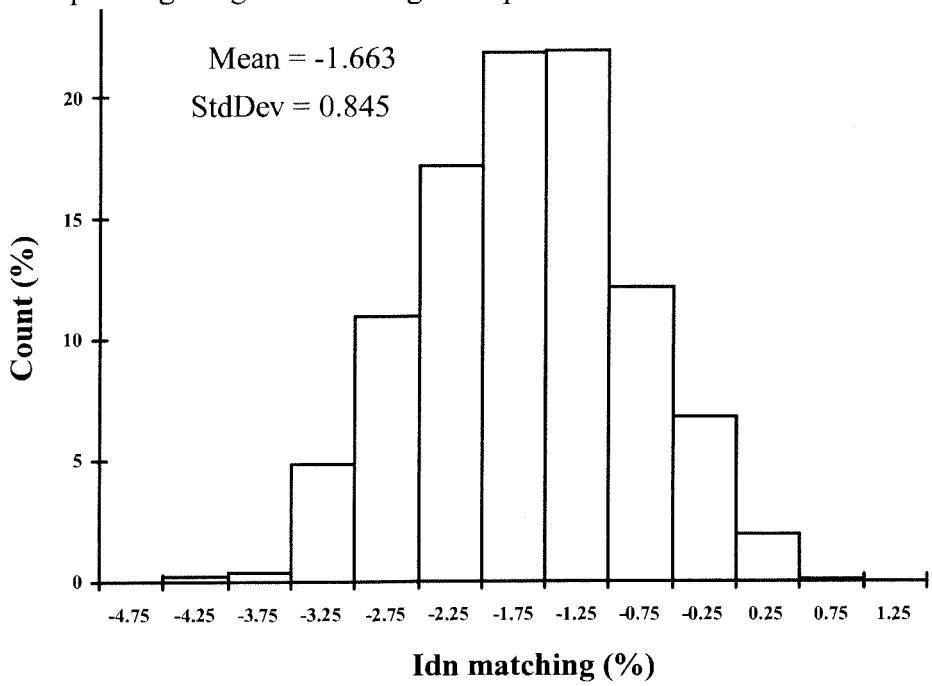


Figure 5.10 Relative drive difference between 10 μm vertically spaced N-channel transistors with horizontal gate. (Courtesy of Mitel Corporation)

The histogram shown in Figure 5.10 reveals an important electrical process characteristic responsible for the sensor grid response distribution. Analogous to the definition of the magnetic field created current imbalance presented in chapter 2, equation

(2.2), the Idn matching represents the intrinsic current imbalance of a pair of horizontal NMOS transistors each having a W/L ratio of 30 μm/1.5 μm and vertically spaced 10 μm apart. This structure is somewhat similar to our double drain/double source sensors of 54μm by 54 μm with a 9 μm wide notch between drains and sources of a same pair. Several of these test structures are spread across a wafer. Figure 5.10 shows the distribution of the measurements obtained from three lots. Idn of the N MOSFETs are measured in the saturation region with V_{GS} equal to V_{DS} at 5 V, the same operating region as the magnetic sensor cells. Another important cause of the intrinsic current imbalance can be found from the variation of the N MOSFET threshold voltage, which is given by measuring the Vtn matching parameter.

In some situations where the gain of the readout circuitry is high, in the case of R_{load} equals infinity, the value of the intrinsic current imbalance of most of the sensor cells is high enough to saturate the output of the readout circuit and thus annihilate the response of those sensor cells. As the value of R_{load} decreases, the gain decreases and the number of zero response cells vanishes as seen in Figure 5.7.

5.3 Sensor Grid Response Calibration

The previous section dealt with ways to electronically improve the sensor grid sensitivity and the response uniformity. This section will now deal with software tools employed to equalize the grid response and to present it in a useful manner. In order to exploit the sensor grid imaging function effectively, the response of each sensor cell must be calibrated; meaning that each output voltage reading must correspond to a known magnetic field strength. Software calibration also improves the grid response uniformity.

5.3.1 Calibration algorithm

A general regression analysis method is employed for modelling the sensor cell responses. For each sensor cell, eleven measurements, $\{x_1, x_2,....x_{11}\}$, are taken within a range of magnetic fields varying from 0 to 1800 Gauss, $\{y_1, y_2,....y_{11}\}$. For each point, a regression equation of order "n" is defined, where the coefficients $\{b_0, b_1,... b_n\}$ are determined by solving an equation system formed by the eleven points of the response. Expressed in matrix form, the solution of the equation system is given by[44]:

$$B = (X'X)^{-1}X'Y \tag{5.2}$$

where B is the matrix of coefficients, Y, the matrix of the independent variable, and X, the matrix of the measured values. The solution calculated from equation (5.2) corresponds to a least square fit of the cell response.

Fit Order (n)	Average Response ($\hat{y}$) (Gauss)	Standard Deviation (σ_y) (Gauss)	$\frac{\sigma_y}{\hat{y}}$ (%)
1	1129.6	215.6	19.1
2	1065.7	206.1	19.3
3	1067.6	122.2	11.4
4	1068.2	127.2	11.9
5	1066.6	123.7	11.6

Table 5.3 Results of the calibrated grid response for five different fit orders.

Table 5.3 lists the calibration results of the sensor grid response for the general regression method employed with a polynomial function of order one to five. The raw response data were measured for a constant magnetic field of 1260 Gauss. The sensor grid response uniformity reaches a maximum at n equals three, where the standard deviation is minimum and where the ratio of the response standard deviation over its average is the

least. Hence, a polynomial fit of the third order has been selected to calibrate the response of each sensor cell.

In order to evaluate the goodness of the third order polynomial fit of the sensor responses, for each sensor cell, equation (5.2) is now evaluated with X being the independent variable, the magnetic field, and Y being the voltage response. The fact of having the same independent variable coordinates for all sensor cells facilitates the fit analysis. Figure 5.11 presents the raw and fitted responses of six sensor cells selected randomly within the grid. A simple visual inspection of these curves reveals a fairly good

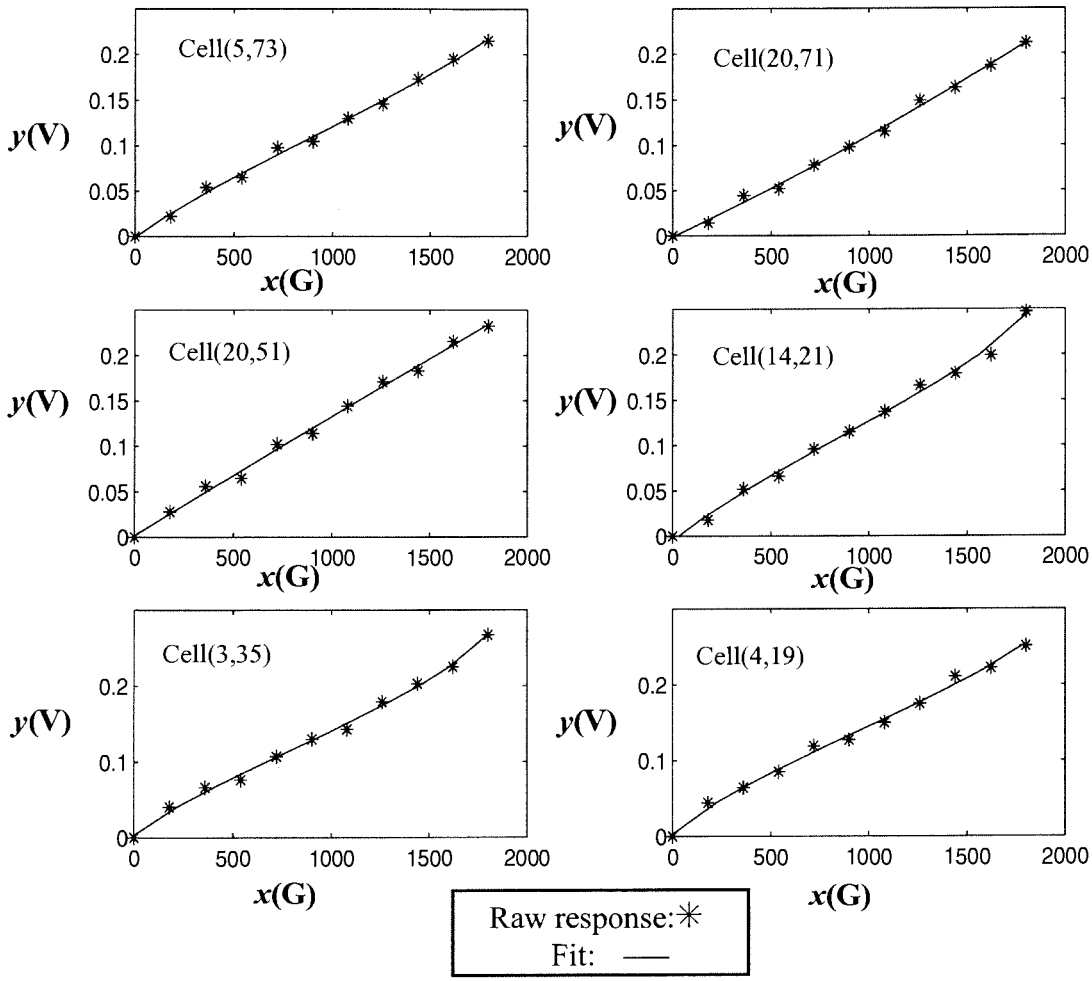


Figure 5.11 Raw and fitted responses of six sensor cells.

agreement of the fit to the raw data. However, a quantitative evaluation of the goodness of the fit of the polynomial model would be more suitable.

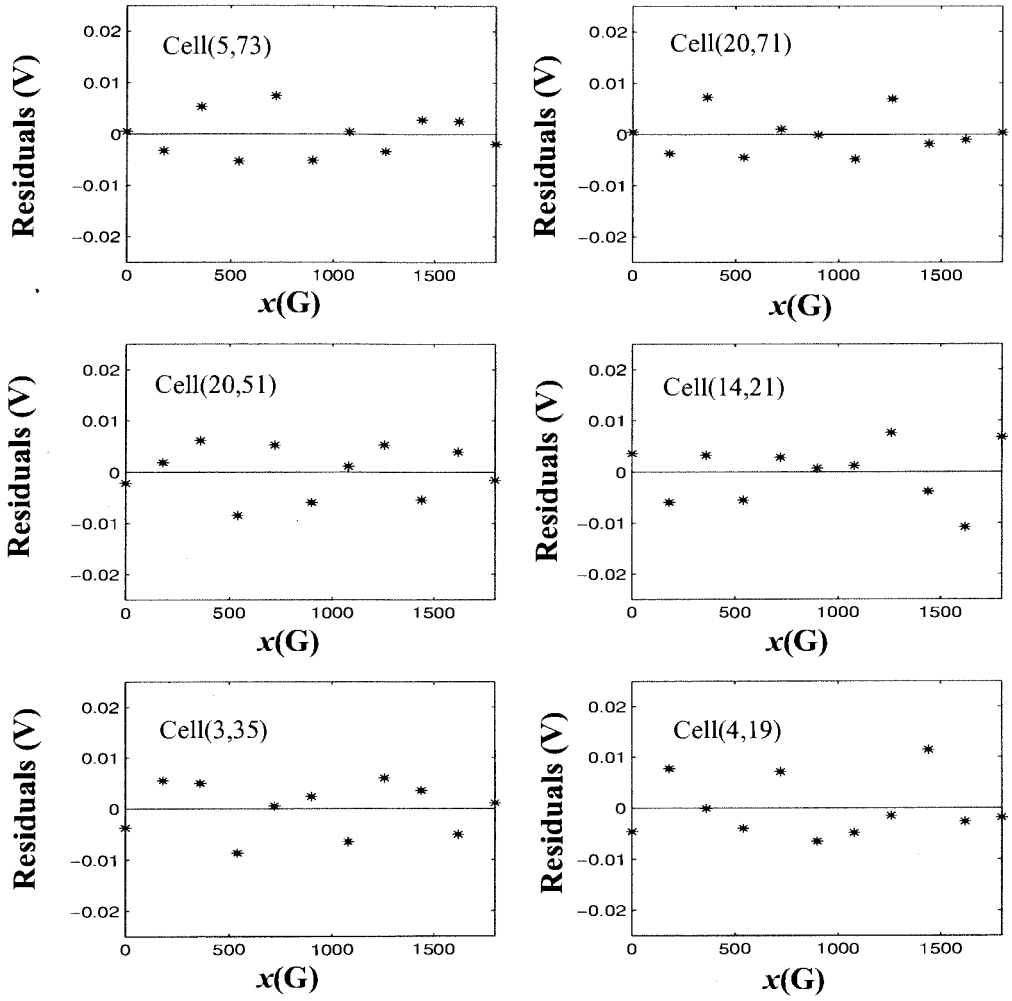


Figure 5.12 Residual plots of the fitted responses of Figure 5.11.

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Figure 5.13 Residual sequence of the case of sensor cell (14,21)

To determine the validity of the fit, the analysis of the residuals of the fitted function has been chosen[44]. Figure 5.12 shows plots of the residuals as a function of the independent variable for the six sensor cells of Figure 5.11. As can be seen, for each sensor cell, the residuals are distributed on each side of the x axis, forming a horizontal

band, which is a good sign of the aptness of the fit. To obtain a quantitative assessment on the validity of the fit, the method of examining the runs, or changes of sign, in a time sequence plot of the residuals is employed. From the plots of Figure 5.12, where values are ordered in a time measurement sequence like the ones of Figure 5.11, the method consists of evaluating the probability of occurrence of a grouping of negative and positive values of residuals for a given plot. For instance, Figure 5.13 depicts the sequence of the eleven residuals of the cell (14,21). The sequence contains seven distinct groupings or runs. Given the number of positive "+" and negative "-" residuals, seven and four respectively, it is possible to calculate the probability of having seven runs. Looking at Drappert and Smith[44], chapter 3, table 3.1, it is found that the probability of achieving such arrangement of residuals is 0.227 and that there exists only one run sequence more probable than this, and six less probable. This result shows that the residual sequence is a very common case, in that only a pure random noise signal slightly displaces the raw data away from the fitted curve. It also indicates that there are no statistically significant unresolved parameters in the sensor cells' behaviour. Hence, the third order polynomial model is appropriate for fitting the response of this sensor cell.

Table 5.4 lists the values of the sequence probability for the residual plots of Figure 5.12, along with the number of sequences having higher and lower probability for the same number of positive and negative residuals. The results demonstrate that the residual sequences of all six sensor cells do not correspond to an extreme low probability case that would jeopardize the random character of the residuals. The worst case encountered in this example is the residual sequence of cell (5,73) where there exist six and three sequences having higher and lower probabilities respectively. From the 1356 sensor cells of the grid it is most likely that some will have a lower probability sequence than the one of cell

(5,73). However, from the calibrated distribution parameters of Table 5.3 and the residual sequences of Table 5.4, it can be asserted that the polynomial model of the third order selected to calibrate the raw data is suitable for the majority of the sensor cells comprising the grid and has been used for all the sensor cells of the grid.

Sensor Cell	Residual Sequence Probability	Number of sequences	
		More Probable	Less Probable
(5,73)	0.022	6	3
(20,71)	0.065	5	4
(20,51)	0.065	5	4
(14,21)	0.227	1	6
(3,35)	0.121	4	3
(4,19)	0.212	2	3

Table 5.4 Probability comparison of the residual sequences.

5.3.2 Comparison parameter

To evaluate the effect of the restructuring on the sensor cell responses, it is useful to define a comparison parameter which will quantify the effect of the restructuring schemes on the performance of the LAMSA. Using the analytical polynomial equation of the fitted response, as described in the previous section, the finite integral of the response over the entire range of magnetic field measurements can be easily evaluated. In fact, this procedure gives exactly the area under the response curve. This calculated value, I_{ij}, is employed to compare the sensor cell responses before and after restructuring, through a response comparison parameter defined as:

$$\Delta_{ij} = 100\left(\frac{Ir_{ij} - I_{ij}}{I_{ij}}\right) \tag{5.3}$$

where Ir_{ij} is the cell response finite integral after restructuring and Δ_{ij} is the response comparison parameter. For each cell, Δ_{ij} gives a percentage value of the difference between the two responses over the entire range of magnetic field variation. For instance, a value smaller than zero represents an overall loss of sensitivity and a value greater than zero represents a gain in sensitivity over the measured range. Presenting these parameters in the form of a histogram gives an overall assessment of the effect of the restructuring for the sensor cells affected. These comparison parameter histograms will be used in chapter 6 to evaluate the effect of the restructuring.

5.4 Repeatability Test

In order to verify the reliability of the sensor system and the test equipment, three sets of identical response measurements have been performed on the chip, CA8-4. This chip comprises a sensor grid of 25 rows and 35 columns. Row number 25 was employed for the purpose of the comparison. Figure 5.14 presents histograms of the comparison parameters for the three possible comparison pairs: a) sets (1) versus (2), b) sets (1) versus (3) and c) sets (2) versus (3). These results show a level of repeatability for the entire line lying roughly between -20% and 20%. However, the bulk of the parameters are located within -10% and 10%. The cause of the variation of the response, from test to test, is identified as noise fluctuations. Sensor cells having weak responses to a magnetic field stimulus are more affected by randomly distributed noise fluctuations and present unstable behaviour as shown by the variation of the distribution tails from these three comparison graphs.

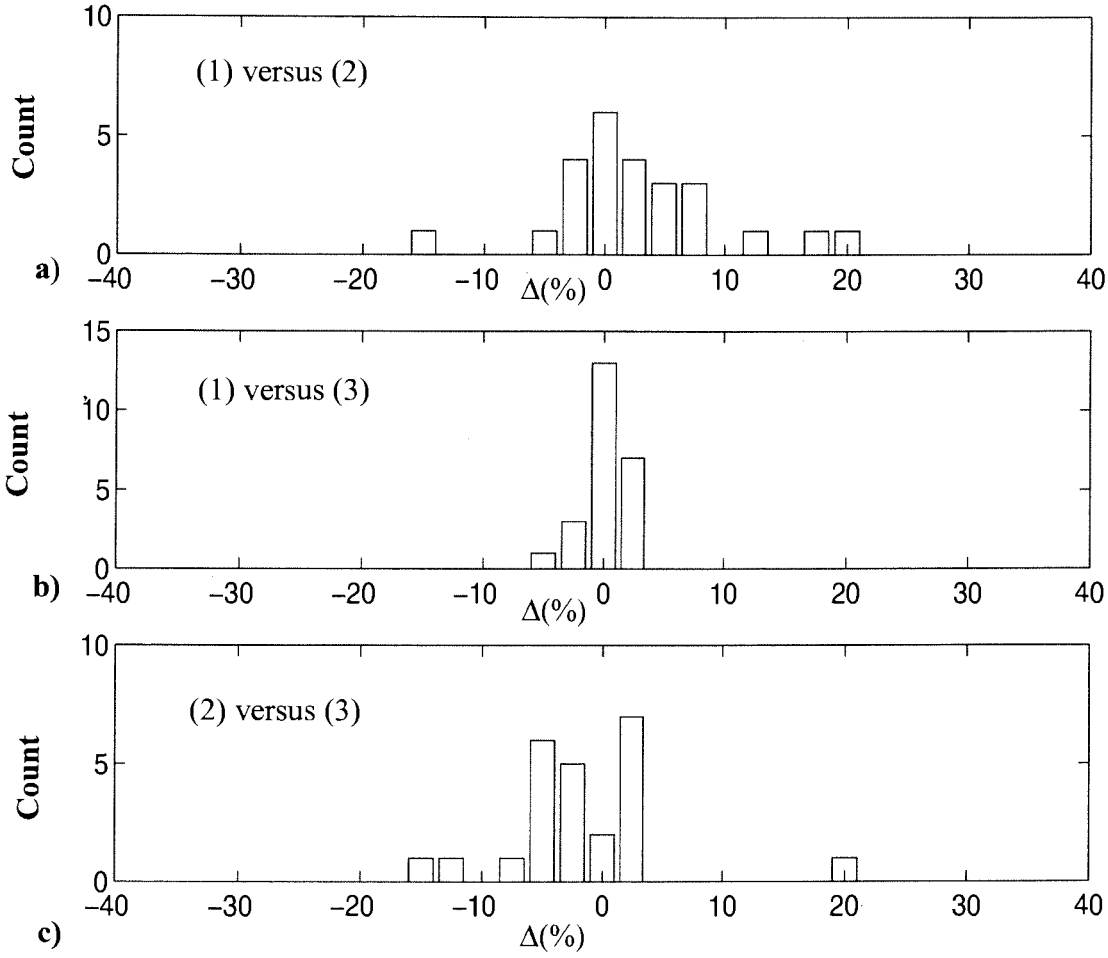


Figure 5.14 Histograms of the repeatability test.

5.5 Summary

Important information concerning the equipment and the software algorithm employed for testing the functionality of the LAMSA have been presented in this chapter. First, the test board and the multifunction digital/analog acquisition board used to generate the test patterns have been reviewed. A measurement sequence consisting of verifying the basic functionality with an oscilloscope and finding the biasing voltage for optimum sensitivity has been described.

Changes in the parameters of the Mitel 1.5 μm CMOS process increased the gain of the LAMSA readout circuit compared to similar designs previously fabricated with the same process. This gain increase negatively affected the response uniformity and a short experiment involving external load resistors was performed only to restore a uniformity level suitable to evaluate the effect of the restructuring on the sensor cell responses. It was found that adding resistor loads of 10 MΩ at the reading output had the effect of improving the sensor grid response uniformity and eliminating most of the zero response cells, while keeping the sensor average sensitivity at 123 μV/G.

A simple analytical expression was used to explain the trend observed on the experimental response distributions as a function of the output resistive load. The intrinsic current imbalance due to the mismatch of drain currents (Idn matching) and threshold voltages (Vtn matching) across the array is suspected to be responsible for the spread of the response distributions and for annihilating the response of some of the cells by saturating the output voltage of the readout circuit.

A third order polynomial fit has been found to be a good choice for calibrating the sensor cell responses. A statistical treatment based on the analysis of the residuals has been performed to evaluate the validity of the polynomial model. Finally a comparison parameter was defined in order to compare the sensor cell response before and after the occurrence of on-chip restructuring. This parameter has been used to verify the measurement repeatability and will be a key element in analysing the restructuring effect on the sensor grid response that will be presented in chapter 6.

Chapter 6

Effects of Restructuring

Having described in chapter 5 the software and hardware tools employed to measure, calibrate and compare the sensor grid response, chapter 6 will focus on the effects of various types of restructuring on the sensor grid response. The influence of the restructuring on the maximum frequency of operation of the sensor array is also presented. First, effects of restructuring at the sensor grid level involving spare gate lines and spare drain lines, as illustrated in Figure 4.2, is analyzed. Second, the impacts of the restructuring of the surrounding control circuits, namely the row and the column scanning circuits and the active load, following the schemes presented in section 4.5, are investigated. For each restructuring type, the laser link and cut sequence involved is described. Finally, a table presents the yield gain obtained due to the redundancy schemes on a sample of 23 tested chips.

6.1 Maximum Frequency of Operation

In order to verify the impact of the restructuring schemes on the maximum

frequency of operation, before and after performing a laser cut and link restructuring sequence, the maximum frequency of operation is measured with an oscilloscope by setting the device in continuous reading mode as explained in section 5.2.1. Having the device voltage VGref set to the value previously determined to obtain the maximum response, as seen in chapter 5, and looking at a waveform display similar to the one presented in Figure 5.2, the maximum operating frequency is determined by gradually increasing the sensor system clock frequency and verifying two conditions:

1) The first cell to be read on each row must reach a constant output voltage plateau.

2) The reading bus discharging ramp, t_d, produced when the scanning sequence shifts from the reading of a blank cell (located between sensor cell subarrays) to an active cell, does not exceed one quarter of the sensor cell plateau period t_p, as shown in Figure 6.1.

The period t_d is measured from 90% to 10% of its voltage swing. The condition 1) only verifies that the row signal charging time is fast enough to apply the proper biasing voltage on the gate of each sensor cell before the column reading sequence is started. Condition 1) must be satisfied first before verifying condition 2).

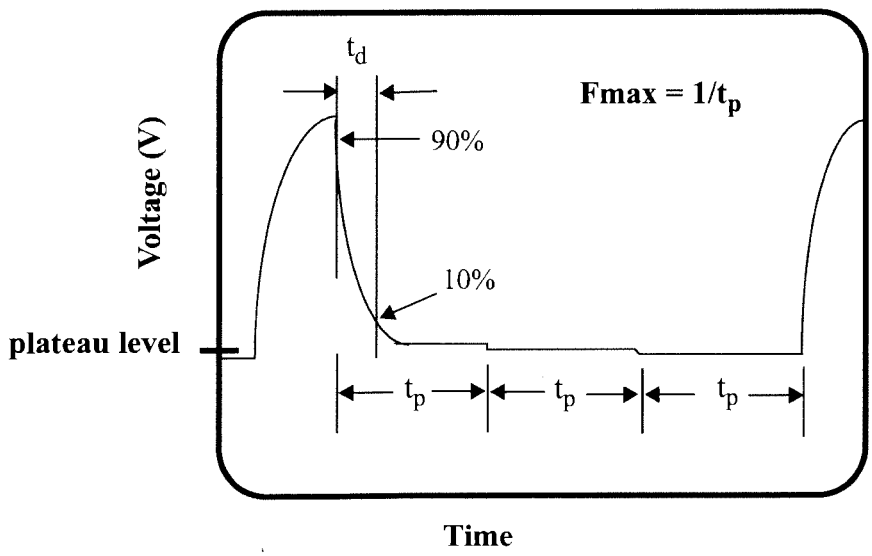


Figure 6.1 Determination of the maximum frequency of operation.

6.2 Sensor Grid Restructuring

6.2.1 Single row

The row restructuring test consists of initially isolating each sensor subarray on a row from the gate line by laser cutting, then reconnecting them to the spare gate lines through laser links. Figure 6.2 sketches the cutting and linking sequence used to restructure row number two of the sample chip CA8-7. The sensor grid response was measured before and after restructuring. Figure 6.3 presents the histograms of the comparison parameter of equation (5.3) on a) the restructured row number two and b) row number fourteen, a non-restructured row. Except for a few outliers, both distributions are closely similar where the bulk of the comparison parameters lies between - 20% and 20% and is centered close to zero. Similar distributions were obtained in the case of the repeatability test of Figure 5.14, proving the quasi null influence of the row restructuring scheme on the sensor cell responses of the restructured row and on the ones of the non-restructured rows as well. Identical maximum operating frequencies of 7575.8 Hz were measured before and after restructuring, according to conditions 1) and 2) described in the previous section.

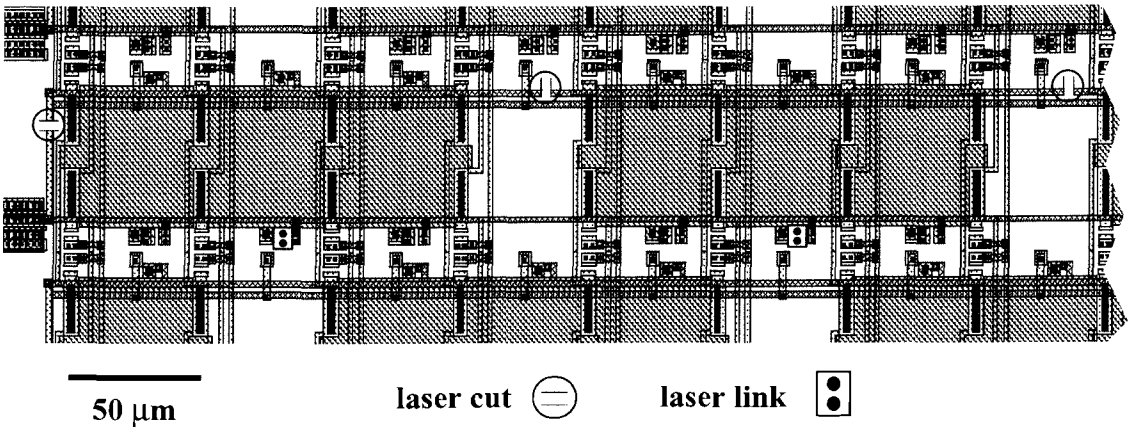


Figure 6.2 Gate line restructuring sequence.

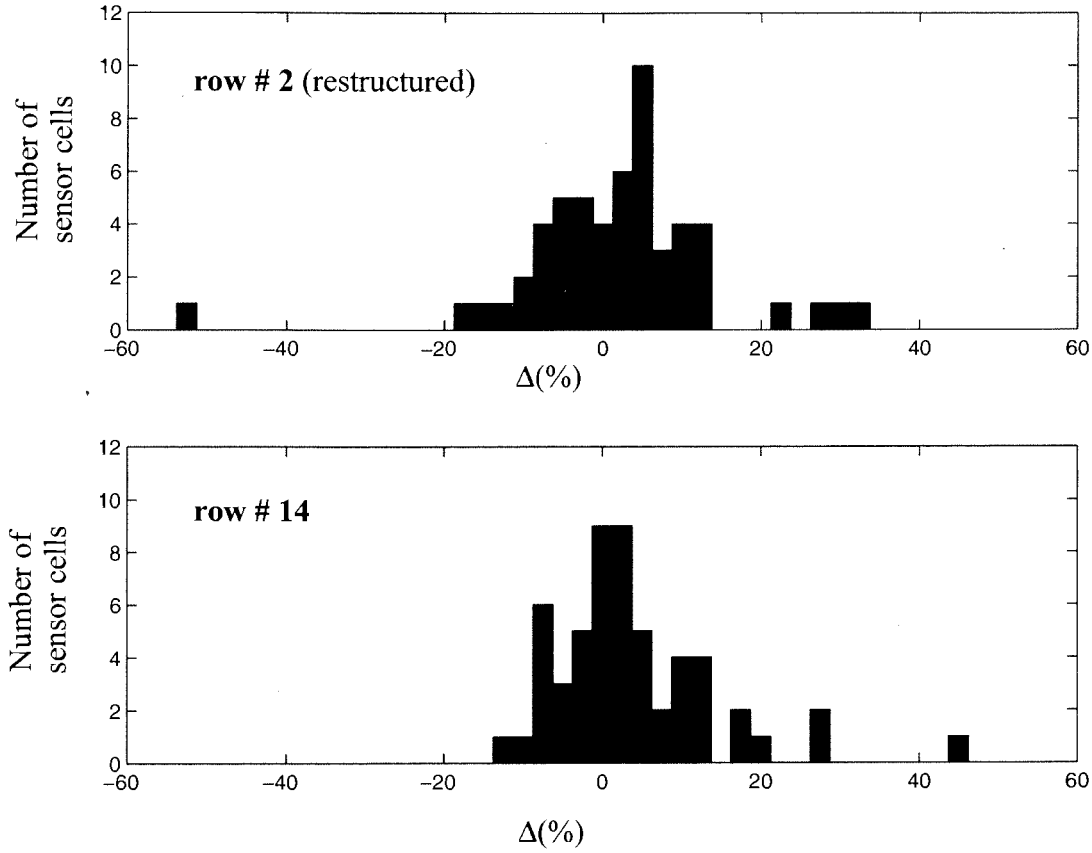


Figure 6.3 Histograms of the comparison parameter for a) one restructured row and b) one non-restructured row.

6.2.2 Single column

To verify the effect of the drain line restructuring scheme on the sensor cell responses, the entire column number five of the chip CA8-7 was restructured. Four possible spare line connection combinations were experimented with. Figure 6.4 illustrates the four laser cutting and linking sequences employed to obtain the four restructuring combinations. Since column number five comprises 24 cells, six cells for each combination have been restructured. Although combinations a) and b) are similar from a restructuring point of view, their effect on the responses might be different since the added resistors, due to the laser links, occur on a different current branch coming from

the current mirror. Hence, adding a resistor in series with the I_{ref} or the I_{out} output of the current mirror (Figure 3.7) may not have exactly the same impact. In the case of combinations c) and d), even though the resistance value added on each branch is the same, the effect of adding it on the sensor source or drain side on the I_{ref} or I_{out} branch might not be the same. These combinations represent the worse case restructuring scenario where one spare line is required for the left and the right pair of drains.

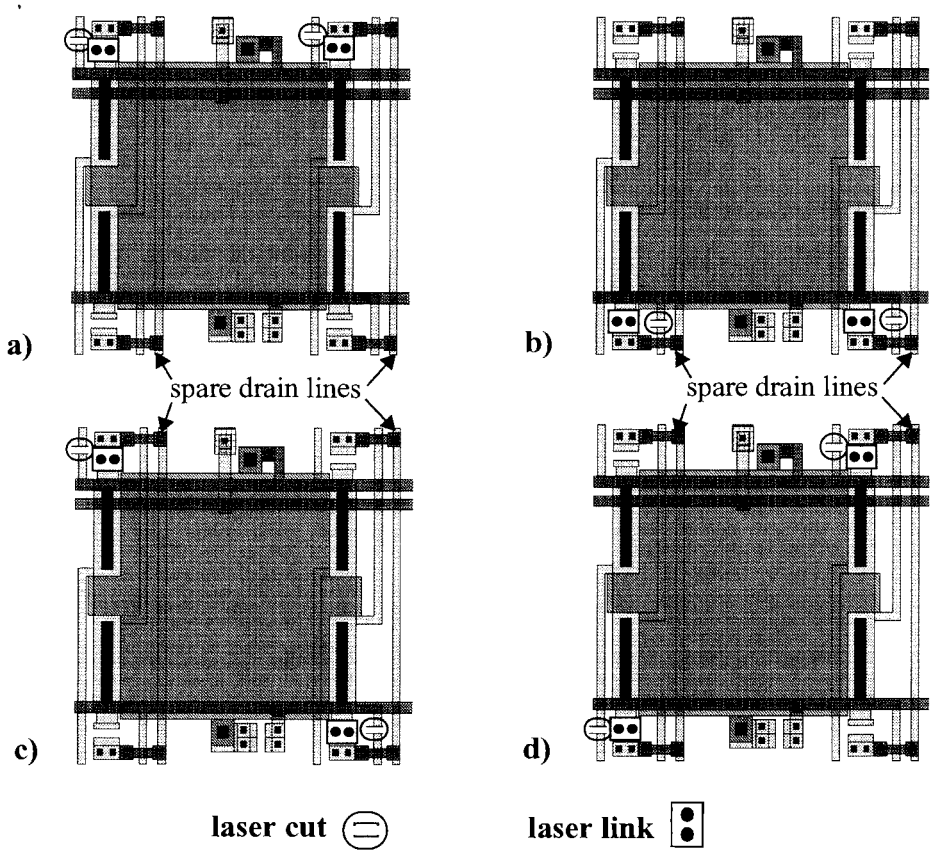


Figure 6.4 Four possible drain line restructuring combinations.

Figure 6.5 presents the distributions of the comparison parameters in the case of a) the restructured column number five including the four combinations of Figure 6.4, and b) the non-restructured column number eleven. Again, two similar distribution patterns of the same kind as the one measured in the repeatability test are obtained, proving the weak

influence of the drain line redundancy scheme on the sensor cell responses.

After verifying the maximum operating frequency on row number five according to the technique described in Figure 6.1, no difference was observed between the restructured column and the non-restructured one.

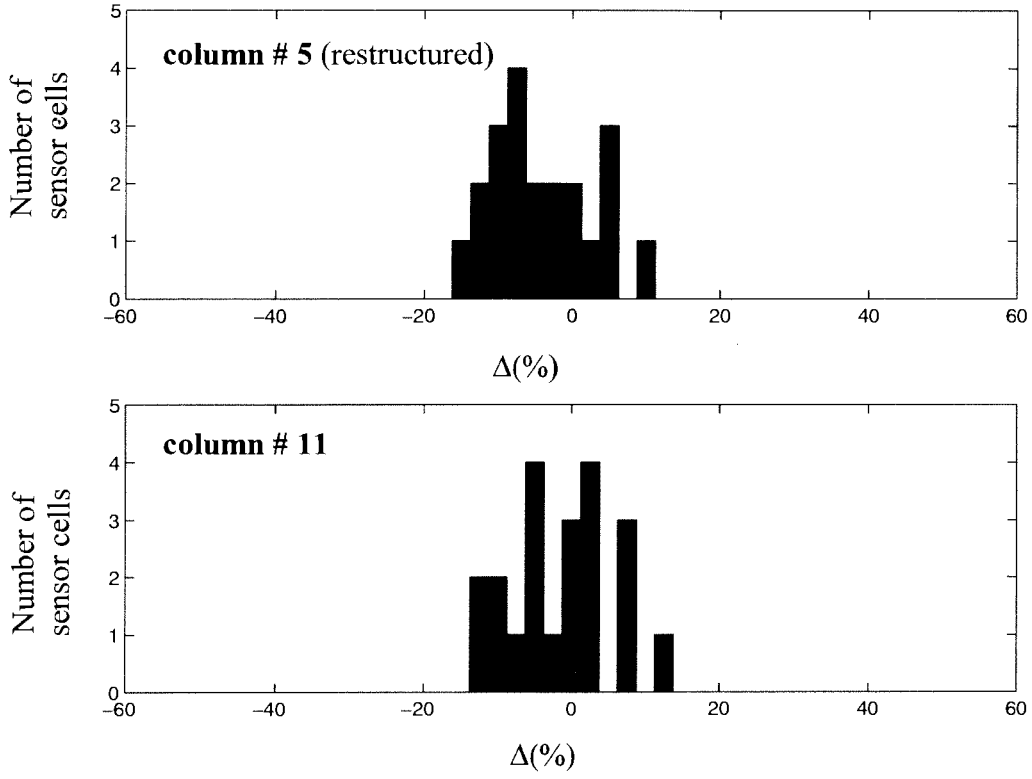


Figure 6.5 Histograms of the comparison parameter for a) one restructured column and b) one non-restructured column.

6.3 Scanning and Active Load Circuit Restructuring

6.3.1 Row scanning circuit

Restructuring a row scanning segment consists of isolating the defective segment by laser cutting and rerouting the scanning flow to the spare segment, which has been isolated from the spare row scanning circuit by laser cutting. Figure 6.6 displays the details of the restructuring of a row scanning segment. Before proceeding with the

restructuring sequence of laser cuts and links, the spare segment to be used is initially tested for shorts between Vdd and Vss by activating the testable laser link (Figure 6.6) and monitoring Idd. The testable laser link, described in section 2.4.2, simply powers the spare segment by connecting it to the ground rail. In the case where a normal Idd is measured, the connection is made permanent by zapping the laser link.

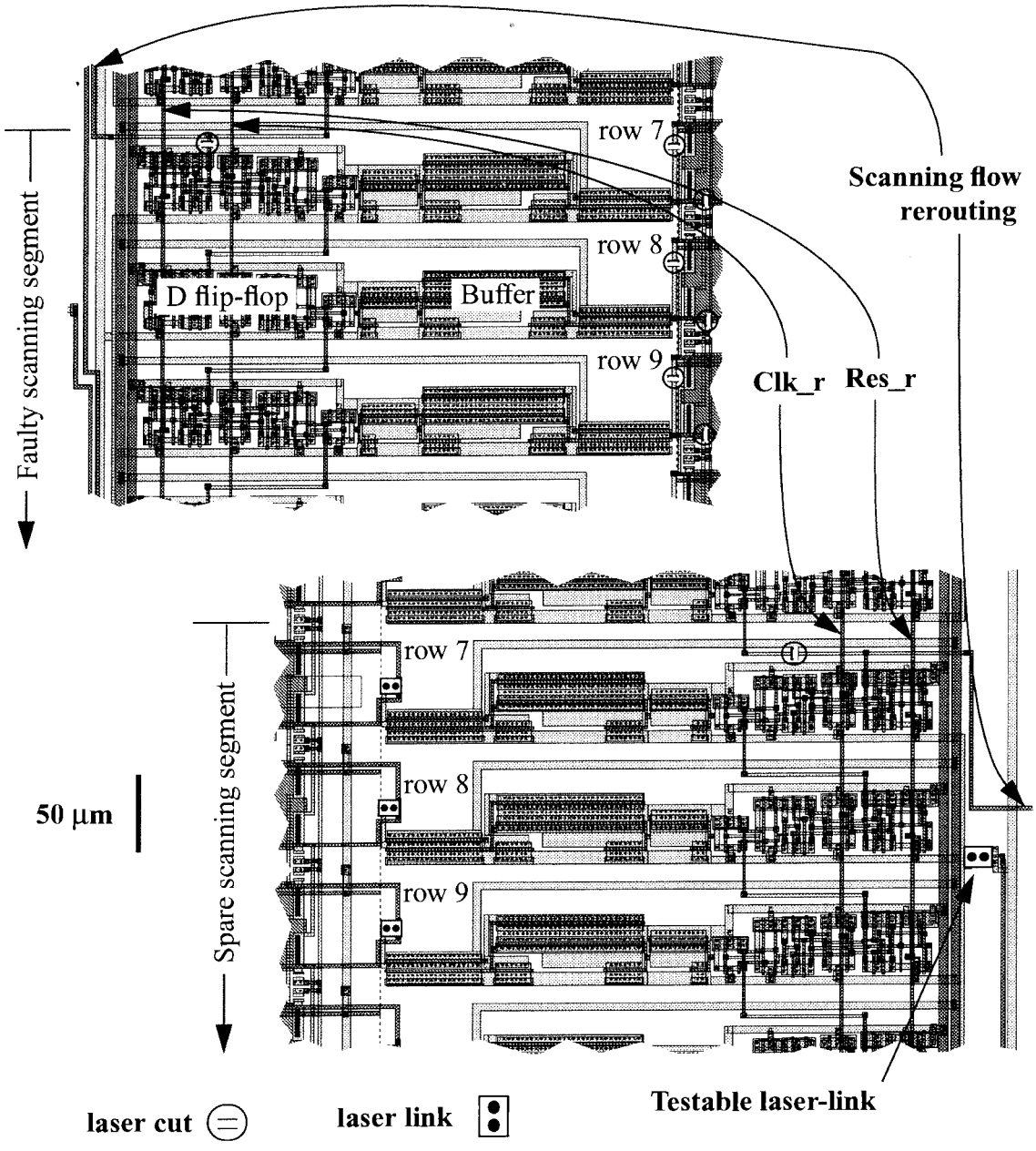


Figure 6.6 Restructuring scheme of a row scanning segment.

For this prototype, output/input rerouting connections have been designed between segments comprising six modules, one module being a D flip-flop and its corresponding buffer. The rerouting of the scanning flow is made through off-chip wiring. In a three metal layer CMOS technology, the metal 3 layer could be employed to fulfill this function. The row clock (Clk_r) and reset (Res_r) lines of the faulty and the spare segments are also externally connected together. Finally, sensor gate lines are disconnected from the drivers of the defective segment by laser cuts and joined to the spare segment drivers through laser links.

Figure 6.7a) presents the comparison results of a restructured segment including rows 7 to 12 of chip CA8-21. The distribution is centered at 5.4% with a standard deviation of 12.2%. The comparison parameter distribution of six adjacent rows, 13 to 18, displayed in Figure 6.7b), which have not been restructured, give about the same distribution shape with an average of 4.4% and a standard distribution of 13.3%. These two histograms suggest that the effect of the row restructuring on the response is weak since the non-restructured rows, 13 to 18, present a similar comparison parameter distribution than the restructured ones, rows 7 to 12. The nearly similar averages located around 5% might be the result of slight variations of the test equipment gains and sensitivities that happened during the time lapse between the measurements before and after restructuring.

The row scanning circuit of chip CA8-13 was restructured and the grid response was measured following the same method as the one used previously for the chip CA8-21. Figure 6.7c) and d) presents the comparison parameter results for the four restructured rows, 7 to 10, and four non-restructured rows, 13 to 16, respectively. The distributions of

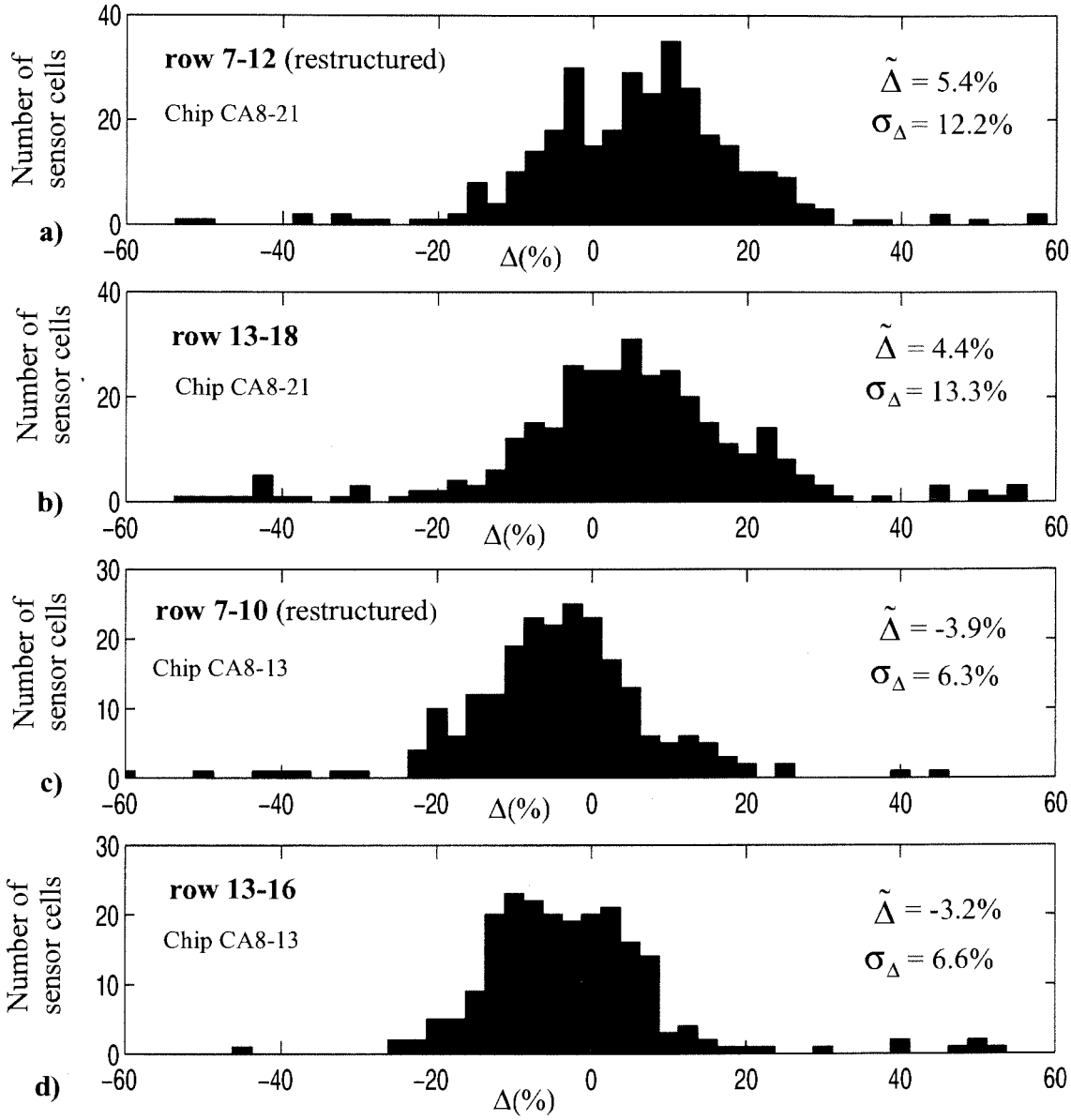


Figure 6.7 Histograms of the comparison parameter for the row scanning circuit restructuring sequence.

of Figure 6.7a) and b) have similar averages[1] and standard deviations. The fact that the distribution averages obtained on the chip CA8-13 differs from the ones obtained on the chip CA8-21, suggests that the measurement variation is due to the test equipment and

1. Contrary to the previous results obtained on one single row or column, the distributions of Figure 6.7 come from the responses of more than sixty sensor cells. Thus, the values of their averages are more reliable and are used for the results analysis.

occurs from test to test while remaining constant throughout a same test sequence. No difference in the maximum frequency of operation was observed for this restructuring scheme.

6.3.2 Column scanning circuit

A similar restructuring approach as the one used for the row scanning segment was employed for the column scanning segment restructuring as illustrated in Figure 6.8. In addition to the column clock (Clk_c) and reset (Res_c) lines, the reading lines Da and Db are also externally connected in this case. For each column, two drain lines must be laser cut from the faulty scanning module, and the same two lines are laser linked on the twin module on the opposite side of the grid. A column scanning module includes a D flip-flop and the corresponding pair of SPDT switches.

The histogram of Figure 6.9a) depicts the restructuring results of columns 57 to 64 of chip CA8-21. The same type of distribution as the row restructuring is observed with the majority of the comparison parameters lying between -20% and 20%. However, in this case, a small isolated group located around -40% presents a loss of sensitivity. The number of cells included in this group is twelve, corresponding to the number of non-zero response cells comprising even column line numbers. This result demonstrates that the restructuring has strongly lowered the sensitivity of one column, most likely due to a link resistance higher than the average added to the signal path. Poor conductive contacts or vias or other defects occurring on the restructured path could also be responsible. Figure 6.9b) presents the distribution of seven adjacent columns not restructured. The same distribution span is observed and both distribution averages and standard deviations are near values, suggesting again that a similar small constant variation affects the measured

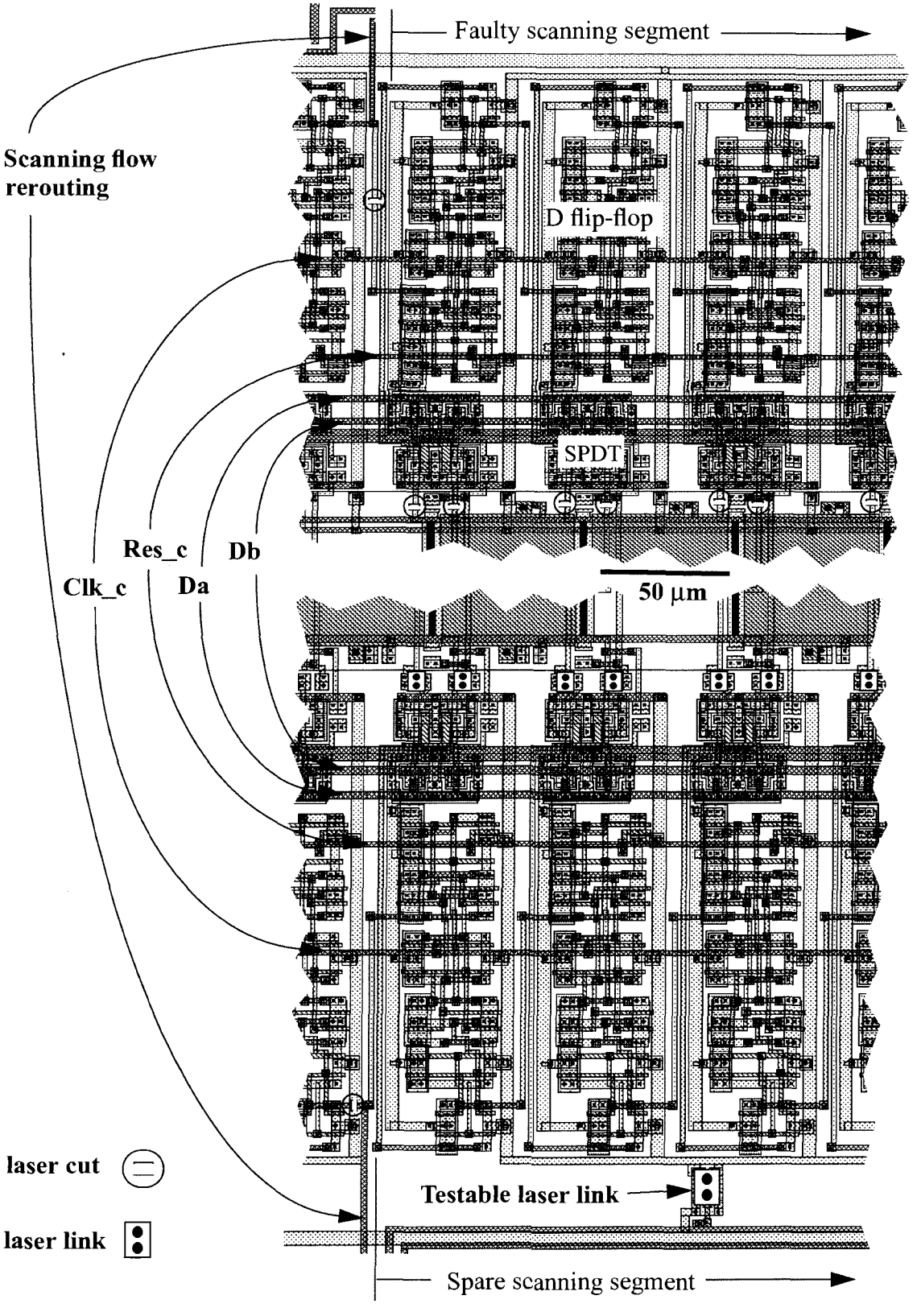


Figure 6.8 Restructuring scheme of a column scanning segment.

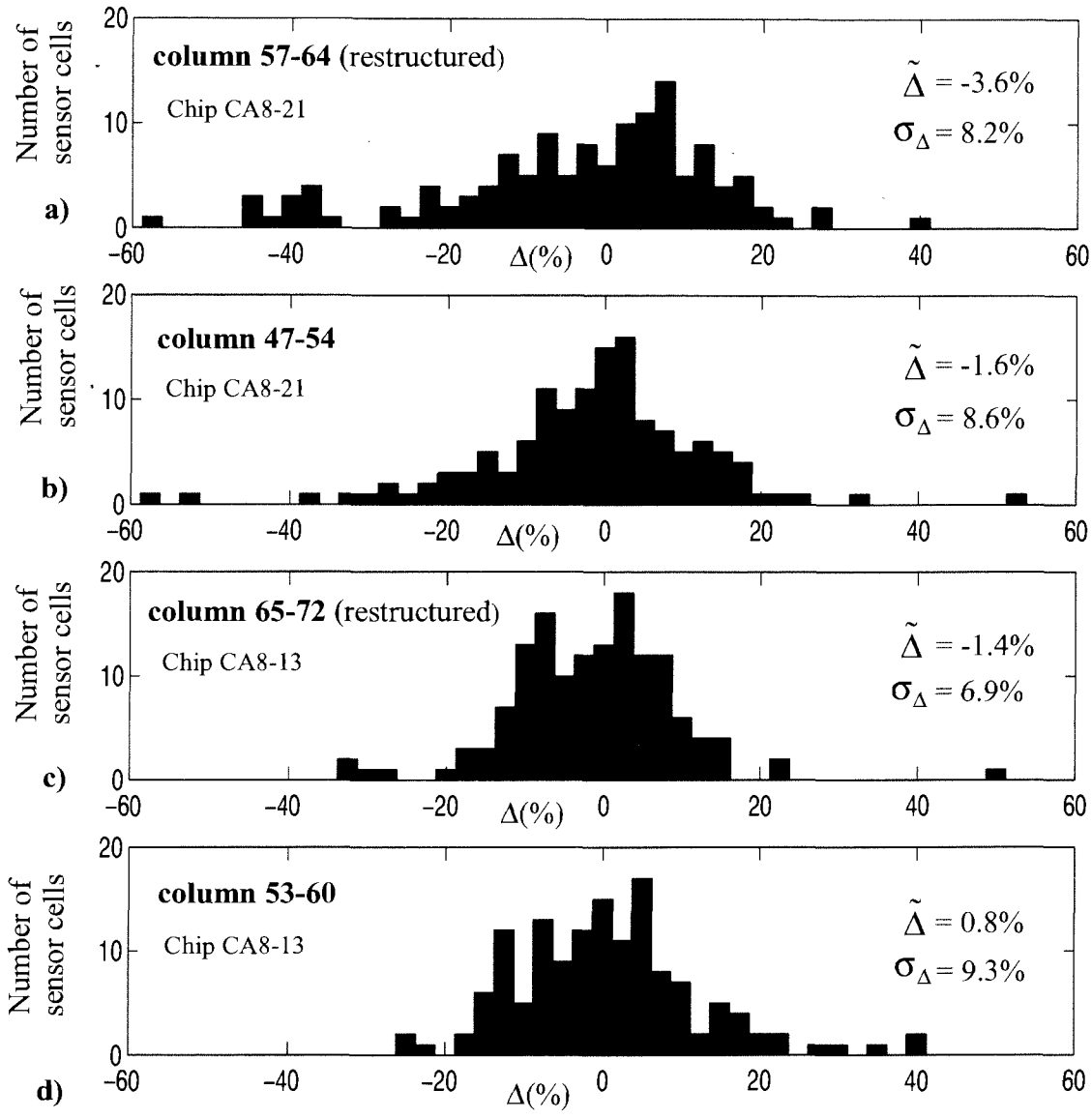


Figure 6.9 Histograms of the comparison parameter for the column scanning circuit restructuring sequence.

values from test to test. Figure 6.9c) shows another restructured segment comprising eight columns of chip CA8-13 along with its adjacent non-restructured segment in Figure 6.9d). Similar behaviors as the one observed so far on all kind of restructuring are noticed. From these results, it has been proven that the column restructuring scheme has a weak effect on the sensor cell responses. No noticeable difference has been measured between the

maximum frequency of operation of the restructured and the non-restructured columns.

6.3.3 Active load

Three spares are available to restructure the current mirror acting as an active load. Figure 6.10 illustrates the initial current mirror with the three possible spares. Different combinations of laser cuts and links are required depending on which spare is needed. Figure 6.10 illustrates the initial current mirror with the three possible spares. The restructuring sequence starts by disconnecting the initial faulty current mirror from the reading bus (lines Da and Db) by laser cutting. Then, in the case of spare 1, located on the same reading bus, only two laser links are required to connect it to the reading bus. The spare 2 is initially wired to the spare reading bus (lines Da_sp and Db_sp), consequently, it has to be laser disconnected from the part of the spare reading bus not directly leading to the Da_sp and Db_sp input/output pads, before being off-chip wired to the initial reading bus. Finally, the same sequence is employed for the restructuring of spare 3, except that an additional step of laser linking the spare current mirror to the spare reading bus is required. As can be seen from Figure 6.10, different combinations of laser links and laser cuts and off-chip wiring can be configured to use any of the current mirrors with one or both reading buses, depending on whether spare column scanning segments are required. All active load restructuring schemes are effective as long as only one current mirror is employed for the entire sensor grid.

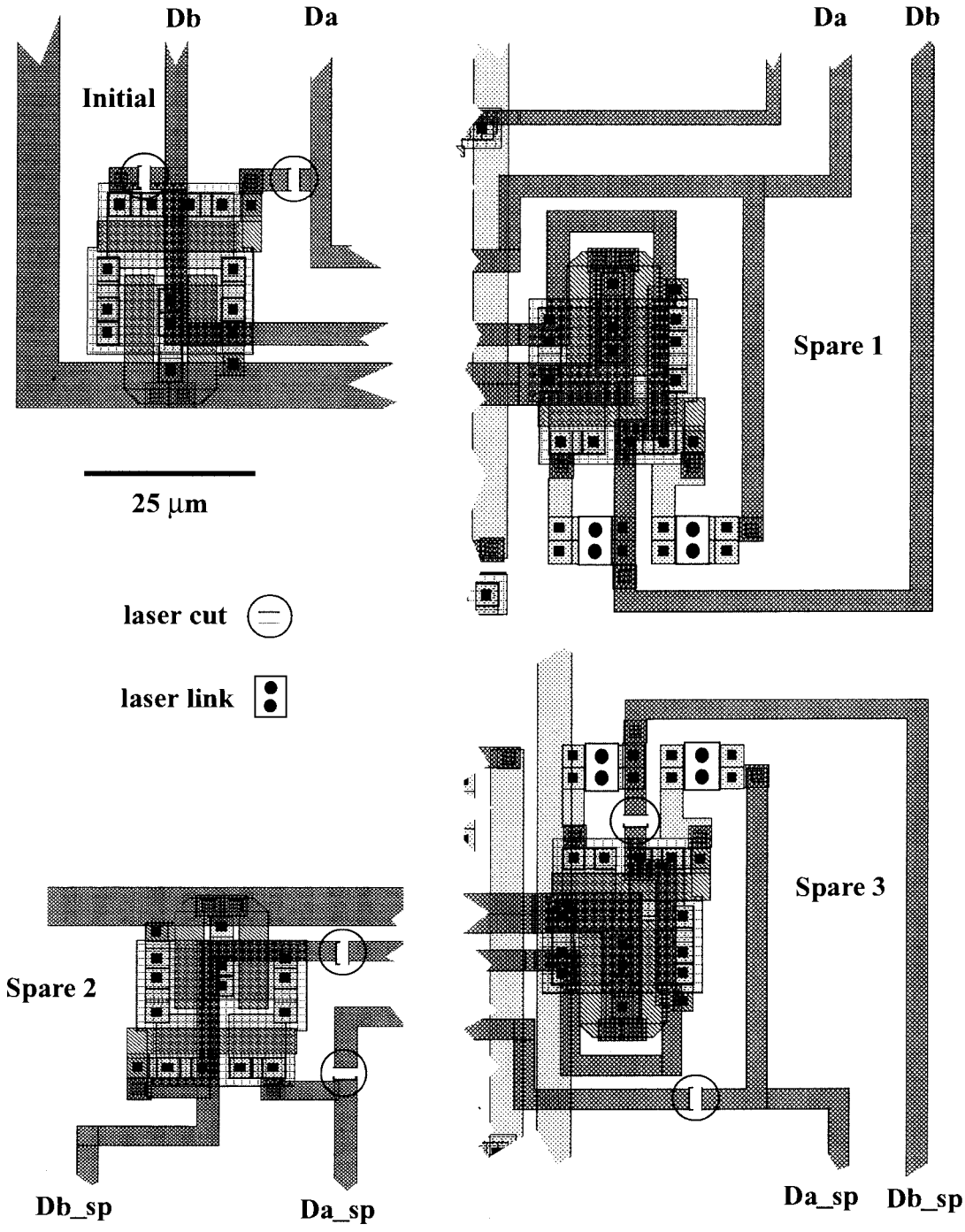


Figure 6.10 Restructuring scheme of the active load.

Figure 6.11 presents two histograms of the response comparison parameters where the cascode current mirror has been restructured on two different chips. As can be seen, these distributions, which include the whole sensor grid, are falling within a comparison

parameter interval of roughly 40%. Measurements of figures 6.3, 6.5, 6.7, 6.9 and 6.11 have demonstrated approximately the same distribution spread, proving the constant nature of the effect causing the response fluctuation, such as noise. Chip CA8-13 experienced an average response reduction of about 22%. On the other hand, using the same restructuring schemes, chip CA8-21 yielded an average response increase of about 15%. These results indicate the crucial dependence of the sensitivity of the sensor grid on the cascode current mirror characteristics. It also reveals the importance of having a good uniformity of the transistor parameters throughout the chip, for the active load redundancy scheme to be reliable.

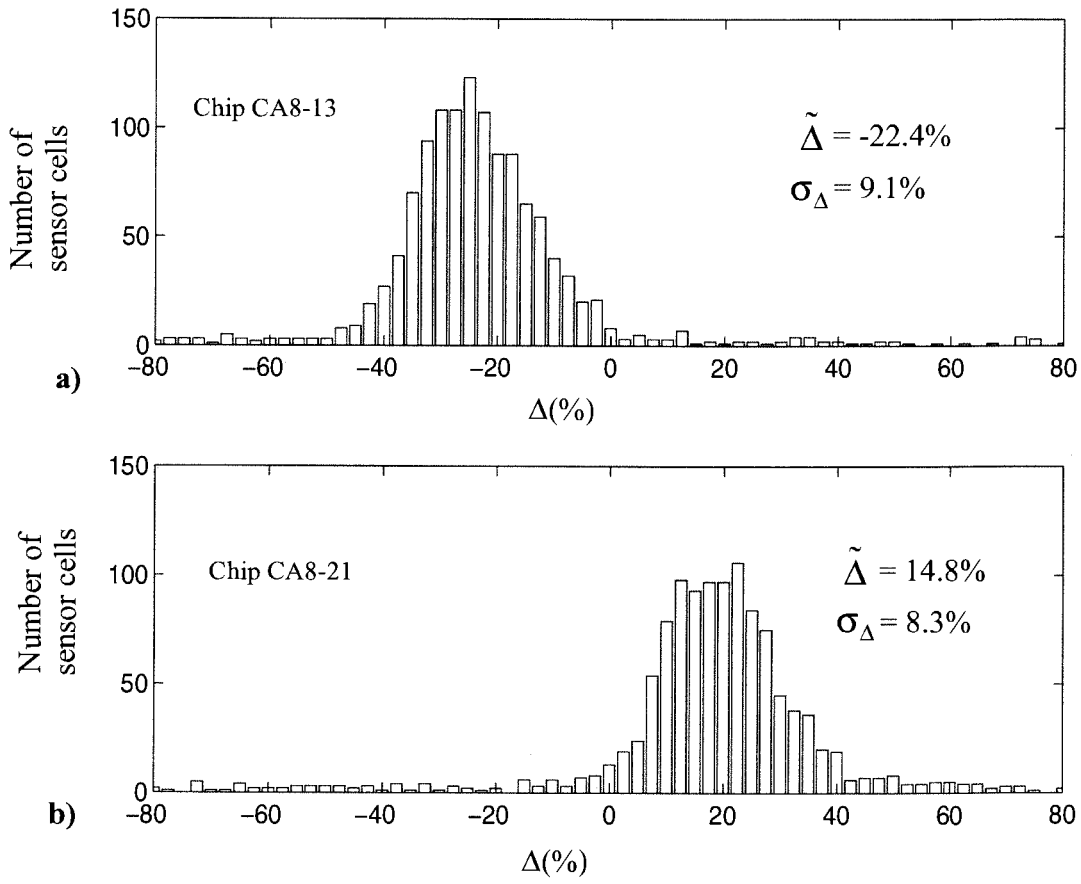


Figure 6.11 Histograms of the comparison parameter for the active load restructuring sequence.

6.3.4 Effect of the active load restructuring on the maximum frequency of operation

Among all the restructuring schemes studied in this chapter, only the active load scenario has a noticeable effect on the maximum frequency of operation. This effect comes from the fact that for every current mirror, is found a corresponding specific VGref, where the sensor grid response is optimum in magnitude and uniformity. Hence, the variations of the maximum frequency of operation are due to differences in the value of the operating voltage VGref. Intuitively, it is possible to deduce a relation between VGref and the maximum frequency of operation. Since the sensor cell to be read works in the saturation region, its current drive is proportional to $(VGref - V_T)^2$, where V_T is the NMOS threshold voltage. This current drive is responsible for charging and discharging the capacitance associated with the reading bus, which includes mainly the metal 2 line capacitance, the parasitic capacitance of the SPDT PMOS transistors attached to them, the output pads capacitance and the oscilloscope probe capacitance. The sensor working in saturation mode acts as a current sink, hence, it is reasonable to assume that the discharge period of the reading bus capacitance is proportional to the inverse of the sensor drive current, meaning that the maximum frequency of operation should be roughly linearly proportional to $(VGref - V_T)^2$. Figure 6.12a) presents a plot of the measured maximum frequency of operation as a function of the $(VGref - V_T)^2$, for five sensor array chips. As expected, the behavior is fairly linear with a slope transition occurring at an abscissa value of about 0.1 V^2. This transition is caused by the effect of the charging current flowing from the current mirror, which slows down the discharging rate. Beyond 0.1 V^2 this current becomes negligible, allowing higher maximum frequencies (Fmax). In order to verify this experimental result, SPICE transient analysis were performed with VGref defined as the sweeping variable. The results of $1/t_d$ as a function of $(VGref - V_T)^2$ are presented in

Figure 6.12b). The method used to measure t_d is the same as the one described in Figure 6.1. A slope transition in the curve is also observed, although the transition point is different, most likely due to differences between the real transistor parameters and the ones of the model used for the simulation. For high values of $(VGref - V_T)^2$ the relation is no longer linear, due to the fact that the sensor operating region is slowly shifting in the linear operating region, reducing the current gain for each $(VGref - V_T)^2$ step, as explained in section 3.2.3.

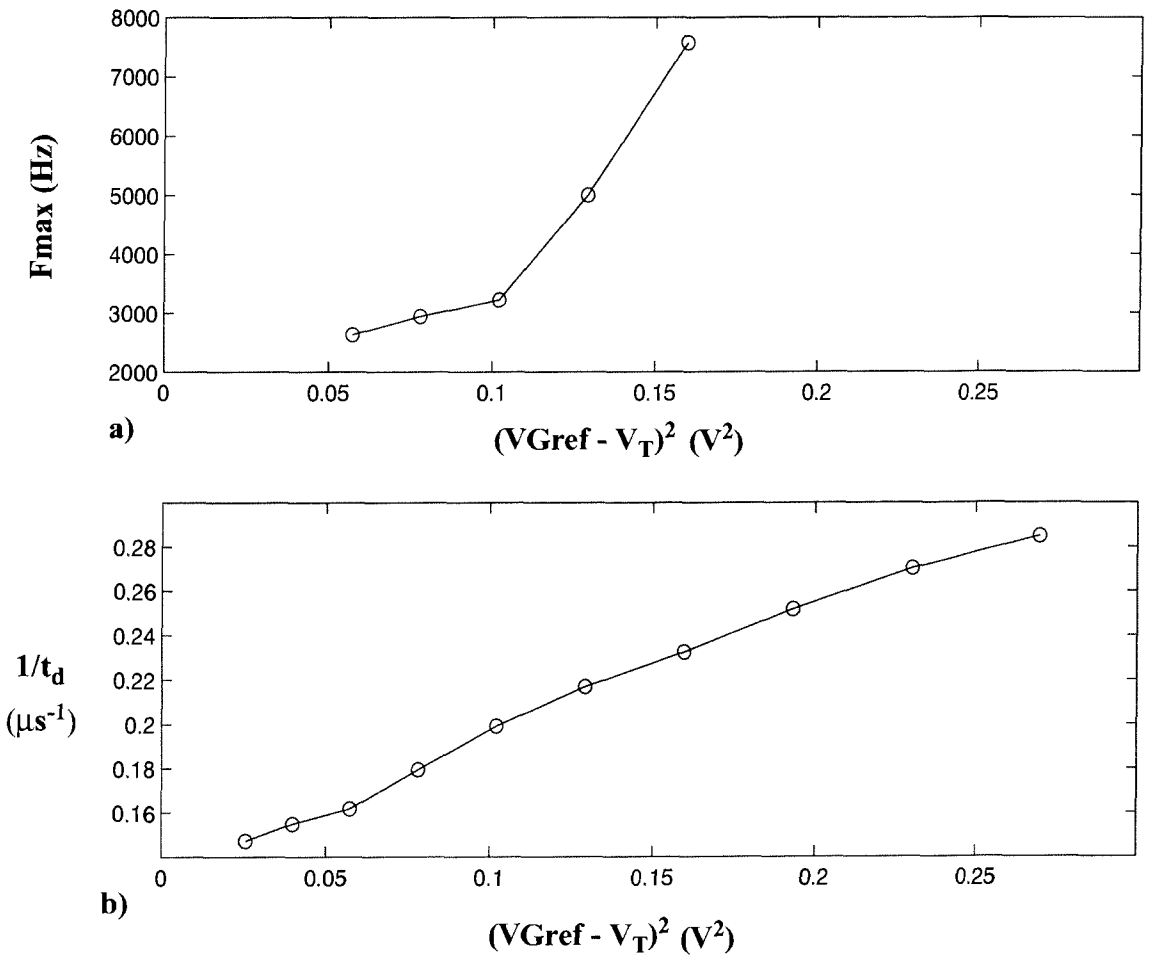


Figure 6.12 Plots of a) the maximum frequency of operation and b) the discharging time.

6.4 Yield Gain

Table 6.1 gives the yield summary of 23 tested and repaired chips. Thanks to the redundancy strategy, the initial yield of 39% has been raised to 61%. From the fourteen initially defective chips, five have been successfully restructured, showing the importance of having a redundant design for yield improvement even for this medium size prototype of 6 mm by 3 mm. Indeed, it would be expected that larger area devices fabricated with the same process would show more row and column failures. The second column of Table 6.1 shows the defective circuits involved in the chip failures, and the corresponding number of chips found defective due to these failed circuits. The cause of failure of four chips could not be attributed to one of the three scanning and readout circuits, or a combination of those three. At the time this LAMSA prototype was fabricated, the Mitel 1.5 μm CMOS process was not mature and had a high defect density. This explains why there is a low initial yield of 39%.

	Circuit involved	Number of chip	Percentage of total tested
Initially Working		9	39%
Defective (before restructuring)	Row Scanning Circuit (RSC)(2)	14	61%
	Col. Scanning Circuit (CSC) (4)		
	CM and reading bus (3)		
	RSC and CM (1)		
	Non-Identified (4)		
Successfully rescued	Spare RSC (2)	5	22%
	Spare CSC (1)		
	Spare CM (1)		
	Spare RSC and Spare CM (1)		

Table 6.1 Yield gain results from 23 tested chips.

From the failed chips having a known cause, the number of those that have been successfully rescued using the corresponding spare circuits is indicated. In the four failed Column Scanning Circuit (CSC) chips, only one could be repaired with a spare CSC. This result can be explained from the fact that for some of the repairs, the chip had been accidentally left powered on. As a result through the restructuring process, laser induced lach-up may have occurred and destroyed the chip. Since the CSC restructuring scheme involves a high number of cuts and links, two cuts and two links per column, compared to one cut and one link per row for the row restructuring scheme, it has the highest probability of generating latch-up from laser zapping. Among the three defective chips, due to the current mirror and the reading bus, only one had been repaired by linking a spare. Since, according to the Monte-Carlo simulation results of section 4.5.2, the yield of the current mirror redundancy scheme is almost 100% for defect densities lower than 700 faults/chips, this result suggests that the fault introduced by the current mirror is rather of a parametric nature, and could also be related to the bus connecting the CM to the SPDT switches.

6.5 Summary

The influence on the sensor cell responses of the restructuring schemes employed for the sensor grid local redundancy and the scanning and active load circuits global redundancy have been evaluated using the comparison parameter defined in chapter 5, section 5.3.2. Only the active load restructuring scheme has produced a significant effect on the sensor cell responses, revealing the direct dependence of the sensor grid response on the cascode current mirror characteristics. The absence of any effect from other restructuring schemes can be easily understood from the fact that the path resistance

between the current mirror and the sensor is fixed by the pass transistors of the SPDT switch. In the best operating conditions, when V_{GS}(NMOS) and V_{SG}(PMOS) equal 5 V, the total serial resistance of the NMOS and the PMOS transistor working in the linear region is about 6.3 KΩ. The average resistance of a laser link is 75 Ω . Therefore, about eight laser links can be added in series onto the current path before changing the total resistance value of 10%. The maximum number of laser links that can be added on the same current branch for the actual prototype of the LAMSA is five.

The active load restructuring scheme has been found to be the only restructuring strategy affecting indirectly the maximum frequency of operation. This effect comes from the fact that most of the time a change in the current mirror requires a new biasing voltage VGref. Helped with SPICE simulations, the dependence of the maximum frequency of operation on VGref has been quantitatively demonstrated. Due to the redundancy schemes, the initial yield of a sample of 23 chips was increased by 56%.

Chapter 7

Applications of the LAMSA

This chapter discusses two major applications of the LAMSA. In the first section, a defects detector for steel pipelines is described, whereas section 7.2 concerns a compliant tactile sensor using a LAMSA die. More emphasis is put on the tactile sensor, since it involves a higher level of technical complexity and has a potentially wide range of applications. Finally, section 7.3 presents some magnetic field mappings obtained with the LAMSA.

7.1 Defects Detector for Steel Pipelines

Accurate monitoring of pipelines is becoming increasingly essential, given environmental concerns regarding possible pipeline ruptures or leakage and the high costs of pipeline repair and replacement. Since oil and gas pipelines are normally buried, in-service inspection is performed by pumping a Smart Electronic Inspection Pig through the pipeline from one compressor station to the next.

The most commonly used inspection tools employ the Magnetic Flux Leakage (MFL) technique to detect internal or external corrosion. The MFL Inspection Pig relies on strong permanent magnets to magnetically saturate the pipe wall[11]. Abnormalities in the pipe wall, such as corrosion pits, result in magnetic flux leakage at the pipe's surface as shown in Figure 7.1. Actual MFL detectors utilize Hall probes or induction coils to detect the leakage flux as it moves along with the Inspection Pig.

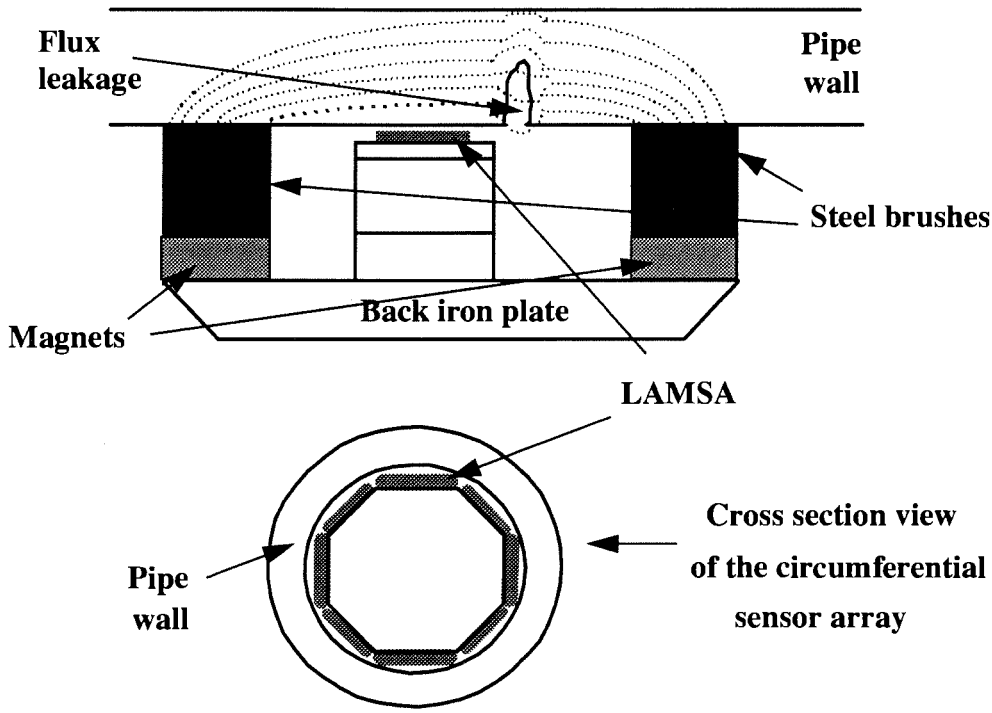


Figure 7.1 Application in defects detection for steel pipelines.

The demands on magnetic inspection tools are now shifting from mere detection, location and classification of pipeline defects, to accurate measurements of defect size and geometry. A magnetic field imaging array such as the LAMSA fits very well within these new requirements. An inner circumferential array of LAMSA, positioned as drawn in the cross-sectional view of Figure 7.1, could generate a real time image of the magnetic field topology at the pipe wall surface as the Inspection Pig moves along. The high spatial

resolution of the LAMSA would allow for the detection of the finest cracks and defects as well as give an accurate measurement of their dimensions.

7.2 Compliant Tactile Sensor

7.2.1 Performance requirements

H. R. Nicholls and M. H. Lee, in their paper entitled "A Survey of Robot Tactile Sensing Technology"[45], mentioned a list of eight specifications identified as the most important for tactile sensing:

1) The sensor surface should be both compliant and durable.

2) The spatial resolution should be 1 to 2 mm.

3) A range of 50 to 200 tactels (tactile pixels) is acceptable (e.g., 5x10, 10x20).

4) The sensor should be able to detect as little as 5 grams (.049 N).

5) A dynamic range of 1000:1 is satisfactory.

6) The sensor must be stable, repeatable, and without hysteresis.

7) The response must be monotonic, thought not necessarily linear.

8) The time resolution for the sensor should be at least 100 Hz.

In addition, the authors mentioned the usefulness of a tactile sensor to be able to carry out local data processing, thus providing compact and high-level information for any automated system to which it may be connected. Depending upon the applications, some of the specifications listed above are more or less important.

7.2.2 Tactile sensor using magnetic transduction methods

Tactile sensors using transduction are divided into two basic categories. The first category groups the sensors using mechanical movement to produce a change in the

magnetic flux. The second category concerns magnetoelastic materials which show a change in the magnetic field when subjected to mechanical stress. Typical examples of these two types of sensors are given in references [46], [47] and [48]. The tactile sensor built from the LAMSA fall into the first category, Figure 7.2 illustrating its principle. The surface of the die is covered with a compliant material coated with a magnetized layer. This flexible magnetic sheet acts as a skin for the tactile system. Whenever an object is in contact with the skin, the top magnetized layer is displaced towards the surface of the LAMSA, increasing locally the magnetic field strength at the surface. As a result, the morphology of the part of the object in contact with the sensor can be easily found from one readout of the array, whereas several consecutive readouts would give information about the slipping movement of the object. Also the strength of the magnetic field measured in the contacted region is proportional to the mechanical pressure applied on the sensor by the object, and vice versa.

From the list of important tactile sensor specifications mentioned in section 7.2.1, items 2, 3 and 7 are largely achieved due to the property of the LAMSA itself. Items 1, 4, 5 and 6 will be strongly dependent on the type of material employed for the covering sheet. Considering the LAMSA maximum operating frequency of 7576 Hz, measured in chapter 6, the time resolution is about 7.6 times better than the minimum requirement of item 8. For the prototype array of 24 rows and 75 columns of tactels, this time resolution allows for a reading rate of four frames per second. This last feature can be greatly improved upon by reducing the spatial resolution, and at the same time, decreasing the tactel count.

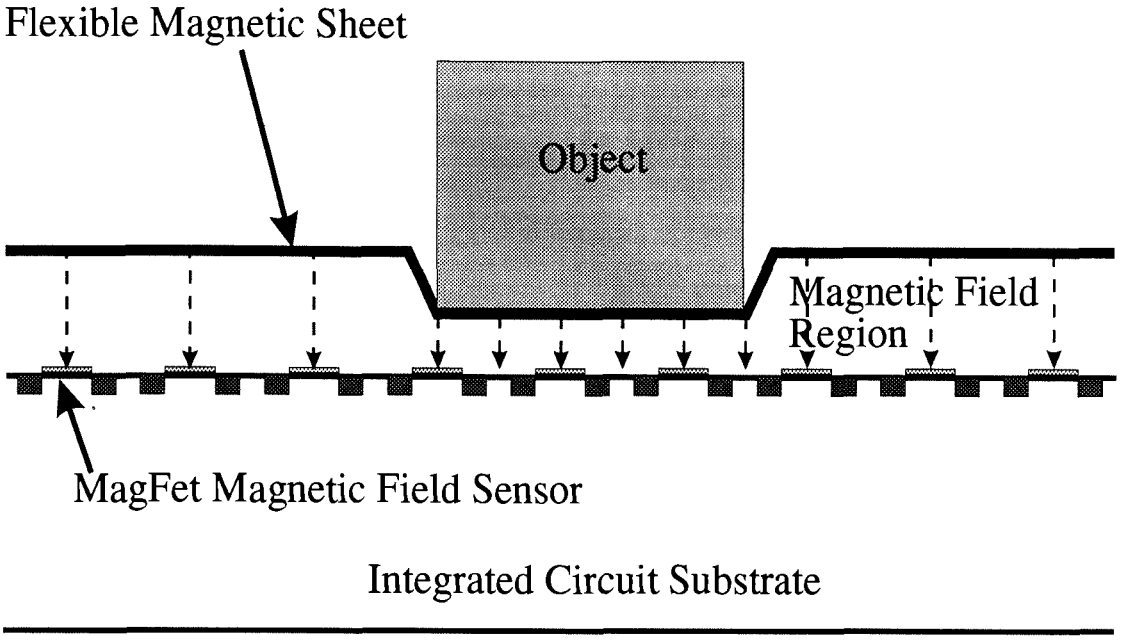


Figure 7.2 Tactile sensor using a LAMSA die.

7.3 Magnetic Field Mapping Experiments

Figure 7.3b) presents the mapping of the magnetic field generated by a copper wire where a DC current of 10 A is flowing. As shown in Figure 7.3a), the wire runs along a side of the sensor array, perpendicular to the rows. The magnetic field topology of Figure 7.3b) is obtained from one row of a sensor array comprising 35 columns. Near the wire, even though the field strength is maximum, the response is weak, since the field lines are crossing the sensor array surface at an angle nearly parallel to the surface. Travelling away from the wire, the response reaches a maximum, where the field lines become perpendicular to the surface, and start decreasing due to the fading field strength away from the source wire. This mapping was obtained directly from the raw data readout of the sensor array: no calibration algorithm was used.

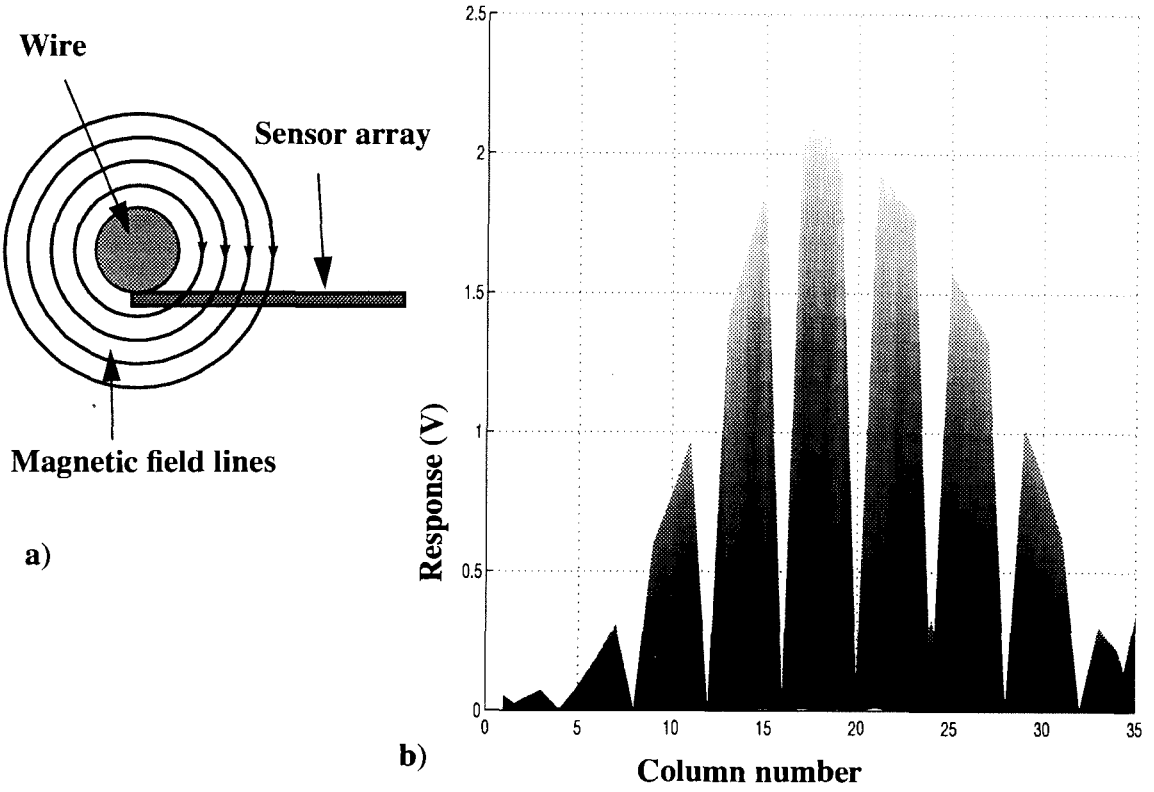


Figure 7.3 a) DC current generating a circular magnetic field, b) Magnetic field topology measured at the surface of the sensor array.

In Figure 7.4a), a rectangular piece of a magnetized tape was cut out and positioned in the center of a sensor array comprising 24 rows and 74 columns. This magnetized tape is commercially available in hardware stores and is used to hang small metallic tools. It has a thickness of about two millimeter. Figure 7.4b) depicts the magnetic field topology produced by the piece of tape. The non-uniformity obtained in the responses of the tactels located underneath the tape could be reduced by using the calibration algorithm developed in chapter 5. This example demonstrates the tactile capability of the sensor array in detecting the morphology of a part of an object contacting the magnetized tape. A thinner version of this magnetized tape could act as the magnetized layer described in the tactile sensor application of Figure 7.2.

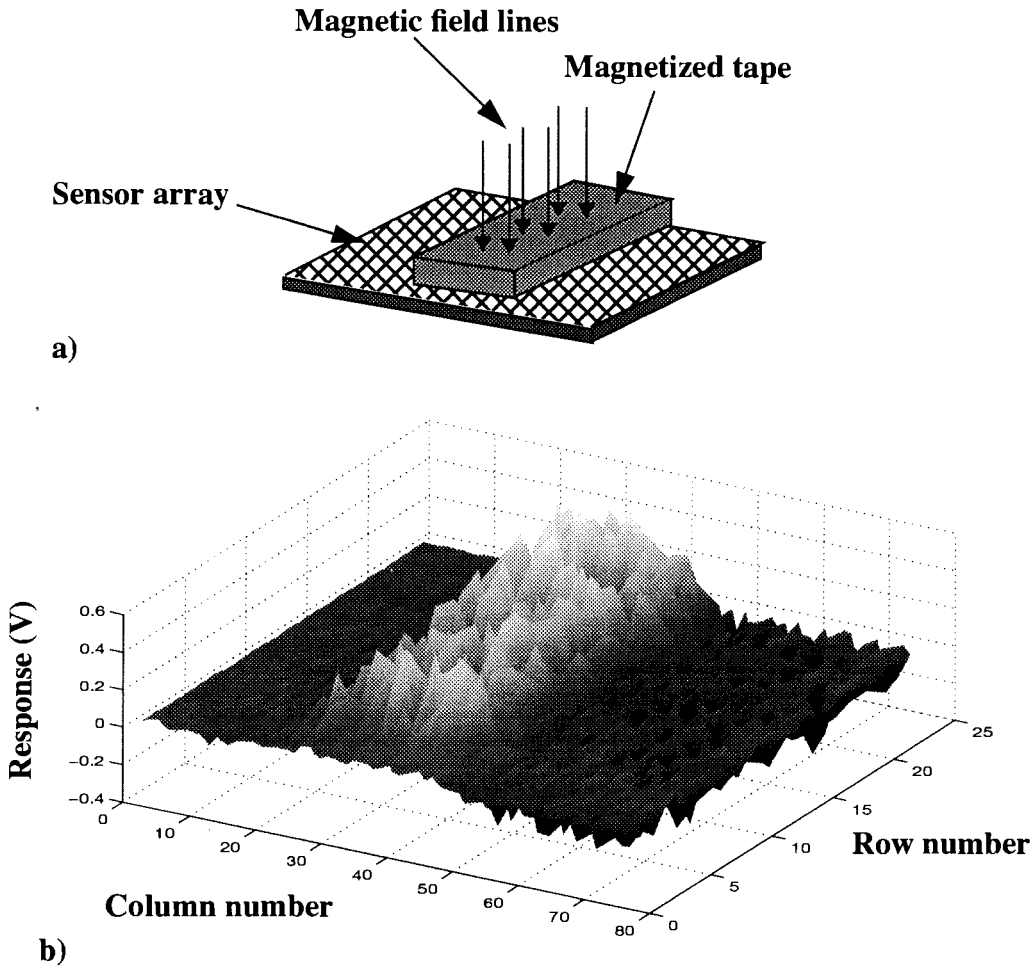


Figure 7.4 a) Piece of magnetized tape positioned in the center of the sensor array. b)Corresponding non calibrated magnetic field topology measured at the surface.

7.4 Summary

In this chapter, two possible applications of the LAMSA were described. The first consisted of a defects detector for steel pipelines, and the second of a tactile sensor. For these applications, conventional die sizes (< 1 cm^2) are insufficient. The redundancy strategy developed and tested in this thesis allows for the fabrication of large sized magnetic field sensor arrays to be economically viable due to improved production yield.

Chapter 8

Conclusion

The work presented in this thesis aims at proving the feasibility of large area integrated sensor arrays, using redundancy schemes for defect avoidance. The study has been performed on a prototype of a large area magnetic field sensor array, where the laser link technology was used as the restructuring tool. This chapter first summarizes the contribution of this work in the field of large area transducer system. Section 8.2 reports on the major findings of the simulation results, and underlines some important features of a fault tolerant design for large area sensor arrays. In section 8.3, design modifications and additions that would improve the performance of the LAMSA prototype, while keeping its restructuring abilities, are discussed. Finally, the conclusion ends with a look into the possible impacts of the techniques developed in this thesis on future microelectronic sensor array systems.

8.1 Thesis Contribution in the Field of Large Area Sensor Arrays

For the first time, a yield simulation tool was developed to study the robustness of different redundancy strategies of the sensor grid and its surrounding control circuits to various fault densities and clusterings of the negative-binomial distribution. Previous experimental works on circuit restructuring only briefly addressed the problem of rerouting analog circuitry. This thesis explored this problem by studying the effect of the restructuring on the sensor grid response. The effect was found to be negligible, since the resistance of the laser link is small compared to the one of the active current mirror used as active load and the transistors of the steering circuit. It is expected that these results and the measurement and response comparison methods developed in this thesis will pave the way towards studies of restructuring schemes for other types of large area sensor arrays. Finally, a novel double drain/double source merged MAGFET sensor has been developed to reduce the number of signal lines required to address the sensor grid, and hence increase the robustness of the device against processing defects. The merged MAGFET sensors also allowed the design of a simple and compact readout circuit. Having the laser link structures directly integrated to the drains/sources of the MAGFET made the redundancy scheme area efficient.

8.2 Successful Redundant Designs for Large Area Sensor Arrays

Contrary to the yield results obtained for the sensor grid, which are rather specific to the LAMSA case, the yield study of the readout circuit is more general and would remain valid for other types of sensor arrays using similar circuits. From the Monte-Carlo simulations results, the redundancy strategy of the active load has been found very effective due to its small size and its three spares. However, the process uniformity is an

important parameter for this analog cell, and could greatly reduce the robustness of this redundancy scheme. Among the 23 tested chips of Table 6.1, the row and column scanning circuit redundancy schemes have been very effective in rescuing four of the seven chips initially identified as defective because of these circuits. Simulation results have also demonstrated that the most robust redundancy scheme for the scanning circuits is achieved when the swapping segments comprise only one module. This scheme is only possible for triple metal process. However, for processes presenting defect clustering, such as the actual CMOS processes, simulations have shown that longer swapping segments, comprising four or eight modules, achieve about the same robustness as the one module segment.

Overall, the effect of adding spare signal lines to each sensor cell has increased the robustness of the sensor grid to processing defects affecting the metal lines, their vias and their contacts. This yield improvement is greatly reduced as the defect clustering increases. In the case of defects affecting the sensor elements, or more precisely the sensor gates in the LAMSA case, grid patterns comprising sensor cells sharing the same gate are more vulnerable than individual gated sensors. However, this discrepancy vanishes as the defect clustering increases. For a wide range of defect densities and clustering and for all the grid patterns studied, the pixel redundancy scheme, comprising at least two sensor cells from which one of them must be working to obtain a valid pixel, resulted in a significant yield improvement. The main draw back of this scheme is that some extra processing is required to extract the images. The advantage of having sensor grid patterns made of sensor cells sharing the same gate resides in their potential to achieve denser grids for applications demanding high spatial resolution.

8.3 Design Improvement of the LAMSA Prototype

The non-uniformity of the sensor grid response has been explained in terms of the sensor cell intrinsic current imbalance and the variation of the threshold voltage across the array. The Idn and Vtn matching parameters revealed the magnitude of those effects for the 1.5 μm Mitel CMOS process. By putting two resistors of 10 MΩ at the output of the reading bus, the response uniformity is improved by reducing its standard deviation by approximately eight times. However, the average response is also decreased by approximately 40%. This gain in uniformity comes from a reduction in the output impedance of the readout circuit due to the added resistors. The same effect could be obtained by increasing the width of the PMOS transistors of the cascode current mirror. To compensate for the drop in sensitivity, the PMOS transistor of the SPDT switch could be replaced by an NMOS transistor driven through an inverter. Thus, the saturation point of the PMOS transistor is avoided, meaning that more current could flow in the sensor and produce a larger response. However, this larger current would also accentuate the mismatched effect and reduce the response uniformity.

The advantage of using a simple active load resides in its simplicity to perform the restructuring. More sophisticated loading and biasing circuits would be required in order to qualify this device for an eventual customer. A better design would include a temperature compensated reference voltage to bias the sensor gate, and to regulate the active load currents. By doing so, the sensor responses would remain stable for a wide range of gate biasing voltages and variations of temperature and process parameters. Also, a proper amplifier and analog driver would be required to interface the sensor grid reading lines with the external world. Then, a higher maximum frequency of operation could be

achieved.

As the process geometry decreases and CMOS systems become faster, enhanced laser link techniques offering better performance are developed. A recent paper reported a compact vertical laser link structure of 10 μm by 10 μm[49], forming a 3 Ω resistor link directly between two superposed metal layers.

8.4 Possible Impacts of the Techniques Developed

The future of large area sensor arrays looks rather promising. Recently, new device prototypes that could easily benefit from the defect avoidance feature have appeared. Lucent Technologies has developed a hard surface finger print sensor for low cost fingerprint recognition system aimed at consumer applications[9]. A silicon chip about the size of a stamp is made of an array of capacitors where one plate is the metal 3 layer and the second is the surface of the finger. The capacitive fluctuations generated by the hills and the valleys of a fingerprint form an image. This company is planning to add onto the chip a RISC engine to encode and perform on-chip fingerprint recognition. This will open the market to stand-alone applications such as cash registers, ABM machines, doorknobs and cars. With the added processing blocks, the chip would reach a critical size, and experience some yield reductions that could boost its price and therefore reduce its potential to reach wide market applications. Defect avoidance techniques could substantially increase the yield and alleviate production costs. For this type of application requiring low imaging resolution, redundancy schemes using subpixels, spare signal lines and redundant scanning circuits, such as the ones presented in this thesis, could be easily implemented.

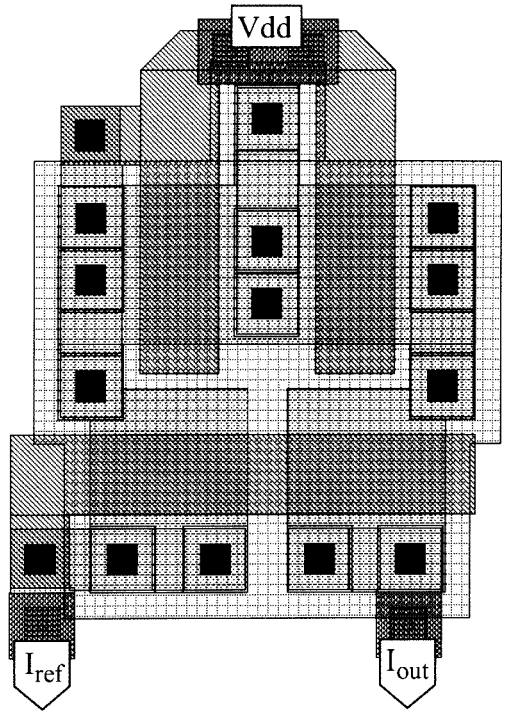
Another field of interest in the sensor array community that has generated a lot of activity recently is CMOS imaging sensor arrays. The target is the potentially wide applications of digital cameras[50]. The advantages over wet film camera are considerable; direct link with a PC system, instant views of pictures through an LCD, the possibility of scanning and rejecting the pictures stored in the camera memory, downloading the picture memory through a phone line or via a cellular phone, etc. However, to access a wide market, including the professional photo industry, digital cameras have to produce good quality post card size photos, meaning sensor arrays of more than one million pixels. The CMOS process is a good candidate to achieve this goal. Its advantage over CCDs are: cheaper process, low power, single supply voltage and possibility of adding on-chip processing. Unlike CCD processes, the CMOS process is not optimized for photonic applications; hence, to obtain a reasonable sensitivity the light sensor must have a large surface. Three transistors per pixel are usually added to the light sensitive surface in order to achieve the reset, the select and the transconductance buffering functions, resulting in a pixel size of about 10 μm^2, even for submicron CMOS technologies. Therefore, a one million pixel monochrome array would be 1 cm^2 alone, excluding the surrounding sensing amplifiers and scanning circuits. For colour arrays, four subpixels per pixel are required, generally one with a blue filter, one with a red filter and two with green filters, meaning an array size reaching 4 cm^2. Again, a redundant design with defect avoidance features could lower the price of an imaging sensor array with on-chip processing and open the market for digital cameras.

8.5 Summary

From the 56% yield improvement obtained on the 23 tested LAMSA chips, the success of the redundant design strategies coupled with laser link restructuring is undeniable. However, before opting for this solution, a serious financial analysis should be undertaken. This analysis should include some yield simulations using carefully selected defect distribution parameters of the targeted process. The process selected should be relatively mature and have a well documented history of its defect density and the fluctuations of its process parameters. A fully automated laser link table represents a serious investment that would pay off only if the demand for a device justifies a reasonable volume.

Appendix A: Circuit Layouts

a) Dimension:
33μm x 25μm



b) Dimension:
46μm x 30μm

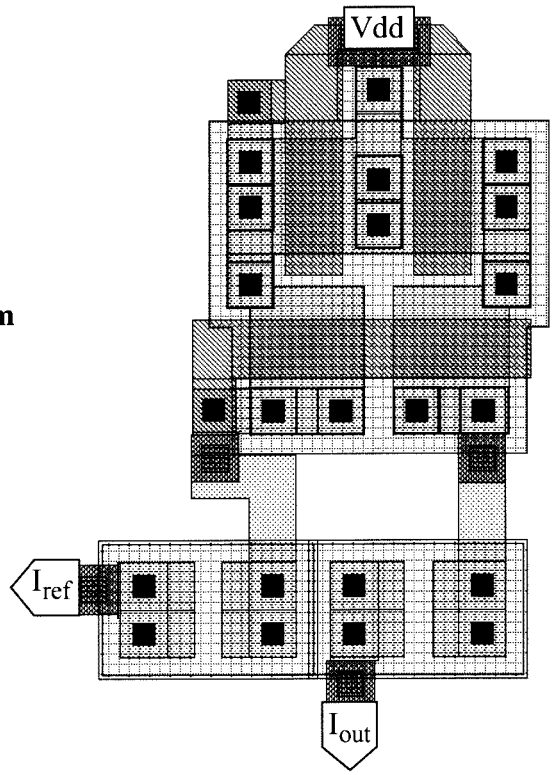
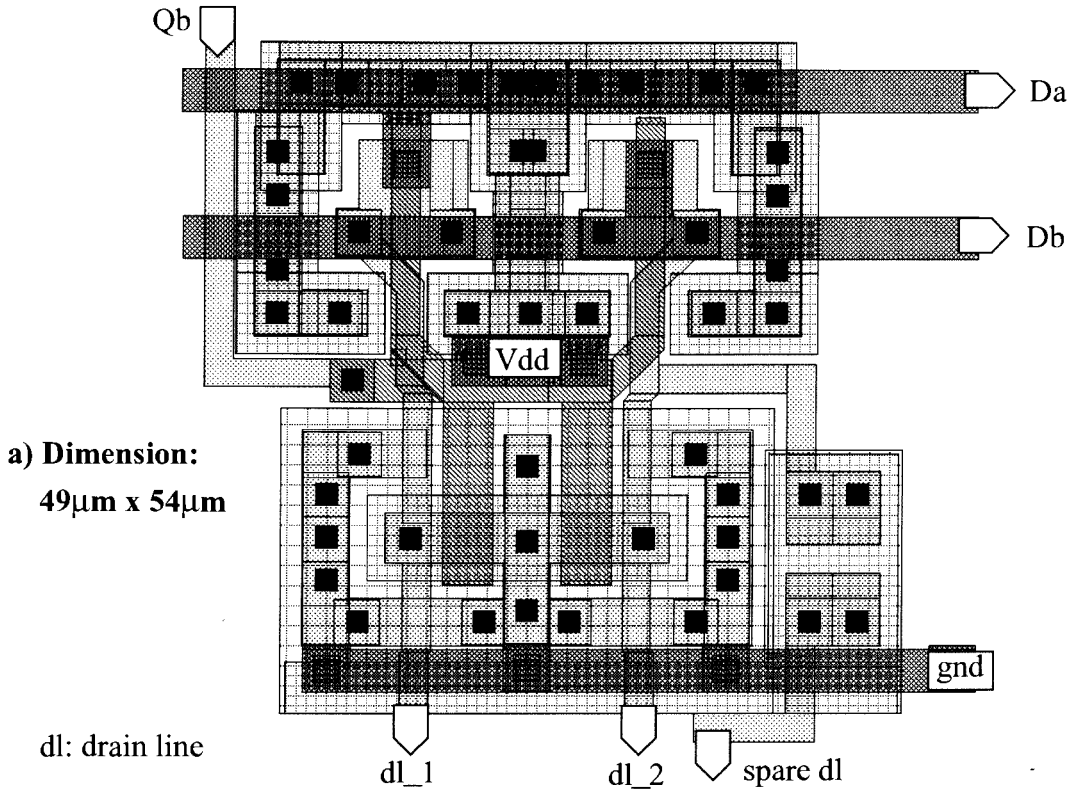
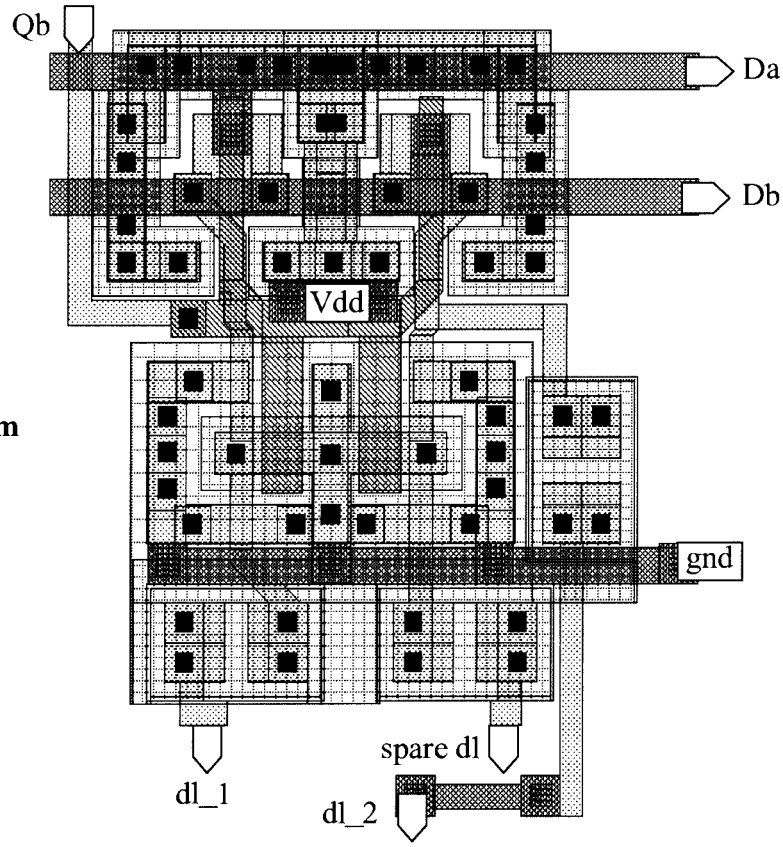


Figure A.1 Layout of the cascode current mirror a) without and b) with restructuring laser links.



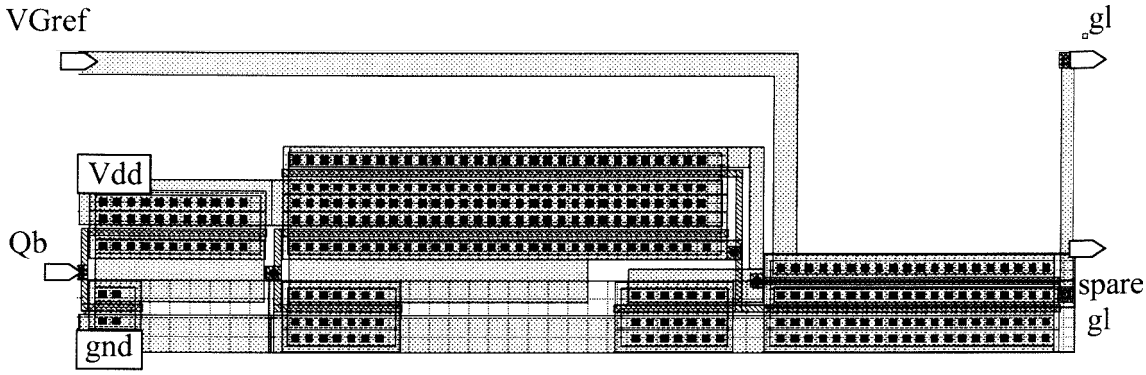
a) Dimension:
49μm x 54μm

dl: drain line

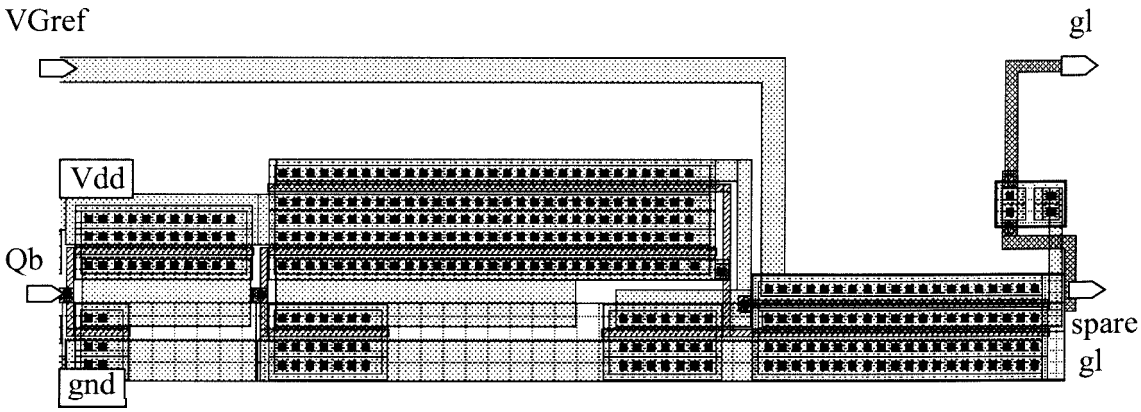


b) Dimension:
65μm x 54μm

Figure A.2 Layouts of a) a pair of SPDTs and b) a spare pair with restructuring laser links.

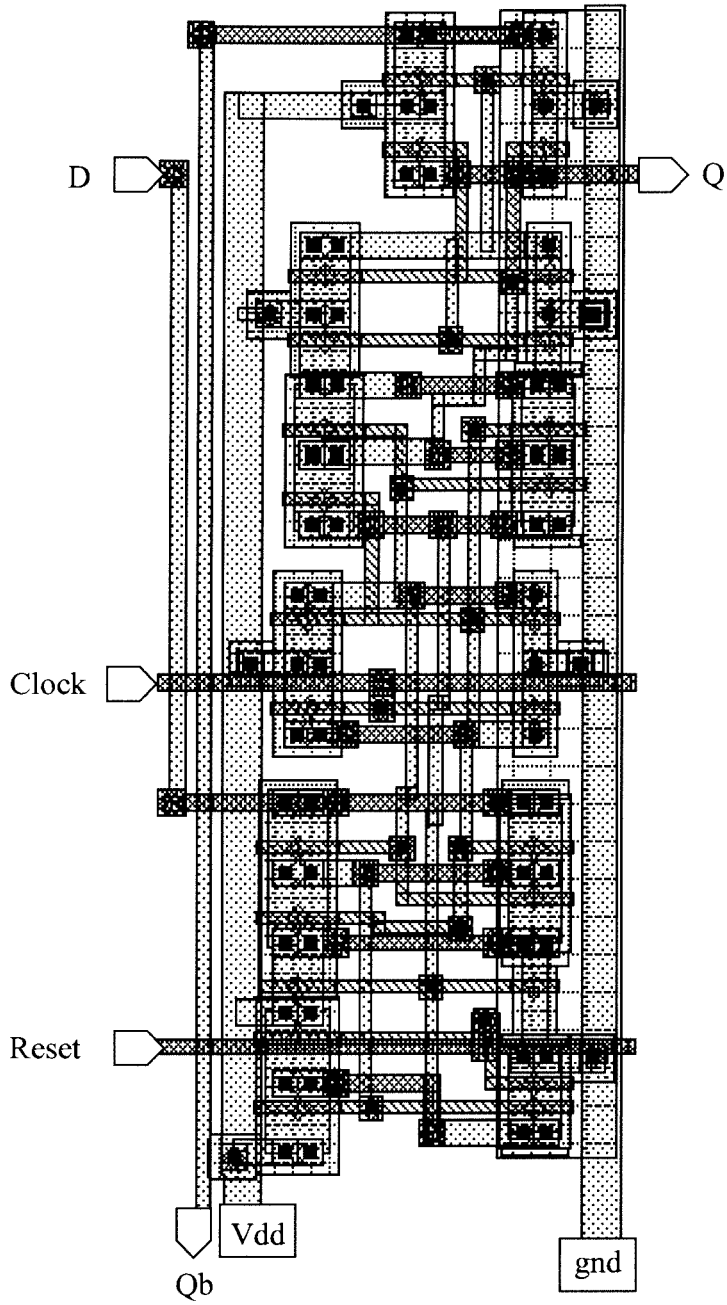


a) Dimension: 78μm x 216μm gl: gate line



b) Dimension: 78μm x 219μm

Figure A.3 Layouts of the a) driver and b) the spare driver with the restructuring laser link.



Dimension: 160μm x 61μm

Figure A.4 Layout of the D flip-flop cell with synchronous reset.

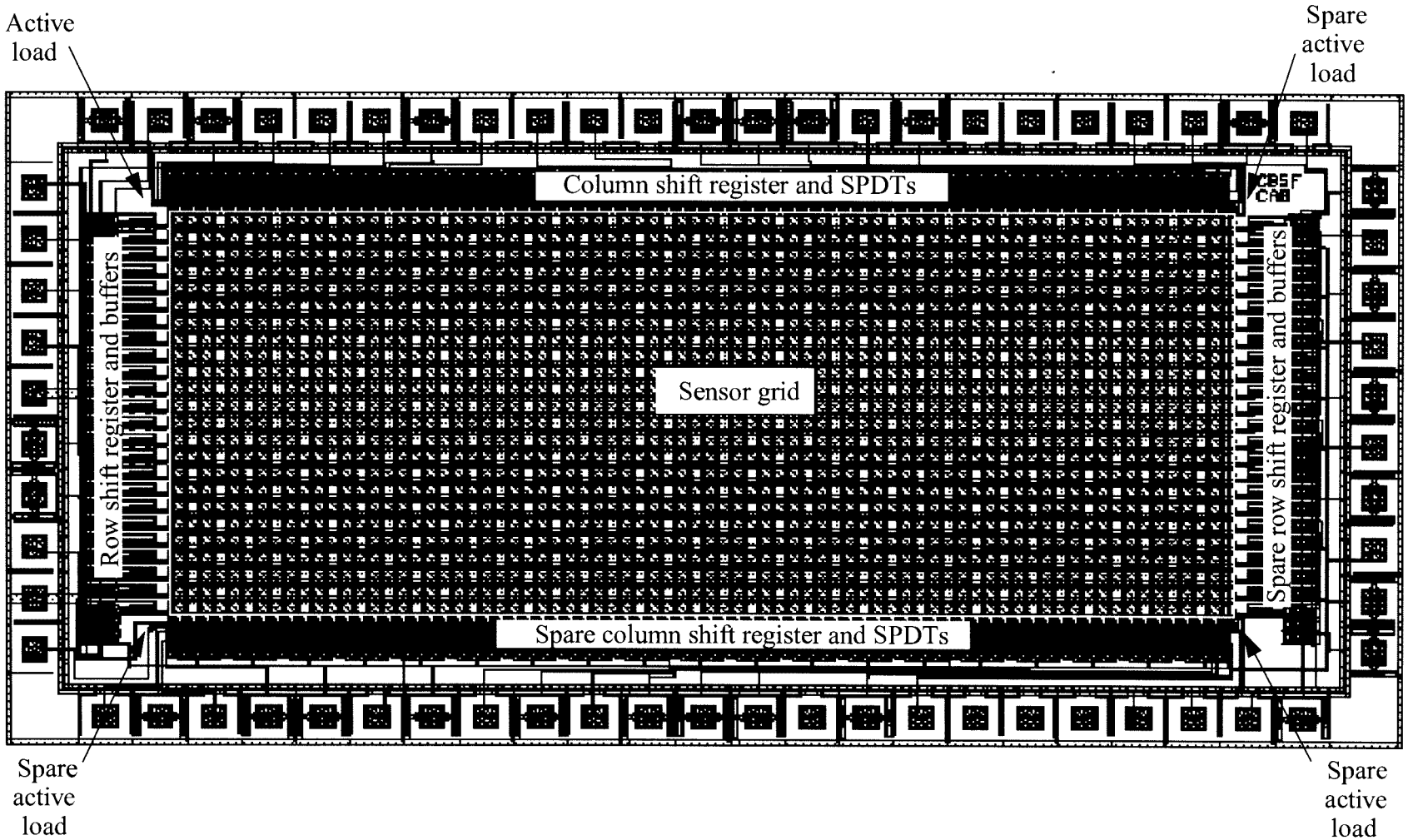


Figure A.5 Layout of the fully restructurable LAMSA having an array of 24 x 74 sensors (Die dimension: 3.1 x 6.2 mm).

Appendix B:

SPICE Input File for the Simulation of Figure 3.10

```
Node voltages and Id1
*
****** HSPICE
*
.MODEL NMITEL nmos
+     level  =     3.0
+     ld     =    1.941e-07
+     dw     =    -1.279e-07
+     xl     =    -1.269e-07
+     vto    =    0.8404
+     tpg    =    1.0
+     nsub   =     1.345e+16
+     cgdo   =     2.716e-10
+     cgso   =     2.716e-10
+     capop  =     4.0
+     tox    =    2.671e-08
+     acm    =     0.0
+     js     =    2.50e-03
+     cj     =    3.161e-04
+     cjsw   =     2.145e-10
+     mj     =    0.3570
+     mjsw   =     0.2847
+     pb     =    0.7191
+     rsh    =    202.6
+     gap1   =     4.73e-04
+     gap2   =     6.36e+02
+     delta  =     1.721
+     eta    =    2.223e-02
+     kappa  =     0.2620
+     nfs    =    5.161e+11
+     theta  =     4.090e-02
+     vmax   =     2.383e+05
+     xj     =    2.197e-07
+     uo     =    527.2
+     tref   =    25.0
*
.MODEL PMITEL pmos
+     level  =     3.0
+     ld     =    1.735e-07
+     dw     =    -2.179e-07
+     xl     =    -1.267e-07
+     vto    =    -0.7281
+     tpg    =    -1.0
+     nsub   =     3.947e+16
+     cgdo   =     2.534e-10
+     cgso   =     2.534e-10
+     capop  =     4.0
+     tox    =    2.672e-08
```

```
+    acm   =     0.0
+    js    =    2.50e-03
+    cj    =    2.898e-04
+    cjsw  =     2.052e-10
+    mj    =    0.3566
+    mjsw  =     0.2450
+    pb    =    0.2259
+    rsh   =    393.4
+    gap1  =     4.73e-04
+    gap2  =     6.36e+02
+    delta =     1.829
+    eta   =    1.522e-02
+    kappa =     9.994
+    nfs   =    9.275e+10
+    theta =     0.1049
+    vmax  =     2.795e+05
+    xj    =    1.762e-07
+    uo    =    193.7
+    tref  =    25.0
*
**** Cascode Current Mirror Description ******************
*
.SUBCKT CAS VD IREF IOUT
*
*  D   G   S  B
MQ1 D1   D2   VD 1 PMITEL L=4.0U W=8.0U
MQ2 IOUT IREF D1 1 PMITEL L=4.0U W=8.0U
MQ3 D2   D2   VD 1 PMITEL L=4.0U W=8.0U
MQ4 IREF IREF D2 1 PMITEL L=4.0U W=8.0U
VDD 1 0 DC 5.0V
.ENDS CAS
*
**** Single-Pole Double-Throw switch *********
*
.SUBCKT SPDT DA DB SRA OUTA OUTB
*
*   D   G   S  B
MXPA OUTA SRA DA 1 PMITEL L=2.0U W=8.0U
MXNA OUTA SRA 0  0 NMITEL L=3.5U W=3.5U
MXPB OUTB SRA DB 1 PMITEL L=2.0U W=8.0U
MXNB OUTB SRA 0  0 NMITEL L=3.5U W=3.5U
VDD 1 0 DC 5.0V
.ENDS SPDT
*
**** Circuit Description **********************************
*
XCAS 1 DA1 DB1 CAS
VIDA DA1 DA
VIDB DB1 DB
*
XSPDT0 DA DB 0 OUTA0 OUTB0 SPDT
XSPDT1 DA DB 1 OUTA1 OUTB1 SPDT
*
MSC0A OUTA0 G OUTA1 0 NMITEL L=54.0U W=27.0U
```

```
MSC0B OUTB0 G OUTB1 0 NMITEL L=54.0U W=27.0U
*
**** Voltages ****************************************
*
VDD 1 0 DC 5.0V
VG  G 0 DC
*
**** Analysis Parameters *********************************
*
.OPTIONS LIMPTS=4000 POST OPTS LIST NODE BRIEF=1 ACCT $PROBE=1
.DC VG 0.0 3.0 0.01
.PRINT DC I(VIDA) V(DB,DA) V(OUTA0) V(OUTB0) V(DA,OUTA0)
.WIDTH IN=100 OUT=100
.END
```

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