High Frequency Noise Modeling of MOSFETs

by

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Abstract

The down-scaling of MOSFETs to deep-submicron dimensions and the resulting very high unity-gain frequencies of tens of GigaHertz make MOSFETs increasingly attractive for applications in integrated high-frequency analog electronics, wireless communications and high-speed digital applications. Therefore, to accurately design low noise h.f. MOSFET or FET-based devices and circuits, their high-frequency characterization and modeling are urgently needed. However, when working at high frequencies, the effect of the noise generated within the device itself will play an increasingly important role in the overall system sensitivity characteristics, dynamic range and signal-to-noise ratio. Thus, it is crucial that we understand the noise mechanisms in sub-micron MOSFETs, and develop appropriate physically-based noise models that can accurately predict the noise performance of transistors over a wide range of operating conditions. To date, one set of existing noise models that include physical noise mechanisms are based on simplified small-signal models which cannot accurately predict the AC (small-signal) performance of transistors. The other set of models are based on very accurate AC models, but they neglect an very important high frequency noise source - the gate resistance thermal noise, their models for the channel thermal noise are very simplistic since velocity saturation and hot-electron effects are neglected, and they do not predict accurately the h.f. noise performance of MOSFETs.

Because of these limitations, we have developed a new model which can predict accurately both AC and the noise performance (all four noise parameters - minimum noise figure NF_{min}, equivalent noise resistance R_n, and optimized source resistance R_{opt} and reactance X_{opt}) of transistors based on s-parameters and noise measurements at microwave frequencies. The model has the following features - it includes all the high frequency noise

sources (including several models for the channel thermal noise and their correlations, and the thermal noise from the channel resistance and gate resistance); it is based on a direct calculation technique for describing the four noise parameters which is suitable for circuit simulators; and it includes a de-embedding procedure for both noise and s-parameters using special test structures. Additionally, it is the first description of a self-consistent small-signal model for MOSFETs that predicts accurately both their AC as well as their noise performance over a range of frequencies and biasing currents. Finally, the impact of gate resistance, the induced gate noise, and the noise improvement using multi-finger gates are investigated both experimentally and theoretically.

Acknowledgments

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Chapter 1

Introduction

1.1 Introduction

Noise is some unwanted fluctuation that, when added to a signal, reduces its information content. In a communication system, noise can be classified into two broad categories depending on its source. Noise generated by components within a communication system, such as resistors, electron tubes, and solid-state active devices is referred to as *internal noise* (or *electronic noise*). The second category, *external noise*, results from sources outside a communication system, including atmospheric, man-made, and extraterrestrial sources. The "statics" heard in a radio, the "snowy screen" of a television, and the fluctuation of a DC signal around its expected value are all examples of electronic noises, and this is the kind of noise of interest to us in this research.

Electronic noise in a communication system defines the lowest limit of a signal that can be detected. Below this limit, the signal would be "drowned out" by the background noise. Therefore, electronic noise directly affects the accuracy of measurements and the minimum power of a signal that can be used in a circuit to transmit information.

Since noise is random in nature, it is represented as a time varying random variable X(t) in noise theory. The mean value, $\overline{X}$, of X(t) and the variance, $\overline{\Delta X^2}$, of X(t) about its mean, are two important parameters for characterizing the random variable X(t). Another important characteristic of a random signal is its power spectral density function (PSDF). The power spectral density function of a signal describes how a signal distributes its power at different frequencies. From definition, PSDF represents the time averaged noise

power over a one Hertz bandwidth at any given frequency f. White noise is a particular kind of noise which has a PSDF that is constant for all frequencies. Thermal noise generated from a resistor and the shot noise generated in a circuit are examples of white noise.

Noise always exists in electronic signals. A DC current I(t) or voltage V(t) is actually the summation of an ideal DC component and a fluctuating AC component. The PSDFs of a DC current I(t) and voltage V(t) are represented by $S_I(f)$ and $S_V(f)$ and abbreviated as their "noise power spectra". These noise spectra describe how their noise powers distribute at different frequencies. The noise voltage generator $V_n(f) = \sqrt{S_V(f)}$ and noise current generator $I_n(f) = \sqrt{S_I(f)}$ are defined such that the total noise power of a circuit can be evaluated by applying AC circuit theory to these quantities.

1.2 Some Attractive Features of Modern MOSFETs

MOS technology is the dominant IC technology for high-density low cost VLSI circuits. The main driving force of submicrometer MOS technology is digital VLSI. However, as speed and circuit complexity increase, it is often desirable to incorporate high-frequency analog circuits on the same chip. Radio frequency designs are increasingly taking advantages of MOS technology advances that makes possible the integration of complete communication systems. As an example, global positioning system (GSP) receivers employ extensive digital signal processing to perform acquisition, tracking, and decoding functions. The use of MOS technology for implementation of the front end electronics in a GPS system is therefore attractive because of the promise of integrating the whole system on a single chip. Therefore, high-frequency characterization and modeling of MOSFETs are becoming more important with the growth in high-frequency analog applications.

1.3 Noise Modeling of Modern MOSFETs

When working at high frequencies, the effect of the noise generated within the device itself will play an increasingly important role in the overall system sensitivity characteristics, dynamic range and signal-to-noise ratio. Therefore it is crucial that we understand the noise mechanisms in sub-micron MOSFETs. Due to the long turn around time and the expensive cost of actual fabrication of an analog circuit, noise simulation of a analog circuit becomes a realistic alternative to determine whether the overall noise performance of a circuit would be good enough to allow the circuit to function properly. In order to perform accurate noise simulation, an appropriate physically-based noise model that can predict accurately the noise performance of transistors over a wide range of operating conditions of frequencies, currents and device geometries is urgently needed. To date, some of the noise models including physical noise mechanisms are based on simplified small-signal models which cannot accurately predict the AC performance of transistors. Others based on very accurate AC models neglect the important high frequency noise source - the gate resistance thermal noise, and the impacts of velocity saturation and hot-electron effects on the thermal noise in the channel, and so they cannot be used for high frequency noise prediction.

1.4 Goal of This Research

The goal of this research is to develop a new model which can predict not only the AC, but also the noise performance of transistors. In this thesis, a new noise model which includes all the high-frequency noise sources and their correlations is developed. Some test structures for the confirmation of the model are designed and different de-embedding procedures for obtaining the noise and s-parameters of intrinsic transistors are discussed. A direct calculation method allows us easily to calculate the four noise parameters of

transistors and to determine the impact of individual noise sources based on the sophisticated small-signal model. In addition, the variation of noise parameters with bias conditions and frequencies, which are important for the low noise RF analog circuit design, are presented. Finally, the impact of gate resistance and the induced gate noise, and the model for multi-finger gate designs are discussed.

Chapter 2

Review of High-Frequency MOSFET Characteristics

2.1 Gain of MOSFETs

The gain of a two-port network (as shown in figure 2.1) is defined as the signal which could be a short-circuit current, a open-circuit voltage, or the power delivered to a load at the output port (port 2) divided by the signal at the input port (port 1). Two kinds of gains that are commonly used to describe the transistor performance are short-circuit current gain and available power gain.

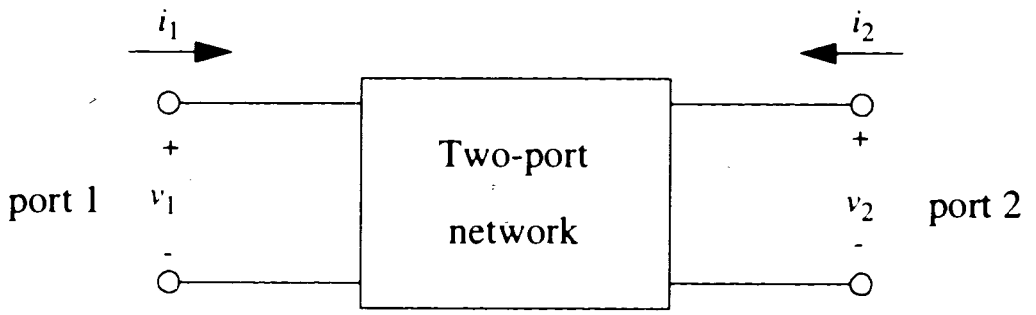


FIGURE 2.1: Two-port network representation.

The short-circuit current gain of a two-port network is defined as the short-circuit current (i_2) obtained at the port 2 divided the current (i_1) flowing into the port 1, i.e.

$$Current\ Gain = \left.\frac{i_2}{i_1}\right|_{v_2 = 0} . \tag{2.1}$$

If we describe the two-port network in terms of its h-parameter representation, then we have that

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ v_2 \end{bmatrix} \tag{2.2}$$

and it is found that the short-circuit current gain is h_{21}.

On the other hand, the power transfer characteristics of a two-port network is required when we are designing amplifiers or filters. The power which can be delivered to the output port depends on the transfer characteristics of the two-port, as well as the impedance characteristics of the source and load at the input and output ports respectively. Figure 2.2 shows the general diagram of a two-port network with source and load impedances, and where Z_o is the system impedance. The need for matching networks arises because amplifiers, in order to deliver maximum power to a load, or to perform in a certain desired way, must be properly terminated at both the input and output ports.

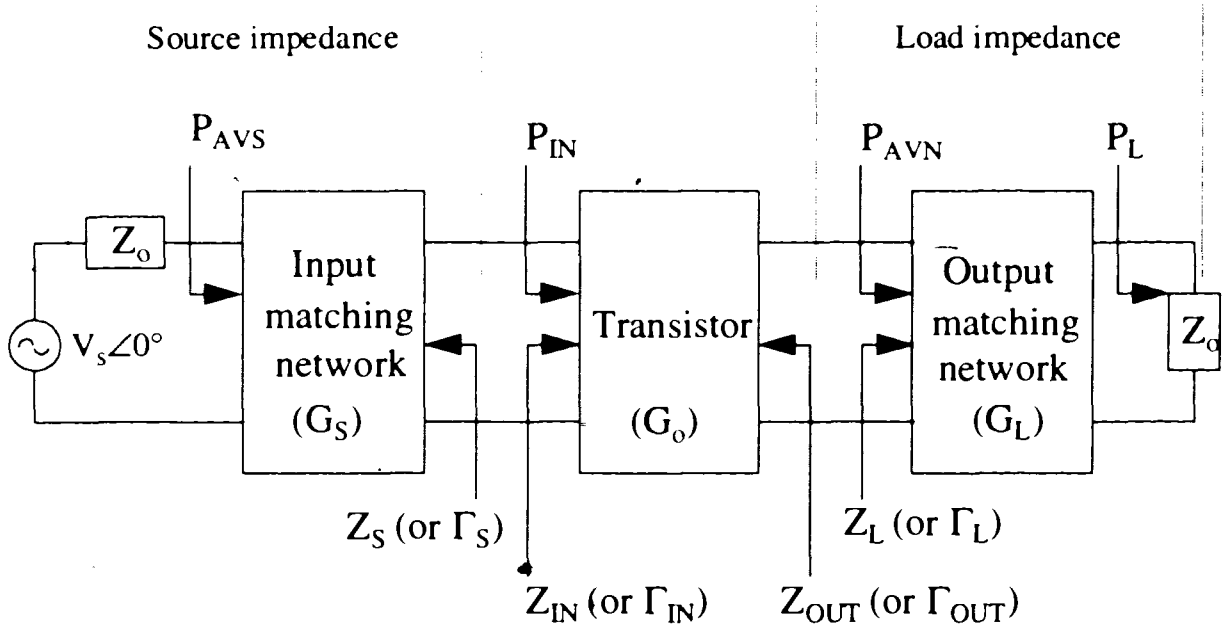


FIGURE 2.2: Block diagram of a two-port network with general source and load impedances.

Power gain equations which appear in the literature [1], and are used in the design of microwave amplifiers, are the transducer power gain G_T, the power gain G_P (also called operating power gain), and the available power gain G_A, and they are defined as

$$G_T = \frac{P_L}{P_{AVS}} = \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source}, \tag{2.3}$$

$$G_P = \frac{P_L}{P_{IN}} = \frac{power\ delivered\ to\ the\ load}{power\ input\ to\ the\ network}, \tag{2.4}$$

and

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{power\ available\ from\ the\ network}{power\ available\ from\ the\ source}. \tag{2.5}$$

From the definitions of power gains, we can represent the power gains in terms of the s-parameters of the two-port network and the impedance reflection coefficients of the matching networks by [1]

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad \text{or} \tag{2.6}$$

$$G_T = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|^2}, \tag{2.7}$$

$$G_P = \frac{1}{1-|\Gamma_{IN}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}, \tag{2.8}$$

and

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{OUT}|^2} \tag{2.9}$$

where

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}, \text{ and} \tag{2.10}$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.11}$$

There are two figures of merit that commonly used by manufacturers of microwave transistors to describe the transistor performance. They are

1. f_T: the unity gain frequency (or the gain-bandwidth frequency, cutoff frequency). It is the extrapolated value of the frequency where the short-circuit current gain $|h_{21}(\omega)|$ is unity.

2. f_{max}: the maximum oscillation frequency. It is the frequency where the maximum available power gain $G_{P,max}$ (MAG) is equal to one.

After the s-parameters of an intrinsic transistor are obtained, we convert the s-parameters to their h-parameter representation and plot the magnitude of h_{21} as a function of frequency, as shown in figure 2.3.

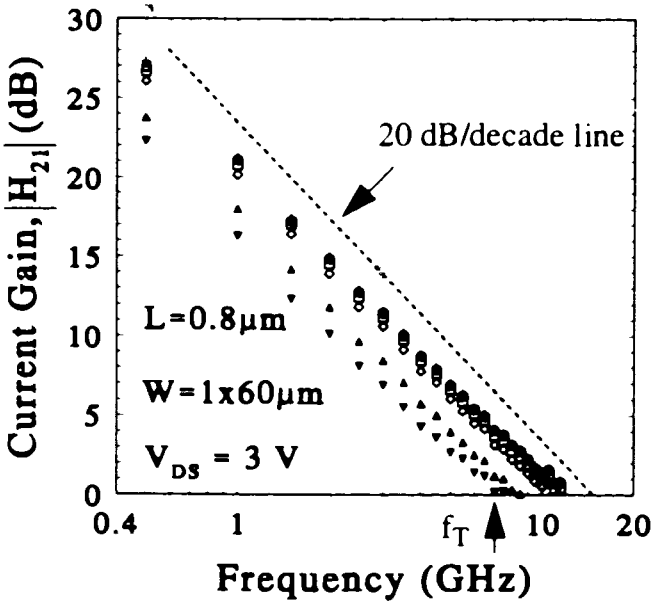


FIGURE 2.3: The magnitude of the measured current gain (H_{21}) of a 0.8 μm nMOSFET as a function of frequency biased at I_{DS} = 1 mA, 3 mA, 5 mA, 7 mA, and 9 mA.

From the extrapolation with the x-axis, we can obtain the unity gain frequency at the specific bias condition. From figure 2.3, it is observed that the magnitude of h_{21} decreases with increasing frequency at the rate of ~ 20 dB/decade.

The maximum power output from a stable amplifier occurs when the amplifier is conjugately matched at both the input and output ports with $\Gamma_S = \Gamma_{IN}^*$ and $\Gamma_L = \Gamma_{OUT}^*$. This gain is sometimes called the maximum available gain (MAG). From (2.10) and (2.11), we see that to calculate Γ_{IN}, we must know Γ_L, and to calculate Γ_{OUT}, we have to know Γ_S. The reflection coefficients that simultaneously satisfy the pair of equations are referred to as Γ_{MS} and Γ_{ML} and are given by

$$\Gamma_{MS} = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}, \qquad \Gamma_{ML} = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{2.12}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2, \qquad C_1 = S_{11} - \Delta S_{22}^* \tag{2.13}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2, \qquad C_2 = S_{22} - \Delta S_{11}^* \tag{2.14}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{2.15}$$

When a transistor is bilaterally matched, the MAG of the transistor can be calculated from

$$G_{P,max} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right), \text{ and } K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.16}$$

and $G_{P,max} = G_A = G_T$. Of course, (2.16) applies only to the transistor that is unconditionally stable, i.e., having no oscillations. Based on (2.16), figure 2.4 shows the

measured MAG of an intrinsic 0.8 μm nMOSFET as a function of frequency for five different I_{DS}'s. From the extrapolation of MAG with the x-axis, we can obtain the maximum oscillation frequency (f_{max}) at each bias condition.

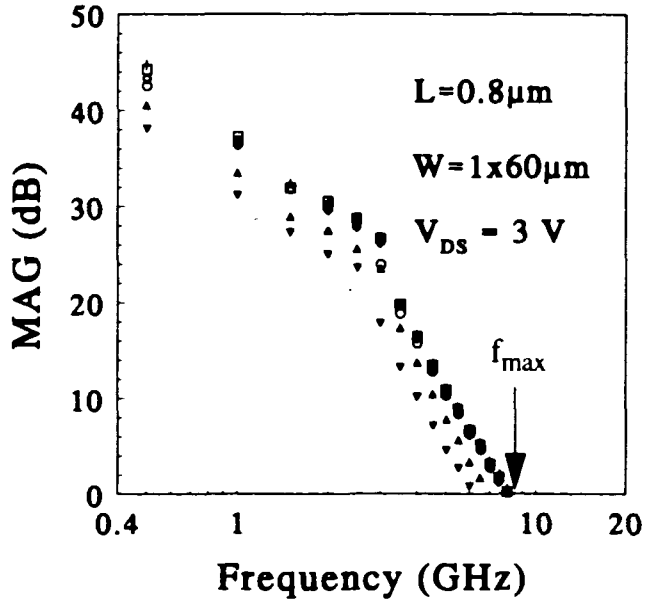


FIGURE 2.4: The maximum available gain (MAG) of a 0.8μm nMOSFET as a function of frequency for bias current I_{DS} = 1mA, 3mA, 5mA, 7mA, and 9mA.

After the f_T and f_{max} are calculated from the measured s-parameters of an intrinsic transistor for each bias current, we can plot the f_T and f_{max} of the intrinsic transistor as a function of bias current. Figure 2.5 shows the measured (symbols) and simulated (dash line) f_T and measured f_{max} vs. I_{DS} characteristics of a 0.8 μm nMOSFET of 60 μm channel width. The f_T of the transistor (dash line in figure 2.5) is obtained using

$$f_T = \frac{g_m}{2\pi (C_{GS} + C_{GD} + C_{GB})}, \tag{2.17}$$

where g_m is the transconductance, C_{GS}, C_{GD}, and C_{GB} are the gate-to-source, gate-to-drain, and gate-to-substrate capacitances, respectively, of the MOSFET.

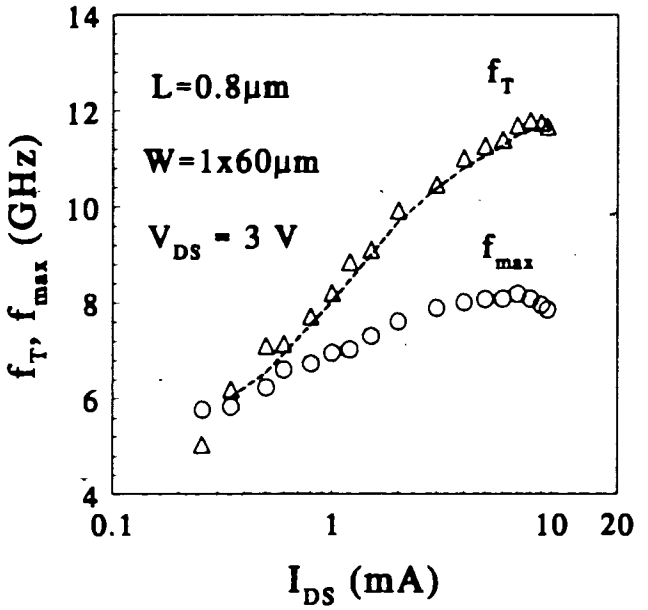


FIGURE 2.5: The unity gain frequency (f_T) and maximum oscillation frequency (f_{max}) of a 0.8μm n-type MOSFET as a function of bias conditions.

2.2 High-Frequency Performance of MOSFETs

There has recently been remarkable progress in improving the high-frequency characteristics of small geometry silicon MOSFETs for analog applications. By downsizing the gate length to the 0.1μm regime, excellent f_T values as high as 118 GHz [2] have been realized. There are expectations that, in the near future, silicon MOSFETs will come into wider use in RF telecommunication integrated circuits. As for the test structure used in high-frequency characterization, multi-finger gate design is usually employed for reducing the gate resistance and the signal delay along the wide channel width. Figure 2.6 shows the typical layout of a nMOSFET test structure [3]. For a fixed

channel length [4], this kind of test structure will significantly improve f_{max}, but it does not change f_T too much.

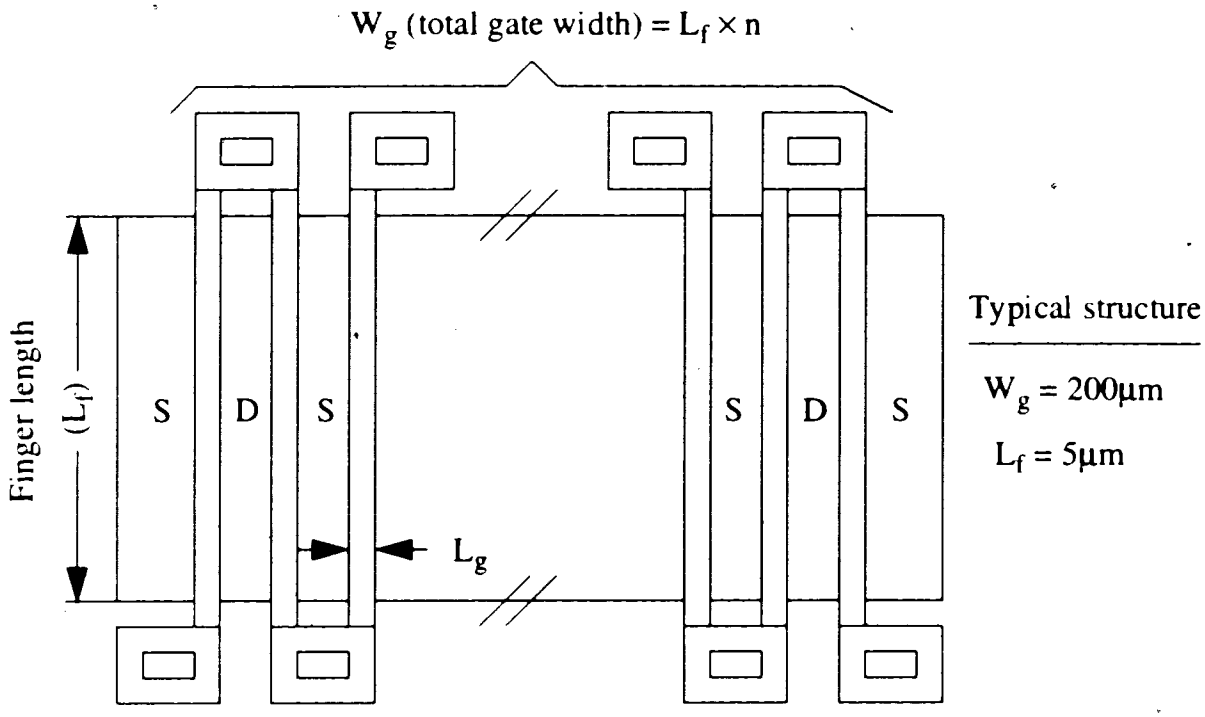


FIGURE 2.6: MOSFET test structure for h.f. measurements from [3].

- **Downscaling effects on the high-frequency performance of MOSFETs**

What we are now interested in is how the downscaling of MOSFET dimensions affects the g_m and f_T for modern MOS technology. Based on the advanced 1.5 nm gate oxide CMOS technology described in [3], figure 2.7 shows the dependence of transconductance on gate length. It is shown that as the gate length is reduced, g_m values increase in inverse proportion to L_g ($g_m \propto 1/L_g$). However, this relation tends to saturate when the gate length approaches 0.1 μm. Figure 2.8 shows the dependence of f_T on gate length. In the longer gate-length region, it is known that f_T values increase in inverse proportion to the square of gate length ($f_T \propto 1/L_g^2$) as the gate length is reduced. In this

figure, it is confirmed that f_T values continue to increase in the same manner down to gate lengths near 0.1 μm, and then saturate.

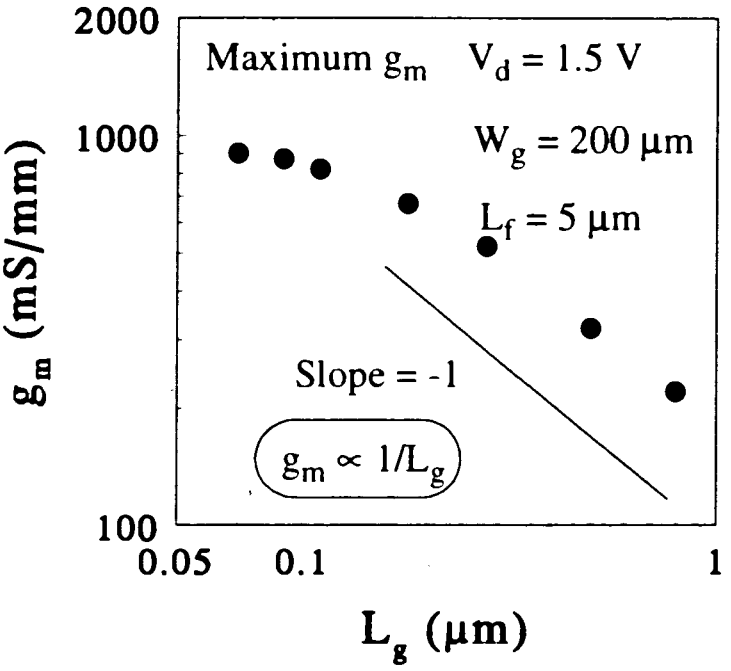


FIGURE 2.7: Dependence of transconductance on gate length from [3].

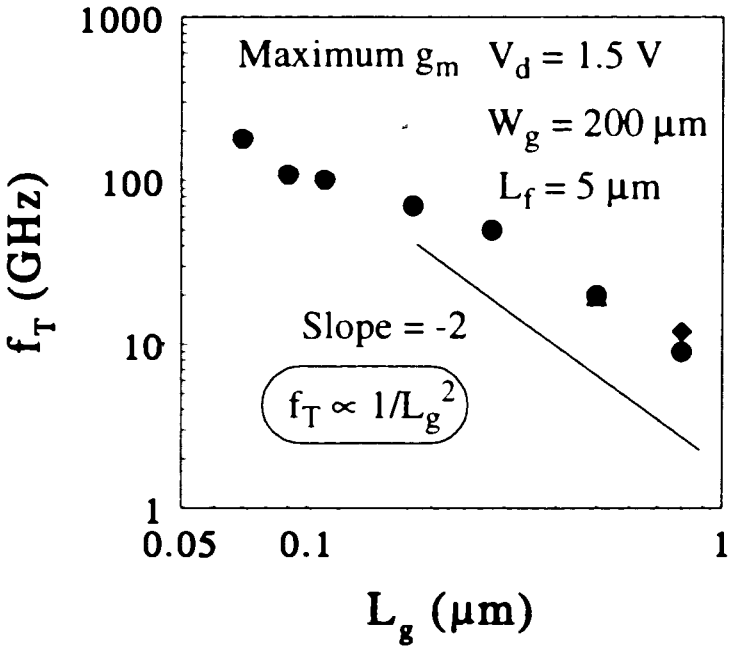


FIGURE 2.8: Dependence of cutoff frequency on gate length from [3] (circle), the f_T (triangle) from [4] (0.5 μm CMOS technology) and the f_T (diamond) of the device measured in this research (0.8 μm BiCMOS technology).

Figure 2.9 shows the relation between f_T and g_m values. It is observed that the cutoff frequency is proportional to the square of transconductance, i.e. $f_T \propto g_m^2$. Corresponding to the extremely high g_m values, extremely high f_T values of more than 150 GHz were obtained with gate length below 0.09 μm.

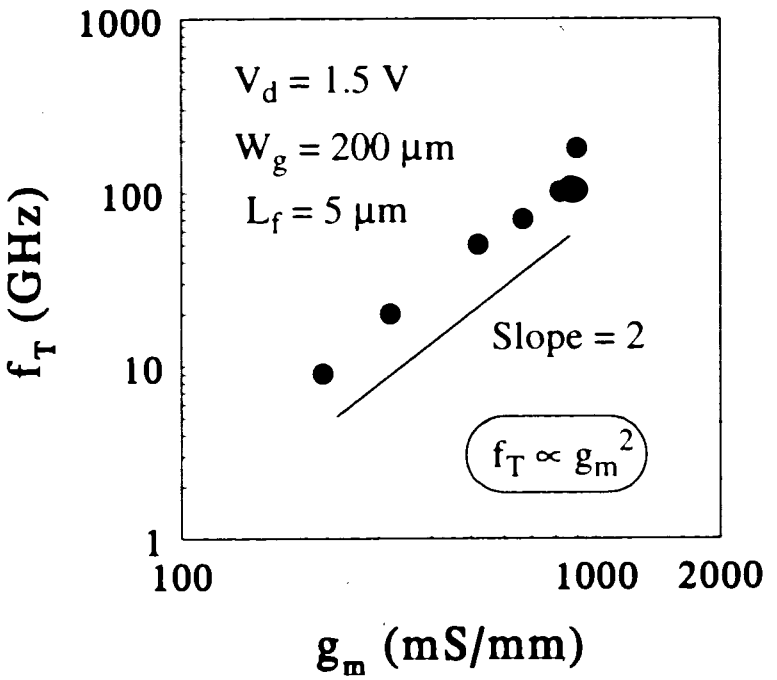


FIGURE 2.9: Dependence of cutoff frequency on transconductance from [3] (g_m here is the maximum value corresponding to each channel length).

- **Effect of multi-finger gate design on the high-frequency performance of modern MOSFETs**

Multi-finger gate design in which there are several intrinsic transistors connected in parallel will reduce the gate resistance and increase f_{max}. For the test structure of multi-finger gates presented in [4], four gate fingers are connected and this results in a 16-fold gate resistance (R_G) reduction, leading to a 2-fold increase in f_{max} without f_T degradation.

Further reduction of the gate resistance, either by decreasing the sheet resistance or by parallel gate fingers does not significantly impact f_T for this feature size. Figure 2.10 shows the measured f_T and f_{max} for single finger and multi-finger gate design presented in [4]. It is shown that multi-finger gate design improves f_{max} dramatically while f_T is not affected too much.

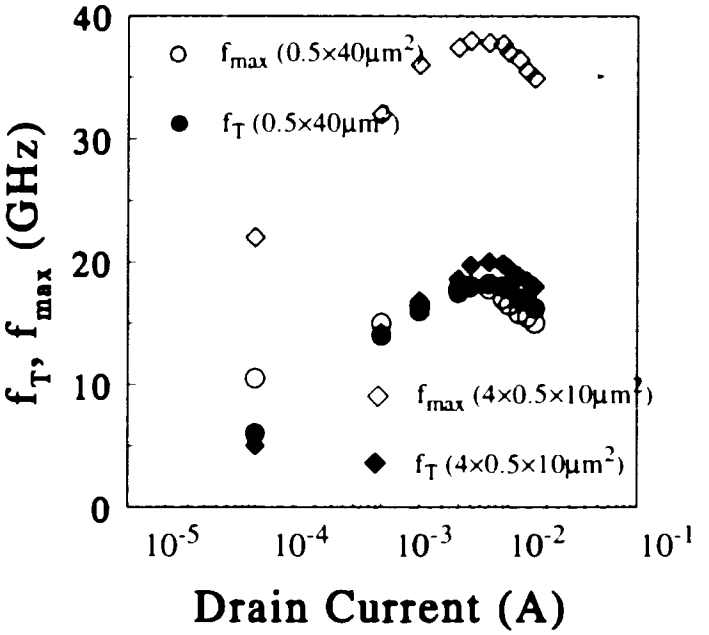


FIGURE 2.10: Layout dependence of f_T and f_{max} for nMOSFETs from [4].

- **Noise performance of modern MOSFETs**

Figure 2.11 shows the NF_{min} and R_n vs. frequency of a 0.5 μm nMOSFET in [4]. The lowest NF_{min} of 1.9 dB at 3.4 GHz for a 0.5 μm n-MOSFET was obtained [4]. Figure 2.12 shows the measured $|\Gamma_{opt}|$ vs. frequency characteristics. In general, $|\Gamma_{opt}|$ decreases when frequency increases [4].

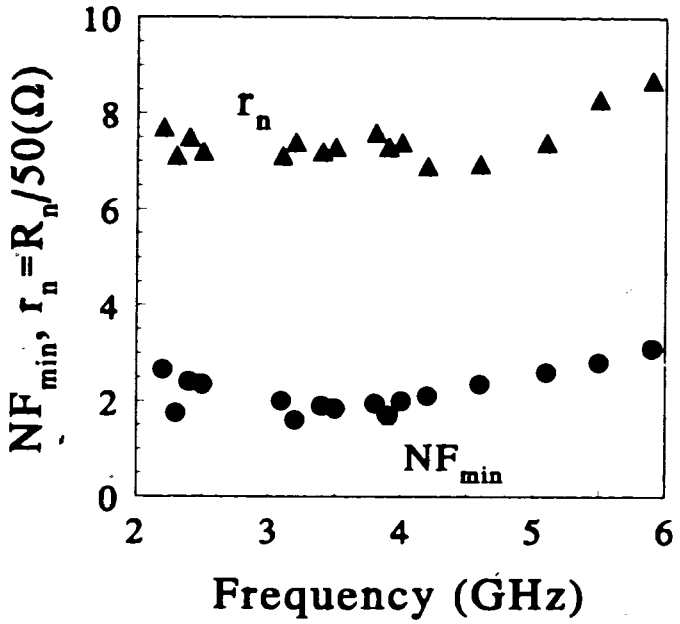


FIGURE 2.11: Noise measurement results for a 0.5 μm nMOSFET (W = 4×10 μm) biased at I_{DS} = 1.97 mA with V_{DS} = 2.5 V reported in [4].

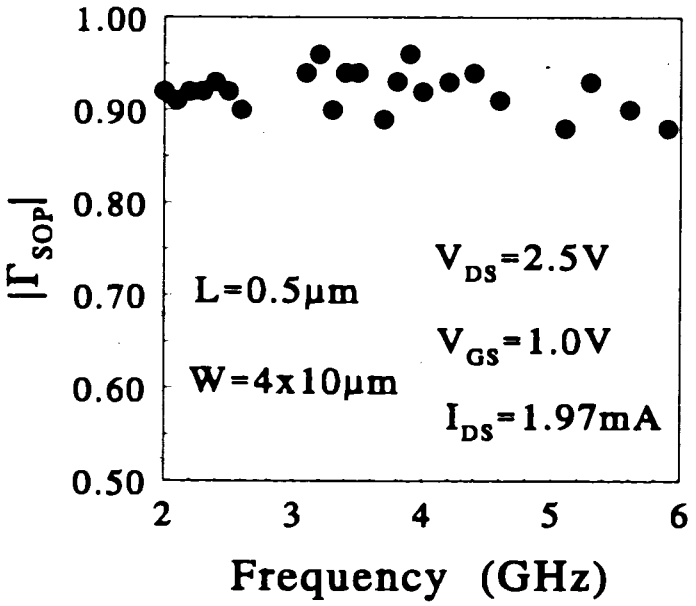


FIGURE 2.12: $|\Gamma_{opt}|$ for a 0.5 μm nMOSFET (W = 4×10 μm) biased at I_{DS} = 1.97 mA with V_{DS} = 2.5 V reported in [4].

Chapter 3

Theoretical Background

3.1 Noise in Semiconductor Devices

The noise discussed in this thesis is the electronic noise which is caused by the small voltage (or current) fluctuations generated within the devices themselves. The most important sources of noise in devices are thermal noise, shot noise, generation-recombination noise, and flicker noise.

- **Thermal noise (also called Nyquist noise or Johnson noise)**

Thermal noise is caused by collisions of the carriers with the lattice due to the thermal motion of the carriers (electrons). In general, the power spectral density of the short-circuit current fluctuation $S_{I,T}$, in A^2/Hz, is a white noise and it can be expressed by [5]

$$S_{I,T} = 4 \cdot \left[\frac{1}{2}hf + \frac{hf}{\exp(hf/kT) - 1}\right] / R \qquad (3.1)$$

where h is Planck's constant, k is Boltzmann's constant, f is the operating frequency, and R is the resistance of the sample. For $hf/kT << 1$, $S_{I,T}$ can be reduced to the widely used expression

$$S_{I,T} = 4kT/R \qquad (3.2)$$

- **Shot noise**

Shot noise is generated when carriers (electrons) cross barriers independently and at random. It is present in diodes and bipolar transistors. The external current I, which appears to be a steady current, is in fact composed of a large number of random independent current pulses. The physical origin of the shot noise is the fluctuation of the emission rate of carriers. For operating frequency lower than the reciprocal of the transit time, the short-circuit power spectral density (A^2/Hz) of the shot noise $S_{I,S}$ is white and is expressed by [5]

$$S_{I,S} = 2qI \tag{3.3}$$

where q is the electronic charge (1.6×10^{-19}C) and I is the current through the sample.

- **Generation-recombination Noise**

The generation-recombination noise (g-r noise for short) is caused by the fluctuation of conductance. Because of the traps and recombination centers in semiconductors, the random trapping and detrapping of carriers results in the fluctuation in the number of free carriers per unit time N, causing the conductance of the device to fluctuate. The power spectral density of g-r noise is given by [5]

$$S_N(f) = \langle \Delta N^2 \rangle \cdot \frac{4\tau}{1 + (2\pi f\tau)^2} \tag{3.4}$$

where $<\Delta N^2>$ is the variance of N, f is the frequency, and the τ is the lifetime of the carriers.

- **Flicker Noise (1/f Noise)**

Flicker noise was discovered in vacuum tubes by Johnson in 1925 and interpreted by Schottky in 1926. Christensen and Pearson were the first to measure flicker noise in carbon microphones and carbon contacts. Because the spectrum varies as $1/f^{\alpha}$, with α close to unity, flicker noise is often called 1/f noise. The origin of 1/f noise is still actively researched and in general two major models have been proposed to account for the origin of flicker noise - the carrier number fluctuation model [6] and the mobility fluctuation model [7]. In the first model, the flicker noise is attributed to the random trapping and de-trapping processes of charges in the oxide traps near Si-SiO_2 interface. The charge fluctuations result in fluctuations of the surface potential, which in turn modulate the channel mobile carrier density. It is assumed that the channel can exchange charges with the interfacial oxide traps though tunneling. However, the second model considers the flicker noise to result from the bulk mobility fluctuation on the basis of an empirical hypothesis. In general, its short-circuit power spectral density is given by the empirical expression [5]

$$S_I(f) = K \frac{I^m}{f^n} \tag{3.5}$$

where K is a constant for a particular device, I is the conduction current, m is a constant in the range of 0.5 to 2 depending on the operating condition and device details, and n is a constant close to unity.

3.2 High Frequency Noise Sources in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

Working in the microwave region, generation-recombination noise and flicker noise are so small that they are negligible at high frequencies. Therefore, only the thermal noise is considered in high frequency noise modeling. In MOSFETs, the total transistor noise has the following components - channel noise (i_d), noise due to the gate resistance (i_G), gate leakage noise (i_g) and its correlation with i_d ($i_g^* i_d$), thermal noise in the source (i_S) and drain (i_D) parasitic resistances.

3.2.1 Thermal Noise in the Conducting Channel

The general expression for the drain current of a MOSFET operated in strong inversion is

$$I_D(x) = W_{eff} \cdot Q_I(x) \cdot v(x) \tag{3.6}$$

where x is the position along the channel, W_{eff} is the effective channel width, $Q_I(x)$ is the inversion layer charge per unit area, and $v(x)$ is the carrier drift velocity in the channel as shown in figure 3.1.

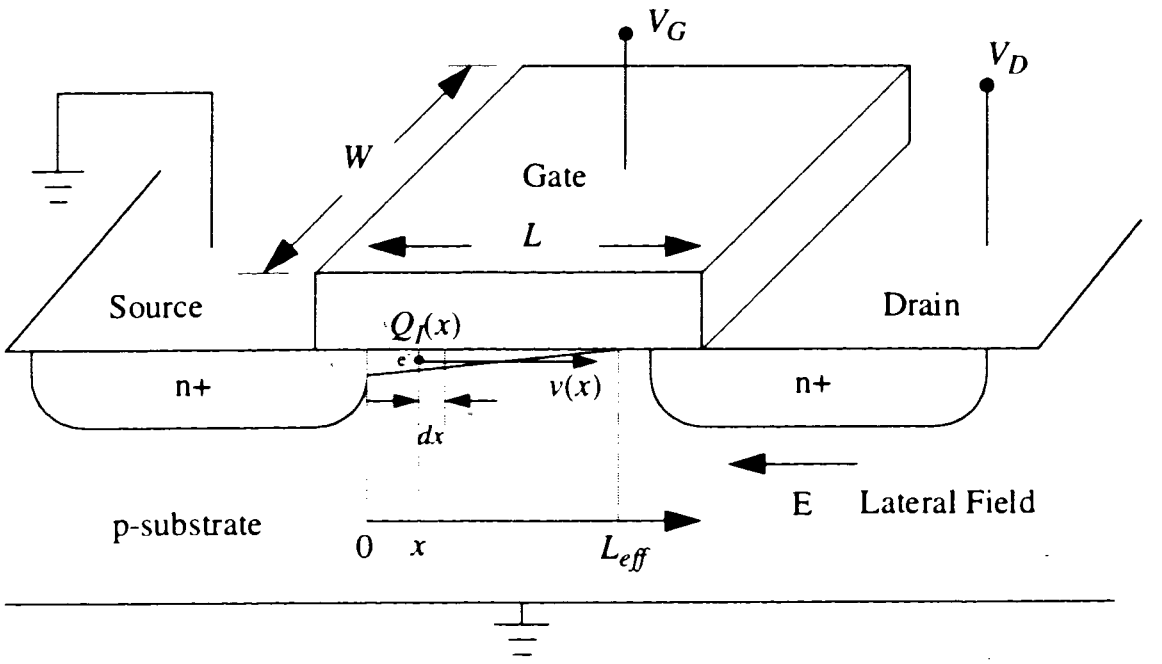


FIGURE 3.1: Schematic diagram of a n-type MOSFET operated in saturation region.

For short channel devices, the carrier drift velocity in the channel will saturate at the high lateral electric field [8], and it can be expressed as

$$v(x) = \begin{cases} \dfrac{\mu_{seff} \cdot E(x)}{1 + \dfrac{E(x)}{E_c}} & E(x) < E_C \\ v_{sat} & E(x) \geq E_C \end{cases} \tag{3.7}$$

where μ_{seff} is the effective surface mobility, $E(x) = dV(x)/dx$ is the lateral electric field, v_{sat} is the saturation velocity, and E_C is the critical field at which carrier velocity saturation occurs. The critical field and the effective surface mobility are given by

$$E_C = \frac{2v_{sat}}{\mu_{seff}} \; ; \qquad \mu_{seff} = \frac{\mu_o}{1 + \theta\,(V_{GS,int} - V_{T0})} \tag{3.8}$$

where μ_o is the low-field mobility, θ is the mobility degradation coefficient due to vertical channel field, V_{T0} is the threshold voltage at the source end of the channel with zero source-substrate bias [11][12][13], and $V_{GS,int}$ is the voltage drop between the gate and source of a intrinsic device (i.e. $V_{GS,int} = V_{GS} - I_D \cdot R_S$), as shown in figure 3.2.

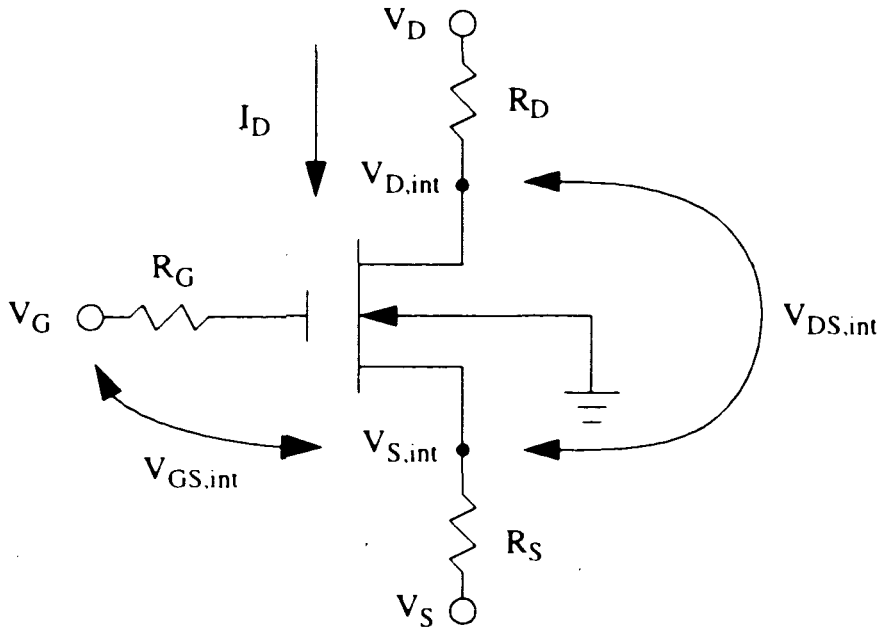


FIGURE 3.2: A n-channel MOSFET with drain (R_D) and source (R_S) series resistances. The terminal voltages (V_G, V_D, and V_S) and the voltages applied to the intrinsic transistor ($V_{D,int}$ and $V_{S,int}$) are indicated.

The saturation velocity, v_{sat}, of the carriers in the channel is approximately 10^7 cm/s for temperature of 300K [9][10].

Substituting (3.7) into (3.6) for $E(x) < E_C$ and rearranging the equation, we can get the drain current I_D is

$$I_D(x) = \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(x) - \frac{I_D(x)}{E_C} \right) \cdot \frac{dV}{dx} \cdot \tag{3.9}$$

where V is the voltage along the channel. Multiplying by dx, integrating over the effective channel length L_{eff} while keeping $I_D(x)$ constant for all positions (because I_D is independent of the position in the channel), and finally solving for I_D gives

$$I_D = \frac{1}{L_{eff}} \int_{V_{S,int}}^{V_{D,int}} \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right) dV \tag{3.10}$$

where $V_{D,int}$ is the channel potential at the drain end of the intrinsic device (i.e. $V_{D,int} = V_D - I_D \cdot R_D$ in linear region and $V_{D,int} = V_D - I_{D,sat} \cdot R_D = V_{D,sat}$, where $V_{D,sat}$ is the saturation voltage and $I_{D,sat}$ is the drain current at $V_D = V_{D,sat}$, in the saturation region), and $V_{S,int}$ is the channel voltage at the source end of intrinsic devices (i.e. $V_{S,int} = V_S + I_D \cdot R_S$). The values of L_{eff}, V_{Dsat} and $Q_I(V)$ depend on models used, and they are of different levels of complexity and will produces different accuracies.

From (3.10), we find that if there is a small time varying voltage fluctuation $\Delta v(t)$ caused by the thermal noise in a unit length segment of the channel, then the current fluctuation $\Delta i(t)$ caused by $\Delta v(t)$ is given by

$$\Delta i(t) = \frac{1}{L_{eff}} \cdot \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right) \cdot \Delta v(t) \tag{3.11}$$

as long as the variation of $\Delta v(t)$ is slow enough so that quasi-static behavior is maintained. Because of the negligibly small $\Delta v(t)$, $Q_I(V)$ is practically constant and independent of $\Delta v(t)$. The mean square value of $\Delta i(t)$ will then be

$$\overline{(\Delta i)^2} = \frac{1}{L_{eff}^2} \cdot \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^2 \cdot \overline{(\Delta v)^2}. \tag{3.12}$$

From (3.9), it can be shown that the resistance ΔR of a small element of the channel of length Δx centered around a point $x = x_1$ is

$$\Delta R = \frac{\Delta x}{\left(\mu_{seff} \cdot W_{eff} \cdot Q_I(x_1) - \frac{I_D(x_1)}{E_C} \right)}. \tag{3.13}$$

since $\Delta V = I_D \cdot \Delta R$. Using the concepts from statistical physics, the power spectral density of the noise voltage generated across a resistor of value R is equal to 4kTR for frequencies at which $hf/kT << 1$, and assuming that the small element of the channel acts as a resistor of resistance ΔR, we will find a small voltage $\Delta v(t)$ across it with a mean square value of

$$\overline{(\Delta v)^2} = \frac{4kT_e(x_1) \cdot \Delta x}{\left(\mu_{seff} \cdot W_{eff} \cdot Q_I(x_1) - \frac{I_D(x_1)}{E_C} \right)} \Delta f. \tag{3.14}$$

where $T_e(x_1)$ is the effective electron temperature at x_1. If the channel does not show hot electron effects, which is valid only for long channel devices, T_e would be the same as T which is the lattice temperature of the device.

Substituting (3.14) into (3.12),we obtain

$$\overline{(\Delta i)^2} = \frac{4kT_e(x_1)}{L_{eff}^2} \cdot \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right) \cdot \Delta f \cdot \Delta x. \tag{3.15}$$

This gives the contribution of the element at x_I to the drain current noise. The contributions of all similar elements in the channel are assumed uncorrelated, and one can thus find the mean square value of their combined effect by adding the individual mean square values. In this limit, letting Δx become a differential, integrating over the effective channel length, and changing the variable dx to dV based on (3.9), we obtain that the power spectral density of the thermal noise in a channel S_{I_d} is given by

$$S_{I_d} = \frac{4k}{L^2_{eff} \cdot I_D} \cdot \int_{V_{S,int}}^{V_{D,int}} T_e(x) \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^2 dV. \tag{3.16}$$

Eqn. (3.16) includes both velocity saturation effects and hot electron effects, and it is a general expression for the thermal noise in a channel. In general, the electron temperature T_e increases with increasing field strength. The exact dependence is not known, but to simplify the calculations, it is assumed that

$$\frac{T_e(x)}{T} = \left(1 + \frac{E(x)}{E_C} \right)^n \tag{3.17}$$

with $0 \le n \le 2$. Solving for E/E_C from (3.6), (3.7), and (3.9) and using $E(x) = dV(x)/dx$, yields

$$1 + \frac{E(x)}{E_C} = \frac{\mu_{seff} \cdot W_{eff} \cdot Q_I(V)}{\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C}} \tag{3.18}$$

so that

$$S_{I_d} = \frac{\overline{i_d^2}}{\Delta f} = \frac{4kT}{L^2_{eff} \cdot I_D} \cdot \int_{V_{S,int}}^{V_{D,int}} \left[\mu_{seff} \cdot W_{eff} \cdot Q_I(V) \right]^n \times \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^{2-n} dV. \tag{3.19}$$

Eqn. (3.19) is valid for the bias conditions at which the lateral electrical field at any position in the conducting channel is smaller than E_C (i.e. the channel pinches off before carriers reach the saturation velocity).

3.2.2 Induced Gate Noise in MOSFETs

At high frequencies, the MOSFET must be considered as an RC distributed network, with the capacitive coupling to the gate representing the distributed capacitance and the channel itself representing the distributed resistance. This means that the high-frequency gate admittance Y_{gs} of the device contains a conductive component. To obtain the capacitive and conductive components, we start from the wave equation of the distributed line representing a MOSFET with a low conductivity substrate [17] given by

$$\frac{d}{dx}[\Delta I_D(x)] = j\omega W_{eff} C_{ox} \Delta v(x) \tag{3.20}$$

where $\Delta v(x)$ is the AC voltage fluctuation along the channel caused by the small variation in gate voltage V_{GS}. Geurst [18] has solved this equation and expanded Y_{gs} in terms of $j\omega$ to get

$$Y_{gs} = g_{mo} \cdot \frac{\frac{2}{3}j\hat{\omega} + \frac{4}{45}(j\hat{\omega})^2 + \frac{2}{405}(j\hat{\omega})^3 + \frac{2}{13365}(j\hat{\omega})^4 + \ldots}{1 + \frac{4}{15}j\hat{\omega} + \frac{1}{45}(j\hat{\omega})^2 + \frac{4}{4455}(j\hat{\omega})^3 + \ldots} \tag{3.21}$$

where

$$g_{mo} = \frac{\mu_{seff} C_{ox} W_{eff}}{L_{eff}} (V_{GS,int} - V_{T0}), \text{ and} \tag{3.22}$$

$$\hat{\omega} = \omega \cdot \frac{L_{eff}^2}{\mu_{seff}(V_{GS,int} - V_{T0})}. \tag{3.23}$$

If we take the first order approximation of (3.21), and model Y_{gs} by a capacitance C_{gs} in series with a resistance R_i, we may write, at saturation, that

$$Y_{gs} = g_{mo} \cdot \left[\frac{2}{3} j\hat{\omega} + \frac{4}{45} \hat{\omega}^2 \right] = \frac{1}{\frac{1}{j\omega C_{gs}} + R_i}. \tag{3.24}$$

For frequency at which $\omega^2 R^2 C^2 << 1$, we may solve for C_{gs} and R_i to get

$$C_{gs} = \frac{2}{3} g_{mo} \frac{\hat{\omega}}{\omega} = \frac{2}{3} C_{ox} W_{eff} L_{eff} \; ; \qquad R_i = \frac{g_{mo} \cdot \frac{4}{45} \hat{\omega}^2}{\omega^2 C_{gs}^2} = \frac{1}{5 g_{mo}}. \tag{3.25}$$

From (3.25), we find that the maximum value of C_{gs} at saturation is 2/3 of the total oxide capacitance and R_i will decrease with increasing $V_{GS,int}$ since g_{mo} is increasing with bias (3.22).

The resistance R_i may have noise associated with it. To evaluate the noise of R_i at higher frequencies, one must know $\overline{i_g i_g^*}$ and the cross-correlation $\overline{i_g i_d^*}$, if they exist. Let's take a section Δx_o at x_o in the channel. It has thermal noise Δv_{xo} and produces a fluctuating voltage $\Delta v(x)$ along the channel. By capacitive leakage to the gate, this produces a gate noise current. The total gate noise current Δi_g flowing out of the gate is found by integrating along the channel, and it is

$$\Delta i_g = j\omega W_{eff} \cdot \int_0^{L_{eff}} C_{ox} \Delta v(x)\, dx. \tag{3.26}$$

In addition, there is a drain noise current Δi_d due to Δv_{xo} flowing out of the drain, and this drain noise current has been discussed in section 3.2.1. Because the gate noise current and drain noise current resulting from the same noise source Δv_{xo}, Δi_g and Δi_d are

correlated. By expressing $\overline{i_g i_g^*}$ and $\overline{i_g i_d^*}$ in terms of Δv_{xo} and integrating over the channel length, one can obtain $\overline{i_g i_g^*}$ and $\overline{i_g i_d^*}$ for MOSFETs at saturation [5] as

$$S_{I_g} = \frac{\overline{i_g^2}}{\Delta f} = 4kT \cdot \frac{\omega^2 C_{ox}^2 W_{eff}^2}{I_D^3} \cdot \int_{V_{S,int}}^{V_{D,int}} \left[\mu_{seff} \cdot W_{eff} \cdot Q_I(V) \right]^n \times \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^{2-n} (V_{as} - V)^2 dV, \quad (3.27)$$

$$S_{I_{gd^*}} = \frac{\overline{i_g i_d^*}}{\Delta f} = 4kT \cdot \frac{j\omega C_{ox} W_{eff}}{I_D^2 L_{eff}} \cdot \int_{V_{S,int}}^{V_{D,int}} \left[\mu_{seff} \cdot W_{eff} \cdot Q_I(V) \right]^n \times \left(\mu_{seff} \cdot W_{eff} \cdot Q_I(V) - \frac{I_D}{E_C} \right)^{2-n} (V_{as} - V) dV, \quad (3.28)$$

where

$$V_{as} = V_{DS,int} + \frac{1}{2} \frac{V_{DS,int}^2}{E_C L_{eff}} - \frac{\frac{1}{2}(V_{GS,int} - V_T) V_{DS,int} - \frac{1}{6} V_{DS,int}^2}{V_{GS,int} - V_T - \frac{1}{2} V_{DS,int}} \left(1 + \frac{V_{DS,int}}{E_C L_{eff}} \right), \quad (3.29)$$

and

$$V_{DS,int} = V_{D,int} - V_{S,int}. \quad (3.30)$$

3.2.3 Thermal Noise from the parasitic resistances

For submicron MOSFETs, there are three major parasitic resistances present - source and drain resistances (R_S and R_D respectively) which play a more important role in degrading the current drive capability of devices [11][15], and gate resistance which has a strong impact on the maximum oscillation frequency (f_{max}), time response, and AC

performance of wide devices working at high frequencies [20]. These resistances, of course, will contribute thermal noise and their power spectral densities are

$$S_{I_{RS}} = 4kT/R_S \; ; \quad S_{I_{RD}} = 4kT/R_D \; ; \quad S_{I_{RG}} = 4kT/R_G \tag{3.31}$$

The resistance values of R_S, R_D, and R_G depend on models based on [13][19][20] and will give different results.

3.3 Review of Models for Current Noise in MOSFETs

There have been several thermal noise models established for MOSFETs in the literature [13][14][16][25][26]. In these models, two important physical effects were not considered - the velocity saturation effect and the hot-electron effect, and these effects are especially prominent in sub-micron transistors.

- **HSPICE Model**

The HSPICE MOSFET noise model has a parameter *NLEV* that is used to select different equations for the calculation of flicker noise and channel thermal noise. If the model parameter *NLEV* is less than 3, then the power spectral density of the channel thermal noise is given by

$$S_{I_d} = \frac{8kT \cdot g_m}{3} \tag{3.32}$$

where g_m is the transconductance and kT is the Boltzmann's thermal energy. The above formula is used in both saturation and linear regions, and it can lead to wrong results in the linear region. For example, at $V_{DS} = 0$, it predicts that S_{I_d} is zero because g_m becomes zero, whereas the power spectral density should be $4kTg_{do}$, where g_{do} is the drain

transconductance g_d at $V_d = 0$. In the analog circuits, such as transconductance-C filters [27] and MOSFET-C continuous-time filters [28], the transistors are operating in the linear region and (3.32) would fail to accurately describe the thermal noise.

If the model parameter *NLEV* is set to 3, HSPICE uses a different equation which is given by

$$S_{I_d} = \frac{8kT}{3} \cdot \beta \cdot (V_{GS,int} - V_{T0}) \cdot \frac{1 + a + a^2}{1 + a} \cdot GDSNIO \tag{3.33}$$

where

$$\beta = \frac{W_{eff}}{L_{eff}} u_{seff} C_{ox}, \tag{3.34}$$

$$a = \begin{cases} 1 - \dfrac{V_{DS,int}}{V_{Dsat} - I_{Dsat} \cdot (R_S + R_D)} & Linear\ region \\ 0 & Saturation\ region \end{cases} \tag{3.35}$$

and the model parameter *GDSNOI* is the channel thermal noise coefficient whose default value is one. This formula is derived assuming that the carrier mobility is constant and therefore the velocity saturation effect is not considered [13][14]. This model works reasonably well for long channel devices, but is not adequate for short channel devices.

- **BSIM3v3 Model**

BSIM3v3 model [29] is the HSPICE Level 49 MOS Model released by UC Berkeley on October 30, 1995 and proposed as a standard MOSFET model for industry use. There are two models for channel thermal noise. Each of these can be toggled by the model

parameter *NOIMOD*. If the value of *NOIMOD* is one, which is the default value, then the power spectral density of the channel thermal noise is modeled as

$$S_{I_d} = \frac{8kT \cdot (g_m + g_{ds})}{3}. \tag{3.36}$$

This model solved the problem at $V_{DS} = 0$ artificially, but it underestimates the noise power in the linear region. For example, at $V_{DS} = 0$, the power spectral density should be $4kTg_{do}$ but it only predicts two third of it. If the model parameter *NOIMOD* is set to two, the power spectral density is given by

$$S_{I_d} = \frac{4kTu_{seff}}{L^2_{eff}} \cdot (-Q_{inv}) \tag{3.37}$$

where

$$Q_{inv} = -W_{eff}L_{eff}C_{ox}V_{gsteff}\left(1 - \frac{A_{bulk}}{2\,(V_{gsteff} + 2vt)}V_{dseff}\right) \tag{3.38}$$

and μ_{seff} is the effective surface mobility. The derivation for this thermal noise expression is based on the noise model in [14]. Again, without taking the velocity saturation effect into consideration, this model is not suitable for the noise modeling of modern transistors.

- **Model of Fox**

Fox [25] presented some comments on the circuit model for MOSFET thermal noise based on Van der Ziel's earlier expressions [5]. According to his simulation results, he suggested that the power spectral density of the channel thermal noise should be expressed as

$$S_{I_d} = \alpha 4kTg_{do} \tag{3.39}$$

where g_{do} is the channel conductance with zero drain-to-source voltage and

$$\alpha = \begin{cases} \dfrac{1 - v + (v^2/3)}{1 - v/2} & V_d < V_{dsat} \\ \dfrac{2}{3} & V_d \geq v_{dsat} \end{cases} \tag{3.40}$$

with $v = V_d/V_{dsat}$. This model works reasonably well for long channel devices but it is not adequate for short channel devices, especially in saturation region, which is the usual region of operation for MOSFETs in analog integrated circuits. Because of the channel-length modulation and carrier heating effects, α will increase much beyond 2/3 for deep-submicron devices [30].

- **Model of Wang et al.**

Wang et al. [16] derived the formula of the channel thermal noise in both the linear and saturation regions for long and short channel devices. In this model, the derivation started from the expression

$$S_{I_d} = \frac{\overline{i_d^2}}{\Delta f} = 4kT\frac{\mu_{eff}}{L_{eff}}Q_N \tag{3.41}$$

and then included the velocity saturation effect in the calculation of Q_N. However, the derivation of (3.41) is based on the assumption that the effective mobility μ_{eff} is independent of lateral electric field [14]. If we include the velocity saturation effect at the very beginning when the power spectral density of channel thermal noise is derived, we should end up with (3.16). On the other hand, without taking the hot-carrier effect into account, this model cannot accurately predict the noise performance of short channel devices.

- **Model of Triantis et al.**

Triantis et al. [31] presented a thermal noise model which included the velocity saturation effect, and hot-electron effect. In this model, the transistor channel is divided into two regions - a gradual channel region and a velocity saturation region, and two channel models were derived for these regions. However, according to the velocity-field relationship in [32], the carrier velocity is not saturated until the electric field reaches the critical field E_C = 4V/μm at room temperature. For 0.5μm devices, this corresponds a V_{Dsat} = 2V. For most analog circuit applications, the devices are biased such that the V_{Dsat} is around 1.2V to 1.5V (e.g. V_{GS} = 2.0V). Therefore, before the carrier velocity saturates, channel pinchoff occurs. If we increase V_{DS} further to push the tip of the channel at the drain side towards to the source end, then the effective channel length is shorter at higher V_{DS} biases, the carrier velocity saturates, and the conducting channel of a transistor should be divided into a gradual channel region and a velocity saturation region. This can be observed from the fig. 5 in [31] where the noise originating from region II (saturation region) is visible only at very high V_{DS}. However, for deep-submicron devices, the maximum drain-to-source voltage V_{DS} is scaled down to prevent punchthrough in the devices, and therefore the maximum carrier velocity is not reached for most analog circuit applications.

Chapter 4

Measurements

4.1 Transistor Measurements

High frequency noise modeling of MOSFETs generally requires measuring the transistor's small-signal two-port network and noise parameters (minimum noise figure NF_{min}, equivalent noise resistance R_n, and optimized source resistance R_{opt} and reactance X_{opt}) over the full operating frequency range up to f_T. Some of the model parameters, such as effective surface mobility (μ_{seff}), transconductance (g_m), and output conductance (g_{ds}) etc. have to be extracted from the I-V characteristics. Other small-signal parameters such as gate-to-source and gate-to-drain overlap capacitances, can be extracted from the high-frequency s-parameters. Based on these extracted model parameters which can accurately predict the DC and AC performance of MOSFETs, we can then characterize the high frequency noise model of MOSFETs.

In this research, we are interested in how the high frequency noise performance of MOSFETs varies with the bias condition, frequency and design geometry i.e. the multi-finger gate design. The transistors measured were fabricated in a 0.8 μm BiCMOS technology with a maximum $f_T \approx 12$ GHz. These transistors have a channel length of 0.8μm and channel width of 1×60μm, and 6×10μm. We measured the s-parameters of the transistors at bias currents determined by varying V_{GS} from 1V to 3V with a fixed drain-source bias voltage, $V_{DS} = 3V$, so that the transistor is always in the saturation region of operation. Measurements were performed on several transistors and the results presented are typical ones.

4.2 Device Under Test (DUT)

In order to characterize the AC small signal behavior of microwave transistors, one has to measure a set of complex two-port parameters. The appropriate method at these high frequencies is the reflection and transmission measurements, which provide us with a set of scattering or s-parameters. When performing HF s-parameter measurements on wafer, probe pads and interconnection lines are required to access the transistor. These elements will introduce some parasitic effects which can have a dramatic impact on not only the measured s-parameters, but also on the noise parameters of a device. Therefore, an accurate procedure to de-embed the DUT from its environment (i.e. parasitics) is required for the characterization of an intrinsic device. As described in [21][22], a dummy device which includes probe pads, interconnections etc. without the transistor is required for the de-embedding procedure. Figure 4.1 shows the top view of the DUT and dummy pads.

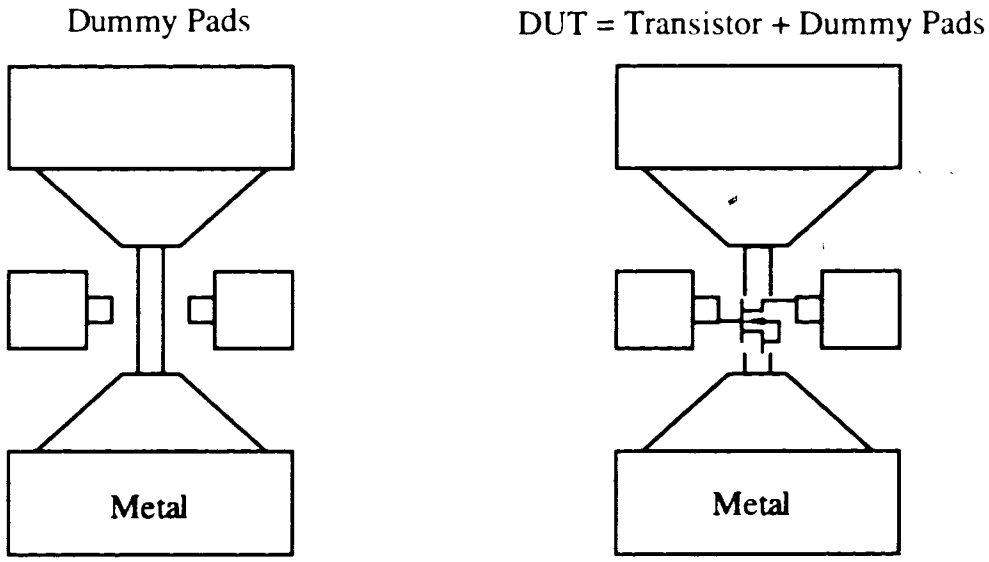


FIGURE 4.1: The layout of a test structure for on-wafer measurements.

The probe pads designed in our transistor test structures were laid out in a 2-port ground-signal-ground (GSG) configuration with the source connected to ground. Note that

the substrate is also connected to ground via metal 1 to the source. Port 1 connected to the gate of the transistor (input port) and port 2 is connected to the drain (output port). This configuration and the distance between the center of signal pad and that of ground pad depend on the microwave probes employed. The trapezoidal part of the ground pad can reduce the parasitic resistance and inductance from the source end of a transistor to the probe tip, and one should design it as close as possible to the transistor.

In our measurements, we used 150 μm pitch GSG microwave probes (Model 40A-GSG-150), fabricated by GGB Industries Inc. The probe tips have three in-line contacts, spaced 150 μm apart. The two outside contacts provide ground connections and the centre contact provides the signal connection. Figure 4.2 shows the top view of he GSG transistor test structure with contacting probe tips.

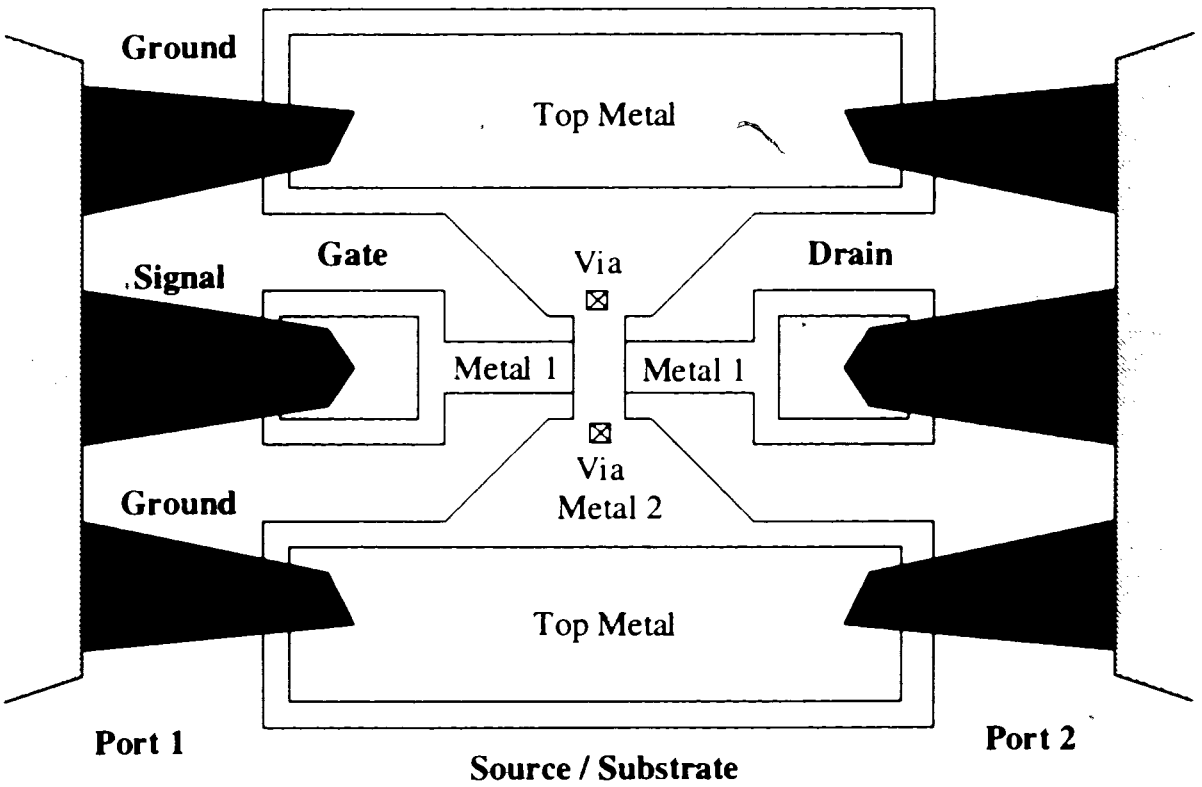


FIGURE 4.2: Schematic representation of the Ground-Signal-Ground (GSG) microwave probes in contact with MOSFET test structure for measuring scattering and noise parameters

4.3 DC Measurements

The I-V characteristics of the transistors are measured as a function of gate-source voltage (V_{GS}) in the linear region (V_{DS} = 0.05V), and drain-source voltage (V_{DS}) for V_{GS} = 1.0V, 1.5V, 2.0V, 2.5V, and 3.0V. Equipment used for DC measurements are the HP4145B semiconductor parameter analyzer and a DC probe station. Figure 4.3 shows the I_{DS}-V_{GS} characteristics of transistors in the linear region with V_{DS} = 0.05V. If we generate a straight line approximation to the I_{DS} vs. V_{GS} curve, having a slope equal to the maximum value of g_m, and positioned tangent to the curve at the curve where maximum g_m occurs, the line would intersect the x axis at a value of V_{GS}. This V_{GS} is the measured threshold voltage. From extrapolation, we can find the threshold voltage of the transistor is ~ 0.76V. Figure 4.4 shows the I_{DS}-V_{DS} characteristics for five different V_G's. It can be observed that in saturation we will expect a very large output resistance (R_{DS}) because of very small increase in I_{DS} over a wide range of V_{DS}.

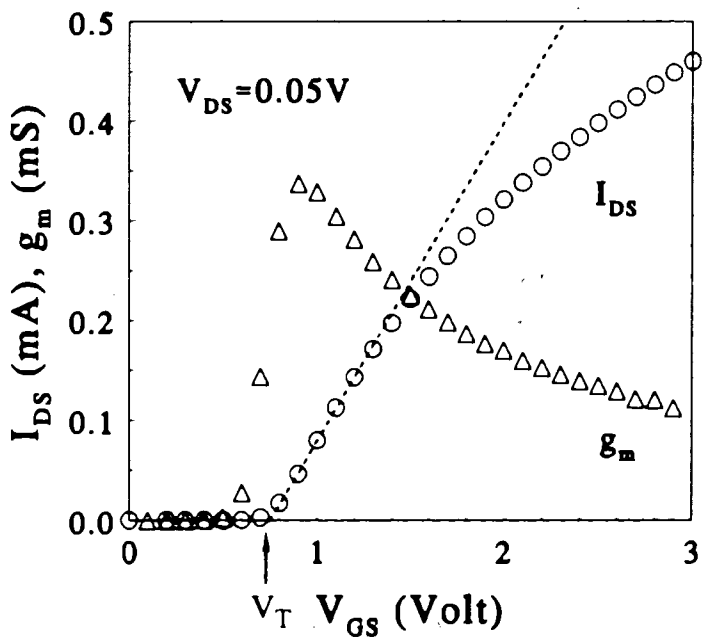


FIGURE 4.3: The I_{DS}-V_{GS} characteristics of a 1×60 μm/0.8 μm n-type MOS transistor. The transistor is biased at V_{DS} = 0.05V.

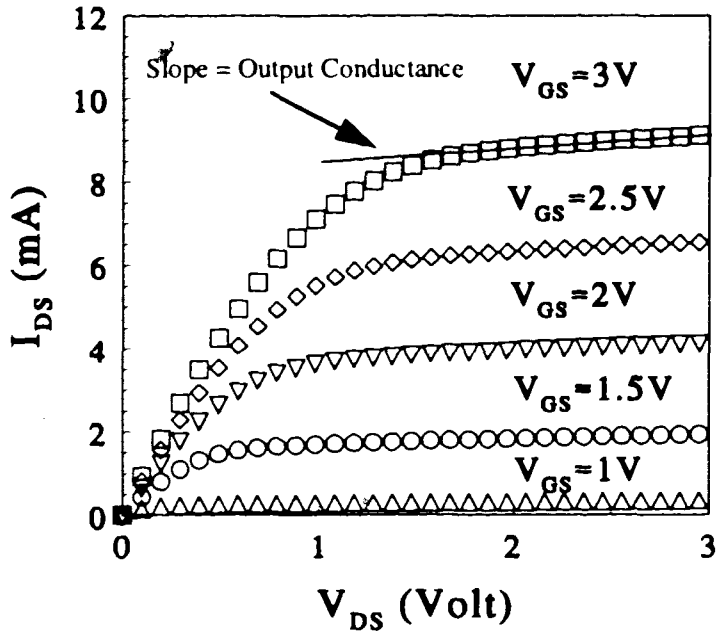


FIGURE 4.4: The I_{DS}-V_{DS} characteristics of a 1×60 μm/0.8 μm n-type MOS transistor.

4.4 Scattering and Noise Parameter Measurements

If the dimension of the components of circuits is at least an appreciable fraction of the wavelength of the voltage and current waves (i.e. distributed circuits), we can not neglect the effect of the phase changes in the waves traveling along the circuit elements. In addition, a practical problem exists when trying to measure voltages and currents at microwave frequencies because direct measurements usually involve the magnitude (inferred from power) and phase of a wave traveling in a given direction. Thus, equivalent voltages and currents, and the related impedance and admittance of circuits become somewhat of an abstraction when dealing with high-frequency networks. A representation more in accord with direct measurements, and with the ideas of incident, reflected, and transmitted waves, is given by the scattering matrix. Therefore, s-parameters are most commonly used in characterizing the high frequency performance of devices and circuits.

In addition, in order to characterize the AC and the noise characteristics of DUT at the same time, the s-parameter and noise parameters of transistors have to be measured successively. Therefore, the measurement system should combine the s-parameter measurement system and noise measurement system together and have the bias tee with variable input impedance for measuring the optimized source impedance. The NP5B Noise Parameter System and S-Parameter Measurement software manufactured by ATN microwave is employed for this purpose. This system is a solid-state tuner based, turn-key solution for complete small-signal device characterization. In conjunction with a network analyzer and noise receiver, it provides noise parameter and s-parameter measurements, equivalent models, and characterizations versus bias. All details, such as system setup, system calibration, and power level setting etc., will be described in the following sections.

4.4.1 System Setup

The complete S-Parameter and Noise Parameter Measurement System is shown in fig. 4.5. The system basically consists of three sub-systems - an ATN NP5B Wafer Prober Test Set, a HP8510 Network Analyzer System, a HP8970 Noise Measurement System, and other peripheral devices such as a printer, a computer, and a microwave probe station. The NP5B mainframe works as a switch for switching between the HP8510B for the s-parameter measurements and the HP8970 for the noise measurements of two-port networks.

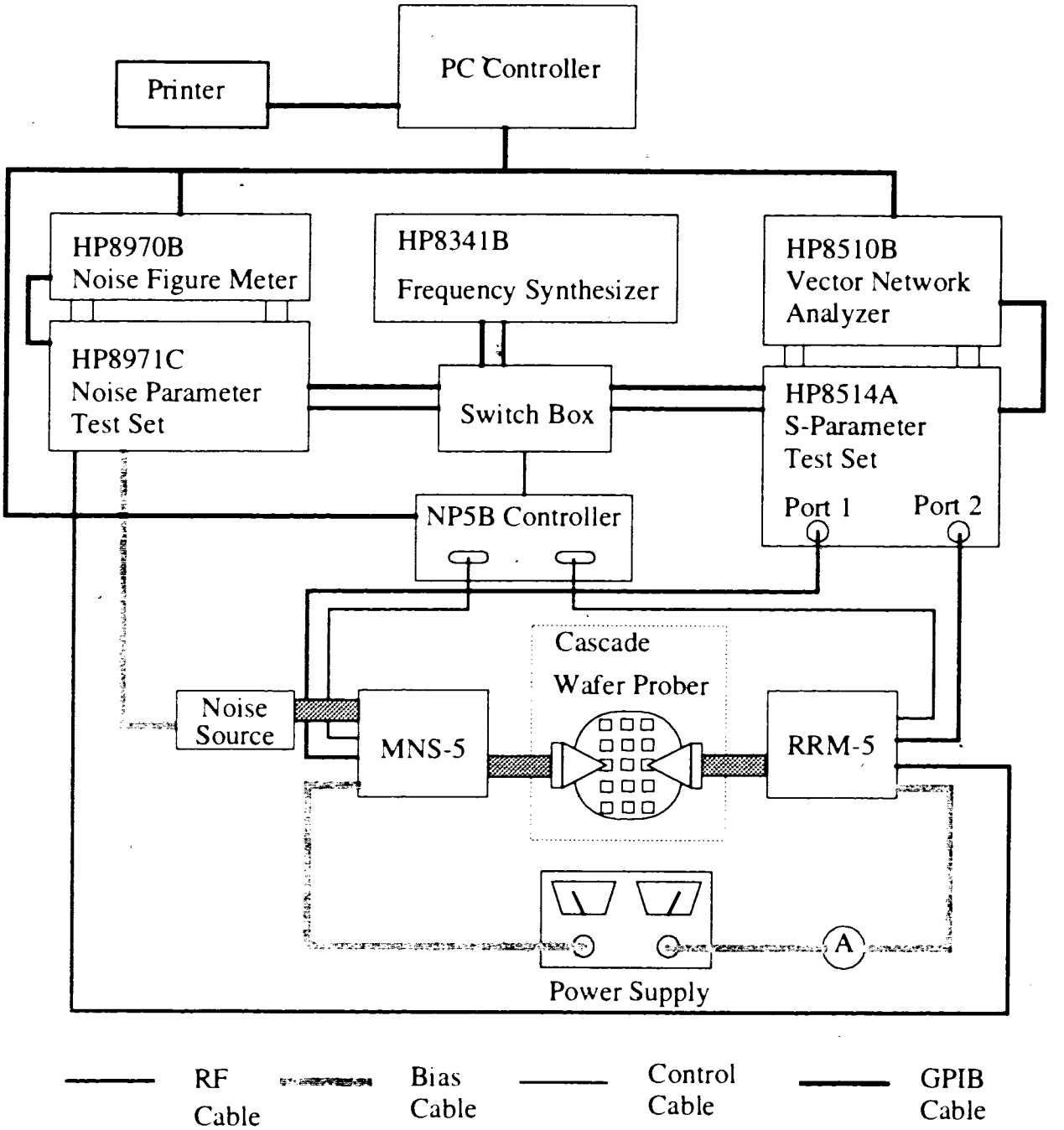


FIGURE 4.5: S-Parameter and Noise Parameter Measurement System for single source configuration.

- **NP5B wafer prober test set**

The ATN NP5B Wafer Prober Test Set is comprised of a main controller unit which drives the externally connected Mismatch Noise Source (MNS5) and the Remote Receiver Module (RRM5). The MNS5 contains a solid state electronic tuner (ET) with a built-in bias-T and RF switches which alternately connect the VNA and the noise source to the DUT while the output of the DUT is connected via the RRM5 unit to either port 2 of the VNA or the HP8970B noise figure meter via the built in low noise amplifier of the RRM5. The low noise amplifier in the RRM5 can lower system noise figure and therefore reduce the measurement uncertainty. The RRM5 also contains a bias-T and the necessary switching circuitry. The switch box in fig. 4.5 is used to pass the RF signal from the HP8341B frequency synthesizer to either the s-parameter measurement system or the noise measurement system if there is only one frequency synthesizer available for different measurement modes. Figures 4.6 to 4.11 show schematically the various measurement modes for the NP5B Noise Parameter Test Set.

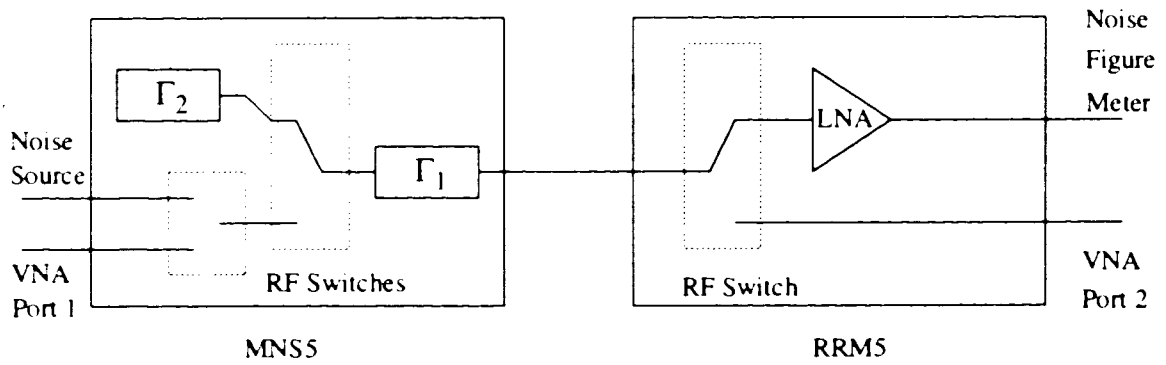


FIGURE 4.6: Mode 1 (low band noise) is used for cold calibration of the LNA and cold measurement of a DUT.

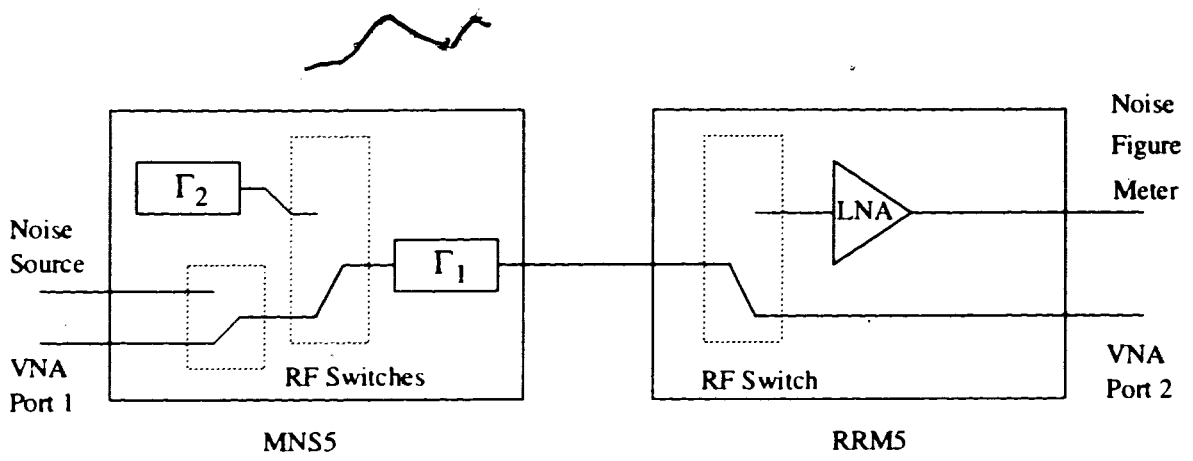


FIGURE 4.7: Mode 3 (s-parameter) is used for full 2-port calibration of the measurement system and for the measurement of the DUT.

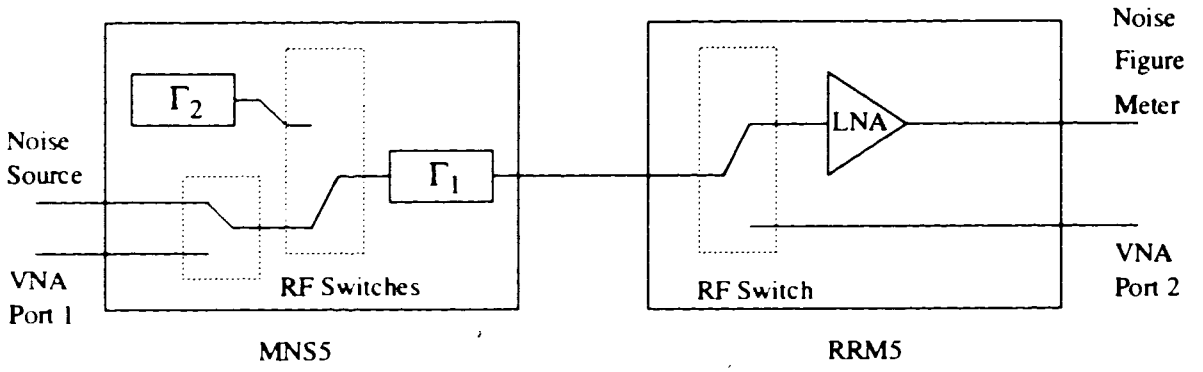


FIGURE 4.8: Mode 4 (low band noise figure system calibration) is used for noise figure measurements during calibration and measurement.

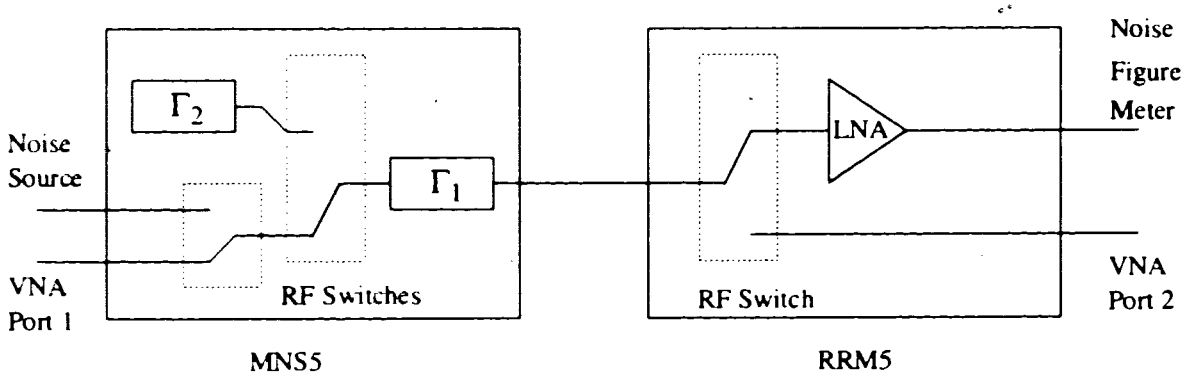


FIGURE 4.9: Mode 6 (low band RRM calibration) is used for the measurement of the input reflection coefficient of the LNA.

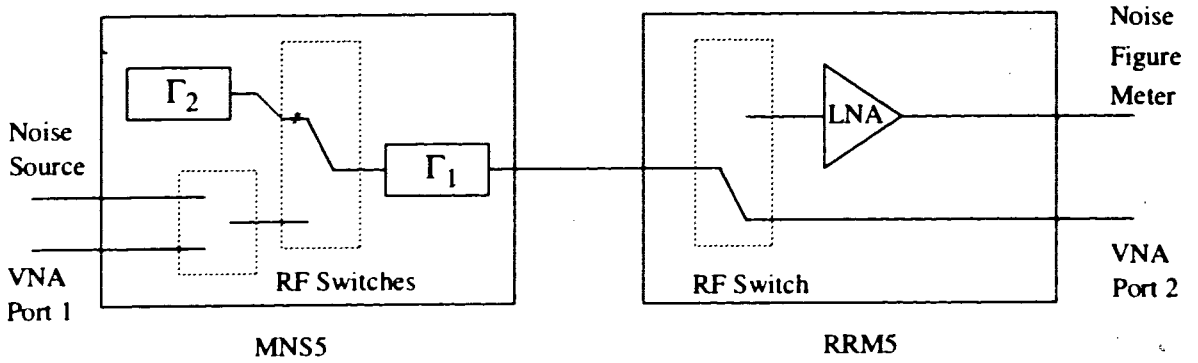


FIGURE 4.10: Mode 8 (Γ_1 and Γ_2) is used for the measurement of the reflection coefficients of the 88 tuner states during calibration.

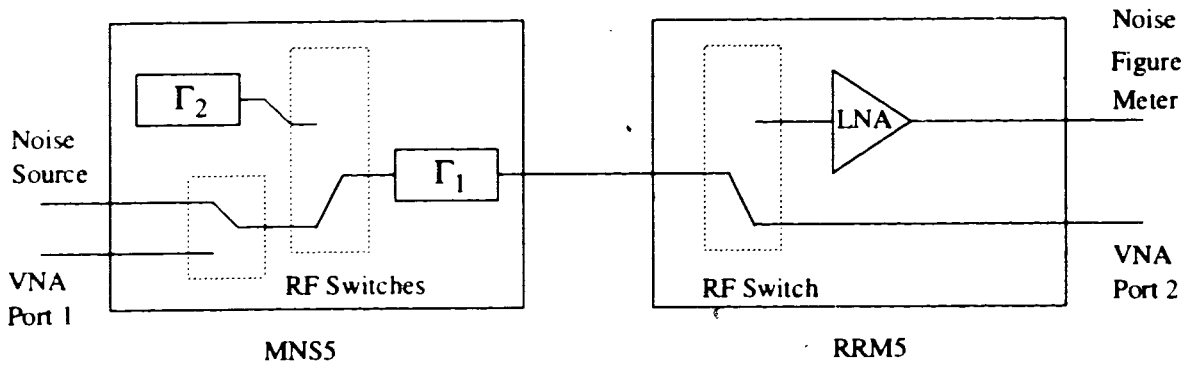


FIGURE 4.11: Mode 9 (Γ_1 and noise source) is used for measurement of the reflection coefficients of the hot and cold noise source and for the determination of the MNS5 network s-parameters using SOL (SHORT, OPEN, and LOAD) standards.

The measurement modes 2, 5 and 7 are omitted because the RRM5 module does not contain a second LNA amplifier for high frequency measurements.

- **S-parameter measurement system**

The s-parameter measurement systems contains the HP8510B Vector Network Analyzer (VNA) and HP8514A S-Parameter Test Set to measure the scattering and gain

parameters of linear two port networks. In the s-parameter measurement mode, the HP8510B controls the RF source (HP8341B) and two kinds measurements are made - reflection and transmission. An incident signal generated by the RF source is applied to the DUT and compared with the signal reflected from or transmitted through the input of the DUT. Reflection measurements are made by comparing the reflected signal to the incident signal. This results in measurement data on reflection characteristics of the DUT such as return loss, standing wave ratio (SWR), reflection coefficient (S_{11} or S_{22}) and impedance. Transmission measurements are made by comparing the transmitted signal to the incident signal. This results in measurement data on transmission characteristics of the network such as insertion loss, transmission coefficient (S_{21} or S_{12}), electrical delay (from which electrical length can be obtained), deviation from linear phase and group delay. By applying the incident signal to the output port of DUT, the reverse characteristics, output impedance and reverse transmission can be measured.

The HP8514A s-parameter test set separates the RF signal into an incident signal sent to the DUT and a reference signal against which the transmitted or reflected signals are later compared. It also routes the transmitted and reflected signals from DUT to the receiver for later processing. Internal attenuation from 0 to 90 dB, in 10 dB increments, are available to control the incident stimulus level at the DUT input without causing a change in the reference level.

- **Noise measurement system**

The noise measurement system consists of the HP8970B Noise Figure Meter and HP8971C Noise Parameter Test Set to measure the noise parameters and gain of DUT. The HP8970B can be tuned between 10 and 1,600 MHz and can also be swept over all or any part of that range. The HP8971C extends the frequency range of the noise figure meter from 1,600 MHz to 26,500 MHz.

- **Other peripheral devices**

Other peripheral devices are a dual DC voltage power supply for biasing the DUT, a current meter to monitor the drain current, a microwave probing station, a switch box used for passing the RF signal from the synthesizer to either the s-parameter measurement system or the noise measurement system depending on the measurement mode, a computer for data collection and a printer for printing the measurement results.

4.4.2 System Setting

After all the instruments are properly set up, we turn on the power switch of each instrument in the following order: s-parameter measurement system or noise measurement system, and then NP5B main control unit. When turning on the power of the s-parameter measurement system, one should follow the following power on sequence: frequency synthesizer, s-parameter test set, system periphery devices if there is any, and network analyzer. The HP8510 itself should turned on last in order for it to control the instruments connected to the system bus. In addition, the whole measurement system has to be turned on at least two hours before the calibration/measurements are performed in order to warm up the HP8971C.

To achieve the maximum measurement accuracy, the power level of the RF signal generated by the HP8341B synthesizer should be as high as possible without overloading the test set. According to the *HP8510 Network Analyzer Operating and Programming Manual* (p. 55-6), the source power between 0 to 10 dBm is optimal. However, when measuring a highly nonlinear device such as MOSFETs, we must ensure the power applied to the device is sufficiently low to avoid nonlinear distortion and gain compression. Attenuators in the port 1 and port 2 signal paths of the s-parameter

measurement test set provide a means of reducing the actual power supplied to the device. The attenuators can be set from 0 to 90 dB in 10 dB increments.

At low frequencies, the drain current I_{DS} varies approximately as $(V_{GS} - V_{TO})^2$, where the threshold voltage, V_{TO}, is ~ 0.76V for the 0.8μm BiCMOS technology. The small-signal model of the transistor is only valid when the small-signal voltage is small compared to the DC voltages i.e. $\Delta V/V << 1$. However, if the power level is too small, the measured s-parameters will appear noisy. On the other hand, if the power level is too large, the measured s-parameters will again be too small because of gain compression. In addition, the measured s-parameters should remain constant over a range of intermediate power levels. For greatest measurement accuracy, we set the power level to a value in the middle of dynamic range of DUT. The procedure must be repeated for both port 1 and port 2. Figure 4.12 shows the general dynamic range of a realistic amplifier with a gain of 10 dB.

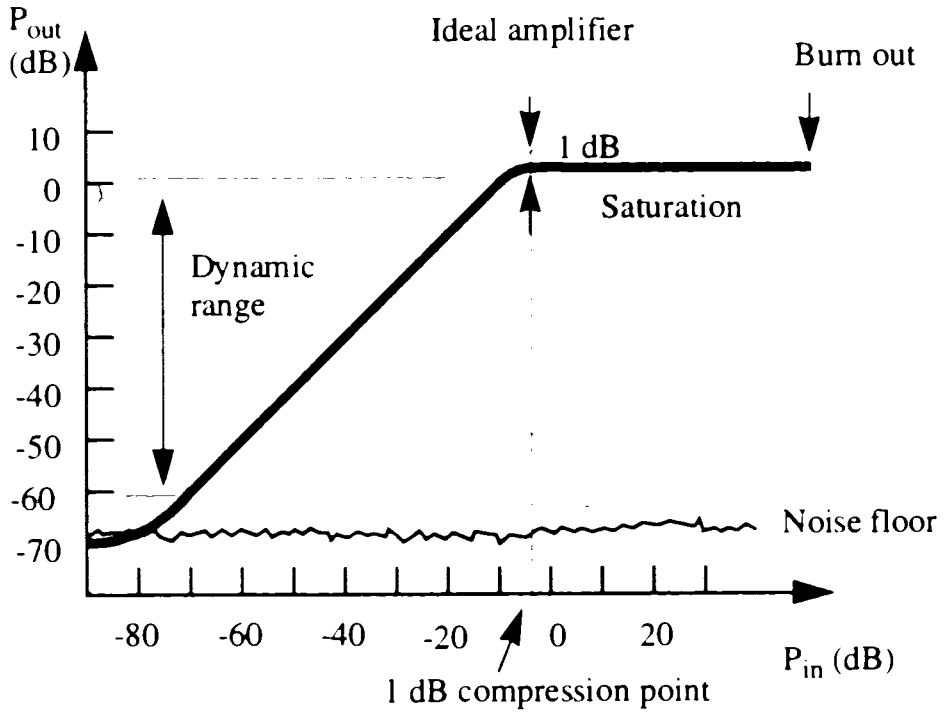


FIGURE 4.12: The dynamic range of a realistic amplifier.

Since the output of the MOSFETs is not as nonlinear as the input, less attenuation is required at port 2. In our measurements, the power level is set to 5 dBm (at the starting frequency of 0.5 GHz) with 30 dB attenuation at port 1 and 10 dB attenuation at port 2. Taking into account about 2 dB loss in the cables, this will give about -27 dBm at port 1 and -7 dBm at port 2.

The optimal power levels will vary with frequency. At higher frequencies, more power is lost in the test set, cabling and bias-T's. In addition, the input and output impedance of the DUT vary with frequency. In order to compensate for the change in the optimal source power, the HP8510B provides a Power Slope setting which allows the source power to either increase or decrease with frequency. In our measurement, the power slope is set to 0.2 dB/GHz.

All s-parameters were measured over the maximum frequency range of the s-parameters test set, from 500 MHz to 18 GHz, and noise parameters were measured from 2 GHz to 6 GHz, with 0.5 GHz frequency step. Because the time for the noise parameter measurements is quite long (depending on the measurement averages) and we do not want the devices to be stressed, the number of measurement points (for different frequencies and bias conditions) and the bias voltages applied (especially V_{DS}) are set to compromised values.

The VNA provides a fast-sweep-mode and a continuous-wave-mode for sweeping the frequency. In the fast-sweep-mode, the synthesizer frequency is gradually swept over the entire frequency range while the VNA measures the s-parameters at the specified frequency points. In continuous-wave-mode, the synthesizer frequency is stepped from one frequency value to another and the VNA measures the s-parameters after a specified settling time. We used the continuous-wave-mode, which is slower but more accurate.

According to the HP8510B manual, a settling time of 2 ms per point is more than sufficient. The settling time is specified indirectly by the Sweep Time parameter. The settling time is approximately equal to the Sweep Time divided by the total number of points.

The HP8510B provides simple data processing features such as data smoothing and data averaging. We disabled the data smoothing feature but enabled data averaging to lower the noise floor. With data averaging on, the s-parameters are repetitively measured a specified number of times and averaged at each frequency point. Although, averaging improves the signal-to-noise ratio, it also dramatically increases measurement time. The averaging factor can be set up to 4096; however, we opted for an averaging factor of 1024 to reduce the measurement time.

All configuration parameters are entered from the NP5B controlling software under the SET CONFIG and SET FREQ manuals of SYSTEM CONFIG. The next section discusses calibration of the overall system to correct for the parasitics of the measurement setup.

4.4.3 System Calibration

The NP5B noise parameter measurement system is based on the Adamian and Uhlir concept which states that the knowledge of the total hot output noise power of a standard noise source plus the total output noise power of several passive one port terminations is sufficient for complete noise parameter characterization of a linear receiver [34][35]. This fundamental receiver concept can be extended to the characterization of a linear two-port by simply using the correlation matrix to de-embed the linear two-port from the overall system and receiver noise parameter [37][38]. According to the circuit theory of linear

noise networks, the necessary and sufficient conditions to calibrate a linear receiver and make noise parameter measurements of linear two-port networks [36] as follows.

1. A calibrated vector network analyzer at the DUT reference planes to make s-parameter measurements over the frequency range of interest.

2. A linear noise power receiver at the DUT reference plane with known noise parameters and input reflection coefficient over the frequency range of interest. This requires a known noise source at the receiver reference plane.

3. A large number of known terminations at the DUT input reference plane over the frequency range of interest.

According to the ATN NP5B Operation Manual, there are several calibration steps which have to be completed in sequence before the s-parameter and noise measurements are made. These steps are explained according to the sequence in the calibration procedure.

1. Calibration of the Short, Open, and Load (C SOL): With a thru' of known delay as the DUT, the NP5B system makes raw S_{22} measurements with a short, open, and load in the place of the noise source. This raw data will be combined with the data taken during the full 2 port calibration (at the device plane) to determine the s-parameters of the MNS5. It is done with 4 factory selected low-loss source impedance settings and averaged.

2. Calibration of the Noise System- Part 1 (C NS1): With the same thru' as in the SOL calibration and having established a reference plane at the noise source from the SOL calibration, the NP5B system makes raw S_{22} measurements with the noise source on and off and calculates the corresponding reflection coefficients

for the noise source. It displays these results for information purpose to the system CRT. The NP5B system then proceeds to make hot and cold power measurements with the noise figure meter. These power measurements are used later to establish the gain and noise figure for the receiver.

Fine tuning calibration (Peaking the YIG) is used to align the passbands of the noise figure meter and noise figure test set at the measured frequencies defined by START FREQ, STOP FREQ and STEP SIZE. Because the noise measurements were done under the single sideband operation and usually most of the measurement frequencies are higher than 2400 MHz, Fine Tuning Calibration is always recommended. The noise measurement system will perform better the more frequently a Fine Tuning Calibration is done. However, once the Fine Tuning Calibration is done, a new fine Tuning Calibration should not be required unless the Noise Figure Test Set is turned off, the ambient air temperature around the Noise Figure Test Set changes more than ±5°C since the last Fine Tuning Calibration or the START FREQ, STOP FREQ or STEP SIZE have been changed.

3. Calibration of the S-Parameters (C SP): This is a standard s-parameter calibration by any of the standard acceptable methods - Short-Open-Load-Thru' (SOLT), Line-Reflect-Match (LRM), Thru'-Reflect-Line (TRL), or Line-Reflect-Line (LRL). Note that the s-parameter reference planes are the noise parameter reference planes in the NP5B software. It is useful to end on a thru' so that once the s-parameter calibration is finished, the thru' can be checked. If the thru' is bad, stop and re-do the s-parameter calibration.

4. Calibration of the Thru' Delay (C TD): With the same thru' as in the SOL and NS1 calibrations as the DUT, the corrected s-parameters are measured and the thru' delay is calculated and displayed for confirmation.

5. Calibration Calculation of the SOL (C CSOL): From the information obtained in the SOL, NS1, SP, and TD calibrations, the s-parameters of the MNS from the noise source to the s-parameter port 1 reference plane are calculated. Also the noise and gain references as measured in C NS1 are transferred to the s-parameter port 2 reference plane.

6. Calibration of the Source Reflection Coefficients - Gammas (C SG): With the same thru' as before, S_{22} measurements are made for the 88 impedance states of the solid state tuner. These impedances are then referred to the s-parameter port 1 reference plane and stored.

7. Calibration of the Post Receiver (C PR): With the same thru' as before, S_{11} measurements are made to determinate the input reflection coefficient of the post receiver. This information is referred to the s-parameter port 2 reference plane and stored.

8. Calibration of the Noise System - Part 2 (C NS2): With the same thru' as before, noise power versus source impedance is measured and the receiver noise parameters are calculated and stored at the s-parameter port 2 reference plane.

After going through the eight calibration procedures listed above, the whole system is ready for the s-parameter and noise parameter measurements.

Chapter 5

AC Modeling and Parameter Extraction

5.1 Pad Effects and S-Parameter De-Embedding

With the continuous downscaling of the device dimensions, the impact of the surrounding parasitics on wafer has steadily gained importance. Since the probe pads contain additional parasitics including resistances, inductances, and capacitances of pads and interconnections, de-embedding techniques must be performed. This de-embedding has to be done prior to the extraction of device parameters to isolate the intrinsic device performance from the extrinsic parasitic effects that show up in the both AC and noise measurements.

Wijnen et al. in 1989 [21] presented a method to get rid of the most important parasitics for on-wafer s-parameter measurements by measuring a dummy structure ('OPEN') on the chip. Koolen et al. [22] improved the method by taking into account the influence of the interconnect lines between pads and transistor with the additional measurement of a 'SHORT' dummy structure. Lee et al. [23] modified the 'SHORT' structure and de-embedding method employed by Koolen so as to be able to extract the parasitic inductances of interconnections. In this section, these two methods will be described.

- **Koolen et. al de-embedding technique**

The RF probe-pad parasitics are subtracted from measured s-parameters using two test structures. Figure 5.1 shows the layouts of DUT and dummy pads used by Koolen [22]. The first is the "open" structure that consists of RF probe pads and interconnections

without contacting to active area of the device. The "short" test structure consists of the "open" structure except with shorted interconnections at the plane of the MOS transistors. The de-embedding technique improved the accuracy by fabricating these test structures using the same process as the actual device, except for skipping the interconnection contact process. Figure 5.2 shows the physical equivalent circuit diagram representing the probe pads used for the de-embedding procedure. This consists of three parallel elements (Y_{PGS}, Y_{PGD}, and Y_{PDS}) and three series elements (Z_G, Z_S, and Z_D).

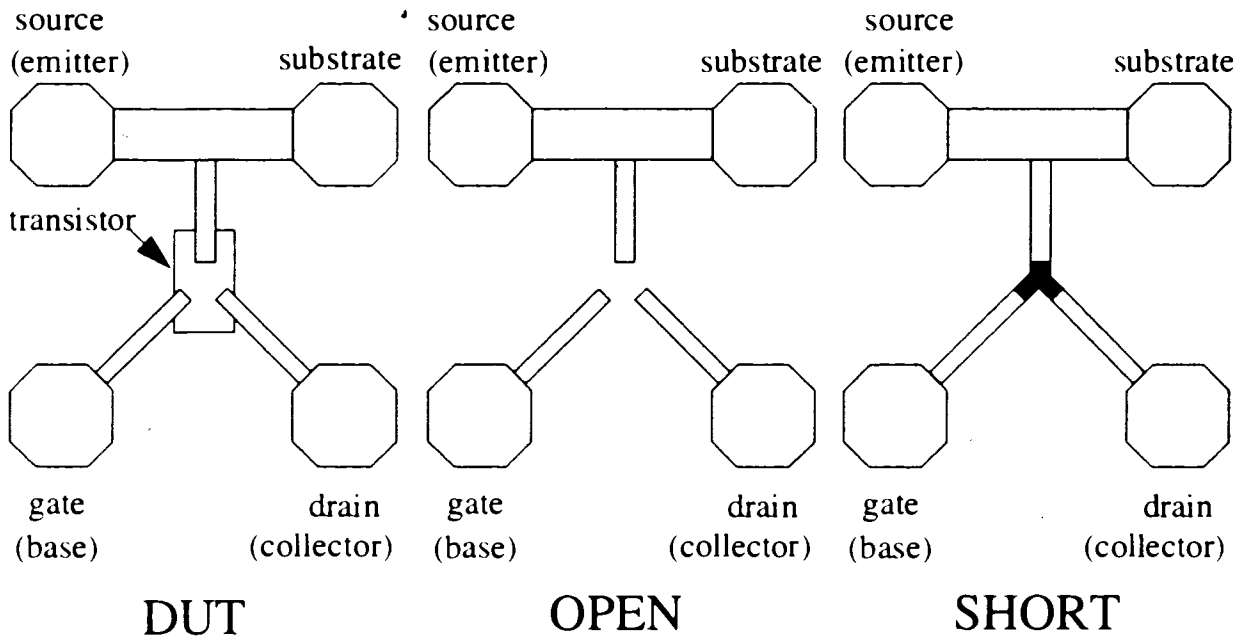


FIGURE 5.1: The schematic layout of a RF probe-pattern based on ground-signal (G-S) configuration used for "on wafer" measurements and dummy pads used for parallel and series parasitics de-embedding.

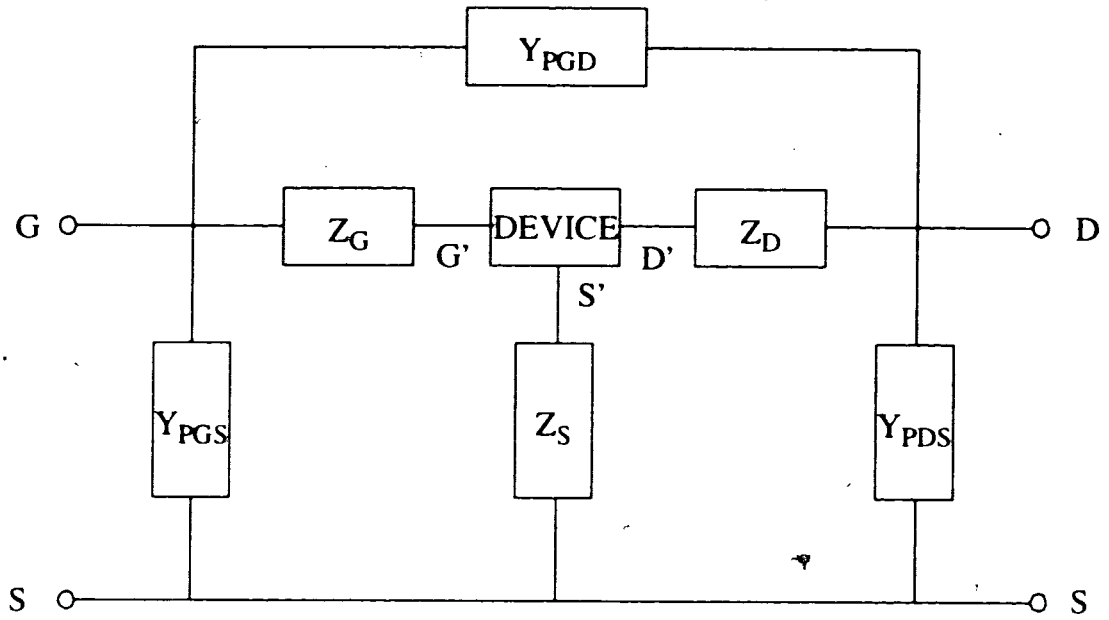


FIGURE 5.2: Equivalent circuit diagram representing the pad structures.

High-frequency s-parameter measurements were performed on each test set structure and the DUT. The de-embedded Z parameters of intrinsic devices were obtained after the probe-pad parasitics are removed through the following procedures.

1. Convert the measured s-parameters $[S_D]$, $[S_O]$, and $[S_S]$ of DUT, "open", and "short" structures to their respective Y parameters $[Y_D]$ $[Y_O]$, and $[Y_S]$. The parallel elements, Y_{PGS}, Y_{PGD}, and Y_{PDS}, in figure 5.2 can be extracted from the $[Y_O]$ by

$$Y_{PGD} = -Y_{12,O} \ (or \ -Y_{21,O}) . \tag{5.1}$$

$$Y_{PGS} = Y_{11,O} + Y_{12,O} . \tag{5.2}$$

$$Y_{PDS} = Y_{22,O} + Y_{21,O} . \tag{5.3}$$

2. Subtract the parallel parasitics, Y_{PGS}, Y_{PGD}, and Y_{PDS}, from the $[Y_D]$, and $[Y_S]$ by

$$[Y_{DA}] = [Y_D] - [Y_O] \quad (5.4)$$

$$[Y_{SA}] = [Y_S] - [Y_O] . \quad (5.5)$$

3. Convert the $[Y_{DA}]$ and $[Y_{SA}]$ to $[Z_{DA}]$ and $[Z_{SA}]$.

4. Subtract all series parasitics, Z_G, Z_S, and Z_D, of RF probe-pad model from $[Z_{DA}]$ to get the intrinsic Z parameters of transistors by

$$[Z] = [Z_{DA}] - [Z_{SA}] . \quad (5.6)$$

- **Lee's de-embedding technique**

With the same DUT and "open" test structures as in [23], figure 5.3 shows the layouts of the modified "short" dummy pads employed by Lee et al [23] for series parasitics de-embedding. The "short 1", "short 2", and "through" test structures consist of the "open" structure except with shorted gate and source (G-S), shorted drain and source (D-S), and shorted gate and drain (G-D) interconnections at the plane of MOS transistors, respectively.

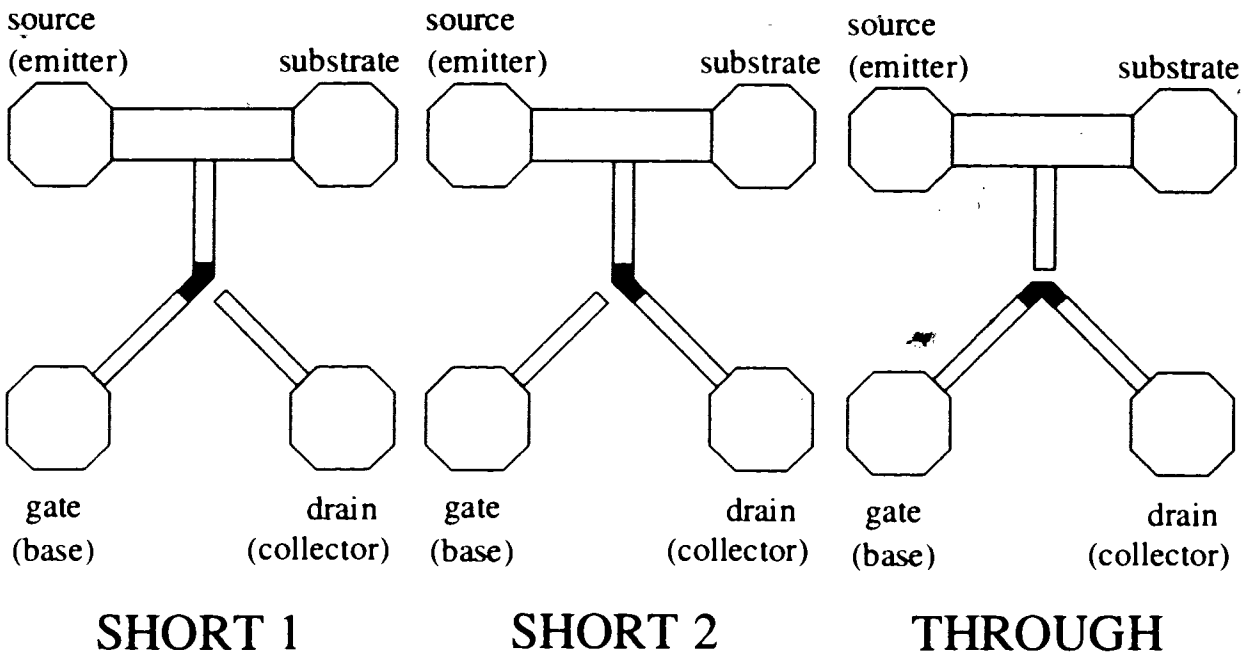


FIGURE 5.3: Modified "SHORT" test structures used for series parasitics de-embedding.

High-frequency s-parameter measurements were performed on each test set structure and DUT. The de-embedded Z parameters of intrinsic devices were obtained after the probe-pad parasitics are removed through the following procedures:

1. Convert the measured S parameters $[S_D]$, $[S_O]$, $[S_{S1}]$, $[S_{S2}]$, and $[S_T]$ of DUT, "open", "short 1", "short 2", and "through" structures to each Y parameters $[Y_D]$ $[Y_O]$, $[Y_{S1}]$, $[Y_{S2}]$, and $[Y_T]$.

2. Subtract Y_{PGS}, Y_{PGD}, and Y_{PDS} from the $[Y_D]$, $[Y_{S1}]$, $[Y_{S2}]$, and $[Y_T]$ by

$$[Y_{DA}] = [Y_D] - [Y_O] . \tag{5.7}$$

$$[Y_{S1A}] = [Y_{S1}] - [Y_O] . \tag{5.8}$$

$$[Y_{S2A}] = [Y_{S2}] - [Y_O]. \tag{5.9}$$

$$[Y_{TA}] = [Y_T] - [Y_O]. \tag{5.10}$$

3. Convert the $[Y_{DA}]$, $[Y_{S1A}]$ and $[Y_{S2A}]$, and to $[Z_D]$, $[Z_{S1}]$ and $[Z_{S2}]$. The series elements, Z_G, Z_S, and Z_D, of RF probe pad model in figure 5.2 can be extracted using $[Z_{S1}]$, $[Z_{S2}]$, and $[Y_{TA}]$ by

$$Z_G = Z_{11,S1} - \frac{1}{2}\left(Z_{22,S2} + \frac{1}{Y_{12,TA}}\right). \tag{5.11}$$

$$Z_S = \frac{1}{2}\left(Z_{11,S1} + Z_{22,S2} + \frac{1}{Y_{12,TA}}\right). \tag{5.12}$$

$$Z_D = Z_{22,S2} - \frac{1}{2}\left(Z_{11,S1} + \frac{1}{Y_{12,TA}}\right). \tag{5.13}$$

4. Subtract all series elements Z_G, Z_S, and Z_C of RF probe-pad model from $[Z_D]$ to get the intrinsic Z parameters of transistors by

$$Z_{11} = Z_{11,D} - Z_{11,S1}. \tag{5.14}$$

$$Z_{12} = Z_{12,D} - \frac{1}{2}\left(Z_{11,S1} + Z_{22,S2} + \frac{1}{Y_{12,TA}}\right). \tag{5.15}$$

$$Z_{21} = Z_{21,D} - \frac{1}{2}\left(Z_{11,S1} + Z_{22,S2} + \frac{1}{Y_{12,TA}}\right). \tag{5.16}$$

$$Z_{22} = Z_{22,D} - Z_{22,S2}. \tag{5.17}$$

The two s-parameter de-embedding techniques cited above assume that the solid lines in the "short" test structure are much shorter than the interconnections so that their series parasitics are negligible. However, for the high-frequency measurements of MOSFETs,

very wide transistors or multi-flinger structures are usually designed in order to increase the measurement accuracy. In these cases, the distances between the tips of interconnections are usually long, and these techniques will overestimate the series parasitics. Therefore, in this research, using a special DUT design, only the "open" test structure is used in de-embedding and the series parasitics are extracted through the parameter extraction of an intrinsic transistor.

5.2 AC Model

The AC equivalent circuit model of the MOSFET is formulated on the basis of its physical structure. Figures 5.4 and 5.5 show the cross-section of a n-type MOSFET in a common source configuration with the source and body connected.

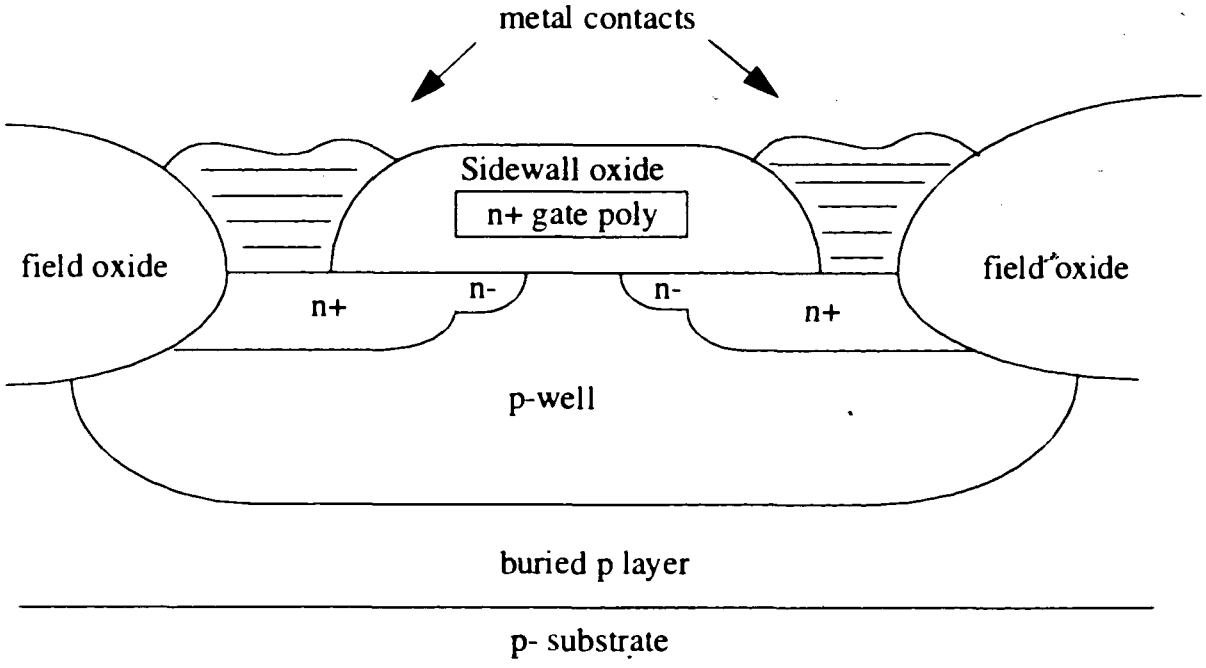


FIGURE 5.4: Process cross-section of a typical n-type MOSFET (not to scale) from [24].

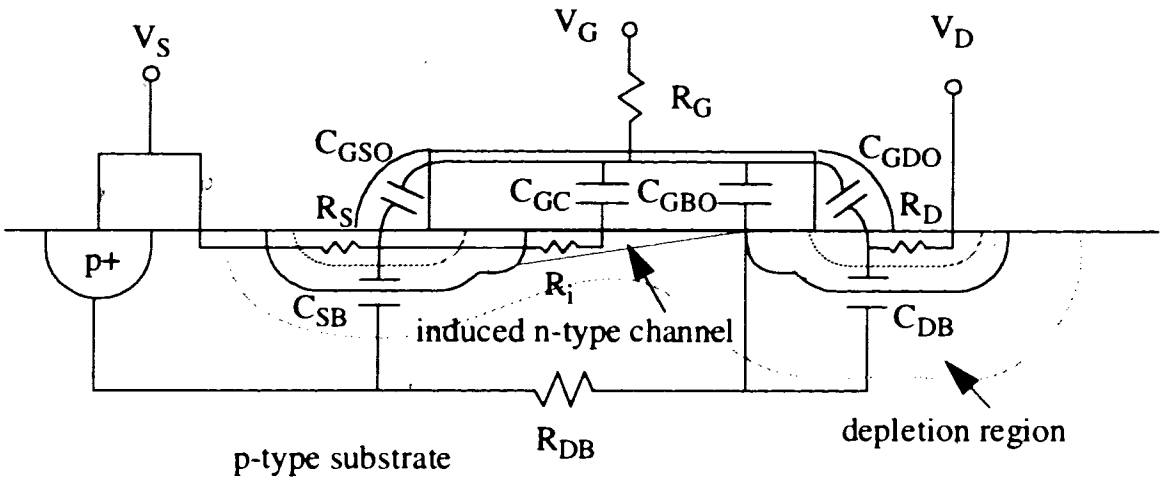


FIGURE 5.5: Cross-section of a n-type MOSFET with corresponding physical components for its high frequency small-signal model.

According to figure 5.5, C_{GSO}, C_{GDO}, and C_{GBO} are gate-to-source, gate-to-drain, and gate-to-bulk capacitance, respectively. C_{GC} is the gate-oxide capacitance between the gate and channel. C_{SB} and C_{DB} are source-to-bulk and drain-to-bulk junction capacitance. R_S and R_D are the source and drain parasitic resistance, R_G is the polysilicon gate resistance, R_i is the channel resistance, and R_{DB} is the substrate resistance. Based on this diagram, figure 5.6 shows the equivalent circuit model for the high-frequency modeling. In this model, the gate-to-source capacitance C_{GS} takes care of the effects of C_{GC} and C_{GSO}, and C_{GD} is C_{GDO}

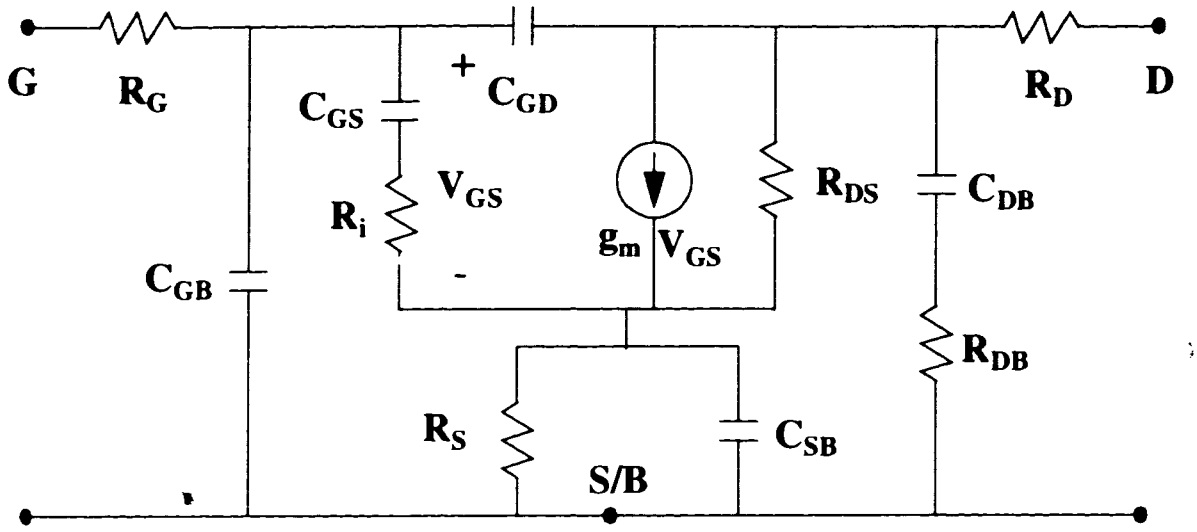


FIGURE 5.6: The equivalent high-frequency small-signal model for MOSFETs including gate resistance R_G and channel resistance R_i.

Based on the high-frequency small-signal model shown in figure 5.6 and the DC and s-parameter measurements, the next step is to extract the model parameters used in noise calculation (from DC measurements) and AC performance characteristics (from s-parameter measurements) as a function of bias conditions.

5.3 Model Parameter Extraction

Before extracting the DC and AC model parameters, some DC and s-parameter measurements have to be conducted. In this research, HSPICE level 3 DC model is used for the simulation of I_{DS} vs. V_{DS} and I_{DS} vs. V_{GS} characteristics. The device-under-test is a n-type MOSFET with channel length 0.8 μm and channel width 60 μm designed in a common-source configuration fabricated by using 0.8 μm BiCMOS technology through Canadian Microelectronics Corporation (CMC) by Nortel. Based on the optimization function in HSPICE and MMICAD, all the model parameters will be extracted.

- **DC parameter extraction:**

Some DC model parameters, such as low field bulk mobility (*UO*), mobility degradation factor (*THETA*), drain resistance (*RD*), source resistance (*RS*), will be extracted from the I_{DS} vs. V_{GS} characteristics in the linear region. Others, maximum drift velocity of carriers (*VMAX*), static feedback factor (*ETA*) for adjusting the threshold voltage, saturation field factor (*KAPPA*) which is used in the channel length modulation equation, will be extracted from the I_{DS} vs. V_{DS} characteristics for different V_{GS} values. The rest of DC model parameters are based on the default values provided by the manufacturer. DC measurements for I_{DS} vs. V_{GS} characteristics in the linear region are carried out with V_{DS} = 0.05 V and V_{GS} is from 0 V to 3 V. Figure 5.7 shows the measured and simulated (using HSPICE) linear I_{DS} vs. V_{GS} characteristics for *UO* = 435 $cm^2/V{\cdot}s$, *THETA* = 0.008 V^{-1}, *RD* = *RS* = 1227 Ω/❑ (using ACM = 2 diode model).

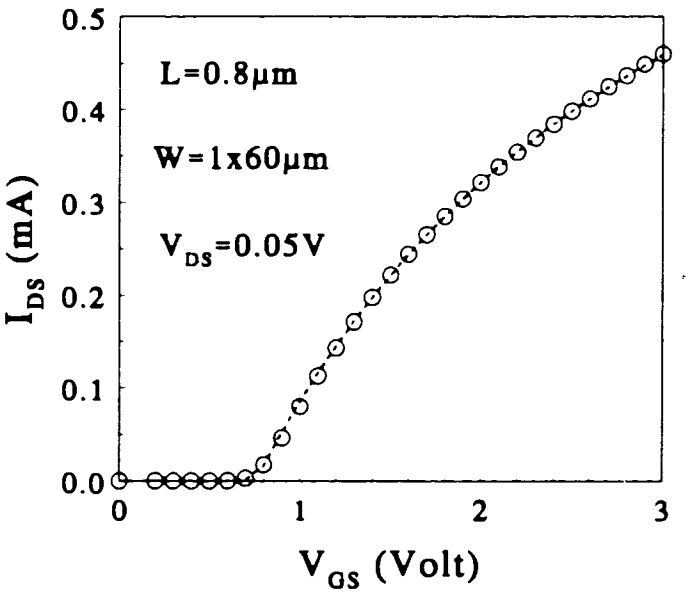


FIGURE 5.7: Measured and simulated I_{DS} vs. V_{GS} characteristics of a 60μm/0.8μm n-type MOSFET biased in linear region for V_{DS} = 0.05V.

After the *UO*, *THETA*, *RD*, and *RS* are extracted, *VMAX*, *ETA*, and *KAPPA* are extracted based on the I_{DS} vs. V_{DS} characteristics. Figure 5.8 shows the measured and simulated I_{DS} vs. V_{DS} characteristics for five different V_{GS} with *VMAX* = $1.0 \cdot 10^7$ cm/s, *ETA* = 0.003, and *KAPPA* = 0 V^{-1}.

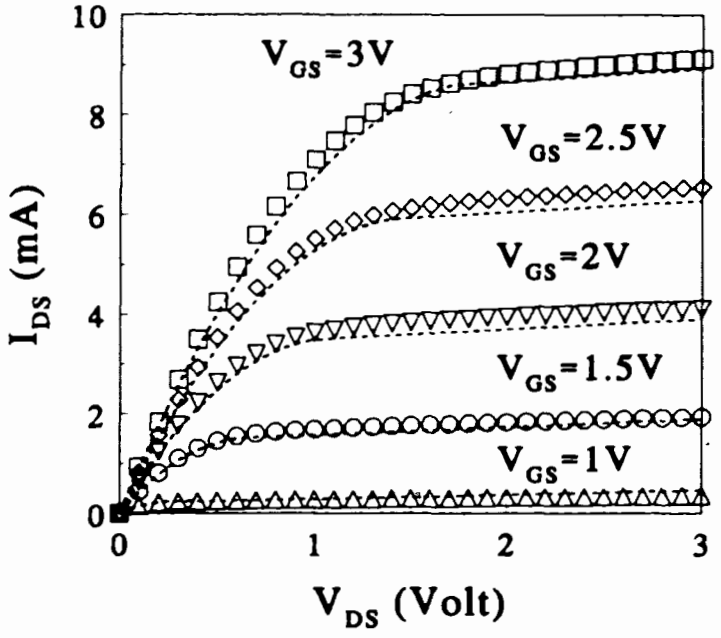


FIGURE 5.8: Measured and simulated I_{DS} vs. V_{DS} characteristics of a 60μm/0.8μm n-type MOSFET for V_{GS} = 1.0V, 1.5V, 2.0V, 2.5V, 3.0V.

After these HSPICE model parameters are extracted, the parameters R_D and R_S in figure 5.6 can be calculated by the equation on page 15-30 in [13] and are end up with 20.4 Ω for this measured transistor.

The next extracted small-signal parameters are g_m and R_{DS}. The transconductance (g_m) is extracted from the first order derivative of I_{DS} vs. V_{GS} characteristics in saturation with V_{DS} = 3.0V. On the other hand, R_{DS}, by definition, is $1/g_{DS}$ where g_{DS} is dI_{DS}/dV_{DS}. In this research, because we are interested in the performance (AC and noise) as a function

of bias current, so rather than extract g_{DS} individually, we performed I_{DS} vs. V_{GS} measurements with V_{DS} = 2.85V, 2.9V, 2,95V, 3.0V, and 3.05V and extract g_{DS} from $dI_{DS}/0.05V$ at specific V_{GS}. Figures 5.9 and 5.10 show the extracted g_m and g_{DS} as a function of I_{DS} at which AC and noise measurements are performed.

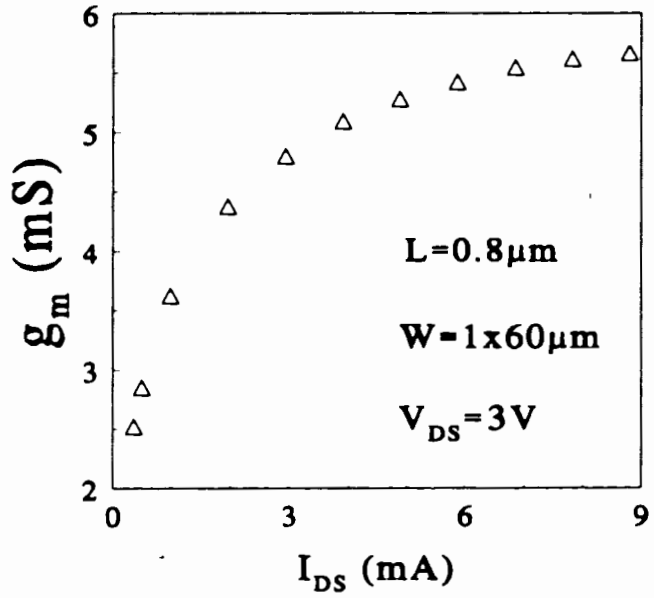


FIGURE 5.9: Extracted g_m as a function of I_{DS} for V_{DS} = 3.0V.

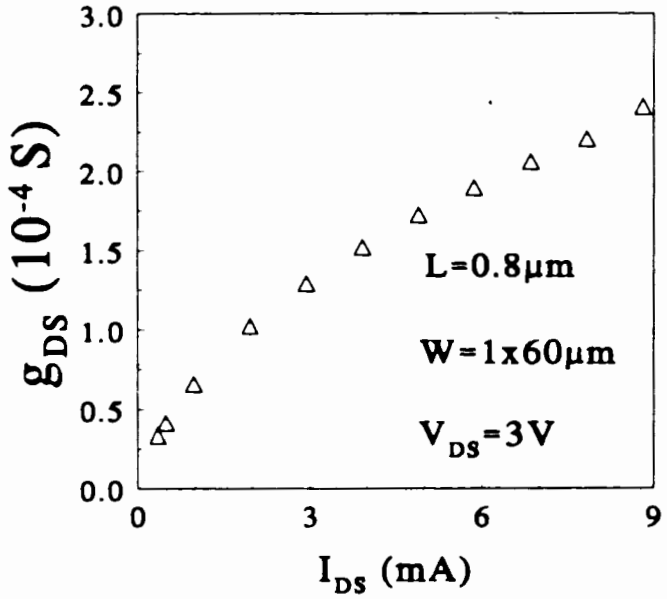


FIGURE 5.10: Extracted g_{DS} as a function of I_{DS} for V_{DS} = 3.0V.

Now the parameters - R_D, R_S, g_m, and R_{DS} in the small signal model are extracted. The next step is to extract the rest of capacitances and resistances from the measured s-parameters.

- **AC parameter extraction:**

AC model parameters are extracted by using the optimization function of MMICAD (Monolithic and Microwave Integrated Circuit Analysis and Design) based on the de-embedded s-parameters. In this research, only the open dummy structure is used to de-embed the parallel parasitics. Therefore, fitting of the de-embedded s-parameters should include the small-signal model and the series parasitics - L_G, L_S, and L_D. S-parameter measurements are conducted in the frequency range from 0.5 GHz to 10 GHz with 0.5 GHz step for each bias current from 0.5 mA to 9.0 mA with a 0.5 mA current step. Figures 5.11 and 5.12 show the magnitude and phase of the measured and simulated s-parameters of the intrinsic transistor for I_{DS} = 6.0 mA with extracted L_G = 850 pF, L_S = 0 pF, and L_D = 240 pF. From the extracted series inductance L_G, it is found that because of very wide channel width, the series inductance is mainly caused by the gate itself instead of the interconnection which makes the "short" structure for de-embedding the series parasitics unsuitable in this case.

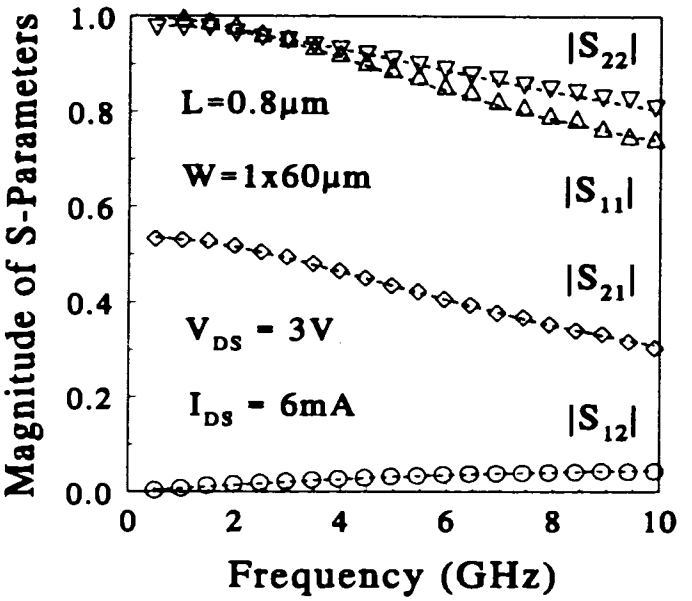


FIGURE 5.11: The magnitude of measured and simulated s-parameters of a intrinsic transistor biased at I_{DS} = 6.0 mA.

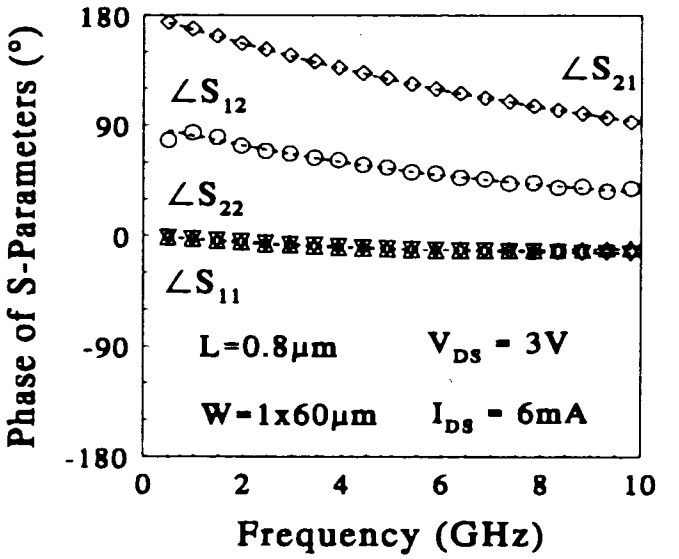


FIGURE 5.12: The phase of measured and simulated s-parameters of a intrinsic transistor biased at I_{DS} = 6.0 mA.

Based on the optimization results shown above, the rest of the model parameters - C_{GS}, C_{GD}, C_{SB}, C_{DB}, C_{GB}, R_i, R_G, and R_{DB} will be extracted as a function of bias currents. Figure 5.13 shows the extracted C_{GS} and C_{GD}.

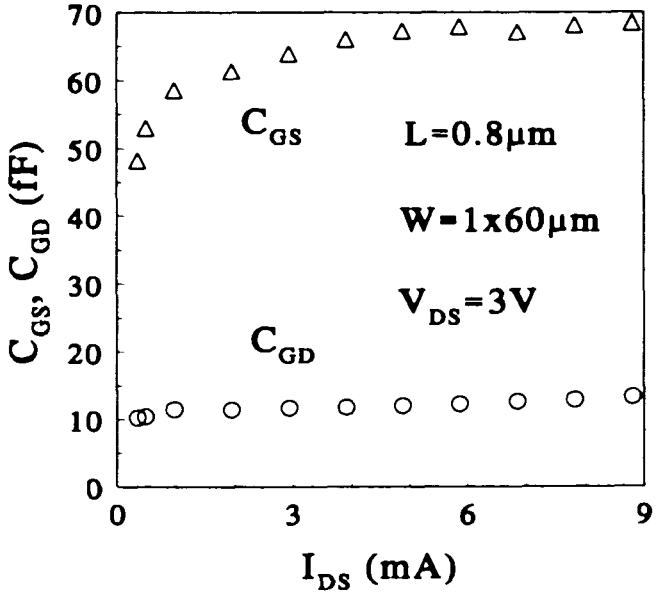


FIGURE 5.13: Extracted model parameters C_{GS} and C_{GD} of a n-type MOSFET as a function of bias current in saturation region.

It is shown that C_{GD} in saturation is the overlap capacitance C_{GDO} which should be bias independent. As for C_{GS}, when I_{DS} increase by increasing V_{GS} in saturation (at a fixed V_{DS}), the pinch-off point of conducting channel will moving towards the drain end. Therefore C_{GS} will increase with I_{DS} which increases because of the increasing V_{GS} increases. Figure 5.14 shows the extracted channel resistance R_i as a function of bias current. When I_{DS} increases, because more carriers are induced in the channel, the channel resistance decreases.

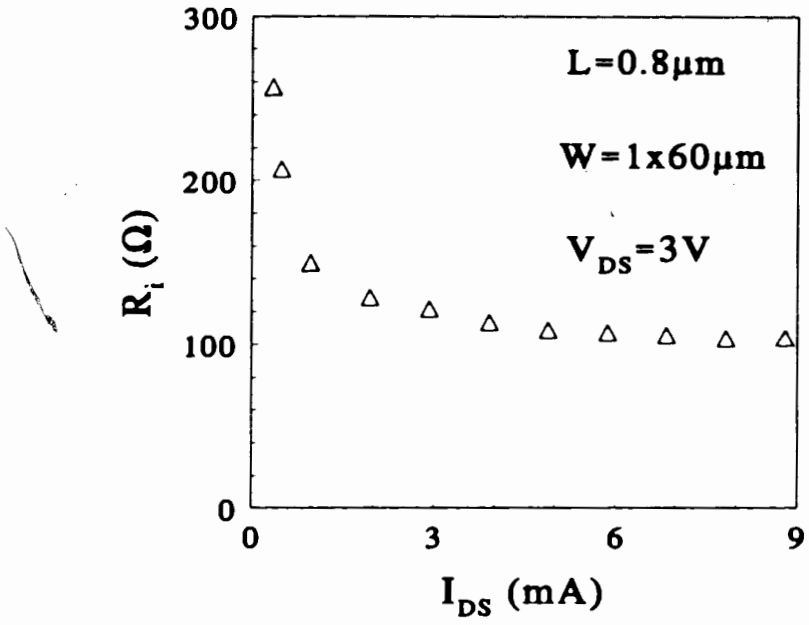


FIGURE 5.14: Extracted channel resistance R_i of a n-type MOSFET as a function of bias current in saturation region.

Beside C_{GS}, C_{GD} and R_i which are bias dependent parameters in this common-source configuration, other small-signal parameter values used in simulation which are bias independent are R_G = 175 Ω, C_{GB} = 1.4 fF, C_{DB} = 41 fF, C_{SB} = 117 fF, and R_{DB} = 320 Ω. Once all the model parameters are obtained, the noise modeling can proceed.

Chapter 6

Noise Modeling

6.1 Theory of Noisy Two-Port Networks

The noise figure, defined as the signal-to-noise ratio at the input port divided by signal-to-noise ratio at the output port, is widely used as a measure of noise performance of a two-port network. It is usually expressed in decibels. The noise figure (*NF*) is generally affected by two factors - the source (input) impedance at the input port of a network and the noise sources in the two-port network itself. In general, the noise figure of a two-port network with any arbitrary source impedance can be calculated by

$$NF = NF_{min} + \frac{R_n}{G_s} \cdot [\,(G_s - G_{opt})^2 + (B_s - B_{opt})^2\,] \tag{6.1}$$

or

$$NF = NF_{min} + \frac{4R_n|\Gamma_s - \Gamma_{opt}|^2}{(1-|\Gamma_s|^2)\cdot|1+\Gamma_{opt}|^2}; \quad \Gamma_s = \frac{R_s + jX_s - Z_o}{R_s + jX_s + Z_o} \tag{6.2}$$

where G_s is the source conductance, B_s is the source susceptance, G_{opt} is the optimized source conductance, B_{opt} is the optimized source susceptance, and Z_o is the system impedance which is 50 Ω in our system. Form (6.1) and (6.2), it is shown that the four noise parameters - the minimum noise figure NF_{min}, the optimum source (input) impedance Z_{opt} at which the NF_{min} occurs, and the equivalent noise resistance R_n, which characterizes how noise figure increases if the source impedance deviates from the optimum value - will reflect how noisy a two-port network itself will be.

A noisy two-port may be represented by a noise-free two-port and two current noise sources as shown in figure 6.1(a), and these two noise sources are usually correlated with each other.

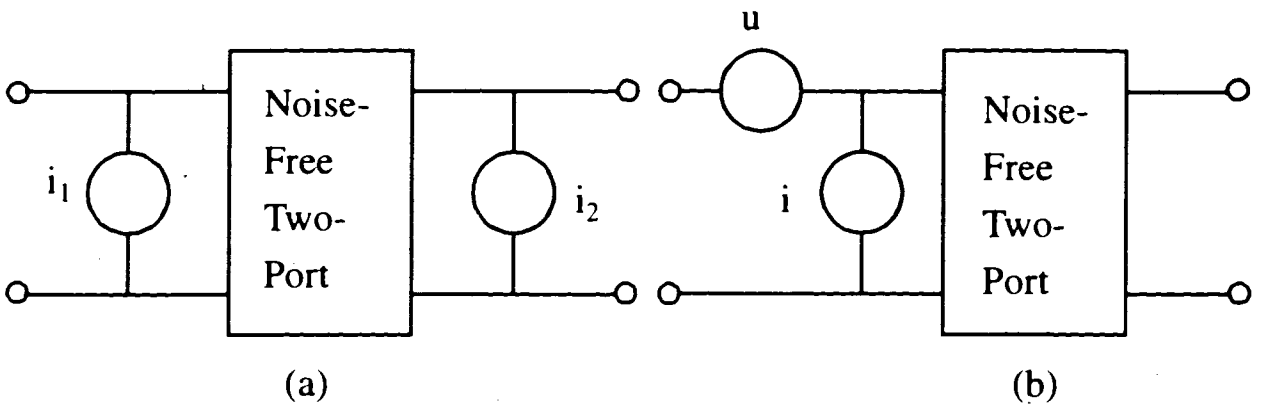


FIGURE 6.1: Different representations of noisy two-port networks

From the y-parameters of the two-port and the noise source information (i_1, i_2 and the correlation term $\overline{i_1 i_2^*}$), we may evaluate the noise parameters of the two-port by transforming the noisy two-port to a noise-free two-port with a noise current and a noise voltage sources at the input side of the two-port (figure 6.1(b)). Here, i and u and the correlation factor called Y_{cor} are calculated using

$$i = i_{un} + uY_{cor} \text{ and} \tag{6.3}$$

$$\overline{iu^*} = Y_{cor}\overline{|u|^2}, \tag{6.4}$$

where

$$u = -\frac{1}{Y_{21}} i_2, \tag{6.5}$$

$$i = i_1 - \frac{Y_{11}}{Y_{21}} i_2, \tag{6.6}$$

$$Y_{cor} = Y_{11} - Y_{21}\frac{\overline{i_1 i_2^*}}{\overline{|i_2|^2}} = G_{cor} + jB_{cor}, \tag{6.7}$$

and

$$\overline{|u|^2} = \frac{\overline{|i_2|^2}}{|Y_{21}|^2} = 4kT\Delta f R_u, \text{ and} \tag{6.8}$$

$$\overline{|i|^2} = \overline{|i_1|^2} + \overline{|i_2|^2}\left|\frac{Y_{11}}{Y_{21}}\right|^2 - 2Re\left\{\overline{i_1 i_2^*} \cdot \frac{Y_{11}^*}{Y_{21}^*}\right\} = 4kT\Delta f G_i. \tag{6.9}$$

From (6.7) to (6.9), we can calculate the four noise parameters from

$$R_n = R_u \tag{6.10}$$

$$G_{opt} = \sqrt{\frac{G_i}{R_n} - B^2_{cor}} \tag{6.11}$$

$$B_{opt} = -B_{cor} \tag{6.12}$$

$$NF_{min} = 1 + 2R_n(G_{cor} + G_{opt}) \tag{6.13}$$

By using generalized matrix approach to the noise analysis of two-port networks shown above, we can write the admittance node equations at port 1 and port 2 as

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} B \\ D \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{6.14}$$

where B = [1 0] and D = [0 1] according to the noise circuit shown in figure 6.1, and define the noise correlation matrix C [37] as

$$C = \begin{bmatrix} \overline{i_1 i_1^*} & \overline{i_1 i_2^*} & \cdots & \overline{i_1 i_n^*} \\ \overline{i_2 i_1^*} & \overline{i_2 i_2^*} & \cdots & \overline{i_2 i_n^*} \\ \overline{i_n i_1^*} & \overline{i_n i_2^*} & \cdots & \overline{i_n i_n^*} \end{bmatrix} \tag{6.15}$$

with n = 2 in the case of a two-port network. Using the y-parameters, B, C, and D matrixes defined in (6.14) and (6.15), we can calculate R_u, G_i and Y_{cor} from the following expressions [50]

$$R_u = \frac{1}{4kT\Delta f} Re\left\{ \frac{1}{|Y_{21}|^2} \times [D]^* \times [C] \times [D]^T \right\}, \tag{6.16}$$

$$G_i = \frac{1}{4kT\Delta f} Re\left\{ \left([B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^* \times [C] \times \left([B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^T \right\}, \tag{6.17}$$

$$\begin{aligned} Y_{cor} &= G_{cor} + jB_{cor} \\ &= \frac{-1}{4kT\Delta f R_n Y_{21}^*} \left\{ [D]^* \times [C] \times \left([B] - \frac{Y_{11}}{Y_{21}} \times [D] \right)^T \right\}, \end{aligned} \tag{6.18}$$

and the noise parameters can be calculated from (6.10) to (6.13).

6.2 Noise Parameter de-embedding

There are two ways to characterize the noise performance of intrinsic devices. One is a straightforward noise de-embedding technique which is similar to the s-parameter de-embedding technique described in section 5.1.1 with the same DUT and test structures used in s-parameter de-embedding. The other method is through the help of the electrical circuit equivalent pad model. In the latter method, the pad model and the intrinsic device model are combined to form the model of the DUT. Based on the model of the DUT, the

noise performance was calculated and compared against the measured noise data of the DUT. The first method is convenient for calculating the noise performance of intrinsic devices; the second method will be employed if we are also interested in optimizing the design of the probe pads [45] ~ [49]. In this section, the straightforward noise de-embedding method is introduced and the pad modeling will be described in the next section.

For the straightforward noise de-embedding, it is convenient to use the formalism of noise correlation matrices, instead of the common noise parameters NF_{min}, Z_{opt}, and R_n. This de-embedding technique presented in [40] is based on the noise power matrix introduced by Haus [36] later renamed the noise correlation matrix in [37]. In [37], various representations and transformations have been tabulated to demonstrate that the correlation matrix was ideally suited for the analysis of noise in linear two-port circuits by computer aided design. Based on the technique in [40] and the same DUT and test structures as those used in [22], the noise de-embedding procedure is as follows.

1. Measure the scattering parameters $[S^{DUT}]$, $[S^{OPEN}]$, and $[S^{SHORT}]$ of the DUT, "open", and "short" structures and convert each of them to the Y parameters $[Y^{DUT}]$, $[Y^{OPEN}]$, and $[Y^{SHORT}]$ with the conversion

$$[Y] = \frac{\begin{bmatrix} (1-S_{11})(1+S_{22})+S_{12}S_{21} & -2S_{12} \\ -2S_{21} & (1+S_{11})(1-S_{22})+S_{12}S_{21} \end{bmatrix}}{Z_o \cdot [(1+S_{11})(1+S_{22})-S_{12}S_{21}]}. \qquad (6.19)$$

2. Measure the noise parameters, $NF_{min}{}^{DUT}$, $Y_{opt}{}^{DUT}$, and $R_n{}^{DUT}$ of the DUT.

3. Calculate the correlation matrix $[C_A{}^{DUT}]$ of the DUT by the measured noise parameters using

$$\left[C_A^{DUT}\right] = 2kT\begin{bmatrix} R_n^{DUT} & \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}(Y_{opt}^{DUT})^* \\ \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}Y_{opt}^{DUT} & R_n^{DUT}\left|Y_{opt}^{DUT}\right|^2 \end{bmatrix}. \quad (6.20)$$

where k is Boltzmann's constant and T is the absolute temperature. The asterisk denotes the complex conjugate.

4. Convert the $[C_A{}^{DUT}]$ matrix to its $[C_Y{}^{DUT}]$correlation matrix with

$$\left[C_Y^{DUT}\right] = [T^{DUT}]\left[C_A^{DUT}\right][T^{DUT}]^{\dagger} \quad (6.21)$$

where $[T^{DUT}]$ is given by

$$[T^{DUT}] = \begin{bmatrix} -Y_{11}^{DUT} & 1 \\ -Y_{21}^{DUT} & 0 \end{bmatrix}. \quad (6.22)$$

$[T^{DUT}]$ only depends on the small signal parameters (here Y parameters) of the DUT and the $\dagger$ in $[T^{DUT}]^{\dagger}$ denotes Hermitian conjugation (transpose and complex conjugate).

5. Calculate the correlation matrix $[C_Y{}^{OPEN}]$ of the "open" test structure with

$$\left[C_Y^{OPEN}\right] = 2kT\Re([Y^{OPEN}]) \quad (6.23)$$

where $\Re(\ )$ stands for the real part of the elements in the matrix. The noise parameters of a passive device are fully determined by its small-signal parameters.

6. Subtract parallel parasitics from the [Y^{DUT}] and [Y^{SHORT}] with

$$[Y_I^{DUT}] = [Y^{DUT}] - [Y^{OPEN}] \tag{6.24}$$

$$[Y_I^{SHORT}] = [Y^{SHORT}] - [Y^{OPEN}]. \tag{6.25}$$

7. De-embed [C_Y^{DUT}] from the parallel parasitics with

$$\left[C_{YI}^{DUT}\right] = \left[C_Y^{DUT}\right] - \left[C_Y^{OPEN}\right]. \tag{6.26}$$

8. Convert the [Y_I^{DUT}] and [Y_I^{SHORT}] to [Z_I^{DUT}] and [Z_I^{SHORT}]with the conversion

$$[Z] = \frac{1}{Y_{11}Y_{22} - Y_{12}Y_{21}} \begin{bmatrix} Y_{22} & -Y_{12} \\ -Y_{21} & Y_{11} \end{bmatrix}. \tag{6.27}$$

9. Convert [C_{YI}^{DUT}] to [C_{ZI}^{DUT}] with

$$\left[C_{ZI}^{DUT}\right] = \left[Z_I^{DUT}\right]\left[C_{YI}^{DUT}\right]\left[Z_I^{DUT}\right]^{\dagger}. \tag{6.28}$$

10. Calculate the correlation matrix [C_{ZI}^{SHORT}] of the "short" test structure after de-embedding the parallel parasitics with

$$\left[C_{ZI}^{SHORT}\right] = 2kT\Re\left(\left[Z_I^{SHORT}\right]\right) \tag{6.29}$$

11. Subtract series parasitics from the [Z_I^{DUT}] to get the Z parameters [Z] of a intrinsic transistor with

$$[Z] = [Z_I^{DUT}] - [Z_I^{SHORT}] \tag{6.30}$$

12. De-embed $[C_{ZI}{}^{DUT}]$ from the series parasitics to get the correlation matrix $[C_Z]$ of a intrinsic transistor with

$$[C_Z] = \left[C_{ZI}^{DUT}\right] - \left[C_{ZI}^{SHORT}\right] \tag{6.31}$$

13. Convert the [Z] of a intrinsic transistor to its chain matrix [A] with the conversion

$$[A] = \frac{1}{Z_{21}}\begin{bmatrix} Z_{11} & (Z_{11}Z_{22} - Z_{12}Z_{21}) \\ 1 & Z_{22} \end{bmatrix} \tag{6.32}$$

14. Transform $[C_Z]$ to $[C_A]$ with

$$[C_A] = [T_A][C_Z][T_A]^{\dagger} \tag{6.33}$$

where $[T_A]$ is given by

$$[T_A] = \begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix} \tag{6.34}$$

15. Calculate the noise parameters, NF_{min}, Z_{opt},and R_n of a intrinsic transistor from the noise correlation matrix in chain representation $[C_A]$ with

$$NF_{min} = 1 + \frac{1}{kT}\left(\Re(C_{12A}) + \sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2}\right) \tag{6.35}$$

$$Y_{opt} = \frac{\sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2} + i\Im(C_{12A})}{C_{11A}} \tag{6.36}$$

$$R_n = \frac{C_{11A}}{2kT} \tag{6.37}$$

where $\Im(\ )$ stands for the imaginary part of the elements in the matrix and i is the imaginary unit.

The noise-parameter de-embedding technique described above assumes that the solid lines in the "short" test structure is relatively shorter than the interconnections so that its series parasitics are negligible. With the same consideration as the one in s-parameter de-embedding, the gate and drain of the transistor of the DUT (shown in figure 4.1) are right next to the signal pads and the trapezoidal part of the ground pad is designed to be as close as possible to the source of the transistor in order to reduce the parasitic resistance and inductance from the source end of a transistor to the ground pad. Based on this special design, Z_G, Z_S, and Z_D in figure 5.2 can be neglected and only the s-parameters of "open" test structure is used in the noise parameter de-embedding procedures. If only the s-parameters of "open" test structure are used, the de-embedding procedure is as follows.

1. Measure the scattering parameters $[S^{DUT}]$, and $[S^{OPEN}]$ of the DUT and the "open" structure and convert them to each Y parameters $[Y^{DUT}]$ and $[Y^{OPEN}]$ with the conversion

$$[Y] = \frac{\begin{bmatrix} (1-S_{11})(1+S_{22})+S_{12}S_{21} & -2S_{12} \\ -2S_{21} & (1+S_{11})(1-S_{22})+S_{12}S_{21} \end{bmatrix}}{Z_o \cdot [(1+S_{11})(1+S_{22})-S_{12}S_{21}]} \qquad (6.38)$$

2. Measure the noise parameters, $NF_{min}{}^{DUT}$, $Y_{opt}{}^{DUT}$, and $R_n{}^{DUT}$, of the DUT.

3. Calculate the correlation matrix $[C_A{}^{DUT}]$ of the DUT by the measured noise parameters with

$$\left[C_A^{DUT}\right] = 2kT\begin{bmatrix} R_n^{DUT} & \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}(Y_{opt}^{DUT})^* \\ \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}Y_{opt}^{DUT} & R_n^{DUT}\left|Y_{opt}^{DUT}\right|^2 \end{bmatrix} \quad (6.39)$$

where k is Boltzmann's constant and T is the absolute temperature. The asterisk denotes the complex conjugate.

4. Convert the $[C_A{}^{DUT}]$ matrix to its $[C_Y{}^{DUT}]$correlation matrix with

$$\left[C_Y^{DUT}\right] = [T^{DUT}]\left[C_A^{DUT}\right][T^{DUT}]^{\dagger} \quad (6.40)$$

where $[T^{DUT}]$ is given by

$$[T^{DUT}] = \begin{bmatrix} -Y_{11}^{DUT} & 1 \\ -Y_{21}^{DUT} & 0 \end{bmatrix} \quad (6.41)$$

$[T^{DUT}]$ only depends on the small signal parameters (here Y parameters) of the DUT and the $\dagger$ in $[T^{DUT}]^{\dagger}$ denotes Hermitian conjugation (transpose and complex conjugate).

5. Calculate the correlation matrix $[C_Y{}^{OPEN}]$ of the "open" test structure with

$$\left[C_Y^{OPEN}\right] = 2kT\Re([Y^{OPEN}]) \quad (6.42)$$

where $\Re(\ )$ stands for the real part of elements. The noise parameters of a passive device are fully determined by its small-signal parameters.

6. Subtract parallel parasitics from the $[Y^{DUT}]$ with

$$[Y_I^{DUT}] = [Y^{DUT}] - [Y^{OPEN}] \tag{6.43}$$

7. De-embed $[C_Y{}^{DUT}]$ from the parallel parasitics with

$$\left[C_{YI}^{DUT}\right] = \left[C_Y^{DUT}\right] - \left[C_Y^{OPEN}\right] \tag{6.44}$$

8. Convert the $[Y_I{}^{DUT}]$ to its chain matrix [A] with the conversion

$$[A] = \frac{-1}{Y_{21}}\begin{bmatrix} Y_{22} & 1 \\ (Y_{11}Y_{22} - Y_{12}Y_{21}) & Y_{11} \end{bmatrix} \tag{6.45}$$

9. Transform $[C_{YI}{}^{DUT}]$ to $[C_A]$ with

$$[C_A] = [T_A]\left[C_{YI}^{DUT}\right][T_A]^{\dagger} \tag{6.46}$$

where $[T_A]$ is given by

$$[T_A] = \begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix} \tag{6.47}$$

10. Calculate the noise parameters, NF_{min}, Z_{opt},and R_n, of a intrinsic transistor from the noise correlation matrix in chain representation $[C_A]$ with

$$NF_{min} = 1 + \frac{1}{kT}\left(\Re(C_{12A}) + \sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2}\right) \tag{6.48}$$

$$Y_{opt} = \frac{\sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2} + i\Im(C_{12A})}{C_{11A}} \tag{6.49}$$

$$R_n = \frac{C_{11A}}{2kT} \tag{6.50}$$

where $\Im(\,)$ stands for the imaginary part of elements and i is the imaginary unit.

6.3 Pad Modeling

Since the effects of probe pads are important in high-frequency s-parameter and noise parameter measurements, then it is important to design the probe pads to increase the accuracy of de-embedding technique. Before achieving this goal, the electrical pad model should be developed and the parameters of the circuit elements extracted from the dummy pad measurements. Figure 6.2 (a) shows the 3-D diagram of probe pads including all physical parasitic elements. Figure 6.2 (b) is the cross-section of the pad pattern from port 1. In these figures, C_1 and C_2 are the capacitances between the top metal and silicon substrate for the signal and ground pad respectively, C_3 is the capacitance between the signal pad and the ground pad, C_4 is the capacitance between these two signal pads at the input and output ports, and R_1 is the resistance of silicon substrate between the signal pads and ground pads. From figure 6.2 (b), it is found that C_1 and C_2 are connected in series (because these two ground pads are connected) and the effective capacitance is dominated by C_1, because, according to the layout, C_2 is much larger than C_1. Therefore, the 3-D model (figure 6.2 (a)) can be simplified to its equivalent model (figure 6.2 (c)) with

$$C_{sub} = C_1, \quad C_m = C_3/2, \quad C_t = C_4, \quad and \quad R_{sub} = R_1/2 \tag{6.51}$$

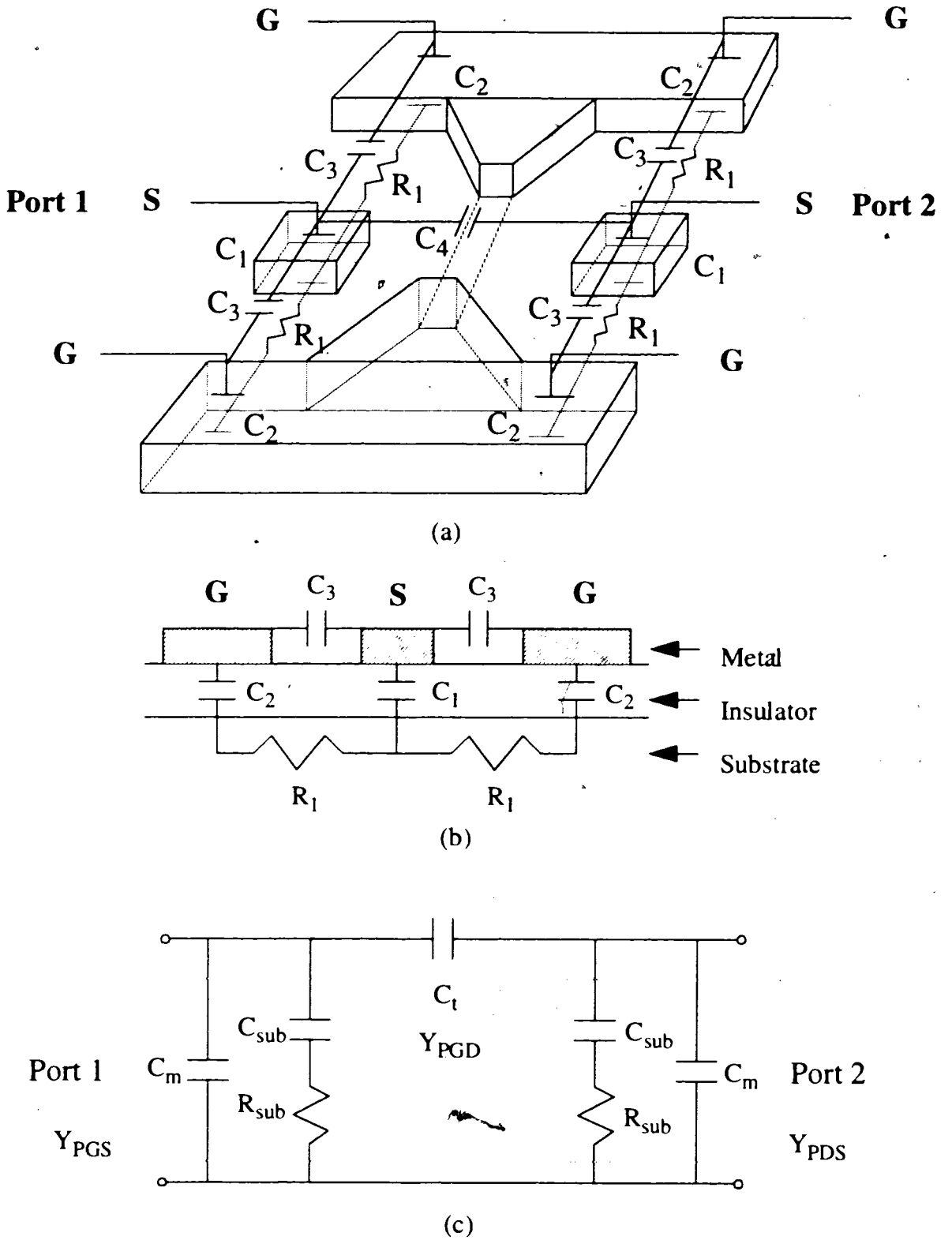


FIGURE 6.2: (a) The 3-D diagram of probe pads including all the physical parasitic components. (b) The cross-section of probe pads from port 1. (c) Equivalent electrical circuit model for the probe pads.

The s-parameters of dummy pads are first measured. Then they are converted to the y-parameters, and the parallel parasitics, Y_{PGS}, Y_{PGD}, and Y_{PDS}, given by (5.1) to (5.3) are extracted. From the equivalent circuit model, C_t can be extracted from the imaginary part of Y_{GD}, and C_m, C_{sub} and R_{sub} are extracted from optimization using the measured data of Y_{PGS} and Y_{PDS}. Figures 6.3 and 6.4 show the measured (symbols) and calculated (dash lines) data based on the parameter values C_{sub} = 25.1 fF, C_m = 19.75 fF, C_t = 2.37 fF and R_{sub} = 680 Ω.

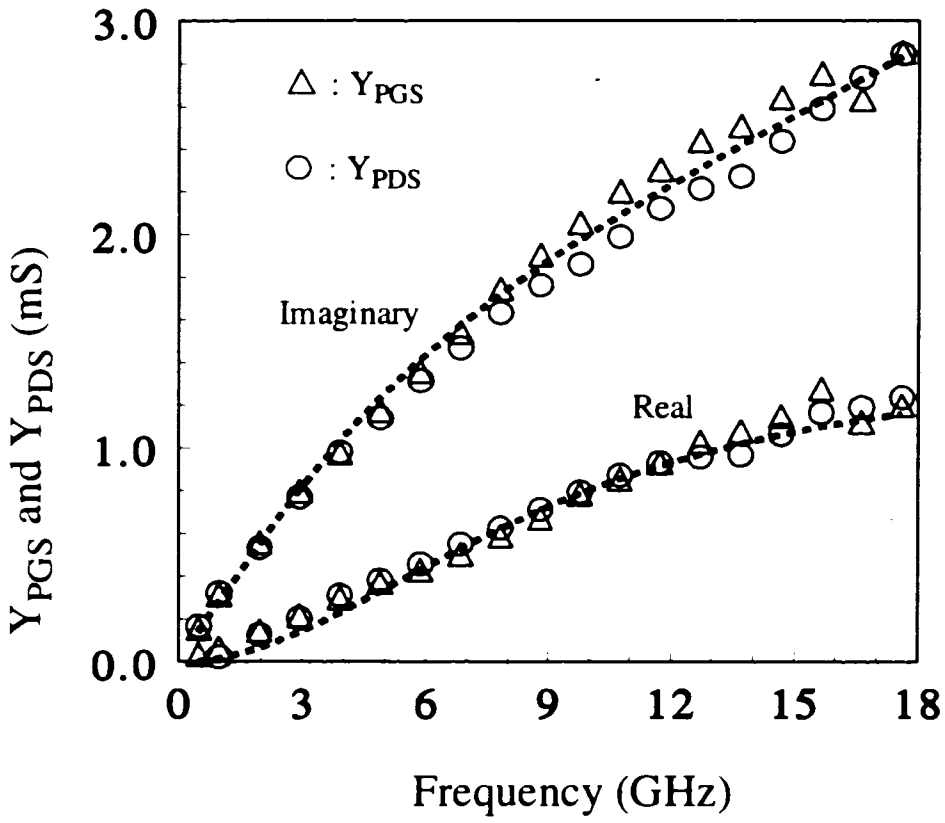


FIGURE 6.3: Measured and calculated data for Y_{PGS} and Y_{PDS}.

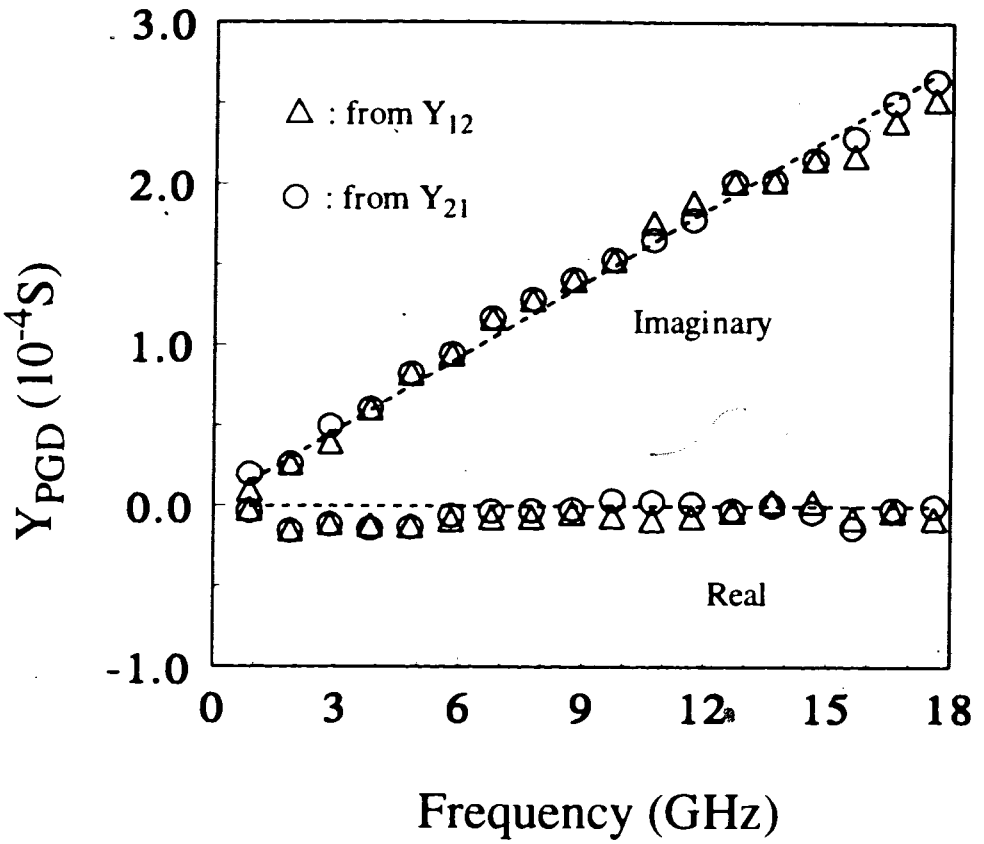


FIGURE 6.4: Measured and calculated data for Y_{PGD}.

6.4 Noise Modeling

The noise model of an intrinsic transistor consists of its small-signal model and all noise sources. Figure 6.5 shows the equivalent noise model which takes into account the following noise sources - channel noise (i_d), noise due to the gate resistance (i_G) and the resistance between the drain and bulk (i_{DB}), induced gate noise (i_g) and its correlation with i_d, thermal noise in the source (i_S) and drain (i_D) parasitic resistances.

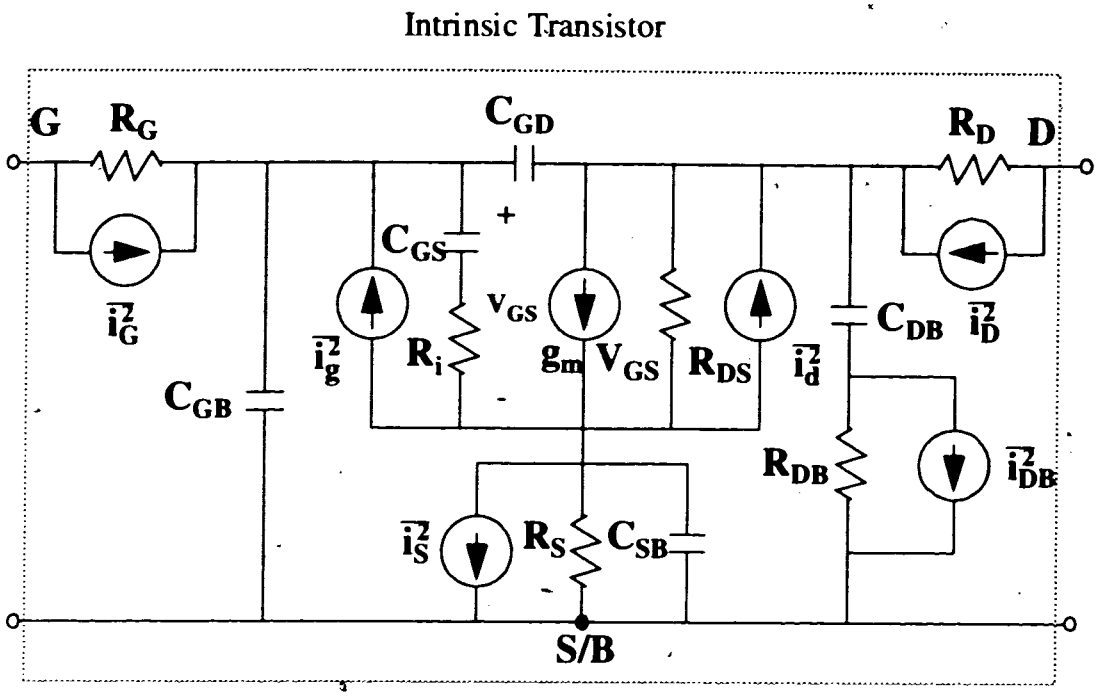


FIGURE 6.5: Equivalent noise circuit model for a intrinsic MOSFET

In this research, the intrinsic transistor model is combined with the pad model which includes the series and parallel parasitics to form a DUT model, and all the calculation comparisons to measurements will be based on the DUT model. Figure 6.6 shows the DUT model used in calculation.

After the DUT model and all model parameters were obtained, the next issue to be addressed is how to calculate the four noise parameters of the DUT. There are two ways to calculate these noise parameters. One is an analytical calculation method which adds all the noise power from each noise sources at the output port together (including the noise power from the source impedance at the input port) and divides this sum by the noise power from the source impedance. The other method is a direct calculation of noise parameters which is based on the theory of noisy two-port networks. The first method is

beneficial for the researchers who are interested in the noise effect of each parameter (e.g. R_G, f_T etc.). However, the drawback of the analytical expression is the tedious calculation procedure, and once the device model has been changed, all the previous results must be redone. Therefore, in the next section, a simplified circuit will be used for the demonstration of an analytical calculation, and the accurate calculation of noise parameters will be based on the direct calculation technique based using the DUT model.

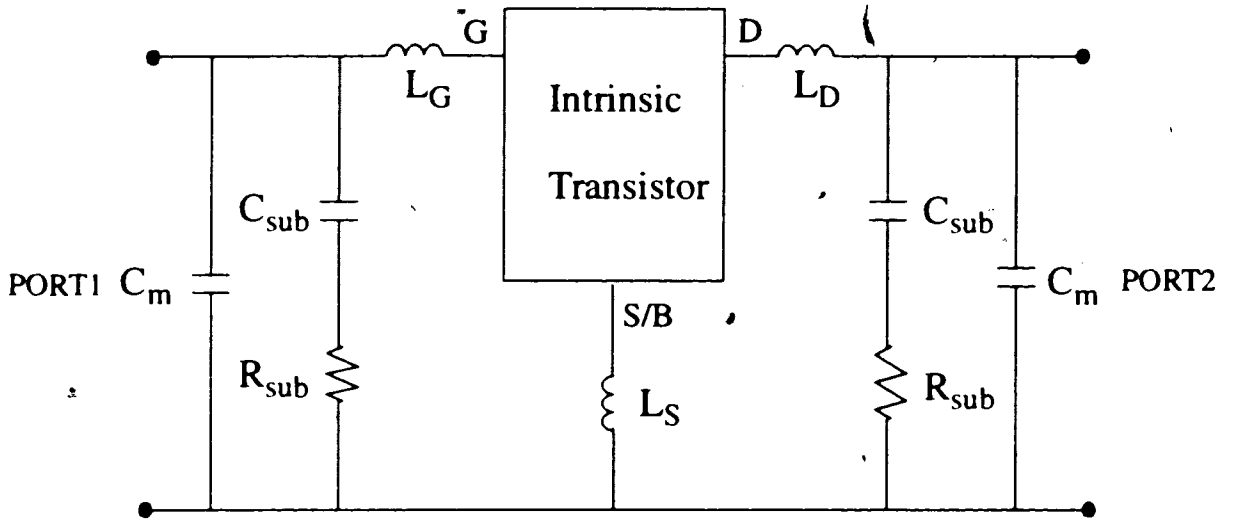


FIGURE 6.6: The DUT model consists of a intrinsic transistor model (shown in figure 6.5) and all series and parallel parasitics.

6.4.1 Analytical Expression for Noise Parameters

Figure 6.7 shows the simplified small-signal model. Based on this model, noise figure is calculated by dividing the total noise power of short-circuit noise current i_{out} at the output port from each noise source by the noise power at the output port from source impedance only. By setting the first order derivative of noise figure to zero and solving for the source resistance (R_{opt}) and reactance (X_{opt}), the solutions will be the optimized source impedance (Z_{opt}). The equivalent noise resistance can be calculated by dividing the

total noise power of short-circuit noise current i_{out} at the output port from each noise source (except the noise power from the source impedance) by the square of the magnitude of current gain. By going through the calculation, these four noise parameters can be expressed as

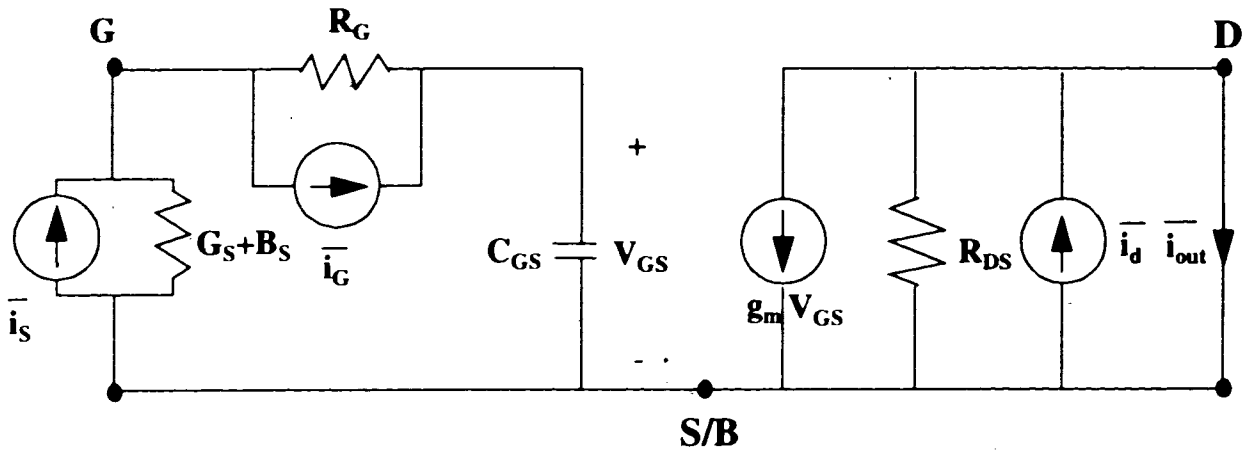


FIGURE 6.7: Simplified equivalent circuit model for analytical calculation of noise parameters.

$$NF_{min} = 1 + \frac{1}{2} R_G \omega C_{GS} i_d \cdot \frac{\omega C_{GS} i_d + \sqrt{\omega^2 C_{GS}^2 i_d^2 + i_G^2 g_m^2}}{g_m^2 kT} \tag{6.52}$$

$$R_n = \frac{1}{4kT} \cdot \left(\frac{1 + \omega^2 C_{GS}^2 R_G^2}{g_m^2} \cdot i_d^2 + R_G^2 i_G^2 \right) \tag{6.53}$$

$$G_{opt} = \frac{\omega C_{GS} R_G i_d \cdot \sqrt{\omega^2 C_{GS}^2 i_d^2 + i_G^2 g_m^2}}{i_d^2 + \omega^2 C_{GS}^2 R_G^2 i_d^2 + R_G^2 i_G^2 g_m^2} \tag{6.54}$$

$$B_{opt} = -\frac{\omega C_{GS} i_d}{i_d^2 + \omega^2 C_{GS}^2 R_G^2 i_d^2 + R_G^2 i_G^2 g_m^2} \tag{6.55}$$

and

$$Z_{opt} = \frac{1}{G_{opt} + j \cdot B_{opt}} \tag{6.56}$$

where $\omega = 2\pi f$ and f is frequency, i_d is channel noise, and i_G is the noise due to the gate resistance.

From the equations listed above, it is found that the gate resistance is very important in high frequency noise modeling.

6.4.2 Direct Calculation of Noise Parameters

Direct calculation of noise parameters uses a matrix operation based on the noisy two-port network theory [41] ~ [44]. In order to perform the matrix calculation of the noisy two-port shown in figure 6.1, we transform our noisy circuit model into its graph. Figure 6.8 shows the graph of DUT. In this graph, Y_{PGS} and Y_{PDS} are the parasitic effects of dummy pads and Y_{PGD} in the pad model in figure 6.3 is replaced by the y-parameters of the intrinsic device model.

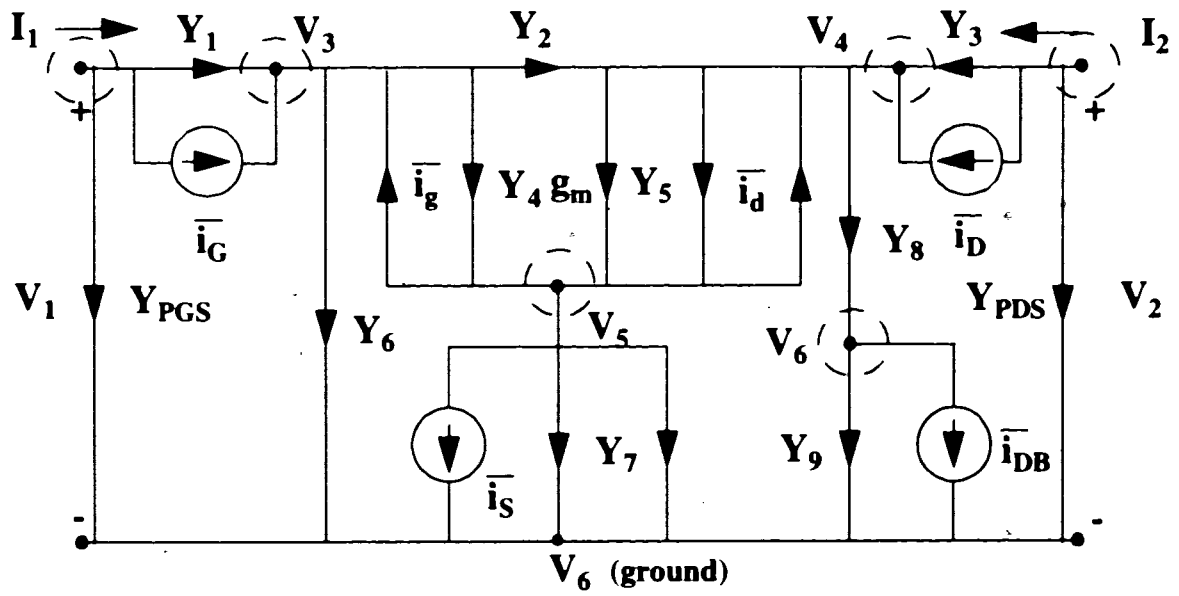


FIGURE 6.8: The graph of the equivalent noise circuit model of DUT.

Based on the graph of DUT shown in figure 6.8, we write the node equations corresponding to each node (sub-set) in a matrix form as

$$\underbrace{\begin{bmatrix} Y_1 + Y_{PGS} & 0 & -Y_1 & 0 & 0 & 0 \\ 0 & Y_3 + Y_{PDS} & 0 & -Y_3 & 0 & 0 \\ -Y_1 & 0 & Y_1 + Y_2 + Y_4 + Y_6 & -Y_2 & -Y_4 & 0 \\ 0 & -Y_3 & g_m - Y_2 & Y_2 + Y_3 + Y_5 + Y_8 & -g_m - Y_5 & -Y_8 \\ 0 & 0 & -g_m - Y_4 & -Y_5 & g_m + Y_4 + Y_5 + Y_7 & 0 \\ 0 & 0 & 0 & -Y_8 & 0 & Y_8 + Y_9 \end{bmatrix}}_{[Y]6x6} \underbrace{\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix}}_{[V]}$$

$$+ \underbrace{\begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ -1 & 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}}_{[A]6x6} \underbrace{\begin{bmatrix} i_g \\ i_d \\ i_G \\ i_S \\ i_D \\ i_{DB} \end{bmatrix}}_{[i_n]} = \begin{bmatrix} I_1 \\ I_2 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.56}$$

where

$$Y_1 = 1/(R_G + SL_G) \tag{6.57}$$

$$Y_2 = SC_{GD} \tag{6.58}$$

$$Y_3 = 1/(R_D + SL_D) \tag{6.59}$$

$$Y_4 = SC_{GS} \tag{6.60}$$

$$Y_5 = 1/R_{DS} \tag{6.61}$$

$$Y_6 = SC_{GB} \tag{6.62}$$

$$Y_7 = \frac{1}{R_S} + SC_{BS} \tag{6.63}$$

$$Y_8 = SC_{BD} \tag{6.64}$$

and

$$Y_9 = \frac{1}{R_{BD}} \tag{6.65}$$

In the above equations, S = jω and ω is the angular frequency. Once the matrix equations are formulated, the network is reduced by eliminating three nodes - node 5, 4, and 3, one by one, leaving only the input and output nodes (node 1 and node 2). For example, we eliminate the node 5 first, then each element of Y and A not in row 5 will be transformed according to the following formulas

$$Y'_{ij} = Y_{ij} - \frac{Y_{5j} \times Y_{i5}}{Y_{55}} \qquad (1 \le i < 5) \qquad (1 \le j < 5) \tag{6.66}$$

$$A'_{ij} = A_{ij} - \frac{A_{5j} \times Y_{i5}}{Y_{55}} \qquad (1 \le i < 5) \qquad (1 \le j \le 6) \tag{6.67}$$

Row 5 and column 5 are deleted from the Y matrix at the first step, however only the 5th row of A is deleted and 6 columns remain. This procedure is followed until only the input and output nodes remain, and then the Y matrix at this time is 2×2, and the A matrix is 2×6 with complex elements. Now we define the B and D matrix by

$$[A] = \begin{bmatrix} B \\ D \end{bmatrix} . \tag{6.68}$$

The correlation matrix C of our noise circuit model is

$$C = \begin{bmatrix} \overline{i_g i_g^*} & \overline{i_g i_d^*} & 0 & 0 & 0 & 0 \\ \overline{i_d i_g^*} & \overline{i_d i_d^*} & 0 & 0 & 0 & 0 \\ 0 & 0 & \overline{i_G i_G^*} & 0 & 0 & 0 \\ 0 & 0 & 0 & \overline{i_S i_S^*} & 0 & 0 \\ 0 & 0 & 0 & 0 & \overline{i_D i_D^*} & 0 \\ 0 & 0 & 0 & 0 & 0 & \overline{i_{DB} i_{DB}^*} \end{bmatrix} \tag{6.69}$$

By using (6.16) to (6.18), and (6.10) to (6.13), we can directly calculate the noise parameters of MOSFETs.

6.5 Comparison with Experiments

Based on the extracted parameters in chapter 5 and all the noise source equations in chapter 3, we compared the calculations against measurements using the direct calculation technique including the pad effects. For state-of-the-art MOSFETs with high quality gate insulator, the induced gate noise (i_g) and its correlation with the channel noise are negligible, and are therefore neglected in the calculations presented later. Figure 6.9 shows NF_{min} vs. bias characteristics at 4 GHz for different hot-electron factor n defined in (3.7) and the calculated NF_{min} based on (6.52) for n = 1. It is shown that the accurate noise modeling of MOSFETs depends on not only an accurate channel thermal noise source but also an accurate small-signal model.

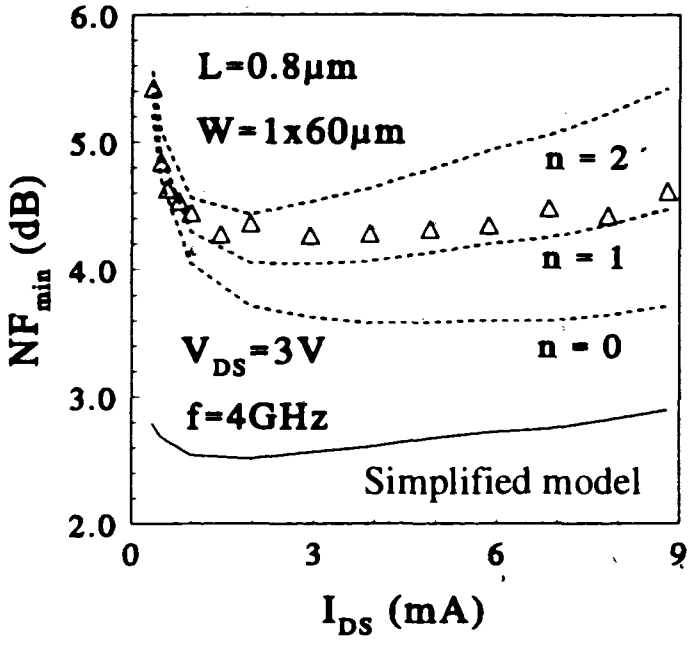


FIGURE 6.9: The measured (symbol) and calculated (lines) minimum noise figure (NF_{min}) vs. I_{DS} characteristics of a n-type MOSFET at 4 GHz for different hot-electron factor *n*. The dash line for n = 0 does not take into account the hot-electron effect. The solid line is calculated data based on (6.52) for n = 1.

From figure 6.9, several issues are shown. Fifst, the induced gate noise and its correlation with the channel noise are negligible for high-frequency noise modeling of modern MOSFETs. Second, NF_{min} is bias dependent and there is a minimum value of NF_{min} corresponding to an I_{DS} at which the device should be biased for low noise circuit design. NF_{min} decreases with increasing I_{DS} at low I_{DS}'s because g_m increases faster than i_d and C_{GS} at the lower current (see (6.52)). At higher I_{DS}'s, NF_{min} increases with I_{DS} because at higher I_{DS}'s, g_m saturates but i_d is still increasing. Third, the hot-electron effects are important in high-frequency modeling of sub-micron devices.

Figure 6.10 shows the normalized noise resistance r_n vs. bias current at 4 GHz for n = 1. The solid line is the calculations of r_n based on (6.53). It is shown that the accuracy of a small-signal model affects r_n as well.

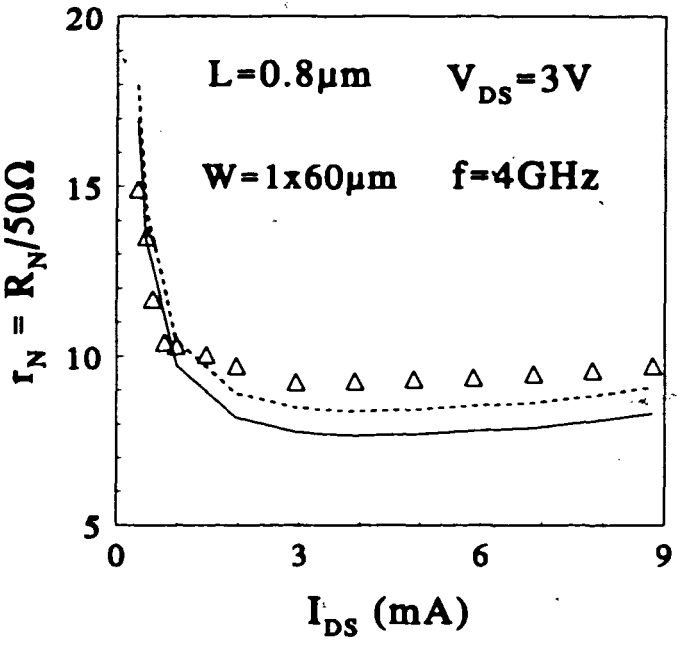


FIGURE 6.10: The measured (symbol) and calculated (lines) normalized noise resistance r_n vs. bias current characteristics of a n-type MOSFET at 4 GHz. The dash line is the calculated data for n = 1 based on the noise equivalent circuit shown in fig. 6.5 and the solid line is based on the simplified noise equivalent model shown in fig. 6.7 for n = 1.

Again, from (6.53), r_n decreases in low current region as the current increases because of the rapid increase of g_m and increases at high current region because g_m saturates but i_d still increases. From figure 6.9 and figure 6.10, the lowest position of NF_{min} and r_n occurs at ~ 3 mA. This means that the bias at which the lowest NF_{min} occurs is also the bias for the lowest r_n.

The last noise parameter we are interested in is the optimized source impedance (or reflection coefficient). Figures 6.11 and 6.12 show the measured and calculated optimized source reflection coefficient as a function of bias currents. The magnitude decreases and the phase is almost constant as the current increases. In general, good agreement between calculation and measurement for the noise parameters vs. bias current were obtained.

Now, results of noise parameters vs. frequency are presented. Figure 6.13 shows the measured and calculated NF_{min} and r_n vs. frequency characteristics from 2 GHz to 6 GHz at a bias current I_{DS} = 5 mA. In general, NF_{min} is approximately proportional to frequency, and from the measured data, it is shown that the simplified noise model shown in figure 6.7 will give a wrong prediction in the NF_{min} vs. frequency characteristics because some of the capacitive components are not included.

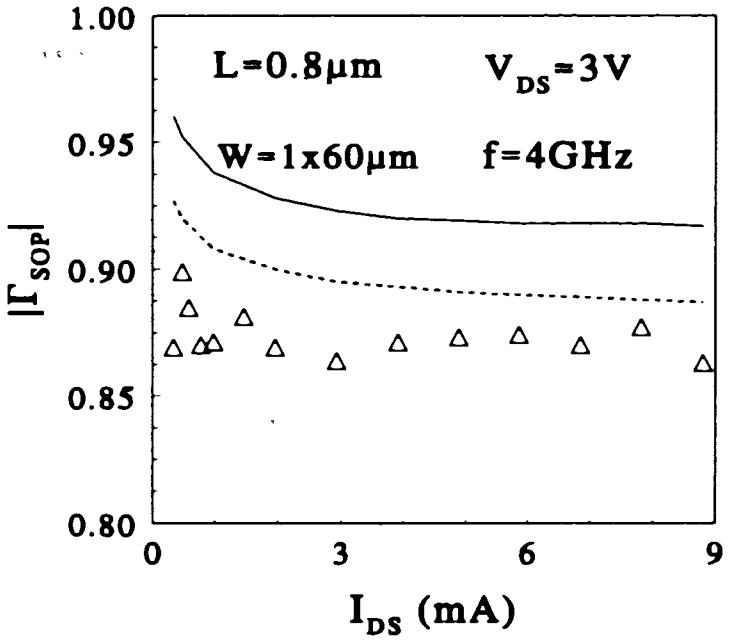


FIGURE 6.11: The measured (symbol) and calculated (lines) magnitude of optimized input reflection coefficient of a n-type MOSFET as a function of bias currents at 4 GHz. The dash line is the calculated data for n = 1 based on the noise equivalent circuit shown in fig. 6.5 and the solid line is based on the simplified noise equivalent model shown in fig. 6.7 for n = 1.

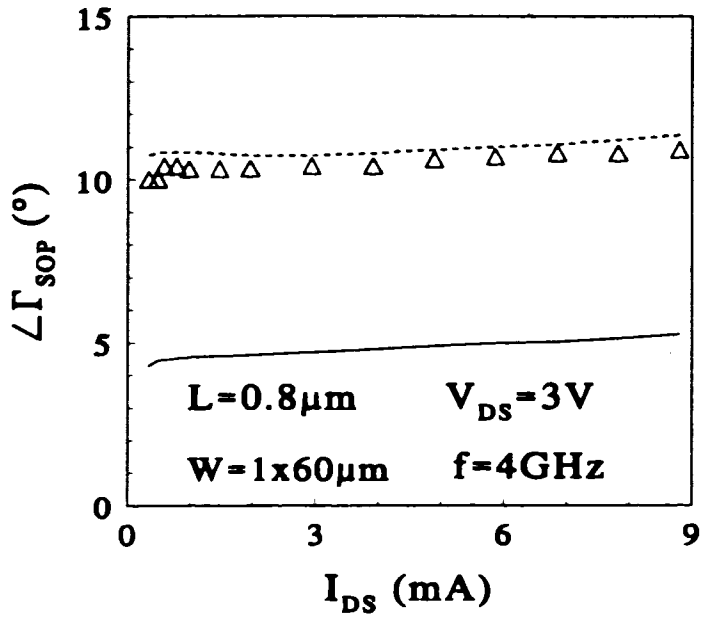


FIGURE 6.12: The measured (symbol) and calculated (lines) phase of optimized input reflection coefficient of a n-type MOSFET as a function of bias currents at 4 GHz.

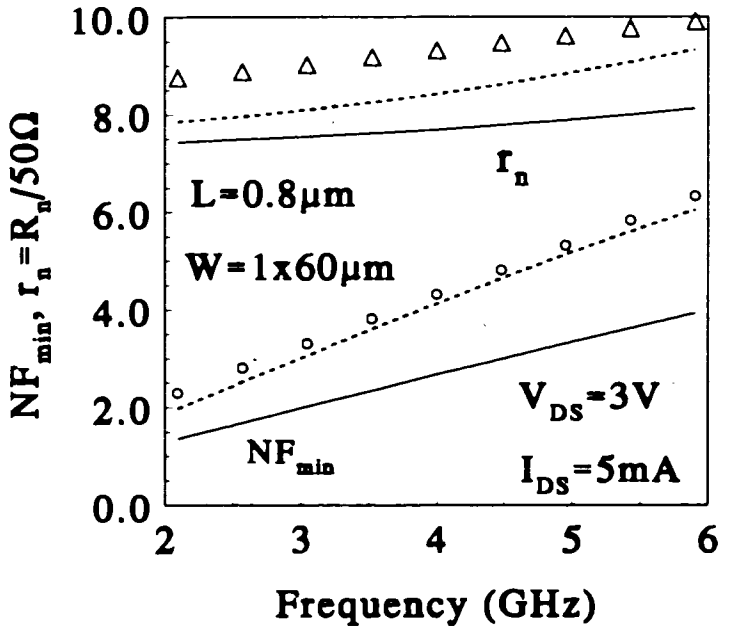


FIGURE 6.13: Measured (symbols) and calculated (dash lines) data for the minimum noise figure (NF_{min}) and normalized noise resistance (r_n) vs. frequency characteristics.

Figure 6.14 and figure 6.15 show the measured and calculated data of the magnitude and phase of the optimized source reflection coefficient at I_{DS} = 5 mA. The magnitude of optimized source reflection coefficient decreases as the frequency increases. Again, it is shown that because of the inaccuracy of the high-frequency small-signal model, the trend of noise parameter prediction is wrong.

Once good agreement between the calculations and measurements were obtained, the next interesting issues are the percentage of the noise contribution from each noise source, the probe-pad effects on the noise performance of DUT, the effect of gate resistance, and techniques to reduce the gate resistance for increasing the maximum oscillation frequency. (f_{max}) and reducing the NF_{min}.

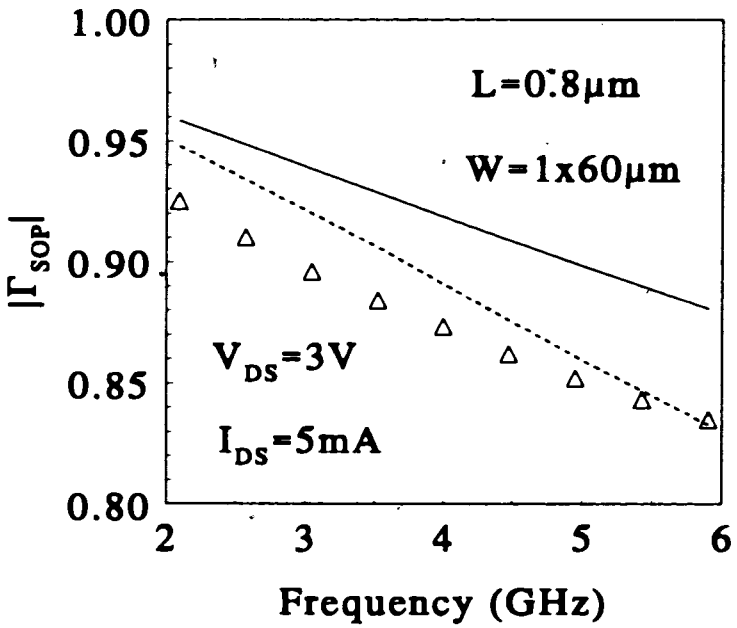


FIGURE 6.14: The measured (symbols) and calculated (dash line) for the magnitude of optimized source reflection coefficient vs. frequency characteristics. The dash line is the calculated data for n = 1 based on the noise equivalent circuit shown in fig. 6.5 and the solid line is based on the simplified noise equivalent model shown in fig. 6.7 for n = 1.

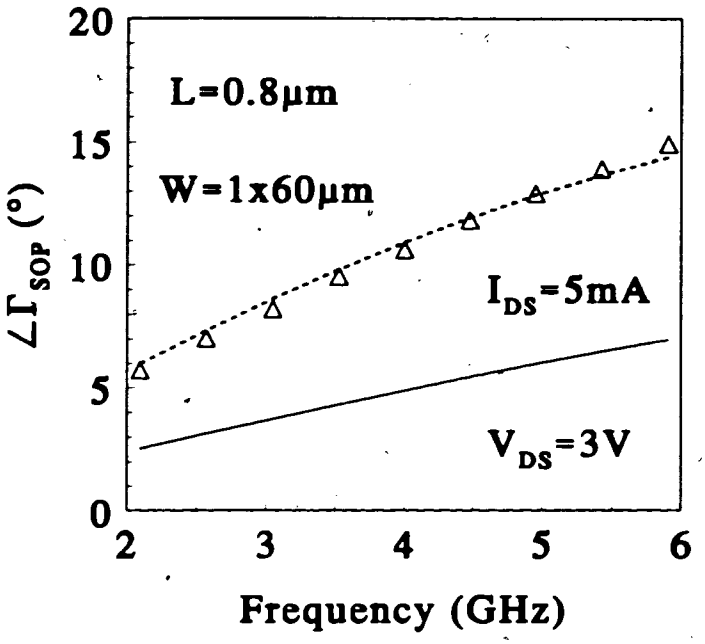


FIGURE 6.15: The measured (symbol) and calculated (lines) data for the phase of optimized source reflection coefficient vs. frequency characteristics.

6.5.1 The impact on NF_{min} from each noise source

Table 6.1 shows the importance of the noise contribution from the channel noise (i_d), the resistance between the drain and bulk (i_{DB}), and thermal noises in the gate (i_G), source (i_S) and drain (i_D) parasitic resistances respectively when the transistor is biased at V_{DS} = 3 V, I_{DS} = 2 mA, and f = 4 GHz with NF_{min} = 2.54 (4.05 dB). The noise contribution of NF_{min} corresponding each noise source in Table 6.1 is obtained by subtracting the NF_{min}, which is calculated by assuming that the corresponding noise source is zero, from 2.54. Note that this noise contribution of corresponding noise source is not the "real" contribution of NF_{min} because when one noise source is taken out of the noise circuit, it will affect the optimized source impedance which depends on the noise sources in the circuit (see (6.54) and (6.55)). This in turn affects the noise power contributions at the output port from other noise sources. So the percentage of decrease in NF_{min} in Table 6.1

will only gives us an idea of how important the corresponding noise source will be and, therefore, the sum of the percentage of decrease in NF_{min} of each noise will not be 100%. From Table 6.1, it is shown that the thermal noise from the conducting channel is the dominant noise source in the high-frequency noise modeling of MOSFETs. The noise from the gate resistance is also very important and should be carefully considered when designing low noise, high-frequency analog circuits. Note, however, that if we keep the same Z_{opt} with and without R_G in the circuit, the removal of R_G results in a 35% decrease in the noise, as shown in figure 6.16 later.

TABLE 6.1. The importance of each noise source
(V_{DS} = 3 V, I_{DS} = 2 mA, f = 4 GHz, NF_{min} = 2.542 (4.051 dB))

Noise Sources	Noise Power (10^{-23}Amp^2/Hz)	Noise Contribution of NF_{min}	% of decrease in NF_{min}
i_d	9.19	1.32	51.8
R_G	9.47	0.48	18.8
R_S	81.29	0.02	0.94
R_D	81.29	0.02	0.87
R_{DB}	5.58	0.003	0.12

Figure 6.16 demonstrates the effect of gate resistance on the NF_{min} of the DUT. It is shown that the gate resistance plays a very important role in RF noise performance of an intrinsic transistor. On the other hand, the gate resistance affects not only the overall noise performance of devices but also the maximum oscillation frequency (f_{max}) [4].

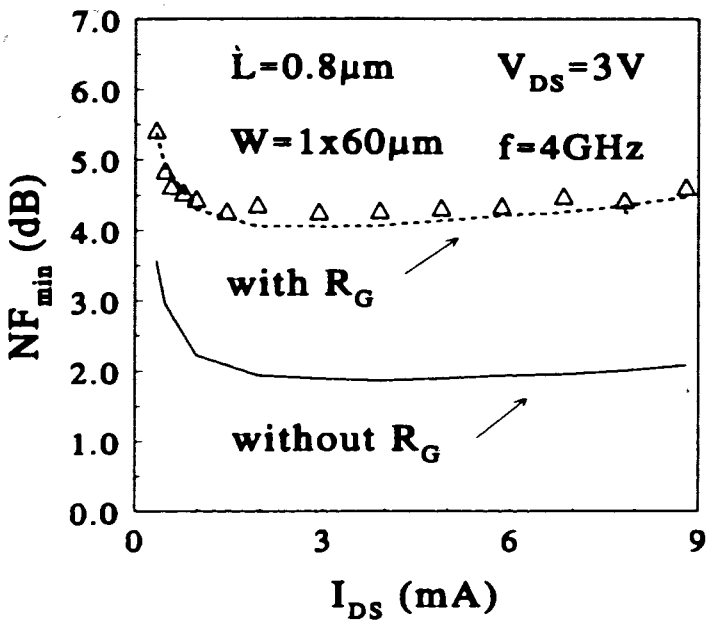


FIGURE 6.16: The effect of gate resistance on the NF_{min} of the DUT. The dash line is the calculated NF_{min} with R_G = 175 Ω and the solid line is the calculated NF_{min} with R_G = 0 Ω.

6.5.2 Intrinsic noise parameters of a MOS transistor - from direct de-embedding and pad modeling

The next issue we want to investigate is the probe-pad effects on the noise parameters and the noise parameters of intrinsic MOS transistor. So far, two kinds of techniques has been introduced. One is the direct de-embedding procedure described in section 6.2, and the other is the pad de-embedding through the pad modeling.

By using (6.38) to (6.50), we directly de-embedded the pad effects from the measured noise parameters of a 0.8 μm/ 60 μm transistor. Figures 6.17 and 6.18 show the measured and de-embedded NF_{min} and R_n as a function of bias currents at 4 GHz. The triangles are the measured parameters with the probe-pad effect, the solid circles are the intrinsic parameters obtained from the direct de-embedding procedure, and the dash lines

are the intrinsic parameters obtained from the pad modeling. In this research, the probe-pads are 60 μm long and 50 μm wide and it is shown that the probe pads will increase NF_{min} (~ 0.5 dB) but they do not affect R_n. The difference in NF_{min} between the solid circles and the dash line is about 0.2 dB, and it is mainly caused by the accuracy of the small-signal model.

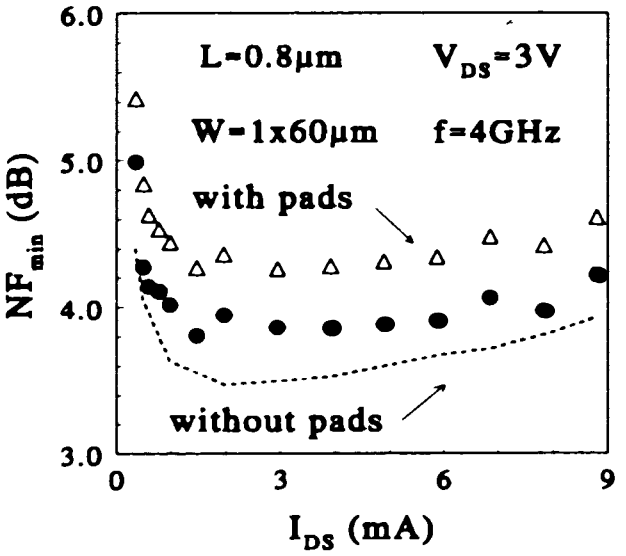


FIGURE 6.17: The measured and de-embedded NF_{min} of a 0.8 μm n-type MOSFET with 60 μm channel width as a function of bias currents.

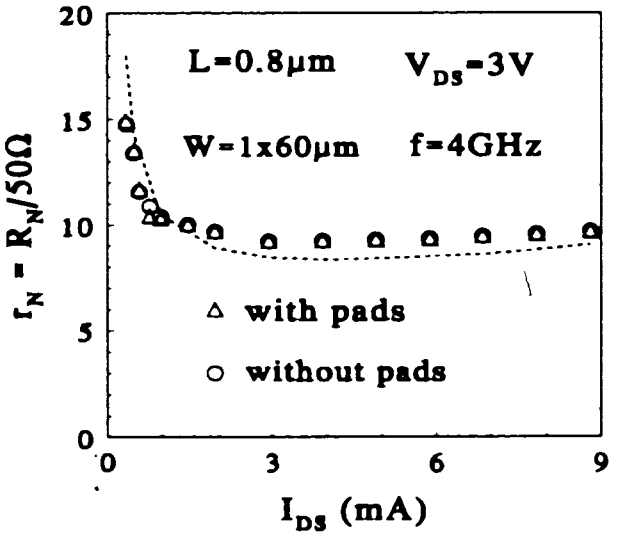


FIGURE 6.18: The measured and de-embedded R_n of a 0.8 μm n-type MOSFET with 60 μm channel width as a function of bias currents.

Figures 6.19 and 6.20 show the measured and de-embedded Γ_{opt} vs. bias current characteristics. It is shown that the probe pad will increase the magnitude (~ 0.01) and decrease the phase (~ 4 °) of the Γ_{opt} of the transistor at 4 GHz.

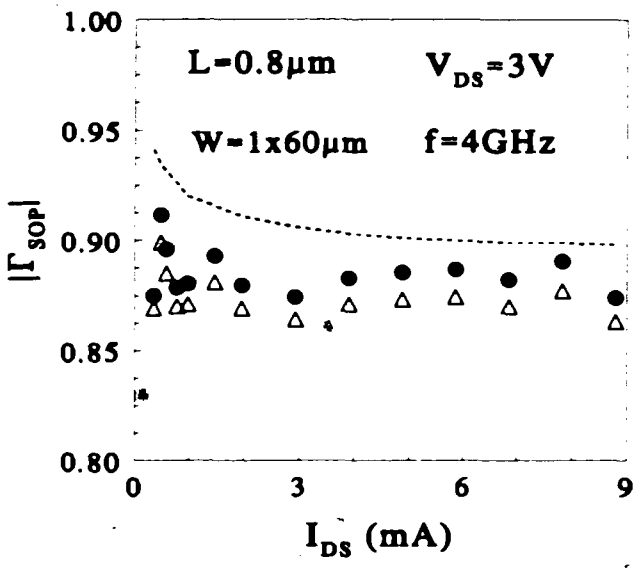


FIGURE 6.19: The measured and de-embedded $|\Gamma_{opt}|$ of a 0.8 μm n-type MOSFET with 60μm channel width as a function of bias currents at 4GHz.

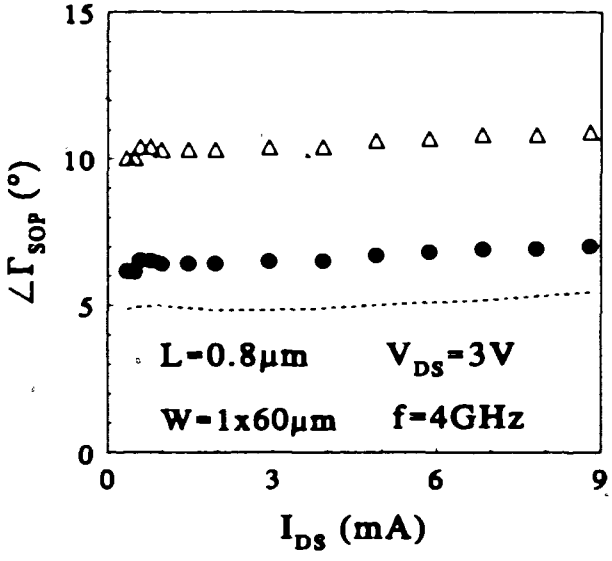


FIGURE 6.20: The measured and de-embedded angle of Γ_{opt} of a 0.8μm n-type MOSFET as a function of bias currents at 4 GHz.

Figures 6.21 and 6.22 show the measured and de-embedded NF_{min} and R_n vs. frequency characteristics at I_{DS} = 5 mA. It is shown that the pad effect on NF_{min} and R_n is frequency dependent, but again it does not have too much influence on R_n.

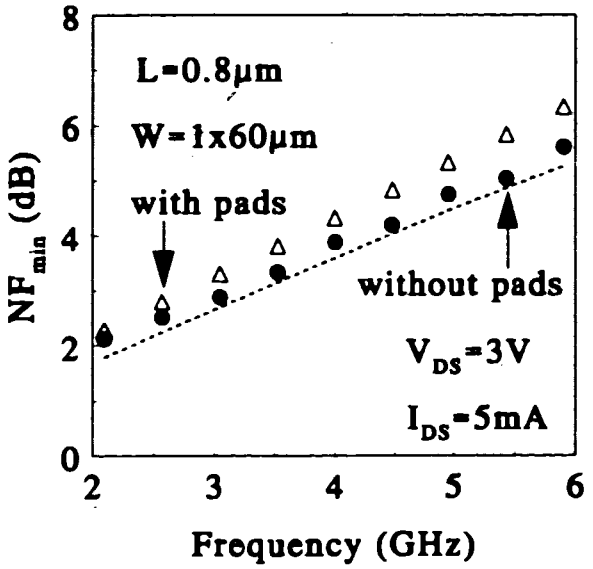


FIGURE 6.21: The measured and de-embedded NF_{min} of a 0.8 μm n-type MOSFET with 60 μm channel width as a function of frequencies at I_{DS} = 5 mA.

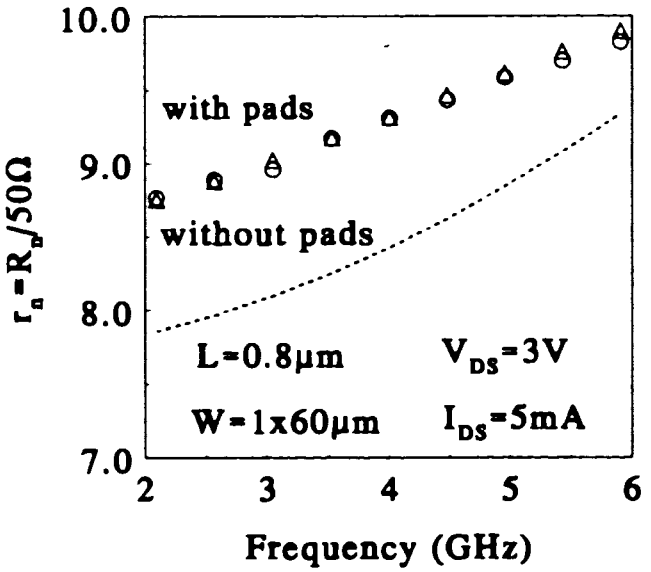


FIGURE 6.22: The measured and de-embedded R_n of a 0.8 μm nNOSFET with 60 μm channel width as a function of frequencies at I_{DS} = 5 mA.

Figures 6.23 and 6.24 show the measured and de-embedded Γ_{opt} as a function of frequencies at I_{DS} = 5 mA. It is shown that the pad effect on the Γopt is frequency dependent as well.

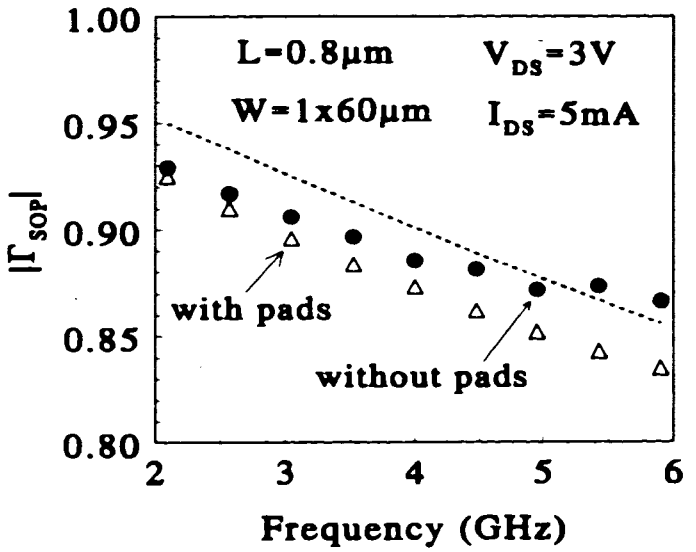


FIGURE 6.23: The measured and de-embedded $|\Gamma_{opt}|$ of a 0.8 μm nNOSFET with 60 μm channel width as a function of frequencies at I_{DS} = 5 mA.

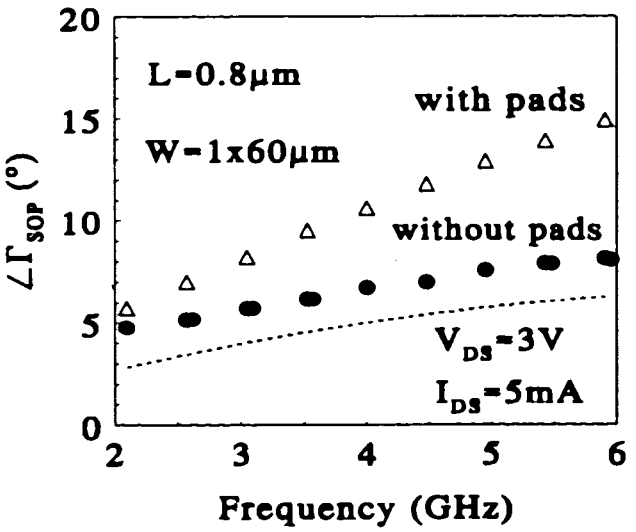


FIGURE 6.24: The measured and de-embedded angle of Γ_{opt} of a 0.8 μm nNOSFET with 60 μm channel width as a function of frequencies at I_{DS} = 5 mA.

6.6 Noise Performance and Modeling of Multi-Finger Gate Design

In order to increase f_{max} by reducing R_G, two approaches were investigated. One involves metal-reinforced gates [51][52] and the other employs the multi-finger design technique. The first approach reduces the R_{GSH} so as to reduce R_G and increase f_{max}. This approach can achieve the goals of reducing the overall noise level and increasing the f_{max} but requires a change to the fabrication process. The multi-finger gate design in which some narrower devices are connected in parallel to reduce R_G based on the existing technology will increase not only f_{max} but also improve the overall noise performance. In general, the maximum oscillation frequency f_{max} can be expressed as

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_{GSH}W^2}{L_g n^2}(g'_{ds} + 2\pi f_T C'_{gd}) + g_{ds}(R_i + R_s)}} \tag{6.70}$$

where L_g is the channel length, W is the channel width, n is the number of fingers, R_{GSH} is the sheet resistance, $g_{ds} = g'_{ds}W$, $C_{gd} = C'_{gd}W$, $R_G = R_{GSH}W/(n^2L_g)$, and $f_T = g_m/2\pi(C_{gs}+C_{gd})$ [4]. From (6.70), it is shown that the gate resistance R_G is proportional to the inverse of the numbers of gate fingers. Figure 6.25 shows the measured NF_{min} of a 60 μm transistor and a multi-finger gate design in which there are six 10 μm transistors connected in parallel. The calculated data of NF_{min} for the 1×60 μm transistor is based on RG = 175Ω and the R_G value for the calculation of NF_{min} for the 6×10 μm transistor is 175 Ω/36. It is shown that the multi-finger gate design will decrease the overall noise performance by decreasing the gate resistance R_G. Also, good agreement between the measured and calculated NF_{min} of multi-finger gate design is obtained.

The noise model and direct calculation technique presented in the thesis can predict not only for our measured devices that were fabricated in 0.8 μm BiCMOS technology,

but also for published data. In order to confirm the accuracy of our model of multi-finger designs, we compared our calculations with the measurements published in [4]. In this comparison, the parameter values we used in the calculations are - L = 0.5 μm, W = 4×10 μm, g_m = 2.282 mS, R_G = 60 Ω, R_S = 15.3 Ω, R_D = 15.3 Ω, R_{DS} = 3.23 kΩ, C_{GS} = 42 fF, and C_{GD} = 11 fF - and they were either taken directly from the figures in [4], or from appropriate scaling of a 0.8 μm BiCMOS technology. Figure 6.26 shows the characteristics of NF_{min} and R_n vs. frequency. Without de-embedding the noise contribution of the probing pads from the noise measurements causes the small difference in NF_{min} between the measured data (symbols) and the calculations (lines). Figure 6.27 shows the $|\Gamma_{sop}|$ vs. frequency characteristics. In general, good prediction was obtained, even though pad parasitics were neglected.

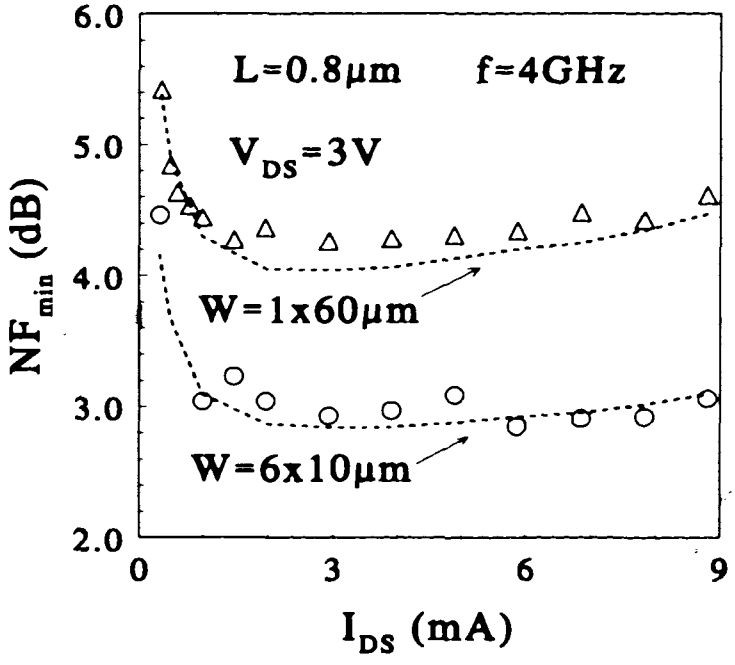


FIGURE 6.25: The measured (symbols) and calculated (dash lines) NF_{min} of a single 60 μm transistor (triangle) and a multi-finger gate design (circle) with six 10 μm transistors connected in parallel. The calculated data for multi-finger gate design is obtained by changing R_G to R_G/n^2 (n = 6 in this calculation) and the rest of model parameters are the same as those used in the noise calculation for the single 60 μm transistor.

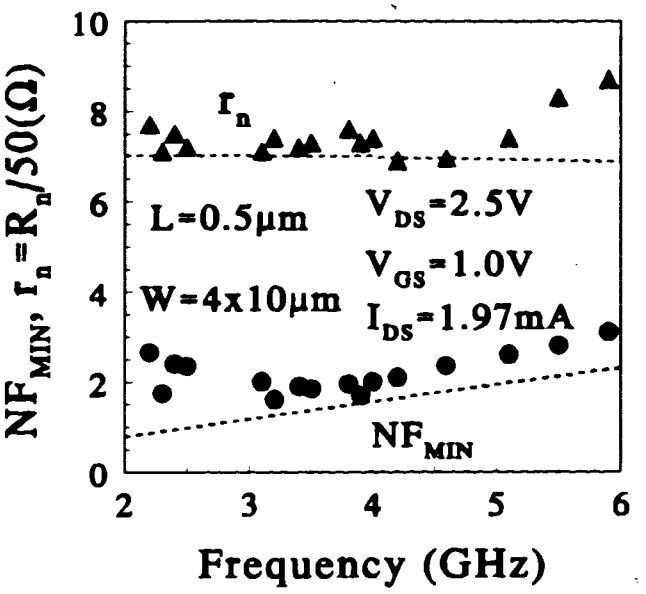


FIGURE 6.26: The characteristics of NF_{min} and R_n vs. frequency. The lines are calculations based on the model presented here, and the symbols are data from [4].

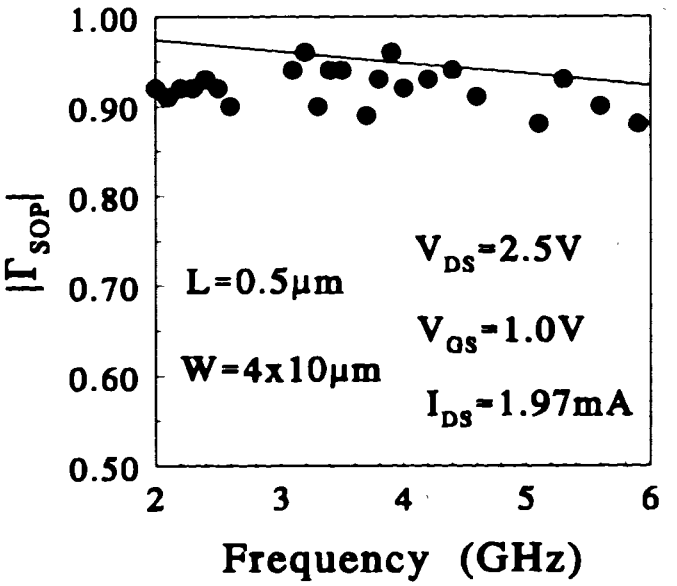


FIGURE 6.27: $|\Gamma_{sop}|$ vs. frequency characteristics. The line is calculation based on the model presented here, and the symbols are data from [4].

6.7 Comparison of Different Noise Models

Finally, several noise models for channel thermal noise were compared. Figure 6.28 shows the calculated data for different channel thermal models. It is shown that the HSPICE level 3 (NLEV < 3) and BSIM3 (NLEV < 3) models tends to saturate in the high current region and underestimate the channel thermal noise. As for HSPICE level 3 (NLEV = 3) model, it is based on (8.5.16) in [14] which does not take into account the velocity saturation effect. Therefore, it gives lower noise prediction for intrinsic transistors. In addition, it is observed that Wang et al.'s model [16] overestimates the channel thermal noise in the high current region compared to the other modes. This is because the model in [16] included the velocity saturation effect based on the noise expression (see (8) in [16]) which is (8.5.16) in [14]. If we include the velocity saturation effect at the very beginning when the noise expression is derived, the channel noise expression we end up with (3.16) which is the proposed model based on Van der Ziel noise expressions in [5], and it gives reasonable noise prediction. Figure 6.29 shows the measured and calculated NF_{min} vs. I_{DS} for different noise models. It is shown that the HSPICE level 3 model (NLEV < 3) gives a wrong trend for NF_{min} vs. I_{DS} characteristics and is unsuitable for low noise RF circuit designs.

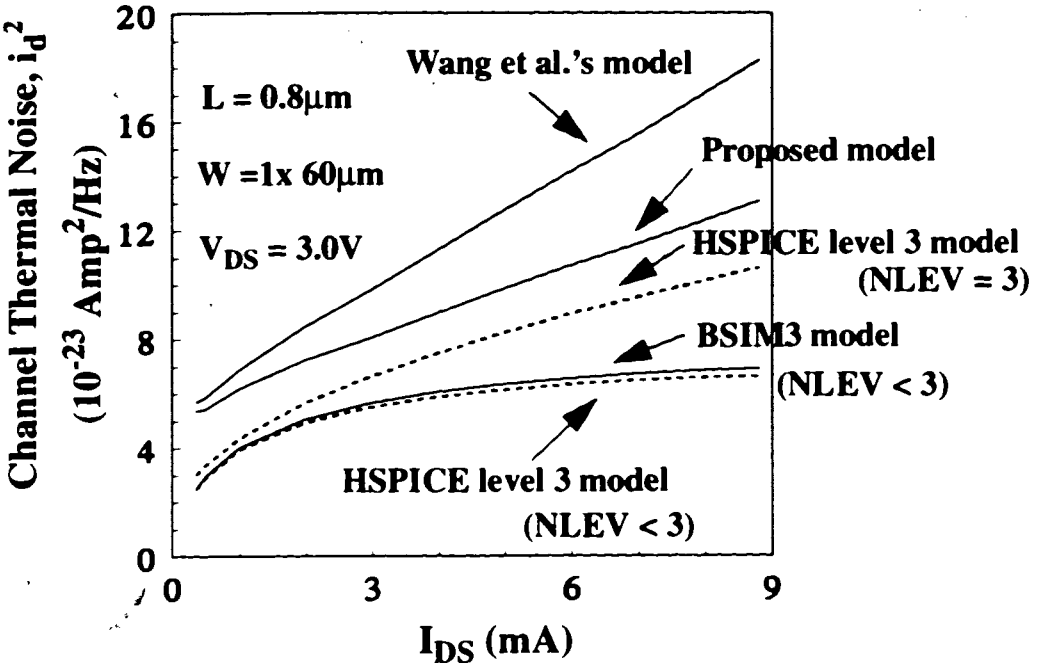


FIGURE 6.28: Calculated power spectral density of channel thermal noise for different models.

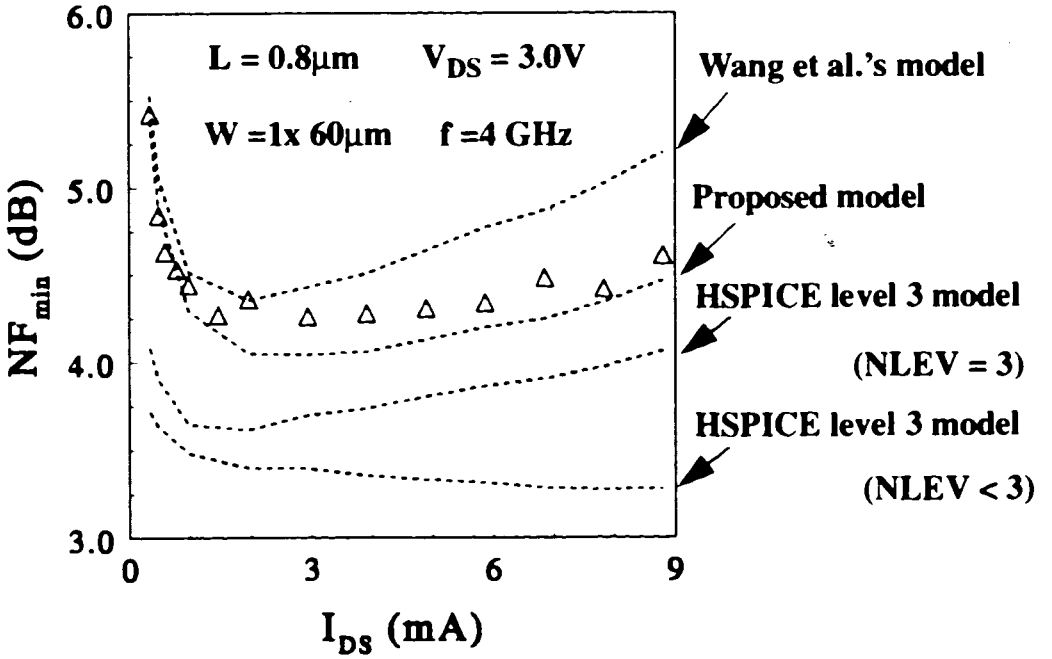


FIGURE 6.29: Measured (symbol) and calculated (dashed lines) NF_{min} vs. I_{DS} for different noise models.

Chapter 7

Conclusions and Recommendations

High-frequency noise characteristics of modern MOSFETs are becoming increasingly important in high-frequency circuit design. In this research, the origin of different noise sources and various noise models for the thermal noise in the conducting channel have been introduced. Hot-carrier effects and velocity saturation effects are two very important effects which have to be taken into account for the noise modeling of sub-micron transistors. Among the noise models described, the model based on Van der Ziel's channel thermal model gives a better noise prediction and it is proven by experiments that the induced gate noise and its correlation with the channel thermal noise are negligible in high-frequency noise modeling for modern devices that were fabricated in 0.8 μm BiCMOS technology and only the noise caused by the DC current has to be taken into account. On the other hand, from the equation of channel thermal noise, an accurate high-frequency noise modeling for intrinsic transistors relies on an accurate DC modeling as well. Therefore, without an accurate DC model, it is not possible to accurately to predict the noise performance.

High-frequency test structures and de-embedding techniques used for both s-parameters and noise parameters are two critical requirements in noise measurements and modeling. In this thesis, the design of dummy pads and DUT are described. An appropriate de-embedding technique has also been explained in detail. In general, the parallel parasitics of probe-pads can be easily de-embedded by the subtraction of the measured y-parameters of an "open" test structure from the measured y-parameters of the DUT. However, the series parasitics caused by the interconnections between probe-pads

and the intrinsic transistors will be difficult to de-embed from the intrinsic transistor because very wide transistors are usually designed for the investigation of high-frequency characteristics, especially for MOSFETs. Therefore, the "short" dummy pads and the corresponding de-embedding technique used for BJTs are not suitable for de-embedding the series parasitics in DUT of MOSFETs. In this research, the gate and drain contacts are right beside the probe-pads and the ground pads are brought to the source/substrate contact as close as possible to reduce the series parasitics, and only the "open" test structure was used in the parasitic de-embedding.

The DC model as well as AC model are required for noise modeling of MOSFETs. In this thesis, a small-signal model for the prediction of high-frequency characteristics has been developed. In this model, the gate resistance R_G, the high-frequency channel resistance R_i and the substrate resistance R_{sub} are found to be very important in the RF modeling of intrinsic MOSFETs. Based on the optimization technique, all the small-signal model parameters are extracted from either DC or s-parameter measurements and are used in the calculation of the noise parameters.

Noise parameters (minimum noise figure, equivalent noise resistance, and optimized source impedance) are the noise indicators of a noisy two-port network. Based on a sophisticated small-signal model which can predict accurately the high-frequency performance of devices, it is usually very difficult to obtain analytical expressions for the noise parameters based on the fundamental definition of noise parameters. In this thesis, the technique of direct calculation of noise parameters based on matrix operation was used for calculating the noise parameters of intrinsic transistors. Based on the DUT model which consists of an intrinsic transistor model and dummy pad model, extracted parameter values, and the direct calculation technique, all noise parameters are calculated and

compared to measured data as a function of bias condition and frequency. In general, good agreement was obtained.

The impact of gate resistance affects not only the maximum oscillation frequency (f_{max}) but also the overall noise performance of devices. In this thesis, the multi-finger gate design in which there are six 10 μm wide transistors connected in parallel to reduce R_G based on the existing technology improves the overall noise performance.

Finally, all the AC model parameters are extracted from the de-embedded s-parameters based on an optimization technique. However, choosing the initial values of parameters is very critical and some of the extracted parameter values can sometimes be physically meaningless. Therefore, the investigation of direct extraction of AC equivalent circuit parameters of MOSFETs is recommended. In addition, the investigation of the optimized number of fingers for a specified channel width should be researched.

References

[1] Guillermo Gonzalez, "Microwave Transistor Amplifiers Analysis and Design", Prentice-Hall, Inc., New Jersey, 1984.

[2] Y. Taur, S. Wind, Y.J. Mii, Y. Lii, D. Moy, K.A. Jenkins, C.L. Chen, P.J. Coane, D. Klaus, J. Bucchignano, M. Rosenfield, M.G.R. Thomson, and M. Polcari, "High Performance 0.1μm CMOS Devices with 1.5V Power Supply", IEDM Tech. Dig., pp. 127 - 130, 1993.

[3] Hisayo Sasaki Momose, Eiji Morifuji, Takashi Yoshitomi, Tatsuya Ohguro, Masanobu Saito, Toyota Morimoto, Yasuhiro Katsumata, and Hiroshi Iwai, "High-Frequency AC Characteristics of 1.5nm Gate Oxide MOSFETs", IEDM Tech. Dig., pp. 105- 108, 1996.

[4] S. P. Voinigescu, S. W. Tarasewicz, T. MacElwee, and J. Ilowski, "An Assessment of the State-of-the-Art 0.5μm Bulk CMOS Technology for RF Applications," Proc. IEDM-95, pp.721-724, 1995.

[5] A. van der Ziel, "Noise in Solid State Devices and Circuits", Chaps. 5-8, John Wiley & Sons, 1986.

[6] A.L. McWhorter, "1/f Noise and Germanium Surface Properties", Semiconductor Surface Physics. Philadelphia: Univ. of Pennsylvania Press, p.207, 1957.

[7] F.N. Hooge, "1/f Noise", Physica, vol. 83B, p. 14, 1976.

[8] K.Y. Toh, P.K. Ko, and R.G. Meyer, "An Engineering Model for Short-Channel MOS Devices", IEEE J. Solid-State Circuits, vol. 23, no. 4, pp. 950-958, Aug. 1988.

[9] C.G. Sodini, P.K. Ko, and J.L. Moll, "The Effect of High Fields on MOS Device and Circuit Performance', IEEE Trans. Electron Devices, vol. 31, no. 10, Oct. 1984.

[10] K.K. Hung, P.K. Ko, C. Hu, and Y.C. Cheng, "A Physics-Based MOSFET Noise Model for Circuit Simulators", IEEE Trans. Electron Devices, vol. 37, no. 5, pp. 1323-1333, May 1990.

[11] M.J. Deen ad Z.X. Yan, "A New Method of Measuring the Threshold Voltage for Small Geometry MOSFETs from Subthreshold Conduction", Solid-State Electronics, Vol 33(5), pp. 503-512, May 1990.

[12] A. Raychaudhuri, J. Kolk, M.J. Deen and M.I.H. King, "A Simple Method to Extract the Asymmetry in Parasitic Source and Drain Resistances from Measurements on a MOS Transistor", IEEE Trans. Electron Devices, vol. 42(7), pp. 1388-1390, July 1995.

[13] "HSPICE User's Manual", vol II, chap. 16, p18, Meta-Software, Inc., 1996.

[14] Yannis P. Tsividis, "Operation and Modeling of the MOS Transistor", McGraw-Hill, Inc., 1987.

[15] A. Raychaudhuri, M.J. Deen, M.I.H. King and J. Kolk, "Finding the Asymmetric Parasitic Source and Drain Resistances from the A.C. Conductances of a Single MOS Transistor", Solid-State Electronics, vol. 39(6), pp. 909-913 (June 1996).

[16] Bing Wang, James R. Hellums, and Charles G. Sodini, "MOSFET Thermal Noise Modeling for Analog Integrated Circuits", IEEE J. Solid-State Circuits, vol 29, no. 7, pp. 833-835, July 1994.

[17] A. van der Ziel, "Solid State Physical Electronics", 3rd ed., pp. 446-453, Prentice-Hall, Englewood Cliffs, NJ, 1976.

[18] J.A. Geurst, "Calculation of High-frequency Characteristics of Thin-film Transistors", Solid-State Electronics, vol 8, pp. 88-90, 563-566, 1965.

[19] Arya Raychaudhuri, "Modeling and Simulation of Saturating Hot Electron Degradation in LDD NMOSFETs - from Early Mode to Late Mode", P.h.D. thesis, chap. 3, Simon Fraser University, 1996.

[20] Behzad Razavi, Ran-Hing Yan, and Kwing F. Lee, "Impact of Distributed Gate Resistance on the Performance of MOS Devices", IEEE Trans. Circuits and Systems - I, vol. 41, no. 11, pp. 750-754, November 1994.

[21] P.J. van Wijnen, H.R. Claessen and E.A. Wolsheimer, "A New Straightforward Calibration and Correction Procedure for "On wafer" High Frequency S-Parameter Measurements (45 MHz - 18 GHz)", IEEE BCTM, pp. 70-73, 1987.

[22] M.C.A.M. Koolen, J.A.M. Geelen and M.P.J.G. Versleijen, "An Improved De-embedding Technique for On-wafer High-frequency Characterization", IEEE Bipolar Circuits and Technology Meeting, pp. 188-191, 1991.

[23] Seonghearn Lee, Byung R. Ryum, and Sang Won Kang, "A New Parameter Extraction Technique for Small-Signal Equivalent Circuit of Polysilicon Emitter Bipolar Transistors", IEEE Trans. Electron Devices, vol. 41, no. 2, pp. 233-238, February 1994.

[24] A.R. Alvarez, "BiCMOS Technology and Applications", 2nd ed., p. 78, Kluwer Academic Publishers, 1993.

[25] Robert M. Fox, "Comments on Circuit Models for MOSFET Thermal Noise", IEEE Journal of Solid-State Circuits, vol. 28, no. 2, February 1993.

[26] Suharli Tedja, Jan Van der Spiegel, Hugh H. Williams, "Analytical and Experimental Studies of Thermal Noise in MOSFET's", IEEE Trans. Electron Devices, vol. 41, no. 11, November 1994.

[27] R. Castello, F. Montecchi, R. Alini, and A. Baschirotto, "A Very Linear BiCMOS Transconductor for High-frequency Filter Applications", Proc. ISCAS pp. 1364-1367, 1990.

[28] Y. Tsividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C Filters in VLSI", IEEE J. Solid-State Circuits, vol. 21, no. 1, pp. 15-30, February 1986.

[29] "BSIM3v3 Manual", Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

[30] Paul A. Layman, and Savvas G. Chamberlain, "A Compact Thermal Noise Model for the Investigation of Soft Error Rates in MOS VLSI Digital Circuits", IEEE J. Solid-State Circuits, vol. 24, no. 1, pp. 79-89, February 1989.

[31] Dimitris P. Triantis, Alexios N. Birbas, and D. Kondis, "Thermal Noise Modeling for Short-Channel MOSFET's", IEEE Trans. Electron Devices, vol. 43, no. 11, pp. 1950- 1955, November 1996.

[32] S.M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons, Inc. p. 46, 1985.

[33] A.A. Abidi, "High Frequency Noise Measurements on FET's with Small Dimensions", IEEE Trans. Electron Devices, vol. ED-33, no. 11, pp. 1801-1805, November 1986.

[34] V. Adamian and A. Uhlir Jr., "A Novel Procedure for Receiver Noise Characterization", IEEE Trans. on Instrumentation and Measurement, vol. IM-22, no. 2, pp. 181-182, June 1973.

[35] V. Adamian and A. Uhlir Jr., "Simplified Noise Evaluation of Microwave Receivers", IEEE Trans. on Instrumentation and Measurement, vol. IM-33, no. 2, pp. 136-140, June 1984.

[36] H.A. Haus and R.B. Adler, "Circuit Theory of Linear Noisy Networks", New York, Technology Press of MIT and Wiley, 1959.

[37] H. Hillbrand H. and P.H. Russer, "An Efficient Method for Computer-Aided Noise Analysis of Linear Amplifier Networks", IEEE Trans. Circuit Syst., vol. CAS-23, pp. 235-238, April 1976.

[38] Pospieszalski M., "On the Measurement of Noise Parameters of Microwave Two-Port", IEEE Trans. on Microwave Theory Tech., vol. MTT-34, no. 4, pp. 456-458, April 1986.

[39] Robert A. Pucel, Wayne Struble, Robert Hallgren, and Ulrich L. Rohde, "A General Noise De-embedding Procedure for Packaged Two-Port Linear Active Devices", IEEE Trans. Microwave Theory Tech., vol. 40, no. 11, pp. 2013-2024, November 1992.

[40] K. Aufinger and J. Böck, "A Straightforward Noise De-embedding Method and Its Application to High-Speed Silicon Bipolar Transistors", Proceedings of ESSDERC'96, pp. 957-960.

[41] C.H. Chen and M.J. Deen, "Direct Calculation of the MOSFET High Frequency Noise Parameters" Journal of Vacuum Science and Technology, 1997 (in press).

[42] C.H. Chen, M.J. Deen, "Direct Calculation of the MOSFET High Frequency Noise Parameters", Proceedings of the 14th International Conference on Noise in Physical Systems and 1/f Fluctuations, Leuven, Belgium, Eds. C. Claeys and E. Simoen, World Scientific Publishing, Singapore, pp. 488-491 (14-18 July, 1997).

[43] C.H. Chen and M.J. Deen, "Direct Calculation of the MOSFET High Frequency Noise Parameters", Eight Canadian Semiconductor Technology Conference, p. 147, Ottawa, Canada (12-15 August, 1997).

[44] M. Ebrahim Mokari and William Patience, "A New Method of Noise Parameter Calculation Using Direct Matrix Analysis," IEEE Trans. on Circuits and Systems - I: Fundamental Theory and Applications, vol. 39, no. 9, Sep. 1992.

[45] M.J. Deen and J. Ilowski, "Modelling of Bonding Pads and Their Effect on the High-Frequency-Noise Figure of Polysilicon Emitter Bipolar Junction Transistors", Canadian Journal of Physics, vol. 74, pp.s200-s204, 1996.

[46] M.J. Deen, "High Frequency Noise Modelling and the Scaling of the Noise Parameters of Polysilicon Emitter Bipolar Junction Transistors", Canadian Journal of Physics, Vol. 74, pp. S195-S199 (1996).

[47] M.J. Deen and J.J. Ilowski, "Microwave Noise Characterization of Poly-Emitter Bipolar Junction Transistors", IEE Electronics Letters, Vol 29(8), pp. 676-677 (15 April, 1993).

[48] M.J. Deen, "Analytical Modelling, Scaling and Bonding Pad Effects on the High Frequency Noise in Bipolar Junction Transistors", Proceedings of the 8th Asia Pacific Microwave Conference (APMC'96), Ed. R.S. Gupta, New Delhi, India, INVITED PAPER, pp. 551-556 (17-20 December 1996).

[49] M.J. Deen, "Issues in Modelling the High Frequency Noise Parameters of Polysilicon Emitter Bipolar Junction Transistors", Proceedings of the First International Conference on Unsolved Problems of Noise (UPON '96), Szeged, Hungary, 6 pages (3-7 September 1996).

[50] M. Ebrahim Mokari and William Patience, "A New Method of Noise Parameter Calculation Using Direct Matrix Analysis," IEEE Trans. on Circuits and Systems - I: Fundamental Theory and Applications, vol. 39, no. 9, Sep. 1992.

[51] A. K. Agarwal, T. J. Smith, M. H. Hanes, R. L. Messham, M. C. Driver, and H. C. Nathanson, "MICROXTH - An Affordable Silicon MMIC Technology", Workshop on Silicon RF Technologies, MTT-Symposium, May 1995.

[52] P. R. de la Houssaye, C. E. Chang, B. Offord, G. Imthurn, R. Johnson, P. M. Asbeck, G. A. Garcia, and I. Lagnado, "Microwave Performance of Optically Fabricated T-Gate Thin Film Silicon-on-Sapphire Based MOSFETs," IEEE Electron Device Lett., vol. 16, pp.289-291, 1995.

Appendix A

MATHCAD Program for Calculating the H_{21} and MAG of an Intrinsic Transistor

This programm is used to calculate the current gain (H21), maximum stable gain (MSG) and maximum available gain (MAG) in dB and outout the data to the files "h21.prn", "msg.prn" and "mag.prn".

Enter the information for the following three lines...

$MEAS := READPRN(nf1w69p6)$ Data file for the measurements

$PAD := READPRN(dumpad)$ Data file for the dummy pads

$n := 0, 1 .. rows(PAD) - 1$ Number of frequency points

Characteristic impedance:

$Z_0 := 50 \cdot ohm \qquad Y_0 := \frac{1}{Z_0}$

S parameters of pads and devices ---------- from measurements

$f_{meas_n} := MEAS_{(n,0)}$

$m_{s11\_meas_n} := MEAS_{(n,1)}$

$\theta_{s11\_meas_n} := MEAS_{(n,2)}$

$m_{s21\_meas_n} := MEAS_{(n,3)}$

$\theta_{s21\_meas_n} := MEAS_{(n,4)}$

$m_{s12\_meas_n} := MEAS_{(n,5)}$

$\theta_{s12\_meas_n} := MEAS_{(n,6)}$

$m_{s22\_meas_n} := MEAS_{(n,7)}$

$\theta_{s22\_meas_n} := MEAS_{(n,8)}$

S parameters of the measured data (including pads and devices)

$$S_{11\_meas_n} = m_{s11\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s11\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s11\_meas_n}}{180} \cdot \pi \right) \right)$$

$$S_{21\_meas_n} = m_{s21\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s21\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s21\_meas_n}}{180} \cdot \pi \right) \right)$$

$$S_{12\_meas_n} = m_{s12\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s12\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s12\_meas_n}}{180} \cdot \pi \right) \right)$$

$$S_{22\_meas_n} = m_{s22\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s22\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s22\_meas_n}}{180} \cdot \pi \right) \right)$$

S parameters of dummy pads

$$f_{pad_n} = PAD_{(n,0)}$$

$$m_{s11\_pad_n} = PAD_{(n,1)}$$

$$\theta_{s11\_pad_n} = PAD_{(n,2)}$$

$$m_{s21\_pad_n} = PAD_{(n,3)}$$

$$\theta_{s21\_pad_n} = PAD_{(n,4)}$$

$$m_{s12\_pad_n} = PAD_{(n,5)}$$

$$\theta_{s12\_pad_n} = PAD_{(n,6)}$$

$$m_{s22\_pad_n} = PAD_{(n,7)}$$

$$\theta_{s22\_pad_n} = PAD_{(n,8)}$$

$$S_{11\_pad_n} = m_{s11\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s11\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s11\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{21\_pad_n} = m_{s21\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{12\_pad_n} = m_{s12\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{22\_pad_n} = m_{s22\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) \right)$$

De-embedding the pad effects:

$$Y_{11\_meas_n} = Y_o \cdot \frac{\left(1 - S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) + S_{12\_meas_n} \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{12\_meas_n} = Y_o \cdot \frac{-2 \cdot S_{12\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{21\_meas_n} = Y_o \cdot \frac{-2 \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{22\_meas_n} = Y_o \cdot \frac{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 - S_{22\_meas_n}\right) + S_{12\_meas_n} \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{11\_pad_n} = Y_o \cdot \frac{\left(1 - S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{12\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{12\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{21\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{22\_pad_n} = Y_o \cdot \frac{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{11\_extr_n} = Y_{11\_meas_n} - Y_{11\_pad_n}$$

$$Y_{12\_extr_n} = Y_{12\_meas_n} - Y_{12\_pad_n}$$

$$Y_{21\_extr_n} = Y_{21\_meas_n} - Y_{21\_pad_n}$$

$$Y_{22\_extr_n} = Y_{22\_meas_n} - Y_{22\_pad_n}$$

$$S_{11\_extr_n} = \frac{\left(Y_o - Y_{11\_extr_n}\right)\cdot\left(Y_o + Y_{22\_extr_n}\right) + Y_{12\_extr_n}\cdot Y_{21\_extr_n}}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

$$S_{12\_extr_n} = \frac{-2\cdot Y_{12\_extr_n}\cdot Y_o}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

$$S_{21\_extr_n} = \frac{-2\cdot Y_{21\_extr_n}\cdot Y_o}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

$$S_{22\_extr_n} = \frac{\left(Y_o + Y_{11\_extr_n}\right)\cdot\left(Y_o - Y_{22\_extr_n}\right) + Y_{12\_extr_n}\cdot Y_{21\_extr_n}}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

Calculate the current gain: H_{21} in dB

$$H_{21\_extr_n} = \frac{-2\cdot S_{21\_extr_n}}{\left(1 - S_{11\_extr_n}\right)\cdot\left(1 + S_{22\_extr_n}\right) + S_{12\_extr_n}\cdot S_{21\_extr_n}}$$

Current Gain: H_{21} in dB

$$WRITEPRN(H21) = \left(f_{meas_n}\ \ 20\cdot\log\left(\left|H_{21\_extr_n}\right|\right)\right)$$

Maximum Stable Gain (MSG) : $|S_{21}| / |S_{12}|$ in dB

$$WRITEPRN(MSG) = \left(f_{meas_n}\ \ 10\cdot\log\left(\frac{\left|S_{21\_extr_n}\right|}{\left|S_{12\_extr_n}\right|}\right)\right)$$

Maximum Available Gain (MAG): in dB

$$\Delta_n = S_{11\_extr_n}\cdot S_{22\_extr_n} - S_{12\_extr_n}\cdot S_{21\_extr_n} \qquad K_n = \frac{1 - \left(\left|S_{11\_extr_n}\right|\right)^2 - \left(\left|S_{22\_extr_n}\right|\right)^2 + \left(\left|\Delta_n\right|\right)^2}{2\cdot\left|S_{12\_extr_n}\cdot S_{21\_extr_n}\right|}$$

$$WRITEPRN(MAG) = \left[f_{meas_n}\ \ 10\cdot\log\left[\left|\frac{\left|S_{21\_extr_n}\right|}{\left|S_{12\_extr_n}\right|}\cdot\left[K_n - \sqrt{\left(K_n\right)^2 - 1}\right]\right|\right]\right]$$

Appendix B

MATHCAD Program for Direct De-Embedding the Parasitic Pad Effects from the Measured Scattering and Noise Parameters

(B.1) S-Parameter De-embedding

This programm is used to de-embed the pad effect from the measured data in order to get the intrinsic S parameters of devices.

Enter the information for the following three lines...

MEAS = READPRN(nf1w69p6) Data file for the measurements

PAD = READPRN(dumpad) Data file for the dummy pads

n = 0, 1 .. rows(PAD) - 1 Number of frequency points

Characteristic impedance:

$Z_o = 50$ $Y_o = \frac{1}{Z_o}$

S parameters of pads and devices ---------- from measurements

$f_{meas_n} = MEAS_{(n,0)}$

$m_{s11\_meas_n} = MEAS_{(n,1)}$

$\theta_{s11\_meas_n} = MEAS_{(n,2)}$

$m_{s21\_meas_n} = MEAS_{(n,3)}$

$\theta_{s21\_meas_n} = MEAS_{(n,4)}$

$m_{s12\_meas_n} = MEAS_{(n,5)}$

$\theta_{s12\_meas_n} = MEAS_{(n,6)}$

$m_{s22\_meas_n} = MEAS_{(n,7)}$

$\theta_{s22\_meas_n} = MEAS_{(n,8)}$

S parameters of the measured data (including pads and devices)

$$S_{11\_meas_n} = m_{s11\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s11\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s11\_meas_n}}{180} \cdot \pi \right) \right)$$

$$S_{21\_meas_n} = m_{s21\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s21\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s21\_meas_n}}{180} \cdot \pi \right) \right)$$

$$S_{12\_meas_n} = m_{s12\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s12\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s12\_meas_n}}{180} \cdot \pi \right) \right)$$

$$S_{22\_meas_n} = m_{s22\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s22\_meas_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s22\_meas_n}}{180} \cdot \pi \right) \right)$$

S parameters of dummy pads

$$f_{pad_n} = PAD_{(n,0)}$$

$$m_{s11\_pad_n} = PAD_{(n,1)}$$

$$\theta_{s11\_pad_n} = PAD_{(n,2)}$$

$$m_{s21\_pad_n} = PAD_{(n,3)}$$

$$\theta_{s21\_pad_n} = PAD_{(n,4)}$$

$$m_{s12\_pad_n} = PAD_{(n,5)}$$

$$\theta_{s12\_pad_n} = PAD_{(n,6)}$$

$$m_{s22\_pad_n} = PAD_{(n,7)}$$

$$\theta_{s22\_pad_n} = PAD_{(n,8)}$$

$$S_{11\_pad_n} = m_{s11\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s11\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s11\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{21\_pad_n} = m_{s21\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{12\_pad_n} = m_{s12\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{22\_pad_n} = m_{s22\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) \right)$$

De-embedding the pad effects:

$$Y_{11\_meas_n} = Y_o \cdot \frac{\left(1 - S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) + S_{12\_meas_n} \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{12\_meas_n} = Y_o \cdot \frac{-2 \cdot S_{12\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{21\_meas_n} = Y_o \cdot \frac{-2 \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{22\_meas_n} = Y_o \cdot \frac{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 - S_{22\_meas_n}\right) + S_{12\_meas_n} \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{11\_pad_n} = Y_o \cdot \frac{\left(1 - S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{12\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{12\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{21\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{22\_pad_n} = Y_o \cdot \frac{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{11\_extr_n} = Y_{11\_meas_n} - Y_{11\_pad_n}$$

$$Y_{12\_extr_n} = Y_{12\_meas_n} - Y_{12\_pad_n}$$

$$Y_{21\_extr_n} = Y_{21\_meas_n} - Y_{21\_pad_n}$$

$$Y_{22\_extr_n} = Y_{22\_meas_n} - Y_{22\_pad_n}$$

$$S_{11\_extr_n} = \frac{\left(Y_o - Y_{11\_extr_n}\right)\cdot\left(Y_o + Y_{22\_extr_n}\right) + Y_{12\_extr_n}\cdot Y_{21\_extr_n}}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

$$S_{12\_extr_n} = \frac{-2\cdot Y_{12\_extr_n}\cdot Y_o}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

$$S_{21\_extr_n} = \frac{-2\cdot Y_{21\_extr_n}\cdot Y_o}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

$$S_{22\_extr_n} = \frac{\left(Y_o + Y_{11\_extr_n}\right)\cdot\left(Y_o - Y_{22\_extr_n}\right) + Y_{12\_extr_n}\cdot Y_{21\_extr_n}}{\left(Y_{11\_extr_n} + Y_o\right)\cdot\left(Y_{22\_extr_n} + Y_o\right) - Y_{12\_extr_n}\cdot Y_{21\_extr_n}}$$

(B.2) Noise Parameter De-embedding

This programm is used to de-embed the pad effect from the measured data in order to get the noise parameters of intrinsic devices.

Enter the information for the following three lines...

MEAS = READPRN(nf1w69p0) Data file for the measured s-parameters

NOISE = READPRN(noise9p0) Data file for the measured noise parameters

PAD = READPRN(dumpad) Data file for the dummy pads

n = 0, 1.. 8 Number of frequency points

Characteristic impedance:

$Z_o = 50$ $Y_o = \frac{1}{Z_o}$ $k = 1.38066\,10^{-23}$ $T = 300$

S parameters of pads and devices

$f_{meas_n} = MEAS_{(n,0)}$

$m_{s11\_meas_n} = MEAS_{(n,1)}$

$\theta_{s11\_meas_n} = MEAS_{(n,2)}$

$m_{s21\_meas_n} = MEAS_{(n,3)}$

$\theta_{s21\_meas_n} = MEAS_{(n,4)}$

$m_{s12\_meas_n} = MEAS_{(n,5)}$

$\theta_{s12\_meas_n} = MEAS_{(n,6)}$

$m_{s22\_meas_n} = MEAS_{(n,7)}$

$\theta_{s22\_meas_n} = MEAS_{(n,8)}$

2. Noise parameters of pads and devices

$f_{noise_n} = NOISE_{(n,0)}$

$nf_{min_n} = NOISE_{(n,1)}$

$m_{\Gamma opt_n} = NOISE_{(n,2)}$

$\theta_{\Gamma opt_n} = NOISE_{(n,3)}$

$R_{n_n} = NOISE_{(n,4)} \cdot 50$

$$\Gamma_{opt_n} = m_{\Gamma opt_n} \cdot \left(\cos\left(\frac{\theta_{\Gamma opt_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{\Gamma opt_n}}{180} \cdot \pi \right) \right)$$

$$Y_{opt_n} = \frac{1}{Z_o} \cdot \frac{1 - \Gamma_{opt_n}}{1 + \Gamma_{opt_n}} \qquad NF_{min_n} = 10^{\frac{nf_{min_n}}{10}}$$

S parameters of dummy pads

$$f_{pad_n} = PAD_{(n,0)}$$

$$m_{s11\_pad_n} = PAD_{(n,1)}$$

$$\theta_{s11\_pad_n} = PAD_{(n,2)}$$

$$m_{s21\_pad_n} = PAD_{(n,3)}$$

$$\theta_{s21\_pad_n} = PAD_{(n,4)}$$

$$m_{s12\_pad_n} = PAD_{(n,5)}$$

$$\theta_{s12\_pad_n} = PAD_{(n,6)}$$

$$m_{s22\_pad_n} = PAD_{(n,7)}$$

$$\theta_{s22\_pad_n} = PAD_{(n,8)}$$

S parameters of the measured data (including pads and devices)

$$S_{11\_meas_n} = m_{s11\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s11\_meas_n}}{180}\cdot\pi\right) + j\cdot\sin\left(\frac{\theta_{s11\_meas_n}}{180}\cdot\pi\right)\right)$$

$$S_{21\_meas_n} = m_{s21\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s21\_meas_n}}{180}\cdot\pi\right) + j\cdot\sin\left(\frac{\theta_{s21\_meas_n}}{180}\cdot\pi\right)\right)$$

$$S_{12\_meas_n} = m_{s12\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s12\_meas_n}}{180}\cdot\pi\right) + j\cdot\sin\left(\frac{\theta_{s12\_meas_n}}{180}\cdot\pi\right)\right)$$

$$S_{22\_meas_n} = m_{s22\_meas_n} \cdot \left(\cos\left(\frac{\theta_{s22\_meas_n}}{180}\cdot\pi\right) + j\cdot\sin\left(\frac{\theta_{s22\_meas_n}}{180}\cdot\pi\right)\right)$$

S parameters of the measured dummy pads

$$S_{11\_pad_n} = m_{s11\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s11\_pad_n}}{180}\cdot\pi\right) + j\cdot\sin\left(\frac{\theta_{s11\_pad_n}}{180}\cdot\pi\right)\right)$$

$$S_{21\_pad_n} = m_{s21\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{12\_pad_n} = m_{s12\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{22\_pad_n} = m_{s22\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) \right)$$

1. Convert the s-parameters to their y-parameters

$$Y_{11\_meas_n} = Y_o \cdot \frac{\left(1 - S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) + S_{12\_meas_n} \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{12\_meas_n} = Y_o \cdot \frac{-2 \cdot S_{12\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{21\_meas_n} = Y_o \cdot \frac{-2 \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{22\_meas_n} = Y_o \cdot \frac{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 - S_{22\_meas_n}\right) + S_{12\_meas_n} \cdot S_{21\_meas_n}}{\left(1 + S_{11\_meas_n}\right) \cdot \left(1 + S_{22\_meas_n}\right) - S_{12\_meas_n} \cdot S_{21\_meas_n}}$$

$$Y_{11\_pad_n} = Y_o \cdot \frac{\left(1 - S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{12\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{12\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{21\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{22\_pad_n} = Y_o \cdot \frac{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

3. Calculate the correlation matrix C_{A}^{DUT}

$$C_{A11_n} = 2 \cdot k \cdot T \cdot R_{n_n} \qquad C_{A12_n} = 2 \cdot k \cdot T \cdot \left(\frac{NF_{min_n} - 1}{2} - R_{n_n} \cdot \overline{Y_{opt_n}} \right)$$

$$C_{A21_n} = 2 \cdot k \cdot T \cdot \left(\frac{NF_{min_n} - 1}{2} - R_{n_n} \cdot Y_{opt_n} \right) \qquad C_{A22_n} = 2 \cdot k \cdot T \cdot \left[R_{n_n} \cdot \left(|Y_{opt_n}| \right)^2 \right]$$

4. Convert C_{A}^{DUT} to C_{Y}^{DUT}

$$C_{YDUT11_n} = -1 \cdot \overline{Y_{11\_meas_n}} \cdot \left(-1 \cdot Y_{11\_meas_n} \cdot C_{A11_n} + C_{A21_n} \right) - Y_{11\_meas_n} \cdot C_{A12_n} + C_{A22_n}$$

$$C_{YDUT12_n} = -1 \cdot \overline{Y_{21\_meas_n}} \cdot \left(-1 \cdot Y_{11\_meas_n} \cdot C_{A11_n} + C_{A21_n} \right)$$

$$C_{YDUT21_n} = \overline{Y_{11\_meas_n}} \cdot Y_{21\_meas_n} \cdot C_{A11_n} - Y_{21\_meas_n} \cdot C_{A12_n}$$

$$C_{YDUT22_n} = \overline{Y_{21\_meas_n}} \cdot Y_{21\_meas_n} \cdot C_{A11_n}$$

5. Calculate the C_{Y}^{PAD}

$$C_{YPAD11_n} = 2 \cdot k \cdot T \cdot \mathrm{Re}\left(Y_{11\_pad_n} \right)$$

$$C_{YPAD12_n} = 2 \cdot k \cdot T \cdot \mathrm{Re}\left(Y_{12\_pad_n} \right)$$

$$C_{YPAD21_n} = 2 \cdot k \cdot T \cdot \mathrm{Re}\left(Y_{21\_pad_n} \right)$$

$$C_{YPAD22_n} = 2 \cdot k \cdot T \cdot \mathrm{Re}\left(Y_{22\_pad_n} \right)$$

6. De-embedding the pad effects:

$$Y_{11\_extr_n} = Y_{11\_meas_n} - Y_{11\_pad_n}$$

$$Y_{12\_extr_n} = Y_{12\_meas_n} - Y_{12\_pad_n}$$

7. De-embedding the pad effect from C_{Y}^{DUT}

$$C_{YI11_n} = C_{YDUT11_n} - C_{YPAD11_n}$$

$$C_{YI12_n} = C_{YDUT12_n} - C_{YPAD12_n}$$

$$Y_{21\_extr_n} = Y_{21\_meas_n} - Y_{21\_pad_n} \qquad C_{YI21_n} = C_{YDUT21_n} - C_{YPAD21_n}$$

$$Y_{22\_extr_n} = Y_{22\_meas_n} - Y_{22\_pad_n} \qquad C_{YI22_n} = C_{YDUT22_n} - C_{YPAD22_n}$$

8. Convert Y matrix to A matrix:

$$A_{11_n} = \frac{-1 \cdot Y_{22\_extr_n}}{Y_{21\_extr_n}} \qquad A_{12_n} = \frac{-1}{Y_{21\_extr_n}}$$

$$A_{21_n} = \frac{-1 \cdot \left(Y_{11\_extr_n} \cdot Y_{22\_extr_n} - Y_{12\_extr_n} \cdot Y_{21\_extr_n}\right)}{Y_{21\_extr_n}} \qquad A_{22_n} = \frac{-1 \cdot Y_{11\_extr_n}}{Y_{21\_extr_n}}$$

9. Convert C_{YIDUT} to C_{AIDUT}

$$C_{AI11_n} = \overline{A_{12_n}} \cdot A_{12_n} \cdot C_{YI22_n}$$

$$C_{AI12_n} = A_{12_n} \cdot C_{YI21_n} - \overline{A_{22_n}} \cdot A_{12_n} \cdot C_{YI22_n}$$

$$C_{AI21_n} = \overline{A_{12_n}} \cdot \left(C_{YI12_n} - A_{22_n} \cdot C_{YI22_n}\right)$$

$$C_{AI22_n} = C_{YI11_n} - A_{22_n} \cdot C_{YI21_n} - \overline{A_{22_n}} \cdot \left(C_{YI12_n} - A_{22_n} \cdot C_{YI22_n}\right)$$

10. Calculate the noise parameters

$$NF_{min\_int_n} = 1 - \frac{1}{k \cdot T} \cdot \left(\mathrm{Re}\left(C_{AI12_n}\right) - \sqrt{\mathrm{Re}\left(C_{AI11_n}\right) \cdot \mathrm{Re}\left(C_{AI22_n}\right) - \mathrm{Im}\left(C_{AI12_n}\right)^2}\right)$$

$$Y_{opt\_int_n} = \frac{-\sqrt{\mathrm{Re}\left(C_{AI11_n}\right) \cdot \mathrm{Re}\left(C_{AI22_n}\right) - \mathrm{Im}\left(C_{AI12_n}\right)^2} + j \cdot \mathrm{Im}\left(C_{AI12_n}\right)}{C_{AI11_n}} \qquad Z_{opt\_int_n} = \frac{-1}{Y_{opt\_int_n}}$$

$$R_{n\_int_n} = \frac{\mathrm{Re}\left(C_{AI11_n}\right)}{2 \cdot k \cdot T}$$

Convert NF_{min} to dB and Y_{opt} to Γ_{opt}

$$NF_{min\_dB_n} = 10 \log\left(NF_{min\_int_n}\right)$$

$$\Gamma_{opt\_int_n} = \frac{Z_{opt\_int_n} - Z_o}{Z_{opt\_int_n} + Z_o}$$

$$R_{n\_norm_n} = \frac{R_{n\_int_n}}{50}$$

Output the intrinsic noise parameters : NF_{min} (dB), $|\Gamma_{opt}|$, $<(\Gamma_{opt})$ in degree, and the **normalized noise resistance** to the file **niose.prn**

$$\text{WRITEPRN(noise)} = \left(f_{noise_n} \quad NF_{min\_dB_n} \quad \left|\Gamma_{opt\_int_n}\right| \quad \frac{\arg\left(\Gamma_{opt\_int_n}\right)}{\pi} \cdot 180 \quad R_{n\_norm_n}\right)$$

Appendix C

HSPICE Program for Extracting DC Level 3 Model Parameters - UO, THETA, RS, RD, VMAX, ETA, and KAPPA

(A.1) Extracting UO, THETA, RS, and RD Based on I_{DS} vs. V_{GS} Characteristics in Linear Region

```
MOSFET LEVEL 3 MODEL PRARMETER EXTRACTION
.OPTION NOMOD POST=2 NEWTOL RELMOS=1E-5 ABSMOS=1E-8
.MODEL OPTMOD OPT ITROPT=100
.PARAM VDS=0 VGS=0 VBS=0 IDS=0

*******MODEL PARAMETERS*******
.PARAM
+    uo   = OPTIDVG(434.4714, 400, 600)
+    theta = OPTIDVG(82.2375E-3, 40E-3, 100E-3)
+    rs   = OPTIDVG(1227, 500, 1500)
+    rd   = OPTIDVG(1227, 500, 1500)
.MODEL MNCH0P8 NMOS LEVEL=3
<MODEL PRAMETERS PROVIDED BY CMC>

*******CIRCUIT DESCRIPTION*******
M1 DRAIN GATE SOURCE BULK MNCH0P8 L=0.8u W=60.0u
+ AD=132p AS=168p PD=124.4u PS=125.6u
VD DRAIN 0 DC VDS
VG GATE 0 DC VGS
VS SOURCE 0 DC 0V
VB BULK 0 DC VBS

*******CIRCUIT ANALYSIS*******
.DC DATA=IDVGL OPTIMIZE=OPTIDVG RESULTS=COMP1 MODEL=OPTMOD
.MEAS DC COMP1 ERR1 PAR(IDS) I(M1) MINVAL=1E-04 IGNOR=1E-05
.DC DATA=IDVGL
.PRINT DC VD=PAR(VDS) VG=PAR(VGS) IDSIM=I(M1) IDMEAS=PAR(IDS)

*******MEASURED IDS VS.VGS CHARACTERISTICS*********
.DATA IDVGL VDS VGS VBS IDS
```

```
0.05000E+00 1.00000E+00 0.00000E+00 80.016E-06
0.05000E+00 1.02500E+00 0.00000E+00 88.394E-06
0.05000E+00 1.05000E+00 0.00000E+00 96.645E-06
                        ...
0.05000E+00 2.95000E+00 0.00000E+00 454.41E-06
0.05000E+00 2.97500E+00 0.00000E+00 457.15E-06
0.05000E+00 3.00000E+00 0.00000E+00 459.80E-06
.ENDDATA

.END
```

(A.2) Extracting VMAX, ETA, and KAPPA Based on I_{DS} vs. V_{DS} Characteristics in Linear and Saturation Region

```
MOSFET LEVEL 3 MODEL PRARMETER EXTRACTION
.OPTION NOMOD POST=2 NEWTOL RELMOS=1E-5 ABSMOS=1E-8
.MODEL OPTMOD OPT ITROPT=100
.PARAM VDS=0 VGS=0 VBS=0 IDS=0

*******MODEL PARAMETERS*******
.PARAM
+    vmax  = OPTIDVD(100.5176E3, 60E3, 110E3)
+    eta   = OPTIDVD(31.8008E-3, 0, 1)
+    kappa = OPTIDVD(10E-3, 0, 1E0)

.MODEL MNCH0P8 NMOS LEVEL=3
<MODEL PRAMETERS PROVIDED BY CMC>

*******CIRCUIT DESCRIPTION*********
M1 DRAIN GATE SOURCE BULK MNCH0P8 L=0.8u W=60.0u AD=132p
AS=168p PD=124.4u PS=125.6u
VD DRAIN  0  DC  VDS
VG GATE   0  DC  VGS
VS SOURCE 0  DC  0V
VB BULK   0  DC  VBS

*******CIRCUIT ANALYSIS*********
.DC DATA=IDVDS OPTIMIZE=OPTIDVD RESULTS=COMP1 MODEL=OPTMOD
.MEAS DC COMP1 ERR1 PAR(IDS) I(M1) MINVAL=1E-04 IGNOR=1E-05
.DC DATA=IDVDS
.PRINT DC VD=PAR(VDS) VG=PAR(VGS) IDSIM=I(M1) IDMEAS=PAR(IDS)

*******MEASURED IDS VS.VDS CHARACTERISTICS*********
```

```
.DATA IDVDS VDS VGS VBS IDS
0.02500E+00 1.00000E+00 0.00000E+00 158.24E-09
0.05000E+00 1.00000E+00 0.00000E+00 43.914E-06
0.07500E+00 1.00000E+00 0.00000E+00 82.061E-06
                          ...
2.95000E+00 3.00000E+00 0.00000E+00 9.1000E-03
2.97500E+00 3.00000E+00 0.00000E+00 9.1057E-03
3.00000E+00 3.00000E+00 0.00000E+00 9.1105E-03
.ENDDATA

.END
```

Appendix D

MATHCAD Program for the Pad Parameter Extraction Based on the Measured S-Parameters of an "OPEN" Dummy Structure

This programm is used to extract the equivalent model parameters of dummy pads .

Enter the information for the following three lines...

$PAD := READPRN(dumpad)$ Data file for the dummy pads

$n := 0, 1 .. rows(PAD) - 1$ Number of frequency points

Characteristic impedance:

$Z_o := 50 \qquad Y_o := \frac{1}{Z_o}$

S parameters of dummy pads

$f_{pad_n} := PAD_{(n,0)} \cdot 10^9$

$m_{s11\_pad_n} := PAD_{(n,1)}$

$\theta_{s11\_pad_n} := PAD_{(n,2)}$

$m_{s21\_pad_n} := PAD_{(n,3)}$

$\theta_{s21\_pad_n} := PAD_{(n,4)}$

$m_{s12\_pad_n} := PAD_{(n,5)}$

$\theta_{s12\_pad_n} := PAD_{(n,6)}$

$m_{s22\_pad_n} := PAD_{(n,7)}$

$\theta_{s22\_pad_n} := PAD_{(n,8)}$

$$S_{11\_pad_n} = m_{s11\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s11\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s11\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{21\_pad_n} = m_{s21\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s21\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{12\_pad_n} = m_{s12\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s12\_pad_n}}{180} \cdot \pi \right) \right)$$

$$S_{22\_pad_n} = m_{s22\_pad_n} \cdot \left(\cos\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) + j \cdot \sin\left(\frac{\theta_{s22\_pad_n}}{180} \cdot \pi \right) \right)$$

De-embedding the pad effects:

$$Y_{11\_pad_n} = Y_o \cdot \frac{\left(1 - S_{11\_pad_n}\right) \cdot \left(1 + S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{12\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{12\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{21\_pad_n} = Y_o \cdot \frac{-2 \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{22\_pad_n} = Y_o \cdot \frac{\left(1 - S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) + S_{12\_pad_n} \cdot S_{21\_pad_n}}{\left(1 + S_{11\_pad_n}\right) \cdot \left(1 - S_{22\_pad_n}\right) - S_{12\_pad_n} \cdot S_{21\_pad_n}}$$

$$Y_{1\_pad_n} = Y_{11\_pad_n} - Y_{12\_pad_n}$$

$$Y_{2\_pad_n} = Y_{22\_pad_n} - Y_{21\_pad_n}$$

$C_1 := 10^{-14}$ $R_1 := 0.6810^3$ $C_2 := 10^{-14}$

$$Y_1(C_1, R_1, C_2, f) := 2i\cdot\pi\cdot f\cdot C_2 + \frac{1}{\left[R_1 - \frac{1}{2}\cdot\frac{i}{\left[\pi\cdot(f\cdot C_1)\right]}\right]}$$

$$SSE(C_1, R_1, C_2) := \sum_n \left(\frac{Y_{1\_pad_n} + Y_{2\_pad_n}}{2} - Y_1(C_1, R_1, C_2, f_{pad_n})\right)^2$$

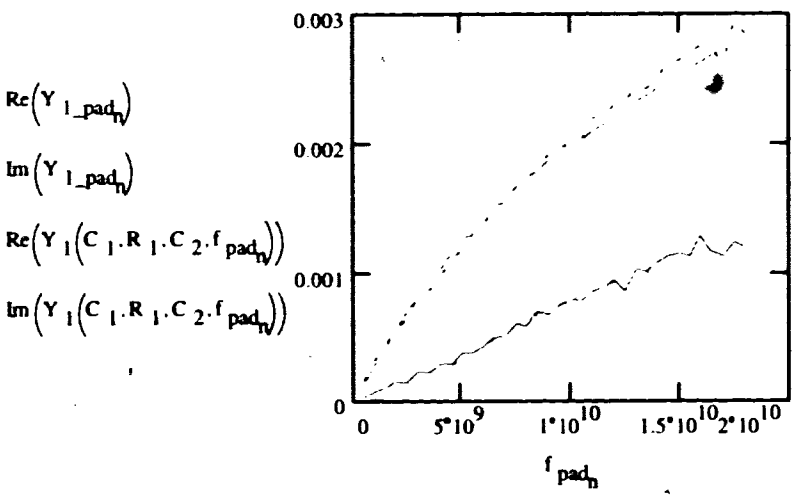
Given

$SSE(C_1, R_1, C_2) = 0$ $C_1 > 0$ $C_2 > 0$ $R_1 > 0$

$1 = 1$ $2 = 2$

$$\begin{bmatrix} C_1 \\ R_1 \\ C_2 \end{bmatrix} := Minerr(C_1, R_1, C_2) \qquad \sqrt{ERR} = 1.439910^{-11}$$

$C_1 = 2.509710^{-14}$ $R_1 = 680$ $C_2 = 1.97510^{-14}$



WRITEPRN(pad) := $Im(Y_1(C_1, R_1, C_2, f_{pad_n}))$

$C := 1 \cdot 10^{-15}$

$Y_{12}(C, f) := -1 \cdot j \cdot 2 \cdot \pi \cdot f \cdot C$

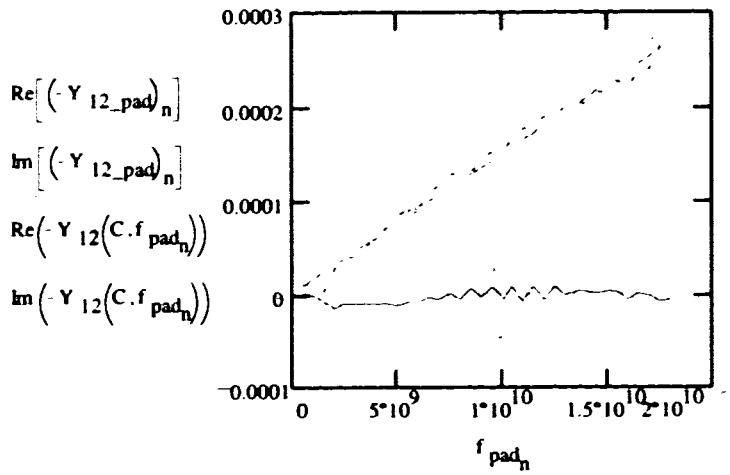
$SSE(C) := \sum_n \left(Y_{12\_pad_n} - Y_{12}\left(C, f_{pad_n}\right) \right)^2$

Given

$SSE(C) = 0 \qquad C > 0$

$C := \text{Minerr}(C) \qquad \sqrt{ERR} = 2.832 \cdot 10^{-5}$

$C = 2.3706 \cdot 10^{-15}$



Appendix E

MMICAD Program for the AC Parameter Extraction Based on the S-Parameters of an Intrinsic Transistor

```
MODE FREQUENCY
GLOBAL
DIM FREQ=1e+009 RES=1 COND=0.001 CAP=1e-015  &
IND=1e-012 LNG=1e-006 TIME=1e-012

FILES
h:\james\s_of_dev\nf1w65P0.s2p CMC0P8 2P FREQ

VAR
G=? 5 5.53345 6 ?
RDS=5801
CGS=? 50 67.617 100 ?
RI=? 0 108.41 500 ?
CDG=? 11 12.0343 14 ?
RG=175
RS=20.38
RD=20.38
CGB=1.4
CDB=41
CSB=117
GMB=0.8627961
RDB=? 0 299.864 1000 ?
LG=850
LS=0
LD=240
T=0
GGS=0
CDC=0
CDS=0
F=1e+100
```

```
CKT
IND 1 3 L=LG
IND 2 4 L=LD
IND 8 0 L=LS
IMP 3 5 R=RG X=0
IMP 4 6 R=RD X=0
IMP 7 8 R=RS X=0
IMP 8 9 R=RDB X=0
CAP 5 8 C=CGB
CAP 6 9 C=CDB
CAP 7 8 C=CSB
FET1 5 6 7 G=G T=T F=F CGS=CGS GGS=GGS RI=RI  &
CDG=CDG CDC=CDC CDS=CDS RDS=RDS
VDCSNF 7 6 8 7 GM=GMB TAU=0 R1=RS R2=1e+020  &
F=1e+100 A=0
DEF2P 1 2 MODEL

FREQ
SWEEP  0.5 10 0.5

MARKER
SWEEP 0.5 10 0.5

OPT
MODEL SPAR EQ CMC0P8  W11=1 W12=0.1 W21=2 W22=1

OUT
MODEL SMI[S21]  Graph1
CMC0P8 SMI[S21]  Graph1
MODEL SMI[S12]  Graph2
CMC0P8 SMI[S12]  Graph2
MODEL SMI[S11]  Graph3
CMC0P8 SMI[S11]  Graph3
MODEL SMI[S22]  Graph4
CMC0P8 SMI[S22]  Graph4
CMC0P8 SPAR     Table1
MODEL SPAR      Table2
GRID
RANGE 0 12 2
```

Appendix F

MATHCAD Program for Calculating the Noise Parameters of an Intrinsic Transistor Based on the Direct Calculation Technigue

(F.1) Calculating the Thermal Noise Source in the Channel

Summary of Process Parameters for a Typical Silicon-Gate n-Well CMOS Process 0.8u Minimum Allowed Gate Length

$$\begin{bmatrix} l \\ w \\ weff \\ leff \\ vgs \\ vds \\ vth \\ vdsat \\ beta \\ id \\ gm \\ gds \\ cgs \\ ri \\ cgd \\ rg \\ rs \\ rd \\ cgb \\ cbd \\ cbs \\ gmb \\ rbd \\ lg \\ ls \\ ld \end{bmatrix} := READPRN(nf1w68p0)$$

$q = 1.60218 \cdot 10^{-19} \cdot coul$ $\quad ev = 1.60218 \cdot 10^{-19} \cdot joule$

$\varepsilon_{ox} = 0.345144 \cdot 10^{-12} \cdot \frac{farad}{cm}$

$micron = 10^{-6} \cdot m$ $\quad h = 6.62617 \cdot 10^{-34} \cdot joule \cdot sec$

$Hz = \frac{1}{sec}$ $\quad k = 1.38066 \cdot 10^{-23} \cdot \frac{joule}{K}$

$\varepsilon_{si} = 1.04 \cdot 10^{-12} \cdot \frac{farad}{cm}$ $\quad T = 300 \cdot K$

Parameters necessary to be modified for different runs: theta, KAPPA, VMAX and uo

(NOTE: KAPPA should be unitless)

$theta = 49.908 \cdot 10^{-3} \cdot volt^{-1}$ $\quad KAPPA = 0$

$v_{max} = 175.5176 \cdot 10^{3} \cdot \frac{m}{sec}$ $\quad \mu_o = 443.5196 \cdot \frac{cm^2}{volt \cdot sec}$

$t_{ox} = 17.52 \cdot 10^{-9} \cdot m$ $\quad NSUB = 3.6 \cdot 10^{16} \cdot cm^{-3}$

$E_c = \frac{v_{max}}{\mu_o}$ $\quad C_{ox} = 1.97 \cdot 10^{-3} \cdot \frac{farad}{m^2}$

$f = 4 \cdot 10^{9} \cdot Hz$ $RGSH = 2.0 \cdot ohm$ $n = 1$ (n is the number of fingers)

$\omega = 2 \cdot \pi \cdot f$ $S = i \cdot \omega$ $L = l \cdot micron$ $W = w \cdot micron$

$L_{eff} = leff \cdot m$ $W_{eff} = weff \cdot m$ $W_{eff} = 59.91 \cdot micron$ $I_D = id \cdot amp$

$C_{GD} = cgd \cdot farad$ $C_{GS} = cgs \cdot farad$ $C_{BS} = cbs \cdot farad$

$C_{BD} = cbd \cdot farad$ $C_{GB} = cgb \cdot farad$

$g_m = gm \cdot \frac{amp}{volt}$ $g_{mb} = gmb \cdot \frac{amp}{volt}$

$R_i = ri \cdot ohm$ $R_i = 103.643 \cdot ohm$

$r_{BD} = rbd \cdot ohm$ $r_{BD} = 310.849 \cdot ohm$

$r_{DS} = rds \cdot ohm$ $r_{DS} = 4.536 \cdot 10^{3} \cdot ohm$

$r_G = rg \cdot ohm$ $r_G = 175 \cdot ohm$

$r_D = \frac{(0.07267 + 0.9243) \cdot micron \cdot (1.076 \cdot 10^{3} \cdot ohm)}{W}$ $r_D = rd \cdot ohm$

$r_S = \frac{(0.07267 + 0.9243) \cdot micron \cdot (1.076 \cdot 10^{3} \cdot ohm)}{W}$ $r_S = rs \cdot ohm$

$V_{th} = vth \cdot volt$ $V_{gs\_ext} = vgs \cdot volt$ $V_{ds\_ext} = vds \cdot volt$ $V_{dsat} = vdsat \cdot volt$

$V_{gs\_int} = V_{gs\_ext} - I_D \cdot r_S$ $V_{ds\_int} = V_{ds\_ext} - I_D \cdot (r_S + r_D)$

$\mu_s = \frac{\mu_o}{1 + theta \cdot (V_{gs\_int} - V_{th})}$

In saturation, we assume that the channel is pinch-off and the voltage drop along the channel is Vdsat

$$V_{dseff} := if\left(V_{ds\_int} > V_{dsat}, V_{dsat}, V_{ds\_int}\right) \qquad V_{dseff} = 1.263 \cdot volt$$

$$v_c := \frac{v_{max} \cdot L_{eff}}{\mu_s} \qquad V_{sint} := I_D \cdot r_S$$

$$\mu_{eff} := if\left[v_{max} > 0 \cdot \frac{m}{sec}, \frac{\mu_s}{1 + \frac{V_{dseff}}{v_c}}, \mu_s\right] \qquad \mu_{eff} = 280.325 \cdot \frac{cm^2}{volt \cdot sec}$$

$$y := \frac{V_{gs\_int} - V_{th}}{E_c \cdot L_{eff}} \qquad V_{dsvan} := E_c \cdot L_{eff} \cdot \left(-1 + \sqrt{1 + 2 \cdot y}\right) \qquad g_{do} := \mu_o \cdot W_{eff} \cdot C_{ox} \cdot \frac{V_{gs\_int} - V_{th}}{L_{eff}}$$

Here we calculate the channel length modulation delta L

$$X_d := \sqrt{\frac{2 \cdot \varepsilon_{si}}{q \cdot NSUB}} \qquad X_d = 1.899 \cdot 10^{-7} \cdot \frac{m}{volt^{0.5}}$$

$$E_p := \frac{v_c \cdot \left(v_c + V_{dsat}\right)}{L_{eff} \cdot V_{dsat}} \qquad E_p = 1.406 \cdot 10^7 \cdot \frac{volt}{m}$$

$$\Delta L := \frac{1 \cdot E_p \cdot X_d^2}{2} + \sqrt{\left(\frac{E_p \cdot X_d^2}{2}\right)^2 + KAPPA \cdot X_d^2 \cdot \left(V_{ds\_int} - V_{dsat}\right)}$$

$$\Delta L = 0 \cdot micron \qquad L_{eff} = 0.655 \cdot micron$$

$$L'_{eff} := L_{eff} - \Delta L$$

$$\alpha_{satn} := \frac{1}{g_{do} \cdot I_D \cdot L'^2_{eff}} \cdot \int_{V_{sint}\cdot volt}^{V_{dseff}} \left[\mu_s \cdot W_{eff} C_{ox}\left(V_{gs\_int} - V_{th} - V\right)\right]^n \cdot \left[\mu_s \cdot W_{eff} C_{ox}\left(V_{gs\_int} - V_{th} - V\right) - \frac{I_D}{E_c}\right]^{2-n} dV$$

Leff should be replaced by (Leff - deltaL)

$\alpha_{sat0} = 0.33 \qquad \alpha_{sat1} = 0.485 \qquad \alpha_{sat2} = 0.728 \qquad y = 0.733$

$$V_{as} = V_{dseff} + \frac{1}{2}\cdot\frac{V_{dseff}^{2}}{E_c\cdot L_{eff}} - \frac{\frac{1}{2}\cdot\left(V_{gs\_int} - V_{th}\right)\cdot V_{dseff} - \frac{1}{6}\cdot V_{dseff}^{2}}{V_{gs\_int} - V_{th} - \frac{1}{2}\cdot V_{dseff}}\cdot\left(1 + \frac{V_{dseff}}{E_c\cdot L_{eff}}\right)$$

$$\delta_{satn} := \frac{g_{do}}{I_D^{3}\cdot L_{eff}^{2}}\cdot\int_{V_{sint}volt}^{V_{dseff}} \left[\mu_s\cdot W_{eff} C_{ox}\left(V_{gs\_int} V_{th} - V\right)\right]^{n}\cdot\left[\mu_s\cdot W_{eff} C_{ox}\left(V_{gs\_int} V_{th} - V\right) - \frac{I_D}{E_c}\right]^{2-n}\cdot\left(V_{as} - V\right)^{2} dV$$

$$\varepsilon_{satn} := \frac{1}{I_D^{2}\cdot L_{eff}^{2}}\cdot\int_{V_{sint}volt}^{V_{dseff}} \left[\mu_s\cdot W_{eff} C_{ox}\left(V_{gs\_int} V_{th} - V\right)\right]^{n}\cdot\left[\mu_s\cdot W_{eff} C_{ox}\left(V_{gs\_int} V_{th} - V\right) - \frac{I_D}{E_c}\right]^{2-n}\cdot\left(V_{as} - V\right) dV$$

$\alpha_{sat} = \alpha_{sat1} \qquad \delta_{sat} = \delta_{sat0} \qquad \varepsilon_{sat} = \varepsilon_{sat0} \qquad i_d = \sqrt{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}}$

$\alpha_{sat} = 0.485 \qquad \delta_{sat} = 0.074 \qquad \varepsilon_{sat} = -0.008 \qquad useless = 0$

$f_T = \frac{1}{2\cdot\pi}\cdot\frac{g_m}{C_{GS} + C_{GD}} \qquad C_s = 300\frac{m}{sec} \qquad \alpha_x = 1$

$$DATA = \begin{bmatrix} \frac{r_G}{ohm} & \frac{r_S}{ohm} & \frac{r_D}{ohm} \\ \frac{r_{DS}}{ohm} & \frac{R_i}{ohm} & \frac{r_{BD}}{ohm} \\ \frac{C_{GS}}{farad} & \frac{C_{GD}}{farad} & \frac{C_{GB}}{farad} \\ \frac{C_{BS}}{farad} & \frac{C_{BD}}{farad} & g_m \cdot \frac{volt}{amp} \\ g_{mb} \cdot \frac{volt}{amp} & \frac{L}{micron} & \frac{W}{micron} \\ \frac{I_D}{amp} & \frac{S}{Hz \cdot i} & \alpha_{sat} \\ \delta_{sat} & \varepsilon_{sat} & g_{do} \cdot ohm \\ \frac{V_{gs\_int}}{volt} & vth & beta \\ \mu_{eff} \cdot \frac{volt \cdot sec}{m^2} & \frac{L_{eff}}{micron} & \frac{W_{eff}}{micron} \\ \frac{V_{dseff}}{volt} & \alpha_x & \mu_s \cdot \frac{volt \cdot sec}{m^2} \\ lg & ls & ld \end{bmatrix}$$

$$DATA = \begin{bmatrix} 175 & 20.38 & 20.38 \\ 4.536 \cdot 10^{3} & 103.643 & 310.849 \\ 6.859 \cdot 10^{-14} & 1.291 \cdot 10^{-14} & 1.4 \cdot 10^{-15} \\ 1.17 \cdot 10^{-13} & 4.1 \cdot 10^{-14} & 0.006 \\ 8.914 \cdot 10^{-4} & 0.8 & 60 \\ 0.008 & 2.513 \cdot 10^{10} & 0.485 \\ 0.074 & -0.008 & 0.015 \\ 2.534 & 0.636 & 0.005 \\ 0.028 & 0.655 & 59.91 \\ 1.263 & 1 & 0.041 \\ 8.5 \cdot 10^{-10} & 0 & 2.4 \cdot 10^{-10} \end{bmatrix}$$

(F.2) Calculating the Noise Parameters of the DUT

$$\begin{bmatrix} R'_g & R'_s & R'_d \\ r'_{ds} & r'_i & r'_{bd} \\ C'_{GS} & C'_{GD} & C'_{GB} \\ C'_{BS} & C'_{BD} & g''_m \\ g'_{mb} & L' & W' \\ \Gamma'_D & S' & \alpha_{sat} \\ \delta_{sat} & \varepsilon_{sat} & g'_{do} \\ vgs'\_int & vth' & beta' \\ \mu'_{eff} & L'_{eff} & W'_{eff} \\ vdseff & \alpha_x & \mu'_s \\ lg & ls & ld \end{bmatrix} = READPRN(data)$$

$h = 6.6261710^{-34}\cdot joule\cdot sec$ $\quad micron := 10^{-6}\cdot m$

$k = 1.3806610^{-23}\cdot\frac{joule}{K}$ $\quad q = 1.6021810^{-19}\cdot coul$

$\varepsilon_{si} = 1.0410^{-12}\cdot\frac{farad}{cm}$ $\quad \varepsilon_{ox} = 0.3451410^{-12}\cdot\frac{farad}{cm}$

Pad capacitances:

$C_1 = 25.09710^{-15}\cdot farad$

$C_2 = 19.7510^{-15}\cdot farad$

$C_3 = 2.370610^{-15}\cdot farad\cdot 0$

$R_1 = 680\cdot ohm$

Characteristic impedance Z_o

$Z_o = 50\cdot ohm$

$Y_o = \frac{1}{Z_o}$

Note: With devices, C3 is replaced by the Y parameters of devices

Parameters necessary to be modified for different runs: theta, KAPPA, VMAX and uo

(NOTE: KAPPA should be unitless)

$theta = 49.90810^{-3}\cdot volt^{-1}$ $\quad KAPPA = 0$ $\quad C_{ox} = 1.9710^{-3}\cdot\frac{farad}{m^2}$

$v_{max} = 175.517610^{3}\cdot\frac{m}{sec}$ $\quad \mu_o = 443.5196\frac{cm^2}{volt\cdot sec}$ $\quad t_{ox} = 17.5210^{-9}\cdot m$

$R_G = R'_g\cdot ohm$ $\quad g_m = g''_m\cdot\frac{amp}{volt}$ $\quad R_i = r'_i\cdot ohm$

$C_{GD} = C'_{GD}\cdot farad$ $\quad R_{DS} = r'_{ds}\cdot ohm$ $\quad C_{BS} = C'_{BS}\cdot farad$

$R_D = R'_d\cdot ohm$ $\quad C_{GB} = C'_{GB}\cdot farad$ $\quad R_{BD} = r'_{bd}\cdot ohm$

$C_{GS} = C'_{GS}\cdot farad$ $\quad R_s = R'_s\cdot ohm$ $\quad C_{BD} = C'_{BD}\cdot farad$

$R_S = R_s$ $\quad R_S = 20.38\cdot ohm$ $\quad I_D = \Gamma'_D\cdot amp$

$W = W' \cdot micron$ $\quad S = S' \cdot \frac{i}{sec}$ $\quad \omega = \frac{S}{i}$

$g_{mb} = g'_{mb} \cdot \frac{amp}{volt}$ $\quad L = L' \cdot micron$ $\quad V_{gs\_int} = vgs'\_int \cdot volt$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ $\quad C_o = C_{ox} \cdot W \cdot L$ $\quad g_{do} = \frac{g'_{do}}{ohm}$

$g'_m = g_m \cdot \frac{1}{1 + S \cdot R_i \cdot C_{GS}}$ $\quad g'_m = 0.006 - 0.001i \cdot ohm^{-1}$ $\quad \beta = beta' \cdot \frac{amp}{volt^2}$

$V_{th} = vth' \cdot volt$ $\quad \mu_{eff} = \mu'_{eff} \cdot \frac{m^2}{volt \cdot sec}$ $\quad L_{eff} = L'_{eff} \cdot micron$

$V_{dseff} = vdseff \cdot volt$ $\quad \mu_s = \mu'_s \cdot \frac{m^2}{volt \cdot sec}$ $\quad W_{eff} = W'_{eff} \cdot micron$

$L_G = lg \cdot henry$ $\quad L_S = ls \cdot henry$ $\quad L_D = ld \cdot henry$

Definition of branches:

$Y_1 = \frac{1}{R_G + S \cdot L_G}$ $\quad Y_2 = S \cdot C_{GD}$ $\quad Y_3 = \frac{1}{R_D + S \cdot L_D}$ $\quad Y_4 = \frac{1}{R_i + \frac{1}{S \cdot C_{GS}}}$

$Y_5 = \frac{1}{R_{DS}}$ $\quad Y_6 = S \cdot C_{GB}$ $\quad Y_7 = \frac{1}{R_S} + S \cdot C_{BS}$ $\quad Y_8 = \frac{1}{R_{BD} + \frac{1}{S \cdot C_{BD}}}$

$Y_9 = S \cdot C_2 + \frac{1}{R_1 + \frac{1}{S \cdot C_1}}$ $\quad Y_{10} = S \cdot C_3$

$Y_1 = 0.006 - 6.872 \cdot 10^{-4} i \cdot ohm^{-1}$ $\quad Y_2 = 3.244 \cdot 10^{-4} i \cdot ohm^{-1}$ $\quad Y_3 = 0.045 - 0.013i \cdot ohm^{-1}$

$Y_4 = 2.979 \cdot 10^{-4} + 0.002i \cdot ohm^{-1}$ $\quad Y_5 = 2.205 \cdot 10^{-4} \cdot ohm^{-1}$ $\quad Y_6 = 3.518 \cdot 10^{-5} i \cdot ohm^{-1}$

$Y_7 = 0.049 + 0.003i \cdot ohm^{-1}$ $\quad Y_8 = 2.993 \cdot 10^{-4} + 9.345 \cdot 10^{-4} i \cdot ohm^{-1}$

Definition of branches for the testing pads:

$$Y_{1p} = S \cdot C_2 + \frac{1}{R_1 + \frac{1}{S \cdot C_1}} \qquad Y_{2p} = S \cdot C_2 + \frac{1}{R_1 + \frac{1}{S \cdot C_1}} \qquad Y_{3p} = S \cdot C_3$$

Definition of noise the C matrix: $a = 0$ GDSNOI = 1

Reference book:

1. TK7871.85 V34 1986 (check pp. 290-292)
2. TK7871.99 M44 T77 (the thought experiment in p337 I think that is a wrong approach)
3. IEEE J of solid-state circuit, vol.29 No. 7, July 1994

$\alpha_{sat} \cdot 4 \cdot k \cdot T \cdot g_{do}$ Channel thermal noise current power density from Venderzel

Channel thermal noise current power density from HSPICE NLEV < 3

$$\frac{8}{3} \cdot k \cdot T \cdot g_m$$

Channel thermal noise current power density from HSPICE NLEV = 3.

$$\frac{8}{3} \cdot k \cdot T \cdot \beta \cdot \left(V_{gs\_int} - V_{th}\right) \cdot \frac{1 + a + a^2}{1 + a} \cdot GDSNOI$$

$\frac{8}{3} \cdot k \cdot T \cdot \left(g_m + \frac{1}{R_{DS}}\right)$ Channel thermal noise current power density from BSIM3V3 noimod=1

$$C = \begin{bmatrix} \delta_{sat} \cdot 4 \cdot k \cdot T \cdot \frac{\omega^2 \cdot C_o^2}{g_{do}} \cdot 0 & \varepsilon_{sat} \cdot 4 \cdot k \cdot T \cdot S \cdot C_o \cdot 0 & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec \\ \overline{\left(\varepsilon_{sat} \cdot 4 \cdot k \cdot T \cdot S \cdot C_o\right)} \cdot 0 & \alpha_{sat} \cdot 4 \cdot k \cdot T \cdot g_{do} & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec \\ \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \frac{4 \cdot k \cdot T}{R_G} & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec \\ \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \frac{4 \cdot k \cdot T}{R_S} & 0 \cdot amp^2 \cdot sec & 0 \cdot amp^2 \cdot sec \\ \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \frac{4 \cdot k \cdot T}{R_D} & 0 \cdot amp^2 \cdot sec \\ \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \overline{\left(0 \cdot amp^2 \cdot sec\right)} & \frac{4 \cdot k \cdot T}{R_{BD}} \end{bmatrix}$$

IMPORTANT NOTE: **i1i2* = (i1*i2)***

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1.221 \cdot 10^{-22} & 0 & 0 & 0 & 0 \\ 0 & 0 & 9.467 \cdot 10^{-23} & 0 & 0 & 0 \\ 0 & 0 & 0 & 8.129 \cdot 10^{-22} & 0 & 0 \\ 0 & 0 & 0 & 0 & 8.129 \cdot 10^{-22} & 0 \\ 0 & 0 & 0 & 0 & 0 & 5.331 \cdot 10^{-23} \end{bmatrix} \cdot \frac{amp^2}{Hz}$$

Node equations: by KCL

node 1: (without pads)

$$Y_1 \cdot (V_1 - V_3) + i_G$$

$$Y_{11.2} = Y_1 \quad Y_{12.2} = 0 \cdot ohm^{-1} \quad Y_{13.2} = -Y_1 \quad Y_{14.2} = 0 \cdot ohm^{-1} \quad Y_{15.2} = 0 \cdot ohm^{-1}$$

node 1: (with pads)

$$Y_1 \cdot (V_1 - V_3) + Y_{1p} \cdot V_1 + Y_{3p} \cdot (V_1 - V_2)$$

$$(Y_1 + Y_{1p} + Y_{3p}) \cdot V_1 - Y_1 \cdot V_3 - Y_{3p} \cdot V_2$$

$$Y_{11.2} = Y_1 + Y_{1p} + Y_{3p} \quad Y_{12.2} = -Y_{3p} \quad Y_{13.2} = -Y_1 \quad Y_{14.2} = 0 \cdot ohm^{-1} \quad Y_{15.2} = 0 \cdot ohm^{-1}$$

$$A_{11.2} = 0 \quad A_{12.2} = 0 \quad A_{13.2} = 1 \quad A_{14.2} = 0 \quad A_{15.2} = 0 \quad A_{16.2} = 0$$

node 2: (without pads)

$$Y_3 \cdot (V_2 - V_4) + i_D$$

$$Y_{21.2} = 0 \cdot ohm^{-1} \quad Y_{22.2} = Y_3 \quad Y_{23.2} = 0 \cdot ohm^{-1} \quad Y_{24.2} = -Y_3 \quad Y_{25.2} = 0 \cdot ohm^{-1}$$

node 2: (with pads)

$$Y_3 \cdot (V_2 - V_4) + Y_{2p} \cdot V_2 + Y_{3p} \cdot (V_2 - V_1)$$

$$(Y_3 + Y_{2p} + Y_{3p}) \cdot V_2 - Y_3 \cdot V_4 - Y_{3p} \cdot V_1$$

$$Y_{21.2} = -Y_{3p} \quad Y_{22.2} = Y_3 + Y_{2p} + Y_{3p} \quad Y_{23.2} = 0 \cdot ohm^{-1} \quad Y_{24.2} = -Y_3 \quad Y_{25.2} = 0 \cdot ohm^{-1}$$

$A_{21.2} = 0 \quad A_{22.2} = 0 \quad A_{23.2} = 0 \quad A_{24.2} = 0 \quad A_{25.2} = 1 \quad A_{26.2} = 1$

node 3: (without pads)

$Y_6 \cdot V_3 + Y_4 \cdot (V_3 - V_5) + Y_2 \cdot (V_3 - V_4) - Y_1 \cdot (V_1 - V_3) - i_G - i_g$

$(Y_6 + Y_4 + Y_1 + Y_2) \cdot V_3 - i_G - Y_1 \cdot V_1 - Y_4 \cdot V_5 - Y_2 \cdot V_4 - i_g$

$Y_{31.2} = -Y_1 \quad Y_{32.2} = 0 \cdot ohm^{-1} \quad Y_{33.2} = Y_1 + Y_2 + Y_4 + Y_6 \quad Y_{34.2} = -Y_2 \quad Y_{35.2} = -Y_4$

node 3: (with pads)

$Y_6 \cdot V_3 + Y_4 \cdot (V_3 - V_5) + Y_2 \cdot (V_3 - V_4) - Y_1 \cdot (V_1 - V_3)$

$(Y_6 + Y_4 + Y_1 + Y_2) \cdot V_3 - Y_1 \cdot V_1 - Y_4 \cdot V_5 - Y_2 \cdot V_4$

$Y_{31.2} = -Y_1 \quad Y_{32.2} = 0 \cdot ohm^{-1} \quad Y_{33.2} = Y_1 + Y_2 + Y_4 + Y_6 \quad Y_{34.2} = -Y_2 \quad Y_{35.2} = -Y_4$

$A_{31.2} = -1 \quad A_{32.2} = 0 \quad A_{33.2} = -1 \quad A_{34.2} = 0 \quad A_{35.2} = 0 \quad A_{36.2} = 0$

node 4: (without pads)

$Y_5 \cdot (V_4 - V_5) + Y_8 \cdot V_4 + g'_m \cdot (V_3 - V_5) - Y_2 \cdot (V_3 - V_4) - Y_3 \cdot (V_2 - V_4) - i_d - i_D + g_{mb} \cdot V_5 + i_{BD}$

$(g'_m - Y_2) \cdot V_3 + (Y_8 + Y_2 + Y_5 + Y_3) \cdot V_4 + [(-Y_5 - g'_m) + g_{mb}] \cdot V_5 - i_D - Y_3 \cdot V_2 - i_d + i_{BD}$

$Y_{41.2} = 0 \cdot ohm^{-1} \quad Y_{42.2} = -Y_3 \quad Y_{43.2} = g'_m - Y_2 \quad Y_{44.2} = Y_2 + Y_3 + Y_5 + Y_8$

$Y_{45.2} = g_{mb} - g'_m - Y_5$

node 4: (with pads)

$Y_5 \cdot (V_4 - V_5) + Y_8 \cdot V_4 + g_m \cdot (V_3 - V_5) - Y_2 \cdot (V_3 - V_4) - Y_3 \cdot (V_2 - V_4) + g_{mb} \cdot V_5$

$(g_m - Y_2) \cdot V_3 + (Y_8 + Y_2 + Y_5 + Y_3) \cdot V_4 + [(-Y_5 - g_m) + g_{mb}] \cdot V_5 - Y_3 \cdot V_2$

$Y_{41.2} = 0 \cdot ohm^{-1} \quad Y_{42.2} = -Y_3 \quad Y_{43.2} = g_m - Y_2$

$Y_{44.2} = Y_2 + Y_3 + Y_5 + Y_8 \quad Y_{45.2} = g_{mb} - g_m - Y_5$

$A_{41.2} = 0 \quad A_{42.2} = -1 \quad A_{43.2} = 0 \quad A_{44.2} = 0 \quad A_{45.2} = -1 \quad A_{46.2} = 1$

node 5: (without pads)

$$Y_7 V_5 + i_g + i_d + i_S - Y_4 (V_3 - V_5) - Y_5 (V_4 - V_5) - g'_m (V_3 - V_5) - g_{mb} V_5$$

$$(-Y_4 - g'_m) \cdot V_3 + (Y_7 + Y_4 + Y_5 + g'_m - g_{mb}) \cdot V_5 + i_S + i_g + i_d - Y_5 V_4$$

$Y_{51.2} = 0 \cdot ohm^{-1}$ $Y_{52.2} = 0 \cdot ohm^{-1}$ $Y_{53.2} = -g'_m - Y_4$ $Y_{54.2} = -Y_5$

$Y_{55.2} = g'_m + Y_4 + Y_5 + Y_7 - g_{mb}$

node 5: (with pads)

$$Y_7 V_5 - Y_4 (V_3 - V_5) - Y_5 (V_4 - V_5) - g_m (V_3 - V_5) - g_{mb} V_5$$

$$(-Y_4 - g_m) \cdot V_3 + (Y_7 + Y_4 - Y_5 + g_m - g_{mb}) \cdot V_5 - Y_5 V_4$$

$Y_{51.2} = 0 \cdot ohm^{-1}$ $Y_{52.2} = 0 \cdot ohm^{-1}$ $Y_{53.2} = -g_m - Y_4$ $Y_{54.2} = -Y_5$

$Y_{55.2} = g_m + Y_4 + Y_5 - Y_7 - g_{mb}$

$A_{51.2} = 1$ $A_{52.2} = 1$ $A_{53.2} = 0$ $A_{54.2} = 1$ $A_{55.2} = 0$ $A_{56.2} = 0$

Matrix elimination:

Eliminate node 5:

$$Y_{11.3} = Y_{11.2} - \frac{Y_{51.2} Y_{15.2}}{Y_{55.2}} \qquad A_{11.3} = A_{11.2} - \frac{A_{51.2} Y_{15.2}}{Y_{55.2}}$$

$$Y_{12.3} = Y_{12.2} - \frac{Y_{52.2} Y_{15.2}}{Y_{55.2}} \qquad A_{12.3} = A_{12.2} - \frac{A_{52.2} Y_{15.2}}{Y_{55.2}}$$

$$Y_{13.3} = Y_{13.2} - \frac{Y_{53.2} Y_{15.2}}{Y_{55.2}} \qquad A_{13.3} = A_{13.2} - \frac{A_{53.2} Y_{15.2}}{Y_{55.2}}$$

$$Y_{14.3} = Y_{14.2} - \frac{Y_{54.2} Y_{15.2}}{Y_{55.2}} \qquad A_{14.3} = A_{14.2} - \frac{A_{54.2} Y_{15.2}}{Y_{55.2}}$$

$$A_{15.3} = A_{15.2} - \frac{A_{55.2} Y_{15.2}}{Y_{55.2}}$$

$$A_{16.3} = A_{16.2} - \frac{A_{56.2} Y_{15.2}}{Y_{55.2}}$$

$$Y_{21.3} = Y_{21.2} - \frac{Y_{51.2} Y_{25.2}}{Y_{55.2}} \qquad A_{21.3} = A_{21.2} - \frac{A_{51.2} Y_{25.2}}{Y_{55.2}}$$

$$Y_{22.3} = Y_{22.2} - \frac{Y_{52.2} Y_{25.2}}{Y_{55.2}} \qquad A_{22.3} = A_{22.2} - \frac{A_{52.2} Y_{25.2}}{Y_{55.2}}$$

$$Y_{23.3} = Y_{23.2} - \frac{Y_{53.2} Y_{25.2}}{Y_{55.2}} \qquad A_{23.3} = A_{23.2} - \frac{A_{53.2} Y_{25.2}}{Y_{55.2}}$$

$$Y_{24.3} = Y_{24.2} - \frac{Y_{54.2} Y_{25.2}}{Y_{55.2}} \qquad A_{24.3} = A_{24.2} - \frac{A_{54.2} Y_{25.2}}{Y_{55.2}}$$

$$A_{25.3} = A_{25.2} - \frac{A_{55.2} Y_{25.2}}{Y_{55.2}}$$

$$A_{26.3} = A_{26.2} - \frac{A_{56.2} Y_{25.2}}{Y_{55.2}}$$

$$Y_{31.3} = Y_{31.2} - \frac{Y_{51.2} Y_{35.2}}{Y_{55.2}} \qquad A_{31.3} = A_{31.2} - \frac{A_{51.2} Y_{35.2}}{Y_{55.2}}$$

$$Y_{32.3} = Y_{32.2} - \frac{Y_{52.2} Y_{35.2}}{Y_{55.2}} \qquad A_{32.3} = A_{32.2} - \frac{A_{52.2} Y_{35.2}}{Y_{55.2}}$$

$$Y_{33.3} = Y_{33.2} - \frac{Y_{53.2} Y_{35.2}}{Y_{55.2}} \qquad A_{33.3} = A_{33.2} - \frac{A_{53.2} Y_{35.2}}{Y_{55.2}}$$

$$Y_{34.3} = Y_{34.2} - \frac{Y_{54.2} Y_{35.2}}{Y_{55.2}} \qquad A_{34.3} = A_{34.2} - \frac{A_{54.2} Y_{35.2}}{Y_{55.2}}$$

$$A_{35.3} = A_{35.2} - \frac{A_{55.2} Y_{35.2}}{Y_{55.2}}$$

$$A_{36.3} = A_{36.2} - \frac{A_{56.2} Y_{35.2}}{Y_{55.2}}$$

$$Y_{41.3} = Y_{41.2} - \frac{Y_{51.2} Y_{45.2}}{Y_{55.2}} \qquad A_{41.3} = A_{41.2} - \frac{A_{51.2} Y_{45.2}}{Y_{55.2}}$$

$$Y_{42.3} = Y_{42.2} - \frac{Y_{52.2} Y_{45.2}}{Y_{55.2}} \qquad A_{42.3} = A_{42.2} - \frac{A_{52.2} Y_{45.2}}{Y_{55.2}}$$

$$Y_{43.3} = Y_{43.2} - \frac{Y_{53.2} Y_{45.2}}{Y_{55.2}} \qquad A_{43.3} = A_{43.2} - \frac{A_{53.2} Y_{45.2}}{Y_{55.2}}$$

$$Y_{44.3} = Y_{44.2} - \frac{Y_{54.2} Y_{45.2}}{Y_{55.2}} \qquad A_{44.3} = A_{44.2} - \frac{A_{54.2} Y_{45.2}}{Y_{55.2}}$$

$$A_{45.3} = A_{45.2} - \frac{A_{55.2} Y_{45.2}}{Y_{55.2}}$$

$$A_{46.3} = A_{46.2} - \frac{A_{56.2} Y_{45.2}}{Y_{55.2}}$$

Eliminate node 4:

$$Y_{11.4} = Y_{11.3} - \frac{Y_{41.3} Y_{14.3}}{Y_{44.3}} \qquad A_{11.4} = A_{11.3} - \frac{A_{41.3} Y_{14.3}}{Y_{44.3}}$$

$$Y_{12.4} = Y_{12.3} - \frac{Y_{42.3} Y_{14.3}}{Y_{44.3}} \qquad A_{12.4} = A_{12.3} - \frac{A_{42.3} Y_{14.3}}{Y_{44.3}}$$

$$Y_{13.4} = Y_{13.3} - \frac{Y_{43.3} Y_{14.3}}{Y_{44.3}} \qquad A_{13.4} = A_{13.3} - \frac{A_{43.3} Y_{14.3}}{Y_{44.3}}$$

$$A_{14.4} = A_{14.3} - \frac{A_{44.3} Y_{14.3}}{Y_{44.3}}$$

$$A_{15.4} = A_{15.3} - \frac{A_{45.3} Y_{14.3}}{Y_{44.3}}$$

$$A_{16.4} = A_{16.3} - \frac{A_{46.3} Y_{14.3}}{Y_{44.3}}$$

$$Y_{21.4} = Y_{21.3} - \frac{Y_{41.3}Y_{24.3}}{Y_{44.3}} \qquad A_{21.4} = A_{21.3} - \frac{A_{41.3}Y_{24.3}}{Y_{44.3}}$$

$$Y_{22.4} = Y_{22.3} - \frac{Y_{42.3}Y_{24.3}}{Y_{44.3}} \qquad A_{22.4} = A_{22.3} - \frac{A_{42.3}Y_{24.3}}{Y_{44.3}}$$

$$Y_{23.4} = Y_{23.3} - \frac{Y_{43.3}Y_{24.3}}{Y_{44.3}} \qquad A_{23.4} = A_{23.3} - \frac{A_{43.3}Y_{24.3}}{Y_{44.3}}$$

$$A_{24.4} = A_{24.3} - \frac{A_{44.3}Y_{24.3}}{Y_{44.3}}$$

$$A_{25.4} = A_{25.3} - \frac{A_{45.3}Y_{24.3}}{Y_{44.3}}$$

$$A_{26.4} = A_{26.3} - \frac{A_{46.3}Y_{24.3}}{Y_{44.3}}$$

$$Y_{31.4} = Y_{31.3} - \frac{Y_{41.3}Y_{34.3}}{Y_{44.3}} \qquad A_{31.4} = A_{31.3} - \frac{A_{41.3}Y_{34.3}}{Y_{44.3}}$$

$$Y_{32.4} = Y_{32.3} - \frac{Y_{42.3}Y_{34.3}}{Y_{44.3}} \qquad A_{32.4} = A_{32.3} - \frac{A_{42.3}Y_{34.3}}{Y_{44.3}}$$

$$Y_{33.4} = Y_{33.3} - \frac{Y_{43.3}Y_{34.3}}{Y_{44.3}} \qquad A_{33.4} = A_{33.3} - \frac{A_{43.3}Y_{34.3}}{Y_{44.3}}$$

$$A_{34.4} = A_{34.3} - \frac{A_{44.3}Y_{34.3}}{Y_{44.3}}$$

$$A_{35.4} = A_{35.3} - \frac{A_{45.3}Y_{34.3}}{Y_{44.3}}$$

$$A_{36.4} = A_{36.3} - \frac{A_{46.3}Y_{34.3}}{Y_{44.3}}$$

Eliminate node 3:

$$Y_{11.5} = Y_{11.4} - \frac{Y_{31.4}Y_{13.4}}{Y_{33.4}} \qquad A_{11.5} = A_{11.4} - \frac{A_{31.4}Y_{13.4}}{Y_{33.4}}$$

$$Y_{12.5} = Y_{12.4} - \frac{Y_{32.4}Y_{13.4}}{Y_{33.4}} \qquad A_{12.5} = A_{12.4} - \frac{A_{32.4}Y_{13.4}}{Y_{33.4}}$$

$$A_{13.5} = A_{13.4} - \frac{A_{33.4}Y_{13.4}}{Y_{33.4}}$$

$$A_{14.5} = A_{14.4} - \frac{A_{34.4}Y_{13.4}}{Y_{33.4}}$$

$$A_{15.5} = A_{15.4} - \frac{A_{35.4}Y_{13.4}}{Y_{33.4}}$$

$$A_{16.5} = A_{16.4} - \frac{A_{36.4}Y_{13.4}}{Y_{33.4}}$$

$$Y_{21.5} = Y_{21.4} - \frac{Y_{31.4}Y_{23.4}}{Y_{33.4}} \qquad A_{21.5} = A_{21.4} - \frac{A_{31.4}Y_{23.4}}{Y_{33.4}}$$

$$Y_{22.5} = Y_{22.4} - \frac{Y_{32.4}Y_{23.4}}{Y_{33.4}} \qquad A_{22.5} = A_{22.4} - \frac{A_{32.4}Y_{23.4}}{Y_{33.4}}$$

$$A_{23.5} = A_{23.4} - \frac{A_{33.4}Y_{23.4}}{Y_{33.4}}$$

$$A_{24.5} = A_{24.4} - \frac{A_{34.4}Y_{23.4}}{Y_{33.4}}$$

$$A_{25.5} = A_{25.4} - \frac{A_{35.4}Y_{23.4}}{Y_{33.4}}$$

$$A_{26.5} = A_{26.4} - \frac{A_{36.4}Y_{23.4}}{Y_{33.4}}$$

Reduced Y and A matrix:

$Y_{11} = Y_{11.5}$ $Y_{12} = Y_{12.5}$ $Y_{21} = Y_{21.5}$ $Y_{22} = Y_{22.5}$

$Y_{11} = 0.001 + 0.003i \cdot ohm^{-1}$ $Y_{12} = -1.069 10^{-4} - 2.911 0^{-4} i \cdot ohm^{-1}$

$Y_{21} = 0.005 - 0.002i \cdot ohm^{-1}$ $Y_{22} = 8.586 10^{-4} + 0.003i \cdot ohm^{-1}$

$B = (A_{11.5}\ A_{12.5}\ A_{13.5}\ A_{14.5}\ A_{15.5}\ A_{16.5})$ $D = (A_{21.5}\ A_{22.5}\ A_{23.5}\ A_{24.5}\ A_{25.5}\ A_{26.5})$

$B = (-0.876 + 0.319i \quad 0.016 + 0.018i \quad 0.108 + 0.294i \quad 0.016 + 0.025i \quad -4.229 10^{-4} - 0.007i \quad 4.229 10^{-4} + 0.007i)$

$D = (0.922 - 0.301i \quad -0.916 + 3.139 10^{-4} i \quad 0.842 - 0.266i \quad 0.08 - 0.034i \quad 0.004 + 0.035i \quad 1.996 - 0.035i)$

Conversions between Y and S parameters

$$S_{11} = \frac{(Y_o - Y_{11}) \cdot (Y_o + Y_{22}) + Y_{12} Y_{21}}{(Y_{11} + Y_o) \cdot (Y_{22} + Y_o) - Y_{12} Y_{21}}$$

$$S_{12} = \frac{-2 \cdot Y_{12} Y_o}{(Y_{11} + Y_o) \cdot (Y_{22} + Y_o) - Y_{12} Y_{21}}$$

$$S_{21} = \frac{-2 \cdot Y_{21} Y_o}{(Y_{11} + Y_o) \cdot (Y_{22} + Y_o) - Y_{12} Y_{21}}$$

$$S_{22} = \frac{(Y_o + Y_{11}) \cdot (Y_o - Y_{22}) + Y_{12} Y_{21}}{(Y_{11} + Y_o) \cdot (Y_{22} + Y_o) - Y_{12} Y_{21}}$$

Noise parameters:

$$R_n = \frac{1}{4 \cdot k \cdot T} \cdot Re\left[\frac{1}{(Y_{21})^2} \cdot \overline{D} \cdot C \cdot D^T\right]$$

$$G_i = \frac{1}{4 \cdot k \cdot T} \cdot Re\left(\left(B - \frac{Y_{11}}{Y_{21}} \cdot D\right) \cdot C \cdot \left(B - \frac{Y_{11}}{Y_{21}} \cdot D\right)^T\right) \qquad G_i = 0.002 ohm^{-1}$$

$$Y_{cor} = \frac{-\left(R_n \cdot \overline{Y_{21}}\right)^{-1} \cdot \left(\overline{D} \cdot C \cdot \left(B - \frac{Y_{11}}{Y_{21}} \cdot D\right)^{T}\right)}{4 \cdot k \cdot T} \qquad Y_{cor} = 7.507 \cdot 10^{-4} + 0.002i \ \cdot ohm^{-1}$$

$$G_{cor} = Re\left(Y_{cor}\right)$$

$$B_{cor} = Im\left(Y_{cor}\right)$$

$$B_{opt} = -B_{cor} \qquad B_{opt} = -0.002 \cdot ohm^{-1}$$

$$G_{opt} = \sqrt{G_i \cdot \left(R_n^{-1}\right) - B_{cor}^{2}} \qquad G_{opt} = 0.001 \cdot ohm^{-1}$$

$$f_{min} = 1 + 2 \cdot R_n \cdot \left(G_{cor} + G_{opt}\right) \qquad f_{min} = 2.72 \qquad G_{cor} = 7.507 \cdot 10^{-4} \ \cdot ohm^{-1}$$

$$Y_{opt} = G_{opt} + j \cdot B_{opt}$$

$$Z_{opt} = \frac{1}{Y_{opt}}$$

$$R_{opt} = Re\left(Z_{opt}\right)$$

$$X_{opt} = Im\left(Z_{opt}\right)$$

Noise parameters:

WRITE(fmin) $= f_{min}$ $\quad G_{opt} = 0.001 \cdot ohm^{-1}$

F_{min} = READ(fmin) $\quad B_{opt} = -0.002 \cdot ohm^{-1}$

$F_{min} = 2.72$

$10 \cdot \log\left(F_{min}\right) = 4.346$ (dB)

$R_{opt} = 227.8 \cdot ohm$

$X_{opt} = 372.029 \cdot ohm$

S parameters of two-port network

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} = \begin{pmatrix} 0.867 - 0.235i & 0.016 + 0.023i \\ -0.35 + 0.28i & 0.883 - 0.233i \end{pmatrix}$$

$$|S_{11}| = 0.898 \qquad \frac{\arg\left(S_{11}\right)}{\pi} \cdot 180 = -15.165 \quad \text{(degree}$$

$$|S_{21}| = 0.448 \qquad \frac{\arg\left(S_{21}\right)}{\pi} \cdot 180 = 141.354 \quad \text{(degree}$$

$R_n = 441.509\,ohm$

$\frac{R_n}{50} = 8.83\,ohm$

$|S_{12}| = 0.028 \quad \frac{\arg(S_{12})}{\pi}\cdot 180 = 55.705 \quad (degree)$

$\left|\frac{R_{opt} + j\cdot X_{opt} - Z_o}{R_{opt} + j\cdot X_{opt} + Z_o}\right| = 0.888$

$|S_{22}| = 0.914 \quad \frac{\arg(S_{22})}{\pi}\cdot 180 = -14.795 \quad (degree)$

$\frac{\arg\left(\frac{R_{opt} + j\cdot X_{opt} - Z_o}{R_{opt} + j\cdot X_{opt} + Z_o}\right)}{\pi}\cdot 180 = 11.205$

Noise parameters based on the simplified small-signal model

$\omega := 2\cdot\pi\cdot 2\cdot 10^9\cdot Hz, 2\cdot\pi\cdot 2.5\cdot 10^9\cdot Hz .. 2\cdot\pi\cdot 6\cdot 10^9\cdot Hz$

$$NF_{min}(\omega) := 1 + \frac{1}{2}\cdot\sqrt{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}}\cdot R_G\cdot\omega\cdot C_{GS}\cdot\frac{\sqrt{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}}\cdot\omega\cdot C_{GS} + \sqrt{\omega^2\cdot C_{GS}^2\cdot\left(\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}\right) + \frac{4\cdot k\cdot T}{R_G}\cdot g_m^2}}{g_m^2\cdot k\cdot T}$$

$$R_n(\omega) := \frac{1}{4\cdot k\cdot T}\cdot\left(\frac{1 + R_G^2\cdot\omega^2\cdot C_{GS}^2}{g_m^2}\cdot\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do} + R_G^2\cdot\frac{4\cdot k\cdot T}{R_G}\right)$$

$$G_{opt}(\omega) := \frac{\sqrt{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}}\cdot R_G\cdot\omega\cdot C_{GS}\cdot\sqrt{\omega^2\cdot C_{GS}^2\cdot\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do} + \frac{4\cdot k\cdot T}{R_G}\cdot g_m^2}}{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do} + \alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}\cdot R_G^2\cdot\omega^2\cdot C_{GS}^2 + R_G^2\cdot\frac{4\cdot k\cdot T}{R_G}\cdot g_m^2}$$

$$B_{opt}(\omega) := -1\cdot\frac{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}\cdot\omega\cdot C_{GS}}{\alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do} + \alpha_{sat}\cdot 4\cdot k\cdot T\cdot g_{do}\cdot R_G^2\cdot\omega^2\cdot C_{GS}^2 + R_G^2\cdot\frac{4\cdot k\cdot T}{R_G}\cdot g_m^2}$$

$$Z_{opt}(\omega) := \frac{1}{G_{opt}(\omega) + j\cdot B_{opt}(\omega)} \qquad \Gamma_{opt}(\omega) := \frac{Z_{opt}(\omega) - Z_o}{Z_{opt}(\omega) + Z_o}$$

$$r_n(\omega) := \frac{R_n(\omega)}{50 \cdot ohm}$$

$NF_{min}(\omega)$	$10 \cdot \log(NF_{min}(\omega))$	$r_n(\omega)$	$\lvert\Gamma_{opt}(\omega)\rvert$	$\frac{\arg(\Gamma_{opt}(\omega))}{\pi} \cdot 180$
1.388	1.424	7.773	0.958	2.654
1.505	1.776	7.826	0.948	3.295
1.631	2.125	7.892	0.938	3.922
1.766	2.47	7.969	0.928	4.533
1.911	2.812	8.058	0.918	5.124
2.065	3.149	8.159	0.908	5.696
2.23	3.482	8.271	0.898	6.245
2.405	3.811	8.396	0.889	6.77
2.591	4.134	8.533	0.879	7.271

$$WRITEPRN(noiseint) := \left(\frac{\omega}{2 \cdot \pi \cdot GHz} \quad 10 \cdot \log(NF_{min}(\omega)) \quad \lvert\Gamma_{opt}(\omega)\rvert \quad \frac{\arg(\Gamma_{opt}(\omega))}{\pi} \cdot 180 \quad r_n(\omega) \right)$$