InAs/AlSb Heterostructure Field-Effect Transistors

by

Martin W. Dvorak
B.Sc. (Eng.), Queen's University, 1995

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NAME: Martin Dvorak

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EXAMINING COMMITTEE:

Chairman: Dr. Shawn Stapleton

Dr. Colombo R. Bolognesi
Senior Supervisor

Dr. Simon P. Watkins
Supervisor

Dr. David H. Chow
External Examiner
Hughes Research Laboratories, Malibu, CA

DATE APPROVED: August 7 1997

ABSTRACT

Heterostructure field-effect transistors (HFETs) based on AlSb/InAs/AlSb quantum wells have demonstrated significant high speed performance: 0.5 μm gate HFETs with cut-off frequencies f_T of 93 GHz at drain voltages of 1 V have been achieved. The Γ-L intervalley separation of ~0.9 eV in InAs, large InAs/AlSb interface conduction band discontinuity of ~1.35 eV, and high room temperature mobilities of 20,000-30,000 $cm^2/V \cdot s$ make this material system very attractive for low-power, high speed transistor applications.

Because of the relatively narrow band gap of InAs (~0.36 eV), these HFETs are subject to several impact ionization related non-idealities, some of which may involve trapping of holes generated by impact ionization. The DC drain characteristics feature an abruptly increased output conductance with increasing drain bias (kink effect). In the present dissertation, two methods aiming to reduce impact ionization effects were studied. The first approach was the fabrication of dual gate HFETs which have demonstrated significant improvements over single gate HFETs under DC operating conditions. Secondly, quantum confinement was used to increase the quantization energies and the effective forbidden energy gap within the InAs quantum well in an effort to increase the impact ionization threshold. Temperature and frequency dependent sidegating measurements were also used to provide the first evidence for the effect of hole traps in InAs/AlSb HFET buffer layers.

Microwave measurements show a strong dependence on the quantum well width: the higher mobility in wider wells result in superior frequency performance that is likely due to an enhanced peak electron velocity in the channel. At microwave frequencies, conventional microwave FET models prove to be inappropriate because they do not account for impact ionization effects which become progressively severe in wider wells. In the course of this work, we have fabricated 0.55 μm gate InAs/AlSb HFETs with a unity current gain

cut-off frequency f_T = 67GHz: these are some of the fastest FETs ever fabricated for that gatelength.

ACKNOWLEDGEMENTS

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Introduction

Overview

In this introductory Chapter, we briefly review the basics of III-V compound semiconductor high-speed metal semiconductor field-effect transistors (MESFETs) and heterostructure field-effect transistors (HFETs). The concept of modulation efficiency developed by Foisy is introduced and used to explain the evolutionary trends in the development of high speed III-V field-effect transistors. Modulation efficiency provides a useful framework to demonstrate the potential advantages of the InAs/AlSb material system for low-power HFET applications. Previous works, and works performed concurrently by other groups on the InAs/AlSb system are then briefly reviewed. Finally, the scope of the present dissertation is summarized.

1.1 Compound semiconductor MESFETs & HFETs

The transistor can generally be described as a three-terminal electronic device in which the current between two terminals is controlled by the third terminal. In a field-effect transistor, the control electrode is the gate and current flows from the drain to the source in a conductive channel. The gate control is of a capacitive nature, through an insulator or a depletion region, and modulates the conductivity of the charge carrying

channel. Hence, the current through the drain is modulated by the potential applied to the gate.

By far the most widely used transistor technology in use today is the silicon MOSFET (metal-oxide-semiconductor FET). In a MOSFET, the conducting semiconductor channel is capped with an insulating silicon oxide film, and the gate is placed on top of the oxide to either induce or deplete a current-carrying channel between the source and drain electrodes.

Although there is no doubt of the continued dominance of MOSFETs for the vast majority of microelectronics applications, compound semiconductor MESFETs (metal semiconductor FETs, with a Schottky barrier in place of the oxide layer of MOSFETs) and HFETs (heterostructure FETs, like a MESFET but with the channel defined by at least one heterointerface between two different semiconductors) have carved out a niche in two important markets: optoelectronics, and microwave and millimeter wave (i.e. very high speed) applications. The explanation for the former is that silicon is an indirect band-gap material characterized by a very low optical emission quantum efficiency: as such, it is unsuitable in the context of monolithically integrated light emitters and transistors. The high electron mobility and peak velocity of direct gap compound semiconductors makes them attractive for the fabrication of high speed electronic devices, with the added advantage of the possibility for band gap engineering. Once the relevant factors are considered, the InAs/AlSb material system emerges as an excellent candidate for the realization of the ultimate high frequency transistor, if certain technological problems can be solved.

Table 1-1 : Material properties of selected semiconductors at 300K[a]

Material	Energy gap (eV)	Transition type and symmetry points	Mobility: electrons	Mobility: holes	Electron drift velocity (10^7 cm/s)
Si	1.12	indirect: $\Gamma_{25'v}-\Delta_{1c}$	1,350	480	~1[b]
Ge	0.66	indirect: $\Gamma_{8v}-L_{6c}$	3,600	1,800	
AlAs	2.15	indirect: $\Gamma_{15v}-X_{1c}$	280	~200[c]	
AlSb	1.58	indirect: $\Gamma_{15v}-\Delta_{1c}$	900	<400	
GaP	2.26	indirect: $\Gamma_{15v}-\Delta_{1c}$	300	150	
GaAs	1.42	direct: $\Gamma_{8v}-\Gamma_{6c}$	5,000-8,000	300	1.8[d]
GaSb	0.72	direct: $\Gamma_{8v}-\Gamma_{6c}$	5,000	1,000	
InP	1.35	direct: $\Gamma_{8v}-\Gamma_{6c}$	4,500	100	2.4[d]
InAs	0.36	direct: $\Gamma_{8v}-\Gamma_{6c}$	20-30,000	450	3.5[d]
InSb	0.17	direct: $\Gamma_{8v}-\Gamma_{6c}$	80,000	450	6.1[e]

a. From Sze [68] except where otherwise indicated
b. Saturated electron velocity [17]
c. From Madelung [44]
d. Peak electron velocity [17]
e. Saturated electron velocity [77]

Consideration of the bulk electronic properties such as the peak velocity and the low-field mobility of various semiconductors (see Table 1-1) leads one to anticipate that compound semiconductors should be suitable for the fabrication of high-speed field-effect transistors. Another advantage of compound semiconductors is that semi-insulating GaAs substrates are widely available, facilitating the integration of microwave circuit elements, such as low-loss spiral inductors and waveguides. Because of the unavailability of high-quality III-V compound semiconductor surface oxides, compound semiconductor FETs have instead relied on rectifying Schottky metal-semiconductor contacts to implement the control terminal. The geometry of a typical n-channel MESFET is given in Figure 1-1, and representative drain current-voltage characteristics for a GaAs MESFET fabricated by the author in the SFU Compound Semiconductor Device Laboratory (CSDL) are shown in Figure 1-2.

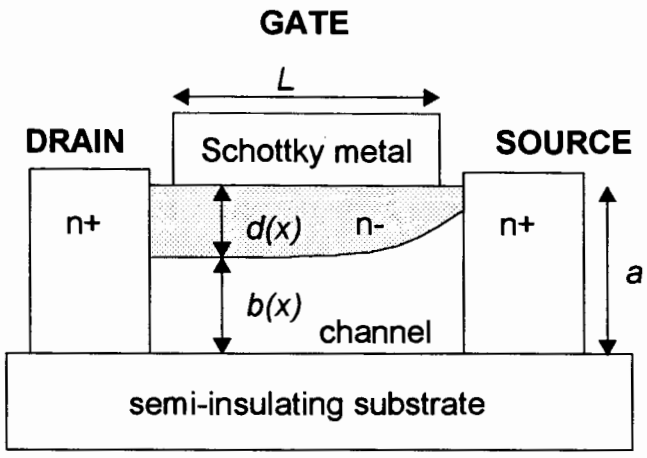

Figure 1-1 : Schematic cross-section of a conventional MESFET.

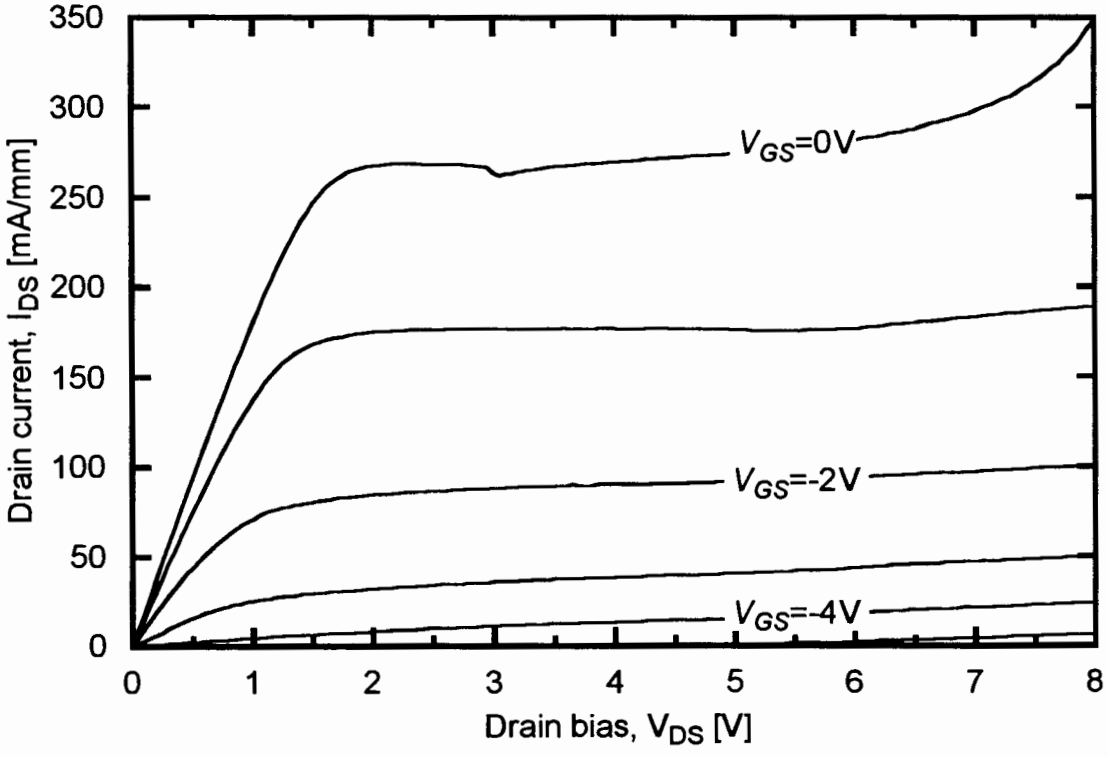

Figure 1-2 : Representative I-V characteristics of a GaAs MESFET fabricated in the CSDL.

In an n-channel MESFET, an Ohmic contact at the source supplies the electrons to the conducting channel underneath the gate; conventional current flows from the drain to the source. Electrons are confined to the channel by Coulombic forces either by an insulating substrate, or by p-doping the buffer layers. Under bias, the Schottky contact at the surface results in a depletion region of varying thickness *d(x)* because of the varying gate-channel bias along the length of the channel, as shown in Figure 1-1. The gate bias therefore controls the cross-section of the channel, and the channel opening is shown to be [40]:

$$b(x) = a\left(1 - \sqrt{\frac{V_{bi} - V_{GS} + V(x)}{V_P + V_{bi}}}\right) \tag{1–1}$$

Here $V_P + V_{bi}$ represents the total reverse voltage required to close (or "*pinch off*") the channel completely. Increasing drain biases lead to channel pinch off at the drain side of the gate and result in a saturation of the drain current.

Another current saturation mechanism is possible in III-V FETs because of the high electron mobility. In a high mobility material, electrons are quickly accelerated according to

$$v_{drift} = \mu E \tag{1–2}$$

where μ is the low-field mobility, and E is the electric field. For fields exceeding a given critical value E_{sat} the velocity saturates at v_{sat}. To a first approximation, the drift velocity dependence upon electric field can be represented by the piecewise linear relation:

$$v = \begin{cases} \mu E, E < E_{sat} \\ \text{or} \\ v_{sat} = \mu E_{sat}, E \geq E_{sat} \end{cases} \tag{1–3}$$

Because of current continuity (assuming to first order zero gate leakage current), the drain current per unit channel width is given by:

$$I_{DS} = qnb(x)v(x) \ [\text{mA/mm}] \tag{1-4}$$

where $v(x)$ is the electron velocity in the channel as a function of position, n is the charge density in the channel and b is the channel thickness at x. With current constant along the channel, and a peak electron velocity $v(x)$ equal to the saturated electron velocity, the current through the channel can saturate before channel pinch off occurs at the drain end. A classical example of this behavior is seen in Figure 1-2: the drain current I_{DS} saturates at $V_{DS} \sim 2\,\text{V}$ for $V_{GS} = 0\,\text{V}$, while the channel pinch-off voltage is $V_{GS} \sim -4.5\,\text{V}$.

Assuming that transport occurs under velocity saturation through the whole channel results in a uniform channel cross-section:

$$I_{DS} = qnbv_{sat} \tag{1-5}$$

The current drive capability of a FET is determined by its transconductance

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} \tag{1-6}$$

Rewriting the drain current as [62]

$$I_{DS} = qnbv_{eff} \approx \frac{Q_G v_{eff}}{L} \tag{1-7}$$

where Q_G is the charge under the gate normalized to unit transistor width, the transconductance is found to be

$$g_m \approx \frac{\partial Q_G}{\partial V_G}\frac{v_{eff}}{L} \approx \frac{v_{eff}C_G}{L} \approx \frac{v_{sat}C_G}{L} \tag{1-8}$$

Here $C_G \approx C_{GD} + C_{GS}$ is the total gate capacitance, L is the gate length, and v_{eff} is the effective velocity of electrons in the channel. When velocity saturation prevails over most

of the channel we can approximate $v_{eff} = v_{sat}$: this assumption is often made and justified on the basis of the high mobilities in direct gap III-V compound semiconductors. By examining the simplified *small-signal equivalent circuit* of the MESFET it becomes clear that for high-frequency performance the transconductance must be maximized to quickly charge device (and parasitic) capacitances (see Figure 1-3).

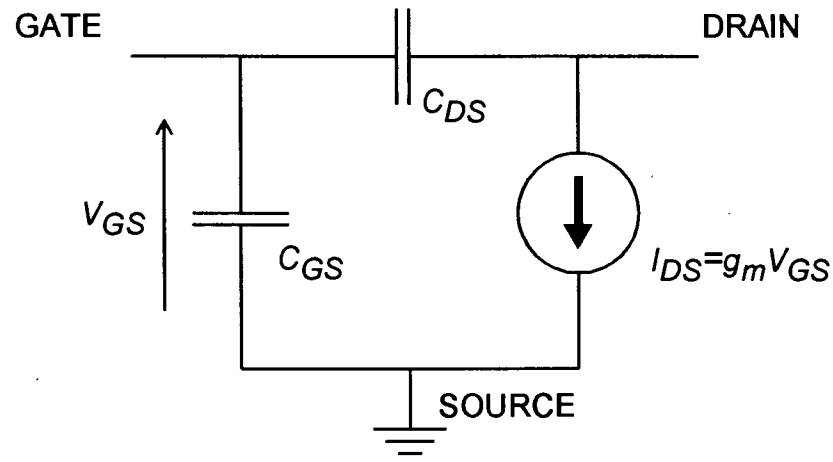

Figure 1-3 : Simplified small-signal equivalent circuit of MESFET or HFET.

A quantity of particular interest is the unity current gain cutoff frequency f_T of the FET. It is defined as the frequency at which the magnitude of the input current equals the magnitude of the output current when the output is short-circuited to ground. It is easily shown to equal

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \approx \frac{v_{sat}}{2\pi L} \qquad (1\text{–}9)$$

From this equation, it would seem that improving the transport properties of electrons in the channel (i.e. increasing $v_{eff} \sim v_{sat}$) and reducing the FET gate length L should proportionately increase the cutoff frequency. It should be emphasized that this is the maximum possible f_T of a FET. The saturated velocity is fixed by the choice of materi-

als through their band structure, while the gate length L is limited by technological considerations.

In practical devices, however, as the aspect ratio of gate length to channel thickness L/d is reduced with shrinking gate length, the device begins to suffer from non-idealities collectively known as "short-channel effects:" effectively, the gate loses control of the channel current. For example, an abrupt increase in output conductance appears at higher drain voltages (the kink effect). These non-ideal effects are with few exceptions[1] deleterious to device performance and lead to such non-idealities as a shift of threshold voltage with gate length and increased output conductance in the saturation regime. Such short-channel effects can be reduced by scaling the channel with the gate length. Thinner channels, however, require proportionally higher doping densities to maintain the drain current density. Unfortunately, increased ionized impurity scattering reduces the low-field mobility and the effective electron velocity v_{eff} in the channel. Clearly, there are diminishing returns to be gained by thinning channels when bulk material properties are relied upon.

The demonstration of modulation doping in AlGaAs/GaAs heterojunctions by Dingle [24] permitted the realization of high mobility high concentration electron gases in narrow *undoped* semiconductor layers, thus allowing higher FET aspect ratios with heterostructures. The term "modulation doping" specifically refers to the spatial separation between parent dopant impurities and the resulting free carriers. This is accomplished as follows: Two semiconductors are placed in intimate contact across a high-quality interface. The material with the higher conduction band edge energy (and generally the wider bandgap) is doped with donors, and the narrower gap semiconductor remains undoped. As a result, electrons accumulate in the undoped material until the Coulombic interactions

1. one exception being deep-submicron FETs with ballistic and velocity overshoot effects, which can yield $v_{eff} > v_{sat}$ because the peak velocity v_{peak} can be several times v_{sat}

between the accumulated electrons and the ionized donors cause the net potential energy to be minimized. Because of the dynamic confinement of electrons in the direction perpendicular to the interface, a quasi-two dimensional electron gas (2DEG) is formed and is free to move in the interface plane.

With the high mobilities (>5000 cm^2/Vs) and 2DEG conductivities possible with modulation doping, several groups designed FETs using modulation-doped layers as conducting channels [47][23]. For a number of years development proceeded under the assumption that higher mobilities alone would lead to improved FET performance (the assumption arose from large high frequency performance (cutoff frequency) improvements observed at cryogenic temperatures which coincided with mobility enhancements in GaAs/AlGaAs quantum wells). It was not until Foisy [30] introduced the concept of modulation efficiency that it was fully understood that the improvements to the low-field transport properties in the channel due to the modulation doping were only partly responsible for the improved high-frequency performance of FETs. For this reason, the term "HEMT" for "High electron mobility transistor" is somewhat misleading, and the more descriptive "HFET" for "Heterostructure FET" is preferred in this dissertation.

The increase in f_T achieved through the use of heterostructures in FETs can be understood by examining the concept of modulation efficiency [30]. Modulation efficiency is a simple technique of accounting for the difference between actual and measured device performance, by incorporating all non-idealities in a single coefficient η. Foisy's analysis was developed for HFETs, but the concept also helps explain the high-frequency performance behavior of MESFETs. The transconductance in equation (1-8) was calculated under the assumption of complete velocity saturation in the channel. Foisy showed that in practice it is important to consider the unsaturated regions of the channel as well: this can be done in a first order approximation by using the piecewise-linear saturated velocity model (1-3). The drain current can be shown to equal [56]:

$$I_{DS} = C_G v_{sat}(\sqrt{(E_{sat}L)^2 + (V_G - V(0) - V_{th})} - E_c L) \tag{1-10}$$

where the bias $V(0)$ is the channel voltage at the source end of the gate, V_{th} is the threshold voltage and E_{sat} is the velocity saturation electric field. From this, using the definition for transconductance (1-6), we find

$$g_m = C_G v_{sat} \frac{V_G - V(0) - V_{th}}{\sqrt{(V_G - V(0) - V_{th}) + (E_{sat}L)^2}}. \tag{1-11}$$

If one expresses the independent parameter V_G in terms of the sheet concentration n_s in the linear approximation, using the definition $qn_s = C_G(V_G - V(0) - V_{th})$, and the difference n_c between the sheet densities at the drain and source ends of the gate:

$$n_c \sim n_s(0) - n_s(L) = E_{sat}C_G/q \tag{1-12}$$

then the transconductance becomes

$$g_m = C_G v_{sat} \frac{1}{\sqrt{1 + (n_c/n_s)^2}} \tag{1-13}$$

where the second term is the modulation efficiency:

$$\eta = \frac{1}{\sqrt{1 + (n_c/n_s)^2}} \tag{1-14}$$

For the sake of simplicity, the above model does not include another important non-ideality in a FET: the modulation of parasitic low-mobility current component that can flow outside the quantum well. Foisy expressed the modulation efficiency as [30]:

$$\eta = \frac{\partial Q_{SVM}}{\partial(Q_{SVM} + Q_{\Delta GC} + Q_{SL})} \tag{1-15}$$

The charge Q_{SVM} represents the charge required to provide the measured drain current under the saturated velocity model:

$$Q_{SVM} = \frac{I_D L}{v_{sat}} \tag{1-16}$$

$Q_{\Delta GC}$ denotes the charge required to account for the non-constant velocity in the channel. Q_{SL} denotes additional parasitic charge present outside the conducting channel, but located in the electron supply layers which normally consist of very low mobility material which behaves as a parasitic MESFET layer. Q_{SL} must be determined by a self-consistent numerical solution to the Poisson and Schroedinger equations along the gate electrode. The current gain cutoff frequency f_T becomes:

$$f_T = \frac{v_{sat}}{2\pi L} \times \frac{\partial Q_{SVM}}{\partial (Q_{SVM} + Q_{\Delta GC} + Q_{SL})} \tag{1-17}$$

From (1-15) we see that modulation efficiency must be in the range $0 \le \eta \le 1$. In the best case, all charge that is modulated by the gate bias is in fact in the conducting channel and moving with velocity v_{sat}.

Let us now consider how to improve the modulation efficiency in HFETs. The fundamental principle to be taken away from (1-14) and (1-17) is that we must maximize the fraction of modulated charge that is actually in the conducting channel. Any charge that accumulates in low-mobility barrier layers reduces the modulation efficiency. For electrons, the conduction band discontinuity determines the maximum sheet concentration n_{sm} that can be confined before electrons begin to populate the barrier layers. Furthermore, when there is no parasitic charge modulation, the modulation efficiency is still reduced due to the presence of an unsaturated portion of the channel as indicated in (1-14).

To maximize the cutoff frequency of HFETs one therefore seeks a material combination that allows excellent transport properties (for both high low-field mobility and a high v_{sat}), and a large conduction band discontinuity (for an excellent electron confinement, the highest maximum sheet charge concentration, and a good modulation efficiency). As seen below, these optimal conditions are met in the InAs/AlSb material

system. Historically, higher modulation efficiencies were achieved adding In to GaAs quantum wells to form strained AlGaAs/GaInAs quantum wells on GaAs substrates, and subsequently, by the development of lattice-matched ($\Delta E_C = 0.52\text{eV}$) and strained GaInAs/AlInAs quantum wells on InP substrates.

1.2 InAs/AlSb HFETs

The accepted bulk band gaps and lattice constants of III-V compounds are shown in Figure 1-3. As highlighted in the Figure, the largest difference in band gaps among a single nearly lattice matched material family is within the 6.1 Å family: AlSb/GaSb/InAs. What is of special interest, however, is the band lineup at interfaces

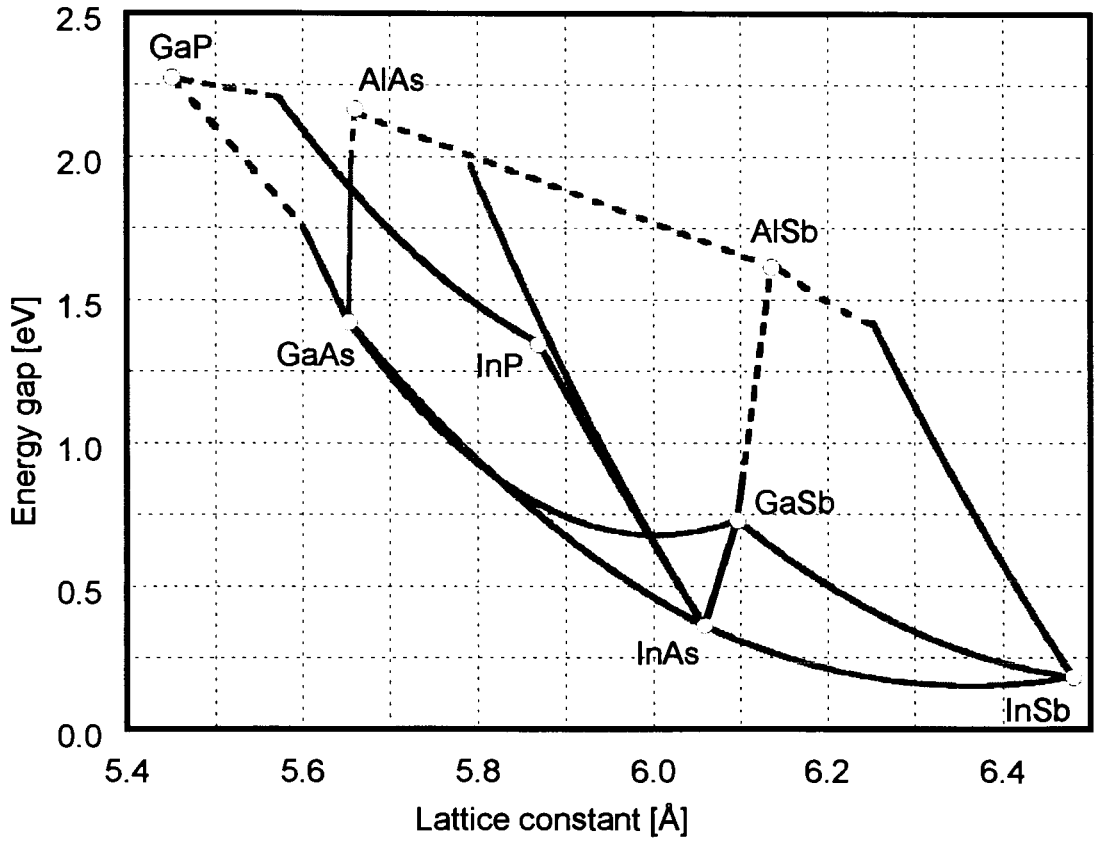

Figure 1-4 : Energy gap vs. lattice constant for III-V compound semiconductors of most interest. The 6.1Å family is blackened.

between two of these materials. From the valence band offset for the InAs/GaSb ($E_{v,InAs/GaSb}$ ~ 0.5eV) and AlSb/GaSb ($E_{v,AlSb/GaSb}$ ~ 0.35-0.40eV) interfaces and from the energy gaps of AlSb ($E_{gap,AlSb}$ ~ 1.58eV) and InAs ($E_{gap,InAs}$ ~ 0.36eV), a slightly staggered band configuration $E_{v,InAs/AlSb} = E_{v,InAs/GaSb} - E_{v,AlSb/GaSb}$ ~ 0.10-0.15 eV and $E_{c,InAs/AlSb} = E_{v,InAs/AlSb} + (E_{gap,AlSb} - E_{gap,InAs})$ ~ 1.32-1.37eV is predicted by the transitivity postulate [50]. This has been confirmed experimentally by Nakagawa *et al.* [50] who measured a conduction band offset of ~ 1.35eV. Dandrea *et al.* [21] theoretically showed that the 1.6% lattice mismatch strain in InAs/AlSb heterojunctions results in a strain-induced narrowing of the InAs gap, leading to a valence band discontinuity of approximately ~ 0.04-0.10eV. The currently accepted band lineup used in this study is given in Figure 1-5.

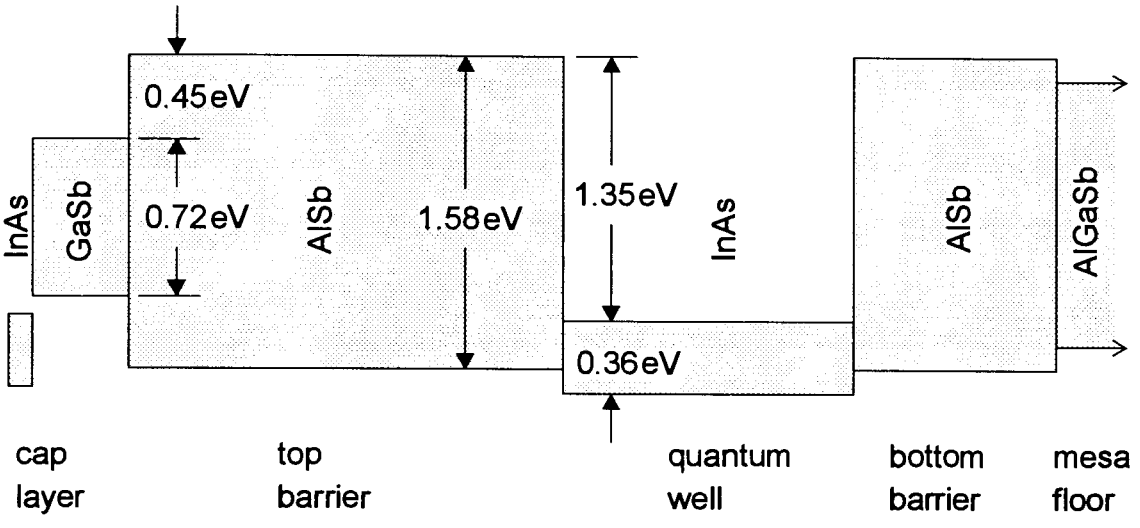

Figure 1-5 : Basic band structure of HFET active layers used in this study.

The very deep quantum well for electrons provided by this material system and the high mobility of InAs at room temperature present a favorable combination of material properties unmatched by any other III-V heterostructure system. As shown by Bolognesi [5], mobilities of 20,000-30,000 $cm^2/V \cdot s$ are readily achievable for quantum wells of widths of 100-150 Å.

1.2.1 Difficulties with InAs/AlSb HFETs

There are certain difficulties inherent to the InAs/AlSb material system that must be addressed in any study of this type:

a) First and foremost is the abrupt increase in output conductance (the kink effect) in InAs/AlSb HFETs operated at drain biases higher than $V_{DS} \sim 0.5$V: see Figure 3-8 on page 48 for example. The appearance of the kink effect has been related to impact ionization in the channel and it has been suggested that traps in buffer layers may interact with the generated holes to amplify the kink effect [39]. The narrow bandgap of InAs coupled with the presumed high trap density in the AlSb barriers make the kink effect particularly noticeable in this material system. Deep levels, which are not completely understood in well-characterized systems, have not yet been identified for InAs/AlSb HFETs. Their effect on device performance also remains unclear. Major portions of the present dissertation address impact ionization and trapping phenomena in InAs/AlSb HFETs.

b) AlSb oxidizes readily in ambient air and is etched relatively easily by alkaline solutions compared to most semiconductors. Because standard photolithographic developers are alkaline, precautions are required to avoid unintended etching of AlSb. The use of InAs/GaSb bilayer caps and the introduction of small quantities of Ga into AlSb layers together can alleviate these problems.

c) This remains a new technology, compared with the InP and GaAs lattice matched material systems. The anticipated high-frequency performance advantage of InAs-based HFETs has yet to be fully reached.

1.2.2 Other work on InAs/AlSb HFETs

The fact that InAs/AlSb quantum well HFETs (Figure 1-5 on page 13) provide the deepest quantum wells and highest mobilities of any lattice-matched material sys-

tem has generated some interest from the research community [19]. The first report of InAs/AlSb HFETs was made by the Santa Barbara group [71]. Because the growth and fabrication technology for devices using this material system was still in its infancy, that and another early work [84] should be considered as proof-of-concepts. At that time, the reasons for the successes and shortcomings of the devices were not understood.

The first breakthrough came with Tuttle's success in growing high mobility InAs/AlSb quantum wells [72][73]. His identification of the role of shutter sequencing at AlSb-InAs interfaces and the effects on the low-field electronic transport properties of the quantum wells paved the way for achieving the transport properties now available in InAs/AlSb quantum wells.

Several groups contributed to the "first generation" of InAs/AlSb HFETs. Still at Santa Barbara, Werking and Bolognesi continued building on the work of Tuttle. Werking *et al.* [78] demonstrated that Ar ion-implantation failed to provide adequate device isolation, and also investigated reactive ion etching schemes for the material system [79]. Yoh *et al.* [84] reported the first successful channel pinch-off in InAs/AlSb HFETs operating at room temperature. Their devices were plagued by a severe kink effect. Nearly kink-free devices were later reported by Wang's group at Columbia University [42], but no satisfactory explanation for the absence of the kink was provided. It was speculated that their undoped structure may have benefited from unintentional (and irreproducible) charge compensation from a high background Te contamination in their MBE chamber.

The breakthrough in the reliable fabrication of InAs/AlSb HFETs with improved DC and microwave characteristics came with the Ph.D. work of Bolognesi [5]. The growth of high mobility InAs/AlSb quantum wells (continuing the work of Tuttle [72]) was improved and made more reproducible, and a reliable process for the fabrication of InAs/AlSb HFETs was developed. Some of the HFET gate leakage current was shown

to arise from impact ionization in the channel, and the kink effect was tentatively explained as resulting from the accumulation of impact ionization generated holes in the buffer layers. This work was followed by Brar *et al.* [13] who furthered the understanding of the kink effect through the demonstration of the effect of back-gating on the kink. In his Ph.D. dissertation, he also presented evidence that the gate diode leakage current can be largely due to thermionic emission of holes generated at the InAs/AlSb interface [12].

Among other groups currently active in this field, the group at Naval Research Laboratories has many published results for InAs/AlSb HFETs [6]-[11],[37],[38]. They have demonstrated the smallest gate geometries this material system, and have reported novel successful Ohmic contact schemes. The NRL group has claimed a 50 GHz·μm performance with 0.5 μm HFETs, but has been unsuccessful in maintaining this performance in 0.1-0.2 μm HFETs. They have provided no explanation for this failure. The Columbia University group recently published results on an Ohmic contact study [85] which was not of the quality of [10]. Of great interest is the recent work by Miya *et al.* from the Asahi Chemical Industry Co. in Japan, who have applied expertise gained on InAs-based Hall effect sensors to the fabrication of InAs/AlGaAsSb HFETs, avoiding the problem of thick, low-quality AlSb buffer layers [49]. Other relevant InAs-based works include the strain compensated InAs inserted-channel HFETs on InP demonstrated by Xu *et al.* in Germany [83] and Chin *et al.* in Taiwan [20]. They have matched or exceeded the best microwave performance of InAs/AlSb HFETs: with a ~50 GHz·μm frequency performance at longer gatelengths $L > 0.5$ μm, and ~35 GHz·μm at shorter gatelengths, an $f_T = 265$ GHz was reported for a 0.13 μm gatelength device [83]. The InAs inserted-channel HFET on InP is a direct challenge to the AlSb/InAs/AlSb deep quantum well HFET, because the approach takes advantage of the high mobility and saturated velocity of InAs while maintaining the technological benefits of better-known InP materials.

1.3 Scope of dissertation

The mandate of this research is, in broad terms, to advance the development and understanding of InAs/AlSb HFETs. Attempts to minimize the kink effect were made by implementing dual-gate HFETs and by increasing the impact ionization threshold by using thinner InAs quantum wells. Because buffer layer traps have been known to influence the characteristics of conventional III-V MESFETs and HFETs, we have studied the effect of buffer layers (and deep levels within the buffer layers) through sidegating measurements which provided the first evidence of the effect of traps on InAs/AlSb HFETs. Finally, we have studied the effects of impact ionization on the microwave properties of InAs/AlSb HFETs.

Chapter 2 begins with an overview of the device technology that was developed at CSDL in order to reliably produce microwave testable sub-micron gate-length devices. The topics given consideration include: MBE growth of the device structures, fabrication sequence, gate lithography and Ohmic contact metallization.

Chapter 3 discusses impact ionization in InAs/AlSb HFETs. Impact ionization generated holes are responsible for the undesirable kink effect in these devices. In this Chapter, two approaches to reducing the kink are examined: the dual-gate HFET is proposed as a technique for preventing hole accumulation (and the resulting positive electrostatic charge) underneath the control gate; and an attempt is made to reduce the rate of impact ionization by increasing the effective channel energy gap through quantum well engineering.

Chapter 4 presents the first direct evidence for the existence of hole traps in the AlSb buffer layer, through the effect of sidegating on the frequency and temperature dependence of current-voltage measurements on InAs/AlSb HFETs. The observation of a new sidegating-induced negative differential resistance (SINDR) effect in InAs/AlSb

HFETs is explained by a model that calls for the transient population of hole traps in the buffer layer.

Chapter 5 discusses the measured DC and microwave performance of InAs/AlSb HFETs. Comparisons between high mobility, wide quantum well devices and low mobility, narrow quantum well devices demonstrate that low-field mobility in addition to peak electron velocity is extremely important in the high frequency performance of HFETs. Anomalously conductive (inductive) measured input (output) reflection coefficients S_{11} (S_{22}) are connected to high rates of impact ionization. We show that the effects of impact ionization in InAs/AlSb HFETs can be so severe that the conventional microwave FET models do not adequately describe the measured device characteristics.

Chapter 6 concludes this dissertation with a summary of the work performed, and provides the scope for future research on InAs/AlSb HFETs. Finally, a list of references is given, and further processing details not mentioned in Chapter 2 are presented in the Appendix.

CHAPTER 2
Device Fabrication

Overview

To study the device physics and measure the microwave performance of InAs/AlSb HFETs, a fabrication process that reliably produces functional submicron gate HFETs is essential. This Chapter describes the implementation of a successful InAs/AlSb HFET fabrication sequence based on a sub-micron optical lithography process.

As discussed in Chapter 1, several groups have been pursuing the development of InAs/AlSb HFETs. The breakthrough came with the Ph.D. work of Bolognesi, who first engineered a reliable and high-yield process based on a combination of selective wet etches [5]. Because that work was confined to the use of photolithographic masks with a feature size ≥ 1.5 μm, the process was not optimized for sub-micron geometries. The present work has refined the process to implement sub-micron gate devices by taking advantage of the facilities available at SFU Compound Semiconductor Device Laboratory (CSDL).

We begin the present Chapter by describing the prototypical InAs/AlSb HFET structure used throughout this work. The processing requirements and their influence on the layer structure of InAs/AlSb HFETs are described. Next, the principal steps to fabricate devices with a reasonable yield are reviewed; the details are left to the Appendix.

The formation of sub-micron gate metallizations by a lift-off process is then discussed. A brief discussion of Ohmic contact metallization schemes concludes the Chapter.

2.1 HFET epitaxial layer structure

Since the pioneering work by Tuttle *et al.* [71]-[73] and Bolognesi [5] at the University of California, Santa Barbara, high quality molecular beam epitaxy (MBE) -grown InAs/AlSb HFET structures now can be achieved in a fairly uniform and reproducible manner. The MBE growth of HFET structures results in semiconductor layers that can be assumed to be grown in close agreement with design specifications; the *in-situ* growth monitoring possible in MBE is key to achieving this result.

A cross-section of the typical InAs/AlSb HFET is shown in Figure 2-1. This device layout is very similar to the standard GaAs MESFET in Figure 1-1 on page 4 except that in the place of the n-GaAs conducting channel, a complex multilayer quantum well structure is used to form a two-dimensional electron gas (2DEG) channel.

All devices layers in this work were grown by molecular beam epitaxy (MBE) on GaAs (100) substrates by Dr. David H. Chow at Hughes Research Laboratories, Malibu, CA. Because the GaAs lattice constant is 5.65 Å, compared to the near-6.1 Å lattice constant of the InAs/(Al,Ga)Sb family, epitaxial growth of InAs/(Al,Ga)Sb layers on GaAs is performed despite a 7% lattice mismatch. GaAs substrates are used because of the unavailability of 6.1 Å semi-insulating substrates.

To improve the run-to-run reproducibility of InAs/AlSb quantum wells, growth on the bare GaAs substrate is initiated with a thin (~1000 Å) GaAs nucleation layer [5]. To accommodate the 7% lattice mismatch, a thick strain-relaxed 2-3 μm AlSb buffer layer is then grown [72]. The mismatch results in a high dislocation density at the initiation of growth, but dislocations undergo pairwise annihilation and a threading dislocation density of $\sim 10^7\,cm^{-2}$ remains with thick buffer layers. Quantum wells grown on GaAs sub-

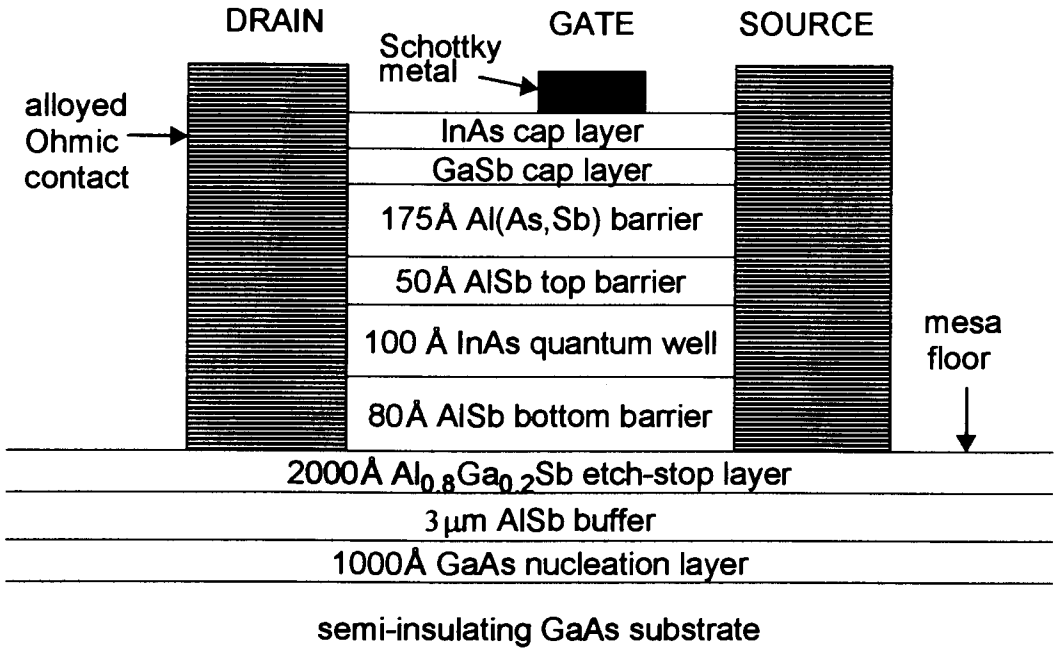

Figure 2-1 : Cross-section of prototypical InAs/AlSb HFET with alloyed Ohmic contacts (not to scale).

strates with thick AlSb buffer layers typically show mobilities of 20,000-30,000 $cm^2/V{\cdot}s$ at 300K for electron sheet densities of ~10^{12} cm^{-2}, and greater than 300,000 $cm^2/V{\cdot}s$ at cryogenic temperatures (< 10K). AlSb buffer layers as thin as 0.25 μm were shown to yield room temperature mobilities of 20,000 $cm^2/V{\cdot}s$, but the low temperature mobilities were far inferior due to the high density of threading dislocations in such thin buffer layers [73].

The AlSb buffer layer is followed by 2000 Å of $Al_xGa_{1-x}Sb$. The aluminum mole fraction x is designed to be ~0.8. AlSb oxidizes in ambient air, increasing in volume and tending to crack and flake from the substrate [78]. The $Al_xGa_{1-x}Sb$ buffer layer composition should remain $x < 0.9$ so as to make the ternary alloy significantly less susceptible to oxidation than the highly reactive AlSb. In wet-etch solutions AlSb tends to etch faster than AlGaSb, thus making the AlGaSb layer an effective etch stop in the formation of the HFET isolation mesa (see next Section).

The typical HFET active region consists of: a 80Å AlSb bottom barrier, a 50-150Å InAs quantum well, a 275Å AlSb(As)-based top barrier and a cap layer. The AlSb top barrier typically contains small amounts of As in the form of short-period Al(As,Sb) digital alloy barriers that provide an improved barrier for holes [5] and reduce gate leakage during transistor operation: the addition of As to AlSb lowers the AlSb valence band edge, providing a barrier to holes attempting to migrate towards the surface.

The InAs/AlSb HFET layers are generally not-intentionally-doped, but some of our more recent work has featured thin, heavily Si-doped InAs δ-doping layers [27] rather than more common Te δ-doping or As soak techniques. Note that for undoped structures, the InAs sheet concentration remains significant. The work of Nguyen *et al.* has identified the Fermi level pinning at the surface of the cap layer to be responsible for most of the electron sheet charge [52]-[54] for quantum wells located near the sample surface, although a residual source of electrons could come from deep levels in the AlSb barriers [18]. Finally, the HFET structure is completed by a composite InAs/GaSb cap layer that protects the underlying structure from oxidation and contamination during processing [5].

2.2 Prototypical HFET processing sequence

HFETs require the same basic processing steps as MESFETs: Ohmic contact formation, device isolation, Schottky gate formation, and so-called "first-level metallization," i.e. probing pads and/or interconnects between devices [81]. A typical device layout is shown in Figure 2-2. The contact pad geometry is designed for microwave-frequency testing using 150μm -pitch coplanar waveguide probes. The "T" shape of the gate reduces the HFET gate resistance compared with single finger gate of the same total 80μm width.

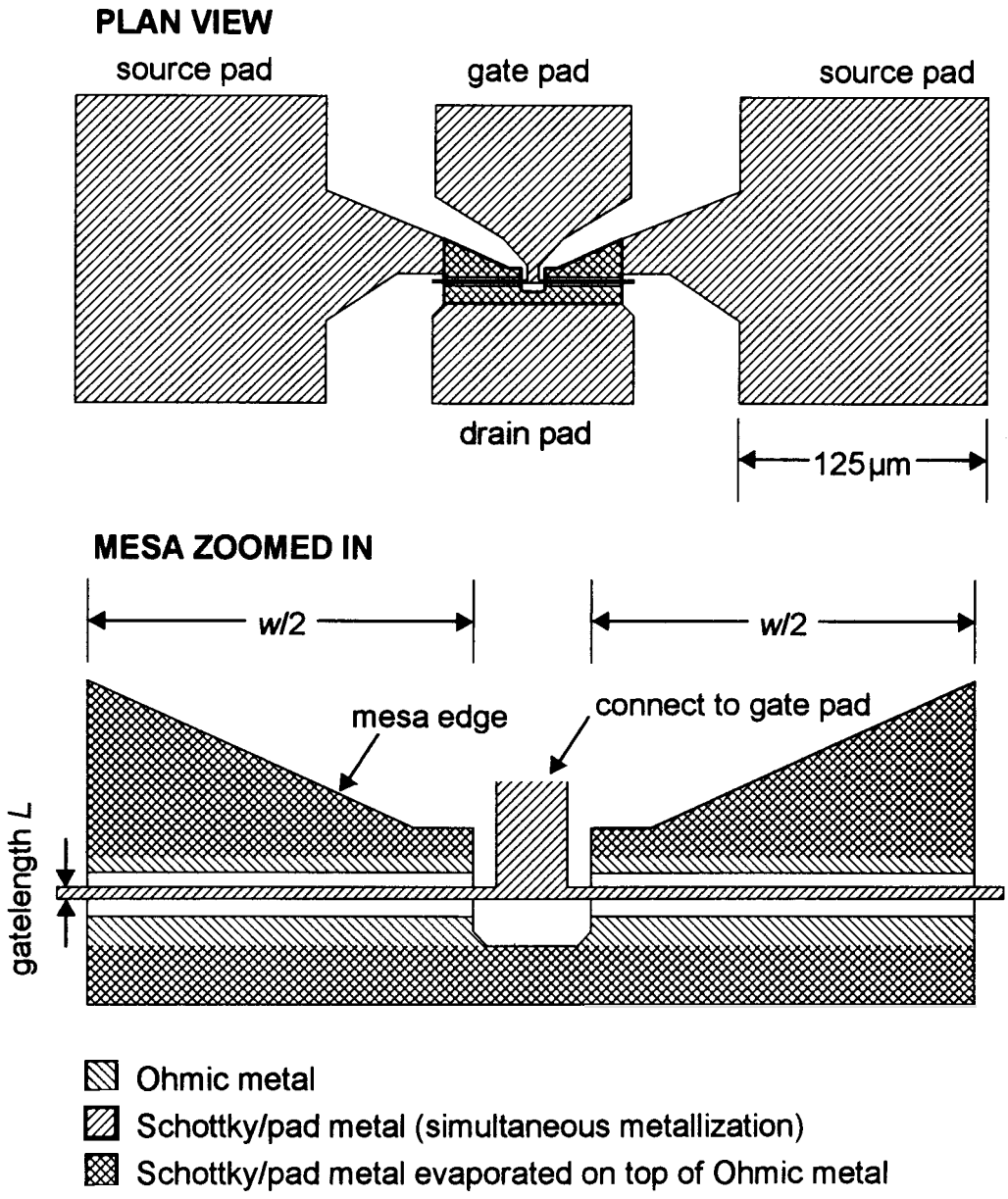

Figure 2-2 : Layout of InAs/AlSb HFET configured for microwave probing. The process only requires 3 photolithographic steps to produce microwave testable devices. The gatelength (here, the narrow gate finger dimension as shown in the zoomed image) is in the range of L ~ 0.5-3.0µm and the transistor width (gate width) is w/2 + w/2 = 80µm. Pads are on AlGaSb mesa floor.

Because of a lack of maturity of the material system, InAs/AlSb -based devices have proven difficult to process. Argon ion-implantation for device isolation can-

not be used, because the narrow band-gap InAs channel remains conductive for all defect densities [78]. The high reactivity of antimonides makes optical lithography using standard basic-solution developers a delicate critically timed process step.

The work of Bolognesi [5] established a reliable fabrication sequence for InAs/AlSb HFETs based on selective wet etches. A complete fabrication sequence is found in the Appendix. We briefly illustrate the fabrication sequence with the aid of Figure 2-3 on page 25, Figure 2-4 on page 26, and Figure 2-5 on page 27. For non-alloyed Ohmic contact HFETs:

(a) Begin with MBE-grown wafer

(b1) Define Ohmic contacts on positive photoresist using standard UV lithography. Etch the cap layer and top barrier layer) to expose the InAs conducting channel.

(c1) Evaporate Ohmic metal (typically Ti/Au or Au/Ge -based metallizations) over the entire wafer, and perform lift-off (see Figure 2-6 on page 29) and strip photoresist using acetone.

(d) Define mesa in photoresist, and then etch down to the AlGaSb buffer. Care must be taken to stop on the AlGaSb to protect underlying AlSb from oxidation in ambient air. Because metal-InAs contacts are non-rectifying, and AlSb is etched by standard photodeveloper, the wet etch process must include a step that provides a significant undercut of the InAs quantum well (see Figure 2-5).

(e) Define gate pattern and first-level pad metallization in photoresist, and evaporate gate metal (typically Ti/Au) on entire wafer. Perform lift-off and strip photoresist using acetone. This is the most critical lithographic step.

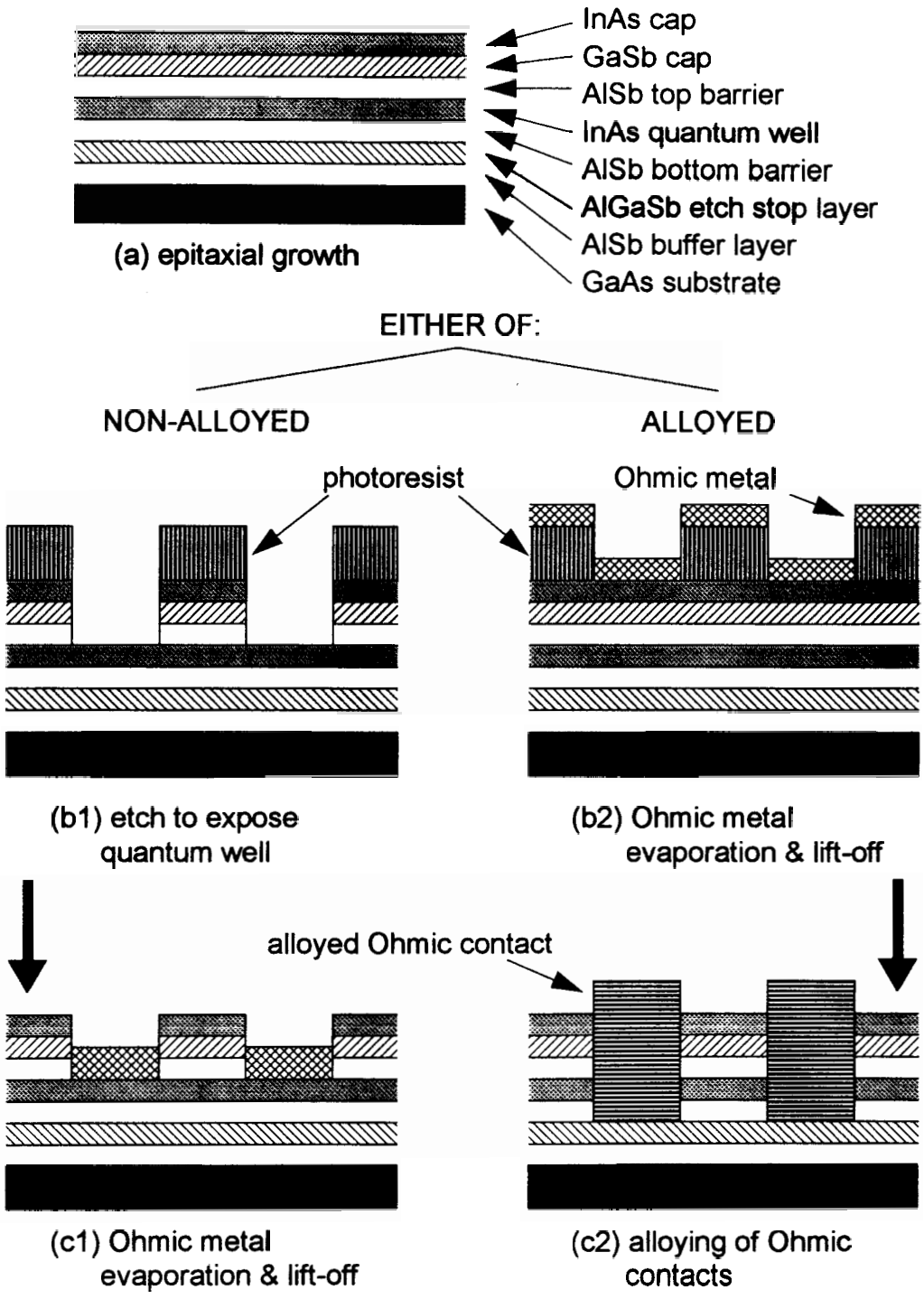

Figure 2-3 : Process run for HFETs (not to scale).

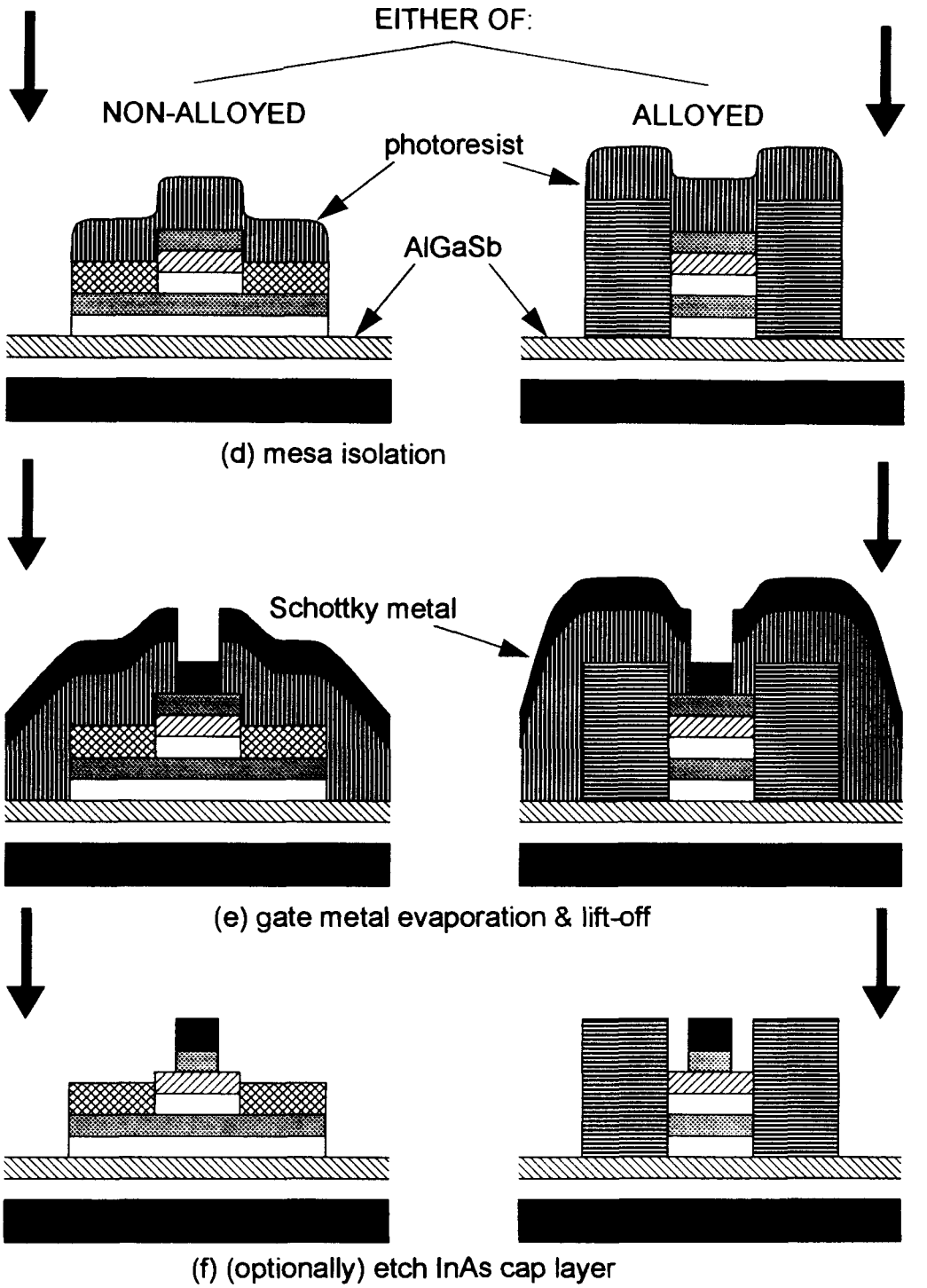

Figure 2-4 : Process run for HFETs (continued; not to scale).

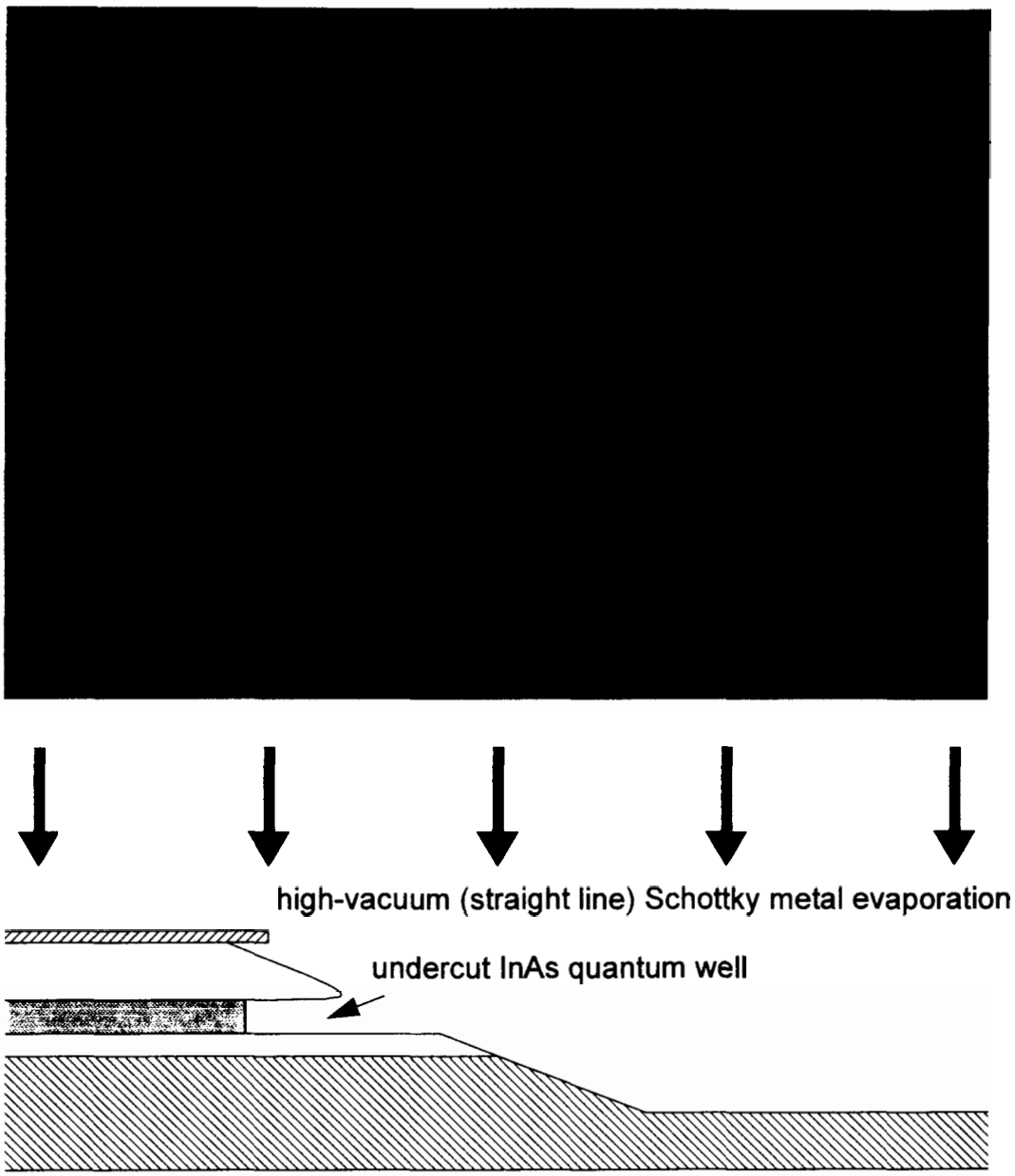

Figure 2-5 : Side-on cross-section view of HFET gate evaporation showing how an undercut is required to avoid gate & pad metal to quantum well short-circuiting (approximately to scale). Because metal evaporated under high vacuum will travel in straight lines, an air gap will prevent metal-InAs contact.

(f) Use highly selective wet etch to remove thin InAs cap. As shown by Bolognesi [5], this final step reduces the parasitic capacitance caused by the additional surface charge in the cap, improves the measured transconductance g_m of the HFET, and reduces gate leakage along the surface.

When alloyed Ohmic contacts are used, the second and third steps become:

(b2) Define Ohmic contacts on photoresist and immediately evaporate metal (typically Ni/AuGe/Ni/Au) over entire wafer. Perform lift-off and strip photoresist using acetone.

(c2) Alloy Ohmic metal with semiconductor in annealing chamber with forming gas (H_2/N_2 10%/90%) ambient.

2.3 Sub-micron gate lithography

As briefly mentioned above, the metallization steps in HFET fabrication involve: opening a window in the photoresist where the metallization is to take place; evaporation of metal over the entire wafer; stripping of the photoresist in acetone, and lifting off metal deposited on the photoresist. Metal deposited directly on the semiconductor surface remains. This "lift-off" process (Figure 2-6) is standard throughout the III-V compound semiconductor industry. In the Si-based device fabrication, on the other hand, a selective metal etch process is used because of the wide availability of selective metal *vs.* Si etchants.

The success of a sub-micron lift-off process depends on several factors: the ability to define very narrow lines in photoresist; and following metallization, the ability to remove the unwanted metal by stripping the photoresist. Stripping the photoresist in a solvent such as acetone aids in the lift-off, because the photoresist swells up as it is being dissolved, literally lifting the metal deposited on it.

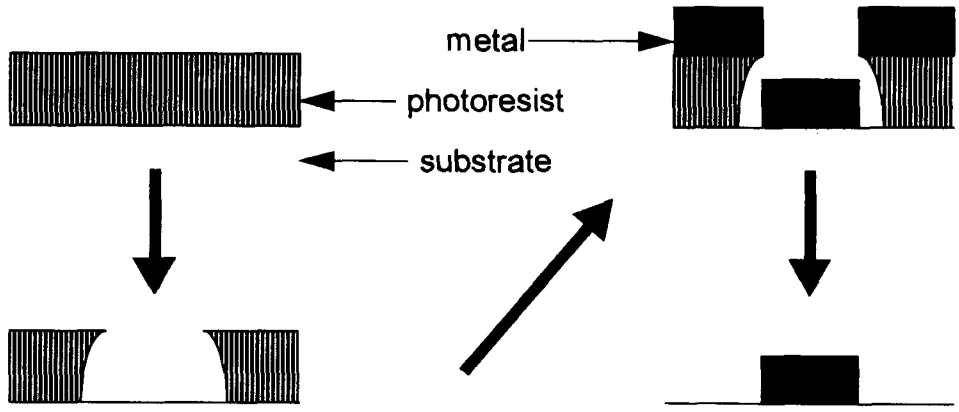

Figure 2-6 : Steps in the lift-off metallization process.

In order to ensure a clean lift-off, a break in the as-deposited metal is required. This is provided by a photolithographic process that provides an undercut photoresist profile, followed by the evaporation of metal under high or ultra-high vacuum (i.e. molecular flow deposition) using e-beam or thermal evaporation. If there is a positive slope to the photoresist sidewalls, or if the metal is deposited by sputtering, there may be no break in the metal: compare Figure 2-7 (a), (b), and (c).

2.3.1 Overhanging photoresist profile obtained using toluene soak

A well-known technique to obtain overhanging photoresist profiles by optical lithography was reported by Hatzakis *et al.* [31]: exposing the top surface of the photoresist to an aromatic solvent prior to development effectively reduces the dissolution rate of the top surface compared to the underlying photoresist. Therefore, the photoresist tends to develop with an overhang profile.

To understand the cause of this phenomenon, we must examine the photolithographic process in more detail. Photoresist contains three critical components: polymer, solvent, and sensitizer.

The polymer is suspended in solvent. The fractional solid content of the polymer determines the viscosity of the photoresist, which in turns determines the thick-

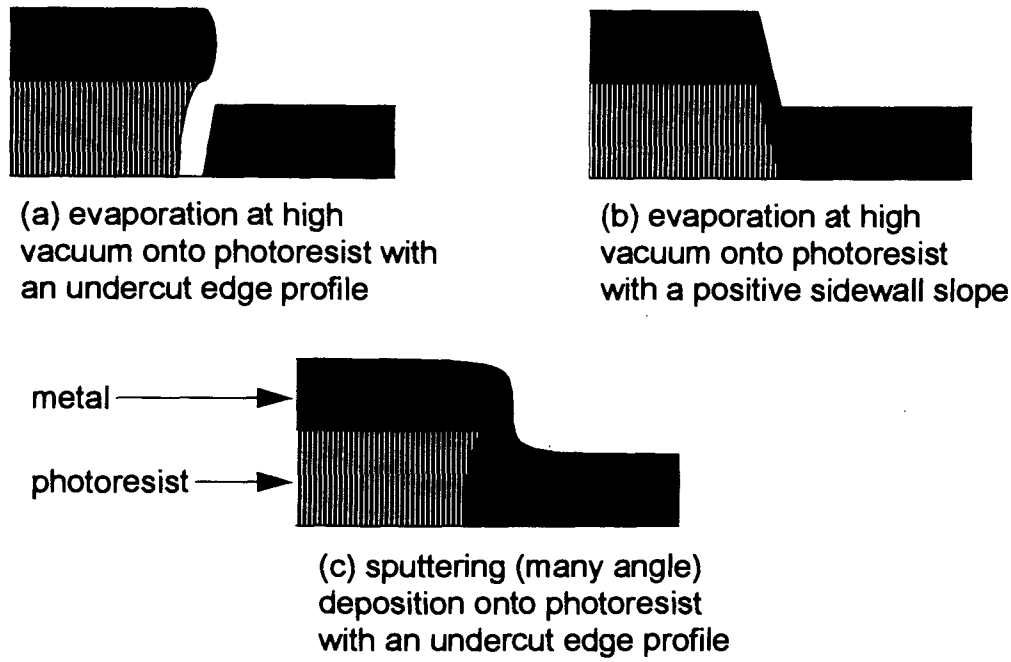

Figure 2-7: Comparison of step coverage of undercut and non-undercut photoresist resulting from high-vacuum evaporation and sputtering.

ness of the photoresist following spin-coating of a wafer. When the photoresist is then baked, much of the solvent is removed. What remains on the wafer is essentially a film of polymerized plastic. During exposure to UV light the sensitizer converts the polymer into a ketone, which is soluble in the aqueous based alkaline developer solution.

Hatzakis *et al.* [31] suggested that soaking the photoresist in an aromatic solvent, such as chlorobenzene and toluene, removes additional solvent from the photoresist surface, and also removes some of the more easily-developed low-molecular-weight polymer. Because of the relatively high toxicity of chlorobenzene fumes, we opted for toluene as a safer alternative in our lift-off process.

Another key point of Hatzakis *et al.* was that the overhang was most significant for lower temperature prebake cycles, because high-temperature bakes remove more solvent, thus reducing the influence of the aromatic solvent soak. With this in mind, a relatively low temperature hotplate bake (105°C) was used. Because of the low temperature

prebake, a post-soak bake was performed to further harden the photoresist surface layer. To further improve the overhang, the post-soak bake was performed in a convection oven because a hotplate bake heats the wafer from bottom to top, forcing the solvent out fairly uniformly, whereas a convection oven bake tends to dry the top surface preferentially and forms a skin (or crust) that traps more soluble resist beneath the surface of the photoresist film. Once the developer breaks through the crust in the exposed areas, the higher resist dissolution rate in the underlying layers naturally results in an overhang profile.

A scanning electron micrograph of the photoresist profiles obtained using the toluene surface treatment (Figure 2-8) shows the distinct overhang. Qualitatively, we have found that toluene-treated photoresist allows easy and complete lift-off within minutes of immersion in acetone. In contrast, poor lift-off recipes may require several-hour or even overnight soaks in acetone, or lift-off aided with immersion in an ultrasonic bath because of an inadequate photoresist overhang profile.

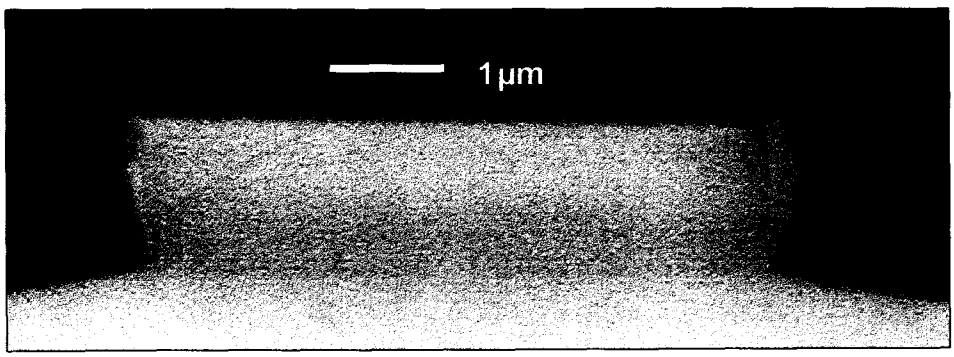

Figure 2-8 : Photoresist edge profiles following lift-off process.

2.4 Ohmic contacts

2.4.1 Introduction

In the design and fabrication of high-speed microwave devices, a minimization of the source and drain resistance is critical. The external (measured) transconduc-

tance value g_m is reduced from the intrinsic transconductance g_0 value because of the effect of the series source resistances:

$$g_m = \frac{g_0}{1 + g_0 R_S} \tag{2-1}$$

where R_S is the total resistance between the source contact and the channel region immediately below the gate, normalized to unit transistor width. This function is plotted in Figure 2-9; for example, a typical series resistance of $R_S = 0.75\,\Omega\cdot$mm would reduce the transconductance from 400mS/mm (intrinsic) to 300mS/mm (extrinsic or measured).

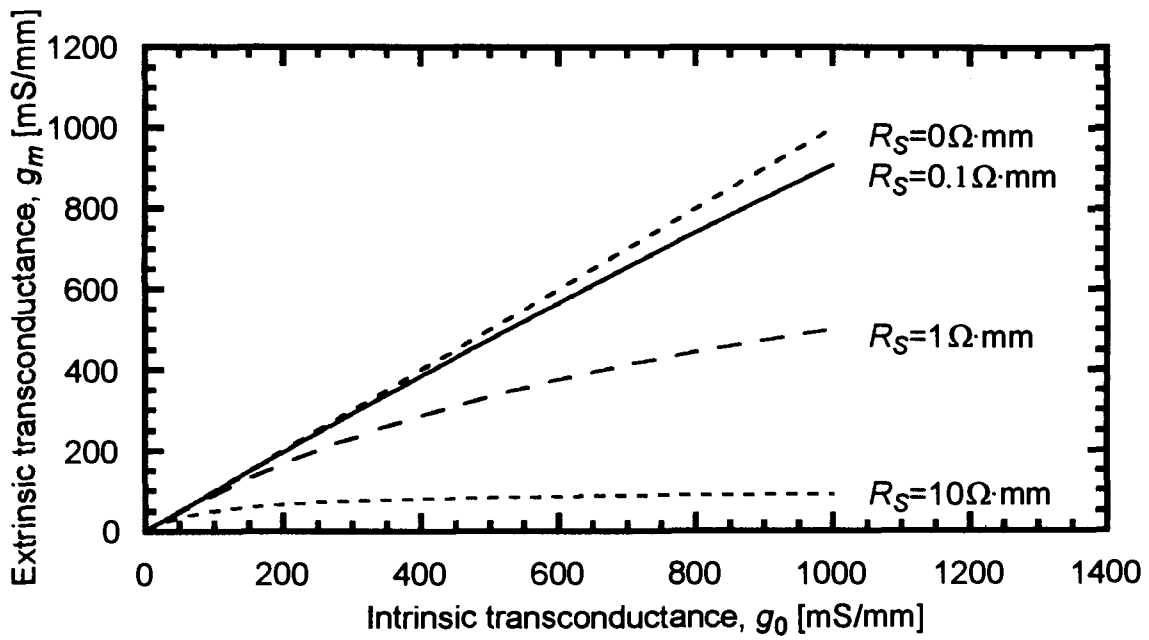

Figure 2-9 : Extrinsic transconductances g_m as a function of source resistance R_S and intrinsic transconductance g_0 (quantities normalized to unit transistor width).

Another consideration becomes important at high frequencies: as was shown by Tasker *et al.*, HFETs suffer a parasitic delay time related to the source and drain resistances that can be expressed in terms of the intrinsic transit time $\tau_i = 1/(2\pi f_T)$ by [69]

$$\tau_p = \tau_t g_m (R_S + R_D)\left\{\frac{G_{DS}}{g_m} + \frac{1}{1 + C_{GS}/C_{GD}}\right\} \qquad (2\text{–}2)$$

where R_S and R_D are the source and drain resistances, G_{DS} is the output conductance, and C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitances respectively. Clearly, for superior high-speed and DC performance the contact resistance of both the source and drain Ohmic contacts must be minimized.

2.4.2 Experimental

In the present study, metal was deposited by e-beam evaporation, and subsequently was annealed at one of several temperatures with a graphite stripe annealer. 4-point (Kelvin) probing measurements were performed using an HP4145B semiconductor parameter analyzer on a transmission line method (TLM) test structure [1]: the structure used features Ohmic contact pads with interpad spacings of 5, 10, and 20 μm defined on a 100 μm wide mesa strip. The measured resistance is the sum of the contact resistance between the metal and the semiconductor, and the resistance in the conducting channel between the contacts:

$$R_{meas} = 2R_c + R_{sheet}\frac{\Delta l}{w} \qquad (2\text{–}3)$$

where R_c is the extracted contact resistance of the Ohmic pad of the TLM, R_{sheet} is the channel sheet resistance, Δl is the interpad separation on the TLM strip, and w is the contact pad width. The measured resistance R_{meas} between Ohmic pads of varying separations is plotted versus Δl, yielding R_c and R_{sheet} directly. The contact resistivity ρ_c is found using the expression [59]

$$\rho_c = \frac{(R_c/w)^2}{R_{sheet}} \qquad (2\text{–}4)$$

if we make the unlikely assumption that the sheet resistance of the channel R_{sheet} is equal under and between the Ohmic contact pads. In Figure 2-10, results for various Ohmic metallizations are presented as a function of the annealing temperature (annealing time was kept at 2min). The results below indicate that Ni/Ge/Au (~110/180/3000Å) or Ge/Au/Ni/Au (~180/350/110/3000Å) metallizations with anneals at ~275°C yield adequate, though far from optimal, contact resistances. The Ni/Ge/Au metallization was

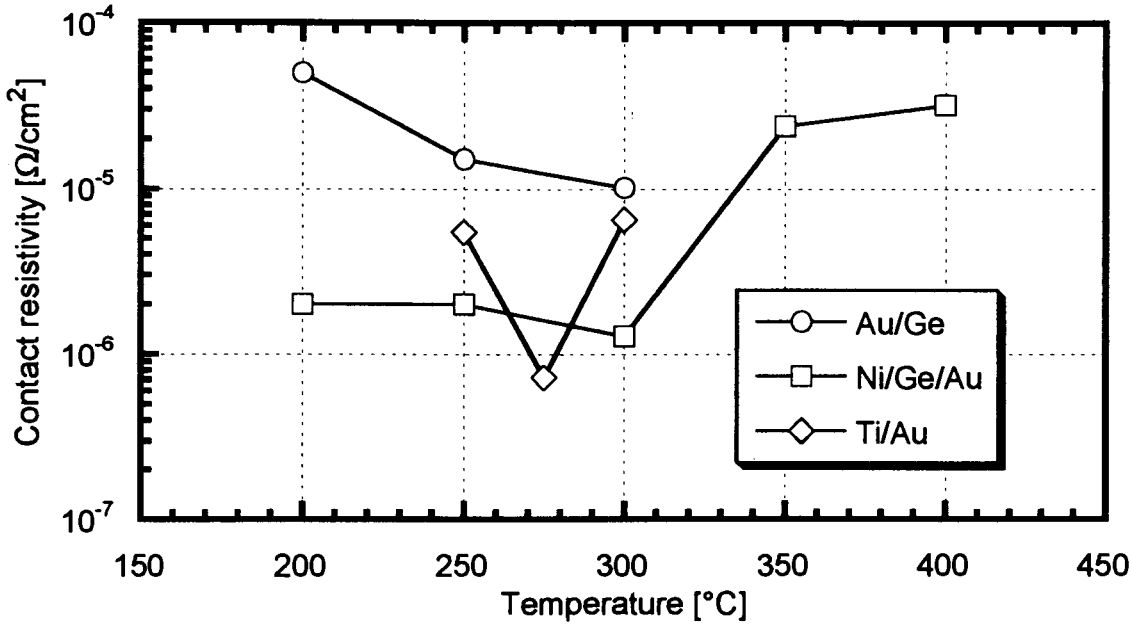

Figure 2-10 : Ohmic contact resistances for various annealing temperatures for three different metallizations.

found to produce a better contact morphology than the Ti/Au (~200/3000Å) metallization. For the remainder of this work we have settled on the Ni/Ge/Au scheme, and left the area of contact optimization to the care of other workers in the field to concentrate on fundamental device issues.

2.4.3 Other recently reported work

Several studies have recently been published on Ohmic contacts for InAs/AlSb HFETs. AuGe/Ni/Pt/Au (500Å/150Å/200Å/300Å) layers were deposited sequentially by thermal and e-beam evaporation [10]. Rapid thermal annealing (RTA) for only 1sec at 300°C was used to alloy the Ge to the semiconductor. Auger profiling showed that the Au diffusion depth was approximately 1500Å; the Ge doping depth was not revealed. The contact resistance was found to be 0.11Ω·mm, yielding a contact resistivity of $\sim 5 \cdot 10^{-7} \Omega/cm^2$. The lateral diffusion, however, was ~ 0.4μm, as measured by scanning electron microscopy. In the same study, Pd/Ge/Au (100Å/500Å/1000Å) metallizations were also studied because of the low temperature solid-state reactions that take place between Pd and other semiconductors. These were annealed at 175°C for 3 hours in forming gas, for a contact resistance of 0.08Ω·mm and a contact resistivity of $\sim 2.5 \cdot 10^{-7} \Omega/cm^2$. While the Pd diffused slightly deeper than the InAs channel layer, Au did not penetrate into the semiconductor because of the Pt barrier and no lateral diffusion was observed. In contrast, when a Pd/Ge/Au (100Å/500Å/1000Å) or Pd/Au (100Å/600Å) metallization was used, significant lateral diffusion into the channel was observed.

At Columbia University, AuGe and AuTe -based RTA annealed Ohmic contacts were studied [85]. Their hypothesis was that since Ge is amphoteric in GaSb and AlSb, whereas Te is a non self-compensating group VI donor, Te would be expected to form superior Ohmic contacts. Ni/AuGe/Ni/Au and Ni/AuTe/Ni/Au metallizations with thicknesses 80Å/1000Å/200Å/1000Å were deposited by a multiple source thermal evaporator, and annealed for 20s by RTA in a forming gas ambient. The optimal contact resistivities and annealing temperatures were $2.3 \cdot 10^{-7} \Omega/cm^2$ when annealing the AuGe-based metallization at 325°C, and $1.3 \cdot 10^{-6} \Omega/cm^2$ when annealing the AuTe-based metallization at 400°C.

Our contact resistivities of ~ $10^{-6}\Omega/cm^2$ for Ni/AuGe/Ni/Au metallizations obtained using a graphite strip annealer are not as low as the state-of-the-art results obtained using RTA or using Pd/Ge/Au. One must keep in mind, however, the very high uncertainty attached to our calculations of specific contact resistivity because of the assumptions made, and because of the large error in determining the contact resistance R_c using our large TLM patterns inappropriately scaled for the high InAs/AlSb 2DEG sheet conductivities.

CHAPTER 3
Impact Ionization

Overview

InAs channel HFETs are more susceptible to impact ionization related short-channel effects than other III-V HFETs: relatively long (several micron) gatelength devices can suffer from a strong kink effect — an abrupt increase in output conductance with increasing V_{DS} — and a high output conductance when compared to other III-V systems. The large intervalley separation $\Delta E_{\Gamma L} \sim 0.9\,\text{eV}$ in InAs is much greater than the fundamental band gap $E_g \sim 0.36\,\text{eV}$, and hot electrons tend to impact ionize rather than scatter to the low-mobility, high effective mass conduction band L satellite valleys. In GaAs in contrast ($\Delta E_{\Gamma L} \sim 0.3\,\text{eV}$, $E_g \sim 1.42\,\text{eV}$) intervalley scattering dominates because of the high density of available states in the L valley. The high impact ionization rate manifests itself by an abruptly increasing output conductance at high drain biases (the kink effect) and by a gate leakage current consisting of impact ionization holes that drain through the negatively biased gate. We argue that impact ionization itself is not the fundamental problem as far as the kink is concerned: rather, the management of the impact-ionization generated holes determines the device behavior. In this Chapter, we look at how the staggered band lineup and lack of hole confinement in InAs/AlSb channels affect DC device performance. We explore two techniques for reducing the kink: dual-gate HFETs, where the second gate drains impact ionization holes from the active region; and quantum well engi-

neering, where the effective band gap to be overcome for impact ionization is increased by increasing quantization in the InAs/AlSb quantum well.

3.1 The kink effect in InAs/AlSb HFETs

In this Section, we discuss the source of the abrupt increase in output conductance that is generally observed in InAs/AlSb HFETs operated above $V_{DS} \sim 0.5\,V$ (the kink effect: see Figure 3-8 on page 48). For simplicity, we only consider depletion-mode InAs/AlSb HFETs.

As electrons migrate through the quantum well from the source to the drain, they must transit under the gate. In the simple electrostatic model for the HFET, a negative bias on the gate lowers the Fermi level in the channel, thus reducing the carrier sheet concentration under the gate (see Figure 3-1). The resulting carrier depletion can be

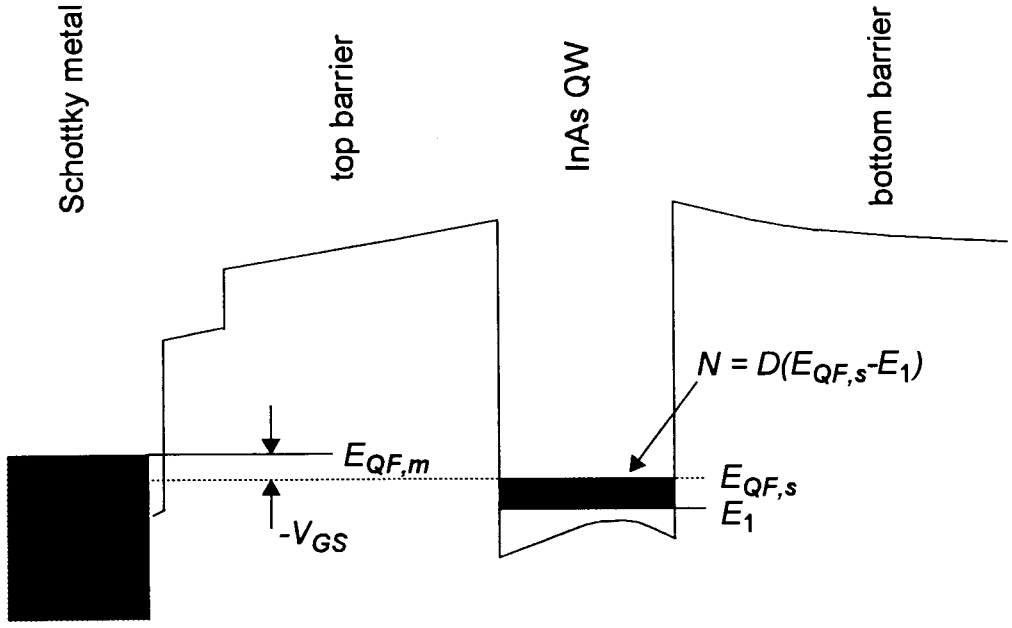

Figure 3-1 : Schematic of conduction band edge of biased InAs/AlSb HFET. N is the electron charge in the quantum well, D is the density of states in the quantum well, $E_{QF,s}$ is the quasi-Fermi level in the semiconductor, $E_{QF,m}$ is the quasi-Fermi level in the Schottky metal, E_1 is the ground state energy in the quantum well, and $-V_{GS}$ is a negative gate bias.

thought of as an effective current controlling energy barrier encountered by the electrons migrating from the source toward the drain. On the drain edge of the gate electrons are accelerated by a strong electric field towards the drain. A plot of the one-dimensional conduction band energy and electric field along the channel of a prototypical $L = 0.2\,\mu m$ gate-length HFET calculated using Silvaco's ATLAS device simulation software is shown in Figure 3-2. The simulated structure consists of a 340 Å $Al_{0.22}Ga_{0.78}As$ top barrier with a δ-doping spike of $8 \cdot 10^{11}\,cm^{-2}$ 30 Å above the channel, a 140 Å $In_{0.78}Ga_{0.22}As$ undoped channel, and a thick $Al_{0.22}Ga_{0.78}As$ bottom barrier, with a δ-doping spike of $2 \cdot 10^{11}\,cm^{-2}$ 30 Å below the channel. The total sheet concentration is approximately $10^{12}\,cm^{-2}$. The gate-source energy barrier is evident in the simulated conduction band profile.

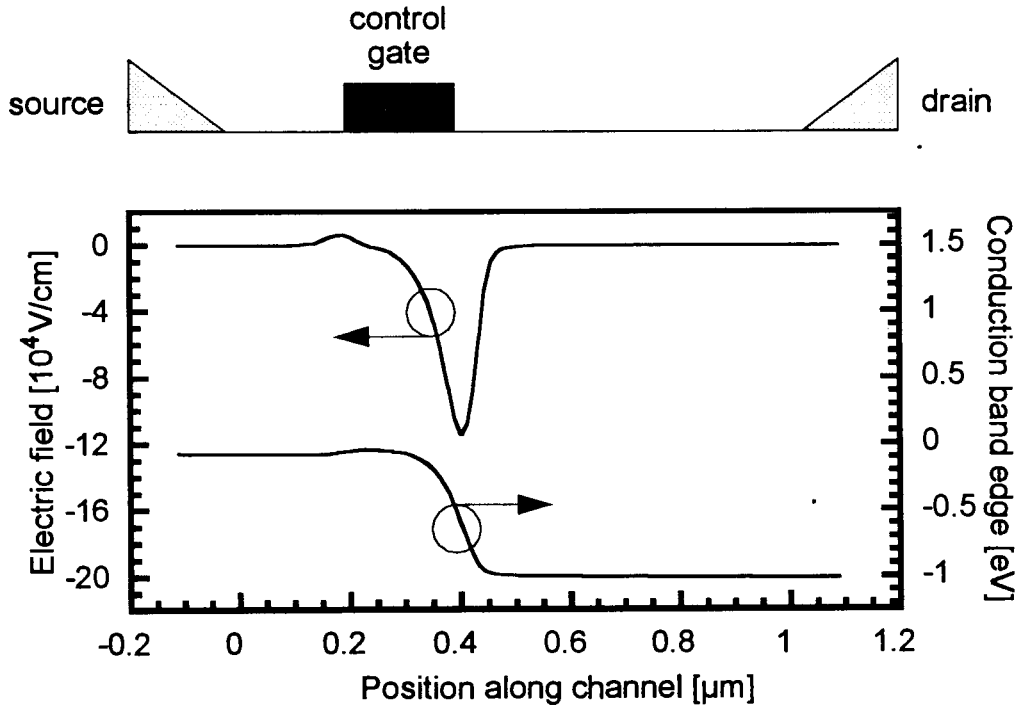

Figure 3-2 : Simulated conduction band energy and electric field along the channel of a standard HFET (drain bias $V_{DS} = 1\,V$, gate bias $V_{GS} = -0.6\,V$).

As seen from the simulated electric field profile in Figure 3-2 for a device with a drain bias $V_{DS} = 1\,V$ and a gate bias $V_{GS} = -0.6\,V$, a high electric field region is set

up in the channel under the drain edge of the gate. In a narrow-bandgap material such as InAs, the electrons heated by the electric fields can undergo impact ionization. In this process, an energetic electron loses kinetic energy by exciting an additional electron-hole pair. Since this event takes place in a high electric field region, the impact ionization generated hole and electron are separated (see Figure 3-3): the electron is drawn towards the drain, and the hole drifts towards the source edge of the gate. (The effective energy barrier

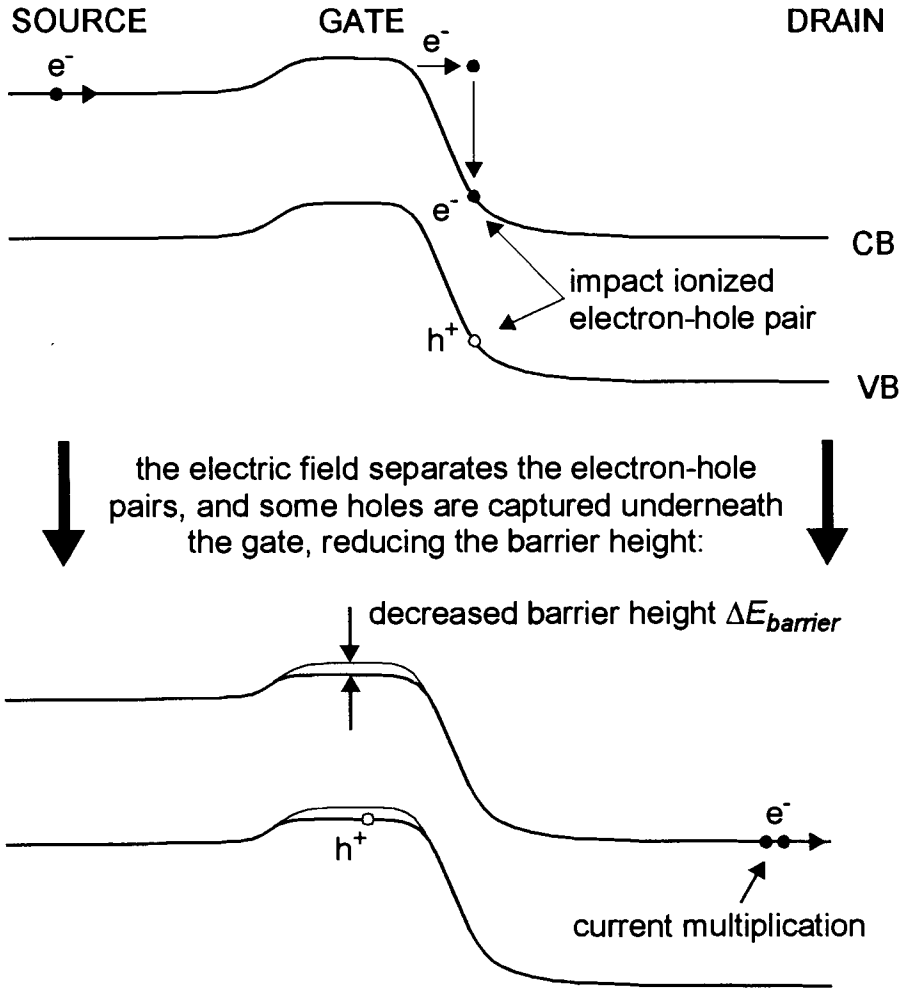

Figure 3-3 : Impact ionization in the high-field region of channel and increase in effective barrier height under the gate. Some of the impact ionization holes appear as gate leakage current due to the lack of confinement in the channel (not shown). Vertical scale exaggerated for clarity of presentation.

to electrons under the gate corresponds to an effective energy trough for holes. Note that the AlSb/InAs/AlSb quantum well provides no hole confinement and therefore holes can migrate to the AlSb barrier layers; see Figure 1-5 on page 13. For simplicity, this is not illustrated in the 1D plot of Figure 3-3.) The quasi-static positive hole charge under the gate lowers the effective energy barrier at the entrance of the channel and allows more electrons to be injected from the source, increasing I_{DS} and preventing current saturation. Impact ionization and the resulting accumulation of holes near the source can be discussed in terms of a parasitic bipolar action. Indeed, the lowering of the source-gate potential barrier due to hole accumulation is completely analogous to the forward biasing of the emitter base junction in an n-p-n bipolar junction transistor (BJT). This interpretation was first given by Bolognesi, who noticed the similarity between the lateral band diagram in FETs and the vertical band diagram in n-p-n BJTs (see Figure 3-3) [5].[1]

The increasing (non-saturating) drain current in the quantum well results in an abrupt increase in output conductance, often referred to as "the kink effect." It was argued by Brar *et al.* [13] that the very low mobility of holes in AlSb (often $< 200\,cm^2/V{\cdot}s$ in MBE material grown on GaAs) leads to a large space charge even for small hole currents through the AlSb buffer: a monotonically increasing positive space charge would prevent current saturation in InAs/AlSb HFETs. Conventional III-V HFETs rely on staggered lineup quantum wells that confine electrons and holes to the quantum well; the electron/hole wave function overlap allows for recombination of impact ionization holes with channel electrons and the kink effect tends to display a clear saturation with increasing drain bias.

1. The impact ionization generated electrons do add to the channel current. Because an incident hot electron loses kinetic energy to the generated electron, however, the net current increases less than one intuitively would expect. Moreover, with the dramatic improvements in output conductance obtainable using dual-gate InAs/AlSb HFETs [2] and back-gate InAs/AlSb HFETs [13] the impact ionization generated electron current (which in the back-gate HFET almost certainly is unaffected) must be discounted as the dominant mechanism responsible for the kink effect.

3.2 Attempts to reduce the kink effect

3.2.1 Dual-gate HFETs

3.2.1.1 Introduction

Dual-gate FETs have long been considered for use in variable gain amplifiers, mixers [70], and other applications (see [35] and references 1-5 therein). In direct-coupled FET logic (DCFL) circuits, very compact NAND logic gates can be constructed using dual-gate HFETs [67]. In addition to the above four-terminal applications of the dual-gate FET, the cascode-connected dual-gate FET (a dual-gate FETs with the drain-side gate held at a common ground with the source) is a three terminal device with improved output impedance and reduced feedback capacitance when compared to a single-gate FET [61].

An important advantage of dual-gate FETs is that they feature a reduction of short-channel effects compared to those observed in single-gate FETs. Monte Carlo modeling by Dollfus *et al.* has showed that for a strained AlGaAs/InGaAs HFET with a very short gatelength (L = 50nm) the addition of a second gate increases the transconductance/output conductance ratio g_m/g_D (i.e. the FET voltage gain) by a factor > 2 compared to that observed in a 100nm single-gate HFET, and by a factor of 3-4 compared to a 50nm single-gate HFET [26]. To gain deeper insight in the operation of dual-gate HFETs, we simulated the characteristics of a 0.2µm AlGaAs/InGaAs/AlGaAs quantum well HFET using Silvaco's ATLAS device simulation software. The simulated structure consists of a 340Å $Al_{0.22}Ga_{0.78}As$ top barrier with a δ-doping spike of $8 \cdot 10^{11}\,cm^{-2}$ 30Å above the channel, a 140Å $In_{0.78}Ga_{0.22}As$ undoped channel, and a thick $Al_{0.22}Ga_{0.78}As$ bottom barrier, with a δ-doping spike of $2 \cdot 10^{11}\,cm^{-2}$ 30Å below the channel. A dual-gate HFET with a 0.2µm second gate located 0.2µm away from the first gate toward the drain was also simulated. The I-V characteristics of the single- and dual-gate HFETs are given in Figure 3-4 (the simulated electric field profile is shown in Figure 3-6 on page 45). The

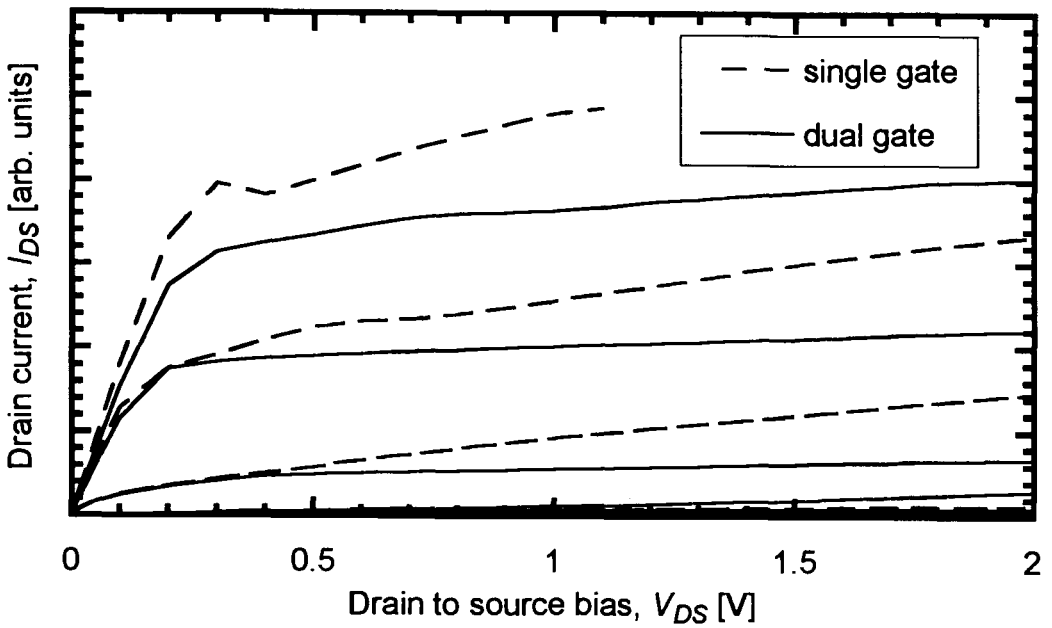

Figure 3-4 : Simulated drain I-V characteristics for single- and dual-gate 0.2μm prototypical AlGaAs/InGaAs/AlGaAs HFETs.

dual-gate device shows significantly improved I-V characteristics with a much reduced output conductance because of the shielding effect of the second gate which decouples the control gate from the high electric field near the drain electrode. Clearly, dual-gate HFETs greatly reduce short channel effects. With the appearance of short-channel effects even in relatively long (~1 μm) gatelength devices, dual-gate structures are very interesting in the fabrication of InAs/AlSb HFETs with improved characteristics.

3.2.1.2 Removal of impact ionized holes in dual-gate InAs/AlSb HFETs

We saw in the previous subsection the reduction in short-channel effects in a dual-gate HFET even when impact ionization -related effects are neglected. In InAs/AlSb HFETs, the second gate provides another benefit: many holes that would be generated by impact ionization at the high-field drain edge of the gate are now generated at the drain edge of the second gate, and are drained by the second gate and so hole accumulation under the first gate is prevented. Effectively, the hole gate leakage through the

second gate eliminates the hole feedback mechanism responsible for the kink effect. This effect, which is particular to InAs/AlSb dual-gate HFETs, was first demonstrated by Bolognesi *et al.* [2][3] and then by Boos *et al.* [9].

The dual-gate InAs/AlSb HFET structure is shown schematically in Figure 3-5 [2]. This approach has the great advantage over the alternative p^+ GaSb back-gates that no change to the epitaxial layers need be made. (See "Back-gate HFETs" on page 55.) The more difficult lithography of dual-gate FETs is a technological challenge, and presents difficulties to any future self-aligned gate lithographic processes. For microwave operation, the second gate does add a parasitic capacitance to the HFET similar in magnitude to the first gate capacitance.

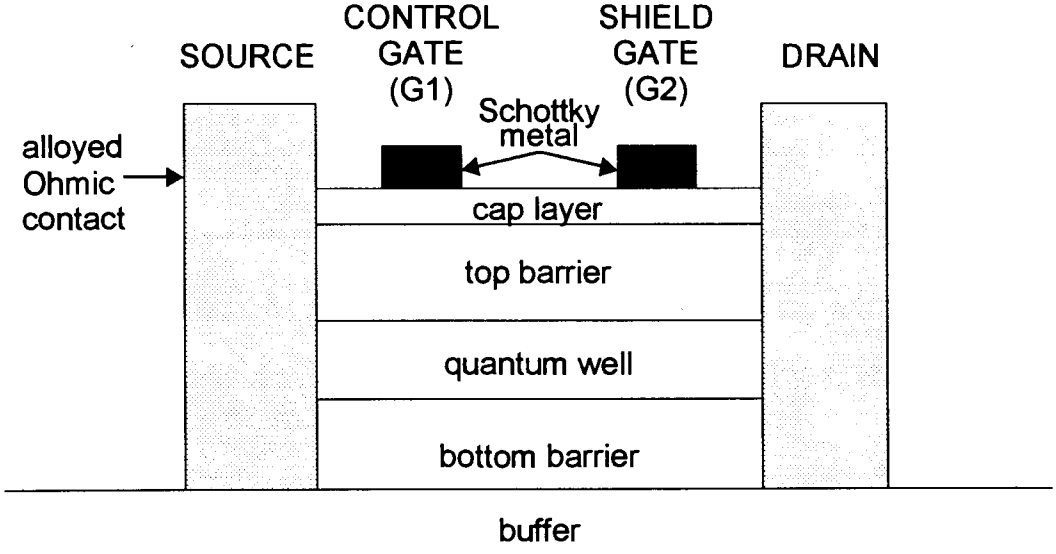

Figure 3-5 : Simplified cross-section of typical dual-gate InAs/AlSb HFET with alloyed Ohmic contacts (not to scale).

In the dual-gate HFET, we refer to the gate nearer the source as the "control gate" (G1) and the gate nearer the drain as the "shield gate" (G2). The control gate is negatively (or zero) biased in normal operation, and the shield gate is grounded. Channel electrons encounter a first potential barrier under the control gate, and they are accelerated

by a strong electric field towards the shield gate. The shield gate also has an effective energy barrier on the source side, and a high electric field region on the drain side. A simulation of the one-dimensional conduction band energy and electric field along the channel of the dual-gate HFET is shown in Figure 3-6.

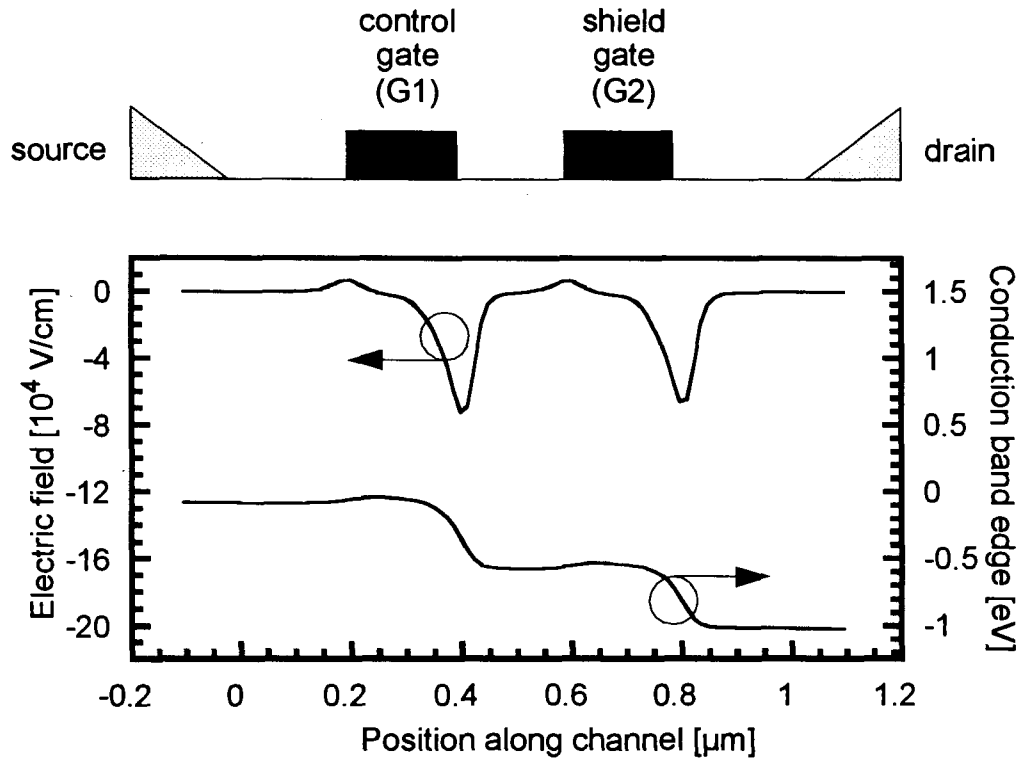

Figure 3-6 : Simulated conduction band energy and electric field along the channel of a dual-gate HFET ($V_{DS} = 1V$, $V_{GS} = -0.6V$, $V_{shield} = 0V$).

The shield gate strongly influences the drain I-V characteristics in InAs/AlSb HFETs. Most of the potential between the drain and the source is accommodated by the electric field at the drain edge of the shield gate when the channel is open, and at the drain edge of the control gate when pinch-off is approached. Under near pinch-off conditions, the channel current is low enough to reduce impact ionization generation of holes to a minimum. Under open channel conditions (when the kink is strongest) the highest electric field is at the drain edge of the shield gate, whereas when the channel is pinched-off the highest electric field is at the drain edge of the control gate (this behavior

was confirmed by simulations on the prototypical structure discussed above). In that part of the channel, holes are generated by impact ionization, and then prevented from collecting under the control gate by the effective barrier at the source edge of the shield gate (see Figure 3-7). There is charge multiplication due to the impact ionization at the shield gate but no parasitic bipolar effect can take place because holes are prevented from drifting back toward the control gate. If V_{DS} and V_{GS} are sufficiently increased, the electric field under the control gate also becomes high enough for impact ionization and the kink appears in the drain characteristics. The use of a dual-gate structure therefore delays the onset of the kink effect to much higher biases and extends the device operational range. The current gain I_{DS}/I_G is also increased.

3.2.1.3 Results

The first demonstration of InAs/AlSb dual-gate HFETs was given by Bolognesi *et al.* [3] at SFU. In this work, the dramatic reduction of the kink effect is evident. In Figure 3-8, the measured drain I-V characteristics for 1.0 μm single-gate and dual-gate HFETs (consisting of two 1.0 μm gates separated by a 1.0 μm space) are compared. Clearly, the use of a dual-gate configuration nearly triples the operational range of InAs/AlSb HFETs. The dual-gate structure also greatly increases the device voltage gain.

In addition to the reduction in the output conductance, the control gate leakage current is greatly reduced by the addition of the shield gate. In a standard InAs/AlSb HFET, the gate leakage current is made up of two components: a diode leakage current component that is a function of the gate-to-*channel* bias; and a leakage current component consisting of impact ionization generated holes and therefore a function of I_{DS} and V_{DS}. In our dual-gate HFETs, these two components are clearly divided between the control gate and shield gate: see Figure 3-9. The slight increase in control gate current at a as the drain bias is increased occurs because the diode leakage current increases for increasing gate-channel bias. The shield gate current consists of impact ionization holes

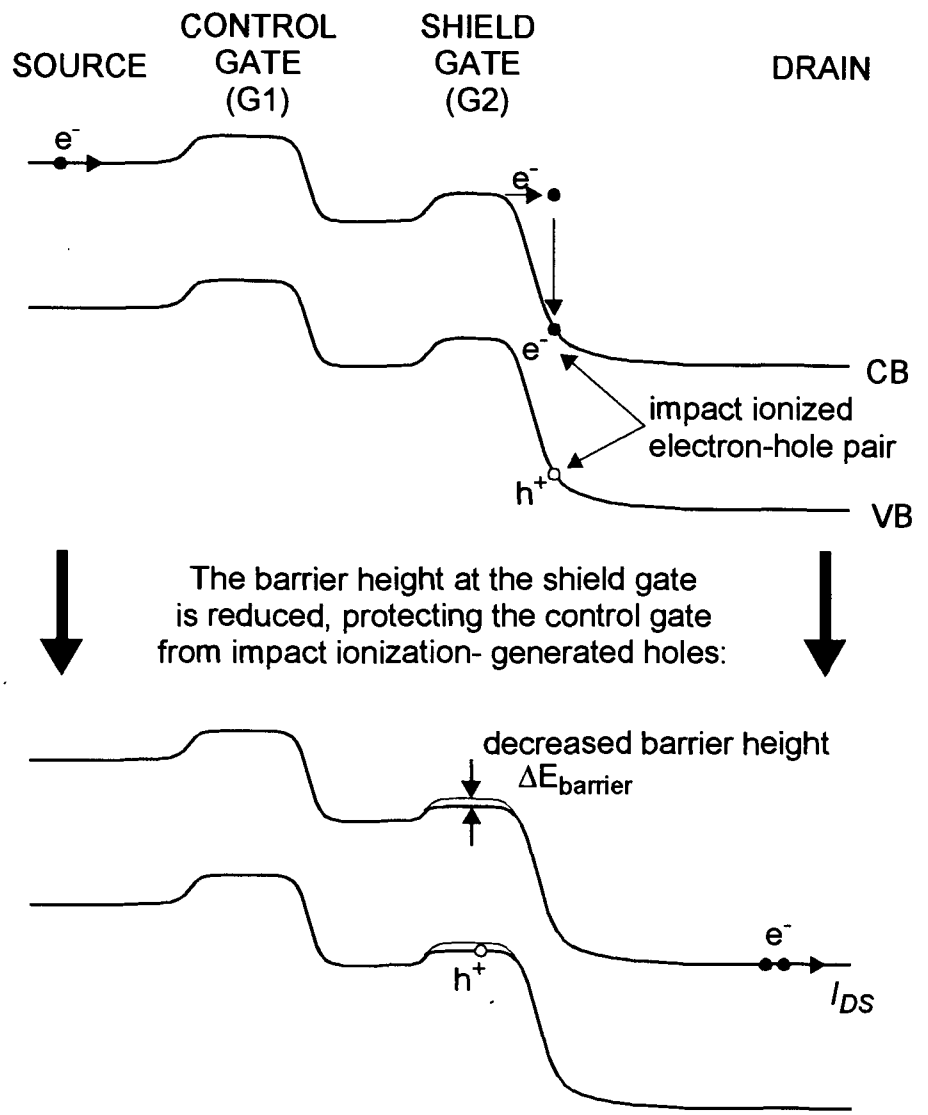

Figure 3-7: Collection of impact ionization generated holes underneath the shield gate and away from the control gate.

generated in the high field region between the shield gate and the drain electrode. The clear decoupling of gate current leakage mechanisms proves that the kink effect in standard InAs/AlSb HFETs takes place through the parasitic bipolar effect arising from the accumulation of impact ionization holes near the source/gate region of single gate HFETs. The dual-gate approach is more attractive than the back-gate approach favored by Brar

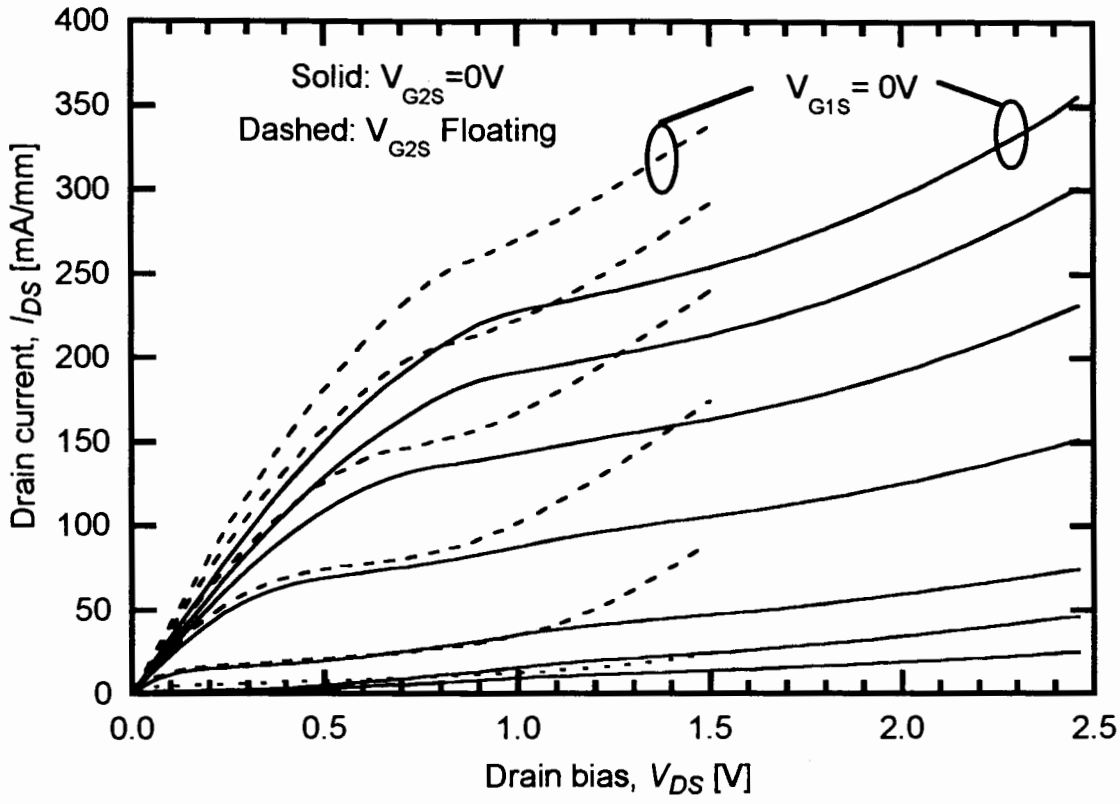

Figure 3-8 : Measured drain I-V characteristics for otherwise identical single- and dual-gate 1.0μm InAs/AlSb HFETs. Gate voltages V_G stepped from 0 to -1.2V.

et al. (see "Back-gate HFETs" on page 55) because it avoids the use of highly doped layers under the device active region, thus eliminating the large parasitic capacitances and leakage currents associated with highly conductive buffer layers.

No microwave characterizations of dual-gate InAs/AlSb HFETs were performed in the course of this work. Other researchers however have found that 0.4 μm dual-gate InAs/AlSb HFETs show cutoff frequencies f_T and f_{MAX} comparable to those of single-gate HFETs fabricated on the same wafer layer structure [13]. Other reports have shown that well designed high-transconductance dual-gate HFETs can show f_T's approaching 80% of those achieved in single-gate HFETs [41].

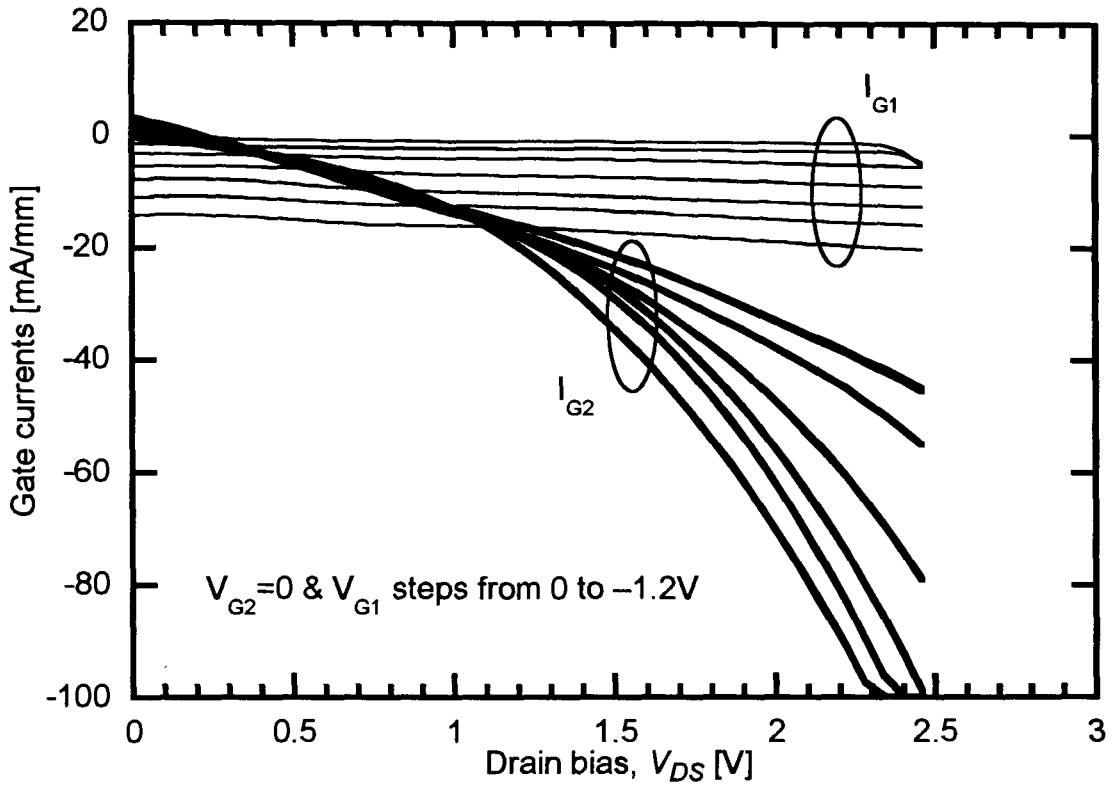

Figure 3-9 : Measured control gate (thin lines) and shield gate (thick lines) currents for dual-gate 1.0μm InAs/AlSb HFET.

3.2.2 AlSb/InAs/AlSb quantum well engineering

Noting that reducing the quantum well thickness increases the ground state energy of a quantum well, Bolognesi recognized that narrower AlSb/InAs/AlSb quantum well may increase the effective bandgap for the InAs quantum well and reduce the rate of impact ionization in the channel layer [5]. Quantum well thicknesses of 130Å down to 70Å were studied in that work, but the increase in energy gap $\Delta E_{G,eff}$= 0.130eV merely delayed the kink effect onset drain bias by a comparable amount. The narrower quantum well was limited by interface roughness scattering, which affects the low-field mobility in InAs/AlSb quantum wells even at room temperature [5]. With the small improvement in the impact ionization rate achieved by narrowing the quantum well at the expense of low-field mobility, there seemed little promise to this approach. In the present work, we revisit

this approach and use an even narrower quantum well. The same layers are also used in Chapter 5 to investigate the effect of quantum well width on the microwave performance of InAs/AlSb HFETs.

In principle, if the quantum well energy gap is sufficiently increased the impact ionization should decrease significantly. Because electrons are quantum mechanically confined to the quantum well, the bound state energy levels follow an approximate inverse square law for the quantum well thickness: for infinite quantum wells, the energy levels are simply:

$$E_n = \frac{\hbar^2 \pi^2}{2m^* n^2 L^2} \tag{3-1}$$

where m^* is the effective mass, L is the quantum well width, and n is the energy level. For non-infinite quantum wells, the following equations must be solved graphically. The even solutions (including the ground state) satisfy the transcendental equation [60]

$$k \tan ka = \kappa \tag{3-2}$$

and the odd solutions satisfy

$$k \cot ka = -\kappa \tag{3-3}$$

where k and $i\kappa$ are the wave numbers inside and outside the quantum well. The above equations are solved simultaneously with the relation for the energy:

$$k^2 + \kappa^2 = \frac{2m^* V_0}{\hbar} \tag{3-4}$$

Unfortunately, the above equations neglect the non-parabolicity of the Γ valley. Tuttle [73] argued that the infinite well approximation is a good one in InAs/AlSb quantum wells, but that one must include the effects of non-parabolicity of the InAs conduction band. He derived a convenient, analytical approximation that gives the energy levels in an infinite, quantum well with a non-parabolic conduction band:

$$E_n = \frac{E_G}{2}\left(\sqrt{1+\frac{2\pi^2 n^2 \hbar^2}{m_p E_G L^2}} - 1\right) \qquad (3\text{–}5)$$

which gives energies within 0.02eV of the solution obtained from *k·p* perturbation theory. The first two energy levels for each model are plotted as a function of quantum well thickness in Figure 3-10; A 50Å quantum well should have an energy gap of 0.34eV higher than in the bulk (nearly doubling the effective energy gap), compared with 0.12eV for a 100Å quantum well, and 0.06eV for a 150Å quantum well. In the work by Bolognesi, however, only a small improvement was seen for the increase of energy gap of 0.13eV between quantum well thicknesses of 130Å and 70Å.

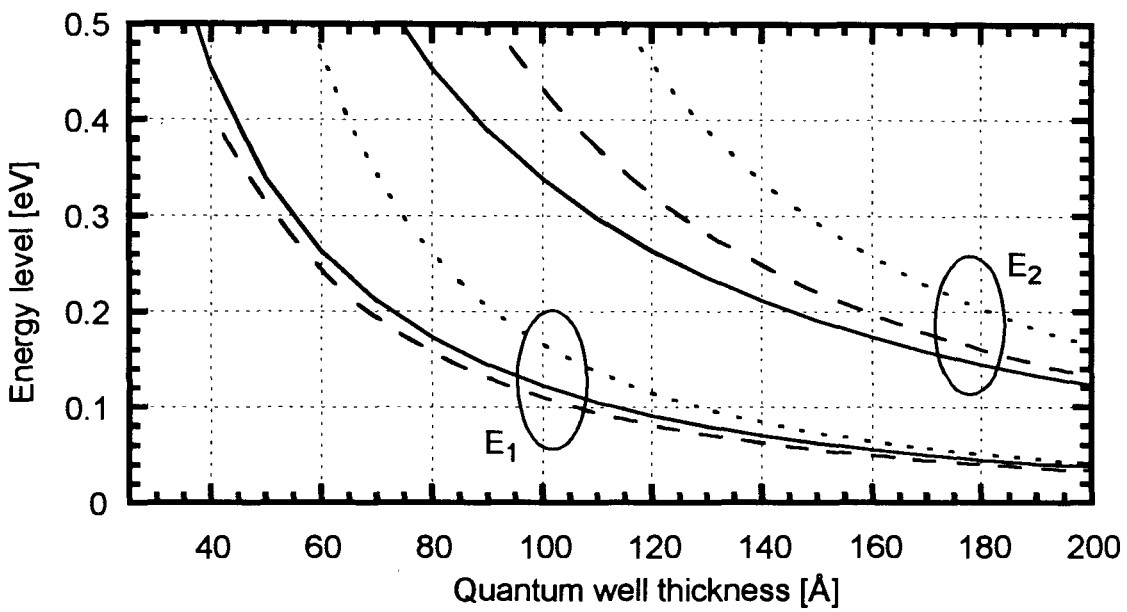

Figure 3-10: First two energy levels of InAs/AlSb quantum well: infinite quantum well including non-parabolicity of bands [73], solid lines; 1.3eV quantum well neglecting non-parabolicity, dashed lines; infinite quantum well neglecting non-parabolicity, dotted lines.

The I-V characteristics of two nominally identical HFETs that differ only in the thickness of the quantum well are shown in Figure 3-11 on page 53. The mobilities of the as-grown 50Å and 100Å quantum well wafers are 9,260cm^2/V·s and

20,720$cm^2/V{\cdot}s$, and the sheet concentrations are $1.7{\cdot}10^{12}cm^{-2}$ and $2.1{\cdot}10^{12}cm^{-2}$ respectively. The much lower mobility of the 50Å wafer results in a lower sheet conductivity; we also suspect that variations in processing of this wafer decrease the channel width by 10%. The narrower quantum well device shows an apparently reduced kink and better saturation of the current which result in a lower output conductance. However, when the current is scaled (normalized) to match the 100Å quantum well sample, the improvement in the I-V characteristics is barely noticeable.

The measured gate leakage current during transistor operation (Figure 3-12) is the sum of the diode leakage current and the impact ionization generated hole leakage current responsible for the bell-shape of the characteristics. As seen in the Figure, the leakage current is of similar magnitude for both the 50Å and the 100Å quantum well devices. This suggests that either the rate of impact ionization is not significantly reduced for the narrower quantum well device, or else that the leakage current is limited by some other mechanism. The higher diode leakage in the 50Å device may be due to mesa sidewall leakage but its origin has not been confirmed.

In Chapter 5, we see that reduced mobility and decreased transconductance in the 50Å devices lead to a ~ 25GHz·μm current gain cutoff frequency (f_T)•gatelength product, while the 100Å quantum well devices show a ~ 40GHz·μm f_T•gatelength product. The power gain to current gain cutoff frequency ratio f_{MAX}/f_T for 50Å devices is consistently higher (> 2) than for the 100Å device (< 1.5), suggesting that some reduction in the rate of impact ionization has been obtained: the f_{MAX}/f_T ratio decreases with increasing output conductance g_{DS} (see [1] for example) which is higher in devices with higher rates of impact ionization. This apparent discrepancy between microwave and DC measurements is resolved in Chapter 5.

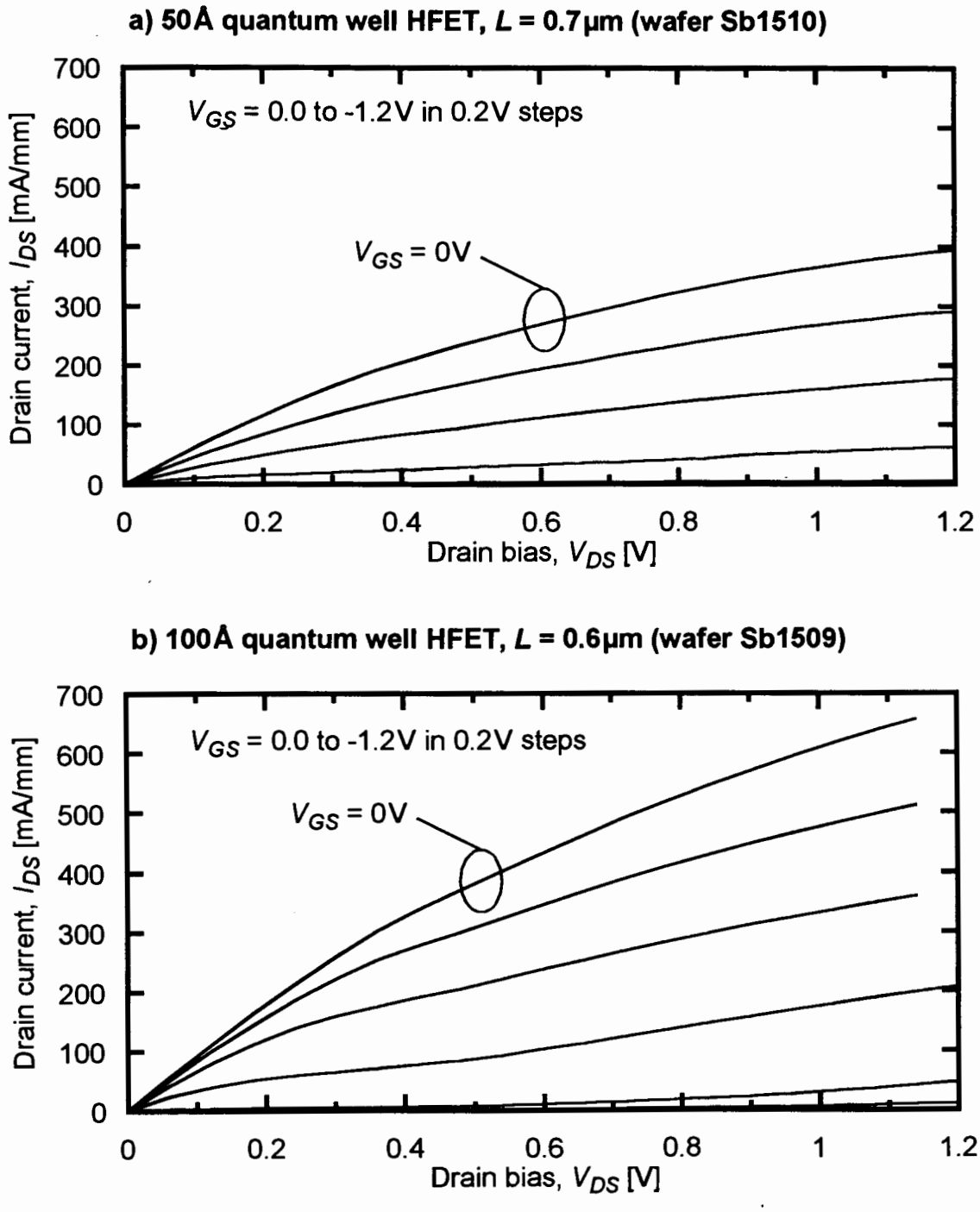

Figure 3-11 : Drain characteristics of (a) 50Å and (b) 100Å quantum well HFETs that are otherwise nominally identical.

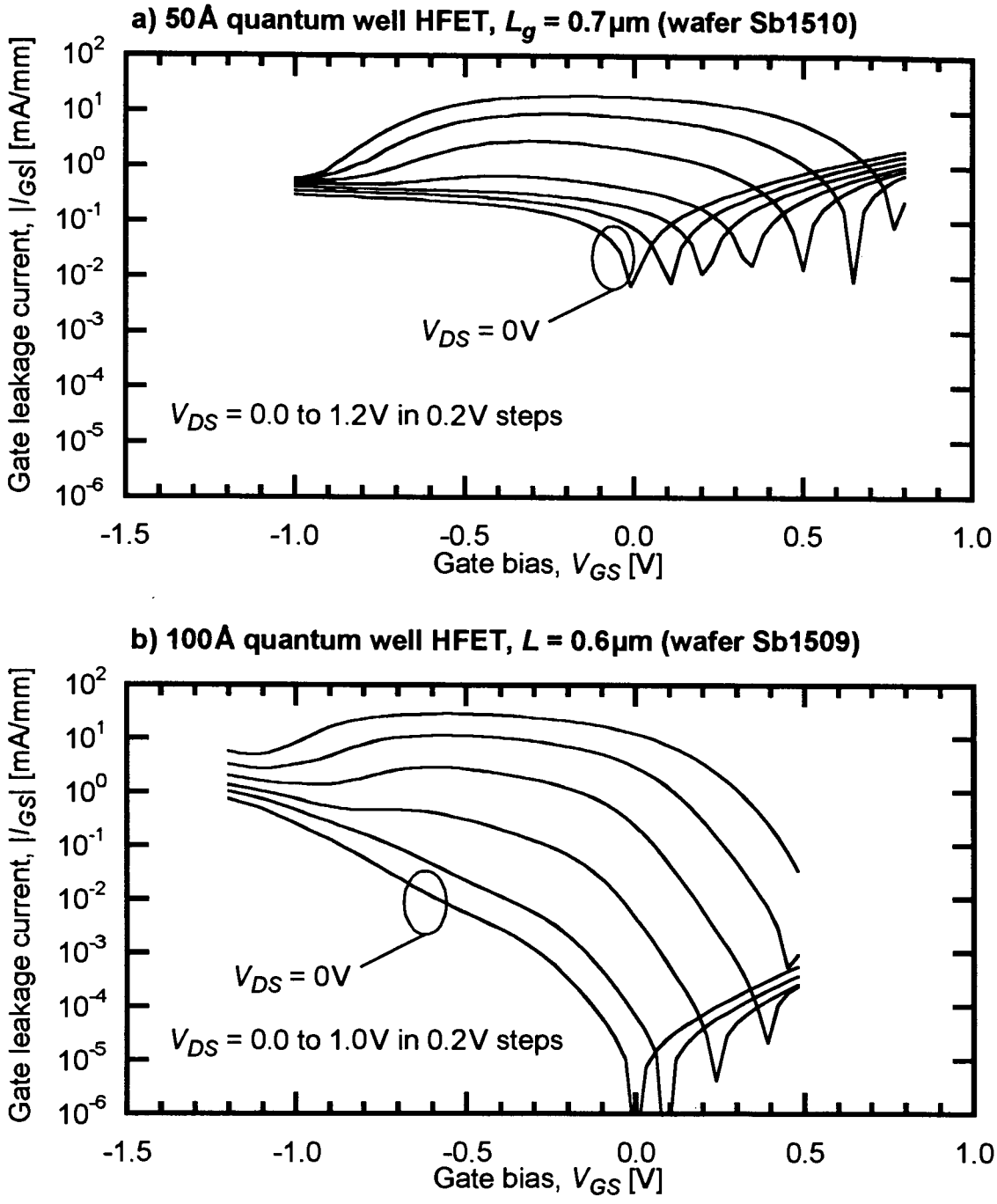

Figure 3-12 : Bell-shaped gate leakage current characteristics of (a) 50Å and (b) 100Å quantum well HFETs that are otherwise nominally identical. Hole leakage is reduced beyond pinch-off (when little current is flowing) and when gate is positively biased. Diode leakage increases with gate-channel bias. The 50Å device suffers from anomalously high diode leakage that may relate to mesa sidewall leakage. The bell shape arises from impact ionization generated holes drained through the gate.

3.2.3 Back-gate HFETs

During the course of this work, the group at UC Santa Barbara further clarified the connection between impact ionization hole accumulation in the buffer layer and the kink effect [13]. The space charge caused by the hole accumulation can be removed by the addition of a grounded, conducting GaSb back-gate to the HFET layer structure: the use of a back-gate results in a dramatic improvement of the DC characteristics. Unfortunately, their work was restricted to long gatelengths.

The first study of the DC and microwave performance of back-gated InAs/AlSb HFETs was reported by Boos *et al.* [11]. The DC characteristics showed a far smaller kink than previous results by the same group. However, their devices fail to pinch-off, probably because of parasitic conduction through the heavily p-doped GaSb back-gate. The microwave performance of these devices was variable, with a stated intrinsic current gain cut-off frequency f_T of approximately 100 GHz for 0.5 µm devices (no data was shown), but of only 150 GHz for 0.1 µm devices. The authors suggest that optimizations of the p^+ GaSb layer thickness and doping concentration are required. Despite the removal of holes, a high output conductance and a large output capacitance probably limit the maximum frequency of oscillation f_{MAX} to only 80 GHz.

The presence of an additional conductive plane in the HFET presents new difficulties to this technology. Additional contacts are required either to ground or to bias the GaSb back-gate. A conductive layer in close proximity to the conducting channel adds parasitic capacitances to the small-signal model. On the other hand, if the GaSb plane is too far below the InAs channel, the hole current being removed from the buffer layers still results in a significant space charge and a significant kink in the output characteristics. To date, it appears the most promising approach to control impact ionization effects in InAs/AlSb HFETs remains the use of a dual-gate architecture.

CHAPTER 4
Evidence of Traps in InAs/AlSb HFETs: Sidegating Measurements

Overview

In the previous Chapter, we examined the importance of impact ionization to the DC performance of InAs/AlSb HFETs. Impact ionization generated holes are not confined to the quantum well, because of the staggered band lineup at InAs/AlSb interfaces (see Figure 1-5 on page 13), but are injected into the barrier and/or buffer layers and lead to the kink effect (see Figure 3-3 on page 40). We have not determined the exact nature of this hole charge, but holes clearly migrate through AlSb barriers while inducing a parasitic bipolar source-gate barrier lowering, as well as some gate leakage current. In this Chapter, we consider the interaction between holes and traps in the barrier and buffer layers. The penetration of impact ionization generated holes into the buffer is not controlled and so impact ionization generated holes are not suitable for a study of a hole/trap interaction. Instead, we look at the effect of holes injected from the bottom of the AlGaSb buffer by a strongly forward-biased sidegate. A sidegate is a common test structure useful for evaluation of the interdevice isolation provided by the buffer layers. Despite the very good isolation provided by these buffers (leakage currents < 10nA for moderate sidegate voltages $|V_{SG}| < 5$V), there is a pronounced *sidegating-induced negative differential resistance* (SINDR) at higher positive sidegate voltages ($V_{SG} > 5$V). This phenomenon was completely unexpected, as no such effect has been reported for any other material system.

The temperature and frequency dependence of SINDR indicates that deep levels must be involved in the effect.

The steady state electron-hole concentrations in HFETs can be described in terms of Shockley-Read-Hall (SRH) statistics [5][39][63]. The steady-state electron occupation probability f_D of a deep level (i.e. trap) is given by

$$f_D = \frac{C_n n + C_p p_D}{C_n(n + n_D) + C_p(p + p_D)} \tag{4–1}$$

where the n and p are the free electron and hole concentrations, n_D and p_D are the electron and hole concentrations when their quasi-Fermi levels are at the deep level, and C_n and C_p are the electron and hole capture rates:

$$n_D = N_C \exp\left(\frac{-(E_C - E_T)}{kT}\right) \qquad p_D = N_V \exp\left(\frac{-(E_T - E_V)}{kT}\right) \tag{4–2}$$

$$C_n = \sigma_n \left(\frac{3kT}{m_n^*}\right)^{1/2} \qquad C_p = \sigma_p \left(\frac{3kT}{m_p^*}\right)^{1/2} \tag{4–3}$$

where σ_n and σ_p are the electron and hole capture cross-sections, E_T is the energy level of the trap, N_T is the trap volumetric density, and the other values retain their usual meaning.

As was argued by Kunihiro *et al.* [39], hole traps emit electrons in the presence of a large hole concentration. Whether the trap is a donor or an acceptor, the hole trap charge changes to a more positive value that can approach the trap concentration. Depending on $(\partial f_D / \partial p) N_T$, the change in charge may exceed the hole concentration [39].

The above idea is important in the understanding of the relationship between holes, hole traps, and the electron concentration in InAs/AlSb HFET channels because the positive space charge associated with the holes and hole traps can affect the channel conductivity. In this Chapter, we begin with a discussion of previous evidence for

traps in InAs/AlSb structures. The experimental results for SINDR are presented next, and we conclude with an analysis of the results.

4.1 Previous evidence of traps in InAs/AlSb system

Because of its very deep quantum well, the InAs/AlSb system has been of interest to the compound semiconductor community since the development of high-quality MBE-grown layers based on this material system. A negative persistent photoconductivity effect was attributed to the presence of an electron trap in the AlSb barrier a little above the Fermi level (see [43] and references 3-5 therein). With illumination at low (< 150K) temperatures, electrons populate these traps, and so induce a net reduced electron sheet concentration in the AlSb/InAs/AlSb channel. Direct evidence for traps was provided when Subanna *et al.* [66] found that heavily Te-doped $Al_{0.8}Ga_{0.2}Sb$ layers feature a negligible dopant activation. The tellurium self-compensates because of an associated DX-center. It also serves as a recombination center for holes [5]. A DLTS study of binary AlSb with Te doping was performed by Nakagawa *et al.* [51], who found that the best-defined electron trap had a thermal electron emission energy of 0.26eV. A sample doped with Te doping of $3.1 \cdot 10^{17} cm^{-2}$ showed a trap concentration of $2.0 \cdot 10^{17} cm^{-3}$. These results are similar to those of Polyakov *et al.* [57], who found that Te-doped $Al_xGa_{1-x}As_{0.08x}Sb_{1-0.08x}$ layers (lattice matched to GaSb) have donors with large ionization energies of 0.12eV to 0.23eV, and that free electron concentrations were orders of magnitude lower than what would be expected from the Te doping levels. Kruppa *et al.* reported output resistance dispersion measurements on two different InAs/AlSb HFET layer structures [38]. They found that transition frequencies and their activation energies were very bias sensitive, and obtained activation energies of 0.05eV to 0.2eV depending on the gate bias. The results were inconclusive, but suggested that traps associated with residual As in AlSb, or perhaps residual Te doping from a contaminated MBE chamber,

may act as a recombination center. All previous reports have been concerned with electron traps. The present work is the first concerned with apparent hole trapping phenomena.

4.2 Sidegating measurements of InAs/AlSb HFETs

4.2.1 Test structure fabrication

The epitaxial layers used in this study were grown on GaAs (100) semi-insulating substrates. From the substrate up (see Figure 4-1), a 1000Å GaAs buffer layer is followed by a 3μm strain-relaxed AlSb buffer layer, and a 2000Å $Al_{0.8}Ga_{0.2}Sb$ etch stop layer that serves as the mesa floor in the device isolation. The active layers in the HFET structure are: an 80Å AlSb bottom barrier, a 100Å InAs quantum well, and an 85Å AlSb top barrier. These are followed by a 175Å $AlSb_{0.9}As_{0.1}$ digital alloy superlattice and a 50Å GaSb/InAs composite cap layer. All epitaxial layers were not-intentionally doped. Hall measurements carried out on the as-grown wafer revealed a 300K mobility of 18,400$cm^2/V{\cdot}s$ and an electron sheet density of $1.86{\cdot}10^{12}cm^{-2}$.

Device fabrication relied on non-alloyed Ti/Au Ohmic contacts being deposited directly on the InAs quantum well. The Ohmic contact formation was followed by a mesa etch and then Ti/Au gate and pad metallization. A detailed process run sheet is given in the Appendix. In addition to the standard HFET structure, a sidegate (Schottky metal) electrode located 4μm away from the HFET mesa edge was deposited directly on the AlGaSb mesa floor (see Figure 4-2). The requirement for non-alloyed Ohmic contacts is clear: alloying Ohmic contacts diffuses gold and dopant deep into the buffer layers. Alloyed Ohmic contacts were found to "short-circuit" much of the sidegating effect.

4.2.2 Room temperature measurements

The initial room temperature sidegating measurements were performed with a conventional HP4145B semiconductor parameter analyzer. Drain characteristics

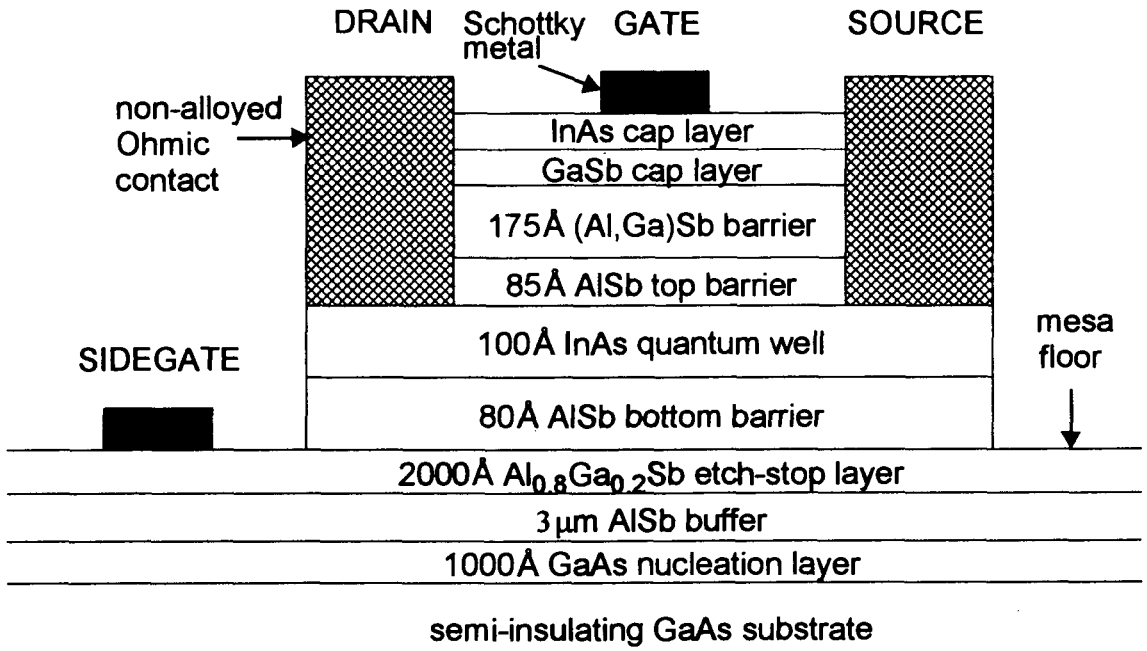

Figure 4-1 : Cross-section of sidegating InAs/AlSb HFET test structure with non-alloyed Ohmic contacts (not to scale).

for an HFET with (a) a positive sidegate potential of +10V and (b) a negative sidegate potential of -10V are shown in Figure 4-3 (a) and (b). The data were taken in the dark, with a positive drain sweep direction and using medium integration time. That is, the drain bias started at $V_{DS} = 0$V, with each sweep taking roughly 1 second. (The sweep direction is important, because the I-V characteristics display a time- and temperature- dependent hysteresis which is investigated in more detail below.) Large positive sidegate voltages result in a clear peak in the I-V characteristics: I_{DS} increases for low drain bias (as compared with a sidegating-free current) but at high drain biases, the drain current becomes independent of sidegate voltage, and rejoins the $V_{SG} = 0$V values.

Such a low drain-bias sidegating-induced negative differential resistance (SINDR), to the best of our knowledge, has not been reported before. Because the SINDR effect occurs at relatively low voltages, we can immediately discount the possibilities of real-space transfer [32] or device self-heating. Under low bias conditions, electrons never

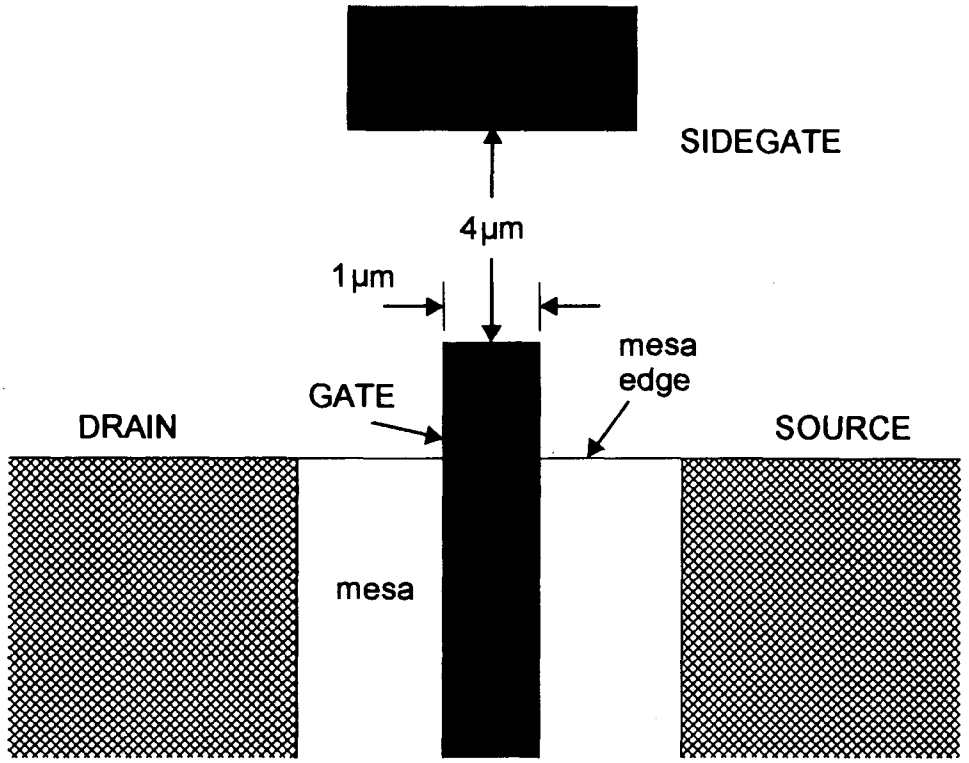

Figure 4-2 : Top view of sidegating InAs/AlSb HFET test structure (approx. to scale).

gain enough kinetic energy to overcome the $\Delta E_C \sim 1.35$eV AlSb/InAs/AlSb quantum well barrier.

The sidegate leakage current measured as a function of bias conditions is shown in Figure 4-4. A small sidegating leakage current < 100nA flows through the sidegate electrode and the buffer during the measurement. There is a small increase in leakage for gate biases near $V_G = 0$V and for higher drain biases V_{DS}. For -5V < V_{SG} < 5V, the sidegate leakage current remains below 10nA, indicating that the buffer layers provide a suitable interdevice isolation for realistic integrated circuit voltages.

4.2.3 Variable sweep frequency measurements

To investigate the frequency dependence of SINDR and the associate hysteresis, we utilized a custom measurement circuit based on a standard DC-10MHz wave

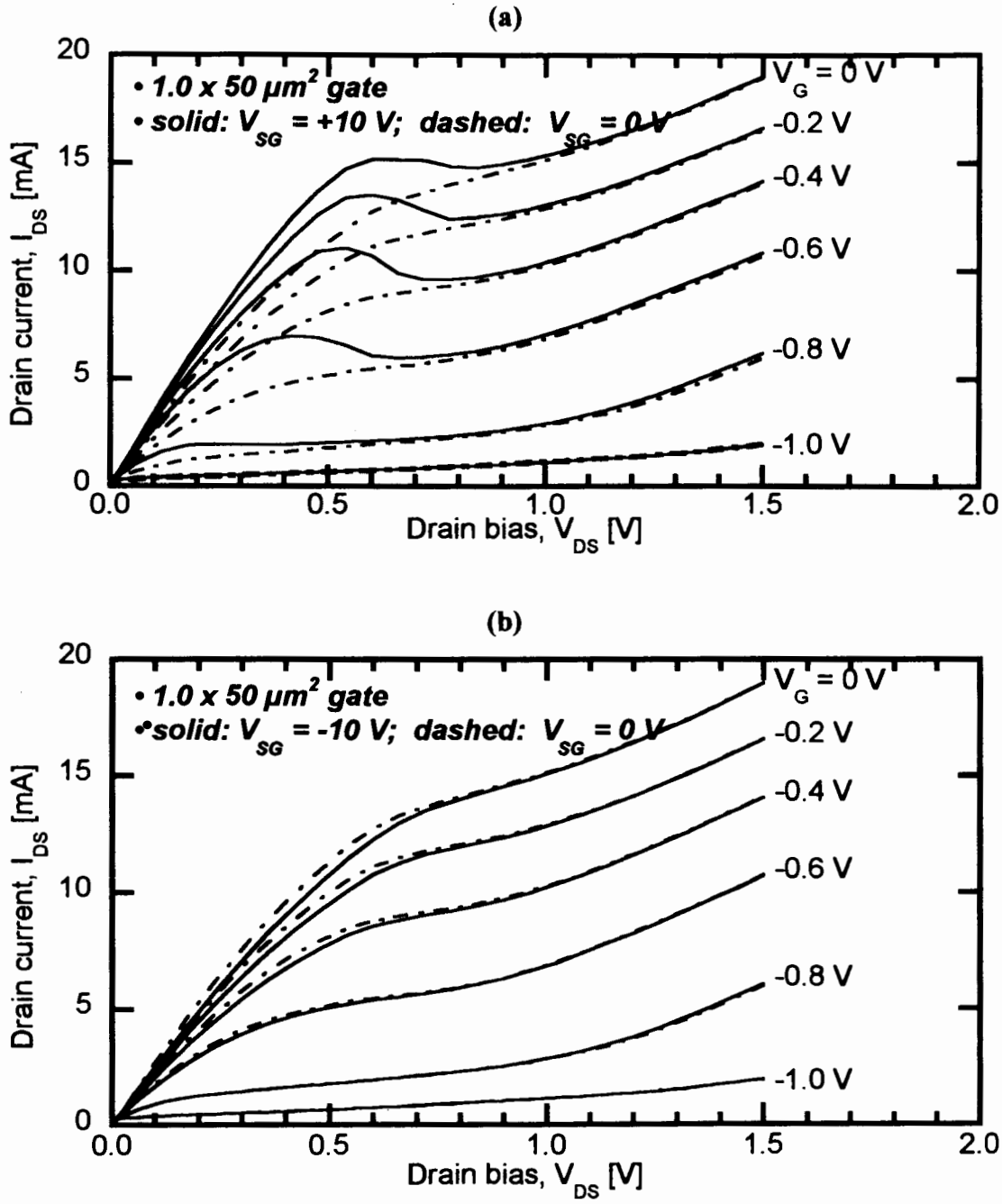

Figure 4-3 : Overlay of room temperature drain characteristics for sidegate voltages of $V_{SG} = 0V$ (dashed lines), and simultaneously (a) $V_{SG} = +10V$ or (b) $V_{SG} = -10V$ (solid lines). At large positive sidegate voltages SINDR appears for low V_{DS}. The characteristics show no sidegating effect at high drain biases. Large negative sidegate voltages have almost no effect on the drain I-V characteristics.

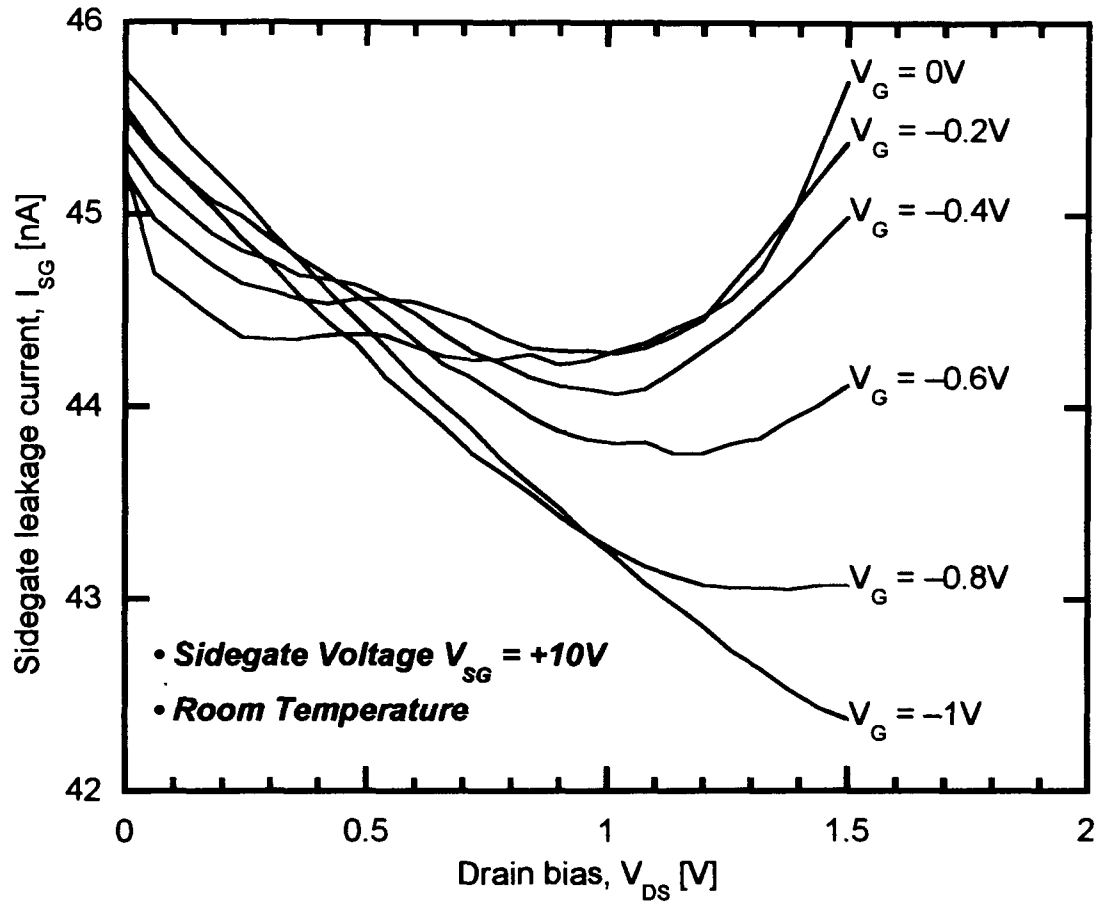

Figure 4-4 : Room temperature sidegate leakage current as a function of bias conditions for a sidegate electrode located 4μm away from the InAs/AlSb HFET mesa edge for a sidegate voltage V_{SG} = +10V.

generator and digitizing oscilloscope (see Figure 4-5). Typical room temperature I-V curves are shown in Figure 4-6, taken with a sidegate bias V_{SG} = 15V, and a gate bias of V_G = -0.5V for drain bias sweep frequencies f = 0.5Hz, 50Hz, 5kHz, and 50kHz. The drain I-V characteristics clearly display NDR on the "up" sweep direction (i.e. increasing from V_{DS} = 0 to 1.5V) whereas SINDR tends to disappear in the "down" sweep direction. Furthermore, SINDR and the associated hysteresis collapse when the sweep frequency reaches the 1-5kHz range, and SINDR is completely quenched at 50kHz. Therefore, there exists a certain cut-off frequency above which the mechanism responsible for SINDR cannot follow the drain bias sweep. The hysteretic behavior of the NDR and its low character-

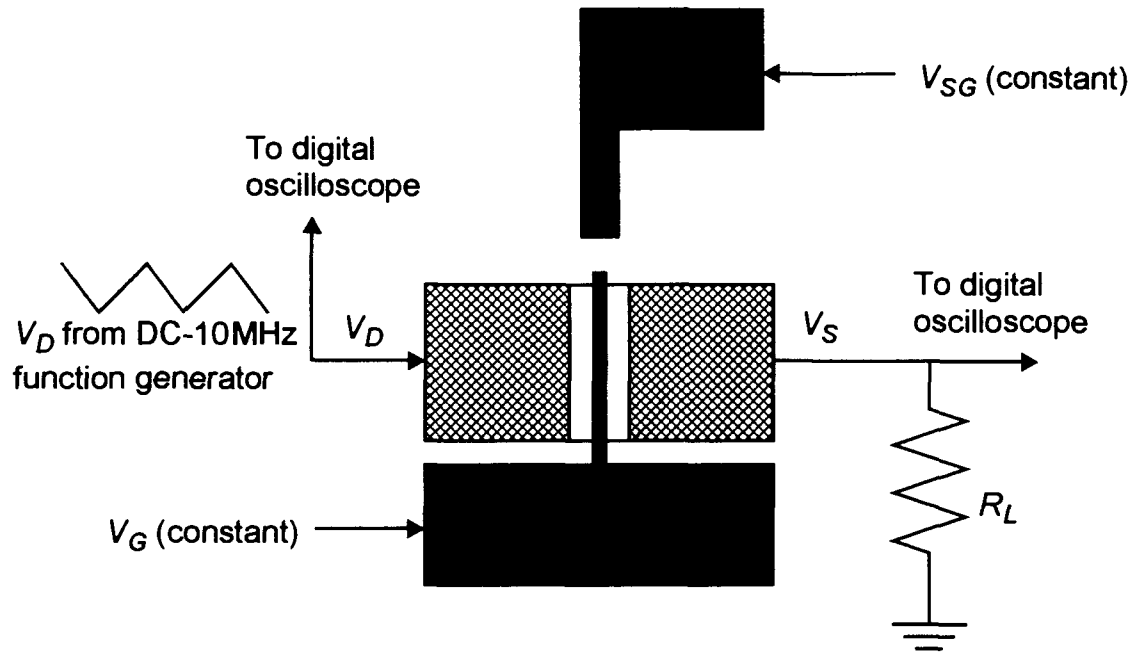

Figure 4-5 : Diagram of variable-frequency sidegating measurement circuit.

istic frequency suggest that one or more deep level center(s) play(s) a fundamental role in SINDR because trapped carriers can have long time constants. Since the characteristic emission time τ from deep level centers is expected to vary with temperature, the SINDR effect should be sensitive to the sample temperature. The temperature dependence of SINDR in InAs/AlSb HFETs is examined in the following Section.

4.2.4 Temperature dependence of SINDR

For the temperature-dependent characterization of SINDR, InAs/AlSb HFETs were wire-bonded and mounted into a closed-cycle cryostat. Sidegating and drain current measurements were performed in the dark, over the temperature range of 250K to 325K; see Figure 4-7 on page 66. The temperature limits were set on the upper end by the temperature controller of the cryostat, and on the lower end simply by the disappearance of SINDR at easily measurable frequencies.

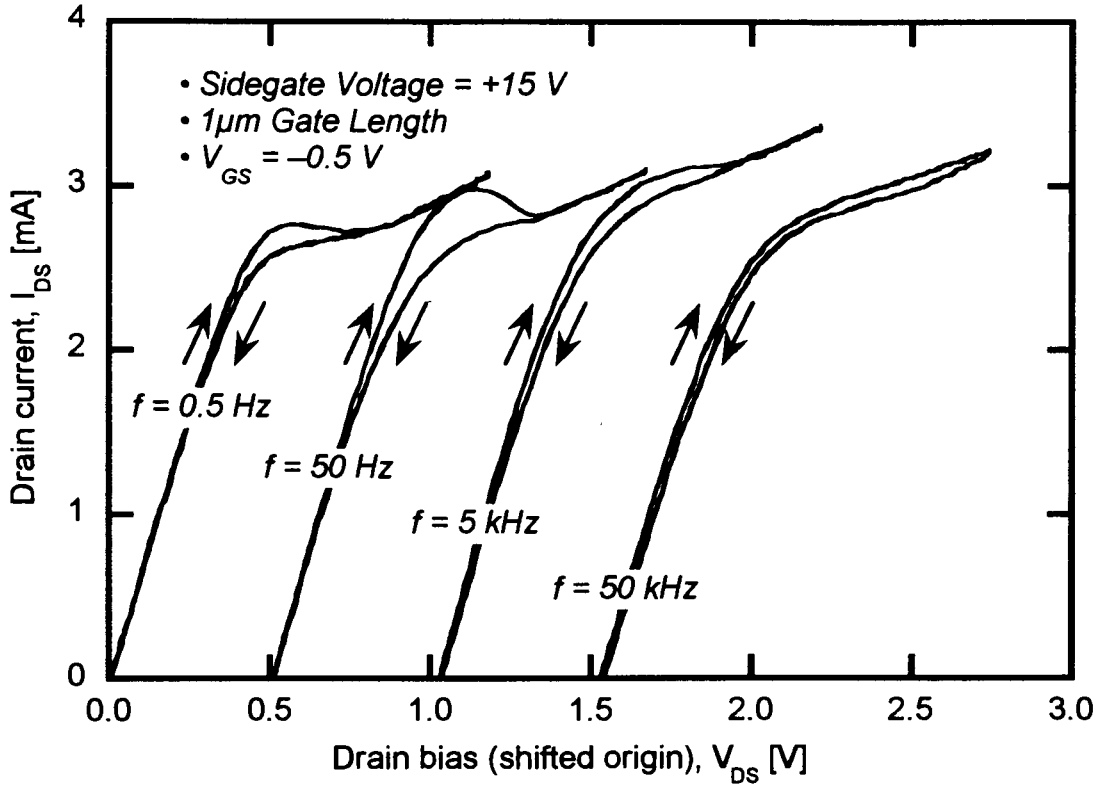

Figure 4-6 : Room temperature drain characteristic measurements obtained using variable sweep frequency circuit with a sidegate potential V_{SG} = +15V, and a gate bias of V_G = -0.5V. The NDR regions and the associated hysteresis disappear at higher frequencies. This behavior suggests that a slow deep level is associated with SINDR.

As the temperature is increased beyond room temperature, the sidegating-induced NDR peak becomes more pronounced. Conversely, the SINDR effect is considerably weaker when the sample is cooled, and disappears for all practical sweep frequencies below 260K. The SINDR effect cut-off frequency also increases with the sample temperature. Figure 4-7 displays typical I-V characteristics for V_{SG} = +15V. The origins of the curves are offset linearly with temperature in the *y* (drain current) direction, and logarithmically with sweep frequency in the *x* (drain bias) direction. Each column, therefore, represents a given sweep frequency, whereas each row represents a given temperature. As lower temperatures increase the characteristic emission (de-trapping) and capture (trapping) time of deep level centers, the SINDR disappears at lower frequencies when the

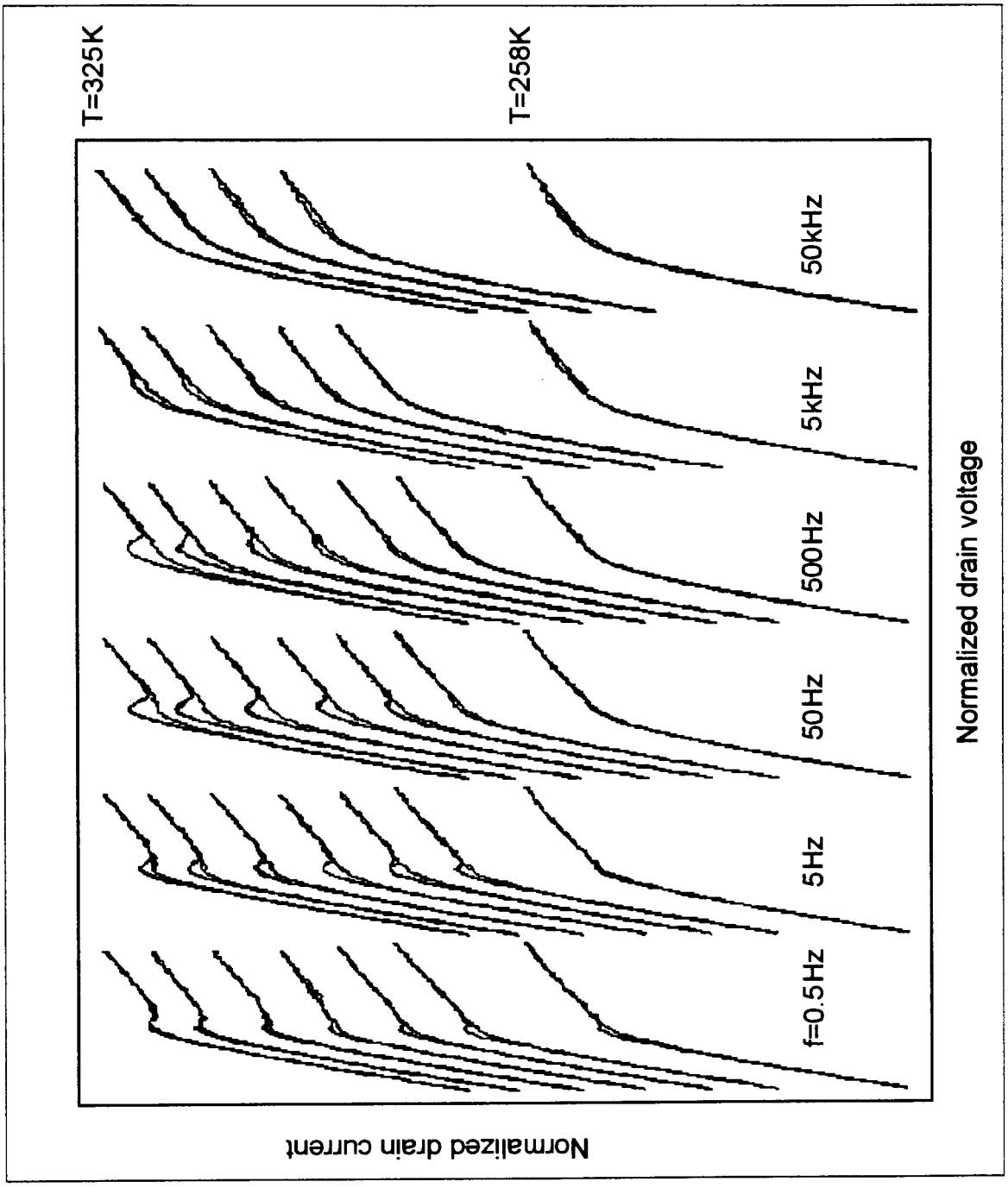

Figure 4-7: Temperature and frequency dependence of SINDR measured at temperatures of 358, 278, 288, 298, 308, 318, and 325K, at sweep frequencies of 0.5, 5, 50, 500, 5000 and 50,000 Hz. The voltage and current axes are normalized for clarity, and offset to show temperature-frequency dependence. No SINDR is observed below 260K.

HFETs are cooled. Plotting the approximate characteristic SINDR cut-off frequency as a function of inverse temperature, we see that the data approximately follow a straight line with an activation energy $E_A = 0.93 \pm 0.05$eV on a semi-log plot (see Figure 4-8). If a single deep center is involved in SINDR, its ionization energy should correspond to the present activation energy.

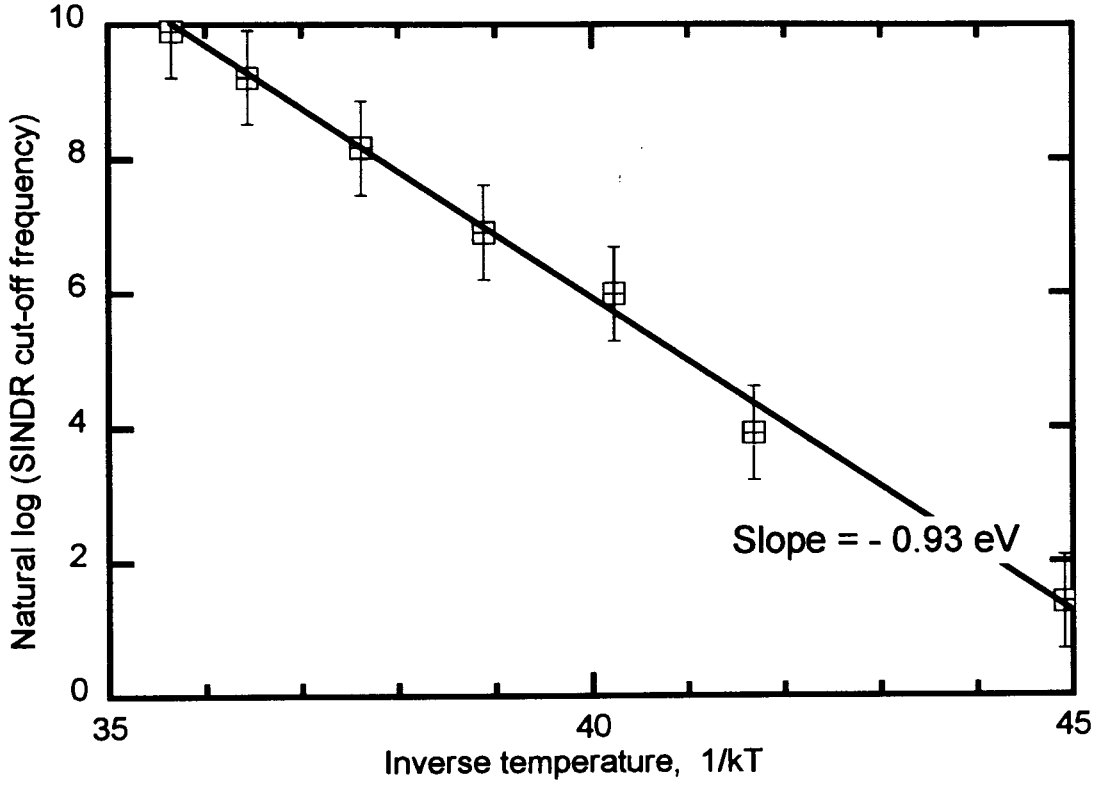

Figure 4-8 : Plot of the natural logarithm of the SINDR cut-off frequency as a function of inverse temperature. SINDR displays an activation energy of 0.93±0.05eV.

4.2.5 Measurements with illumination

For on-wafer measurements, one can introduce a source of illumination simply by turning on the microscope light (halogen white light). With illumination, a large number of electron-hole pairs are optically generated, changing the dynamics of SINDR. Figure 4-9 shows typical room temperature I-V curves taken with a sidegate bias $V_{SG} = 15$V, and a gate bias of $V_G = -0.5$V for drain bias sweep frequencies of $f = 0.5$Hz,

50Hz, 500Hz, 5kHz and 50kHz, with the microscope light at its minimum setting. At higher light levels, the sidegating-induced NDR washes out: the peak decreases and widens at moderate frequencies (Figure 4-10).

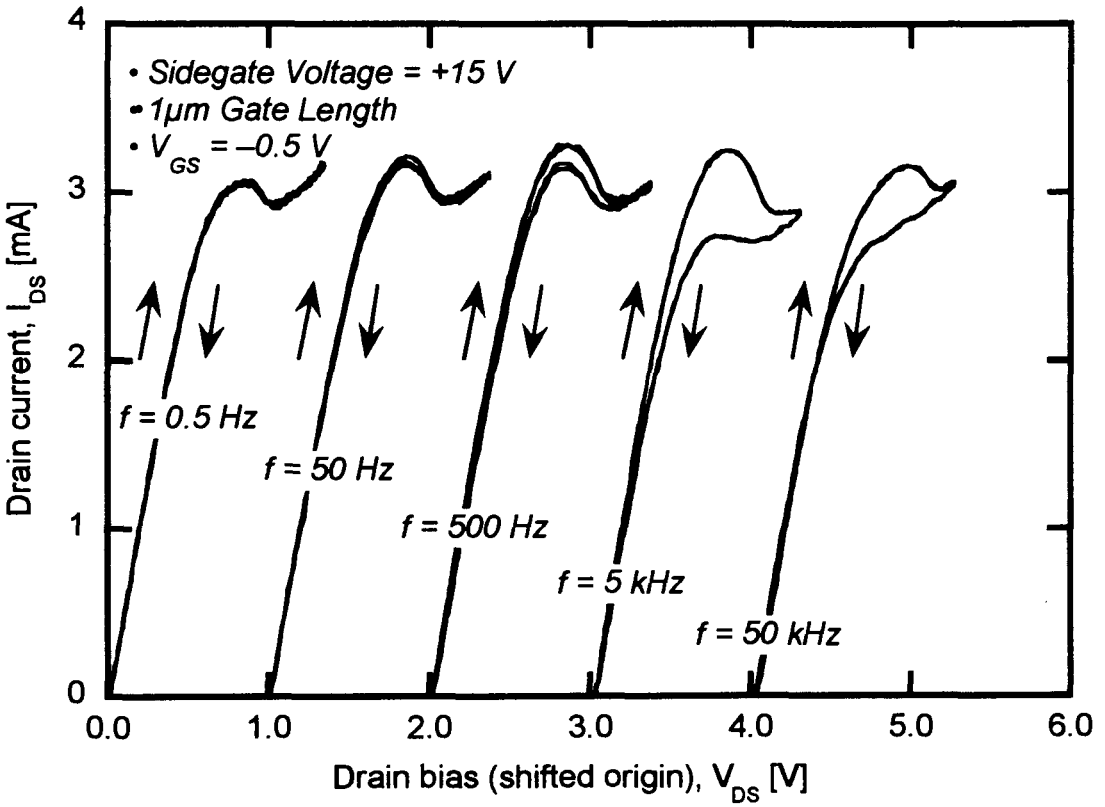

Figure 4-9 : Room temperature drain I-V measurements obtained with low illumination through the microscope lens. Measurements were obtained with variable sweep frequency measurement circuit, using a sidegate potential V_{SG} = +15V, and a gate bias of V_G = -0.5V.

At low frequencies, the hysteresis disappears but the NDR occurs in both sweep directions. At the higher frequencies at which SINDR starts to disappear without illumination, SINDR remains and strong hysteresis occurs with illumination. With the experimental setup used, frequencies much beyond 50kHz were not possible because significant parasitic capacitances mask SINDR. In addition, illumination was not compatible with the cryostat used for the temperature dependent measurements.

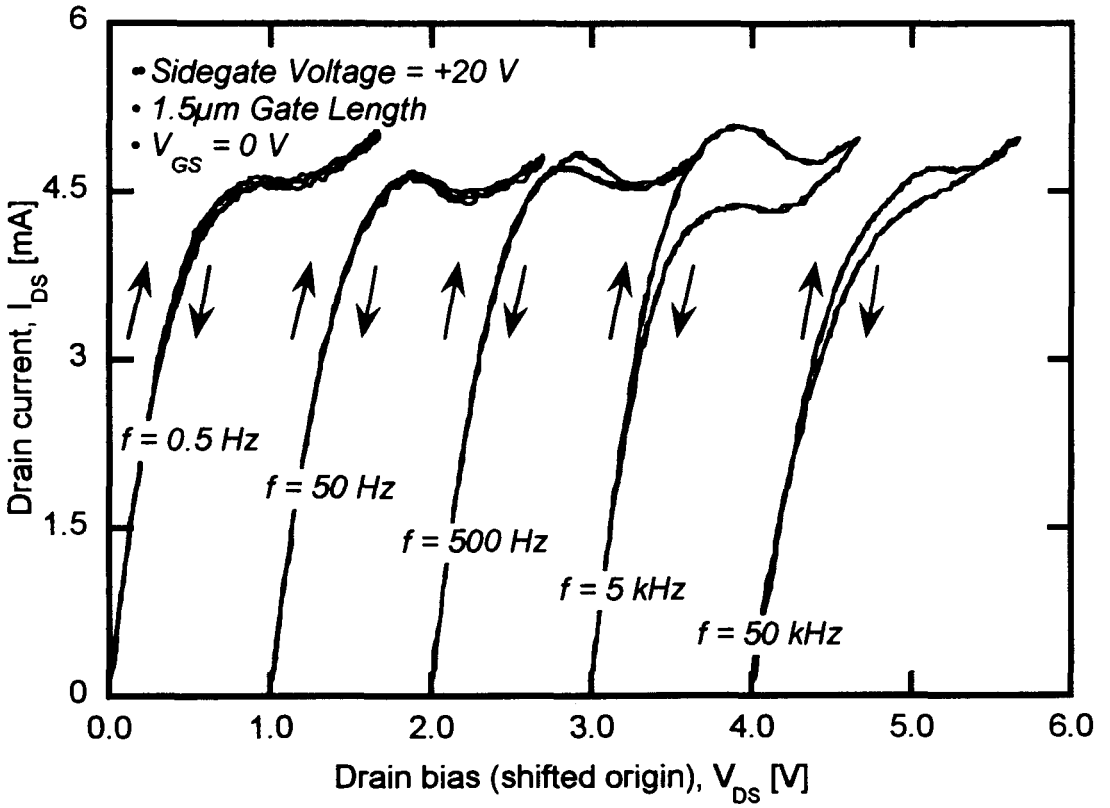

Figure 4-10 : Room temperature drain I-V measurements obtained with maximum illumination through the microscope lens. Measurements were obtained with variable sweep frequency measurement circuit, using a sidegate potential V_{SG} = +20 V, and a gate bias of V_G = 0 V.

4.3 Analysis and discussion

Because of the low hole Schottky barrier height of metals on antimonide surfaces, the sidegate current mechanism most likely occurs by injection of holes from the sidegate into the AlGaSb buffer layers. From the Shockley-Read-Hall (SRH) analysis introduced earlier in equation (4-1), we see that the sidegate hole injection and the associated excess hole concentration p in the AlGaSb buffer reduce the electron occupancy f_D of deep hole centers (traps) in the buffer underlying the InAs quantum well. Buffer layer electrons transfer to the quantum well, and therefore enhance the quantum well conductivity at low V_{DS}: see Figure 4-11 (a). At higher V_{DS}, we postulate that the trapped holes get

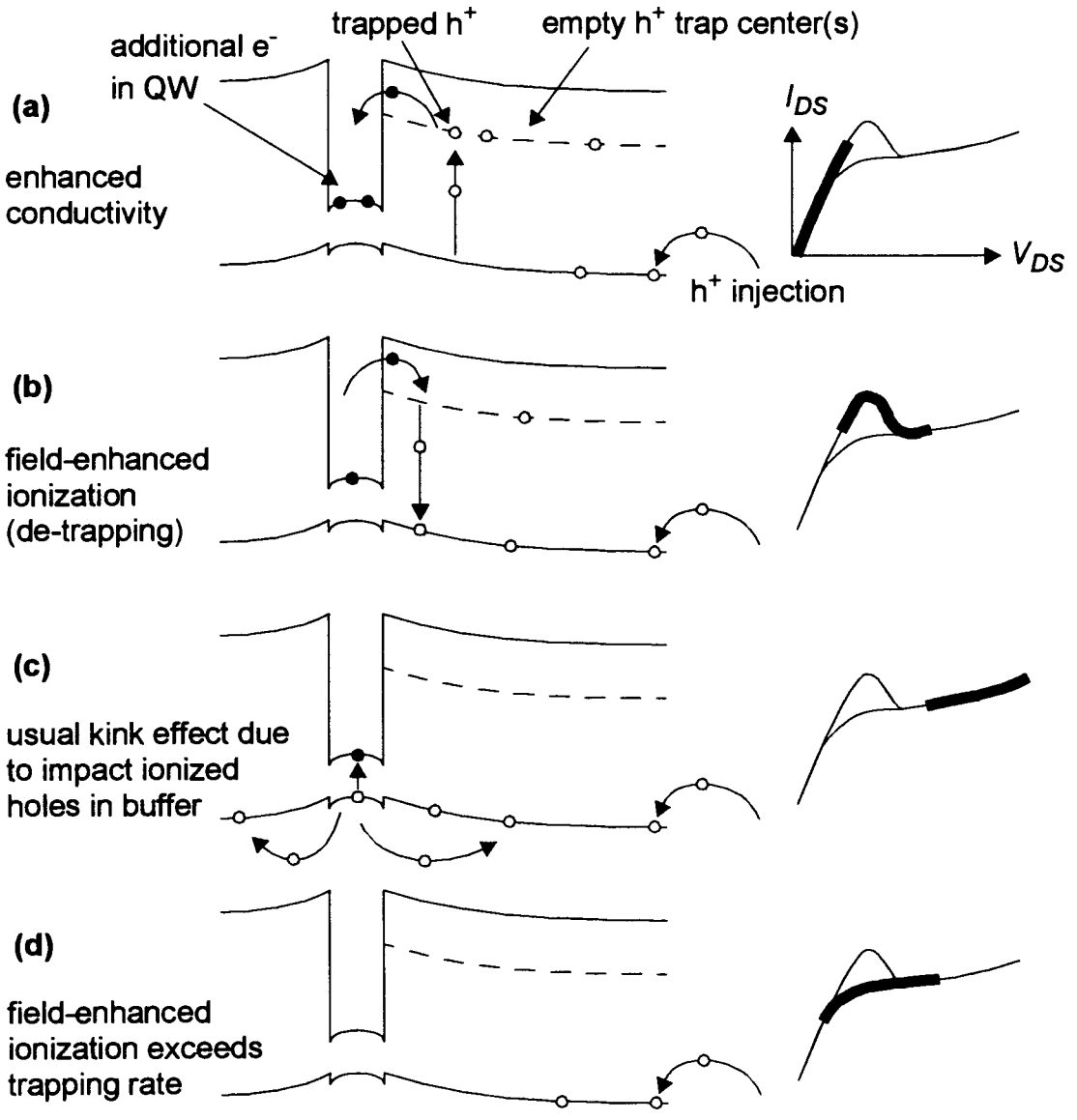

Figure 4-11 : Proposed mechanism for sidegating-induced negative differential resistance (SINDR) in InAs/AlSb HFETs: a) at low drain biases, hole traps are occupied by holes injected from the positively biased buffer, and so add electron charge $\Delta f_D N_T$ to QW; b) as the drain bias V_{DS} is increased, a net emission of holes takes place; c) at high drain biases, no holes remain trapped and a regular kink regime is entered; d) as the bias is lowered, no holes are trapped until below the SINDR hump. SRH statistics link the presence of trapped holes with an increased electron density, as long as the characteristic frequencies of the trapping process is high compared with the sweep frequency.

field-ionized, causing the quantum well conductivity to drop to its sidegating-free level and thus giving rise to the NDR features in the I-V characteristics: see Figure 4-11 (b) and (c). Field-dependent electron trapping and de-trapping times from deep centers has been shown by Canali *et al.* to vary by an order of magnitude with increasing drain bias in AlGaAs/GaAs HFETs [16]. The quantum well electron density contribution from deep centers can then be described as a function of time (and bias, implicitly) by [74]

$$N_s(t) = N_{[t=0]}(T)\exp\left(-\frac{t}{\tau(V_{DS})}\right) \qquad (4\text{–}4)$$

where τ is the characteristic hole emission time from the deep level, and where $N_{[t=0]}(T)$ is the initial contribution due to trapped holes and is determined by the sidegate bias and the ambient temperature. The application of an electric field (through V_{DS}) shortens the emission time τ, reducing the quantum well conductivity at higher drain biases.

The transient modulation of the quantum well conductivity arises because the presence of a non-equilibrium excess hole concentration Δp_e in the AlGaSb buffer must be accommodated either electrostatically and/or by a change in the occupation probability Δf_D of deep centers present in the buffer. The occupation probability f_D is given by the usual SRH relation given by equation (4-1). By charge conservation, $\Delta f_D N_T$ electrons (where N_T is the deep level volumetric density) are transferred to the InAs well, where they increase the channel conductivity at low drain biases.

On the drain bias "down" sweep, no NDR is observed because buffer layer deep levels have been emptied by the application of a high V_{DS} (and the resultant shortening of the deep level emission time), thus accounting for the hysteresis in the drain characteristics: see Figure 4-11 (d). The transient occupation of deep levels therefore explains both the NDR and the hysteresis in the drain I-V characteristics measured in the dark.

It is interesting to note that the magnitude of the sidegating-induced drain current enhancement ΔI_{DS} shown in Figure 4-3 on page 62 is indeed much larger than the

sidegate leakage current I_{SG}: the SINDR increase in drain current features a current gain $\Delta I_{DS}/I_{SG} \approx 2\,\text{mA}/[10 \rightarrow 100\,\text{nA}] = 20{,}000$ to $200{,}000$. In comparison, the ratio of electron mobility in the InAs quantum well (~ 20,000) to the hole mobility in the AlGaSb (~ 200-400) only comes up to a factor of 500 to 1000. Clearly, the magnitude of I_{SG} cannot account alone for the SINDR peak. As already pointed out by Kunihiro *et al.* [39], the positive charge associated with the deep centers can exceed Δp_e, to almost match N_T, under certain conditions determined by the quantity $(\partial f_D/\partial p)N_T$ if hole traps are present in the buffer layer. The present observation lends support to the "*static charge amplifier*" concept put forward by Kunihiro *et al.* in connection with the enhanced drain conductance (kink effect) arising from impact ionization holes present in the GaAs HFET buffer layers.

Based on the above considerations, the SINDR frequency dependence shown in Figure 4-6 on page 65 can be readily understood in terms of a transient occupation of buffer layer deep level centers by comparing the deep level carrier emission rate (determined by the energy separation between the deep level and the pertinent band edge) with the curve tracer sweep frequency. At intermediate frequencies, deep levels can change their charge state rapidly enough to follow the drain bias sweep and the quantum well conductivity is therefore modulated during any single sweep. As the frequency increases, statistically fewer deep level centers can respond to the drain bias sweep, and the width of the hysteresis in the I-V characteristics widens while the NDR peak-to-valley current ratio diminishes; at still higher sweep frequencies, the hysteresis and NDR completely disappear from the drain characteristics because the sweep time period becomes much smaller than the characteristic emission time for the trapped carriers in the buffer layers. For very slow drain bias sweeps, on the other hand, the bias sweep direction must become irrelevant because the quantum well and the buffer layer carrier concentrations must remain in a quasi-steady-state; this is seen in the higher temperature, very low frequency data of Figure 4-6. For quasi-static measurements one would expect SINDR to altogether disappear from the I-V characteristics because competing recombination pro-

cesses reduce the initial trap occupancy even at low drain biases. Figure 4-6 shows that indeed, SINDR tends to collapse for the lowest sweep frequency of $f = 0.5\,\mathrm{Hz}$.

With illumination, electron-hole pairs are continuously generated throughout the HFET structure. The mesa floor resistivity is reduced by the higher charge carrier concentration, and sidegating-induced hole injection rates into the buffer under the HFET structure are increased. Carrier generation in the active layers should be a comparatively negligible effect because of the small volume of those layers. The threshold at which holes are emitted from the traps is unchanged, and so the SINDR appears at approximately the same drain biases. At sweep frequencies near the trapping frequency, SINDR will still only appear in the up sweep direction. The high hole injection rate under illumination ensures that traps can be refilled (on the down sweep) fast enough to maintain NDR in *both* sweep directions. The maximum cutoff frequency could not be determined with the present experimental setup because of excessive capacitances. At very high illumination levels, the abundance of charge carriers renders the variation in trap occupancy due to trap emission at higher drain biases negligible, thus washing out the NDR features.

The fact that the peculiar "resonant-like" SINDR frequency dependence is fully accounted for by our interpretation of SINDR in terms of transient deep level population lends support to our qualitative model.

4.4 Conclusion

In conclusion, we have presented the first measurements of sidegating in InAs/AlSb HFETs grown by MBE on GaAs semi-insulating buffer layers. We found that the thick strain-relaxed AlGaSb/AlSb buffer layers provide adequate inter-device isolation for typical voltages encountered in low-power integrated circuits. Large positive sidegate voltages result in the appearance of pronounced sidegating-induced NDR (SINDR) at low drain biases (pre-kink voltages) that was investigated as a function of bias, frequency, and

temperature. It was found that SINDR can be understood in terms of the transient occupation of yet to be identified deep level center(s) in the HFET buffer layers. This effect is quite independent of the GaAs substrate: with the combination of thick (few μm) AlGaSb buffers, and a calculated valence band offset of E_v = -0.16eV at the strained AlSb/GaAs interface [75], holes should not penetrate the GaAs substrate. The present study reveals the importance of AlGaSb buffer layers in InAs/AlSb HFET technology and calls for a full characterization of deep levels in MBE-grown AlGaSb layers.

CHAPTER 5
Microwave Performance of InAs/AlSb HFETs

Overview

In this Chapter, we examine the importance of carrier mobility and impact ionization on the microwave performance of InAs/AlSb HFETs. We present the first study of the microwave performance dependence on quantum well width for InAs/AlSb HFETs. Since the narrower (50Å) quantum well devices are distinguished from the wider (100Å) quantum well devices by a diminished low-field mobility (as well as an increased effective bandgap due to quantization), we demonstrate that low-field mobility is important to the microwave performance of HFETs because it affects the effective electron velocity in the InAs channel. This is an important finding because there has been much debate on the relative importance of the peak electron velocity and the low-field mobility on the microwave performance of millimeter-wave HFETs.

Because the quantum well width affects the effective bandgap of the channel, we use the same samples to examine the effect of impact ionization on the microwave characteristics of InAs/AlSb HFETs. The effect of bias on measured scattering (S-) parameters is studied and we show that impact ionization rates in InAs/AlSb HFETs can affect the S-parameters to the extent that they become qualitatively different from S-parameters measured in conventional low impact-ionization devices such as GaAs MES-

FETs. The output reflection coefficient S_{22} in InAs/AlSb HFETs shows an *inductive* behavior below a critical frequency that increases with increasing impact ionization rates. At very high levels of impact ionization, the input reflection coefficient S_{11} is also affected: S_{11} is increasingly shunted by a parasitic gate leakage current that is not present in the conventional MESFET/HFET model (see Figure 5-12 on page 91). We show that the conventional small signal equivalent circuit commonly used to model the microwave frequency behavior of MESFETs/HFETs is inadequate at all frequencies when the rate of impact ionization is high. A new small signal equivalent circuit model that adequately describes impact ionization in GaInAs/AlInAs/InP HFETs [58] is applied to the measured S-parameters, and yields satisfactory results for the 50Å quantum well devices but completely fails to describe the effects of the higher impact ionization rates in the wider channel devices.

5.1 Microwave performance and InAs quantum well width

5.1.1 Introduction

In this Section, we present the first study of the microwave performance dependence on quantum well width for InAs/AlSb HFETs. We examine the differences between devices that are nominally identical except for the thickness of the InAs quantum well (see Figure 5-1). The epitaxial layers consist of a GaAs nucleation layer followed by a 2μm strain-relaxed AlSb buffer layer, and a 2000Å $Al_{0.8}Ga_{0.2}Sb$ etch stop layer that serves as the mesa floor in the device isolation. The active layers in the HFET structure are: an 80Å AlSb bottom barrier, a 100Å or 50Å InAs quantum well, and an 85Å or 55Å AlSb top barrier. These are followed by a 175Å $AlSb_{0.9}As_{0.1}$ digital alloy superlattice and a 30Å/12Å GaSb/InAs composite cap layer. The 100Å and 50Å InAs quantum wells show nearly identical electron sheet concentrations n_s but the narrow well has a much smaller low-field electron mobility μ: Hall measurements on the as-grown wafers revealed

12Å InAs cap layer
30Å GaSb cap layer
175Å $AlSb_{0.9}As_{0.1}$ barrier
55Å (85Å) AlSb top barrier
50Å (100 Å) InAs quantum well
80Å AlSb bottom barrier
2000Å $Al_{0.8}Ga_{0.2}Sb$ etch-stop layer
2μm AlSb buffer
GaAs nucleation layer
semi-insulating GaAs substrate

Figure 5-1 : Layer structure of 50Å and 100Å InAs quantum well HFETs used in this study.

$\mu = 9260\,cm^2/V{\cdot}s$ and $n_s = 1.7{\cdot}10^{12}\,cm^{-2}$ for the 50Å quantum well compared with $\mu = 20{,}720\,cm^2/V{\cdot}s$ and $n_s = 2.1{\cdot}10^{12}\,cm^{-2}$ for the 100Å quantum well. The fabrication sequence consisted of alloyed Ni/AuGe/Ni/Au Ohmic contacts, followed by a standard mesa etch, and a Ti/Au gate and pad metallization. A detailed process run sheet is given in the Appendix.

Since the narrower (50Å) quantum well devices are distinguished from the wider (100Å) quantum well devices by a much lower low-field mobility, we hereby demonstrate that low-field mobility is an important factor in the microwave performance of HFETs.

5.1.2 Microwave measurements

An HP 8510B Network Analyzer was used for microwave characterization of InAs/AlSb HFETs and GaAs MESFETs. The HP 8516A test set passes a small signal 0.045-40GHz electromagnetic wave through GGB 2.9mm 50Ω waveguides and GGB 40A Picoprobes to each terminal of the device under test (DUT) separately while the

other terminal is held matched to 50Ω, and the reflected and transmitted voltage waves for each terminal are measured. The input/output voltage ratios are expressed as scattering, or S-parameters. Calibration to move the source/measurement reference plane to the probe tips was performed using a GGB short-load-open-thru (SLOT) calibration chip. Analog power supplies were used to bias the FETs through the HP 8510B, and the measured data were transferred to an IBM compatible PC from the network analyzer via an HPIB bus.

From the measured S-parameters we calculate the current gain $|H_{21}|^2$ and the Maximum Available Gain (MAG) using the standard formulae (e.g. Vendelin [76]):

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \tag{5–1}$$

and

$$\mathrm{MAG} = \left|\frac{S_{21}}{S_{12}}\right|(k-\sqrt{k^2-1}) \tag{5–2}$$

where the stability factor k is defined as

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{21}S_{12}|^2}{2|S_{21}||S_{12}|}. \tag{5–3}$$

When k is less than unity, the MAG is undefined. The Maximum Stable Gain (MSG) is obtained instead by setting $k = 1$ so that $\mathrm{MSG} = |S_{21}/S_{12}|$. The frequency for unity current gain $|H_{21}|^2 = 0\,\mathrm{dB}$ is defined as f_T (the so-called unity current gain cutoff frequency), while the frequency for unity MAG = 0 dB is defined as f_{MAX} (maximum frequency of oscillation). Since actual cutoff frequencies often exceeded the highest measurement frequency of 40GHz, the standard extrapolation at -20dB/decade was used beyond 40GHz.

From on-wafer S-parameter measurements we directly obtain the *extrinsic* transistor parameters; the cutoff frequencies calculated from the measured S-parameters

include all parasitics (and thus include probe pad effects). The gate and drain contact pads slow device performance because their high parasitic capacitance C_{pad} shunts the input and output signals to ground, reducing the measured gain of the DUT. We can express the cutoff frequency $f_T = 1/2\pi\tau_{total}$ in terms of the sum of intrinsic τ_{int} and parasitic charging delays [55]:

$$\frac{1}{2\pi f_T} = \tau_{total} = \tau_{int} + \frac{C_{pad}}{g_m} \times \frac{1}{W} \tag{5–4}$$

where g_m is the measured device transconductance per unit transistor width and W is the device width. The intrinsic f_{MAX} is obtained similarly since $f_{MAX} \propto f_T$. The gate pad capacitance is directly extracted by measuring the input reflection coefficient S_{11} of a dummy device lacking a gate finger (see Figure 5-2). The relationship

$$S_{11} = \frac{1 - \omega^2 Z_0^2 C_{pad}^2}{1 + \omega^2 Z_0^2 C_{pad}^2} - j\frac{2\omega C_{pad}}{1 + \omega^2 Z_0^2 C_{pad}^2} \tag{5–5}$$

(where $Z_0 = 50\Omega$ is the characteristic impedance of the measurement system) yields a pad capacitance of $C_{pad} = 28$fF (ignoring the contribution from the drain pad capacitance). This is exactly the capacitance obtained by multiplying the area of the gate pad using empirical estimates of 10fF per $50\times50\,\mu m^2$ of gate pad [56]. The output reflection coefficient S_{22} for this test structure is difficult to interpret because the source and drain pads are in Ohmic contact via the conducting channel, enabling a series inductance and conductance to dominate the drain pad capacitance. For this reason the effect of the parasitic drain pad capacitance was not removed, keeping estimates of high-speed response conservative.

5.1.3 Results

The values for the maximum intrinsic cutoff frequencies f_T and f_{MAX} as a function of drain bias V_{DS} for each quantum well thickness are shown in Figure 5-3 for

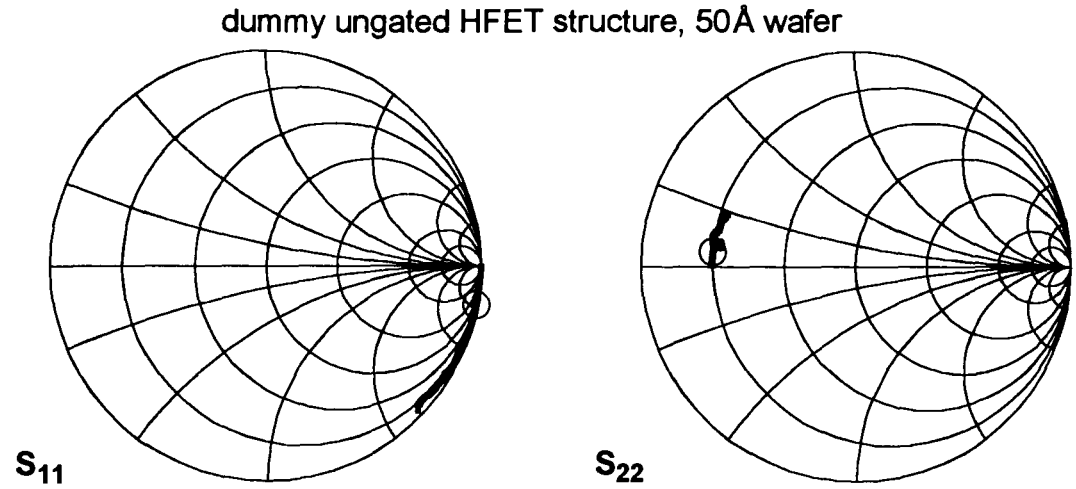

Figure 5-2 : S_{11} and S_{22} of dummy ungated HFET structure from 0-40GHz (smoothed data). S_{11} is capacitive (C_{pad} = 28fF) and S_{22} is inductive. Marker indicates 10GHz.

devices with measured gatelengths of $L = 0.7\,\mu m$ and $L = 0.6\,\mu m$ for the 50Å and 100Å quantum well devices respectively. The maximum cutoff frequencies are plotted with both V_{DS} and V_{GS} tuned for optimum performance in Figure 5-4. The unity current gain cutoff frequency-gatelength scaling products $f_T \cdot L$ (as shown in Figure 5-5) are approximately 40GHz·μm and 25GHz·μm for the 100Å and 50Å quantum well devices respectively. The cutoff frequencies saturate for 100Å devices around 0.8V, and for the 50Å devices around 1.0V-1.2V. The increased bias needed for saturation is consistent with the lower mobility and lower channel conductance in the 50Å quantum well devices.

5.1.4 Analysis

In this Section, we analyze the difference in cutoff frequencies between the 50Å and 100Å quantum well HFETs in terms of the difference in mobilities in the devices and the effect on device transconductance. The cutoff frequency is directly proportional (to first order) to the measured transconductance:

$$f_T = \frac{g_m}{2\pi C_G} \tag{5–6}$$

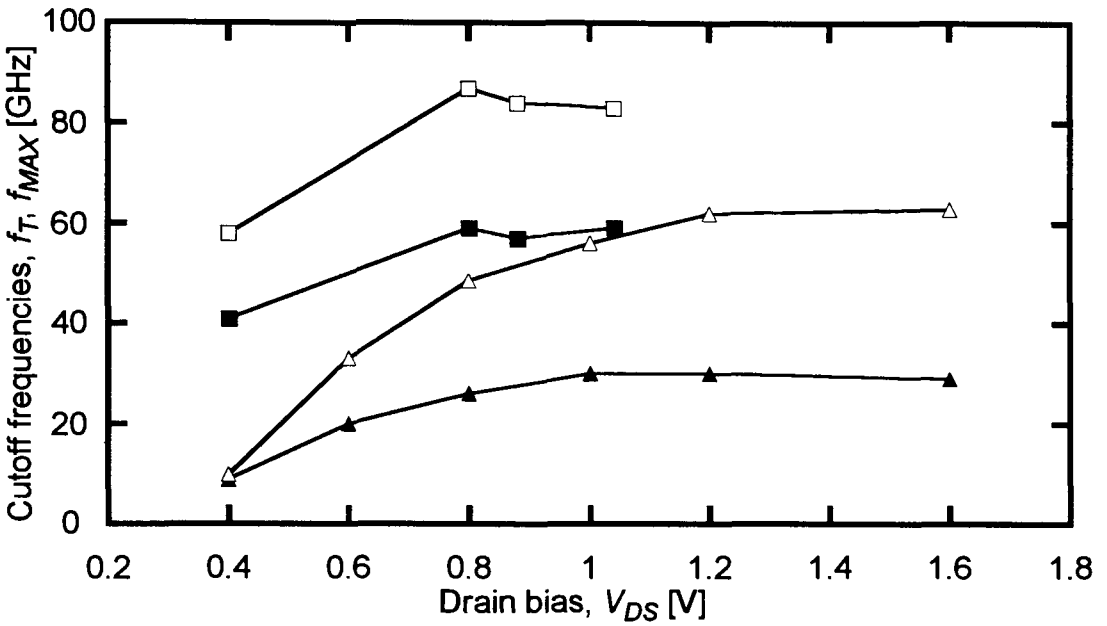

Figure 5-3 : Unity current gain and MAG intrinsic cutoff frequencies f_T (filled markers) and f_{MAX} (hollow markers) as a function of V_{DS}. Square markers: 100Å InAs quantum well, 0.6μm gatelength; triangular markers: 50Å InAs quantum well, 0.7μm gatelength. We see that the values for f_T are much higher for the 100Å devices but the ratios f_T/f_{MAX} are much greater for the 50Å devices.

For convenience we repeat the equation for transconductance involving modulation efficiency (1-13)

$$g_m = \frac{C_G v_{sat}}{L} \frac{1}{\sqrt{1 + (n_c/n_s)^2}} \tag{5–7}$$

where $n_c \equiv E_{sat} C_G / q$ and the gate capacitance is approximately $C_G = \varepsilon L/(d + \Delta d)$ where $d + \Delta d$ is the effective gate-to-channel separation and L is the gatelength. Following the work of Masselink [46], the reduction in electron mobility μ indirectly leads to a lower effective velocity v_{eff}. Masselink showed that if the mobility and the electron relaxation time are assumed approximately constant for electric fields below E_{sat}, the peak velocity v_{peak} is proportional to the square root of the low-field mobility $v_{peak} \propto \mu^{1/2}$ [46]. His experimental results showed this to be true for GaAs. According to this picture, the 9,260 $cm^2/V \cdot s$ mobility in the 50Å quantum well (compared to

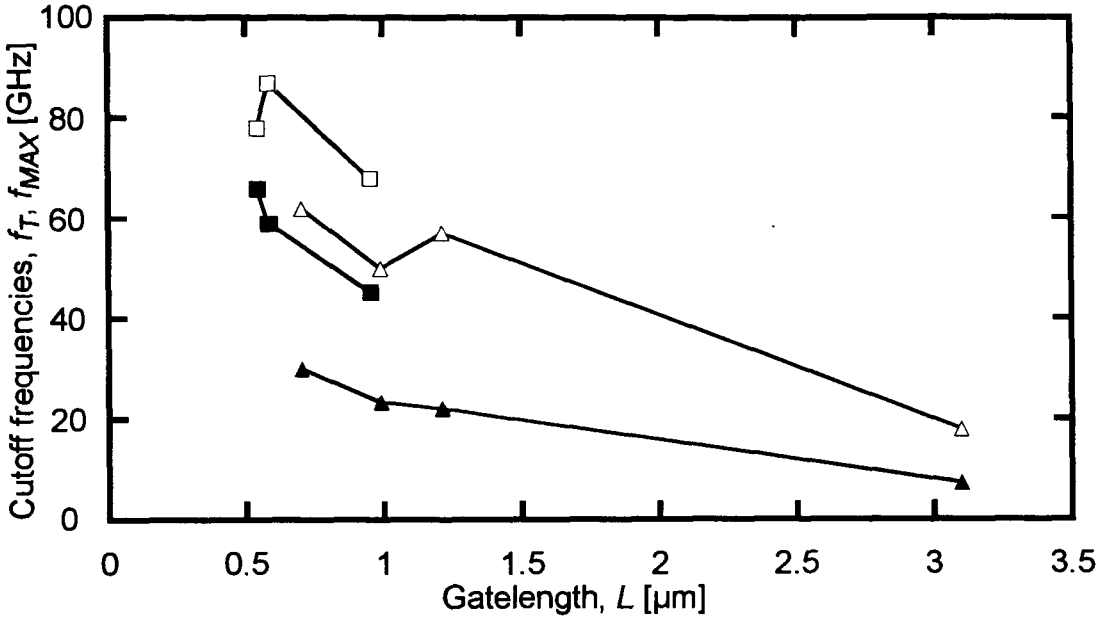

Figure 5-4 : Maximum f_T (filled markers) and f_{MAX} (hollow markers) as a function of gatelength for optimized V_{DS} and V_{GS}. Square markers: 100Å InAs quantum well, 0.6µm gatelength; triangular markers: 50Å InAs quantum well, 0.7µm gatelength.

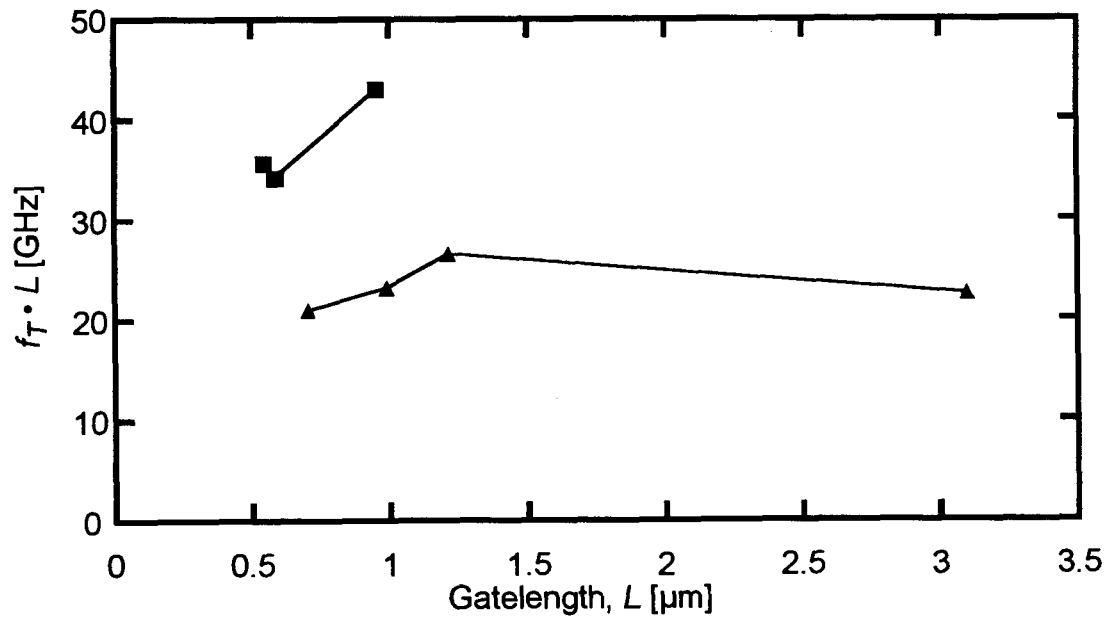

Figure 5-5 : Unity current gain cutoff frequency × gatelength product $f_T \cdot L$ as a function of gatelength. Solid square markers: 100Å InAs quantum well; solid triangular markers: 50Å InAs quantum well.

20,720cm^2/V·s in the 100Å quantum well) should reduce the 50Å well peak velocity to only 67% of the 100Å velocity. We assume values of: $v_{sat} = 3 \cdot 10^7$ cm/s for $\mu = 20{,}700 \text{cm}^2/\text{V} \cdot \text{s}$[1], $\varepsilon = 12\varepsilon_0$, and $d + \Delta d = 340$Å (310Å) for the 100Å (50Å) quantum well devices. Calculation results in the values tabulated below:

Table 5-1 : Calculated parameters for 50Å and 100Å quantum well HFETs for gatelengths of 0.7μm and 0.6μm. Measured parameters at $V_{DS} = 1.0V$.

	InAs well width [Å]	
Parameter	50	100
E_{sat} [10^3V/cm]	2.17	1.45
n_c [10^{11}cm^{-2}]	3.25	1.70
modulation efficiency	0.98	0.99
g_m (calculated,intrinsic) [mS/mm]	675	937
f_t (calculated,intrinsic) [GHz]	45	68
g_m (measured,extrinsic) [mS/mm]	560	800
f_t (measured,intrinsic) [GHz]	29	59

A typical ~5Ω source resistance reduces an intrinsic transconductance of 700-900mS/mm by approximately 20% to the measured transconductance values (see Section 2.4 on page 31). The calculated and measured transconductances therefore agree within the 10-20% uncertainty in measured transconductance caused by variations in gate-length and probing contact quality.

1. The choice of $v_{sat} = 3 \cdot 10^7$cm/s for the 100Å quantum well was taken from the bulk InAs peak saturated velocity of InAs $v_{sat} = 4 \cdot 10^7$cm/s at 77K [25], approximating v_{sat} at 300K by using quite arbitrarily the v_{sat} ratio between 77K and 300K of $v_{sat,300K}/v_{sat,77K} = 0.71$ for GaAs [64]. Before making any further attempts at modelling InAs devices, the actual electron velocity profile with electric field at room temperature in our InAs/AlSb channels must be determined. The geometric magnetoresistance (GMR) technique of Masselink *et al.* for ungated HFETs [45] will yield an effective carrier velocity when impact ionization generated carriers are present. The GMR technique can be implemented either on TLM microstrips or ungated HFETs, with measurements performed on modified Hall apparatus.

5.2 S-parameter frequency evolution with high rate of impact ionization

5.2.1 Introduction

In this Section, we intend to demonstrate that the behavior of InAs/AlSb HFETs is *qualitatively* different from that of standard FETs because of the high rates of impact ionization under normal operating conditions. We begin by examining the reflection S-parameters as a function of drain bias for 0.7 μm and 1.2 μm gatelength HFETs implemented with a 50 Å quantum well, by using the applied voltage to vary the impact ionization rate. With the dependence of microwave characteristics on impact ionization established, we then study the characteristics of 100 Å devices. Based on the evolution of S-parameters with increasing impact ionization established earlier, we conclude that the rate of impact ionization in the 100 Å devices is significantly higher than for the 50 Å devices, despite the similar magnitudes of impact ionization related effects at DC (see Section 3.2.2 on page 49). The higher rate of impact ionization is further demonstrated by a comparison of the frequency dispersion of extracted small-signal model parameters for devices with different quantum well widths. Finally, we contrast the microwave characteristics of InAs/AlSb HFETs with those of a standard GaAs MESFET fabricated by the author using the same mask. The textbook characteristics of the GaAs MESFET confirm that the non-ideal microwave frequency behavior of InAs/AlSb HFETs is not a consequence of device geometry or calibration error.

5.2.2 Drain bias dependence of reflection S-parameters for 50 Å quantum well devices

We show the input and output reflection S-parameters S_{11} and S_{22} of 50 Å quantum well HFETs with 0.7 μm and 1.2 μm gates as a function of drain bias, with the gate biased to V_{GS} = -0.7 V and -0.4 V, in Figure 5-8 and Figure 5-9. For low drain biases the output reflection coefficient S_{22} is nearly purely capacitive/conductive, but with

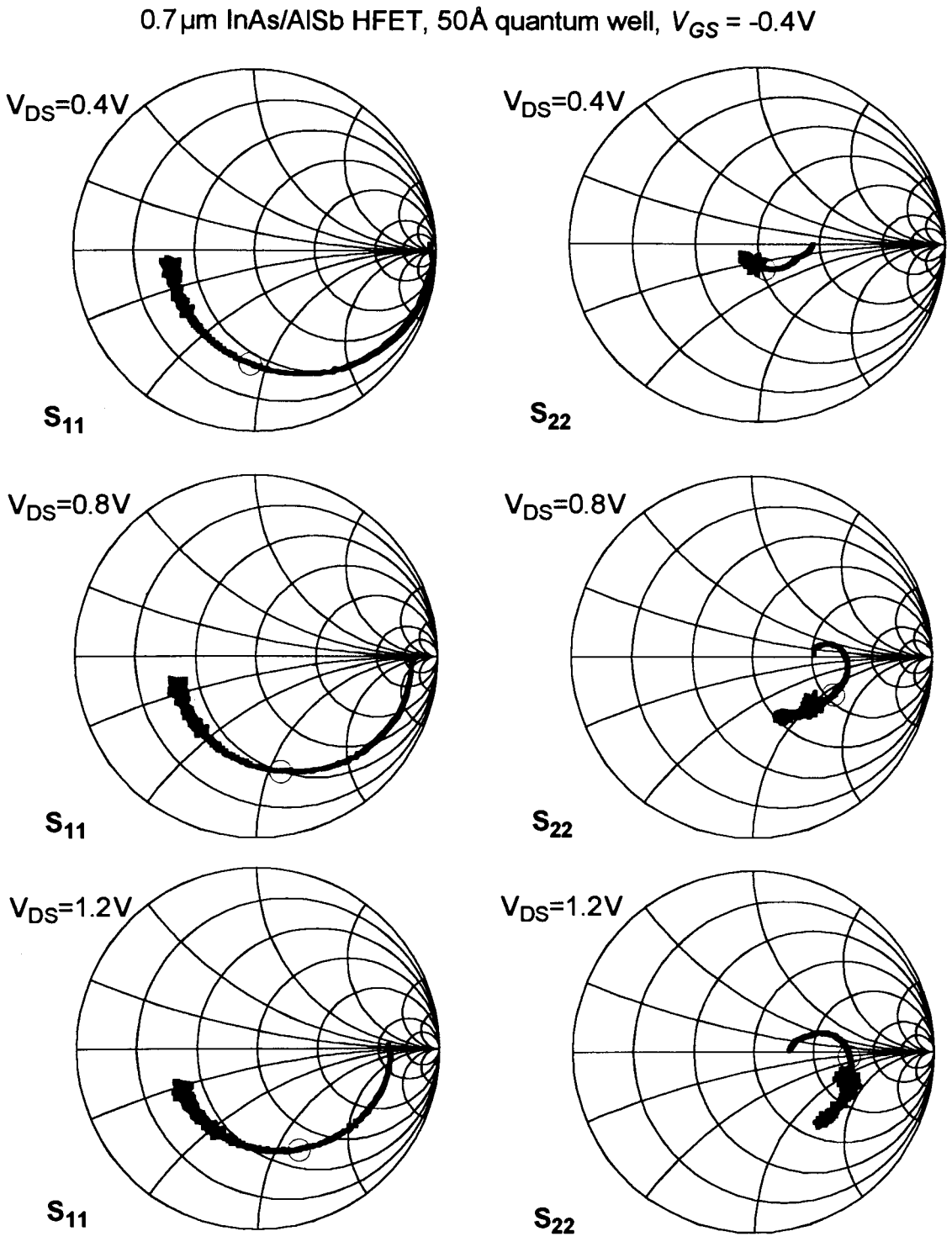

Figure 5-6 : S_{11} and S_{22} of 0.7µm HFET (50Å quantum well) at drain biases V_{DS} = 0.4V, 0.8V, 1.2V and gate bias of V_{GS} = -0.4V. Circular marker indicates 10GHz

1.2μm InAs/AlSb HFET, 50Å quantum well, V_{GS} = -0.4V

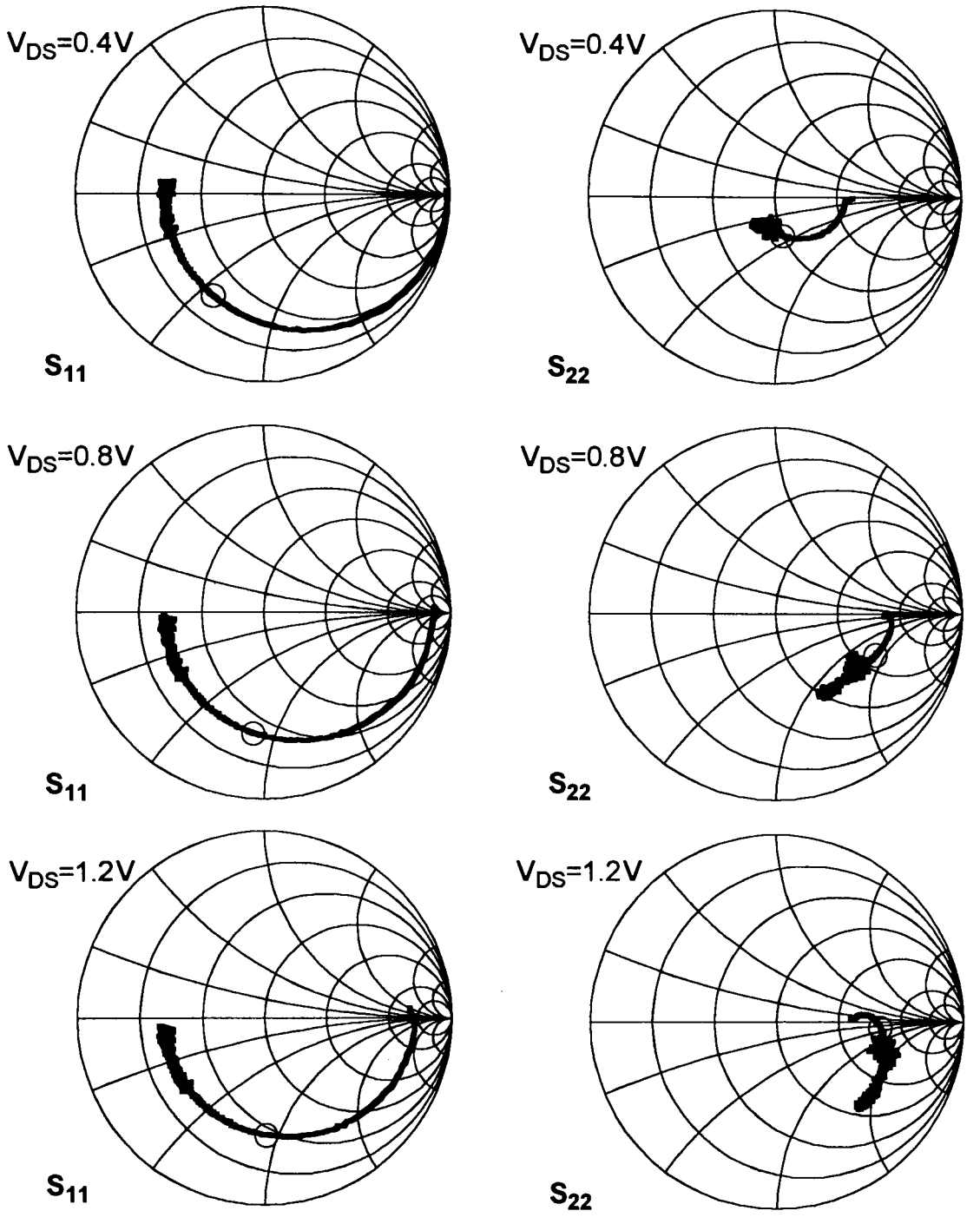

Figure 5-7: S_{11} and S_{22} of 1.2μm HFET (50Å quantum well) at drain biases V_{DS} = 0.4V, 0.8V, 1.2V, and gate bias of V_{GS} = -0.4V. Circular marker indicates 10GHz.

increasing drain bias there is inductive behavior at low frequencies. The inductive behavior with increasing impact ionization was previously reported by Kruppa *et al.* in InAs/AlSb HFETs [37]. The input reflection coefficient S_{11} behaves as a capacitor at low drain biases, but becomes increasingly conductive with increasing drain bias as a result of shunt conductances. To our knowledge such a behavior has never been reported.

5.2.3 S-parameters for 100Å quantum well device

The trends with increasing impact ionization established for the 50Å quantum well device are far more pronounced in 100Å quantum well devices. Figure 5-8 and

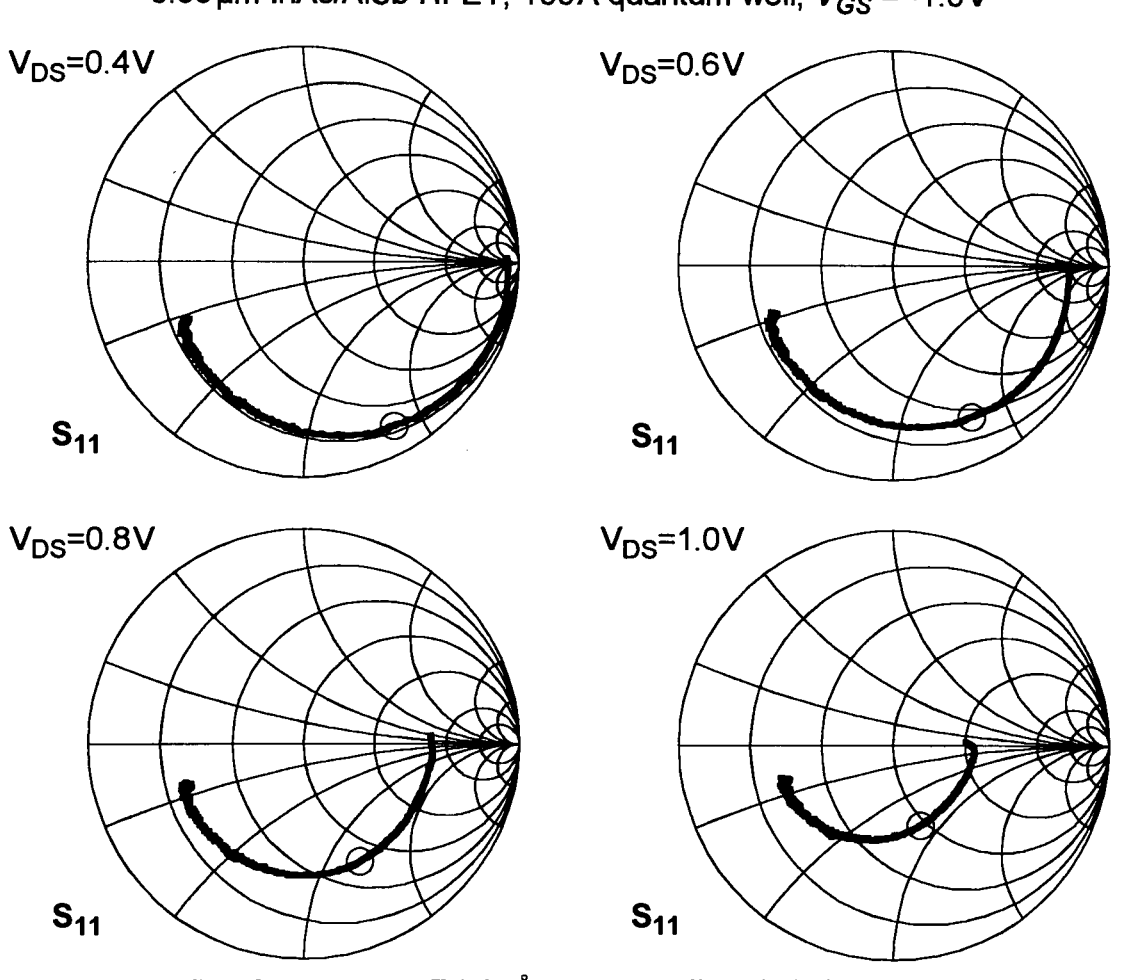

Figure 5-8 : S_{11} of 0.55μm HFET (100Å quantum well) at drain biases V_{DS} = 0.4V, 0.6V, 0.8V, 1.0V, and gate bias of V_{GS} = -1.0V. Circular marker indicates 10GHz

Figure 5-9 show the reflection parameters S_{11} and S_{22} for a 0.55μm device as a function of drain bias. The inductive behavior of S_{22} remains up to a remarkable 26GHz for a drain bias of V_{DS} = 1.0V. The unusual shift in S_{11} with increasing drain bias is far more prevalent than in the 50Å devices despite a very similar kink in the normalized DC characteristics. As we see more directly in the next Section, the gate shows mostly capacitive behavior at high frequencies but includes inductive behavior at low frequencies. Finally, we show the trends in the transmission parameters S_{12} and S_{21} with increasing drain bias in Figure 5-10 and Figure 5-11 on pages 89-90.

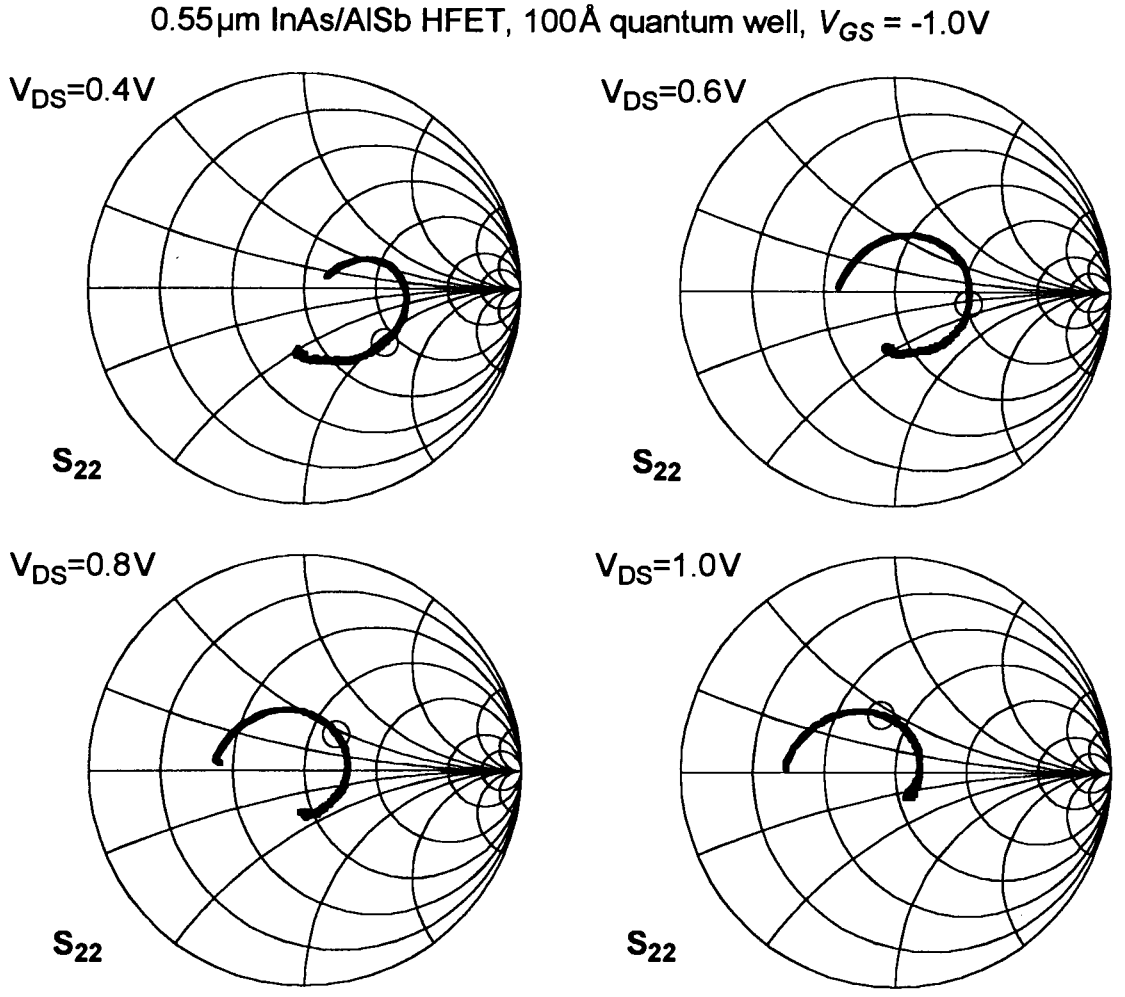

Figure 5-9 : S_{22} of 0.55μm HFET at drain biases of V_{DS} = 0.4V, 0.6V, 0.8V, 1.0V, and gate bias of V_{GS} = -1.0V. Circular marker indicates 10GHz.

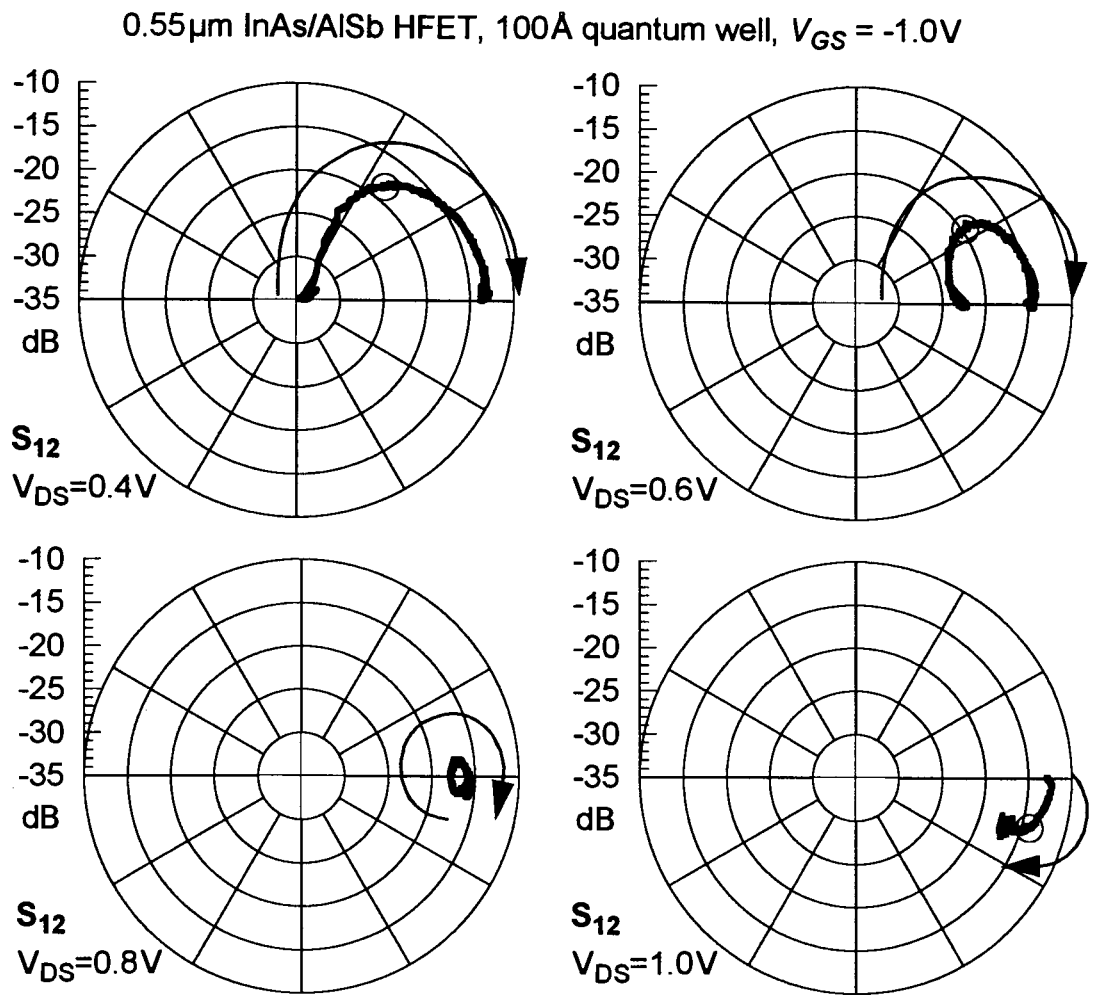

Figure 5-10 : S_{12} of 0.55μm HFET (100Å quantum well) at drain biases V_{DS} = 0.4V, 0.6V, 0.8V, 1.0V, and gate bias of V_{GS} = -1.0V. Circular marker indicates 10GHz. Arrow indicates direction of increasing frequency from 0 to 40GHz.

5.2.4 Dispersion of extracted small-signal equivalent circuit parameters

Although rigorous modelling of the microwave performance of InAs/AlSb HFETs is beyond the scope of this dissertation, we utilize the conventional intrinsic small-signal FET model to show that the simplified model performs increasingly poorly with increasing rates of impact ionization in InAs/AlSb HFETs. Several higher order models exist in the literature but they are not considered here because none account for impact ionization effects, with the recent exception of the work of Reuter *et al* [58]. We therefore

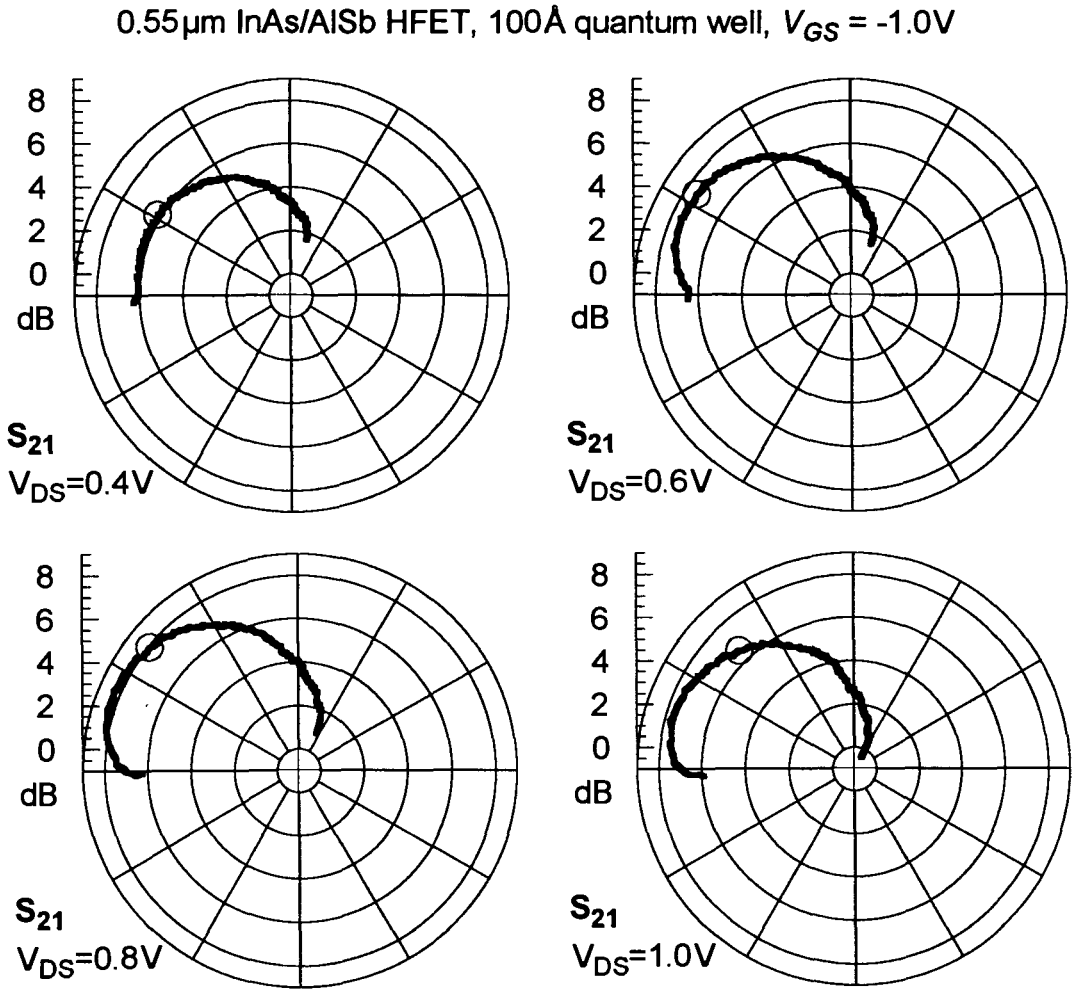

Figure 5-11 : S_{21} of 0.55μm HFET (100Å quantum well) at drain biases V_{DS} = 0.4V, 0.6V, 0.8V, 1.0V, and gate bias of V_{GS} = -1.0V. Circular marker indicates 10GHz.

use the simplified small-signal model (see Figure 5-12) because it has the advantage of leading to a unique analytical solution for each of the parameters. We then look at the trends that develop in the extracted parameters with changing frequency for different rates of impact ionization.

The Y-parameters are computed from the measured S-parameters, and each of the model parameters can be directly extracted using formulae given in [34] and [65]. The Y-parameters for the equivalent circuit are given by [65]:

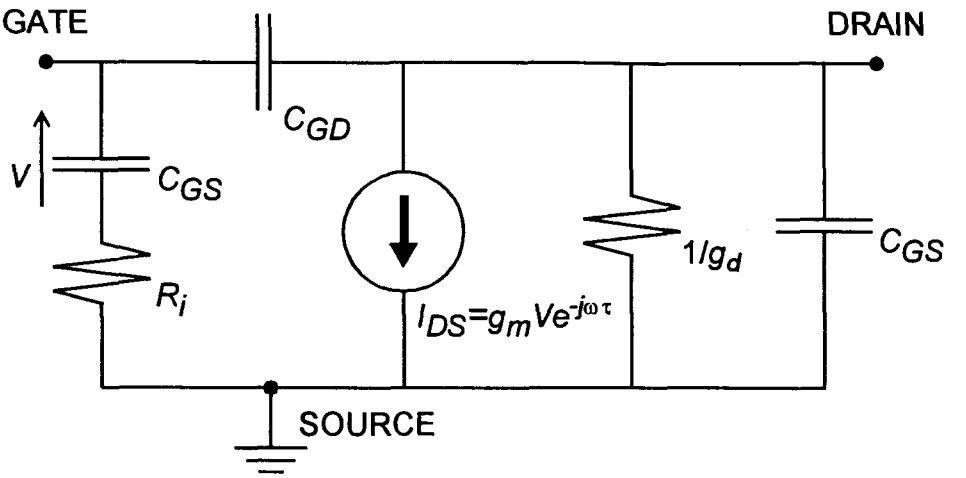

Figure 5-12 : Conventional simplified small-signal intrinsic equivalent circuit for MESFET/HFET.

$$
\begin{aligned}
Y_{11} &= \frac{R_i C_{GS}^2 \omega^2}{1+\omega^2 C_{GS}^2 R_i^2} + j\omega\left(\frac{C_{GS}}{1+\omega^2 C_{GS}^2 R_i^2} + C_{GD}\right) \\
Y_{12} &= -j\omega C_{GD} \\
Y_{21} &= \frac{g_m e^{-j\omega\tau}}{1+\omega C_{GS} R_i} - j\omega C_{GD} \\
Y_{22} &= g_d + j\omega(C_{DS} + C_{GD})
\end{aligned}
\qquad (5\text{–}8)
$$

where ω is the small signal frequency in rad/s, and all other quantities are parameters of the model shown in Figure 5-12. The above model neglects intrinsic non-idealities (such as gate leakage and impact ionization) as well as external parasitics (such as probe and pad capacitances and inductances, and contact resistance). To verify the validity of the above conventional FET model, the parameters in the simplified model were first extracted for a standard ~0.7 µm GaAs MESFET fabricated by the author using the same mask set as for InAs/AlSb HFET fabrication. Because the extracted model elements are nearly frequency independent for $f < 10$ GHz (see Figure 5-13), the external parasitics can safely be neglected as causes of low-frequency dispersion in measured data.[1] For higher frequencies $f > 20$ GHz, the error due to parasitics cannot be ignored: in Figure 5-17 on page 99, we

show dispersion curves for a simulated HFET (see Section 5.2.5 on page 95) including all external parasitic elements, as well as the dispersion curves for the same HFET but with all (parasitic) inductances set to zero. The plots show that parasitic inductances cannot be neglected at sufficiently high frequencies.

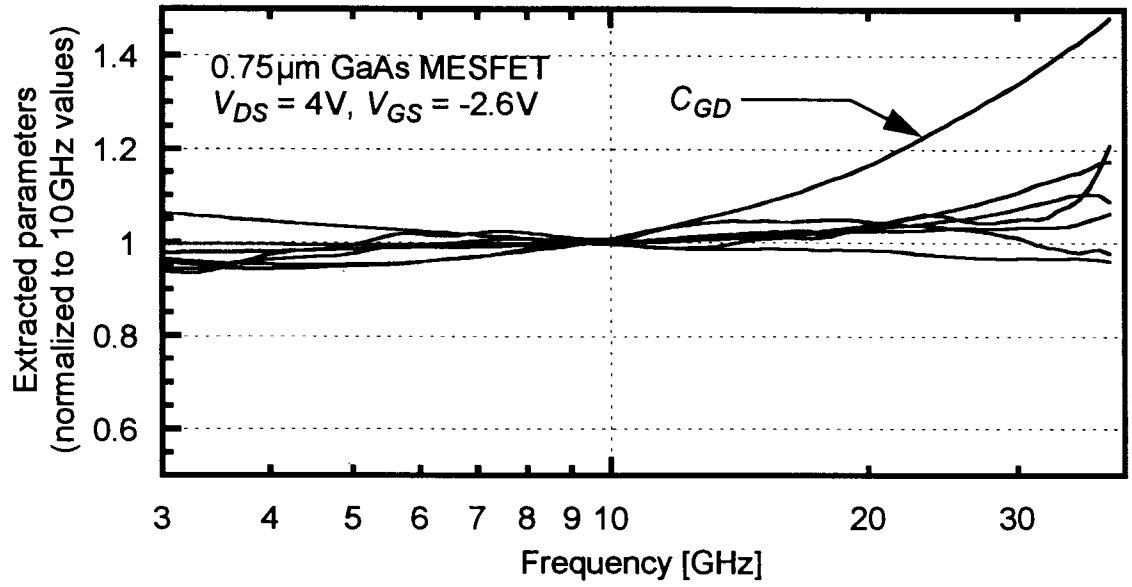

Figure 5-13 : Extracted conventional intrinsic small-signal model parameters for ~0.75µm GaAs MESFET with drain bias V_{DS} = 4V and gate bias V_{GS} = -2.6V. For clarity of presentation, normalization is performed to values at 9.65GHz and smoothing follows. There are very low levels of dispersion up to 10GHz for all parameters. (Low frequency dispersion is related to measurement noise.) The exceptionally large relative error in C_{GD} corresponds to a ~5fF absolute error compared with the >100fF total device capacitance.

The dispersion curve of the transconductance and output conductance (Figure 5-14) and of gate capacitances (Figure 5-15) are plotted for a L = 1.2µm gate-length HFET (50Å quantum well) with drain and gate biases of V_{DS} = 0.4V and V_{GS} = -0.4V; L = 0.7µm (50Å quantum well), V_{DS} = 0.8V and V_{GS} = -0.6V; and L = 0.6µm (100Å quantum well), V_{DS} = 0.8V and V_{GS} = -0.6V. The long gatelength of

1. The noisy behavior for the MESFET measurement is due to excessively high frequency sweep rates combined with a large (0.8GHz) frequency spacing between data points. The first few data points at low frequencies are unusable and therefore not shown < 3GHz. The HFET measurements share the same problem but at frequencies < 500MHz because of the 0.2GHz frequency spacing.

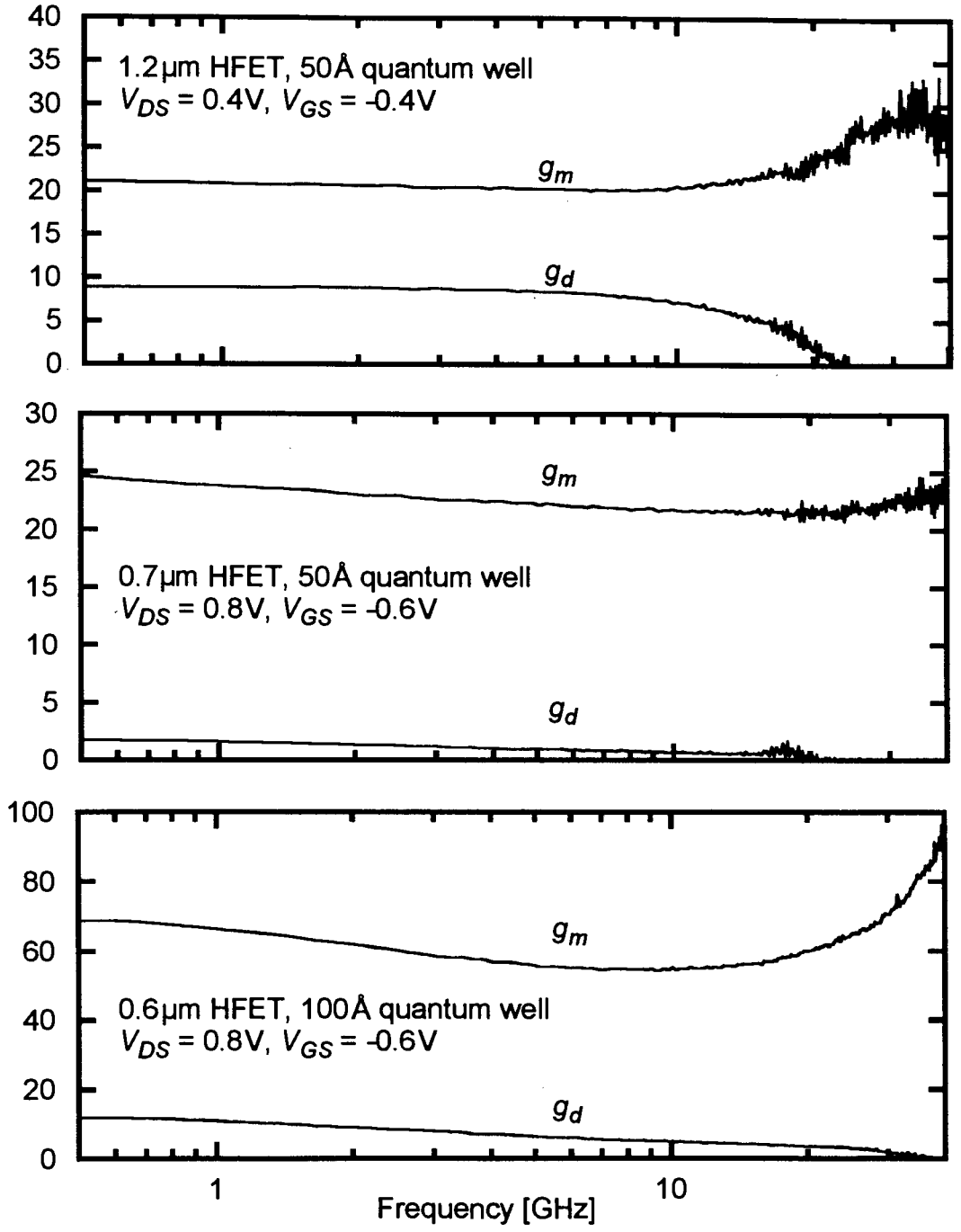

Figure 5-14 : Dispersion curves of extracted transconductance g_m and output conductance g_d for HFETS with following parameters, from top to bottom: gatelength L = 1.2µm, 0.7µm, 0.6µm; quantum well width 50Å, 50Å, 100Å; drain bias V_{DS} = 0.4V, 0.8V, 0.8V; drain bias V_{GS} = -0.4V, -0.6V, -0.6V. Units are in mS. Note the ideal dispersion in top panel below 10GHz.

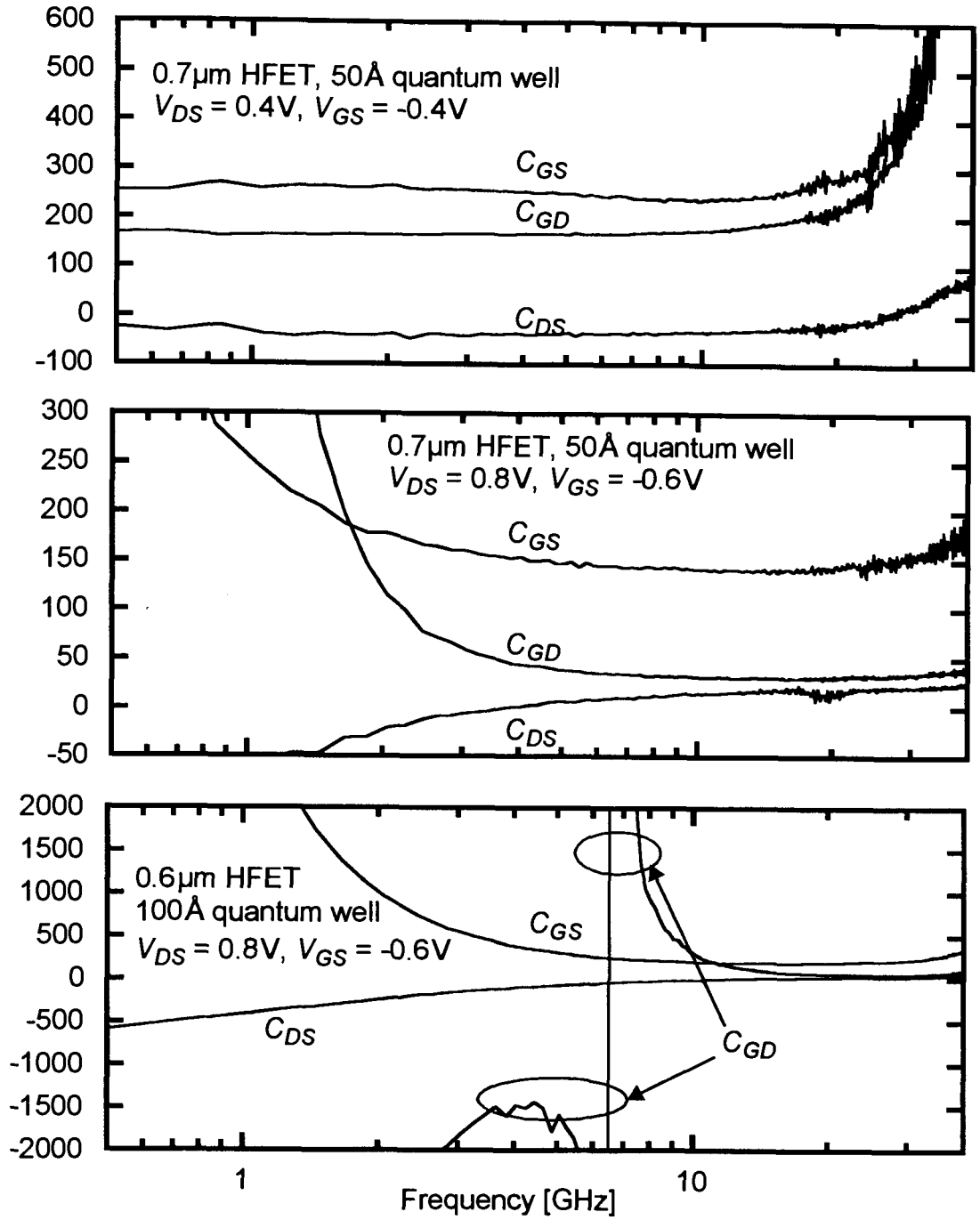

Figure 5-15 : Dispersion curves of extracted capacitances C_{GS}, C_{GD} and C_{DS} for HFETS with following parameters, from top to bottom: gatelength L = 1.2µm, 0.7µm, 0.6µm; quantum well width 50Å, 50Å, 100Å; drain bias V_{DS} = 0.4V, 0.8V, 0.8V; drain bias V_{GS} = -0.4V, -0.6V, -0.6V. Units are in fF.

1.2 µm and the low gate-drain voltage difference $V_{DG} = 0.8\,V$ together result in impact ionization-free characteristics for the 50 Å quantum well: the dispersion of the extracted parameter values is comparable to that obtained for the GaAs MESFET. Dispersion resulting from increasing impact ionization in the otherwise identical ~0.65 µm 50 Å and 100 Å quantum well HFETs is also shown in Figure 5-14 and Figure 5-15. Further discussion follows below.

5.2.5 Analysis and modelling

Impact ionization may affect microwave measurements because additional space charges are generated on different time scales: a space charge results from the application of a DC bias; and an RF space charge is generated at the microwave signal frequency. The total space charge includes DC and RF components of the positive hole feedback that causes the kink effect in InAs/AlSb HFETs. The low hole mobility should cause a time delay before the positive feedback due to the RF generated holes can affect the current flowing through the channel by the parasitic bipolar effect: we thus expect that the impact ionization will result in a frequency dispersion in the equivalent circuit parameters in the HFET model. The space charge associated with impact ionization electron products near the drain end of the gate should operate to higher frequencies, because impact ionization occurs on short time scales.

Turning to the dispersion of the extracted small signal model parameters, we first note the near-ideal behavior of the 50 Å, low $V_{DG} = 0.8\,V$ bias trace (top panels of Figure 5-14 and Figure 5-15). The total absence of low-frequency dispersion at low biases contrasted with the significant dispersion at higher biases unambiguously correlates the low-frequency dispersion with the hole space charge due to impact ionization. In the same Figures, the bottom two panels compare the parameter dispersion of otherwise identical 100 Å and 50 Å quantum well HFETs under the same bias conditions. The 100 Å device shows a much stronger low frequency dispersion, pointing to a higher rate of impact ion-

ization. (The discontinuity in C_{GD} follows from the inappropriate assumption that there is no gate leakage conductance at microwave frequencies — an assumption that worsens for wider InAs wells: see the plots of S_{12} for another device in Figure 5-10 on page 89.) This contrasts with the comparison between DC characteristics of otherwise identical devices (Figure 3-12 on page 54): at DC, we measured similar gate hole leakage currents which would suggest that impact ionization rates are not so different in the 50Å and 100Å InAs wells, in apparent disagreement with the microwave measurements. We also saw in Figure 3-11 on page 53 that when the output current is scaled to account for the lower channel conductance of the 50Å device, the kink and the output conductance g_d become nearly identical. Despite much lower rates of impact ionization (as determined by microwave measurements) the kink remains present in the DC characteristics. These observations suggest that even with a low impact ionization rate, the accumulation of holes in the buffer/barrier layers is sufficient to cause a kink measurable at low frequencies. To remove the kink, the rate of impact ionization must be reduced by orders of magnitude; or the hole feedback mechanism must be eliminated by the removal of holes with back-gate or dual-gate techniques, or by the introduction of fast recombination centers such as in LT-grown buffer layers [14]. These results explain the success of dual-gate HFETs and the failure of narrower quantum wells in reducing the kink, as reported in Chapter 3.

The evolution of the S-parameters with increasing rates of impact ionization underscores the non-ideal behavior of InAs/AlSb HFETs, and is not accounted for by standard FET models. Two groups have reported models that attempt to account for impact ionization effects in HFETs. Kruppa *et al.*, who were also working on InAs/AlSb HFETs, argued that since impact ionization results in carrier generation following application of a bias (that is, the current lags the voltage by a given phase factor) a shunt drain inductor effectively models the process [37]. Reuter *et al.*, however, criticized Kruppa's approach as being unphysical because it represented impact ionization by a parameter independent of the small-signal gate-drain bias v_{DG}. On the basis of their DC measure-

ments of impact ionization, Reuter *et al.* have determined that the generation of electron-hole pairs should be represented by a v_{DG} -controlled current source. They then added the frequency dependence phenomenologically using an RC circuit [58]. One suspects that either approach is dubious because Kruppa *et al.* apparently neglect carriers generated by the v_{DG} small signal, whereas Reuter *et al.* do not include the effects of the impact ionization generated hole feedback on the channel current (although for GaInAs/AlInAs/InP HFETs this may be a reasonable assumption because of hole confinement to the channel). The approach of Reuter *et al.* adequately (error < 1 dB) models the behavior of InAs/AlSb HFETs under low impact ionization conditions (see Figure 5-16) but under high impact ionization conditions, their model performs poorly.[1] Because their model uses *21 parameters* to describe 4 fairly well-behaved vector functions in the complex plane, one is not too shocked that a reasonable numerical fit is achievable. Because the model is so heavily parametrized, the obtained parameter values have little physical meaning, however.

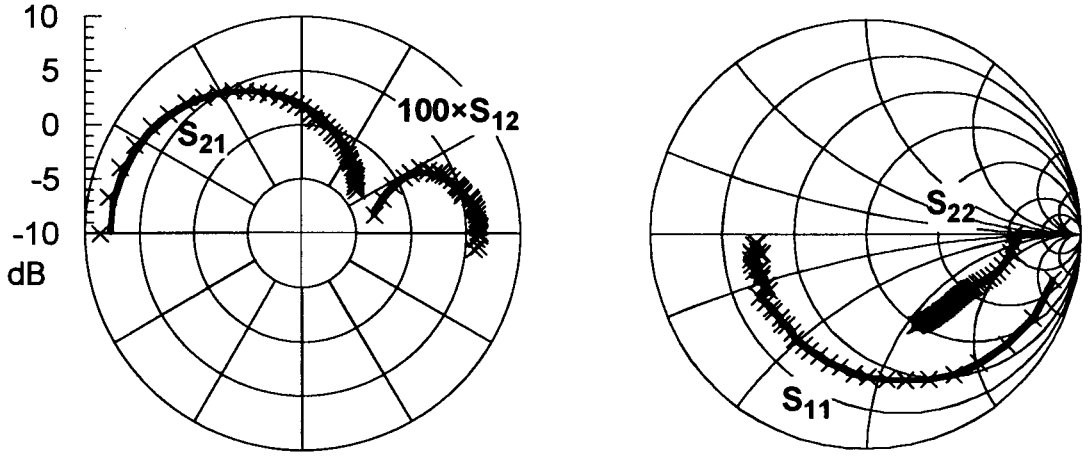

Figure 5-16 : Least squares fit using model of Reuter et al. to measured S-parameter data for 1.2 µm gate HFET at a drain bias of V_{DS} = 0.8 V and gate bias of V_{GS} = -0.4 V (50 Å quantum well). Lines: model predictions; markers: data. Frequencies from 0-40 GHz, spacing of 1 GHz.

1. Since only a standard "simplex" technique was available to minimize an error function representing the sum of the normalized errors for each of four S-parameters, one cannot discount the possibility that a more advanced optimization technique may find the proper fit (e.g. evolution theory and genetic algorithms used by Reuter *et al.*; see refs. 16-18 in [58]).

We emphasize that even the apparently good fit in Figure 5-16 still poses problems: the obtained parameters are unphysical (e.g. g_m = 59mS compared with DC value of ~33mS); and when the fits to S_{11} and S_{22} are examined more closely, they match well quantitatively (relative error) but poorly qualitatively (systematic error). The poor fit at low frequencies is consistent with the absence of a feedback term on the gate. To verify that the model of Reuter *et al.* describes qualitatively different results than those measured for InAs/AlSb HFETs, we generated the Y-parameters from the element values published by Reuter *et al.* for a 0.7µm GaInAs/AlInAs/InP HFET, and re-extracted the conventional intrinsic model element parameters as previously done for the InAs/AlSb devices (see Figure 5-17). The relatively minor (and certainly *qualitatively* different) dispersion seen for GaInAs/AlInAs/InP HFETs compared to InAs/AlSb HFETs (see Figure 5-14 on page 93 and Figure 5-15 on page 94) confirms that the model of Reuter *et al.* does not adequately describe high levels of impact ionization in InAs/AlSb HFETs. A model that better accounts for the impact ionization generated hole space charge in addition to impact ionization at the small signal frequency remains to be derived.

5.3 Current gain roll-off with frequency for InAs/AlSb HFETs

In the conventional small signal equivalent circuit model, the current gain $|H_{21}|^2$ and maximum available gain MAG ideally roll off with a single time constant -20dB/decade slope. Standard GaAs MESFETs (Figure 5-18) and 0.7µm GaInAs/AlInAs/InP HFETs [58] (Figure 5-19) certainly approach this ideal behavior. At high frequencies and when the gain H_{21} is low, parasitic inductances enhance the extrinsic gain, reducing the ideal -20dB/decade roll-off slope. The MSG/MAG are shown for information purposes only: we may note, however, that the voltage gain MSG in the MESFET is low mainly because of relatively high-resistance Ohmic contacts.

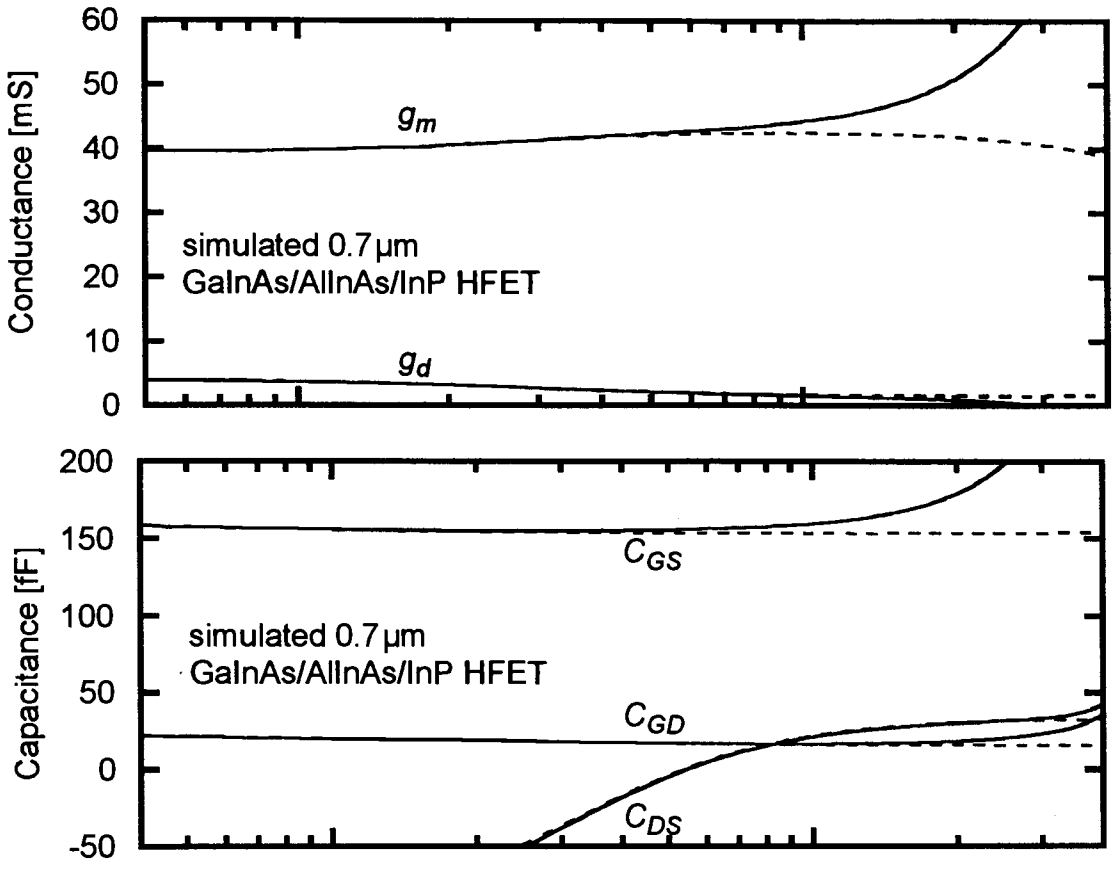

Figure 5-17: Dispersion curves calculated from fit parameters published for 0.7µm GaInAs/AlInAs/InP HFET in [58]. Solid lines represent the full model, while dashed lines have all parasitic inductances set to zero. The full dispersion curves resemble the dispersion curves of the V_{DS} = 0.4V, V_{GS} = -0.4V 1.2µm InAs/AlSb HFET, i.e. the measurement showing the least dispersion because of the low rate of impact ionization. Dispersion of C_{DS} at low frequencies is mostly due to the leakage conductance term.

In contrast, InAs/AlSb HFETs do *not* exhibit a -20dB/decade roll-off: the peak current gains for both 1.2µm, 50Å quantum well (Figure 5-20 on page 101) and 0.55µm, 100Å quantum well (Figure 5-21 on page 102) HFETs show reduced current gain roll-off. The roll-off is approximately -18GHz/decade from 2 to 18GHz for the 50Å device, and -16dB/decade from 4 to 40GHz for the 100Å device. There is a clear trend: with increasing impact ionization, the gain roll-off with frequency decreases. At very low

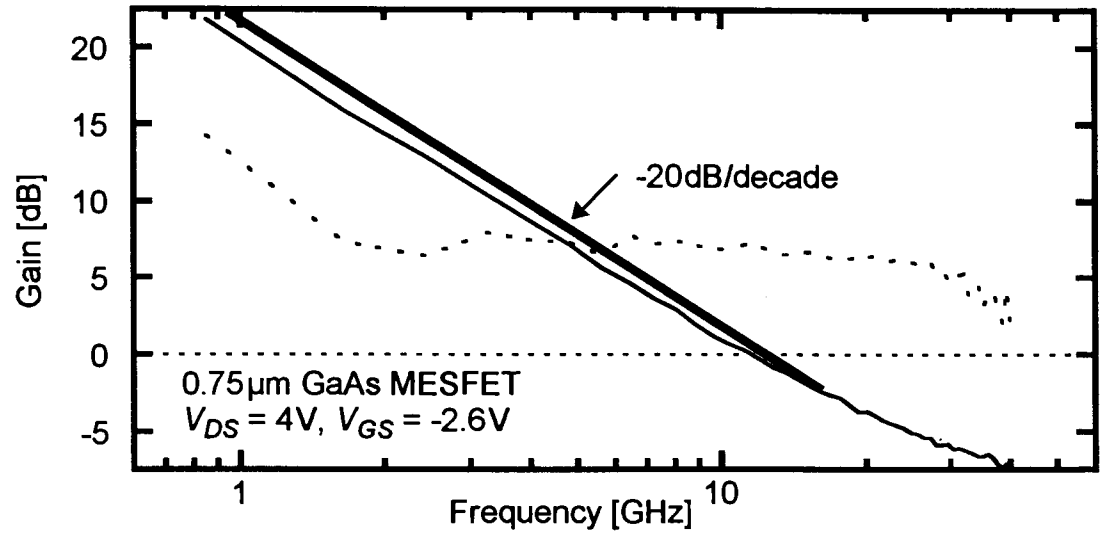

Figure 5-18 : Microwave performance for ~0.75μm GaAs MESFET: V_{GS} = -2V, V_{DS} = 4V. Solid line: $|H_{21}|^2$; dotted line: MSG/MAG. A near -20dB/decade roll-off appears down to near 0dB until parasitics dominate gain. Unsmoothed measured data shown.

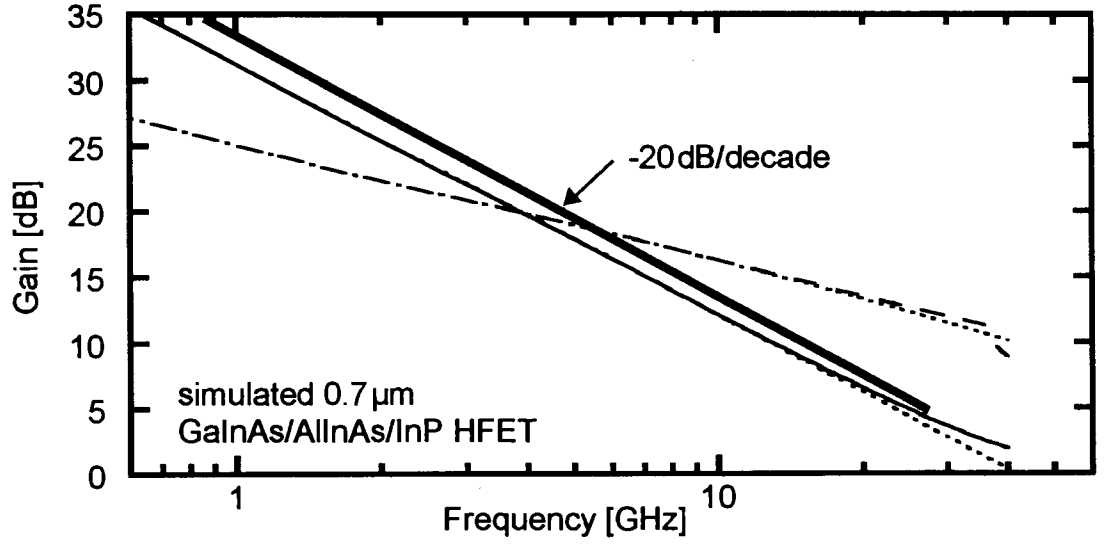

Figure 5-19 : Microwave performance of 0.7μm GaInAs/AlInAs/InP HFET calculated from parameters given in [58]. Solid line: $|H_{21}|^2$ including all parasitics; dashed line: MSG/MAG; dotted lines: gains with all inductances set to zero. The -20dB/decade rolloff dominates until high frequencies, where parasitic inductances reduce the roll-off.

frequencies (< 2GHz) the current gain saturates due to gate leakage; this further reduces the low-frequency roll-off.

A -20dB/decade roll-off of the gain is based on the assumption that the transistor can be modelled by circuit elements that have values *independent of frequency*. This is clearly not the case for InAs/AlSb HFETs when the conventional small signal equivalent circuit is used. On purely physical grounds, one expects that the conventional approach must fail if impact ionization is significant, because impact ionization has some characteristic time constant(s) and therefore any effect related to impact ionization is not independent of frequency. A small signal equivalent circuit may *approximate* impact ionization (as was shown by Kruppa *et al.* [37] and Reuter *et al.* [58]) using capacitors and inductors to incorporate phenomenologically the frequency dependence to first order. But combinations of standard reactive elements will not easily reproduce a roll-off other than a multiple of -20dB/decade. Of most importance, however, is that the experimental data demonstrates that the -16dB/decade roll-off observed is *intrinsic* to the device and so extrapolation from low frequencies at -20dB/decade is not necessarily justified.

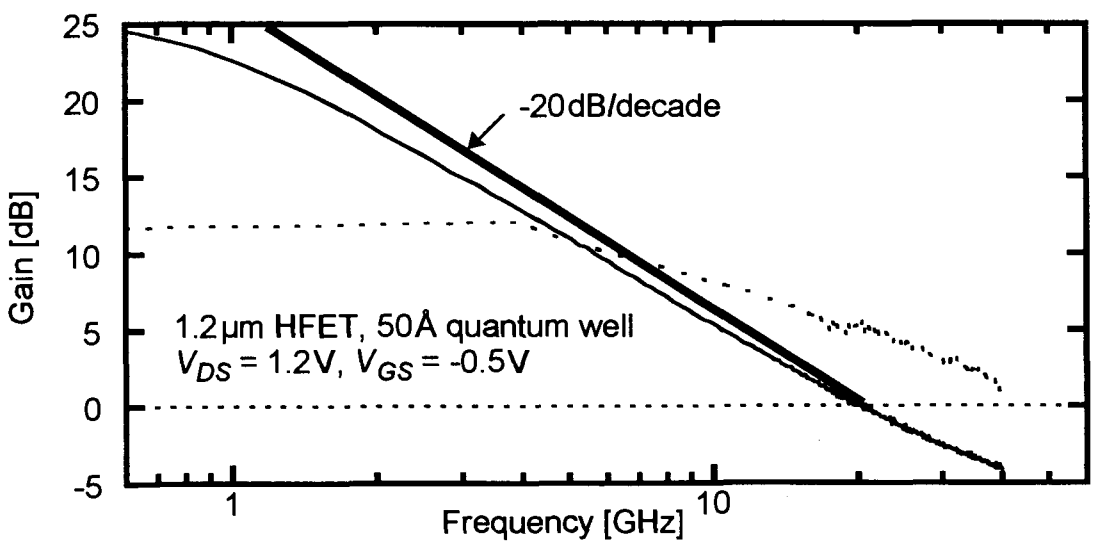

Figure 5-20: Peak microwave performance of 1.2µm gatelength (50Å quantum well) InAs/AlSb HFET. V_{GS} = -0.5V, V_{DS} = 1.2V. Solid line: $\|H_{21}\|^2$; dotted line: MSG/MAG. A -18dB/decade roll-off from about 2 to 18GHz dominates below the extrinsic f_T = 20GHz (f_{MAX} = 45GHz). Unsmoothed measured data shown.

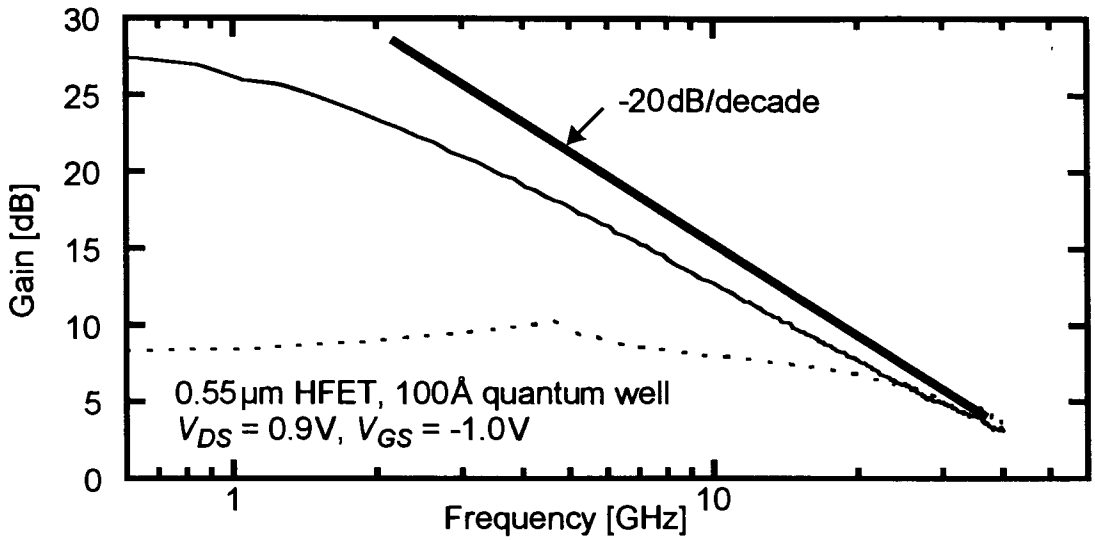

Figure 5-21 : Peak microwave performance of 0.55µm (100Å quantum well) InAs/AlSb HFET. V_{GS} = -1.0V, V_{DS} = 0.9V. Solid line: $\|H_{21}\|^2$; dotted line: MSG/MAG. A -16dB/decade rolloff from about 4 to 40GHz dominates, with no apparent conventional inductive effects on the current gain to 40GHz. Measured f_T = 56GHz, f_{MAX} = 58GHz, intrinsic f_T ~ 67GHz. Unsmoothed measured data shown.

CHAPTER 6
Summary and Conclusions

Overview

InAs/AlSb HFETs have much potential for high-speed low-power applications but have also shown a great sensitivity to short-channel effects. The present dissertation has been concerned with furthering the understanding of InAs/AlSb HFETs —and has particularly focused on the effects of the high rates of impact ionization in the narrow band gap InAs channels. The high output conductance and kink effect present in DC measurements were explained by an impact ionization generated hole feedback effect that can be likened to a parasitic bipolar transistor effect that may be amplified by the presence of traps in buffer layers (static charge amplification). Two techniques for controlling the rate of impact ionization and the location of generated holes were studied: dual gate HFETs and the use of quantum confinement in narrow quantum well HFETs to increase the ionization threshold. Injection of holes by a sidegating electrode at high positive bias was used to study the effect of the buffer layers on device performance: a new sidegating-induced negative differential resistance (SINDR) in InAs/AlSb HFETs was discovered and explained in terms of the transient trapping and field-emission of holes in the buffer layers. Finally, the microwave performance of InAs/AlSb HFETs as a function of quantum well thickness (and hence mobility) and the influence of impact ionization on measured S-parameters were examined. In the course of this dissertation, the exceptional

microwave performance of these HFETs was demonstrated with the fabrication of InAs/AlSb HFETs with gatelengths of ~0.55 μm with intrinsic current gain cutoff frequencies f_T up to 67 GHz. We believe that these are some of the fastest devices made for that gatelength — they are the fastest FETs ever made in Canada.

In this concluding Chapter, we first briefly review the key research findings of this dissertation. In doing this, we raise new questions that must be resolved, and these form the basis for future work on InAs/AlSb HFETs.

6.1 Summary of research findings

6.1.1 Control of the kink effect: dual gate HFETs and quantum well engineering

The problem of impact ionization and the resulting kink in the DC output characteristics of InAs/AlSb HFETs was examined in Chapter 3. Impact ionization generated holes form a positive space charge that provides a positive feedback to the channel sheet charge (and conductivity) that leads to an increase in output conductance at higher drain biases. The dual-gate HFET was introduced as an approach that both reduces the rate of impact ionization in the device, and shields the control gate depletion from impact ionization generated holes. This approach produced significantly improved DC characteristics in comparison to those of single gate HFETs. A quantum well engineering approach aiming to increase the energy gap in InAs by reducing the quantum well thickness (and thereby increasing the quantization energies in the quantum well) was attempted by fabricating otherwise identical 50 Å and 100 Å InAs channel HFETs. The similar magnitude of gate leakage in these devices suggested that impact ionization was *not* reduced by this approach. The output conductance and kink magnitude were reduced, but when the drain currents were normalized the drain characteristics appear similar for both channel thicknesses. Because microwave measurements show that the impact ionization levels *are* different for both well thicknesses, we must conclude that the kink appears through a charge

storage effect: even with a reduced ionization rate, enough positive space charge eventually builds up to increase the DC output conductance. This assertion is supported by the fact that the output conductance is several times lower at microwave frequencies.

6.1.2 Hole traps

We presented the first study of hole traps in AlSb/AlGaSb buffer layers using sidegating measurements on InAs/AlSb HFETs. The hole injection from the sidegate populates hole traps in the buffer layers. These hole traps show a significant field-dependence of ionization rate, so that when the drain bias is swept forward, holes are emitted from the traps in such a way that a pronounced sidegating-induced negative differential resistance (SINDR) results. The temperature and frequency dependence of SINDR was studied, and was found to show an activation energy of $E_A = 0.93 \pm 0.05\,\mathrm{eV}$. The present study reveals the importance of AlGaSb buffer layers in InAs/AlSb HFET technology and calls for a full characterization of deep levels in MBE-grown AlGaSb layers. Our work shows that the interaction of holes with traps in the AlGaSb buffer layers can cause significant distortions of the HFET low-frequency drain characteristics which may well be related to the presence of the kink in the I-V characteristics (note that the source of holes, and the bias conditions are different for the kink and sidegating effects).

6.1.3 Microwave performance dependence on mobility

Microwave measurements of otherwise identical 50Å and 100Å quantum well HFETs were performed. The significantly lower electron mobility in the 50Å channel resulted in much lower high-speed performance. This could be accounted for by the direct reduction of the effective electron velocity because of the reduced low-field mobility.

6.1.4 Impact ionization and microwave performance

The effect of increasing impact ionization on the scattering (S-) parameters was studied by several approaches. By increasing the drain bias for fixed gate bias, the rate of impact ionization in several devices was increased, affecting the S-parameters to the extent that they become qualitatively different from S-parameters in low impact-ionization devices. With impact ionization, the output reflection coefficient S_{22} shows *inductive* behavior below a certain frequency threshold that increases with increasing impact ionization rates. For very high levels of impact ionization, the input reflection coefficient S_{11} is also affected: instead of a purely capacitive and conductive behavior, S_{11} follows more complicated behavior suggestive of a positive feedback mechanism on the gate. A recently developed small signal equivalent circuit model intended to account for impact ionization is applied to the measured S-parameters, and the poor fit at high impact ionization rates highlights model inadequacies.

We found that impact ionization can affect microwave measurements to such a degree that certain common assumptions based on the standard small signal equivalent circuit model for HFETs (most notably the -20dB/decade roll-off in gain) become invalid. Specifically, we have seen that the frequency roll-off in current gain becomes shallower with increasing impact ionization rates. Several complementary measurements were presented to support our assertion: the quantum well width dependence of the microwave performance; the impact ionization rate (which varies with drain bias) dependence of the microwave performance; and a direct comparison of current gain roll-off with frequency between standard GaAs MESFETs, GaInAs/AlInAs HFETs, and the InAs/AlSb HFETs indicate that the standard microwave FET equivalent circuit model is inadequate in the presence of impact ionization.

Equivalent circuit parameters extracted using a small signal equivalent circuit that neglects impact ionization show much higher frequency dispersion for 100Å

quantum well devices than 50Å quantum well devices, further demonstrating that the impact ionization rate is significantly lower for the 50Å quantum well devices.

6.2 Future directions

6.2.1 Compliant substrates

The standard InAs/AlSb HFET design calls for very thick (a few μm) AlSb buffer layers to accommodate the 7% lattice mismatch between the 6.1Å InAs/AlSb/GaSb family and the GaAs substrate. These buffer layers are of low quality in comparison to the buffer layers of conventional InP or GaAs lattice-matched HEMTs. While AlSb/AlGaSb buffers are semi-insulating, they contain deep levels that are responsible for the strong kink in InAs/AlSb HFETs. The long growth time (~ 3 hours) required to grow these buffers is also of concern. Even with the thick AlSb buffers, a high density ($\sim 10^7 cm^{-2}$) of threading dislocations is present.

Recently, Cornell University researchers have demonstrated the growth of dislocation free, 3000Å thick GaSb [28] and 6500Å thick InSb [29] on a "Compliant Universal" (CU) GaAs substrate. The amazing properties of CU substrates are obtained by wafer bonding a GaAs thin film on a GaAs substrate with a 45° twist angle. The procedure results in the generation of an extremely dense, elastically deformable two dimensional array of screw dislocations that is strictly confined to the bonding interface and that can accommodate large amounts of strain energy. This technology presents a golden opportunity to level the playing field between InAs/AlSb HFETs and HFETs grown on semi-insulating lattice-matched substrates. The proposed process is the following:

a) start with LT-GaAs grown on standard SI GaAs substrate
b) using CU technology, wafer-bond a 30Å GaAs film at a 45° misalignment
c) grow AlSb/InAs/AlSb quantum well directly on the CU substrate, and follow with standard cap layer structure
d) perform standard fabrication, using the LT-GaAs as the mesa floor

A simplified schematic of the final device structure is shown in Figure 6-1. Depending on the initial quality of MBE AlSb growth, the bottom barrier layer thickness may be minimized to reduce the volume that holes can be trapped in before they reach the LT-GaAs buffer.

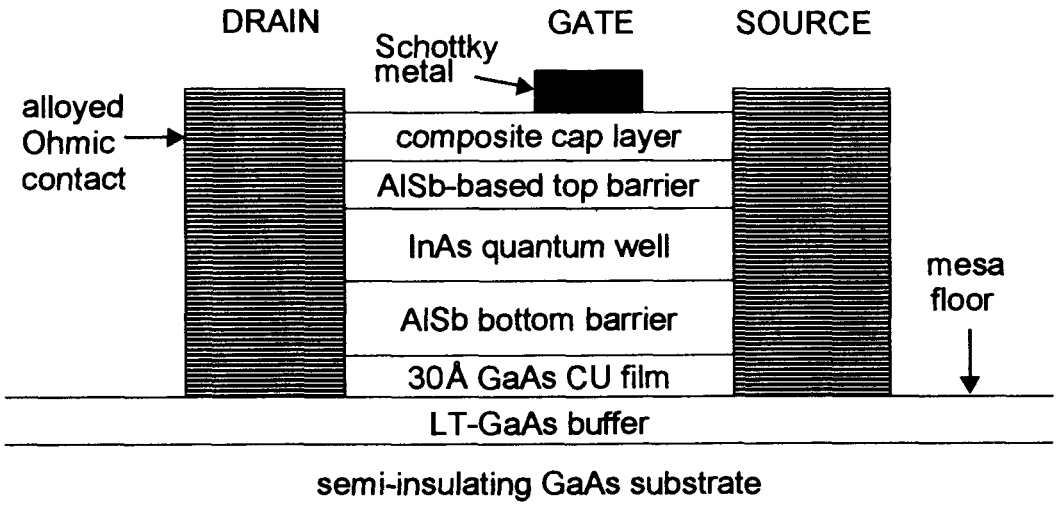

Figure 6-1 : Cross-section of proposed InAs/AlSb HFET grown on CU substrate with an LT-GaAs buffer layer (not to scale).

Any impact-ionized holes injected into the LT-GaAs layer would quickly recombine, thus eliminating the parasitic bipolar and "static charge amplifier" effects that plague ordinary InAs/AlSb HFETs. The effect of the buffer layer has been shown to be dramatic in other high-kink HFETs: 0.2μm AlInAs-GaInAs HFETs grown using a standard high-resistivity AlInAs buffer have an output conductance of 88mS/mm and a transconductance of 880mS/mm, whereas the same HFETs grown on an LT-AlInAs buffer have an output conductance of less than 10 mS/mm with only a slight reduction in transconductance to 800mS/mm [14]. Another advantage of using CU technology would be the realization of dislocation-free InAs/AlSb HFET layers.

The difficulty in producing "large" (> cm^2) CU substrates is their greatest perceived disadvantage. However, the potential advantages of CU substrates are many-

fold. Most obvious is the potential improvement in device performance. Not only should the LT-GaAs buffer reduce the kink effect in these HFETs, but the absence of threading dislocations may improve device characteristics. The impact of dislocations on device performance in InAs/AlSb HFETs remains to be determined.

6.2.2 Other buffer layer schemes

Less extreme efforts to improve the present InAs/AlSb buffer layer schemes may be sufficient, however. Simply reducing the buffer layer thickness, and performing mesa isolation down to the underlying GaAs substrate, may also be advantageous for device applications. Thinner buffer layers (~0.25 μm) have been used in early work by Tuttle [73]. The resulting InAs channels showed similar room temperature mobilities of 20,000 $cm^2/V{\cdot}s$, but much lower low temperature mobilities when compared with quantum wells grown on thick buffer layers.

Other buffer layer compositions are also promising. As was demonstrated by Miya *et al.* [49], AlGaAsSb layers lattice-matched to GaSb can be used to produce relatively thin (0.8 μm) buffer layers but still achieve good ($f_T{\cdot}L$ = 40 GHz·μm) high frequency performance. The AlGaAsSb also serves as the channel barrier, and the likely valence band offset at the InAs/AlGaAsSb interface serves to confine holes to the channel.

6.2.3 Device characterization and modeling

The InAs/AlSb material system remains poorly studied in comparison to the GaAs and InP -based systems. A DLTS study that provides quantitative identification of traps in the device layers remains to be performed. To our knowledge, the electron velocity in InAs/AlSb quantum wells has never been directly measured. Such a measurement could be achieved on ungated FET structures by the geometric magnetoresistance technique [45].

The microwave characterization of InAs/AlSb HFETs revealed that standard models (even those attempting to include the effect of impact ionization) fail to describe adequately even qualitatively the measured S-parameters. A model that properly addresses the DC and microwave effects of impact ionization remains to be derived.

APPENDIX A
InAs/AlSb HFET Processing Details

A *Process run sheet for alloyed Ohmic contact HFET*

1. Source/drain Ohmic contact lithography (using AB-Manufacturing contact aligner)

a) standard clean: hot TCE/cold ACE/hot METH/cold ISO, N_2 blow dry, evaporate residual solvent on 105 °C hot plate (HP) for 2 min

b) spin on Shipley 412 photoresist (PR) 30 sec @ 6.75 krpm

c) HP bake 30 sec @ 105 °C

d) expose 380 nm mid-UV 12 sec @ 25 mW/cm^2

e) soak in toluene 10 min

f) oven bake 10 min @ 80 °C

g) develop in Shipley Microposit Concentrate: de-ionized (DI) water (3:1) for 2 min 15 sec, agitating every 35 sec

2. Source/drain Ohmic contact metal evaporation

a) load wafers in Gene's Beast; pump until base pressure reaches ~$3 \cdot 10^{-7}$ torr

b) evaporate: ~180 Å of Ge at 2-4 Å/s with I=0.03 A, ~340 Å of Au at 4-6 Å/s with I=0.04 A, ~110 Å of Ni at 2-3 Å/s with I=0.07 A, ~3000 Å of Au at 4-6 Å/s with I=0.04 A

c) soak >5 min in ACE, and perform lift-off by squirting ACE directly at wafer; rinse in METH and ISO

3. Source/drain Ohmic contact alloying

a) place wafers in graphite stripe reaction chamber and purge with forming gas > 3 min

b) alloy for 2 min @ 275°C

c) let cool to <100°C in chamber

4. Mesa lithography (using AB Manufacturing contact aligner)

a) standard clean

b) spin on Shipley 812 PR 30 sec @ 4 krpm

c) HP bake 45 sec @ 115°C

d) expose 380 nm mid-UV for 12 sec @ 25 mW/cm^2

e) develop in Shipley Microposit Concentrate: DI (3:1) for 2 min 15 sec, agitating every 35 sec

5. Mesa isolation by wet etching

a) etch through AlSb top barrier using NH_4OH:DI 7:35 mL

b) etch through InAs quantum well using Acetic:DI:H_2O_2 25:25:5 mL

c) etch through AlSb bottom barrier down to AlGaSb etch stop layer using NH_4OH:DI 7:35 mL

d) undercut InAs quantum well to prevent short-circuiting using Acetic:DI:H_2O_2 25:25:5 mL

e) strip resist in ACE, and rinse in METH/ISO

6. Gate lithography (using AB Manufacturing contact aligner)

a) standard clean

b) spin on Shipley 412 PR 30 sec @ 6.75 krpm

c) HP bake 30 sec @ 105°C

d) expose 380 nm mid-UV 12 sec @ 25 mW/cm^2

e) soak in toluene 10 min

f) oven bake 10 min @ 80°C

g) develop in Shipley Microposit Concentrate: DI (3:1) for 2 min 15 sec, agitating every 35 sec

7. Source/drain Ohmic contact metal evaporation

a) load wafers in Gene's Beast; pump until base pressure reaches ~$3 \cdot 10^{-7}$ torr

b) evaporate either:

(i) ~3500 Å of Al at 2-3 Å/s with I=0.03 A, or

(ii) ~300-1500 Å of Ti at ~2 Å/s with I=0.03 A, and ~3000 Å of Au at 4-6 Å/s with I=0.04 A

c) soak >5 min in ACE, and perform lift-off by squirting ACE directly at wafer; rinse in METH and ISO

8. (optional) InAs cap etch

a) standard clean

b) etch InAs cap using Acetic:DI:H_2O_2 25:25:5 mL

B Process run sheet for non-alloyed Ohmic contact HFET

1. Source/drain Ohmic contact lithography (using AB Manufacturing contact aligner)

a) standard clean

b) spin on Shipley 412 PR 30 sec @ 6.75 krpm

c) HP bake 30 sec @ 105 °C

d) expose 380 nm mid-UV 12 sec @ 25 mW/cm^2

e) soak in toluene 10 min

f) oven bake 10 min @ 80 °C

g) develop in Shipley Microposit Concentrate: DI (3:1) for 2 min 15 sec, agitating every 35 sec

2. Expose InAs quantum well

a) etch through AlSb top barrier using NH_4OH:DI 7:35 mL

b) strip resist in ACE, and rinse in METH/ISO

3. Source/drain Ohmic contact metal evaporation

a) load wafers in Gene's Beast; pump until base pressure reaches ~$3 \cdot 10^{-7}$ torr

b) evaporate: ~200-1500 Å of Ti at 2-4 Å/s with I=0.03 A, ~2000-3000 Å of Au at 4-6 Å/s with I=0.04 A

c) soak >5 min in ACE, and perform lift-off by squirting ACE directly at wafer; rinse in METH and ISO

The remaining steps of mesa isolation and gate metallization are identical to steps 4-8 of the alloyed InAs/AlSb alloyed Ohmic contact HFET process.

C *Note on edge bead removal*

Because of the wave nature of light, contact lithographic imaging is extremely sensitive to the separation between the photolithographic mask and the photoresist. In practice, this separation is set by an edge bead of photoresist, approximately 2-3 μm thicker than the ~1 μm photoresist thickness, which forms around the edge of the wafer as the result of surface tension and viscosity effects. For reliable sub-micron imaging, the edge bead must be removed. A clean and reliable technique of edge bead removal is: expose the photoresist along the edge of the wafer for ~2 min at 25 mW/cm^2, and develop for approximately 2 min in the standard developer solution. Two images taken from the same wafer (Figure A-1) illustrate the resolution variation across a wafer when the edge bead is not removed.

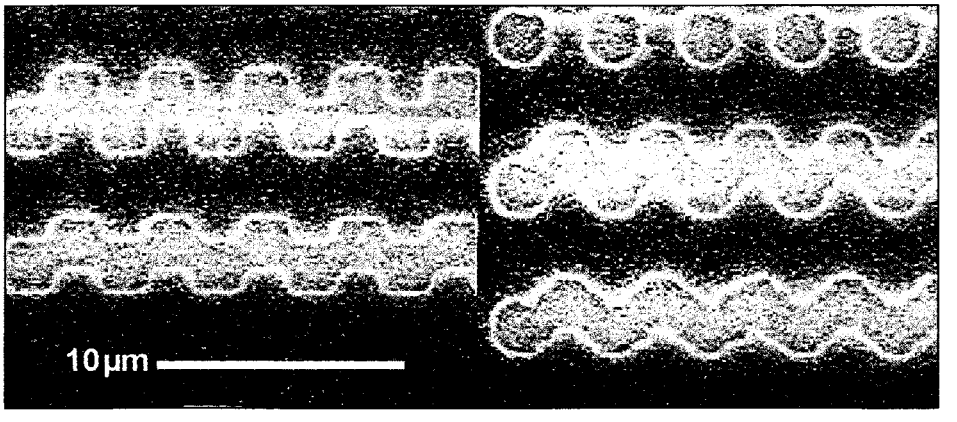

Figure A-1 : Demonstration of inconsistent resolution obtained at two different parts of same wafer when no edge bead removal is performed.

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