MODELING AND SIMULATION OF SATURATING HOT ELECTRON DEGRADATION IN LDD NMOSFETs - FROM EARLY MODE TO LATE MODE

by

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ABSTRACT

In this thesis, we report an extensive investigation on the saturating hot-electron degradation effects in sub-micron lightly-doped-drain (LDD) n-channel metal oxide semiconductor field effect transistor (NMOSFET) devices. We have developed a new phenomenological device degradation model based on propagation of hot-electron defects from the sub-spacer silicon-silicon dioxide interface region to the sub-gate interface region. The main implication of this model is that the defects do not accumulate at one point in the device structure, as previously thought, but the defects profile extends into the device with increasing hot-electron stress.

Based on various experimental features of these devices under hot-electron degradation, we have used both analytical modeling and 2-D device simulation within an in-house developed virtual factory environment to delineate the special features of the hot-electron degradation in LDD devices. These features include a sharp rate of early mode degradation, followed by a much lower rate of late mode degradation. The initial degradation is shown to increase the parasitic drain series resistance in the gate-edge subspacer LDD region, thus making the device asymmetric. We therefore developed a simple and general method to extract the asymmetric parasitic source and drain resistances using a single MOSFET and its small signal transconductance and drain conductance data.

Using the floating gate measurement technique, we extracted an interesting evolution in the hot-electron gate currents in the early phase of the degradation which correlated very well with the corresponding evolution in drain parasitic resistances. These evolutions, coupled with corresponding evolutions in substrate currents, linear and saturation drain currents lead to a 2-D simulation framework involving negative trapped charges in the gate-edge interface region in the earlymode degradation situation.

Further experiments of the various MOSFET currents during the late mode degradation situation are seen to match very well with simulation results after placement of trapped charges above the sub-gate LDD region. These correlations help us develop an analytical phenomenological model for defects propagation length versus stress time. It is seen that the propagation length saturates with increasing stress time. We then couple this model with defects propagation simulation to actually demonstrate the two-stage transconductance degradation observed in practice.

Finally, we report a simple technique based on evolving saturation drain currents in a progressively stressed MOSFET, to estimate the evolutions in three main parameters of the device, namely, mobility, series resistance, and threshold voltage. This simple technique can be used to update the circuit simulation model parameters for circuit reliability simulations. We expect that the results of this thesis will be useful for developing new hot-electron lifetime prediction methods, better device design, and parametric esimation algorithm.

DEDICATION

To my parents, my wife Debasree, and my daughter Nirokhi

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a0, a1, and a2	coefficients of the curve fitting polynomial
C	proportionality constant for hot-carrier lifetime calculation (Ch.2)
C	constant in the expression for gate bias dependence of (R_S+R_D)
C (F)	total capacitance associated with gate (Ch. 4)
C_1	proportionality constant for substrate current calculation
C_2	proportionality constant for gate current calculation
C_3	proportionality constant for interface traps calculation
C_{ox} (F/cm^2)	gate oxide capacitance per unit area
$C_{0.5d}$ (F/cm^2)	capacitance due to oxide trapped charge distribution region
d (Å)	vertical width of oxide trapped charge distribution
E (V/cm)	local lateral electric field, scalar
$\boldsymbol{E}$ (V/cm)	local lateral electric field, vector
E_1, E_2(V/cm)	local lateral electric fields at stress times t_1, t_2
E_{sat} (V/cm)	critical field for velocity saturation
E_m (V/cm)	maximum channel field
f (Hz)	gate pulse frequency
g_m (A/V)	measured transconductance
g_{mf} (A/V)	transconductance measured in normal mode
g_{mr} (A/V)	transconductance measured in reverse mode
$g_{mr,d}$ (A/V)	g_{mr} for degraded device
$g_{mr,v}$ (A/V)	g_{mr} for virgin device
g_{m0} (A/V)	intrinsic transconductance

g_{mS} (A/V)	g_m measured with R_X added to source side
g_{mD} (A/V)	g_m measured with R_X added to drain side
g_d (A/V)	measured drain conductance
g_{d0} (A/V)	intrinsic drain conductance
g_{b0} (A/V)	intrinsic substrate conductance (mag.)
I_{CP} (A)	charge pumping current
I_{DS} (A)	drain current
$I_{DS,sat}$ (A)	saturated drain current
$I_{DS,sat,reverse}$ (A)	saturated drain current measured reversely
I_G (A)	channel hot-electron induced gate current
$I_{G,d}$ (A)	I_G for degraded device
$I_{G,v}$ (A)	I_G for virgin device
I_{SUB}, I_B (A)	impact ionization induced substrate current
$I_{B,\max}$ (A)	maximum I_B in I_B vs. V_{GS} curves
I_E (A)	channel hot-electron induced injection current
$\boldsymbol{J}$ (A/cm^2)	local current density vector
k_B (J/°K)	Boltzmann's costant
K (Ω)	constant in the expression for gate bias dependence of (R_S+R_D)
K , K' (A/V^2)	gain factor in drain current expression (Ch. 6)
l (μm)	calculated length of the velocity-saturation region
l' (μm)	simulated length of the velocity-saturation region
L, L_m (μm)	drawn gate length
L_{eff}, L' (μm)	effective channel length

m	power of substrate current in hot-carrier lifetime calculation
m_e (gm)	electron effective mass
n	power of stress time in hot-carrier degradation over time
n_i (/cm^3)	intrinsic carrier concentration in silicon
N_{it} (/cm^2)	interface trap density
N_{SUB} (/cm^3)	substrate doping concentration
N_{LDD} (/cm^3)	lightly doped drain doping concentration
N_t (/cm^3)	oxide trapped charge density
q (C)	electronic charge
Q_B (C)	bulk depletion charge
Q_{INV} (C)	channel inversion charge
Q_{it} (C)	interface trapped charge
$Q_n(y)$ (C/cm^2)	induced mobile electronic charge density in channel
R_S (Ω)	source parasitic resistance
R_{Sm} (Ω/V)	derivative of source parasitic resistance with respect to gate bias
R_D (Ω)	drain parasitic resistance
R' (Ω)	R_D-R_S
R_t (Ω)	R_S+R_D
R_{Dm} (Ω/V)	derivative of drain parasitic resistance with respect to gate bias
R_X (Ω)	externally added resistance
ΔR_{S1} (Ω)	error in R_S due to neglect of mobility degradation
ΔR_{S2} (Ω)	error in R_S due to neglect of R_{Sm} and R_{Dm}
s (°K/cm)	slope of the electron temperature profile in to channel

S (mV/$\log_{10}$A)	subthreshold slope
t (s)	time of stress
t_0 (s)	initial time instant for degradation
t_1, t_2 (s)	intermediate time instants for degradation
T_e (°K)	electron temperature
T (°K)	lattice temperature
T_{ox}, t_{ox}(cm)	gate oxide thickness
V_{GS} (V)	gate-to-source bias
V_{GS}' (V)	intrinsic gate-to-source bias
V_{DS} (V)	drain-to-source bias
V_{DS}' (V)	intrinsic drain-to-source bias
$V_{DS,sat}$ (V)	saturation drain-to-source bias
V_{BS} (V)	bulk-to-source bias
V_{SB}' (V)	intrinsic source-to-bulk bias
V_S (V)	applied source bias in charge pumping measurement
V_D (V)	applied drain bias in charge pumping measurement
V_R (V)	equal V_S and V_D applied in charge pumping measurement
ΔV (V)	V_D - V_S
V_T (V)	threshold voltage
$V_C(y)$ (V)	channel potential at point y
v (cm/sec)	the velocity of a single electron
v_d (cm/sec)	the mean drift velocity of electrons
W (μm)	channel width

X_S (μm)	interfacial position of the source depletion width
X_D (μm)	interfacial position of the drain depletion width
X_j, x_j (cm)	source/drain junction depth
ε_s (F/cm)	silicon permittivity
μ (cm^2/V-s)	effective mobility of the channel electrons
μ_0 (cm^2/V-s)	low field mobility
θ (1/V)	constant for calculation of gate bias dependence of mobility
λ_r (nm)	accoustic (elastic) scattering mean free path
λ (nm)	optical (inelastic) scattering mean free path
λ (1/V)	inverse of Early voltage (Ch. 3)
Φ_F (V)	Fermi potential
Φ_i (eV)	characteristic energy for impact ionization
Φ_b (eV)	oxide-silicon barrier height
Φ_{it} (eV)	characteristic energy for interface trap creation
τ (s)	hot-carrier lifetime

*Additional symbols used in Appendices have been explained contextually.

Chapter 1

Introduction

1.1 Introduction

Microchips represent the workhorse of modern information technology. From computers to digital watches, from electronic dashboard of cars to hand-held video games, microchips are everywhere. These integrated circuits control the production of ships and aircrafts. The technology of satellites and spacecrafts are heavily dependent on their widespread use in these vehicles as well as in the ground-based control stations. If we removed the microchips from all these applications, the world as we see it today could come to a grinding halt.

With a continuous push to perform more and more functions on a single chip, the complexity of the integrated circuits, invented in 1959, has grown exponentially over the years [1.1]. At the same time the chip size has grown only modestly. This enormous increase in packing density was possible only by reducing the size of the basic component of the integrated circuit, namely, the transistor. In spite of its popularity as the candidate for integrated circuits, the bipolar transistors [1.2] have given way to their more modern counterparts, namely, the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [1.3]. The MOS technologies can achieve a higher packing density at a lower cost. Even the inherent superiority of the bipolar transistors in terms of higher speeds has been largely overcome by continuously shrinking the size of the MOSFET, in a systematic effort known as scaling [1.4].

But scaling of MOSFETs gives rise to two problems, namely, the short channel effects [1.5] and the hot-carrier effects [1.6]. The short channel effects are responsible for

some unexpected and undesirable modifications of the electrical characteristics of the device, that affect its functionality. On the other hand, the hot-carrier effects degrade the electrical performance of the device over time, reducing the acceptable life span of the device. This is, therefore, a reliability problem.

The hot-carrier effects represent one of the most important reliability issues for the scaled MOSFETs. In fact, it has been shown through a systematic performance optimization procedure that for submicron MOSFETs, in either digital or analog environment, both channel length reduction and supply voltage are limited mainly by hot carrier induced degradation among a host of important performance and reliability constraints [1.7]. Therefore, it was only natural that this subject should receive as much research attention as it has received and continues to do so.

1.2 Aim of this thesis

In this thesis, we study some of the aspects of hot-carrier effects as they affect the sub-micrometer lightly doped drain (LDD) MOSFETs [1.8] [1.9] that represent a frequently used version of the conventional MOSFET. The LDD MOSFETs were introduced to overcome the hot-carrier effects to some extent. However, they have their own features of current degradation behavior. These features are listed below.

(1) The hot carrier degradation increases the drain parasitic resistance in a significant way, making the transistor progressively asymmetric, that is, the source and drain parasitic resistances (R_S and R_D) become increasingly unequal over time.

(2) There is a very sharp early phase of the degradation of the transistor current, followed by a much slower late phase of the degradation. This is unlike the constant rate (on a logarithmic scale) of degradation in the case of conventional transistors.

(3) The net degradation in MOSFET current is a result of the shift in three parameters, namely, drain parasitic resistance (R_D), carrier mobility (μ), and threshold voltage (V_T).

In this work we will address these issues for the submicron LDD NMOSFET. We developed a phenomenological model for the hot-carrier degradation in the LDD MOSFET; a model that attempts to understand the detailed experimental features of the degradation through a defects propagation scheme [1.10].

For the first time, we report a parameter extraction procedure [1.11] [1.12] that decouples the parasitic resistances R_S and R_D from measurements of transconductances and drain conductances on a single LDD MOSFET. We then use this technique to study the early mode degradation of the MOSFET that mainly effects an evolution in R_D, a corresponding evolution in the channel hot-carrier induced gate current (I_G), and impact ionization induced substrate current (I_B). Correlation of the shifts in these three parameters (R_D, I_G, and I_B) leads to a 2-D device simulation framework that helps us locate and quantify the early mode defects in drain side gate edge region [1.13] [1.14]. We also use spatial profile charge pumping measurements [1.15], and show that these defects cannot be detected by the charge pumping measurement. Hence, the use of 2-D device simulation is necessary. Using the simulation framework, and various experimental features of degradation, we model the two-stage current degradation in the MOSFET with a propagating defects scheme [1.16], and provide an analytical model for the defects propagation with hot-carrier stress time. We finally provide a simple procedure to separately extract three main quantities ΔR_D, $\Delta\mu$, and ΔV_T that determine the evolving degradation of the LDD NMOSFET. This simple parameter extraction method will be useful in updating the SPICE parameters of a degrading MOSFET. In most previous works on hot-carrier modelling, the linear region of operation of the MOSFET was used for hot-carrier degradation analysis. In this thesis, we establish the fact that the saturation

region operation of the transistor is also appropriate and useful in hot-carrier degradation analysis.

We believe that the results of this work will be useful for better device design for hot-carrier reliability, hot-carrier life time modelling, and parameter extraction. We have tried to keep the mathematical models simple, so that the results are appealing for engineering applications.

A very important requirement in proper device design for sub-micron CMOS/ BiCMOS technologies is the ability to perform matrix process and device simulations to assess the effects of process modifications on the performance and reliability of transistors. We have spent quite a bit of effort in this direction and developed a capability for matrix process simulation [1.17] and matrix device simulation [1.18] using TSUPREM4 2-D process simulator [1.19] and MEDICI 2-D device simulator [1.20] respectively. We hope these *"virtual factory"* schemes will allow a user to perform meaningful device optimization for performance and reliability.

1.3 Organization of this thesis

In the next chapter, we provide a brief background of the hot-carrier problem, starting with a simplified description of the structure and operation of the MOSFET. We discuss the physical basis of hot-carrier generation, the currents and degradation produced by hot-carrier generation, and some hot-carrier modelling aspects. We finally introduce the LDD NMOSFET, and discuss its special features of hot-carrier degradation.

In chapter 3, we discuss a new technique for extracting the parasitic source and drain series resistances (R_S and R_D) separately from the measurements of the a.c. conductances on a single MOSFET. We develop the theory of these conductances including the effect of gate bias dependent series resistances. We apply this theory on the saturation currents to

extract the difference between R_S and R_D, and on linear currents to extract their sum. We also discuss in detail the accuracy of this new technique.

In chapter 4, we investigate the sharp early mode of hot-carrier degradation in the LDD NMOSFET using the floating gate technique and the transconductance technique developed in chapter 3. We show an interesting correlation between the evolution of channel hot electron induced gate currents, and the drain parasitic resistances in the early phase of the degradation. We also use the spatial profiling charge pumping technique to track the interface traps in the near-drain channel region that may be produced during the early phase of the degradation, and show that the interface traps actually decrease towards the drain, in contrast to previous results. Also, little trapped-charge-induced shift in the raw charge pump profile indicates that the early mode degradation occurs outside the channel region of the transistor.

In chapter 5, the most important chapter of this thesis, we develop a phenomenological model for defect propagation under progressive hot-carrier degradation, starting with the early mode defects. Defects are assumed to be trapped negative charges in the interfacial oxide arising out of electron-filled oxide traps and interface traps. Their location and quantity has been determined using a 2-D device simulation framework built up using the experimental results of chapter 4, and further measurements and simulation under early mode and late mode degradation. The simulation results and the corresponding experimental features of early mode and late mode degradation help us build up a simple analytical model for defects propagation with time. We verify the model through defects propagation simulation, and matching with the experimental two-stage transconductance degradation for our MOSFET.

In chapter 6, we demonstrate a simple technique for extracting the degradation parameters ΔR_D, $\Delta\mu$, and ΔV_T under progressive hot-carrier degradation of an LDD NMOSFET from degrading saturation current measurements on a single transistor. These

parameters are then used to update the SPICE parameters of the transistor, and it is shown that the updated SPICE parameters model the degraded I-V characteristics (measured) of the transistor very well. The same parameters extracted from an indirect method using degrading linear characteristics of the transistor show a good match with those obtained from the direct method.

In chapter 7, we conclude the thesis. This chapter highlights the originality and usefulness of this work.

Each chapter is self-contained with its own set of bibliographical references and embedded figures. But references are made to previous chapter(s) whenever appropriate. Two appendices have been added at the end of the thesis. The first appendix discusses the virtual factory scheme used to control 2-D process and device simulations. The simulated MOSFETs were generated using this scheme. The second appendix gives some model details for the MEDICI 2-D device simulator [1.19] that are relevant to our work.

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Chapter 2

Background

2.1 Introduction

In this chapter we will provide a brief background to the hot-carrier problem, starting with a discussion of the structure and operation of the MOSFET which is the main device of our study. As discussed in the introductory chapter, the hot-carrier problem is an effect of transistor scaling or down-sizing. In order to appreciate the effects of scaling, the brief discussion of the structure and operation of the conventional MOSFET (with heavily doped source and drain) in the next section is very relevant. Only first order theory of the MOSFET is considered for simplicity.

What are hot carriers? How are they generated? What is their effect on the transistor operation? How can they be modelled? These are some of the questions that we will try to answer in the succeeding sections of the thesis. We will discuss the physical basis for hot-carrier generation, and show how the hot-carrier problem is aggravated due to dimensional down-scaling. We then go on to discuss the hot-carrier induced currents and performance degradation in the MOSFET. Three approaches have been tried to model the hot-carrier effects. Of them, the analytical "lucky electron" model is the most commonly used engineering model for life-time prediction purposes. We will briefly discuss this model and its implications for the analysis of the conventional MOSFET. Finally, we will introduce the reader to the basic LDD structure and the special features of hot carrier degradation of the LDD device. The importance of the parasitic source and drain resistances (R_S and R_D) for the LDD transistor will be discussed as well. We will also discuss why, due to the lack of adequate direct experimental techniques, device simulation

is necessary to probe at the hot-carrier induced defects in the LDD MOSFETs, and eventually model their growth. An example will be given to show the circuit effect of hot-electron degradation using a ring oscillator circuit that employs the LDD MOSFETs. The purpose of providing this example is to indicate a motivation for development of a simple, yet robust technique for parameter extraction in the course of hot carrier degradation process, so that circuit simulation parameters can be easily upgraded.

2.2 The MOSFET structure and operation

MOSFETs are of two types, namely, n-channel MOSFETs (NMOSFETs in short) and p-channel MOSFETs (PMOSFETs) depending on whether the current is carried by electrons or holes, respectively. They are unipolar field-effect transistors usually fabricated on moderately doped silicon wafers through such technological steps as oxidation, selective etching, selective ion implantation, and materials deposition. Selection of regions for etching and ion implantation is achieved through photolithographic techniques. Fig. 2.1 shows the typical structure of an NMOSFET. Oxidation is used to produce silicon-dioxide layers that serve 1) to separate the deposited polysilicon gate from the underlying silicon in the form of a thin (100-1000Å) gate oxide, and 2) to create isolation regions between two transistors on the same wafer in the form of a thick field oxide (5000-10000Å). Selective etching is used to delineate the gate region, to open holes for making contacts to the source, the drain, and the gate regions, and to define the poly and metal interconnections between devices. The contact to the gate region is not shown in fig. 2.1(a) since this contact is normally made away from the channel region which is the region of silicon between source and drain. Ion implantation is done to create the heavily doped source, drain, and bulk contact regions. The bulk contact and the source contact is shown to be shorted in fig. 2.1(a). While this is often the case in many circuit situations where the combined contact is at the ground potential, this is not always

the case. For this reason, we show the bulk terminal as a separate terminal in the schematic of fig. 2.1(b). The deposited materials in the structure shown in fig. 2.1(a) include the n^+ gate poly layer, the metal layer, and the CVD (chemical vapor deposited) oxide layer that separates the poly and metal layers. The processing sequence used to generate the structure is known as a planar LOCOS (local oxidation of silicon) [2.1] process. More detailed description of the process sequence can be found in ref. [2.2].

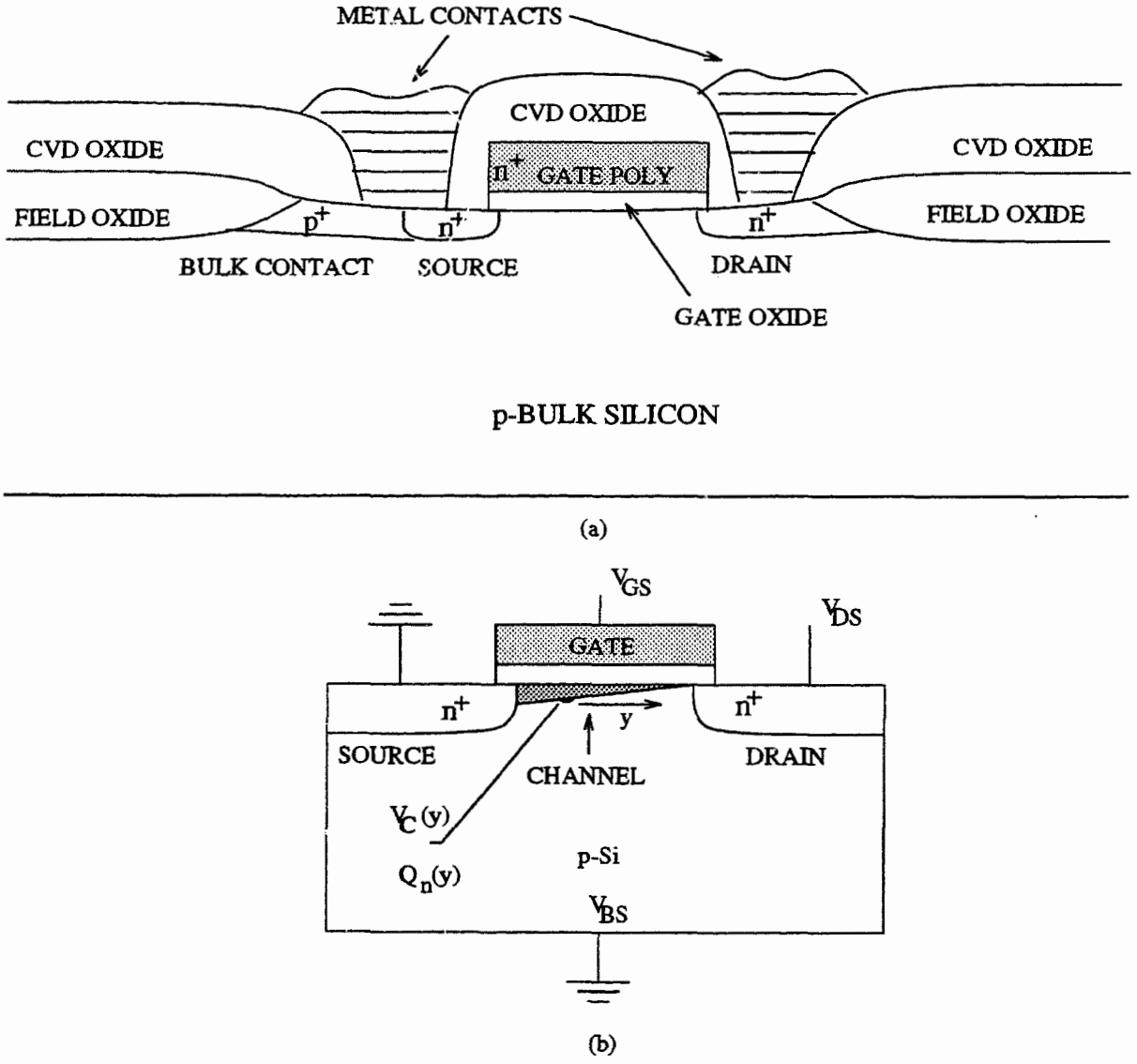

Fig. 2.1. (a) The structure of a typical conventional NMOSFET. (b) The corresponding schematic diagram. In general, V_{BS} can be at a potential other than ground.

It is appropriate to mention at this point that, structurally, a PMOSFET differs from an NMOSFET in that the polarity of all the doping types are opposite, i.e., the source and the

drain are implanted p^+, and the bulk contact region is implanted n^+ on an n-type silicon wafer. However, the gate poly is often of the same doping type (n^+) as with NMOSFETs.

When a gate voltage V_{GS} higher than the threshold voltage V_T is applied to the gate of the NMOSFET shown schematically in fig. 2.1(b), the minority carriers (electrons) from the p-type substrate accumulate below the gate oxide to form a channel between the source and the drain. This "strong inversion" of the polarity of the sub-surface silicon region takes place due to the capacitive induction of charge across the gate oxide layer. Now, an applied V_{DS} can drive current through the MOSFET. Also, the channel resistance, and hence the drain current I_{DS} can be modulated by changing the gate bias V_{GS}. This is the basic field-effect transistor action. It should be mentioned here that a small subthreshold current exists even for $V_{GS}<V_T$, the "weak inversion" situation. But, most operations of the MOSFET depend on its above-threshold characteristics. We will therefore concentrate on this region of operation.

The application of the drain bias V_{DS} makes the channel non-uniform as shown in fig. 2.1(b) due to the potential drop along the channel. The induced mobile electronic charge density $Q_n(y)$ at any point y in the channel is given, to a first-order approximation, by

$$Q_n(y) = -\left[V_{GS} - V_T - V_C(y)\right]C_{ox} \tag{2.1}$$

where C_{ox} is the gate oxide capacitance per unit area, and $V_C(y)$ is the channel potential at y. Also, if W is the width of the channel (direction perpendicular to the surface of paper), and μ the effective mobility of the channel electrons, then the drain current I_{DS} is given by,

$$I_{DS} = \mu W \frac{d}{dy} V_C(y) \left| Q_n(y) \right|. \tag{2.2}$$

Combining, eqns. (2.1) and (2.2), it is easy to eliminate $Q_n(y)$. We can then integrate both sides of the resulting expression between source and drain, and express the drain current

in terms of the applied biases V_{GS} and V_{DS} as well as the physical parameters of the device, namely, μ, C_{ox}, W, and L_{eff}, the effective channel length between the source and drain junctions. It is obvious that the effective channel length is less than the length L of the gate due to side diffusion of the implanted source and drain regions. The resulting equation for I_{DS} is given by

$$I_{DS} = \mu C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS}. \tag{2.3}$$

The above equation (2.3) is known as the linear drain current equation and it is valid when $V_{DS}<V_{GS}-V_T$. The reason why it is called a linear drain current equation is that when V_{DS} is small, the $V_{DS}/2$ term in the bracket on the right side of (2.3) is negligible compared to the normally high gate drive ($V_{GS}-V_T$) term, and the current is seen to vary linearly with V_{DS}. As V_{DS} grows, and ultimately equals $V_{GS}-V_T$, the channel pinches off at the edge of the drain junction as shown in fig. 2.1(b). Further, increase of V_{DS} fails to increase the current, which essentially levels off at

$$I_{DS,\,sat} = \mu C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_T)^2. \tag{2.4}$$

The above equation (2.4) represents the saturated drain current of the NMOSFET, and is valid when $V_{DS} > (V_{GS}-V_T)$. When V_{DS} equals ($V_{GS}-V_T$), we call this the saturation drain bias $V_{DS,sat}$ corresponding to a particular V_{GS}. The equations (2.3) and (2.4) represent the first order approximation of the electrical behavior of an NMOSFET. The same set of equations are also valid for the PMOSFET with all voltage and current polarities reversed.

When a MOSFET is scaled to sub-micron channel lengths, several second order effects need to be properly accounted for in order to accurately model its electrical behavior. Such effects as V_T lowering due to source-drain proximity, vertical field dependent mobility, inversion layer capacitance, channel length shortening in the

saturation region, velocity saturation of the channel electrons, and increasing role of source and drain parasitic resistances cause the I-V characteristics deviate from the simple model given above. An excellent description of these effects in relation to device scaling is given in [2.3], and the detailed analysis of the theory of the MOSFET is given in [2.4].

However, most of these short channel effects except the last two of the mentioned above are not directly relevant to the hot-carrier problem, and therefore will not be discussed here. We will explain the relevance of the velocity saturation effect, and that of the issue of the source and drain parasitic resistances to the hot-carrier problem later. It must be mentioned here that the hot-carrier effect which arises due to high electric fields ($>10^4$ V/cm) in short channel MOSFETs is, by itself, a short channel effect because, it enhances the drain current for higher V_{DS} biases in the MOSFET's I_{DS}-V_{DS} characteristics. This additional role of the hot-carrier effect on top of its reliability implications will become clear in the succeeding discussion.

2.3 Hot carrier generation

When a drain bias V_{DS} is applied to a MOSFET, the carriers (electrons in the case of NMOSFET) gain energy from the resulting longitudinal electric field, and lose it through collisions with the thermally excited vibrations of the crystal lattice, popularly known as phonons. While collision with low frequency acoustic phonons, mainly redirects a moving electron, the latter principally loses energy through collisions with higher frequency optical phonons. The redirection process of the electron is known as elastic scattering, and the energy-loss process is called inelastic scattering. Both of these scattering processes are characterized by respective mean free paths, λ_r and λ. Widely used values of these quantities for room temperature silicon are 61.6 nm and 9.2 nm respectively [2.5]. When the MOSFET works in the linear region, the channel electric field (derivative of the channel potential $V_C(y)$ with respect to y as in fig. 2.2) is nearly constant and small. But, as the MOSFET approaches saturation, the electric field increases rapidly near the drain.

This situation can be easily demonstrated by plotting $V_C(y)$ vs. y using the linear region expression for $V_C(y)$ as derived using equations (2.1) and (2.2) above,

$$V_C(y) = V_{GS} - V_T - \sqrt{(V_{GS} - V_T)^2 - \frac{2}{\mu C_{ox} W} I_{DS} y}. \qquad (2.5)$$

The above equation is plotted below for two values of drain current I_{DS}, 0.4 mA and 1.9 mA for a typical transistor. The 0.4 mA curve represents the linear curve for an L_{eff} of just above 1 μm, while the 1.9 mA curve corresponds to a situation when the transistor approaches saturation with the field near drain exceeding 10^4 V/cm.

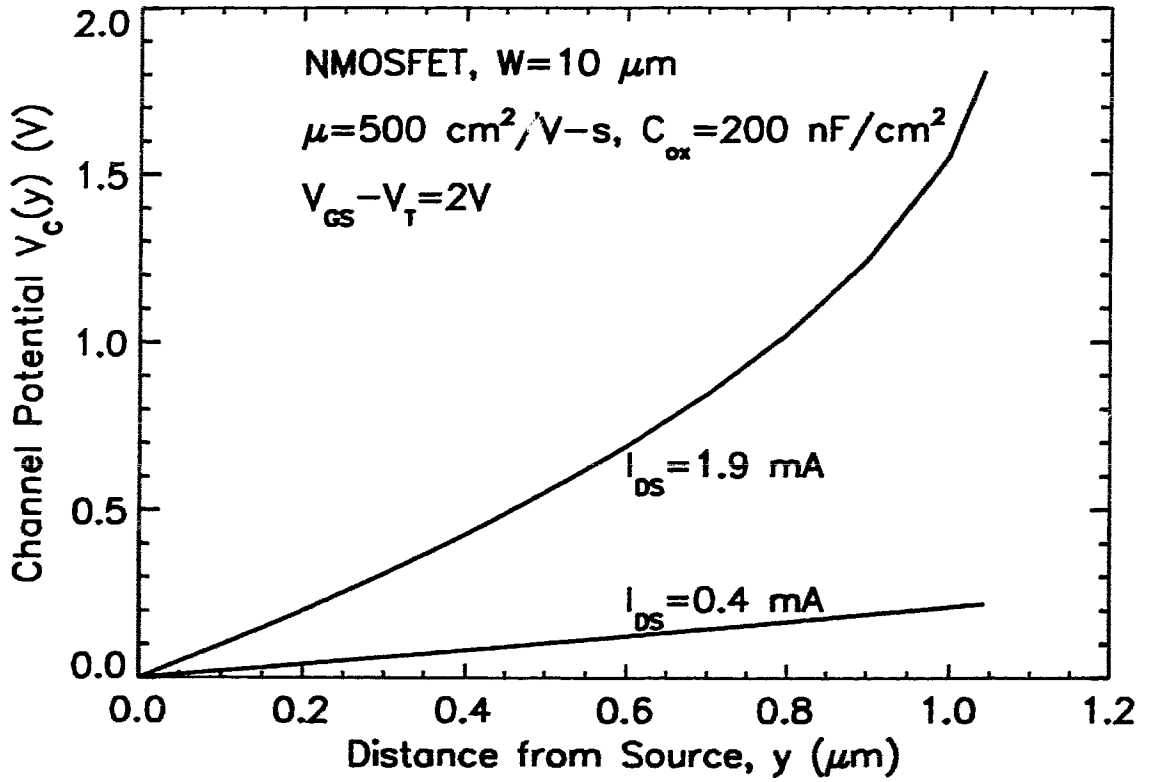

Fig. 2.2. Channel potential $V_C(y)$ versus distance y from source for two cases, linear operation of the MOSFET (I_{DS}=0.4 mA), and near saturation operation (I_{DS}=1.9 mA).

The above depiction of channel potential in two cases, corresponds to the following schematic (fig. 2.3) of the band bending along the channel. Also, the motion of electrons

as they traverse the channel and suffer successive collisions with phonons is shown schematically.

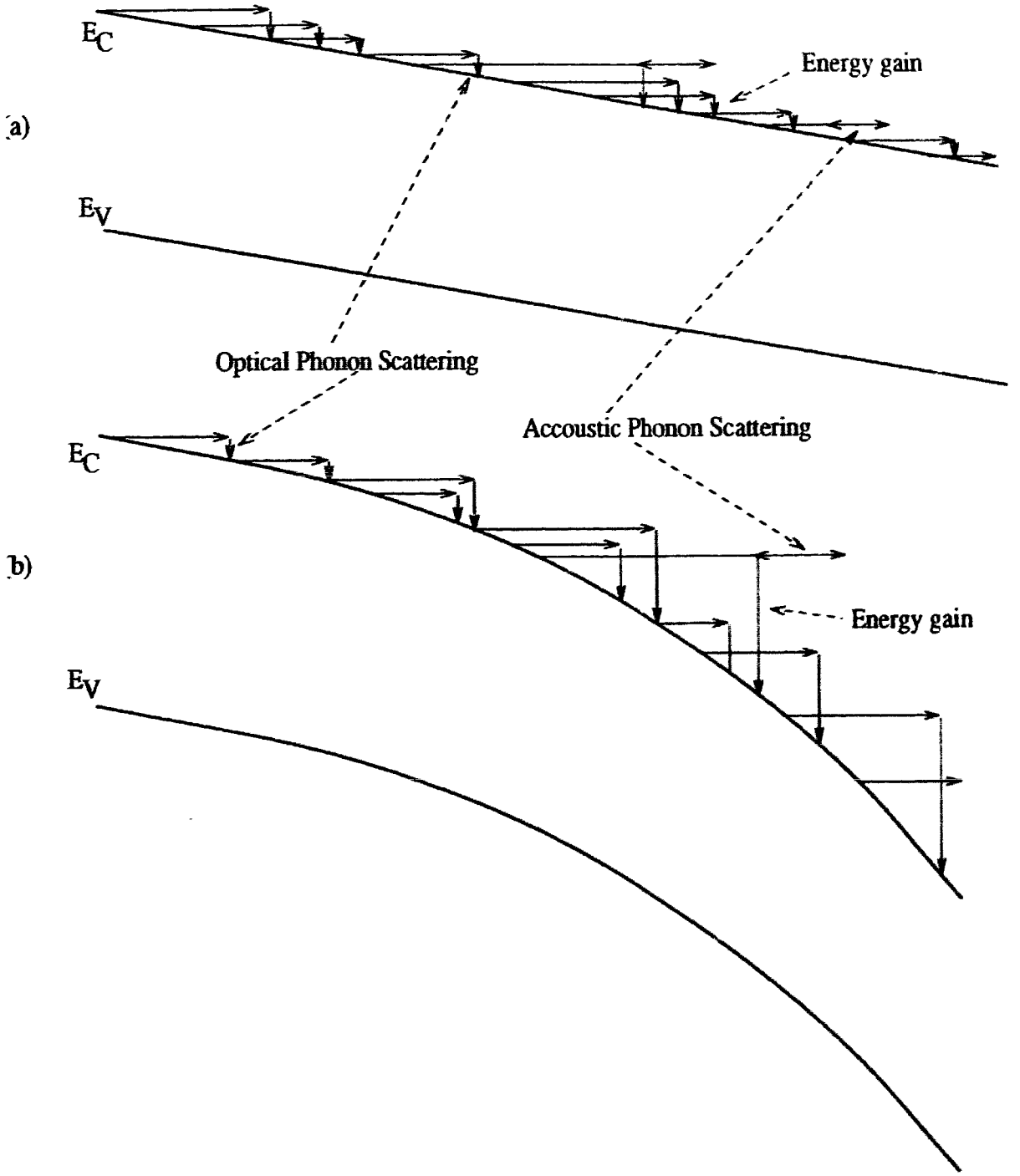

Fig. 2.3. Schematic showing energy loss in optical phonon scattering, and redirection by acoustic phonon scattering of electrons moving in the channel of an NMOSFET in two situations shown earlier in fig. 1.2, (a) linear operation of the MOSFET, and (b) near-saturation operation. Obviously, energy gain of the electron in the second case is higher due to curvature of the bands. These high-energy electrons are termed hot electrons.

In the first case, shown in fig. 2.3(a), the field is small. The electrons have to travel much longer to gain sufficient kinetic energy gain from the electric field. However, the probability of a long travel is cut short by an energy loss due to collision with an optical phonon. It should be mentioned here that the redirection of an electron through acoustic phonon scattering does not necessarily take place only in the direction shown (for convenience, we have assumed in fig. 2.3 that the vertical direction is the energy axis, and the horizontal direction is the space axis). In general, the redirection can be in any space direction. In effect, this type of scattering also serves to thwart the energy gain process of the electron. As a result of both types of scattering, the additional kinetic energy gained from the field is small compared to the thermal energy of the free carriers ($3k_BT/2$, k_B being the Boltzmann's constant). Hence, the electrons remain in near thermodynamic equilibrium with the lattice, and their velocity distribution follows the usual Maxwellian distribution. However, the electrons maintain a mean drift velocity (v_d) in the direction of the electric field and proportional to it through the mobility term μ, limited mainly by the acoustic phonon scattering.

In the second case, shown in fig. 2.3(b), however, the strong electric field enhances the curvature of the bands near the drain, and the energy gained between two collisions becomes significant, particularly near the drain. In this situation, the velocity v of a single electron of effective mass m_e can be much higher than the mean velocity v_d, and the electron can be considered to have a temperature T_e (normally, between 1000 and 10000 °K) much higher than the lattice temperature T, and given (conceptually) by,

$$\frac{3}{2}k_B T_e = \frac{m_e}{2}(v - v_d)^2. \qquad (2.6)$$

However, since we do not deal with single electrons in MOSFET channels, but rather with ensemble of electrons, the electron temperature T_e makes better sense as the width of an energy distribution (often assumed to be a Maxwellian distribution) of the electrons. A

higher value of electron temperature indicates a wider distribution, i.e., more electrons with higher energies, or more hot electrons. From the above discussion, it is clear that the hot carrier generation is directly related to the electric field near the drain.

Therefore, one of the ways to appreciate why the hot-carrier generation gets enhanced when the device is scaled would be to show that the maximum channel electric field near the drain in a saturated MOSFET increases with device scaling. This requires us to first note that the velocity of the hot carriers is mainly limited by optical phonon scattering, as opposed to acoustic phonon scattering in the case of "colder" carriers. Their velocity increases sub-linearly with the field and approaches a saturation velocity of about 10^7 cm/s beyond a certain high field ($E_{sat} \approx 10^5$ V/cm). This leads to saturation of the drain current even before the channel pinch-off discussed in section 2.2 for short channel devices. The corresponding $V_{DS,sat}$ has been modelled [2.3][2.6] as

$$V_{DS,sat} = \frac{E_{sat}L_{eff} \cdot (V_{GS} - V_T)}{(V_{GS} - V_T) + E_{sat}L_{eff}} . \tag{2.7}$$

Also, the maximum channel electric field E_m near the drain has been modelled [2.3] as

$$E_m = \frac{(V_{DS} - V_{DS,sat})}{0.22T_{ox}^{1/3}X_j^{1/2}} , \tag{2.8}$$

where T_{ox} and X_j are respectively the oxide thickness and source-drain junction depth of the MOSFET in centimeters. In a constant voltage scaling scheme [2.7] pursued widely for the MOSFET, T_{ox} and X_j values are scaled in the same proportion as the channel length, but the supply voltage V_{DS} and the threshold voltage V_T remain fixed. Under this scheme, therefore, one can plot E_m versus progressively decreasing effective channel length L_{eff} as shown below in fig. 2.4. The rapid rise in E_m for shorter channel lengths is evident. The only mitigating factor is the decrease in the number of scattering events for channel lengths shorter than 0.15 μm [2.8]. This decrease in the number of scattering

events reduces the spread of the electron energy distribution, and hence slightly reduces the electron temperature T_e. Also, the constant voltage scaling scheme used for plotting fig. 2.4 gives a worst-case estimate of the impact of scaling on E_m, since the supply voltage V_{DS} is actually reduced somewhat with scaling. Nevertheless, hot carrier generation remains a major issue in the sub-micron NMOSFET devices. In contrast, the

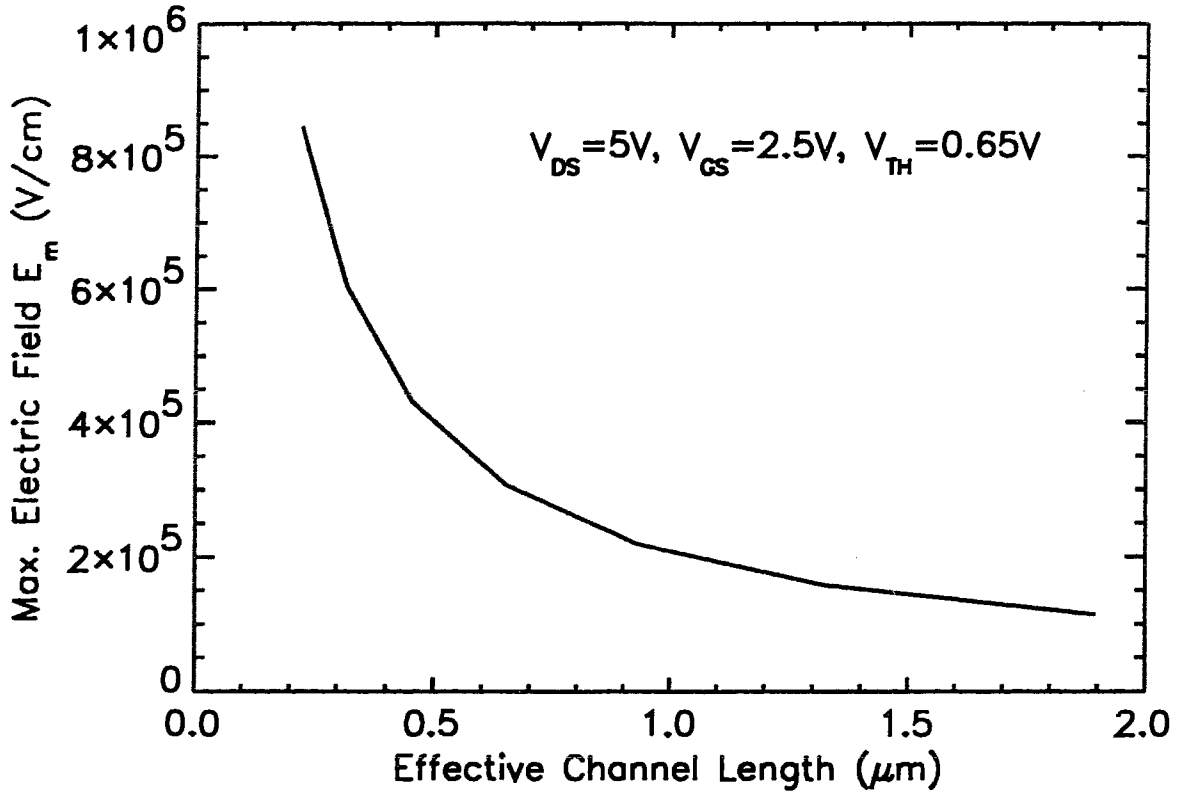

Fig. 2.4. Impact of constant-voltage scaling on the maximum channel electric field E_m.

carriers in PMOSFET devices are much cooler due to a much smaller value of λ (~1 nm) for holes in these devices.

2.4 Effects of hot carrier generation

These hot electrons cause two important phenomena. First, electrons that acquire an energy (~1.3 eV) [2.5] can create an electron-hole pair by impact ionization. The generated holes are mostly collected at the substrate as a measurable substrate current, I_B, and the generated electrons move on to be collected at the drain. Secondly, if the electrons

get sufficiently energetic to surmount the silicon-silicon dioxide band offset (~3.2 eV) they will tend to do so, giving rise to an injection current I_E. However, they will actually succeed in reaching the gate only if the injected electrons are not scattered back by a repelling gate bias. This current of electrons can actually be measured in a MOSFET as the gate current I_G and it reaches its maximum value for biases $V_{GS} \cong V_{DS}$. On the other hand, both I_B and I_E tend to maximize near $V_{GS} \cong V_{DS}/2$. If V_{GS} is too low, there are very few electrons in the channel to cause impact ionizations, or to get injected into the oxide. Again, if V_{GS} is close to V_{DS}, the transistor tends towards the linear operation and the lateral electric field in the pinchoff region decreases, leading to "colder" electrons. While I_B and I_G can be directly measured, I_E can be simulated [2.9] or measured with a special split gate structure [2.10], where an additional gate biased at a potential much higher than V_{DS} is interposed between the regular gate and the drain to collect the injection current. The nature of the currents I_E and I_G [2.9] is schematically shown in fig. 2.5 below. Some of the holes generated by impact ionization may be sufficiently energetic to get injected into the oxide. But they are far less efficient than electrons because they face a much higher S-SiO_2 band offset (~4.8 eV). That is the reason they have been neglected in the above diagram.

Figure 2.5 also shows the normal measurement modes for I_B and I_G, the two frequently monitored hot-carrier currents. That is, the drain bias is held constant and the gate bias is swept. The similarity in the shapes of I_B and I_E suggests that if we monitor I_B we can get a fair estimate of the electron injection (I_E) which is mainly responsible for long term device degradation. On the other hand, I_G is a direct indicator of the electron injection process. Some of the injected electrons remain trapped in the oxide to produce negative oxide charge, and others break interfacial Si-O bonds to produce interface traps. Both types of defects accumulate over time and give rise to the degradation of the MOSFET's *I-V* characteristics, and hence the performance of circuits in which the MOSFETs are used.

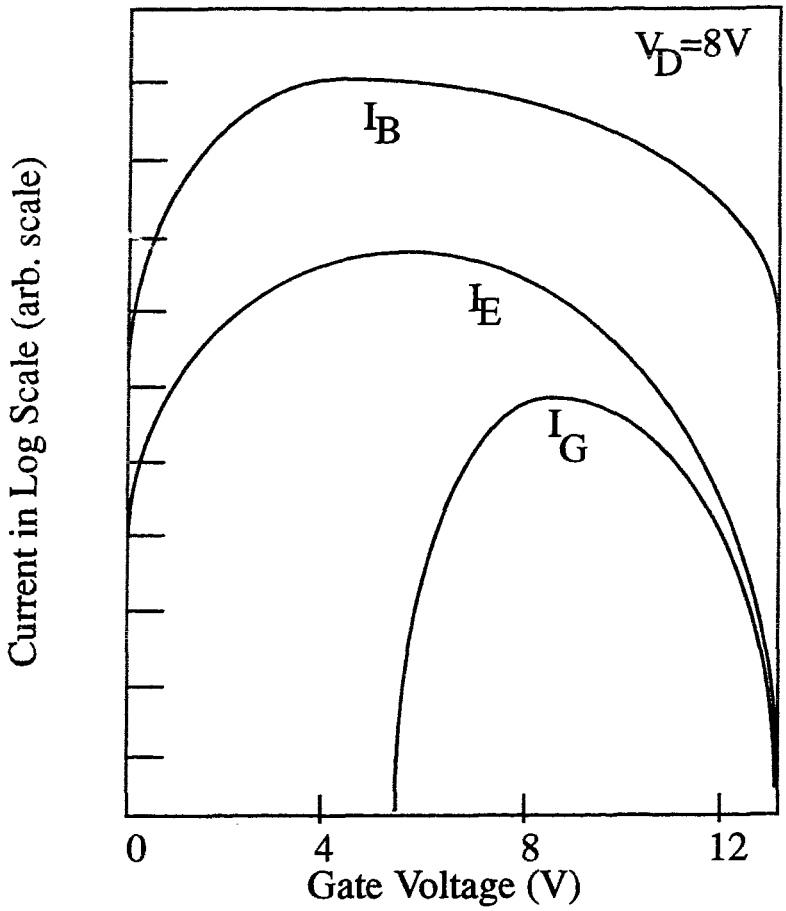

Fig. 2.5. Schematic diagram of the electron injection current I_E, and the actual gate current I_G.

Time dependent degradation effects of hot carrier generation is the main concern of this thesis. However, it should be mentioned here that the hot carrier induced substrate current I_B itself can cause an undesirable effect in CMOS (Complementary MOS, where NMOSFET and PMOSFET devices are used together) circuits, namely latchup [2.11]. In a latchup situation, a low resistance path between the supply voltage and ground is established, leading to circuit failure. Transistor parameters that are usually monitored over hot-carrier stress times in conventional MOSFETs are linear current (I_D) at a specific gate bias, linear transconductance (g_m), threshold voltage (V_T), and subthreshold slope (S) measured in mV/decade for the drain current that varies exponentially with gate bias below the threshold voltage V_T. It has been shown that the shifts in these parameters are

directly correlated, and that they follow a t^n dependence on stress time, with n varying between 0.5 and 0.75 for a conventional MOSFET. In figure 2.6, the effects of hot carrier generation have been schematically summarized.

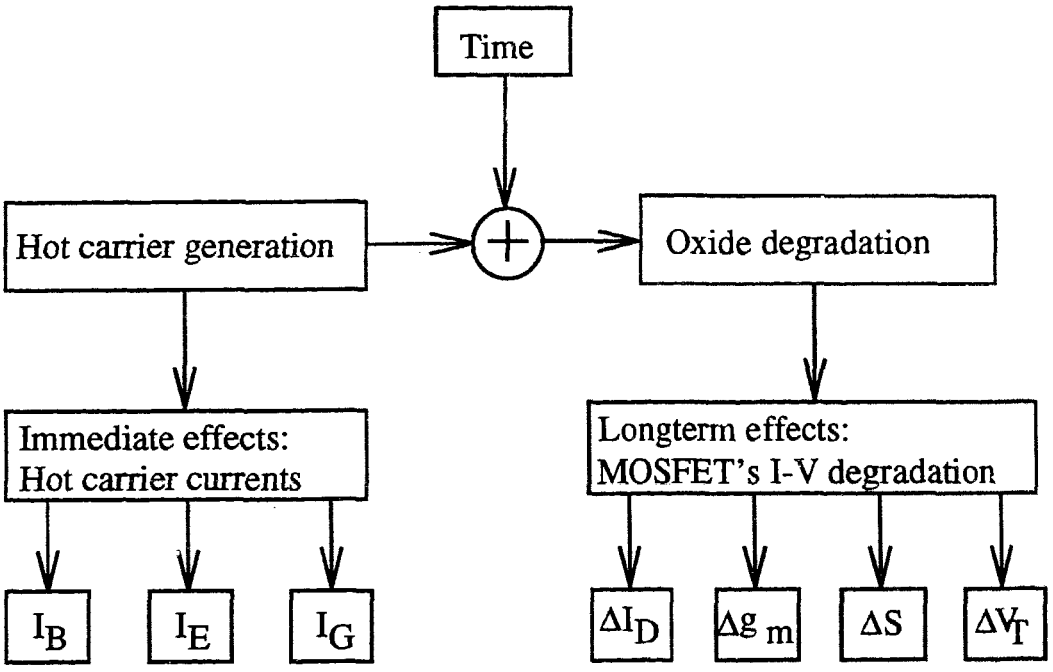

Fig. 2.6. Schematic diagram of the effects of hot carrier generation.

2.5 Modeling of hot carrier currents and degradation

Three different approaches have been tried to model the hot carrier currents in MOSFETs. They are

(1) an analytical approach [2.12] [2.13] [2.5] based on an approximate formulation of the local electric field near the drain such as the eqn. (2.8),

(2) a numerical approach [2.14] that uses either electric fields or electron temperatures obtained from numerically solving the drift diffusion equations [2.14] alone or drift diffusion plus energy balance equations [2.15] on a MOSFET structure, and

(3) a Monte-Carlo approach [2.16] that traces the electrons individually during their motion in the MOSFET, and take into account their interactions with the electric field and phonons.

The Monte-Carlo approach is the most accurate method to look at the hot carrier currents. However, it is also the most computer-time intensive. It has been suggested [2.17] that this method is most appropriate for very short channel lengths (below ~0.15 μm). Since the geometries used in our work are much larger (0.8 μm drawn gate length), we have used a combination of the first and the second approaches for our work. While the numerical approach (as used in the 2-D device simulator MEDICI [2.18] in our case) serves as the most important tool in our work, and as a benchmark in many situations, the simplified analytical approach, popularly known as the lucky electron model, is more instructive for a physical picture. We therefore defer the discussion of the models used in our 2-D simulations to Appendix 1.

The analytical approach based on the lucky electron model is a useful tool to broadly understand the physical processes involved in the production of the two major hot-carrier induced currents, namely, I_B and I_G, and the interface traps N_{it} which is the most important hot carrier degradation species. The interface traps, when filled with electrons give rise to negative interface charge that cause the measurable changes in linear current (I_D) at a specific gate bias, linear transconductance (g_m), threshold voltage (V_T), and subthreshold slope (S), as mentioned before. The interface traps can be directly measured as charge pumping current I_{CP} [2.19], and is often a recommended parameter [2.20] to study in hot carrier life time experiments.

In the lucky electron approach, a hot electron (or hole), in order to produce an impact ionization event, or get injected over the oxide-silicon barrier, it must acquire characteristic energies Φ_i and Φ_b respectively. In order to acquire an energy of Φ_i eV, for example, an electron must travel a distance of Φ_i / qE_m in the electric field E_m given by

eqn. (2.8) without a lossy collision. Considering the mean free path λ for a lossy collision, the probability that the electron does not suffer an energy losing collision before acquiring an energy of Φ_i eV is $\exp(-\Phi_i/q\lambda E_m)$. Since, I_{DS} is the rate of supply of cold electrons, the substrate and gate currents are modelled using the following equations (2.9) and (2.10). In following equations Φ_i =1.3 eV [2.21], and Φ_b which is, strictly speaking, a function of the vertical electric field E_{ox} that induces some image force barrier lowering, can be approximated by 3.2 eV.

$$I_B = C_1 I_{DS} exp\left(-\frac{\Phi_i}{q\lambda E_m}\right), \tag{2.9}$$

$$I_G = C_2 I_{DS} exp\left(-\frac{\Phi_b}{q\lambda E_m}\right). \tag{2.10}$$

In the above two equations, $C_1 \cong 2$, and $\cong 2\text{x}10^{-3}$ for $V_{GS} \geq V_{DS}$. For $V_{GS} < V_{DS}$, C_2 is set equal to 0, because the electrons are scattered back to silicon by an opposing electric field in the oxide. The growth rate of interface traps (N_{it}) has been modelled [2.21] as,

$$\Delta N_{it} = C_3 \left(t \frac{I_{DS}}{W} exp\left(\frac{-\Phi_{it}}{q\lambda E_m}\right)\right)^n , \tag{2.11}$$

where, Φ_{it} is the characteristic energy (~3.7 eV) for interface trap creation. The above eqn. (2.11) is an important relation in the engineering analysis of the hot carrier lifetimes. Essentially, it states that the current degradation is proportional to t^n for conventional MOSFET devices. The value of n (normally between 0.5 and 0.75) can be easily determined by plotting ΔI_{CP} vs. hot carrier stress time on a log-log graph and computing the slope of the resulting straight line. Such parameters as $\Delta I_{DS}/I_{DS}$, $\Delta g_m/g_m$, ΔV_T, and ΔS can also be plotted in place of ΔI_{CP}, because they all have the same dependence on stress time. Stressing is normally performed at the maximum I_B-biasing situation for a particular drain bias (see fig. 2.5). The lifetime (τ) of a device is often defined as the time at which

the ΔI_{CP}=30 pA, or $\Delta I_{DS}/I_{DS}$=10% under d.c. stress. This corresponds to a particular constant value of ΔN_{it}. Hence, by combining (2.9) and (2.11), we get for a constant ΔN_{it}, that

$$\frac{\tau I_{DS}}{W} \propto \left(\frac{I_B}{I_{DS}}\right)^{-\Phi_{it}/\Phi_i} \quad . \tag{2.12}$$

or, more explicitly,

$$\tau = CW\,[\Delta I_{CP}]^{\frac{1}{n}} / (I_B^m / I_{DS}^{m-1}) \quad . \tag{2.13}$$

where m=(Φ_{it}/Φ_i) can be obtained from plotting τ versus I_B on a log-log graph at a constant I_{DS} for a particular value of ΔI_{CP} (e.g., 30 pA) or $\Delta I_{DS}/I_{DS}$ (e.g., 10%). The constant I_{DS} situation is achieved by varying V_{DS} in the flat saturation region of the drain current. In this situation, only I_B changes, but I_{DS} remains fixed. The value of m is also obtained by plotting (τI_{DS}/W) versus (I_B/I_{DS}) as in eqn. (2.12). In this case, one can vary V_{DS} and V_{GS} more freely while choosing a bias combination for stressing till ΔI_{CP} for a particular τ. The value of C in eqn. (2.13) can be obtained easily by solving for a known combination of τ, I_B, and I_{DS}. Knowing C, n, and m as above, eqn. (2.13) can be regarded as a master expression for lifetime estimation under any d.c. stressing situations, that is, any combination of I_B and I_{DS}. In the case of dynamic stressing (real circuit situation), it has been shown [2.22] that the total degradation is roughly equal to the integrated sum of the bits of degradation under individual pulses of stress. Thus, knowing the time varying I_B and I_{DS} for a single pulse cycle, one can integrate the denominator of (2.13) over the pulse time period and divide by the pulse time period to normalize.

2.6 The LDD structure and the associated problem

The picture given so far is valid for a conventional heavily doped source/drain MOSFET structure. However, in order to improve the long term reliability of the device, the lightly doped drain (LDD) device structure [2.23] (see fig. 2.7) has been widely used in the industry for submicron devices. The great advantage of the LDD structure has been in reducing the peak lateral electric field (E_m) near the drain by introducing a lighter doped (n^-) extension region between the heavily doped drain/source and the channel as shown in fig. 2.7. The n^- regions are first implanted, followed by the implantation of the n^+ regions that are spaced with the help of the spacer oxide mask. Now, the peak lateral electric field

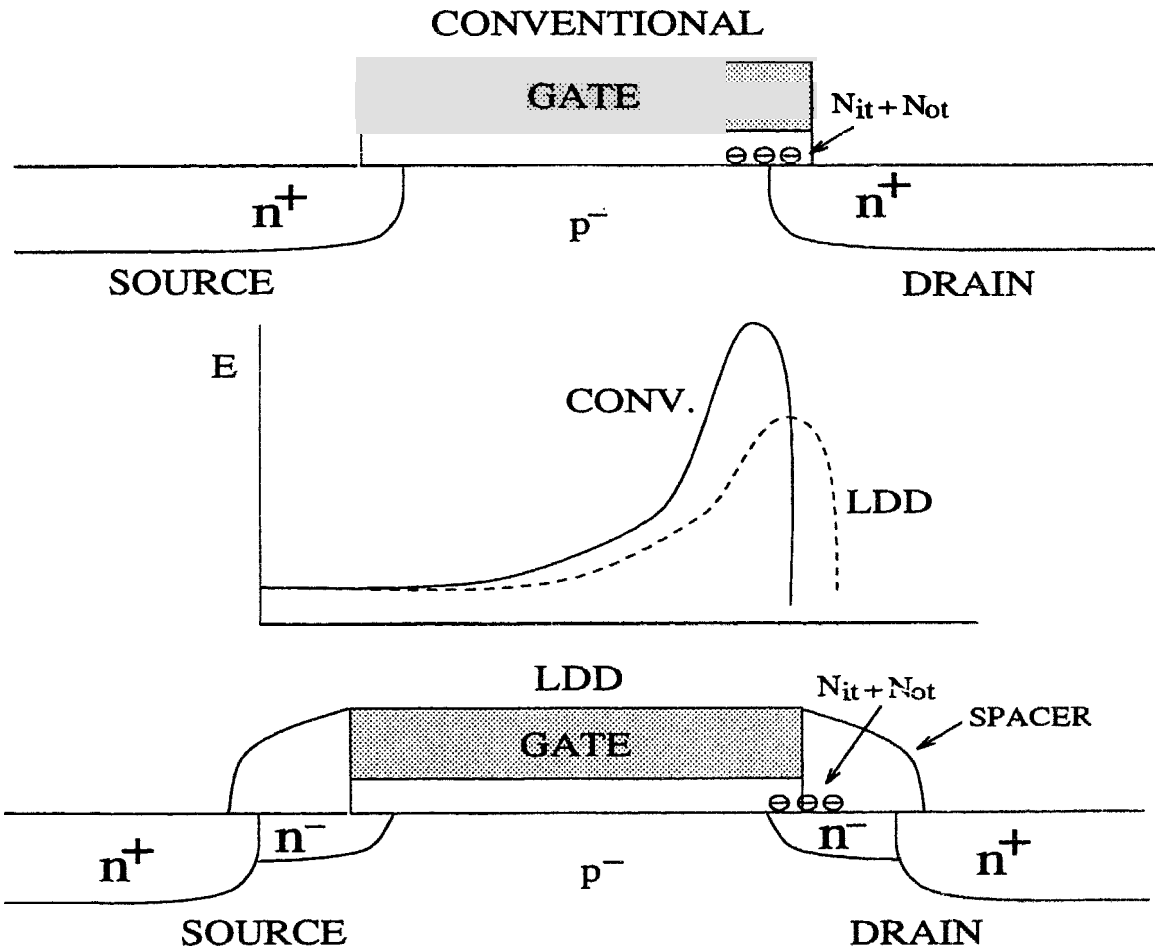

Fig. 2.7. Comparison between the conventional and the LDD structures, corresponding lateral electric fields, and degradation modes.

not only decreases in magnitude, but also shifts in position - it moves outwards, shifting the position of the hot carrier defects, i.e., the charged interface traps (N_{it}) and oxide traps

(N_{ot}). While the LDD structure serves to reduce the substrate and the gate currents due to the reduction in E_m, the degradation mode changes considerably, with respect to a conventional structure. This is due to two reasons.

(1) The degradation species are produced in the weak gate edge region and the spacer oxide region which is normally a poorer quality deposited oxide than the thermally grown gate oxide, and

(2) the LDD region has lower doping concentration than the heavily doped n+ region, and, therefore, can be easily depleted by the negative trapped charges, giving rise to a fast increase in the drain parasitic resistance. This gives rise to a fast early mode of the current degradation, followed by a slower saturating degradation [2.24-2.28]. This is unlike the single t^n type degradation behavior exhibited by conventional devices, and as modelled by eqn. (2.11).

In spite of the above-mentioned effort in this direction, there was no strong physical basis for the saturating nature of the hot-carrier degradation in the case of LDD NMOSFETs. One of the main problems has been the lack of simple experimental methods to study the degradation species (interface traps and oxide traps) in the gate edge region and their growth with time. Recently, some efforts [2.29] [2.30] [2.31] have been directed towards extracting oxide trapped charge and interface trap information in the gate overlapped drain region through measurements of gated-drain-diode tunnel currents or charge pumping currents. But there is no technique to extract this information in the sub-spacer region near the gate-edge. Therefore, 2-D device simulation needs to be used to obtain information about defects in this region.

Another important feature of the LDD structure is the increased importance of the source and drain parasitic resistances (R_S and R_D) due to the lightly doped n^- regions. They not only reduce the current drive capability of the transistor, but they tend to become

asymmetric due to processing (e.g., implant shadowing effect) or hot carrier stressing that affects the drain side only. Therefore, it is important to extract them separately in order to study the effect of hot-carrier degradation on them.

We therefore recognized that these resistances, once extracted separately, offer us a means to study the effects of charges generated in the sub-spacer region. If we could couple the evolution of R_D with other measurements and 2-D device simulations, we would be able to build up a physical basis for the saturating nature of the degradation in the case of LDD NMOSFETs. This was the main motivation for the work to be discussed in the following chapters.

We had another concern that arose from the circuit effect of the hot-carrier degradation as evident from the following fig. 2.8. The frequency degradation of an experimental 59-stage CMOS ring oscillator using our transistors is shown here. In order

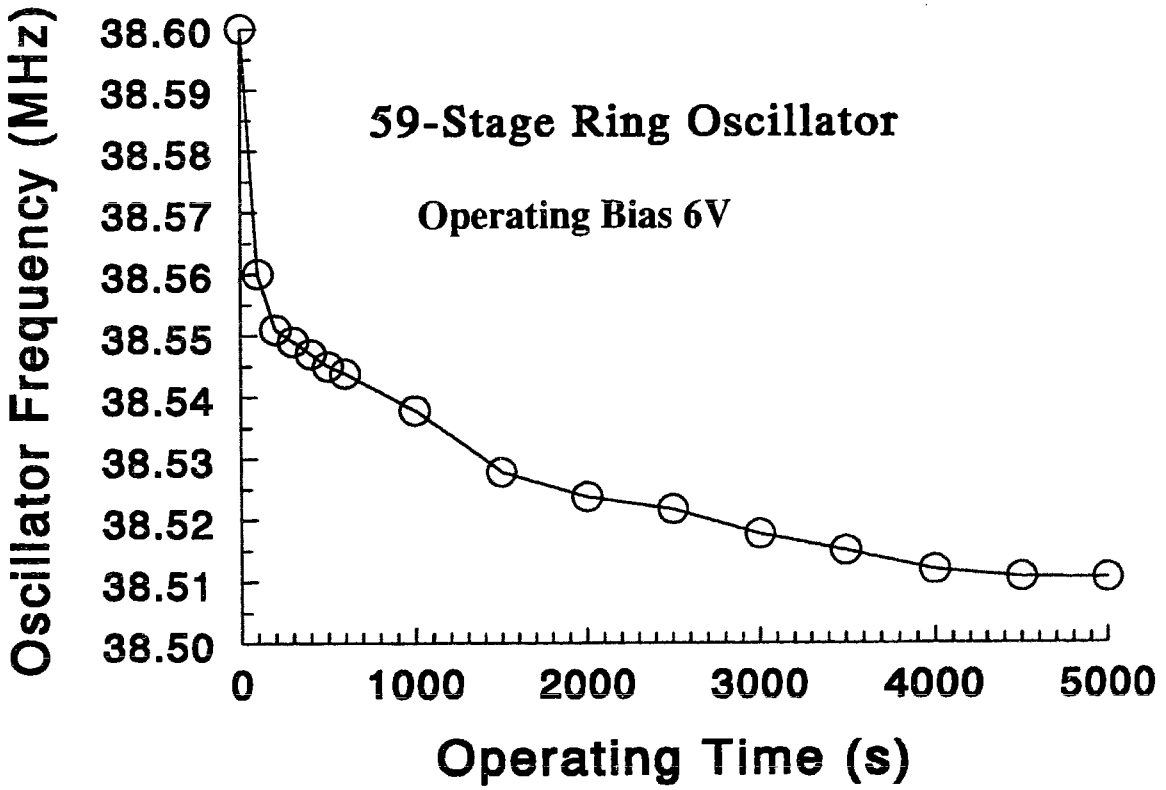

Fig. 2.8. Early mode hot-carrier degradation affecting the frequency of oscillation in a 59-stage ring oscillator built with 0.8 mm LDD NMOSFETs.

to predict the performance of a circuit such as above we need to simulate the circuit with updated SPICE parameters. We therefore need a simple but accurate method to extract the "degraded" parameters of a transistor under hot-carrier stress. This motivated the work reported later in chapter 6 of this thesis.

2.7 Conclusion

In this chapter, we have attempted to provide a *brief* background of the particular aspect of hot-carrier problem that this thesis proposes to tackle. It must be mentioned here that the volume of work that has been published on the issue of hot-carrier effects is enormous. Therefore, we had to be selective in choosing the references. The main purpose of this chapter was to present a motivation and introductory framework for the research to be discussed in the chapters that follow.

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Chapter 3

Finding the asymmetric parasitic source and drain resistances from the small-signal conductances of a single MOS transistor

3.1 Introduction

For submicron MOSFETs, the source and drain parasitic resistances (R_S and R_D respectively) can be comparable with the intrinsic device resistances. As such, they start playing a more important role in degrading the current drive capabilities of the device. Also, any asymmetry in their values arising out of layout, process, or electrical stressing shows up more clearly in their asymmetric performance when the roles of the source and the drain are interchanged. It is therefore important to accurately extract the source and drain parasitic resistances separately. However, the conventional method discussed in [3.1] and the methods reviewed in [3.2] are unsuitable for this purpose for two reasons. First, they all extract only the sum of the source and drain resistances assuming them to be equal; and second, they depend on measurements on more than one transistor with different geometries [3.3], each of which is assumed to have exactly similar situation in terms of layout, processing, and electrical stressing. While it is often possible to ensure uniformity in layout, it is difficult to ensure zero asymmetry in source and drain resistances due to processing; and it is impossible to control the evolution of these resistances under situations where devices are electrically stressed. We therefore need a method that extracts these resistances using a single transistor only.

Earlier efforts [3.4],[3.5] in this direction suffer from questionable extrapolation of the analysis to either high gate biases [3.4] or zero drain bias [3.5], and the undesirable requirement of prior knowledge of threshold voltage. Also, the authors of the more recent

paper [3.4] found their extrapolation inappropriate for very short transistors. In this chapter, we will discuss a simple and robust method to extract these resistances separately using a single short channel transistor. Rather than using the static resistances of MOSFETs like most authors, we will use the dynamic trans- (g_m) and drain-conductances (g_d) as the measured parameters for the MOSFET. The choice of these parameters makes our method more direct and straight forward without requiring any extrapolation, human judgement, or prior knowledge of threshold voltage. In fact the threshold voltage is obtained as a by-product. In this chapter, we first derive the generalized trans- and drain-conductance relations used for the extraction. We then describe our method to extract the difference of the parasitic resistances (R_D-R_S) from the saturation region [3.9] and then their sum (R_S+R_D) from the linear region [3.12], so that each resistance can be found separately. We finally discuss the accuracy of the method [3.12], [3.13]. We will also show, how this extraction technique allows us to predict and show a logarithmic dependence of R_S and R_D on gate bias V_{GS}.

3.2 Derivation for g_m and g_d

Referring to fig. 3.1 below we first note that

$$I_{DS} = f(V_{GS}', V_{DS}', V_{SB}') \text{ and}$$
$$I_{DS} = f(V_{GS}, V_{DS}). \tag{3.1}$$

We also note that

$$V_{GS}' = V_{GS} - I_{DS}R_S, \quad V_{DS}' = V_{DS} - I_{DS}(R_S + R_D)$$
$$V_{SB}' = I_{DS}R_S. \tag{3.2}$$

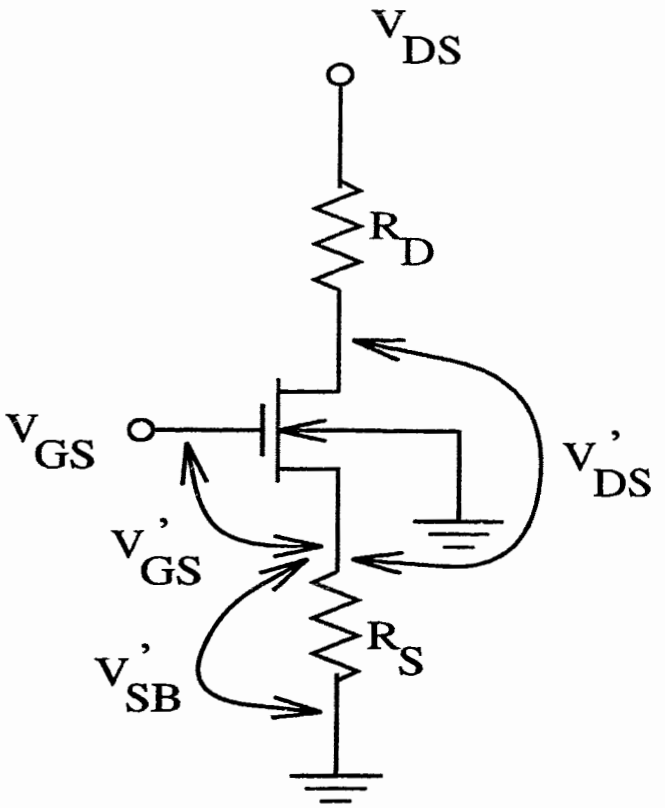

Fig. 3.1. The MOSFET (n-channel) with source (R_S) and drain (R_D) series resistances. The applied voltages (V_{GS} and V_{DS}) and the intrinsic voltage drops (V_{GS}', V_{DS}', and V_{SB}') are also indicated.

We then define the conductances with respect to gate (*m*), drain (*d*), and substrate (*b*). First, the intrinsic (0) conductances are given by,

$$g_{m0} = \left.\frac{dI_{DS}}{dV_{GS}'}\right|_{V_{DS}', V_{SB}'}, \quad g_{d0} = \left.\frac{dI_{DS}}{dV_{DS}'}\right|_{V_{GS}', V_{SB}'}, \quad -g_{b0} = \left.\frac{dI_{DS}}{dV_{SB}'}\right|_{V_{GS}', V_{DS}'} \tag{3.3}$$

and, then the measured ones by,

$$g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}}, \quad g_d = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{GS}}. \tag{3.4}$$

Now, using calculus on (3.1), we may equate the incremental change in I_{DS} to those in V_{GS}', V_{DS}', and V_{SB}', given by (3.2) as follows,

$$\begin{aligned}\Delta I_{DS} &= \frac{\partial}{\partial V_{DS}} I_{DS} \cdot \Delta V_{DS}' + \frac{\partial}{\partial V_{GS}} I_{DS} \cdot \Delta V_{GS}' + \frac{\partial}{\partial V_{SB}} I_{DS} \cdot \Delta V_{SB}' \\ &= g_{d0}\Delta\left[V_{DS} - I_{DS}(R_S + R_D)\right] + g_{m0}\Delta\left[V_{GS} - I_{DS}R_S\right] \\ &\qquad -g_{b0}\Delta\left(I_{DS}R_S\right) \\ &= g_{d0}\Delta V_{DS} - g_{d0}\Delta I_{DS}(R_S + R_D) - g_{d0}I_{DS}\Delta(R_S + R_D) + \\ &\qquad g_{m0}\Delta V_{GS} - g_{m0}\Delta I_{DS}R_S - g_{b0}\Delta I_{DS}R_S - g_{b0}I_{DS}\Delta R_S.\end{aligned} \tag{3.5}$$

We now find g_m and g_d from (3.5). In order to find g_m, we simply divide both sides of (3.5) by ΔV_{GS} and making ΔV_{DS} equal to zero everywhere. Thus, using the definition of g_m given in (3.4) and letting ΔV_{GS} become infinitesimally small, we evaluate, after transpositions,

$$g_m = \frac{g_{m0}\left[1 - \left(1 + \frac{g_{b0}}{g_{m0}}\right) I_{DS}R_{Sm} - \frac{g_{d0}}{g_{m0}} I_{DS}(R_{Sm} + R_{Dm})\right]}{1 + (g_{m0} + g_{b0})R_S + g_{d0}(R_S + R_D)} \tag{3.6}$$

where R_{Sm} and R_{Dm} are given as,

$$R_{Sm} = \left.\frac{dR_S}{dV_{GS}}\right|_{V_{DS}} \qquad R_{Dm} = \left.\frac{dR_D}{dV_{GS}}\right|_{V_{DS}}. \tag{3.7}$$

As I_{DS} is normally small, a few milliamperes or less, and also if we neglect the gate bias dependence of R_S and R_D, we can approximate (3.6) as [3.14],

$$g_m = \frac{g_{m0}}{1 + (g_{m0} + g_{b0}) R_S + g_{d0} (R_S + R_D)}. \tag{3.8}$$

Since, g_{b0} is a small fraction (~0.1) of g_{m0}, and g_{d0} is negligible with respect to g_{m0} in saturation, the equation (3.8) above is a very accurate approximation in saturation. Originally, the authors of [3.6] had not considered the effect of g_{b0} at all in deriving the relation for g_m.

However, in the linear region, since g_{d0}/g_{m0} can be large, the third term in the numerator of (3.6) may not be negligible if R_{Sm} and R_{dm} are not very small. We will come to this discussion later in the chapter.

In a similar way, we can derive the expression for g_d from (3.5) by simply dividing both sides of (3.5) by ΔV_{DS} and putting ΔV_{GS} to zero everywhere. In this case, if we neglect the drain bias dependence of R_S and R_D. We thus get g_d as [3.14]

$$g_d = \frac{g_{d0}}{1 + (g_{m0} + g_{b0}) R_S + g_{d0} (R_S + R_D)}. \tag{3.9}$$

The above expression for g_d (3.9) is an accurate approximation in all regions of operation since the drain bias dependence of R_S and R_D is nominally negligible.

3.3 Methodology of extraction: R_D-R_S from saturation

In saturation, as g_{d0} is normally negligible compared to (g_{m0}+g_{b0}) the sum of R_S and R_D as it occurs in the third term of the denominator of eqn. (3.8) has little effect on the measured g_m. As such the measured value of g_m is sensitive to only R_S. Now, if the source and drain are interchanged, the measured value of g_m is sensitive to only R_D. Hence any asymmetry in R_S and R_D is most likely to show up in the measured g_m values. Therefore, the I_{DS} vs. V_{GS} characteristics in saturation is measured normally, and again with the

source and drain interchanged. In fig. 4.2, we show these saturation I_{DS} vs. V_{GS} characteristics for an LDD NMOSFET of channel length 0.8 μm (as drawn) and channel width 24 μm.

This MOSFET had asymmetric layout with the source side interconnection to the pad much longer than that on the drain side. The oxide thickness of the MOSFET measured was 175 Å, the LDD phosphorus implant dose was $2x10^{13}$ cm^{-2} at 40 keV, followed by a drive cycle at 900 °C in a combination of dry O_2 and N_2 ambients for about 70 minutes. The MOSFET had salicided arsenic-implanted source/drain regions.

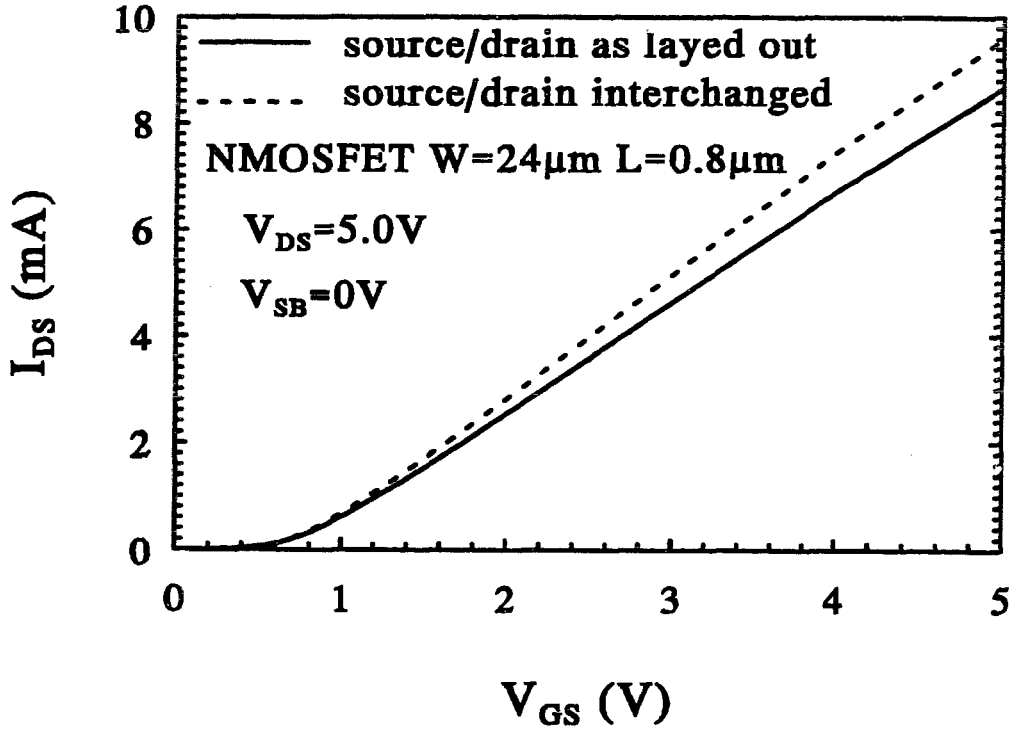

Fig. 3.2. Saturation transconductance characteristics of the MOSFET with V_{DS}=5V. The asymmetry in R_S and R_D translates directly into these characteristics with source/drain as laid out and as interchanged. In this case R_S is greater than R_D.

Now, one of the ways [3.5] to find R_D-R_S from these two characteristics is to place external resistances in series with the source or the drain (whichever side has lower resistance) and try to equate the two characteristics. The value of the external resistance

for which the two characteristics become equal gives (R_D-R_S). However, while this method is easy, the results largely depend on the judgement of the observer, and as such they are prone to errors. We have therefore worked out a more direct and robust method to find out R_D-R_S from equation (3.8) above, and use the above-discussed technique of equating the two characteristics as a verification of the method. Our method to find R_D-R_S from the saturation I_{DS} vs. V_{GS} characteristics is as follows

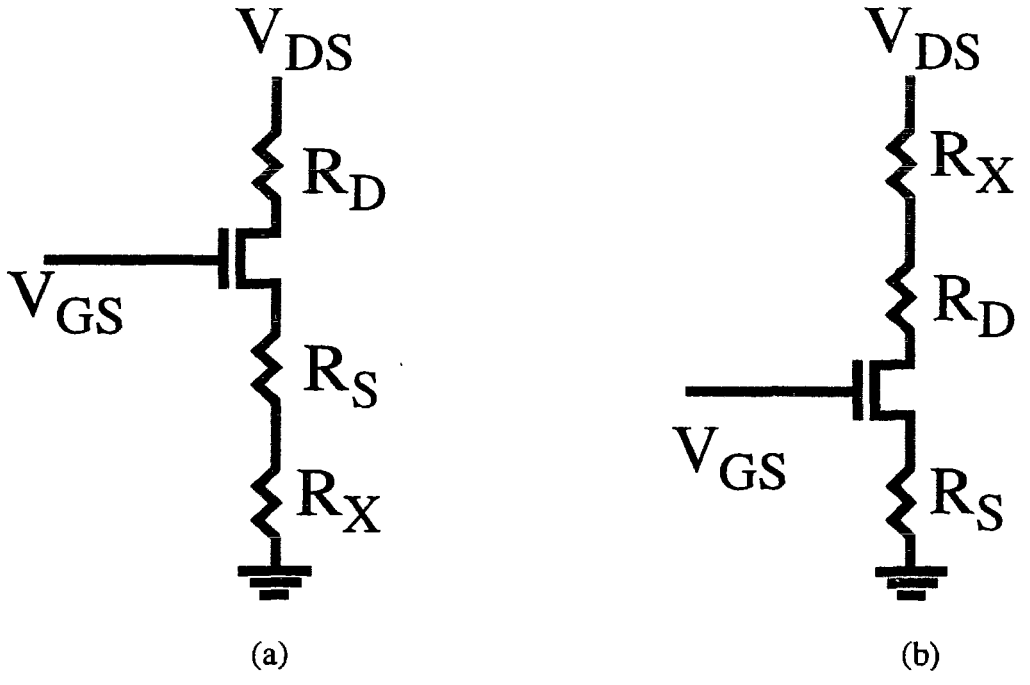

Fig. 3.3. (a) Add R_X to Source, measure g_m, call it g_{mS}. (b) Add R_X to Drain, measure g_m, call it g_{mD}. Both g_{mS} and g_{mD} are measured in forward mode at constant I_{DS}.

As shown in fig. 3.3, if we intentionally add external resistances (R_X) to the source side and measure the transconductance g_{mS} (measured straight, i.e. source and drain not interchanged), it should be given (using eqn. (3.8) above) by

$$\frac{1}{g_{mS}} = \frac{1}{g_{m0}} + R_S\left[1 + \frac{g_{b0}}{g_{m0}}\right] + \frac{g_{d0}}{g_{m0}}(R_S + R_D) + R_X\left[1 + \frac{g_{b0}}{g_{m0}} + \frac{g_{d0}}{g_{m0}}\right]. \quad (3.10)$$

On the other hand, if we intentionally add external resistances (R_X) to the drain side and measure the transconductance g_{mD} (measured straight, i.e. source and drain not interchanged), it should be given (using eqn.(3.8) above) by,

$$\frac{1}{g_{mD}} = \frac{1}{g_{m0}} + R_S\left[1 + \frac{g_{b0}}{g_{m0}}\right] + \frac{g_{d0}}{g_{m0}}(R_S + R_D) + R_X\left[\frac{g_{d0}}{g_{m0}}\right]. \quad (3.11)$$

If for different values of R_X, g_{mS} and g_{mD} are measured in <u>saturation</u> for a constant current I_{DS}, we can assume g_{m0}, g_{d0}, and g_{b0} to be roughly constant because,

$$g_{m0} \;\alpha\; \sqrt{I_{DS}} \qquad \text{and} \qquad g_{d0} \;\alpha\; \lambda I_{DS} \quad (3.12)$$

where $1/\lambda$ is the Early voltage. Also

$$g_{b0} \;\alpha\; \frac{1}{\sqrt{I_{DS}[R_S + R_X] + 2\Phi_F}} \quad (3.13)$$

where Φ_F represents the Fermi potential corresponding to the substrate doping concentration. For small I_{DS}, g_{b0} represents a very slowly varying function of R_X for low R_X (<100 Ω). The above assumptions are justified when we plot $1/g_{mS}$ and $1/g_{mD}$ (measured at a constant saturation I_{DS} of 3 mA in our case) as in eqns. (3.10) and (3.11) versus R_X, and obtain two straight lines with the same intercept (~480 Ohms) as in figure 3.4.

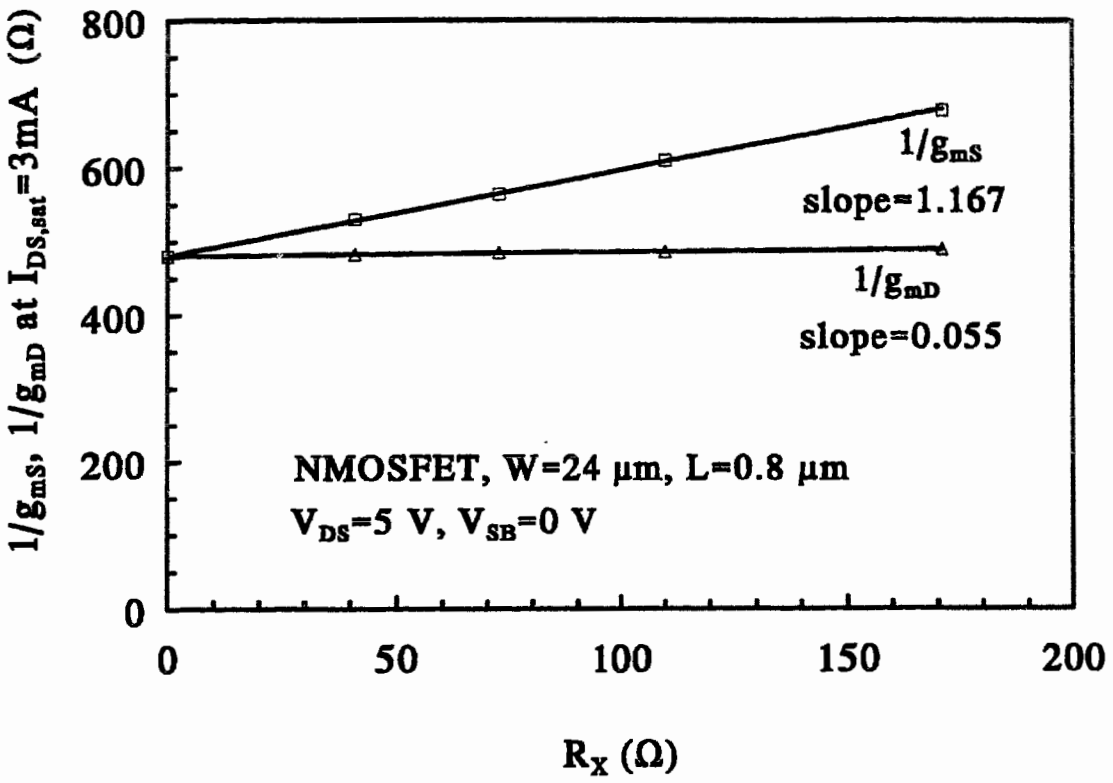

Fig. 3.4. $1/g_{mS}$ and $1/g_{mD}$ measured at saturation I_{DS} of 3mA versus R_X. The straight lines through the points are least-squares fitted. g_{mS} is g_m measured with R_X on source side and g_{mD} is g_m measured with R_X on drain side.

The slopes of these least-squares-fitted lines obtained from fig. 3.4 are given by

$$(1 + \frac{g_{b0}}{g_{m0}} + \frac{g_{d0}}{g_{m0}}) = 1.167 \qquad \text{and} \qquad \frac{g_{d0}}{g_{m0}} = 0.055. \tag{3.14}$$

Therefore, we get on taking the difference of the slopes in (3.14) that

$$1 + \frac{g_{b0}}{g_{m0}} = 1.112. \tag{3.15}$$

If we now remove the external resistances (R_X) and measure at the same constant current (3 mA in our case) the forward (g_{mf}) and reverse (g_{mr}) saturation transconductances, i.e.

g_{mf} with source and drain as connected, and g_{mr} with source and drain interchanged, we can show using eqn. (3.8) that

$$R_D - R_S = \frac{\frac{1}{g_{mr}} - \frac{1}{g_{mf}}}{1 + \frac{g_{b0}}{g_{m0}}}. \tag{3.16}$$

Substituting the value for $1+g_{b0}/g_{m0}$ from eqn. (3.15) into the denominator of eqn. (3.16), we obtained (R_D-R_S)= -39 Ω. In fact all 24 μm x 0.8 μm devices with similar layout asymmetry between source and drain showed (R_D-R_S) between -30 and -40 Ω using the above method. When this difference resistance was placed in series with the drain, the forward and reverse saturation transconductance characteristics matched exactly, confirming the accuracy of the extraction method. To further verify this technique, we measured the linear characteristics of this asymmetric device, as well as that of a representative symmetric device on another wafer where no layout asymmetry was present. The difference in R_S between the symmetric device and the asymmetric device of about 39 Ω manifested in the simulation of the linear characteristics of the two devices using the MEDICI [3.15] program is shown in fig. 3.5.

In this case, we first simulated and matched the linear characteristic of the symmetric device, and then placed 39 Ω in series with the source and resimulated to find a very good match (as shown) with the linear characteristic of the asymmetric device. The threshold voltages of the two devices were adjusted in simulation by adjusting the electron affinity of the poly gate.

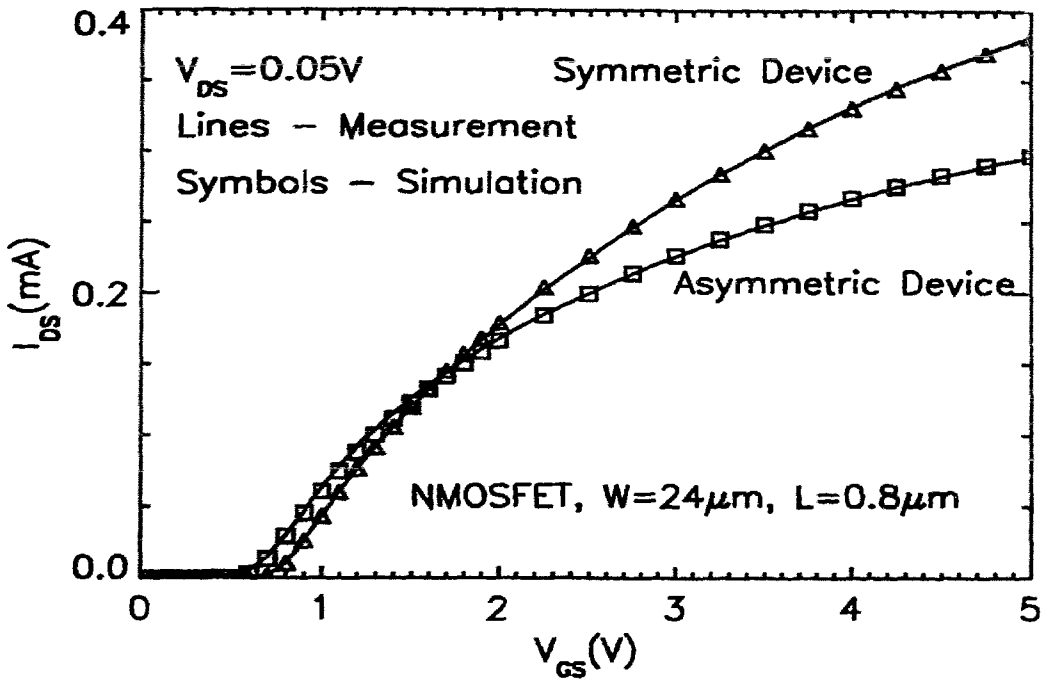

Fig. 3.5. Measurement vs. MEDICI simulation of linear characteristics. The asymmetric device was simulated with 39 Ω in series with the source of the symmetric MEDICI device. Note that R_D - R_S=-39 Ω for the asymmetric device.

3.4 Methodology of extraction: R_D+R_S from linear region

As discussed above in the context of eqn. (3.8), transconductance characteristics are most sensitive to (R_D-R_S) in saturation and so we extracted (R_D-R_S) from transconductance measurements in saturation. At the same time both eqns. (3.8) and (3.9) suggest that both g_m and g_d are sensitive to (R_S+R_D) in linear region because of the much larger values of g_{d0} with respect to g_{m0} in the linear region. As such, for extracting (R_S+R_D), the traditional and natural choice has been the linear region. However, unlike previous researchers, we will use trans- and drain conductances rather than d.c. resistances. The choice of these parameters follows naturally from the guiding eqns. (3.8) and (3.9). Also, as we will see, this choice allows us to extract (R_S+R_D) with reasonable accuracy from a single transistor. Using the value of (R_D-R_S) as above and denoted by R', we now go on to find out R_S and R_D separately as follows.

Using eqns. (3.8) and (3.9) given previously, neglecting mobility degradation with gate bias (we will discuss the effect of this neglect later), and, for a very small drain bias (50 mV) with respect to gate biases used, we can write

$$\frac{g_d}{g_m} = \frac{g_{d0}}{g_{m0}} = \left(\frac{V_{GS}' - V_T}{V_{DS}'}\right). \tag{3.17}$$

Combining eqns. (3.17) and (3.2) above we arrive at

$$V_{GS} - \frac{g_d}{g_m}(V_{DS} - I_{DS}R') = R_S I_{DS}\left(1 - \frac{2g_d}{g_m}\right) + V_T \tag{3.18}$$

where $R'=(R_D-R_S)$, as discussed above. Eqn. (3.18) represents a straight line of the left hand side versus $I_{DS}(1-2g_d/g_m)$, with slope R_S and intercept V_T. The scheme as applied to our asymmetric device is shown in figure 3.6. Measurements of g_d and g_m in the linear region with V_{DS}=50 mV were taken at 22 equispaced bias points between 0.8 V and 5V. From the slope of the least-squares-fitted straight line we get R_S=69.1 Ω, and the intercept gives V_T=0.608 V. The latter matches well with the linearly extrapolated threshold voltage of ~0.6 V. From the values of R_S and R', we obtain R_D as 30.1 Ω. This makes (R_S+R_D)=99.2 Ω that matches well with 95.3 Ω found by applying a conventional method [3.10] using more than one transistor of different channel lengths, but of the same layout pattern.

We also applied our new technique to a symmetric transistor on a different wafer where, unlike in the previous one, transistors were symmetrically laid out, i.e., $R'= (R_D-R_S) = 0$. This case which is shown in fig. 3.7.

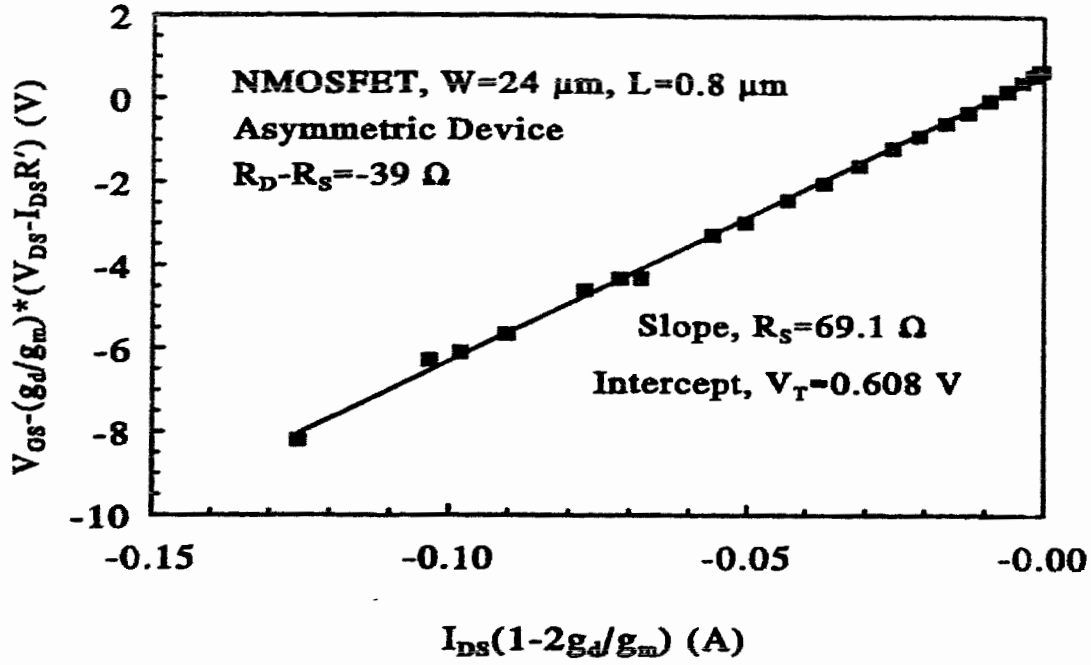

Fig. 3.6. V_{GS}-$g_d/g_m(V_{DS}-I_{DS}R')$ versus $I_{DS}(1-2g_d/g_m)$ for our asymmetric transistor with $R_S>R_D$. R' is R_D-R_S. g_d and g_m were measured at 22 equispaced bias points between 0.8 and 5 V. The slope gives R_S and the intercept V_T.

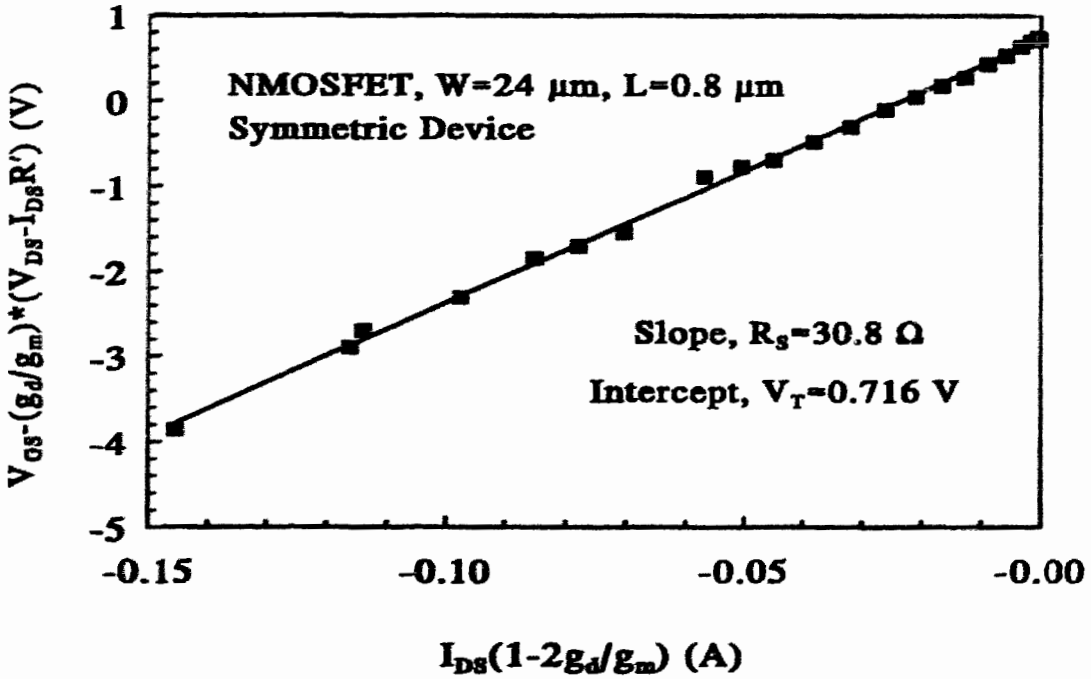

Fig. 3.7. The method of fig. 3.6 repeated for a symmetric device.

Here, we obtain a value of $R_S = R_D = 30.8\ \Omega$ that makes $(R_S+R_D)=61.6\ \Omega$. For this device the method [3.10] gave $(R_S+R_D)=55.9\ \Omega$. Also, the threshold voltage $V_T=0.716$ V matched the linearly extrapolated value of about 0.720 V for that device. The overestimation of (R_S+R_D) is due to the neglect of mobility degradation, and this is discussed in the next section.

3.5 Discussion of accuracy

As applied to real devices, our method appears to give a reasonably accurate estimate of the individual source and drain series resistances based on measurements on a single transistor. The only errors in our method originate from:

(a) The neglect of mobility degradation in eqn. (3.17) above, and we denote this error term by ΔR_{S1}.

(b) The neglect of the variation of R_S and R_D with applied V_{GS} in the linear region case of eqn. (3.8), we denote this error term by ΔR_{S2}.

However, we will show that these errors oppose one another. The first of these errors gives rise to an overestimation, while the second, to an underestimation.

3.5.1 Derivation for ΔR_{S1}

If we do not neglect the gate bias dependence of μ in equation (3.17), we rewrite (3.17) as

$$\frac{g_d}{g_m} = \frac{g_{d0}}{g_{m0}} = \frac{\mu\,(V_{GS}' - V_T)}{\dfrac{d\mu}{dV_{GS}'}(V_{GS}' - V_T)\,V_{DS}' + \mu V_{DS}'}$$

$$= \frac{V_{GS} - I_{DS}R_S - V_T}{-\dfrac{\left|\dfrac{d\mu}{dV_{GS}'}\right|}{\mu^2 C_{ox}\dfrac{W}{L}} I_{DS} + V_{DS} - I_{DS}(2R_S + R')}. \qquad (3.19)$$

In deriving the above equation (3.19), we have noted that $d\mu/dV_{GS}'$ is negative. By transposing (3.19), it is easy to show that

$$V_{GS} - \frac{g_d}{g_m}(V_{DS} - I_{DS}R') = R_S I_{DS}(1 - \frac{2g_d}{g_m}) - \frac{2g_d}{g_m} I_{DS} \frac{\left|\frac{d\mu}{dV_{GS}'}\right|}{2\mu^2 C_{ox}\frac{W}{L}}. \qquad (3.20)$$

Since $2g_d/g_m >> 1$ in linear region, we can approximate (3.20) as

$$V_{GS} - \frac{g_d}{g_m}(V_{DS} - I_{DS}R') \cong \left(R_S + \frac{\left|\frac{d\mu}{dV_{GS}'}\right|}{2\mu^2 C_{ox}\frac{W}{L}} \right) I_{DS}(1 - \frac{2g_d}{g_m}). \qquad (3.21)$$

Comparing equation (3.21) with (3.18) we readily obtain,

$$\Delta R_{S1} \cong \frac{\left|\frac{d\mu}{dV_{GS}'}\right|}{2\mu^2 C_{ox}\frac{W}{L}}. \qquad (3.22)$$

We note that ΔR_{S1} is an overestimation term on R_S. In eqn. (3.22) μ and $d\mu/dV_{GS}'$ represent average values of mobility and its degradation rate with gate-to-source bias, and C_{ox} and W/L' are respectively the oxide capacitance per unit area and the aspect ratio for the MOSFET, W being the channel width, and L' the effective channel length. If we assume the SPICE level 3 model [3.11] for μ versus V_{GS}', given by

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS}' - V_T)}, \qquad (3.23)$$

where μ_0 is the low-field mobility, and θ is a constant, ΔR_{S1} can be shown to be given by,

$$\Delta R_{S1} \cong \frac{\theta}{2\mu_0 C_{ox}\frac{W}{L'}}. \tag{3.24}$$

From our parametric data we use, θ=0.073 V^{-1}, μ_0=535 cm^2/V-s, C_{ox}= 203 nF/cm^2, W=24 μm, L'= 0.65 μm for our 0.8 μm device. This gives us ΔR_{S1}= 9.1 Ω. However, this is much higher than 2-3 Ω by which our value of R_S overestimates that obtained by the method [3.10]. We think that part of ΔR_{S1} is counterbalanced by the second error term ΔR_{S2} that we derive next.

3.5.2 Derivation for ΔR_{S2}

In this case we do not neglect the gate bias dependence of R_S and R_D, as was done in simplifying eqn. (3.6) into eqn. (3.8). Since, g_{d0}/g_{m0} is large in the linear region, a more accurate simplified expression for g_m is given by,

$$g_m = \frac{g_{m0}\left(1 - \frac{g_{d0}}{g_{m0}} I_{DS}\frac{d}{dV_{GS}}(R_S + R_D)\right)}{1 + (g_{m0} + g_{b0})R_S + g_{d0}(R_S + R_D)}. \tag{3.25}$$

In that case, equation (3.17) is modified to

$$\frac{g_d}{g_m} = \frac{V_{GS}' - V_T}{V_{DS}'}\left[1 + \frac{g_d}{g_m}(R_{Sm} + R_{Dm})I_{DS}\right]. \tag{3.26}$$

By breaking up V_{GS}' and V_{DS}' using eqn. (3.2), and transposing, we can show that,

$$V_{GS} - \frac{g_d}{g_m}(V_{DS} - I_{DS}R')$$

$$= I_{DS}\left(1 - \frac{2g_d}{g_m}\right)\left(R_S - \frac{\frac{g_d}{g_m}(V_{GS}' - V_T)\ (R_{Sm} + R_{Dm})}{1 - \frac{2g_d}{g_m}}\right). \tag{3.27}$$

Again, since $2g_d/g_m >> 1$, we can approximate (3.27) as

$$V_{GS} - \frac{g_d}{g_m}(V_{DS} - I_{DS}R')$$

$$\cong I_{DS}\left(1 - \frac{2g_d}{g_m}\right)\left[R_S + \frac{1}{2}(V_{GS}' - V_T)\ (R_{Sm} + R_{Dm})\right]. \tag{3.28}$$

Therefore, ΔR_{S2} is given by,

$$\Delta R_{S2} \cong \frac{(V_{GS}' - V_T)}{2}\frac{d}{dV_{GS}}(R_S + R_D)\,. \tag{3.29}$$

ΔR_{S2} represents an underestimation term, since normally $d(R_S+R_D)/dV_{GS}$ is negative [3.8]. Also, the voltage dependent nature of the first term on the right side of eqn. (3.29) suggests that if the magnitude of $d(R_S+R_D)/dV_{GS}$ were not of a form $C/(V_{GS}'-V_T)$, where C is a constant, we would not obtain good linearity in the curves of figs. 3.6 and 3.7. Conversely, good linearity (particularly, for higher gate biases, i.e., to the left of the abscissa) of the curves of figs. 3.6 and 3.7 suggests that the magnitude of $d(R_S+R_D)/dV_{GS}$ is of the form suggested above over most of the gate bias range measured. This observation matches with the indications in [3.8] where the appearance of the gate

bias dependent series resistance matches a logarithmic nature of the dependence [3.13], i.e.,

$$R_S + R_D = K - C \cdot ln\,(V_{GS}' - V_T)\,, \tag{3.30}$$

where, K and C are constants. It should be noted that this empirical model is expected to describe the behavior of (R_S+R_D) versus V_{GS}' for higher values of $(V_{GS}'-V_T)$.

In order to obtain values of K and C, The relation (3.30) was matched with the extracted dependence of (R_S+R_D) on V_{GS} in fig. 3.8. The match is good for higher V_{GS}, with K=70, and C=14. The effect is a mutual cancellation of the two error terms to give rise to a net predicted overestimation in R_S of about 2 Ω that matches well with the overestimation of 2-3 Ω in our method when compared with the method in [3.10]. The extraction of the dependence of (R_S+R_D) on V_{GS} was made using four transistors of symmetrical layouts, and mask gate lengths (L_m) of 0.8, 1.2, 2.0, and 3.0 μm. The technique used is discussed below.

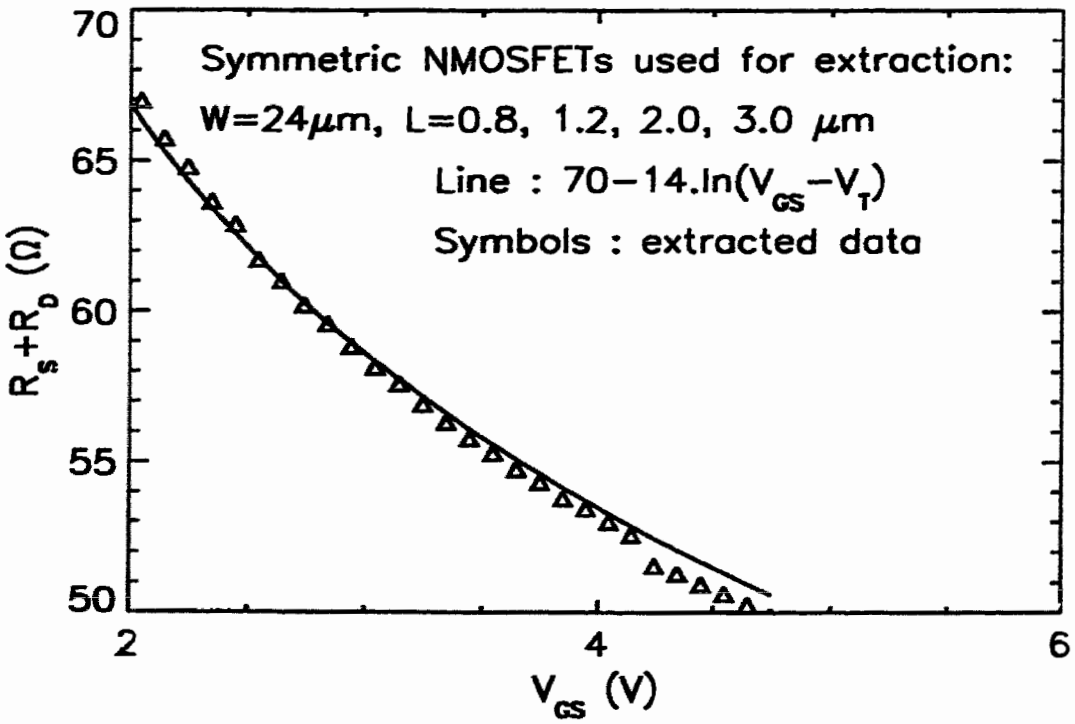

Fig. 3.8. The match between the empirical relation for R_S+R_D and its extracted values versus V_{GS}.

For a MOSFET, it can be shown [3.16] that,

$$R_m(V_{GS}) = \frac{V_{DS}}{I_{DS}(V_{GS})} = (L_m - \Delta L(V_{GS})) \left[\frac{1}{\mu_0 W C_{ox}(V_{GS} - V_T)} + \frac{\theta}{\mu_0 W C_{ox}} \right] + R_t(V_{GS}) \quad (3\,31)$$

where we have used the expression (3.23) for gate bias dependent μ. W and C_{ox} represent the width and the oxide capacitance of the device respectively. The total parasitic resistance R_t (=R_S+R_D) as well as the effective channel length shortening term ΔL are functions of gate bias as well. Therefore, by plotting R_m versus L_m for fixed values of (V_{GS}-V_T) for all four transistors, we obtain straight lines with slopes $Slp(V_{GS})$ and intercepts $Int(V_{GS})$. By inspecting the eqn. (3.31), we can recognize, that

$$Slp(V_{GS}) = \left[\frac{1}{\mu_0 W C_{ox}(V_{GS} - V_T)} + \frac{\theta}{\mu_0 W C_{ox}} \right], \text{ and}$$
$$Int(V_{GS}) = R_t(V_{GS}) - \Delta L(V_{GS}) \cdot Slp(V_{GS}) \quad (3\,32)$$

Therefore, knowing $\Delta L(V_{GS})$ we can obtain R_t at each V_{GS} as plotted in fig. 3.8 above. In order to find $\Delta L(V_{GS})$ we used a simulation technique suggested in [3.8]. Simulated [3.15] electron concentration under the gate was equated with the vertically integrated net impurity concentration in the LDD region to find the demarcation between the channel and the source/drain regions. The portion between these demarcation points was L_{eff} given by L_m-ΔL.

3.6 Conclusion

In this chapter, we have discussed the method of extraction for the source and drain series resistances of a MOSFET, using a single transistor. This appears to be a very simple and practical method to estimate asymmetrical resistances due to source and drain diffusions. We do not need the aid of any other transistor for this extraction. The method is therefore well suited in situations where a transistor undergoes progressive degradation due to trapping of charges in the LDD spacer region, as with a floating gate measurement, or where transistors are differently affected by layout or processing variations. In our view, the unique feature of our approach is the use of the dynamic conductances of the MOSFET in appropriate regions of operation. We have provided a detailed error analysis for this technique and show that the overestimation error due to the neglect of mobility degradation with gate bias is largely compensated by the underestimation error due to the neglect of the dependence of the parasitic resistances on gate to source bias.

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Chapter 4

Experimental features of the early-mode hot-carrier degradation in LDD NMOSFETs

4.1 Introduction

In submicron LDD NMOSFETs, one of the most critical elements is the oxide above the LDD region, part of which is the gate oxide and the remaining part the spacer oxide. Hot-carrier-induced electron traps in this oxide can cause depletion of the underlying LDD region. This leads to increase of the parasitic resistance due to the LDD regions [4.1], and therefore reduced current drive capability of the transistor. However, the amount of parasitic resistance increase is dependent on several factors. The most critical of these factors are the quality of the oxide above the LDD region, the doping concentration in the LDD region, and the length of gate overlap of the LDD region.

As the quality of the oxide at the edge of the gate as well as the spacer oxide is likely to be poorer than that of the gate oxide above the channel region, this oxide region at the gate edge is most likely to be degraded much earlier in any hot-carrier stressing situation. There has been little work to date concerning this early-mode of hot-carrier degradation. Most authors [4.2],[4.3] have concentrated on the long-term degradation in the channel region near the drain under maximum substrate current stressing situations, i.e. with $V_{GS} \sim V_{DS}/2$.

Methods to characterize the long-term in-channel degradation using shifts in threshold voltage, linear transconductance or subthreshold slope, and the charge pumping technique are well established. However, in this long term degradation situation, under high electron injection, the early mode degradation gets coupled and masked by threshold

voltage shifts. Therefore, in order to assist in optimizing and characterizing the LDD region, this early-mode of hot-carrier degradation of the LDD-region oxide should be observed and interpreted from measurements involving stressing in low injection situations; measurements that allow direct observation of this degradation without being masked by threshold voltage shifts.

In our hot-carrier degradation measurements, we have observed a particularly sharp early-mode degradation. Hence, our interest in studying this effect. We have studied this early degradation of the LDD-region oxide through a simple experiment that combines the floating gate measurement [4.4]-[4.6] with I_{DS} versus V_{GS} measurements taken in the saturation region [4.7],[4.8]. We have also used a spatial profiling charge pumping method [4.7],[4.9]-[4.11] to study this phase of the degradation. In this chapter, we will discuss these experimental techniques and the results of their application on our devices, that delineate the features of the early-mode hot-carrier degradation.

Since there are not enough techniques to probe deep into the LDD region close to the spacer oxide, 2-D simulations seem to be a vital tool to understand the problem. The observations of this chapter allow us to develop a simulation framework (to be discussed in chapter 5) involving interface trapped charges at the drain-side gate edge.

4.2 Device details and measurement instrumentation

All MOSFET's tested/simulated had drawn gate length of 0.8 μm, gate oxide thickness of 175 Å, spacer width of 0.2 μm, LDD phosphorus implant dose of $2\text{x}10^{13}$ / cm^2 at 40 keV followed by a drive cycle at 900°C in a combination of O_2 and N_2 ambients for about 70 minutes, and salicided As-implanted source/drain regions. The MOSFET's were fabricated using a standard BiCMOS process.

Hot-carrier degradation measurements, floating gate measurements, and transconductance measurements were performed using a computer controlled HP 4145B

semiconductor parameter analyzer (SPA). The devices were directly probed on wafers placed on a Karl Suss PM8 manual prober that is kept inside a shielded box with a dry nitrogen flow. The HP 4145B machine is controllable through a IBM PC that uses PASCAL programs to control measurements and data collection over an IEEE 488 interface.

The charge pumping measurements were performed using a HP 8115A (50 MHz) dual channel pulse generator, a HP 4145B semiconductor parameter analyzer, and a Keithley 617 electrometer. Again, the wafer was placed in a Karl Suss PM8 manual prober. The instruments were controlled by HP-VEE graphical programs running on a IBM PC. The schematics of the floating gate and charge pumping measurements are shown later in sections discussing these measurements.

4.3 Degradation measurements

Two-stage hot-carrier degradation as observed in our LDD NMOSFET devices is shown in fig. 4.1. The early mode (1000 - 3000s) of the degradation is characterized by

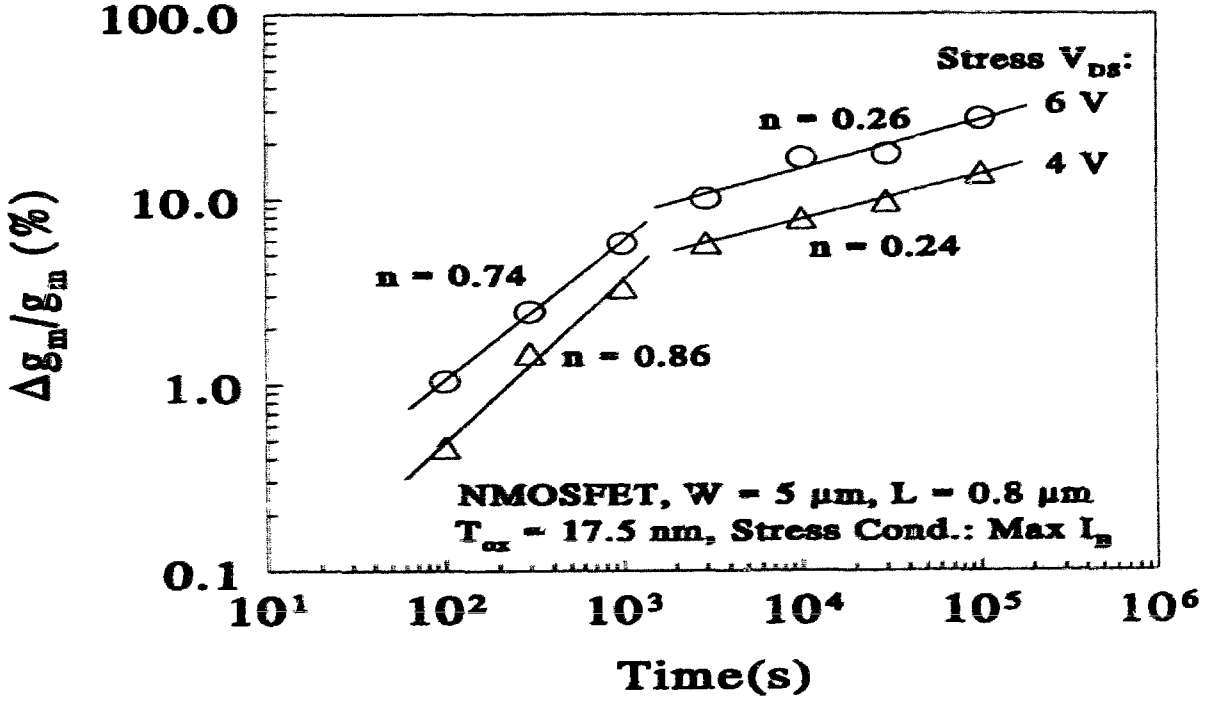

Fig. 4.1. Evidence of two-stage hot-carrier degradation in oxide-spacer LDD NMOSFET characterized by a sharp rate (high n) of initial degradation, and a much slower rate (low n) afterwards.

a sharp rate (n ~ 0.8, assuming an $A.t^n$ dependence) of linear g_m degradation. However, the rate of the late mode degradation is much lower (n~0.25) and matches well with that (n=0.22) reported in [4.12]. Also, the early mode degradation is accompanied by an initial fall in both $I_{B,max}$ and I_B/I_D at maximum I_B, as shown in fig. 4.2. While these quantities rise again in the late mode, $I_{B,max}$ measured in the reverse mode decreases continuously until 10^5s of stress.

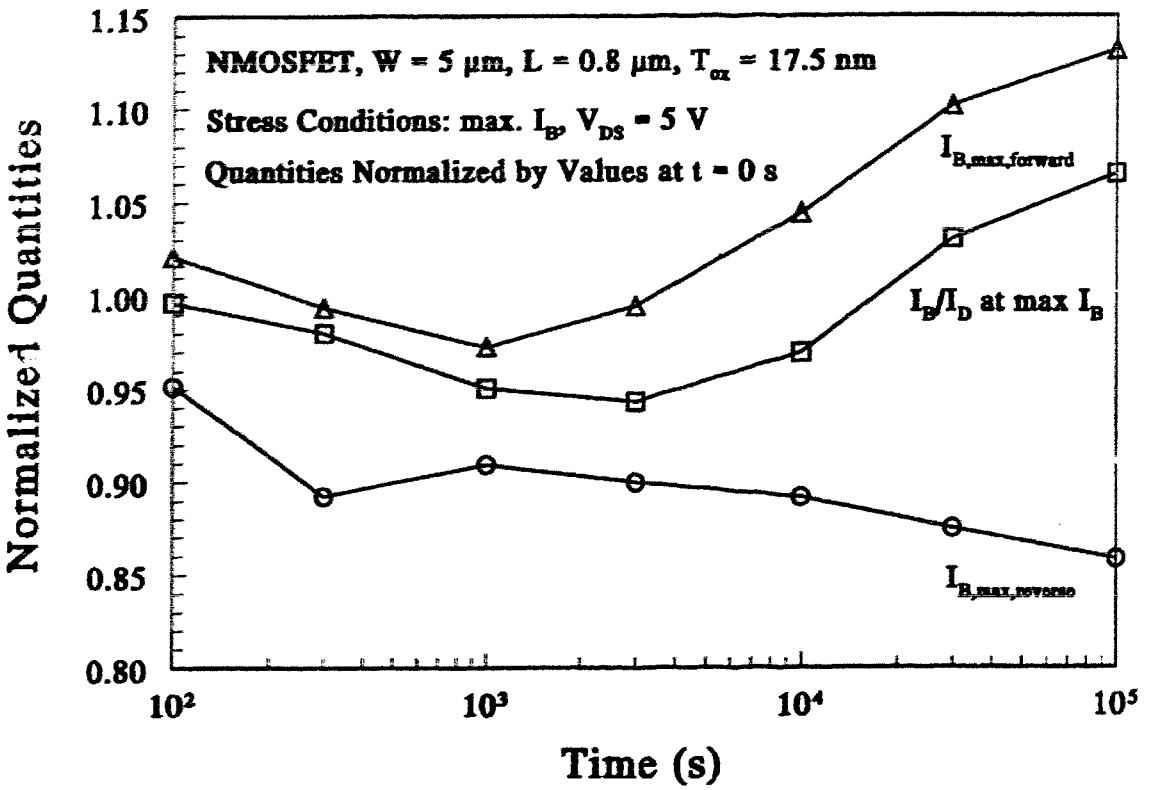

Fig. 4.2. Both $I_{B,max}$ and I_B/I_D at max. I_B measured in the forward mode drop in the initial phase. In the reverse mode, $I_{B,max}$ falls all the way as in conventional degradation.

4.4 Experimental Techniques

4.4.1 Floating gate measurement

The floating gate technique is a very sensitive and simple method to observe the otherwise intractable impact ionization induced gate currents in MOSFETs. An NMOSFET is biased in the maximum gate current situation ($V_{GS} \sim V_{DS}$) to start with.

Immediately afterwards, the gate probe is lifted leaving the positive charge on the gate and hence a gate to source voltage. The setup is shown in fig. 4.3

We chose V_{DS}=7.5V and starting V_{GS}=7V to facilitate reasonably high impact-ionization-induced hot-electron gate current, but a lower-than-maximum electron injection situation for the initial biasing condition. In this situation the electrons injected into the gate in the form of a gate current start neutralizing the positive charge on the gate pad, and, therefore, the gate-to-source

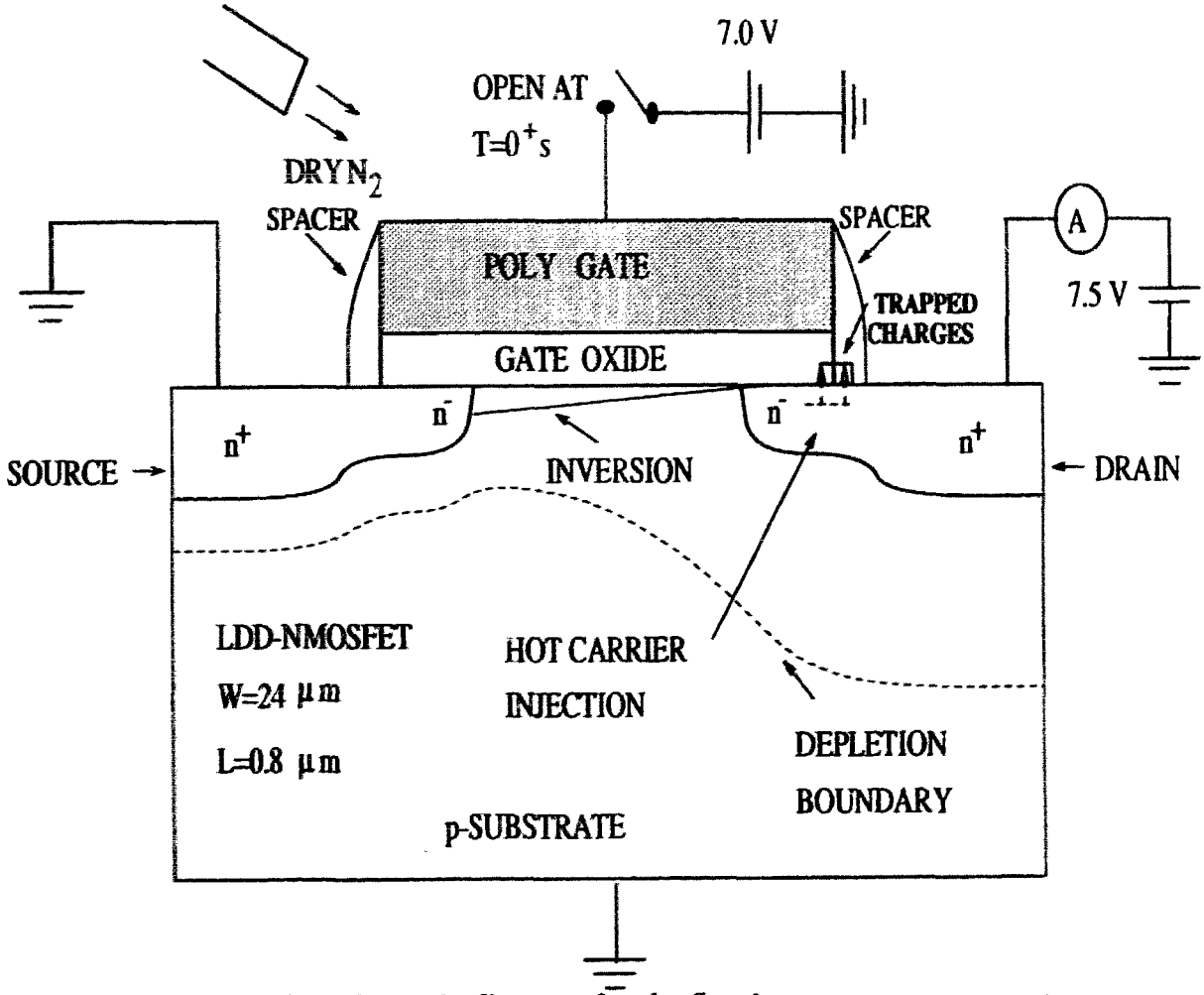

Fig. 4.3. The schematic diagram for the floating gate measurement.

voltage. Thus, the saturation drain current monitored by the current meter starts dropping from its initial biased value. We record this decaying drain current over time. The wafer is placed under dry nitrogen jet to reduce the possibility of any other leakage mechanism. By

comparing the decaying drain currents with a saturation I_{DS} versus V_{GS} (V_{DS}=7.5V and V_{GS} swept from 0 to 7V) characteristic of the virgin MOSFET, we can obtain the decaying V_{GS} vs. time characteristic. The latter yields $I_G(V_{GS})$ as

$$I_G(V_{GS}) = C\frac{dV_{GS}}{dt} \tag{4.1}$$

where C represents the total capacitance associated with gate, i.e., the pad, interconnections, etc. We measure C with a high frequency C-V meter. As C is dominated by thicker oxide capacitances due to pad and interconnections, the use of high frequency measurements is justified. Also, for the same reason, the bias dependence of C is minimal.

First, a floating gate measurement was performed with biases of V_{DS}=0.1V and V_{GS}=7V. There was negligible decay in the drain current that was monitored until 500s, after the gate probe was lifted at about 10s from the start of the measurement. This initial floating gate cycle is shown in figure 4.4. It indicates that there is negligible electron

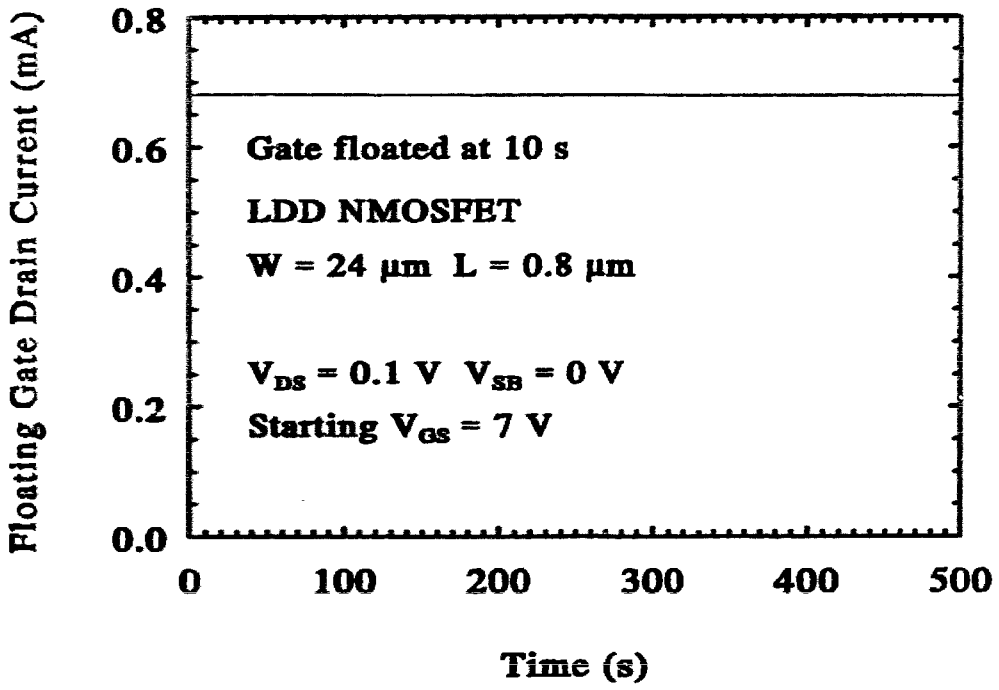

Fig. 4.4. Floating gate measurement with the MOSFET biased in the linear region to check for leakages from gate.

injection across the gate oxide through either Fowler-Nordheim tunneling [4.13] or any other leakage mechanism.

Another 5 cycles of floating gate measurements were performed with the device biased in saturation with V_{DS}=7.5V and starting V_{GS}=7V as shown in fig. 4.5. During these measurements, we observed a prominent evolution (see figure 4.5) of the floating gate drain current going from one cycle to another, each lasting 500s. In each cycle, the gate was floated around 15s from the start. It must be mentioned here that lifting the gate probe before 15s did not make much

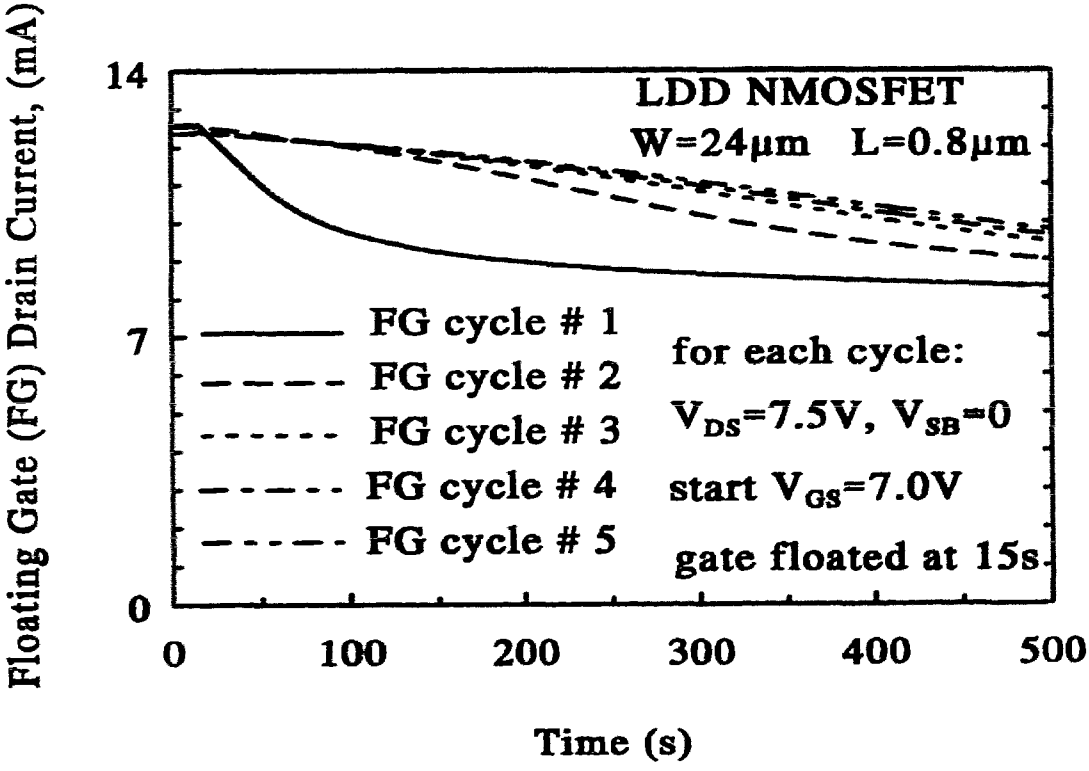

Fig. 4.5. Evolution of floating gate drain current over several cycles. The biasing configuration maximizes hot-electron gate current.

difference when tried on other devices. Interestingly, the value of the threshold voltage remained virtually unchanged (V_T=623 mV after 5 floating gate cycles) with respect to its value for the virgin device (V_T=622 mV). Also, the subthreshold slope remained virtually

unchanged. Similar results were also obtained by the authors of [4.6], [4.14]. These results indicate generation of negative charge due to trapped electrons, or electron filled acceptor-type interface traps outside the channel region, mostly assumed to be in the oxide in gate-drain overlap region or the spacer oxide at the edge of the gate [4.15]. These trapped electrons impede further injection by increasing the effective barrier height the hot electrons need to overcome in order to be injected into the gate oxide. Also, there appears to be a saturation in the number of electrons that can be trapped - so that the floating gate drain current characteristics tend to converge after the third cycle as shown in fig. 4.5. Obviously, most of the early mode of degradation is complete within the first cycle of 500s.

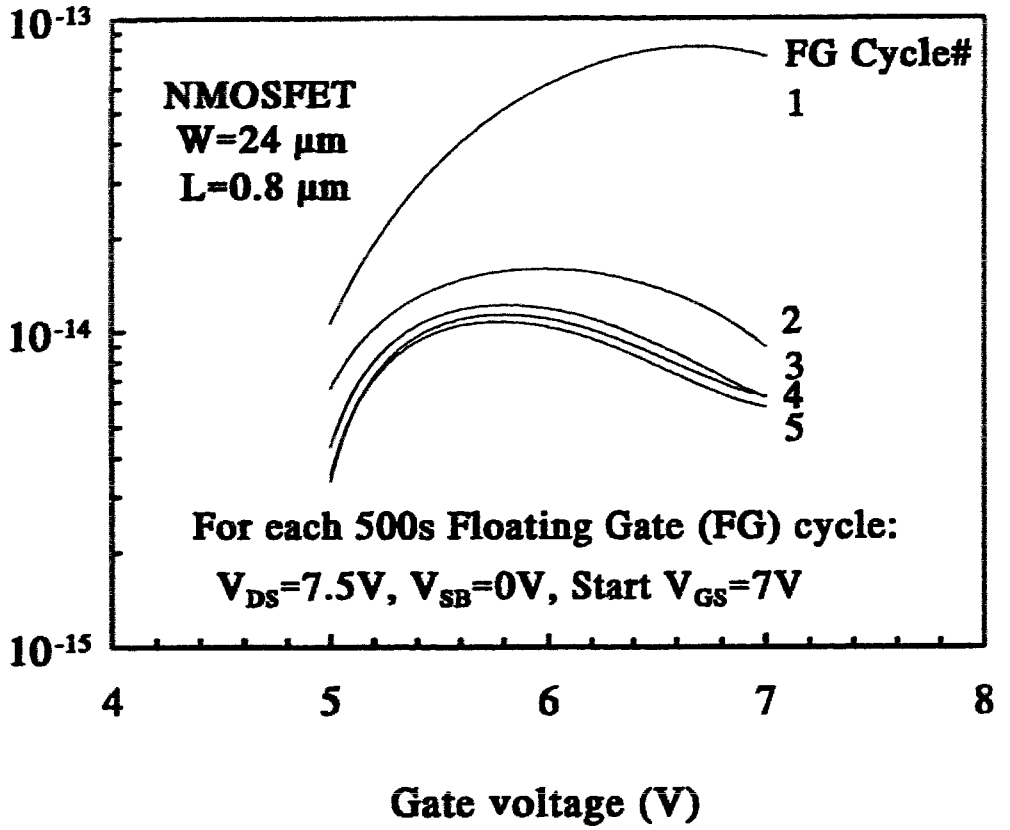

Fig. 4.6. Gate currents extracted from the floating gate cycles of fig. 4.5. The shift in the peaks of the gate currents to lower gate biases is remarkable.

The corresponding I_G vs. V_{GS} curves were extracted using eqn. (4.1) above with a measured C of 2.75 pF and the method described earlier, and the results are shown in fig. 4.6. While the decrease in gate current over succeeding cycles is expected [4.15] as explained above, an interesting new feature of our observation is the shift of the gate current peaks to lower gate biases with each cycle (see fig. 4.6). This is particularly true for the first three cycles. We will explain this observation in the discussion section. From the evolution of the gate currents, we extracted the corresponding evolution of ϕ_b, the barrier height to gate current injection. The results are presented in fig. 4.7. This evolution was extracted using the following equation derived from the Lucky-Electron Model [4.16].

$$\Delta\phi_b \equiv \phi_i ln\left(\frac{I_{G,d}}{I_{G,v}}\right) / \left(ln\left(\frac{I_B}{I_{DS}}\right)\right) \tag{4.2}$$

where ϕ_i=1.3 eV [4.16] and $I_{G,d}$ and $I_{G,v}$ are the gate currents for the degraded and virgin transistor at V_{GS}=7V, and V_{DS}=7.5V. The ratio of the substrate current to drain current

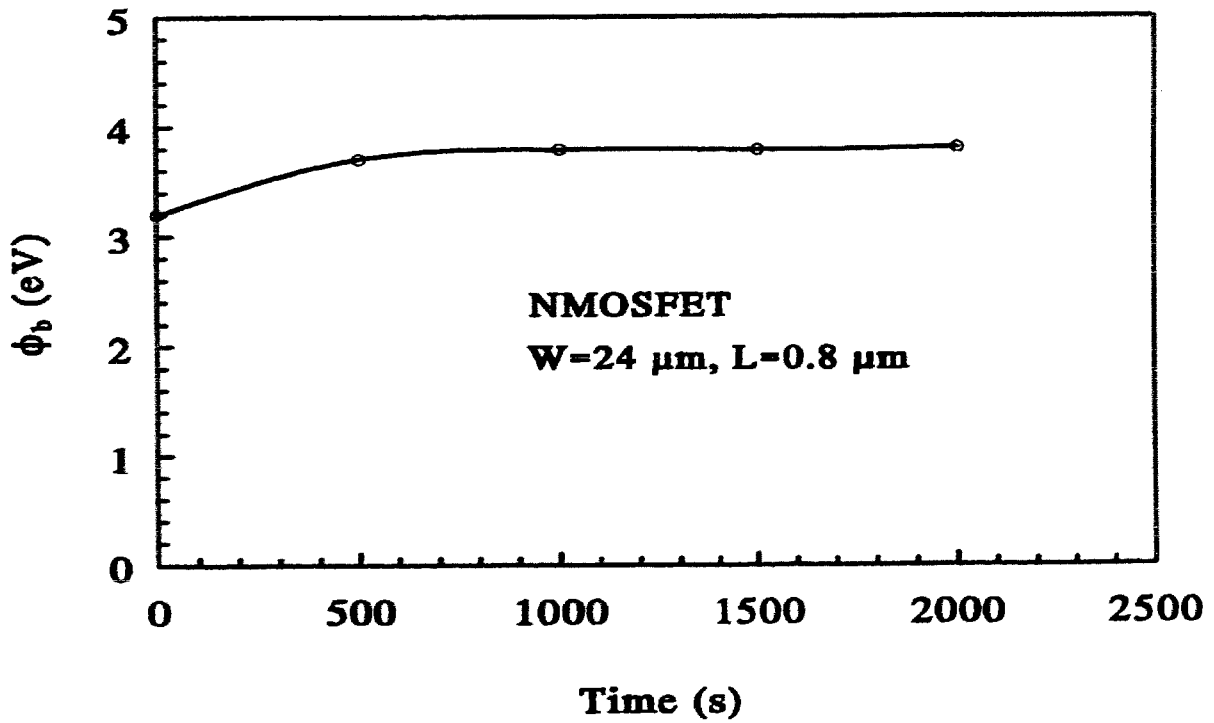

Fig. 4.7. Evolution of the barrier height ϕ_b to gate current injection during the early mode degradation.

(I_B/I_{DS}) for this bias was taken to be that for the virgin device. The value of ϕ_b for the virgin device (3.2 eV) was assumed to be the difference between electron affinities of silicon and silicon dioxide.

The above evolution of ϕ_b shows a saturating nature, suggesting a saturation of the electron trapping process in the early mode of the degradation. How this electron trapping leads to depletion of the underlying LDD region, and consequently results in a corresponding evolution in R_D is studied by the transconductance technique we discuss next.

4.4.2 Transconductance technique

For a MOSFET with parasitic resistances R_S and R_D associated with source and drain respectively, it was show in chapter 4 that the measured transconductance (g_m) is given by

$$g_m = \frac{g_{m0}}{1 + (g_{m0} + g_{b0})R_S + g_{d0}(R_S + R_D)} \tag{4.3}$$

where g_{m0}, g_{d0}, and g_{b0} are the magnitudes of the intrinsic conductances with respect to internal gate, drain, and substrate biases respectively. In saturation, as g_{d0} is normally negligible compared to (g_{m0}+g_{b0}), the sum of R_S and R_D times g_{d0} as it occurs in the third term of the denominator of eqn. (4.3) has little effect on the measured g_m. As such, the measured value of g_m with normally connected source and drain, and denoted by g_{mf}, is sensitive to *only* R_S, because, from eqn. (4.3) above,

$$g_{mf} \cong \frac{g_{m0}}{1 + (g_{m0} + g_{b0})R_S}. \tag{4.4}$$

Now, if the source and drain are interchanged, the measured value of g_m, and denoted by g_{mr}, is sensitive to *only* R_D, because, from eqn. (4.3) above,

$$g_{mr} \cong \frac{g_{m0}}{1 + (g_{m0} + g_{b0}) R_D}. \tag{4.5}$$

Hence any variations in R_S and R_D will separately show up in the measured g_{mf} and g_{mr}, and hence in the I_{DS} vs. V_{GS} characteristics in saturation measured normally, and again with the source and drain interchanged. This situation is distinctly different from that with the linear transconductance (I_{DS} vs. V_{GS}) characteristics where g_{d0} is the dominant conductance, and hence the third term in the denominator of eqn. (4.3) above dominates over the second term. Therefore, both normal and reverse characteristics coincide even if R_S and R_D are different. In order to evaluate the effect of stress-induced charges on the parasitic series resistances R_S and R_D of the MOSFET, one should therefore choose the transconductance (I_{DS} vs. V_{GS}) characteristics in saturation.

We monitored these pairs of saturation I_{DS} vs. V_{GS} characteristics (with V_{DS}=5V) for our LDD NMOSFET before any floating gate cycle as well as after each of the cycles shown in figure 4.5. The pairs of these saturation I_{DS} vs. V_{GS} characteristics taken for the virgin device and taken after the first and the fifth floating gate cycles are shown in figure 4.8.

The dispersion between the forward (lower curve of each pair, with normal source/ drain connection) and reverse (upper curve of each pair, with reversed source/drain connection) I_{DS} vs. V_{GS} characteristics for the virgin device is due to the fact that the source side interconnection resistance was larger than that of the drain side (69 Ω and 30 Ω respectively, measured using a technique discussed in chapter 3) due to layout asymmetry. However, this helps us visualize the variations in R_S and R_D better. The pairs of I_{DS} vs. V_{GS} characteristics taken after cycle # 2, 3, and 4 lie between those after cycle #1 and 5, and are therefore omitted from fig. 4.8. It must be mentioned here that the

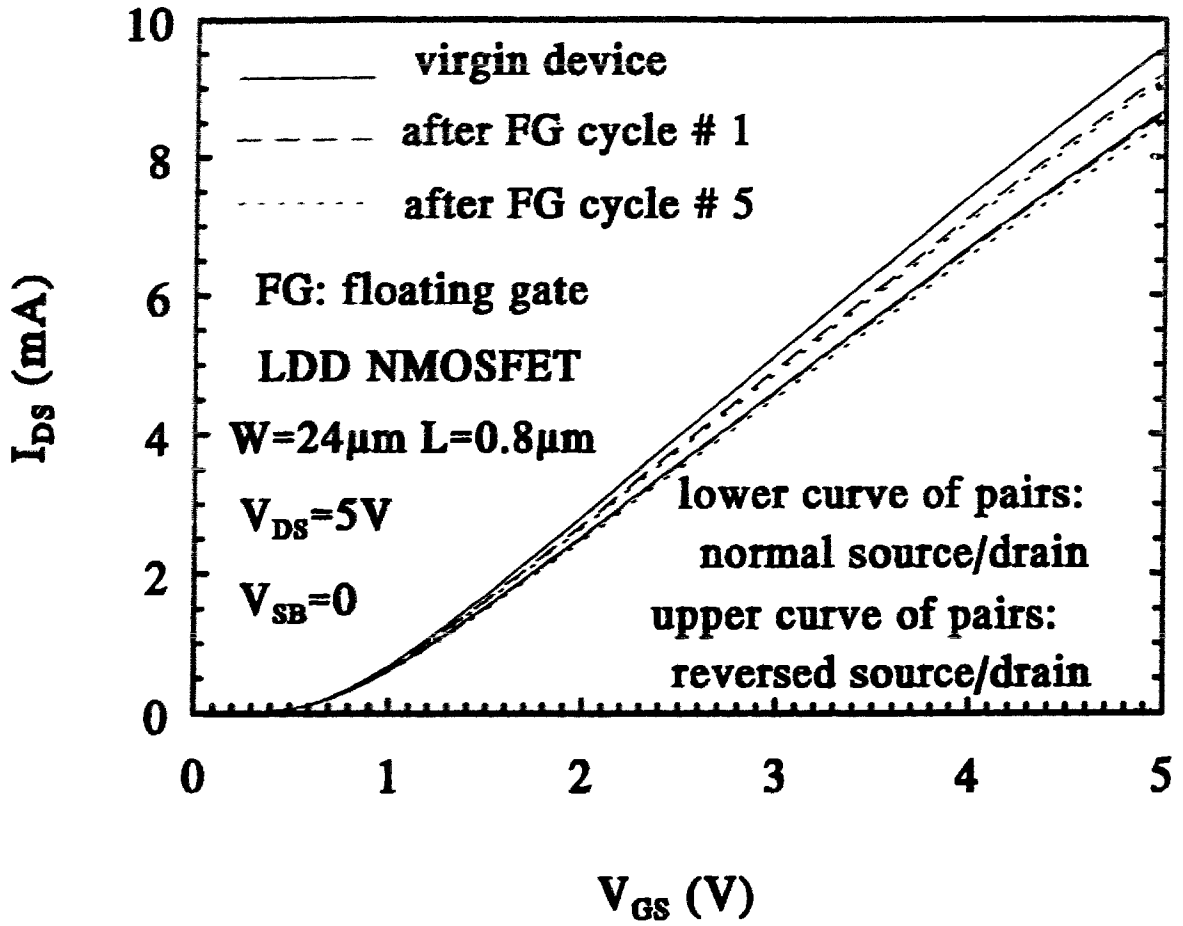

Fig. 4.8. Reverse and forward saturation I_{DS} vs. V_{GS} characteristics for the MOSFET during the floating gate cycles shown in fig. 4.5.

forward and reverse substrate currents measured on the virgin device did not show any double humps as in [4.17]. This rules out the possibility of source or drain side non-overlap. Hence, the indication that the asymmetry in the I_{DS} vs. V_{GS} saturation characteristics occurs due to layout difference alone is strong. We need to mention here that there was no special reason for choosing the asymmetric devices, except that we started experimenting with them for the work discussed in chapter 3. The corresponding evolution of R_D and R_S is shown in fig. 4.9. These curves were generated from values of ΔR_S and ΔR_D quantified using measured g_{mf} and g_{mr} for the virgin device and after each floating gate cycle. For example, using eqn. (4.3) we can show that,

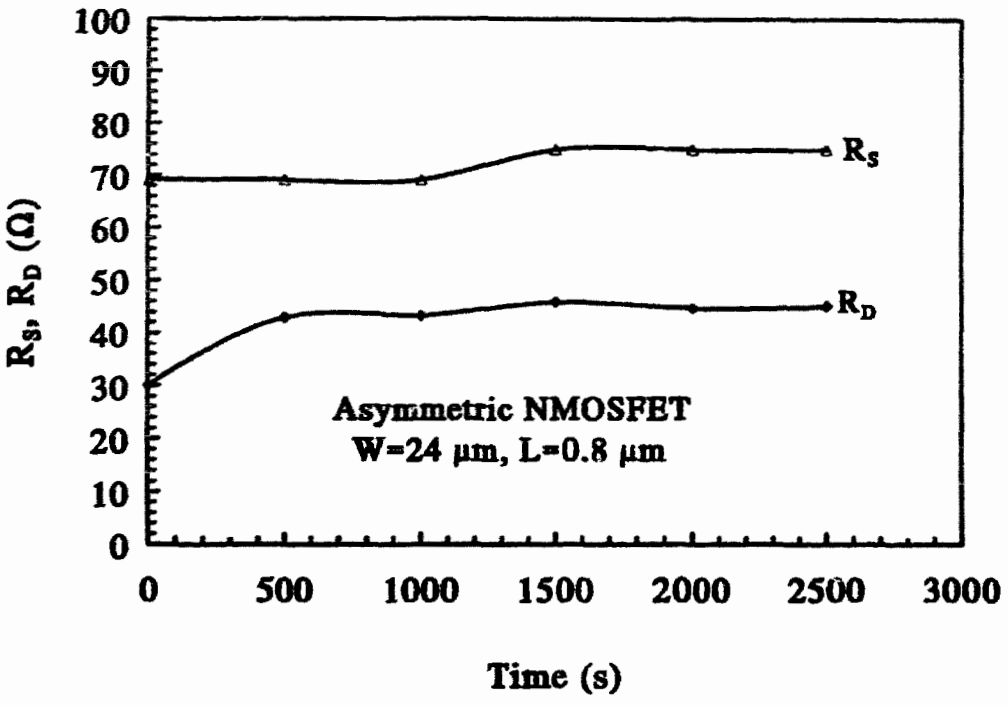

Fig. 4.9. Evolution of R_D and R_S during the early mode degradation.

$$\Delta R_D = \frac{\frac{1}{g_{mr,d}} - \frac{1}{g_{mr,v}}}{1 + \frac{g_{b0}}{g_{m0}}} \tag{4.6}$$

where, d and v in the subscript of g_{mr} denote degraded and virgin devices respectively, measured at the same drain current (3 mA in our case). A similar expression holds for ΔR_S involving g_{mf} in stead of g_{mr} in eqn. (4.6) above. As the channel region of the device remains undegraded in this early mode degradation, the assumption of a constant denominator in eqn. (4.6) above is valid. The value of the denominator was found to be 1.112 for our device, using the method discussed in chapter 3. The evolution of R_D is seen to match very well with that of ϕ_b shown in fig. 4.7. The small evolution of R_S is most likely due to an increase in effective channel length as discussed later in chapter 6.

4.4.3 Charge pumping technique

The charge pumping set up is shown in fig. 4.10 in the next page. In the charge pumping technique, periodic pulses are applied to the gate of the NMOSFET with the source and drain terminals reverse biased as shown in fig. 4.10. The gate pulses periodically drive the MOSFET between accumulation and inversion. During the lo-hi transition of the gate pulse, a negative charge packet Q_B, the depletion charge, is drawn from the substrate circuit to the oxide-silicon interface. Also, another negative charge packet (Q_{INV}+Q_{it}), consisting of the inversion charge Q_{INV} and the charge Q_{it} needed to fill up the interface states between (roughly) the Fermi level positions corresponding to accumulation and inversion is drawn from the source-drain circuit to the oxide-silicon interface. During the reverse transition of the gate pulse, only Q_{INV} is returned to the source-drain circuit, while (Q_B+Q_{it}) is now returned to the substrate circuit. This happens because the interface trapped charge Q_{it} cannot disappear as quickly as Q_{INV} into the source-drain circuit due to the former's much larger emission times compared to the gate pulse transition times, and are therefore, neutralized through recombination with the accumulating majority carriers coming from the substrate circuit. Thus, in each cycle of the gate pulse, a net negative charge Q_{it} is transferred or pumped from the source-drain circuit to the substrate circuit. This gives rise to a net charge pumping current (I_{CP}), measurable by a d.c. ammeter and typically given for a spatial interface states distribution $N_{it}(x)$

$$I_{CP} = f \cdot q \cdot W \int_{X_S}^{X_D} N_{it}(x)\, dx. \tag{4.7}$$

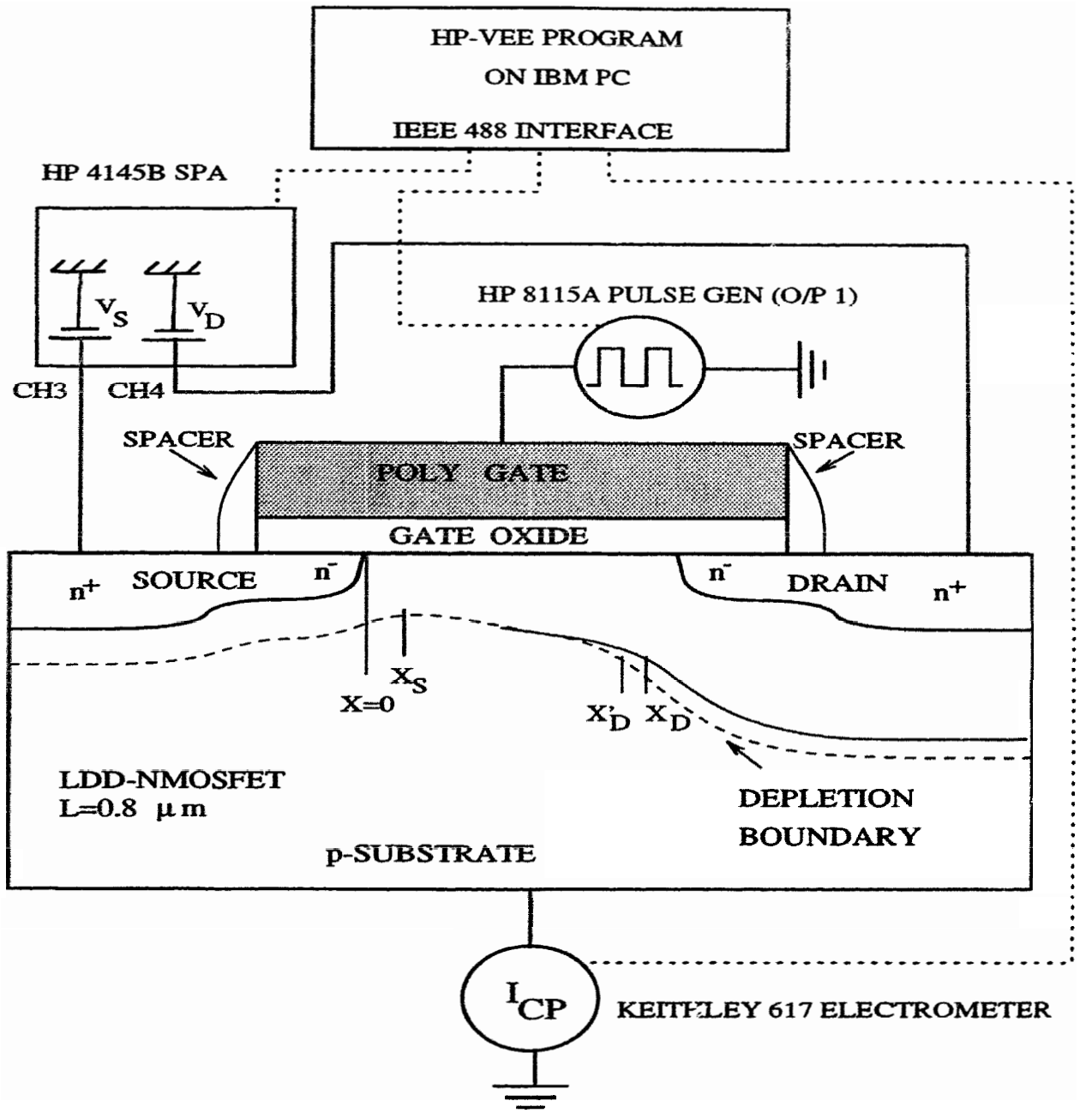

Fig. 4.10. Spatial profiling charge pumping set up.

Here, f is the gate pulse frequency, q is the electronic charge, and W is the MOSFET width. X_S, X_D denoting the interfacial positions of the source and drain depletion widths for applied source (V_S) and drain (V_D) biases respectively are given by

$$X_S = \{\sqrt{\frac{2\varepsilon_s N_{LDD}(V_S + V_{bi} - 2\Phi_F)}{qN_{SUB}(N_{LDD} + N_{SUB})}}\}, \tag{4.8}$$

and,

$$X_D = L_{eff} - \{\sqrt{\frac{2\varepsilon_s N_{LDD}(V_D + V_{bi} - 2\Phi_F)}{qN_{SUB}(N_{LDD} + N_{SUB})}}\}. \tag{4.9}$$

In the above equations, L_{eff}, N_{SUB}, N_{LDD}, ε_s are respectively the effective channel length, substrate doping concentration, LDD doping concentration, and the silicon permittivity. Also, the Fermi potential Φ_F is given by,

$$\Phi_F = \frac{kT}{q} \cdot ln\left(\frac{N_{SUB}}{n_i}\right). \tag{4.10}$$

Built-in voltage V_{bi} for the substrate-LDD junction is given by,

$$V_{bi} = \frac{kT}{q} \cdot ln\left(\frac{N_{SUB}N_{LDD}}{n_i^2}\right). \tag{4.11}$$

In eqns. (4.10) and (4.11) above, n_i represents the intrinsic carrier concentration in silicon.

Thus, by varying the drain (V_D) and source (V_S) biases independently as shown in fig. 4.10, but keeping their difference $\Delta V = V_D - V_S$ small (< 100 mV), N_{it} near the drain and source regions can be determined. For example, keeping V_S fixed while V_D is varied between $V_S \pm \Delta V$ results in changes in the depletion edge X_D near the drain, from which N_{it} near the drain at V_D or $N_{it}(X_D)$ can be determined from eqn. (4.11) below. In a similar manner, we can determine $N_{it}(X_S)$ from eqn. (4.12).

$$N_{it}(X_D) = \frac{1}{f \cdot W \cdot q} \cdot \left(\frac{dX_D}{dV_D}\right)^{-1} \cdot \left(\frac{dI_{CP}}{dV_D}\right)\Bigg|_{V_S = fixed}. \tag{4.12}$$

$$N_{it}(X_S) = \frac{1}{f \cdot W \cdot q} \cdot \left(\frac{dX_S}{dV_S}\right)^{-1} \cdot \left(\frac{dI_{CP}}{dV_S}\right)\Bigg|_{V_S = fixed} . \qquad (4.13)$$

For the application of the above technique, we configured the system shown in fig. 4.10. The HP 4145B SPA was used to bias the source (channel 3) and drain (channel 4) terminals. The HP 8115A 50 MHz dual channel pulse generator was used to generate square wave pulses needed to pump the gate. A 50 Ω terminator was used in parallel with the gate to obtain proper pulse amplitude from the pulse generator. The charge pumping current (I_{CP}) was monitored using the high precision Keithley 617 electrometer. The wafers were probed on a Karl Suss PM8 manual wafer prober placed inside a shielded box. The whole setup was controlled by HP-VEE graphical programs (developed for this purpose) running on a 486 personal computer.

For our experiments, we used 1 MHz square wave pulses of 5V amplitude. The rise and fall times of the pulses were 7 ns each. These small rise and fall times ensure sweeping the bandgap between Fermi levels corresponding to accumulation and inversion. The base level of the pulses was varied from -7V to 1V. First, we did the experiment with both source and drain grounded for a standard charge pumping measurement. We used a symmetrically laid out device of width 5 µm. The measurement was repeated after 500s of hot-carrier stress under maximum substrate current situation to see the effect of early mode degradation on the charge pumping current. Very little change in charge pumpingcurrent was monitored as shown in fig. 4.11. An $I_{CP,max}$ of about 25 pA amounts to N_{it} of about 5×10^9 /cm^2. It is clear that the channel region of the transistor is unaffected by the early mode degradation. This directly points to the sub-spacer and gate-edge LDD region as the damaged region.

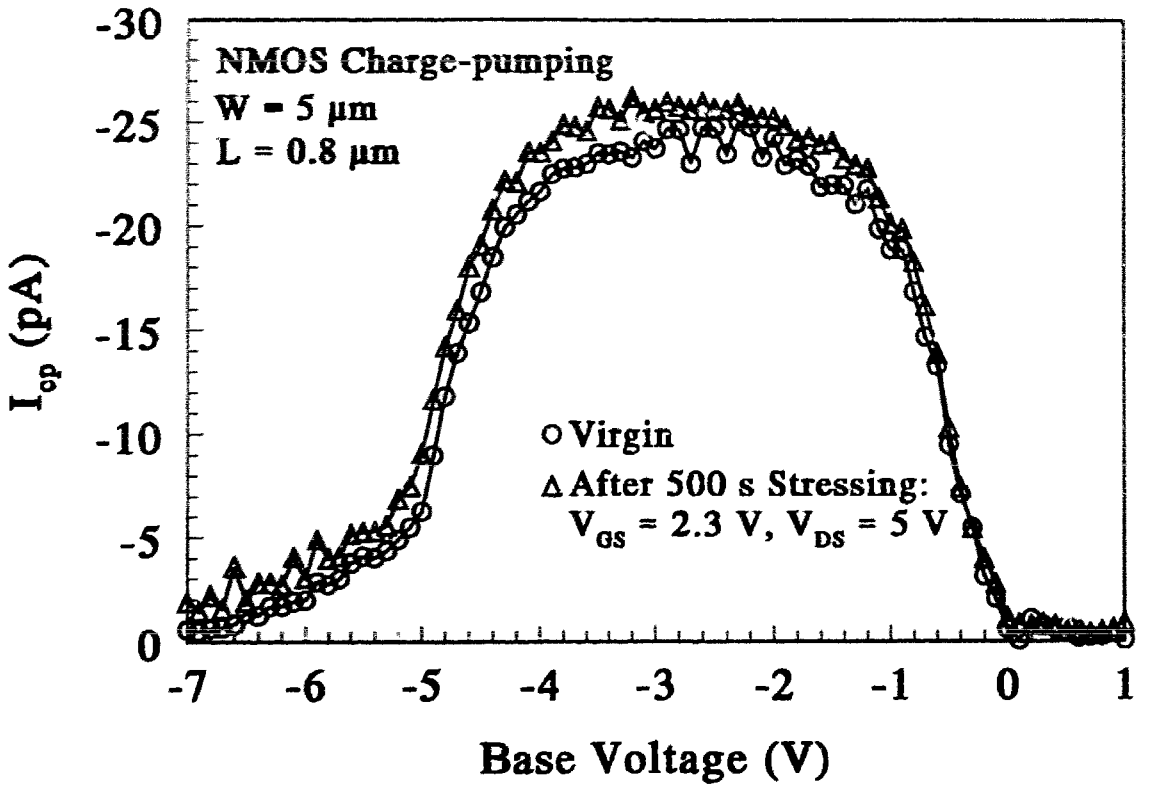

Fig. 4.11. Charge pumping currents with 1 MHz square wave pulses of 5V amplitude before and after early mode degradation.

We then performed the spatial profiling experiment to further investigate the effect of early mode hot-carrier degradation on the distribution of interface traps near drain and source, using the theory discussed earlier. For proper application of the above mentioned technique, proper choice of ΔV is to be made. While theoretically ΔV should be as small as possible, too small a value of ΔV makes measurement of ΔI_{CP} inaccurate. On the other hand, a bigger value of ΔV leads to a higher drain current and hence a larger impact ionization induced substrate current that would interfere with the measurement of ΔI_{CP}. While the optimum value of ΔV should depend on the measurement setup and the devices under test, a value of 50 mV was found reasonable for our situation. This was ascertained by varying ΔV and finding N_{it} at some points on the channel of a MOSFET. The minimum ΔV at which the extracted N_{it} stabilizes was chosen.

The other important issue is that of gate-bias dependent ΔI_{SUB} due to source-drain junction reverse leakage being comparable to ΔI_{CP} for higher drain-source biases. This limits the depth into the channel the above mentioned method can penetrate. However, one must ensure that even for higher drain-source bias combinations used in the experiment, the ΔI_{SUB} is much less compared to $\Delta I_{CP,MAX}$ for corresponding drain-source bias combinations. In our devices, we could go up to 3V for V_D and V_S without this problem affecting the results.

Also, as we used a pulse amplitude of 5V, we needed to ascertain that we do not enter the non-useful falling edge [4.18] of the charge pumping current versus reverse bias on source and drain (tied together, for this case, i.e., V_S=V_D=V_R) up to 3V, for our 0.8 μm device. For this experiment, we used four transistors of varying channel lengths (3 μm, 2 μm, 1.2 μm, and 0.8 μm) and channel width 24 μm. The same setup as shown in fig. 4.10 was used, with V_S=V_D=V_R. We varied V_R and plotted the maximum charge pumping current versus V_R in fig. 4.12.

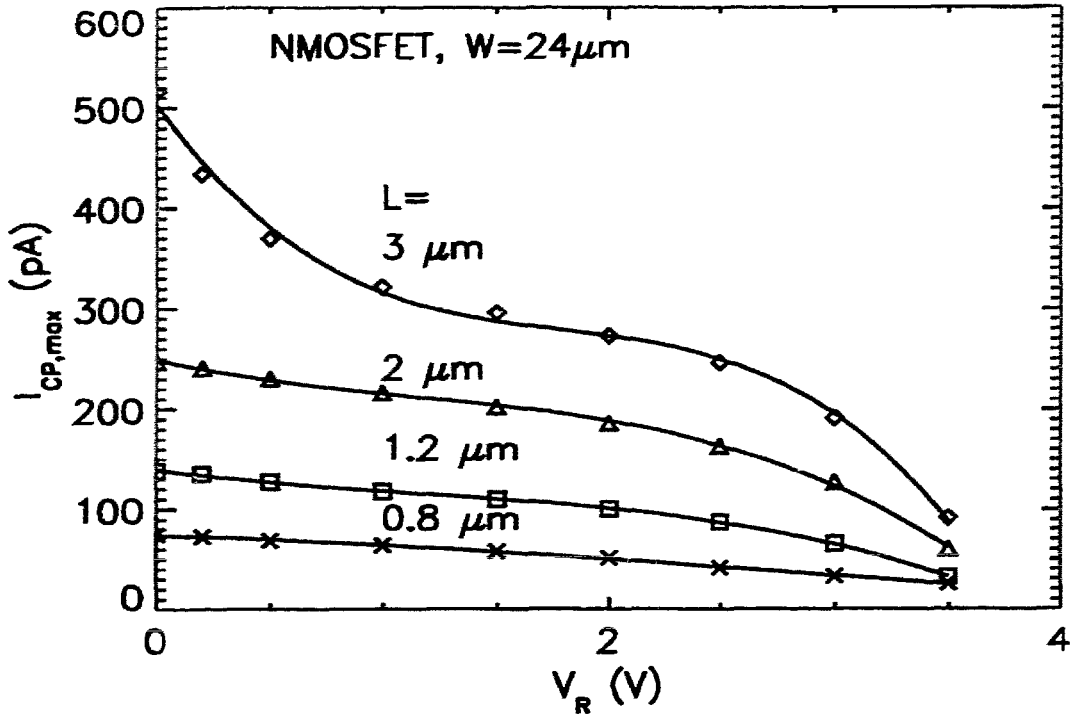

Fig. 4.12. Charge pumping current versus V_R for different channel lengths. Amplitude of square wave pulses applied to the gate was 5 V, with V_S=V_D=V_R.

It is clear from fig. 4.12 that the knee voltage where the charge pumping current starts falling sharply against V_R, increases with decreasing channel length. This is happening due to the short channel effect on the threshold voltage V_T. Also, for the shortest channel length of 0.8 μm that we are investigating for the early mode degradation, the knee voltage is definitely above 3 V. This makes the application of V_S and V_D up to 3 V in our differential spatial profiling technique valid.

The extracted N_{it}'s in the source and the drain side using the spatial profiling technique are plotted in fig. 4.13 below. It is clear that the N_{it}'s near drain increase only a

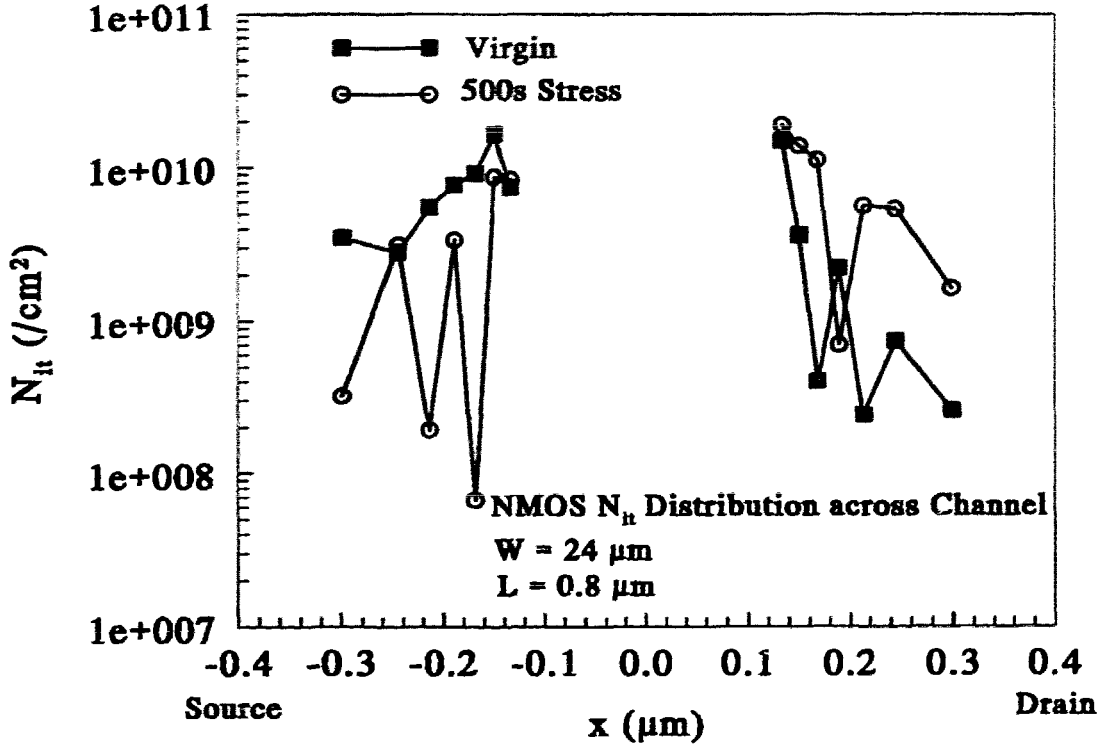

Fig. 4.13. N_{it} distributions near source and drain extracted by spatial profiling charge pumping.

little (less than an order of magnitude) after early mode hot-carrier stress. Also, the values roughly match the $5x10^9/cm^2$ obtained from conventional charge pumping. At the same time, the difference between the N_{it}'s before and after stress tends to decrease towards the centre of the channel. This suggests that the early mode of hot-carrier degradation does not affect the channel region of the transistor in a significant way. On the source side, a little decrease in the N_{it}'s is indicated. This is possibly due to some passivation effect on

account of the charge pumping experiment itself. Another interesting feature of the above observation is that the N_{it} decreases to the substrate-LDD junctions, for the virgin as well as the stressed device. This is in contrast with previous reports [4.7],[4.11]. But, this is not unexpected because the Fermi level sweep of the bandgap near the source/drain edges is expected to be less than that in the middle of the channel.

4.5 Conclusion

In this chapter, we have discussed the measurement techniques, namely floating gate, transconductance, and spatial profiling charge pumping, that we have used to study the effects of the early mode of hot-carrier degradation. The basic principles of these measurement techniques were discussed, and the results obtained from using these techniques in characterizing the features of early mode hot-carrier degradation have been shown. A saturating nature of the early mode degradation was revealed through floating gate and transconductance measurements. The conventional and spatial charge pumping techniques reveal very little increase in the interface trap density in the channel region of the MOSFET. In the next chapter we will correlate some of these results to 2-D simulation that will eventually help us build a model for the dynamics of hot-carrier degradation. At the end, we must mention that the combination of the techniques discussed in this chapter is meant for complete characterization of the Si/SiO_2 interface, right from the source end up to the drain end.

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Chapter 5

Location and quantification of defects using 2-D device simulation and dynamics of defects propagation

5.1 Introduction

The two-stage or saturating nature of hot-carrier degradation in LDD NMOSFETs has been a topic of considerable research [5.1]-[5.6] in the last few years. In [5.1], the authors showed some salient features of this degradation through measurements and simulations. They also pointed out the lack of validity of the conventional method [5.7] for lifetime prediction of these devices. It was noted that the saturating effect was caused by a reduction in the maximum electric field (E_m) due to accumulation of interface charges in the gate edge region. In another work [5.2], it was pointed out that the decrease in E_m was not sufficient to explain the saturation behavior. Rather, a shift in the location of the peak electric field towards the spacer region causes a slowing down of the degradation rate in the channel and gate-overlapped LDD regions. The authors of [5.3] modelled the saturating behavior by considering an increasing barrier height (ϕ_{it}) to defect creation beyond a threshold defect level. Starting with a well-known degradation rate equation [5.8], they could show that while the degradation follows the regular power-law dependence [5.8] on stress time below the threshold level, a logarithmic dependence on time describes the degradation beyond the threshold. The authors of [5.4] have suggested that a modified empirical mobility model [5.9] can be applied to the gate-overlapped LDD region where the defects (N_{it}) accumulate, keeping ϕ_{it}/E_m constant, irrespective of the amount of N_{it}. More recently, the authors of [5.5] have done some detailed investigation into the two-stage nature of the degradation, and suggested that the early mode of the degradation is dominated by a saturating series resistance increase in the sub-spacer

region, followed by a reduction of carrier mobility in the gate-overlapped LDD region and the channel region. This observation is also supported by the authors of [5.6] who have separated mobility degradation from series resistance increase.

The works described in [5.5], [5.6], as well as our own work [5.10], [5.20], [5.21] suggest a movement of the degraded region from the sub-spacer LDD region towards the channel region. In this chapter, we investigate this movement of the damage profile from the early mode of the degradation to the late mode through measurements and 2-D device simulation. We will show how these simulations allow us to better understand the degradation process, and ultimately build a simple model for the growth of the degraded region with stress time. From this model, we conclude that the saturating nature of the degradation is due to the saturating characteristic of the growth of the damage profile, as opposed to decreasing E_m [5.1] or increasing ϕ_{it} [5.3].

We will first locate and quantify the early mode defects by correlating the measurement results of chapter 4 with 2-D device simulation.

5.2 Device and simulation details

All devices simulated for, are the same as those described in section 4.2. Process simulation was performed using a virtual factory program [5.13] that uses a TSUPREM-4 [5.14] 2-D process simulator. Process simulation matched the fabrication details closely. Also, the initial simulation grid was generated automatically using mask information.

Device simulation was performed using a MEDICI [5.15] 2-D device simulator. We used an analytic mobility model [5.16] for calculation of drain currents. An energy balance solution [5.17] was performed to determine mean electron temperatures. Also, a post processing temperature-dependent impact ionization analysis [5.15] was performed to calculate substrate currents. The gate currents were calculated using a temperature-

dependent Lucky-Electron Model [5.18] as implemented in MEDICI. The capability of MEDICI to place charges on oxide nodes was used to place and study the effect of defects.

5.3 The simulation framework

The evolution of the parasitic drain resistance R_D during early mode hot-carrier degradation was extracted using the transconductance technique discussed in chapter 4 (see fig. 4.9). The corresponding evolution in the barrier height ϕ_b to gate current injection was extracted using the floating gate technique and also discussed in chapter 4 (see fig. 4.7). The correlation between these two evolutions is remarkable, and is shown in fig. 5.1 below.

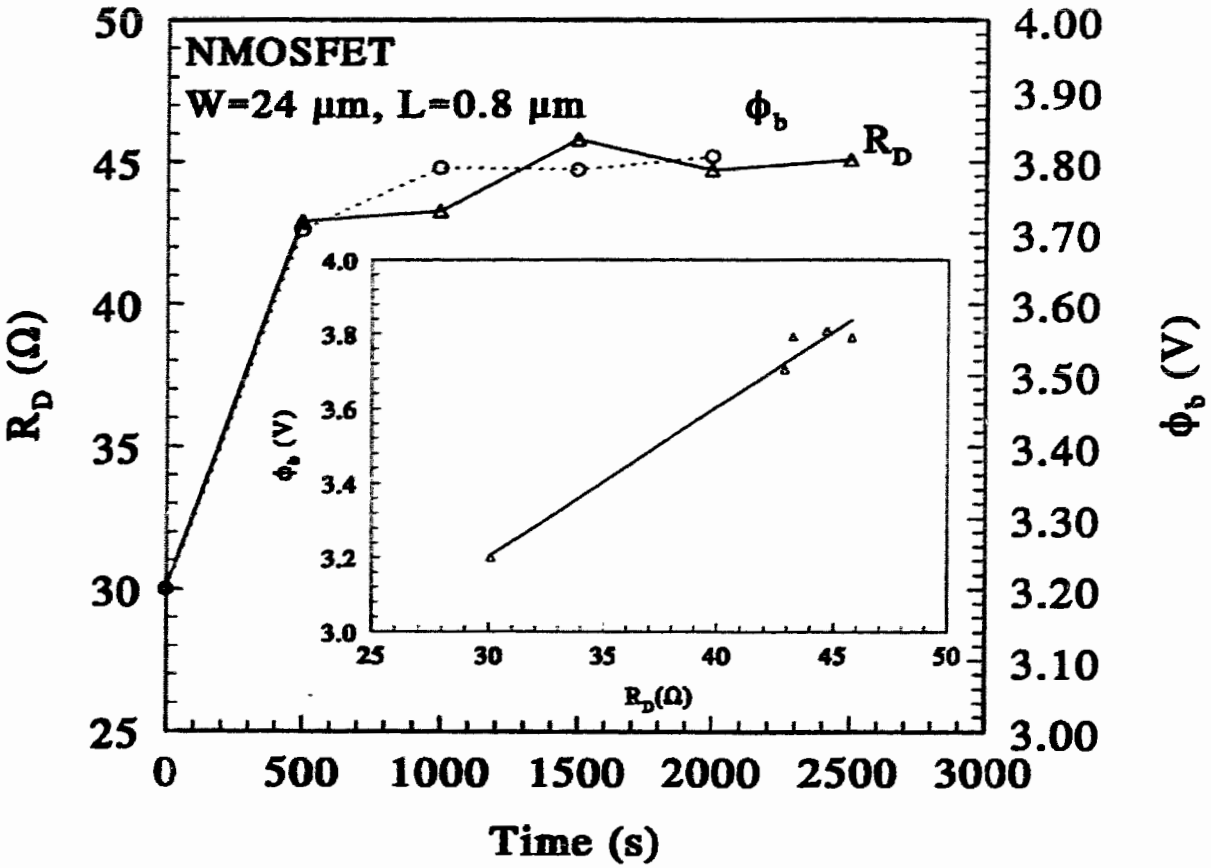

Fig. 5.1. Correlation between the evolutions in R_D and ϕ_b during the early mode of hot-carrier degradation.

The almost linear correlation between the two evolutions is evident (see inset of fig. 5.1). The correlation between R_D and ϕ_b points to a common cause, namely, trapped negative charges in the oxide. These charges, on the one hand, increase the potential barrier to electron injection into the oxide, and, on the other, depletes the underlying silicon - giving rise to an increment in the drain-side parasitic resistance, R_D. We suspect the weaker oxide in the gate edge region [5.1], partly under the gate and partly under the spacer oxide, to be the location of the trapped negative charges produced in the early-mode hot carrier degradation. Assuming that the charges are distributed over about 100Å above the interface, we derive the eqn. (5.1) from Poisson's equation. We then calculated the number of charges from the net change in ϕ_b of about 0.6 eV as seen in fig. 5.1.

$$\Delta\phi_b = \frac{N_t \cdot d \cdot q}{C_{0.5d}} \tag{5.1}$$

Here N_t represents the magnitude of the trapped charge in numbers per cm^3, d the vertical width of the charge distribution (100 Å in our case), q the electronic charge ($1.6x10^{-19}$ C), and $C_{0.5d}$ the capacitance due to half the oxide (690 nF/cm^2 for 50 Å oxide in our case) thickness of the bounding box (assuming the charge to be uniformly distributed). For $\Delta\phi_b$ of 0.6 eV, we obtained $N_t \cong 2.5x10^{18}/cm^3$ from eqn. (5.1) above. This charge was placed in the gate edge region as indicated by the Region 1 in fig. 5.2 below. This Region 1 extends from under the gate where the simulated electron temperatures peak in the virgin device into the spacer oxide over 400 Å length. Of this length, 200 Å is under the gate, and 200 Å outside it. We arrived at this location of defects after repeated simulations involving placement of negatively charged defects at various locations in the spacer and sub-gate region oxides above the LDD region, and qualitatively matching the simulated electrical characteristics with the experimental ones as indicated in the next section.

This placement of charges is seen to increase the electron temperature peaks in magnitude, and attract them outwards [5.2] to the outer edge of the damage region. Also,

the electron temperature magnitude corresponding to the peak electron temperature for $V_{GS} = 7V$ moves inwards with decreasing gate bias. This indicates that in the floating gate measurement, the damage profile moves inwards with decreasing gate bias. The vertical potential profile through the peak electron temperature in the damaged device with the

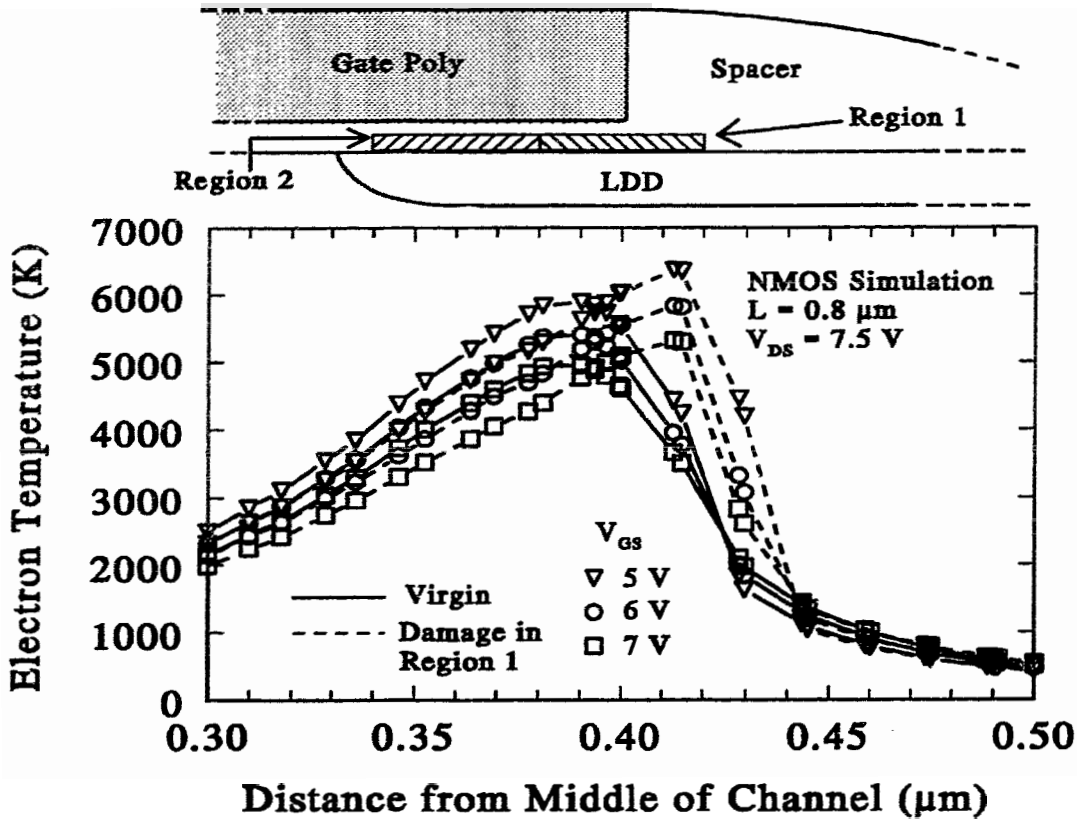

Fig. 5.2. Lateral electron temperature profiles for virgin and damaged device (with damage in Region 1).

defects placed as above in the gate edge region (Region 1) was obtained from simulation. This is depicted in fig. 5.3, in contrast with the vertical potential profile for the virgin device, again drawn through the peak of lateral electron temperature profiles in the virgin device. The potential barrier of about 0.6 eV going from silicon into oxide in the case of the damaged device supports the calculation in eqn. (5.1). Also, the simulated gate currents for the virgin as well as the damaged device (damage in Region 1) are shown in fig. 5.4. We observe the matching decade drop in simulated gate currents at $V_{GS} = 7V$, as was observed experimentally in fig. 4.6 of chapter 4. However, the experimentally

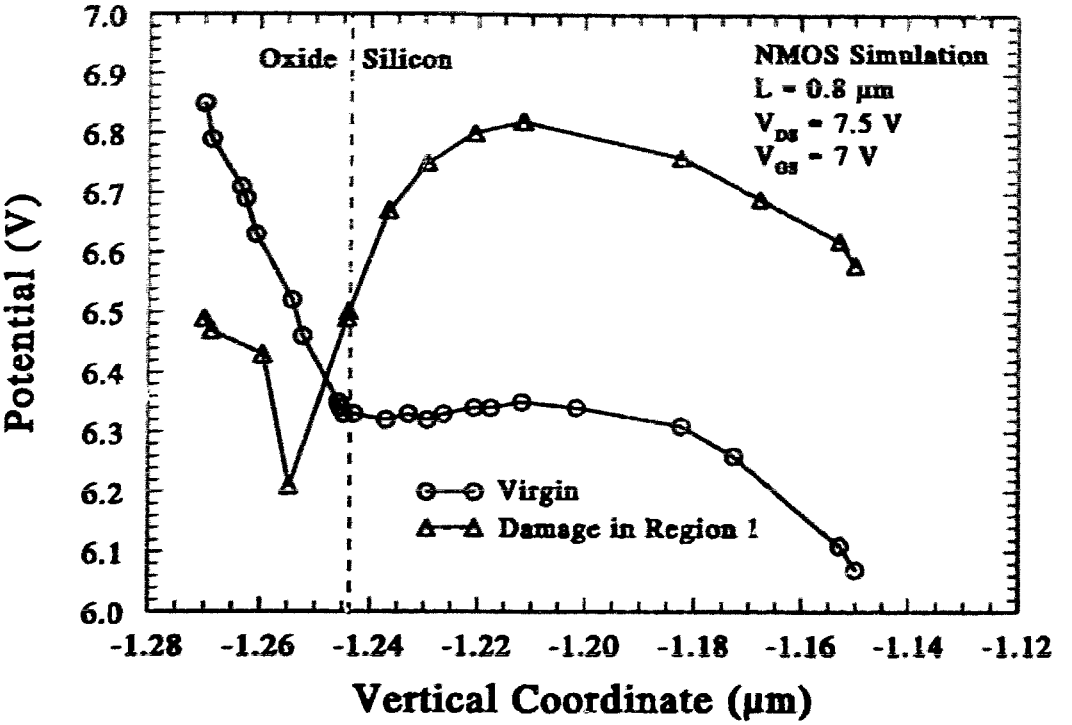

Fig. 5.3. Simulation of the vertical potential profiles at the peak of lateral electron temperature profiles (see fig. 5.2).

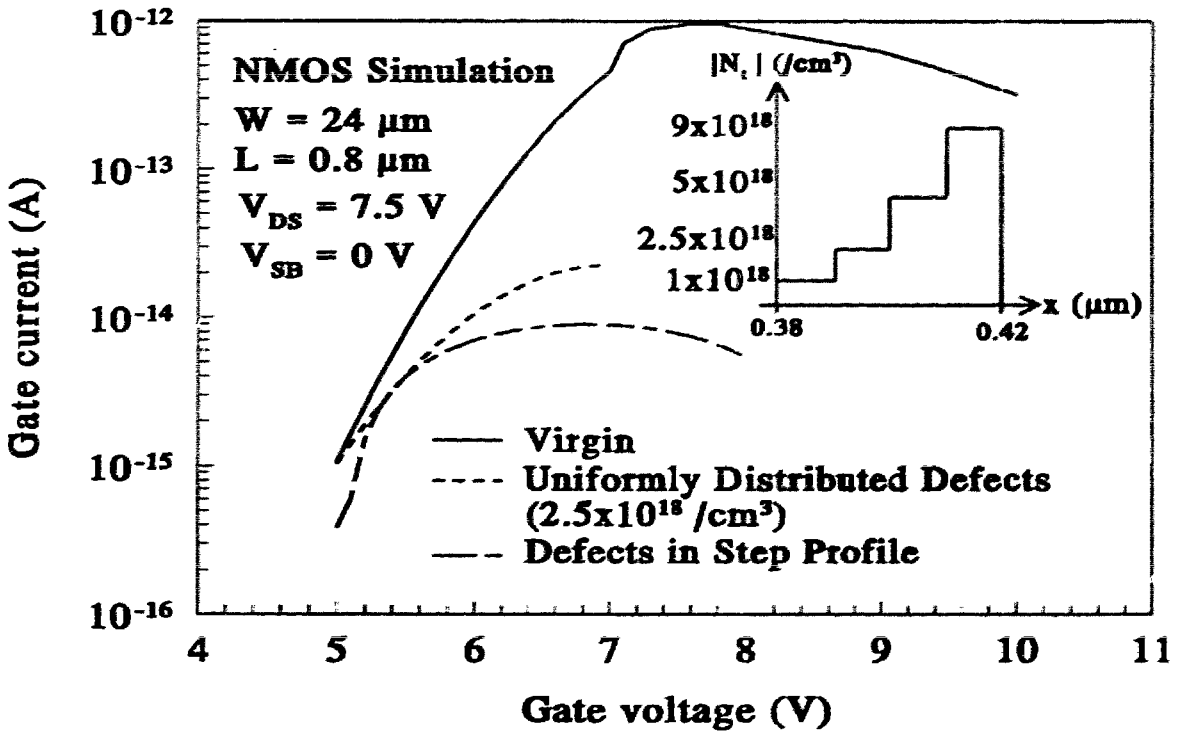

Fig. 5.4. Gate currents simulated for the virgin device as well as for the device with defects in Region 1 of fig. 5.2. Inset shows the step profile of defects used.

observed shift in the gate current peaks could not be obtained in simulation. We suspect that this is due to the non-uniform nature of the defect distribution in the real device, going from spacer into the device. In contrast, we assumed a uniform defect distribution in the simulated device. To test this hypothesis, we performed a simulation with a step profile in defects as shown in the inset of fig. 5.4. Indeed, a shifted peak in the gate current is observed with this more realistic defects profile. The abscissa of the defects profile corresponds to the abscissa of fig. 5.2.

The location of the defects in Region 1, however, raises the question as to how the defects initiate at a point beyond the electron temperature peaks for the fresh device, as shown in fig. 5.2. We think that this can happen in two ways. First, some weak interfacial region or existing traps can initiate the degradation at a point slightly removed from the electron temperature peak; or second, a non-local effect as suggested in [27] can start the degradation beyond the electron temperature peak.

5.4 Region 1 versus Region 2

As discussed earlier, in order to confirm that the location of the defects in the early mode hot carrier degradation is indeed the gate edge region (Region 1) as opposed to any other location, we performed a number of simulation experiments. In these experiments, defects were placed alternately in different possible locations, and the simulation results were matched with measurements. Of particular interest was the under-the-gate LDD region indicated by Region 2 in fig. 5.2. In this section we show how our simulation experiments help us identify Region 1 as the location of early-mode defects, as opposed to the Region 2, for example.

5.4.1 Substrate currents

The results of the first of these experiments are shown in fig. 5.5. In this case the measured substrate currents during the floating gate experiments are compared with the

simulated I_B's. The measured I_B's after FG cycle #2 did not change much, and hence they have been omitted from the figure. It is clear from simulation that defects placed in Region 2 increase the substrate current. This matches with the late mode degradation results as observed by us (fig. 4.2 of chapter 4), as well as by the authors of [5.5]. However, placement of defects in Region 1 produces qualitatively similar results as with the early mode measurements during the FG cycles (fig. 5.5) and normal stressing experiments (fig. 4.2 of chapter 4). Early mode experimental results obtained by the authors of [5.1], [5.5] are also similar. It must be mentioned here that we were not able to match the peaks of simulated I_B's with those of measured I_B's. But, in this case we were mainly interested to check the increase or decrease in the peak value. The extension of the

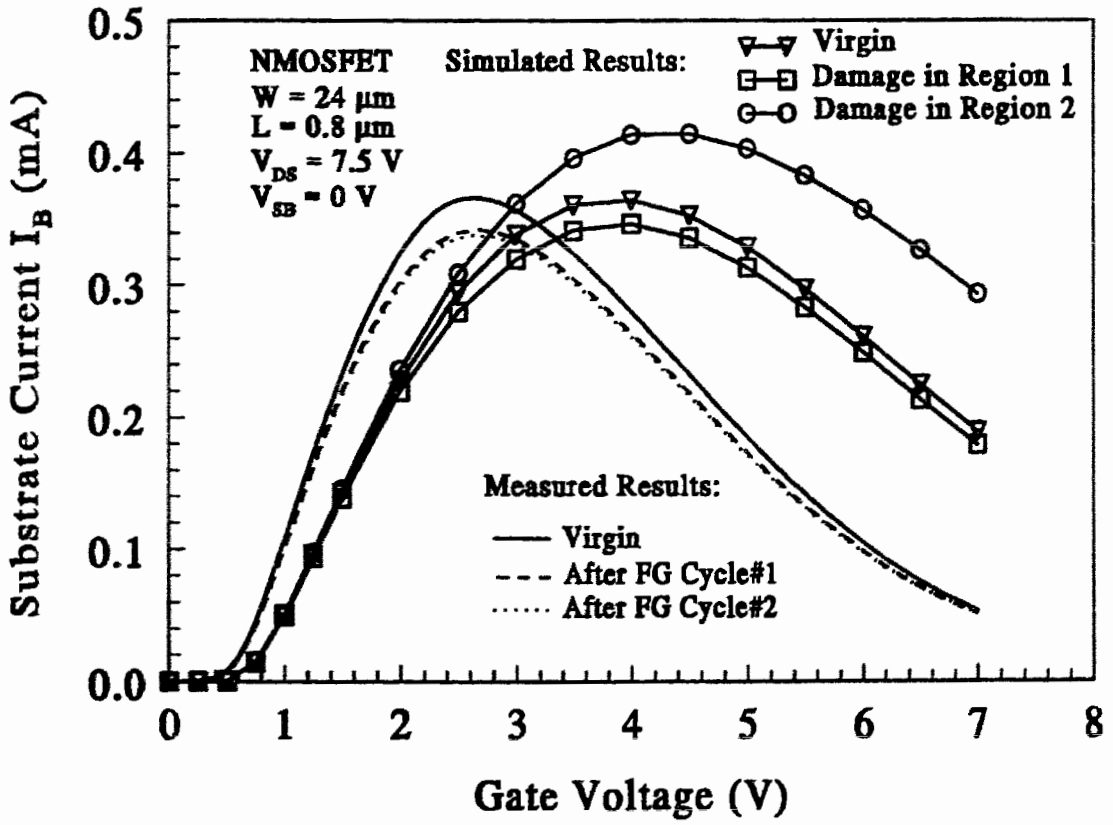

Fig. 5.5. Decrease of measured I_B with the FG cycles. The current does not change much after the FG cycle #2. Simulated I_B for virgin and damaged (both Regions 1 & 2 of fig. 5.2) devices suggests that the probable location of damage is Region 1 (gate edge).

defect profile from the sub-spacer LDD region to the gate-overlapped LDD region going from the early mode to the late mode can be inferred from this simulation experiment.

5.4.2 Linear currents

In the second experiment, shown in fig. 5.6, the measured degradation in linear current was matched with the simulated ones with the defects placed alternately in Region 1 and Region 2. The measured degradation was monitored for the linear *I-V* characteristic after the 5th FG cycle with respect to the virgin device for different V_{GS} biases. It may be

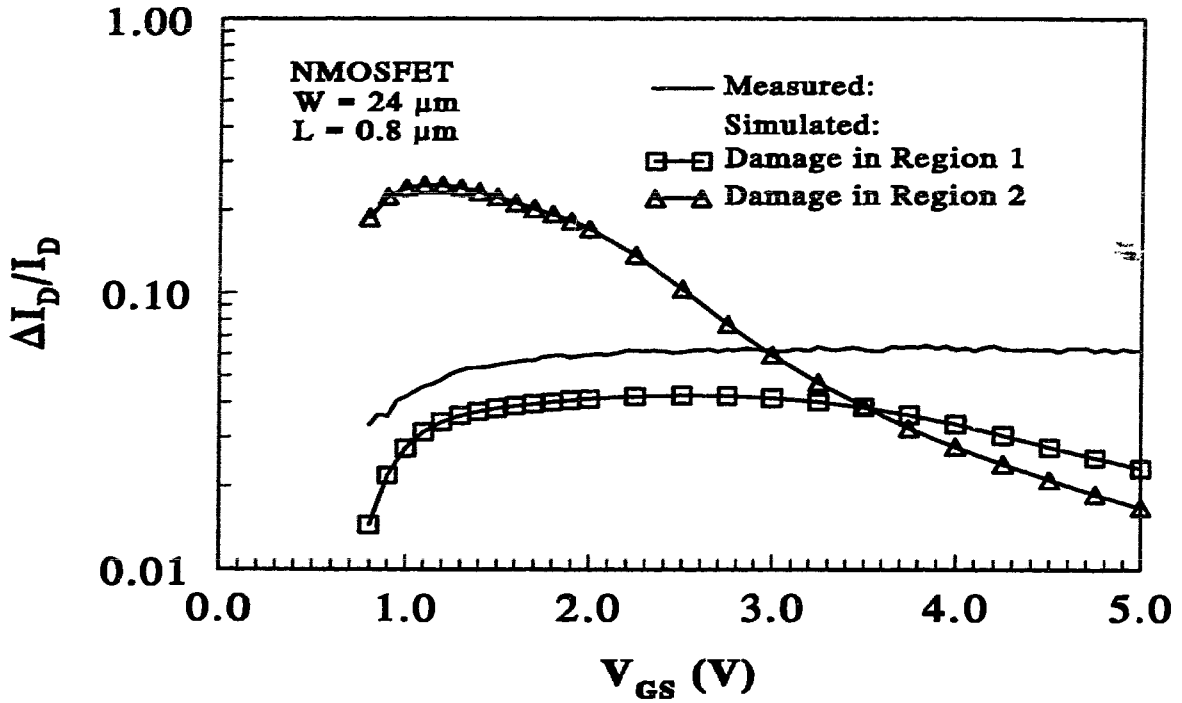

Fig. 5.6. Measured linear current degradation vs. gate bias over the 5 FG cycles matches better with the simulated values for damage in Region 1.

mentioned here that similar degradation characteristic was also observed by the authors of [5.5] in the early stages of the degradation process. Again, placement of defects in Region 1 qualitatively matches the measured degradation behavior during FG cycles that correspond to the early mode degradation. On the other hand, the placement of defects in Region 2 produces results similar to the case of late stages of degradation behavior shown

in [5.5], as well as that in fig. 5.7 for our device. This latter device was from another wafer that had no layout asymmetry between source and drain. A combination of threshold

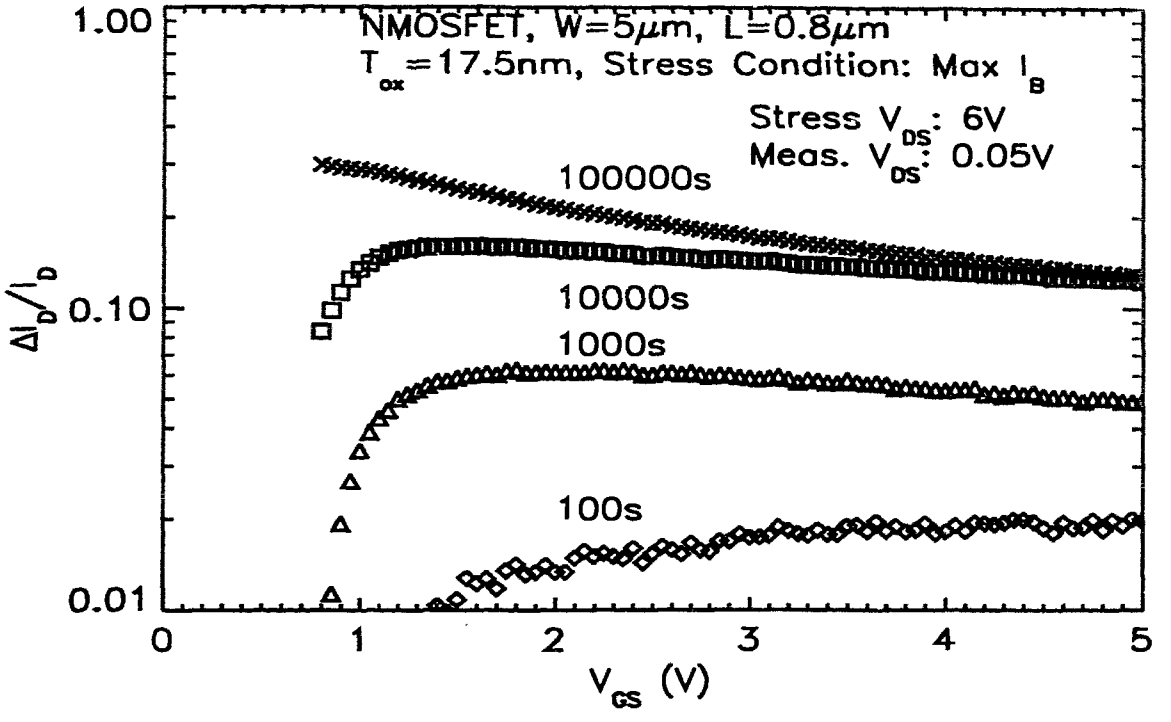

Fig. 5.7. Linear current degradation versus measurement gate bias at various stress times. Measurement was done in the forward mode.

voltage (V_T) shift and mobility degradation seems to be the cause of the late mode degradation behavior. Thus, the results shown in figs. 5.6 and 5.7, coupled with the nature of lateral electron temperature profiles of fig. 5.2 suggest that the defects, first created in the weaker spacer oxide region move inwards with time.

5.4.3 Saturation currents

In another experiment, shown in fig. 5.8, the voltage shifts in the degraded saturation I_{DS}-V_{GS} characteristics with respect to the virgin device were monitored at fixed saturation currents. The measurements and simulations were performed in the reverse mode. Again, placement of defects in Region 1 produces results that qualitatively match the measurements. On the other hand, defects in Region 2 yield much bigger and nearly

constant shifts. This indicates V_T shift for the case with defects in Region 2. To check the simulated late mode characteristic of the defects, we performed degradation measurements on saturation currents measured both in reverse and forward modes. These results are shown in figs. 5.9 and 5.10 respectively. For these measurements, the stressing was done in maximum substrate current situation on. The device used was the same as the one characterized in fig. 5.7. There is strong qualitative similarity between the early mode (100s) degradation of the reverse saturation current as shown in fig. 5.9 with the simulated voltage shifts when defects are placed in Region 1 as shown in fig. 5.8. This is the predominant effect of increasing R_D in the early mode that manifests only on the reverse saturation current, but not on forward saturation currents as evident from fig. 5.10 where the early mode voltage shifts are negligible.

On the other hand, the late mode (100000s) voltage shifts in the reverse mode

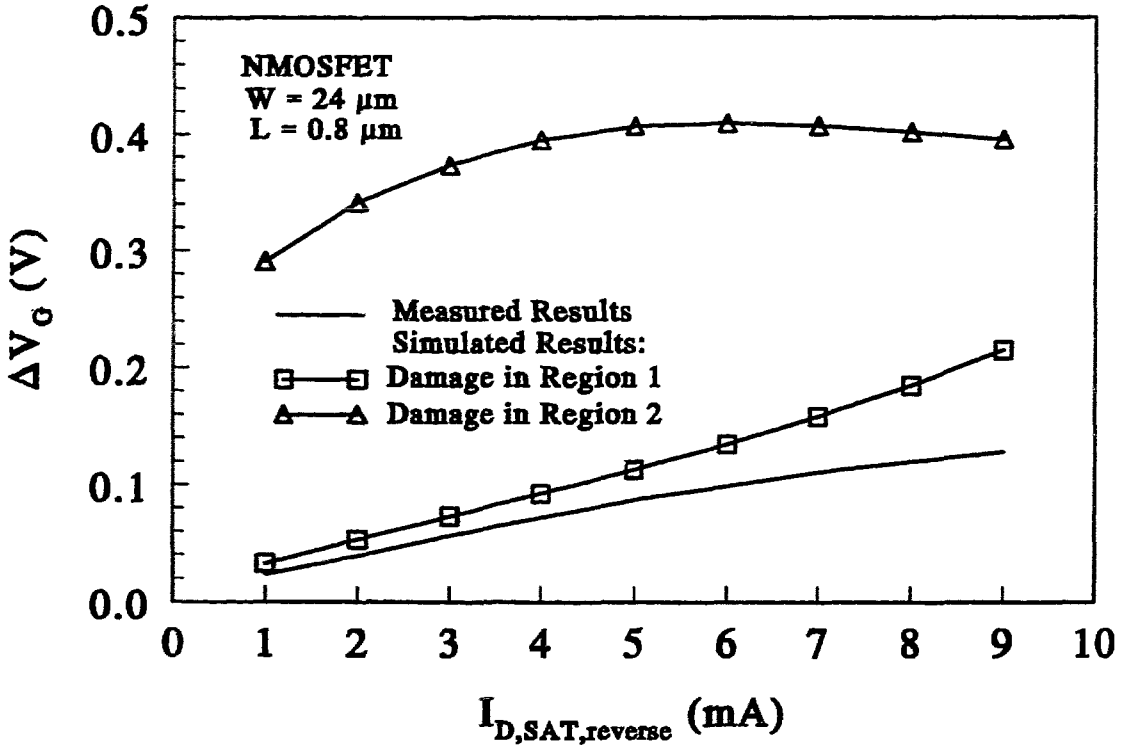

Fig. 5.8. Measured voltage shift in the reverse $I_{D,sat}$ vs. V_{GS} curve with V_{DS}=5 V over the 5 FG cycles matches better with the simulated values for damage in Region 1 (see fig. 5.2).

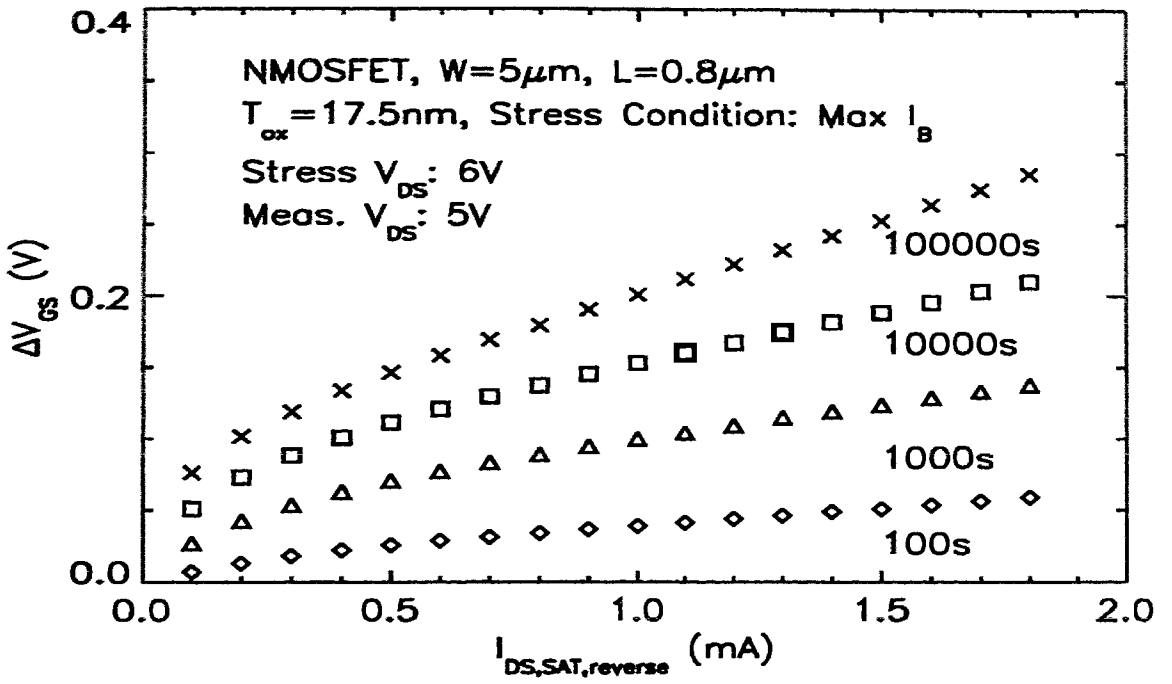

Fig. 5.9. Measured voltage shift in the reverse $I_{D,sat}$ vs. V_{GS} curve over hot-carrier stress experiment.

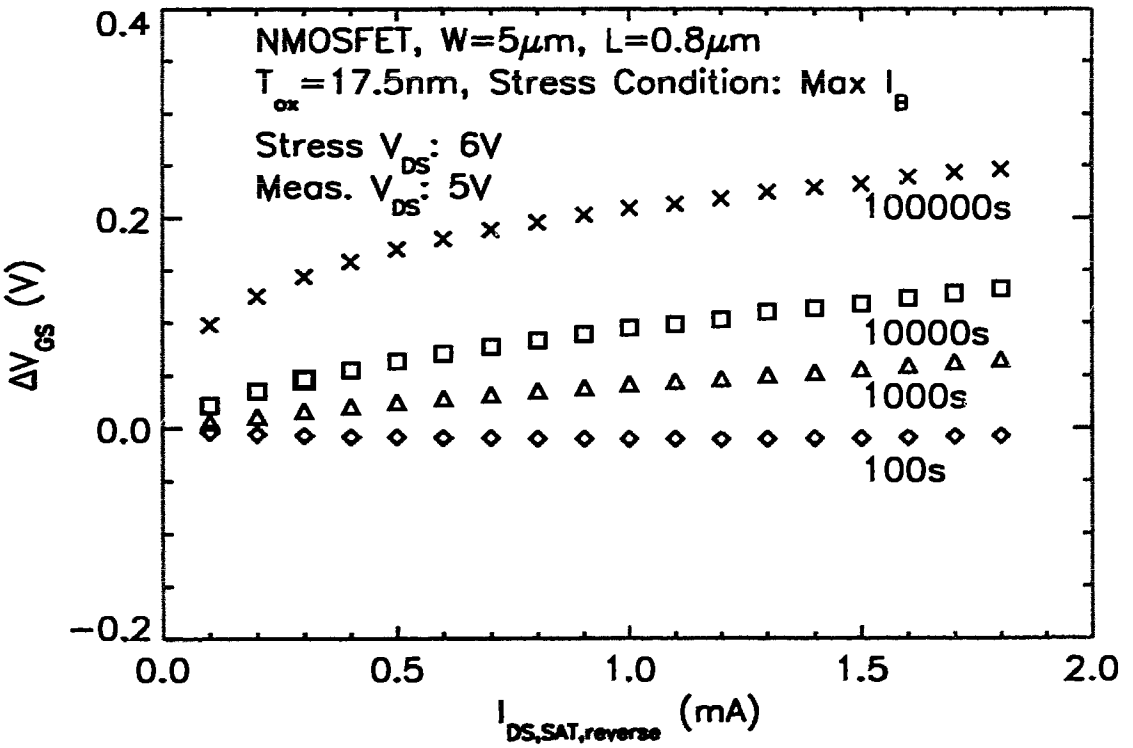

Fig. 5.10. Measured voltage shift in the forward $I_{D,sat}$ vs. V_{GS} curve over hot-carrier stress experiment.

(fig. 5.9) represent a combined effect of increasing R_D, threshold voltage (V_T) shift, and mobility degradation. Since, in simulation with defects in Region 1, we did not also place defects in Region 2, the effect of R_D is less prominent in that case. That is why, we see a saturating nature of the voltage shifts in simulation, as opposed to a rising nature in the late mode voltage shifts in fig. 5.9. On the contrary, for the forward mode measurements (fig. 5.10), we see a saturating nature in the late mode voltage shifts. This is due to the fact that R_D no longer plays a role in these voltage shifts. On the whole, these simulations and measurements indicate that there is indeed a movement of the defects from the early mode to the late mode.

5.4.4 R_S increase?

As suggested in fig. 4.9 of chapter 4, there is an apparent increase of R_S after early mode degradation. As discussed earlier, this increase in R_S was extracted from the saturation transconductances measured in the forward mode, in course of the floating gate

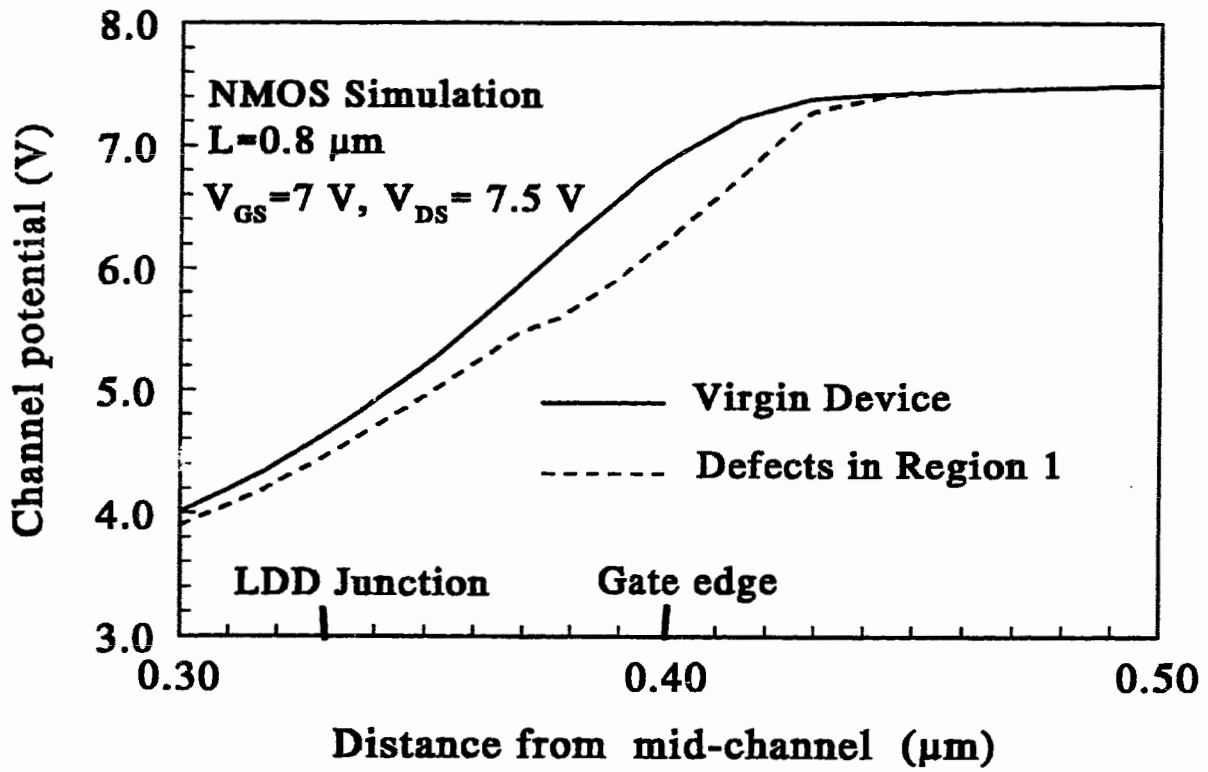

Fig. 5.11. The simulated channel potential profiles near drain, for the virgin device, and the device with defects in Region 1.

measurements. We also observed a slight drop in the forward saturation currents in simulation with defects in Region 1. In order to investigate this issue we looked at the simulated channel potential profiles near drain, for the virgin device, as well as for the device with defects in Region 1. These profiles are drawn in fig. 5.11. As can be seen, there is a shift (about 0.01 μm at the LDD junction) in the potential profiles to the drain side after the early mode of degradation. This causes an increase in the channel length of the device, resulting in lower currents. Thus the apparent increase of R_S is not real, it is an effect of the early mode degradation when the electrical activity near the drain gets pulled outwards due to defects generation on the gate edge.

5.4.5 Behavior of substrate currents

We have observed in fig. 5.5 that during the early mode of hot carrier degradation, the substrate current decreases, and that it corresponds to placement of defects in the Region 1. At the same time, placement of defects in Region 2 increases the substrate current. f To explain this behavior of substrate currents, we extracted the vertical electron

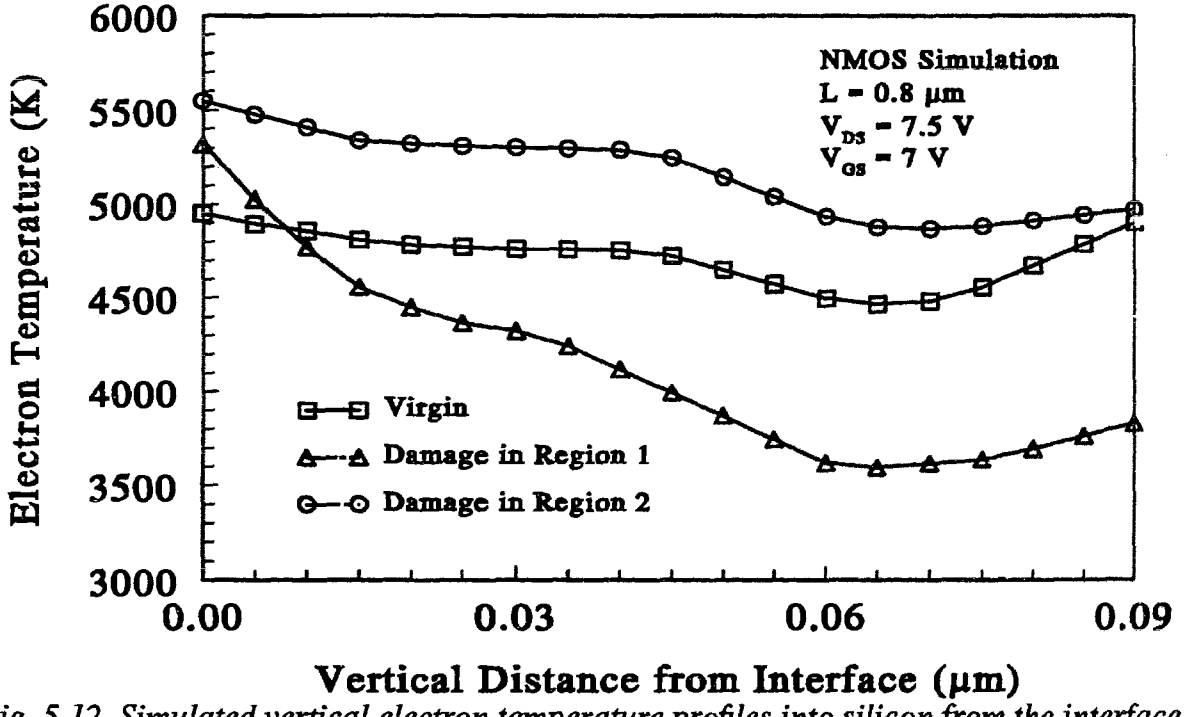

Fig. 5.12. Simulated vertical electron temperature profiles into silicon from the interface through the lateral electron temperature peaks (as in fig. 5.2). Sharp fall for damage in Region 1 is notable.

temperature (fig. 5.12) and vertical current density profiles (fig. 5.13) into silicon through the lateral electron temperature peaks. It is clear from these profiles that the electron temperatures at the interface always increase irrespective of the position of the defects. This observation is contrary to earlier claims [5.1], [5.5] that channel electric field decreases with increasing series resistance on the drain side during the early mode degradation. However, we observe here that the electron temperature falls quickly below the surface in the case of defects in Region 1, and the currents are pushed down to the regions of lower electron temperatures in this case. The latter effect is more prominent in the case of defects in Region 1 rather than those in Region 2 due to stronger gate control of Region 2 defects. The reason for the sharp fall in electron temperatures in the case of Region 1 defects is as follows. As the current carriers are pushed down by the defects,

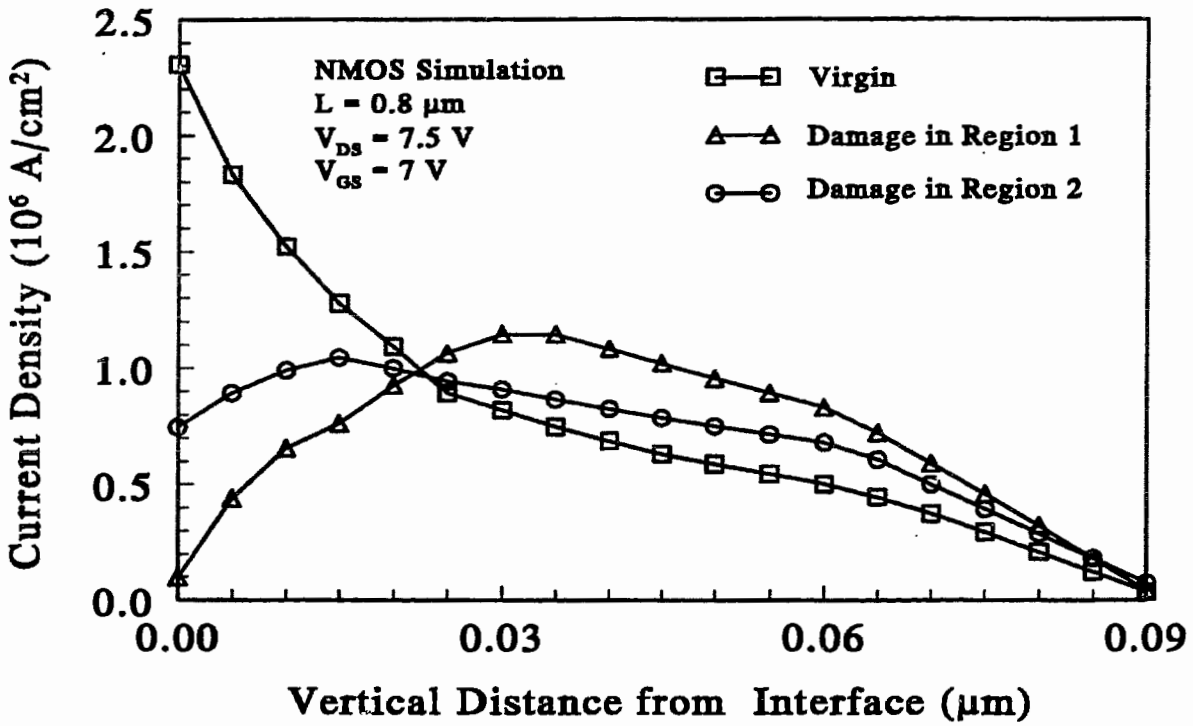

Fig. 5.13. Simulated current density profiles into silicon from the interface through the lateral electron temperature peaks (as in fig. 5.2). The profile gets pushed inwards for damage in Region 1.

they are forced to traverse a longer path between two points at the interface (we verified this with our simulation results). This cools them down due to increased scattering. This

observation cannot be fully explained by earlier reports [5.1], [5.5] that channel electric field decreases with increasing series resistance on the drain side during the early mode degradation. Because, a decreasing channel electric field would give rise to uniformly decreasing electron temperatures from interface downwards. That is clearly not the case as shown in fig. 5.12. The 2-D nature of current flow in this region should be taken into account. In fact, we find that the more appropriate electric field term to consider is $\boldsymbol{J}.\boldsymbol{E}/|\boldsymbol{J}|$, where, $\boldsymbol{J}$ and $\boldsymbol{E}$ represent the local current density and electric field vectors respectively. The maxima of this electric field term at the interface when plotted along the channel is found (not shown here) to precede the electron temperature peak, and also increase in magnitude over that with the virgin device. It appears that the electrons are acquiring a vertical component of the electric field that forces them to travel sub-surface.

5.5 Defects growth model

The authors of [5.1], [5.5] have contended that the saturation of drain series resistance takes place due to inversion of the gate-edge LDD region. But, our experimental results shown in fig. 5.1 suggests that the saturation of R_D correlates very well with the saturation of ϕ_b that is due to the filling up of all available defect sites which number about $2.5\text{x}10^{12}/\text{cm}^2$ in our case, as obtained from simulation. This number matches well with $10^{12}/\text{cm}^2$ reported in [5.12], $1.2\text{x}10^{12}/\text{cm}^2$ reported in [5.22] but somewhat higher than $4\text{x}10^{11}/\text{cm}^2$ reported in [5.2]. In comparison, the charge pumping results of chapter 4 suggested an increase in interface charge of the order of $\sim 10^9/\text{cm}^2$ in the channel region near drain for the early mode degradation. Clearly, this region is ruled out from consideration of early mode degradation.

Although we do not have any other experimental evidence to support the idea of saturation of defect sites of a particular area density, we would not obtain saturating ϕ_b in fig. 5.1 if this did not happen. Also, the presence of a finite number of chemical bonds

available to break makes one expect a constant number of available defect sites at a particular location. This situation, coupled with the simulation experiments discussed in the previous section, and the damage-shifted lateral electron temperature profiles of fig.5.2 point to the following model for the saturating hot-carrier degradation for the LDD NMOSFET.

The defects are first created in the spacer-LDD interface region. These negatively charged defect sites pull the electron temperature maxima, $T_{e,max}$ (see fig. 5.2), as well as the corresponding lateral electric field maxima (E_m) to the defect location. Defect sites saturate with electrons, but the electron temperature profile, as well as the corresponding lateral electric field profile gets stuck to that location. With further stress, the location next to the saturated location gets filled up with electrons. But, this takes longer due to the lower temperature/electric field below it, and so on. Thus the growth of the degraded

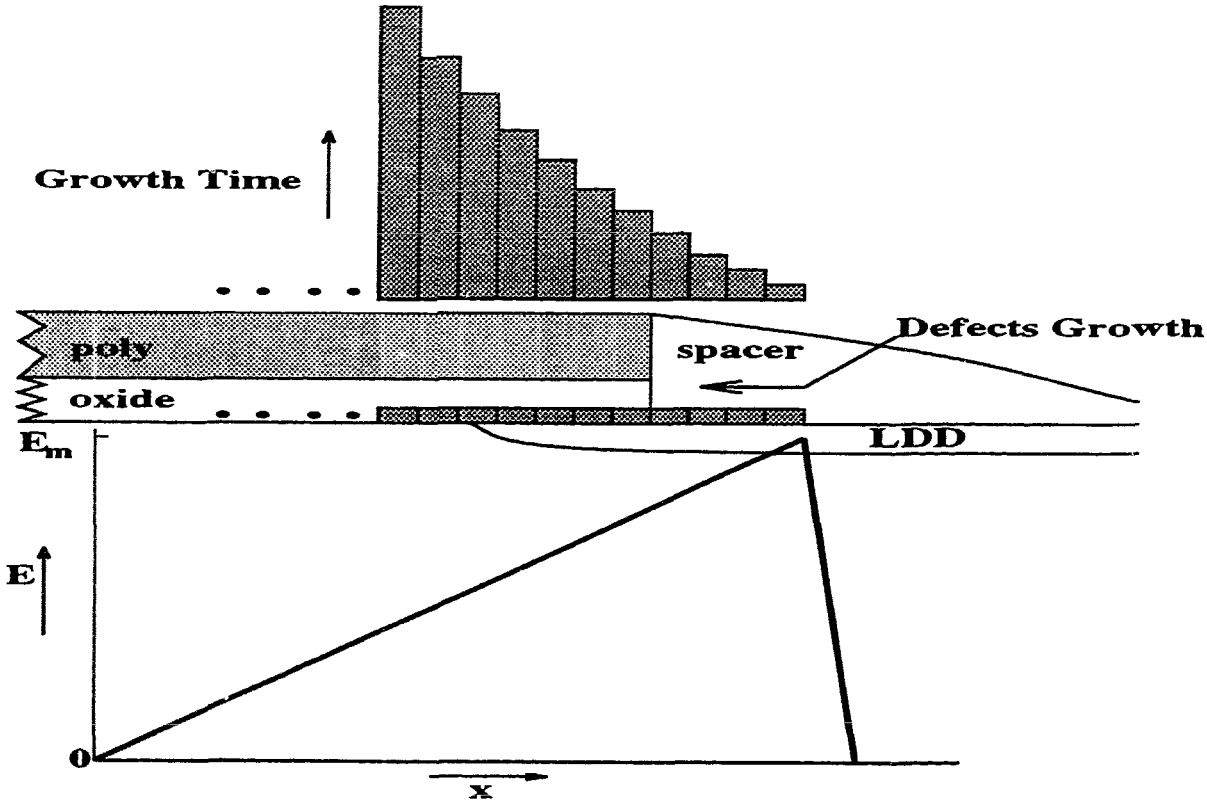

Fig. 5.14. The schematic picture of the growth of the degraded region. The electric field profile is inferred from fig. 5.2.

region proceeds at increasingly slower rates with time. Hence, we obtain a saturating growth of the degraded region with time. This situation is schematically shown in fig. 5.14

With this scheme in mind, and assuming a constant density of defect sites N_{it} along the length of the degradation, and given by an empirically correct [5.4] unknown function $F(t\cdot(I_D/W)\cdot\exp[-\phi_{it}/(q\lambda E)])$ [5.3], where λ is electron mean free path, W is device width, q is electronic charge, and E is the local lateral electric field, we can conceive the extension of the defect profile with time as depicted in fig. 5.15. It must be mentioned here that N_{it}

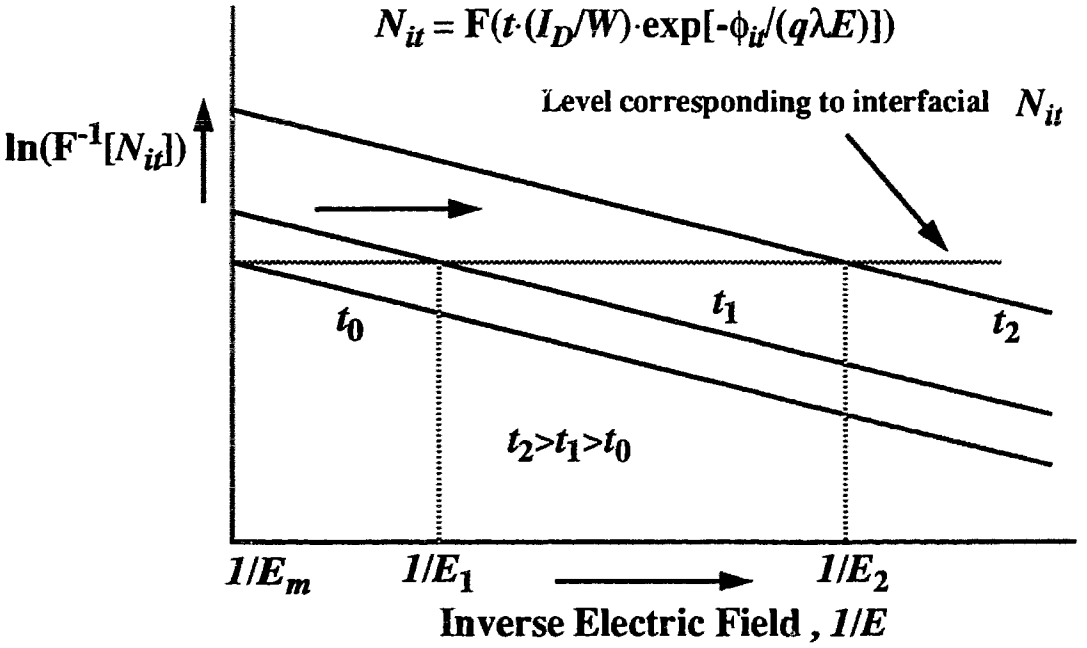

Fig. 5.15. An analytical scheme that corresponds to the picture presented in fig. 5.14. In this case we assume a constant value of the density (N_{it}) of interface traps along the length of degradation.

represents the integrated oxide trap density N_t (volume density, /cm^3) used in our simulations earlier. It is, therefore, analogous to electron filled interface traps. While the actual interface trap occupancy is dependent on the local electron quasi-Fermi level, i.e., the combination of gate and drain biases, our simplified analysis assumes them to be entirely filled with electrons and distributed uniformly along the degraded region. Each of the advancing parallel lines represents the function $\ln(F^{-1}[N_{it}])$ at various increasing times

t_0, t_1, t_2, etc., where t_0 is the initial time instant when the region close to the injection peak gets saturated with defects. Based on this model, and assuming that the lateral electric field falls linearly into the channel from its maximum value E_m at the outer edge of the damage profile with same slope s as do the electron temperatures in fig. 5.2, we can obtain an equation (5.2) for the length x of degradation versus time.

$$x = \frac{\frac{E_m}{s} \cdot ln(\frac{t}{t_0})}{\frac{\phi_{it}}{q\lambda E_m} + ln(\frac{t}{t_0})}. \tag{5.2}$$

In order to plot x vs. t using the above eqn. (5.2), we use, $E_m = T_{e,max}/8.5\text{x}10^{-3}$, λ = 7.3 nm, and ϕ_{it}/q = 3.7 V from [5.19]. The length E_m/s over which the electric field/ electron temperature falls to 0, was calculated from fig. 5.2 for the case of V_{DS}=7.5V, and V_{GS}=5V, and was found to be 0.18 μm. This value appears to be independent of V_{GS}, but higher than the length of the velocity-saturation region, l given [5.19] by $l = 0.22(t_{ox})^{1/3}(x_j)^{1/2}$, which, for our case, evaluates to 0.125 μm. This is not unexpected, considering the fact that electric field does not vanish at the velocity saturation point (or pinch-off point). We can, therefore, simplify the equation (5.2) by using a constant l' in place of E_m/s. After doing this substitution, and using the values of the constants as noted above, we obtain

$$x = \frac{l' \cdot ln(\frac{t}{t_0})}{\frac{5.1x10^6}{E_m} + ln(\frac{t}{t_0})}. \tag{5.3}$$

The above equation directly suggests that, initially, when t is close to t_0, x increases logarithmically with stress time. But, later on, when $\ln(t/t_0)$ becomes greater than the first term in the denominator, x gradually saturates to l'. This behavior of x vs. t is evident from the plot in fig. 5.16 for the simulated electron temperature profiles of fig. 5.2. For this

curve t_0 was taken to be 100s, to roughly match the degradation length after the early mode (~2500s) degradation corresponding to the FG experiment. This figure suggests that it will take about 10 years to reach a degradation length of just above 0.1 μm. It is apparent that for higher values of E_m (lower V_{GS}), x saturates earlier. This is observed in our degradation experiment (fig. 1), as well as in the works of [5.1], [5.3]-[5.5]. In fig. 5.16, we also plot x vs. t for the case of V_{GS}=7V using the formula [5.19] for l discussed

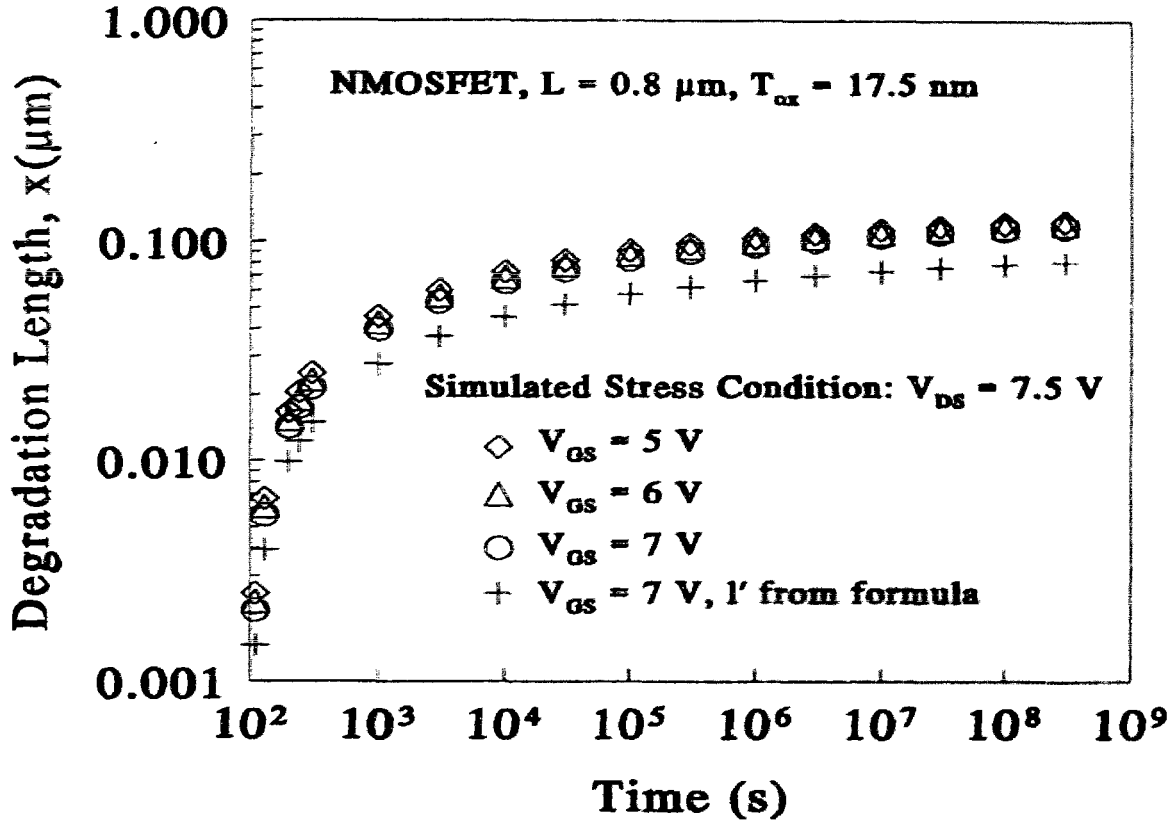

Fig. 5.16. The model for the growth of degradation length, as presented in eqn. (5.3) is plotted here for the three gate biases simulated in fig. 5.2. Also, the curve for V_{GS} = 7V is replotted with l'=0.125 μm obtained using the formula given in [5.19]. For other curves l'=0.18 μm obtained from the temperature profiles (after damage) of fig. 5.2.

above in place of l', i.e., using l'=0.125 μm in eqn. (5) instead of 0.18 μm used for other curves. This leads to a downward shift in the corresponding curve for V_{GS}=7V by 0.055 μm. Obviously, l' is very critical in determining the lifetime of the device via degradation length. In contrast, the effect of the constant $\phi_{it}/q\lambda$ is less critical. The very fast rise of R_D in early mode degradation (fig. 5.1) also correlates with the fast initial rise in x. Also, the

spread of the degradation length is independent of N_{it} if the latter remains constant along the length, as assumed here. This situation is likely to be responsible for the nearly equal slopes in the late mode degradation in our work, and in the work of the authors of [5.5].

In order to prove that the above phenomenological model for the growth of defects really leads to the two stage degradation discussed earlier in section 5.2 (see fig. 5.1) we simulate the defects growth phenomenon in our 2-D simulation framework. The results of these simulations are discussed in the next section.

5.6 Defects growth simulations

In these simulations we try to mimic the defects growth situation depicted in fig. 5.14. But, in this case, we start placing the defects from deeper inside the spacer region. In fact, the first simulations were done after placing the defects between 0.54 and 0.52 μm from the centre of the channel, i.e. over 200 Å starting from 0.54 μm. In the succeeding simulations another 200 Å was added to the defects length corresponding to the previous simulation, until the edge of the defects length reached 0.34 μm from the centre of the channel. Due to lack of proper oxide grids near the interface, and deep in the spacer region, we used, as defects, negative interfacial charge density of magnitude $2.5\text{x}10^{12}$ / cm^2 in stead of $-2.5\text{x}10^{18}$ /cm^3 spread over 100 Å of interfacial oxide, as used in the previous simulations. This is to ensure the same magnitude of flux density due to defects. After each incremental defects length, we monitored the simulated linear drain current V_{DS}=0.05 V, and the simulated saturation current with V_{DS}=5 V.

From the linear drain currents, we first extracted the threshold voltage shifts (ΔV_T's) with respect to that of the virgin device. Threshold voltages extracted from the simulated linear currents correspond to a fixed drain current of 1 μA. The ΔV_T's are plotted against the distance of the defects edge from the channel centre in fig. 5.17 below.

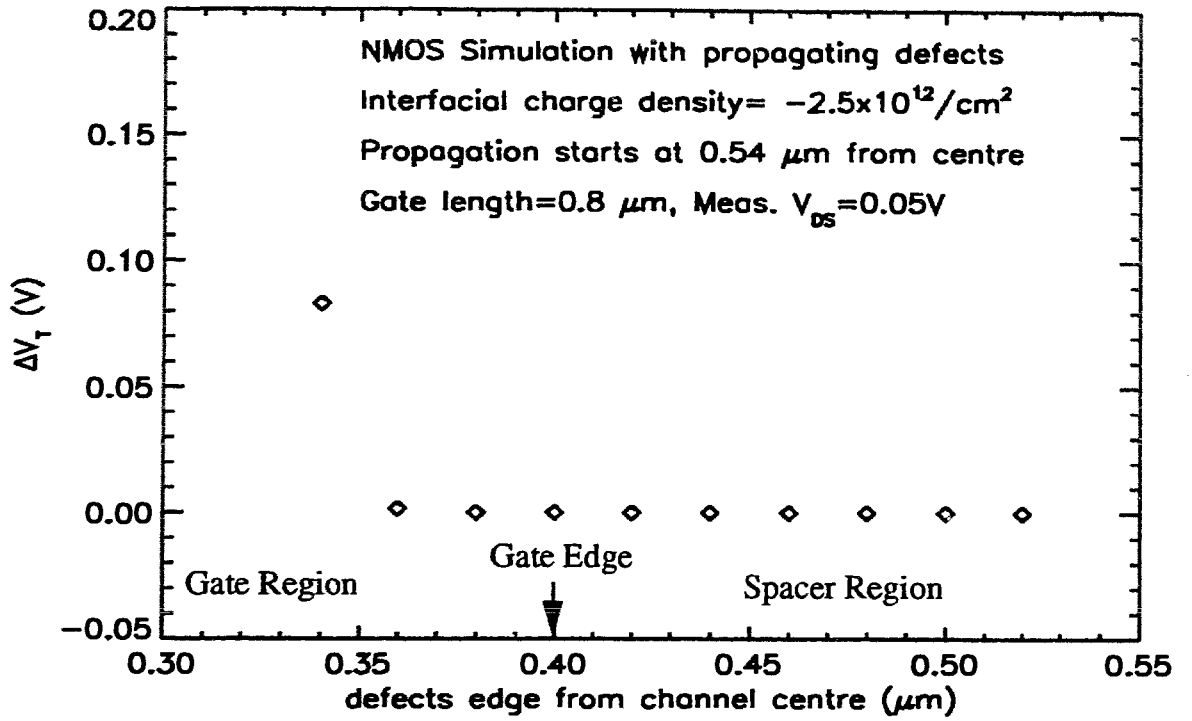

Fig. 5.17. ΔV_T versus defects progression from under the spacer region towards the centre of the channel.

Expectedly, the threshold voltages do not shift much until defects move well under the gate region. On the other hand, the degradation of linear g_m's extracted from the degrading linear currents with defects progression shows a distinctly different behavior when plotted in fig. 5.18 below. In this case, we find that the effect of defects to be negligible (less than 0.1% of $\Delta g_m/g_m$) when the defects lie deep inside the spacer region. In this region, where the doping concentration of the LDD is high, the rate of degradation of g_m's is linear. But, later, as the doping concentration starts falling, closer to the gate edge region, the rate of degradation gets progressively steeper as the defects move inwards.

Thus we obtain, $\Delta g_m/g_m$ vs. x from fig. 5.18 as a result of simulation. We had already modelled in the last section x vs. t for several V_{GS}'s with V_{DS}=7.5 V corresponding to our floating gate experiment discussed in chapter 5. Combining $\Delta g_m/g_m$ vs. x and x vs. t as

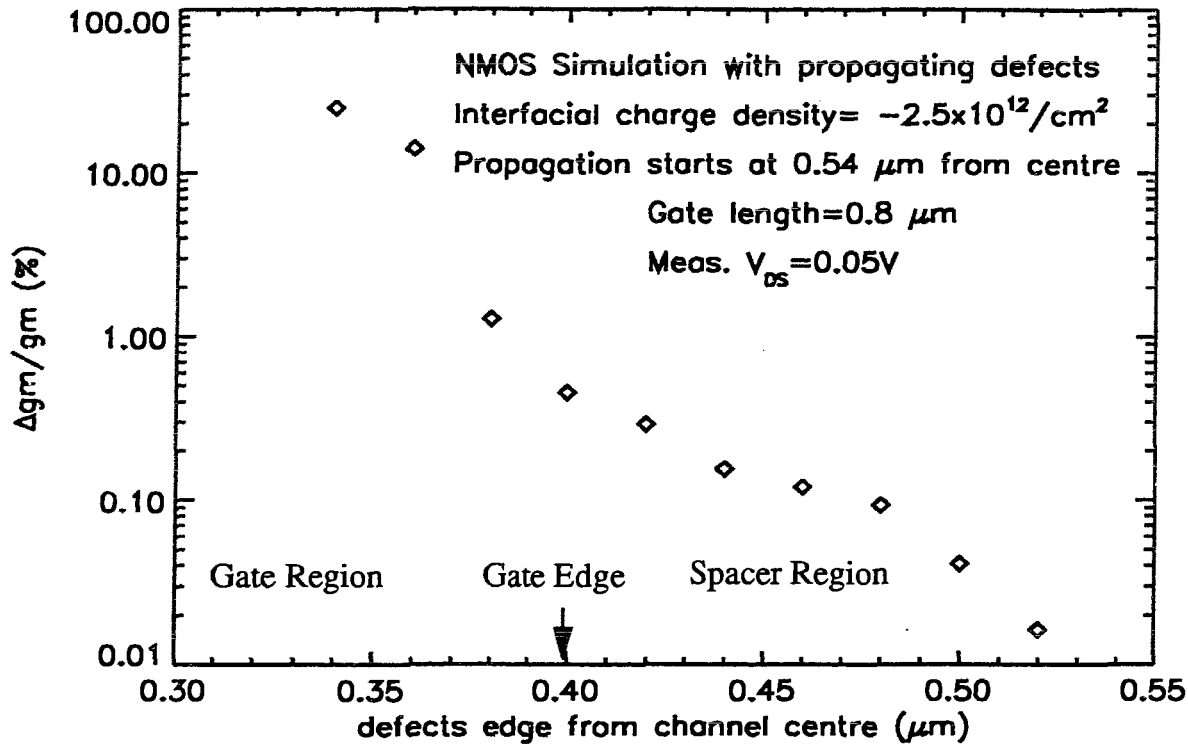

Fig. 5.18. $\Delta g_m/g_m$ versus defects progression from under the spacer region towards the centre of the channel.

obtained above we expect to obtain $\Delta g_m/g_m$ vs. t, that should show the two stage nature of the degradation as depicted in fig. 4.1 of chapter 4. In order to demonstrate this effect, we choose the case with V_{DS}=7.5 V and V_{GS}=5 V. We assume that the defects start progressing from 0.43 μm from centre of the channel, i.e. about 100 Å deeper than the defects edge of 0.42 μm found for the case with the early mode defects earlier (0.42 μm to 0.38 μm). Since we are dealing with a different device here, the choice of this starting point for defects progression is arbitrary. The main purpose here is to demonstrate the two stage nature of the degradation through linear interpolation between $\Delta g_m/g_m$ vs. x and x vs. t data. The result is shown in fig. 5.19.

The two-stage nature of the degradation in linear g_m's is quite apparent. In fact the slope n = 0.22 of the late mode degradation matches quite closely with our experimentally

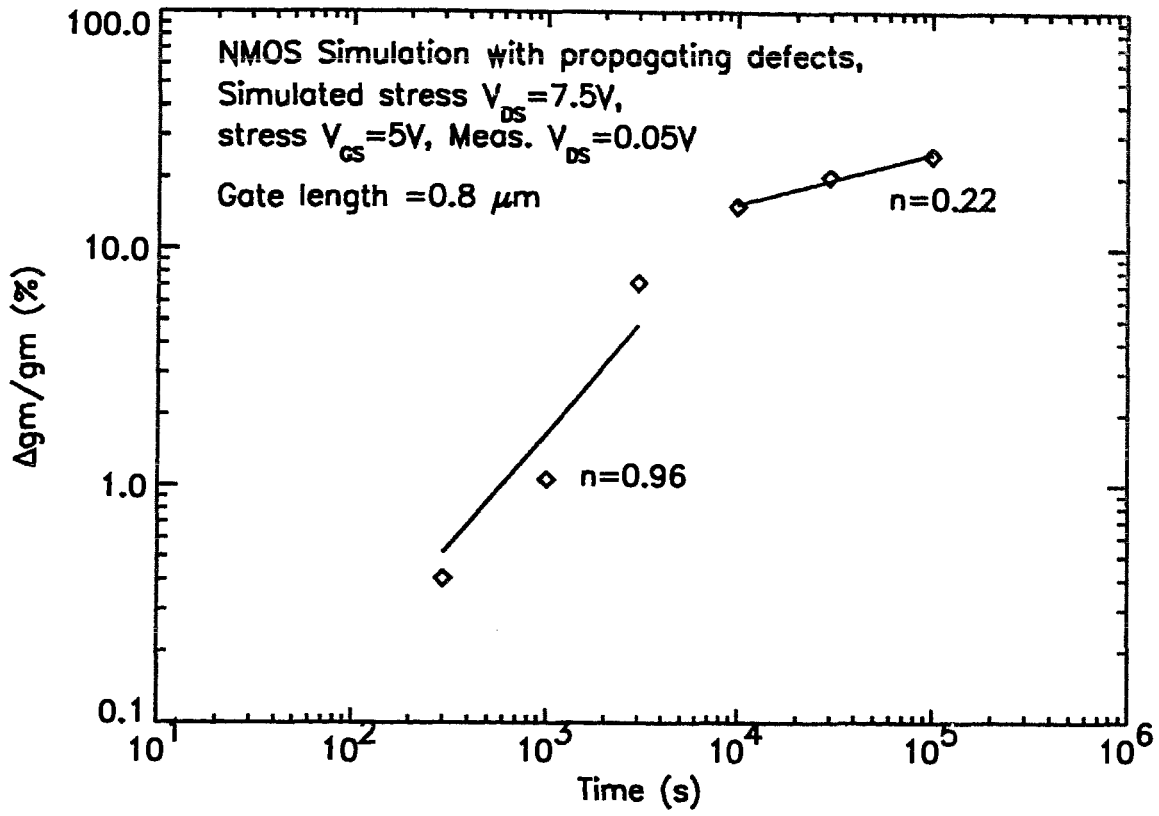

Fig. 5.19. $\Delta g_m/g_m$ versus time under defects progression from under the spacer region towards the centre of the channel.

observed values of 0.24-0.26 (see fig. 4.1 of chapter 4) as well as the value reported by the authors of [5.5]. However, the early-mode slope is steeper than our experimental values. This could be due to a lower defect density actually present in the devices characterized experimentally in fig. 4.1 of chapter 4. However, the result depicted in fig. 5.19 serves to demonstrate the validity of our model for defects propagation under hot carrier degradation. To further illustrate the effect of defects migration, we plot in fig. 5.20 the normalized linear current decrease, $\Delta I_{DS}/I_{DS}$ against measurement gate bias V_{GS} for various positions of the progressing defects edge. Striking similarity between these curves of fig. 5.19 and those of fig. 5.7 as well as those shown in the work [5.5] (see fig. 5 of [5.5]) gives strong basis for the defects migration scheme proposed by us. The behavior of $\Delta I_{DS}/I_{DS}$ against measurement gate bias V_{GS} can be explained by considering that

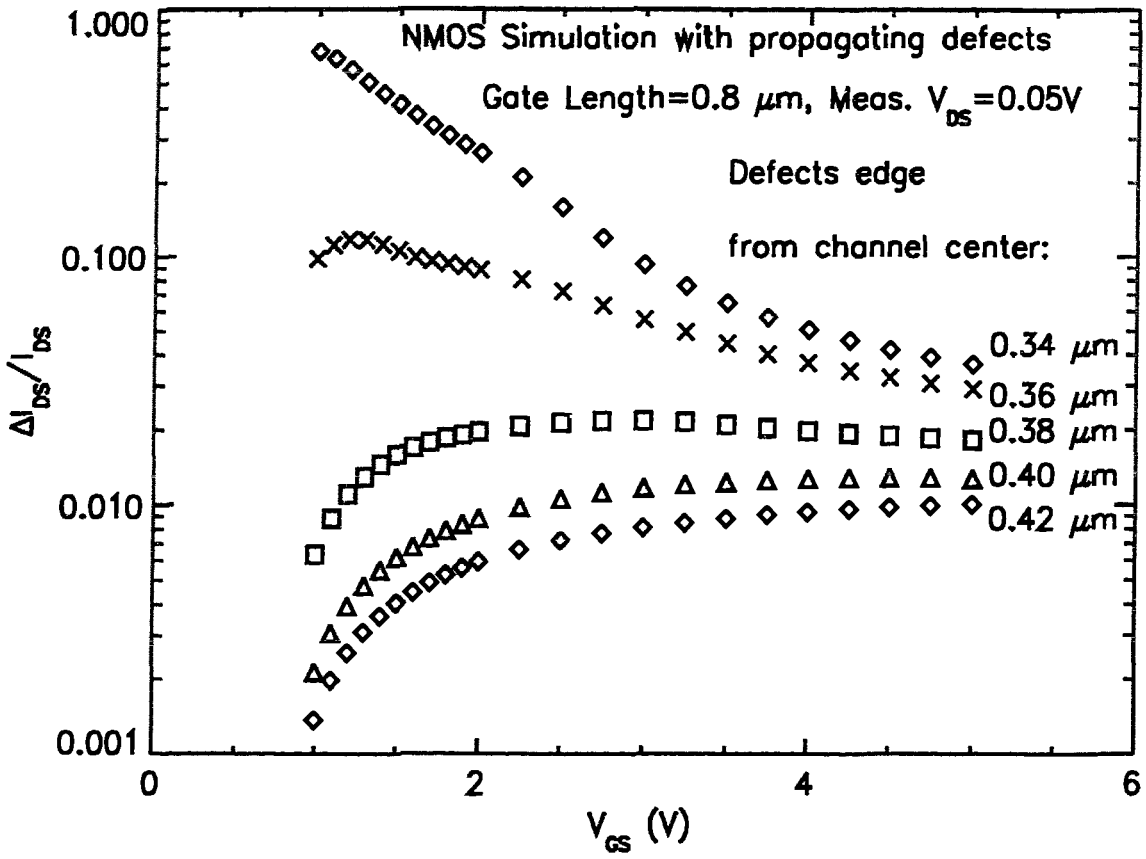

Fig. 5.20. Linear $\Delta I_{DS}/I_{DS}$ versus defects progression from under the spacer region towards the centre of the channel.

there are three parameters shifting during the course of hot-carrier degradation. These are drain series resistance R_D, effective carrier mobility μ, and the threshold voltage V_T. While, in the initial stages of degradation, μ and R_D are likely to change, V_T changes only in the late mode of the degradation. The amount of change in each of these parameters will depend on where under the spacer region, the degradation starts, stressing biases under static or dynamic situations, and the defect density produced during the degradation process. However, from a practical point of view we need to extract these parameter shifts under hot-carrier degradation from measurements on a degraded transistor. This will enable us perform circuit simulations with a "degraded" set of parameters. In the next chapter we will therefore discuss a simple method that we have developed to extract ΔR_D, $\Delta\mu$, ΔV_T from measurements of a degraded transistor.

5.7 Conclusion

In this chapter, we have reported the results of our investigations on the propagation of the damage region in hot carrier degradation. We have shown how the correlation between increasing drain parasitic resistance and increasing barrier height to electron injection leads to a simulation framework involving negatively charged oxide traps in the gate-edge/spacer oxide region. Other measurements and corresponding simulation help us locate and quantify the defects in this region which is otherwise inaccessible to existing experimental techniques. Our results indicate that the defects are roughly of the magnitude of 2.5×10^{12} negative charges per cm^2 spread over a length of 400 Å at the gate edge region, with 200 Å under the gate, and 200 Å in the spacer region. We also show that the defects attract the interfacial lateral electron temperature peaks outwards and increase their magnitude. Simulations indicate that the profile of defects, first produced in the spacer region proceed inwards with time. In the late mode degradation, they occupy the gate oxide region under the gate and above the LDD. The reason for substrate current reduction in the early mode and substrate current increase in the late mode is also explained with the help of simulation. It is seen that the substrate current reduction in the early mode is largely due to the efficiency of the early mode defects in pushing the surface electron currents to regions of lower electron temperatures occurring due to curved current paths. Finally, we derive an analytical model for the growth of the degraded region with stress time, based on our simulation results. The main implication of the model is that the saturation of hot-carrier degradation in LDD NMOSFETs is due to the saturation of the growth of the degradation length with stress time. We demonstrate the validity of this model through defects growth simulations that help us establish the two stage nature of the degradation process for LDD NMOSFETs. We believe that this phenomenological model for defects growth will be useful in better device design, and location of defects in the sub-spacer region.

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Chapter 6

Extraction of degradation parameters, $\Delta\mu$, ΔV_T, and ΔR_D from a degraded NMOS transistor

6.1 Introduction

In the last chapter, we have noted that the long term degradation effect in a hot-carrier degraded NMOSFET is characterized by a migration of defects from the sub-spacer region to the sub-gate region. Also, that the degradation is accompanied by shifts in three main device parameters, namely, mobility μ, threshold voltage V_T, and drain parasitic resistance R_D. It will therefore be very useful to have a direct and simple method to extract the shifts in these parameters that take place in the course of a long term degradation experiment. This will enable us to upgrade the model parameters for circuit simulation of degraded devices with greater ease and confidence. Some authors have considered the shift in either μ only [6.1], R_D only [6.2], or all model parameters [6.3]. However, we will show that consideration of $\Delta\mu$, ΔV_T, and ΔR_D is appropriate and predicts the measurements well. There has been little effort to date to directly extract these shifts from a single degraded transistor. Recently, the authors of [6.4] have extracted $\Delta\mu$ and ΔR_D from a degraded MOSFET. They did not consider ΔV_T at all in a self-consistent manner. Also, their method requires another MOSFET of different gate length, but same gate width for the extraction process. We have developed a technique that extracts these parameters without the assistance of any other device, and directly from the voltage shift data for reverse mode saturation current measurements as shown in fig. 5.9 of chapter 5. Using these extracted values of $\Delta\mu$, ΔV_T, and ΔR_D, we will then upgrade the SPICE level 3 [6.5] [6.6] parameters extracted for virgin NMOSFET devices using AURORA [6.7] program for each stage of degradation, and match the measured degraded characteristics

with the modelled characteristics. Two further show the accuracy of the extracted $\Delta\mu$, ΔV_T, and ΔR_D, we will extract these parameters from the linear currents, as well. However, this extraction is not a direct extraction, and will use the level 3 SPICE parameters extracted earlier. The purpose of this latter extraction is to show the accuracy of our direct extraction method from saturation currents mentioned earlier.

6.2 Device, stressing, and parameter extractor details

Devices used in this chapter were the same symmetrical LDD NMOSFETs reported in fig. 5.9 of chapter 5. They all have a drawn gate width of 5 μm, and gate length of 0.8 μm. Their processing details were discussed in section 4.2 of chapter 4.

These devices were hot carrier stressed at maximum substrate current situation with V_{DS}=6V. Various currents (saturation, linear, etc.) were monitored at 100s, 300s, 1000s, 3000s, 10000s, 30000s, 100000s of stress. For example, the $\Delta g_m/g_m$ vs. stress time was plotted in fig. 4.1 of chapter 4, and voltage shifts ΔV_{GS} versus reverse and forward saturation drain currents at various stress times were shown in figs. 5.9 and 5.10 respectively, and linear $\Delta I_{DS}/I_{DS}$ versus measurement V_{GS} was shown in fig. 5.8 of chapter 5.

The SPICE level 3 parameters were extracted with AURORA program which was used to control measurements on transistors of various geometries fabricated with the same process. We then set an optimization routine that enables AURORA to extract the parameters. The measuring instrument controlled by AURORA from a SPARC station was a HP4145 Semiconductor Parameter Analyzer. The direct and indirect extraction of $\Delta\mu$, ΔV_T, and ΔR_D from reverse saturation and forward linear currents respectively were accomplished with routines written by us in a PV-WAVE environment on the SPARC station.

6.3 Method of extraction from saturation currents

We start with the first order equation for saturation currents measured in the reverse mode, $I_{DS,sat,reverse}$. It is given by,

$$I_{DS,\,sat,\,reverse} = \mu C_{ox}\frac{W}{2L'}(V_{GS} - I_{DS,\,sat,\,reverse}\cdot R_D - V_T)^2. \qquad (6.1)$$

In the above equation, we have mobility μ, oxide capacitance per unit area C_{ox}, device gate width W, effective channel length L', drain parasitic resistance R_D, applied gate bias V_{GS}, and threshold voltage V_T. By taking the square root of both sides and transposing, we obtain

$$V_{GS} = I_{DS,\,sat,\,reverse}\cdot R_D + \frac{(\sqrt{I_{DS,\,sat,\,reverse}})}{\sqrt{\mu C_{ox}\frac{W}{2L'}}} + V_T. \qquad (6.2)$$

Therefore, at a constant $I_{DS,sat,reverse}$, any small variation ΔV_{GS} as a result of ΔR_D, $\Delta\mu$, and ΔV_T, and can be given by,

$$\Delta V_{GS} = \frac{\partial V_{GS}}{\partial R_D}\cdot\Delta R_D + \frac{\partial V_{GS}}{\partial \mu}\cdot\Delta\mu + \frac{\partial V_{GS}}{\partial V_T}\cdot\Delta V_T. \qquad (6.3)$$

If we take the derivatives in (6.3), and consider the magnitude of mobility reduction as $\Delta\mu$, we obtain

$$\Delta V_{GS} = \Delta R_D\cdot I_{DS,\,sat,\,reverse} + \frac{\Delta\mu\cdot\sqrt{I_{DS,\,sat,\,reverse}}}{\sqrt{\mu^3 C_{ox}\frac{2W}{L'}}} + \Delta V_T. \qquad (6.4)$$

or,

$$\Delta V_{GS} = \Delta R_D\cdot I_{DS,\,sat,\,reverse} + \frac{\Delta\mu}{\mu}\cdot\frac{1}{\sqrt{2K}}\sqrt{I_{DS,\,sat,\,reverse}} + \Delta V_T. \qquad (6.5)$$

where K is given by,

$$K = \mu C_{ox} \frac{W}{L}. \tag{6.6}$$

The above equation (6.5) represents a second order polynomial expression in $\sqrt{I_{DS,\,sat,\,reverse}}$. Hence, if we replot the ΔV_{GS}'s of fig. 5.9 of chapter 5 versus the $\sqrt{I_{DS,\,sat,\,reverse}}$ values at various stress times, and fit the data with second order polynomials, we should get good fit as shown in fig. 6.1 below. The coefficients of the polynomials a0, a1, and a2 for a curve corresponding to a particular stress time should be given by

$$\begin{aligned} a0 &= \Delta V_T \\ a1 &= \frac{\Delta\mu}{\mu} \cdot \frac{1}{\sqrt{2K}} \\ a2 &= \Delta R_D. \end{aligned} \tag{6.7}$$

While ΔV_T and ΔR_D can be directly obtained from a0 and a2 respectively, the value of $\Delta\mu/\mu$ requires the knowledge of K.

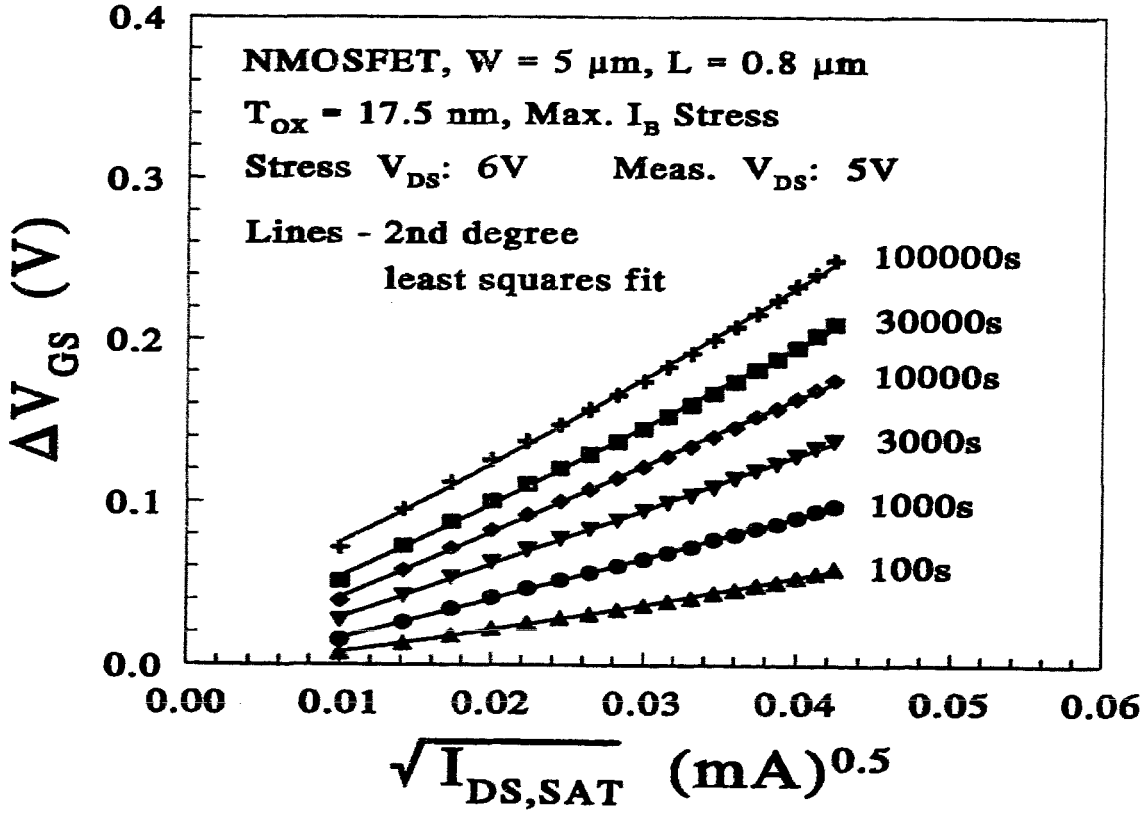

Fig. 6.1. ΔV_{GS} versus $\sqrt{I_{DS,\,sat,\,reverse}}$ at various stress times.

We will show later that we can get very good estimate of $1/K$ from the linear I_{DS} vs. V_{GS} characteristic of the virgin device, by simply plotting V_{DS}/I_{DS} versus $1/(V_{GS}-V_T)$ and taking the slope of the corresponding straight line as $1/K$. Once we obtain $1/K$ we can easily calculate $\Delta\mu/\mu$ from a1 given in eqn. (6.7) above. Assuming a value of 535 cm^2/V-s for μ, as obtained from SPICE level 3 model parameter extraction (discussed later) we can plot $\Delta\mu$ versus stress time as shown in fig. 6.2 below.

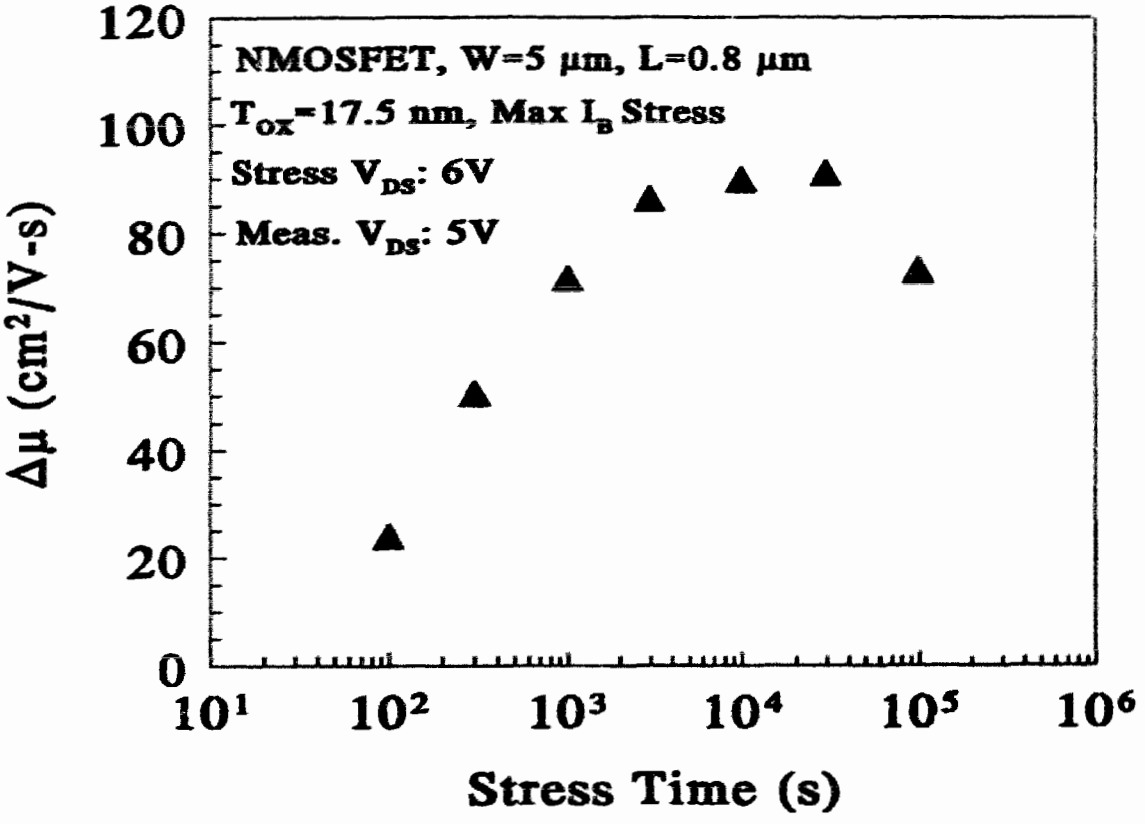

Fig. 6.2. Mobility reduction versus stress time obtained from the curves of fig. 6.1.

The saturation of mobility reduction at higher stress times, and a steep increase in the reduction at lower stress times are the major features in fig. 6.2. The mobility increase at 10^5s of stress is another interesting feature here. As seen here, we are able to quantify the amount of mobility reduction at each stress time quite easily with our method. While we have assumed a value of mobility for the virgin device obtained from another source, our method gives $\Delta\mu/\mu$ directly, without the requirement of any other extraction.

The corresponding shifts ΔV_T and ΔR_D versus stress time are depicted in fig. 6.3 and fig. 6.4 respectively.

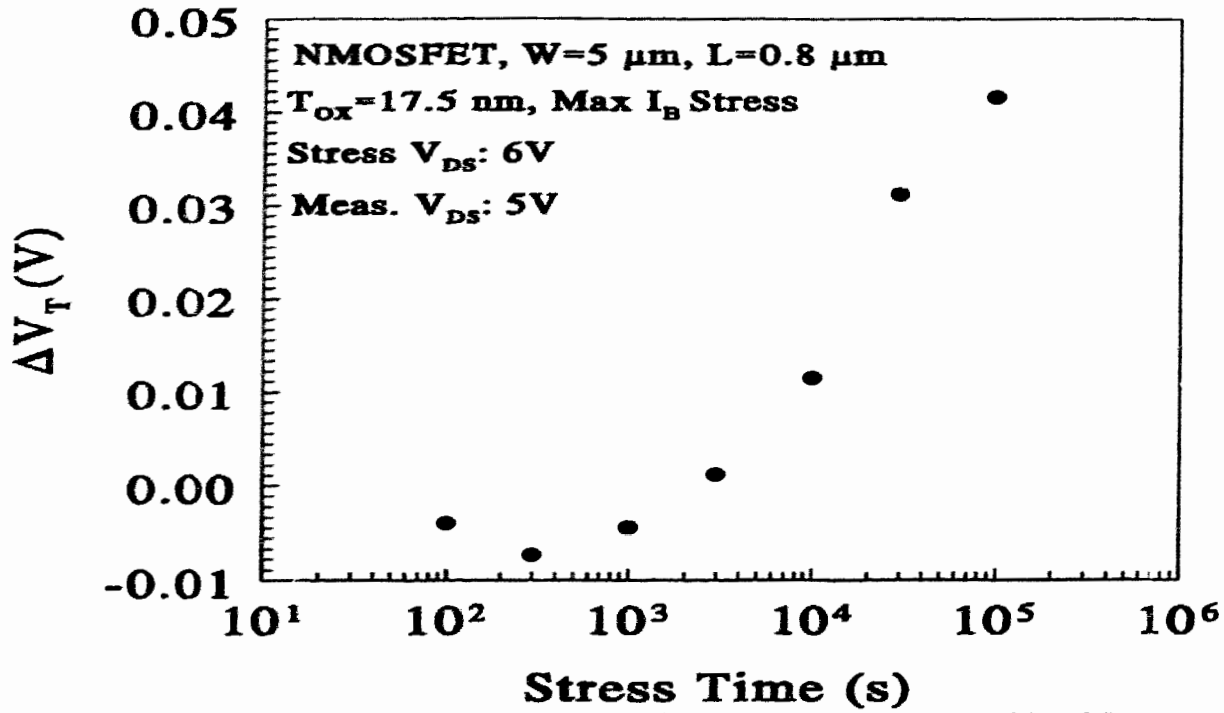

Fig. 6.3. Threshold increase versus stress time obtained from the curves of fig. 6.1.

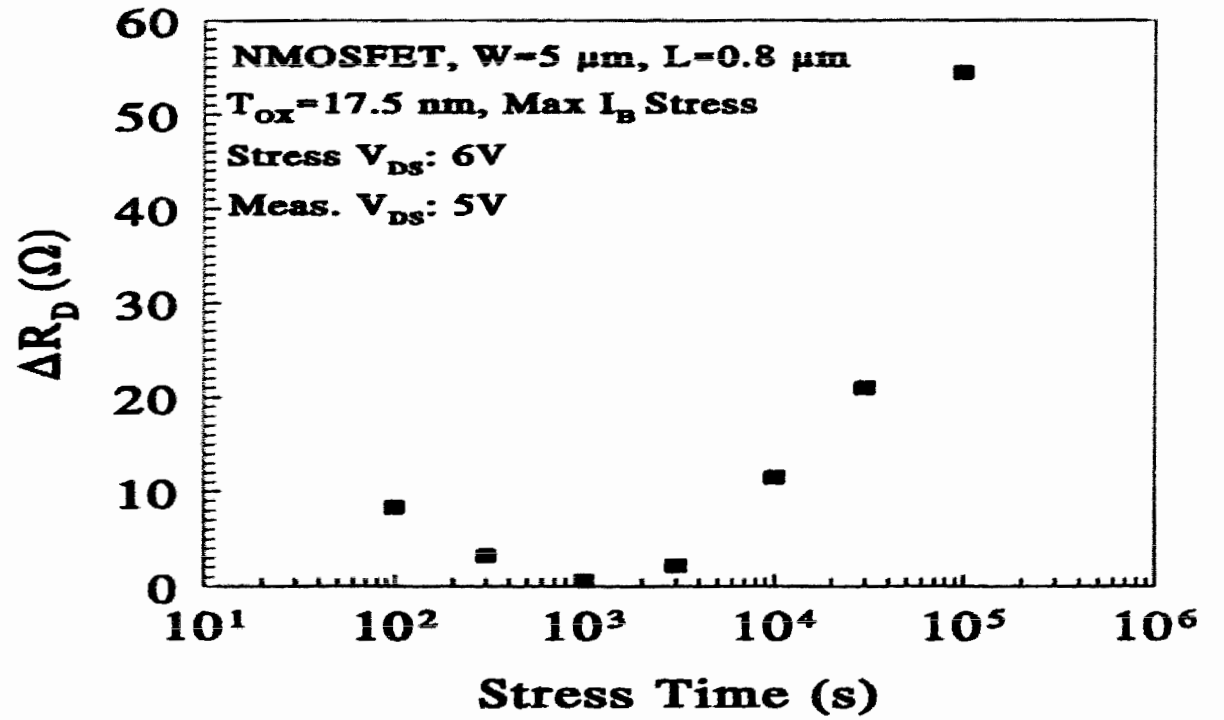

Fig. 6.4. R_D increase versus stress time obtained from the curves of fig. 6.1.

Nearly negligible threshold shifts in the initial stress times match well (qualitatively) with the V_T-shift results of defects growth simulations presented in fig. 5.17 of chapter 5. That is, the threshold voltages start shifting only when the defects progress enough into the sub-gate LDD region. However, the V_T-shift magnitude for the deeper defects was higher than that extracted here for long stress times. It could be due to lower number of defects actually created than $2.5x10^{12}/cm^2$ assumed for simulations.

The most interesting evolution is observed in the case of extracted values of ΔR_D here. While there is an increase of about 10 Ω at the initial stress point (100s), subsequently, a decrease is noted here till about 1000s. Afterwards, R_D increases again by about 55 Ω towards the longer stress times. This behavior of R_D, particularly, the decrease after the initial increase, is not expected by our model of defects growth discussed in chapter 5. Because, we expected a saturation of the increase in R_D, rather than decrease, during the early mode of degradation. However, the extracted behavior may be possible due to a complex change in the current flow lines near the edge of the gate. The evidence of late mode increase of R_D concurrent with the decrease of μ has already been reported in [6.4].

In the simple method discussed above, we have assumed that μ and L' are independent of $I_{DS,sat,reverse}$ for the purpose of curve-fitting with a second order polynomial involving a0, a1, and a2 given by eqn. (6.7). However, in reality, that is not true. Because, both μ and L' are somewhat dependent on applied V_{GS} for a particular applied V_{DS} in saturation. This must give rise to some error in our extraction. But, how severe is the error? To answer this question, we first check the match of the experimental saturated and linear I-V characteristics taken at various stress times with the ones modelled with the SPICE level 3 model parameters incremented by our extracted values of $\Delta\mu$, ΔV_T, and ΔR_D at the corresponding stress times. We will then extract the $\Delta\mu$, ΔV_T,

and ΔR_D values from the stressed linear currents using an indirect method, and match them with the values obtained here. We will see that the error is not severe.

6.4 Match with experimental curves

In order to match the stressed saturation and linear currents with the modelled currents, we first extract the SPICE level 3 model parameters given below in Table 6.1.

Table 6.1. SPICE level 3 parameters for virgin device.

Name	Value	Description
type	1.0	1 for n-channel, -1 for p
level	3	model level (1,2, or 3)
vto	0.804 V	zero-bias threshold voltage
tox	1.7e-8 m	gate oxide thickness
nsub	2.12e16 /cm^3	substrate doping
xj	1.41e-7 m	short-channel effect on V_T
ld	7.52e-8 m	Leff = Lmask - 2*ld
uo	5.35e2 cm^2/V-s	low-field mobility
vmax	1.4e5 m/s	velocity saturation
delta	2.00	narow-channel effect on V_T
theta	7.3e-2 /V	mobility reduction
eta	6.8e-2	DIBL output conductance
kappa	0.00	output conductance factor
dw	2.23e-7 m	Weff=Wmask-dw
rs	125.0 Ω	drain resistance
rd	125.0 Ω	source resistance

The above parameters were extracted using the AURORA program [6.7] and I-V data of 3 transistors of different geometries, namely, long & wide, short & wide, and short & narrow. Sets of model parameters were optimized using different portions of the I-V data

set, while other parameters were kept constant. Finally, the whole extraction procedure was repeated until there was negligible variation between parameters extracted from succeeding extractions. Fig. 6.4 shows an example of the fit between the modelled curves and the experimental ones for the short & wide transistor. The fit appears to be quite good.

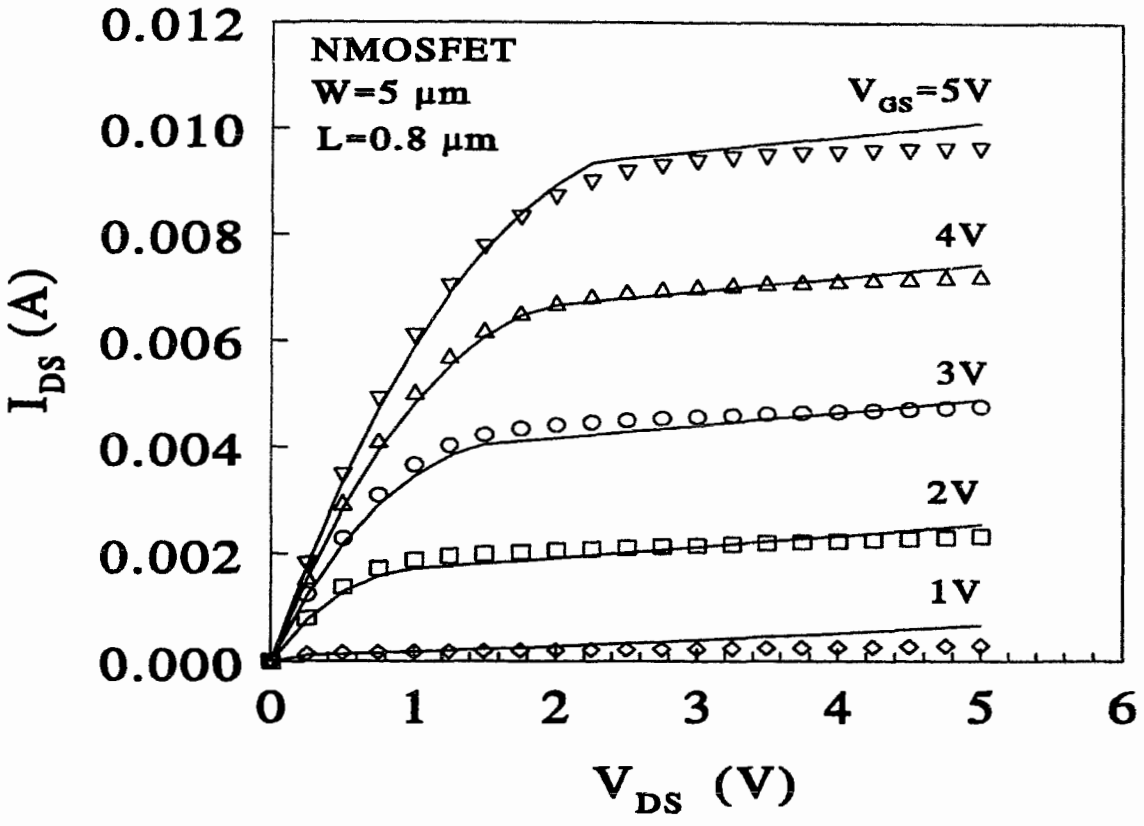

Fig. 6.5. Fit between modelled (SPICE level 3) curves with the parameters of Table 6.1 and measure data (symbols) for the short & wide transistor.

We then updated the model parameters of Table 6.1 with the extracted values of $\Delta\mu$, ΔV_T, and ΔR_D and generated model parameter sets for each stress time. We actually changed the three parameters uo, vto, and rd among the list of parameters given in Table 6.1. Each of these "stressed" parameter sets was then used to model the I_{DS} vs. V_{GS} curves monitored after various stress times from the same device as was used for the extraction of $\Delta\mu$, ΔV_T, and ΔR_D. We did this for both saturated I_{DS} vs. V_{GS} curves with V_{DS}=5 V (see fig. 6.6), and linear I_{DS} vs. V_{GS} curves with V_{DS}=0.05 V (see fig. 6.7). We chose the curves for the virgin device and the device after 1000s and 100000s of stress to show the

two cases of early mode and late mode stress, and to avoid clutter. The fit appears to be

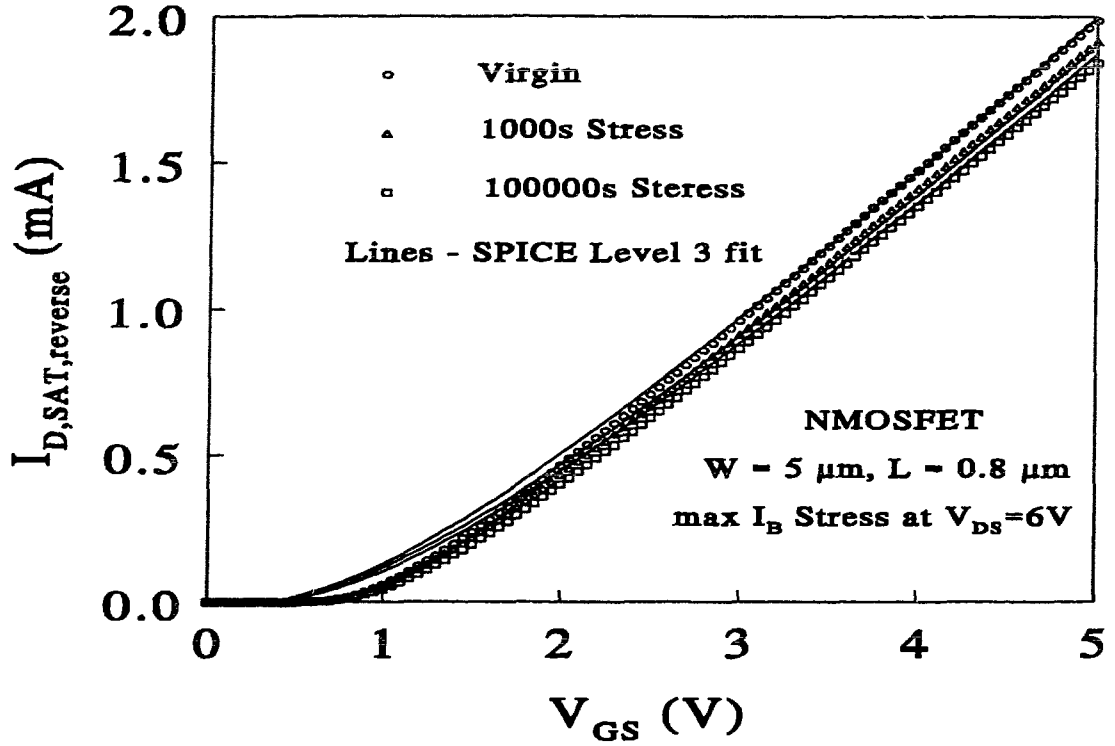

Fig. 6.6. Fit between experimental "stressed" curves and the ones modelled with updated SPICE level 3 parameters. Measurement V_{DS} was 5V.

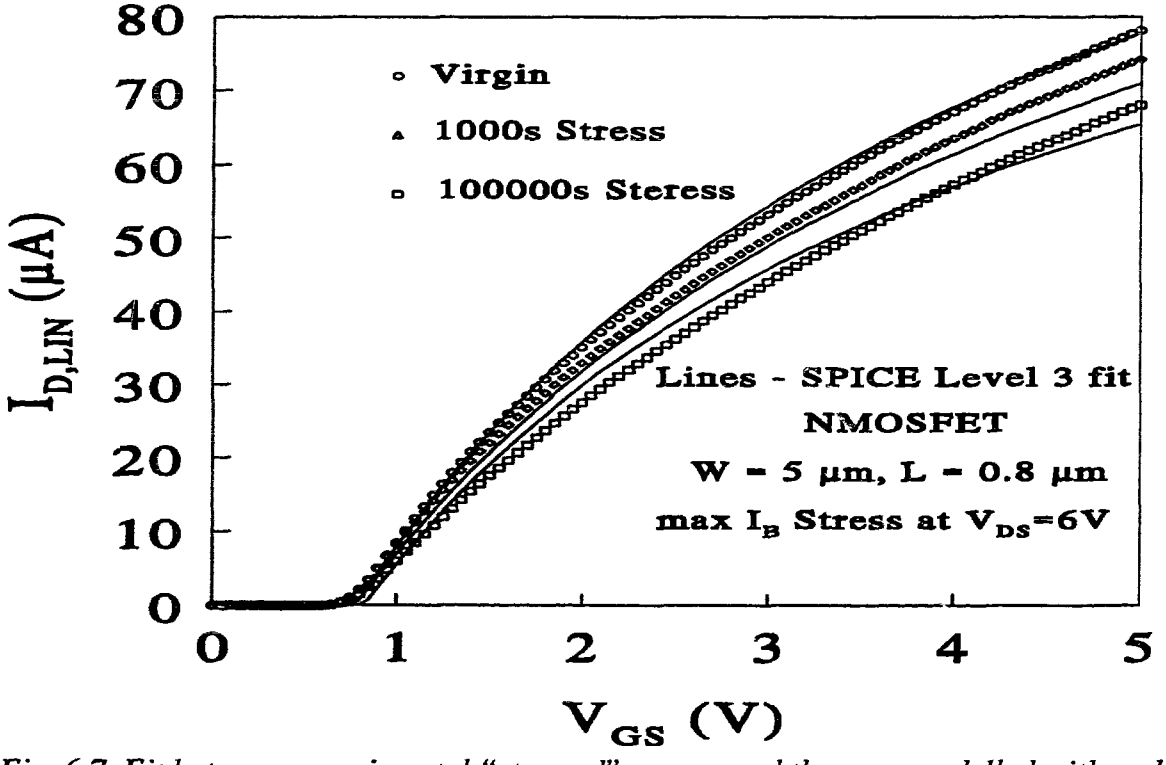

Fig. 6.7. Fit between experimental "stressed" curves and the ones modelled with updated SPICE level 3 parameters. Measurement V_{DS} was 0.05V.

quite good, particularly for the saturated curves. This shows accuracy of our method.

6.5 Match with extraction from linear region

In this case we would like to obtain the values of $\Delta\mu$, ΔV_T, and ΔR_D from the virgin and stressed linear I-V curves of the MOSFET. The purpose is only to check the accuracy of the extracted parameters as obtained from the saturated curves. In the case of the linear currents, it can be shown that the d.c. resistance R ($=V_{DS}/I_{DS}$) of the MOSFET is given by,

$$R = \frac{1}{K'(V_{GS}-V_T)} + \left(\frac{\theta}{K'} + R_t\right). \tag{6.8}$$

In the above equation (6.8), K' is given by

$$K' = \mu_0 C_{ox} \frac{W}{L'}, \tag{6.9}$$

where, μ_0 is the low-field mobility. In this case, we are taking the mobility's degradation with gate bias into account in order to obtain accurate values of R_t, which is equal to R_S+R_D. The mobility μ is given by the SPICE level 3 model,

$$\mu = \frac{\mu_0}{1+\theta(V_{GS}-V_T)}. \tag{6.10}$$

In this extraction procedure, we first extract the V_T's from the linear I-V curves of the virgin device and the same device after various stress times. The V_T's correspond to a fixed linear current of 1μA. From these V_T's we easily compute the ΔV_T's versus stress time as shown in fig. 6.8 below. We then obtain the K' values by plotting R vs. $1/(V_{GS}-V_T)$, and monitoring the slopes ($1/K'$) of the straight lines thereby obtained for the virgin device as well as the stressed device after each stress time. From these values of K', we obtain μ_0's using eqn. (6.10). We use W=5 μm, and values of C_{ox} and L' were calculated from the SPICE parameters of Table 6.1. These μ_0's were used to compute the $\Delta\mu$ versus stress time curves of fig. 6.9 below. Also, from the intercepts of the R vs. $1/(V_{GS}-V_T)$ straight

lines (see eqn. (6.8)), we obtained R_t's using θ (theta) value from Table 6.1. These R_t's are used to plot ΔR_t vs. stress time in fig. 6.10 below.

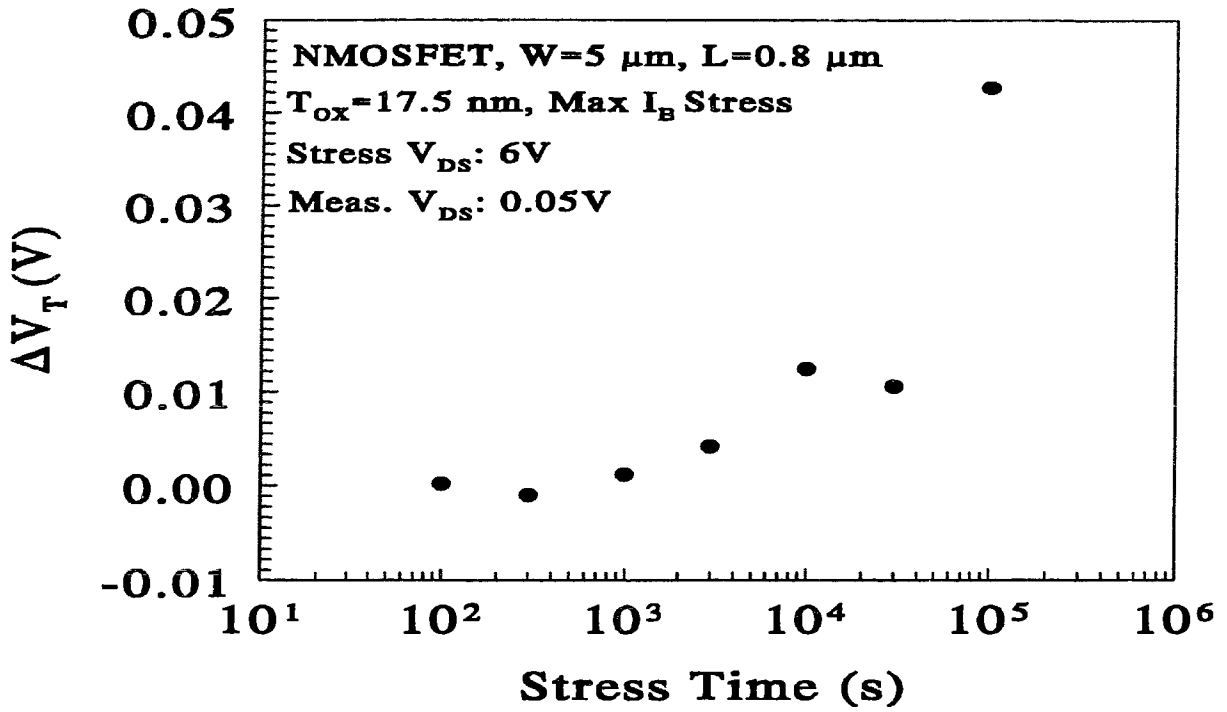

Fig. 6.8. ΔV_T versus stress time extracted from the linear currents.

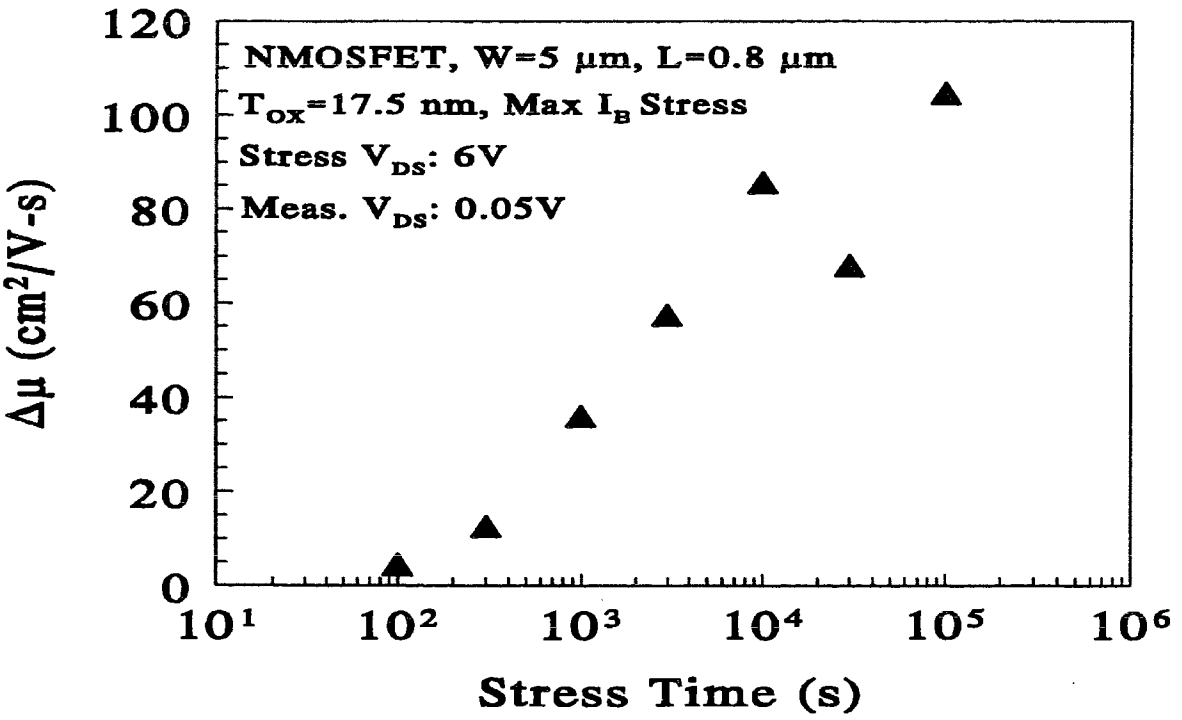

Fig. 6.9. Δμ versus stress time extracted from the linear currents.

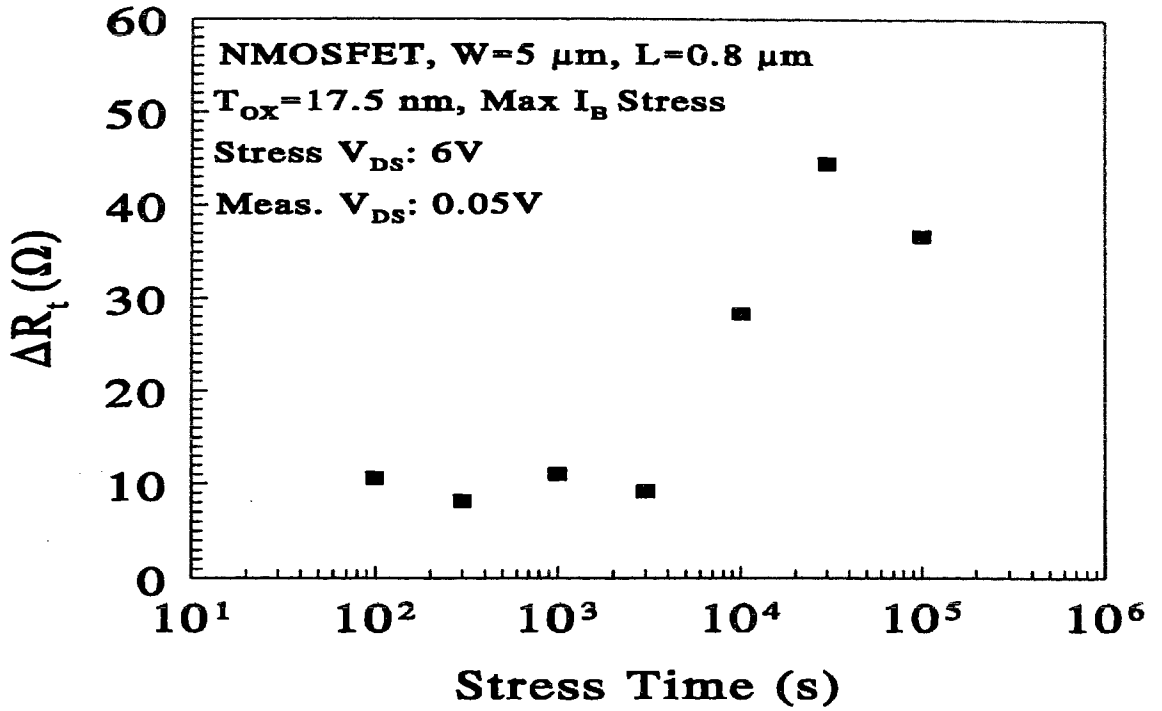

Fig. 6.10. ΔR_t versus stress time extracted from the linear currents.

If we compare fig. 6.10 with fig. 6.3, we see that the ΔV_T's extracted from the linear currents match quite well with those from the direct method using saturation currents. ΔV_T is negligible at first, and then rises pretty rapidly. Comparing fig. 6.9 with fig. 6.2, we find the same qualitative trend of the saturation of $\Delta\mu$ at higher stress times. Also, the saturated values match roughly (~100 cm^2/V-s). However, at lower stress times, the $\Delta\mu$ values obtained from the linear method are lower than those extracted from the saturation currents. Again, ΔR_t versus stress time curve of fig. 6.10 matches quite well with the ΔR_D versus stress time curve of fig. 6.4. Only difference is that we do not notice the fall in ΔR_t during the initial phase of the degradation. This is expected due to the saturation of ΔR_D in the early phase of the degradation. Hence, we observe that our simple method for the extraction of $\Delta\mu$, ΔV_T, and ΔR_D from the saturation currents does yield reasonably accurate values of these parameters without the aid of any other transistor or extractions. These extracted values can then be used to update SPICE parameters for simulations.

6.6 Conclusion

In any hot-carrier degradation situation, three main parameters, namely mobility, drain series resistance, and threshold voltage of an NMOSFET shift with stress. In order to successfully carry out simulations, one needs to update the SPICE parameters with the values of these shifting parameters. Therefore, one needs a simple technique to extract these three quantities from the measured I-V characteristics of a single NMOS transistor undergoing progressive stress. In this chapter, we have demonstrated a simple method to extract the values of $\Delta\mu$, ΔV_T, and ΔR_D from the saturated I_{DS}-V_{GS} data measured reversely on a single NMOS transistor going from virgin state to the stressed states following various intervals of d.c. stress at maximum substrate current. We have then updated the SPICE level 3 parameters of the virgin device and shown that the experimental "stressed" I_{DS}-V_{GS} curves, both in linear region and saturation region, are well predicted by the "stressed" model parameters. We have also extracted $\Delta\mu$, ΔV_T, and ΔR_D from the linear drain currents of the MOSFET at various points of stress with an indirect method that uses some of the extracted SPICE parameters. It is seen that $\Delta\mu$, ΔV_T, and ΔR_D versus stress time as extracted from the linear currents match reasonably well with those extracted from the saturation currents. We thus conclude that the error in our direct technique in neglecting the dependence of mobility and effective channel length on saturated drain current is not severe, and that this technique will be useful in studying the effect of hot-carrier degradation on the three major parameters of the MOSFET.

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Chapter 7

Conclusions and recommendations

In this thesis we have, for the first time, established a firm concept [1.10] [1.16] of defects migration under hot-electron degradation of LDD NMOSFET devices. We performed appropriate measurements and corresponding 2-D numerical device simulations to investigate this effect that gives rise to a saturating degradation characteristic in these devices, as opposed to conventional highly doped source/drain transistors. Specifically, the following were established.

Extraction technique for R_S and R_D

A new and generalized technique [1.11] [1.12] [3.13] for the extraction of the parasitic source and drain resistances R_S and R_D of the MOSFET was established. The speciality of this technique as opposed to previous ones is two-fold.

(1) It requires a single MOS transistor to accomplish the extraction, while most previous techniques required more than one device of varying physical dimensions on the same wafer.

(2) It uses generalized expressions for device transconductance and drain conductance to accomplish the extraction. This was the first published technique of this nature.

As the channel length of the transistor is shrinking, the importance of the parasitic resistances is increasing. Hence, the demand for simple, yet reasonably accurate methods for their extraction. Also, due to hot-electron stress, processing effects, and layout situations, the transistor is liable to become asymmetric. In such situations it is necessary to extract these resistances separately, rather than getting just their sum as most existing

methods do. The new method addresses this issue adequately. We have also provided an error analysis for the method.

Characterization of the early mode of hot-electron degradation

We have characterized [1.13] [1.14] [1.15] the sharp early mode of hot electron degradation using a novel application of the floating gate technique, and the saturation transconductance technique developed in connection with the R_S and R_D extraction method mentioned above. We have also applied the spatial profiling charge pumping technique in this characterization. A remarkable evolution in the channel hot-electron gate currents was found to correlate with a corresponding evolution in the saturation transconductances in the early mode of the degradation. A carefully applied charge pumping method was used to eliminate the channel region from consideration for defects generation in the early phase of the degradation. We have not seen any previous reports that deal specifically with the sharp and important early mode of degradation seen in LDD NMOSFETs due to the spacer region. In this context, the simple, yet insightful techniques used in our characterization are extremely relevant. The experimental characterization directly helped us to develop a 2-D device simulation framework, involving trapped negative charges in the gate-edge region. The location and quantification of these defects were established through careful matching of electrical features of the degraded transistor with corresponding simulated features.

Defects migration model and validation

The detailed 2-D device simulation clearly suggested that the early mode defects are created in the gate-edge region - partly above the sub-spacer LDD region, and partly above the sub-gate LDD region. At the same time, the late mode defects are created above the sub-gate LDD region. This led us to a new defects migration model [1.16] [1.10] that spans the early and the late modes of the degradation. This model is simple and it suggests

a logarithmic dependence of the degradation length with hot-electron stress time in the initial phase of the degradation, while the degradation length saturates at long stress times. This model, in our view, is a significant development. This will not only help formulate new hot-electron lifetime expressions for the LDD NMOSFET device, it will also help design devices keeping the degradation length in mind. This model was validated using defects migration simulations and experimental long-term hot-electron degradation characteristics for the linear transconductance.

Extraction technique for $\Delta\mu$, ΔV_T, and ΔR_D

Circuit effects of hot-electron reliability are best analyzed through simulation of circuits using updated SPICE parameters. Three main parameters, namely, mobility μ, threshold voltage V_T, and drain parasitic resistance R_D are the ones most severely affected by hot-electron degradation. We have developed a new and simple method based on reverse saturation transconductances of the transistor to extract the progressive variations in these parameters over continued hot-electron stress. In spite of certain simplifying assumptions, this method is seen to yield reasonably accurate estimates of $\Delta\mu$, ΔV_T, and ΔR_D. The accuracy was checked out through corresponding extractions using linear drain currents. This method has been submitted for publication.

The "virtual factory" approach for simulations

A "virtual factory" approach [1.17] [1.18] for simulations was developed for efficient matrix process and device simulations. This approach is essential for proper optimization of performance and reliability characteristics of devices during CMOS/BiCMOS technology development phases. For this purpose, we have developed a software framework installed in our laboratory, as well as at an industrial establishment. This software framework enables a user to perform matrix simulations in a user-friendly manner.

In conclusion, we have attempted to combine substantial fundamental research work on hot-electron degradation of LDD NMOSFET devices with appropriate applied work aimed at better and more reliable device design for new sub-micron technologies.

Recommendations

The work reported in this thesis should lead to further investigation of the hot-electron defects migration in LDD devices. We believe, one of the most important future development would be to explore an appropriate direct experimental technique to study this defects migration process and compare the results with our model. Also, our model can be used to develop more accurate lifetime prediction formulas for LDD NMOSFETs. In terms of device design, our model should be used to set such important process parameters as spacer width, LDD doping, etc. Also, since this model predicts a saturation of the length of degradation, a mechanism to create defects artificially and deep under the spacer should be investigated.

One of the interesting feature of our work has been the frequent use of saturation current of the MOSFET in the study of hot-electron effect, as well as parameter extraction. This is in contrast with the standard practice of using linear currents. We believe, that our published work will lead other researchers in this area to use the saturation currents more frequently. We think that this is the natural current to use for many studies.

There is a large scope of development in the area of the "virtual factory" scheme. Augmentation to parameter extraction and circuit simulation should be the first step.

Appendix 1: The Virtual Factory Scheme

I. Introduction

In this appendix, we discuss the software framework that performs matrix process simulation on Canadian Microelectronics Corporation's (CMC) 0.8 μm BiCMOS process recipes using TSUPREM4 [A1.1], subsequent matrix device simulation using MEDICI [A1.2], and SPICE parameter modeling using AURORA [A1.3] in a user-friendly manner. In the course of development of a VLSI process technology, one needs to vary and adjust various geometrical and process parameters of the individual transistors in order to design the optimal device with appropriate performance and reliability characteristics. This is achieved through running the so called matrix process batches and subsequent device characterization steps. Before committing the wafers to these costly matrix experiments, it is necessary to go through a matrix simulation procedure to ascertain the minimal matrix batch size and its parameters. It is in this effort that our framework is intended to be helpful. The framework minimizes user intervention in the tedious and time-consuming steps of editing the recipe files, creating appropriate simulation input files, and organizing the simulation results in appropriate sub-directories.

While the software framework is in working condition for matrix process simulation and subsequent matrix device simulation, the parameter modeling part is yet to be integrated. Also, at this point, we have implemented NMOS and PMOS transistors for the simulations. Bipolar transistors are yet to be included. Apart from providing a general idea of the various components of the framework, this appendix is meant to be a guide to future developers or users of the technology CAD setup of our laboratory. The scheme of the entire framework is shown in fig. A1.1 below. Most of the post processing work was done using the PV-WAVE [A1.4] program, and some details about the PV-WAVE scripts and

Fig. A1.1. The virtual factory scheme.

their use are provided in a technical report [A1.5]. Also, the UNIX and C programs that control the matrix process simulations are listed in [A1.6].

II. The Principle of Matrix Process Simulation

The basic idea of virtual factory for matrix process simulation is to enable us simulate transistors with varying physical parameters such as channel length, oxide thickness, LDD doping level, spacer width, etc. with the minimal effort. The user simply specifies the physical parameters for each transistor (NMOS or PMOS) in a file (called **device_form**) and our software framework does the rest. The results (virtual devices) are stored in user-specified sub-directories, one unique sub-directory for every transistor. Thus the software framework working on the BiCMOS recipes act like a virtual factory. The function of the software framework is to intelligently modify the appropriate recipe files according to the user's specifications of device physical parameters, and then run TSUPREM4 on the set of modified and unmodified recipe files, and finally store the results in appropriate sub-directories. Although, at the present moment, we have treated only MOS transistors for four user specified parameters mentioned above and one open parameter for which the user must supply an appropriate script, the framework can be easily extended to more parameters and/or transistors.

In the following, some details of the software framework developed by us are given. We will also discuss some modifications that were necessary with the original recipe files to avoid a few problems we faced during our work.

III. The Software Framework

The software framework that controls the matrix process simulation with TSUPREM4, consists of two UNIX C-shell scripts, namely,

(i) *make_device**, and (ii) *matrix_suprem4**.

as well as a few executable utilities (source codes written in C), namely,

(i) *bsp**

(ii) *maskchg**

(iii) *defchg**

(iv) *goxchg**

(v) *swchg**

(vi) *lddchg**

(vii) *gdchg**

(viii) *mosS4chg**.

The latter utilities are called by the UNIX scripts to perform specific tasks. All of the above routines should be placed in one single sub-directory in the user's environment, with the path to that sub-directory being set in the user's .cshrc file. Also, the path to the recipes sub-directory in the user's environment must be specified in the line "set recipe_dir=....." of the C-shell script matrix_suprem4*. These steps must be completed before the user starts using the framework. The matrix simulation is performed by simply issuing the command "matrix_suprem4" after the user has specified the specs of the devices to be simulated in a file called **device_form** at her/his **~/suprem4/bicmos** level. Brief descriptions of the constituents of the software framework are given below.

The two UNIX script programs *make_device** and *matrix_suprem4** facilitate the user to specify (make up the **device_form** file) and simulate the devices respectively.

*make_device** asks the user for the number of devices to be simulated, and the type of device (NMOS or PMOS), the name of sub-directory of storage (DN), the channel length (CL), the gate oxide thickness (TO), the sidewall spacer width (SW), the LDD implant dose (LD), and the simulation grid density (GD) of each individual device. An extra user specified parameter (SP) is also available if the user provides the utilities to convert files associated with this parameter. The full path-name of the user-written script should be provided for SP. Then *make_device** stores the acquired information in a text file **device_form** in the user's **~/suprem4/bicmos** sub-directory. A typical **device_form** looks like the following:

```
2
NMOS
DN=NMOS_CL_0.7
CL=0.7
TO=175
SW=0.2
LD=2.0E13
GD=1.0
SP=
PMOS
DN=PMOS_SW_0.1
CL=0.8
TO=175
SW=0.1
LD=2.0E13
GD=1.0
SP=
```

Right now, *make_device** is a character-based program. A better user interface can be considered to make this utility easier to use.

*matrix_suprem4** is the main program for generating devices by TSUPREM4. It reads **device_form** to obtain the information of the transistors to be simulated. It creates the device sub- directories as specified by DN under user's **~/suprem4/bicmos** level, then it converts (if the physical parameters demand) appropriate definition files and process

files, taken from the recipes sub-directory and places them in the specific device sub-directories. The following are the parameters to be altered, the affected files, and the respective utilities created to alter the files:

CL: Channel Length

Utilities:

*maskchg**As channel length is changed from the default value (0.8 μm), the two mask files **MASK0** and **MASK1** as well as the grid generation files **NMOS(PMOS).MASK** (these files are incorporated in addition to **MASK0** and **MASK1** of original recipes to solve some grid generation problems as discussed later) must be changed. The corresponding source program *maskchg.c* is a C-program which takes the device type and the new channel length as the input. It reads in the mask files, determines which dimensions on the masks have to be changed, and by how much, and writes the new dimensions to the new mask files, which are to be placed in the device sub-directory.

*defchg** The device definition files **NMOS.DEFINE** and **PMOS.DEFINE** inform TSUPREM4 the gate length, how the simulation region is defined, the well type, etc. *defchg.c* is a C-program written to update the device definition files. It takes the device type and the new channel length as the input. It reads in **NMOS.DEFINE** for an n-MOS device and **PMOS.DEFINE** for a p-MOS device, alters the following parameters according to the new channel length: LGATE (gate length), XSTART (where the simulation region starts), XSTOP (where the simulation region stops), and X0 (centre of the simulation region, and where the reflection of the region takes place), and writes the new device definition file into the device sub-directory.

TO: Gate Oxide Thickness

Utility:

*goxchg**The recipe file **GATE_OXIDE** is modified when the required TO is not the default 175 Å. *goxchg.c* is a C program which takes the new gate oxide thickness as the input. The original recipe in **GATE_OXIDE** specifies two stages for growing oxide. The first stage is by diffusion with dry oxygen. A layer of 137 Å thick oxide is grown. Then the second stage is by oxide deposition. Thus *goxchg** has two cases: if the required thickness is more than 137 Å, *goxchg* specifies an oxide deposition of (TO_{new} - 137 Å) thick; otherwise, it specifies an oxide etch of (137 Å - TO_{new}) thick.

SW: Sidewall Spacer Width

Utility:

*swchg**To change the sidewall spacer width, the device definition file **BiCMOS.DEFINE**, the recipe file **NMOS_SIDEWALL_SPACER** or **PMOS_SIDEWALL_SPACER**, and the plotting definition file **NMOS_PLOT.DEFINE** or **PMOS_PLOT.DEFINE** have to be changed. The C-program *swchg.c* takes the new sidewall spacer width, the device type, and optionally the gate oxide thickness, as its inputs. In **BiCMOS.DEFINE**, the parameters WSWS (width of the sidewall spacer) and TSWS (thickness of the sidewall spacer oxide) are modified as specified by user. For the recipe files, two cases are possible, SW=0 and SW > 0. In the first case, SW=0, all of the base oxide and gate oxide as well as the sidewall spacer due to it is removed by appropriate statements in the recipe files. For SW>0, an additional TSWS is deposited after the above step (for SW=0), and finally an etch statement (THICKNESS=TSWS) produces the required sidewall spacer. For the plotting definition files, the viewing window of the device is to be 0.3 μm beyond the

sidewall spacer. These files are modified accordingly. The sidewall spacer issue required us to make some modifications in the original recipes as discussed later.

LD: LDD Level

Utility

*lddchg**:The recipe files **NMOS_LDD_IMPLANT** and **PMOS_LDD_IMPLANT** instruct TSUPREM4 to carry out LDD implantation. *lddchg.c* is a C-program which accepts the type of device and the new LDD implant dose as the input. It replaces the original dose values in the implant files with the user-specified dose values.

GD: Grid Density

Utility:

*gdchg**:The grid density is critical in achieving a balance between accuracy of numerical solutions and the computational time of the calculation. The definition file **GRID_DENSITY** informs TSUPREM4 the desired grid density. The default value is 1.0. *gdchg.c* is a C-program which takes the desired grid density as the input and puts it in **GRID_DENSITY**. Because TSUPREM4 cannot accept a grid density of 0, when the user defines GD=0, *gdchg** informs the user of such an error, and leaves **GRID_DENSITY** unchanged.

SP: Special Parameter

To modify another parameter that is not listed above, the user must provide the required script and related utilities if any to modify and transfer the appropriate recipe files,

SOURCES file etc. The path name of the user-written script should be specified for SP in the **device_form** file. Only advanced users are expected to handle this parameter.

Whenever the user has specified any of the above parameters whose values differ from the default values in the recipe files, *matrix_suprem4** places the modified files into the device sub-directory. TSUPREM4 must be informed that the new files are the ones to be used in the simulation. To that effect, the file **SOURCES** contains the named paths of the recipe and other files TSUPREM4 needs to "fabricate" a device. The UNIX alias **mod_SOURCES** is defined in *matrix_suprem4** to modify the file **SOURCES**. It takes the names of the paths to be redefined as the input. Then **mod_SOURCES** searches **SOURCES** for the pathname and changes the path from user's recipes sub-directory to the device sub-directory.

To simulate the fabrication of a MOSFET, the four instruction input files **WELL**, **DEVICE_WELL**, **DEVICE**, and **BACKEND** are run in this sequence and the resultant **STRUCTURE** files as well as runtime **listing** files are placed in the device sub-directories along with the **spec_form** file containing the specs for the individual devices in the sub-directories. Also, the final (reflected) MEDICI input **STRUCTURE** files **NMOS(PMOS)_STRUCTURE.MEDICI** are also placed in the device sub-directories. The utility *mosS4chg** is used to modify the **NMOS(PMOS)_SUPREM4.DEFINE** files to be used by MEDICI. These files are first copied into the device sub-directories after the simulation and then modified according to the specs of individual devices. The utility *mosS4chg** takes as input the device type and the physical parameters (CL, TO, SW) of the device to be simulate.

IV. Changes to Original Process Recipes

For the proper use of the virtual factory scheme, we had to make a few changes in the original recipes to remove some of the difficulties we faced while using the recipes for simulation. These changes/issues are listed below.

(i) Refining Simulation Grids

As we have found out, the grids generated by TSUPREM4 in the original recipes are not very suitable for use by MEDICI. The TSUPREM4 grids are not dense enough at the source/drain junctions critical for determinig the device electrical characteristics. Also, regrids by MEDICI for doping profiles and potentials are observed to distort the shape of the source/drain junctions. This distortion is not desirable. We were therefore advised by TMA to create denser and more appropriate (for device simulation with MEDICI) grids right at the TSUPREM4 level itself. Therefore, the TSUPREM4 grids are modified so that they are dense enough at the source/drain junctions for MEDICI to determine device characteristics. This was done by modifying the **INITIALIZE** file and incorporating two new files **NMOS.MASK** and **PMOS.MASK**. Instead of **MASK0**, now we use **NMOS(PMOS).MASK** to generate the grid, thus enabling us to go to reasonably dense grids. Correspondingly, we changed the file **EPI** and the file **SOURCES** (a new pathname **MGRDDIR** for the **NMOS(PMOS).MASK** files has been added. Under the present scheme, a grid density of 0.5 appears to be appropriate for process as well as device simulation.

Also, we had observed in some cases that the nitride(metal) over gate poly falls over the edge of poly. To avoid this situation we have changed the CM-L level in the **MASK1** file to keep the nitride(metal) 10 nm inside the poly edge.

(ii) A New Recipe for Sidewall Spacer

TSUPREM4 did not obtain the default sidewall spacer width (0.2 μm) with the original recipe. It gave a sidewall spacer of approximately 0.26 μm. The presence of the base oxide, which is essential to fabricating bipolar devices, before the sidewall spacer process is the main concern of the original recipe. Therefore, a new recipe for generating and controlling the sidewall spacer by TSUPREM4 has been developed.

In this recipe, the base oxide is first removed completely. This is achieved in two steps. In the first step, the base oxide is etched vertically for a thickness of the base oxide layer plus the gate oxide. After this step, only the step coverage oxide, right beside the poly gates, is left. This oxide hump is etched away in the second step. If the sidewall spacer (SW) is specified as 0, we stop at this point. However, for non-zero sidewall spacer, we proceed as follows.

A layer of oxide is deposited on top of the structure. The relationship of the thickness of this oxide TSWS and the simulated sidewall spacer width SW is found to be

$$SW \cong TSWS$$

from a simulation experiment. Hence we use the thickness TSWS of the sidewall spacer oxide to be the same as the sidewall spacer length SW specified by user. The file **BiCMOS.DEFINE** is modified accordingly. Finally, this oxide is etched by a thickness of TSWS. The oxide remaining beside the gate will be the desired sidewall spacer.

In order to implement the above procedure, we have created two files **NMOS_SIDEWALL_SPACER** and **PMOS_SIDEWALL_SPACER** in place of the earlier **SIDEWALL_SPACER**. Also, the **DEVICE** file is changed accordingly.

V. Matrix Device Simulation

Matrix device simulation is performed using the script *matrix_medici** which picks up the simulated (with TSUPREM4) virtual devices from the respective sub-directories and runs MEDICI on those to produce I-V data in corresponding device simulation sub-directories. The file **device_form** in this case is produced by the user, and it instructs the program where to look for the virtual device results obtained with TSUPREM4. A typical **device_form** file placed in the user's **~/medici/bicmos** level looks like the following:

```
2
NMOS
DN=NMOS_SW0.1
medici_bat1
NMOS
DN=NMOS_SW0.2
medici_bat2
```

In the above example, 2 NMOS devices are requested for simulation. They vary in spacer width, one with 0.1 μm, and the other with 0.2 μm. The sub-directory name parameter DN instructs *matrix_medici** to look for the virtual devices in the user's **~/suprem4/bicmos/**NMOS_SW0.1 and **~/suprem4/bicmos/**NMOS_SW0.2 respectively. The simulation results after MEDICI simulation are to be placed in the sub-directories with the same name under the user's **~/medici/bicmos** level. Initially, a zero bias initial solution of the structure is performed using the MEDICI input file NMOS(PMOS)_STRUCTURE.IN and the solution results are placed in the respective directories. The batch file **medici_bat1** (or **medici_bat2**) contains instructions as to which MEDICI input files to run to obtain specific I-V data. A typical medoci_bat1 (or medici_bat2) file may look like the following:

```
cd ~/medici/batmos/NMOS_SW0.1
mybias -d 5 -t 2
medici NMOSIMP_VG.IN
```

In the above batch file the *mybias* unix script is used to bias the device appropriately before a particular simulation. In this case the MOSFET is biased with a drain bias of 5V. The parameter -t 2 indicates that MEDICI should perform an approximate energy balance solution, as opposed to a drift diffusion solution (-t 1) or a full energy balance solution (-t 3). Finally the MEDICI input file NMOSIMP_VG.IN is run to generate substrate and gate current data. Similarly, we could run other input files such as NMOS_VG.IN to generate I_{DS} vs. V_{GS} data, or NMOS_VD.IN to generate I_{DS} vs. V_{DS} data. We could also include in the above batch file invocation to utilities that convert MEDICI-generated I-V data LOG files to normal column formatted files for post-processing using PV-WAVE.

VI. Matrix Parameter Extraction

Once we have generated the I-V data in the respective sub-directories, we use AURORA to do SPICE parameter extraction. Both measurement data (collected using AURORA itself) and simulation data are used for parameter extraction. The matrix scheme as suggested fig. A1.1 is yet to be established. At this time, user intervention is required in the parameter extraction process.

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Appendix 2: Models for 2-D Simulation

I. The basic equations

We solve the three basic semiconductor equations, Poisson's equation, and the electron and hole continuity equations, for electrostatic potential ψ, electron and hole concentrations, n and p respectively [A2.1].These equations are given below as (A2.1), (A2.2), and (A2.3).

$$\varepsilon \nabla^2 \psi = -q\,(p - n + N_D^{+} - N_A^{+}) + \partial_s, \tag{A2.1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet \boldsymbol{J}_n - U_n \text{ , and} \tag{A2.2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet \boldsymbol{J}_p - U_p. \tag{A2.3}$$

In the above equations, ε is silicon permittivity, N_D^{+} and N_A^{-} are the ionized donor and acceptor concentrations respectively. The term ∂_s corresponds to fixed charge in oxide or charged interface states. U_n and U_p represent net electron and hole recombination rates respectively. The current densities J_n and J_p are computed from electric fields $\boldsymbol{E}_n$ and $\boldsymbol{E}_p$, and n and p using the following equations.

$$J_n = q\mu_n n\boldsymbol{E}_n + qD_n \nabla n, \text{ and} \tag{A2.4}$$

$$J_p = q\mu_p p\boldsymbol{E}_p - qD_p \nabla p, \tag{A2.5}$$

where μ_n and μ_p are the electron and hole mobilities, and D_n and D_p are the electron and hole diffusivities respectively. The electric field vectors $\boldsymbol{E}_n$ and $\boldsymbol{E}_p$ are computed from the solution variable ψ using the following relation.

$$\boldsymbol{E}_n = -\nabla\left(\psi + \frac{kT}{q} ln\left(n_{ie}\right)\right), \text{ and} \tag{A2.6}$$

$$\boldsymbol{E}_p = -\nabla\left(\psi - \frac{kT}{q} ln\left(n_{ie}\right)\right). \tag{A2.7}$$

The above equations include the effective intrinsic carrier concentration n_{ie} as a result of the bandgap narrowing effect discussed later in this appendix.

II. The generation recombination process

The recombination rate U ($=U_n = U_p$) has been assumed to be the sum of Shockley-Read-Hall (SRH) recombination rate and Auger recombination rates given by,

$$U = U_n \approx U_p = U_{SRH} + U_{Auger},$$

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie} \cdot exp\left(\frac{E_t}{kT}\right)\right] + \tau_n\left[p + p_{ie} \cdot exp\left(\frac{-E_t}{kT}\right)\right]}, \tag{A2.8}$$

$$U_{Auger} = C_{cn}^{AU}\left(pn^2 - n_{ie}^2 n\right) + C_{cp}^{AU}\left(np^2 - n_{ie}^2 p\right).$$

In the above description of recombination, we have used the default value of E_t (=0) to place the recombination center in the SRH recombination process right at the mid-gap for most efficient recombination. We have used values of electron and hole lifetimes τ_n and τ_p as concentration dependent parameters, as discussed below. Also, the effective intrinsic carrier concentration n_{ie} is computed from temperature and bandgap narrowing effects. The values of the Auger capture coefficients C_{cn}^{AU} and C_{cp}^{AU} are taken from literature and they are $5\text{x}10^{-32}$ cm^6/s [A2.2] and $9.9\text{x}10^{-32}$ cm^6/s [A2.3] respectively. We

have used the following empirical relations for space-dependent lifetimes $\tau_n(x,y)$ and $\tau_p(x,y)$ for SRH recombination mentioned above.

$$\tau_n(x,y) = \frac{\tau_{n0}}{a_n + b_n\left(\frac{N_D+N_A}{N_n}\right) + c_n\left(\frac{N_D+N_A}{N_n}\right)^{nn}} \quad \text{, and} \qquad \text{(A2.9)}$$

$$\tau_p(x,y) = \frac{\tau_{p0}}{a_p + b_p\left(\frac{N_D+N_A}{N_p}\right) + c_p\left(\frac{N_D+N_A}{N_p}\right)^{pp}} \quad . \qquad \text{(A2.10)}$$

The constants τ_{n0}, a_n, b_n, c_n, nn, N_n and τ_{p0}, a_p, b_p, c_p, pp, N_p were determined experimentally (not as a part of the research work reported in this thesis) during the technology development phase for the devices used in our experiments and they differ from the default values set in MEDICI. Their values used in our simulations are listed in TABLE A1.1 below.

TABLE A1.1.

Parameters for doping dependent lifetimes					
τ_{n0}	=	8×10^{-6}s	τ_{p0}	=	5×10^{-6}s
a_n	=	2.03	a_p	=	0.0042
b_n	=	254.8	b_p	=	38.3
c_n	=	13.1	c_p	=	58.6
nn	=	1.72	pp	=	2
N_n	=	1×10^{18}	N_p	=	6.7×10^{18}

III. Bandgap narrowing

The bandgap narrowing effect determines an effective intrinsic concentration $n_{ie}(x,y)$ as a function of the total ionized impurity concentration ($N_D^+ + N_A^-$) and the temperature dependent intrinsic concentration $n_i(T)$, given by [A2.4],

$$n_{ie}(x,y) = n_i(T) \cdot$$

$$exp\frac{q \cdot 9x10^{-3}}{2kT}\left[ln\left(\frac{N_D^{+} + N_A^{-}}{1x10^{17}}\right) + \sqrt{ln^2\left(\frac{N_D^{+} + N_A^{-}}{1x10^{17}}\right) + 0.5}\right]. \quad \text{(A2.11)}$$

In the above empirical formula, $n_i(T)$ is taken as the default value for room temperature in our case, since all our calculations are at room temperature.

IV. The mobility models

The values of μ_n and μ_p used in equations (A2.4) and (A2.5) are modelled as a product of the low field mobility μ_{0n} or μ_{0p} with a term that models the effect of perpendicular electric field, and another term that models the effect of parallel electric field. We show below the expressions used for μ_n only, because we analyzed only NMOS transistors for this thesis. Similar expressions hold for PMOS transistors.

The low-field mobility μ_{0n} is given by [A2.5],

$$\mu_{0n} = \mu_{n0} + \frac{\mu_{n1}}{1 + \frac{N_D + N_A}{N_{ref}}}. \quad \text{(A2.12)}$$

The constants μ_{n0} and μ_{n1} were adjusted to 100 and 2200 cm^2/V-s to get good fit to experimental I_{DS}-V_{DS} and I_{DS}-V_{GS} curves. The value of N_{ref} used in our calculations was $1.26x10^{17}/cm^3$, set as default in MEDICI. The perpendicular electric field effect is modelled [A2.6] as

$$\mu_{Sn} = G_{Sn} \cdot \frac{\mu_{0n}}{\sqrt{1 + E_{\perp n}/E_{\perp n}^{C}}}. \qquad \text{(A2.13)}$$

In the above equation $E_{\perp n}$ is the components of electric field perpendicular to the side of a simulation element, while, $E_{\perp n}^{C}$ is the critical electric field for electrons to implement this model, and G_{Sn} is the low-field surface reduction factor for electron mobilities. These reduction factors are only applicable at interfaces between semiconductor and insulator. Everywhere else, they should be considered to have values of unity. We have adjusted the value of $E_{\perp n}^{C}$ to be 8.62×10^4 V/cm, while G_{Sn} =1 has been used as with the MEDICI default.

The effect of the parallel component of the electric field on mobility can be modelled using analytical expressions for the drift velocity v_d as a function of the electric field E_x in the direction of current flow and defining $\mu(E_x) = v_d(E_x)/E_x$. For silicon regions, the low field mobility is modified according to the following expression [A2.7],

$$\mu_n = \frac{\mu_{Sn}}{\left[1 + (\mu_{Sn} \cdot E_{xn}/v_{satn})^{\beta_n}\right]^{1/\beta_n}}. \qquad \text{(A2.14)}$$

The values of β_n and v_{satn} were adjusted to 1.5 and 1.035×10^7 cm/s respectively.

We also adjusted the electron affinity of polysilicon to obtain a good fit to the measured data. The values of χ_{poly} used to get reasonable curve-fits ranged from 4.275 eV for the asymmetric transistor to 4.4 eV for the symmetric device

V. Substrate current

For the calculation of substrate currents, **MEDICI** has two models for simulating the impact ionization generation rate. The first model is electric field dependent, while the second model is carrier temperature dependent.

The first model for calculating the total impact ionization generation rate G^{II} is given by the classical Chynoweth's formulas [A2.8].

$$G^{II} = \alpha_{n,ii} \cdot \frac{|J_n|}{q} + \alpha_{p,ii} \cdot \frac{|J_p|}{q}, \text{where}$$

$$\alpha_{n,ii} = \alpha^{\infty}_{n,ii} \cdot exp\left[-\left(\frac{E^{C}_{n,ii}}{E_{xn}} \right)^{\beta_n} \right], \qquad \text{(A2.15)}$$

$$\alpha_{p,ii} = \alpha^{\infty}_{p,ii} \cdot exp\left[-\left(\frac{E^{C}_{p,ii}}{E_{xp}} \right)^{\beta_p} \right].$$

where $\alpha_{n,ii}$ and $\alpha_{p,ii}$ are the electron and hole ionization coefficients, respectively. They have a unit of cm^{-1}. $\alpha^{\infty}_{n,ii}$ and $\alpha^{\infty}_{p,ii}$ are electron and hole ionization coefficients for very high fields. $E^{C}_{n,ii}$ and $E^{C}_{p,ii}$ are the critical electric fields for electron and hole ionization, E_{xn} and E_{xp} are the electric field components in the direction of current flow. The exponents β_n and β_p have been extracted by many authors to have a value of 1 [A2.9]. This model is an empirical model, as several fitting parameters are required for its implementation.

MEDICI calculates the generation rate at each node of the simulation mesh based on the electric field and the current density. The generation rate is integrated over the entire device to obtain the total impact ionization current.

The second model is derived from the classical local electric field-dependent Chrynoweth law and the homogeneous case temperature-field relation:

$$G_n^{II}(u_{Tn}) = \frac{\alpha_{n,ii}^{\infty}}{q} \cdot |\boldsymbol{J_n}| \cdot exp\left[-\left(\frac{u_{T,crit}}{u_{Tn}-u_{T0}}\right)^{\beta_n}\right], \qquad \text{(A2.16)}$$

where u_{T0} is the lattice thermal energy (kT_0/q), u_{Tn} is the electron thermal energy (kT_n/q), and

$$u_{T,crit} = \frac{2}{3} \cdot v_{satn} \cdot \tau_{wn} \cdot E_{n,ii}^{C}, \qquad \text{(A2.17)}$$

where τ_{wn} is the electron energy relaxation time, given as 2.0 x 10^{-13}s for silicon. Impact ionization generation rate for holes has similar equations. We have adjusted $\alpha_{n,ii}^{\infty}$ and $E^{C}_{n,ii}$ to 1.075x10^6 /cm and 1.7x10^6 V/cm respectively for substrate current calculations using the carrier temperature dependent model. The value of T_n was calculated using an approximate energy-balance solution discussed below.

VI. Gate current

MEDICI utilizes the lucky-electron concept [A2.10] to model the gate current of a MOSFET. Basically, the model calculates probabilities for certain scattering events to occur that will lead to carriers being injected into the gate.

The total gate current (per unit length perpendicular to the simulation plane) may be obtained by integrating the flux of electrons injected into the gate from each location in the device structure:

$$I_g = \iint \Gamma_n(x,y)|\boldsymbol{J_n}(x,y)|dxdy \ , \qquad \text{(A2.18)}$$

where Γ_n and Γ_p are probabilities per unit length that electrons or holes in the vicinity of the point (x,y) will be injected into that gate; they are products of the probability factors for the various scattering events involved:

$$\Gamma_n = \frac{P_{\Phi_{b,n}} P_{s,n} P_{in,n}}{\lambda_{r,n}}. \tag{A2.19}$$

For an electron to be collected by the gate, it must acquire enough kinetic energy from the electric field to surmount the potential barrier in the insulator and then be re-directed toward the semiconductor-insulator interface. The factor $\lambda_{r,n}$ represents the probability per unit length that an electron gets redirected without losing a significant amount of energy. The factor $P_{\Phi_{b,n}}$ is the probability that an electron will acquire enough kinetic energy to surmount the insulator potential barrier $\Phi_{b,n}$, and will retain the appropriate momentum after re-direction. $P_{\Phi_{b,n}}$ may be expressed as

$$P_{\Phi_{b,n}} = 0.25\left(\frac{\lambda_n E_{xn}}{\Phi_{b,n}}\right) exp\left[-\left(\frac{\Phi_{b,n}}{\lambda_n E_{xn}}\right)\right], \tag{A2.20}$$

where λ_n is the hot electron scattering mean-free path, and $\Phi_{b,n}$ in eV may be expressed as

$$\Phi_{b,n}(E_{ox} > 0) = 3.2 - B_n \cdot \sqrt{E_{ox}} - \vartheta \cdot E_{ox}^{2/3} - \Delta\psi_{int}. \tag{A2.21}$$

E_{ox} is the transverse electric field in the insulator, B_n is the barrier lowering factor due to the image field, ϑ is the factor for the possibility of tunneling, and $\Delta\psi_{int}$ is the potential difference between the interface and the point (x,y). In the case that $E_{ox} < 0$ (a repelling field for electrons), $P_{\Phi_{b,n}}$ is set to zero.

After gaining enough kinetic energy and being re-directed in the appropriate direction, the electron must not be scattered again before reaching the peak of the potential barrier in the insulator if it is to be collected by the gate. $P_{s,n}$, the probability that an electron will not be scattered in the semiconductor before reaching the interface, is

$$P_{s,n} = exp(-\frac{d_{int}}{\lambda_n}), \tag{A2.22}$$

where d_{int} is the distance from the point (x,y) to the interface. Finally, $P_{in,n}$, the probability that an electron will not scatter in the insulator between the interface and the potential barrier peak, is

$$P_{s,n} = exp(-\sqrt{\frac{E_{ox}^{C}}{E_{ox}}}). \tag{A2.23}$$

where E_{ox}^{C} is a critical electric field for electron scattering in the insulator.

In the electron temperature dependent lucky electron model that we have used for our calculations, the electron temperatures $T_{e,n}$ calculated from an approximate energy balance solution (discussed below) was used to compute the longitudinal electric fields E_{xn} used in eqn. (A2.20). The following formula [A2.11] was used for this evaluation.

$$E_{xn} = \frac{3kT_{e,n}}{2qv_{satn}\tau_{wn}}. \tag{A2.24}$$

In order to get a reasonably good fit to the measured gate currents we had to adjust the value of λ_n to 6 nm from the default value of 9.2 nm. Other parameters were taken at their default value used in **MEDICI**.

VII. The energy balance equations

While the traditional drift-diffusion model, described earlier, yields good approximation for many occasions, it fails to include the inevitable cooling effect which occurs on impact under accelerating field. Moreover, carriers travelling in a strong accelerating field require a certain time until they gain sufficient energy for impact ionization; the drift-diffusion model has neglected this effect. Thus the drift-diffusion solutions overestimate the impact ionization generation rate and hence the substrate current. Since substrate current and gate current have been two parameters examined closely in this work, the drift-diffusion solutions are simply not good enough. Therefore, the energy balance models were necessary for the computation of I_B and I_G.

For generating the approximate energy balance solutions, a carrier temperature-based model is used for impact ionization instead of the electric field model whenever impact ionization is specified for the solution. Current density becomes more generalized, with temperature-dependency incoporated in it,

$$J_{(n,p)} = q\mu_{(n,p)} \cdot \left[\binom{n}{p} \cdot E_{(n,p)} \pm \nabla \left(\binom{n}{p} \cdot u_{T0} \right) \right]. \qquad \text{(A2.25)}$$

Furthermore, the hydrodynamic model includes the following electron and hole energy balance equations [A2.12] [A2.13] including transient effects and carrier cooling due to impact ionization:

$$\nabla \bullet S_{(n,p)} = \frac{1}{q} J_{(n,p)} \bullet E_{(n,p)} - \frac{3}{2}\left[\binom{n}{p} \cdot \frac{u_{T(n,p)} - u_{T0}}{\tau_{w(n,p)}} + \frac{\partial}{\partial t}\left(\binom{n}{p} \cdot u_{T(n,p)} \right) \right] + E_g G^{II}_{(n,p)} , \qquad \text{(A2.26)}$$

$$S_{(n,p)} = \mp\frac{5}{2}u_{T(n,p)}\left[\frac{J_{(n,p)}}{q} \pm \kappa_{(n,p)}\mu_{(n,p)} \cdot \binom{n}{p} \cdot \nabla u_{T(n,p)}\right]. \quad \text{(A2.27)}$$

where $S_{(n,p)}$ is the energy flow density of electrons/holes, and $\kappa_{(n,p)}$ represents electron/hole thermal conductivity coefficient. The other terms have been explained earlier. The equations (A2.25), (A2.26), and (A2.27) have been written in compact form to apply for both electrons and holes. The carrier temperature-dependent impact ionization is adopted but the mobility is still electric field dependent. The thermal diffusion term in the generalized current density expression and the mobility model using the carrier mean energy (temperature) are not utilized. They would apply to a full energy balance solution. In this work, the approximate energy balance model is utilized in favour of the full energy balance model for faster computations at very little cost in terms of accuracy.

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Appendix 3: Derivation of eqns. (5.1) & (5.2)

Equation 5.1

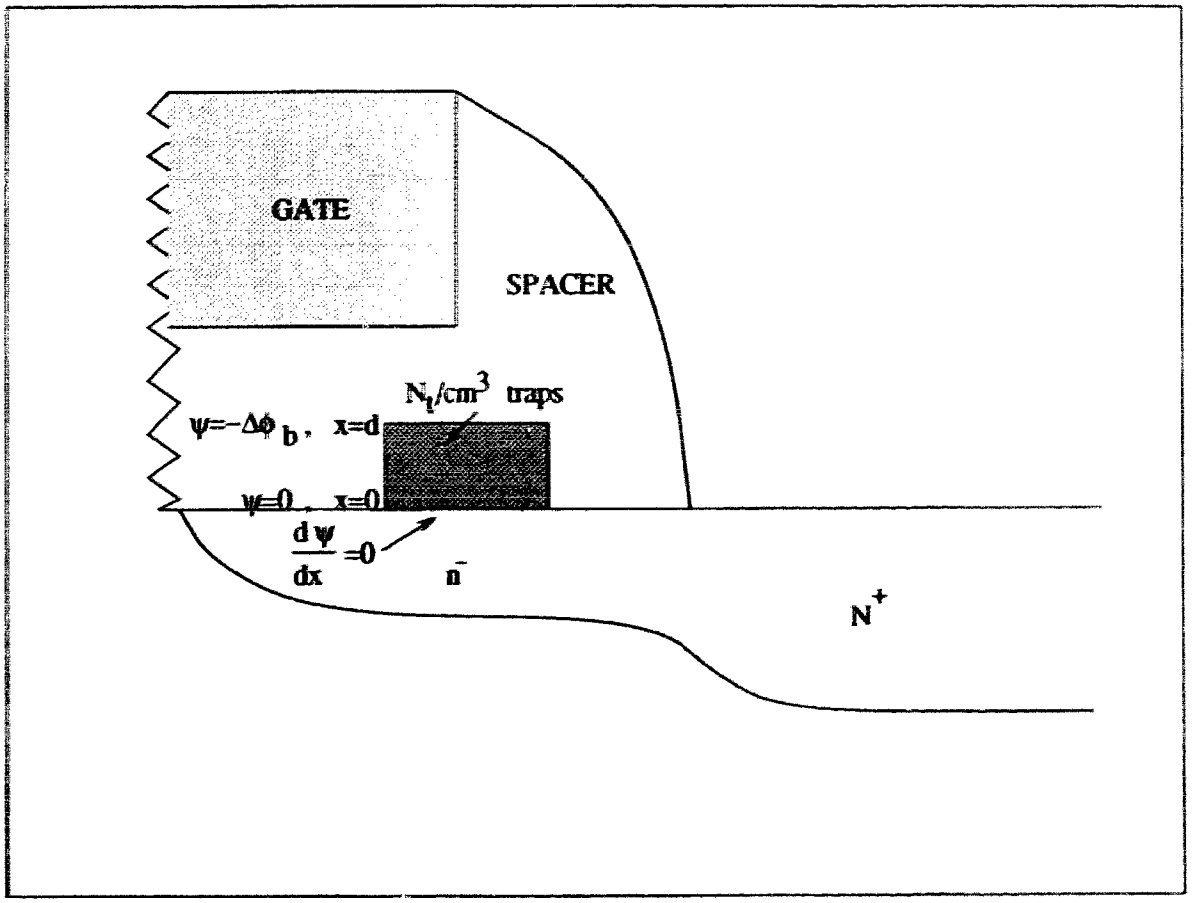

Fig. A3.1. The magnified picture of the gate edge region with negatively charged defects.

At x=0, i.e., at the interface, we assume the local potential ψ and its derivative with respect to x to be both 0, i.e.,

$$\psi = 0$$
$$\frac{d\psi}{dx} = 0 \qquad \text{(A3.1)}$$

The latter assumption is valid since $V_{GS} \cong V_{DS}$ for the floating gate measurement, and the n^- region is near metallic.

We can then write a one-dimensional Poisson's equation for the trap box as,

$$\frac{d^2\psi}{dx^2} = \frac{-N_t q}{\varepsilon_{ox}} \tag{A3.2}$$

where, N_t is the trap density in numbers/cm^3, q is the electronic charge, and ε_s is silicon permittivity. On integration of (A3.2) twice with respect to x, and application of the initial conditions as listed in (A3.1), we obtain

$$\psi = -\frac{N_t q}{\varepsilon_{ox}} \frac{x^2}{2} \tag{A3.3}$$

Substituting x=d, and $\psi = -\Delta\phi_b$ in (A3.3) we obtain

$$\Delta\phi_b = \frac{N_t q}{\varepsilon_{ox}} \frac{d^2}{2} = \frac{N_t q d}{\frac{\varepsilon_{ox}}{(d/2)}} = \frac{N_t \cdot d \cdot q}{C_{0.5d}} \tag{A3.4}$$

Equation 5.2

As depicted in fig. 5.15 of chapter 5, we assume an advancing defects profile of a fixed density N_{it} given by an empirically correct unknown function $F(t \cdot (I_D/W) \cdot \exp[-\phi_{it}/(q\lambda E)])$, where λ is electron mean free path, W is device width, q is electronic charge, and E is the local lateral electric field. We can then frame the following equation,

$$t_0\left(\frac{I_D}{W}\right) exp\left(\frac{-\phi_{it}}{q\lambda E_m}\right) = t\left(\frac{I_D}{W}\right) exp\left(\frac{-\phi_{it}}{q\lambda E}\right) \tag{A3.5}$$

for any $t=t_1$, t_2, etc. On transformation, we obtain,

$$\frac{q\lambda}{\phi_{it}} ln\left(\frac{t}{t_0}\right) = \left[\frac{1}{E} - \frac{1}{E_m}\right]. \tag{A3.6}$$

As shown in fig. 5.2, the electron temperature (T_e) at a particular combination of gate and drain biases fall towards the channel with a linear slope of s. Since the lateral electric fields are proportional to T_e, we can describe E as,

$$E = E_m - sx \tag{A3.7}$$

illustrated in fig. 5.14. Substituting the above value of E in (A3.6) and after some algebraic transformation, we obtain,

$$x = \frac{\frac{E_m}{s} \cdot ln\left(\frac{t}{t_0}\right)}{\frac{\phi_{it}}{q\lambda E_m} + ln\left(\frac{t}{t_0}\right)}. \tag{A3.8}$$

Appendix 4: Publications arising out of this thesis

Refereed Journal Publications:

1. A. Raychaudhuri, M.J. Deen, M.I.H. King and W. Kwan, *"Features and Mechanisms of the Saturating Hot-Carrier Degradation in LDD MOSFETs"*, **IEEE Transactions on Electron Devices,** Vol. 43(7), pp. 1114-1122 (July 1996).

2. A. Raychaudhuri, M.J. Deen, M.I.H. King and J. Kolk, *"Finding the Asymmetric Parasitic Source and Drain Resistances from the A.C. Conductances of a Single MOS Transistor"*, **Solid-State Electronics,** Vol. 39(6), pp. 909-913 (June 1996).

3. A. Raychaudhuri, M.J. Deen, M.I.H. King and J. Kolk, *"A Simple Method to Qualify the LDD Structure Against the Early Mode of Hot-Carrier Degradation"*, **IEEE Transactions on Electron Devices,** Vol 43(1), pp. 110-115 (January 1996).

4 W.S. Kwan, A. Raychaudhuri and M.J. Deen, *"Location and Quantification of the Interface Defects in Stressed MOSFETs Using a Combination of Floating Gate and Transconductance Techniques, and Charge Pumping Methods"*, accepted for publication to **Canadian Journal of Physics**, 20 ms pages, (September 1995).

5. A. Raychaudhuri, J. Kolk, M.J. Deen and M.I.H. King, *"A Simple Method to Extract the Asymmetry in Parasitic Source and Drain Resistances from Measurements on a MOS Transistor"*, **IEEE Transactions on Electron Devices,** Vol. 42(7), pp. 1388-1390 (July 1995).

Refereed Conference Publications:

6. A. Raychaudhuri, W.S. Kwan, M.J. Deen and M.I.H. King, *"Propagation of Defects in Hot-Carrier Degradation of LDD NMOSFETs - From the Early Mode to the Late Mode"*, **Proc. of ISDRS '95**, Charlottesville, Virginia, pp. 781-784 (6-8 December 1995).

7. A. Raychaudhuri, M.J. Deen, M.I.H. King, and J. Kolk, *"A Simple Method to Extract the Parasitic Resistances from a Single MOSFET Using Measurements of Small-Signal Conductances"*, **25th European Solid-State Device Research Conference (ESSDERC '95)**, The Hague, Nederland, pp. 749-752 (25-27 September 1995).

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