CHARACTERIZATION, SIMULATION AND OPTIMIZATION OF TYPE-II GAASSB-BASED DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS

by

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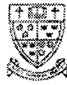

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ABSTRACT

In recent years, GaAsSb/InP double heterojunction bipolar transistors (DHBTs) have been demonstrated to be promising alternatives to InP/InGaAs HBTs, for next generation microwave/millimeter wave applications and optoelectronic integrated circuits (OEICs). However, GaAsSb-based DHBTs featuring the novel base material and type-II band alignment have not been well studied. This thesis investigated type-II GaAsSb DHBTs in the following aspects: periphery surface recombination current, Kirk effect, two dimensional (2D) simulation and device optimization. The present work provided insights into device operation, and guidances for further device development.

A series of physical models and parameters was implemented in 2D device simulations using ISE TCAD. Band gap narrowing (BGN) in the bases was characterized by comparing experimental and simulated results. Excellent agreements between the measured and simulated DC and RF results were achieved.

Emitter size effects associated with the surface recombination current were experimentally characterized for emitter sizes of 0.5 by 6 to 80 by 80 square micrometer. The 2D simulations by implementing surface state models revealed the mechanism for the surface recombination current. Two device structures were proposed to diminish surface recombination current.

Numerical simulations for type-II GaAsSb-InP base-collector (BC) junctions showed that conventional base "push-out" does not occur at high injection levels, and instead the electric field at the BC junction is reversed and an electron barrier at the base side evolves. The electron barrier was found to play an important role in the Kirk effect, and the electron tunnelling through the barrier delays the onset of the Kirk effect. This novel mechanism was supported by the measurement for GaAsSb/InP DHBTs with two

base doping levels. The study also showed that the magnitude of the electric field at the BC junction at zero collector current directly affects onset of the Kirk effect.

Finally, optimizations for the emitter, base and collector were carried out through 2D simulations. A thin InAlAs emitter, an (Al)GaAsSb compositionally graded base with band gap variance of 0.1eV, and a high n-type delta doping in the collector were proposed to simultaneously achieve high frequency performance, high Kirk current density and high breakdown voltage.

Keywords: Heterojunction bipolar transistor; InP; GaAsSb; device simulation

Subject Terms: Bipolar transistors – design and construction; bipolar transistors – computer-aided dsign; bipolar transistor mathematical models

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Chapter 1:

Introduction

1.1 Overview

Heterojunction bipolar transistors (HBTs) grown on InP substrates have been recognized as promising candidates for future generations of integrated circuits (ICs) operating at data rates of over 100 Gbit/s. For optoelectronic integrated circuits (OEICs), InP-based HBTs offer unique advantages over the competing SiGe/Si HBT technology, which was intensively promoted over the last few years [1]. SiGe/Si HBTs have become attractive because they leverage the mature low-cost Si technology and infrastructure. Besides OEIC applications, InP-based HBTs inherently offer material advantages over the SiGe/Si HBTs in terms of carrier transport properties and breakdown voltages. For example, SiGe/Si HBTs were recently shown to have a cutoff frequency f_T = 350 GHz but a common-emitter breakdown voltage of only BV_{CEO} = 1.4 V [2], though the InP-based HBTs can simultaneously achieve f_T > 380 GHz and BV_{CEO} > 6 V [3].

Traditionally, $In_xGa_{1-x}As$ is used as the narrow band material for InP-based HBTs because $In_xGa_{1-x}As$ has excellent electron mobility and peak electron velocity. InP/InGaAs single heterojunction bipolar transistors (SHBTs) have reached by far the highest cutoff frequency f_T = 720 GHz with graded bases [4], but due to the small band gap of the InGaAs collector, the breakdown voltage BV_{CEO} is only 1.7 V, which is nearly as low as that found in the highest frequency SiGe/Si HBTs. Using a wide bandgap InP collector to construct InP/InGaAs/InP double heterojunction bipolar transistors (DHBTs)

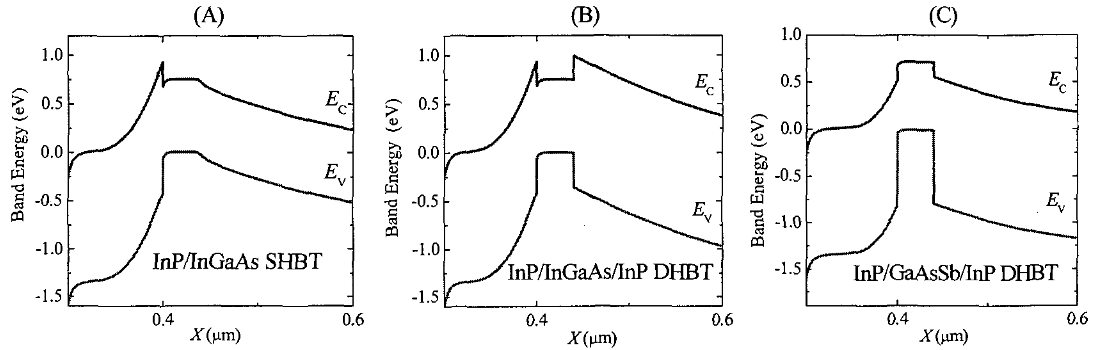


Figure 1-1: Energy band diagrams for (A) type-I InP/InGaAs SHBT, (B) type-I InP/InGaAs/InP DHBT without compositional grading, and (C) type-II abrupt junction InP/GaAsSb/InP DHBT.

can in principle greatly improve the breakdown voltage [5, 6]. Still, an electron blocking barrier then occurs as a result of the type-I [1]conduction band alignment between the InGaAs and InP (see Fig. 1-1B), and must be suppressed by a compositionally graded layer inserted between the InGaAs base and the InP collector [7]. Implementing compositionally graded layers increases the device design complexity and complicates the epitaxial layer growth. In addition, while thinner collectors may result in higher speeds, experimental trends demonstrate that InP/InGaAs DHBTs with collectors thinner than 0.1 μm tend to lose their breakdown voltage advantage over InP/InGaAs SHBTs [3]. Another drawback of the grading scheme is that because the grading layer causes asymmetry in the BE and BC junctions, the device offset voltage may increase [8]. This offset voltage is defined as the collector-emitter voltage at which the collector current is zero, in the forward biased common emitter configuration. A low offset voltage is helpful to minimize power dissipation and is a necessity in some low supply-voltage applications.

In a type-II GaAsSb/InP DHBT (see Fig. 1-1C) consisting of a GaAsSb base, and the InP collector and emitter[2] layers, the aforementioned electron barrier does not exist between the base and the collector because the GaAsSb conduction band edge sits above

---

[1] Three possible band edge alignments between two materials denoted by 1 and 2 are: type-I, if $E_{C1} < E_{C2}$, and $E_{V1} > E_{V2}$; type-II, if $E_{C1} > E_{C2}$, and $E_{V1} > E_{V2}$; type-III, if $E_{V1} > E_{C2}$.

[2] Other wide bandgap materials such as InAlAs [9] and InAlP [10] have also been used as the emitter materials.

the InP conduction band edge. Furthermore, an electron launcher (ΔE_C) at the BC junction due to the conduction band offset between GaAsSb and InP may enhance the electron overshoot into the collector [11]. Because of their symmetric BE and BC abrupt junctions, InP/GaAsSb/InP DHBTs have experimentally demonstrated a low offset voltage of < 0.1 V [12]. This is particularly beneficial for lowering circuit power consumption. More importantly, GaAsSb/InP DHBTs have experimentally shown by far the highest Johnson limit (defined as the product of cut-off frequency and breakdown voltage) $f_T \times BV_{CEO} > 2280$ GHz-V [3].

In 2001, InP/GaAsSb/InP DHBTs fabricated in the Compound Semiconductor Device Laboratory (CSDL) of SFU demonstrated world record high-speed performance: $f_T > 300$ GHz [13]. Since then, GaAsSb/InP DHBTs have drawn much interest from both industry [9, 14, 15] and academia [3, 16-18]. While most of the research has focused on the GaAsSb/InP devices, some circuit applications that use GaAsSb/InP DHBTs have been reported [19, 20]. More interestingly, the type-II GaAsSb/InP unitraveling carrier photodiodes (UTC-PDs) for applications of near 1.55 μm wavelength have shown a bandwidth of 105 GHz [21]; type-II GaAsSb/InP double heterojunction bipolar light-emitting transistors (HBLETs) have been experimentally demonstrated to have light emission of 1.6 μm wavelength [22]. All of these achievements indicate that type-II GaAsSb/InP DHBTs are a promising candidate for the next generation microwave/millimeter wave applications and OEICs.

Compared to the InP/InGaAs HBTs, the GaAsSb/InP DHBTs feature two important differences: a novel base material GaAsSb, and a rather unusual type-II energy band alignment for a bipolar transistor. InGaAs has been extensively studied, in part thanks to its optoelectronic applications, and most physical properties of InGaAs are well-characterized in the literature. In contrast, many physical properties of GaAsSb such as minority carrier mobility, surface states and band gap narrowing, have not been documented. The type-II band alignment distinguishes the GaAsSb/InP DHBTs from other III-V HBTs, however, the detailed implications of this band structure to the device characteristics (e.g., electron transport across BE and BC junctions and high injection phenomenon) have not yet been thoroughly studied.

1.2 Emitter Size Effects of GaAsSb/InP DHBTs

Emitter size effects (ESEs), which arise from periphery surface recombination currents associated with the extrinsic base region, have a strong influence on the scalability of all HBTs because ESEs reduce the DC current gain with decreasing emitter sizes. InP/InGaAs HBTs display ESEs [23] unless an effective surface passivation is applied [24]. As a promising alternative to the InP/InGaAs HBTs, GaAsSb/InP DHBTs should also be investigated in terms of the ESEs, especially when the devices are scaled to deep submicron dimensions to maximize both the transistor dynamic performance and transistor counts in integrated circuits. This investigation can help us to understand the mechanism for the periphery surface recombination, and guide further investigations pertaining to the passivation and reliability of GaAsSb/InP DHBTs.

Surface recombination can arise through two possible mechanisms [25]: 1) the two-dimensional (2D) potential at the emitter mesa intersection with the extrinsic base surface directly injects electrons from the emitter onto the extrinsic base surface [26] where they no longer contribute to the transistor gain, and eventually recombine through Shockley–Read–Hall (SRH) dynamics and/or at the base contact (hereafter "mechanism A"); and 2) electrons injected into the intrinsic base region directly under the emitter experience large angle scattering and deflection to the extrinsic base surface region before they subsequently recombine ("mechanism B") [27]. GaAsSb/InP and InP/InGaAs systems are fundamentally different in emitter/base injection mechanisms. Whereas GaAsSb/InP devices rely on a type-II emitter-base junction dominated by thermal injection, InP/GaInAs HBTs involve hot electron injection from the type-I InP emitter. In this thesis work, we compare the experimental periphery current density (the total periphery current divided by the emitter perimeter, which is denoted as $K_{B,Surf}$) of GaAsSb/InP DHBTs with that of InP/InGaAs SHBTs, revealing the mechanism for the surface recombination. Based on the experimental observation, we model the surface recombination current for GaAsSb/InP DHBTs by means of the sophisticated simulation program: ISE TCAD v. 7 [28]. Modelling results are then compared with the experimental data.

1.3 High Injection Effect in GaAsSb/InP DHBTs

At high collector current levels, the increasingly significant mobile electron density may change the electric field profile in the space charge region. This high injection phenomenon featuring the Kirk effect has received close attention in the study of HBTs because HBTs must routinely be operated at high current densities in both analogue and digital circuits to maximize their operating speeds. The Kirk effect originally referred to the hole spreading from the base into the collector (base push-out) when the electric field at the base-collector (BC) junctions decreases to zero due to high collector current density [29]. The Kirk effect in SHBTs with homojunction collectors (e.g., AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs SHBTs) has been well studied [30-32]. Mazhari *et al.* [33] first pointed out that the high current effects in BC heterojunctions such as SiGe/Si DHBTs appear to be different from that in BC homojunctions because of the valence band offset. Few studies of the Kirk effect in type-I InP/InGaAs DHBTs have been reported. The reason for this is not clear, but it is noted that the valence band offset between InP and InGaAs is relatively smaller ($\Delta E_V \sim 0.35$ eV) and the BC junction is usually compositionally graded. Therefore, compared to the type-II GaAsSb/InP abrupt BC junction, the graded InP-InGaAs BC junction is conceptually closer to a homojunction. Bolognesi [34] first pointed out that the mechanism for the Kirk effect in type-II GaAsSb/InP DHBTs is essentially different from the classic one for BC homojunctions. The electron blocking effect in GaAsSb/InP DHBTs at high injection level has been mentioned [35, 36], though no thorough investigation has been reported. In the present work, we first theoretically compare the Kirk effect in GaAsSb/InP DHBTs to that in AlGaAs/GaAs SHBTs (as a prototype of BC homojunctions) using numerical simulations. We then experimentally characterize the Kirk current densities for GaAsSb/InP DHBTs. A comparison of the modelling results and the measured data discloses a new mechanism for the high injection effect in GaAsSb/InP DHBTs.

1.4 Numerical Simulation

Device simulation provides us the ability to carry out "virtual experiments" without processing real wafers. Thus, we can explore various device designs using

numerical simulations, and implement the most promising design in the actual fabrication. Naturally, simulation results are only as valid as the physical models and the material parameter values used by the model. Due to the lack of the measurement data for the GaAsSb alloy material parameters, the simulation for GaAsSb/InP DHBTs presents a number of challenges. Nevertheless, a comparison between experimental measurements and simulation results can help not only to understand the device operation, but to adjust the material parameters as well. A number of simulation results for GaAsSb/InP DHBTs have been reported: Parikh *et al.* first used the Monte Carlo (MC) method to study electron transport in the devices [37]; Balaraman *et al.* performed the simulation using the drift-diffusion model [38]; and Belhaj *et al.* [39], Maneux *et al.* [40] and Vicente *et al.* [41] performed 2D simulations using the hydrodynamic model. None of the previous works addressed the issue of surface states and recombination, which is important for the scaling of sub-micron DHBTs. Also, no comparison between measured and simulated results has been shown in terms of high frequency performance, and a better match of DC characteristics between experimental and simulation results is also necessary to better guide the development of the next generation of ultrahigh performance GaAsSb/InP DHBTs.

Technology Computer Aided Design (TCAD) tools have been widely used for semiconductor device, process and circuit simulations, and have reached an especially mature state for silicon-based applications. Today, advanced computer technology makes the TCAD tools increasingly more powerful and sophisticated, e.g., going from one dimensional (1D) to full three dimensional (3D) simulations. There is a wide variety of commercial device simulation programs. ISE TCAD v. 7 [28] is a product of the former Integrated Systems Engineering AG (now acquired by Synopsys), and has a broad area of applicability to process, circuit, system, and complete package simulations. Its device simulator, DESSIS, features a comprehensive set of physical models that incorporates most techniques relevant to compound semiconductor devices. The popularity of ISE TCAD is evident by the increasing number of reported results [42-44] and by the fact that 18 of the top 20 semiconductor manufacturers currently make use of ISE TCAD tools [28]. In fact, this product has become one of the leading simulation tools in the semiconductor area.

Table 1-1: Comparisons of f_T, f_{max} and BV_{CEO} between InP/InGaAs HBTs and GaAsSb/InP DHBTs.

System	f_T (GHz)	f_{max} (GHz)	BV_{CEO} (V)	Reference
InP/InGaAs SHBTs	710	340	1.75	[4]
InP/InGaAs/InP DHBTs	350	500	4	[45]
InP/InGaAs/InP DHBTs	450	450	3.9	[46]
InP/GaAsSb/InP DHBTs	500	245	4	[16]
InP/GaAsSb/InP DHBTs	300	335	6	[47]

In the course of this work, we used ISE TCAD v. 7 to perform 2D simulations. Comparisons between the experimental data and the simulated results displayed an excellent agreement in both DC and RF characteristics. This is the first time in the CSDL at SFU where the 2D simulations were performed using a commercial TCAD.

1.5 GaAsSb-based DHBT Design and Optimization

As previously discussed, GaAsSb/InP type-II DHBTs have shown significant advantages over the counterpart InP/InGaAs DHBTs. However, as a promising alternative to the InP/InGaAs type-I system, the GaAsSb-based type-II system should demonstrate comparable or even higher device performances in order to provide tangible new added value. Table 1-1 lists some state-of-the-art high frequency performances for InP/InGaAs HBTs and GaAsSb/InP DHBTs: it is interesting to note that GaAsSb/InP DHBTs now offer the highest current gain cutoff frequencies f_T of all DHBTs, despite their relative lack of maturity compared to InGaAs-based devices. It is also apparent from Table 1-1 that to compete with InP/InGaAs SHBTs, GaAsSb/InP DHBTs need to show greatly improved f_T and f_{max} while maintaining the advantage of BV_{CEO}. Besides the RF performances, it would also be desirable to increase the DC current gain of GaAsSb/InP DHBTs. For deep sub-micron devices with the same thickness of the base heavily doped to $> 8\times10^{19}$ cm^{-3}, the DC gain β of InP/InGaAs HBTs can be >100 [4], but the β of GaAsSb/InP DHBTs so far is less than 30 [17]. Some of this difference comes from the differences in electron mobility between the GaAsSb and InGaAs alloys, and the rest must be accounted for by different recombination processes. The investigation of recombination in GaAsSb/InP DHBTs is therefore of great importance in order to enable further improvements in this technology.

In addition, increasing the Kirk current density of GaAsSb/InP DHBTs will also be shown to be beneficial to the device high frequency performances. After clarifying the electron blocking mechanisms in the type-II GaAsSb/InP DHBTs, we will investigate ways to further delay the electron blocking effect.

In this thesis work, we explore new designs for GaAsSb/InP DHBTs. By means of the ISE TCAD simulations, we optimize the emitter, base and collector structures. The purpose of this work is to find a solution for GaAsSb-based DHBTs to achieve a very competitive device performance with simultaneously high f_T, f_{max} and BV_{CEO} that continue to show advantages over the competing more mature technologies.

1.6 Scope of Dissertation

In this introductory Chapter, we reviewed the salient advantages of type-II GaAsSb/InP DHBTs over other HBTs. We also compared the state-of-the-art results achieved with different HBT systems. The comparison showed that type-II GaAsSb/InP DHBTs offer a promising alternative to conventional type-I InP/InGaAs HBTs. This motivated our choice of four main contribution areas for the present dissertation: 2D simulation, the study of surface recombination, the study of high-current injection effects, and device optimization for maximum performances. These considerations naturally evolved into the following four chapters. Chapter 2 describes physical models and methodologies in the 2D simulations using ISE TCAD. Simulated and measured DC and RF results are then compared. Chapter 3 discusses the periphery surface recombination current for sub-micron GaAsSb/InP DHBTs. Experimental characteristics and then 2D simulation results with surface state modelling are then presented. Two solutions for reducing the surface recombination current for GaAsSb/InP DHBTs are suggested. Chapter 4 investigates the mechanism for the high injection effect in type-II GaAsSb/InP DHBTs. A comparison of the high injection effect between type-II BC heterojunctions and BC homojunctions is carried out through numerical simulations. The importance of an electrostatically induced electron barrier at the base side of the BC heterojunction is demonstrated through experiments and simulations: this mechanism has not been discussed before in the literature. Chapter 5 develops new designs for GaAsSb-based

type-II DHBTs to reach higher DC and RF performances. Results of the optimization performed with numerical simulations for the emitter, base and collector are presented. Chapter 6 summarizes the thesis work and discusses future work on GaAsSb-based type-II DHBTs. Appendix A gives all material parameters used in the simulations. Appendix B provides definitions of two-port network parameters and their conversion formulae.

Chapter 2:

GaAsSb-based DHBT Simulation Framework

2.1 Overview

In this chapter, we discuss the two dimensional (2D) numerical device simulation of InP/GaAsSb/InP DHBTs using a sophisticated commercial TCAD package: ISE TCAD v. 7 [28]. This is the initial 2D simulation work in the SFU Compound Semiconductor Device Laboratory (CSDL), and it is motivated by the desire to optimize device geometry, materials, and composition and doping profiles to achieve higher device performance. The present Chapter sets the scene for simulation work elsewhere in the dissertation by briefly describing various aspects of the physical models used in the simulation of GaAsSb-based DHBTs.

The task of numerical simulation for semiconductor devices is to solve the Boltzmann Transport Equation (BTE), the Poisson equation, and the continuity equation simultaneously. Even by today's standards, this process is extremely computationally intensive. The most widely used simplification is the Drift-Diffusion (DD) model [48] in which the carrier gas is assumed to be in thermal equilibrium with the lattice [49], (i.e. the electron temperature T_{n}, the hole temperature T_{p} and the lattice temperature T_{L} are all equal). The electron and hole current densities are then given as

$$\mathbf{J}_{\mathrm{n}} = q\left(n\mu_{\mathrm{n}}\mathbf{E} + D_{\mathrm{n}}\nabla n + \frac{\mu_{\mathrm{n}}k_{\mathrm{B}}n}{q}\nabla T_{\mathrm{L}} \right), \quad \mathbf{J}_{\mathrm{p}} = q\left(p\mu_{\mathrm{p}}\mathbf{E} + D_{\mathrm{p}}\nabla p + \frac{\mu_{\mathrm{p}}k_{\mathrm{p}}p}{q}\nabla T_{\mathrm{L}} \right), \qquad (2\text{-}1)$$

where n and p denote electron and hole densities respectively, and the electron and hole diffusivities D_n, D_p and mobilities μ_n, μ_p satisfy Einstein relationships:

$$D_n = \frac{k_B T_n}{q} \mu_n , \quad D_p = \frac{k_B T_p}{q} \mu_p . \qquad (2\text{-}2)$$

In a steady state, electrons are in equilibrium with the lattice and the carrier drift velocity depends on the electric field **E**, e.g., $\mathbf{v}_n = \mu_n \mathbf{E}$ for electrons. In other words, the carrier velocity is said to be "local." Specifically, in the low field regime, the carrier velocity is proportional to the **E**, but beyond a certain critical electric field, a negative differential mobility appears, and the velocity falls and eventually saturates. This is true of most compound semiconductors such as GaAs and InP due to inter-valley transitions [50].

As modern devices tend to be more aggressively scaled (laterally and vertically), the spatial variation of electric field becomes so rapid that the charge carriers cannot respond instantaneously. As a result, there is a delay connecting the average carrier energy to the electric field: the velocity is "non-local." In these situations, the mobility depends on both the carrier's energy and electric field [51] and the DD model becomes invalid [52].

The Monte Carlo (MC) method is accepted to be the most reliable and precise tool for numerical simulation in that this tecnique can directly mimic the physical process of the carrier transport in crystal [53, 54]. In the MC method, each carrier is treated microscopically, and its motion in the crystal with respect to both real space and k-space is simulated. This simulation which can reproduce the distruibution fuction $f(\mathbf{r}, \mathbf{k})$ is equivalent to the solution of BTE [55]. However, the computational cost of MC simulation is so high that it cannot be routinely used, especially in an industrial setting. A hydrodynamic (or energy balance) model that provides a good compromise between computational cost and accuracy has been developed and has become a standard tool in industry for sub-micron device simulation [52]. The most important advantage of the

hydrodynamic model over the DD model is that "hot carrier" phenomena[3] can be properly described. We applied hydrodynamic model for all our HBT simulations and, for computational efficiency, we only performed two dimensional (2D) rather than three dimensional (3D) simulations.

Following the overview section, we discuss the important physical models that we applied to the device simulations. In the third Section, we introduce techniques used in the implementation of the simulation, the device structure under consideration, and some of physical parameters necessary to perform accurate simulations for GaAsSb-based devices. In the fourth Section, we give an overview of the experimental work of this thesis to understand the measurement results presented in the next section and other chapters. We then discuss some simulated results including DC and RF for InP/GaAsSb/InP DHBTs, and present comparisons between measurements and simulations in the fifth Section. The chapter is concluded in the last Section.

2.2 Physical Models

2.2.1 Hydrodynamic Model

Several different versions of hydrodynamic models have been discussed in the literature to account for the relevant physics in different applications. The model implemented in ISE DESSIS v. 7 is based on the work of Stratton [56] and Blotekjer [57]. This model also accounts for the effect of band edge energy and position on the effective carrier masses. In ISE DESSIS v. 7 the current densities are given as [58]

$$
\begin{aligned}
\mathbf{J}_\mathrm{n} &= \mu_\mathrm{n}\left(n\nabla E_\mathrm{C} + k_\mathrm{B}\nabla(T_\mathrm{n}\cdot n) - \frac{3nk_\mathrm{B}T_\mathrm{n}}{2}\nabla(\ln m_\mathrm{e})\right), \\
\mathbf{J}_\mathrm{p} &= \mu_\mathrm{p}\left(p\nabla E_\mathrm{V} - k_\mathrm{B}\nabla(T_\mathrm{p}\cdot p) - \frac{3pk_\mathrm{B}T_\mathrm{p}}{2}\nabla(\ln m_\mathrm{h})\right),
\end{aligned}
\qquad (2\text{-}3)
$$

[3] Typically, carriers are "heated" up in the regions of the device featuring very high electric field, and the carrier temperature can become very elevated because the carriers are not in thermal equilibrium with the lattice.

where E_C and E_V are the conduction and valence band edges respectively, and m_e and m_h are electron and hole effective masses respectively. Here, the first two terms account for the spatial variation of the energy bands and carrier concentrations; the last term accounts for the effective mass variations. The major difference between (2-3) and (2-1) is that carrier temperatures are allowed to be different from the lattice temperature. The most important aspect of the hydrodynamic model is the energy balance equations given as

$$
\begin{aligned}
n\frac{\partial w_n}{\partial t} + \nabla \cdot \mathbf{S}_n &= \mathbf{J}_n \cdot \nabla E_C - R w_n - n\frac{w_n - w_0}{\tau_{en}}, \\
p\frac{\partial w_p}{\partial t} + \nabla \cdot \mathbf{S}_p &= \mathbf{J}_p \cdot \nabla E_V - R w_p - p\frac{w_p - w_0}{\tau_{ep}}, \\
c_L\frac{\partial T_L}{\partial t} + \nabla \cdot \mathbf{S}_L &= R\left(w_n + w_p + E_g\right) + n\frac{w_n - w_0}{\tau_{en}} + p\frac{w_p - w_0}{\tau_{ep}},
\end{aligned} \tag{2-4}
$$

where the energy fluxes $\mathbf{S_n}$ and $\mathbf{S_p}$ are

$$
\begin{aligned}
\mathbf{S}_n &= -\frac{3}{2}\left(\frac{k_B T_n}{q}\mathbf{J}_n + \frac{k_B^2}{q} n\mu_n T_n \nabla T_n\right), \\
\mathbf{S}_p &= -\frac{3}{2}\left(\frac{k_B T_p}{q}\mathbf{J}_p + \frac{k_B^2}{q} p\mu_p T_p \nabla T_p\right), \\
\mathbf{S}_L &= -k_L \nabla T_L .
\end{aligned} \tag{2-5}
$$

Here $w_n = \frac{3k_B T_n}{2}$, $w_p = \frac{3k_B T_p}{2}$, c_L and k_L are the lattice heat capacity and thermal conductivity, respectively, and R is the recombination/generation rate. The equilibrium energy density is given as $w_0 = \frac{3k_B T_L}{2}$. In this dissertation, constant relaxation times are assumed and the TCAD default values (τ_{en} = 1 ps and τ_{ep} = 0.4 ps) are used [48, 59]. However, for more precise simulation, the relaxation times can be modelled to be lattice and carrier temperature dependent [60], and the dependency of τ_{en} and τ_{ep} on temperature has to be verified by (or more precisely, calibrated to) MC simulation [37, 59]. In this manner, hydrodynamic simulation results are tuned to match the MC simulation results.

2.2.2 Recombination Model

Shockley-Read-Hall (SRH) [55] recombination is used as a major recombination model. In this case, for a single type of spatially uniform traps, the net non-radiative recombination rate is given as

$$R_{\mathrm{net}}(SRH) = \frac{np - n_{\mathrm{i}}^2}{\tau_{\mathrm{p}}(n + n_1) + \tau_{\mathrm{n}}(p + p_1)}, \tag{2-6}$$

where $n_1 = n_{\mathrm{i}} e^{\frac{E_{\mathrm{Trap}}}{k_{\mathrm{B}}T}}$ and $p_1 = n_{\mathrm{i}} e^{\frac{-E_{\mathrm{Trap}}}{k_{\mathrm{B}}T}}$, n_{i} is the intrinsic density, and E_{Trap} is the energy separation between the defect level and the intrinsic level. The lifetimes τ_{n}, τ_{p} are doping dependent as described in the empirical Scharfetter relation [49]:

$$\tau(N_{\mathrm{i}}) = \tau_{\mathrm{min}} + \frac{\tau_{\mathrm{max}} - \tau_{\mathrm{min}}}{1 + \left(\frac{N_{\mathrm{i}}}{N_{\mathrm{ref}}}\right)^{\gamma}}. \tag{2-7}$$

Here the parameters τ_{min}, τ_{max}, γ and N_{ref} can be tuned in the model. Due to lack of the data of GaAsSb, $E_{\mathrm{Trap}} = 0$ is assumed [40]. The parameters were determined through the comparison between the simulation and measurement, which is described in Section 2.5, e.g., for electrons, $\tau_{\mathrm{min}} = 0$, $\tau_{\mathrm{max}} = 10^{-8}$ ps, $\gamma = 1$ and $N_{\mathrm{ref}} = 5\times10^{18}$ cm^{-3} in the GaAsSb base; $\tau_{\mathrm{min}} = 0$, $\tau_{\mathrm{max}} = 10^{-10}$ ps, $\gamma = 1$ and $N_{\mathrm{ref}} = 5\times10^{19}$ cm^{-3} in the InP emitter.

The dominant parasitic recombination in the base of most HBTs is Auger recombination. However, it has been experimentally found to be less of a factor in heavily doped GaAsSb HBTs [61]. We can simply ignore it for GaAsSb bases. For InP, the Auger coefficient is about 9×10^{-31} cm^6/s [62].

When electrons and holes recombine directly by emitting light, radiative recombination occurs and this effect in InP/GaAsSb/InP DHBTs has been experimentally demonstrated by Feng *et al.* [22]. Radiative recombination can be modelled as

$$R(r) = C_{\mathrm{R}}\left(np - n_{\mathrm{i}}^2\right), \tag{2-8}$$

where C_R is a coefficient. For GaAsSb, C_R is assumed to be similar to the one in InGaAs: 4×10^{-10} cm^3/s [63]; for InP, C_R is about 1.2×10^{-10} cm^3/s [62].

The above-mentioned SRH recombination model can also be applied to a surface or to an interface between two different materials, e.g., at interfaces between atmosphere or dielectrics and the semiconductor. The recombination rate at a surface is given by

$$R_{\mathrm{net}}^{\mathrm{surf}}(SRH) = \frac{np - n_{\mathrm{i}}^2}{(n+n_1)/s_{\mathrm{p}} + (p+p_1)/s_{\mathrm{n}}}, \qquad (2\text{-}9)$$

where n_1, p_1 have the same definitions as in (2-6) but here are surface (cm^{-2}) rather than volume densities (cm^{-3}). The surface recombination velocities s_{p}, s_{n} are functions of doping concentration at the surface [64], and are given by

$$s_{\mathrm{n,p}} = s_0\left[1 + s_{\mathrm{ref}}\left(\frac{N_{\mathrm{i}}}{N_{\mathrm{ref}}}\right)\right], \qquad (2\text{-}10)$$

where s_0, s_{ref} and N_{ref} are constants. For simplicity, it is assumed that surface recombination occurs only at the exact plane of the surface without any transition area between the surface and bulk where both types of recombination occur.

2.2.3 Mobility Model

The two most important scattering mechanisms for carriers in doped bulk semiconductors, at room temperature or above, are phonon scattering and impurity scattering. These lead to the dependency of carrier mobility on lattice temperature and doping level. There are several mobility models available in the ISE TCAD simulation environment, and we used the Arora model [65] because it was found to fit the empirical data for III-V semiconductors well [66]. In this model, the mobility in the presence of doping is formulated as follows:

Table 2-1: Parameters of Arora model for n-type materials

Parameter	InP	$In_{0.53}Ga_{0.47}As$	$In_{0.52}Al_{0.48}As$	Unit
μ_{min}	400	300	800	$cm^2/V\cdot s$
μ_{d}	4800	13700	400	$cm^2/V\cdot s$
N_0	3×10^{17}	1.3×10^{17}	3×10^{16}	cm^{-3}
A	0.47	0.48	1.1	1

$$\mu_{\text{Dop}} = \mu_{\text{min}} + \frac{\mu_{\text{d}}}{1+\left(\frac{N_{\text{i}}}{N_0}\right)^A}. \qquad (2\text{-}11)$$

Here N_{i} is the doping level, and parameters μ_{min}, μ_{d}, N_0 and A all are functions of lattice temperature T_{L}. The parameter values at room temperature for some representative n-type materials as listed in Table 2 -1 [66].

The above mobility model is only used to determine the low-field mobility denoted as μ_{low}. In order to model the mobility at high field for III-V semiconductors, the Transferred-Electron model [58] is used, and the high-field mobility is taken as

$$\mu_{\text{high}} = \frac{\mu_{\text{low}} + \left(\frac{v_{\text{sat}}}{F}\right)\left(\frac{F}{E_0}\right)^4}{1+\left(\frac{F}{E_0}\right)^4}. \qquad (2\text{-}12)$$

At room temperature, saturated velocity v_{sat} is set to be a constant, and E_0 is a reference parameter. F is called the driving force which, for the hydrodynamic model, is given by

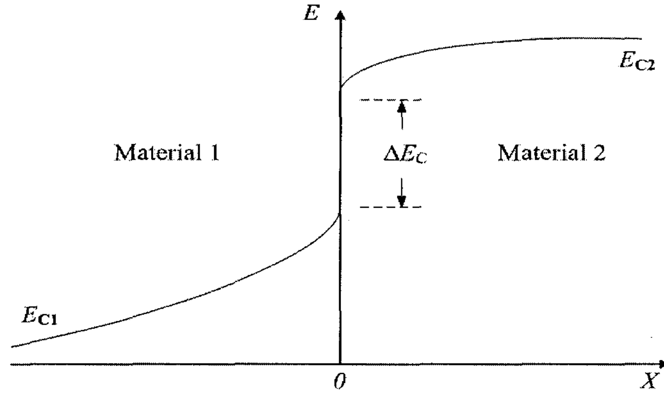


Figure 2-1: Conduction band example of an abrupt heterojunction.

$$F = \sqrt{\frac{3k_B(T_C - T_L)}{2\tau_{e,c} q \mu_{high}}} . \qquad (2\text{-}13)$$

Here T_C is carrier temperature, and $\tau_{e,c}$ is the carrier energy relaxation time. The high field-mobility is obtained by substituting (2-13) into (2-12) and solving for μ_{high}. Based on the comparison between the simulated and measued average electron velocity in the InP collector [67], E_0 and v_{sat} were determined as 6.5×10^3 V/cm and 1.5×10^7 cm/s respectively.

Magneto-transport measurements have been used to characterize the minority-carrier electron mobility in the base of bipolar transistors [68, 69]. In order to determine the minority carrier electron mobility in the base of GaAsSb, we carried out magneto measurements on GaAsSb/InP DHBTs with very thin GaAsSb bases (250Å) and high p-doping levels (4×10^{19} cm^{-3}). The effective minority electron mobility in 250 Å GaAsSb bases was ~ 400 $cm^2/V\cdot s$. According to the observation in [70], the electron mobility in bulk InGaAs is over three times higher than that in thin InGaAs bases (500 Å). By analogy with this result, we assume that the bulk electron mobility in p-type ($4\times10^{19}cm^{-3}$) GaAsSb is ~ 1200 $cm^2/V\cdot s$. This value yields good agreement with the transistor delay times measured for devices fabricated in our laboratory [67].

2.2.4 Thermionic Emission and Barrier Tunneling Models

2.2.4.1 Thermionic Emission

At abrupt heterojunctions, such as that shown in Fig. 2-1, thermionic emission models need to be considered to describe the transport of electrons from one material to another [71]. Thermionic emission occurs when electrons in material 1 have enough thermal energy to overcome the barrier (ΔE_C) to enter material 2. We assume that an electron will not scatter back across the interface if electron mean free path, λ, in material 2 is greater than a distance, d_T, over which the electron potential drops by $k_B T/q$. Normally, the electric field at most HBT interfaces is high enough to prevent backscattering with $\lambda >> d_T$ [55].

If $J_{n,2}$ and $S_{n,2}$ are the electron current density and electron energy flux density entering material 2 and $J_{n,1}$ and $S_{n,1}$ are the electron current density and electron energy flux density leaving material 1, then (Page 166, [71])

$$J_{n,2} = J_{n,1},$$

$$S_{n,2} = S_{n,1} + \frac{1}{q} J_{n,2} \Delta E_C, \qquad (2\text{-}14)$$

$$J_{n,2} = 2q\left[v_{n,2} - \frac{m_2}{m_1} v_{n,1} n_1 \exp\left(-\frac{\Delta E_C}{k_B T_{e,1}} \right) \right], \qquad (2\text{-}15)$$

$$S_{n,2} = -4\left[v_{n,2} n_2 k_B T_{e,2} - \frac{m_2}{m_1} v_{n,1} n_1 k_B T_{e,1} \exp\left(-\frac{\Delta E_C}{k_B T_{e,1}} \right) \right]. \qquad (2\text{-}16)$$

Here, subscript 1 and 2 denote material 1 and 2 respectively, and m_1 and m_2 are electron effective masses, $T_{e,1}$ and $T_{e,2}$ are electron temperatures, n_1 and n_2 are electron densities, and ΔE_C is the conduction band offset, i.e. barrier height. The emission velocities $v_{n,1}$ and $v_{n,2}$ are defined as

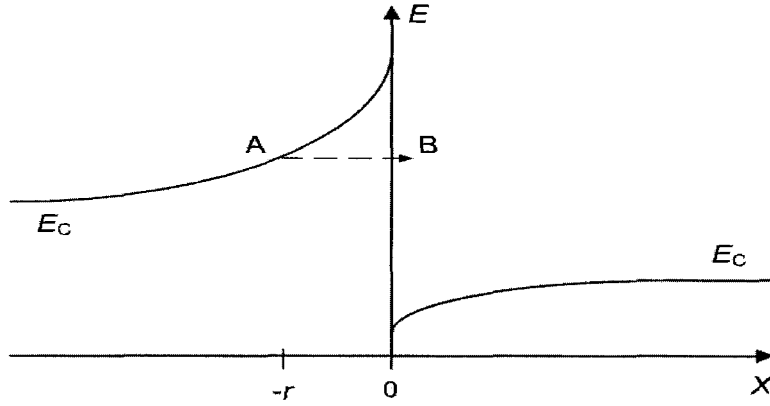


Figure 2-2: Non-local recombination / generation for tunnelling mechanism.

$$v_{n,i} = \sqrt{\frac{k_B T_{e,i}}{2\pi \cdot m_i}}, \qquad (2\text{-}17)$$

where $i = 1$ and 2. Similarly, we can have the thermionic equations for holes.

2.2.4.2 Barrier Tunnelling

Quantum mechanical tunnelling through barriers is often an important mechanism for carrier transport at heterojunction interfaces. In order to model such a non-local process in ISE TCAD, barrier tunnelling is treated as a recombination/generation process [72]. The tunnelling process shown schematically Fig. 2-2, is modelled by an electron recombining (disappearing) at Point A in order to be generated (re-appearing) at Point B. The generation and recombination rates in the continuity equation are proportional to the tunnelling probability Γ_{WKB}, which is evaluated by using the WKB (Wentzel-Kramers-Brillouin) approximation [73] in ISE TCAD. The WKB approximation is used in solving the time-independent one-dimentional Schrödinger equation, and inherently assumes that the electron potential varies slowly on the scale of the wavelength of an electron wave packet [74]. This condition is of course not satisfied at Point B in Fig. 2-2, but the approach offers a compromise between physical accuracy and ease of computation. The detailed formulation of the tunneling model as implemented in ISE TACD can be found in [58].

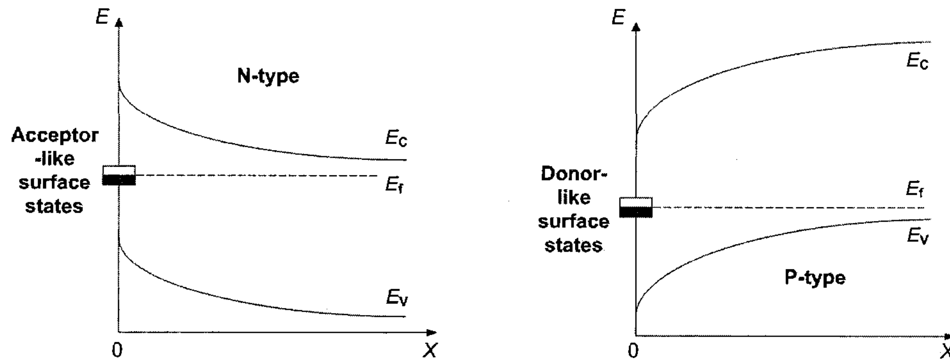


***Figure 2-3:** Schematic diagrams of band bending due to charged surface states for n-type and p-type semiconductors (Page 60, [75]).*

Except at high injection levels, the importance of tunnelling in type-II GaAsSb/InP DHBTs is not as high as in type-I InP/InGaAs/InP DHBTs. This issue will be discussed in Chapter 4. It should be noted that the implementation of the abovetunnelling model was found to easily cause the simulation to fail due to convergence problem. The reason has not been clarified yet, but sometimes, the problem may be avoided by adjusting mesh structure or excluding other models such as surface states from the simulation.

2.2.5 Fermi Level Pinning and Surface State Model

At semiconductor interfaces, especially between the semiconductor and vacuum, air, or dielectrics, there are often so-called "surface states" located in the band gap. Surface states can be caused by a number of reasons, such as interruption of the atomic periodicity at the surface leading to dangling bonds or reconstruction of the surface atoms, surface contamination or adatoms, and native or adsorbate-induced defects which might occur on the surface during processing [75]. There are typically two types of surface states within the band gap: acceptor-like and donor-like. Surface states may be populated by carriers from the bulk, depending on the position of the surface state relative to the bulk Fermi level. At thermal equilibrium, the occupation of surface states results in a space charge which causes energy band bending near the surface [75]. Fig. 2-3 schematically shows the respective band bending situations for an n-type semiconductor with acceptor surface states, and for a p-type semiconductor with donor

surface states. Note that there would be no band bending if an n-type semiconductor were to only have acceptor-like states with energy levels located below the Fermi level, or if a p-type semiconductor had only donor-like states with energy levels above the Fermi level. In such cases, surface states would not be charged. Sometimes, as in the case of InP, both acceptor and donor states can coexist at the semiconductor surface. This can thus result in band bending at the surface for both n and p-type materials [76, 77].

If band bending occurs due to surface states, the distance between the Fermi level energy and the conduction band edge at the surface is different from that in the bulk. When the surface state density is high enough, the Fermi level position at the surface can be considered to be fixed, regardless of the bulk doping level. This effect is referred to as the "Fermi level pinning" of the surface.

DESSIS provides a comprehensive trap model that can be used to model bulk and surface recombination as well as surface Fermi level pinning. We implement only singular energy levels instead of energy distributions for each acceptor or donor state, as the experimental results for InP surfaces have shown [78]. This simplification was found to be adequate to model the surface Fermi level pinning. We further assume that these surface states act as recombination centres.

In the presense of traps, Poisson's equation is given as

$$\nabla \cdot \varepsilon \nabla \varphi = -q\left[p - n + N_{\mathrm{d}} - N_{\mathrm{a}} + \left(N_{\mathrm{Dt}} - n_{\mathrm{Dt}}\right) - \left(N_{\mathrm{At}} - p_{\mathrm{At}}\right)\right], \qquad (2\text{-}18)$$

where, N_{Dt} and N_{At} are the donor and acceptor trap densities respectively. Here $n_{\mathrm{Dt}} = N_{\mathrm{Dt}} \cdot f_{\mathrm{n}}$ and $p_{\mathrm{At}} = N_{\mathrm{At}} \cdot f_{\mathrm{p}}$, where f_{n} and $f_{\mathrm{p}} = 1 - f_{\mathrm{n}}$ are the electron and hole occupation probabilities respectively. In a steady state, where $\frac{d(n,p)}{dt} = 0$, the recombination rate for one trap level is given by

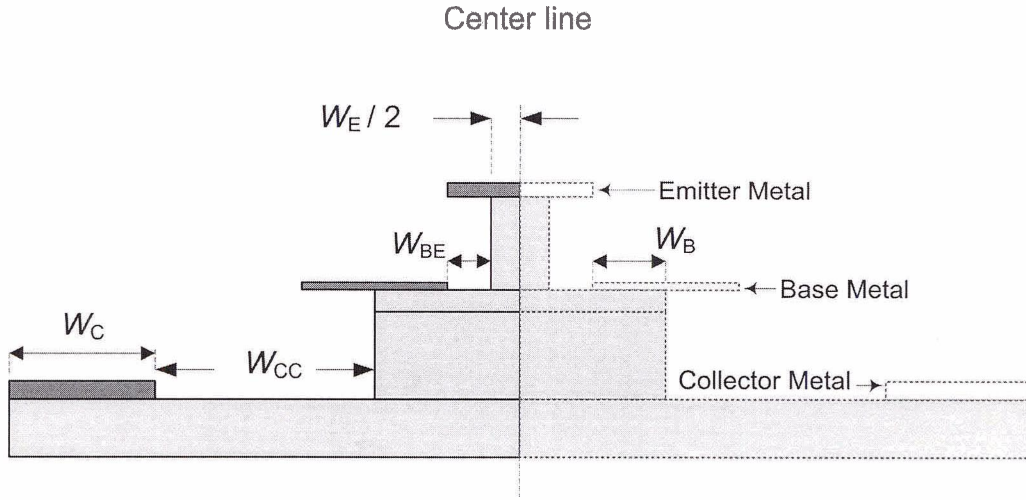


Figure 2-4: Schematic cross-section of an actual triple mesa HBT.

$$R_t = N_t \frac{v_{th}^n \sigma_n v_{th}^p \sigma_p (np - n_i^2)}{v_{th}^n \sigma_n (n + n_1) + v_{th}^p \sigma_p (p + p_1)}, \qquad (2\text{-}19)$$

where N_t is the trap density, v_{th}^n and v_{th}^p are the thermal velocities (at 300K) for electrons and holes. σ_n and σ_p are the electron and hole capture cross-sections, $n_1 = n_i e^{\frac{E_t}{k_B T}}$, $p_1 = n_i e^{\frac{-E_t}{k_B T}}$, and E_t is the energy separation between the trap level and the intrinsic level.

At interfaces or surfaces, all densities and concentrations are taken per unit area. Referring to (2-9) the surface recombination velocities S_n and S_p can be written as: $S_n = N_t v_{th}^n \sigma_n$ and $S_p = N_t v_{th}^p \sigma_p$. Note that in the non-equilibrium case, the trap capture cross section may be field dependent, and then the surface recombination velocity is no longer a constant.

2.3 2D Simulation for GaAsSb/InP DHBTs

2.3.1 Device Structures

The simulated device structure is based on [8], and is symmetrical with respect to the centre line of the device (see Fig. 2-4). For computational efficiency, we limit

ourselves to simulating half of the actual device. For the actual device structure, the collector metal is quite wide ($W_C \sim 20$ μm) and sits more than 1 μm away from the side wall of the collector mesa. Because the sub-collector is highly doped, we can ignore the extrinsic part (W_{CC}) and simply place the collector metal underneath the collector in the simulated device structure [40, 48]. In this way, we can shrink the lateral size of simulated device to further increase computational efficiency. As seen in Fig 2-5, this simplification results in no significant difference from the simulations of the full size device. However, in the case of high power operation, the extra substrate material affects the treatment of severe self-heating, so the entire half structure is needed [48]. A typical simulated device structure is shown in Fig. 2-6 in which the base, collector and collector metal have the same width of ($W_E/2 + W_B + W_{BE}$) (see Fig. 2-4 for definitions). In the simulated structure, we also assume that the InGaAs and InP emitter layers have the same lateral width ($W_E/2$), and that the GaAsSb base and InP collector have the same width ($W_B + W_{BE}$). In reality, these assumptions may not be correct due to differences between InGaAs, InP and GaAsSb wet etching rates, and the emitter side wall may exhibit a negative or positive slope with respect to the extrinsic base surface depending on the orientation of the emitter stripe.

With the wet etches employed in our process, a spacing (W_{BE}) of 0.1 μm is usually achieved between the base metal and the emitter sidewall [25]. Table 2-2 lists typical device dimensions used in our device simulations.

2.3.2 Physical Parameters and Considerations

The most important models, and pertinent variables and parameters were introduced in Section 2.1. Some special simulation considerations and physical parameters are presented here. InGaAs and InP have been well studied and most of their physical parameters are easily found in the literature. However, the same cannot be said for GaAsSb. In cases where specific parameters for GaAsSb were not available, they were found through the linear interpolation between GaAs and GaSb. Composition dependency for most parameters was disabled in order to simplify the simulation. For instance, $In_{0.53}Ga_{0.47}As$ was used in all of our GaAsSb HBTs, hence it was not necessary

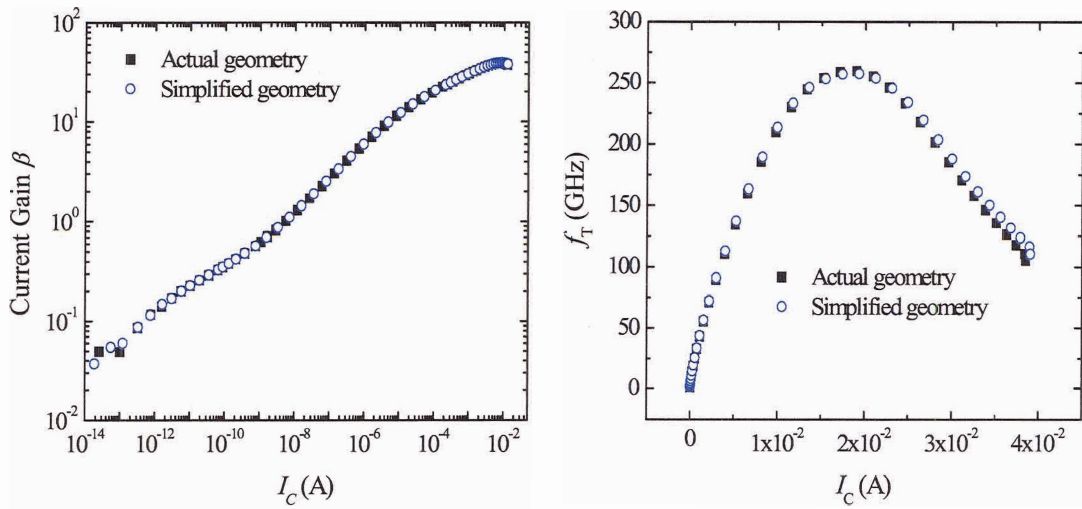


Figure 2-5: Comparisons of AC and DC simulation results between the structures of actual dimension and the simplified dimension (the collector metal sits right underneath the collector).

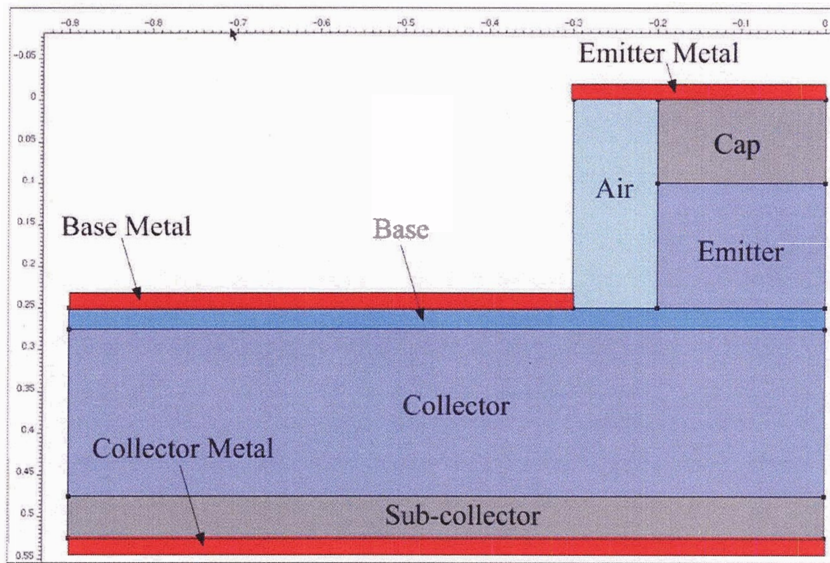


Figure 2-6: A typical 2D layout of simulated devices.

Table 2-2: Typical Dimensions of simulated devices based on #6671

Layers	Vertical Thickness (μm)	Lateral Width (μm)
Emitter metal	—	0.35
$In_{0.53}Ga_{0.47}As$ cap	0.1	0.25
InP cap	0.05	0.25
InP emitter	0.07	0.25
$GaAs_{0.51}Sb_{0.49}$ base	0.025	0.95
Base metal	—	0.6
InP collector	0.2	0.95
$In_{0.53}Ga_{0.47}As$ sub-collector	0.05	0.95
Collector metal	—	0.95

to introduce the mole fraction dependent models for $In_xGa_{1-x}As$, and only the parameters for this specific composition were included. Some variables in the physical models can be adjusted as mentioned in the previous section. Table 2-3 gives several critical parameter values at room temperature, some of which might need to be changed according to the particular simulation requirements. In the case of GaAsSb, band gap narrowing associated with changes of band offsets (ΔE_C, ΔE_V) has been reported [39, 40]. In our simulations, it was found that the GaAsSb band parameters have significant impacts on the results, and this topic will be discussed in detail later. More properties and parameters of various materials can be found in Appendix A.

To model the contact resistances of the emitter, base and collector electrodes, we used typical experimental results measured by transmission line method (TLM). There are two ways to implement contact resistances: (1) they are automatically calculated by the program based on the specific contact resistance we defined in the input file; or, (2) they are manually calculated and added to the extrinsic resistances in the two-port network as shown in Fig. 2-8. The first method may lead to a failure in the simulation depending on the choice of mesh structure. For this reason, we chose the second method for our simulations. The three contact resistances can be manually calculated using the following formulae (Pages 714-719, [81]):

Table 2-3:   Some important material parameters [62, 79, 80].

Parameters	InP	$In_{0.53}Ga_{0.47}As$	$GaAs_{0.51}Sb_{0.49}$	$In_{0.52}Al_{0.48}As$
Electron affinity (eV)	4.38	4.63	4.23	4.18
Dielectric permittivity	12.4	13.9	14.2*	12.4
Band gap (eV)	1.35	0.75	0.68**	1.44
Electron effective density of states(cm^{-3})	5.66×10^{17}	2.8×10^{17}	2.42×10^{17}	5.11×10^{17}
Hole effective density of states (cm^{-3})	1.1×10^{19}	6.0×10^{18}	7.8×10^{18}	8.98×10^{18}

* From linear interpolation of GaAs and GaSb (see Appendix A).
** At a doping level of ~ 4×10^{19} cm^{-3}.

$$R_{CE} = \frac{2r_{CE}}{L_E W_E},$$

$$R_{CB} = \frac{\sqrt{R_{ShB} r_{CB}}}{L_E} \coth\left(W_B \sqrt{\frac{R_{ShB}}{r_{CB}}}\right), \qquad (2\text{-}20)$$

$$R_{CC} = \frac{\sqrt{R_{ShC} r_{CC}}}{L_E} \coth\left(W_C \sqrt{\frac{R_{ShC}}{r_{CC}}}\right).$$

Here, r_{CE}, r_{CB} and r_{CC} are the emitter, base and collector specific contact resistances respectively in units of Ωcm^2. R_{ShB} and R_{ShC} are the base and collector sheet resistances respectively in units of Ω/□. L_E is the emitter stripe length, and W_E, W_B and W_C are defined in Fig. 2-4. It should be noted that experimental contact resistances may exhibit significant wafer-to-wafer and run-to-run variations.

In our simulations, the devices were exposed to ambient temperatures (T = 300K). Since the device thermal resistance and self-heating effect were ignored, the device lattice temperature was also set to the same value [58]. Actually, all device measurements in the present work were carried out at room temperature.

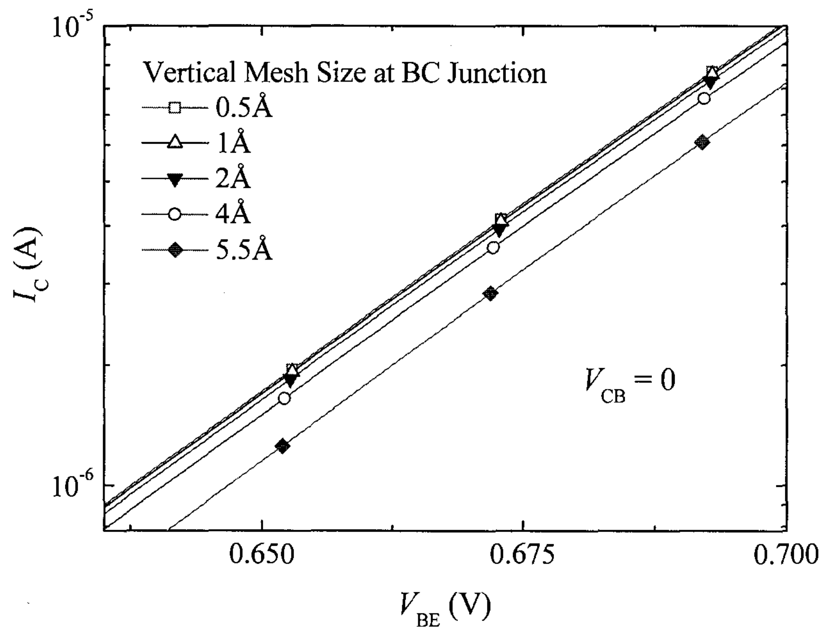


Figure 2-7: Simulated collector versus base-emitter bias for a InP/GaAsSb/InP DHBT with various mesh sizes around the base-collector junction. The vertical mesh size at base-emitter junction is 1.5 Å.

2.3.3 Doping and Mesh Setup

All epilayers in our HBTs were uniform in doping and composition except where intentionally graded bases are considered. Although an incomplete ionization model is available in the TCAD, we assumed 100% dopant ionization for simplicity in setting our n and p-type concentrations because, for most devices, the data of doping level is obtained from Hall measurements which directly show the ionized dopant concentrations.

Building a mesh is indispensable for a simulation since most modern TCAD programs employ finite element analysis to perform their numerical computations. A mesh is generated to divide the device area into a large number of elements or nodes, each of which represents one data point of the calculation. The mesh spacing can significantly affect simulations, and important results may be missed because of poor mesh choice. Therefore, for regions where physical quantities change rapidly, e.g., interfaces and PN junctions, a finer mesh is needed. MDRAW can automatically create the mesh for a device based on user-defined criteria. In practice, the width and length of

each device are significantly larger than the thickness, so the lateral mesh size is more relaxed than the vertical one. This is true except for the intersection area between the emitter sidewall and the extrinsic base. Details of the mesh building algorithm can be found in [58].

Using an excessively refined mesh can result in computational requirements exceeding our current resources. It was also found that an inappropriate mesh structure could cause the simulation to fail under certain conditions. Fig. 2-7 shows the simulated collector current versus base emitter bias with different mesh refinements at the BC junction. We can see that there is no significant change of the collector current when the vertical mesh size is less that 2 Å. Therefore, it would be adequate in terms of the accuracy to maintain the refined mesh less than 2 Å at the BE and BC junctions which are the most critical areas in HBTs. Mesh optimization proved to be a constant challenge in our numerical simulations.

2.3.4 RF Simulation

In ISE TCAD, one can not only perform simulations for a single device, but also perform mixed-mode simulations for a combination including a small number of devices and/or circuits. In a HBT, there are parasitic capacitances and resistances that affect the overall device performance. These parasitic elements are added to the intrinsic device as shown in Fig. 2-8. The inductances are usually ignored for small signal characterization [81] as their added impact is minimal. In the AC simulations, *Y*- parameters (see Appendix B) are obtained by examining the current response at one port to the small signal voltage at another port, and the *Z*-, *H*- and *S*- parameters are then calculated by conversion from the *Y*-parameters (see Appendix B).

f_T and f_{max} are the most important small-signal figures-of-merit, and they can be determined through a number of methods in ISE TCAD. We employed the common theoretical definitions: f_T occurs at unity current gain $|H_{21}| = 1 = 0$ dB, and f_{max} occurs at unity of Mason's unilateral gain (MUG), i.e.,

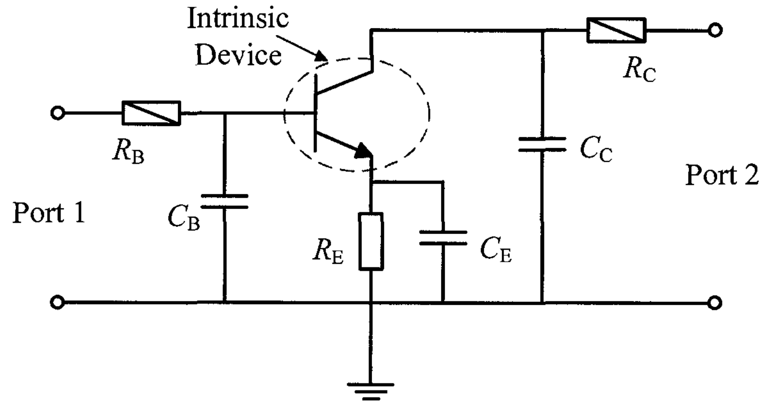


Figure 2-8: A two-port circuit for RF mixed mode simulation. The intrinsic device refers to the one defined in 2D MDRAW as previously described. All resistors and capacitors represent the parasitic effects.

$$MUG = \frac{|Z_{21} - Z_{12}|^2}{4[\Re(Z_{11}) \cdot \Re(Z_{22}) - \Re(Z_{12}) \cdot \Re(Z_{21})]} = 1 = 0\,\text{dB}. \qquad (2\text{-}21)$$

At extremely high frequencies, gain curves may not follow a –20 dB/decade roll-off because of increasingly dominant parasitic elements. In such cases, another method may be used, in which the –20 dB/decade line is extrapolated to unity from a set point where the gain drops by a specified amount from its low-frequency value, e.g., 10 dB.

2.4 Experimental Work Overview

Before introducing the experimental results in the following sections and chapters, we need to describe briefly the experimental work performed in this thesis work. There are four wafer structures used in this work: #6671, #4720, #4450 and #4451. #6671 was primarily used for the study of the emitter size effect and high cut-off frequency f_T measurement; #4720 was used for exploring high maximum frequency of occilation f_{max}; #4450 and #4451 were used to investigate the base band gap narrowing effect and base controlled Kirk effect.

Table 2-4: Epi-layer structures of #4451 and #4450

Layers	Nominal Thickness (Å)	Measured Thickness (Å)	Nominal Doping Level (cm^{-3})
$In_{0.53}Ga_{0.47}As$ cap	1000	1100	(Si): 1×10^{19}
InP cap	500	550	(Si): 3×10^{19}
InP emitter	1000	1100	(Si): 3×10^{17}
$GaAs_{0.59}Sb_{0.41}$ base	400	400	(C): 5×10^{19} (#4450) (C): 5×10^{18} (#4451)
InP collector	5000	5500	(Si): 1.0×10^{16} (CV measured) ~1.5×10^{16}
$In_{0.53}Ga_{0.47}As$ sub-collector	500	660	(Si): 1×10^{19}
InP sub-collector	3000		(Si): 3×10^{19}

2.4.1 Wafer Epilayers

Wafer #6671 was industrially grown by MOCVD at Nortel Networks (Ottawa, ON), and growth details were reported in [15]. The epi-layer stack consists of an n^+ 1000 Å $Ga_{0.47}In_{0.53}As$ cap, a 500 Å InP emitter contact layer Si-doped to 1×10^{19} cm^{-3}, a 700 Å InP emitter Si-doped to 1×10^{17} cm^{-3}, a 250 Å $GaAs_{0.51}Sb_{0.49}$ base with C-doping to 5×10^{19} cm^{-3}, a 2000 Å InP collector doped to 2×10^{16} cm^{-3} with Si, a heavily doped 500 Å GaInAs etch-stop layer, and a 3000 Å InP sub-collector doped with Si at 1×10^{19} cm^{-3}.

Wafer #4720 was grown by MOCVD at SFU, and the epi-layer stack consists of an n^+ 1000 Å $Ga_{0.47}In_{0.53}As$ cap doped to 1×10^{19} cm^{-3}, a 700 Å InP emitter contact layer Si-doped to 3.8×10^{19} cm^{-3}, a 500 Å InP emitter Si-doped to 2.4×10^{17} cm^{-3}, a 100 Å InP spacer without intentional doping, a 250 Å (nominal thickness is 200 Å) $GaAs_{0.59}Sb_{0.41}$ base C-doping to 9×10^{19} cm^{-3}, a 2000 Å InP collector doped to 4.5×10^{16} cm^{-3} with Si, a 500 Å GaInAs etch-stop layer doped to 1×10^{19} cm^{-3}, and a 3000 Å InP sub-collector doped with Si at 3.8×10^{19} cm^{-3}.

Wafers #4450 and #4451 were grown by gas source MBE at Agilent Technologies in Palo Alto CA. The epi-layers are shown in Table 2-4, in which the average measured thicknesses as determined by stylus profilometry for each layer during processing are also listed.

2.4.2 Device Fabrication

All wafers were processed in CSDL using standard triple mesa and wet etching techniques. Although some of the processing details may be different depending on the wafer structure, the device frabrication followed similar sequence [8]:

1. Emitter metal photolithography and metallization;
2. Emitter mesa etching with emitter metal as the mask;
3. Base metal photolithography and deposition for self-aligned devices using emitter metal as the mask, and for non self-aligned devices using photoresist as the mask;
4. Base mesa etching with emitter base junction area protected by photoresist;
5. Collector metal photolithography and deposition using photoresist as the mask (non self-aligned);
6. Isolation mesa photolithography and etching with intrinsic device area protected by photoresist;
7. Photolithography and metal deposition for pads and interconnections with airbridges.

2.4.3 Device Measurements

DC measurements were performed using a semiconductor parameter analyzer HP4156 and a Cascade Microtech probe station. The high-frequency response of devices was characterised through their scattering parameters (S-parameters) which were measured to 40 GHz on the network analyser HP8510B with GGB coaxial cables and GGB Picoprobes connected to the device under test. Detailed RF measurements of f_T and f_{max} can be found in [8]. All measured devices were not passivated, and the measurements were carried out at room temperature.

2.5 DC Simulation Results

2.5.1 Energy Band Alignment and Band Narrowing

In a common emitter configuration, the plot of the base and collector currents as a function of V_{BE} for a specific V_{BC} (usually $V_{BC} = 0$) is called the Gummel characteristic. The Gummel characteristic is widely used to characterize the DC performance of bipolar transistors. As mentioned in Section 2.1, the energy band gap of the GaAsSb base has a great effect on the GaAsSb/InP DHBT DC simulated characteristics. This is shown in Fig. 2-9 where the only free parameter is the GaAsSb base bandgap. The larger base band gap leads to a significant increase in the turn-on voltage of the device, but the impact on the current gain was found to be negligibly small. The effect of the conduction band offset ΔE_C between the InP and GaAsSb is shown in Fig. 2-10. The base current has a small variation at low bias, but the collector current shows no noticeable change, in agreement with the results of [40].

Heavily doped semiconductors feature Band Gap Narrowing (BGN) where the effective band gap shrinks due to strong many-body interactions between electrons, holes, and ionized impurities [82]. For GaAsSb-based DHBTs, BGN is important because GaAsSb can be doped higher than 10^{20} cm^{-3} [83], which is beneficial to RF devices with thin bases to maintain low base sheet resistance. For our devices, BGN in the base significantly affects the device characteristics, as shown in Fig. 2-9. The effective base band gap (E_{gB}) can be determined by comparing the simulated and measured collector current in the common emitter configuration [40]. Fig. 2-11 and Fig. 2-12 show the measured and calculated collector current density for the InP/GaAsSb/InP DHBTs (#4451 and #4450) with two base doping levels. The device structures of #4451 and #4450 are nominally the same except the base doping levels: $N_A = 5\times10^{19}$ cm^{-3} for #4450, and $N_A = 5\times10^{18}$ cm^{-3} for #4451. The two wafers are described in detail in Chapter 4, and the device fabrication and measurements are generally described in Section 3.2. DC simulations for these two structures were performed with various base E_{gB} values. We can assert from Fig. 2-11 and 2-12 that the effective band gap of $GaAs_{0.51}Sb_{0.49}$ is 0.67 eV and 0.72 eV for doping levels of 5×10^{19} cm^{-3} and 5×10^{18} cm^{-3} respectively.

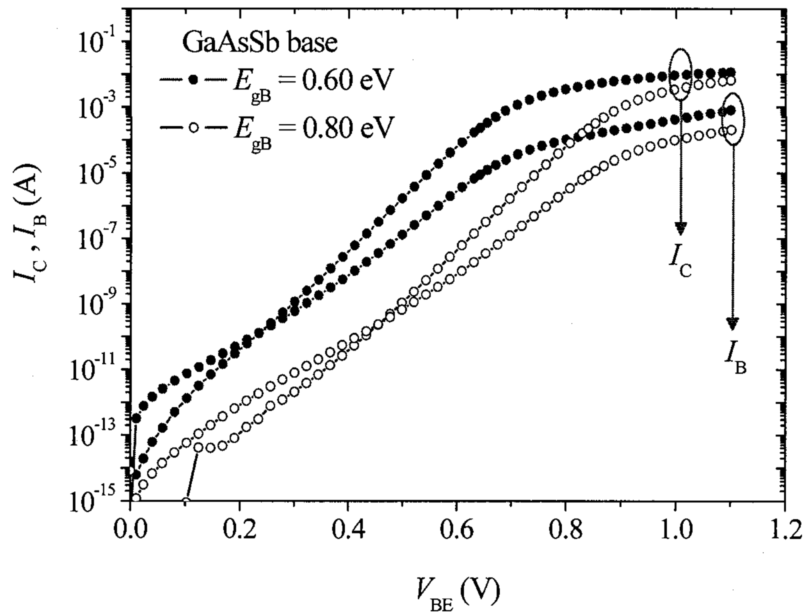


Figure 2-9: Simulated Gummel plots for InP/GaAsSb/InP DHBTs with two base energy band gaps (E_{gB}).

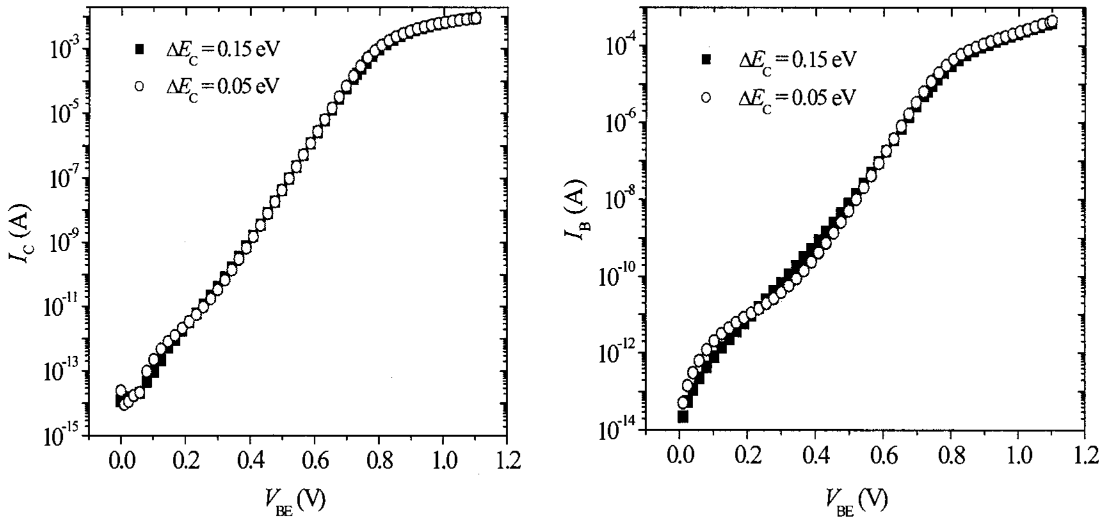


Figure 2-10: Computed Gummel plots (I_C and I_B are separately shown for clarity) for InP/GaAsSb/InP DHBTs with two conduction band offsets (ΔE_C) between GaAsSb and InP. E_g = 0.68 eV in both cases.

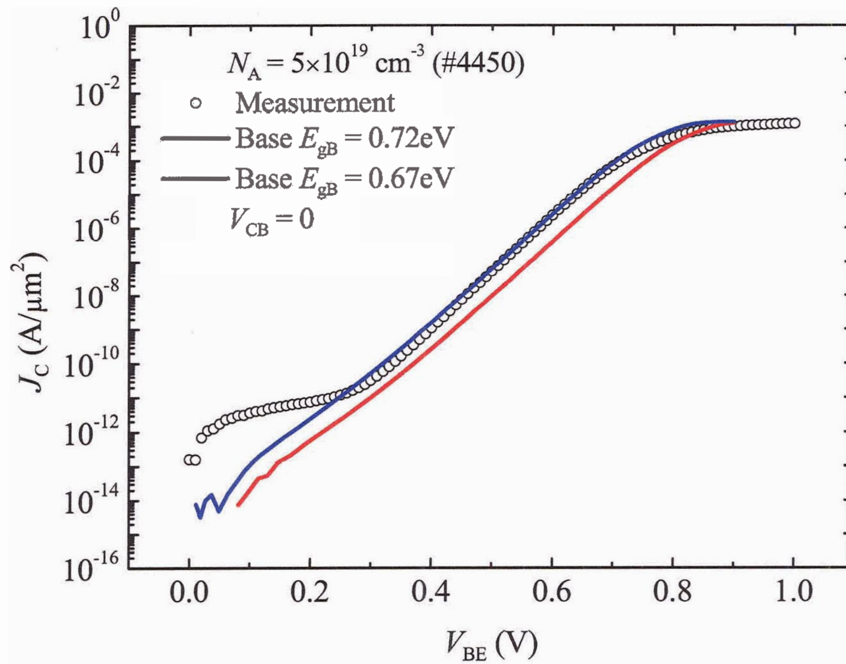


Figure 2-11: Comparison of collector current density between a measured (circles) and simulated InP/GaAsSb/InP device with a heavily doped base (N_A = 5×10^{19} cm^{-3}). The blue line (E_{gB} = 0.67 eV) fits the experimental data.

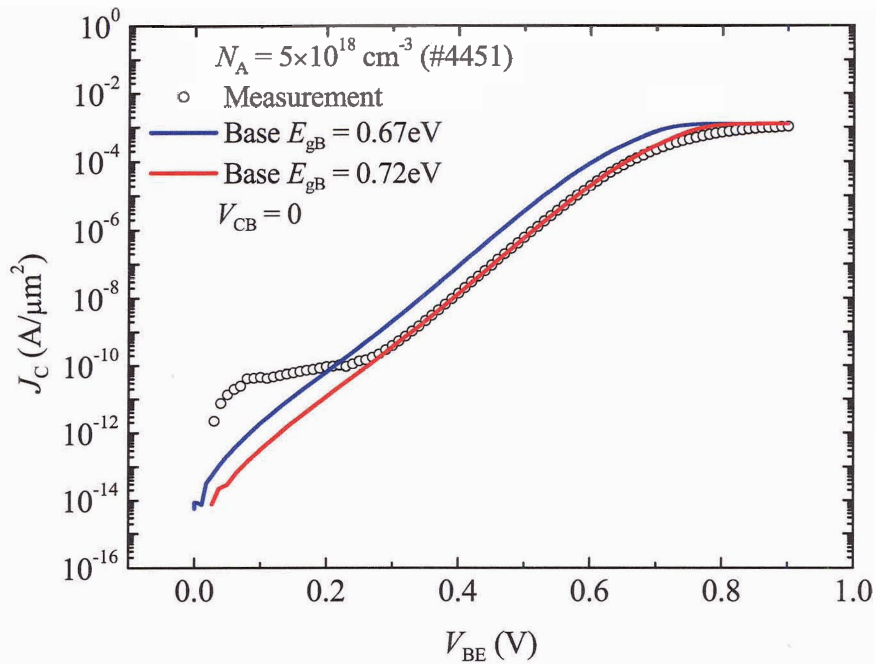


Figure 2-12: Comparison of collector current density between a measured (circles) and simulated InP/GaAsSb/InP device with a lightly doped base (N_A = 5×10^{18} cm^{-3}). The red line (E_{gB} = 0.72 eV) fits the experimental data.

The BGN models incorporated into ISE TCAD v. 7 are primarily applicable to silicon, and an alternate treatment was needed. In our work, we used a model developed by Jain *et al.* [84]. This model has been shown to be applicable to compound semiconductors and the amount the band gap shrinkage in a doped semiconductor with respect to its intrinsic band gap is given as [85]:

$$\Delta E_{\mathrm{g}}^{\mathrm{BGN}} = C_1\left(\frac{N}{10^{18}}\right)^{1/\alpha} + C_2\left(\frac{N}{10^{18}}\right)^{1/2} + C_3\left(\frac{N}{10^{18}}\right)^{1/\beta} + C_4\left(\frac{N}{10^{18}}\right)^{1/2}, \qquad (2\text{-}22)$$

where $C_1 = \dfrac{0.36307 m_{\mathrm{dh}}^{0.25}}{\varepsilon^{1.25}}$, $C_2 = \dfrac{0.0186 m_{\mathrm{de}}}{N_{\mathrm{bp}}\varepsilon^{0.5} m_{\mathrm{dh}}^{1.5}}$, $C_3 = \dfrac{0.2126 A}{\varepsilon \cdot N_{\mathrm{bp}}^{0.33}}$, $C_4 = \dfrac{0.0186}{N_{\mathrm{bp}}(\varepsilon \cdot m_{\mathrm{dh}})^{0.5}}$, and N is the doping density. For our p-type $GaAs_{0.51}Sb_{0.49}$ base, $\alpha = 4$, $\beta = 3$, $N_{\mathrm{bp}} = 2$, $A = 2$ [85], the relative dielectric constant is $\varepsilon = 14.2$, the effective electron mass $m_{\mathrm{de}} = 0.045$, and the effective hole mass $m_{\mathrm{dh}} = 0.46$ (in unit of m_0) (see Table 2-3). According to (2-22), we have:

$$\Delta E_{\mathrm{gB}}^{\mathrm{BGN}}(N = 5\times10^{19}) - \Delta E_{\mathrm{gB}}^{\mathrm{BGN}}(N = 5\times10^{18}) \approx 0.0899 - 0.0404 \approx 0.05\,\mathrm{eV},$$

which is in good agreement with what we extracted in our simulation: $E_{\mathrm{gB}}(N = 5\times10^{18}) - E_{\mathrm{gB}}(N = 5\times10^{19}) = 0.72 - 0.67 = 0.05$ eV.

It is also important to note that according to [84], most of the BGN occurs in the valence band and secondly, as previously stated, that a small change in ΔE_{C} does not affect J_{C} versus V_{BE}. Therefore, the conduction band offset ΔE_{C} was assumed to be fixed and independent of doping for the simulation.

2.5.2 Surface States

Surface states and recombination are the extremely important aspects of modelling the DC characteristics of sub-micron devices in which the periphery surface recombination currents are significant. Fig. 2-13 shows the comparison of two simulated

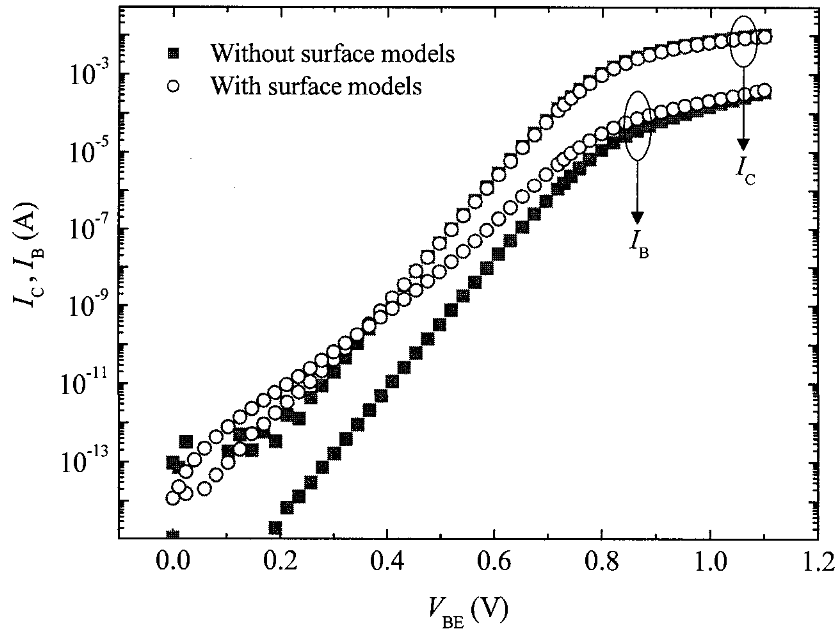


Figure 2-13: Computed Gummel plots for InP/GaAsSb/InP DHBTs with and without the inclusion of surface recombination effects. The emitter size is 0.5×12 μm^2.

Gummel plots with and without the inclusion of surface state models. If the emitter sidewall and the extrinsic base surface are considered to be perfect (i.e., like the bulk material), the base current will be very small. Note that surface states have no effect on the collector current when $V_{BE} > 0.35$ V. Also, note that without the addition of surface states the base current is always smaller than the collector current. However, the addition of surface states and recombination significantly increases the base current, and at $V_{BE} <$ 0.35 V, it even surpasses the collector current. Another way of looking at this is that the base current non-ideality factor increases due to the effect of surface states. In this particular case, surface states cause the base current non-ideality factor to increase from 1.03 to 1.7 at $V_{BE} = 0.3$ V, and to 1.3 at $V_{BE} = 0.6$ V. This finding indicates that the non-ideality factor of the surface recombination current is closer to 2 rather than to 1, which is similar to the observation for InP/InGaAs HBTs [86]. As mentioned above, in the presence of surface state models, the base and collector currents cross (Fig. 2-13) for InP/GaAsSb/InP DHBTs. This behaviour has often been observed experimentally, and the effects of surface recombination are discussed in detail in Chapter 3.

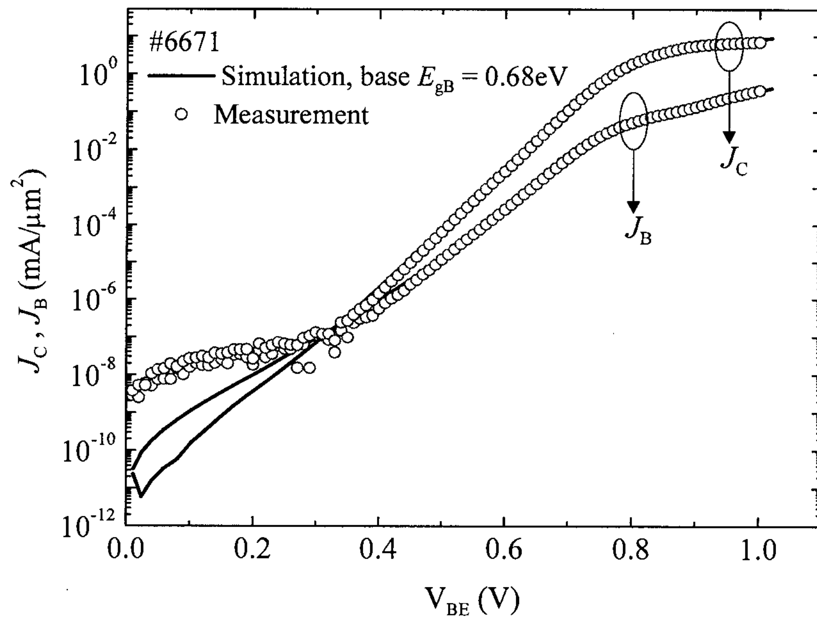


Figure 2-14:* *Comparison of measured and simulated Gummel plots. Surface recombination effects are included in the simulation.

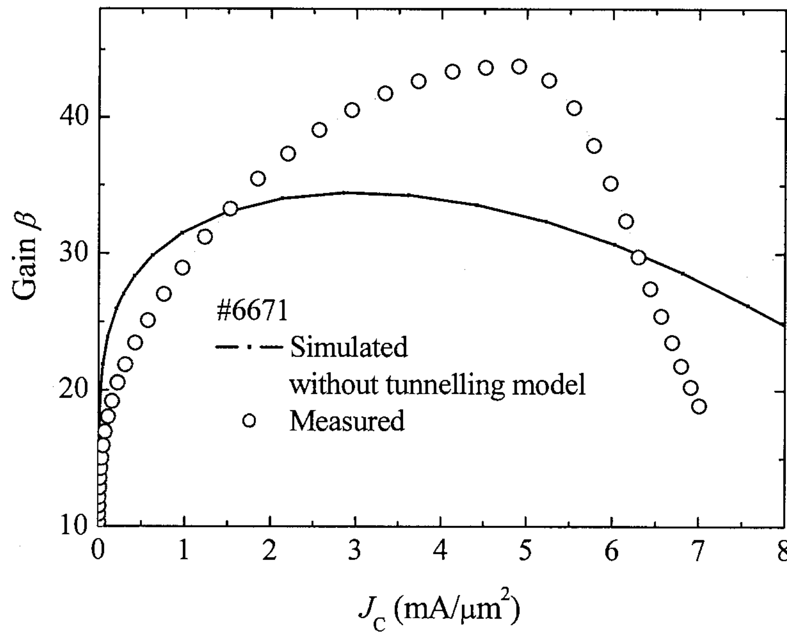


Figure 2-15:* *Comparison of high-current gain plots for measured and simulated devices. The measured peak gain and the Kirk current density are higher than the simulated ones. (The simulation was performed without tunnelling model at the BC junction).

2.5.3 Comparison to Measurement

Fig. 2-14 compares the simulated and experimental Gummel plots for a device fabricated on the layers as described in Table 2-2. The area of the emitter metal was (0.6×6 μm^2) and the area of the emitter was (0.4×5.5 μm^2). For the simulation, the parameters listed in Table 2-3 were used. For wafer #6671, the base was doped at 4×10^{19} cm^{-3}, a band gap of 0.68 eV was used (which agrees with the BGN result obtained in last Section). The most important aspect of Fig. 2-14 is the excellent agreement between the experimental measurements and the simulated results in most of the low current regime. This agreement supports the surface state and recombination model used in our simulations.

Despite the close agreement between the simulated and experimental Gummel plots, there are still some discrepancies. While not obvious in Fig. 2-14, the difference is seen to be significant in the high-current gain plot (Fig. 2-15). The experimentally measured peak gain and peak current (Kirk current) are higher than those determined through simulation. The reason for this discrepancy is that tunnelling through the BC junction at high current could not be modelled properly in that simulation. As described in Section 2.1, incorporating BC junction tunnelling model often resulted in failure of the simulation especially in the case of thin base. As we will discuss in Chapter 4, the Kirk effect in type-II DHBTs exhibits a non-classical mechanism, where the conduction band at the base side of the BC junction curls up at high current levels, resulting in the formation of an induced electron barrier. The formation of this barrier makes the inclusion of tunnelling model very important as the tunnelling facilitates electron transport across BC junction. Tunnelling at the BC junction would increase the current gain and delay the Kirk effect.

2.6 RF Simulation Results

Two most important figures of merit used in the evaluation of DHBT frequency response are f_T and f_{max}. f_T corresponds to an emitter-collector transit time τ_{EC}, given as

$\tau_{EC} = \dfrac{1}{2\pi \cdot f_T}$ [87]. We divide the emitter-collector transit time into subcomponents based on device physics and small-signal delay times:

$$\tau_{EC} = \tau_B + \tau_C + (R_E + R_C)\cdot C_{jC} + \frac{nkT}{qI_C}\cdot(C_{jE} + C_{jC}). \qquad (2\text{-}23)$$

Here τ_B is the electron propagation time through the base and is given as $\tau_B = \dfrac{X_B^2}{\gamma \cdot D_{nB}} + \dfrac{X_B}{v_{BC}}$ [73] where X_B is the base thickness, D_{nB} is the electron diffusivity in the base, v_{BC} is the electron exit velocity at the BC junction, and γ is a factor which depends on the magnitude of the quasi-electric field in the base. τ_C denotes the collector signal delay time, given as $\tau_C = \dfrac{X_C}{2v_C}$ where X_C is the collector thickness (this assumes that the collector is fully depleted) and v_C is a constant velocity in which electrons propagate through the collector. C_{jE} and C_{jC} denote the junction capacitances for the BE and BC junctions respectively, and R_E and R_C are the emitter and collector resistances respectively [81].

According to Vaidyanathan and Pulfrey [88], f_{max} can be calculated as $f_{max} = \sqrt{\dfrac{f_T}{8\pi(RC)_{eff}}}$, where $(RC)_{eff}$ is a general time constant and is approximated by

$$(RC)_{eff} \approx (R_B C_{jC})_{eff} + (2\pi \cdot f_T R_C C_{jC})\cdot\left(R_E + \frac{1}{g_m}\right)\cdot C_{jC}. \qquad (2\text{-}24)$$

Here g_m is the transconductance given by $g_m = \dfrac{nk_B T}{qI_C}$. The $(R_B C_{jC})_{eff}$ term is an effective base-collector time constant which takes into account the distributed network of capacitors and resistors in the base and collector regions.

The above analytical formulae for f_T and f_{max} indicate that the junction capacitances and access resistances are the primary factors limiting device performance.

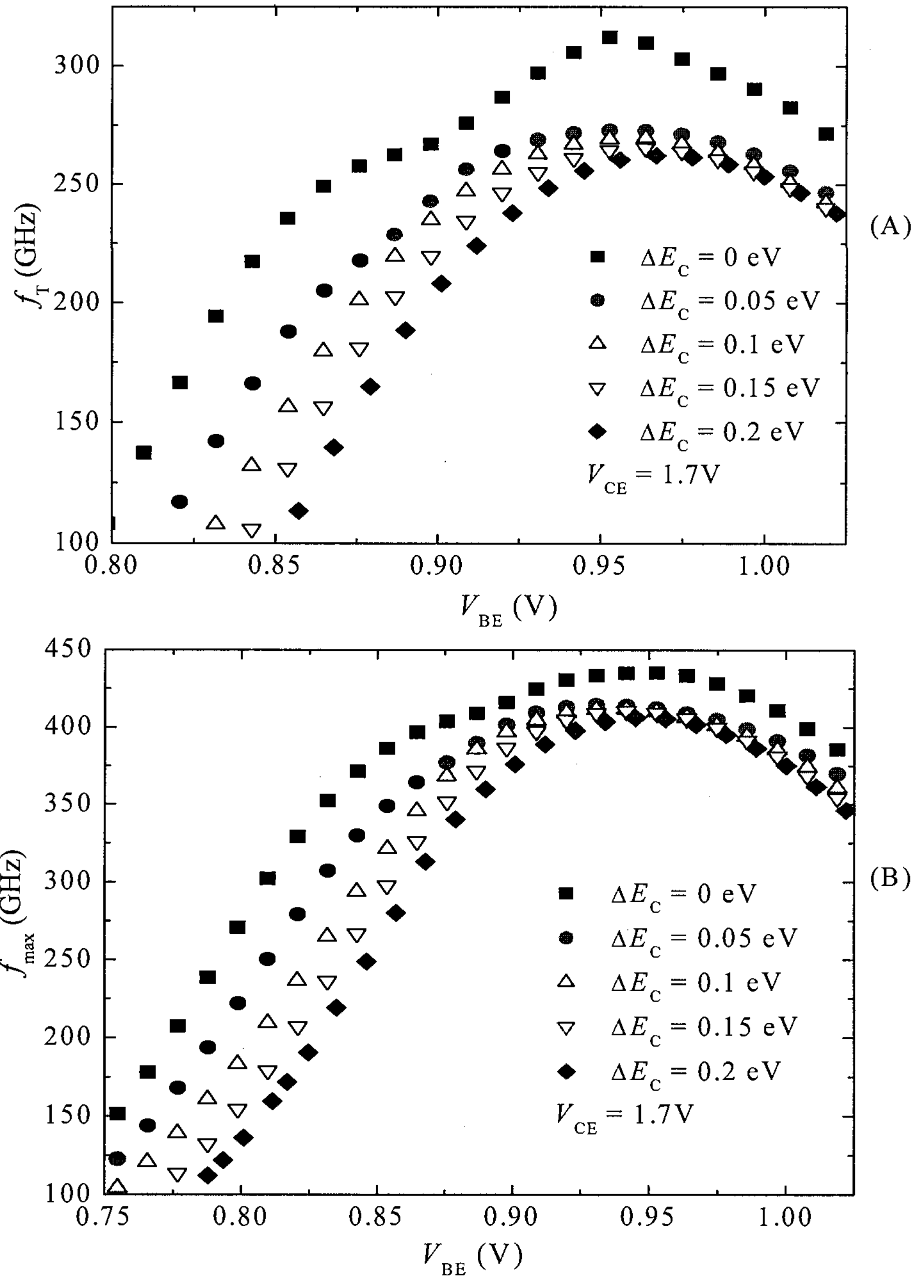


Figure 2-16: Simulated f_T (A) and f_{max} (B) vs. base emitter bias for type-II InP/GaAsSb/InP DHBTs with different conduction band (ΔE_C) offsets. E_{gB} = 0.68 eV for the GaAsSb bases.

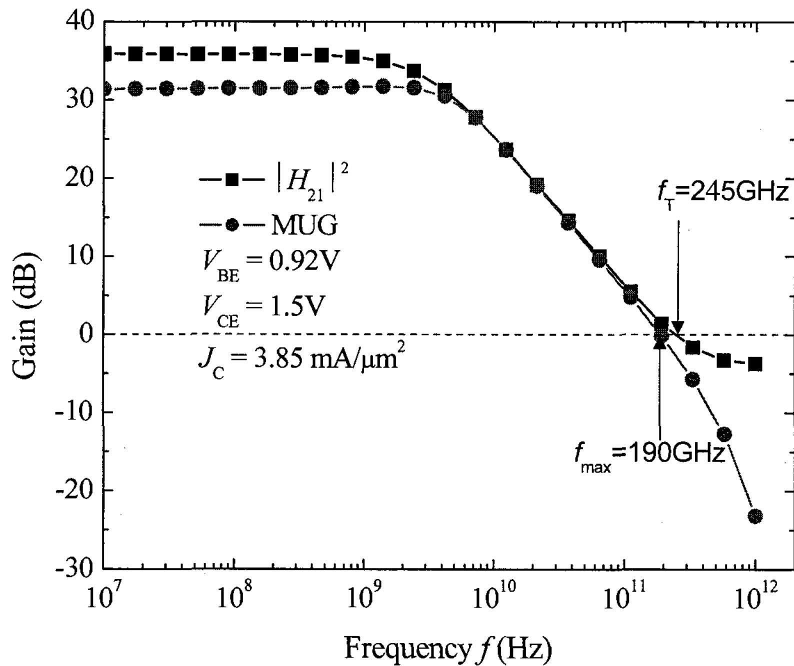


Figure 2-17: Simulated small signal current gain (dB) and Mason's unilateral gain (dB) vs. frequency. Device structure is the same as #6671, and the emitter area is 0.5×11 μm²^2***.***

For this reason, vertically and laterally scaling device dimensions is an important approach to improve the high-frequency characteristics. However, aggressive scaling is not without limitations, and trade-offs always exist. For example, decreasing the device area to decrease junction capacitances may result in a larger emitter resistance. Decreasing the base thickness reduces the base transit time but also results in higher base resistance, necessitating higher p-type doping levels to maintain a reasonable base resistance.

Besides the device dimensions, physical parameters such as the electron mobility in the base and the conduction band offset (ΔE_C) also impact the frequency performance. For example, decreasing ΔE_C improves the frequency response as shown in Fig. 2-16. The reason for this improvement is that the smaller ΔE_C results in a larger built-in voltage and in turn, lower junction capacitances, leading to increased f_T and f_{max} as shown in equations (2-29) and (2-30).

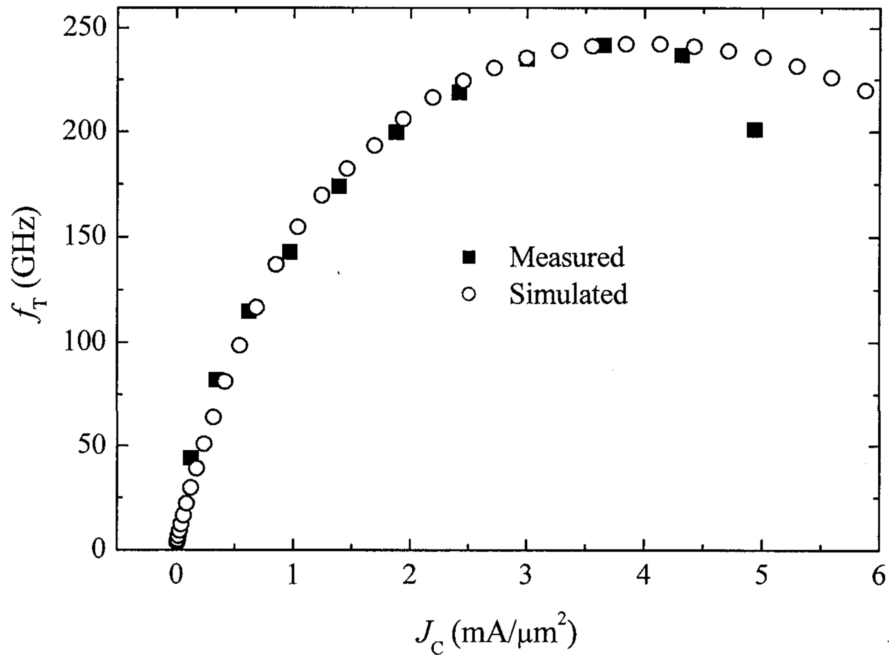


Figure 2-18: Computed and measured cut-off frequency vs. collector current density for InP/GaAsSb/InP DHBTs. The device structure is the same as #6671, the emitter area is 0.5×11 μm^2, and V_{CE} = 1.5 V.

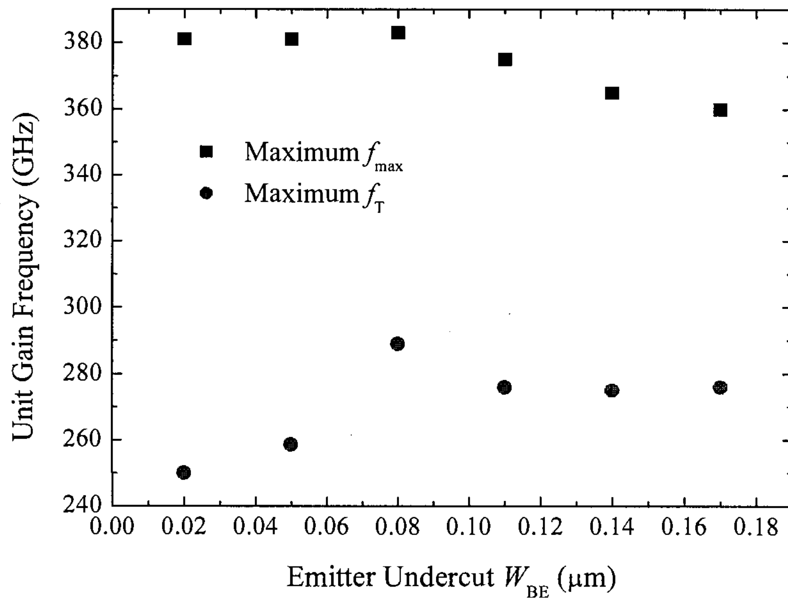


Figure 2-19: Simulated maximum f_T and f_{max} for InP/GaAsSb/InP DHBTs with different emitter undercuts. The emitter metal width W_{BE} + W_E / 2 = 0.3 μm and the base metal width W_B = 0.35 μm.

Table 2-5: Typical Dimensions of simulated devices based on #4720.

Layers	Vertical Thickness (μm)	Lateral Width (μm)
Emitter metal	—	0.25
$In_{0.53}Ga_{0.47}As$ cap	0.1	0.17
InP cap	0.07	0.17
InP emitter	0.05	0.17
InP spacer	0.01	0.17
$GaAs_{0.59}Sb_{0.41}$ base	0.025	0.6
Base metal	—	0.35
InP collector	0.2	0.6
$In_{0.53}Ga_{0.47}As$ sub-collector	0.05	0.6
Collector metal	—	0.6

Fig. 2-17 shows the simulated small signal current gain $|H_{21}|$ and Mason's unilateral gain MUG as a function of frequency, up to 1000 GHz (device dimensions are shown as Table 2-2). f_T and f_{max} are determined directly from the 0 dB intercept of the curves. Fig. 2-18 shows a comparison of the simulated and measured cut-off frequencies as a function of collector current density. The simulated result is in good agreement with our measured result reported in [15]. However, it seems that at high current, after the onset of the Kirk effect, the measured f_T drops more quickly than the simulations would suggest. This difference may be explained by the fact that we did not take the device self-heating into account, or that we did not employ the tunnelling model in the RF simulations of Fig. 2-18.

The device structure in Fig. 2-17 is not optimized for high f_{max} performance because the base doping level is low, leading to a high base sheet resistance and high base contact resistance (see (2-24)). Another important factor affecting f_{max} is the base-collector capacitance: decreasing the lateral dimensions results in smaller C_{jC} because of the reduced base-collector junction area. One subtle effect of lateral scaling is the emitter undercut, the spacing between the base metal and the emitter mesa sidewall (W_{BE}). Fig. 2-19 shows the maximum f_T and f_{max} simulated with various amounts of emitter undercuts.

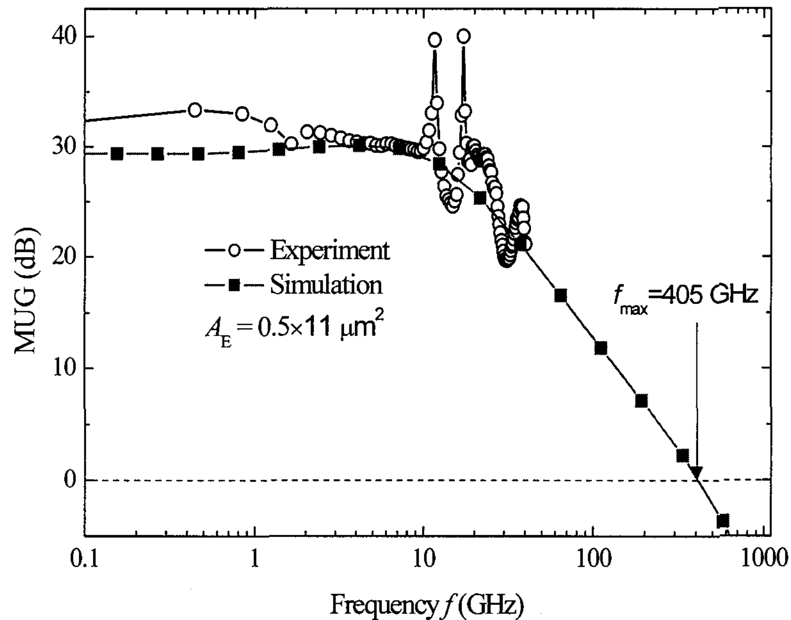


Figure 2-20: Measured and simulated Mason's Unilateral Gain (MUG) vs. frequency up to 40 GHz (measured) and 1000 GHz (simulated). Device biases are: V_{BE} = 0.92 V, V_{CE} = 1.7 V. I_C is ~ 13 mA and 14 mA for experimental and simulated results respectively.

It seems that the optimum emitter undercut is approximately 0.08 μm. Fabrication of such a small undercut is possible by carefully adjusting the wet etching conditions, and/or by a combination of wet and dry etching methods. Our minimum achievable undercut by wet etching is approximately 0.06 μm [89].

In order to achieve higher f_{max}, we fabricated sample #4720. The epilayer structure is described in Section 2.4.1 and the device dimensions are shown in Table 2-5. The base was very heavily doped (9×10^{19} cm^{-3}) resulting in a sheet resistance as low as 1000 Ω/□. The emitter metal width was scaled down to nearly a half micron, and a very aggressive wet etch was used for the base mesa. Typically, the lateral size of the base metal was about 1.25 μm, and if an aggressive collector etch was used, the undercut would often be large enough as to cause the base metal to bend, or even collapse. However, it is desirable to have as wide an undercut as possible (to reduce the base-collector capacitance). We have found that for base metal thicknesses of 0.15−0.2 μm,

bending does not even appear for undercuts up to 0.7 μm, and only becomes noticeable for undercuts over 0.8 μm [89]. It is important to note that the GaAsSb in structure #4720 is under tensile strain as the Sb composition is 0.41 rather than the lattice-matched value 0.49. According to [90], the conduction band offset of $GaAs_{0.59}Sb_{0.41}$ with respect to InP would decrease by around 35%, and the band gap would increase by around 8% compared to the lattice-matched $GaAs_{0.51}Sb_{0.49}$ values. In addition, the base band narrowing in #4720 is much stronger due to heavier base doping than in #6671. Therefore, we assumed that the base band gap of #4720 is approximately the same as that of #6671, but the conduction band offset ΔE_C decreases from 0.15 eV for #6671 to 0.05 eV for #4720.

Fig. 2-20 shows the comparison of the measured and simulated MUG plots. Note that the measured data was so noisy that we may not accurately determine f_{max} by the standard –20dB/decade extrapolation method. By fitting the simulated result, however, we find that this device can reach a high f_{max} of more than 400 GHz.

2.7 Conclusions

The ISE TCAD v. 7 simulation package has been studied and a complete simulation procedure, using various tools on the GENESISe platform, has been set up. The general simulation methodology used in this work is applicable for not only HBTs but also other semiconductor devices such as HEMTs and even GaAsSb/InP photodiodes.

All the principal physical models have been introduced and implemented in our simulations. Combined with analytical formulations, the simulation results have provided some insights into the performance issues important to GaAsSb/InP DHBTs, e.g., the impacts of conduction band offset and emitter undercuts on f_T and f_{max}. $GaAs_{0.51}Sb_{0.49}$ band gap narrowing has been investigated by means of the simulation. A measured result suggestive of a high f_{max} has been confirmed by the simulation. Good agreement between DC and RF simulated and experimentally measured results indicate that the physical models and parameters used in our simulations are appropriate and meaningful: the present simulation environment is thus expected to bear fruitful results toward the optimization of GaAsSb based DHBTs.

Chapter 3:

Surface Recombination in GaAsSb-based DHBTs

3.1 Overview

In this chapter, we study the effects of surface recombination (SR) at the emitter periphery in GaAsSb/InP DHBTs. Surface recombination is responsible for the so-called emitter size effect (ESE) which manifests itself in HBTs by a reduction in current gain as the emitter contact size is reduced. The ESE phenomenon is clearly undesirable because it results in a non-scaling behaviour of device characteristics as a function of emitter area. The ESE is an important issue for sub-micron devices because of the importance of scaling down feature sizes to achieve high-speed performances.

In a triple-mesa HBT structure (see Fig. 2-4), the base current consists of a bulk[4] recombination current and a surface recombination current, if we reasonably omit the hole injection current from the base to the emitter [81]. The base surface recombination current $I_{B,Surf}$ occurs at or near to the boundary between the emitter sidewall and the extrinsic base, and therefore $I_{B,Surf}$ is found to be proportional to the emitter *perimeter*. In contrast, the base bulk recombination current, including all possible recombination mechanisms in the bulk regions such as the base-emitter (BE) interface and space-charge region, is proportional to the emitter *area*. The total base current I_B is thus written as

$$I_B = A_E \cdot J_{B,Bulk} + P_E \cdot K_{B,Surf} , \qquad (3\text{-}1)$$

[4] Here the term bulk is used in the sense of "*not involving external surfaces*."

where A_E and P_E are the emitter area and perimeter respectively, $J_{B,Bulk}$ represents a total bulk current density that is proportional to the emitter area, and $K_{B,Surf}$ is a total *linear* periphery current density. Using the current gain definition $\beta = \frac{I_C}{I_B}$, (3-1) can be reformulated as

$$\frac{J_C}{\beta} = J_{B,Bulk} + K_{B,Surf} \frac{P_E}{A_E}. \qquad (3\text{-}2)$$

For a rectangular emitter of width W_E and length L_E, the perimeter is $P_E = 2(L_E + W_E)$, and the area is $A_E = L_E \cdot W_E$. Assuming the device and material are uniform, $J_{B,Bulk}$ and $K_{B,Surf}$ are independent of L_E and W_E, and then, (3-2) shows that at a constant collector current density, current gain decreases with shrinking emitter area. This behaviour is usually referred to in the literature as the emitter size effect (ESE). Equation (3-2) also shows that $\frac{J_C}{\beta}$ should vary linearly with $\frac{P_E}{A_E}$, and the slope $K_{B,Surf}$ can be used to experimentally characterize the periphery surface recombination current in a given process when devices with varying periphery-to-area ratios are compared.

In this chapter, we first experimentally characterize the SR current for GaAsSb/InP DHBTs. In the third Section, we perform 2D simulations to model SR and ESE, and compare the simulated results with the measured data. Through the modelling, we theoretically analyze the SR of GaAsSb/InP DHBTs. In the fourth Section, we propose some solutions to diminish the SR current and ESEs for GaAsSb-based DHBTs. The last Section is a summary.

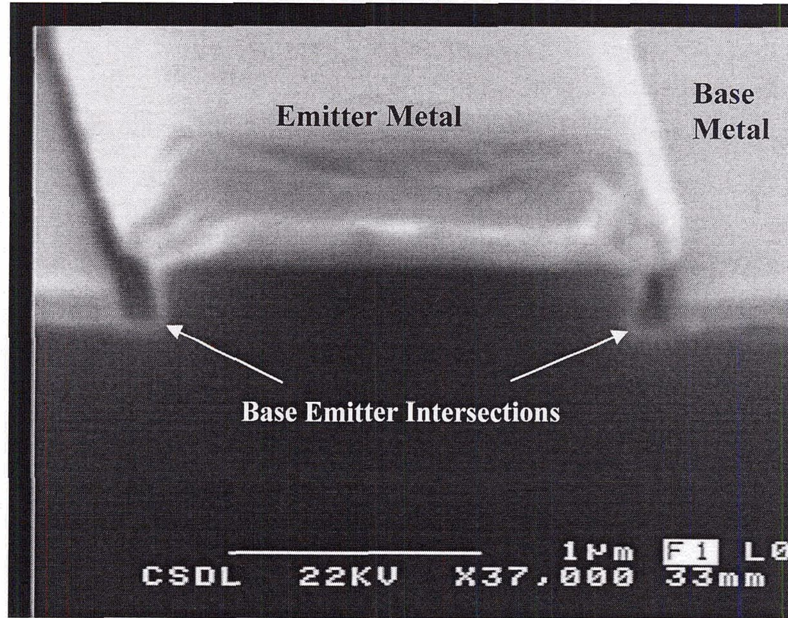


Figure 3-1: End-view scanning electron micrograph (SEM) of the cross section of a fabricated device with deposited metal. The emitter finger is along [110] direction.

3.2 Experimental Characterization

We measured devices #6671 and #4720 in this study. It is noted that the stripe of the emitter finger is along the [110] direction so that the emitter mesa profile presents a negative slope in order to permit self-aligned base/emitter contacts with a reduced short-circuit risk. Fig. 3-1 shows the emitter undercut typically formed in the process. If W_E and L_E represent the matrixes of all different nominal emitter width and length respectively, and W_{BE} is the spacing between the base metal and emitter mesa edge, all available nominal emitter metal sizes are $W_E \times L_E = (0.5, 0.75, 1, 2) \times (6, 12, 24)$ μm^2 for self aligned devices, $W_E \times L_E = (0.5, 1) \times 12$ μm^2 for non self-aligned devices with $W_{BE} =$ 1.5 μm, and $W_E \times L_E = (10\times20, 20\times30, 40\times40, 80\times80)$ μm^2 for non-self-aligned devices with $W_{BE} = 3.5$ μm.

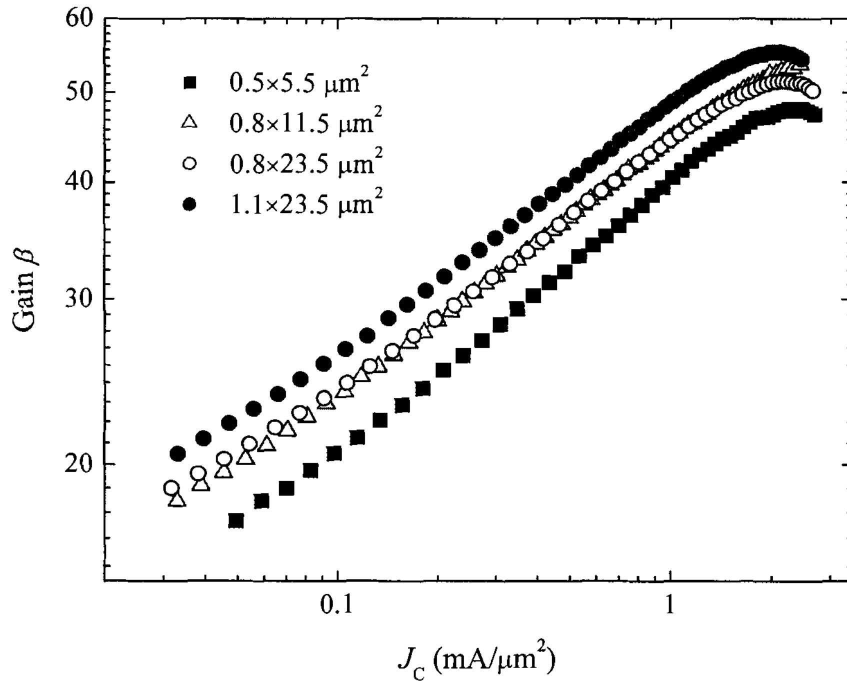


Figure 3-2: ***Typical emitter size effect for self-aligned devices of #6671.*** $V_{CB} = 0$ ***in all measurements.***

3.2.1 Measurement Results

The emitter size was determined by the emitter metal dimensions as measured in our scanning electron microscope (SEM), and by subtracting the emitter undercut that is ~ 0.1 μm, as mentioned in Chapter 2. A typical manifestation of the emitter size effect is shown in Fig. 3-2. The size effect seems to be more significant at low current level since the surface recombination current is relatively more important at low injection levels.

An interesting finding for #6671 is that there is nearly no difference between self-aligned (SA) and non self-aligned (NSA) devices in terms of the size effect. Fig. 3-3 shows that for the same emitter area, the current gain as a function of the collector current density is the same for SA and NSA devices. To further verify this phenomena, we measured both SA and NSA devices and extracted the base periphery current density $K_{B,Surf}$ according to (3-2). As shown in Fig. 3-4, $K_{B,Surf}$, which is the slope in equation

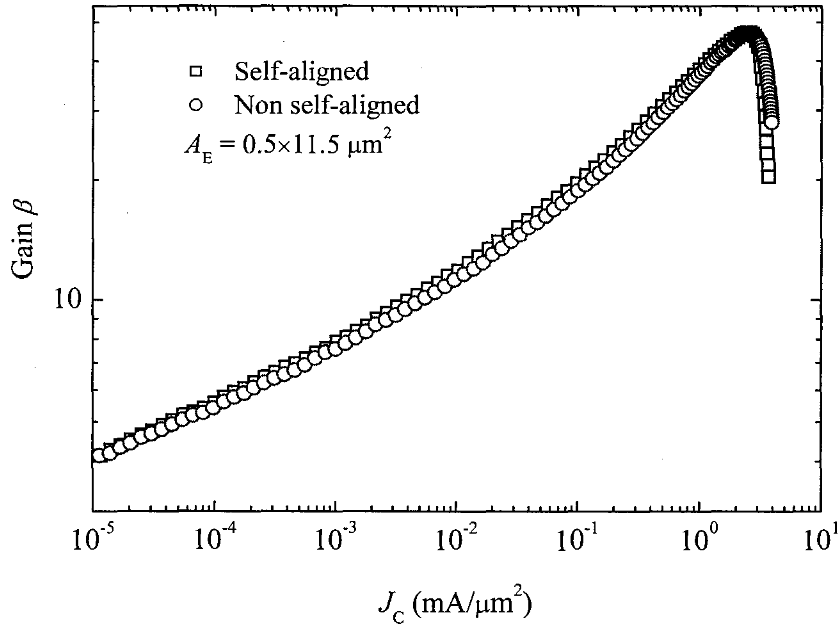


Figure 3-3: Measured current gain vs. collector current density for self-aligned and non self-aligned devices of #6671.

(3-2), is the same for SA and NSA devices. Table 3-1 gives the measured $K_{B,Surf}$ of SA and NSA devices at different current levels. It should be noted that the comparison was only made at relatively low current levels because the measurement of large area (e.g., 40×40 μm^2) NSA devices at high current levels can give rise to considerable uncertainties due to the self-heating and emitter current crowding effects (non-uniform emitter current density). The result indicates that the base metal has a negligible influence on the surface recombination current.

Table 3-1: Measured $K_{B,Surf}$ for SA and NSA devices of #6671

J_C (mA/μm^2)		10^{-4}	10^{-3}	10^{-2}
$K_{B,Surf}$ (μA/μm)	SA	1.75×10^{-2}	3.48×10^{-2}	1.12×10^{-1}
	NSA	1.79×10^{-2}	3.76×10^{-2}	1.06×10^{-1}

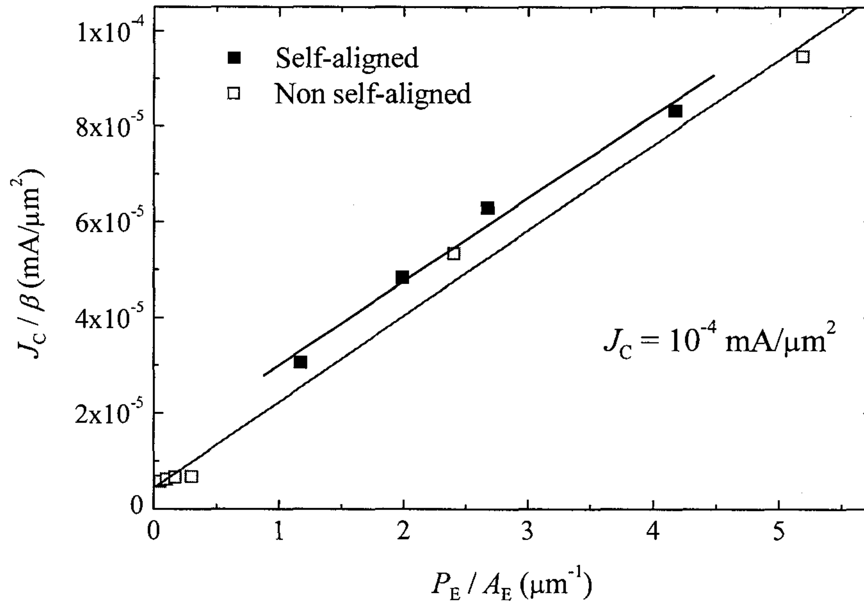


Figure 3-4: ***Measured size effects according to (3-2) for self-aligned and non self-aligned devices. The slope of the fitting lines is $K_{B,Surf}$ in (3-2). SA device areas are (0.5, 0.8, 1.1, 2)×11.5 μm^2 and NSA device areas are (0.45, 0.9)×11, 10×20, 20×30, 40×40 and 80×80 μm^2.***

Fig. 3-5 shows the measured size effects for SA devices at various collector current densities, and Fig. 3-6 shows the $K_{B,Surf}$ as a function of the collector current density extracted from Fig. 3-5. $K_{B,Surf}$ increases slowly at lower J_C but more rapidly at higher J_C. We found that for J_C between 0.1 and 1 mA/μm^2, our measured $K_{B,Surf}$ coincides with the values reported for non-passivated SA InP/InGaAs HBTs [23]. In other words, the InP/InGaAs and GaAsSb/InP HBTs show nearly identical surface recombination current characteristics despite fundamental differences in electron injection mechanisms from the emitter to the base (hot injection for InP/GaInAs *vs.* thermal injection in InP/GaAsSb emitters). This strongly suggests that both types of HBTs share a common mechanism for the surface recombination current [25].

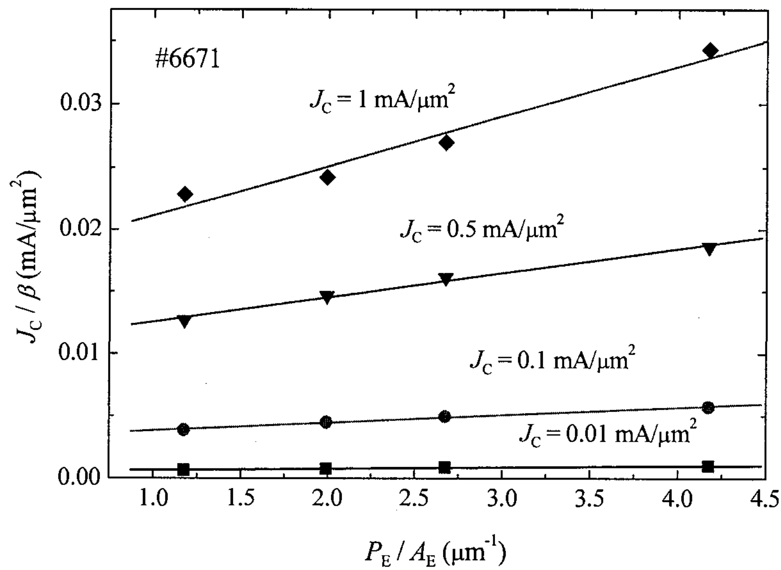


Figure 3-5: Measured emitter size effect for Self-aligned devices of #6671 according to (3-2) at different collector current densities. The SA device areas are (0.5, 0.8, 1.1, 2)×11.5 μm^2.

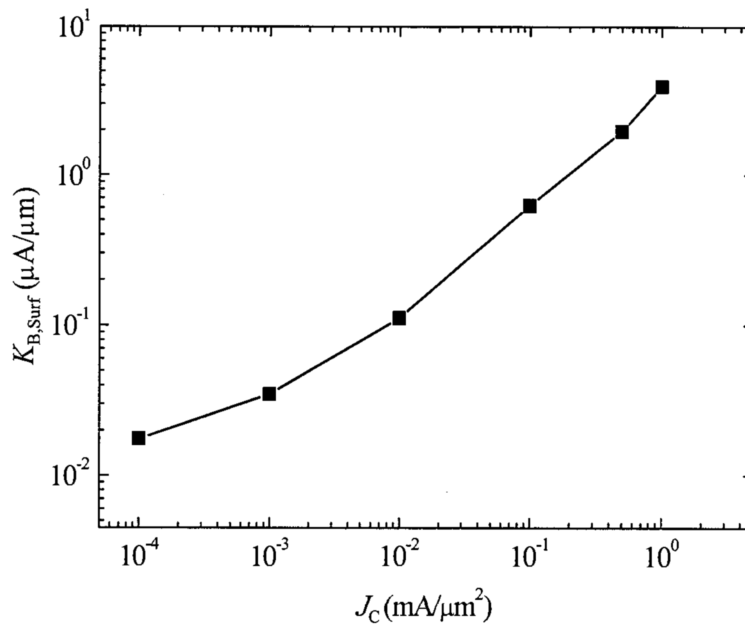


Figure 3-6: Measured periphery surface recombination current density as a function of collector current density for self-aligned devices of #6671.

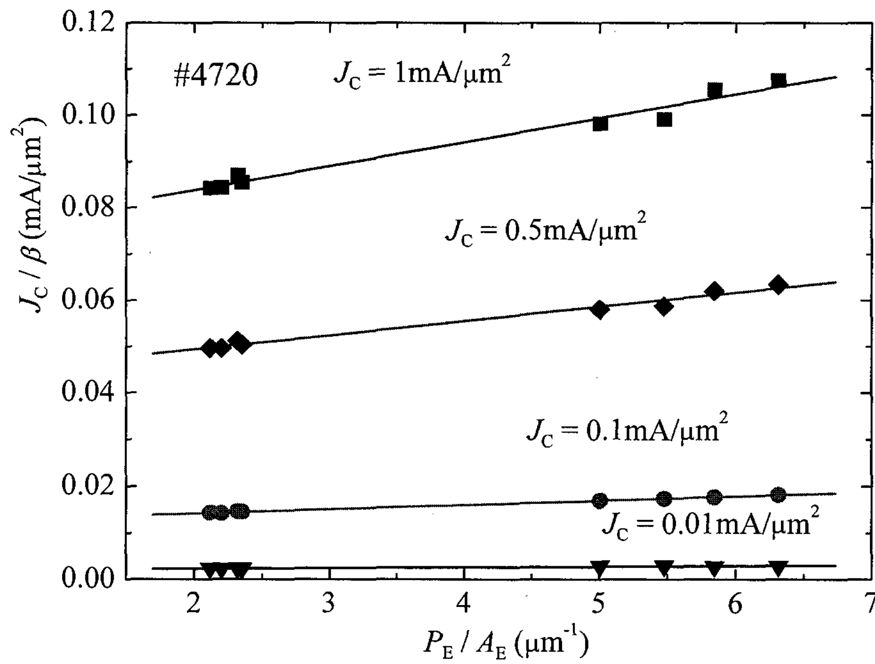


Figure 3-7: ***Measured emitter size effect for self-aligned devices of #4720 at different collector current densities. The SA device areas are (0.98, 0.94)×23.5, (0.93, 0.91)×11.5, (0.39, 0.43)×5.3 and (0.32, 0.35)×11.2 μm²***.

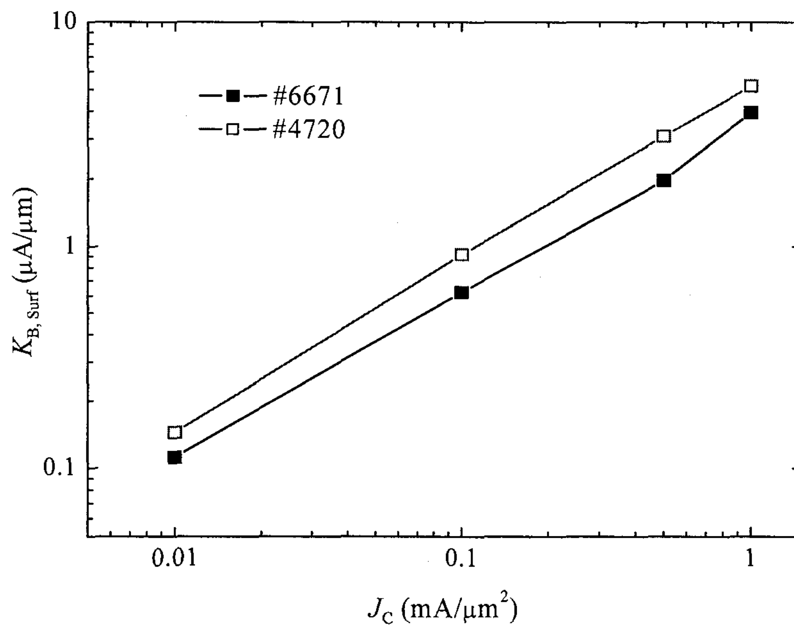


Figure 3-8: ***Comparison of measured $K_{B,Surf}$ as a function of J_C in #6671 and #4720.***

Similarly, we measured the size effect for SA devices of #4720 as shown in Fig. 3-7. Fig. 3-8 shows the extracted $K_{B,Surf}$ as a function of J_C and for comparison, the data of #6671 is also displayed. The surface recombination current in #4720 is in average 35% higher than that in #6671. It is noted that #4720 features heavy base doping (9×10^{19} cm^{-3} in #4720, and 4×10^{19} cm^{-3} in #6671), and a tensile strained base layer with smaller Sb composition (x = 0.41 in #4720 and x = 0.49 in #6671). We return to these differences in the next Section.

3.3 Simulation and Theoretical Analyses

The surface recombination current depends on the recombination rate (or surface recombination velocity) and the electron concentration at the base surface. A mechanism for the supply of electrons to the extrinsic base surface is therefore required for recombination to take place. By introducing the surface Fermi level pinning effects into the 2D simulation, one easily finds that electrons are directly injected from the emitter to the extrinsic base surface through the so-called "*saddle point*" in the conduction band potential [26]. The saddle point forms at the edge of the emitter sidewall and extrinsic base as illustrated by the numerically computed band diagram shown in Fig. 3-10. From a modelling point of view, the surface state conditions are thus fundamental to the simulation of periphery surface recombination currents in HBTs.

3.3.1 Surface Fermi Level Pinning for Emitter and Base

The surface Fermi level positions are assumed to be as follows: 0.43 eV below the conduction band for n-type InP [78], 0.22 eV above the valence band for p-type $GaAs_{0.51}Sb_{0.49}$ [91], 0.5 eV above the valence band for p-type $In_{0.53}Ga_{0.47}As$ [92] and 0.69–0.99 eV below the conduction band for n-type $In_{0.52}Al_{0.48}As$ [93]. For simplicity, we used a single surface trap state, with acceptor-type states for the n-type emitter, and with donor-type states for the p-type base [58]. To strongly pin the Fermi level at a specific energy, the surface state density should be high enough. Fig. 3-9 is an example of the calculated valence band bending near the surface of a p-type GaAsSb layer with different surface state densities. We can find that $N_{Dt} = 5\times10^{13}$ cm^{-2} is enough to pin the Fermi level at position of 0.22 eV above the valence band edge and the surface charge

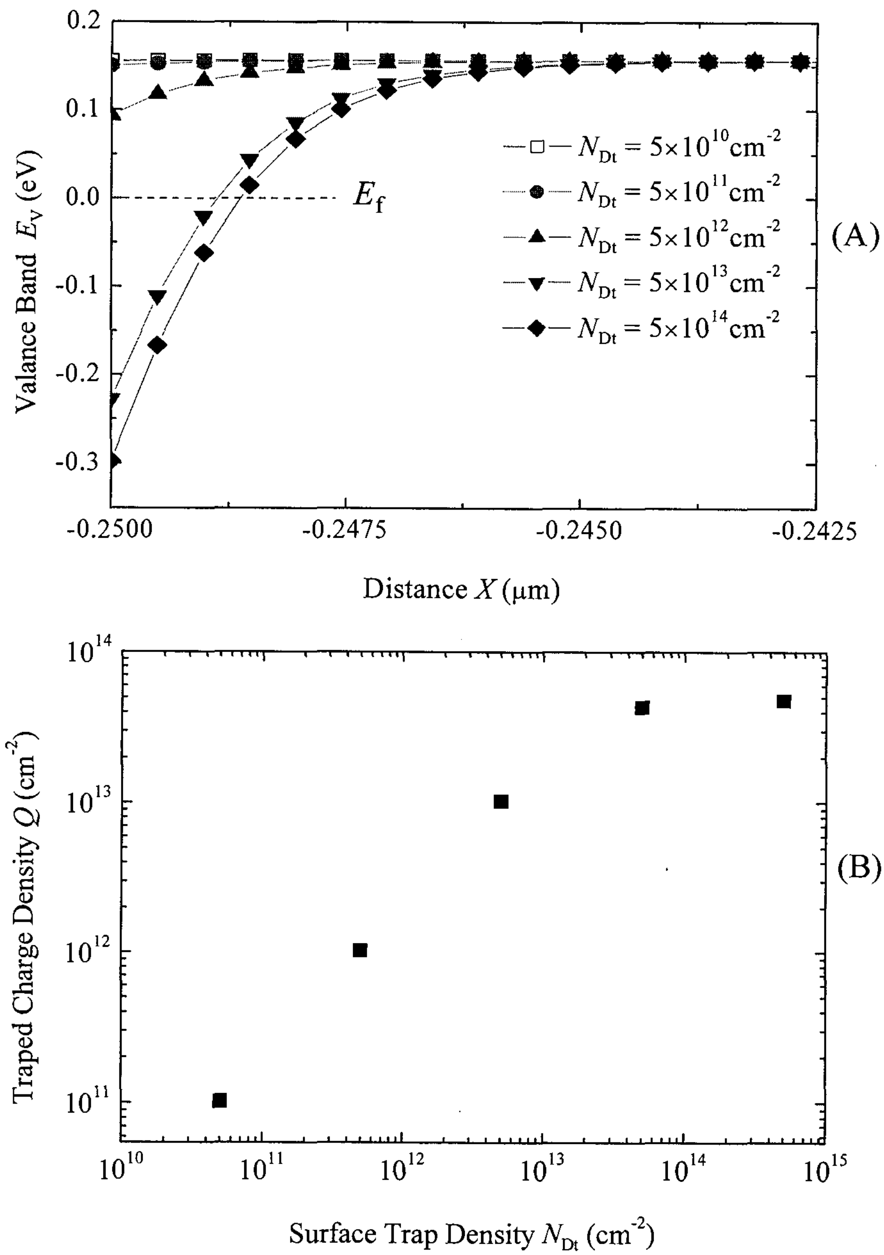


Figure 3-9: ***Calculated valence band bending near the surface ($X = -0.25\mu m$) (A) and the corresponding surface charge densities (B) of p-type GaAsSb at thermal equilibrium with various surface state densities: $N_{Dt} = 5\times10^{10} - 5\times10^{14}$ cm^{-2}. Bulk p-doping level is 4×10^{19} cm^{-3}.***

does not change much when the surface state density is greater than 5×10^{13} cm^{-2}.

It should be noted that the surface orientation with respect to crystallographic planes might influence the surface states due to different surface structures, and as a result, the surface charges and surface recombination may vary with the surface orientation [94, 95]. Due to the unavailability of experimental data, our simulations assume that for a particular emitter or base, the surface state conditions for all different crystal plane orientations are the same. Our assumption is experimentally justified since the InP (100) and (110) crystal planes have shown similar surface state properties [76, 77].

3.3.2 Simulation Results for InP/GaAsSb/InP DHBTs

3.3.2.1 Direct Injection Mechanism

Fig. 3-10 shows the 3D plots of the equilibrium conduction band edge profile at an InP/GaAsSb emitter-base junction. For clarity, the band diagrams for two device regions (e.g., a region including the emitter and intrinsic base, and a region including the intrinsic and extrinsic base), are plotted on different scales as shown in Fig. 3-10A and B, respectively. In the emitter area away from the BE junction, e.g., at $Y \sim 0.20$ μm, the upward conduction band edge near the emitter sidewall due to surface depletion prevents electrons from reaching toward the emitter sidewall to recombine. This upward bending, however, disappears near the BE junction, and instead, the InP emitter conduction band edge turns downward and toward the intersection of the emitter mesa sidewall and the extrinsic base surface, as shown in Fig. 3-10A. This is the "saddle point" potential which physically arises because the continuity of electric field (density) and the band discontinuity between InP and GaAsSb must be enforced at the intersection between the InP mesa and the GaAsSb exposed surface. Accordingly, electrons are driven to the intersection of the emitter mesa and the base surface. In the base area near the extrinsic base surface, the conduction band edge bends downward due to the surface Fermi level pinning, as shown in Fig. 3-10B, and electrons tend to be confined on the base surface until they recombine. Indeed, the 3D conduction band edge forms an electron injection channel from the emitter to the extrinsic base surface through the saddle point [26]

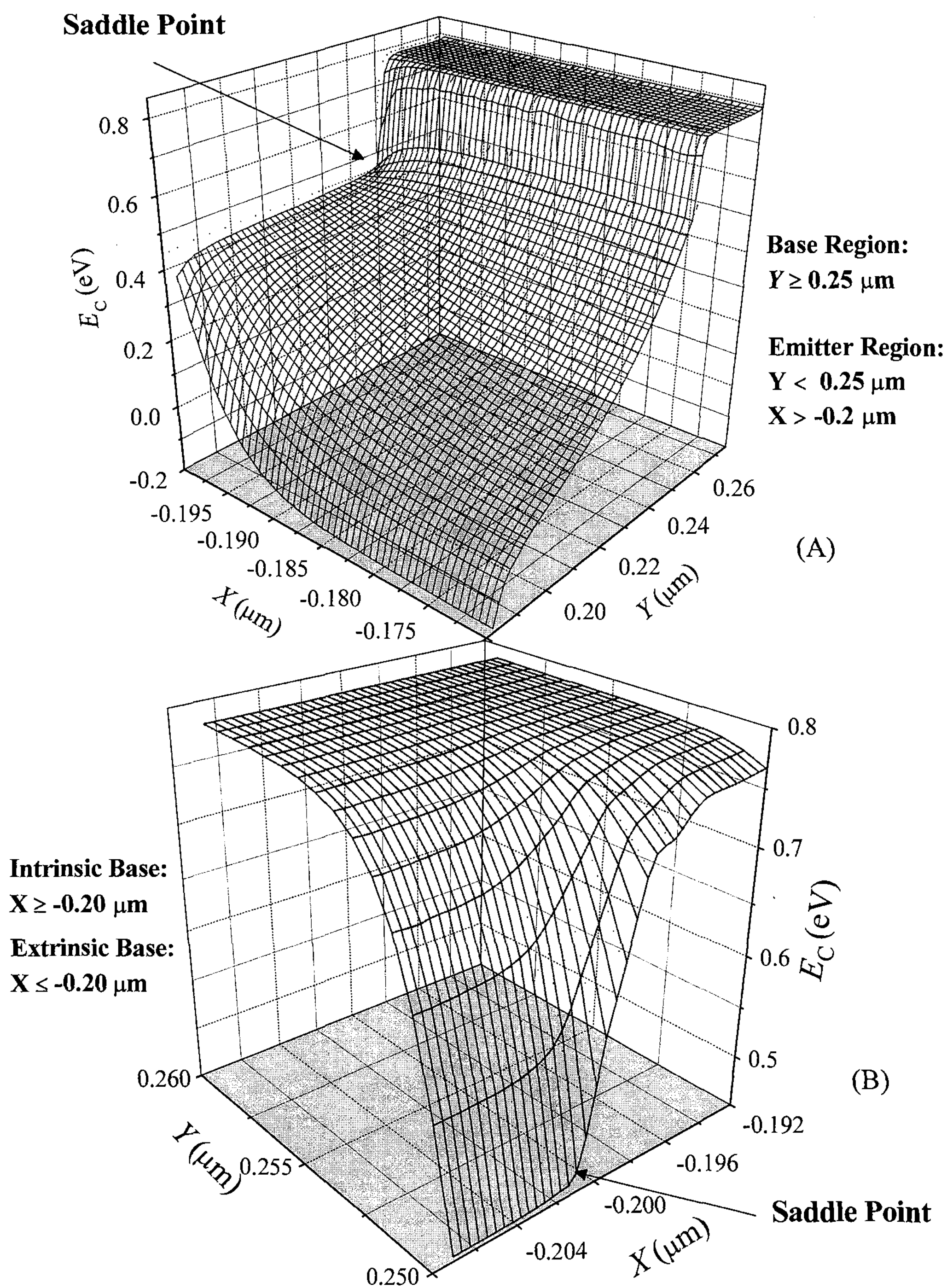


Figure 3-10: Simulated conduction band diagram around the GaAsSb/InP emitter-base intersection in thermal equilibrium. (A): intrinsic emitter and base area; (B): extrinsic and intrinsic base area.

which is located at the intersection of the emitter sidewall and the base. Fig. 3-11A and B show the 3D conduction band edges with an applied forward BE bias. We still can see the electron injection path through the saddle point.

Fig. 3-12 and Fig. 3-13 present 2D contour maps of the electron concentration (n) and SRH recombination rate (R_{SRH}) respectively at the same bias. The highlighted contour lines indicate that a lateral electron projection along the extrinsic base surface takes place as the arrow shows in Fig. 3-12. We can also see that within a small distance (~ 100Å) from the intersection toward the intrinsic base (i.e., to the right and the center of the emitter mesa), n and R_{SRH} are very low near the BE interface, while in the opposite direction, within about the same distance from the emitter sidewall edge toward the extrinsic base, n and R_{SRH} are quite high at the base surface. This scenario indicates that the recombined electrons at the extrinsic base surface are supplied from the emitter by direct surface injection at the intersection between the emitter sidewall and the extrinsic base surface.

3.3.2.2 Emitter Size Effect and $K_{B,Surf}$

Usually, a relation such as (3-2) is used to describe the emitter size effects. However, in the case of our 2D simulation, there is only one side of the emitter finger (L_E) which is subject to the surface recombination (see Fig. 2-7). Therefore, equation (3-2) must be modified in the following manner to enable comparisons between simulations and measured results:

$$J_C / \beta = J_{B,Bulk} + K_{B,Surf} \frac{1}{W_E} . \qquad (3\text{-}3)$$

Fig. 3-14 shows the simulated size effect according to (3-3) with four different emitter widths. It is found that linear correlation values of all the line fits used to evaluate $K_{B,Surf}$ are all equal to 1.000. Therefore, the simulation of only two different emitter widths is sufficient to numerically determine $K_{B,Surf}$ for HBTs in our simulation environment.

Fig. 3-15 shows the numerically evaluated $K_{B,Surf}$ as a function of J_C with various state densities (N_{Dt}) and electron capture cross sections (σ_n) at the extrinsic base surface.

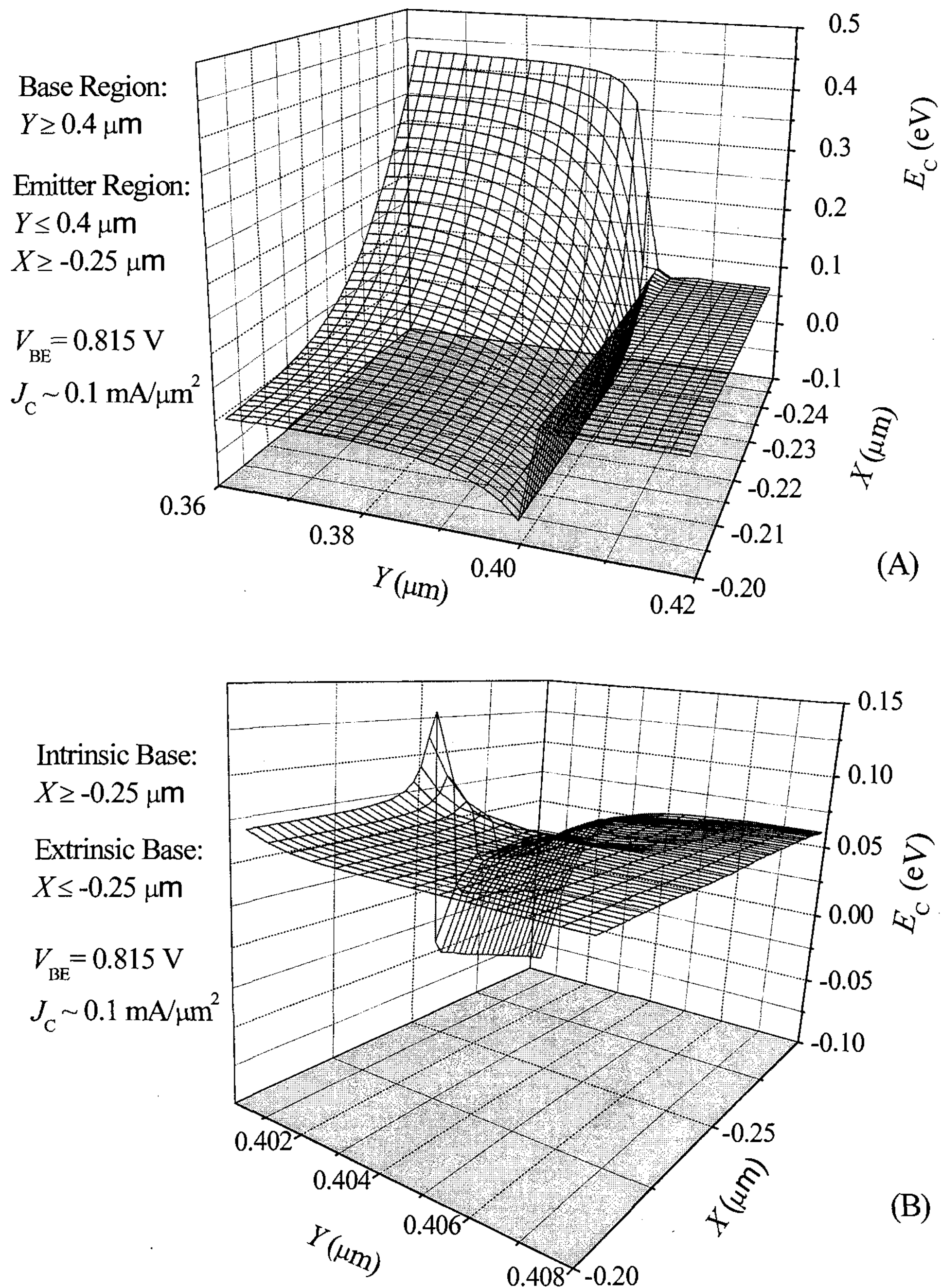


Figure 3-11: Simulated conduction band diagram around the GaAsSb/InP emitter-base intersection at bias of V_{BE} = 0.815 V and J_C ~ 0.1 mA/μm². (A): intrinsic emitter and base area; (B): extrinsic and intrinsic base area. The emitter-base intersection is at Y = 0.4 μm and X = -0.25 μm.

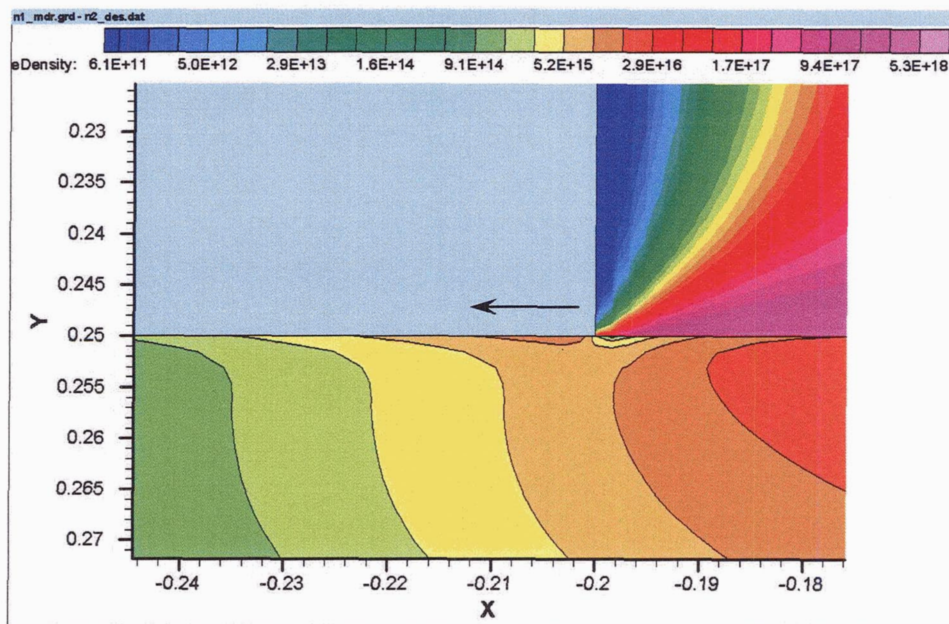


Figure 3-12: ***Simulated 2D electron density around emitter base edge at $V_{BE} = 0.785$ V and $J_C \sim 0.66$ mA/µm^2. The unit of density in the legend is cm^{-3}. In the base area, contour lines are highlighted.***

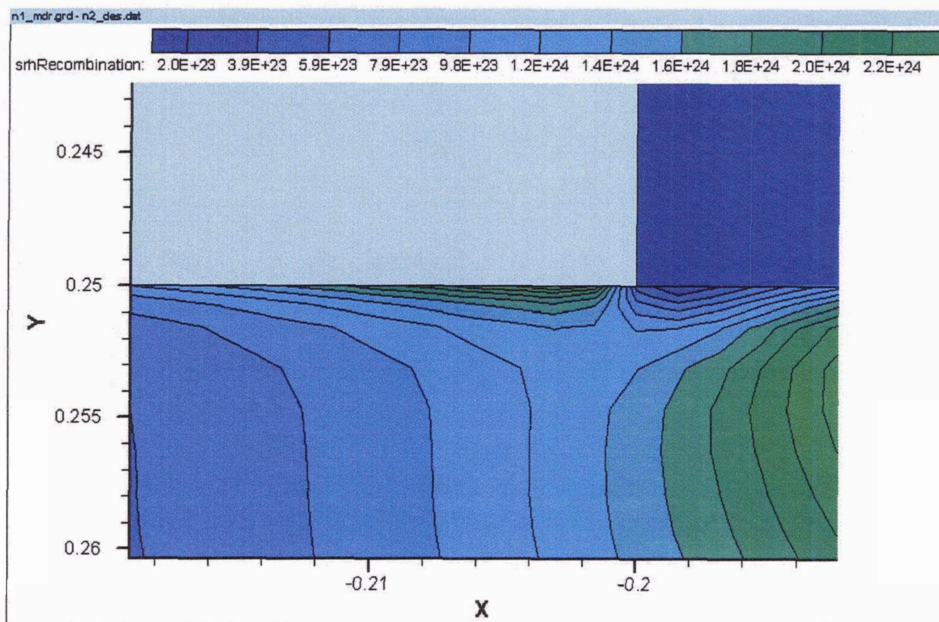


Figure 3-13: ***Simulated 2D SRH recombination rate around emitter base edge at $V_{BE} = 0.785$ V and $J_C \sim 0.66$ mA/µm^2. The unit of recombination rate in the legend is cm^{-3}/s. In the base area, contour lines are highlighted.***

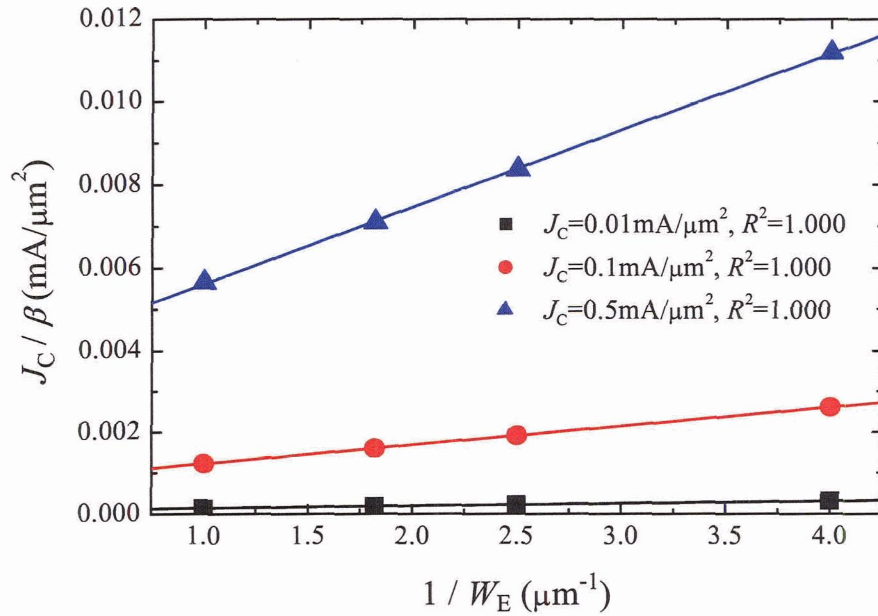
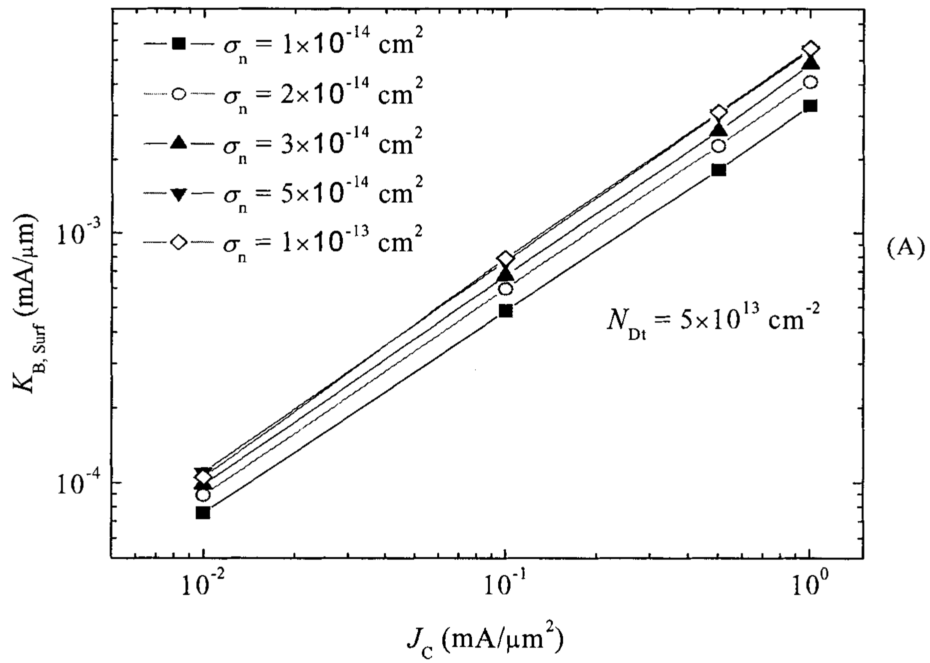


Figure 3-14: ***Simulated size effect of GaAsSb/InP DHBTs at three different collector current densities according to the equation (3-3). The emitter sizes are W_E = 0.25, 0.4, 0.55 and 1 μm, and L_E = 11.5 μm. The linearity of each fit line (at each collector current density) is nearly perfect.***

The two parameters (N_{Dt}, σ_n) determine the base surface recombination velocity. It is noted that σ_n has a higher influence on $K_{B,Surf}$ at high injection levels, and that $K_{B,Surf}$ does not change significantly when $\sigma_n > 5\times10^{-14}$ cm^2. Therefore, the base surface recombination current is electron injection level limited if the surface recombination velocity is high, and otherwise is surface recombination velocity limited. N_{Dt} has greater impact on the surface recombination current than σ_n, because it affects not only the surface recombination rate but also the energy band bending near the base surface (see Fig. 3-9).

Fig. 3-16 shows a comparison of the calculated and measured $K_{B,Surf}$ vs. J_C for both GaAsSb/InP DHBTs and InP/InGaAs SHBTs. The epilayers and experimental data for InP/InGaAs SHBTs is from [23]. In the simulation for InP/InGaAs SHBTs, it is assumed that the surface state density is the same as that in GaAsSb, but the surface Fermi level is ~ 0.5 eV above the valence band edge. It is found that at high current levels



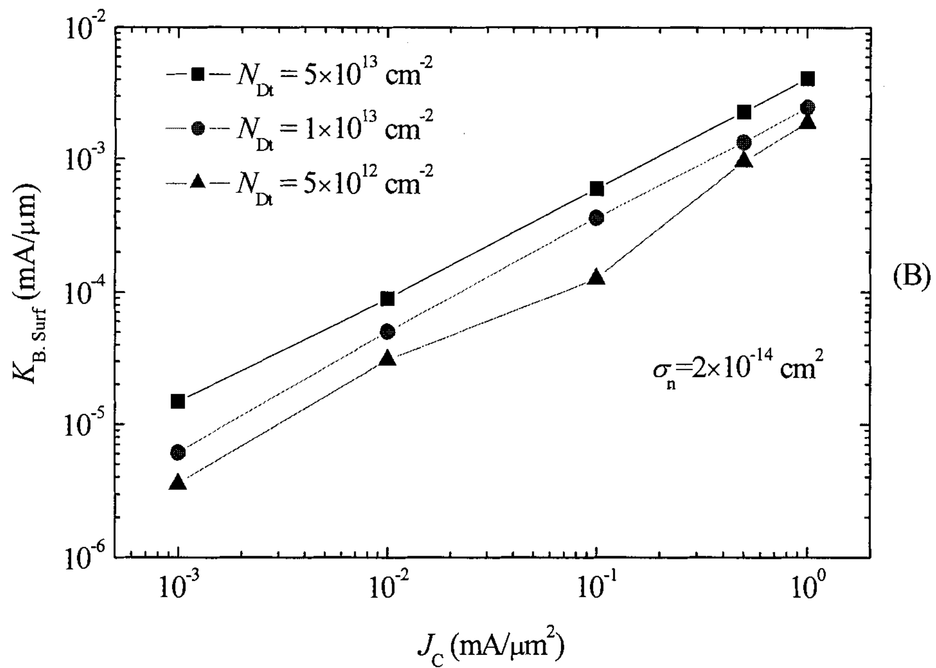


Figure 3-15: Simulated $K_{B,Surf}$ vs. J_C for different electron capture cross sections (A) and for different state densities (B) at the base extrinsic surface.

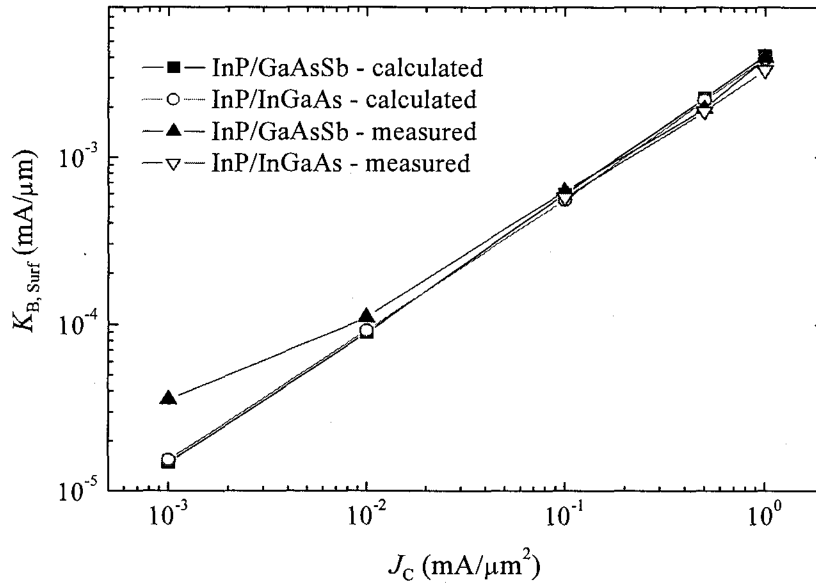


Figure 3-16: Comparisons of simulated and measured periphery base current density $K_{B,Surf}$ for GaAsSb/InP DHBTs and InP/InGaAs SHBTs. The experimental data for InP/InGaAs SHBTs is only available at $J_C \geq 0.1$ mA/μm² [23].

(0.01 to 1 mA/μm^2) the measured and simulated results show a good agreement, but at lower collector current densities, the calculated values are relatively lower than measured ones. In other words, the calculated $K_{B,Surf}$ vs. J_C exhibits an almost linear relation, but the measured results do not obey the same trend at lower J_C. This is probably because the extrinsic leakage currents were not taken into account [96] in the simulations. In Fig. 3-16, the capture cross section in InGaAs ($\sigma_n \sim 6\times10^{-15}$ cm^2) is smaller than that in GaAsSb ($\sigma_n \sim 2\times10^{-14}$ cm^2), which could suggest that the surface recombination velocity of InGaAs is smaller than that of GaAsSb (surface state density N_{Dt} is the same). However, it should be noted that the tunnelling model, which is important to the type-I InP/InGaAs abrupt BE junction, was not employed in the simulation. Therefore, we cannot reliably comment on surface recombination velocity differences between the two material systems at this time.

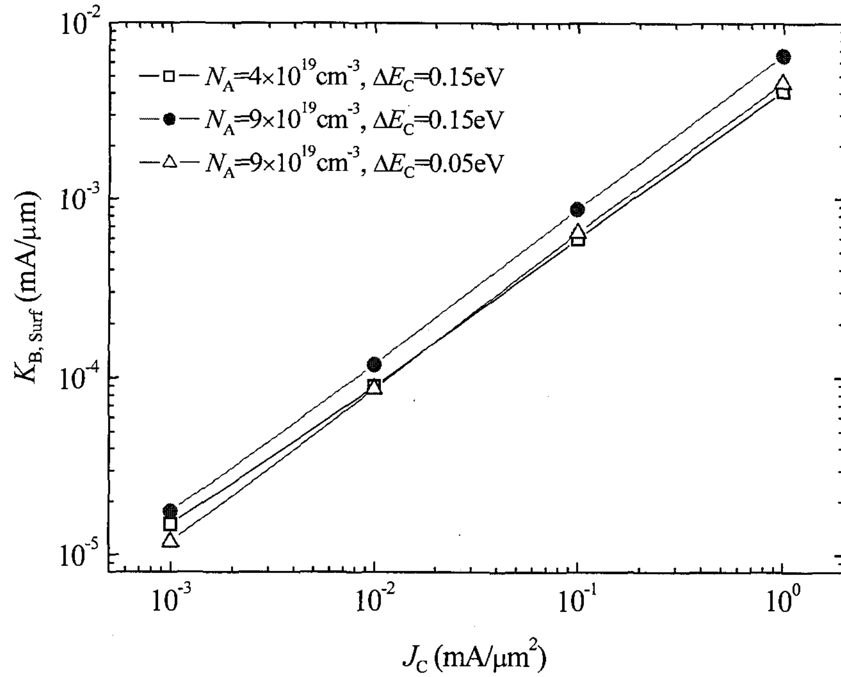


Figure 3-17: Comparisons of calculated $K_{B,Surf}$ between structure #6671 (squares) and #4720 (triangles) assuming all surface state conditions of both structures are the same.

3.3.2.3 Wafer #4720

The differences between the structure #6671 and #4720 are not only the base doping level (N_A) but also the BE conduction band offset (ΔE_C) as discussed in Chapter 1. Fig. 3-17 shows the simulated $K_{B,Surf}$ as a function of J_C based on the structures of #6671 and #4720. In the simulation, we assumed that the surface state conditions are identical for samples #6671 and #4720. As shown in Fig. 3-17, if only N_A increases from 4 to 9×10^{19} cm^{-3} and ΔE_C fixed (0.15 eV), $K_{B,Surf}$ generally increases because higher N_A results in more band bending at the base surface and enhances the electron injection channel. However, if N_A increases from 4 to 9×10^{19} cm^{-3} and ΔE_C decreases from 0.15 eV (#6671) to 0.05 eV (#4720), $K_{B,Surf}$ does not change much and even decreases at low current level. Apparently, decreasing ΔE_C can reduce electron injection to the extrinsic base surface. This is what one would expect from consideration of the band bending and

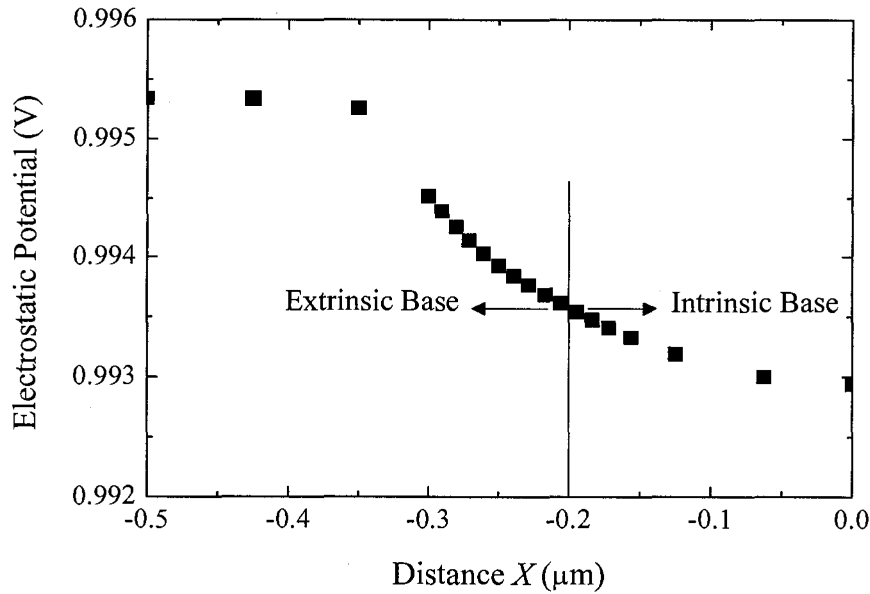


***Figure 3-18:** Simulated lateral electrostatic potential in the base at a base current of 0.278 mA and V_{BE} = V_{CE} =1 V. The base thickness is 250 Å, doping level is 4×10^{19} cm^{-3}. X = 0 is the emitter centre.*

its effects on the strength of the saddle-point potential. However, our measurement demonstrated that $K_{B,Surf}$ for #4720 is higher than that of #6671 as shown in Fig. 3-8.

The question of the different surface recombination characteristics between #4720 and #6671 remains. The solution may reside with the fact that one sample was grown at SFU with a certain set of precursors (#4720, using TBAs and TBP sources) while the other was produced at Nortel (#6671, using AsH_3 and PH_3 sources). It would then be plausible to find somewhat different surface state properties for each sample. As shown above, this would be sufficient to lead to different surface injection characteristics.

3.4 Some Issues Pertinent to the Periphery Current

3.4.1 Emitter Crowding Effect

In principle, base current will give rise to a lateral potential drop due to the finite base resistance. In the intrinsic base area, this potential drop results in a lateral V_{BE} variation under the emitter, assuming the potential is uniform at the emitter side of the BE

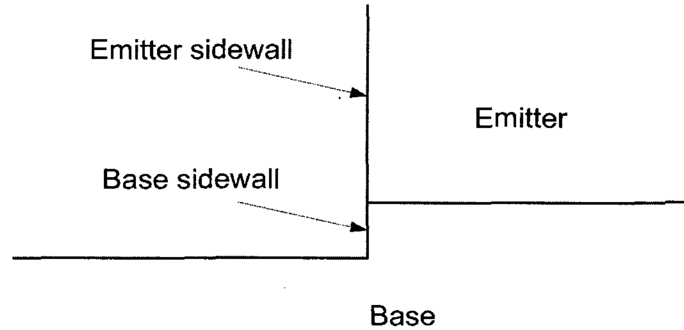


Figure 3-19: A schematic of a base sidewall with etched extrinsic base.

junction. In other words, the higher V_{BE} near the emitter perimeter leads to a higher injected current density at the periphery than in the middle of the emitter. This effect is called "emitter current crowding" [81]. Emitter crowding seems to enhance the electron injection onto the extrinsic base surface. However, due to the high base doping level and small emitter width of actual devices, this current crowding does not really occur. Fig. 3-18 shows the calculated lateral potential from the extrinsic base to the intrinsic base at a very high injection level. In the intrinsic area, the potential difference from the emitter centre to the perimeter is less than 1 mV. This potential drop is much smaller than kT/q, verifying that indeed emitter current crowding is not significant in the high-speed DHBTs under consideration here.

3.4.2 Impact of the Extrinsic Base Etching

In the above modelling, we assume that the emitter mesa etching perfectly terminates on the surface of the base layer. In reality, however, the extrinsic base would be etched out a little bit due to the finite wet etching selectivity and the electrochemical effect[5] [97, 98]. This base "over-etching" results in a small base sidewall (see Fig. 3-19). It has been found for GaAs HBTs that this etch of the extrinsic base may cause the periphery surface recombination current to increase [27]. For GaAsSb/InP type II HBTs, if the surface state condition on the base sidewall is assumed to be the same as that on the

[5] A process of converting chemical energy into electrical energy. In a solution, there might be current between the exposed base and metal electrode due to different surface potentials, which causes the electrochemical etching on the base.

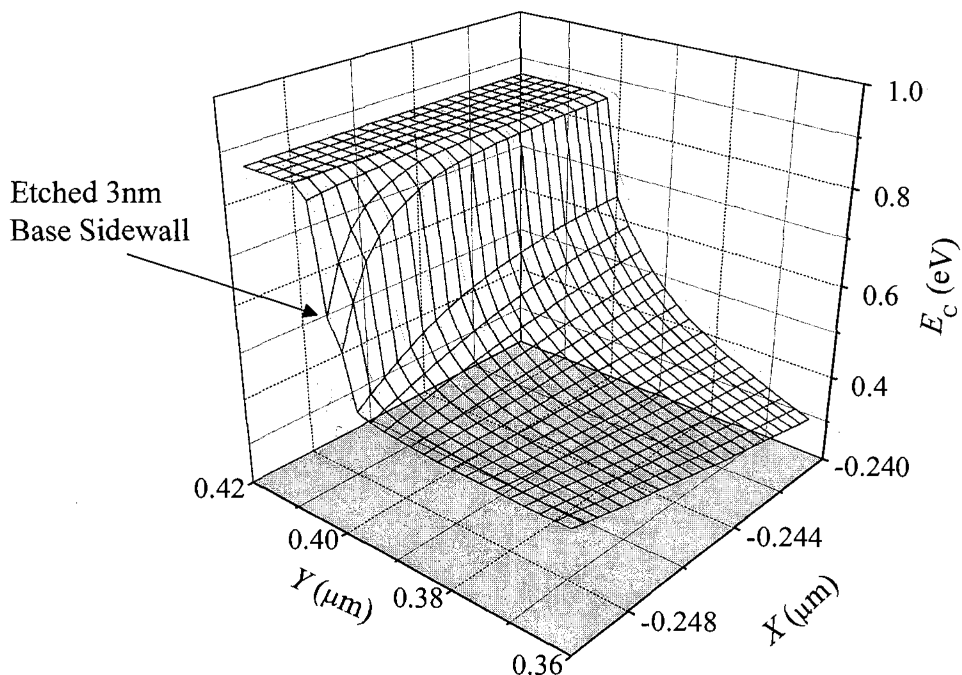


Figure 3-20: Simulated conduction band diagram in equilibrium around base and emitter sidewalls for GaAsSb/InP DHBTs with an etched extrinsic base of 30 Å. The extrinsic base region (not shown) is at $X < -0.25$ µm and $Y > 0.403$ µm, the intrinsic base region is at $X > -0.25$ µm and $Y > 0.400$ µm, the emitter region is at $Y < 0.40$ µm and the sidewall is at $X = -0.25$ µm.

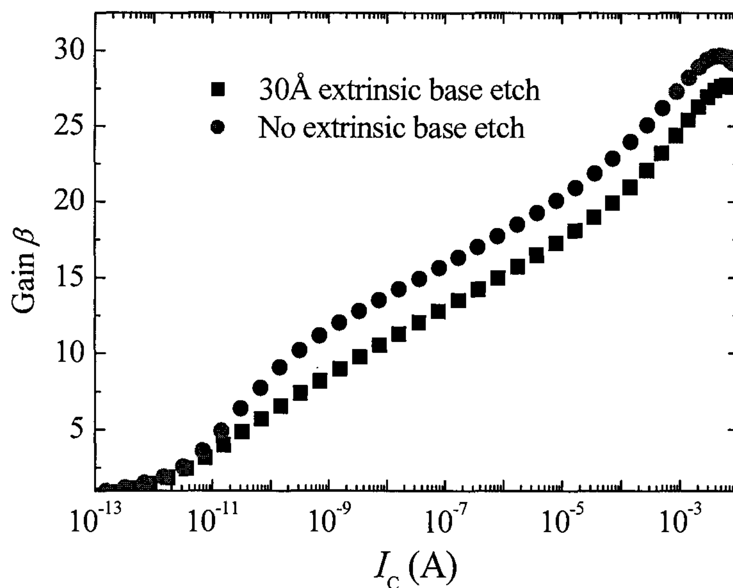


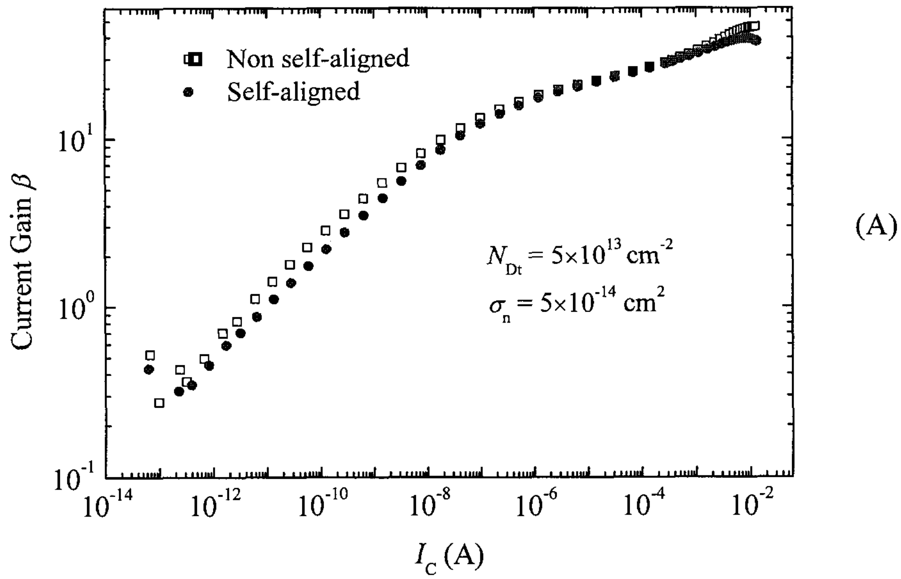
Figure 3-21: Simulated DC current gains for GaAsSb/InP DHBTs with 30 Å etched extrinsic base (squares) and without extrinsic base etching (circles).

extrinsic base surface (100), the downward band bending near the base sidewall due to the surface Fermi level pinning will directly drive the injected electrons toward the base surface where recombination takes place. Fig. 3-20 is the equilibrium conduction band 3D diagram around the base sidewall. Fig. 3-21 is a plot of the calculated DC current gain versus collector current for devices with and without a base sidewall induced by over-etching. We see that the etched base sidewall indeed increases the base surface recombination current and decreases the current gain.

3.4.3 Comparison of Self-aligned and Non Self-aligned Devices

Our experimental results show that self-aligned devices and non self-aligned devices display the same $K_{B,Surf}$, which means the emitter-base contact separation does not contribute to the size effect. In other words, all injected electrons recombine at the base surface, well before they can diffuse to the base contact.

To perform the simulation, we assumed that 0.1 μm and 0.5 μm are representative distances between the base contact and emitter edge for self-aligned and non self-aligned structures respectively. In this case, the emitter, base, and collector electrodes are set to be purely Ohmic contacts, and the recombination velocity at such contacts is assumed to be infinite. Simulations show that it is possible for SA and NSA devices to exhibit the same size effect (see Fig. 3-22). Note that in the modelling, the surface parameters and also the bulk parameters such as diffusion length have an impact on the electron transport near the base surface. Fig. 3-22 conceptually shows that if all electrons near the base surface recombine within a short distance, e.g., < 0.1 μm from the intersection of the base and emitter, the position of the base contact has no effect on the base surface recombination current. Fig. 3-22 confirms that the base-emitter contact separation only has a weak effect for typical material surface properties. This conclusion is in good agreement with our experiment results.



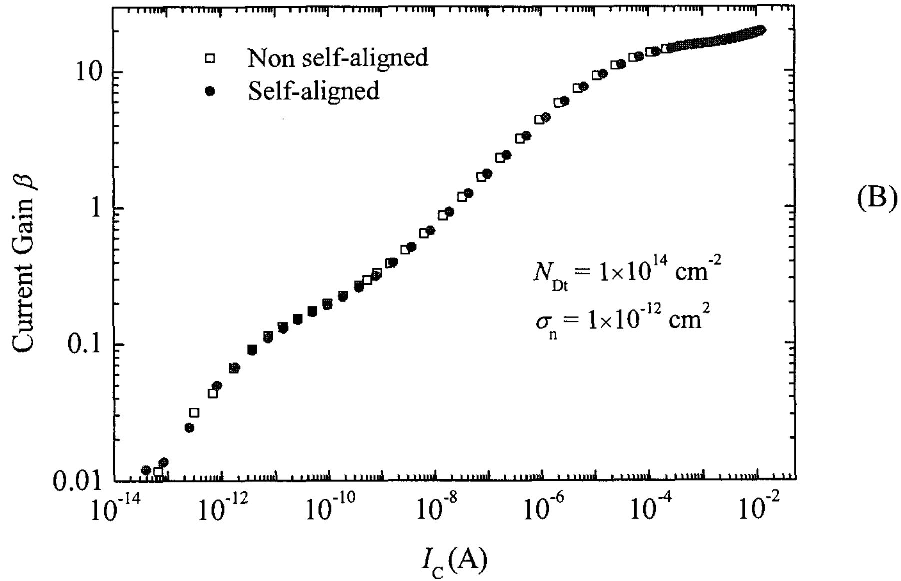


Figure 3-22: ***Simulated DC gain vs. collector current for self-aligned ($W_{BE} = 0.1\mu m$) and non self-aligned ($W_{BE} = 0.5\mu m$) devices with surface state modelling. The surface state density N_{Dt} and the electron capture cross section σ_n of the extrinsic base are 5×10^{13} cm^{-2} and 4×10^{-14} cm^{-2} for (A), and 1×10^{14} cm^{-2} and 1×10^{-12} cm^{-2} for (B).***

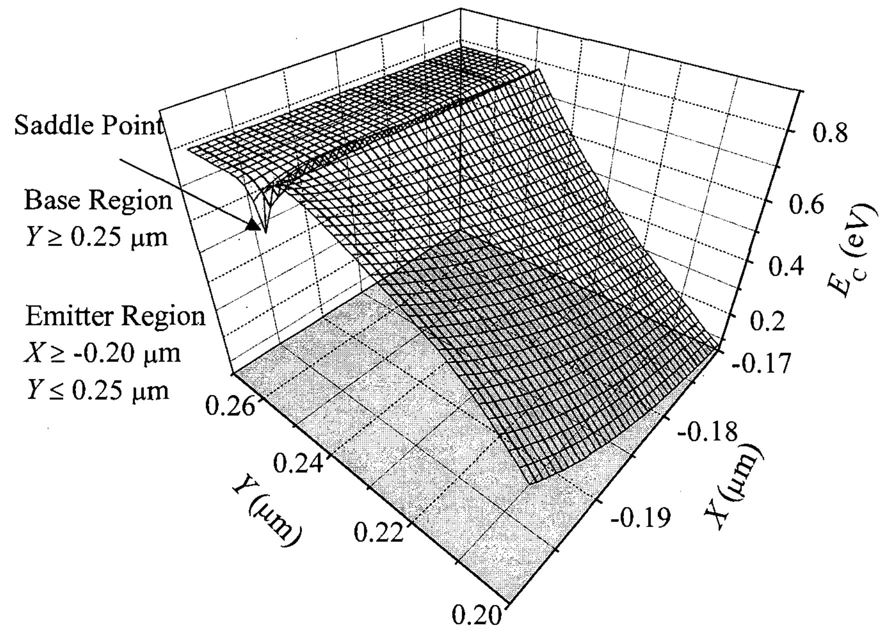


Figure 3-23: ***Simulated thermal equilibrium conduction band in the intrinsic base and emitter region of InAlAs/GaAsSb/InP DHBTs. The band alignment at the BE interface is a week type-I ($\Delta E_C \sim 0.05$ eV) which is different from the type-II in InP/GaAsSb/InP DHBTs.***

3.5 Solutions for Diminishing Surface Recombination Current

Surface passivation with dielectrics has been widely used to reduce surface recombination current and improve device reliability [24, 99]. As shown previously in our modelling, the surface recombination current primarily depends on the surface state conditions of both the base and emitter. Therefore, any passivation must modify the surface conditions such as the surface state density of the extrinsic base [100].[6] The following proposed solutions are based on modifications of the device structure itself rather than the use of dielectric passivation to diminish the periphery current.

3.5.1 $In_{0.52}Al_{0.48}As$/ $GaAs_{0.51}Sb_{0.49}$/InP DHBTs

In order to provide a direct comparison with InP/GaAsSb/InP DHBTs, the InAlAs/GaAsSb/InP DHBT structure is chosen to be identical to the previous

[6] Or prevent electrons from reaching the extrinsic base surface.

InP/GaAsSb/InP DHBTs with the exception that the InP emitter is replaced with lattice matched $In_{0.52}Al_{0.48}As$. The main parameters of $In_{0.52}Al_{0.48}As$ at room temperature are specified as follows [101]: energy band gap E_g = 1.44 eV, electron effective mass m_n= $0.074m_0$ and hole effective mass $m_p = 0.5m_0$. As for the conduction band offset at the BE junction, it has been reported that $\Delta E_C = E_C$(InAlAs) − E_C (GaAsSb) = 0.01 to 0.05 eV [102] which exhibits a week type-I band alignment, and on the other hand, the valence band offset with $GaAs_{0.51}Sb_{0.49}$ was measured as 0.64 eV [103]. Then, if the band gap of $GaAs_{0.51}Sb_{0.49}$ is 0.72 eV, the conduction band offset would be 0.06 eV. Therefore, we use ΔE_C(InAlAs/GaAsSb) = 0.05 eV for simulations. It has been found that there are two acceptor state centres at the $In_{0.52}Al_{0.48}As$ surface and their positions are about 0.65 eV and 1.00 eV below the conduction band edge respectively [104, 105]. Depending on the ratio of these two surface state densities, Fermi level could be pinned between 0.65 eV and 1.00 eV [106]. For simplicity, we still use single discrete surface states to model the surface Fermi level pinning.

Fig. 3-23 is a 3D plot of the conduction band edge of intrinsic InAlAs/GaAsSb BE area in thermal equilibrium. The conduction band of the extrinsic base is similar to Fig. 3-10B. A downward band bending toward the "saddle point" still can be seen, but the curvature seems weaker compared to the InP/GaAsSb/InP case of Fig. 3-10A. This is probably due to the larger surface Fermi level pinning under the conduction band edge in InAlAs.

Fig. 3-24 shows the calculated $K_{B,Surf}$ as a function of J_C for InP/GaAsSb/InP and InAlAs/GaAsSb/InP DHBTs with different Fermi pinning levels at InP and InAlAs surfaces respectively. We can see that the lower the Fermi level position below the conduction band edge, the smaller the $K_{B,surf}$ would be, because more energy band upward bending near the emitter sidewall will weaken the electron injection into the saddle point. In the simulation of Fig. 3-24, the surface state density N_{Dt} and electron capture cross section σ_n at GaAsSb base surface are 5×10^{13} cm^{-2} and 2×10^{-14} cm^2 in all cases.

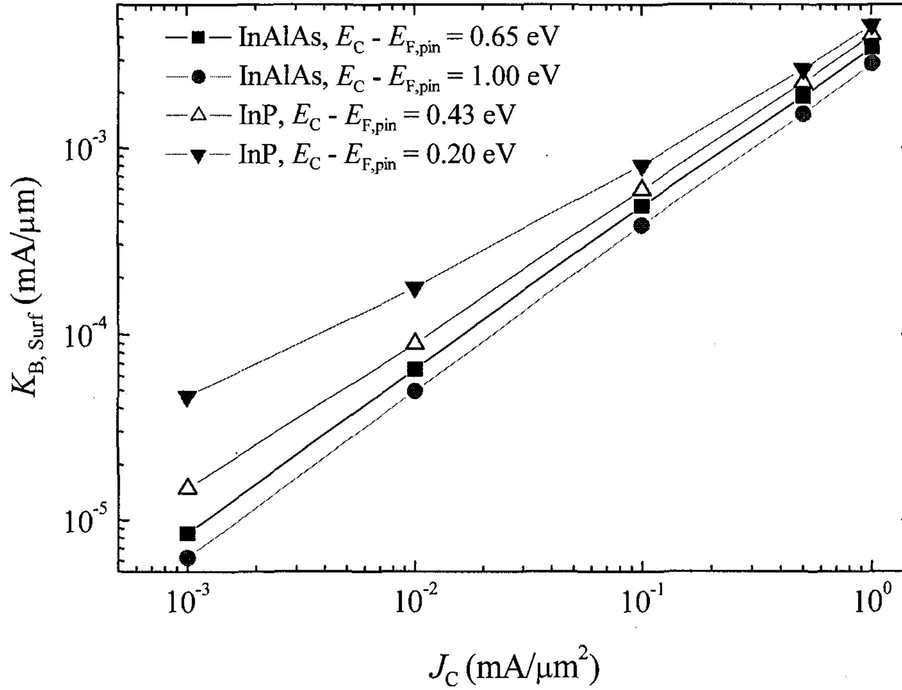


Figure 3-24: Simulated periphery surface recombination current density ($K_{B,Surf}$) vs. collector current density (J_C) for InAlAs/GaAsSb/InP and InP/GaAsSb/InP DHBTs with different Fermi levels at the InAlAs and InP surfaces respectively. The Fermi pinning levels displayed in the legend present the values below the corresponding conduction band edge.

It has been reported that some kinds of passivation on InP/InGaAs HBTs make the base surface recombination current even larger [107] because the deposited dielectrics, e.g., silicon oxide, can pin the Fermi level at the InP surface close to the conduction band edge. This results in more electron injection onto the extrinsic base surface. Fig 3-24 shows that the InP surface with a Fermi level of 0.2 eV below the conduction band edge gives rise to the highest $K_{B,Surf}$, while the lowest $K_{B,Surf}$ is due to the InAlAs surface with a Fermi pinning level of 1 eV below the conduction band edge.

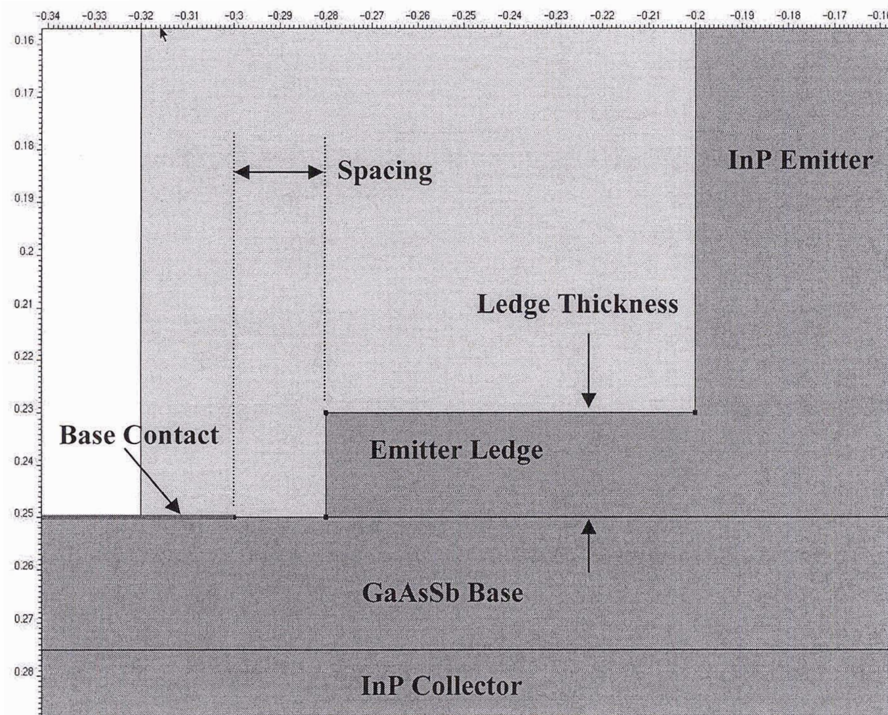


Figure 3-25: An InP/GaAsSb/InP DHBT cross section with emitter ledge.

3.5.2 InP Emitter Ledge

In the fabrication of GaAs HBTs, the emitter ledge has been used to dramatically decrease the base surface recombination current. Recently, a great improvement of the reliability of InP/InGaAs HBTs with a ledge structure has been reported [108]. Similarly, we could use the InP emitter ledge in our GaAsSb-based DHBTs as schematically shown in Fig. 3-25. The ledge has two features: it reduces the exposed area of the extrinsic base surface and it is highly depleted not only by the Fermi pinning at the upper and left surfaces (see Fig. 3-25) but also by the interface with the base.

We studied four different ledge structures in which the ledge thickness is either 200 Å or 50 Å, and the spacing between the base metal and ledge is either 200 Å or zero. The ledge with zero spacing covers the entire extrinsic base [109] and is called a full ledge (and the other is called a partial ledge). Comparisons of a normal device without ledge and the devices with four different ledge sizes are shown in Fig. 3-26. Compared to the normal device, a thick ledge (200 Å) with a spacing (200 Å) does not make much

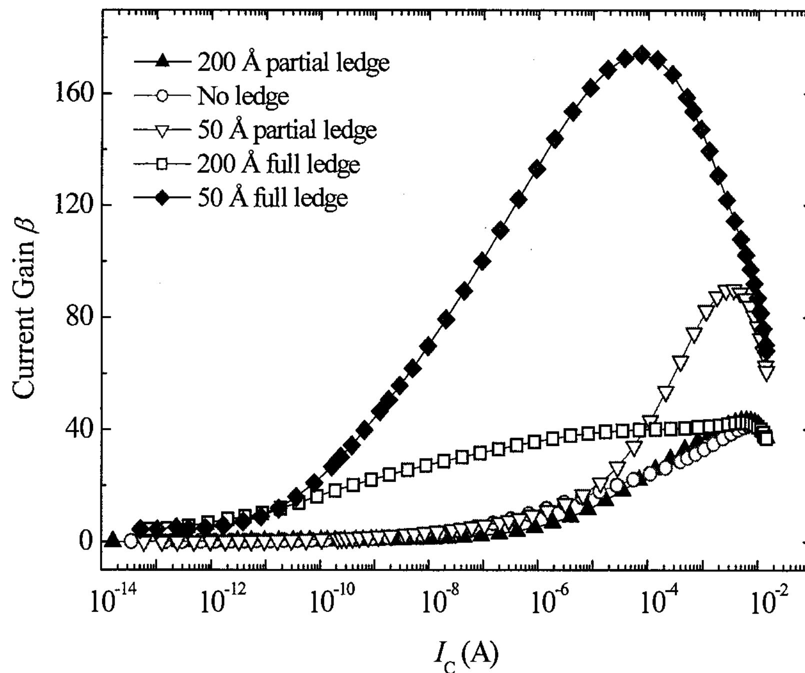


Figure 3-26: Simulated DC current gain β vs. collector current I_C for GaAsSb/InP DHBTs with different InP emitter ledge structures. Triangles: 200 Å spacing between the base metal and ledge with 200 Å thickness; circles: without emitter ledge; inverted triangles: 200 Å spacing between the base metal and ledge with 50 Å thickness; squares: zero spacing between the base metal and ledge with 200 Å thickness; diamonds: zero spacing between the base metal and ledge with 50 Å thickness.

difference, which indicates that many electrons are still injected from the thick ledge and recombine at the extrinsic base surface within the spacing area. If the ledge thickness is reduced to 50 Å while the spacing does not change, electron injection onto the extrinsic base surface can be significantly depressed and the current gain becomes nearly two fold higher, especially at high collector current levels. Zero spacing means no more base surface states, which will be beneficial for decreasing the periphery current. Even for the thick ledge, zero spacing gives rise to a significantly higher gain especially at low current levels. The highest gain at most current levels may be obtained by using thin ledge (50 Å) without spacing between the base metal and ledge.

Fig. 3-28 shows a 2D electron density contour map at a high bias for the device with a ledge of 200 Å thickness and zero spacing. We can see that the electron density at

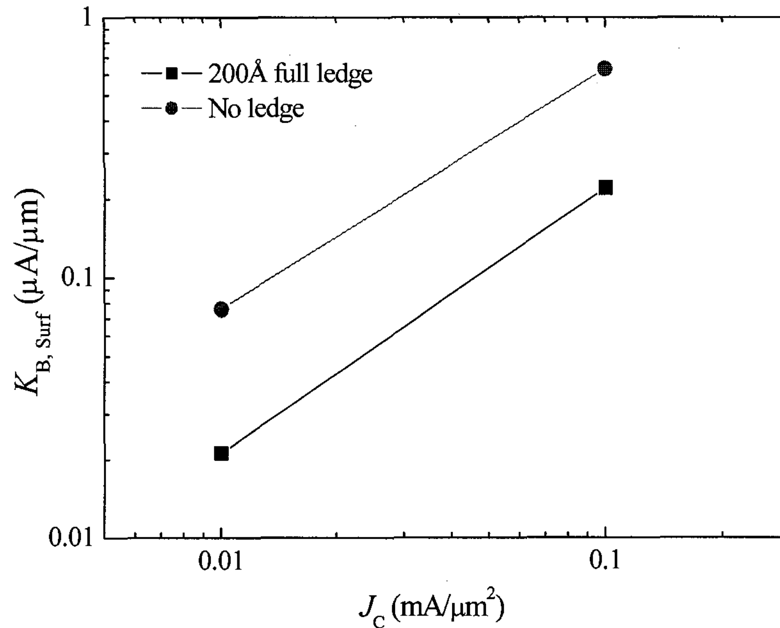


Figure 3-27: Simulated periphery recombination current density $K_{B,Surf}$ vs. collector current density J_C for InP/GaAsSb/InP DHBTs with full emitter ledge of 200 Å thickness (squares) and without emitter ledge (circles).

the InP ledge surface is extremely small and the surface recombination current is negligible. At high collector current levels, the electron density near the interface of the ledge and base is very high, which indicates a certain electron injection across the base ledge interface. It is noted that the emitter size effect for devices with zero spacing ledge structures still exists, although it is very weak. Instead of the base surface recombination, the following two recombination processes might be responsible for this residual size effect: bulk recombination of the electrons injected from the ledge to the base (especially at high bias), and the recombination at the base contact. Nevertheless, the periphery current density $K_{B,Surf}$ of devices with a full ledge is much weaker than that for devices without ledge, as shown in Fig. 3-27. Although only the data at two collector current densities is displayed in Fig. 3-27, the same trend can be found at other current levels (see Fig. 3-26).

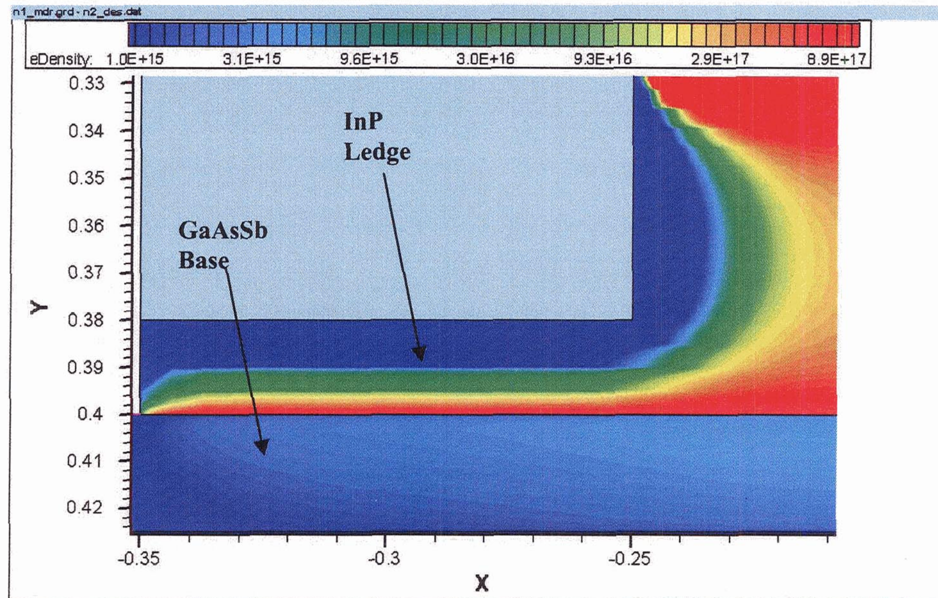


Figure 3-28: Simulated 2D electron concentration of the InP/GaAsSb/InP DHBT with an emitter ledge at the collector current density of around 0.08 mA/μm².

3.6 Conclusions

We experimentally characterized the emitter size effect in InP/GaAsSb/InP DHBTs in terms of the base surface recombination current density $K_{B,Surf}$ for self-aligned and non self-aligned devices. We also found that the SA and NSA devices show the same size effect, and that a base with heavy doping level and tensile strain will apparently give rise to higher $K_{B,Surf}$ than a moderately doped lattice matched base. More importantly, we have observed that InP/GaAsSb/InP DHBTs exhibit the same surface recombination characteristics as InP/InGaAs HBTs.

To model the ESE for GaAsSb/InP DHBTs, we performed simulations using ISE TCAD. The results showed that the surface recombination current primarily depends on the surface state conditions at the extrinsic base surface and emitter sidewall, since the surface states determine not only the surface recombination velocity but also the degree of band bending around the "saddle point" through which electrons are injected onto the extrinsic base surface. The measured ESE is in a good agreement with the simulated one.

Based on our modelling, we have discussed the emitter crowding effect and extrinsic base over-etching, which are related to the device periphery current. We have also proposed two solutions to diminish the periphery surface recombination current and ESEs in GaAsSb-based DHBTs. These two solutions further demonstrate that from device structure point of view, the periphery current strongly depend on the surface conditions of both the emitter and base.

Chapter 4:

Kirk Effect in Type-II GaAsSb/InP DHBTs

4.1 Overview

In the present Chapter, we examine the high-current level operation of GaAsSb/InP DHBTs. The subject is of high importance because the transistors are often used at high current densities to maximize their operating speeds.

In Chapter 2, we introduced the current gain cut-off frequency f_T of a bipolar transistor in (2-30), which we repeat here for convenience:

$$f_T = \frac{1}{2\pi \cdot \tau_{EC}} \text{ and } \tau_{EC} = \tau_B + \tau_C + (R_E + R_C)\cdot C_{jC} + \frac{nkT}{qI_C}\cdot (C_{jE} + C_{jC}).$$

This expression suggests that the emitter-collector delay time τ_{EC} is continuously reduced with an increasing collector current I_C, but in practice it is found that τ_{EC} increases beyond a certain critical current level. The decrease in transistor dynamic performance is accompanied by a simultaneous current gain reduction visible in the Gummel characteristics. The effects of increasing current levels on the cut-off frequency and DC current gain of bipolar transistors are shown in Fig. 4-1.

C. T. Kirk developed a theory to explain such effects in silicon bipolar (homo)junction transistors (BJTs) [29]. The theory shows that at high collector current, the electron density travelling through the depleted n-type collector can no longer be ignored with respect to the positive space charge of depleted donors in the collector, and that consequently, the electric field at the BC junction decreases.

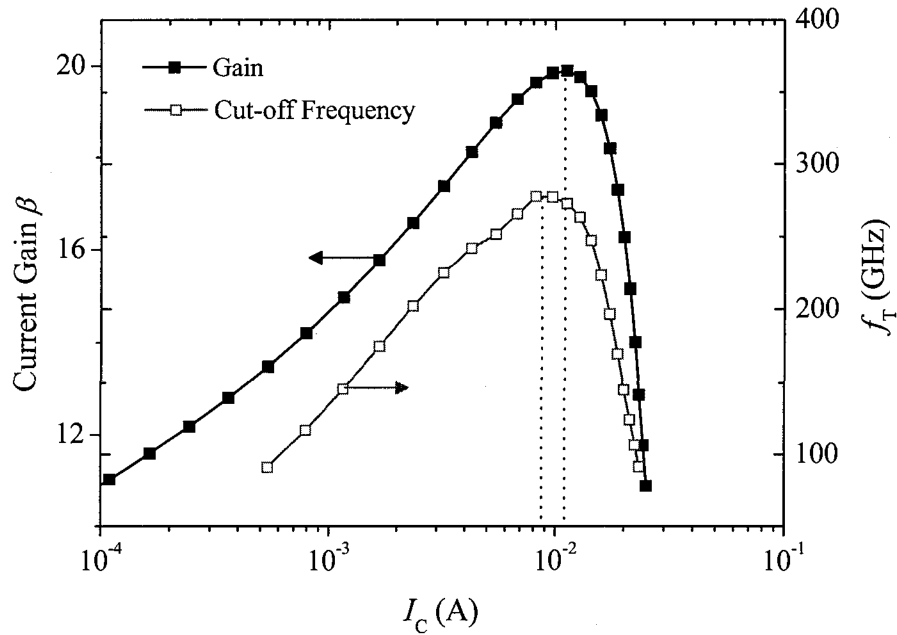


Figure 4-1: ***The fall-off of the DC gain and of the current gain cut-off frequency at high injection levels due to the Kirk effect in a InP/GaAsSb/InP DHBT. The cut-off frequency begins its roll-off at slightly lower current levels.***

It must be noted that under zero-current conditions the peak electric field occurs right at the metallurgical junction between the p^+-base and the n-collector (see Fig. 4-2A). When the electric field at the BC junction collapses, it no longer prevents holes from the base region from entering into the collector, and the so-called "*base pushout*" occurs. This sequence of events is commonly referred to as the "Kirk effect". Base pushout dramatically increases the base transit time associated with the new effective base thickness, and therefore $f_T = \frac{1}{2\pi \cdot \tau_{EC}}$ decreases precipitously. The enhanced recombination accompanying the base extension into the collector region also causes a reduction of the current gain.

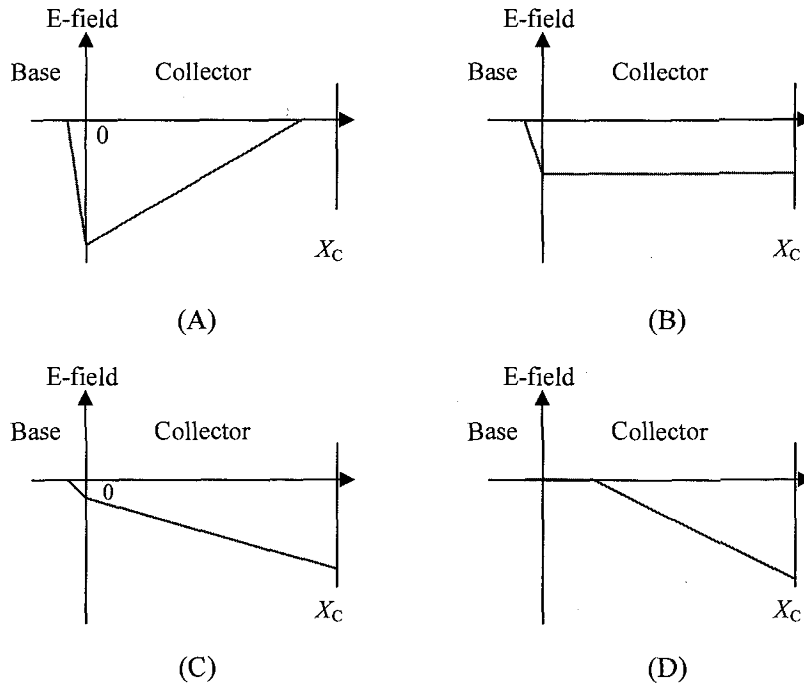


Figure 4-2: ***The evolution of the electric field at a BC junction with increasing current level. The BC junction is at the origin, and X_C is at the collector-subcollector junction. (A): J_C is low and the mobile electron density is negligible, (B): J_C increases so that the mobile electron density is comparable to the collector doping density, (C): J_C is high and the mobile electron density is greater than the collector doping level so that the field at the junction decreases to zero, (D): with further increasing J_C, base pushout occurs.***

The mobile electron density in the collector depletion region is given as

$$n = \frac{J_C}{qv}, \quad (4\text{-}1)$$

where J_C is the collector current density, and v is the electron velocity which we assume to be constant for the sake of reaching a closed-form solution in our analysis. Conventionally, the assumption of a constant velocity v is rooted in the electron saturation velocity v_{sat} in high electric fields. The Poisson equation relating the electric field to the net space charge density in the collector depletion region can be written as

$$\frac{dE}{dx} = \frac{1}{\varepsilon}\left(qN_{\mathrm{C}} - \frac{J_{\mathrm{C}}}{v}\right), \qquad (4\text{-}2)$$

where N_{C} is the collector doping concentration assuming the donors are fully ionized and that hole concentration in the collector is neglected. At low current density, n is much smaller than N_{C} and can be neglected in (4-2). By solving (4-2), one can obtain the Kirk critical current density at which the electric field E at the BC junction goes to zero:

$$J_{\mathrm{Kirk}} = v\left(qN_{\mathrm{C}} + \frac{2\varepsilon(V_{\mathrm{CB}} + \varphi_{\mathrm{CB}})}{X_{\mathrm{C}}^2}\right), \qquad (4\text{-}3)$$

where V_{CB} is the applied reverse bias to the BC junction, X_{C} is the collector thickness and φ_{CB} is the built-in voltage of the BC junction. In a bipolar transistor with a BC homojunction, the classic Kirk effect is characterized by base pushout, and the Kirk current density is entirely determined by the collector quantities such as the doping, thickness, and electron velocity in the collector.

In this Chapter, we demonstrate both experimentally and with the aid of numerical simulations that in type-II GaAsSb/InP DHBTs, the *base layer* can also play an important role in determining the high-current performance limitations. Until now, the pertinence of base parameters on the high-current performance of type-II DHBTs has not yet been discussed by others.

We first present a comparison of the Kirk effect in BC homojunctions and in type-II BC heterojunctions in Section 4.2. In Section 4.3, we experimentally characterize the Kirk effect for GaAsSb/InP DHBTs with differing base doping levels. In Section 4.4, we develop a modified Kirk effect theory using 2D numerical simulation. The last Section summarizes the findings of this Chapter.

4.2 Numerical Simulation of Kirk effect

As early mentioned, the investigation of Kirk effect essentially involves solving the Poisson equation for different collector current densities. Modern numerical simulators such as ISE TCAD [28] self-consistently solve both the Poisson and the

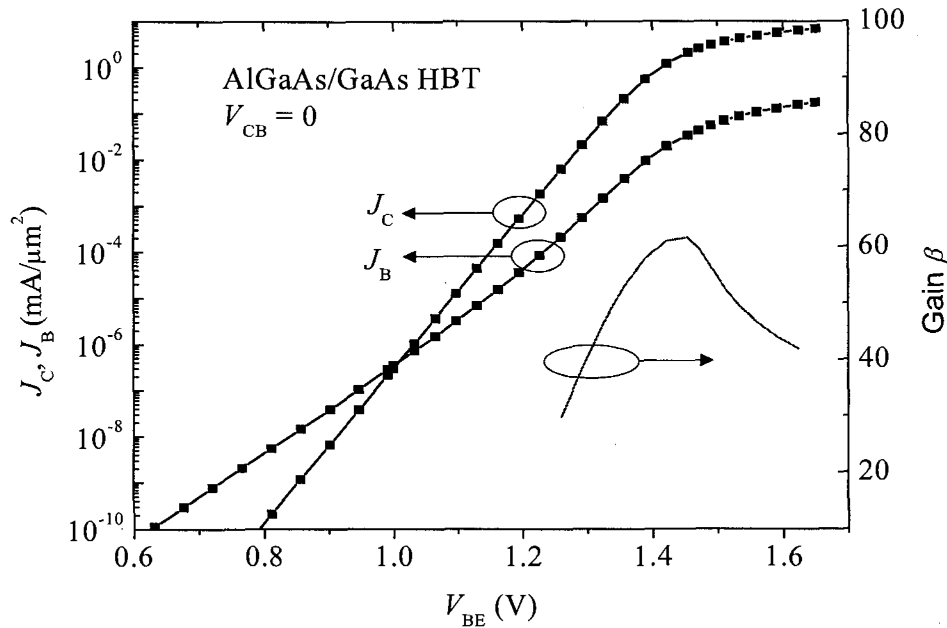


Figure 4-3: Simulated Gummel plot for an AlGaAs/GaAs HBT. The onset of Kirk effect is at V_{BE} = 1.45 V when the gain β peaks.

transport equations, and allow a more advanced investigation of the Kirk or high-current effects than can be achieved by simple analytical approximations. The principal over-simplification in (4-3) is that electron velocity is assumed to be constant due to velocity saturation in the collector. However, the electron velocity strongly depends on the electric field profile in the collector, and electron "overshoot" always occurs near the BC junction [110]. We first begin with the numerical modelling of the Kirk effect in a prototypical AlGaAs/GaAs HBT BC homojunction.

4.2.1 BC Homojunction Prototype: The AlGaAs/GaAs HBT Case

The structure consists of a 2000 Å AlGaAs emitter n-doped to 8×10^{17} cm^{-3}, a 1000 Å GaAs base p-doped to 1×10^{19} cm^{-3} and a 3000 Å GaAs collector n-doped to 1×10^{17} cm^{-3}. Simulations were performed at V_{CB} = 0 V for different injection levels determined by the applied base-emitter voltage: V_{BE} = 1.15, 1.45, 1.5 and 1.6 V. The onset of the Kirk effect is at V_{BE} = 1.45V as shown in Fig. 4-3: this also corresponds to the bias for peak current gain $\beta = I_C / I_B$. The corresponding electron density, electric

field, hole density and conduction band edge profiles in the base and collector are shown in Fig. 4-4, Fig. 4-5, Fig. 4-6 and Fig. 4-7 respectively.

We can see from Fig. 4-4 that the collector electron density is comparable to the doping level at the onset of the Kirk Effect: the electric field dramatically decreases toward zero near the BC junction compared to the situation at V_{BE} = 1.15 V. When the injection level continues to increase, the collector electron density increases, and the slope of the electric field becomes negative, in agreement with the behaviour expected from Equation (4-2). Eventually, the zero-field region extends from the BC metallurgical junction toward the sub-collector because of the need to enforce a constant base-collector voltage (corresponding to the area under the electric field profile through the collector).

Most importantly, with increasing bias, holes from the base layer spill into the collector as shown in Fig. 4-6. Even at a relatively low bias of V_{BE} = 1.45 V corresponding to the onset of the Kirk effect, holes clearly enter the collector. The pushout hole density corresponds to the electron density in order to maintain neutrality in the extended base region. The collapse of the electric field at the base-collector junction flattens both the conduction and the valence bands near the metallurgical junction: the resulting band diagram looks as *if* the base layer widened into the collector. This situation is often referred to as "base pushout" for reasons that are immediately apparent from the band diagram. On the base side of the metallurgical BC junction, the electron density is seen to increase with the injection level and the narrow base depletion region vanishes as the electric field collapses at the junction.

We can find from Fig. 4-3 that the simulated Kirk collector current density $J_{C,Kirk}$ ~ 2.02 mA/μm^2. On the other hand, according to (4-3), $J_{C,Kirk}$ ~ 1.96 mA/μm^2, if we use the same parameters in the simulation: $N_C = 1\times10^{17}$ cm^{-3}, $v_{sat} = 1\times10^{7}$ cm/s, $\varepsilon = 13$, φ_{CB} = 1.4 V, and X_C = 0.3 μm. Apparently, the simulation results for AlGaAs/GaAs HBTs agree very well with the original Kirk effect theory.

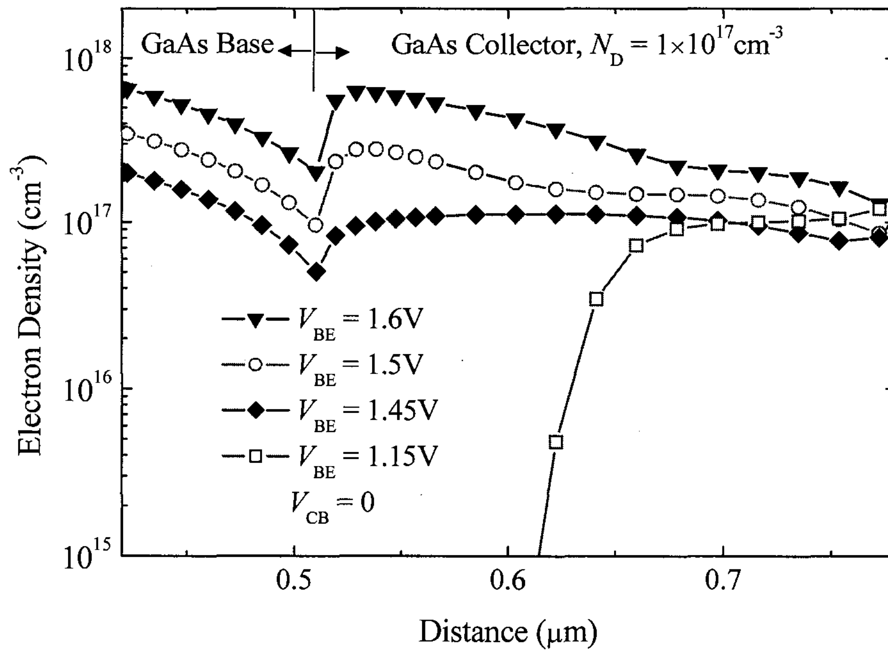


Figure 4-4: ***Simulated electron density around BC homojunction of an AlGaAs/GaAs HBT with different biases. The onset of Kirk effect is at V_{BE} = 1.45V.***

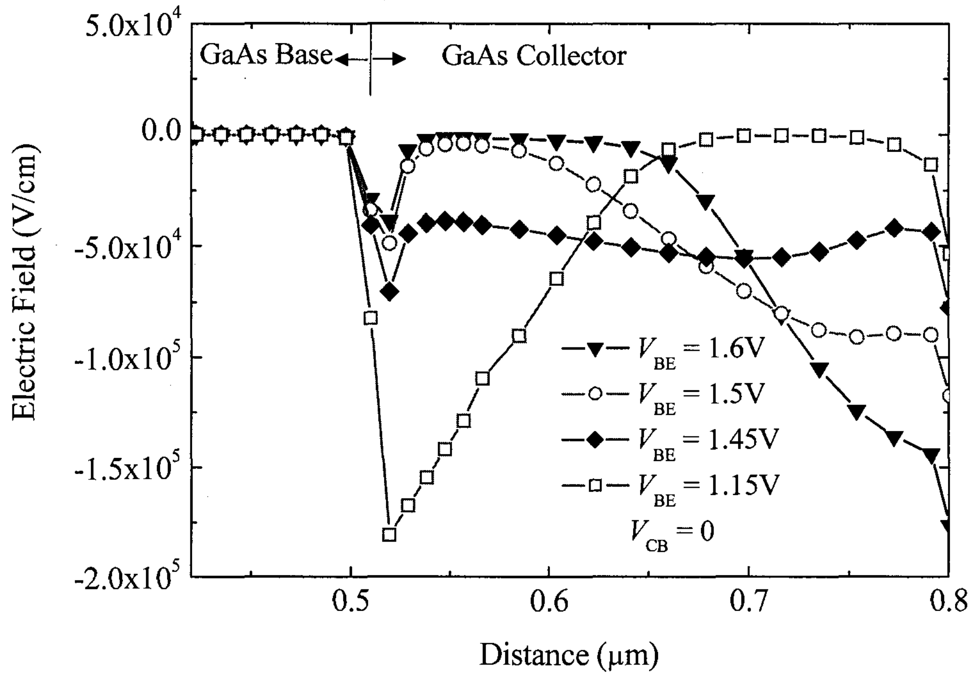


Figure 4-5: ***Simulated electric field around BC homojunction of an AlGaAs/GaAs HBT with different biases. The onset of Kirk effect occurs at V_{BE} = 1.45V.***

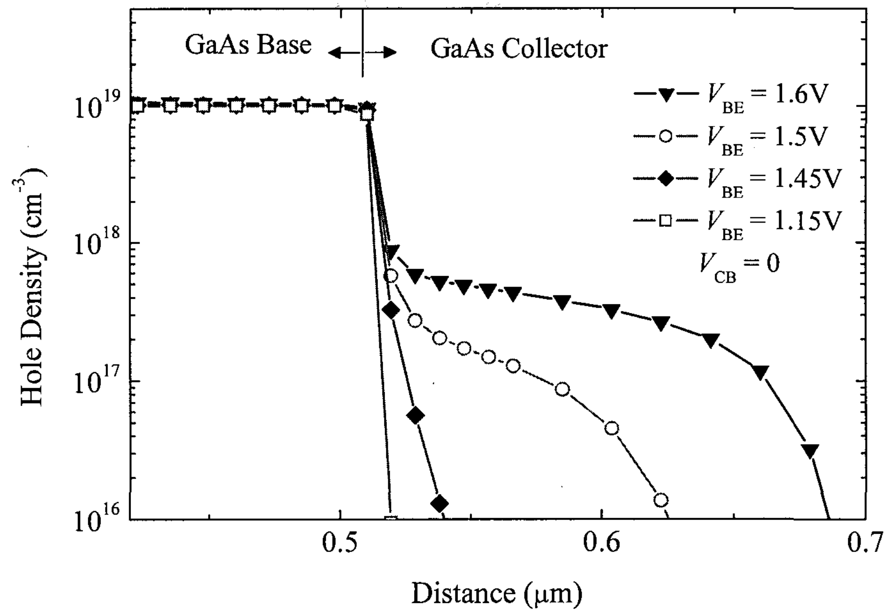


Figure 4-6: ***Simulated hole density around the BC homojunction of an AlGaAs/GaAs HBT with different biases. The onset of Kirk effect occurs at V_{BE} = 1.45V.***

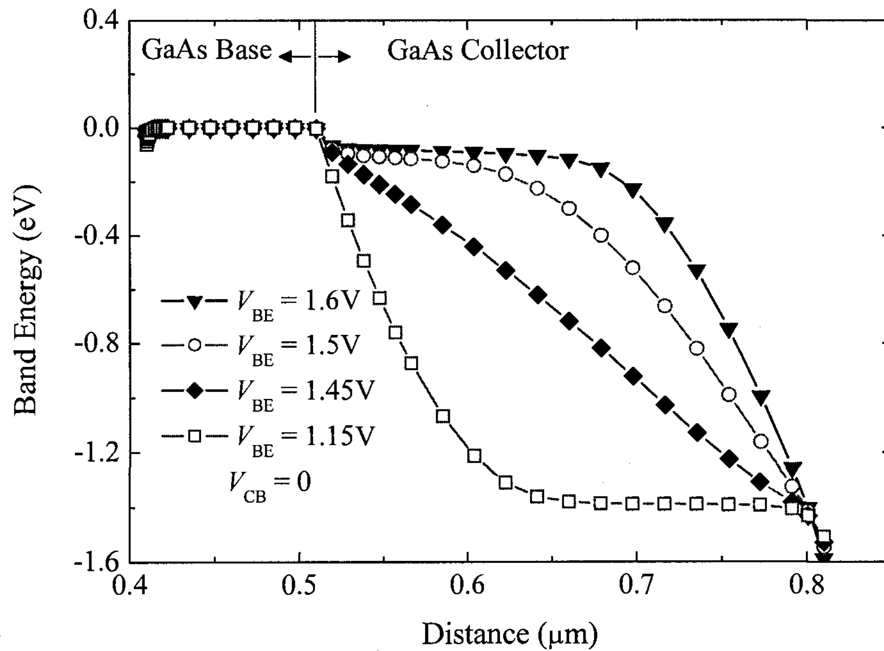


Figure 4-7: ***Simulated conduction band profile across the BC homojunction of an AlGaAs/GaAs HBT with different biases. The onset of Kirk effect occurs at V_{BE} = 1.45 V.***

4.2.2 Type-II BC Heterojunction DHBTs

The type-II GaAsSb/InP DHBT structure (#4451) we used for simulation is shown in Table 4-1, and will be described in detail later. The simulation was performed at three different injection levels: V_{BE} = 0.52, 0.69 and 0.76V, representing a low current level, the onset of the Kirk effect, and a high current level, respectively. Fig. 4-8, Fig. 4-9, Fig. 4-10, and Fig. 4-11 show the profiles of the electron density, electric field, hole density, and conduction band edge profile throughout the base and collector regions.

Let us first consider the situation from low biases to the onset of Kirk effect. The electron density in the collector increases with the injection level, and at the onset of Kirk effect, it is close to the donor doping level in the depleted collector region. The electric field decreases toward zero, and the change of the field profile indicates that the space charge region expands throughout the collector. Also, the curvature of the conduction band edge profile becomes smaller at both base and collector sides, and the depletion space charge at the base side is vanishing as the hole density of the base near the BC junction increases to the base doping level. The scenario is so far similar to the case of the BC homojunction. Hence, the picture presented by the original Kirk theory is applicable to the type-II BC heterojunction under low injection levels.

The situation changes at higher injection levels. The electric field points in a given direction throughout most of the collector, but it becomes inverted near the BC junction. The conduction band edge bulges upward on the collector side, and it becomes convex on the base side near the BC junction. The change of the conduction band profile demonstrates that an electron barrier is developing on the base side of the BC junction with further increase of the injection. Most importantly, Fig. 4-10 shows that there is no hole spilling into the collector, and that hole accumulation occurs on the base side. In other words, no base pushout takes place because of the band alignment in type-II GaAsSb/InP DHBTs. For further demonstration, the computed hole density and valence band edge profiles under an extremely high injection level are shown in Fig. 4-12. We can see that there is still *no evidence whatsoever of base pushout* because of the large valence band discontinuity between GaAsSb and InP. The valence band offset ΔE_V in the case of #4451 is set to be 0.78 eV. At an injection level corresponding to 6 times of the

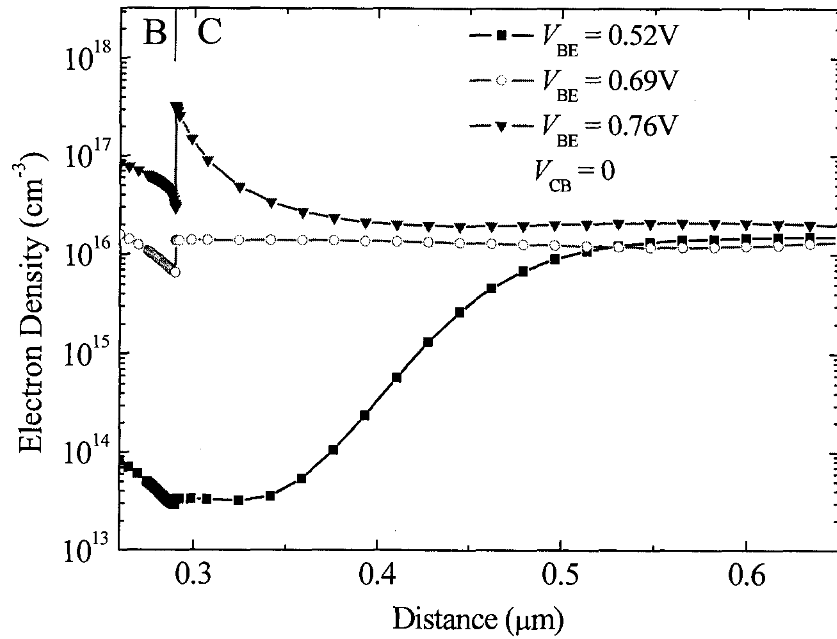


Figure 4-8: ***Simulated electron density in the base and collector of a GaAsSb/InP DHBT at various biases. The onset of the Kirk effect occurs at V_{BE} = 0.69 V when the current gain peaks.***

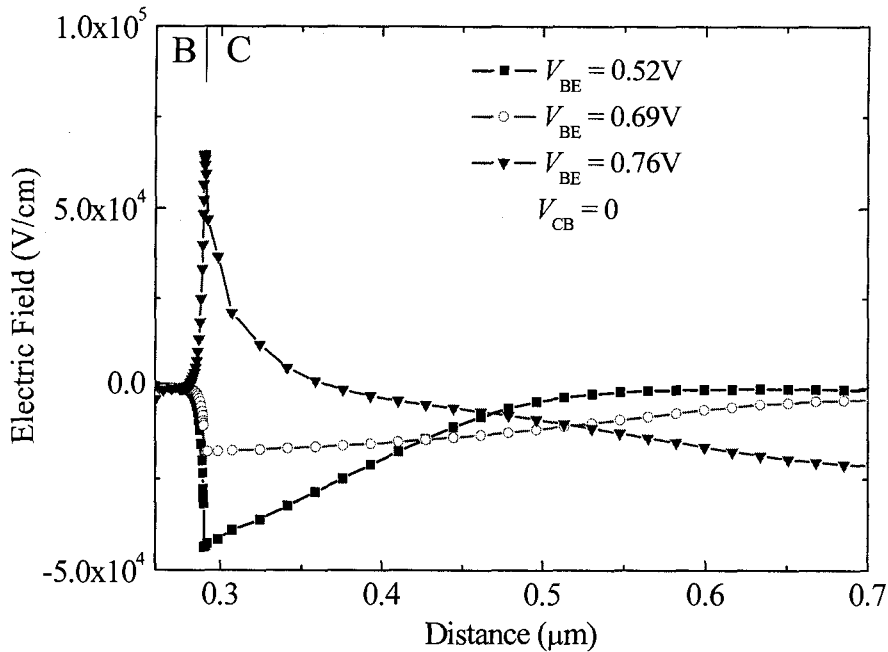


Figure 4-9: ***Simulated electric field in the base and collector of a GaAsSb/InP DHBT at various biases. The onset of the Kirk effect occurs at V_{BE} = 0.69 V.***

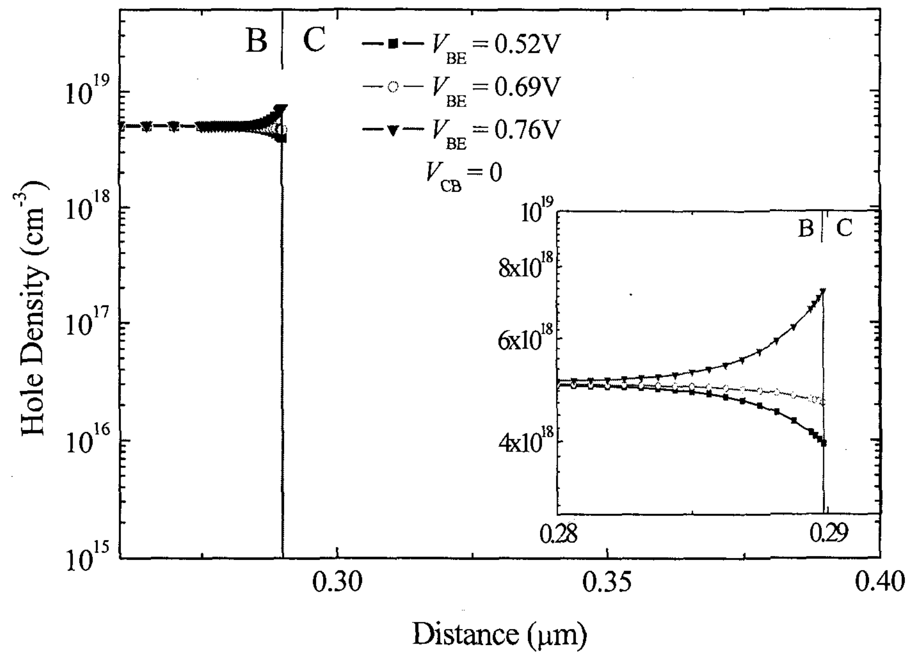


Figure 4-10: ***Simulated hole density in the base and collector of an GaAsSb/InP DHBT at various biases. The onset of the Kirk effect occurs at V_{BE} = 0.69 V. No base pushout is found and hole accumulation occurs at the base side of the BC junction. Inset is the magnified hole density profiles near the BC junction.***

critical Kirk current density, the effective valence band offset $\Delta E_V - \phi$ [33] is still as high as 0.5 eV, where ϕ is the total electron barrier that is shown in Fig. 4-12.

Because base pushout is not possible, hole accumulation occurs on the *base* side of the BC junction and as a result, an *induced* electron barrier develops (see the inset of Fig. 4-10). This barrier directly impedes the outflow of electrons from the base into the collector by limiting the exit velocity from the base in a way that is very similar to a thermionic barrier. Consequently, the electron blocking gives rise to an increased base recombination, and the base current increases. At the collector side of the BC junction, electrons also encounter an impediment due to the local polarity reversal in electric field. However, due to the type-II conduction band offset electrons still enter the collector with enough kinetic energy to overcome the opposing field until the reversed electric field becomes so high that $\phi > \Delta E_C$.

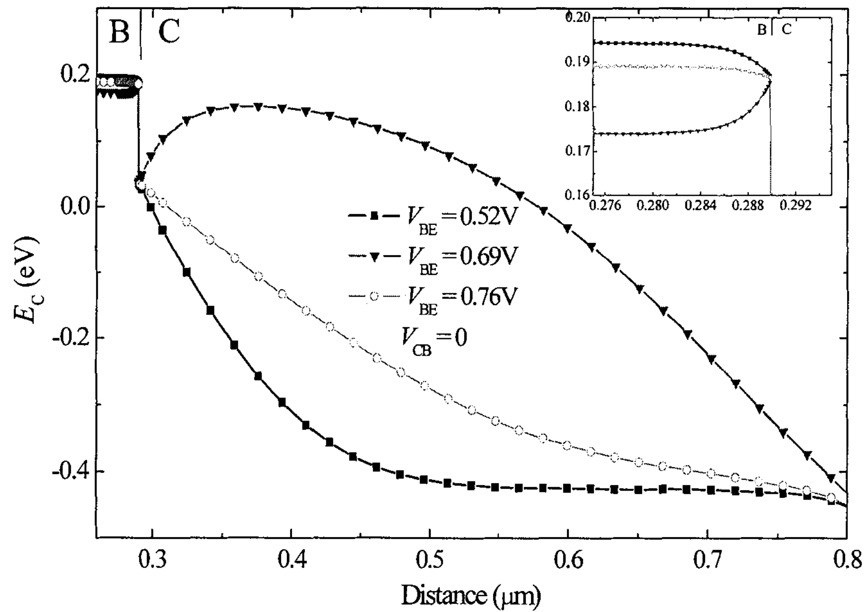


Figure 4-11: Simulated conduction band edge in the base and collector of an GaAsSb/InP DHBT at various biases. The onset of the Kirk effect occurs at V_{BE} = 0.69 V. Inset is magnified conduction band edge profiles on the base side of the BC junction.

We have determined that high injection effects in type-II GaAsSb/InP DHBTs appear by the induction of an electron blocking barrier in the base rather than by the spreading of the base region into the collector as in homojunction devices. For this developing barrier, electrons should obey thermionic-field emission [73, 111]. We anticipate that in the early stage of the barrier development, the barrier height and width are so small that electrons can still tunnel as if it were transparent. When the barrier grows to a certain point where electrons are efficiently blocked, base recombination current increases and the current gain drops sharply. Therefore, the Kirk effect mechanism in type-II GaAsSb/InP DHBTs is quite different from that in conventional BC homojunction HBTs.

We now apply the quantum mechanical tunnelling model to the simulation of GaAsSb DHBTs to study the electron barrier developing at high injection levels. Fig. 4-13 presents simulated characteristics with and without including the tunnelling process to the barrier induced at the BC junction. We find that:

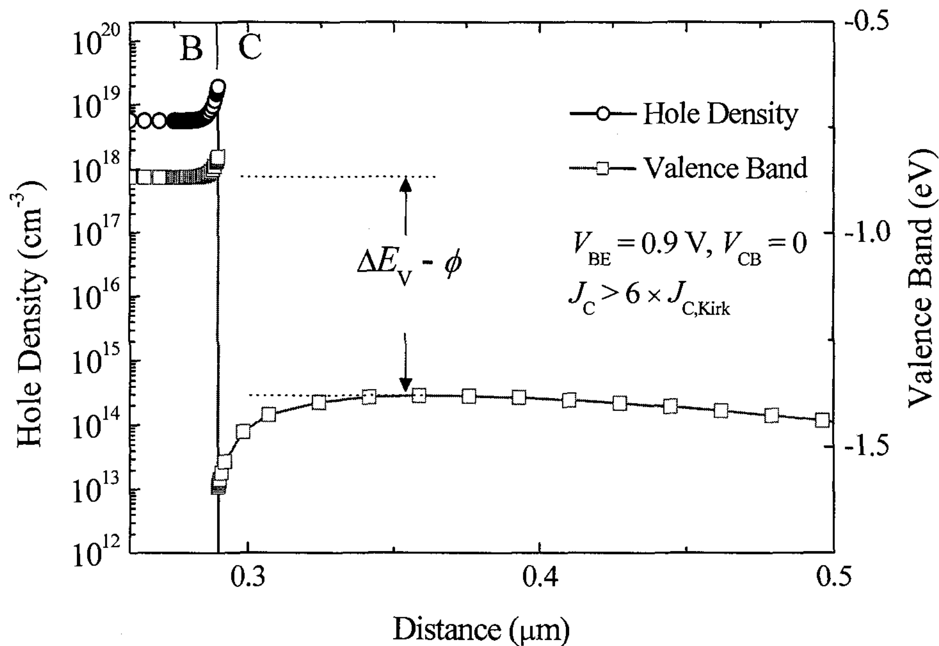


Figure 4-12: Simulated hole density and valence band edge in the base and collector of a GaAsSb/InP DHBT at high bias. The effective valence band offset at the BC junction is nearly 0.5 eV.

1. The difference between two Gummel plots appears only in the high current level regime, which indicates that the electron barrier only becomes important at high injection levels. In particular, the base current with the tunnelling model exhibits a notable "knee" feature around the bias of the peak collector current. This "knee" was observed experimentally in our devices (see Fig. 4-15).

2. Both the current level at the onset of the Kirk effect and the resulting current gain predicted with the tunnelling model are higher than those computed without applying the tunnelling model. This shows that the tunnelling weakens the barrier effect, and helps postpone the onset of Kirk effect.

3. Quantitatively, the Kirk current density of the Gummel plot without tunnelling model is about 0.22 mA/μm^2. This value is close to the one calculated with conventional Kirk current formula (4-3) which gives 0.27 mA/μm^2 if we use the same parameters as in the simulation, e.g., $v_{sat} = 1\times10^7$ cm/s, $\varphi_{CB} = 0.45$ V, $N_C =$

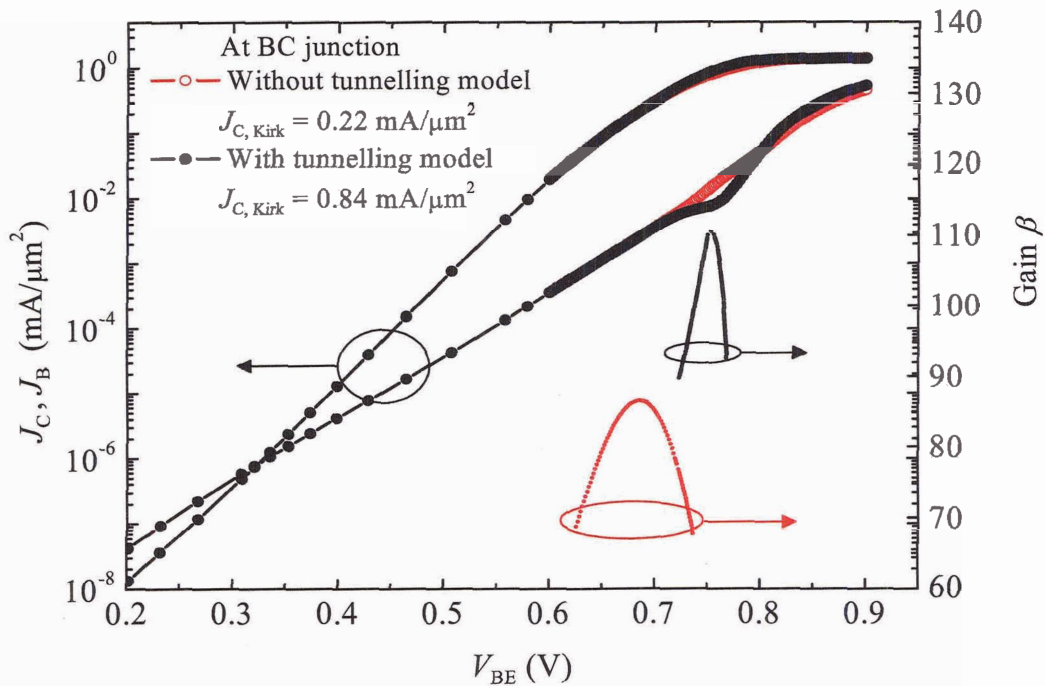


Figure 4-13: Simulated Gummel plots and current gains for #4451 with and without tunnelling model applied to the BC junction. A clear "knee" is visible in the base current for high biases when tunnelling is turned on in the simulations. The knee is an important feature of the measured characteristics.

1.5×10^{16} cm^{-3}. However, the experimentally measured Kirk current density is significantly higher at ~ 0.6 mA/μm^2 (see Fig.4-16), and thus closer to the Kirk current density of 0.84 mA/μm^2 predicted by the tunnelling model (see Fig.4-13).

As we mentioned in Chapter 2, the tunnelling model relies on the WKB approximation, which might overestimate the tunnelling current because it neglects quantum-mechanical reflection [71]. Although the implementation of tunnelling model is not quite calibrated to reproduce measured results, the simulation results demonstrate that the details of electron transport through the barrier on the base side of the BC junction play an important role in determining the experimentally observed Kirk effect threshold.

Table 4-1: ***Typical TLM measurement results: sheet resistance and specific contact resistance, for the base, emitter and collector***

Wafer	Emitter		Base		Collector	
	R_{sh} (Ω / □)	r_C (Ω cm^2)	R_{sh} (Ω / □)	r_C (Ω cm^2)	R_{sh} (Ω / □)	r_C (Ω cm^2)
#4451 ($N_A = 5\times10^{18}$)	24	3×10^{-7}	16000	2×10^{-5}	10	3×10^{-7}
#4450 ($N_A = 5\times10^{19}$)	24	3×10^{-7}	1300	1×10^{-6}	11	7×10^{-7}

4.3 Experimental Results

As shown by the previous simulations, the base seems to play a significant role in the Kirk effect of type-II GaAsSb/InP DHBTs. In this experiment, we measured wafers #4450 and #4451 which nominally have the same structure with the exception of widely different base doping levels in order to determine the role of base doping on the high-current limitations in GaAsSb/InP type-II DHBTs. The measured contact resistances for the emitter, base and collector contacts as determined from transmission line measurement (TLM) method are given in Table 4-1.

4.3.1 Comparison of AC and DC Measurements for Kirk Effects

Both AC [112, 113] and DC [39, 114] measurements can be used to characterize the Kirk effect in bipolar transistors. We used DC Gummel measurement to characterize the Kirk effect in the present work for the following reasons:

1. The original Kirk theory is based on a DC analysis as mentioned in the first Section. In the small-signal AC operation, high bias conditions not only cause the Kirk effect which increases the base transit time τ_B and base collector capacitance C_{jC}, but also cause other changes such as in the base emitter capacitance C_{jE} which cause f_T to begin its roll-off before the base-collector field drops to zero, as suggested in Fig. 4-1. Although it is widely recognized that the fallout of f_T is primarily due to Kirk effect, we believe DC characteristics parameterize the Kirk effect less ambiguously for our purposes.

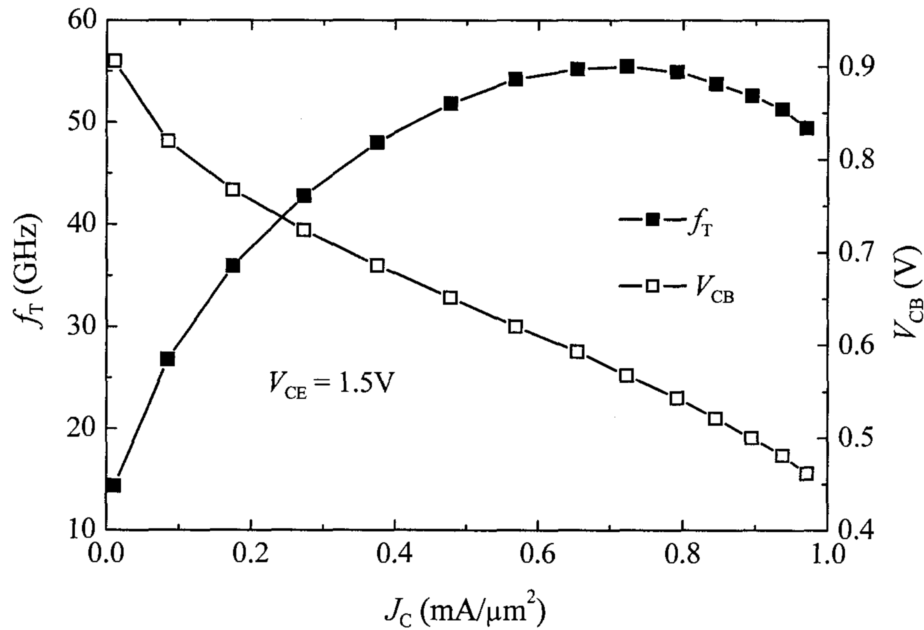


Figure 4-14: Measured cut-off frequency (solid squares) and base-collector potential (open squares) as a function of collector current density for #4451 in common emitter configuration with base current sweeping.

2. Our devices are not passivated, and we should try to minimize device degradation during measurements. Prolonged frequency sweeping during vector network analyzer measurements to determine the f_T vs. J_C characteristics will result in more severe electrical stresses to the devices than the short term bias sweeps involved in a DC measurement with a semiconductor parameter analyzer.

3. In our common emitter configuration for AC measurements, the base is biased by a current source, and the collector is biased at a fixed voltage. Hence, during the base current sweeping, V_{CB} changes as shown in Fig. 4-14. This arrangement does not allow one to maintain a fixed BC bias while increasing the collector current, thus providing an ambiguous characterization of high current effects.

4.3.2 Gummel Characteristics of #4451 and #4450

Due to the oscillation problems found in most RF devices built with narrow bases and air bridges, the measurements focused on a type of non-RF devices implemented

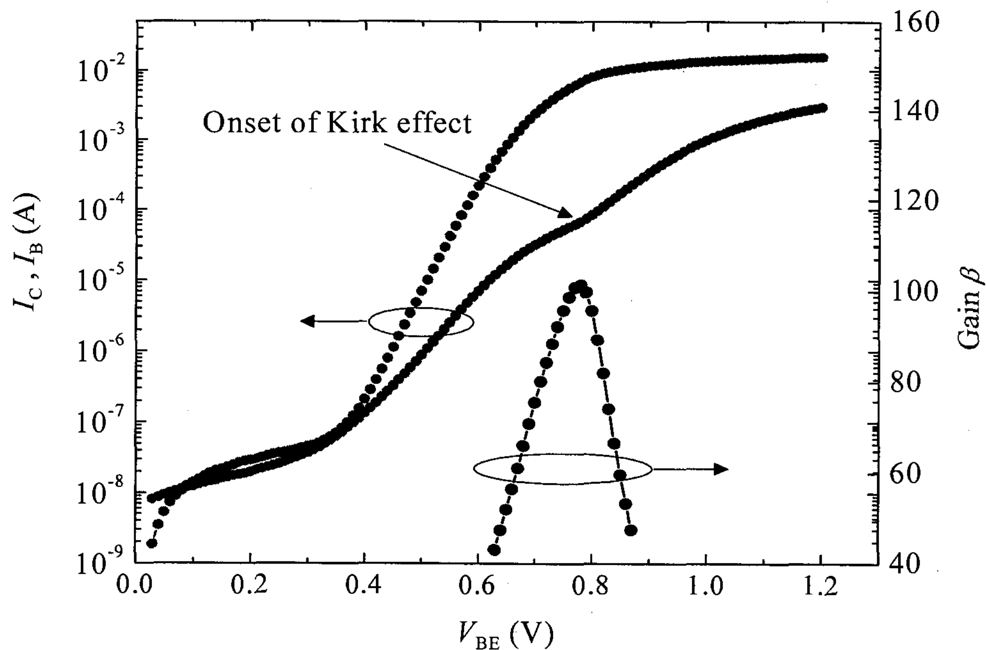


Figure 4-15: Measured Gummel plot of sample #4451 at V_{CB} = 0. An obvious "knee" in the base current coincides with the onset of the Kirk effect.

with large area base contacts and without air bridges: the large associated base capacitance suppresses RF oscillations in the measurement circuit. The nominal emitter contact size of these devices is 1×12 μm². A typical Gummel plot for #4451 is shown in Fig. 4-15, and the Kirk threshold current is located at the peak gain. To verify the effect of the base collector voltage on the Kirk effect, we measured Gummel characteristics at V_{CB} = 0 and 1 V. The current gain ranges from 80 to 100 for #4451 (lightly doped base), and from 15 to 20 for #4450 (heavily doped base). From the Gummel characteristics, we plotted the current gain versus collector current density for #4451 and #4450 as shown in Fig. 4-16. Fig. 4-17 shows the Kirk current density at V_{CB} = 0 and 1 V for all measured devices. Emitter contact dimensions were determined by SEM measurements as described in Chapter 3 in order to obtain reliable current density values.

When V_{CB} increases from 0 to 1 V, the Kirk current density increases in both samples. This trend seems to agree well with the classic formula (4-3). It is noted that the Kirk current density of #4451 is smaller than that of #4450 under both bias conditions.

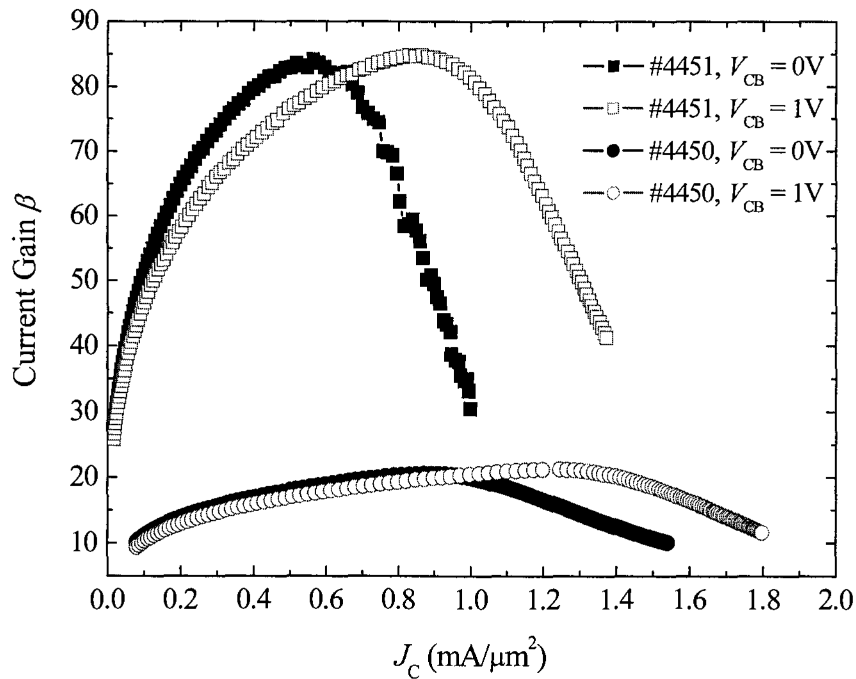


Figure 4-16: ***Measured current gain vs. collector current density for #4451 and #4450 at different V_{CB}. The emitter areas of #4451 and #4450 are 0.95×11.5 μm^2 and 0.88×11.5 μm^2 respectively.***

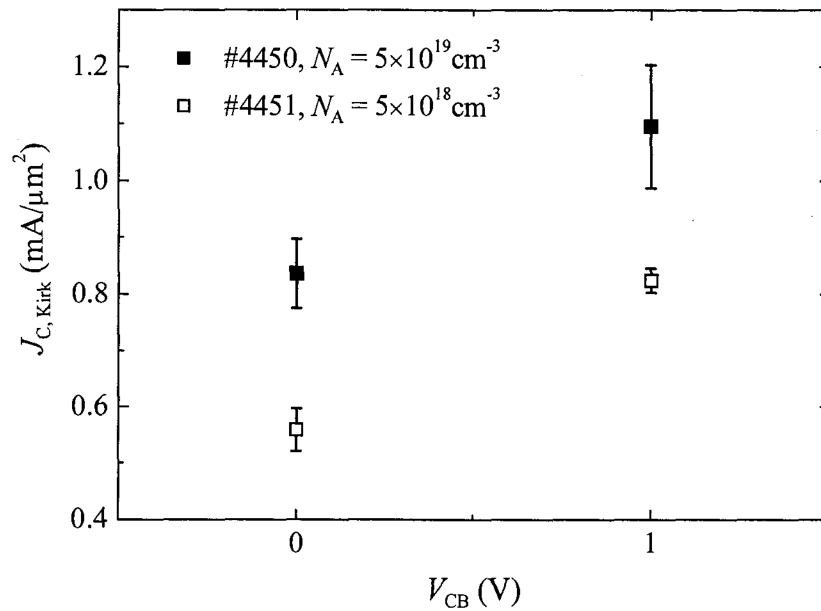


Figure 4-17: ***Measured Kirk current density for #4450 (solid squares) and #4451 (open squares) at two base collector biases. Standard deviation error bars are also displayed for 10 devices of #4450 and 8 devices of #4451.***

In other words, a heavier base doping level results in a higher the Kirk current density. This behaviour is markedly different than in the case of a BC homojunction where the base doping level does not directly affect the Kirk threshold density. The present observation has not yet been raised in the literature, and must be related to the band alignment in type-II GaAsSb/InP DHBTs.

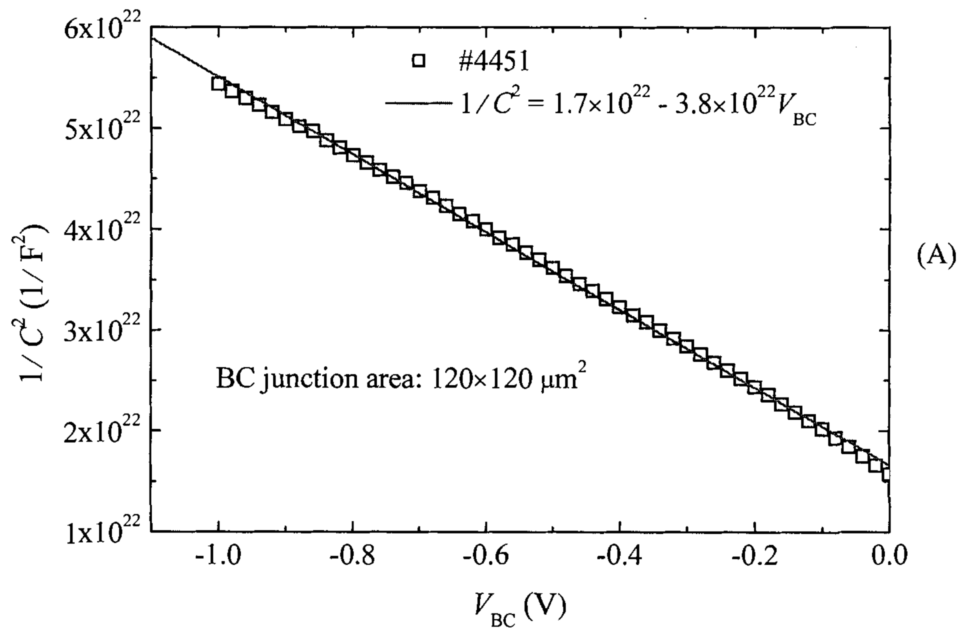
4.3.3 Other Factors Possibly Involved In the Difference of $J_{C,Kirk}$ Between #4451 and #4450

Although samples #4450 and #4451 were nominally grown to be identical with the exception of their base doping level, we must verify whether residual differences can safely be excluded as major causes for the difference in the $J_{C,Kirk}$ values we have measured. To verify the collector doping level, we carried out CV measurement for BC junctions of #4450 and #4451, and the results are shown in Fig. 4-18. The dependence of the capacitance C with the bias voltage V is given by [55]:

$$\frac{1}{C^2} = \frac{2}{S^2 q\varepsilon \cdot N_C}(\varphi_{CB} - V), \tag{4-4}$$

where S is the BC junction area, ε is the dielectric constant of the collector, and N_C is the collector doping level. Since the base doping level is much higher than the collector doping density, the base doping level does not affect our C-V measurements, as expected in one-sided junctions. The good linearity of measured curves of $1/C^2$ vs. V indicates that the doping is uniform in the collector. Fitting the data according to Equation (4-4), we obtain N_C = 1.54×10^{16} cm^{-3} and 1.42×10^{16} cm^{-3}, and φ_{CB} = 0.63 eV and 0.45 eV for #4450 and #4451 respectively.

According to the conventional formula of Kirk current density (4-3), any change of N_C and φ_{CB} will affect the Kirk current. If we insert the measured N_C and φ_{CB} into (4-3), and assume that υ is the saturation velocity 1×10^7 cm/s, and X_C is as measured 0.55 μm, we can obtain a relative difference in Kirk current density between #4451 and #4450 of about 11%. If we take into account the current spreading in collector [113, 115], the Kirk current density will be modified by a factor of η and given as $\eta \cdot J_{C,Kirk}$, where $J_{C,Kirk}$



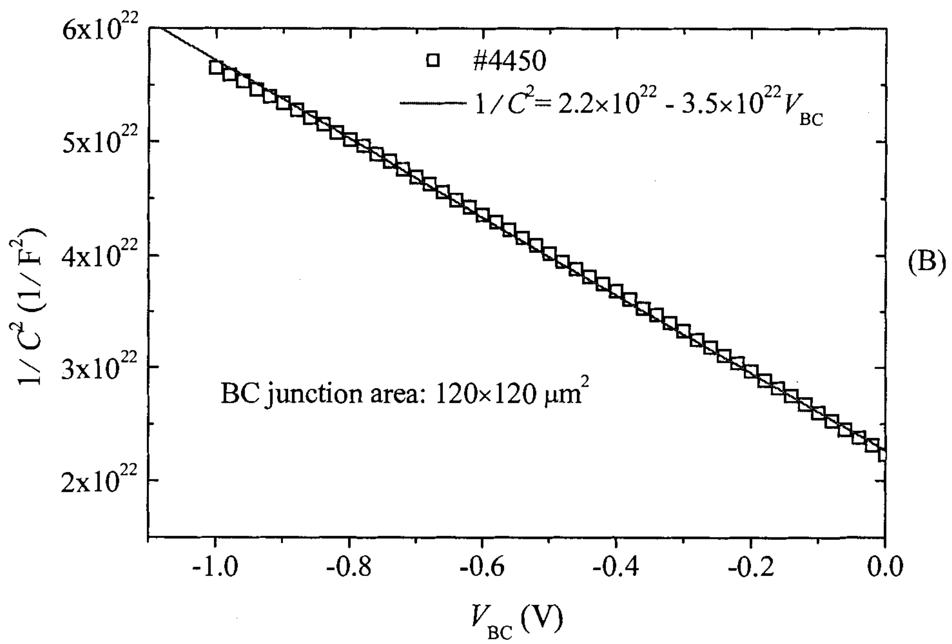


Figure 4-18: C-V measurement results for the BC junctions of #4451(A) and #4450 (B).

is given by (4-3). The factor η is emitter size dependent. According to [113], and using the measured sizes of #4451 and #4450 (measured as 0.95×11.5 μm^2 and 0.88×11.5 μm^2 respectively), we find that the difference of η between #4451 and #4450 is only about 2%, which can be safely ignored in the present context.

It should now be noted that (4-3) still does not take into account the contact resistance and extrinsic base resistance. From the measurement point of view, (4-3) should be modified as [114]:

$$J_{CK} = v\left(qN_C + \frac{2\varepsilon\left(V_{CB} + \varphi_{CB} - R_C I_{CK} + R_B I_B\right)}{X_C^2}\right), \tag{4-5}$$

where V_{CB} is the external base collector voltage, R_C is the collector contact resistance plus sub-collector resistance, R_B is the base contact resistance plus extrinsic base resistance. For simplicity, here we do not consider the effect of current spreading. In (4-5) we have $I_{CK} = A_E J_{CK} = \beta \cdot I_B$ where A_E is the emitter area, and β is the current gain. Solving (4-5), we have

$$J_{CK} = \frac{J_{CK0}}{\delta} = \frac{v\left(qN_C + \dfrac{2\varepsilon\left(V_{CB} + \varphi_{CB}\right)}{X_C^2}\right)}{1 + \dfrac{2\varepsilon v \cdot A_E\left(\beta \cdot R_C - R_B\right)}{\beta \cdot X_C^2}}, \tag{4-6}$$

where J_{CK0} is the same as (4-3), and δ is an error factor due to Ohmic losses. With the measured emitter areas, contact resistances, and current gains (see Fig. 4-16 and Table 4-2), we obtain δ values of 1.010 and 1.008 for #4450 and #4451 respectively. The change in δ is negligibly small between the two samples: although the base resistance in #4451 is large, its current gain is also large and, importantly, the measured device size is quite small. Therefore, the extrinsic resistances do not play a significant role in the observed differences in Kirk effect current densities.

The above considerations indicate that the base doping level in GaAsSb/InP DHBTs plays, perhaps surprisingly, an important role in determining the practical

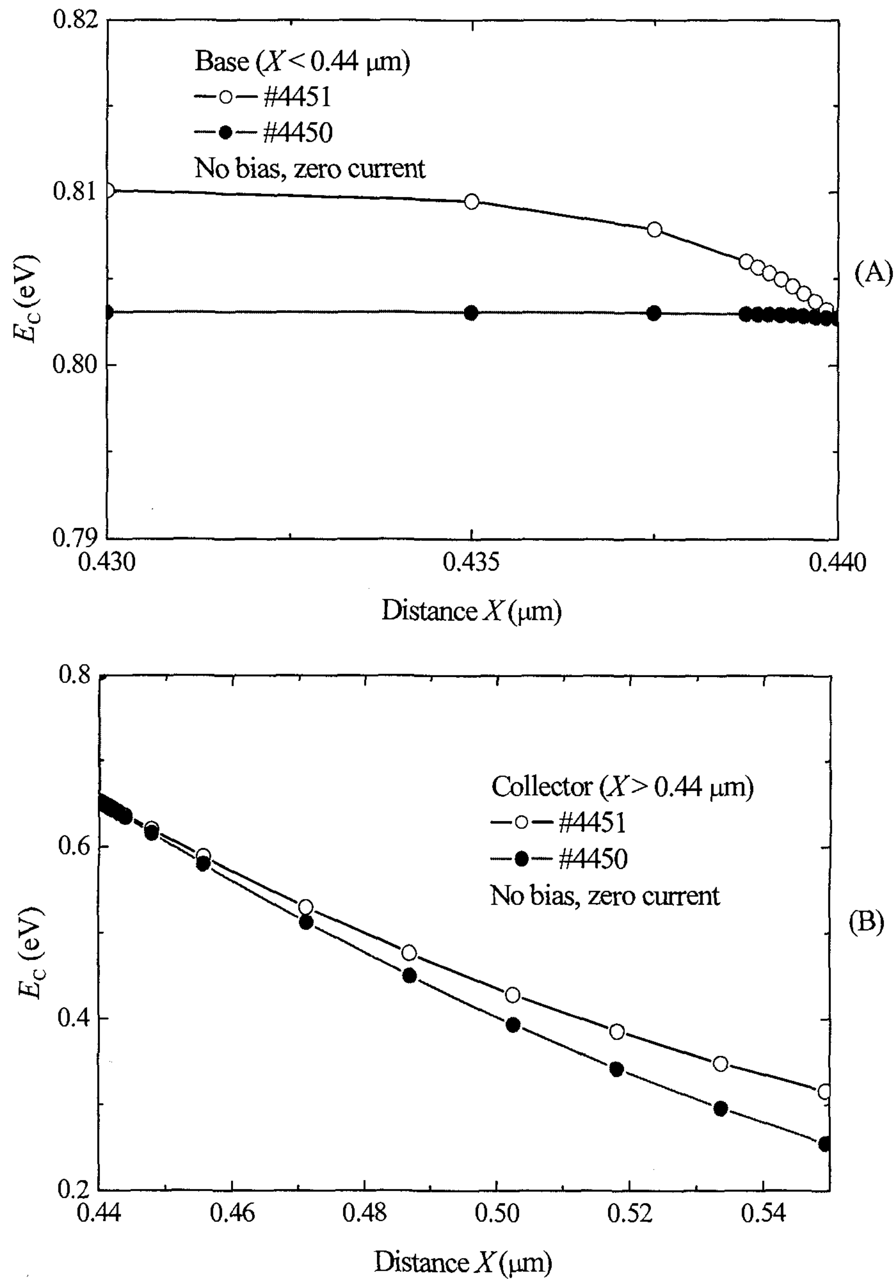


Figure 4-19: Simulated conduction bands around BC junction for the structures of #4451 (open circles) and #4450 (solid circles) at zero current. (A) is on the base side and (B) is on the collector side of the junction.

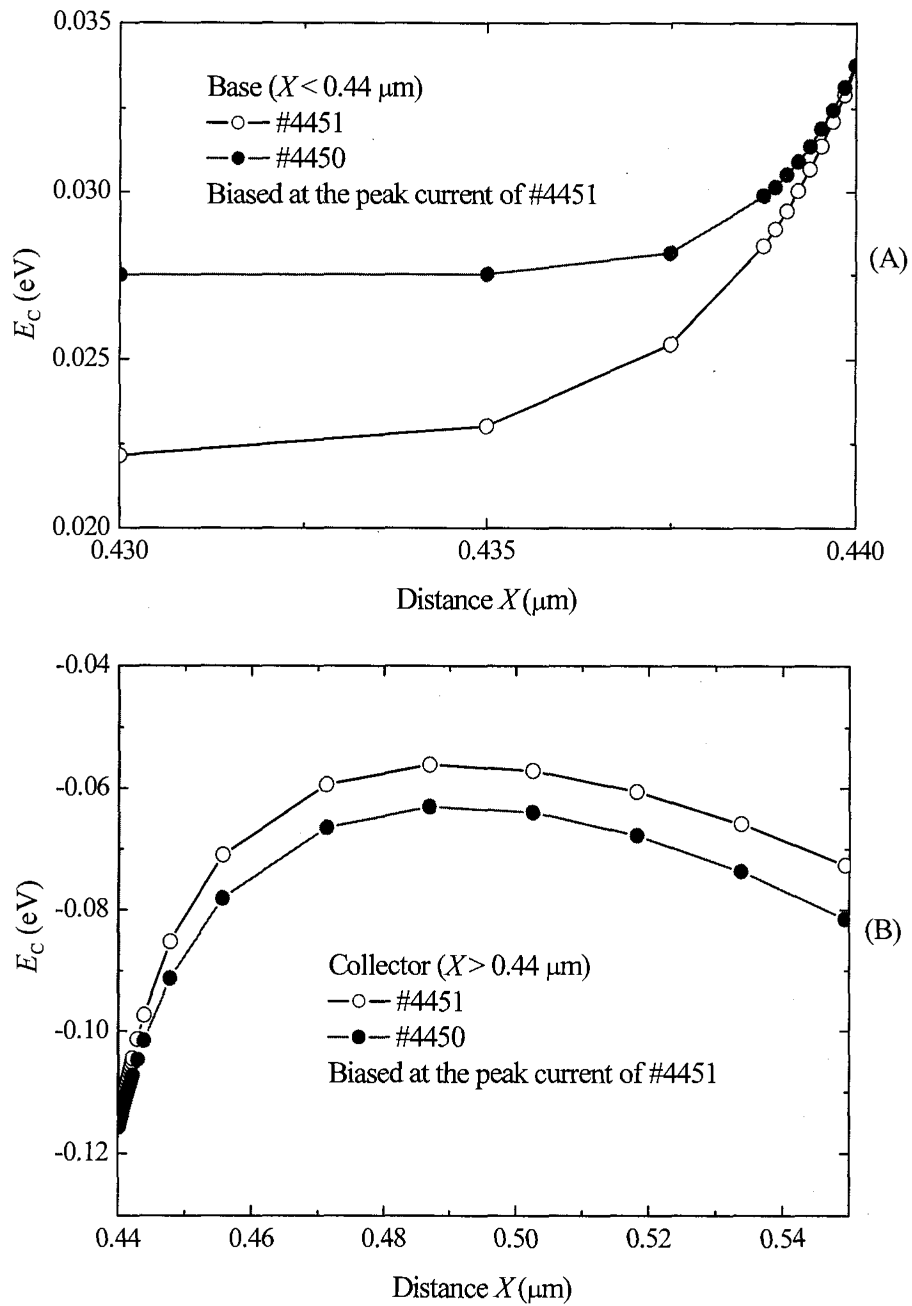


Figure 4-20: Simulated conduction bands around BC junction for the structures of #4451 and #4450 at the peak current of #4451. (A) is on the base side and (B) is on the collector side of the junction.

high-current Kirk effect limitations of transistors: type-II GaAsSb/InP DHBTs therefore effectively display a unique "*base-controlled Kirk effect*". The effect is counter-intuitive to those habituated to the classical Kirk effect described in the literature because the latter only depends on properties of the collector.

4.4 Base Controlled Kirk Effect

We have experimentally shown that when the base doping level is increased by one order of magnitude, the Kirk current density increases by nearly 50%. To understand this phenomenon, we performed simulations for layer structures #4450 and #4451 which include tunnelling transport at the BC junction. Fig. 4-19 shows the conduction band edges around BC junctions in thermal equilibrium. On the collector side, the conduction band edge of #4450 features a stronger bending than that of #4451, which means the built-in voltage φ_{CB} of #4450 is higher than that of #4451. We return to this point later. The band profile for #4451 also shows evidence of significant base depletion due to the lower base doping level.

Fig. 4-20 shows the conduction band edges at the Kirk collector current of #4451 with V_{CB} = 0 V. We can see that the conduction band of #4451 changes much more than that of #4450 on the base side (see Fig. 4-19A and Fig. 4-20A). In other words, the induced electron barrier at the base side in #4451 develops faster than the one in #4450. It is also noted that on the collector side, the conduction band edge of #4451 is always above the one of #4450, however, their difference becomes much smaller at the bias condition than the one in thermal equilibrium (see Fig. 4-19B and Fig. 4-20B). This indicates that the impediment to the electron transport at the collector side tends to be the same at high injection levels for #4451 and #4450. From the development of the electron barrier shown in Fig. 4-20, one can observe that the onset of Kirk effect in #4450 will come later (i.e., at higher current densities) than the one in #4451. In this particular simulation, the Kirk current of #4450 is about 30% higher than that of #4451, which is less than what was observed experimentally (50%). The reason for this discrepancy may be as follows: As discussed in Section 4-2 (see Fig. 4-13), the calculated peak current is higher than the measured one using the built-in tunnelling model in ISE TCAD v. 7,

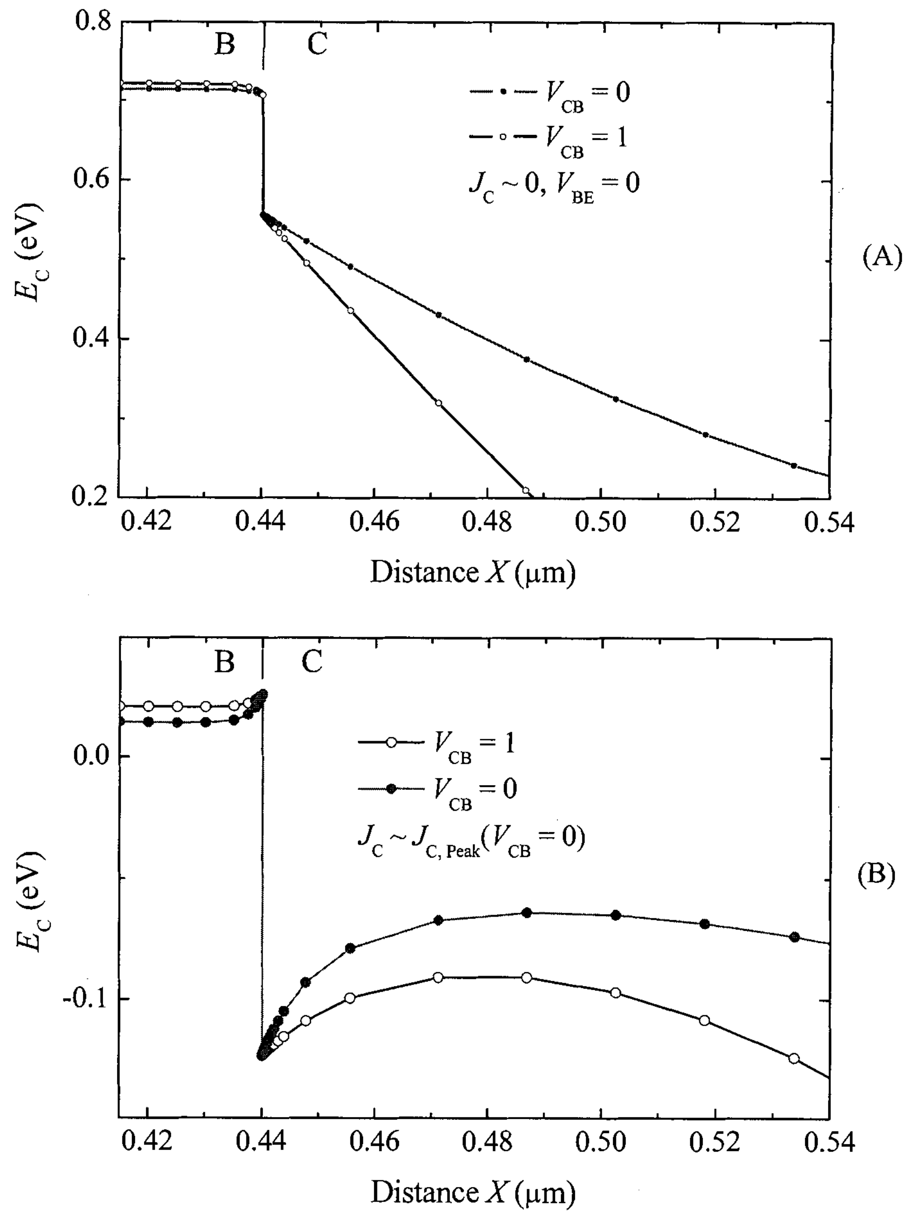


Figure 4-21: Simulated conduction bands around BC junction for the structures of #4451 at different base collector biases: $V_{CB} = 1$ V (open circles) and $V_{CB} = 0$ (solid circles). (A): No injection, $J_C = 0$; (B): J_C equals the Kirk current density in the case of $V_{CB} = 0$.

because the WKB approximation implemented in this model probably overestimates the tunnelling process. The significance of this overestimation may increase with increasing barrier height and width, because proportionally more carrier reflections are ignored for a larger barrier. Accordingly, the calculated peak current for #4451 which has a larger barrier than #4450 (see Fig. 4-20A) is too high, and as a result, the difference of the calculated peak current between #4451 and #4450 is smaller than we expected.

The fact that Kirk current increases with the reverse bias for the BC junction V_{CB}, can be explained by Fig. 4-21, which shows the comparison of the conduction band edge in #4451 between V_{CB} = 0 and V_{CB} = 1 V at the same injection current. When the injection is $J_C = 0$ (see Fig. 4-21A), the reverse bias (V_{CB} = 1 V) dramatically pulls down the band edge at the collector side and pull up the band edge at the base side, compared to the band edge at V_{CB} = 0 V. Therefore, when the collector current increases to high levels, the electron barrier at V_{CB} = 1 V will evolve later than when V_{CB} = 0 V. As shown in Fig. 4-21B, the induced electron barrier at V_{CB} = 1 V is significantly suppressed at a injection level of the Kirk current at V_{CB} = 0 V, so that the onset of the Kirk effect is delayed with respect to that at V_{CB} = 0 V.

Based on the above simulation results, we now conclusively describe the occurrence of high injection effects in type-II GaAsSb/InP DHBTs as follows. First, if we assume there is no interface charge, the electric flux density $D = \varepsilon \cdot E$ is continuous at the BC metallurgical junction, and for simplicity, the small difference of the dielectric constant ε between the base and collector can be ignored, i.e. ε(GaAsSb) $\approx$ ε(InP). Therefore, the electric field, which is proportional to the slope of the conduction band edge, e.g., $E = \frac{1}{q}\frac{dE_C}{dx}$, is continuous at the BC junction. As shown in Fig. 4-22, the base and collector are at $x < 0$ and $x > 0$ respectively, and line "b-c" represents the local slope of the conduction band edge at the BC junction ($x = 0$). Then, the electric field at the BC junction can be represented by the angle (θ) made by line "b-c" with the x-axis. At zero injection (see Fig. 4-22A), the electric field at $x = 0$ is negative so that $\theta = -\theta_0$. As the injection increases, line "b-c" rotates counter-clockwise, and when the injection level is so high that the electric field decreases to zero (see Fig. 4-22B), the line "b-c" is parallel

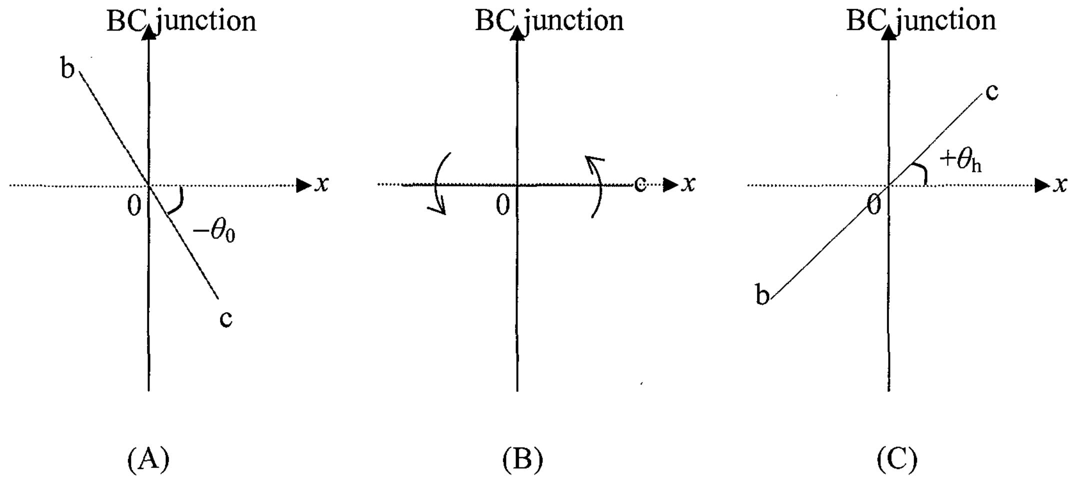


Figure 4-22: Illustrations of the development of the Kirk effect in type-II GaAsSb/InP DHBTs. bc line represents the local slope of the conduction band and the angle with respect to x axis represents the electric field at the BC junction.(A): At zero injection, the electric field is negative represented by $-\theta_0$; (B): at a certain injection level, the electric field collapses to zero and θ=0; (C): at a very high current level, the electric field becomes positive presented by $+\theta_h$.

with the x-axis so that $\theta = 0$. Line "b-c" continues to rotate with increasing injection levels. Meanwhile, the local BC junction electric field becomes inverted ($\theta = +\theta_h$), giving rise to an electron barrier in the base — as we have seen, electrons still tunnel through the barrier. When the injection level reaches a certain threshold current ($\theta = +\theta_{Kirk}$), electron blocking becomes strong enough to result in a severe drop in transistor performance. It is noted that the θ_0 in #4450 is greater than that in #4451.

Both experimental and simulated results have shown that high current levels bring on electric field reversal at the BC junction, and that the resulting electron barrier in the lightly doped base (#4451) is higher than that in the heavily doped base (#4450). Effectively, one can postpone the onset of the Kirk effect in type-II GaAsSb/InP DHBTs by increasing the built-in voltage (or equivalently, the electric field under thermal equilibrium) so as to delay the local field reversal at the BC junction.

4.5 Conclusions

We have compared the Kirk effect in type-II GaAsSb/InP DHBTs with that in AlGaAs/GaAs SHBTs using TCAD simulation. We have found that for type-II GaAsSb/InP BC heterojunctions, no classical base pushout occurs at high injection levels but instead, hole accumulation occurs on the base side, and the electric field is eventually locally reversed around the BC junction. The simulated energy band diagram shows that an induced electron barrier evolves in the base, and becomes significant (i.e., increasingly opaque to electrons) as the injection level increases. Simulations including thermionic-field emission applied to the BC junctions showed that the tunnelling process plays an important role in the Kirk effect of GaAsSb/InP DHBTs.

Devices with two different base doping levels were experimentally characterized in terms of their high-current properties: it was found that the Kirk effect in devices with a low base doping level occurs at lower current densities than in high base doping devices. The reason for this base controlled Kirk effect is that the induced electron barrier in the lightly doped base grows faster than in the heavily doped base. In this sense, type-II GaAsSb/InP DHBTs feature Kirk effect characteristics that are dependent on the base layer properties, in clear contrast to the more common situation in homojunction collectors.

Chapter 5:

Design and Optimization for GaAsSb-based DHBTs

5.1 Overview

This Chapter focuses on structure optimization and the maximization of device performance in type-II GaAsSb-based DHBTs. This work is required to support the development of devices with a higher DC current gain (β), higher current gain cut-off (f_T) and maximum oscillation (f_{max}) frequencies, while simultaneously maintaining a high breakdown voltage.

Vertically scaling the base and collector in HBTs is a common approach to decrease the base and collector transit times, τ_B and τ_C, so that the overall transistor delay time τ_{EC} decreases. The expressions of τ_B, τ_C, and τ_{EC} are given as in (2-27), and are repeated here:

$$\tau_B = \frac{X_B^2}{\gamma \cdot D_{nB}} + \frac{X_B}{v_{BC}},\ \tau_C = \frac{X_C}{2v_C},\ \text{and}\ \tau_{EC} = \tau_B + \tau_C + (R_E + R_C)\cdot C_{jC} + \frac{nkT}{qI_C}\cdot(C_{jE} + C_{jC}).$$

Decreasing the base thickness X_B may increase f_T, but it will eventually degrade f_{max} because of the resulting increase in base sheet resistance while the base conductivity cannot be increased indefinitely by higher doping. On the other hand, an extremely thin GaAsSb base will cause difficulties in the device fabrication with current processing techniques. The fabrication of the devices with base thicknesses of $150 - 200$ Å has been

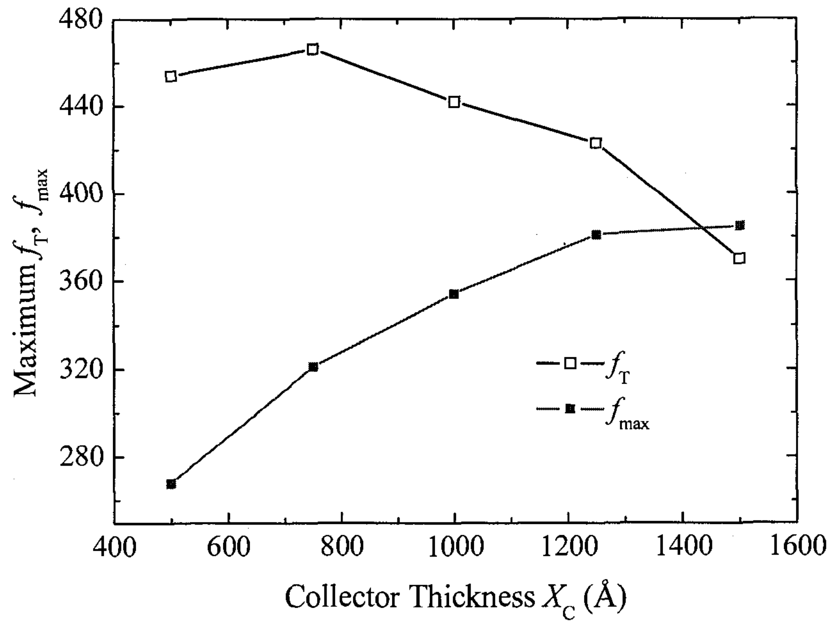


Figure 5-1: ***Simulated maximum f_T and f_{max}, as functions of the collector thickness X_C for InP/GaAsSb/InP DHBTs. The collector and base doping levels are $N_D = 2\times10^{16}$ and $N_A = 1\times10^{20}$ cm^{-3}, respectively.***

shown to be well-controlled, and simultaneously high f_T and f_{max} values have been obtained [3, 8].

Continuously reducing the collector thickness does not always improve f_T, because the collector capacitance C_{jC} increases with decreasing space charge thickness, thus cancelling some of the speed improvement associated with the reduction of the electron signal delay time τ_C. Fig. 5-1 shows f_T and f_{max} as a function of collector thickness for InP/GaAsSb/InP DHBTs. We can see that f_T no longer increases when the collector thickness is less than about 750 Å, while f_{max} continuously decreases with collector thickness, indicating that the BC capacitance is a dominant controlling factor for f_{max}. As well, decreasing the collector thickness will directly reduce the device breakdown voltage BV_{CEO} [82]. The present design work will show that a good value for collector thickness should be 750 1000 Å.

As mentioned in Chapter 2, scaling the lateral dimensions decreases the device junction areas and the junction capacitances to improve the high frequency performances.

Based on the state-of-the-art fabrication techniques in place in academic laboratories [17, 47], we use an emitter width W_E / 2 = 0.2 μm, an emitter undercut W_{BE} = 0.1 μm, and a base contact width W_B = 0.3 μm, as typical lateral dimensions (see Fig. 2-4). In the last Section of this Chapter, we further re-examine the question of optimal lateral dimensions.

In this Chapter, we investigate the influences of various emitter, base, and collector structures on DC and RF performances by performing 2D simulations based on the framework we previously built. Sections 5.2, 5.3, and 5.4 examine the emitter, base, and collector designs, respectively. In the last Section, we further refine the device structure that incorporates all of the design improvements in an attempt to predict the highest achievable performances for GaAsSb-based type-II DHBTs.

5.2 Emitter Design

5.2.1 InAlAs and InP Emitters

In Chapter 2, we discussed the impact of the type-II conduction band offset ΔE_C on the RF performances of InP/GaAsSb/InP DHBTs. From the viewpoint of carrier injection, ΔE_C acts as a barrier to the electron transport from the emitter to base layer. Therefore, decreasing ΔE_C will benefit f_T and f_{max}, as shown in Fig. 2-17. By using $In_{0.52}Al_{0.48}As$ as the emitter material, the above mentioned barrier can be eliminated since the InAlAs/GaAsSb heterojunction features a weak type-I band alignment [102]. In addition, InAlAs/GaAsSb/InP DHBTs may exhibit a lower surface recombination current than InP/GaAsSb/InP DHBTs, as already discussed in detail in Chapter 3. A disadvantage of using InAlAs is the reduced electron mobility which is much lower than that of InP, e.g., μ_{InAlAs} ~ 39% μ_{InP} at a doping level of 3×10^{17} cm^{-3} [66]. The issue of emitter resistance becomes important with continued scaling of the emitter contact, as discussed in the following sub-section.

InAlAs has long been used as an alternative to the InP emitter in InGaAs-based HBTs [44, 116, 117]. Recently, some results on the epi-layer growth and DC characteristics of InAlAs/GaAsSb/InP DHBTs were reported [9, 118], but detailed

performance comparisons with InP/GaAsSb/InP DHBTs designs have not yet been reported.

5.2.2 Emitter Resistance

The emitter resistance R_E consists of the metal contact resistance R_{CE} and the epi-layer resistance $R_{E,Epi}$. $R_{E,Epi}$ arises from two contributions: the heavily doped cap layer under the metal, and the undepleted lightly doped emitter layer (Fig. 2-6). The resistivity of the heavily doped cap layer is estimated to be about 0.43×10^{-8} Ωcm^2, assuming that the cap layer consists of 0.1 μm InGaAs, doped to 1×10^{19} cm^{-3}, and 0.05 μm InP, doped to 3×10^{19} cm^{-3}, and that their mobilities are in accordance with the Arora model (Table 2-1).

For the lightly doped emitter layer (hereafter: the emitter layer), the situation is complicated: the depletion width depends on the forward BE bias, and the depletion region due to Fermi level pinning on the emitter sidewall also should be taken into account in determining the cross-section available for conduction. As described in Chapter 2, for InP and InAlAs emitters doped to 3×10^{17} cm^{-3}, the surface depletion widths due to Fermi level pinning are around 0.02 and 0.04 μm respectively, which amount to a considerable fraction of the 0.2 μm emitter width. With increasing the forward BE biases the sidewall (vertical) edge depletion width becomes smaller, and the non-depleted emitter thickness becomes larger. The resistance of this non-depleted emitter material contributes to R_E. Therefore, when the emitter thickness is close to the depletion width at high BE biases, no extra non-depletion resistance arises from the emitter layer. Fig. 5-2 shows f_T and f_{max} as a function of the emitter thickness X_E at a doping level of 3×10^{17} cm^{-3} for both InAlAs and InP emitter DHBTs. We can see that both f_T and f_{max} increase with decreasing emitter thickness until $X_E \sim 150$ Å. When $X_E >$ 150 Å, the f_T of the InP-emitter device is higher than that of the InAlAs-emitter device. This is because the electron mobility of InP is higher than that of the InAlAs, and therefore, the undepleted emitter resistance in the InP-emitter is lower than that in the InAlAs-emitter. When $X_E < 150$ Å, the f_T is about the same for both InP and InAlAs emitter devices, since the resistance difference has been eliminated. Also, for $X_E < 350$ Å,

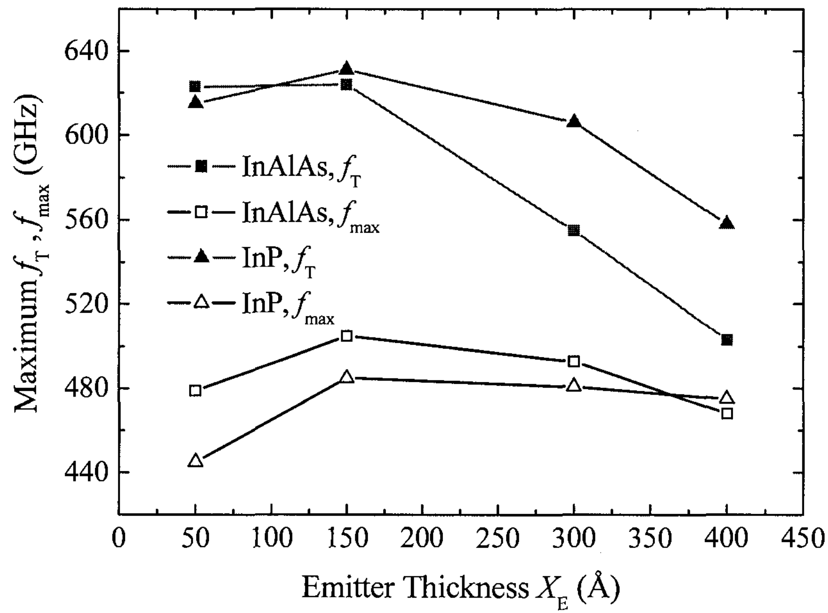


Figure 5-2: ***Simulated maximum f_T and f_{max} as a function of the emitter thickness for InAlAs/GaAsSb/InP and InP/GaAsSb/InP DHBTs. The emitter doping is 3×10^{17} cm^{-3}, the emitter contact resistivity r_{EC} is 4.6×10^{-8} Ωcm^2, and the emitter area is 0.2×11.5 μm^2.***

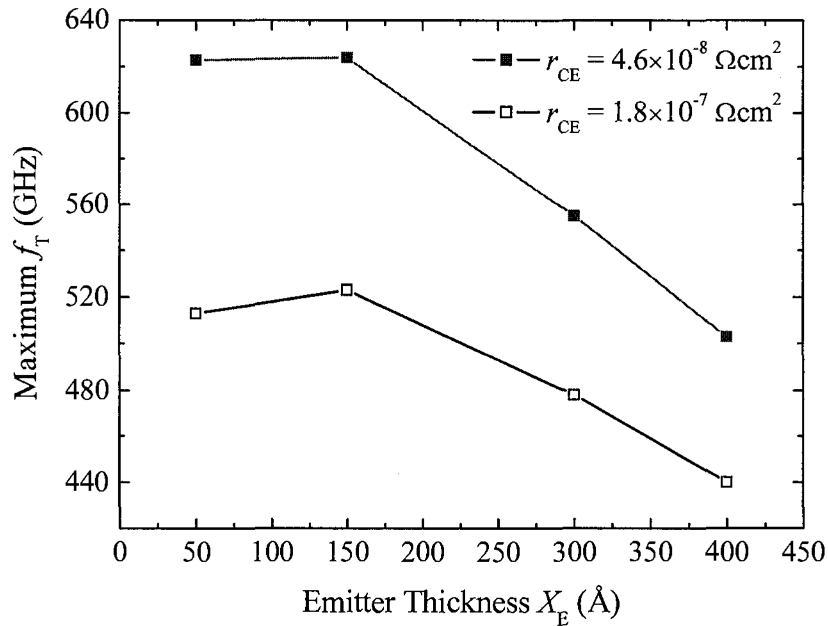


Figure 5-3: ***Simulated maximum f_T as a function of the InAlAs emitter thickness X_E with two emitter specific contact resistances.***

the f_{max} of the InAlAs-emitter device is higher than that of the InP-emitter device. Therefore, if the emitter thickness X_E is to be ~150 Å, the InAlAs-emitter offers a slight advantage over the InP-emitter.

The emitter specific contact resistance r_{CE} can be 2–3×10^{-7} Ωcm^2 in our fabrication process. However, others have reported [119, 120] r_{CE} to be as low as 4–5×10^{-8} Ωcm^2. Fig. 5-3 demonstrates that the emitter contact resistance has a great impact on the f_T. We also find that the difference in f_T caused by the change in contact resistances is larger at X_E = 150 Å than that at X_E = 400 Å. This again illustrates the effect of the undepleted emitter resistance on the total emitter resistance R_E as the emitter thickness X_E increases from 150 to 400 Å.

Compared to the contact resistance, the cap layer resistance is much smaller. Fig. 5-4 shows the f_T and f_{max} vs. BE bias for devices with two emitter cap layer thicknesses. Even when the emitter cap layer thickness $X_{E,Cap}$ decreases by more than 40%, the f_T and f_{max} show little change. The cap layer thickness does not have a great influence on performance. From a physical point of view, it is primarily set by process architecture concerns such as undercutting during wet etching steps and metal thicknesses in self-aligned contacts.

5.2.3 Emitter Doping

The doping level in the emitter cap layer should be as high as possible to reduce the contact resistance and epi-layer resistance. The impact of the doping level in the emitter layer on the device performance depends on the emitter layer thickness. Fig. 5-5 shows the maximum DC current gain as a function of the emitter thickness for two emitter doping levels. When the doping level increases (or the thickness decreases), the current gain decreases. The impact of the thickness on the gain seems to be more significant. Fig. 5-6 shows the current gain as a function of the collector current for the devices with two emitter thicknesses. The gain of the device with a 400 Å emitter is higher than with a 150 Å emitter, and the difference is even larger at low current levels. Fig. 5-6 indicates that the surface recombination current might also play an important role. A thinner emitter layer or a higher doping level can reduce the depletion area near

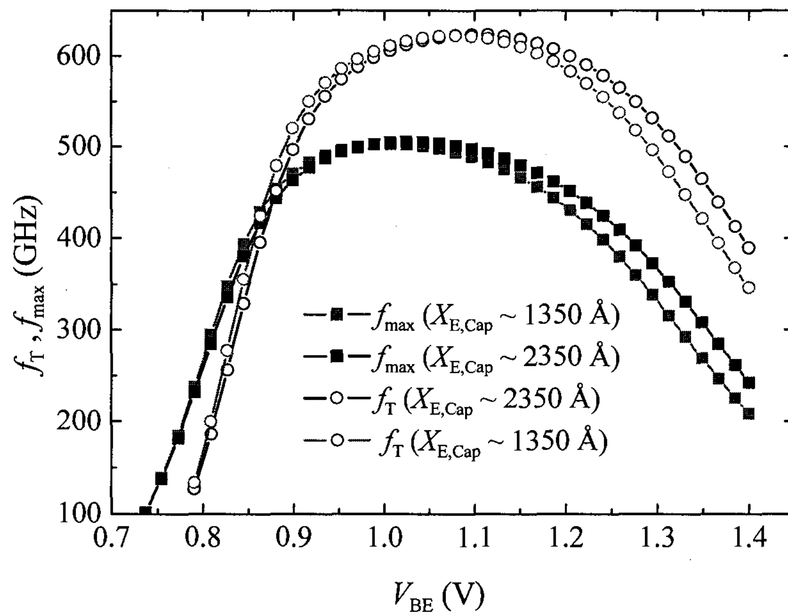


Figure 5-4: ***Simulated f_T and f_{max} as a function of the BE bias for InAlAs/GaAsSb/InP DHBTs with different emitter cap layer thicknesses. The emitter layer thickness is 150 Å.***

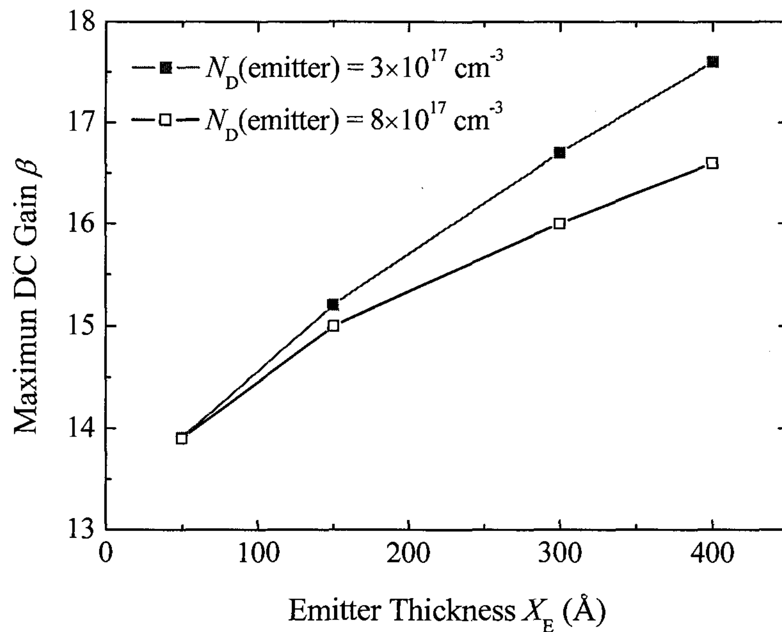


Figure 5-5: ***Simulated maximum DC current gain as a function of the InAlAs emitter thickness X_E with two emitter doping levels. The emitter area is 0.2×11.5 μm^2.***

the emitter sidewall, and as a result, the electron injection from the emitter onto the extrinsic base surface might increase. Fig. 5-7 shows the maximum f_T and f_{max} as a function of the doping level in the emitter layer for two emitter thicknesses. For the thin emitter (X_E = 150 Å), the doping level has almost no impact on the f_T and f_{max}, and for the thick emitter (X_E = 400 Å), the higher doping level gives rise to significantly higher f_T and f_{max}. The explanation for this could be that the resistance of the undepleted area in the thick emitter decreases with increasing doping levels, and hence, both f_T and f_{max} increase.

5.3 Base Design

The electron minority carrier mobility in p-type $Ga_{0.51}As_{0.49}Sb$ bases is recognized to be significantly lower than that in $In_{0.53}Ga_{0.47}As$ [67, 121]. In Chapter 2 it was estimated to be about one-third of that in $In_{0.53}Ga_{0.47}As$, at a p-doping level of 4×10^{19} cm^{-3}. To overcome this disadvantage of GaAsSb and to minimize the base transit time, we need to employ base grading schemes, which have also been widely used for other types of HBTs [122-124]. InP/(In)GaAsSb DHBTs, with a quaternary indium-graded InGaAsSb base have been experimentally demonstrated to have excellent RF performances [17]. Aluminum-graded (Al)GaAsSb bases, which may be advantageous over the indium-graded base because they can be grown without serious strain limitations, were first proposed by Bolognesi *et al.* [125], but have not yet been reported. In this work, we first examine the effect of the grading schemes on the GaAsSb-based DHBTs using 2D numerical simulations.

The purpose of base grading is to establish an electric (or quasi-electric) field to aid electron transport across the base, and thus decrease the base transit time. If we ignore base recombination and invoke current continuity, the collector current consists of both the diffusion and drift components in the base in the presence of electric field, and is given as:

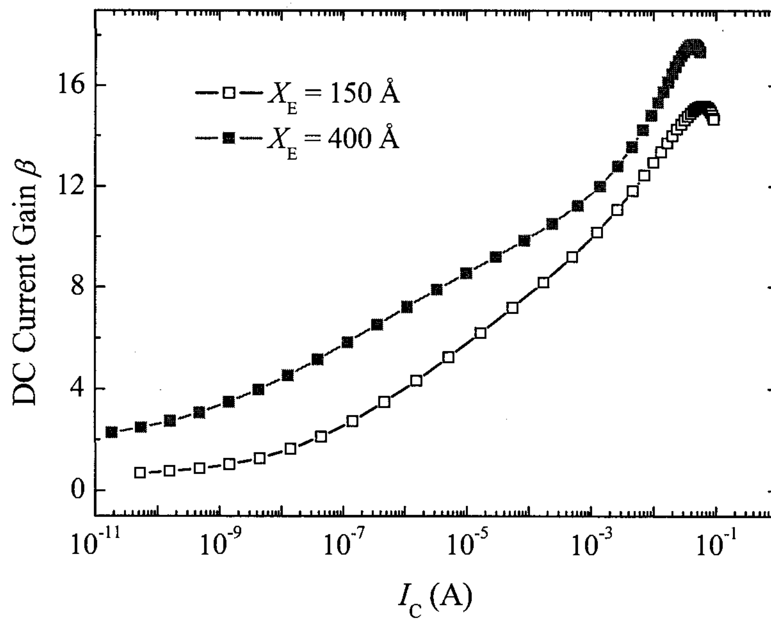


Figure 5-6: ***Simulated current gain as a function of collector current for InAlAs/GaAsSb/InP DHBTs with emitter layer thickness of 150 Å (open squares) and 400Å (solid squares). The emitter doping level is $3\times10^{17}cm^{-3}$.***

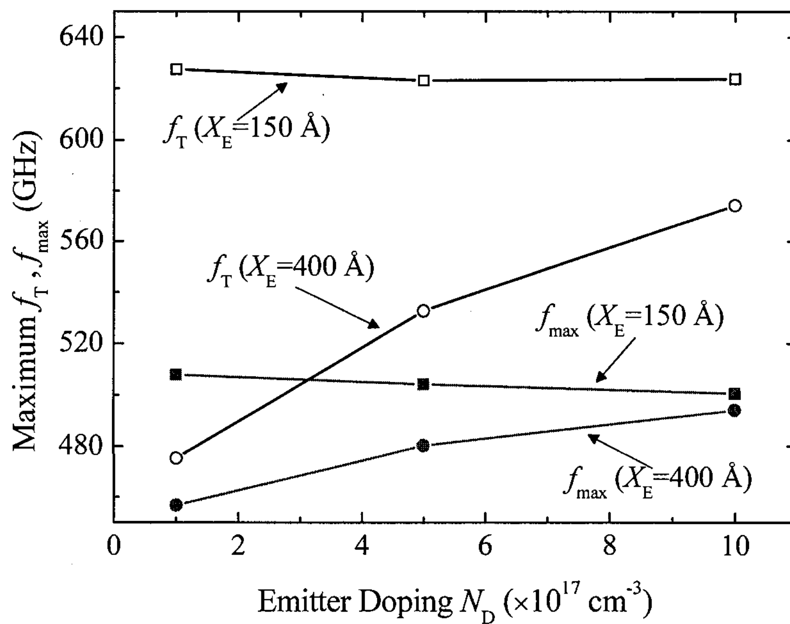


Figure 5-7: ***Calculated maximum f_T and f_{max} as a function of the emitter doping level N_D for InAlAs/GaAsSb/InP DHBTs with two emitter layer thicknesses.***

$$J_C = qD_{nB}\frac{dn(x)}{dx} + q\mu_{nB}n(x)E_B, \qquad (5\text{-}1)$$

where D_{nB} is the electron diffusivity, μ_{nB} is the electron mobility, $n(x)$ is the electron density, and E_B is the total electric field due to the base grading. Assuming that the electron density is negligible at the BC junction, the electron transit time can be obtained according to (5-1): $\tau_B = \frac{X_B^2}{\gamma \cdot 2D_{nB}}$ [81], where X_B is the base thickness and γ is an E_B-dependent coefficient, and $\gamma \geq 1$. In the absence of an electric field in the base, $\gamma = 1$. Two grading approaches are possible: base compositional grading, and the grading of the base doping profile. The two options are discussed in the following Sections.

5.3.1 Compositionally Graded Base

The energy band gap in a compound semiconductor can be tuned by adjusting the composition of the alloy. This technique is well known, and is often referred to as "band-gap engineering." The band gap of an alloy is usually assumed to change linearly with the composition, in the first order [126]. If we linearly grade the band gap through the base from the BE junction to the BC junction, the established field (which is also called a "quasi-electric field") is given by: $E_B = \frac{\Delta E_{gB}}{qX_B}$, where ΔE_{gB} is the band gap change across the base (from the BE to BC junction), and X_B is the base thickness. Fig. 5-8 shows an example of the equilibrium band diagram of an InP/GaAsSb/InP DHBT with a linearly graded base. Note that the slope of the conduction band edge in Fig. 5-8 is proportional to the magnitude of the quasi-electric field.

One simple method of grading $GaAs_{1-x}Sb_x$ is to change the composition x. This method, however, causes strain in the graded base since the lattice-matched composition to InP is x = 0.49. To maintain an InP-lattice matched base, indium or aluminium can be added to GaAsSb to make quaternary alloys: $Ga_xIn_{1-x}As_{1-y}Sb_y$ and $Al_xGa_{1-x}As_{1-y}Sb_y$. Fig. 5-9 shows the band gap vs. lattice constant for the alloys of interest. The vertical solid lines represent the InP-lattice matched alloys: $(Ga_{0.47}In_{0.53}As)_z(GaAs_{0.51}Sb_{0.49})_{1-z}$ [127] (red short line) and $Al_xGa_{1-x}As_{0.51}Sb_{0.49}$ [128] (long blue line). We can determine that

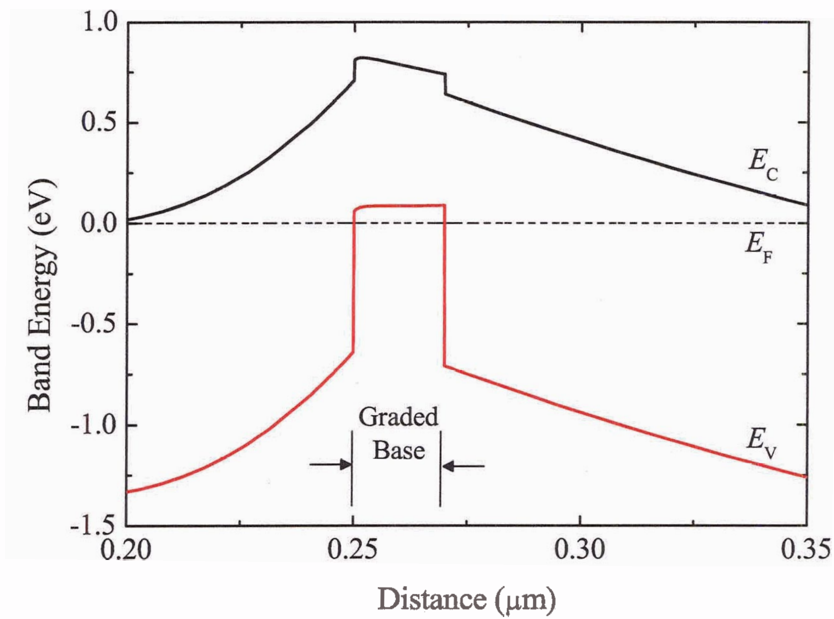


Figure 5-8: ***The equilibrium band diagram of an InP/GaAsSb/InP DHBT with a compositionally graded base.***

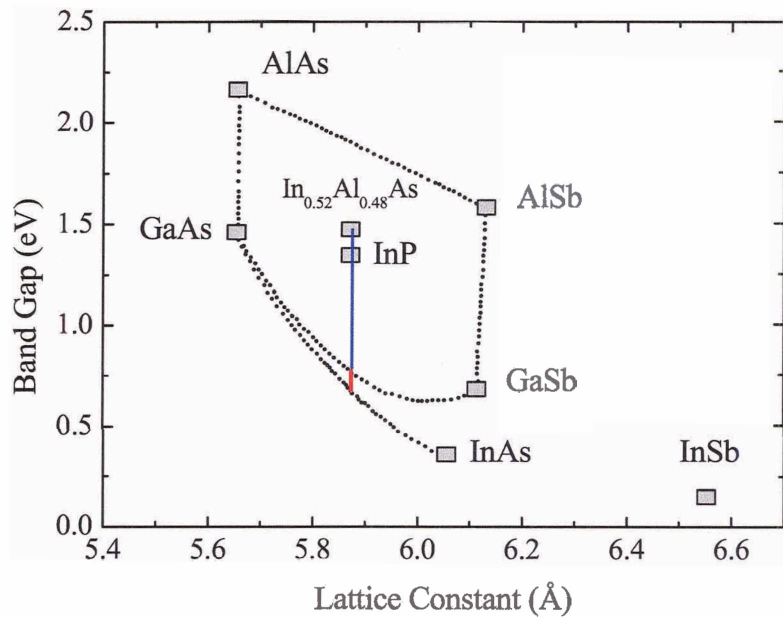


Figure 5-9: ***Energy band gap vs. lattice constant for alloys InP, $In_{0.52}Al_{0.48}As$, $Al_xGa_{1-x}As_{1-y}Sb_y$ and $Ga_xIn_{1-x}As_{1-y}Sb_y$. Vertical blue and red lines indicate InP lattice matched range.***

the maximum achievable band gap variance of $(Ga_{0.47}In_{0.53}As)_z(GaAs_{0.51}Sb_{0.49})_{1-z}$ is much smaller (0.05 – 0.1 eV) than that of $Al_xGa_{1-x}As_{0.51}Sb_{0.49}$ (> 0.6 eV assuming that the base band gap should not exceed the band gap of InP). In other words, using aluminium to grade $GaAs_{0.51}Sb_{0.49}$ should provide more flexibility than would indium, in terms of the band gap engineering. In addition, from the epi-layer growth point of view, the Al-alloy, rather than the In-alloy, would favour carbon doping [129]. A high doping level in the base is important for reducing the base sheet resistance and for improving the Kirk current. According to [17], the indium-graded InGaAsSb base exhibits unexpected high sheet resistance and as a result, f_{max} was low. Although it remains to be demonstrated experimentally, the Al-grading scheme along with the use of the InAlAs emitter could eliminate the type-II conduction band offset at the BE junction.

Fig. 5-10 shows simulated electric field and electron velocity profiles in the uniform and linearly graded bases of InP/(Al)GaAsSb/InP DHBTs. In the simulation, we set the base doping to be uniform and, for simplicity, we assume that other physical parameters, such as the conduction band offset and the electron effective mass, are independent of the band gap. We find that, in the uniform neutral base (ΔE_{gB} = 0), the electric field is nearly zero, and the electron velocity roughly corresponds to the thermal velocity (2-3×10^7 cm/s). In the graded base, the electric field increases almost linearly with increasing band gap variation ΔE_{gB}. The electron velocity increases dramatically when ΔE_{gB} changes from zero to 0.1 eV. Further increases in ΔE_{gB}, however, offer diminishing returns. The simulations indicate that the electron overshoot can be observed in this thin base layer. Fig. 5-11 shows the maximum f_T, f_{max} and DC gain vs. ΔE_{gB}. The f_T, f_{max} can be significantly improved by the graded base with ΔE_{gB} = 0.1 eV. With more aggressive grading (ΔE_{gB} = 0.2 and 0.3 eV), however, the f_T, f_{max} stop increasing and instead, exhibit a very small amount of degradation. The reason for this is not clear yet, but the electron velocity tends to saturate with increasing electric field and hence, the base transit time cannot be expected to decrease without bounds. The DC current gain continuously increases with ΔE_{gB} from 0 to 0.3 eV, which indicates that the bulk recombination is reduced with increasing ΔE_{gB}.

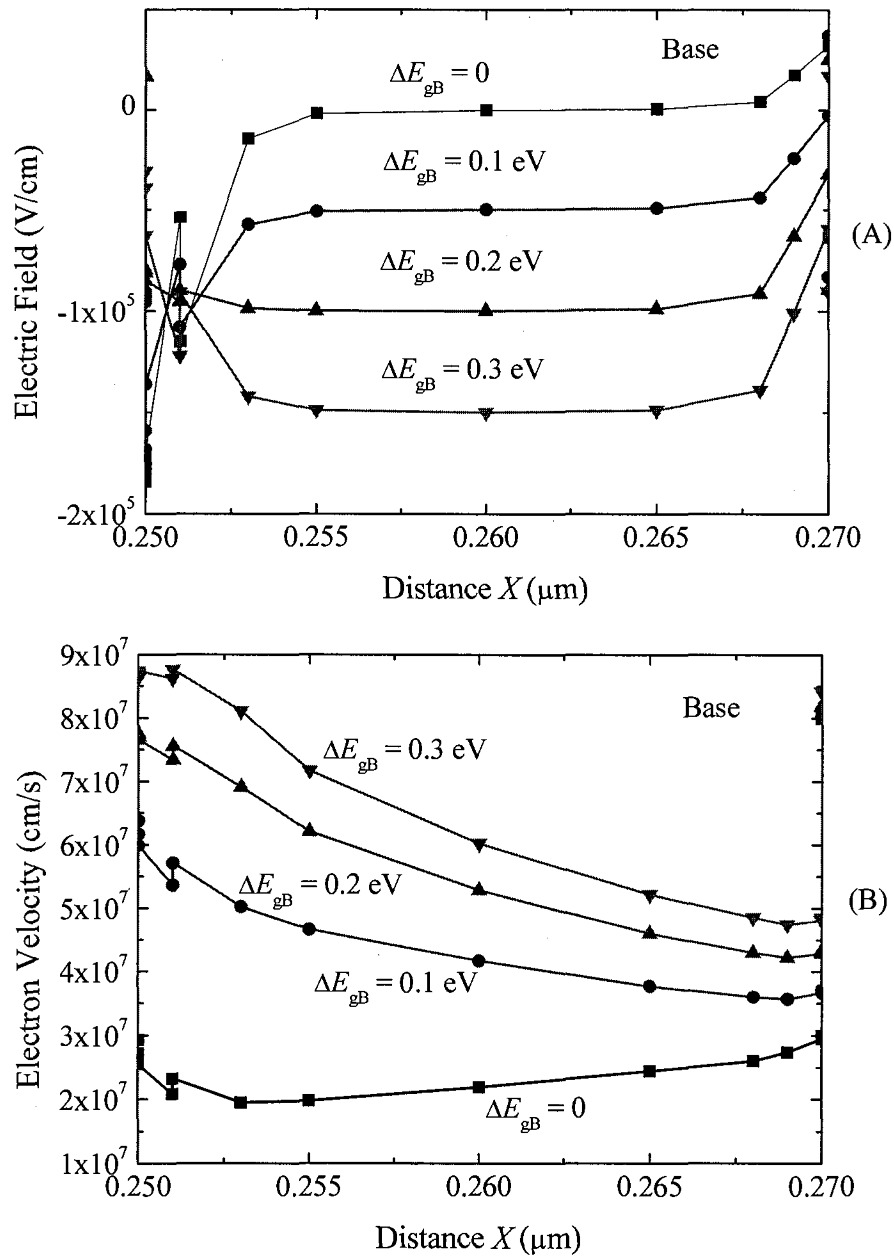


Figure 5-10: ***Simulated electric field (A) and electron velocity (B) profiles in the uniform and compositionally graded (Al)GaAsSb bases of InP/GaAsSb/InP DHBTs. The base band gap decreases linearly from the BE junction (X = 0.25 μm) to BC junction (X = 0.27 μm), and ΔE_{gB} = 0 (squares), 0.1 eV (circles), 0.2 eV (triangles), and 0.3 eV (inverted triangles).***

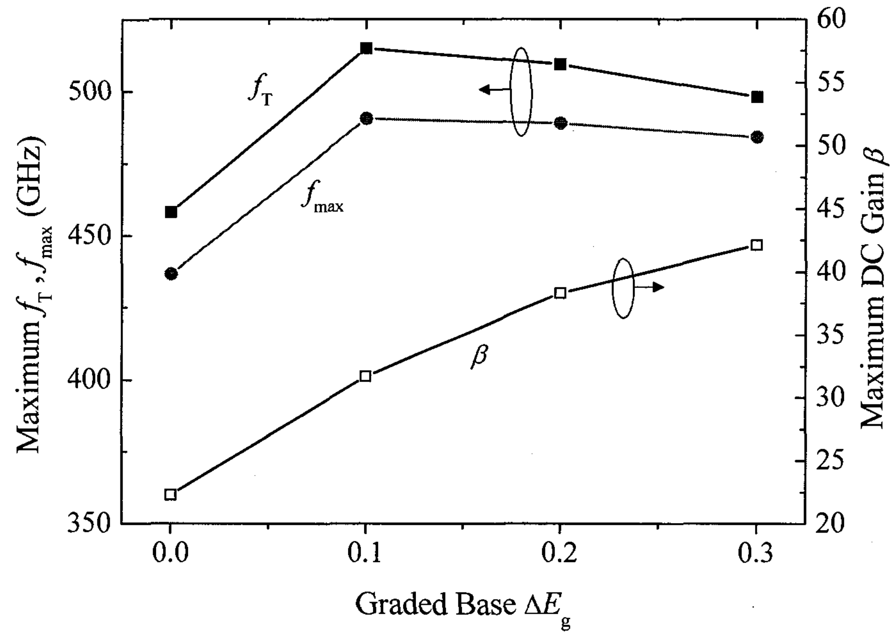


Figure 5-11: ***Simulated maximum f_T, f_{max} and DC current gain β vs. the band gap variance ΔE_g in the linearly graded base for InP/(Al)GaAsSb/InP DHBTs. The biases for RF and DC simulations are V_{CB} = 0.5 V and V_{CB} = 0, respectively.***

5.3.2 Doping Graded Base

Grading the base dopant density can also establish an aiding base electric field. This built-in field is given as [81]

$$E_B = \frac{kT}{qN_A(x)} \frac{dN_A(x)}{dx}, \qquad (5\text{-}2)$$

where $N_A(x)$ is the p-type dopant profile in the base. If we assume the highest achievable p-doping level in the base is 1×10^{20} cm^{-3}, then for a linear grading profile from 1×10^{20} cm^{-3} at the BE junction to 1×10^{19} cm^{-3} at the BC junction, the equilibrium energy band is shown in Fig. 5-12. This built-in field in Fig. 5-12 is not a constant, but if the doping density $N_A(x)$ varied exponentially across the base, a constant field would arise according

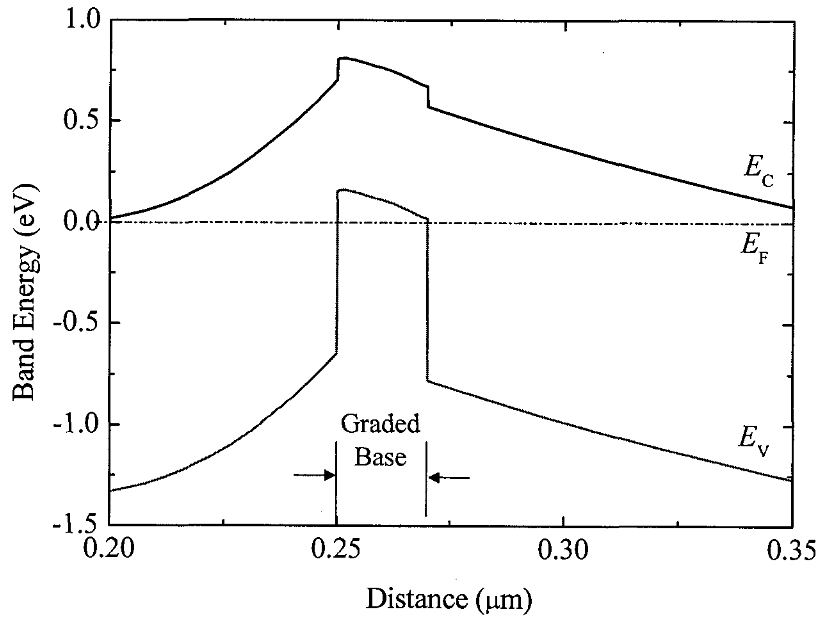


***Figure 5-12:** The equilibrium band diagram of an InP/GaAsSb/InP DHBT with a linearly dopant-graded base. The p-type doping level linearly changes from 1×10^{20} cm^{-3} at the BE junction to 1×10^{19} cm^{-3} at the BC junction.*

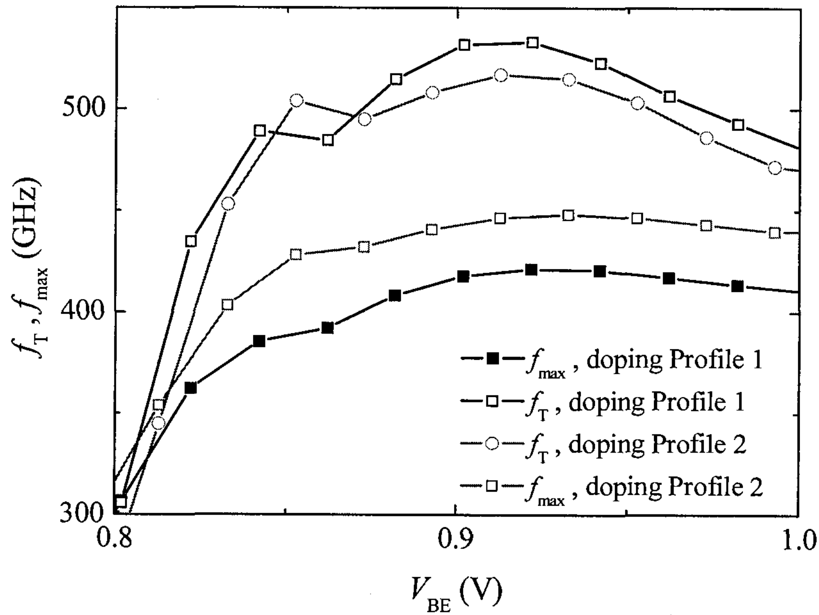


***Figure 5-13:** Simulated f_T and f_{max} as functions of the bias V_{BE} for InP/GaAsSb/InP DHBTs with dopant-graded bases. The doping density linearly changes from 1×10^{20} cm^{-3} at the BE junction to 1×10^{19} cm^{-3} (Profile 1) and 5×10^{19} cm^{-3} (Profile 2) at the BC junction.*

to (5-2). Fig. 5-13 shows f_T and f_{max} as functions of the BE bias for InP/GaAsSb/InP DHBTs with two base doping profiles. In Profiles 1 and 2, the doping level linearly changes from 1×10^{20} cm^{-3} at the BE junction to 1×10^{19} cm^{-3} and 5×10^{19} cm^{-3} at the BC junction, respectively. The f_T for Profile 1 is a little higher than that for Profile 2, because Profile 1 gives rise to a higher electric field than does Profile 2. Nevertheless, the f_{max} for Profile 1 is lower than that for Profile 2. This demonstrates a disadvantage of using a dopant grading scheme: the base sheet resistance increases due to the reduced integrated base doping level. Actually, when compared to the uniformly doped (1×10^{20} cm^{-3}) but compositionally graded base (see Fig. 5-11), the dopant-graded base leads to a significantly lower f_{max}. The DC current gains of the devices with the base doping Profiles 1 and 2 are also found to be higher than that of the device with an uniform base doped to 1×10^{20} cm^{-3}. This is due to the combined effects of the aiding built-in field and of the reduced base recombination associated with the lower average doping level.

As in the previous Section, we assume that in the simulations, no other parameters of the base layer are affected by the varying doping level. If we consider the band gap narrowing effect, the linear doping profile will result in a linear increase of the band gap from the BE to BC junctions. This band gap change may give rise to an undesirable electric field that would tend to oppose the electron movement from the emitter toward the collector. Moreover, the lower base doping level at the BC junction may have an adverse impact on the Kirk current, according to our findings of Chapter 4.

5.4 Collector Design

For the collector design, two features must be considered: the Kirk current density and the breakdown voltage. As discussed in Chapter 4, increasing the base and collector doping levels will delay the onset of the Kirk effect because the magnitude of the zero current electric field at the BC junction increases. Assuming that the collector is uniformly doped and fully depleted, and that the mobile electron density is negligible, i.g., ignoring the Kirk effect, we can write the peak electric field at the BC junction [81]:

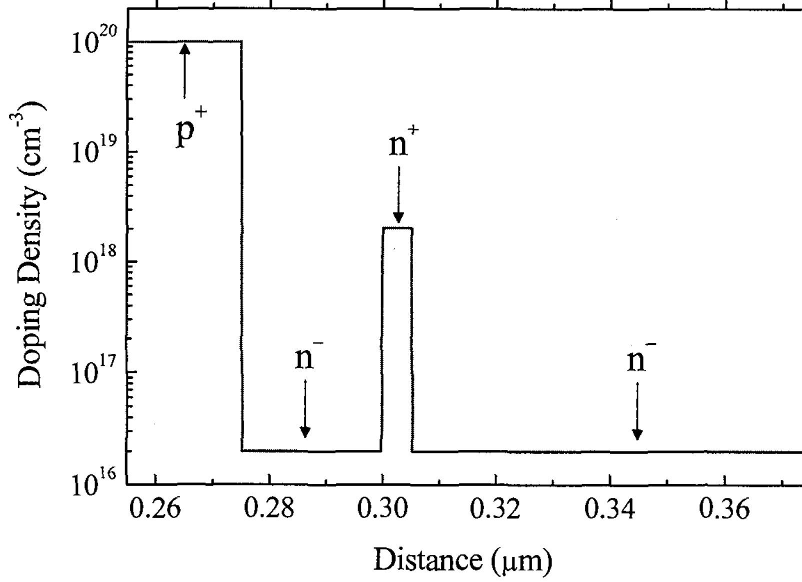


Figure 5-14: The doping profile in the base and collector with $n^- - n^+ - n^-$ structure.

$$E_{\mathrm{CB}}(0) = \frac{1}{X_{\mathrm{C}}}\left(V_{\mathrm{CB}} + \varphi_{\mathrm{CB}} + \frac{1}{2\varepsilon_C} qN_{\mathrm{D}}X_{\mathrm{C}}^2\right), \tag{5-3}$$

where X_{C} is the collector thickness, V_{CB} is the applied voltage across the BC junction, φ_{CB} is the BC built-in voltage, and N_{D} is the doping density in the collector. If the peak electric field exceeds a certain threshold, the collector current increases sharply and the breakdown occurs. From (5-3), we can see that the higher the doping density, the lower is the breakdown voltage, for a given critical field. A linear or exponential doping profile in the collector has been suggested to increase the Kirk current by 50% [130], but this doping grading increases the complexity of the collector growth. In this work, we propose a simple collector doping structure for type-II GaAsSb-based DHBTs: the InP collector doping profile shall be $n^- - n^+ - n^-$. We show here that a thin n^+ doping layer in an otherwise lightly doped collector can significantly reduce the electron blocking effect at the type-II BC junction, wihtout significantly deteriorating the collector breakdown voltage.

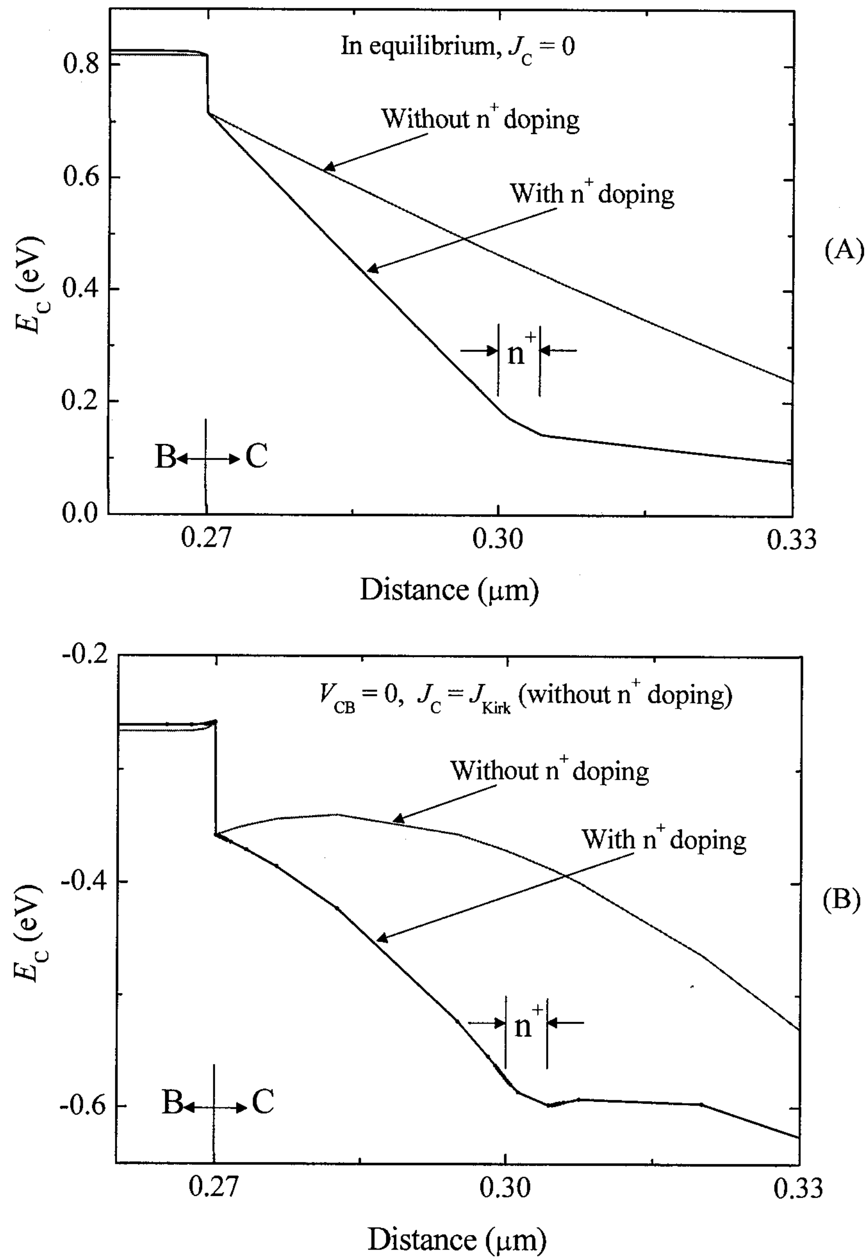


***Figure 5-15:** Simulated conduction band edges across the BC junctions of InAlAs/GaAsSb/InP DHBTs with and without n^+ doping in the collector. (A): in thermal equilibrium; (B): at the Kirk current level for the device with uniform n^- doping.*

2D simulations were performed for InP/GaAsSb/InP DHBTs to compare the uniform n^- and $n^- - n^+ - n^-$ collector doping profiles. Fig. 5-14 illustrates a typical doping profile with the $n^- - n^+ - n^-$ structure. Here, the base is uniform with a doping level of 1×10^{20} cm^{-3}. Fig. 5-15 shows the conduction band diagrams of the BC junctions with and without the n^+ doping spike, at zero and at high injection levels. When the injection level increases from zero to the onset of the Kirk effect with the uniform n^- collector doping, the n^+ doping spike significantly postpones the development of the induced electron barrier in the base. As a result, the onset of the Kirk effect is delayed to higher current densities. In particular, the Kirk current was increased by 43% due to the presence of the narrow n^+ doping in the collector. Fig. 5-16 shows the electric field profiles corresponding to Fig. 5-15. The n^+ doping in the collector enhances the equilibrium electric field at the BC junction (see Fig. 5-16A). At a high injection level corresponding to J_{Kirk} (see Fig. 5-16B) for the device with the n^+ doping, the onset of the Kirk effect still does not occur though the electric field around the n^+ doping spike begins to reverse. This phenomenon is different from what was described in [130],[7] which is only suitable for BC homojunctions that feature base pushout at high injection. For type-II GaAsSb/InP BC junctions, no base pushout occurs, and the electron barrier and tunnelling across it play the determinant roles under high injection conditions (see detailed discussion in Chapter 4).

We also found that to maintain the same peak current density as in the aforementioned $n^- - n^+ - n^-$ collector, the doping level of a uniformly doped collector should be increased to over 1×10^{17} cm^{-3}, and that such a highly doped collector would degrade the breakdown voltage. As shown in Fig. 5-17, if we define the breakdown voltage BV_{CEO} at a current density of J_C = 1 kA/cm^2 [3], the values of BV_{CEO} for the collectors with and without n^+ doping in the collector are very close: ~ 5.5 V. However, the BV_{CEO} for the collector uniformly doped to 1×10^{17} cm^{-3} is about 5 V, and the reverse current density (J_C before breakdown) is significantly higher than other two cases.

[7] The authors argue that, in a collector with non-uniform doping, as soon as the electric field drops to zero at any point within the collector, the base pushout or the onset of the Kirk effect occurs.

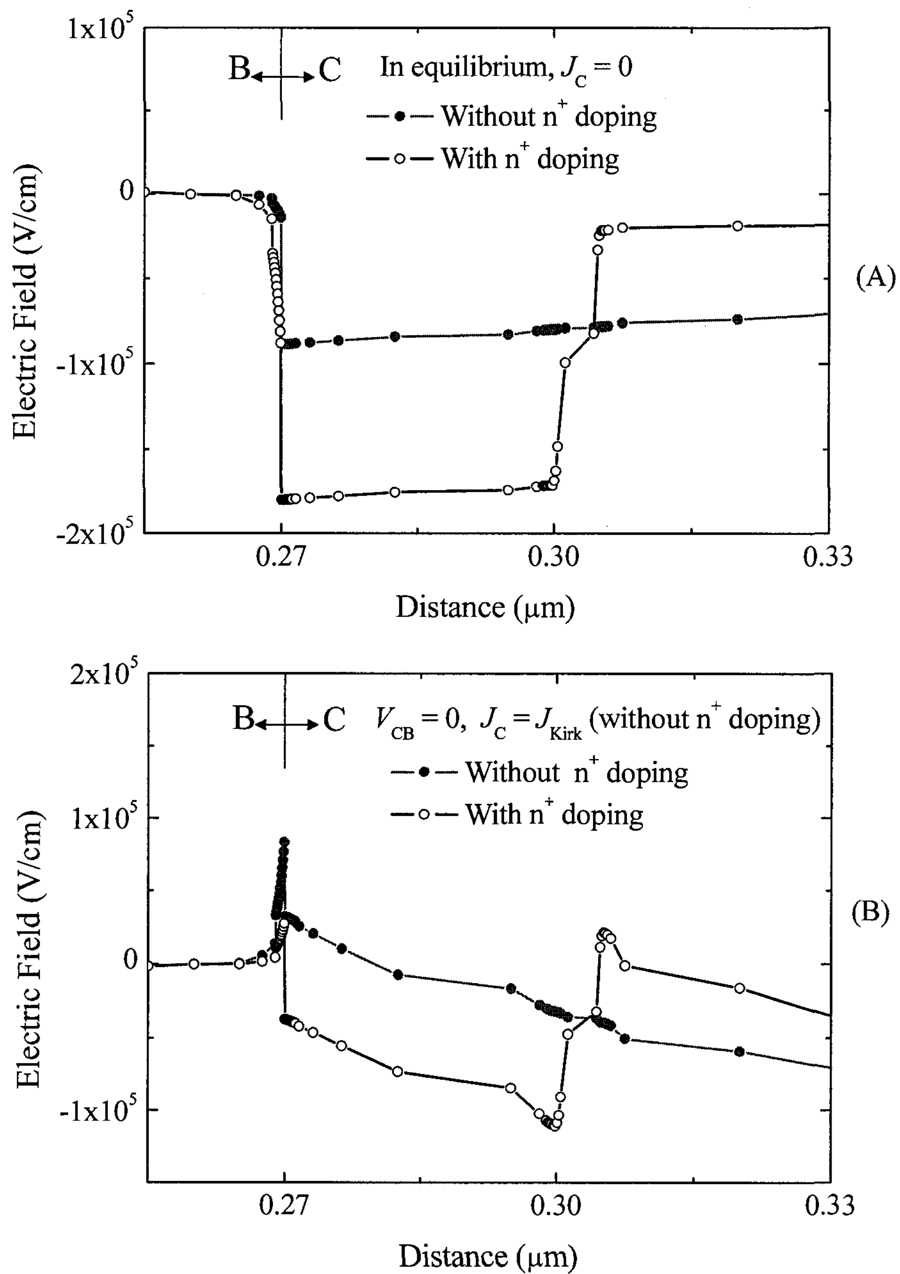


Figure 5-16: Simulated electric field across the BC junctions of InAlAs/GaAsSb/InP DHBTs with and without n^+ doping in the collector. (A): in thermal equilibrium; (B): at the Kirk current level for the device with uniform collector n^- doping.

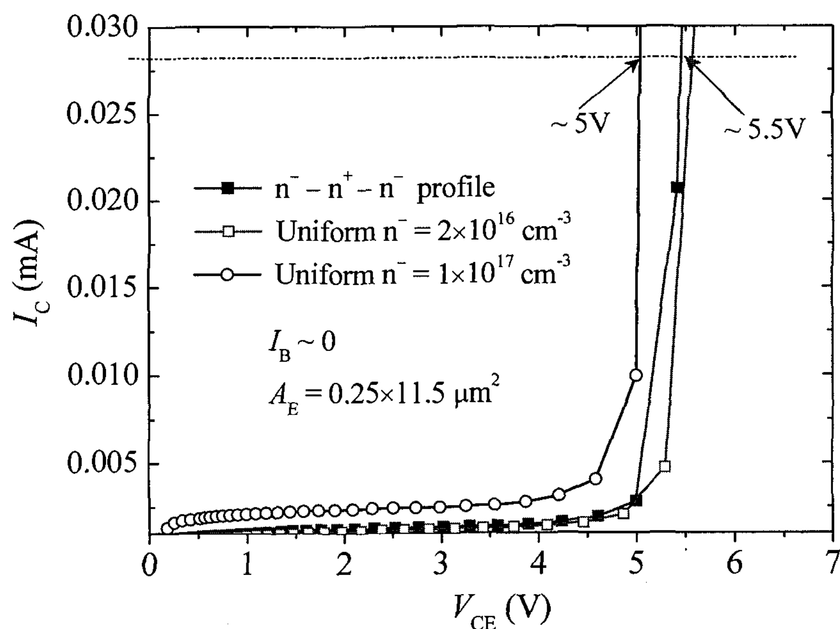


***Figure 5-17:** Simulated collector current vs. collector-emitter voltage at nearly zero base current for InAlAs/GaAsSb/InP DHBTs with n^- – n^+– n^- doping (solid squares), lower uniform doping n^- (open squares) and higher uniform doping n^- (open circles) in the collectors. The InP collector thickness is 1000 Å, and n^- – n^+ – n^- doping profile is 2×10^{16} – 2×10^{18} – 2×10^{16} cm^{-3}.*

Unfortunately, we are unable to present the comparison of the RF results between different collector structures, due to the difficulties of implementing the tunnelling models in the RF simulation.

5.5 Predicted High Performances of InAlAs/(Al)GaAsSb/InP DHBTs

Based on previous design work, we now propose three different structures for InAlAs/GaAsSb/InP DHBTs and compare them, as shown in Table 5-1. For all three structures, the bases are compositionally graded so that ΔE_{gB} = 0.1 eV and the n^- – n^+ – n^- collector doping profile is also applied. The f_T and f_{max} vs. collector current density for these three structures are shown in Fig. 5-18. If we vertically scale the base from 200 to 150 Å and scale the collector from 1000 to 750 Å (from structure-I to structure-II), the

Table 5-1: Proposed InAlAs/(Al)GaAsSb/InP DHBT structures

Parameters	Structure-I	Structure-II	Structure-III
Emitter width W_E / 2 (μm)	0.2	0.2	0.15
Emitter undercut W_{BE} (μm)	0.1	0.1	0.08
Extrinsic base W_B +W_{BE} (μm)	0.4	0.4	0.35
Emitter length L_E (μm)	11.5	11.5	11.5
Emitter cap thickness (μm)	0.1	0.1	0.1
Emitter ($In_{0.52}Al_{0.48}As$) thickness X_E (μm)	0.015	0.015	0.015
Emitter ($In_{0.52}Al_{0.48}As$) doping (cm^{-3})	3×10^{17}	3×10^{17}	3×10^{17}
Base (graded AlGaAsSb ΔE_{gB}=0.1eV) thickness	0.02	0.015	0.015
Base (graded AlGaAsSb ΔE_{gB}=0.1eV) doping	1×10^{20}	1×10^{20}	1×10^{20}
Collector (InP) thickness X_C (μm)	0.1	0.075	0.075
Collector (InP) n^- doping (cm^{-3})	2×10^{16}	2×10^{16}	2×10^{16}
Collector (InP) n^+ doping (cm^{-3})	2×10^{18}	2×10^{18}	2×10^{18}
Distance of the n^+ doping from the base (μm)	0.03	0.025	0.025

maximum f_T increases from about 700 GHz to 870 GHz. However, the maximum f_{max} decreases from about 580 GHz to 520 GHz, due to the increased base resistance and collector capacitance. To improve the f_{max}, we need to scale the lateral dimensions of the device more aggressively. By taking advantage of the current process techniques, we can further decrease the emitter width (W_E / 2) from 0.2 to 0.15 μm [131, 132], decrease the emitter undercut (W_{BE}) from 0.1 to 0.08 μm, and decrease the base metal contact width (W_B) from 0.3 to 0.25 μm (see Chapter 2). This lateral scaling (structure-III) significantly improves the f_{max} from about 520 to 620 GHz, while the f_T also slightly increases from 870 to 888 GHz. According to the result in [17], the breakdown voltage (BV_{CEO}) of structure-III with the collector thickness of 750 Å should be higher than 4 V. It is noted that the tunneling model was not employed in these RF simulations, and therefore, the frequencies would probably be even higher with the tunneling model applied due to the delay of the Kirk effect as discussed in Chapter 4.

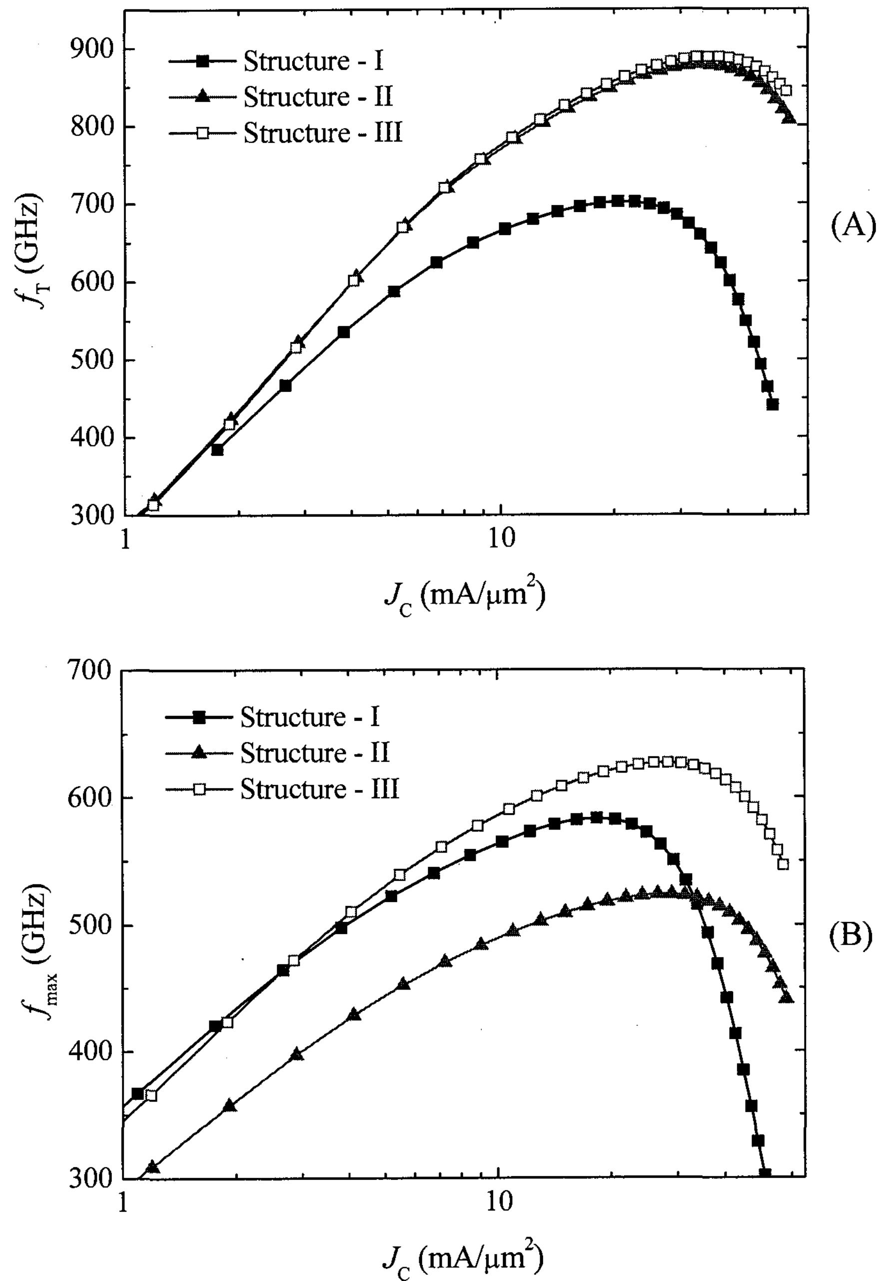


***Figure 5-18:** Simulated f_T (A) and f_{max} (B) as functions of J_C for InAlAs/(Al)GaAsSb/InP DHBTs with the three structures as shown in Table 5-1.*

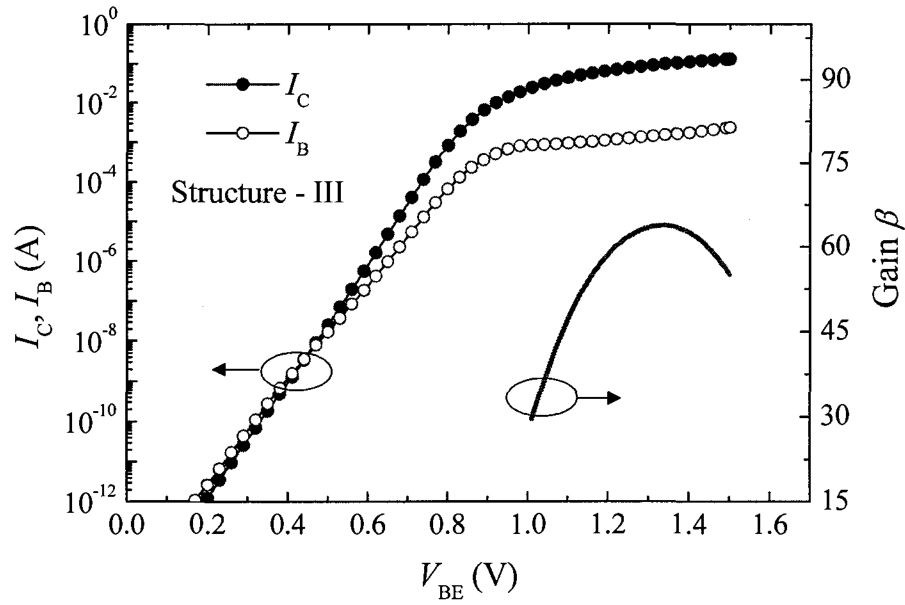


Figure 5-19: Simulated Gummel plot and current gain for structure III. $V_{CB} = 0$ ***V.***

The highest DC current gain (β) could reach over 60 as shown in Fig. 19. in which the tunneling model was sucessfully implemented. Nevertheless, surface passivation is strongly recommended for the highly scaled GaAsSb-based DHBTs to further improve the gain. Our results show that it is possible for type-II GaAsSb-based DHBTs to achieve higher performances than InGaAs-based HBTs, which recently showed peak performances: $f_T \sim 710$ GHz, $f_{max} \sim 340$ GHz and $BV_{CEO} \sim 1.7$ V [4], and $f_T \sim 215$ GHz and $f_{max} \sim 680$ GHz [133].

Chapter 6:

Summary and Future Work

6.1 Summary

Type-II GaAsSb-based DHBTs are now recognized as a promising alternative to the type-I InGaAs-based HBTs for high-frequency and optoelectronic applications. The present dissertation focussed on some important issues associated with type-II GaAsSb-based DHBTs, and through both experiments and numerical simulations, provided useful new insights to guide further improvements in device performance.

6.1.1 2D Simulation

This work laid the foundation for 2D simulations using the leading commercial simulation tool (ISE TCAD) at the SFU Compound Semiconductor Device Laboratory. A series of physical models, such as the hydrodynamic model, mobility model, and surface state model were successfully implemented in the 2D simulations for GaAsSb-based DHBTs.

Band gap narrowing in heavily doped $Ga_{0.51}As_{0.49}Sb$ base layers was studied by comparing the simulated forward collector currents with the measured results for InP/GaAsSb/InP DHBTs. The comparison suggested that the effective base energy band gaps (E_{gB}) are 0.67 and 0.72 eV for doping levels of 5×10^{19} cm^{-3} and 5×10^{18} cm^{-3}, respectively. This study was helpful in verifying that the E_{gB} is 0.68 eV for a doping level of 4×10^{19} cm^{-3}, in the sample #6671 (a 200 mm diameter high-quality wafer grown at Nortel that has undergone extensive characterization in the CSDL). An adequate

modelling of the base band gap narrowing effect is necessary in HBTs because the base energy gap controls the base-emitter turn-on voltage.

All parameters in the physical models were carefully defined, based on our experimental results or on published data. Excellent agreement was achieved between the simulated DC and RF characteristics and the corresponding measured experimental results for the InP/GaAsSb/InP DHBTs (#6671). For the experimentally measured Mason's Unilateral Gain (MUG) of the sample #4720, which exhibited too much noise to reliably define a maximum oscillation frequency f_{max} through the common –20dB/decade extrapolation, we verified that the f_{max} was ~ 400 GHz, by fitting the accurately simulated MUG curve to the measured one.

6.1.2 Surface Recombination Current

We fabricated the InP/GaAsSb/InP DHBTs (#6671) and experimentally characterized self-aligned and non self-aligned devices in terms of their periphery surface recombination currents. The emitter sizes of the measured devices ranged from 0.5×6 to 80×80 μm^2. The emitter size effect was parameterized and the extracted periphery current density was found to be comparable to that reported for InP/InGaAs SHBTs. We also modelled the surface recombination current for InP/GaAsSb/InP DHBTs by implementing surface state models in the 2D simulations. We found that the surface state conditions at both the emitter sidewall and extrinsic base surface, predominantly give rise to the periphery recombination current by enhancing the injection of electrons from the emitter to the extrinsic base surface.

2D simulations with the surface state modelling also indicated that the base overetching that occurs during the emitter mesa etching process, would increase the periphery surface recombination current, comparing to the non-base etching situation where the emitter mesa etching perfectly stops at the base layer (i.e., infinite etch selectivity).

The measured surface recombination current of #4720 (SFU grown) with tensile strained and highly doped (9×10^{19} cm^{-3}) bases was found to be significantly larger than

that of #6671 (Nortel grown) with lattice matched and moderately doped (4×10^{19} cm^{-3}) bases. It is not clear whether the differences arise because of layer designs or from the fact that layers were produced in different reactors using different precursors.

Two solutions were proposed in order to reduce the surface recombination current of GaAsSb/InP DHBTs: by means of 2D numerical simulations, InAlAs emitters and emitter ledges were shown to reduce the direct injection of electrons from the emitter onto the extrinsic base surface by weakening the strength of the saddle point potential at the emitter-base sidewall.

6.1.3 High Injection Effect

This study demonstrates a new mechanism for the high injection effect in type-II GaAsSb-based DHBTs, which differs from the conventional Kirk effect. By comparing the simulated behaviour of BC homojunctions with the type-II BC heterojunctions in 2D simulations, we confirmed that no base pushout occurs for type-II GaAsSb-InP BC junctions, even under high injection levels. Instead, the electric field at the BC junction is reversed, and an electron barrier develops at the base side. We applied the tunnelling model to the type-II BC junctions, and found that the tunnelling process significantly increases the current gain and the peak collector current. This indicates that the electron barrier that develops at the base side plays an important role in the high injection effect for type-II GaAsSb-based DHBTs. Up to now, the importance of quantum mechanical tunnelling transport at the BC heterojunction in type-II DHBTs had not been appreciated.

We fabricated the In/GaAsSb/InP DHBTs with base doping levels of 5×10^{19} cm^{-3} (#4450) and 5×10^{18} cm^{-3} (#4451), but with nominally identical structures otherwise. Our measurements indicate that the peak current density of #4450 is higher than that of #4451. The observation was surprising since in the context of the classical Kirk effect the peak current density in a bipolar transistor is uniquely determined by the collector doping level and electron velocity. The results were explained by the simulations, which show that the electron barrier in the lightly doped base develops faster than in the heavily doped base at high current injection levels. We further found that the higher the electric field at the BC junction at zero current level, or equivalently, the higher the BC built-in

voltage, the slower the electron barrier develops at high current levels. The last observation indicates that a trade-off situation can also be exploited between breakdown voltage and maximum current drive in type-II DHBTs.

6.1.4 Device Optimization

This work provides guidance for achieving greatly improved performances in GaAsSb-based DHBTs. Our results show that, based on current fabrication techniques, type-II GaAsSb-based DHBTs could reach competitive f_T, f_{max}, and BV_{CEO}, compared to the type-I InGaAs-based HBTs. In this work, we used the TCAD to design and optimize the emitter, base, and collector.

By comparing the InAlAs with the InP emitters, and the different emitter thicknesses and doping levels, we found that using InAlAs as the emitter was advantageous, and that the optimum thickness is ~ 150 Å at a doping level of 3×10^{17} cm^{-3} for high-frequency performance.

We examined both compositional and dopant grading schemes for the base layer, and found that compositionally graded bases are favourable because they enable the simultaneous improvement of both f_T and f_{max}. We also found that for high-frequency performance the optimum band gap variation across the base layer is ΔE_{gB} ~ 0.1 eV in a compositionally graded base.

We proposed an n^-–n^+– n^- doping profile for the collector, in which the n^+ doping is very thin compared to the total collector thickness. The simulated results showed that adding a narrow n^+ doping (2×10^{18} cm^{-3}) to the collector with n^- doping (2×10^{16} cm^{-3}) at a location close to the base, e.g., one third of the collector width, significantly decreases the induced electron barrier on the base side at high injection levels, and increases the Kirk current density by over 40%. We also found that the breakdown voltages (BV_{CEO}) of the devices with this collector doping scheme remains almost unchanged. For the best high-frequency performance, the collector thickness should be 750–1000 Å at a doping level of 2×10^{16} cm^{-3}.

In considering all of the optimized results, non-passivated InAlAs/(Al)GaAsSb/InP DHBTs with the emitter area of 0.3×11.5 μm^2 and base-collector junction width of 0.96 μm would be able to achieve f_T > 800 GHz, f_{max} > 600 GHz, BV_{CEO} > 4 V, and β > 60. Achieving such performance levels would once again allow GaAsSb/InP DHBTs to set new performance standards with a record $f_T \times BV_{CEO}$ > 3.2 THz-V.

6.2 Future Work

6.2.1 Monte Carlo Simulation

A significant electron overshoot was found in the collector of type-II GaAsSb/InP DHBTs, as the average electron velocity in a 0.2 μm collector is about 4.3×10^7 cm/s [67], and thus much larger than the saturation velocity in InP: $v_{sat} = 1\times10^7$ cm/s. In the present mobility model, with constant relaxation time τ_{en}, we should increase v_{sat} to 1.5×10^7 cm/s to achieve the experimentally measured average velocity in the collector (as shown in Fig, 6-1). The discrepancy is probably associated with our use of a constant τ_{en} value. As mentioned in Chapter 2, an energy dependent τ_{en} is critical for better modelling the electron overshoot in the collector side of BC junction in a hydrodynamic model. However, the energy dependence of τ_{en} must be verified and calibrated by MC simulations. The average electron energy, as a function of the electron temperature T_n, is given by $w_n = \frac{3k_B T_n}{2}$, and Fig. 6-2 shows a typical τ_{en} as a function of the electron temperature. The detailed method for extracting τ_{en} from MC simulations can be found in [48].

6.2.2 More Accurate and Solid Methods to Simulate Tunnelling Process

As was mentioned in Chapter 4, the WKB method that was used to calculate the tunnelling probability in the ISE TCAD, may not be accurate enough for the electron barrier at the BC junction. To overcome this shortcoming of the WKB method, a more rigorous model is needed, such as the flux method which was used for the emitter-base energy band spike in InP/InGaAs and AlGaAs/GaAs HBTs [134, 135].

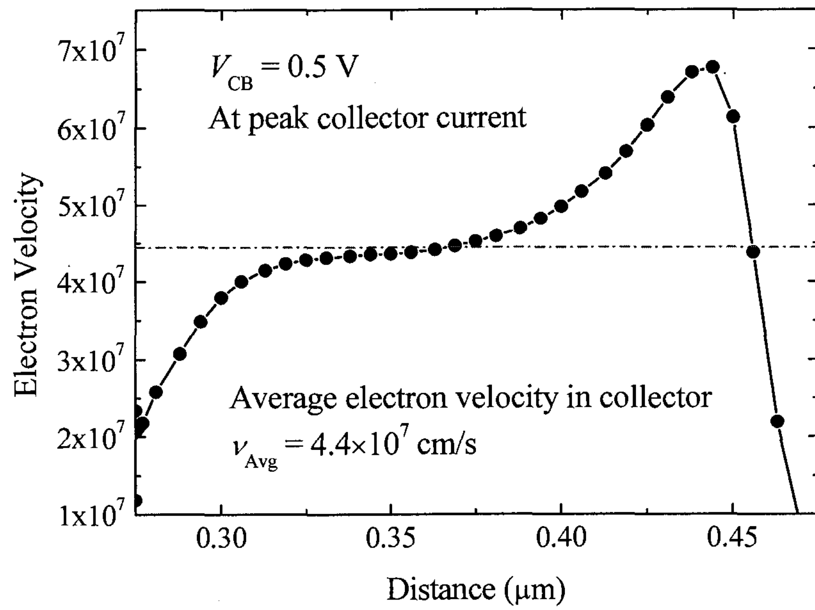


Figure 6-1: ***Simulated electron velocity in a 0.2 μm InP collector with τ_{en} = 1 ps and v_{sat} = 1.5×10^7 cm/s.***

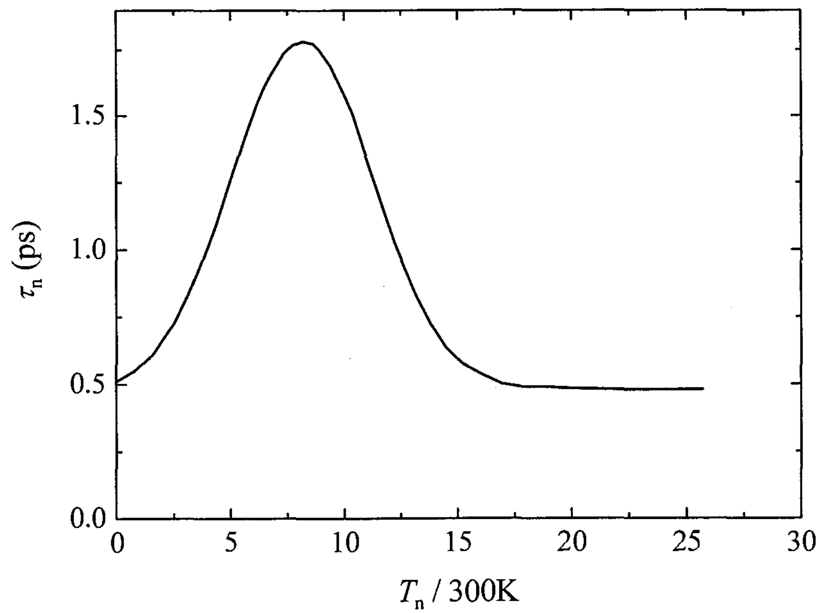


Figure 6-2: ***Electron energy relaxation time as a function of electron temperature for GaAs (after [48]).***

6.2.3 Measurement of Electron Mobility in p-type GaAsSb Using Magneto Transport Techniques

We have carried out magneto-transport measurement [68] to determine the effective electron mobility in GaAsSb/InP DHBTs with a base thickness of 250 Å, as mentioned in Chapter 2. However, in order to parameterize the bulk electron mobility of p-type GaAsSb, we need to measure the devices with a number of different base thicknesses, e.g., 200, 400, 600 and 800 Å, so that we can extract the bulk electron mobility and mean free path according to [70]. The measurement for different base doping levels, e.g., 5×10^{18}, 1×10^{19}, 5×10^{19}, and 1×10^{20} cm^{-3} is also required to find how the electron mobility changes with the p-doping level and further to explore the electron scattering mechanism in GaAsSb [136].

6.2.4 Self-heating Modelling and Thermal Resistance for GaAsSb-based DHBTs

Any bipolar transistor has a certain amount of thermal resistance R_{th}, and therefore, when electric power is dissipated through the device, the device temperature, or specifically the lattice temperature T_{L} will increase according to (in forward common emitter operation mode):

$$T_{\mathrm{L}} = T_0 + R_{\mathrm{th}} V_{\mathrm{CE}} I_{\mathrm{C}}, \qquad (6\text{-}1)$$

where T_0 is the temperature with zero power, I_C is the collector current and V_{CE} is the collector bias. The increase of T_{L} will change many material properties, e.g., the carrier mobility, and in turn, the device characteristics. This is called the self-heating effect [81]. To employ the self-heating model for more accurate simulations, we need to specify the temperature dependences of all material parameters. The device thermal resistance R_{th} can be experimentally determined [137, 138].

6.2.5 Leakage Current Modelling

The BE and BC leakage currents (or reverse currents) are measured when the BE and BC junctions are reverse-biased, and they are usually of the order of nA. Our simulated reverse currents did not quite match to the measured ones, as shown in Fig. 6-3. This problem might be solved by modifying the generation-recombination models and

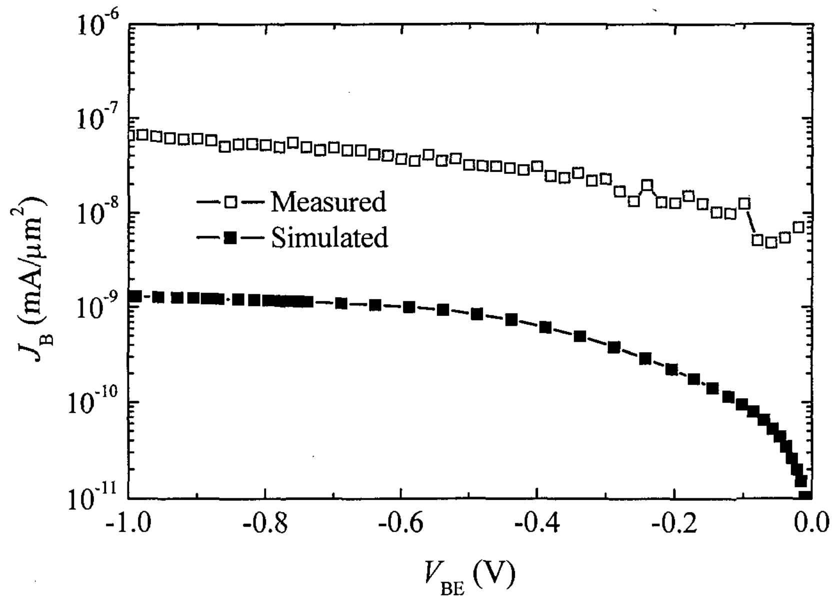


Figure 6-3: Measured and simulated reverse base-emitter current density as a function of the base-emitter voltage. The collector is open-circuited.

the surface state models since a surface current flowing between two contact metals is identified to contribute to the leakage current [96, 139]. For the collector-emitter leakage current a fully three-dimensional (3D) simulation is required [48, 140] [141].

6.2.6 Passivation for Sub-micron GaAsSb-based DHBTs

We addressed the issue of the surface recombination in GaAsSb/InP DHBTs in Chapter 3. The problem may be resolved by device passivation [24, 142, 143]. Although passivation films might increase the parasitic capacitances, because the dielectric constant of the material used for the passivation is higher than that of air, device reliability becomes increasingly important as GaAsSb-based DHBTs tend to be widely used in commercial applications. Agilent Technologies, for example, uses Si_3N_4 to passivate GaAsSb-based DHBTs [14], but the influence of the dielectric on the surface recombination current has not been reported.

6.2.7 Impacts of Emitter Orientation on Device Performances

In Chapter 3, we assumed that the emitter sidewall is strictly vertical to the extrinsic base surface (100). In reality the emitter sidewall exhibits either positive or negative slope, depending on the emitter orientation [144]. It was also reported that the emitter orientation has a significant impact on the characteristics of HBTs, such as AlGaAs/GaAs HBTs [145], InP/InGaAs HBTs [146] and GaInP/GaAs HBTs [147]. In our GaAsSb/InP DHBTs, the emitter stripes are along [011], which makes the emitter sidewall exhibit a negative slope. Kurishima *et al.* found that the self-aligned HBTs with the emitter along [01-1], which makes the emitter sidewall exhibit a positive slope, displays better characteristics, e.g., smaller periphery current, compared to those with the emitter along [011] [146].

The mechanism for such differences, caused by the emitter orientation, is not clear, though some workers postulate that the piezoelectric effect is responsible [145]. This proposed mechanism may explain why our theoretical analyses in Chapter 3 showed that the surface recombination velocity at the extrinsic base surface is larger than expected. To clarify the aforementioned mechanism, or to find an alternative fabrication technique for better device performance, further investigations are needed on the effect of the emitter orientation effects in GaAsSb-based DHBTs.

6.2.8 Experimental Achievement of High Performance GaAsSb-based DHBTs

To achieve in reality the optimized performances of GaAsSb-based DHBTs, as described in Chapter 5, additional experiments are necessary, even though our designs are based on current fabrication techniques. For example, the growth of high quality aluminium-containing graded thin bases and extremely low emitter contact resistance ($< 5\times10^{-8}$ Ωcm^2) in GaAsSb-based DHBTs have not been reported yet, although the optimized device structures were selected to remain in the domain of what can reasonably be expected.

APPENDIX A

Material Parameters Used for Simulations

The following tables list all material parameters used in our simulations for InP, $GaAs_{0.51}Sb_{0.49}$, $In_{0.53}Ga_{0.47}As$, $In_{0.52}Al_{0.48}As$, InAs, GaAs, GaSb, and AlAs.

Table A-1: Material parameters of GaAs and GaSb (T = 300K).

Parameters	Symbol	GaAs	Ref.	GaSb	Ref.
Electron affinity (eV)	χ	4.07	[62]	4.06	[62]
Dielectric permittivity	ε	12.9	[62]	15.7	[62]
Mass Density (g/cm^3)	ρ	5.32	[62]	5.61	[62]
Band gap (eV)	E_g	1.42	[62]	0.73	[62]
Electron effective density of states(cm^{-3})	N_C	4.7×10^{17}	[62]	2.1×10^{17}	[62]
Hole effective density of states (cm^{-3})	N_V	9.0×10^{18}	[62]	1.8×10^{19}	[62]
Lattice heat capacity (J/(Kcm^3))	C_L	1.75	[62]	1.40	[62]
Lattice thermal conductivity (W/(cmK))	K_L	0.55	[62]	0.32	[62]

Table A-2: Material parameters of InAs and AlAs (T = 300K).

Parameters	Symbol	InAs	Ref.	AlAs	Ref.
Electron affinity (eV)	χ	4.9	[62]	3.67	[48]
Dielectric permittivity	ε	15.2	[62]	10.1	[148]
Mass Density (g/cm^3)	ρ	5.68	[62]	3.76	[148]
Band gap (eV)	E_g	0.35	[62]	2.2	[148]
Electron effective density of states(cm^{-3})	N_C	8.7×10^{16}	[62]	4.8×10^{18}	[48]
Hole effective density of states (cm^{-3})	N_V	6.6×10^{18}	[62]	1.8×10^{19}	[48]
Lattice heat capacity (J/(Kcm^3))	C_L	1.42	[62]	1.65	[48]
Lattice thermal conductivity (W/(cmK))	K_L	0.27	[62]	0.8	[48]

Table A-3: Material parameters and variables for InP and InAlAs (T = 300K).

Parameters	Symbol	InP	Ref.	$In_{0.52}Al_{0.48}As$	Ref.
Electron affinity (eV)	χ	4.38	[62]	4.18	[102]
Dielectric permittivity	ε	12.4	[62]	12.5	[48]
Electron energy relaxation time (ps)	τ_n	1	[58]	1	[58]
Hole energy relaxation time (ps)	τ_p	0.4	[58]	0.4	[58]
Mass Density (g/cm^3)	ρ	4.8	[62]	4.75	*
Band gap (eV)	E_g	1.35	[62]	1.44	[101]
Electron effective density of states(cm^{-3})	N_C	5.66×10^{17}	[62]	5.11×10^{17}	[101]
Hole effective density of states (cm^{-3})	N_V	1.1×10^{19}	[62]	8.98×10^{18}	[101]
Lattice heat capacity (J/(Kcm^3))	C_L	1.49	[62]	1.53	*
Lattice thermal conductivity (W/(cmK))	K_L	0.70	[62]	0.53	*

* From linear interpolation of InAs and AlAs.

Table A-4: Material parameters and variables for InGaAs and GaAsSb (T = 300K).

Parameters	Symbol	$In_{0.53}Ga_{0.47}As$	Ref.	$GaAs_{0.51}Sb_{0.49}$	Ref.
Electron affinity (eV)	χ	4.63	[80]	4.23	[80]
Dielectric permittivity	ε	13.9	[79]	14.2	*
Electron energy relaxation time (ps)	τ_n	1	[58]	1	[58]
Hole energy relaxation time (ps)	τ_p	0.4	[58]	0.4	[58]
Mass Density (g/cm^3)	ρ	5.5	[79]	5.46	*
Band gap (eV)	E_g	0.75	[79]	0.68	**
Electron effective density of states(cm^{-3})	N_C	2.8×10^{17}	[79]	2.42×10^{17}	[79]
Hole effective density of states (cm^{-3})	N_V	6.0×10^{18}	[79]	7.8×10^{18}	[79]
Lattice heat capacity (J/(Kcm^3))	C_L	1.65	[79]	1.57	*
Lattice thermal conductivity (W/(cmK))	K_L	0.05	[79]	0.41	*

* From linear interpolation of GaAs and GaSb
** At a doping level of ~ 4×10^{19} cm^{-3} (see Section 2.5.1)

APPENDIX B

Two-port Network Parameters

Most of the electrical blocks or networks can be simplified to only have two ports: input port and output port, as shown in Fig. B-1. The relation between the input (i_1, u_1) and output (i_2, u_2) is defined by network parameters. The input and output relation for a two-port network can be expressed in different forms which give rise to different parameter sets or matrices.

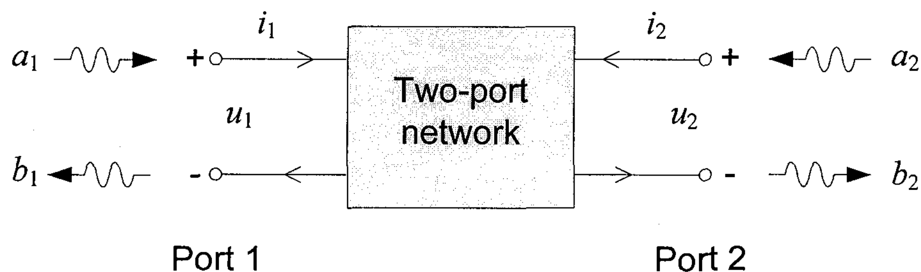


Figure B-1: ***A schematic two-port network. i_1 and v_1 are the input current and voltage respectively, and i_2 and v_2 are the output current and voltage respectively. a_1 and b_1 represent the incident and reflected power waves at Port 1 respectively, and a_2 and b_2 represent the incident and reflected power waves at Port 2 respectively.***

B.1 Definitions of Two-port Network Parameters

(1) Y-parameters

We define a Y-matrix $\begin{bmatrix} Y_{11} Y_{12} \\ Y_{21} Y_{22} \end{bmatrix}$ so that

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} Y_{12} \\ Y_{21} Y_{22} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}, \qquad \textbf{\textit{(B - 1)}}$$

where Y_{11}, Y_{12}, Y_{21} and Y_{22} are called Y-parameters and the Y-matrix is also called admittance matrix.

(2) *Z*-parameters

We define a *Z*-matrix $\begin{bmatrix} Z_{11} Z_{12} \\ Z_{21} Z_{22} \end{bmatrix}$ so that

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} Z_{11} Z_{12} \\ Z_{21} Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}, \qquad \textbf{\textit{(B - 2)}}$$

where Z_{11}, Z_{12}, Z_{21} and Z_{22} are called *Z*-parameters and the *Z*-matrix is also called impedance matrix.

(3) *H*-parameters

We define a h-matrix $\begin{bmatrix} H_{11} H_{12} \\ H_{21} H_{22} \end{bmatrix}$ so that

$$\begin{bmatrix} u_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} H_{11} H_{12} \\ H_{21} H_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ u_2 \end{bmatrix}, \qquad \textbf{\textit{(B - 3)}}$$

where H_{11}, H_{12}, H_{21} and H_{22} are called *H*-parameters and the *H*-matrix is also called hybrid matrix.

(4) *S*-parameters

Before defining the *S*-parameters, we need to define an incident normalized power wave a_n (entering the network) and a reflected normalized power wave b_n (leaving the network) where $n = 1$ or 2 representing the Port 1 and Port 2, as shown in Fig. B-1:

$$a_n = \frac{1}{2\sqrt{Z_0}}(u_n + Z_0 i_n), \quad b_n = \frac{1}{2\sqrt{Z_0}}(u_n - Z_0 i_n) \qquad \textbf{\textit{(B - 4)}}$$

Where Z_0 is a characteristic impedance of the connecting lines or transmission lines, which is assumed to be the same at the Port 1 and Port 2 for simplification. Now, we define a S-matrix so that

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} S_{12} \\ S_{21} S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ b_2 \end{bmatrix} \quad \textbf{(B - 5)}$$

where S_{11}, S_{12}, S_{21}, and S_{22} are called S-parameters and they are determined as follows:

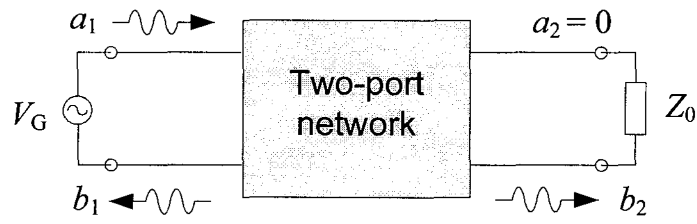
$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} = \frac{\text{reflected wave at port 1}}{\text{incident wave at port 1}}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} = \frac{\text{trasmitted wave at port 2}}{\text{incident wave at port 1}}$$

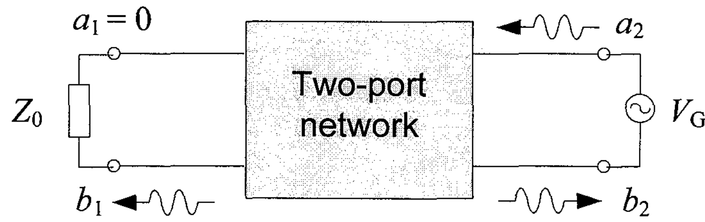
$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} = \frac{\text{reflected wave at port 2}}{\text{incident wave at port 2}}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} = \frac{\text{transmitted wave at port 1}}{\text{incident wave at port 2}}$$

$a_2 = 0$ and $a_1 = 0$ imply that no power waves enter the network at Port 2 and Port 1 respectively and these conditions can be met by connecting a load impedance with the same amount of the characteristic impedance to either Port 2 or Port 1, as shown in Fig. B-2.



(A)



(B)

Figure B-2: Configurations for the conditions $a_2 = 0$ (A) and $a_1 = 0$ (B) to determine the S-parameters of a two-port network. The characteristic resistances of both input and output connecting lines are the same as Z_0.

B.2 Conversion between Different Network Parameter Sets

All parameter sets provide equivalent descriptions of two-port networks and they can be converted into one another [149]. It is noted that in practical measurements, *S*-parameters are measured because of the difficulties in providing true short/open terminations at microwave frequencies, however, in the TCAD simulations, *Y*-parameters are first calculated. Here, we only list the conversions from the *Y*-parameters to the Z-, H-, S-parameters, which are used in our simulations:[6]

$$Z_{11} = \frac{Y_{22}}{D_Y},\ Z_{12} = \frac{-Y_{12}}{D_Y},\ Z_{21} = \frac{-Y_{21}}{D_Y},\text{and } Z_{22} = \frac{Y_{11}}{D_Y}; \qquad (B-6)$$

$$H_{11} = \frac{1}{Y_{11}},\ H_{12} = -\frac{Y_{12}}{Y_{11}},\ H_{21} = \frac{Y_{21}}{Y_{11}},\text{ and } H_{22} = \frac{D_Y}{Y_{11}}; \qquad (B-7)$$

$$S_{11} = \frac{(1 - Z_0 Y_{11})(1 + Z_0 Y_{22}) + Y_{12} Y_{21} Z_0^2}{N_Y}, \quad S_{12} = \frac{-2 Y_{12} Z_0}{N_Y},$$

$$S_{21} = \frac{-2 Y_{21} Z_0}{N_Y}, \text{ and } S_{22} = \frac{(1 + Z_0 Y_{11})(1 - Z_0 Y_{22}) + Y_{12} Y_{21} Z_0^2}{N_Y}, \qquad (B-8)$$

where $D_Y = Y_{11} Y_{22} - Y_{12} Y_{21}$, $N_Y = (1 + Z_0 Y_{11})(1 + Z_0 Y_{22}) - Y_{12} Y_{21} Z_0^2$ and Z_0 is the characteristic impedance which is conventionally set to be 50 Ω.

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