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PARAMETER EXTRACTION OF LDD SHORT-CHANNEL AND NARROW-WIDTH MOSFETS UNDER VARYING OPERATING CONDITIONS

by

Joseph Liang

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THESIS SUBMITTED IN PARTIAL FULFILMENT OF

THE REQUIREMENTS FOR THE DEGREE OF

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of

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ABSTRACT

With the demand for faster and denser circuits, the geometrical dimensions of a MOSFET must be shrunk to even smaller values. However, this reduced-dimension device comes at the price of a more complicated description of its electrical behaviour due to the increasing importance of higher order effects that are negligible in larger dimension devices, and a more complicated device structure using Lightly-Doped Drain (LDD) technology for improved device reliability. The goal of this research is to investigate in detail the electrical behaviour of LDD MOSFETs — both wide short-channel and long narrow-width devices under different biasing conditions and at varying operating temperatures.

While all electrical parameters are extracted and described, for the ohmic region of device operation, particular emphasis is placed on channel length (ΔL) and width (ΔW) reductions, and parasitic series resistance (R_p) and parallel conductance (G_p) at varying biasing and operating temperature conditions. For example, we found that R_p and ΔL decrease with increasing effective gate drive (V_{ge}), but they increase with drain (V_{ds}) and substrate (V_{sb}) biases. Both parasitic parameters R_p and ΔL increase with temperature. The results also show that G_p and ΔW increase with V_{ge}, V_{ds} and V_{sb}.

Our results clearly show that these parameters, together with other extracted parameters such as threshold voltage (V_T), intrinsic mobility (μ_o), mobility degradation constants (θ_0, θ_B), and drain modulation factor (δ), are required for the accurate modelling and simulation of the electrical characteristics of LDD MOSFETs.

DEDICATION

To my parents,

and my wife, Jane.

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Chapter 1 INTRODUCTION

In the past, the lack of detailed studies of both short-channel and narrow-width MOSFETs under different biasing conditions such as gate, drain and substrate biases, resulted in only limited MOSFET models that can be used accurately for implementation in technology characterization, process control, device design and even simulation packages. Moreover, studies of the effect of temperature variation on small geometry metal-oxide semiconductor field-effect transistor (MOSFET) provide a better understanding of the electrical characteristics of MOSFET. It is hope that the results from this research will lead to improved electrical characterization and better models for wide short-channel and long narrow-width LDD MOSFETs.

1.1 BACKGROUND

Although the first semiconductor device [1] was invented more than half a century ago, a thorough investigation of the parasitic resistance and conductance, and channel length and channel width reductions, respectively, of small geometry MOSFET only began in the late 1970's [2]. However, the phenomenon of these parasitic parameters affecting the performance of semiconductor circuits were first discussed in the 1970's by Gaensslen [3]. Since then, several publications [4-9] have described the effects of these parameters in small geometry MOSFET under different biasing conditions such as gate and drain biasing. This research was inspired by one of the first method of extracting parasitic resistance and channel length reduction of short-channel MOSFET

by Terada and Muta [2], in which some of the theoretical problems and limitations such as the carrier mobility effect and threshold voltage determination were discussed. After that, a large number of papers was published on the extraction techniques of small geometry MOSFET, mostly n-channel MOS transistors; some [10-22] of which were for short-channel devices while some of them [23-28] for narrow-width devices. The rapid development of the extraction methods is mostly spurred by the advancement of fabrication technologies in very large scale integration (VLSI) circuits.

As the progress of fabrication technologies pushed the feature size of a MOSFET into the submicrometer range, accurate modeling of its electrical characteristics becomes increasingly important. As the size of a MOSFET shrinks, the terminal current-voltage characteristics can no longer be accurately described by the ideal behavior of long- and wide-channel MOSFET. The presence of the second-order effects, which arise in a small-geometry MOSFET, becomes significant and cannot be ignored in modeling the device characteristics. Therefore, the electrical, not the physical, characteristics of small-geometry MOSFET are important and the parasitic parameters that are inherent in these miniature devices shall be included when modeling its behavior.

In this research, short-channel and narrow-width effects are the primary target in the investigation of second-order effects. The parasitic resistance and conductance, and the channel length and width reductions will be vigorously dealt with in this study. Other important parameters such as threshold voltage fluctuation, channel mobility degradation, and temperature-dependent parameters are also discussed. Part of the discussion will be dedicated to simulation of current-voltage characteristics of both a wide short-channel

and a long narrow-width MOSFETs using the parameters extracted.

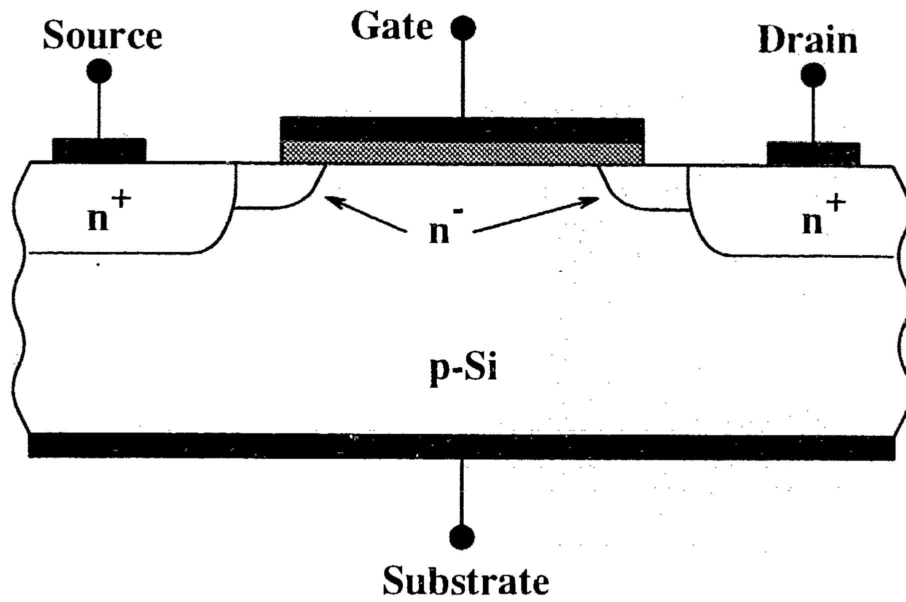
1.2 LDD MOSFET

Most of the research to-date have been carried out on n-channel MOS (NMOS) devices because the carrier mobility of the conventional NMOS transistor is much higher than that of p-channel MOS (PMOS) devices. This is largely due to the fact that the effective mass of electrons is smaller than that of holes. It is however, not always true for small geometry MOSFET. Chatterjee et. al. [29] had found that, for sub-micrometer MOSFETs, the saturation mobility of PMOS is comparable to that of NMOS.

The reliability of small-geometry MOSFET during operation degrades due to the following reasons :-

1. carriers (holes/electrons) are more susceptible to velocity saturation than long and wide-channel MOSFET, and hence the velocity of the carriers reach the saturation value at a lower biases; and
2. carriers are more prone to hot carrier effect, and under bias, this will cause their characteristics change with time.

Hence, a drain-engineered lightly-doped drain (LDD) MOSFET [30] has been developed, in which the lightly-doped or n^- regions are introduced between the drain and source diffusion regions and the channel, to minimize this problem. Fig 1.2.1 shows the cross-section of an n-channel LDD MOSFET. The source and the drain diffusion regions, normally written as n^+, have a higher doping concentration than the n^- regions. The resulting hot-electron effect is reduced because the doping concentration of the source and the drain regions near the channel is reduced. The electric field lines occurring near the



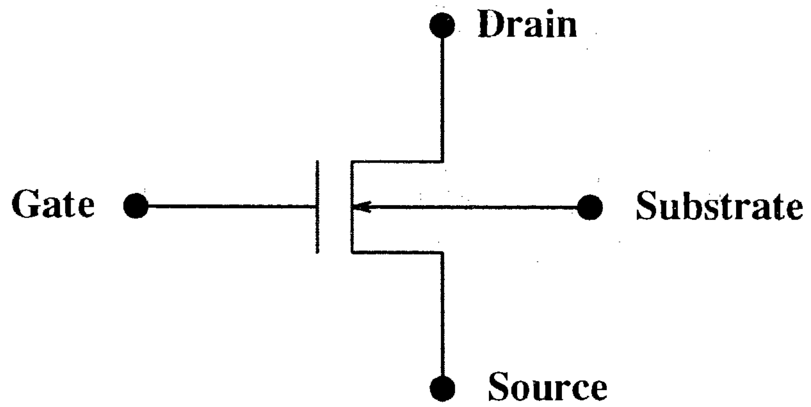


Figure 1.2.1. The cross-section of an n-channel LDD MOSFET. (a) Two-dimensional structure of an n-channel LDD MOSFET. (b) Symbolic representation of the device.

drain spread-out in the n^- region.

Compared to a conventional MOSFET, the LDD MOSFET has the following advantages.

1. In LDD MOSFET, the electric field intensity between the drain and the channel regions is reduced.
2. The breakdown voltage near the drain of LDD MOSFET is higher.
3. A LDD MOSFET has a higher saturation drain voltage $V_{D,sat}$.

Since the n^- regions improve increase the lifetime of the device, these advantages help propel LDD MOSFET to be used in today's microelectronic applications.

1.3 EFFECT OF OPERATING CONDITIONS ON MOSFET CHARACTERISTICS

To-date, MOS technology has progressed at an extremely rapid pace in terms of both propagation speed and level of integration. The silicon technology, that is used to fabricate the MOSFET, is today's most mature technology in the semiconductor industry. Since the midst of 1970's, MOS integrated circuits (ICs) have prevailed beyond what their bipolar counterparts dominated the IC market in the 1960's. Due to the advantages in device miniaturization, low power dissipation and relatively high yield, MOS ICs will continue to dominate the market for some time before another totally new technology is evolved.

The electrical performance of a MOSFET operating under different biasing conditions, such as variations in gate voltage and ambient temperature, will be altered due to the change of the physical properties of the materials which are used in the transistors.

The factors that affect the change in the physical properties of a MOSFET is categorized into two subsections described below.

1.3.1 Temperature

Some of the commonly used materials for MOSFET are single-crystalline silicon, poly-crystalline silicon and aluminum. Fig 1.3.1 [31] shows the temperature dependence of normalized resistivities of aluminum and heavily-doped silicon. The normalized resistivities of heavily-doped silicon increases with temperature. The property of changing resistivity with temperature is very useful in the modelling of MOSFET since it changes the operational speed of the system through the signal transmission delay.

Another important parameter that changes with temperature is the thermal conductivity of the material in the MOSFET. Fig 1.3.2 [31] shows that the thermal conductivities of silicon and aluminum decrease with increasing temperature. This variation of thermal conductivity with temperature is very important because, as the level of circuit integration increases, the heat generated by the individual transistors poses a serious problem. However, the problem of heat dissipation can be reduced if the operating temperature of MOSFET decreases and hence, permits a higher level of circuit integration.

The carrier mobility decreases with an increase in MOSFET operating temperature. This will result in a decrease in the propagation speed of the circuit. It is due to the fact that the scattering of charge carriers in silicon becomes more prononced at higher temp-

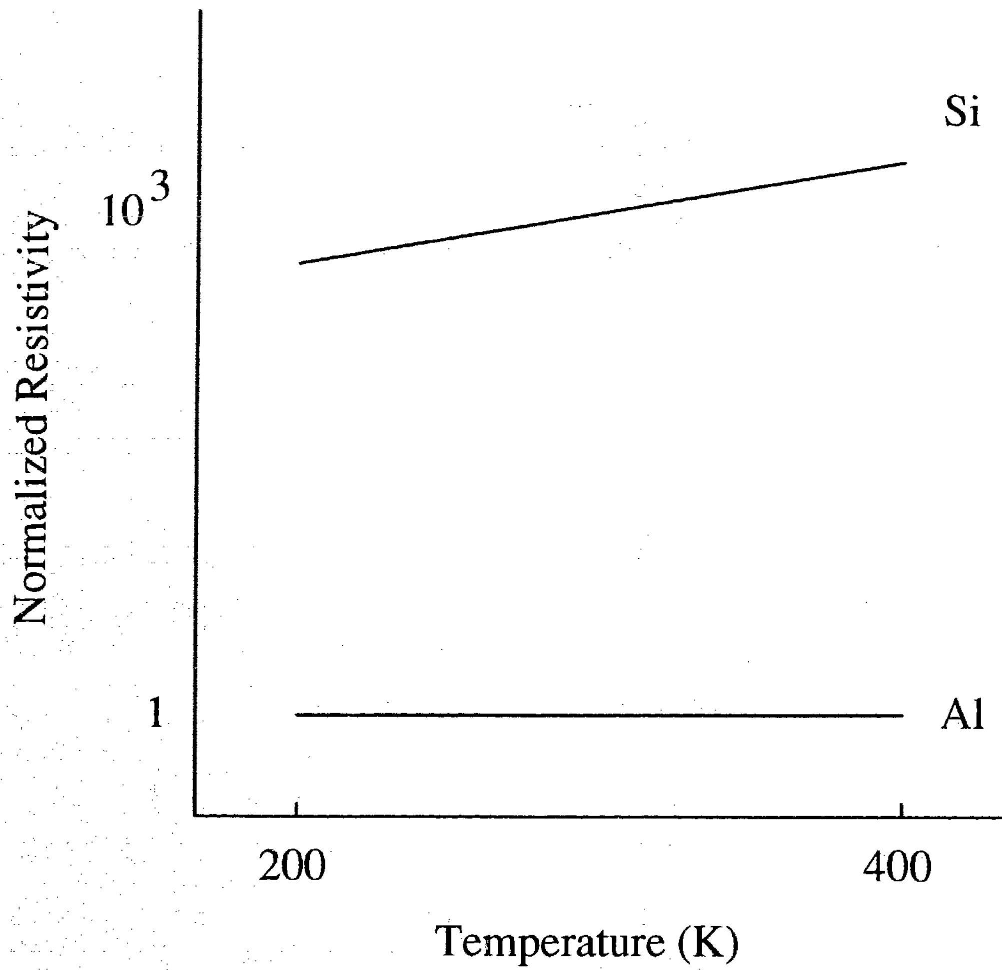


Figure 1.3.1. The temperature dependence of normalized resistivities of aluminum and heavily-doped silicon. The resistivity values of heavily-doped silicon is normalized to aluminum at different temperatures.

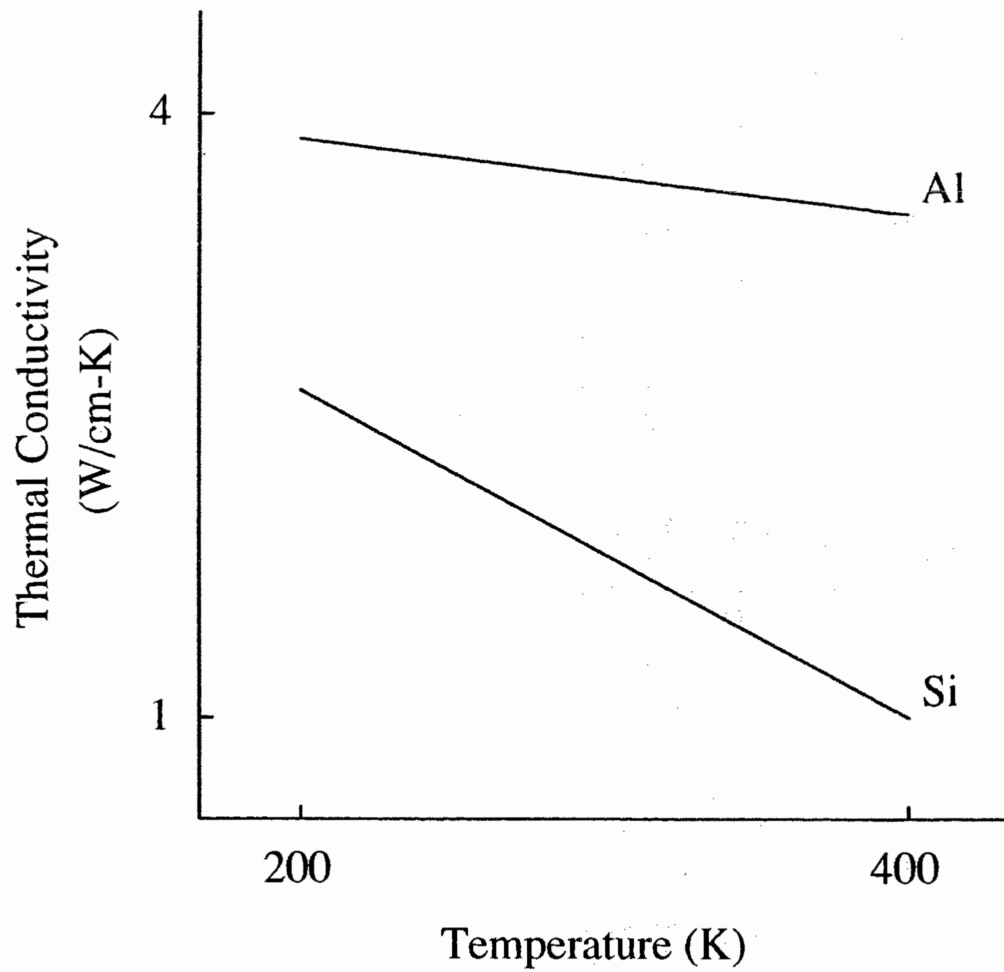


Figure 1.3.2. Measured thermal conductivities for silicon and aluminum versus temperature.

eratures. Fig 1.3.3 [31] shows the carrier mobility in silicon changes with temperature. As the temperature is lowered, the charge carriers suffer less phonon scattering, thus gaining higher energies without being scattered. This, in turn, increases the carrier mobility. However, if the energy of these carriers is high enough, then these "hot" carriers will degrade the performance of the transistor by creating electron-hole pairs, by interacting with the interface states and by being trapped in the oxide, causing the characteristics of the transistor to be changed.

The next important parameter that can be affected by temperature variation is the subthreshold region of MOSFET. It characterizes the behaviour of turning on or off in MOSFET. The lower the operating temperature, the steeper the subthreshold slope. This property of sharper subthreshold region is becoming more important than the mobility of charge carriers mentioned above. In order to achieve higher level of system integration, the individual transistor has to be shrunk according to specified down-scaling rules. By doing so, it is expected that the performance of the transistor can be improved accordingly. However, some undesirable characteristics hinder the expected result, and subthreshold slope is an important one. This non-scaling of the subthreshold slope may constrain lowering the power level that prevents further down-scaling of MOSFET. In [3], it is reported that the variation of temperature during the operation of the transistor can provide a unique way to scale down this parameter, along with other scaled transistor parameters resulting in a higher integration of circuits.

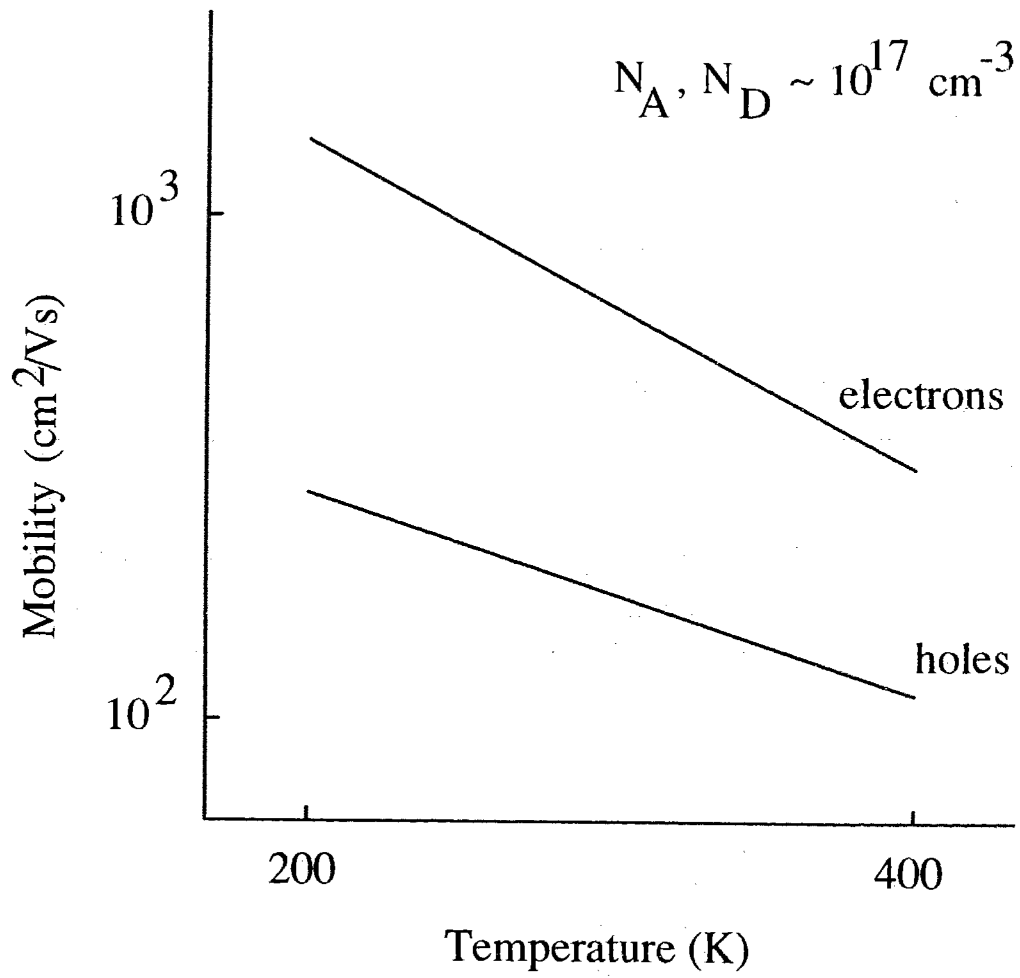


Figure 1.3.3. Mobility of holes and electron in silicon as a function of temperature.

1.3.2 Voltages

In the previous subsection, the electrical characteristics of a MOSFET can be changed by varying the operating temperature while maintaining the biases at the terminals constant. In this subsection, the temperature at which the MOSFET under studied, will be maintained constant. The operation of MOSFET under the influence of varying voltage biasing on the gate, drain and substrate terminals can alter the electrical characteristics of the transistor. This is due to the change of the intensity of the electric field acting on the carrier charges.

In Chapter 2, the theory of NMOS will be derived using Poisson's equation in which the charge carriers can be related to the presence of the electric field. The field lines, which are created by any applied bias impressed upon the gate, drain and substrate terminals, are able to modulate the concentration of the charge carriers in the inversion layer. The change in carrier concentration can gives rise to the change in the electrical performance of a MOSFET.

1.4 MOTIVATION

This research is mostly motivated by the fact that only a small fraction of the research to-date have investigated the effect of gate biasing voltage on the parasitic resistance and channel length reduction of conventional MOSFET. Since all previous research, except [32], were carried out by using conventional MOSFET, those models will be unacceptable for application to the LDD MOSFET due to the presence of the n^- regions. This clearly leaves a void in the development of parameter extraction techniques for small

geometry MOSFET, especially LDD MOSFET, and the performance of these transistors at different operating temperatures. In addition, drain and backgate (substrate) biasing can significantly affect the performance of MOSFET at different temperatures. Besides, there is a need to provide a comprehensive model for narrow-width MOSFET since there are only a limited number of models currently available.

One of the main objective of this research is to develop a method of extracting the parasitic resistance R_p and conductance G_p, and the channel length ΔL and width ΔW reductions of n-channel LDD MOSFET under different biasing conditions and at temperatures ranging from 200 K to 400 K. The remaining parts of the thesis details other relevant parameters and their extraction. The results and discussions of all parameters are then presented.

Chap' . 2 describes the theories of the operation of a MOSFET from weak to strong inversion region, and of short-channel, narrow-width and temperature-related effects. Chapter 3 describes the experimental details of the transistors used in this study. The experimental setup for the collection of experimental data is also included. The parameter extraction scheme for both the short-channel, and the narrow-width MOSFETs are presented in the following chapter. The results that were obtained from the measured data using the extraction technique are presented and discussed in Chapter 5. Finally, Chapter 6 gives the conclusion of this research and recommendation for future work.

Chapter 2 THEORETICAL BACKGROUND OF MOSFET

2.1 INTRODUCTION

One of the most widely used electronic devices in the semiconductor industry, particularly in digital IC applications, is the MOS transistor. As Sah [33] wrote, the MOS transistor is "The most abundant object made by man on this planet Earth!"

The principle of the surface field-effect transistor was first proposed by Lilienfeld [1] in 1930, followed by Heil [34] in 1935 and subsequently, was studied by Shockley and Pearson [35] in the late 1940's. In 1960, Kahng and Atalla [36] proposed and fabricated the first MOSFET using a thermally oxidized silicon structure. Since then, the basic device characteristics have been studied by a number of researchers like Ihantola and Moll [37], Hofstein and Heiman [38], and Sah [39]. The technology, application and device physics have been reviewed by Wallmark and Johnson [40], Richman [41], Brews [42] and Sze [31].

A perspective view of the basic structure of an enhancement mode NMOS transistor is illustrated in Fig 2.1.1. It is a typical four-terminal device consisting of a p-type semiconductor substrate acting as a backbone into which two heavily-doped n^+ regions are formed. The n^+ regions are known as the source and the drain of a MOSFET. Due to its symmetry as a single device, the source and the drain regions can be interchanged.

The so-called "metal" contact on top of the substrate is the gate terminal, which is usually made of either aluminum or heavily-doped polycrystalline silicon or a combina-

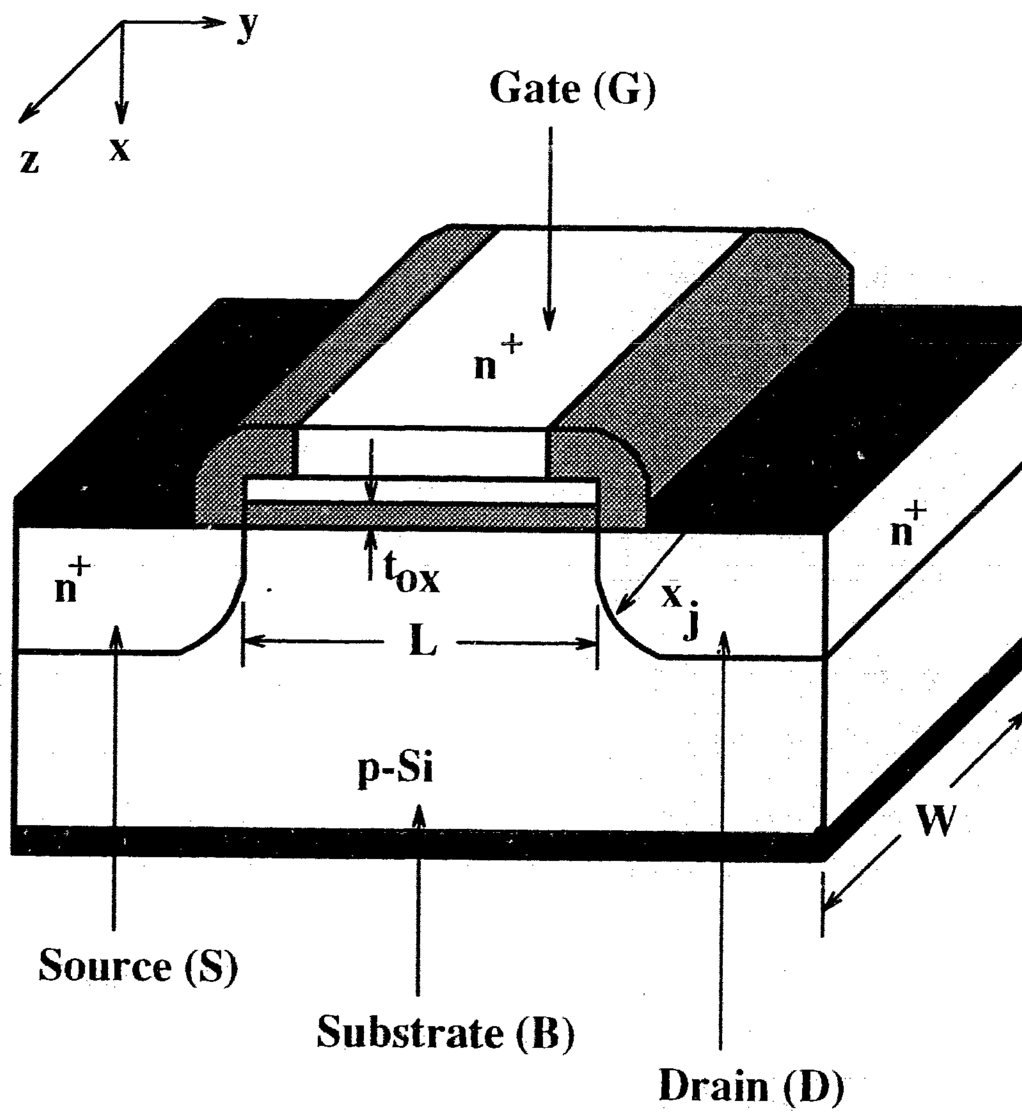


Figure 2.1.1. A three-dimensional view of a basic structure of an n-channel enhancement-mode MOSFET.

tion of silicide and polysilicon. A layer of silicon dioxide between the gate and the substrate contacts acts as a dielectric material. A thin silicon region below the oxide and bounded between the source and the drain regions forms the channel of the transistor.

The basic transistor parameters are the drawn channel length L or L_m; the drawn channel width W or W_m; gate oxide thickness t_{ox}; the junction depth x_j; and the substrate doping N_A. In an actual circuit, there is a thick layer of field oxide or other types of isolation surrounding each transistor to isolate from other transistors. Other transistor parameters can be obtained experimentally [45-55].

In this research, the source terminal will be used as a reference terminal. When no voltage is applied to the gate terminal, the only current that can flow from the source to the drain is the reverse leakage current. When a sufficiently large positive bias is applied to the gate and drain contacts, the source and the drain are then connected by a conducting channel through which a current can flow. The conductance of this inversion channel can be modulated by varying the gate, drain and substrate contacts, individually as well as through the operating temperature or device processing.

2.2 PHYSICS OF N-CHANNEL MOSFET

The operation of a LDD MOSFET is similar to that of conventional MOSFET. In this section, the fundamental physics of a conventional MOSFET in normal operation will be described. All the theories used in the derivation will be expressed in one dimension (1-D) unless it is specified, although more rigorous results can be obtained by solving the two-dimensional (2-D) or three-dimensional (3-D) equations. This section derives

the relation between the surface potential, space charge and electric field, and finally the current-voltage relationship of a MOSFET.

The electric potential distribution in a semiconductor can be described by using the 1-D Poisson's equation

$$\nabla^2 \psi_{1D} = -\frac{\rho(x)}{\epsilon_s} \tag{2.2.1}$$

where ψ is the electric potential in the semiconductor, ρ(x) is the electric charge density in the transistor, and ϵ_s is the permittivity of the semiconductor. The charge density ρ(x) in a MOS structure under equilibrium state is given by

$$\rho(x) = q\left(N_D^+ - N_A^- + p_p - n_p\right) \tag{2.2.2}$$

where N_D^+ and N_A^- are the densities of the ionized donors and acceptors, respectively; and p_p and n_p are the densities of mobile holes and electrons, respectively, in the substrate material. In the bulk of the semiconductor, charge neutrality must exist and so, Eqn (2.2.2) becomes

$$N_D^+ - N_A^- = n_{p0} - p_{p0} \tag{2.2.3}$$

where n_{p0} and p_{p0} are the corresponding electron and hole concentration in the bulk at equilibrium. The hole and electron concentrations as a function of ψ are given by

$$\begin{aligned} p_p &= p_{p0} \exp\left(-\psi/V_t\right) \\ n_p &= n_{p0} \exp\left(\psi/V_t\right) \end{aligned} \tag{2.2.4}$$

where V_t is the thermal voltage and is equal to kT/q , q is the electric charge, k is Boltzmann's constant and T is temperature in Kelvin.

Using Eqn (2.2.2) and (2.2.4), the resultant Poisson's equation becomes

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{p0}\left(e^{-\frac{\psi}{V_t}} - 1\right) - n_{p0}\left(e^{\frac{\psi}{V_t}} - 1\right)\right]. \tag{2.2.5}$$

Integrating the above equation from the bulk to the surface of the material gives rise to the relationship between the electric field ξ $\left(= \frac{\partial\psi}{\partial x}\right)$ and ψ, and after a few manipulations, Eqn (2.2.5) becomes

$$\xi^2 \approx (2V_t)^2\left(\frac{qp_{p0}}{2\epsilon_s V_t}\right)\left[\left(e^{-\frac{\psi}{V_t}} + \frac{\psi}{V_t} - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\frac{\psi}{V_t}} - \frac{\psi}{V_t} - 1\right)\right]. \tag{2.2.6}$$

By Gauss's Law, the space charge required to produce this field under the gate is given by

$$Q_s = -\epsilon_s\xi_s = \mp\frac{\sqrt{2}\epsilon_s V_t}{L_D}F\left(\frac{\psi_s}{V_t}, \frac{n_{p0}}{p_{p0}}\right) \tag{2.2.7}$$

where the subscript s denotes the surface of the substrate, and the Debye length is defined as

$$L_D = \left(\frac{\epsilon_s V_t}{qp_{p0}}\right) \tag{2.2.8}$$

and

$$F\left(\frac{\psi_s}{V_t}, \frac{n_{p0}}{p_{p0}}\right) = \left[\left(e^{-\frac{\psi}{V_t}} + \frac{\psi}{V_t} - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\frac{\psi}{V_t}} - \frac{\psi}{V_t} - 1\right)\right]^{\frac{1}{2}} \tag{2.2.9}$$

Fig 2.2.1 [31] shows a typical variation of space-charge density Q_s versus surface potential ψ_s in the semi-log scale. From this figure, the condition for strong inversion can be approximated as

$$\psi_s(inv) = 2\psi_B = 2V_t \ln\left(\frac{N_A}{n_i}\right) \tag{2.2.10}$$

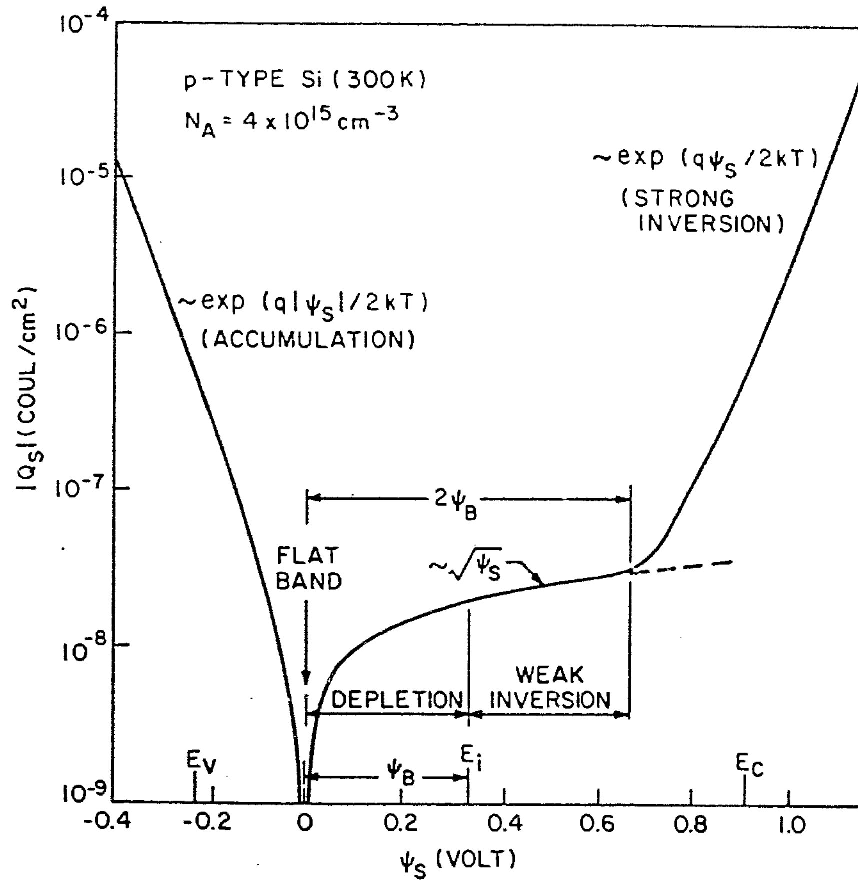


Figure 2.2.1. Variation of space-charge density Q_s in the semiconductor as a function of the surface potential ψ_s for a p-type silicon with $N_A = 4x10^{15}$ cm^{-3} at room temperature. (taken from [31], p.369)

where ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level and n_i is the intrinsic carrier concentration of silicon.

In the absence of any work function difference, the minimum gate voltage V_{gs} required for channel inversion will appear partly across the oxide and partly across the semiconductor, and so

$$V_{gs} = V_{ox} + \psi_s \tag{2.2.11}$$

where V_{ox} is the potential across the gate oxide. In real MOSFET operation, the voltage acquired from Eqn (2.2.11) is not enough to produce channel inversion condition. The required voltage has to take into account the difference of both the gate and the semiconductor work functions, the amount of channel implant and the total charge density in the gate oxide.

The value of gate voltage required to produce strong inversion should include two more components into Eqn (2.2.11). They are :

1. ϕ_{ms} which is the difference in work functions between the gate and the semiconductor.
2. Q_{ox} which is the total undesired charges present at the interface between the oxide and the surface of the semiconductor and in the oxide.

In order to flatten the energy band from the bulk to the surface of the semiconductor before inversion, a flatband voltage V_{fb} is required and is given as

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}. \tag{2.2.12}$$

The surface charge density Q_s is the sum of the inversion layer charge density Q_I and the ionized charge Q_A in the depletion region. Q_I plays a dominant role during strong

inversion condition. $Q_I(y)$ is in the direction of the channel and can be equated to

$$Q_I(y) = Q_s(y) - Q_A(y). \tag{2.2.13}$$

The total current density in the channel consists both the drift and diffusion currents. The drift current component dominates the total current in strong inversion region while the diffusion component is the dominant term in the weak inversion condition. Hence, during strong inversion condition the drain current I_{ds} can be approximately equated to

$$I_{ds} = \mu W Q_I(y) \frac{\partial \psi_s}{\partial y} \tag{2.2.14}$$

assuming $Q_I(y)$ is very close to $Q_s(y)$; μ is the carrier mobility in the channel and is assumed constant.

Integrating Eqn (2.2.14) along the channel gives (see Appendix A)

$$I_{ds} = \frac{\mu C_{ox} W}{L} \left[\left(V_{gs} - \psi_s - V_{fb} - \frac{V_{ds}}{2}\right) V_{ds} - \frac{2\gamma}{3}\left((V_{ds} + \psi_s)^{\frac{3}{2}} - (\psi_s)^{\frac{3}{2}}\right)\right] \tag{2.2.15}$$

where γ is called the body effect factor given by

$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}}. \tag{2.2.16}$$

Eqn (2.2.15) predicts that, for a given V_{gs}, the drain current I_{ds} first increases linearly with drain voltage V_{ds} and then gradually levels off. In the linear region of operation where V_{ds} is small, Eqn (2.2.15) reduces to

$$I_{ds} = \frac{\mu C_{ox} W}{L}\left[(V_{gs} - V_T)V_{ds} - \frac{1}{2}(1+\delta)V_{ds}^2\right] \tag{2.2.17}$$

where δ is given by

$$\delta = \frac{\gamma}{2\sqrt{\psi_s}} \tag{2.2.18}$$

and V_T is called the threshold voltage given by

$$V_T = \psi_s + V_{fb} + \gamma \psi_s^{\frac{1}{2}}. \qquad (2.2.19)$$

If $V_{ds} << (V_{gs}-V_T)$, Eqn (2.2.17) can be reduced further to give

$$I_{ds} = \frac{\mu C_{ox} W}{L}[(V_{gs} - V_T)V_{ds}]. \qquad (2.2.20)$$

If V_{ds} is increased to a point where $V_{ds} = V_{ds,sat}$, I_{ds} in Eqn (2.2.20) is no longer increases linearly with V_{ds}. This $V_{ds,sat}$, called the saturation drain voltage, is extracted from Eqn (2.2.17) by setting $dI_{ds} / dV_{gs} = 0$, and is given as

$$V_{ds,sat} = \frac{V_{gs} - V_T}{1 + \delta}. \qquad (2.2.21)$$

The corresponding saturation drain current $I_{ds,sat}$ is

$$I_{ds,sat} = \frac{\mu C_{ox} W}{2L}\frac{(V_{gs} - V_T)^2}{1 + \delta}. \qquad (2.2.22)$$

Note that $I_{ds,sat}$ in Eqn (2.2.22) does not depend on V_{ds} but increases quadratically with $(V_{gs}-V_T)$.

When $V_{gs} < V_T$, the surface of the semiconductor is weakly inverted and the corresponding drain current is called the subthreshold current. This region is particularly important for scaled transistors because the subthreshold region determines the turn-on/off characteristics of a MOSFET. The subthreshold current I_{sub} can be written as [31]

$$I_{sub} = -qAD_n\frac{dn}{dy} \qquad (2.2.23)$$

where A is the area of the cross-section of the current flow and D_n is the diffusion coefficient of electrons.

The subthreshold slope, S, can be used to deduce the steepness of the subthreshold region and is defined as [31]

$$S = \ln 10 * \frac{dV_{gs}}{d\ln\left(I_{sub}\right)}. \tag{2.2.24}$$

For a long and wide channel MOSFET, S is given by

$$S = V_t \ln\left(10\right)\left[1 + \frac{C_D(\psi_s)}{C_{ox}}\right]\left\{1 - \left(\frac{2}{a^2}\right)\left[\frac{C_D(\psi_s)}{C_{ox}}\right]^2\right\} \tag{2.2.25}$$

where $C_D(\psi_s)$ is the depletion capacitance evaluated at ψ_s and a is defined as

$$a = \frac{\sqrt{2}\epsilon_s}{C_{ox}L_D}. \tag{2.2.26}$$

Note that the a values increase with increasing doping concentration and oxide thickness.

2.3 SHORT-CHANNEL EFFECTS

Since the beginning of the IC era, the minimum feature length has been reduced by two orders of magnitude [31]. As the channel length L is reduced, the characteristics of the transistor depart from that of corresponding long channel transistor. This departure arises as a result of more than 1-D high electric field distribution in the channel region and stronger drain induced barrier lowering (DIBL).

For a given channel doping concentration and decreasing L, the depletion layer widths of the source and the drain junctions become comparable to the channel depth. 1-D theory is not sufficient to describe the behaviour of a scaled transistor. Hence, 2-D, or perhaps 3-D, numerical analysis must be applied to understand and get accurate results. However, this technique requires considerable amount of tedious calculation time and the physics involved is complex.

For this reason, it is necessary to develop a much simpler theory or model by using an empirical or semi-empirical approach, that is suitable for circuit simulation or for readers who do not possess strong physics background. A simple approach is to adopt the characteristics of the long channel transistor and to modify it to account for short-channel or narrow-width effects. Recently, this approach has been used and demonstrated in publications such as [63-68]. Only some of the short-channel and narrow-width effects will be studied in this research, and they will be briefly described in the following subsection.

2.3.1 Definition of Short-Channel Device

Sze [31] has defined a short-channel device based on two criteria :

1. the length of the channel is considered short if there is a 10% departure of the short-channel I_{ds} from linear dependence upon 1/L.
2. a device is considered short-channel device if there is a 10% increase in the $(I_{ds,short} - I_{ds,long}) / I_{ds,long}$.

In addition, if L is in the same order of mangitude as the source and the drain depletion depths, then the device is considered short according to Ong [4].

2.3.2 Threshold voltage

In Section 2.2, the V_T expression in Eqn (2.2.19) is valid as long as the channel is long and wide, and does not violate the definition for short-channel mentioned above. As L decreases, V_T decreases rapidly and the expression in Eqn (2.2.19) has to be

modified to include the corresponding short-channel effects. In this subsection, V_T for short-channel transistor will be discussed.

The concept of charge sharing both provides physical insight into the development of the V_T expression and predicts the trend correctly. From Eqn (2.2.19), the total amount of charge under the gate determines a portion of V_T. If L is much longer than either the source or the drain depletion region, the charge sharing which occurs from these regions can be neglected.

If L is reduced to a distance comparable to the source or the drain depletion widths, part of the charge which is induced under the gate is also contained in the source and the drain regions. Fig 2.3.1 [8] shows the charge sharing model for short-channel MOSFET. In other words, charge sharing is occurring in both the source and the drain depletion regions with the gate region. This implies that the total effective charge induced under the gate can no longer be approximated by a rectangular shape. Hence the amount of charge reflected to the gate can be expected to reduced. This, in turn, decreases V_T as L decreases.

The change in V_T can be calculated based on this model. Eqn (2.2.19) is rewritten in a different form where the last term is related to the depletion region charge density Q_D as

$$V_T = \psi_s + V_{fb} + \frac{Q_D}{C_{ox}} \tag{2.3.1}$$

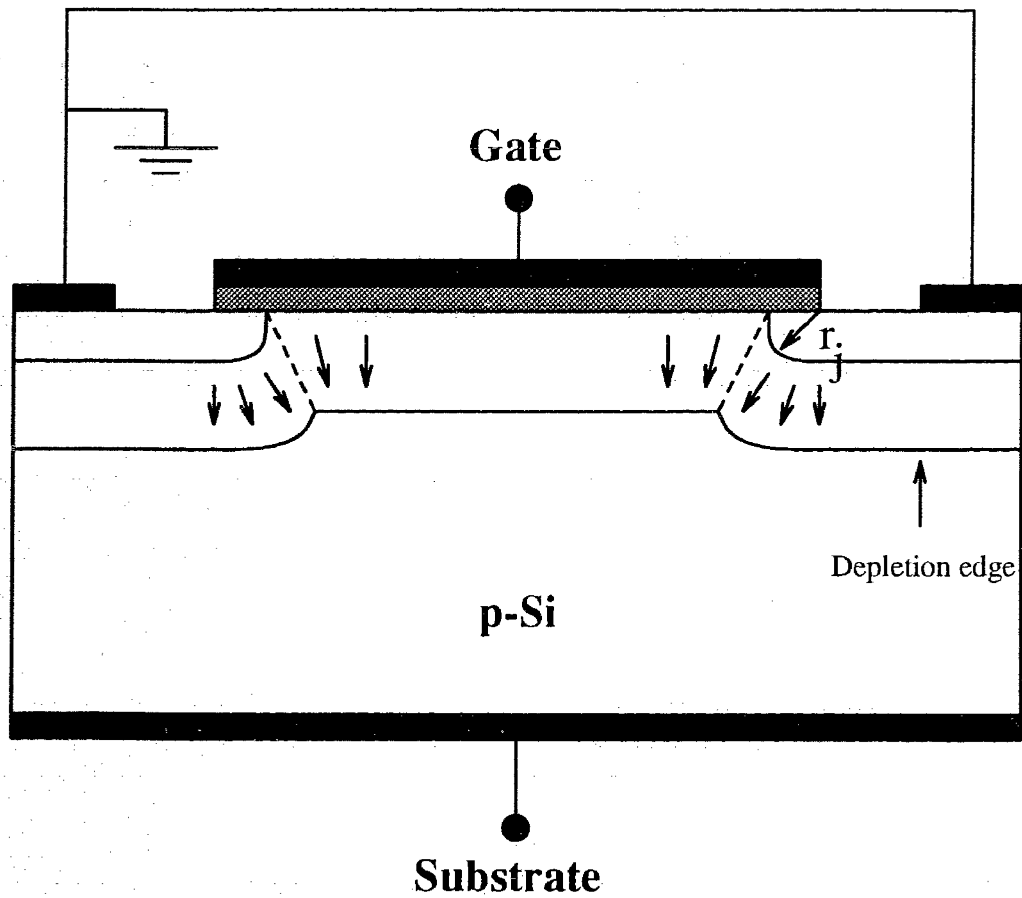


Figure 2.3.1. Charge sharing model in a short-channel MOSFET.

where

$$Q_D = \sqrt{2\epsilon_s q N_A \psi_s}. \tag{2.3.2}$$

The application of drain and substrate voltage V_{sb} can be easily incorporated in the above equation by changing the term ψ_s to $(\psi_s + V_{ds} + V_{sb})$.

The charge sharing model uses the effective depletion charge density $Q_{D,eff}$ to replace Q_D and Eqn (2.3.1) becomes

$$\begin{aligned} V_T &= \psi_s + V_{fb} + \frac{Q_{D,eff}}{C_{ox}} \\ &= \psi_s + V_{fb} + \frac{Q_{D,eff}}{Q_D}\gamma\sqrt{\psi_s + V_{ds} + V_{sb}}. \end{aligned} \tag{2.3.3}$$

This equation is similar to Eqn (2.2.19) except that γ becomes $(\gamma\ Q_{B,eff}\ /\ Q_B)$. The enclosed total charge that is induced under the gate can be approximated by a trapezoidal region, as shown in Fig 2.3.1. A simple geometry derivation yields

$$\frac{Q_{D,eff}}{Q_D} = 1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2w_D}{r_j}} - 1\right) \tag{2.3.4}$$

where r_j is the radius of curvature of the source and the drain junctions and w_D is the maximum depletion layer depth given by

$$w_D = \sqrt{\frac{2\epsilon_s(\psi_s + V_{ds} + V_{sb})}{qN_A}}. \tag{2.3.5}$$

By substituting Eqn (2.3.4) into the Eqn (2.3.3), the new expression for V_T becomes

$$V_T = \psi_s + V_{fb} + \gamma\sqrt{\psi_s + V_{ds} + V_{sb}}\left[1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2w_D}{r_j}} - 1\right)\right] \tag{2.3.6}$$

For small V_{ds}, the above equation shows that the difference between the source and the drain depletion depths is negligible. For large V_{ds} or $V_d >> V_s$, the square bracket of

the last term in the previous equation is replaced by

$$\left[1 - \frac{r_j}{2L}\left(\sqrt{1 + \frac{2w_d}{r_j}} - 1\right) - \frac{r_j}{2L}\left(\sqrt{1 + \frac{2w_s}{r_j}} - 1\right)\right] \tag{2.3.7}$$

where w_d and w_s are the depletion depths of the drain and the source, respectively. Fig 2.3.2 [4] shows a schematic representation of the effect of drain and substrate voltage on V_T. The threshold voltage shift ΔV_T due to short-channel effect is

$$\Delta V_T = -\frac{Q_{D,eff}}{C_{ox}}\frac{r_j}{2L}\left[\left(\sqrt{1 + \frac{2w_d}{r_j}} - 1\right) + \left(\sqrt{1 + \frac{2w_s}{r_j}} - 1\right)\right]. \tag{2.3.8}$$

In practice, the above formulation is too complicated to be used in actual calculation and simulation. However, it can been shown from Tsividis [5], that Eqn (2.3.4) can be approximated by

$$\frac{Q_{D,eff}}{Q_D} = 1 - \alpha_1 \frac{w_D}{L} \tag{2.3.9}$$

where α_1 is an empirical fitting parameter. Using Eqn (2.3.9), the corresponding empirical V_T expression becomes

$$V_T = \psi_s + V_{fb} + \gamma\sqrt{\psi_s + V_{ds} + V_{sb}}\left[1 - \frac{\alpha_1 \zeta}{L}\left(\sqrt{\psi_s + V_{ds} + V_{sb}}\right)\right] - \frac{\alpha_2 V_{ds}}{L} \tag{2.3.10}$$

where ζ is defined as

$$\zeta = \sqrt{\frac{2\epsilon_s}{qN_A}} \tag{2.3.11}$$

and the corresponding ΔV_T is given by

$$\Delta V_T = 2\alpha_1 \frac{\epsilon_s}{\epsilon_{ox}} \frac{t_{ox}}{L}[(\psi_s + V_{sb}) + \alpha_2 V_{ds}] \tag{2.3.12}$$

where α_2 is an empirical fitting parameter for the V_{ds} effect.

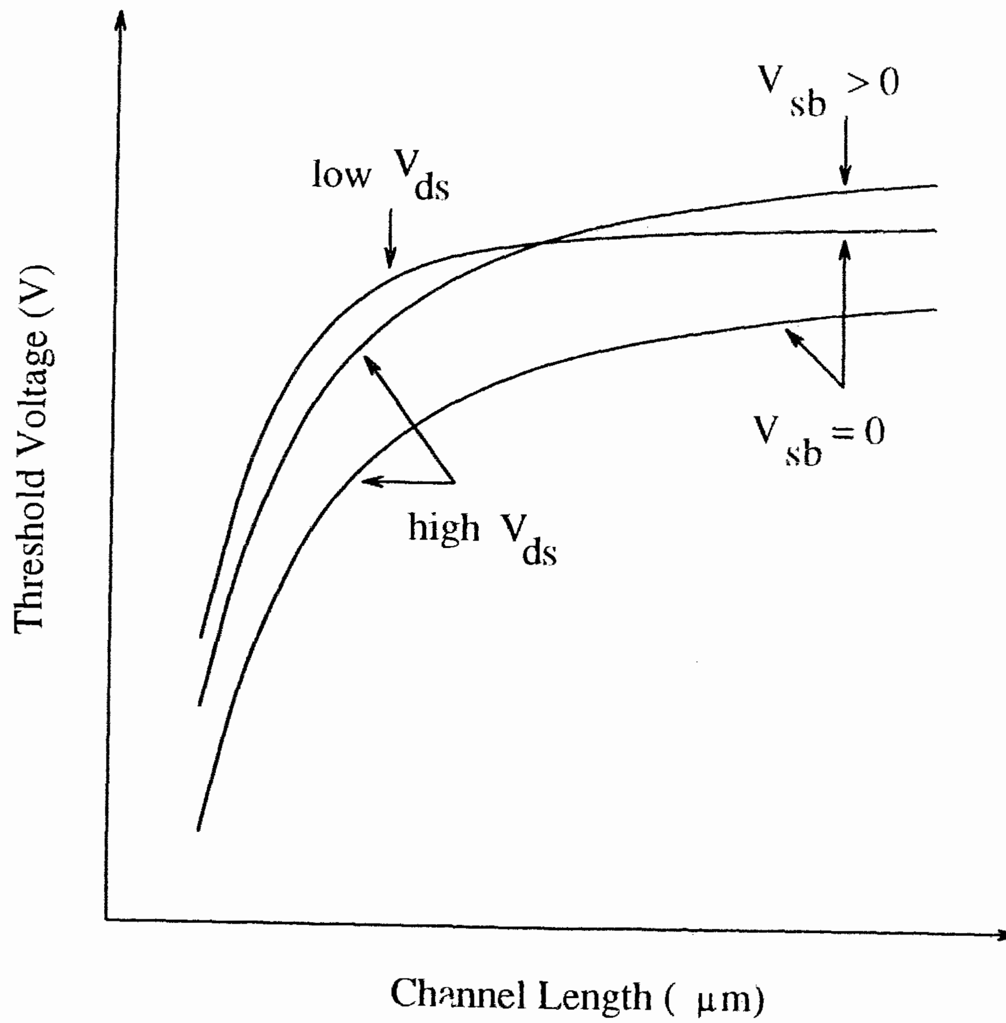


Figure 2.3.2. A schematic representation of the effect of drain and substrate biasing on V_T for short-channel devices.

2.3.3 Subthreshold Slope

The short-channel effect is also manifested in the subthreshold slope characteristics. Eqn (2.2.25) has to be modified to include short-channel effect by the charge sharing model. The term $C_D(\psi_s)$ in Eqn (2.2.25) decreases due to charge sharing with the source and the drain junctions. Since weak inversion occur in the subthreshold region, the charge carriers in the channel can be approximately equal to the depletion charge Q_D. For short-channel transistor with a uniformly-doped channel, the effective depletion capacitance $C_{D,eff}(\psi_s)$ is defined as

$$C_{D,eff} = C_D\left(1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2w_D}{r_j}} - 1\right)\right). \tag{2.3.13}$$

And the corresponding new subthreshold slope S_l is

$$S_l = V_t \ln(10)\left[1 + \frac{C_{D,eff}(\psi_s)}{C_{ox}}\right]\left\{1 - \left(\frac{2}{a^2}\right)\left[\frac{C_{D,eff}(\psi_s)}{C_{ox}}\right]^2\right\}. \tag{2.3.14}$$

As transistors are fabricated with shorter channel lengths, the slope of the subthreshold current can be reduced.

2.3.4 Channel Length Reduction

In this section, the channel length reduction ΔL corresponds with the reduction of the channel near the drain when the device is operating in the ohmic region. In a long channel MOSFET, the applied drain voltage V_{ds} has a negligible effect on the lateral electric field in the channel region between the source and the drain. The electric field is defined as

$$\xi = \frac{V}{y} \tag{2.3.15}$$

where V is the applied voltage across the channel and y is the channel distance.

As channel length becomes shorter in a conventional MOSFET, the lateral field increases, and this will cause problem in the reliability of the device due to hot-electron effect near the drain region. Since LDD devices will be used in this research, the reliability problem is minimized by spreading out the electric field lines in the n^- region near the drain. For LDD devices, the reduction ΔL will mainly occurr in the n^- region near the drain. The reduction ΔL in a short-channel device becomes significant in proportion to the drawn channel length L_m and cannot be ignored, and hence the conducting channel length will be different to L_m given as

$$L_e = L_m - \Delta L \tag{2.3.16}$$

where L_e is the effective channel length.

Since the doping concentration in the n^- region is about 10 to 100 times lower than that of the actual diffusion junctions, any biasing on the gate, drain and substrate will be able to modulate the doping concentration in the n^- region, and hence influence ΔL. For instance, when a small V_{ds} is applied to the drain and a fixed V_{gs} at the gate, the channel will be formed linking the drain to the source. As V_{ds} increases, the concentration of charge carriers in the channel approaches to that of the n^- region near the drain, and hence increases L_e.

2.3.5 Parasitic Resistance

In a real MOSFET, the resistance of the channel is known as the intrinsic or channel resistance while the resistance of the current path outside the channel boundary is called

the extrinsic or parasitic resistance. The derivation of I_{ds} in Section 2.2 assumes that the MOSFET has a long and wide channel in which the value of the intrinsic resistance is much greater than the parasitic resistance. Normally, the off-state of the transistor has a resistance in the order of megaohm (MΩ) and the on-state has a few kiloohm (kΩ).

As a MOSFET is scaled down, the parasitic resistance R_p becomes significant and comparable to the resistance of the channel R_c. Fig 2.3.3 shows the symbolic representation of a MOSFET with the associated source and drain parasitic resistances. To further illustrate each components of R_p, Fig 2.3.4 shows the resistive path of current traversing in a LDD MOSFET. Due to the nature of n^- regions, the resistance R_{int} is a combination the accumulation resistance R_{ac} of carriers, the spreading resistance R_{sp} of current path from n^- regions to n^+ regions and the resistance under the sidewall spacer R_{si} from fringing field; and it is a function of voltage biasing which will be described in Chapter 5. The external resistance R_{ext} is the sum of the resistance between the spacer oxide and the contact R_{sx}, resistance due to current crowding R_{cw} under the contact, contact resistance R_c between the metal and silicon; and metal resistance R_m. In this research, it is assumed that the extrinsic resistance at the source side is similar to that of the drain, and the sum of these two components is equivalent to R_p. From Fig 2.3.5, R_p can be summarized into [56-60]

1. constant resistance of the n^+ regions,
2. variable resistance of the n^- regions, and
3. resistance due to process technology.

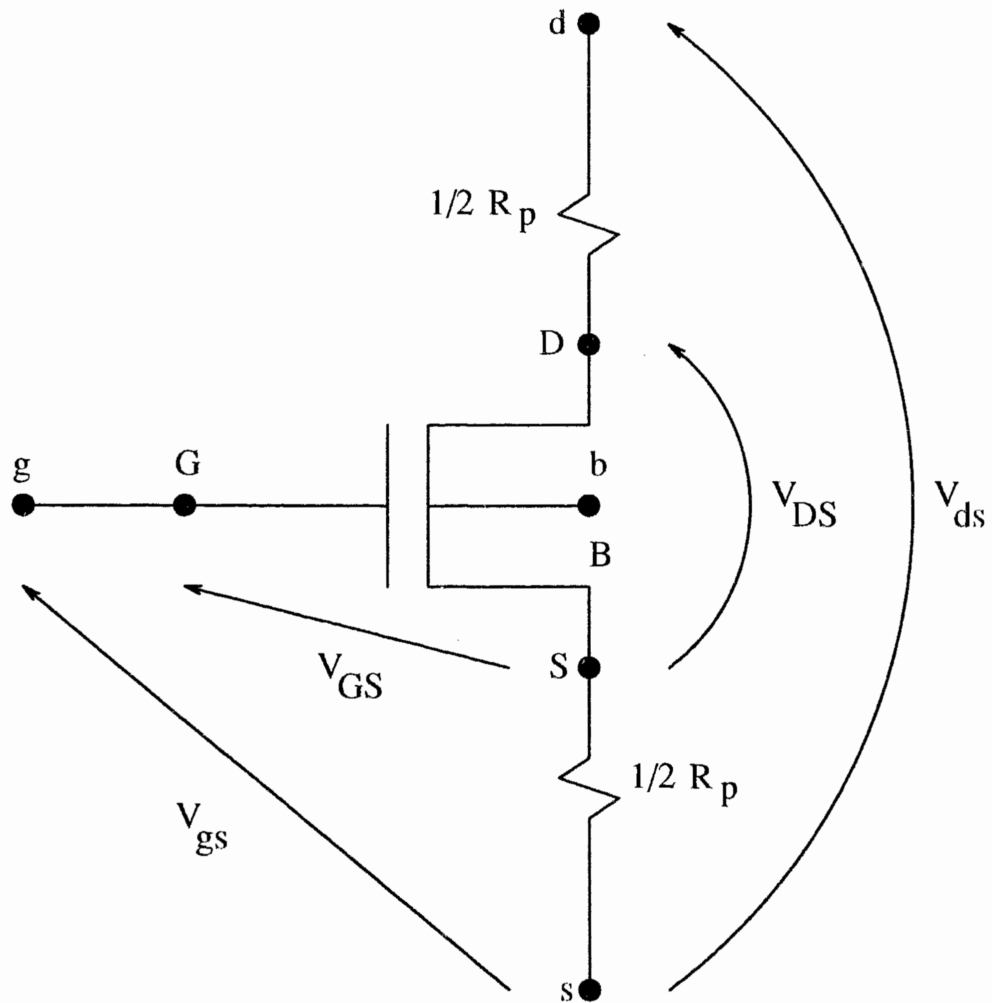


Figure 2.3.3. Device representation of a short-channel MOSFET.

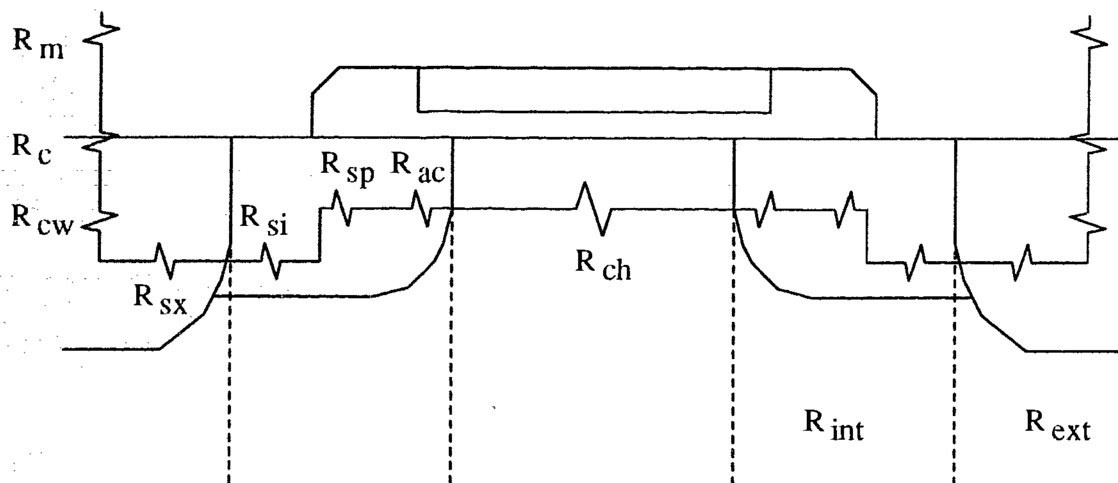


Figure 2.3.4. A resistive current path in a LDD MOSFET. R_{ch} represents the channel resistance, R_{ac} = accumulation resistance, R_{sp} = spreading resistance, R_{si} = resistance under sidewall spacer, R_{sx} = resistance between spacer oxide and contact, R_{cw} = resistance due to current crowding under contact, R_c = contact resistance between metal and silicon, R_m = metal resistance, R_{int} = internal resistance; and R_{ext} = external resistance.

For a sub-micron device, the voltage between the source and the drain is different from the applied drain voltage V_{ds} at the terminals. From Fig 2.3.3, the effective drain voltage V_{DS} appears across the channel is less than V_{ds} by an amount equal to the voltage drop across R_p, and V_{DS} is given as

$$V_{DS} = V_{ds} - I_{ds}R_p. \tag{2.3.17}$$

By the same reason, the effective gate voltage V_{GS} is

$$V_{GS} = V_{gs} - \frac{I_{ds}R_p}{2}. \tag{2.3.18}$$

2.3.6 Mobility and Velocity Saturation

Another short-channel effect is the effective mobility of the charge carriers. The mobility μ, appeared in Section 2.2, is assumed constant with respect to the applied electric field variation. However, it has been mentioned in the past [7] that the effective mobility μ_e of carriers in the inversion layer is smaller than that of the bulk. The reason is that the carriers are confined to a region very close to the silicon-silicon dioxide interface, and are influenced by the thickness of the inversion layer. This makes μ_e of a MOSFET to be dependent on the surface roughness and the number of interface traps present which can trap and retard carriers motion.

At a given temperature, μ decreases with increasing effective transverse field ξ_x, defined as the electric field averaged over the electron distribution in the inversion layer,

and is given by [31]

$$\xi_x = \frac{Q_A + 2Q_I}{2\epsilon_s}. \tag{2.3.19}$$

For a given ξ_x, the velocity is proportional to the longitudinal electric field ξ_y at low ξ_y, and the proportionality constant is μ. Fig 2.3.5 [5] shows a typical graph of electron drift velocity v_d against ξ_y. However, as ξ_y increases, v_d tends to saturate to a constant value $v_{d,sat}$. This phenomenon is called velocity saturation.

At low V_{ds}, the effective surface mobility μ_e can be described by the semi-empirical equation

$$\mu_e = \frac{\mu_o}{1 + \alpha\xi_x} \tag{2.3.20}$$

where μ_o is the low field mobility and α is a fitting parameter. Using

$$Q_A = \gamma C_{ox}(\psi_s + V_{sb})^{\frac{1}{2}} \tag{2.3.21}$$

and

$$Q_I = C_{ox}\left(V_{gs} - V_T - \frac{(1+\delta)}{2}V_{ds}\right) \tag{2.3.22}$$

into Eqn (2.3.20), it becomes

$$\mu_e = \frac{\mu_o}{1 + \theta f} \tag{2.3.23}$$

where θ is given by

$$\theta = \frac{\alpha C_{ox}}{2\epsilon_s} \tag{2.3.24}$$

and f is given by

$$f = V_{ge} + 2\gamma(\psi_s + V_{sb})^{\frac{1}{2}} \tag{2.3.25}$$

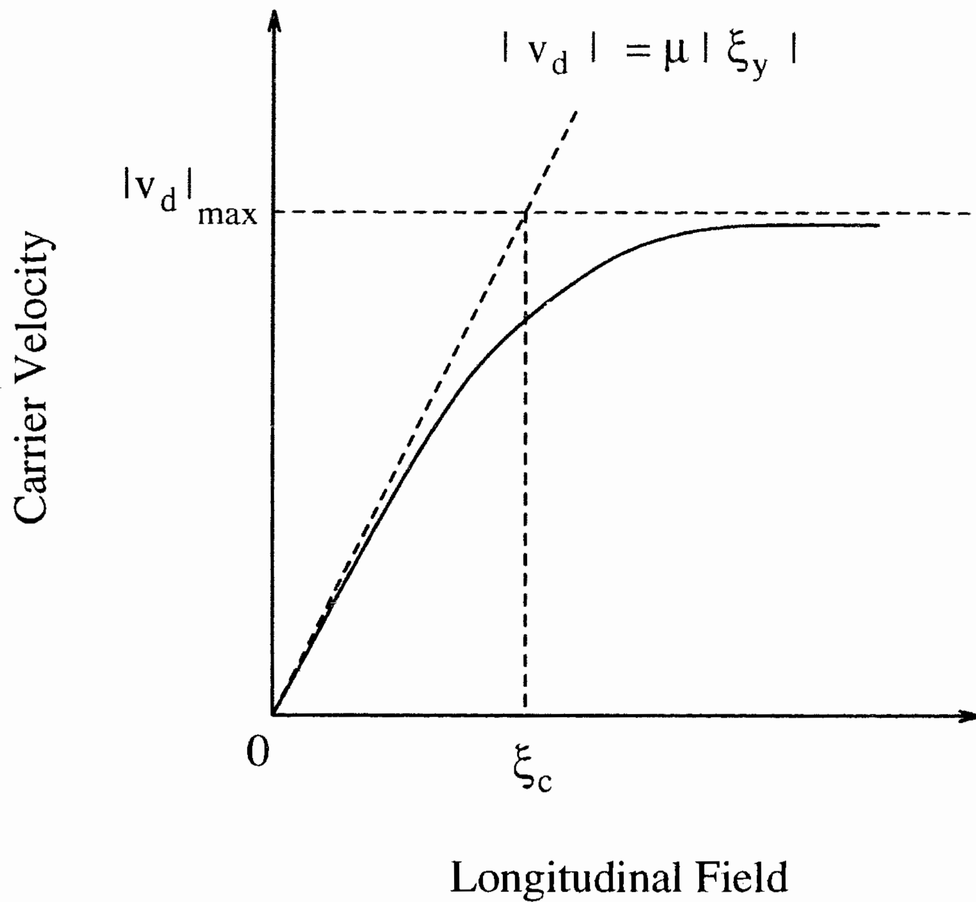


Figure 2.3.5. A typical plot of magnitude of carrier velocity in the inversion layer versus magnitude of longitudinal component of the electric field.

where V_{ge} is the effective gate voltage given as

$$V_{ge} = V_{gs} - \left(V_T + \frac{(1+\delta)}{2} V_{ds} \right). \tag{2.3.26}$$

In the past, several semi-empirical approximations for μ_e have been presented [20, 43-47], and one of the most common expressions of μ_e for small V_{ds} is given as

$$\mu_e = \frac{\mu_o}{1 + \theta_0 V_{ge} + \theta_B V_{sb}} \tag{2.3.27}$$

where θ_0 and θ_B are fitting parameters responsible for V_{ge} and V_{sb}, respectively.

2.4 NARROW-WIDTH EFFECTS

In the past, most of the research on small geometry MOSFET was concentrated on short-channel effects. However as scaled MOSFET shrinks all dimensions, a better understanding of the narrow-width effects is required to complement the existing research on short-channel MOSFET. Moreover, past researches [5-8] have indicated that the channel width W of a MOSFET has a significant effect on its electrical behaviour.

Due to complex field distribution in the channel, simple models that deal with small geometry MOSFETs are difficult to provide. For this reason, this section will concentrate on long and narrow channel MOSFET. Normally, a MOSFET is considered narrow when the width is in the same order of magnitude as the depletion layer depth [4].

2.4.1 Threshold Voltage

The charge sharing model, described in the previous section, is also used here to derive the V_{TW} expression for narrow-width MOSFET. Fig 2.4.1 [6] shows the cross-section of a MOSFET parallel to the channel width. The gate material overlaps the field

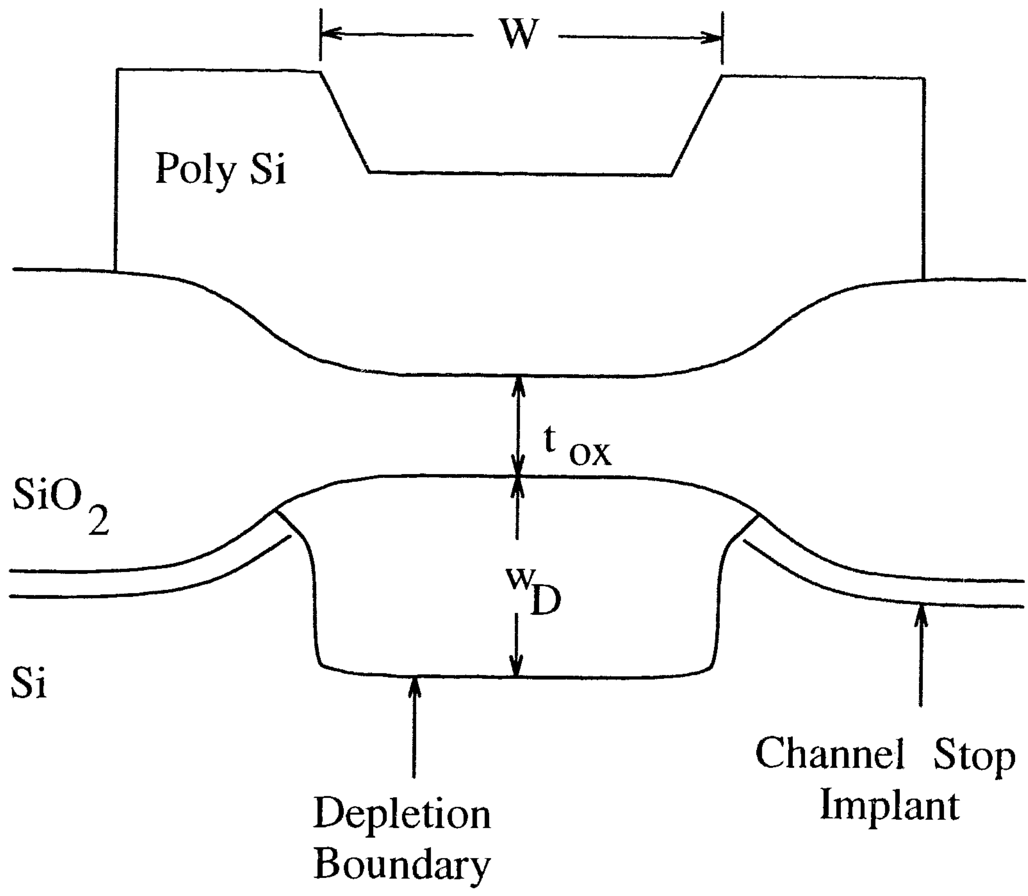


Figure 2.4.1. The width cross-section of a MOSFET.

oxide on both sides of the thin gate oxide. The depletion region is not just the area directly below the gate oxide but also include both sides of the field oxide. This is because some of the fringing field lines from the gate terminate on the ionized acceptor atoms on both sides of the field oxide. As W is reduced, these sides become a large percentage of the total width. Thus a higher V_{gs} is required to deplete these ionized acceptor atoms before an inversion layer can be formed.

Using a simple geometry derivation, the effective depletion charge density $Q_{DW,eff}$ is [4]

$$\frac{Q_{DW,eff}}{Q_D} = 1 + \frac{\pi}{2}\frac{w_D}{W}. \tag{2.4.1}$$

The threshold voltage shift ΔV_{TW} for narrow channel is given by

$$\begin{aligned} \Delta V_{TW} &= \left(\frac{Q_{DW,eff}}{Q_D} - 1\right)\gamma\sqrt{\psi_s + V_{sb}} \\ &= \frac{\pi}{2}\frac{w_D}{W}Q_D. \end{aligned} \tag{2.4.2}$$

The corresponding empirical expressions for V_{TW} with narrow-width effects has been shown as [5]

$$V_{TW} = \psi_s + V_{fb} + \gamma\sqrt{\psi_s + V_{sb}}\left[1 + \frac{\alpha_3\pi\zeta}{2W}\left(\sqrt{\psi_s + V_{sb}}\right)\right] \tag{2.4.3}$$

and ΔV_{TW} is given by

$$\Delta V_{TW} = \alpha_3\pi\frac{\epsilon_s}{\epsilon_{ox}}\frac{t_{ox}}{W}[(\psi_s + V_{sb})] \tag{2.4.4}$$

where α_3 is an empirical fitting parameter.

Note that the ΔV_{TW} in the narrow-width MOSFET represents an increase while ΔV_T of the short-channel effects tend to lower it. If both L and W of a MOSFET are reduced

simultaneously, the short- and narrow-channel effects often tend to cancel, so that the threshold voltage of a small geometry MOSFET remains relatively constant.

2.4.2 Subthreshold Slope

Using the same procedure described in Subsection 2.3.3, the expression of subthreshold slope S_W for narrow-width MOSFET can be obtained. For narrow-width MOSFET with uniform doped channel, the effective depletion capacitance $C_{DW,eff}(\psi_s)$ is defined as

$$C_{DW,eff} = C_D\left(1 + \frac{\pi}{2}\frac{w_D}{W}\right). \qquad (2.4.5)$$

And the corresponding new subthreshold slope S_W is

$$S_W = V_t \ln(10)\left[1 + \frac{C_{DW,eff}(\psi_s)}{C_{ox}}\right]\left\{1 - \left(\frac{2}{a^2}\right)\left[\frac{C_{DW,eff}(\psi_s)}{C_{ox}}\right]^2\right\}. \qquad (2.4.6)$$

As channel width becomes narrower, the slope of the subthreshold current is increased which is an adverse effect for narrow-width MOSFETs.

2.4.3 Parasitic Conductance and Channel Width Reduction

From the previous subsection, it is clear that the narrow-width effects play an important role in the modelling of MOSFET characteristics. These narrow-width effects can cause an increase in the threshold voltage and a decrease in the channel carrier mobility. This is because the conducting channel width can vary with both V_{gs} and V_{sb}. Channel width variation in narrow-width MOSFET becomes unavoidable in predicting accurately the drain current I_{ds} of a small geometry MOSFET.

The effective channel width W_e is different from the physical mask width of the gate W_m by an amount known as channel width reduction ΔW. This reduction ΔW can be

due to oxide encroachment, accuracy of mask line-widths and photolithographic undercut, and terminal biasing conditions. Normally, W_e is wider than W_m because high gate bias can invert the region around the channel width due to gate poly overlapping the field oxide. When the channel is wide, the reduction ΔW is insignificant with respect to W_m. However, ΔW becomes comparable to W_m when the channel is narrow, and hence

$$W_e = W_m - \Delta W. \tag{2.4.7}$$

Since it is W_e which will be used to model the electrical characteristics of a MOSFET, prior determination of ΔW is required. The determination of ΔW will be shown in the extraction algorithm in Chapter 4.

Another parameter, that accompanied ΔW and associated with the narrow edge effects, is the parasitic conductance G_p. It is a parasitic conductance which is parallel to the intrinsic conductance of a MOSFET. The amount of G_p depends on overlapped gate poly and the isolation around the device. Fig 2.4.2 shows the parasitic resistance and conductance of a narrow-width MOSFET on a device symbol. By incorporating Eqn (2.4.7) and G_p into Eqn (2.2.17), the drain current I_{ds} for a narrow-width MOSFET becomes

$$I_{ds} = \frac{\mu_e C_{ox}}{L} V_{ge}(V_{ds} - I_{ds}R_p)(W_m - \Delta W) + G_p V_{ds} \tag{2.4.8}$$

The paramter extraction model for narrow-width MOSFET in Chapter 4 will be used to find the value of G_p.

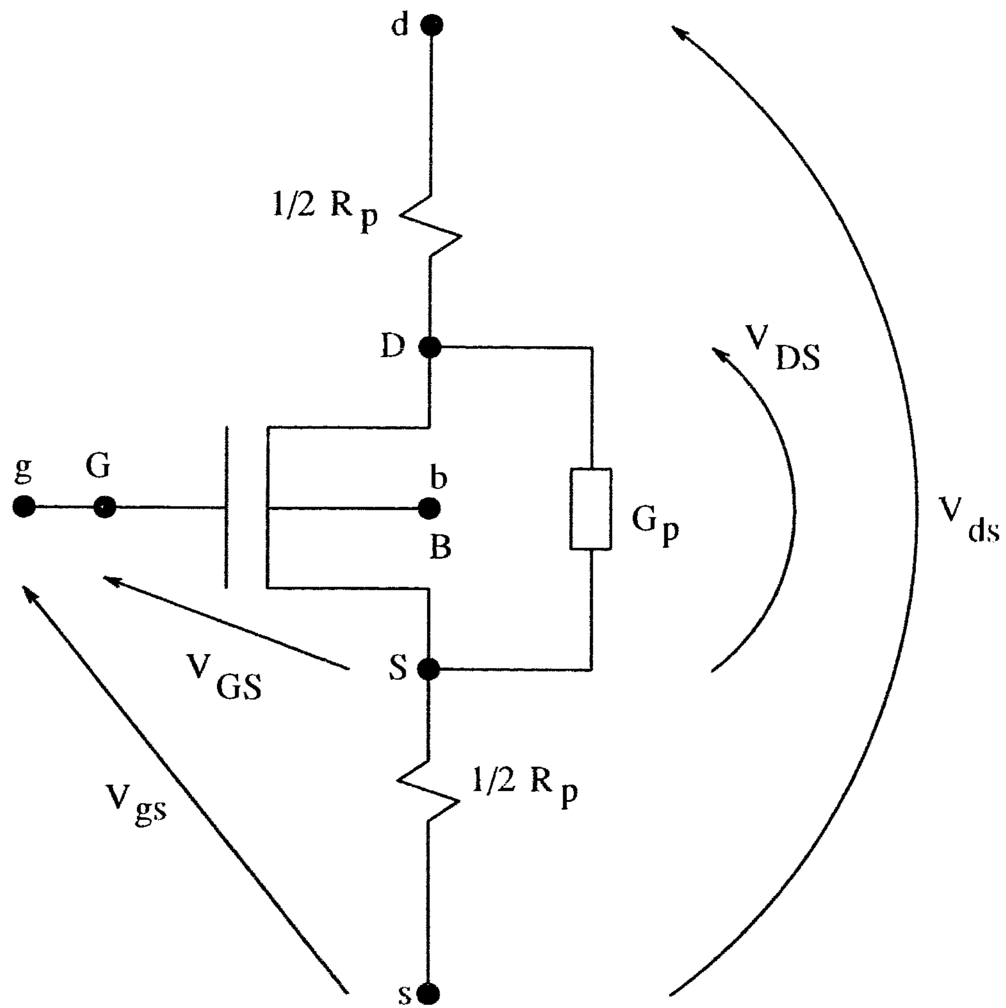


Figure 2.4.2. Device representation of a narrow-width MOSFET.

2.5 TEMPERATURE DEPENDENCE

The derivation of I_{ds} in Section 2.2 does not include the effect of temperature variation. However, the characteristics and performance of a MOSFET experience a significant change with temperature. This section will described briefly on some of the MOSFET parameters that can vary with temperature.

One of the main parameters that can be affected by temperature variation is the effective carrier mobility μ_e. The conductance and transconductance of a MOSFET depend on this parameter. The mobility μ_e in the inversion layer has a negative power dependence on the operating temperature, and an often used approximation is given as [5]

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-n} \tag{2.5.1}$$

where T is absolute temperature; T_r is room absolute temperature, normally 300 K; and n is a fitting constant with various values used for it between 1.5 and 2.0 [31, 5]. From this equation, it can be deduced that μ_e increases as temperature decreases, and thus higher I_{ds} can be obtained at a lower temperature.

Another temperature-dependent parameter is V_T. The carrier concentration in the channel varies with temperature because p_p and n_p change with temperature as indicated by the V_t, n_i and N_A terms in Eqn (2.2.4). The change in carrier concentration will affect the surface potential of the channel, and this in turns changes V_T. The effect of temperature on V_T is found to exhibit an almost straight line increase with decreasing temperature. As temperature decreases, the characteristics of a MOSFET improve due

to an increase in V_T. The most important improvement from decreasing temperature is the reduction in the subthreshold swing, S. The improvement comes mainly from the term V_t in Eqn (2.2.25).

Other parameters which benefit from lower operating temperature include higher transconductance, lower power comsumption and lower junction leakage current. M.J. Deen et. al. [61-62] had shown some of the advantages of operating devices at low temperature. However, there are disadvantages associated with MOSFET operating at low temperature. One of the disadvantages is the degradation of performance and reliability of small geometry MOSFET caused by hot-carrier effect. The hot carriers are induced by high effective carrier mobility μ_e at low temperature. Another drawback is the additional equipment required for setting up the low-temperature measurement.

Chapter 3 EXPERIMENTAL DETAILS

3.1 INTRODUCTION

As described in the previous chapter, a MOSFET that has short and narrow channel is difficult to study. This is due to the complexity of the three-dimensional field distribution in the channel. In the past, only two papers [3, 46] have been published on small geometry MOSFET, in which both the short-channel and narrow-width effects are combined in the models, and the physics involved is quite advanced. So, this research concentrates on studying the effects of short-channel MOSFET and narrow-width MOSFET separately. By studying the effects separately, a better understanding of the behaviour of small geometry MOSFETs and their semi-empirical models can be obtained.

3.2 TEST DEVICES

All the MOS transistors used in this study were n-channel enhancement-mode LDD MOSFETs. The LDD NMOS were designed using a layout tool called Xkic in Xwindow environment. Then, the layout of the devices was saved in a file in kic format. Since Canadian Microelectronics Corporation (CMC) accepts the design in cif format, a conversion program, known as kictocif, was used to convert the design to cif file.

The design consists of 16 LDD NMOS, of which eight of them are short-channel MOSFETs while the rest are narrow-width MOSFETs. The short-channel transistors have gate lengths of 1.2, 1.4, 1.6, 1.8, 2, 3, 5 and 10 μm, and constant channel width of 20 μm. The varying width group have gate widths of 2, 2.2, 2.4, 2.6, 2.8, 3, 5 and 10 μm

with constant gate length of 10 μm. Each groups of MOSFETs have a common gate, source and substrate terminals, but different drain output pads for individual transistors. There is no input or output protection circuits connected to any of the pads.

With standard CMOS4S twin-tub technology, these MOSFETs were fabricated on a <100> p-type substrate. Since this research used n-channel LDD MOSFETs, the devices were in a p-well with an implant concentration of ~ 2 x 10^{12} cm^{-2}. The thickness of the field oxide and gate oxide is approximately equal to 700 nm and 25 nm respectively. The gate material for the transistors is heavily-doped n^+ polysilicon. The n^+ regions of the source and drain are heavily-doped with arsenic and the n^- regions are implanted with phosphorus. The implant dose for n^+ and n^- is ~ 5 x 10^{15} cm^{-2} and ~ 10^{14} cm^{-2}, respectively.

Both set of MOSFETs were fabricated together and were wire-bounded in a 68 pin grid array (PGA) package. After the bonding, the chip was sealed with a metal cap to avoid light and electromagnetic field interference.

3.3 MEASUREMENT SETUP

The block diagram of the experimental setup is shown in Fig 3.3.1. It consists of a HP 4145B Semiconductor Parameter Analyzer, an IBM compatible personal computer, a HP 16058A Test Fixture with appropriate Personality Board, a Keithley 195A Multimeter, a Watlow S942 Ramping Temperature Control and a Tenney Test Chamber.

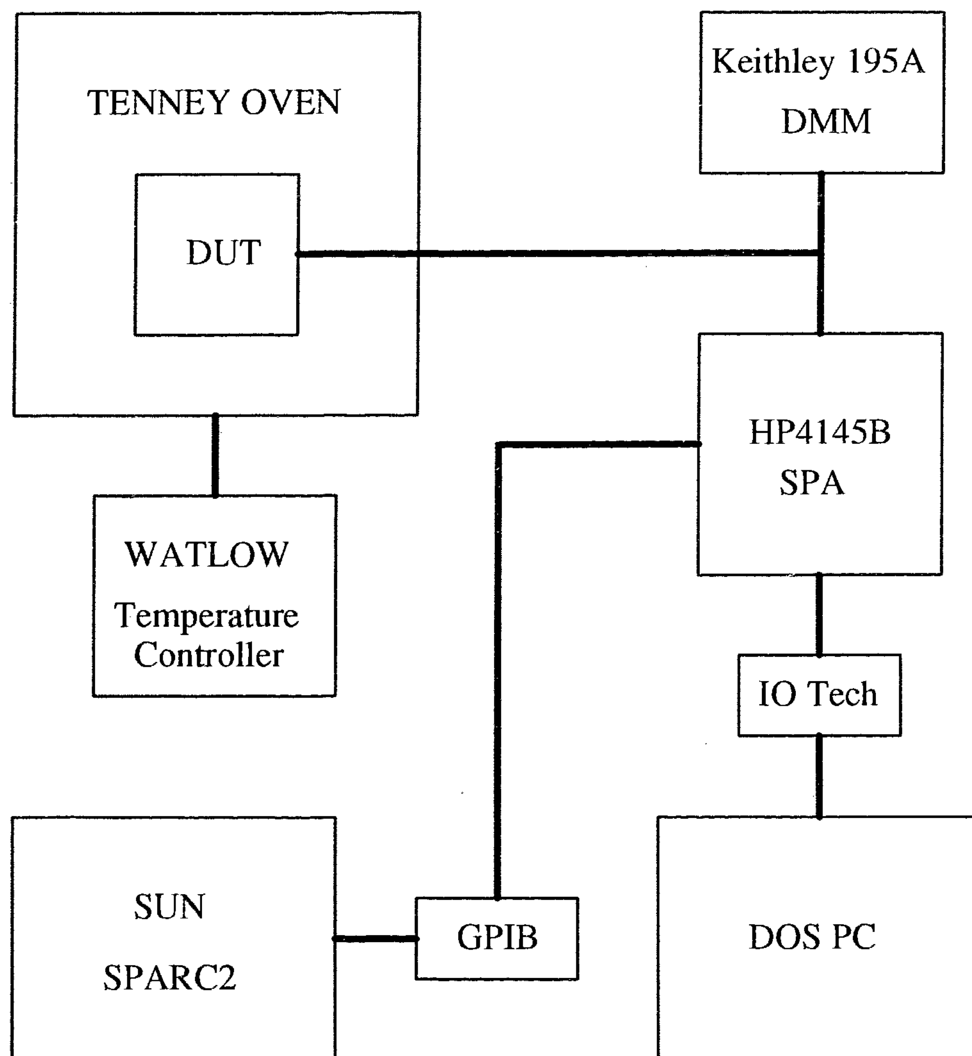


Figure 3.3.1. Block diagram of the equipment setup.

The HP 4145B Semiconductor Parameter Analyzer (SPA) is a high performance and programmable test equipment designed to measure and display the current and voltage characteristics of semiconductor devices. The IBM compatible personal computer is connected to the SPA for controlling the biasing during measurement. It is also used for acquiring data from the SPA, data analysis and parameter extraction which will be explained in the following chapter. The interface between the computer and the SPA is through an IOTech IEEE 488 Bus Interface Board.

The test chip is mounted on the Personality Board in the Test Fixture. The Test Fixture is used to shield electromagnetic noise so as to allow stable readings during measurement. The Fixture is connected to the SPA through coaxial cables. Small and short jump-wires are used to switch individual devices.

The temperature of the devices during the measurement period is maintained constant by the Watlow S942 Ramping Temperature Control. The Fixture is placed in the Tenney Test Chamber for about an hour at a constant temperature. Same set of measurements is performed at every temperature.

3.4 OPERATING CONDITIONS

In this study, the operating temperature and the applied biases to all the terminals of the MOSFET will be used in the measurement to obtain a number of different I_{ds}-V_{gs} data. By extracting the parasitic parameters against one of the external biases while maintaining the rest constant, it is possible to study in more detail the effect of an individual external bias on either R_p or ΔL. In this way, any variation of these parasitic parameters is due

mainly to the external bias. Other parameters can be studied using this method.

The voltages applied to the terminals of each device are controlled by the computer through the SPA. The range of terminal biases are as follows :-

1. V_{gs} is from 0 to 5 V, stepsize of 0.05
2. V_{ds} is from 0.1 to 0.5 V, stepsize of 0.1
3. V_{sb} is from 0 to 3 V, stepsize of 1

The ambient temperature range is varied between 200 K and 400 K with stepsize of 25. This range of temperature is chosen because most of the electronics operate within this range. The temperature ambient can be ramped up or down by using digital key pad on the front panel of Watlow Microprocessor-based Temperature Controller.

Chapter 4 PARAMETER EXTRACTION MODEL

The effects of short-channel and narrow-width were represented by parameters in the equations described in Chapter 2. The methods that are used for extracting the parameters will be presented in this chapter. Once the values of these parameters are known, understanding and modelling of the electrical characteristics of small geometry MOSFET can be enhanced. Since both short-channel and narrow-width effects of small geometry MOSFET are studied separately in this research, the model of the drain current I_{ds} for short-channel device is quite different from that of narrow-width device.

Most of the parameters are extracted using matrix manipulations within the MATLAB program. A sample file for short-channel devices at room temperature is listed in the Appendix, in which measured I_{ds}-V_{gs} data is input into the MATLAB program to provide the slopes and intercepts at specified gate biases in this case.

4.1 SHORT-CHANNEL MOSFET

The I_{ds} model used for the short-channel MOSFET is similar to Eqn (2.2.17), except the effect of the parasitic resistance R_p is included here, and is given as

$$I_{ds} = \beta\left[\left(\left(V_{gs} - \frac{1}{2}I_{ds}R_p\right) - V_T - \frac{(1+\delta)}{2}(V_{ds} - I_{ds}R_p)\right)(V_{ds} - I_{ds}R_p)\right] \quad (4.1.1)$$

where μ_e is the effective carrier mobility given by Eqn (2.3.27); W_e is the effective channel width; L_e is the effective channel length and β is given as

$$\beta = \frac{\mu_e C_{ox} W_e}{L_e}. \quad (4.1.2)$$

The parameter δ is defined in Eqn (2.2.18). It is usually very small and can be neglected in first-order approximation so that Eqn (4.1.1) can be reduced to

$$I_{ds} = \beta V_{ge}(V_{ds} - I_{ds}R_p) \tag{4.1.3}$$

where V_{ge} is defined in Eqn (2.3.25).

For short and wide channel MOSFET, L_e is different from the mask channel length L_m and is given in Eqn (2.3.16). However, since the reduction at the edges of the channel width is insignificant compared to the mask channel width W_m for wide channel MOSFET, W_e is approximately equal to W_m.

Eqn (4.1.3) is valid under strong inversion condition and for small and moderate V_{ds}. The extraction algorithm will extract the following parameters : R_p, ΔL, μ_o, θ_0 and θ_B. The extraction process requires the measurement data I_{ds} vs V_{gs}, which are obtained using the equipment setup described in the previous chapter.

By rearranging Eqn (4.1.3), the total measured resistance R_m of a MOSFET can be obtained as follow

$$R_m = \frac{V_{ds}}{I_{ds}} = \frac{1}{\beta V_{ge}} + R_p. \tag{4.1.4}$$

Note that the first term of Eqn (4.1.4) represent the channel resistance R_c of a MOSFET as R_m is the sum of R_c and R_p.

Since R_m is linearly proportional to L_m, linear least-squares fitting method can be used to extract the parameters. That is, the equations for the extraction algorithm will be arranged in a straight-line format. By rearranging Eqn (4.1.4), R_m is given as

$$R_m = \frac{(L_m - \Delta L)}{K_l V_{ge}} + R_p \tag{4.1.5}$$

where K_l is given as

$$K_l = \mu_e C_{ox} W_e = \frac{\mu_o C_{ox} W_m}{1 + \theta_0 V_{ge} + \theta_B V_{sb}}. \quad (4.1.6)$$

When R_m is plotted against L_m, a series of straight lines for different V_{ge} will be obtained. By using the slopes and intercepts of these straight lines, the five parameters listed above can be determined. The rest of this section shows the steps involved in the extraction process.

For V_{sb} = 0 V case, Eqn (4.1.6) reduces to

$$K_{l0} = \frac{\mu_o C_{ox} W_m}{1 + \theta_0 V_{ge}} \quad (4.1.7)$$

and Eqn (4.1.5) becomes

$$R_m = \frac{(1 + \theta_0 V_{ge})}{\mu_o C_{ox} W_m V_{ge}} (L_m - \Delta L) + R_p. \quad (4.1.8)$$

From Eqn (4.1.8) using linear regression of R_m with respect to L_m, the corresponding slope S_1 and the intercept I_1 can be obtained at different $V_{ge} \pm \Delta V_{ge}$ to get R_p and ΔL. Therefore, by varying V_{ge}, we will be able to get the resulting variations of parasitics R_p and ΔL with effective gate biasing.

$$S_1 = \frac{1}{K_{l0} V_{ge}} = \frac{1}{\mu_o C_{ox} W_m V_{ge}} + \frac{\theta_0}{\mu_o C_{ox} W_m} \quad (4.1.9)$$

and

$$I_1 = R_p - \frac{\Delta L}{K_{l0} V_{ge}} = R_p - \Delta L \left(\frac{1}{\mu_o C_{ox} W_m V_{ge}} + \frac{\theta_0}{\mu_o C_{ox} W_m} \right). \quad (4.1.10)$$

From Eqn (4.1.10), the intercept I_1 can be related to the slope S_1 through linear regression, and I_1 can be written as

$$I_1 = R_p - S_1 \Delta L. \quad (4.1.11)$$

By using linear regression of I_1 with S_1 in Eqn (4.1.11), the slope S_2 and the intercept I_2 can provide the parasitic parameters R_p and ΔL.

$$S_2 = -\Delta L \Rightarrow \Delta L = -S_2$$
$$I_2 = R_p \Rightarrow R_p = I_2 \qquad (4.1.12)$$

By plotting all the values of S_1 in Eqn (4.1.9) against $1/V_{ge}$, the corresponding slope S_3 and the intercept I_3 can be determined and the parameters μ_o and θ_0 can be extracted as follows.

$$S_3 = \frac{1}{\mu_o C_{ox} W_m} \Rightarrow \mu_o = \frac{1}{S_3 C_{ox} W_m}$$
$$I_3 = \frac{\theta_0}{\mu_o C_{ox} W_m} \Rightarrow \theta_0 = \frac{I_3}{S_3} \qquad (4.1.13)$$

For the case of changing V_{sb}, one more parameter is required to include the effect of V_{sb} biasing. The parameter θ_B is used to include this effect. K_{l0} in Eqns (4.1.9) and (4.1.10) will be replaced by K_l, and the respective slope S_4 and intercept I_4 will be given by

$$S_4 = \frac{1}{K_l V_{ge}} = \frac{1 + \theta_B V_{sb}}{\mu_o C_{ox} W_m V_{ge}} + \frac{\theta_0}{\mu_o C_{ox} W_m} \qquad (4.1.14)$$

and

$$I_4 = R_p - \frac{\Delta L}{K_l V_{ge}} = R_p - \Delta L\left(\frac{1 + \theta_B V_{sb}}{\mu_o C_{ox} W_m V_{ge}} + \frac{\theta_0}{\mu_o C_{ox} W_m}\right). \qquad (4.1.15)$$

The method for extracting the parasitic paramters R_p and ΔL from Eqn (4.1.15) is similar to the one shown in Eqn (4.1.11). The parameter θ_B can be extracted from S_5 which is similar to that of S_4.

S_3

$$S_5 = \frac{1 + \theta_B V_{sb}}{\mu_o C_{ox} W_m}$$
$$I_5 = \frac{\theta_0}{\mu_o C_{ox} W_m} \qquad (4.1.16)$$

Other short-channel effects such as α_1 in the V_T expression in Eqn (2.3.10) can be determined using the same linear regression technique with $\alpha_2 = 0$ at small V_{ds}. The subthreshold slope S can be found by using Eqn (2.2.24) on the measured data and the results will be shown in the next chapter.

4.2 NARROW-WIDTH MOSFET

For a long and narrow channel MOSFET, the I_{ds} model is given as

$$I_{ds} = \beta[V_{ge}(V_{ds} - I_{ds}R_p)] + V_{ds}G_p \qquad (4.2.1)$$

where G_p is the parasitic conductance of the channel edges in the width direction. Since the group of MOSFETs has a long channel, the channel length reduction will be insignificant in comparison to L_e, and hence L_m can be taken as L_e. In this case, W_e is different from W_m and is given in Eqn (2.4.7).

For small and moderate V_{ds} and reasonable V_{sb}, Eqn (4.2.1) is valid under strong inversion condition. The extraction algorithm for narrow-width MOSFET will extract the following parameters : G_p, ΔW, μ_o, θ_0 and θ_B. The extraction process requires the measurement data I_{ds} vs V_{gs} which are obtained using the equipment setup described in the previous chapter.

Eqn (4.2.1) can be rearranged similar to Eqn (4.1.5), so that I_{ds} is proportional to W_m given by

$$I_{ds} = K_w V_{dp} V_{ge}(W_m - \Delta W) + V_{ds}G_p \qquad (4.2.2)$$

where K_w is given as

$$K_w = \frac{\mu_e C_{ox}}{L_e} = \frac{\mu_o C_{ox}}{L_e(1 + \theta_0 V_{ge} + \theta_B V_{sb})} \tag{4.2.3}$$

and V_{dp} is defined as

$$V_{dp} = V_{ds} - I_{ds} R_p. \tag{4.2.4}$$

For first-order approximation, V_{ds} will be used to replace V_{dp}. By plotting I_{ds} against W_m, a series of straight lines for different V_{ge} will be obtained. The five parameters can be extracted by using the slopes and intercepts of these straight lines.

For the case of V_{sb} = 0 V, Eqn (4.2.3) is simplified to

$$K_{w0} = \frac{\mu_o C_{ox}}{L_e(1 + \theta_0 V_{ge})} \tag{4.2.5}$$

and Eqn (4.2.2) becomes

$$I_{ds} = \frac{\mu_o C_{ox} V_{ds} V_{ge}}{L_e(1 + \theta_0 V_{ge})}(W_m - \Delta W) + V_{ds} G_p. \tag{4.2.6}$$

From Eqn (4.2.6) using inear regression of I_{ds} with respect to W_m, the corresponding slope S_1 and I_1 can be obtained as

$$S_1 = K_{w0} V_{ds} V_{ge} = \frac{\mu_o C_{ox} V_{ds} V_{ge}}{L_m(1 + \theta_0 V_{ge})} \tag{4.2.7}$$

and

$$I_1 = G_p V_{ds} - K_{w0} V_{ds} V_{ge} \Delta W. \tag{4.2.8}$$

From Eqn (4.2.8), the intercept I_1 can be related to the slope S_1 through linear regression, and I_1 can be written as the parasitic parameters G_p and ΔW can be obtained as

$$I_1 = G_p V_{ds} - S_1 \Delta W. \tag{4.2.9}$$

By using linear regression of I_1 with S_1 in Eqn (4.2.9), the slope S_2 and the intercept I_2 can provide the parasitic parameters G_p and ΔW.

$$
\begin{aligned}
S_2 &= -\Delta W \Rightarrow \Delta W = -S_2 \\
I_2 &= G_p V_{ds} \Rightarrow G_p = \frac{I_2}{V_{ds}}.
\end{aligned}
\tag{4.2.10}
$$

By plotting all the values of $1/S_1$ in Eqn (4.2.7) against $1/V_{ge}$, the corresponding slope S_3 and the intercept I_3 can be determined and the parameters μ_o and θ_0 can be extracted as follows.

$$
\begin{aligned}
S_3 &= \frac{L_m}{\mu_o C_{ox} V_{ds}} \Rightarrow \mu_o = \frac{L_m}{S_3 C_{ox} V_{ds}} \\
I_3 &= \frac{L_m \theta_0}{\mu_o C_{ox} V_{ds}} \Rightarrow \theta_0 = \frac{I_3}{S_3}.
\end{aligned}
\tag{4.2.11}
$$

For the case of changing V_{sb}, one more parameter is required to include the effect of V_{sb} biasing. The parameter θ_B is used to include this effect. K_{w0} in Eqns (4.2.7) and (4.2.8) will be replaced by K_w, and the respective slope S_4 and intercept I_4 will be given by

$$
S_4 = K_w V_{dp} V_{ge} = \frac{\mu_o C_{ox} V_{dp} V_{ge}}{L_m(1 + \theta_0 V_{ge} + \theta_B V_{sb})} \tag{4.2.12}
$$

and

$$
I_4 = G_p V_{ds} - K_w V_{dp} V_{ge} \Delta W = G_p V_{ds} - \Delta W \frac{\mu_o C_{ox} V_{dp} V_{ge}}{L_m(1 + \theta_0 V_{ge} + \theta_B V_{sb})}. \tag{4.2.13}
$$

The method for extracting the parasitic paramters G_p and ΔW from Eqn (4.2.13) is similar to the one shown in Eqn (4.2.8). The parameter θ_B can be extracted from S_5 which is similar to that of S_4.

$$
\begin{aligned}
S_5 &= \frac{L_m(1 + \theta_B V_{sb})}{\mu_o C_{ox} V_{ds}} \Rightarrow \theta_B = \frac{1}{V_{sb}}\left(\frac{S_5 \mu_o C_{ox} V_{ds}}{L_m} - 1\right) \\
I_5 &= \frac{L_m \theta_0}{\mu_o C_{ox} V_{ds}} \Rightarrow \theta_0 = \frac{I_5 \mu_o C_{ox} V_{ds}}{L_m}.
\end{aligned}
\tag{4.2.14}
$$

Other narrow-width effects such as α_3 in the V_{TW} expression can be extracted using the same linear regression technique on Eqn (2.4.3). The subthreshold slope S_w can be found by using Eqn (2.4.6) on the measured data and the results will be shown in the following chapter.

Since parameters such as μ_o, V_T and S_w are temperature dependent, the short-channel and narrow-width extraction processes are repeated for every temperature step. Hence, some of the extracted parameters such as α_1 and α_3 will also be temperature dependent, and the results will be shown in the following chapter.

Chapter 5 RESULTS AND DISCUSSION

5.1 INTRODUCTION

This chapter will present the complete experimental results using the extraction algorithm which was described in the previous chapter. It also provides the relevant discussion based upon these results and the equations which were written in Chapter 2. The measurement data for this research were performed in the linear region of MOSFET operation for small V_{ds}. Due to the length of this chapter, the results and discussion of parameters will be group into three major sections. The results will also include modelling results of short-channel and narrow-width MOSFETs.

5.2 V_T AND S

In this section, the results of threshold voltage V_T and subthreshold slope S that will be influenced by short-channel effects, narrow-channel effects and temperature dependence are discussed. In relation to V_T, other parameters such as α_1 and α_3 will also be included in this section.

The derivation of V_T in short-channel and narrow-channel MOSFETs was previously given in Chapter 2, but an explanation for the extraction of V_T is required. For very small V_{ds}, Eqn (2.2.15) becomes Eqn (2.2.20) which symbolize as an equation of straight line about V_{gs}. So, the problem of finding this straight line experimentally is difficult since the I_{ds}-V_{gs} data for small geometry MOSFETs are not linear throughout the curve. However, a small segment of the curve is linear. This region satisfies the basic drain

equation because it has minimum influence of vertical field modulation and is in strong inversion region. Thus, Eqn (2.2.20) is a good approximation for this region.

In order to find the lowest influence of vertical field modulation by V_{gs}, an important device parameter called transconductance will be used to accurately find that point. The transconductance g_m is defined as

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\mu_o C_{ox} W V_{ds}}{L(1 + \theta_0 V_{ge} + \theta_B V_{sb})} \tag{5.2.1}$$

This equation shows that, at zero V_{sb}, g_m is maximum where $\theta_0 V_{ge}$ equals to zero. This $g_{m,max}$ point correspond to the inflection point in the linear region of the I_{ds}-V_{gs} curve. Then a straight line using least square fitting through the inflection point to the x-axis with the intercept given as V_T.

The extracted results of V_T for short-channel and narrow-width MOSFETs for different V_{sb} are shown in Figs 5.2.1 and 5.2.2, respectively. As shown in Fig 5.2.1, V_T is slowly decreasing for channel length down to about 2 μm. V_T decreases rapidly for all V_{sb} when channel length is less than 2 μm. The change of V_T with respect to the change in L_m for short-channel devices is -0.1445 V/μm and is -0.0016 V/μm for longer ones. This indicates that short-channel modulation is important for submicron devices. For narrow-width devices, the narrow-width effect is visible for widths less than 3 μm. However, the narrow-width effect on V_T is not as pronounced as those for short-channel devices. The variation of V_T with respect to the change in W_m for narrow-width devices is 0.026 V/μm and is 0.0019 V/μm for wider ones. The shape of the curves in both figures is almost independent of temperature. The change of V_T for short-channel devices at T = 200 K and 400 K are -0.14 V/μm and -0.15 V/μm, respectively. For narrow-width

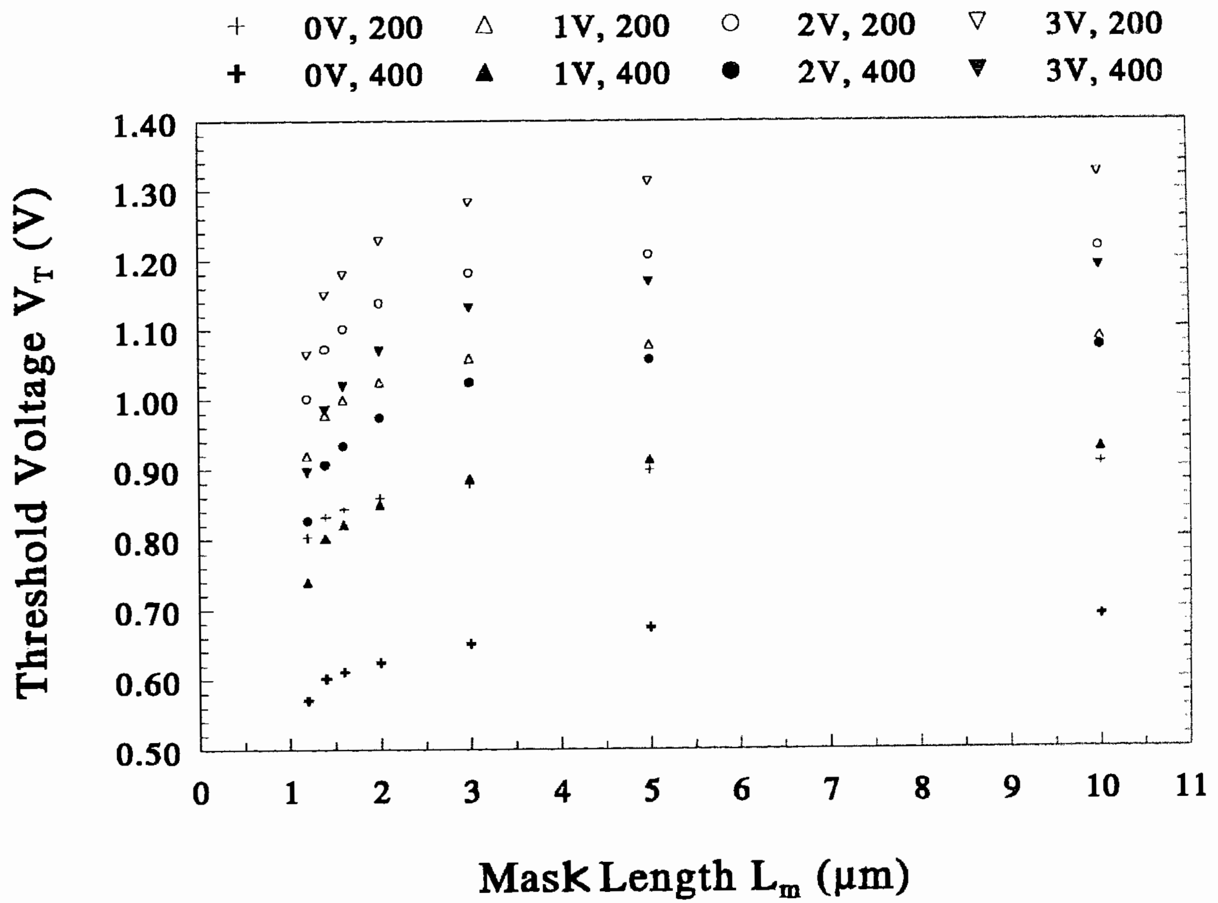


Figure 5.2.1. V_T vs L_m for different V_{sb} at T = 200 K & 400 K, and V_{ds} = 0.1 V.

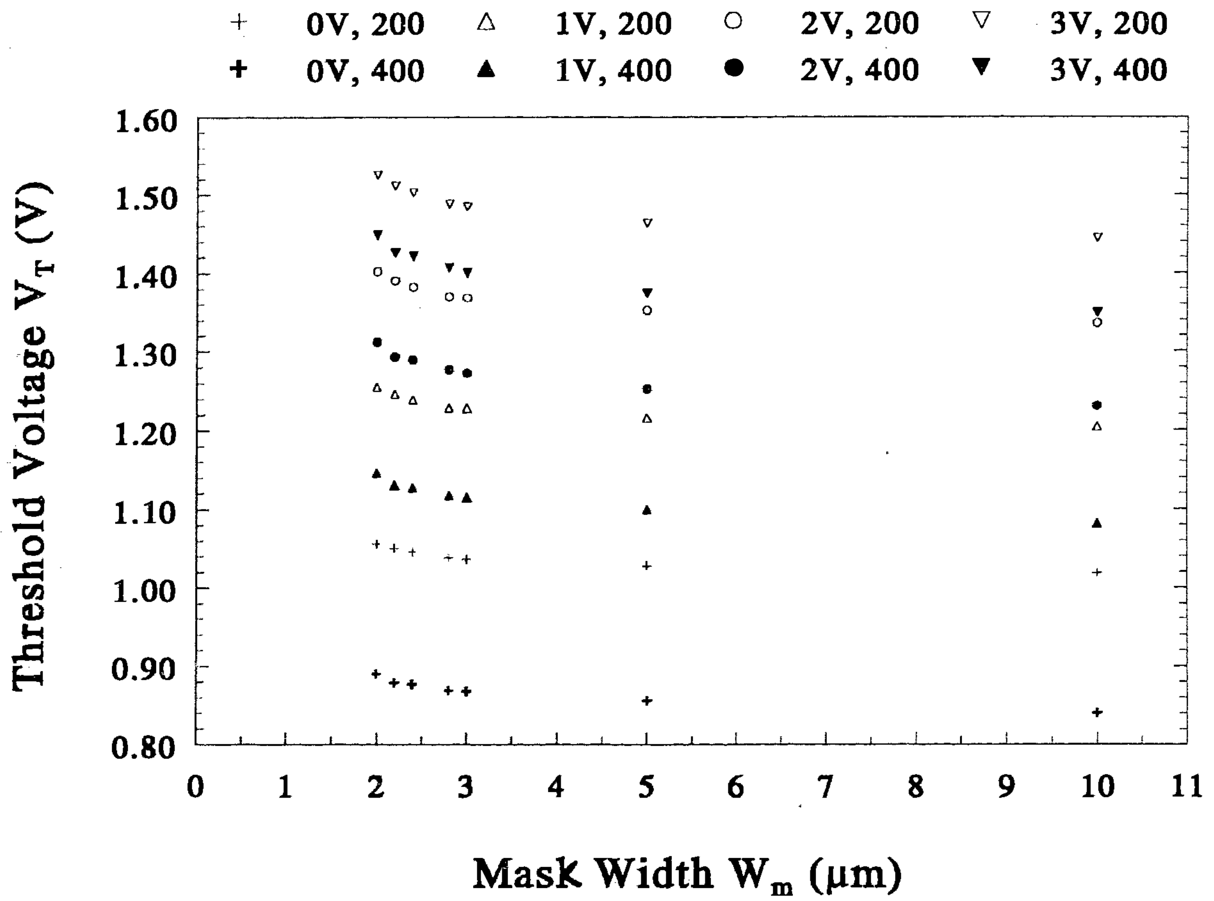


Figure 5.2.2. V_T vs W_m for different V_{sb} at T = 200 K & 400 K, and V_{ds} = 0.1 V.

devices, the change of V_T are 0.026 V/μm at T = 200 K and 0.03 V/μm at T = 400 K. This implies that both short-channel and narrow-width effects does not depend on temperature significantly.

The above results were taken using a single V_{ds} to maintain constant lateral field effect. It is equally important to see how V_T changes with different V_{ds}. For different V_{ds}, Eqn (2.2.17) will be used to extract the value of V_T. By reducing Eqn (2.2.17) similar to Eqn (2.2.20), it has shown that linear extrapolation method can still be applied on V_T. Now, the extrapolation will produce $V_T - \frac{(1+\delta)}{2}V_{ds}$ rather than V_T. Then a simple algebraic manipulation of $\frac{(1+\delta)}{2}V_{ds}$ will yield V_T, and δ can be calculated using Eqn (2.2.18). Figs 5.2.3 and 5.2.4 show the extracted values of V_T as a function of varying channel lengths and channel widths, respectively, for different V_{ds} at room temperature and zero V_{sb}. From Fig 5.2.3, the effect of V_{ds} on shorter channel devices is more significant than on longer ones. The change of V_T with respect to V_{ds} for L = 1.2 μm is 0.083 and is 0.013 for L = 10 μm. It is due to an increase in lateral field as channel length decreases. Also, described in Chapter 2, this phenomenon is known as Drain-Induced Barrier Lowering or DIBL effect. For varying channel width devices, the effect of V_{ds} has less impact on V_T because the length of the channel is relatively long (see Fig 5.2.4). The change of V_T with respect to V_{ds} for W = 2 μm is 0.019 and is 0.017 for W = 10 μm. As expected, the effect of V_{ds} has more impact on short-channel effect than on narrow-width effect.

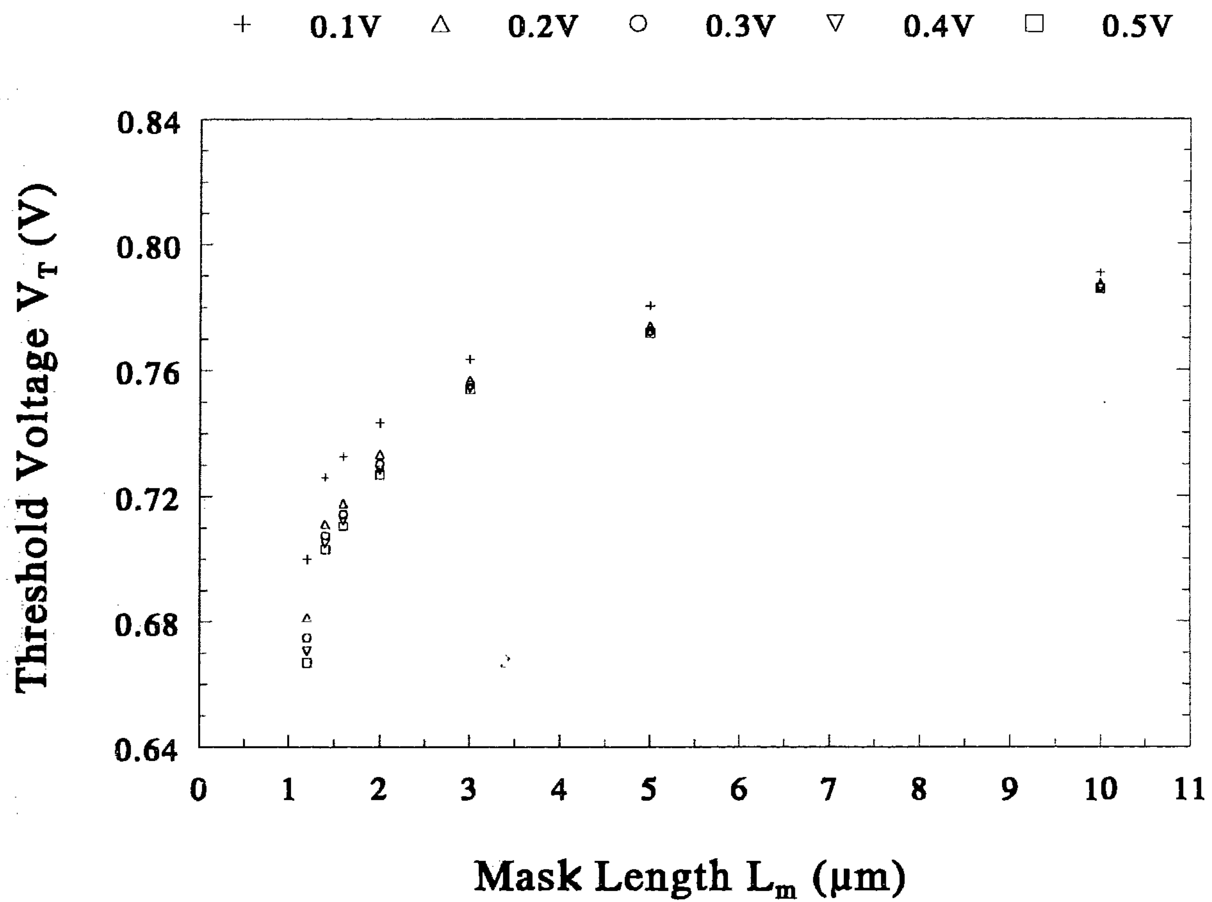


Figure 5.2.3. V_T vs L_m for different V_{ds} at T = 300 K and V_{sb} = 0 V.

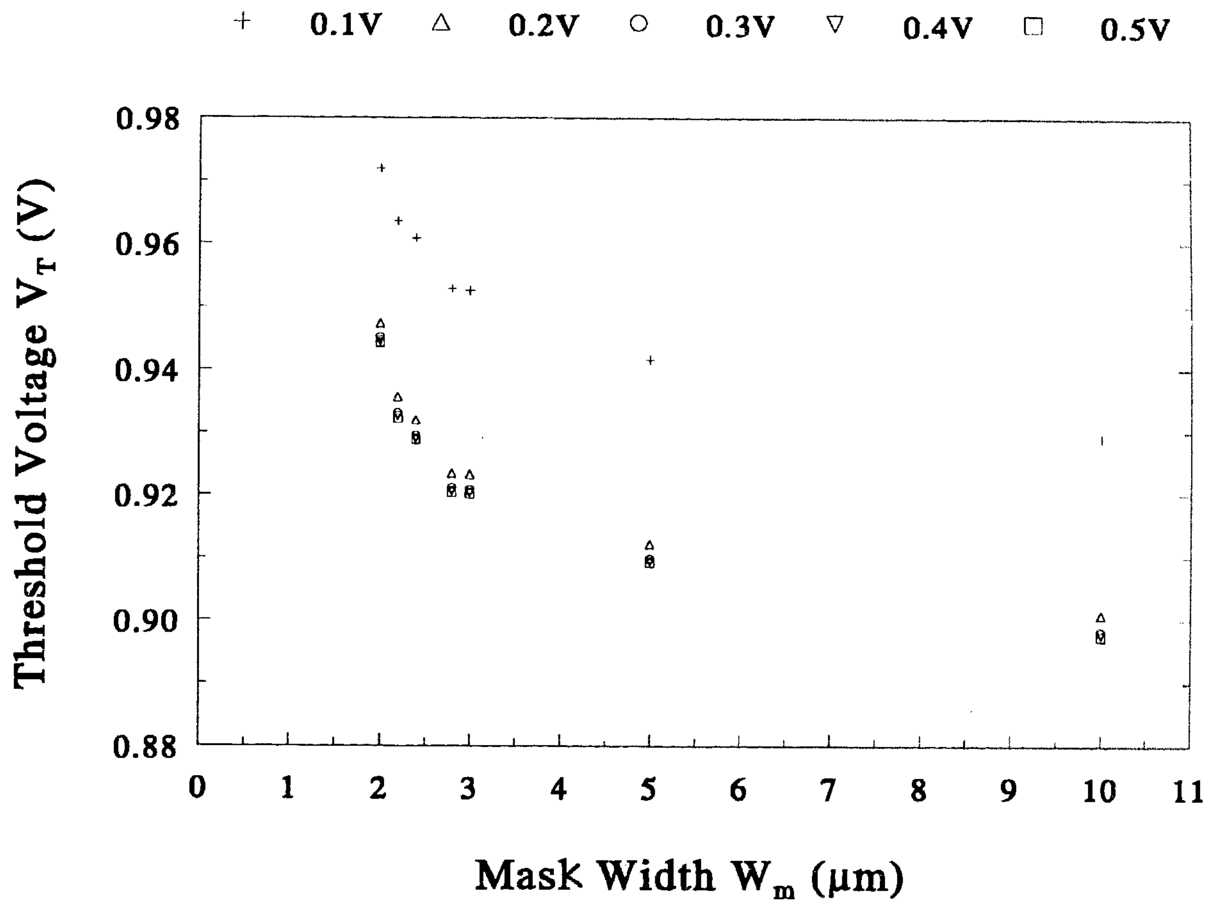


Figure 5.2.4. V_T vs W_m for different V_{ds} at T = 300 K and V_{sb} = 0 V.

By using Eqn (2.3.10) to fit the V_T results of short-channel devices, the channel length modulation constant α_1 can be found assuming $\alpha_2 = 0$ for very small V_{ds}. Similarly, Eqn (2.4.3) can be used to find the narrow-width modulation α_3. Fig 5.2.5 shows the results of α_1 and α_3 for different V_{sb} at room temperature and $V_{ds} = 0.1$ V. The graph shows that both α's decrease with increasing V_{sb}. The reason is that the channel depletion widths w_D of the source and the drain increases with V_{sb}. According to the charge-sharing model which was described in Chapter 2, the variation of the depletion regions can cause $Q_{D,eff} / Q_D$ in Eqn (2.3.9) to be smaller and V_T to be larger. Hence, this leads to smaller values of α_1 and α_3.

Figs 5.2.1 and 5.2.2 also show V_T varies with temperature. The effect of temperature on V_T with V_T at 200 K is higher than that at 400 K. To further illustrate how V_T varies with temperature, Figs 5.2.6 to 5.2.9 were drawn to show the variation of V_T with temperature for varying channel length and channel width devices at $V_{sb} = 0$ and 3 V, respectively. Both graphs show V_T increases almost linearly with decreasing temperature. At $V_{ds} = 0.1$ and $V_{sb} = 0$ V, V_T for L = 1.2 μm drops from 0.80 V at T = 200 K to about 0.57 V at T = 400 K, and hence the rate of decrease of V_T is -1.16E-3 V/K. As for W = 2.0 μm, V_T decreases from about 1.1 V to 0.89 V with the decreasing rate of -8.28E-4 V/K at the same temperature range. This change in V_T with temperature is mainly caused by the change in Fermi potential which include the thermal voltage V_t and intrinsic carrier concentration n_i. Fig 5.2.10 shows the surface potential ψ_s as a function of temperature for all devices and from eqn (2.2.10) the Fermi potential is half of ψ_s.

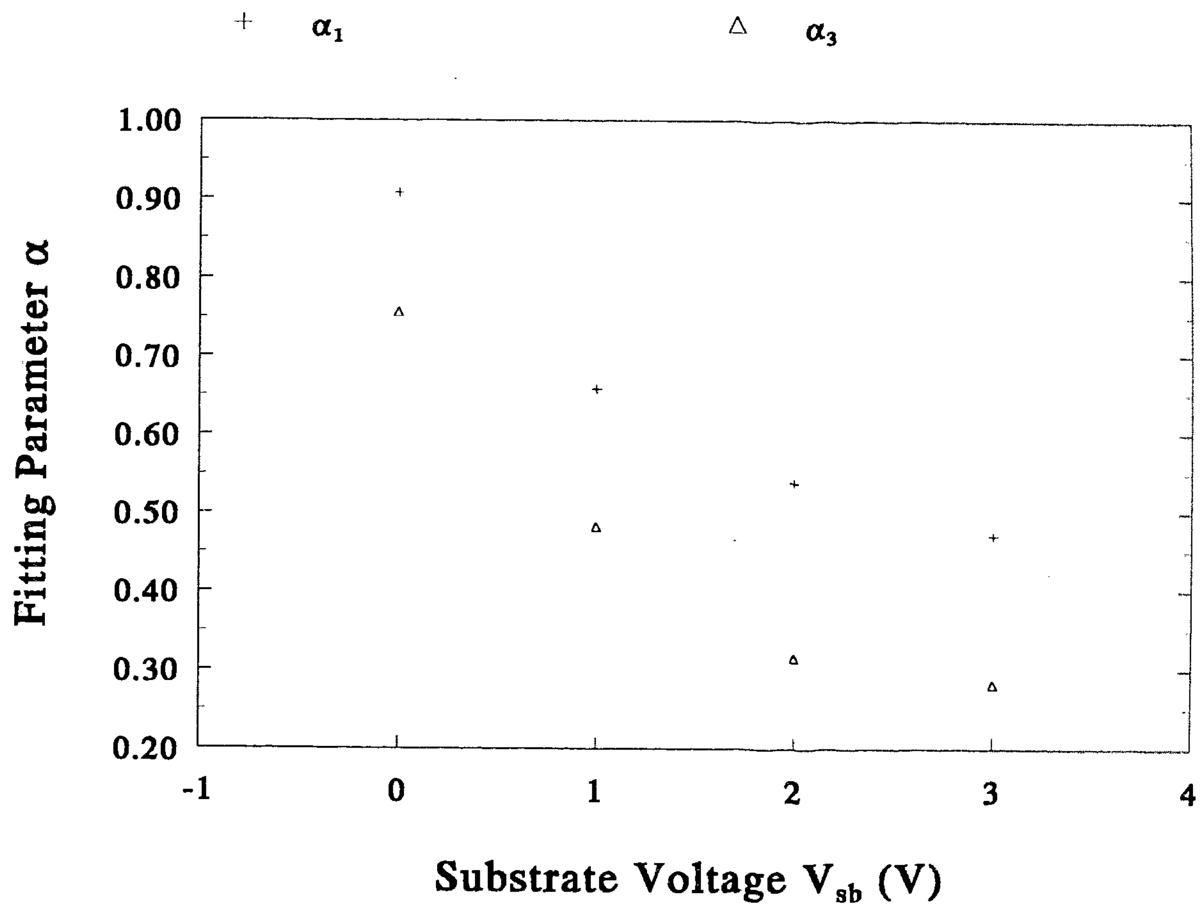


Figure 5.2.5. α_1 and α_3 vs V_{sb} at T = 300 K and V_{ds} = 0.1 V.

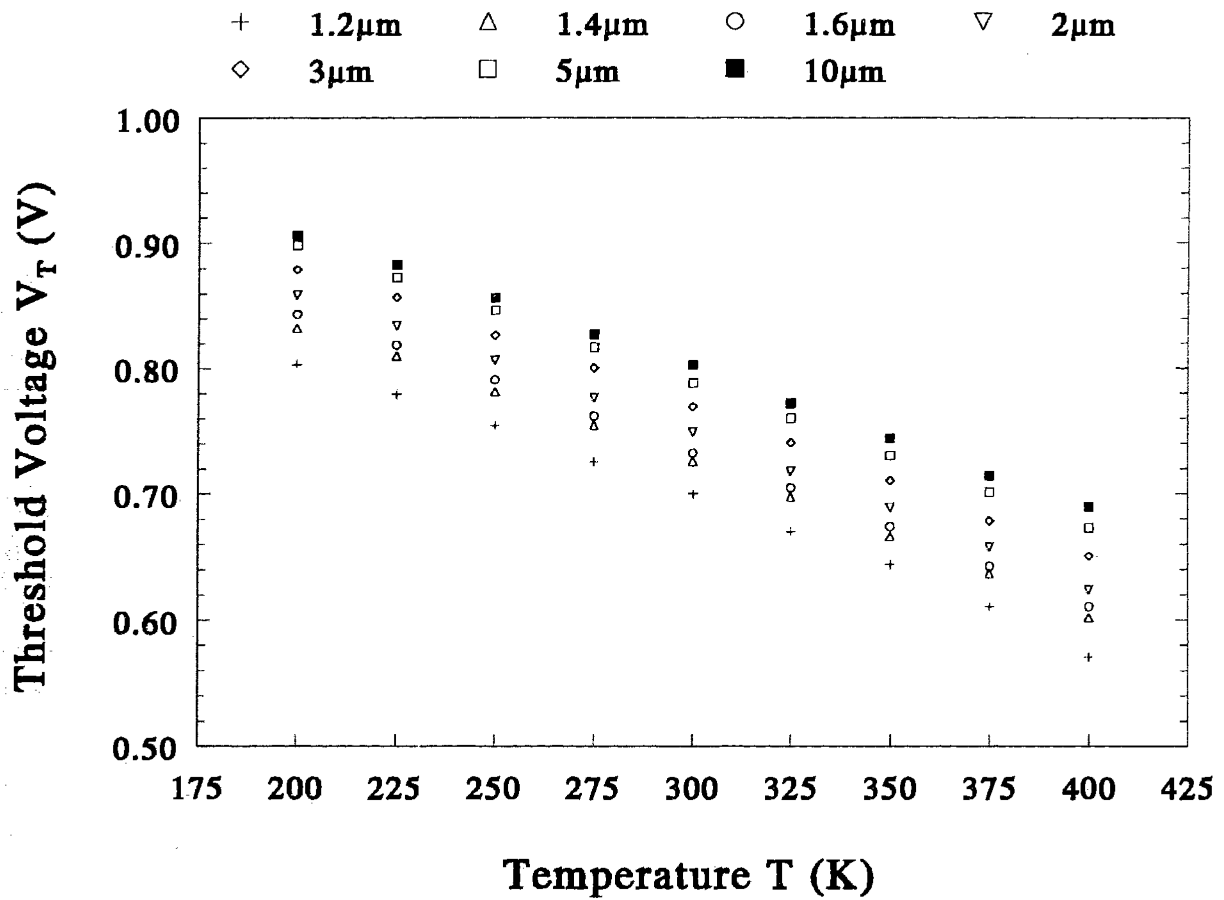


Figure 5.2.6. V_T vs T for different L_m at V_{ds} = 0.1 V and V_{sb} = 0 V.

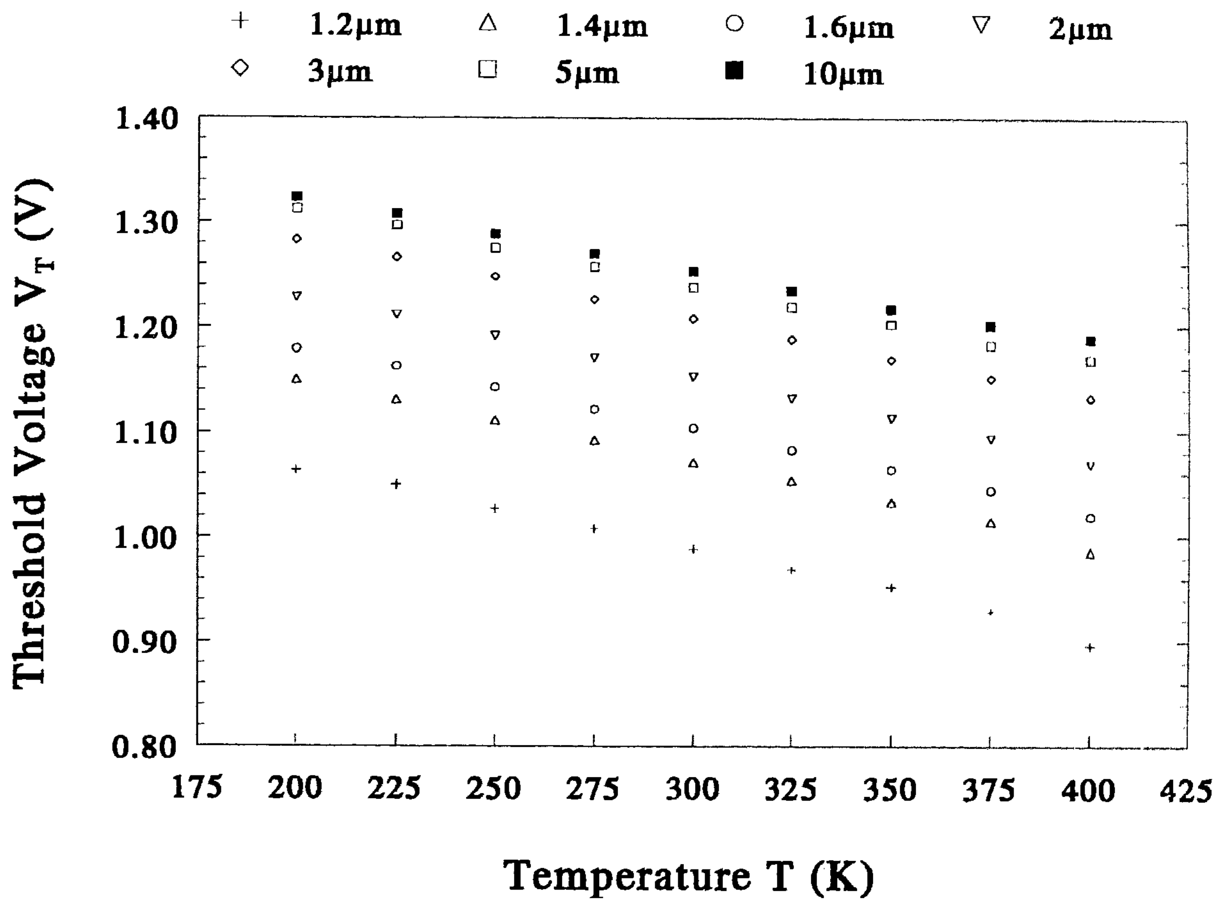


Figure 5.2.7. V_T vs T for different L_m at V_{ds} = 0.1 V and V_{sb} = 3 V.

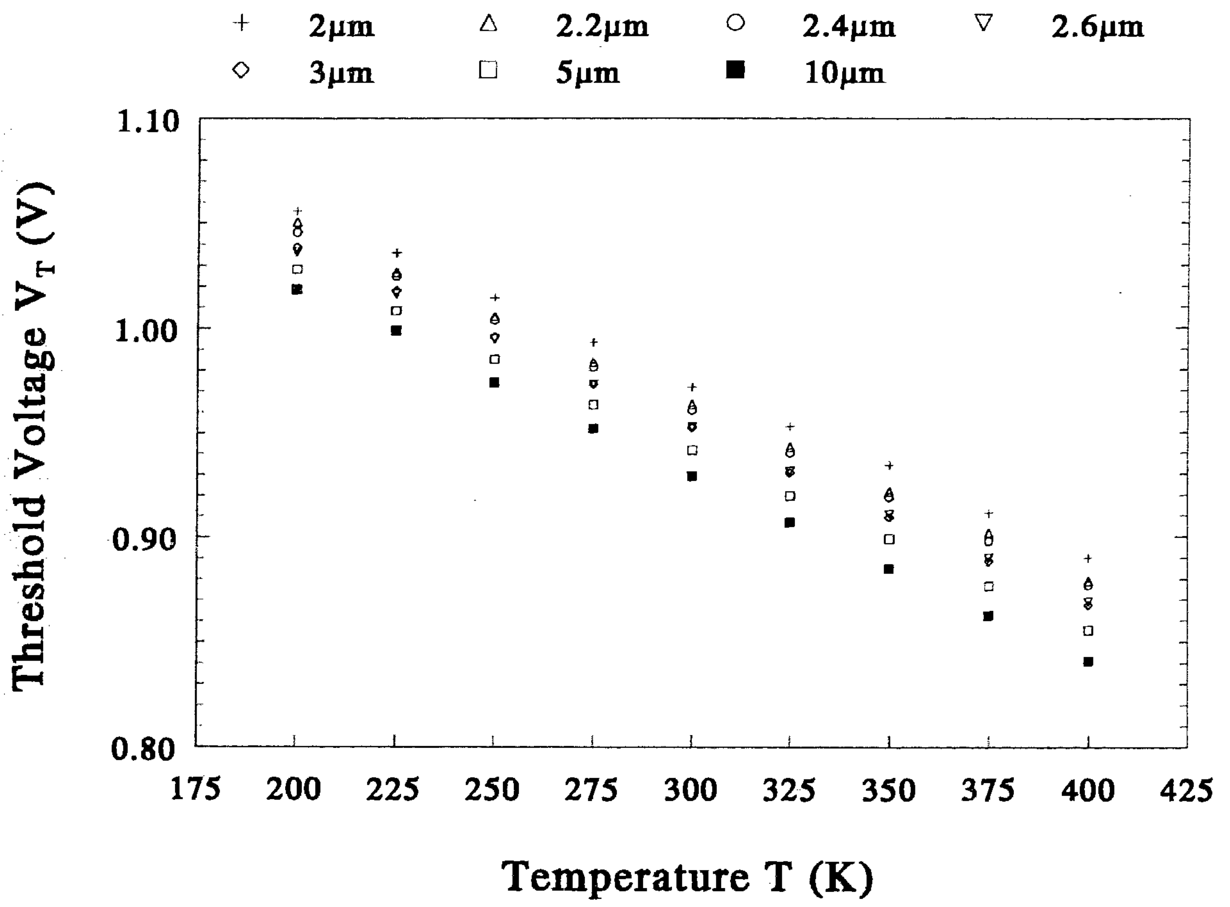


Figure 5.2.8. V_T vs T for different W_m at V_{ds} = 0.1 V and V_{sb} = 0 V.

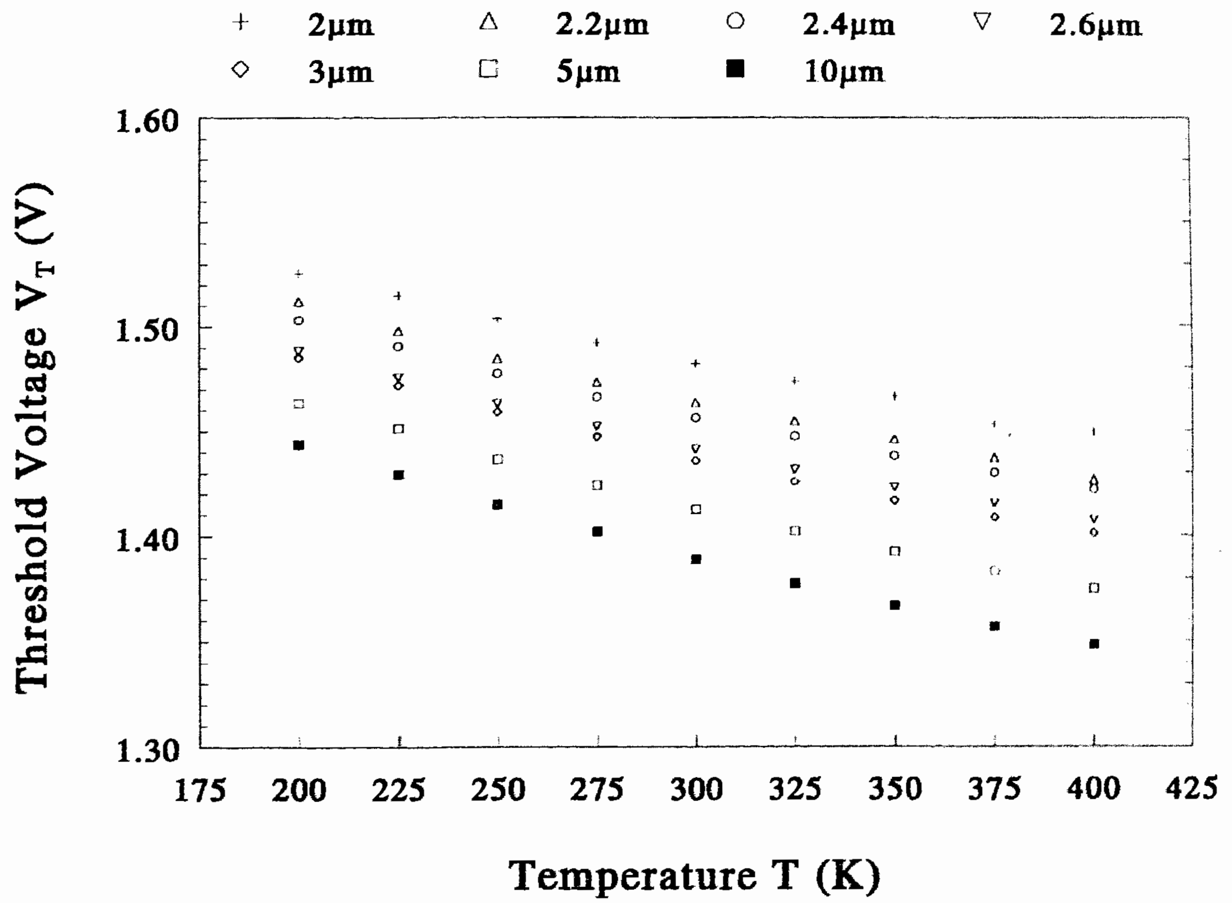


Figure 5.2.9. V_T vs T for different W_m at V_{ds} = 0.1 V and V_{sb} = 3 V.

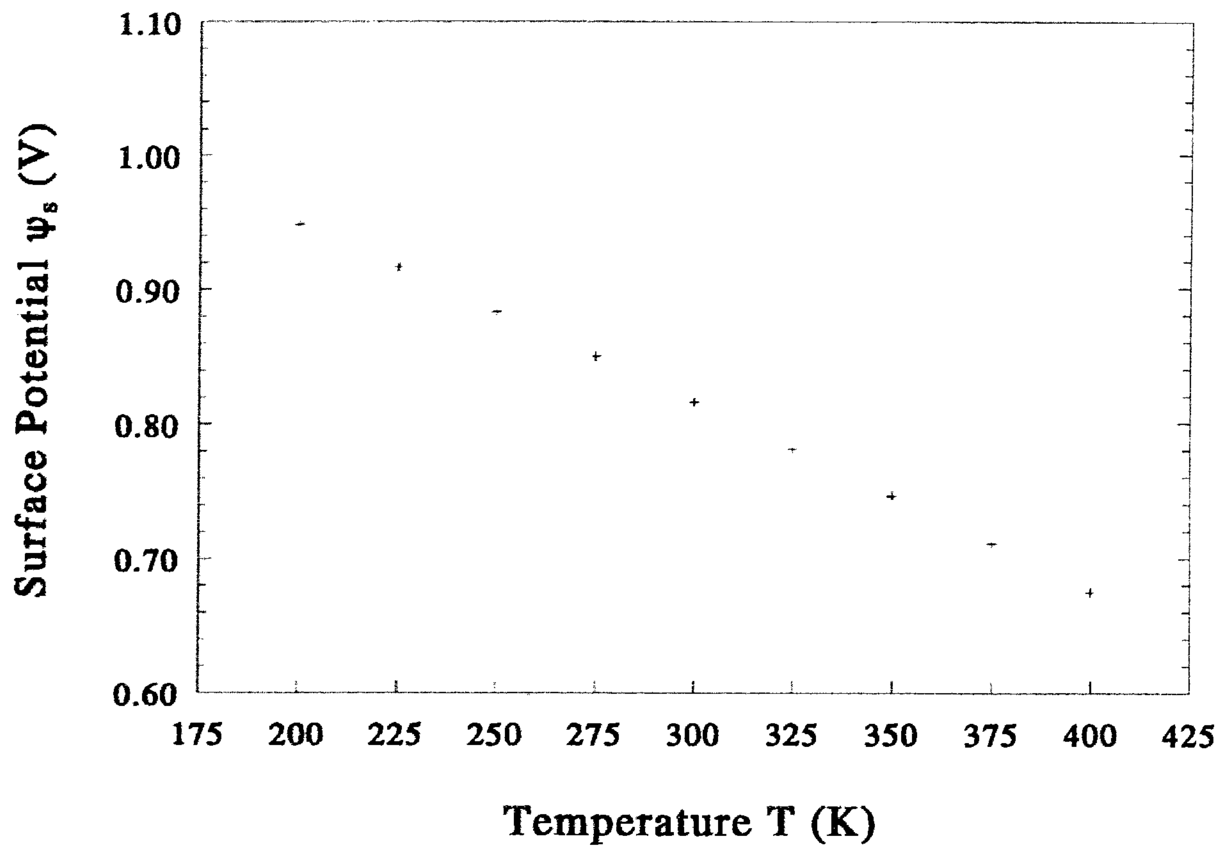


Figure 5.2.10. ψ_s vs T at V_{ds} = 0.1 V and V_{sb} = 0 V.

Figs 5.2.11 and 5.2.12 show the variation of V_T as a function of temperature for both channel length and channel width devices at varying V_{ds}. Again, both graphs show V_T increases almost linearly with decreasing temperature. As mentioned earlier, the DIBL effect can be used to explain why the value of V_T at V_{ds} = 0.1 V is higher than that at V_{ds} = 0.5 V. The lateral field between the diffusion junctions increases as V_{ds} increases, and hence reduces V_T.

Figs 5.2.13 and 5.2.14 show α_1 and α_3, respectively, as a function of temperature at different V_{sb}. By using linear regression, the rate of increase for α_1 and α_3 is 2.73E-3 and 3.64E-3, respectively, for each Kelvin. As expected, the values of α_1 and α_3 are smaller at lower temperature because of decreased depletion width w_D around the source and the drain. In eqn (2.3.5), w_D can be shown as a function of temperature variations and voltage biasing because both built-in potential and substrate concentration are temperature-dependent. Figs 5.2.15 and 5.2.16 show w_D as a function of temperature for varying V_{ds} and V_{sb}, respectively. The depletion width w_D changes with temperature can be due to both the terms V_t and n_i. Eventhough both terms contribute to the decrease at lower temperatures, the effect of V_t on decreasing V_T is stronger than that of n_i. The charge density of the intrinsic semiconductor decreases at lower temperature causing the built-in potential of the junction between the diffusion regions and the substrate to decrease, and α_1 and α_3 will be lower. Therefore, V_T increases as temperature decreases. Figs 5.2.13 and 5.2.14 graphs also show that the dependence of V_{sb} at lower temperatures is not as strong as at higher temperatures. Carrier freeze-out or hot-electrons effect in the sustrate can cause V_T to be less sensitive to V_{sb} at low temperatures.

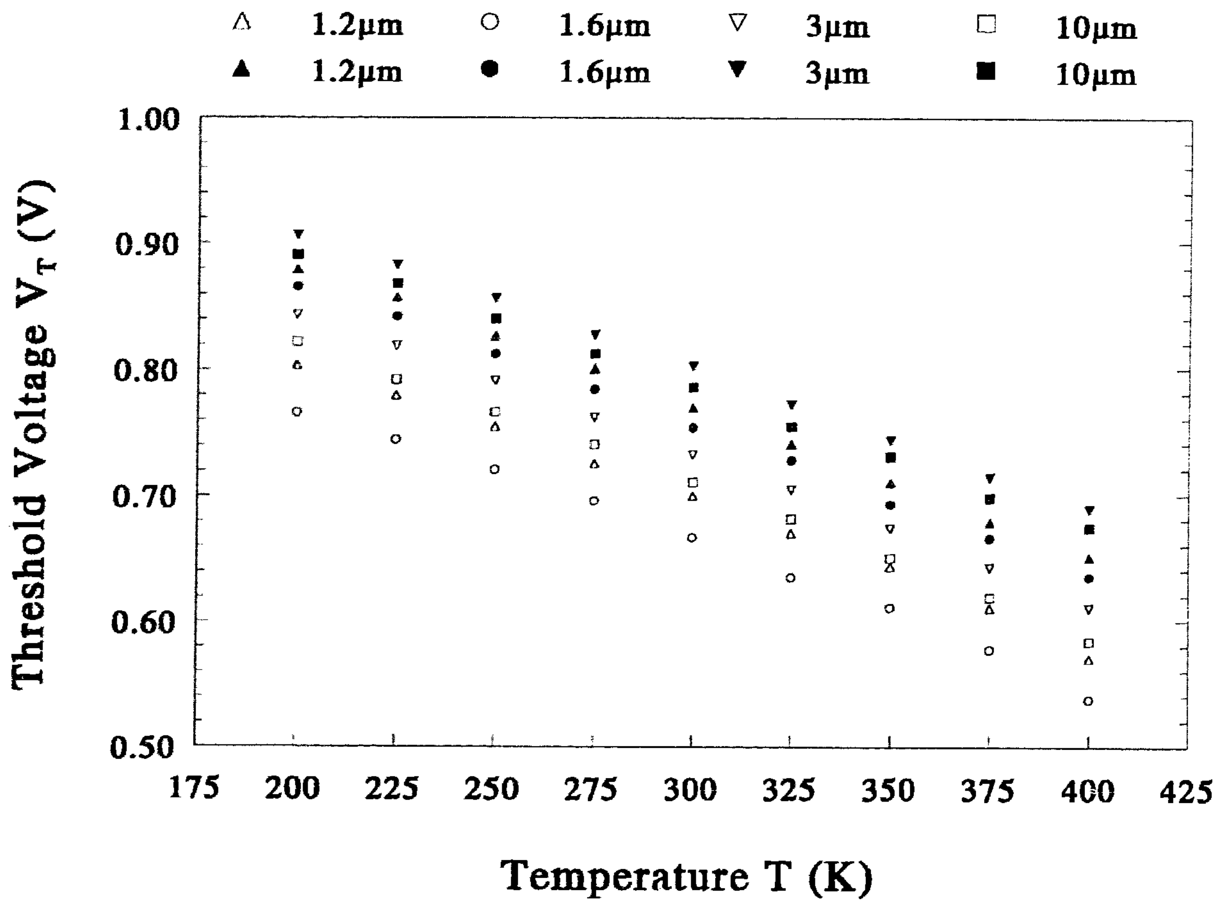


Figure 5.2.11. V_T vs T for different L_m at V_{ds} = 0.1 V & 0.5 V, and V_{sb} = 0 V. Note that the outline symbol denotes the data set at V_{ds} = 0.1 V and the solid-filled symbol for V_{ds} = 0.5 V.

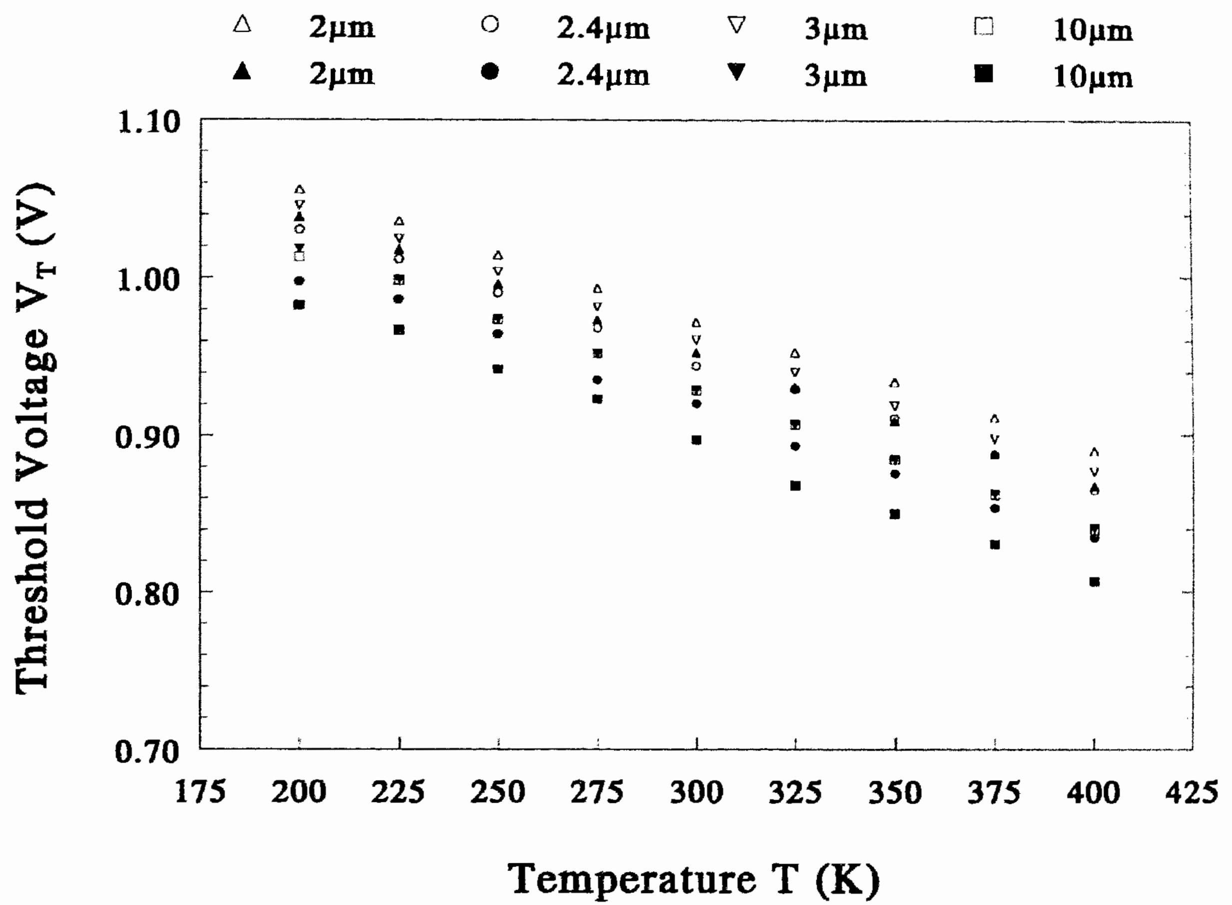


Figure 5.2.12. V_T vs T for different W_m at V_{ds} = 0.1 V & 0.5 V, and V_{sb} = 3 V. Note that the outline symbol denotes the data set at V_{ds} = 0.1 V and the solid-filled symbol for V_{ds} = 0.5 V.

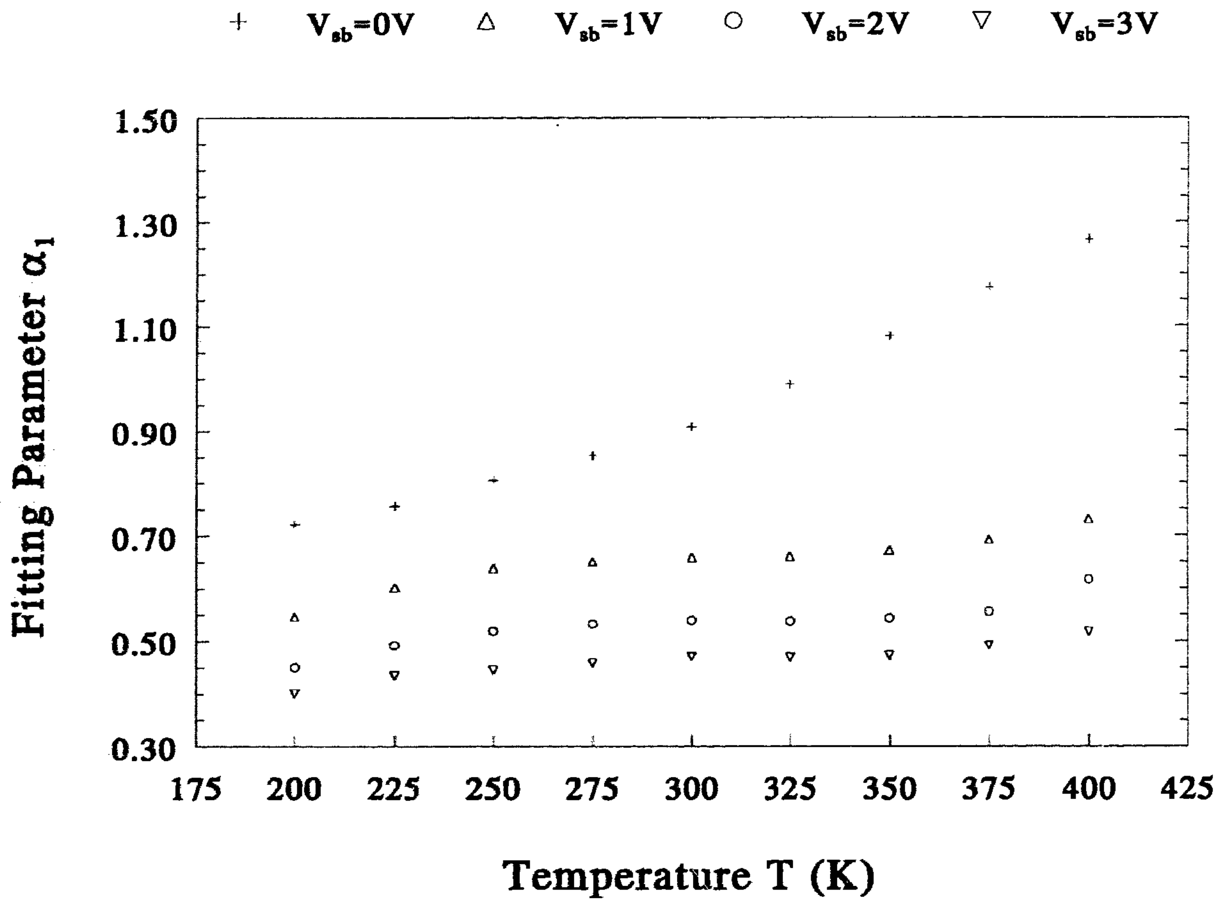


Figure 5.2.13. α_1 vs T for different V_{sb}.

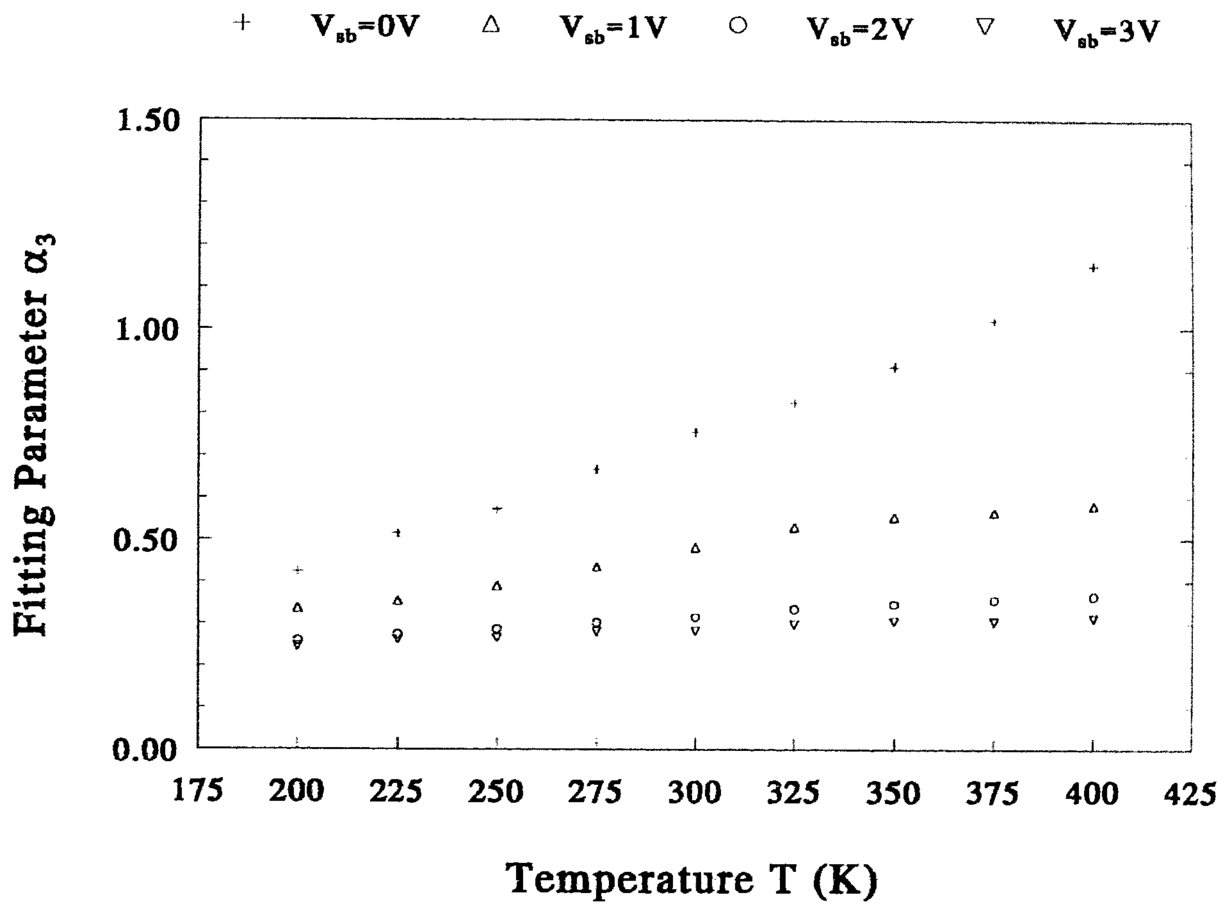


Figure 5.2.14. α_3 vs T for different V_{sb}.

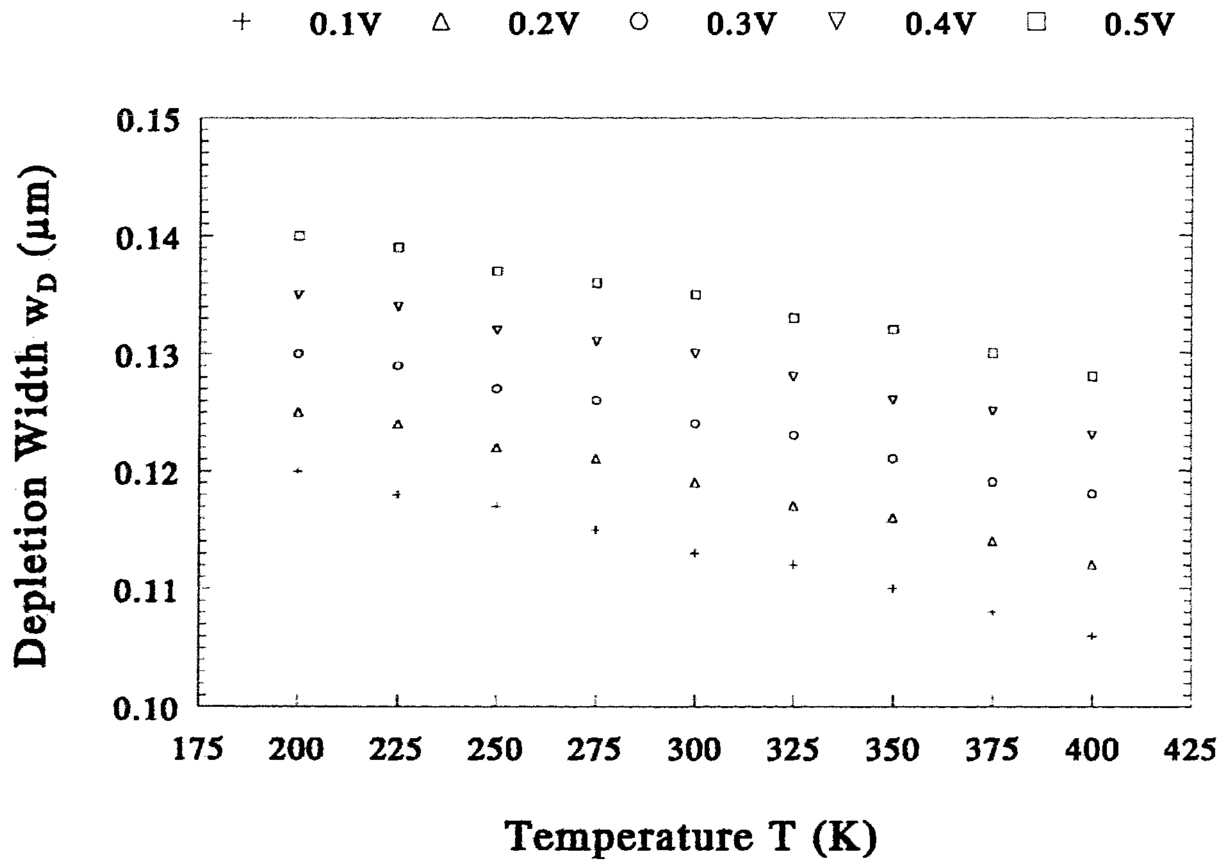


Figure 5.2.15. w_D vs T for different V_{ds}.

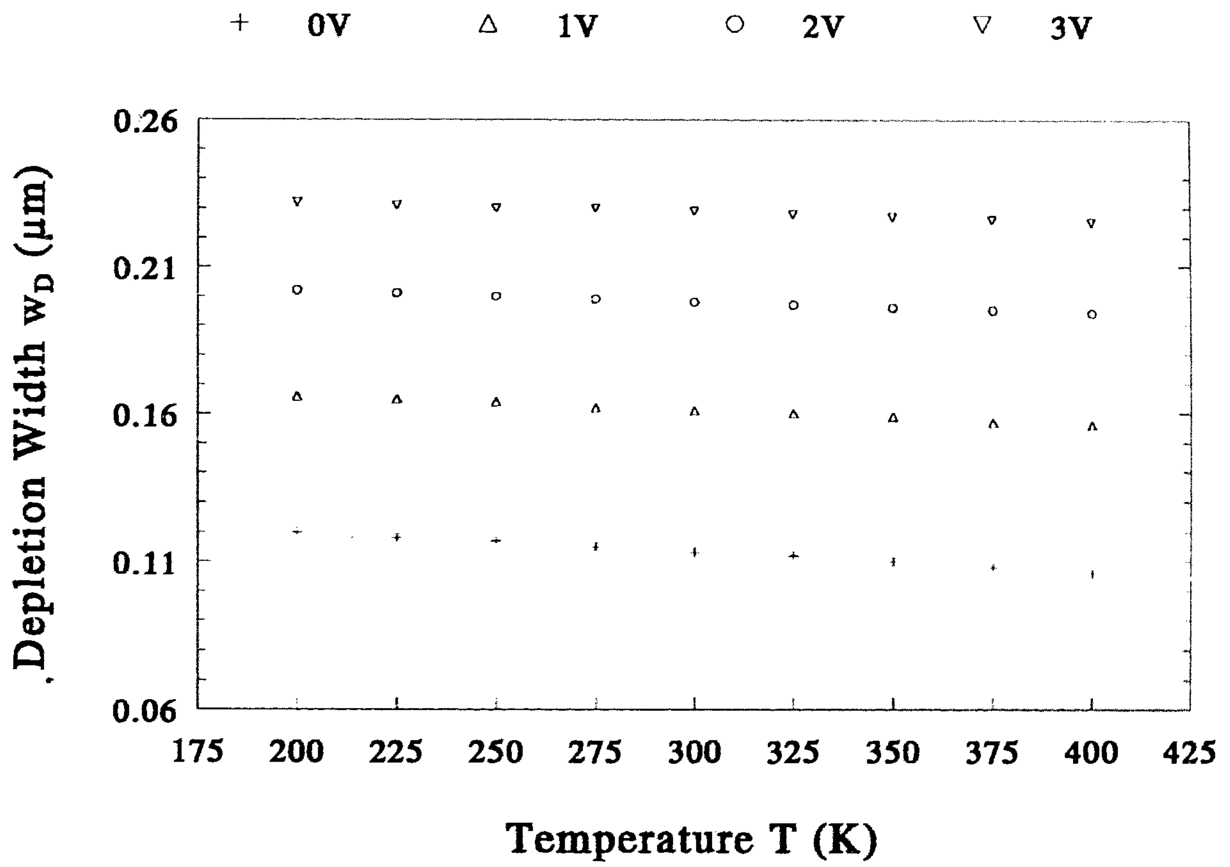


Figure 5.2.16. w_D vs T for different V_{sb}.

Fig 5.2.5 also shows how both α_1 and α_3 varies with V_{sb} at room temperature. In order to further illustrate the effect of temperature on α_1 and α_3, Figs 5.2.13 and 5.2.14 are plotted for different channel length and channel width devices, respectively. Both figures illustrate how the effect of temperature can affect both α's. For all devices, both α_1 and α_3 increase with temperature.

The subthreshold slope S is considered to be one of the important parameter in down-scaling CMOS devices, for reason described in Chapter 2. In Chapter 2, the small geometry effect on S was discussed and the S expression for small geometry devices of uniformly-doped channel was derived. As the devices used in this study are nonuniformly-doped, their behaviour will be different from those presented in Eqns (2.3.14) and (2.4.6). Figs 5.2.17 and 5.2.18 show the extracted values of S as a function of temperature for short-channel and narrow-width devices, respectively. Both figures show S was almost linearly dependent on temperature, and it is in agreement with Eqn (2.2.25) in which S is proportional to temperature from the term V_t. Since I_{ds} for narrow-width devices are much smaller than that of short-channel ones, the noise had more impact on narrow-width devices than on short-channel ones. As described in Eqn (2.3.14), the theory predicted that S for short-channel devices should be smaller than the long-channel ones but the result in Fig 5.2.17 shows S is greater for short-channel devices. According to Eqn (2.2.24), the values of S for narrow-width devices are slightly higher than that of wider ones.

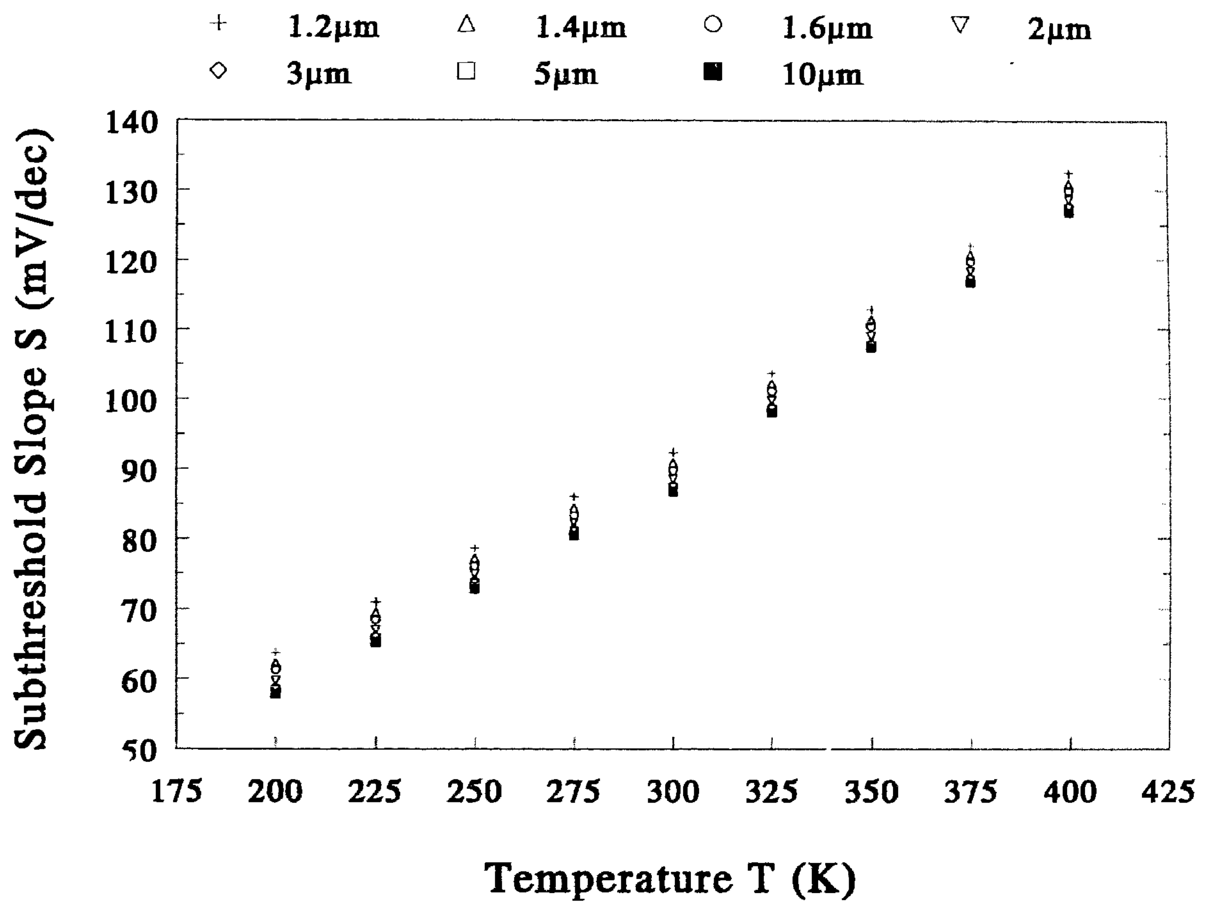


Figure 5.2.17. S vs T for different L_m at V_{ds} = 0.1 V and V_{sb} = 0 V.

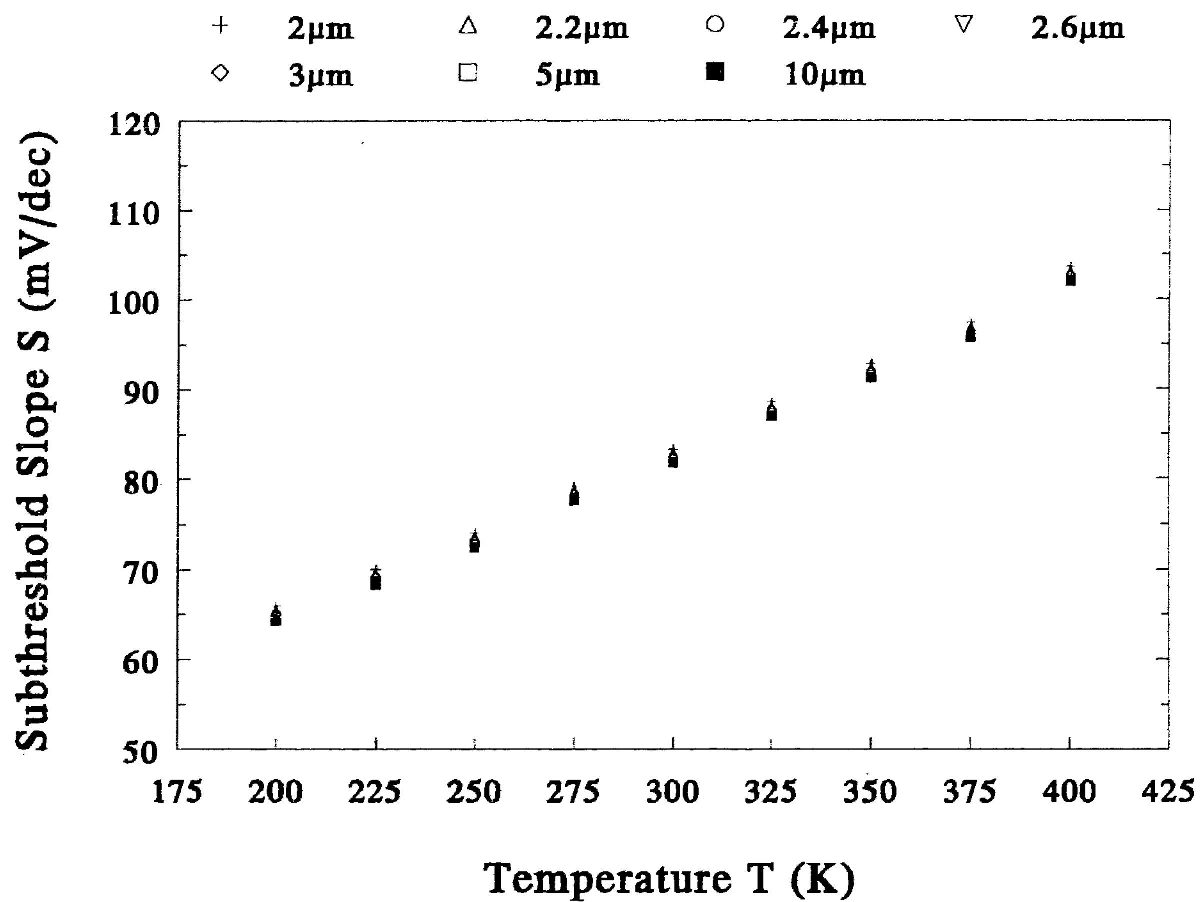


Figure 5.2.18. S vs T for different W_m at $V_{ds} = 0.1$ V and $V_{sb} = 0$ V.

The result of S as a function of L_m and W_m for different V_{sb} at T = 300 K are shown in Figs 5.2.19 and 5.2.20, respectively. Fig 5.2.19 shows S is better at higher V_{sb} because the parameter C_D in Eqn (2.3.13) decreases as V_{sb} increases. It can be shown, from this figure, S increases as channel length L decreases and it increases quite significantly when L_m is less than 2 μm. For short-channel devices, the full effect of depletion region bulk charge on the threshold voltage is reduced due to charge sharing model. Because of this reduction, the surface potential ψ_s for a given V_{gs} increases leading to an increase in subthreshold current. The nonuniform-doping may possibly contribute to an increase in S for short-channel device. For narrow-width devices, the increase of I_{ds} causes S to decrease with increasing channel width. From Figs 5.2.17 to 5.2.20, it can show that S can be improved at lower temperature, and it also depends on the channel doping uniformity and the quality of oxide.

Finally, the effects of short-channel, narrow-width and temperature variation on V_T and S, which were discussed in this section, are summarized in Table 5.2.1.

Table 5.2.1. The effects of short-channel, narrow-width and temperature variation on V_T and S. Note that the uparrow (↑) denotes an increase in value with respect to biasing and downarrow (↓) shows a decrease.

	V_T	S
short-channel effect	↓	↑
narrow-width effect	↑	↑
T increase	↓	↑

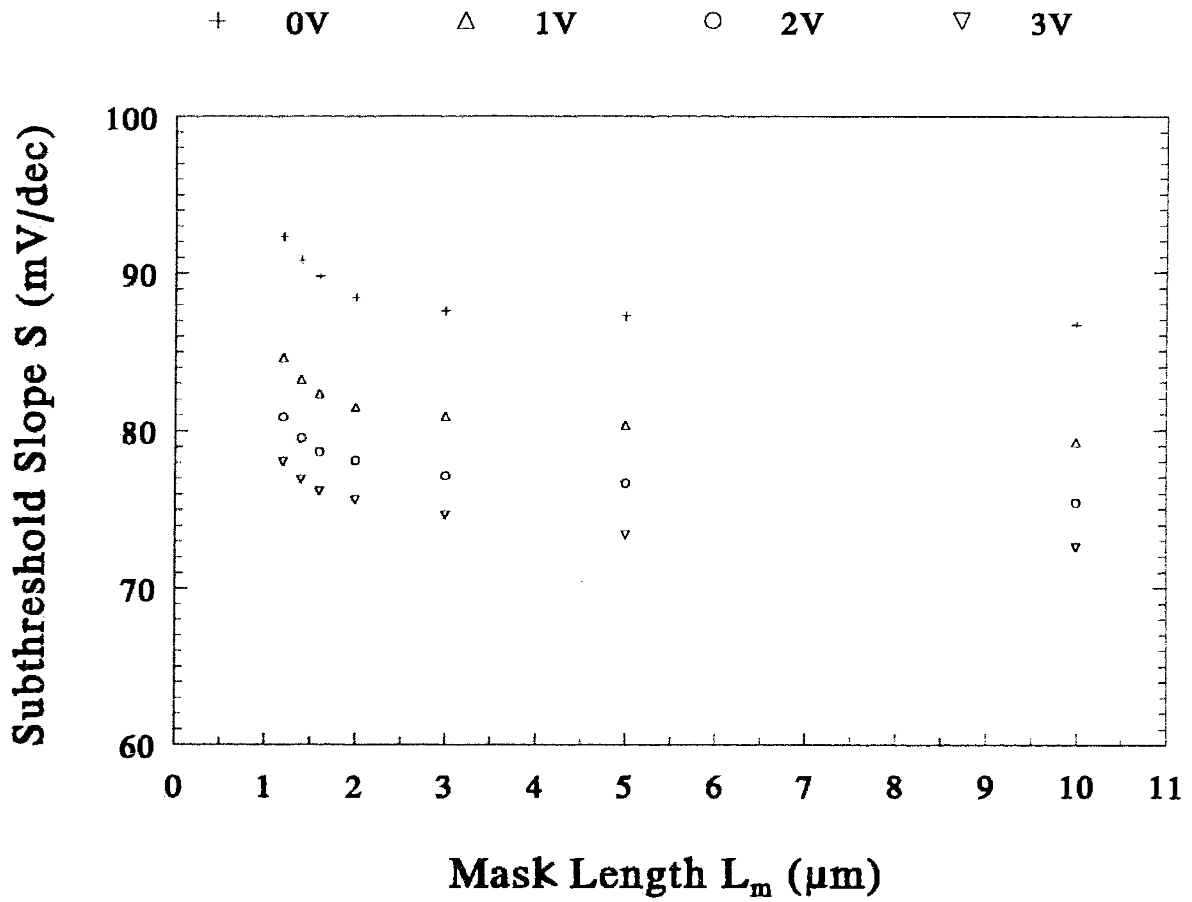


Figure 5.2.19. S vs L_m for different V_{sb} at V_{ds} = 0.1 V and T = 300 K.

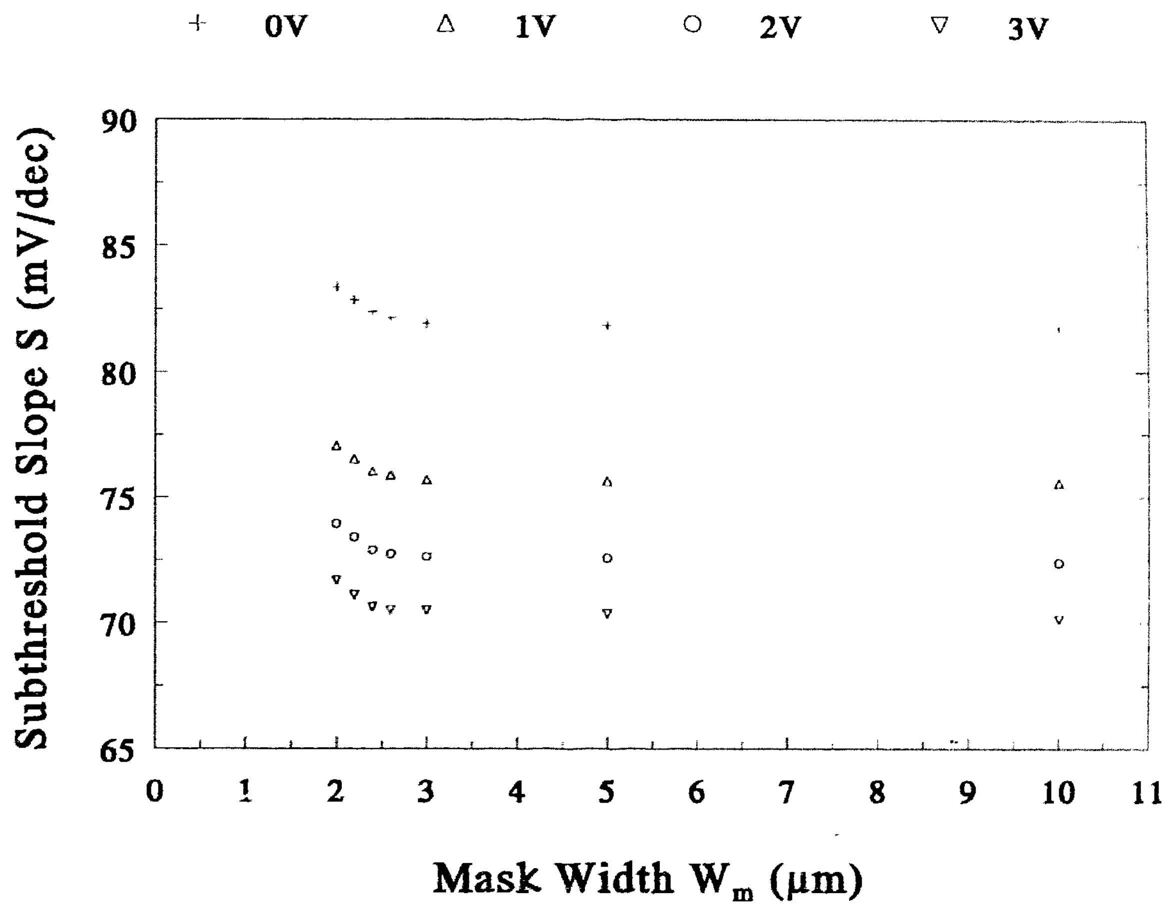


Figure 5.2.20. S vs W_m for different V_{sb} at V_{ds} = 0.1 V and T = 300 K.

5.3 g_m AND μ

As stated earlier, the maximum transconductance $g_{m,max}$ was used to determine the inflection point of I_{ds}-V_{gs} curve. This $g_{m,max}$ value is important to device and circuit designers since it corresponds to the gain factor of the devices. As such, $g_{m,max}$ is plotted as a function of temperature for different channel lengths and channel widths in Figs 5.3.1 and 5.3.2, respectively. As shown in both figures, $g_{m,max}$ is higher at 200 K than at 400 K due to larger carrier mobility, and simultanoeusly $g_{m,max}$ degradation is more severe at 200 K than at 400 K due to higher surface degradation. Also, the geometry of the device has an impact on the value of $g_{m,max}$.

One important parameter that is closely related to $g_{m,max}$ is the mobility of charge carriers μ_o. In addition to demonstrating the fundamental properties of the material as well as of the device, μ_o provides an important role in device and circuit performance. Because current flows in the inversion layer, mobility is expected to be influenced by the thickness of the inversion layer and therefore, it can be affected by temperature. Other parameters such as gate bias and substrate bias degradations can be found by using Eqns (2.3.27) and (5.2.1).

Since μ_o is calculated at low field, it should be the same for all devices, and it should not depend on any device parameters, only on operating temperature. As such, Fig 5.3.3 shows the variation of μ_o as a function of temperature. It shows μ_o for narrow-width devices is slightly smaller than that from short-channel devices. For instance, the values of μ_o at room temperature are 410 $cm^2/V.s$ for varying channel length devices and 390

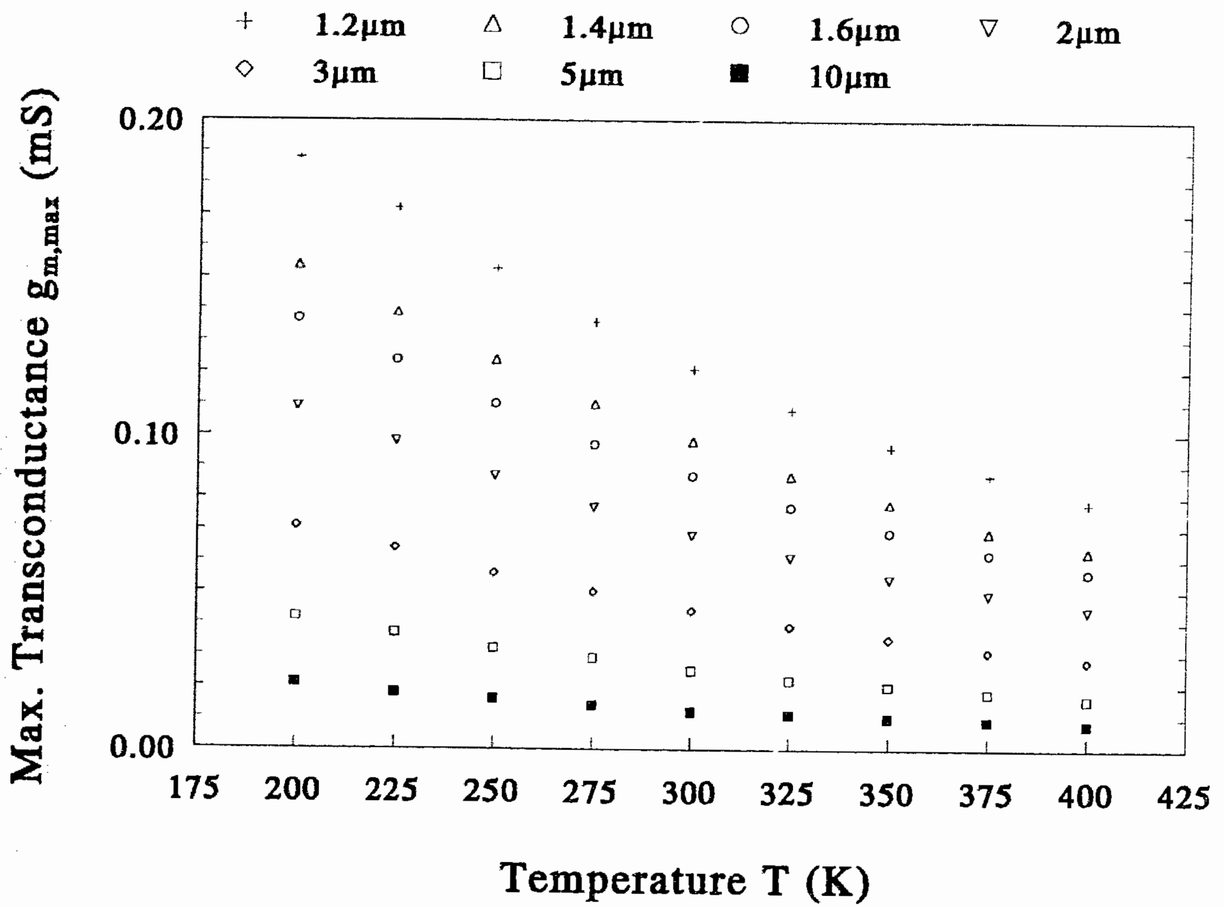


Figure 5.3.1. $g_{m,max}$ vs T for different L_m at V_{ds} = 0.1 V and V_{sb} = 0 V.

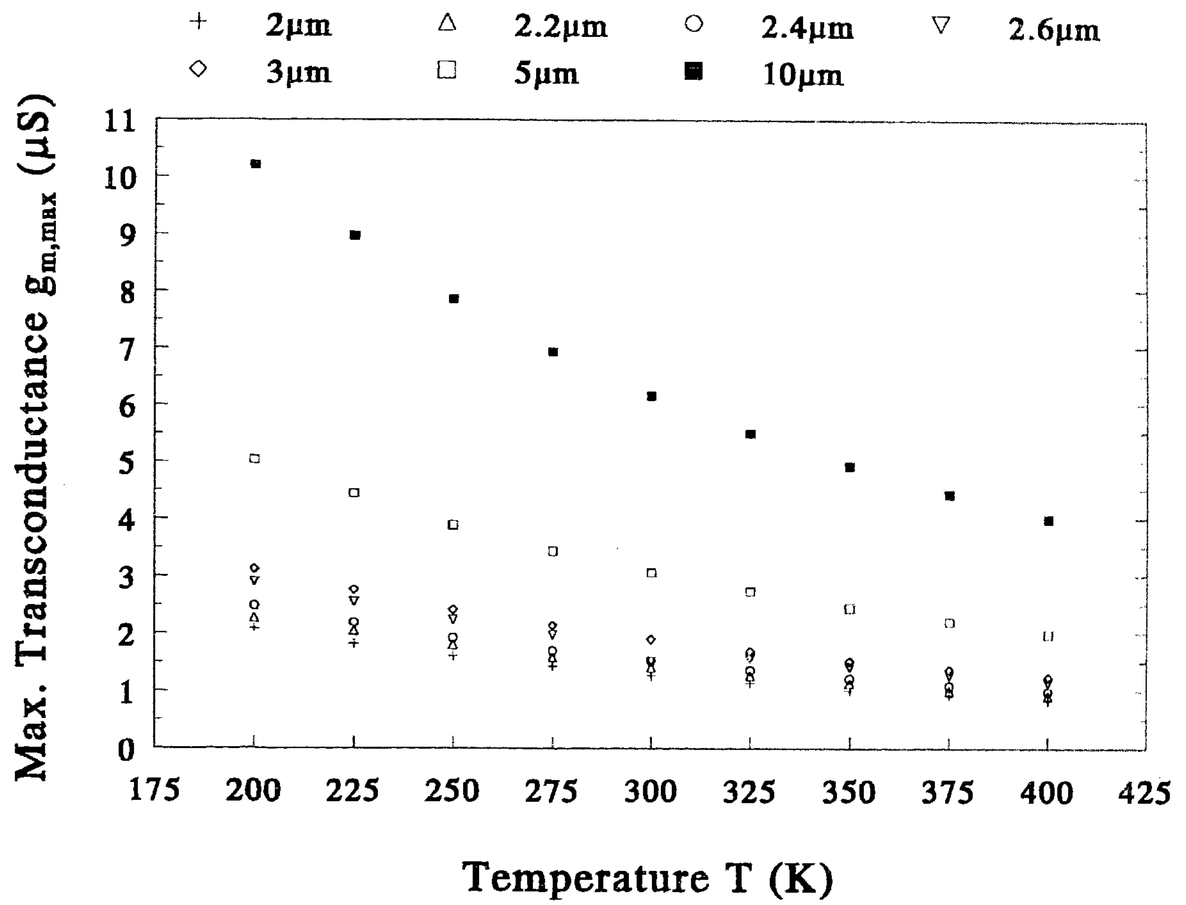


Figure 5.3.2. $g_{m,max}$ vs T for different W_m at V_{ds} = 0.1 V and V_{sb} = 0 V.

Figure 5.3.3. μ_o vs T for different L_m and W_m.

$cm^2/V.s$ for varying widths devices. The reason is that the I_{ds} data of the former is about an order or two magnitude smaller than that of the latter due to narrow channel width, and hence the data for varying channel width device are more noisy. However, they show the same dependence on temperature.

A strong vertical force between the gate and substrate attracts the carriers to the silicon surface. When the source and the drain experience a potential difference, the carriers travelling at the silicon surface encounter scattering and retardation due to surface roughness. The surface degradation factor θ_0 is used to measure the silicon surface roughness scattering. Its dependence on temperature shows an increase with decreasing temperature, as shown in Fig 5.3.4. Also, θ_0 for short-channel devices are greater than the narrow-width ones because the horizontal field is coupled more strongly to the vertical field in the short-channel devices. For varying length devices, θ_0 decreases from 0.088 at T = 200 K to 0.025 at T = 400 K and it increases from 0.085 to 0.023 for the same temperature range for varying width devices.

Figs 5.3.5 and 5.3.6 show the result of the substrate bias degradation factor θ_B for varying channel length and width devices, respectively, as a function of temperature at V_{sb} = 3 V. This degradation exists because increasing V_{sb} also increases the vertical field in the channel. The vertical field restricts the movement of the carriers in the silicon surface and thereby affects its mobility. Both graphs show θ_B decreases as temperature increases.

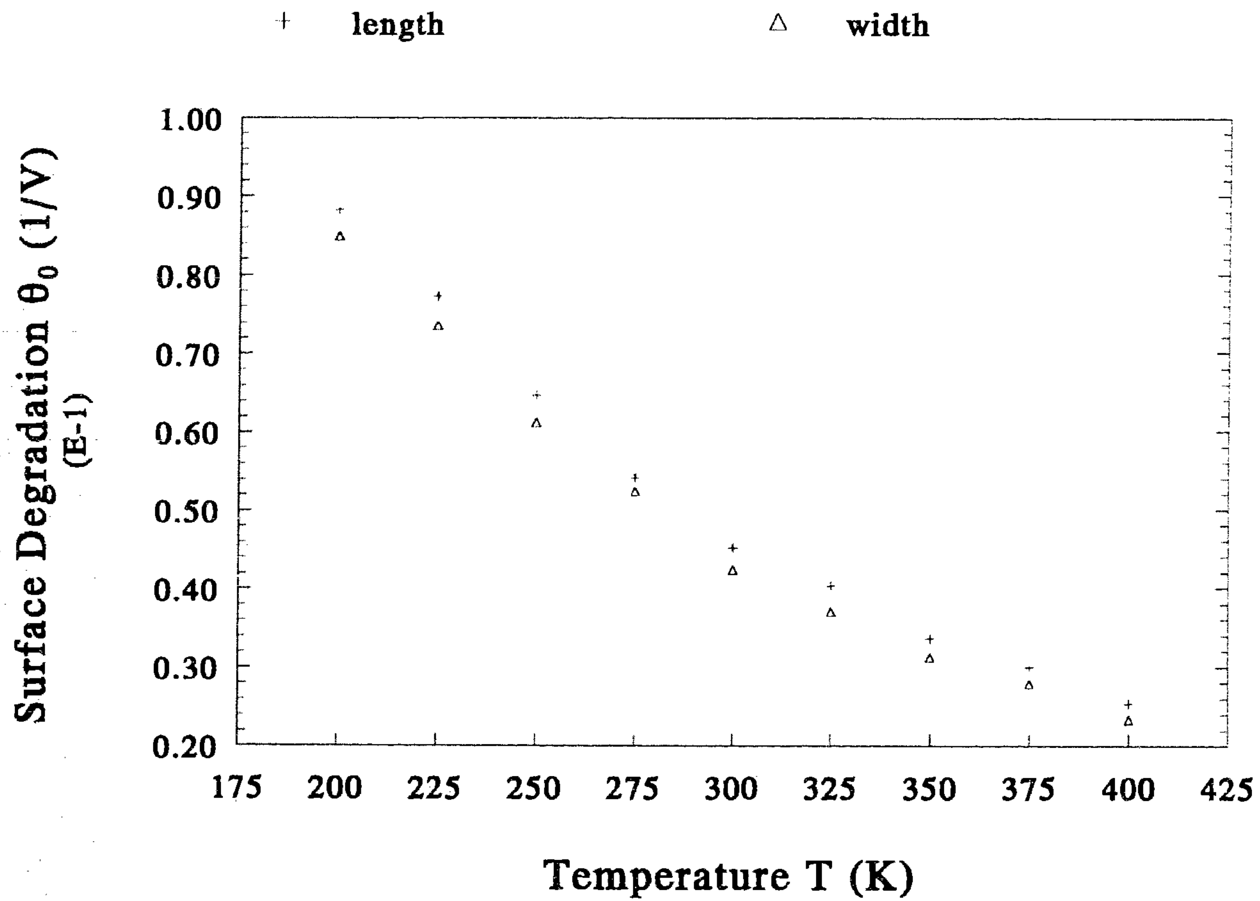


Figure 5.3.4. θ_0 vs T for different L_m and W_m.

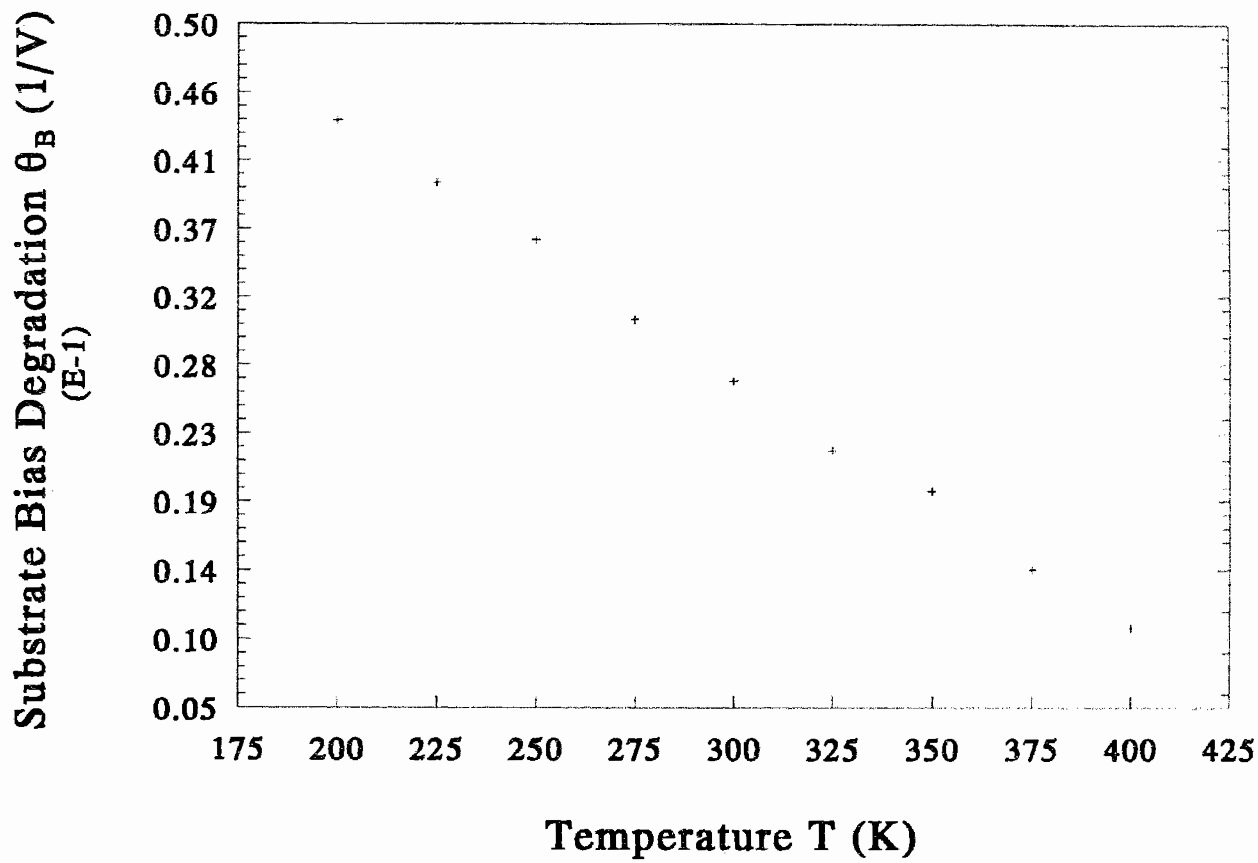


Figure 5.3.5. θ_B vs T for different L_m

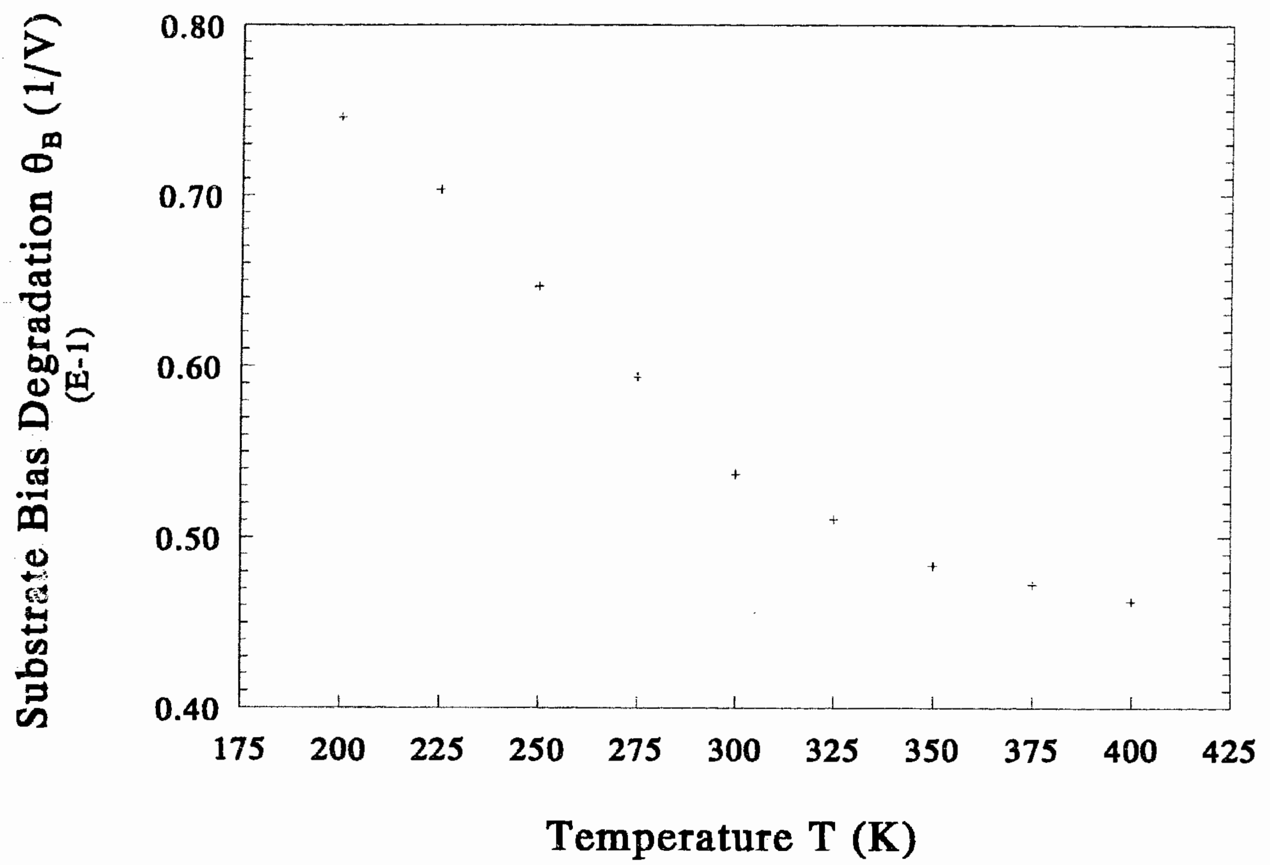


Figure 5.3.6. θ_B vs T for different W_m.

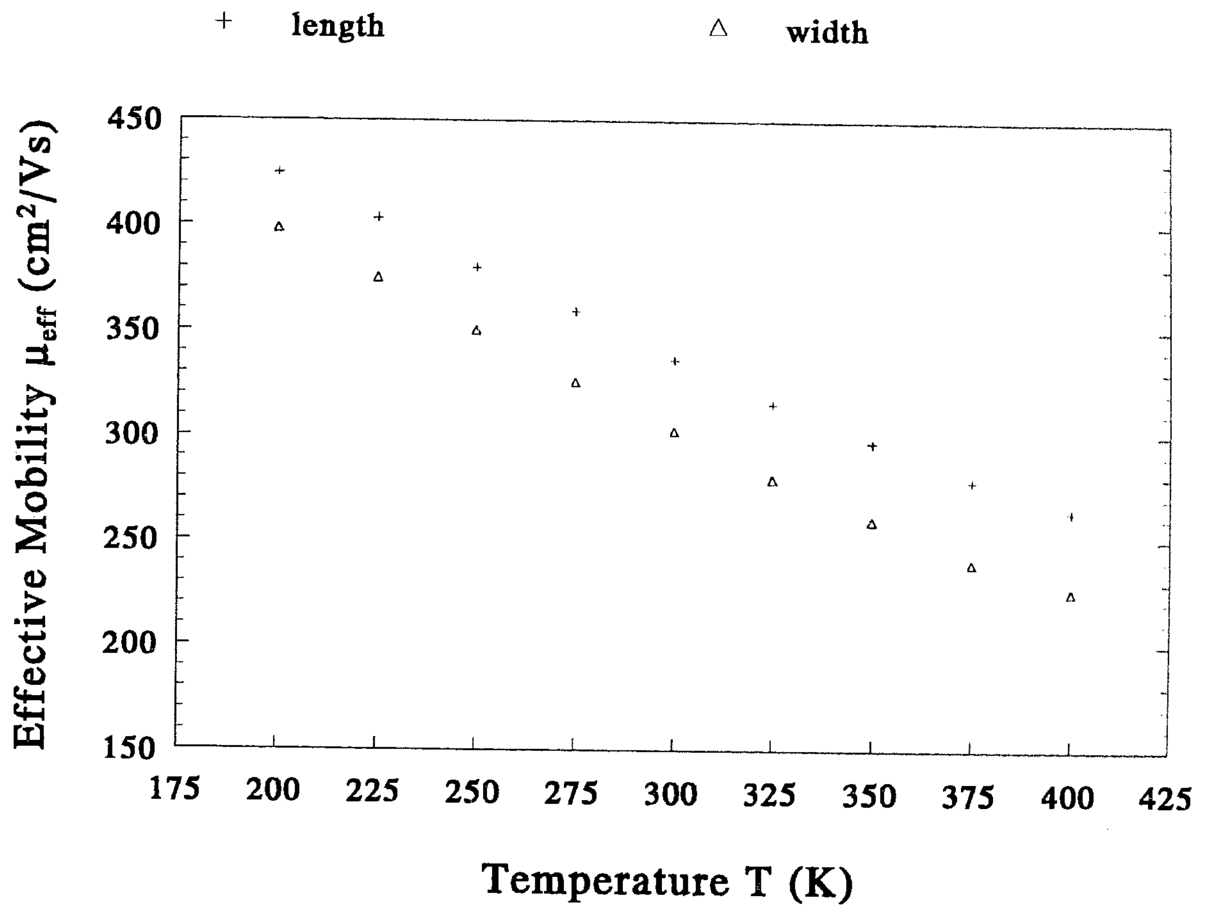


Figure 5.3.7. μ_{eff} vs T.

The effective carrier mobility μ_{eff}, which is defined in Eqn (2.3.27), is sometimes more useful than μ_o, especially in analog circuits. μ_{eff} is calculated using Eqn (2.3.27) and the extracted parameters, and the result is plotted against temperature at V_{ge} = 3 V and V_{sb} = 3 V in Fig 5.3.7. The graph indicates that μ_{eff} increases for all devices as temperature decreases. As temperature increases, the effective mobility for different channel length decreases from 424 $cm^2/V.s$ at T = 200 K to 264 $cm^2/V.s$ at T = 400 K and it decreases from 398 $cm^2/V.s$ to 225 $cm^2/V.s$ for the same temperature range for varying width devices.

The effects of short-channel, narrow-width, voltage biasing and temperature variation on $g_{m,max}$, μ_o and other parameters are summarized in Table 5.3.1.

Table 5.3.1. The effects of short-channel, narrow-width, voltage biasing and temperature variation on $g_{m,max}$, μ_o, μ_0 and μ_B. Note that the uparrow (↑) denotes an increase in value with respect to biasing and downarrow (↓) shows a decrease. The shaded area implies that data is not applicable or not available in this research.

	$g_{m,max}$ (L)	$g_{m,max}$ (W)	μ_o	θ_0	θ_B
short-channel	↑				
narrow-width		↓			
T increase	↓	↓	↓	↓	↓

5.4 R_p, ΔL, G_p AND ΔW

This section presents the most important results of this study. Due to short-channel and narrow-width effects, the parasitic parameters include R_p, ΔL for short-channel devices and G_p and ΔW for narrow-width devices. All the parameters were extracted using the methods described in the previous chapter. In particular, R_p and ΔL were extracted using the technique shown in Section 4.1 on short-channel devices whereas G_p and ΔW were extracted from narrow-width devices based on the scheme illustrated in Section 4.2. The physical meanings for these parameters were described in Chapters 2 and 4.

Figs 5.4.1 and 5.4.2 show the extracted values of R_p and ΔL, respectively, as function of effective gate biasing V_{ge} for different V_{ds} at room temperature and V_{sb} = 0 V. As expected, both graphs show the parasitic parameters decrease with increasing V_{ge}. The total parasitic resistance R_p decreases from 128 Ω for V_{ge} = 0.6 V to about 78 Ω for V_{ge} = 3.4 V. Simultaneously, ΔL reduces from 0.2 μm to 0.09 μm. As V_{ge} increases, the decrease of both parasitics is due to the fact that the gate covers part of the n^- regions, and the fringing field in the spacer oxide at the drain side increases with V_{ge} at a constant V_{ds}. The carrier concentration in the n^- regions increases as V_{ge} increases, and hence the extrinsic resistance at the drain side decreases. The channel length near the drain is affected by the modulation of the charge concentration in the n^- region. As the concentration of the n^- regions approaches that of the n^+ region, the reduction ΔL decreases accordingly.

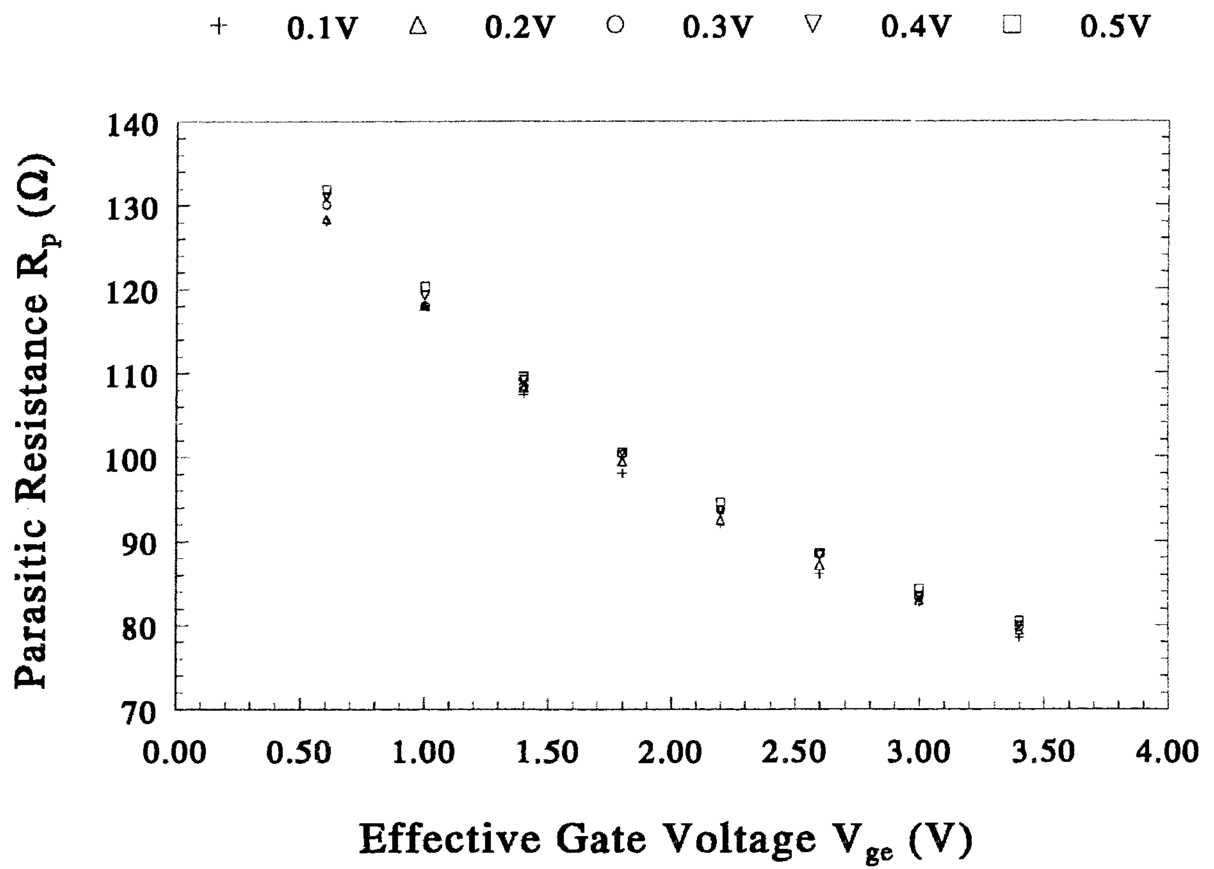


Figure 5.4.1. R_p vs V_{ge} for different V_{ds} at T = 300 K and V_{sb} = 0 V.

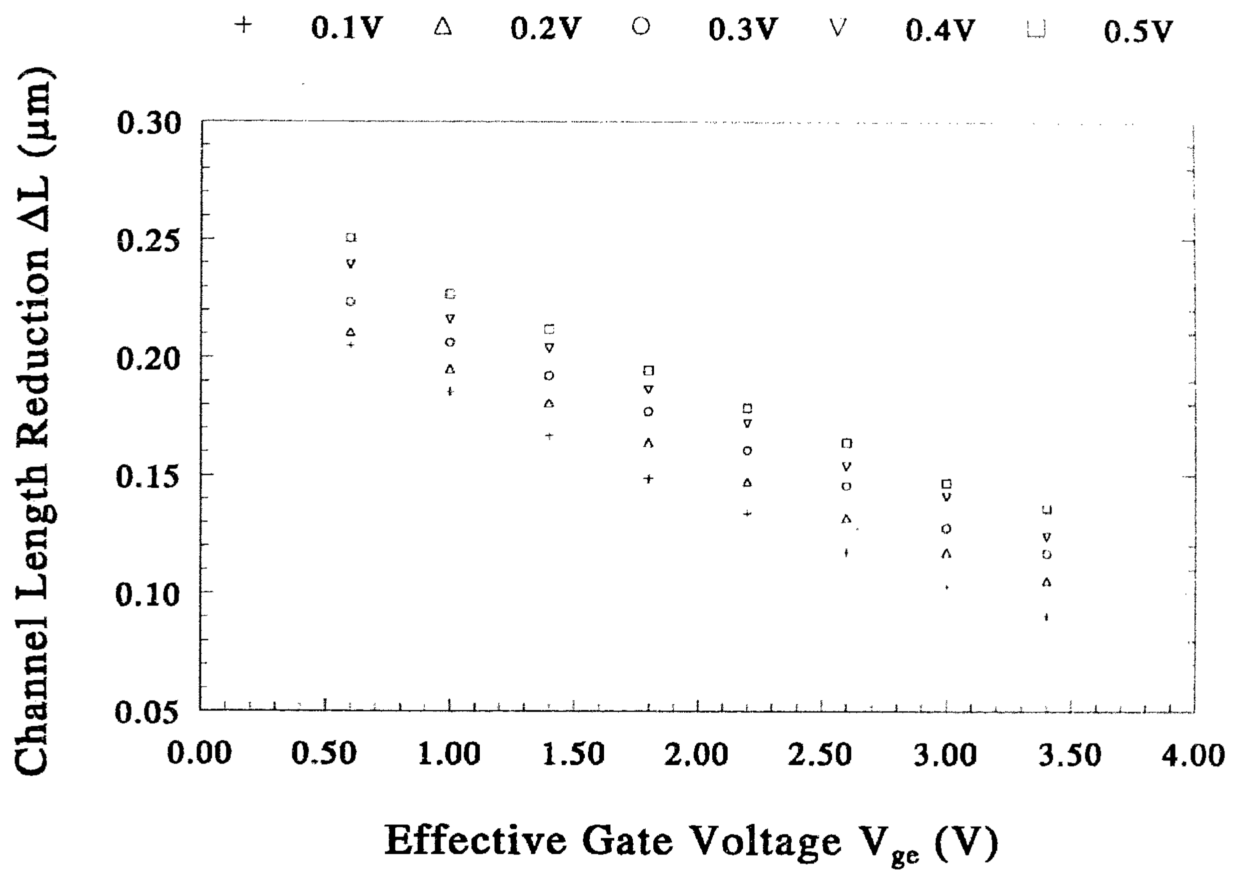


Figure 5.4.2. ΔL vs V_{ge} for different V_{ds} at T = 300 K and V_{sb} = 0 V.

From Figs 5.4.1 and 5.4.2, the values of R_p and ΔL increase as V_{ds} increases at a constant V_{gs}. The potential difference between V_{gs} and V_{ds} at the edge of the drain decreases as V_{ds} increases, the fringe field in the spacer oxide decreases and hence, decreases the carrier concentration in the drain n^- region. Also, when V_{ds} increases, the end point of the effective channel length at the drain side will move toward the source side and this increases the depletion width of a p-n junction at the drain side. As a result, ΔL increases with V_{ds} since the intrinsic drain point move toward the source side. Therefore, the parasitic resistance at the drain side increases as V_{ds} increases and this contributes to an increase in the total parasitic resistance R_p.

For narrow-width devices, the corresponding G_p and ΔW are plotted against V_{ge} for different V_{ds} at room temperature and V_{sb} = 0 V in Figs 5.4.3 and 5.4.4, respectively. G_p increases from 0.012 μS for V_{ge} = 0.6 V to about 0.42 μS for V_{ge} = 3.4 V, and ΔW increases from 0.07 μm to 0.18 μm. The actual values of both parameters are negative and only their absolute values are shown in the figures. From now on, $|\Delta W|$ denotes channel width increase. In order to explain the existence of negative parasitic conductance $-G_p$ and channel width reduction $-\Delta W$, it is important to look at the variation of the threshold voltage in the region from the intrinsic channel to the channel stop implant region under the field oxide. The doping density of the channel region increases toward the stop region. Simultaneously, the thickness of the oxide between the gate poly and these edges increases from the channel region to the stop region. Hence, the threshold voltage increases from under the intrinsic gate poly to under the field oxide due to increases in both the doping concentration of silicon surface and the thickness of oxide.

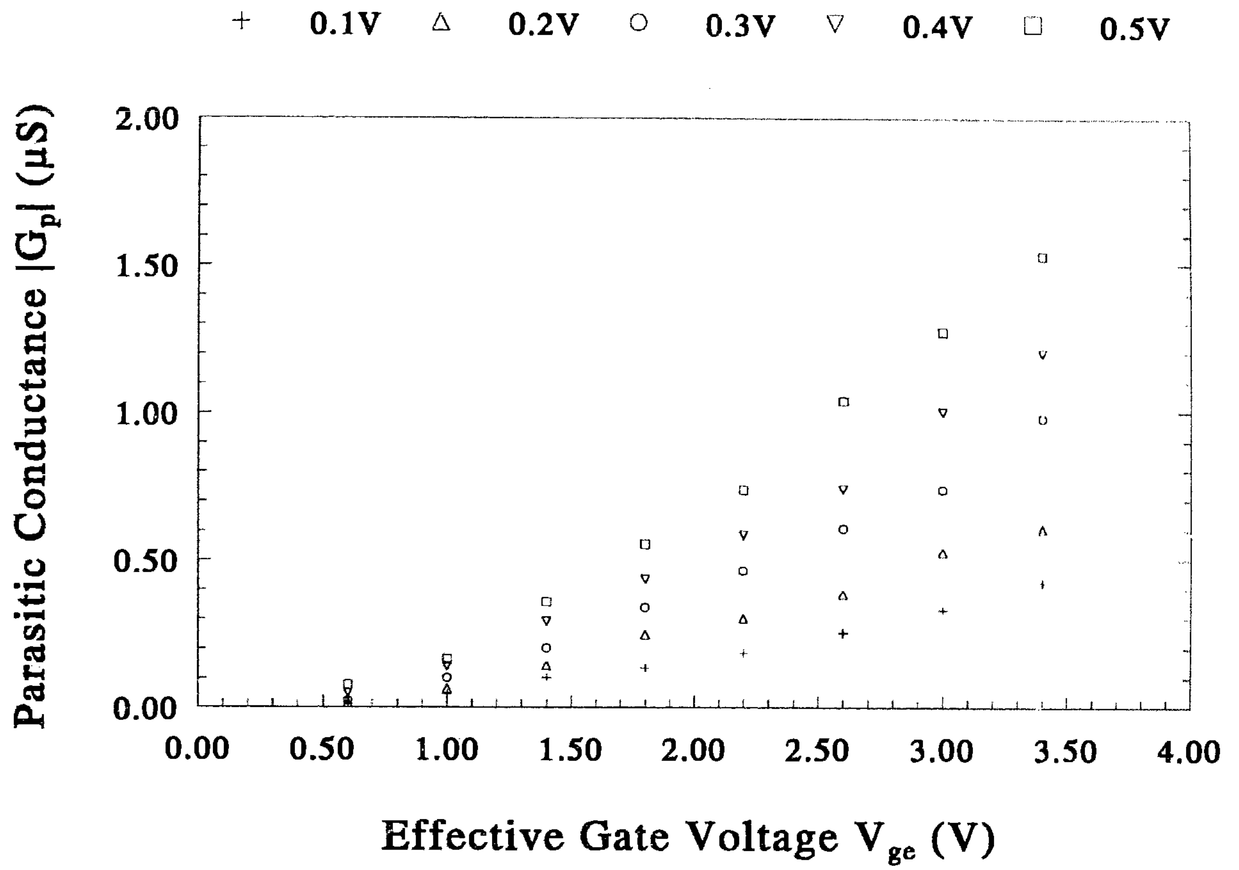


Figure 5.4.3. $|G_p|$ vs V_{ge} for different V_{ds} at T = 300 K and V_{sb} = 0 V.

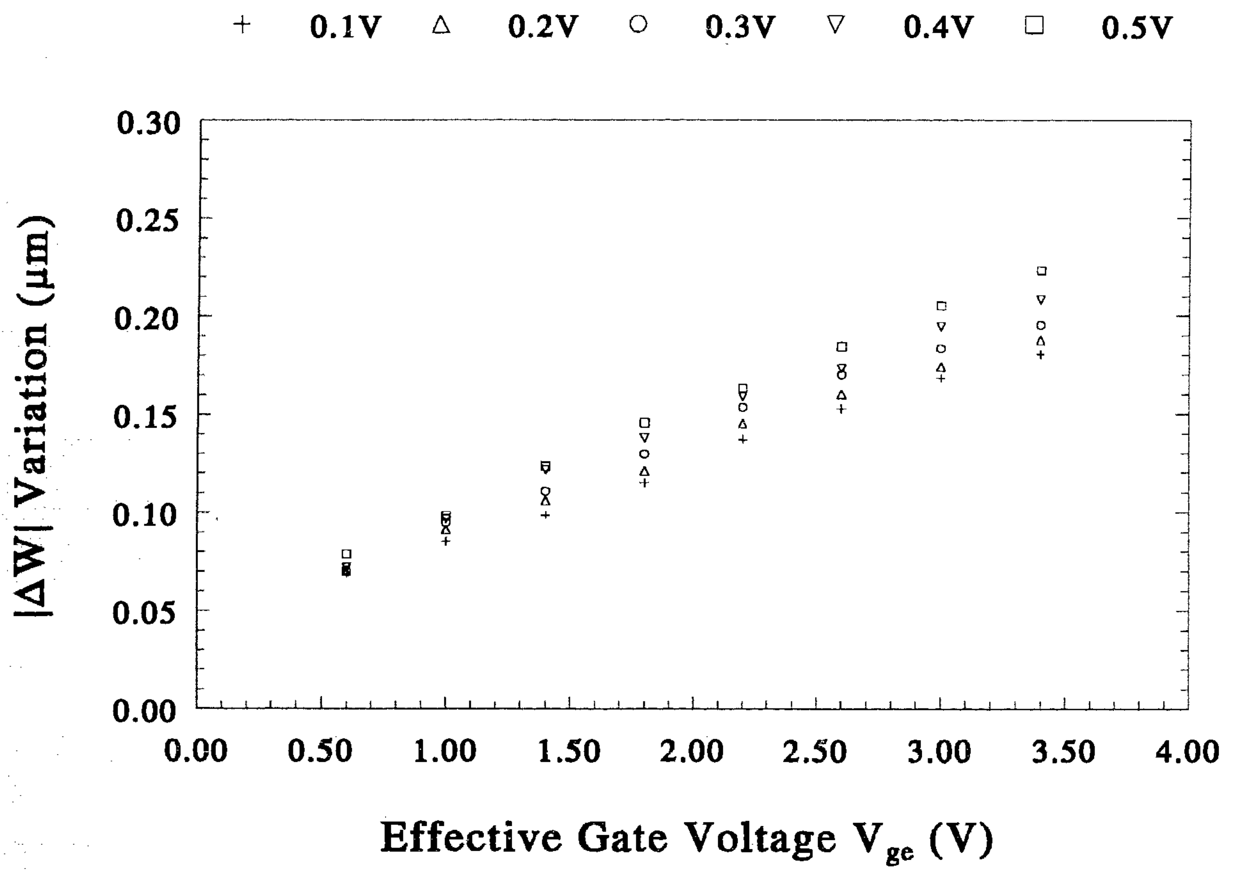


Figure 5.4.4. $|\Delta W|$ vs V_{ge} for different V_{ds} at T = 300 K and V_{sb} = 0 V.

As V_{ge} increases, more and more of these edges of the channel below the bird's beak structure become accumulated with charge carriers eventhough the threshold voltage of these edge regions under the field oxide is higher than the intrinsic channel. Due to an increase in these edge regions, the effective channel width is wider than design width. When the device channel is narrow, the increase of these edges becomes significant and appropriate to include in the modelling of narrow-width devices. Hence, the absolute value of ΔW increases with V_{ge} as shown in Fig 5.4.4. When these edge regions attain a certain surface potential, the "extra" carriers begin to accumulate and will contribute to the total drain current. Therefore, the value of $|G_p|$ increases with V_{ge} as shown in Fig 5.4.3. Since the value of I_{ds} obtained by Eqn (4.2.1) is the sum of the drain current of intrinsic channel and the current through the edges, an equivalent negative $|G_p|$ is required to compensate the edge effect caused by channel-width widening. Due to the variation of threshold voltage in these regions, the contribution of these carriers to the device conductance is not proportional to the increase in the effective channel width, as indicated by the curvature of $|G_p|$ in Fig 5.4.3. That is, $|G_p|$ increases quadratically whereas $|\Delta W|$ increases linearly. Both parasitic parameters for the narrow-width devices behave differently from R_p and ΔL of short-channel devices because the edges of the channel are increasingly easier to turn-on as the surface potential at these regions increases.

Figs 5.4.3 and 5.4.4 also show the effect of V_{ds} on parasitic conductance $|G_p|$ and channel width increase $|\Delta W|$ as function of gate biasing. Both parameters increase with V_{ds}. The effect of drain biasing shows that the increase of $|G_p|$ is not proportional to the increase in $|\Delta W|$. The existence of the edge regions and its corresponding parasitic

conductance is parallel to the intrinsic channel between the drain and the source. As V_{ds} increases, the potential difference between the drain and the source increases, and thereby increases the parasitic current in the edge regions. Therefore, the parasitic conductance of the edge regions increases faster than the increase in channel width.

The explanation to the effect of V_{sb} biasing on these parasitics is similar to that of changing V_{ds}. Figs 5.4.5 and 5.4.6 show the effect of V_{sb} biasing on R_p and ΔL, respectively, as function of V_{ge}. As V_{sb} increases, the depletion width at the drain side increases, contributing to an increase in ΔL. The depletion width at the source side also increases but does not contribute much to ΔL as the drain side. Since the potential of the drain side is higher than the source, the channel end point at the drain side moves toward the source side. The parasitic resistance at the drain side also increases because more of n^- regions are involved in calculating R_p. At fixed V_{sb} and increasing V_{ge}, both parameters decrease with increasing V_{ge} with the same implication as the one for varying V_{ds}. The concentration of the charge carriers in the channel and n^- regions increases.

Figs 5.4.7 and 5.4.8 show the effect of V_{sb} biasing on $|G_p|$ and $|\Delta W|$ as function of V_{ge}. $|G_p|$ and $|\Delta W|$ increase with V_{ge} for different V_{sb} at room temperature and fixed V_{ds} = 0.1 V. From Section 5.2, we know that the threshold voltage increases with V_{sb}. As V_{sb} increases, the depletion layer of the edges widens and its threshold voltage increases due to an increase of immobile charges in the depletion layer. Therefore, the parasitic current contributed by the edges should decrease as V_{sb} increases. However, this is not the case shown in Fig 5.4.7. It is because the value of V_{ge} includes V_T of the effective channel width.

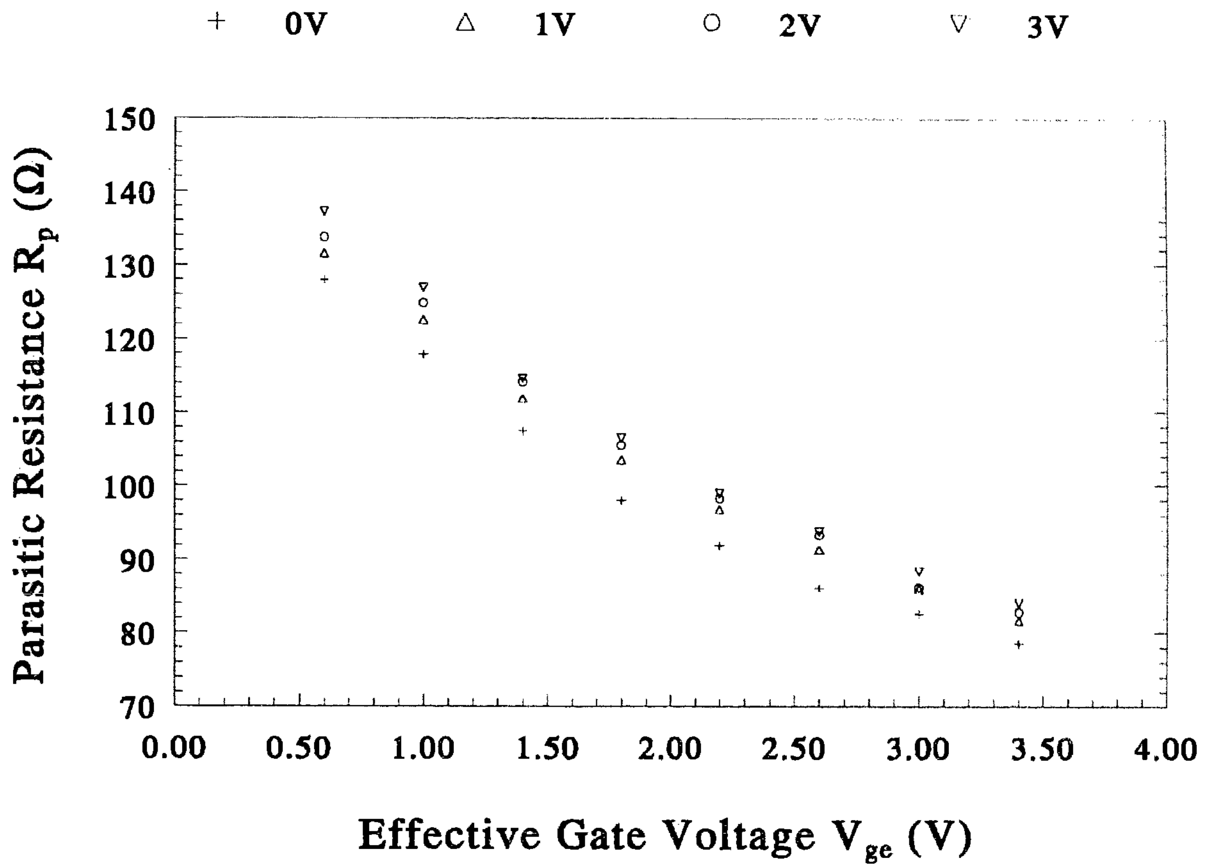


Figure 5.4.5. R_p vs V_{ge} for different V_{sb} at T = 300 K and V_{ds} = 0.1 V.

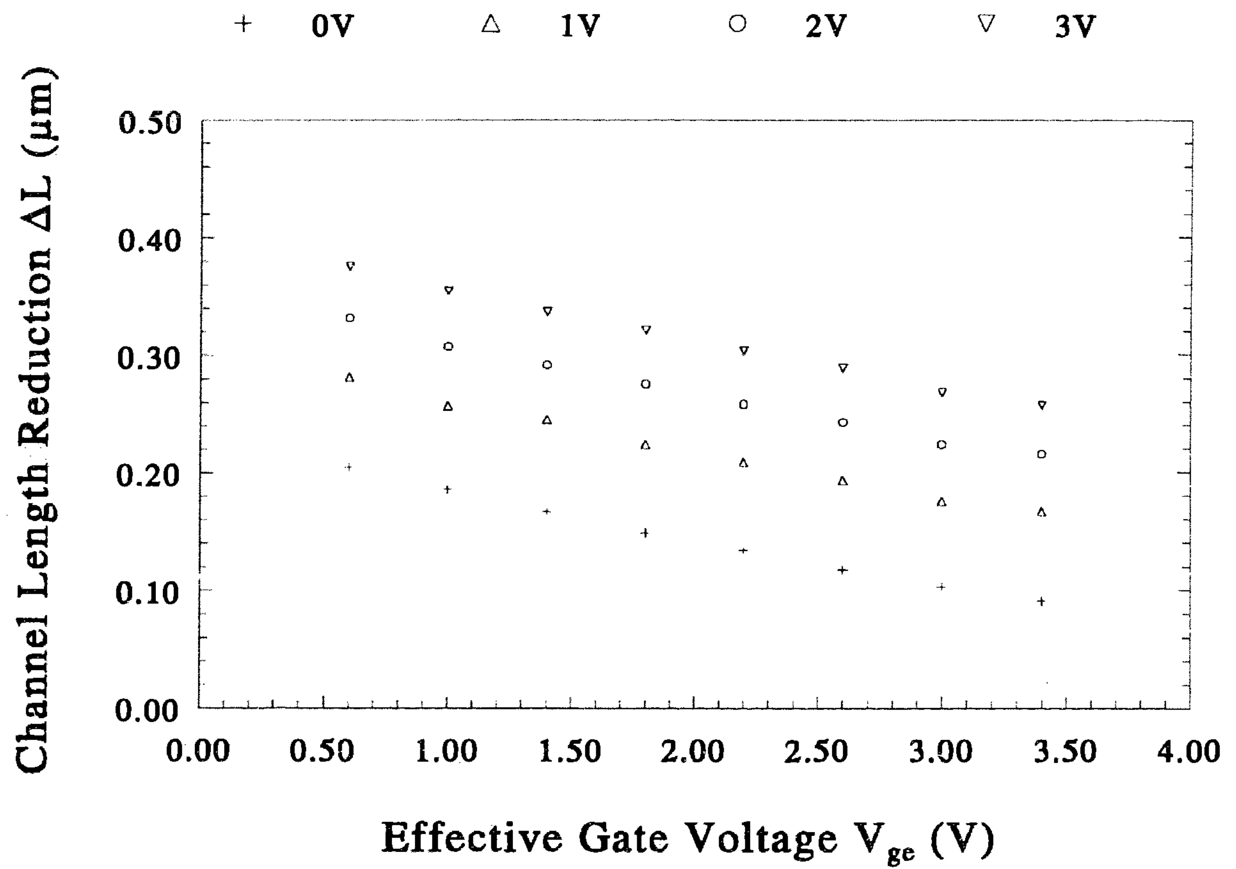


Figure 5.4.6. ΔL vs V_{ge} for different V_{sb} at T = 300 K and V_{ds} = 0.1 V.

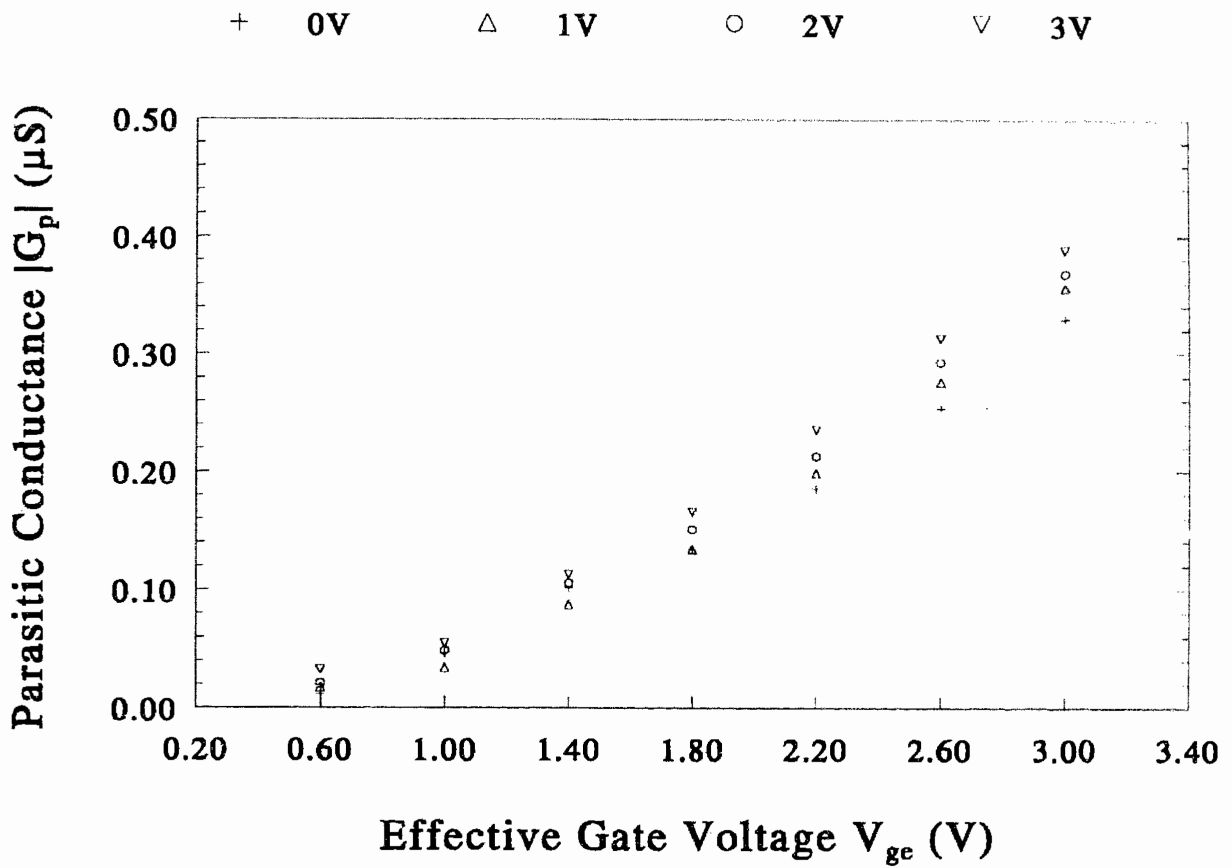


Figure 5.4.7. $|G_p|$ vs V_{ge} for different V_{sb} at T = 300 K and V_{ds} = 0.1 V.

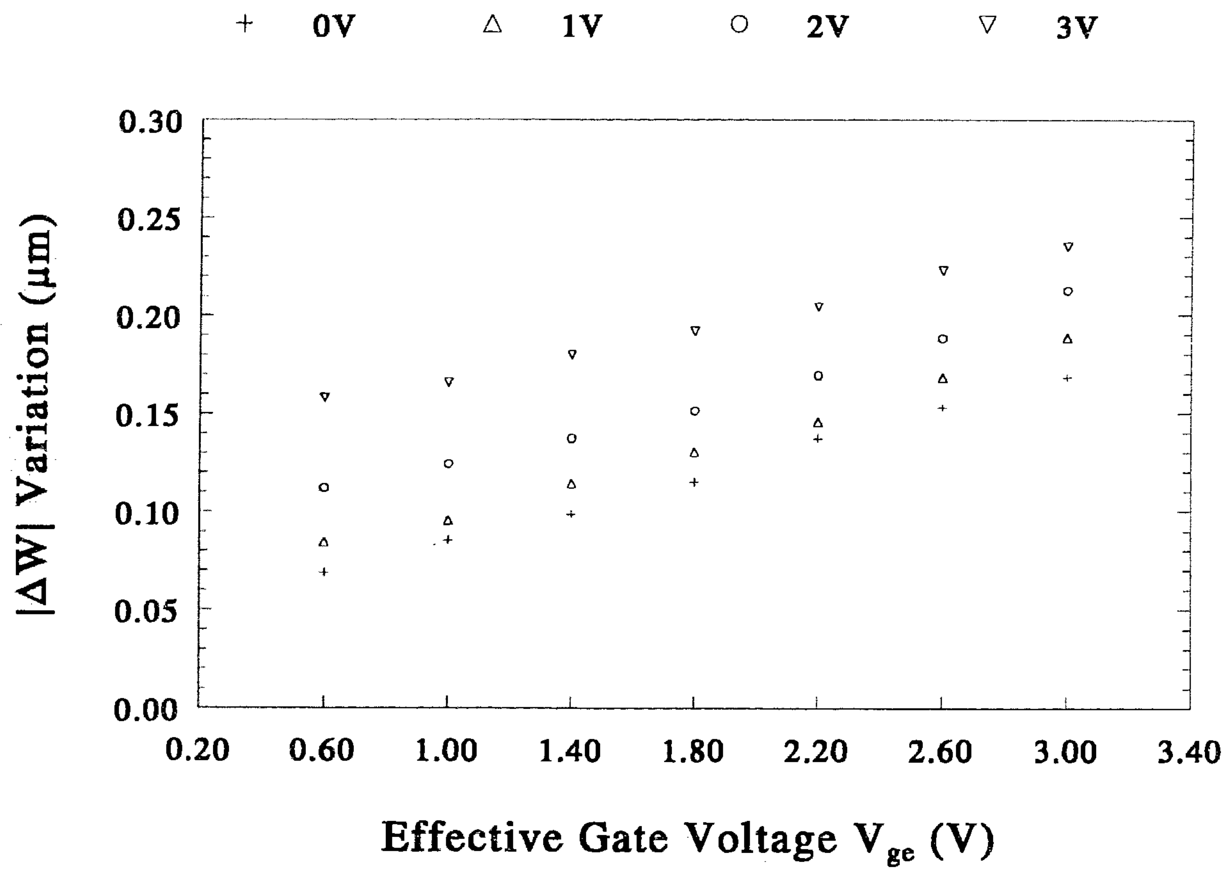


Figure 5.4.8. $|\Delta W|$ vs V_{ge} for different V_{sb} at T = 300 K and V_{ds} = 0.1 V.

At constant voltage biasing, parasitic parameters can also be affected by temperature variations. Before proceeeding further, it is appropriate to look at the effect of temperature on the depletion width since R_p and ΔL are dependent on the depletion width. In eqn (2.3.5), both doping concentration N_A and ψ_s terms are function of temperature, and hence depletion width w_D can be changed by temperature variations. Fig 5.2.15 shows that w_D decreases as temperature increases, and this implies that R_p should decrease. But, this is not the case as shown in Fig 5.4.10 because it shows R_p increases with temperature. Theoretically, the resistivity of silicon is a function of temperature and it increases with temperature. An increase in the resistivity of silicon ρ_{si} causes R_p to increase at higher temperature. Consequently, R_p increases from 75 Ω at T = 200 K to 82 Ω at T = 400 K for V_{ds} = 0.1 V, and ΔL increases from 0.07 μm to 0.11 μm at the same temperature range. It shows that ρ_{si} plays a more dominant role than w_D in the determination of R_p with temperature. At a constant temperature, R_p increases with V_{ds}.

Fig 5.4.11 shows ΔL increases with temperature for different V_{ds}. Eventhough the depletion width w_D decreases, ΔL increases with temperature. For short-channel devices, the horizontal depletion-layer widths, y_D and y_S, at the drain and source side are smaller than the vertical depletion-layer width w_D. Due to charge sharing model, the transverse field strongly influences the potential distribution at the silicon surface. The expression for y_D as a function of temperature at V_{sb} = 0 can be written as [31]

$$y_D = \sqrt{\frac{2\epsilon_s(V_{bi} - \psi_s + V_{ds})}{qN_A}} \tag{5.4.1}$$

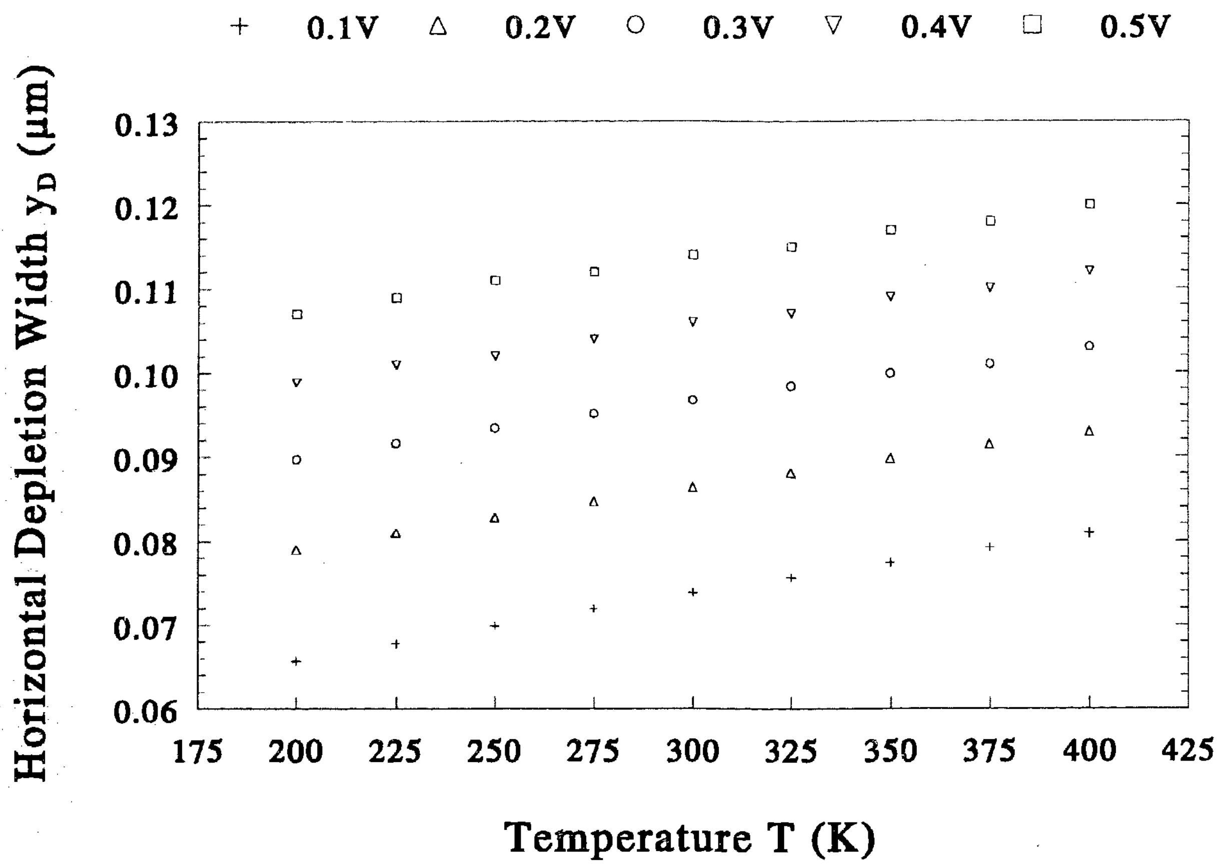


Figure 5.4.9. y_D vs T for different V_{ds} at V_{sb} = 0 V.

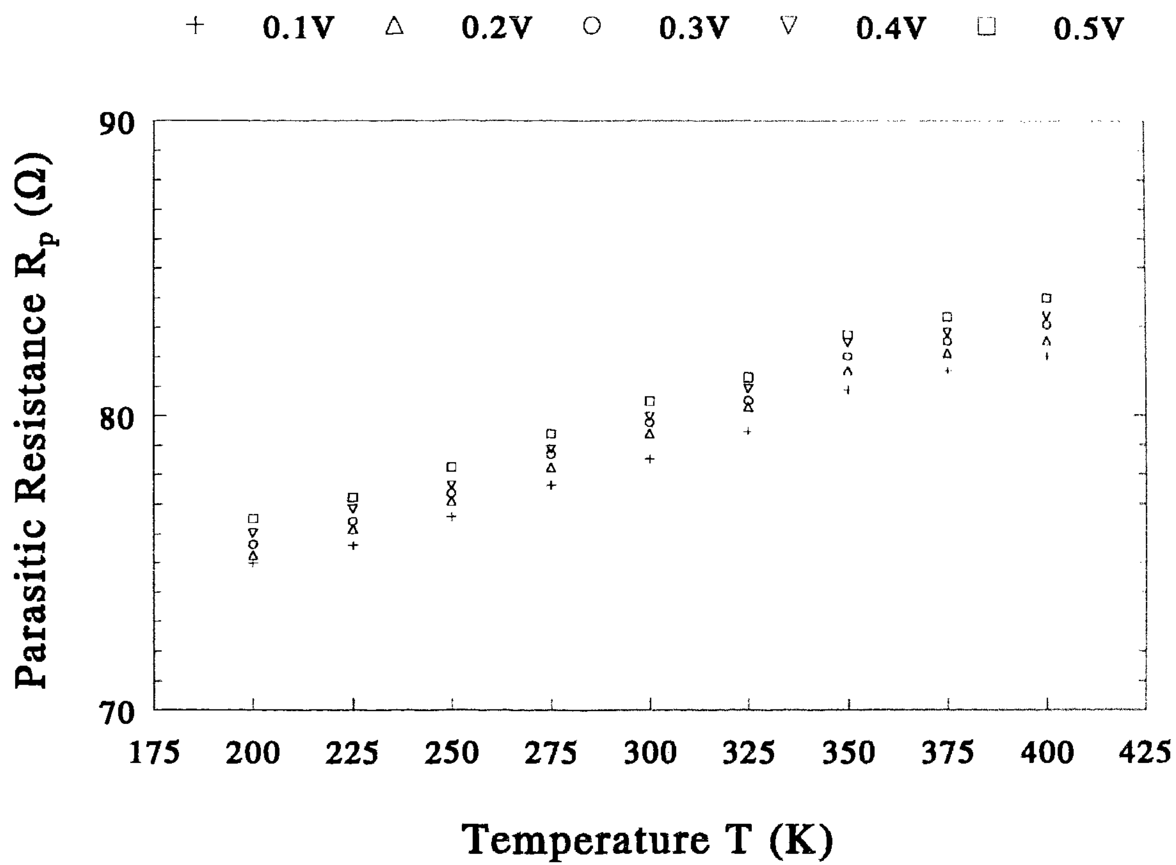


Figure 5.4.10. R_p vs T for different V_{ds} at V_{sb} = 0 V.

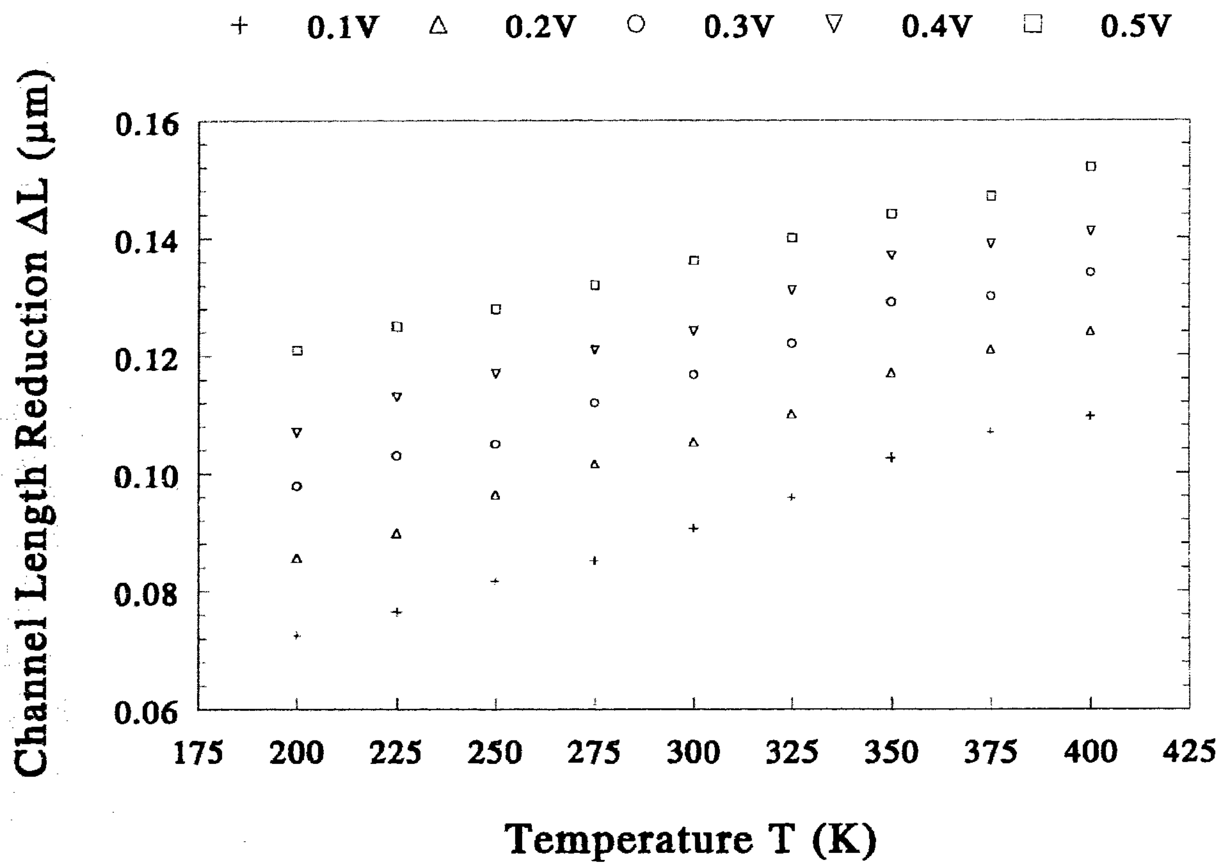


Figure 5.4.11. ΔL vs T for different V_{ds} at $V_{sb} = 0$ V.

where V_{bi} is the built-in potential of a p-n junction. Fig 5.4.9 shows y_D increases with temperature. In the ohmic region of device operation, the reduction ΔL reduces the effective channel length similar to the depletion y_D and hence, ΔL also increases with temperature.

For varying width devices, $|G_p|$ and $|\Delta W|$ are shown in Figs 5.4.12 and 5.4.13, respectively as function of temperature variation for different V_{ds}. $|G_p|$ decreases with increasing temperature while $|\Delta W|$ increases with temperature. As discussed earlier, the resistivity of silicon ρ_{si} increases with temperature. Since conductance is the reciprocal of resistance, $|G_p|$ decreases with temperature. At a fixed temperature, the effect of V_{ds} on both parasitics is similar to those in Figs 5.4.3 and 5.4.4.

The effect of temperature on R_p, ΔL, $|G_p|$ and $|\Delta W|$ for different V_{sb} are shown in Figs 5.4.14 to 5.4.17, respectively. The variations of all parasitic parameters with respect to temperature are similar to changing V_{ds}. At a constant V_{sb} and increasing temperature, R_p increases and $|G_p|$ decreases due to an increase in temperature-dependent resistivity of silicon and the depletion y_D causes ΔL and $|\Delta W|$ to increase. The depletion width around the drain region increases with V_{sb}, and hence causes all parameters to increase with V_{sb} at a constant temperature.

The effects of voltage biasing and temperature variation on R_p, ΔL, $|G_p|$ and $|\Delta W|$ discussed in this section are summarized in Table 5.4.1.

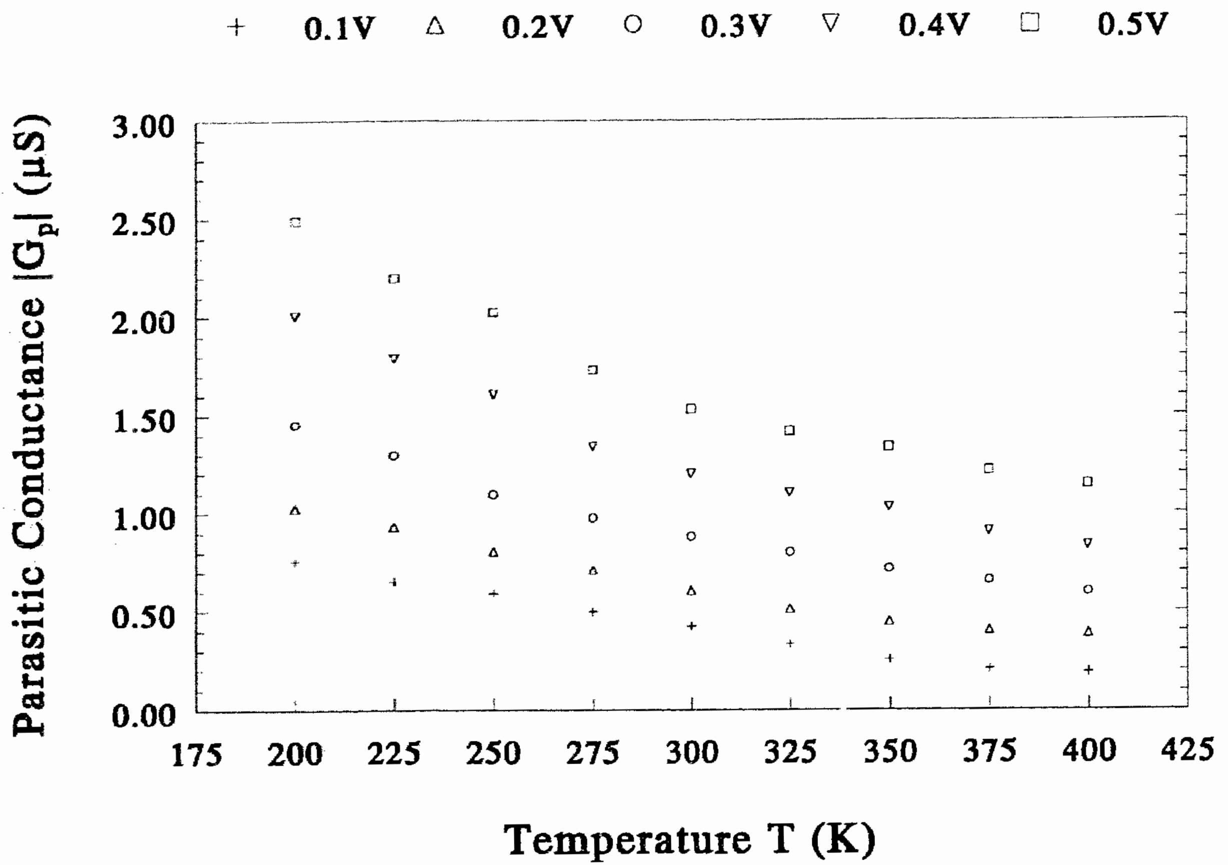


Figure 5.4.12. $|G_p|$ vs T for different V_{ds} at V_{sb} = 0 V.

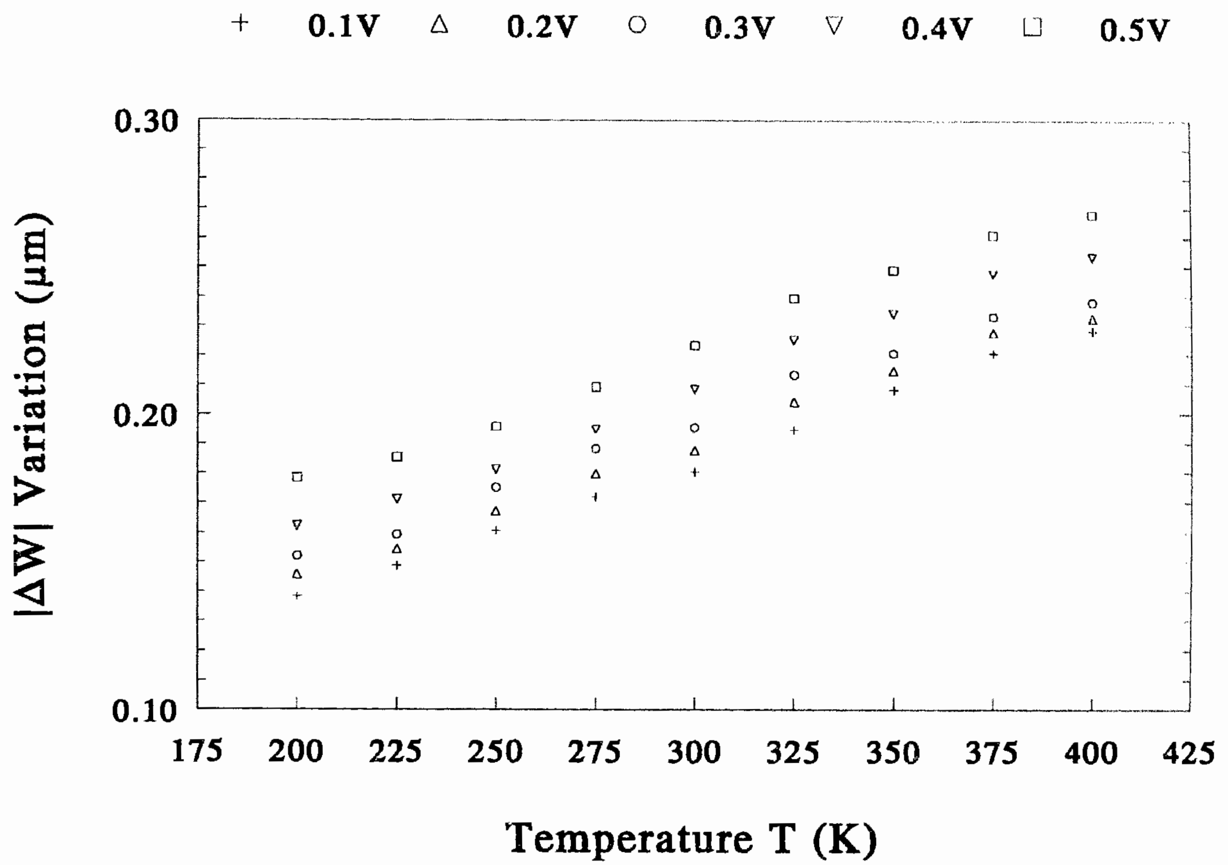


Figure 5.4.13. $|\Delta W|$ vs T for different V_{ds} at V_{sb} = 0 V.

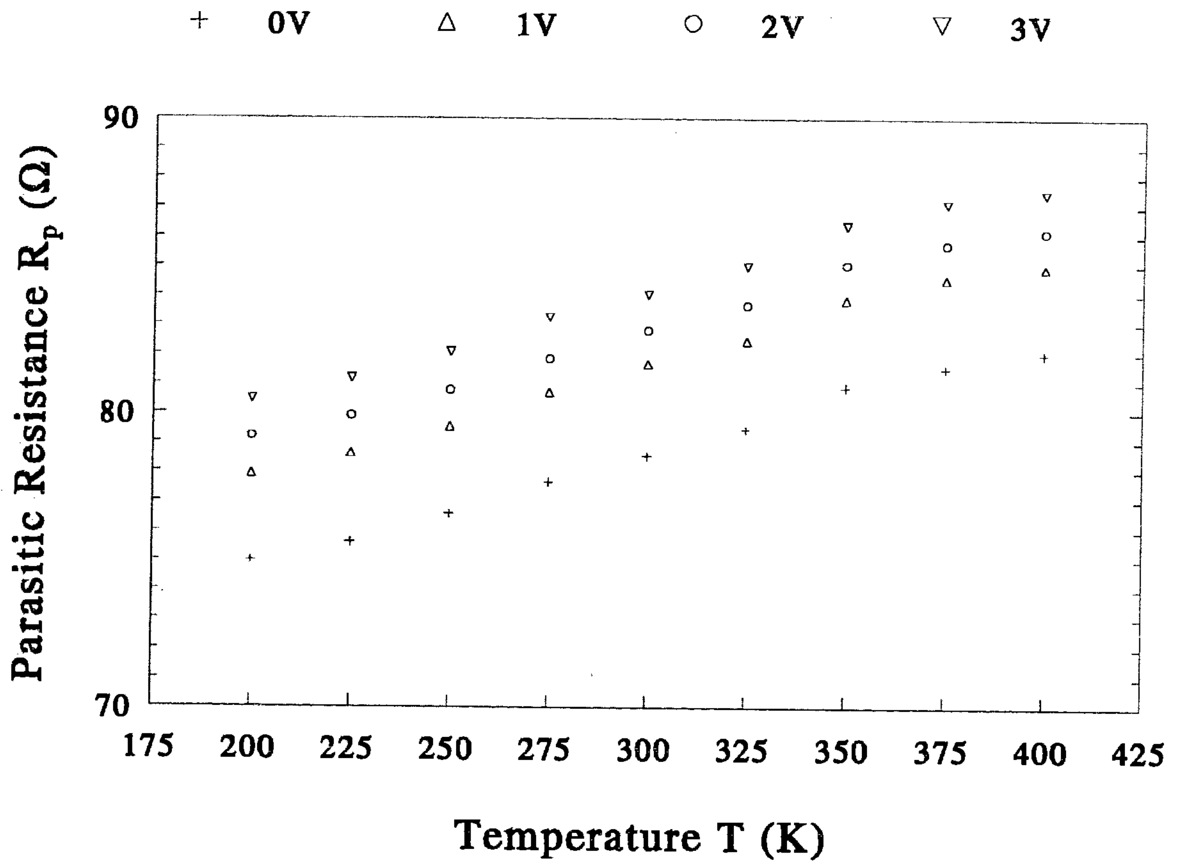


Figure 5.4.14. R_p vs T for different V_{sb} at V_{ds} = 0.1 V.

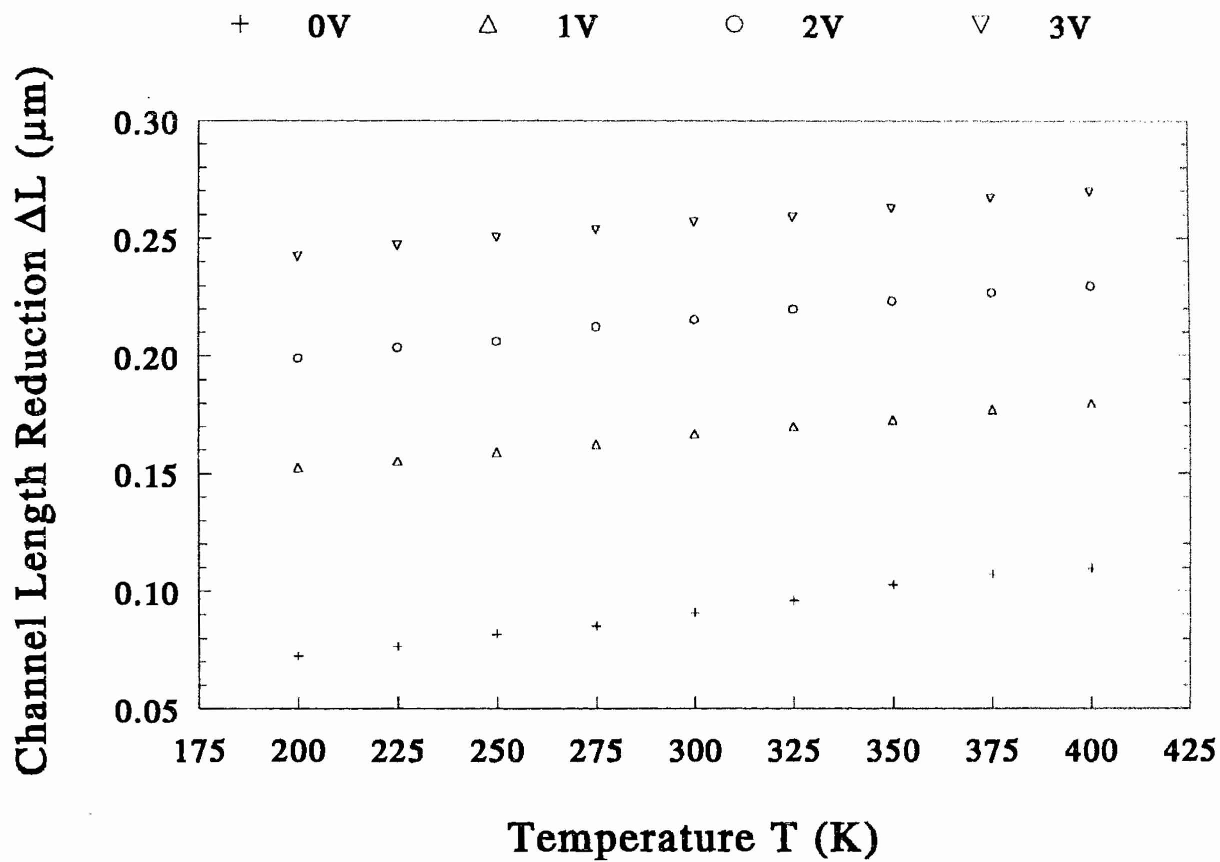


Figure 5.4.15. ΔL vs T for different V_{sb} at V_{ds} = 0.1 V.

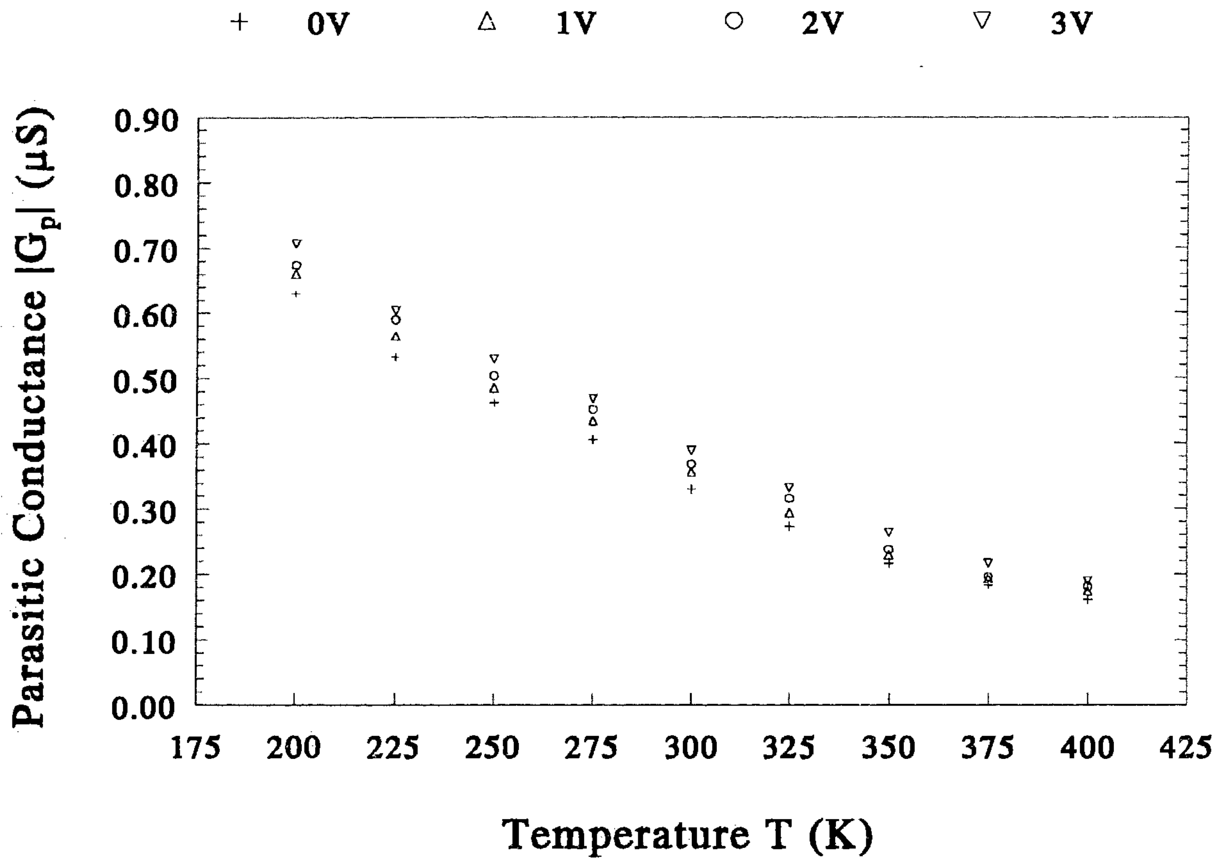


Figure 5.4.16. $|G_p|$ vs T for different V_{sb} at V_{ds} = 0.1 V.

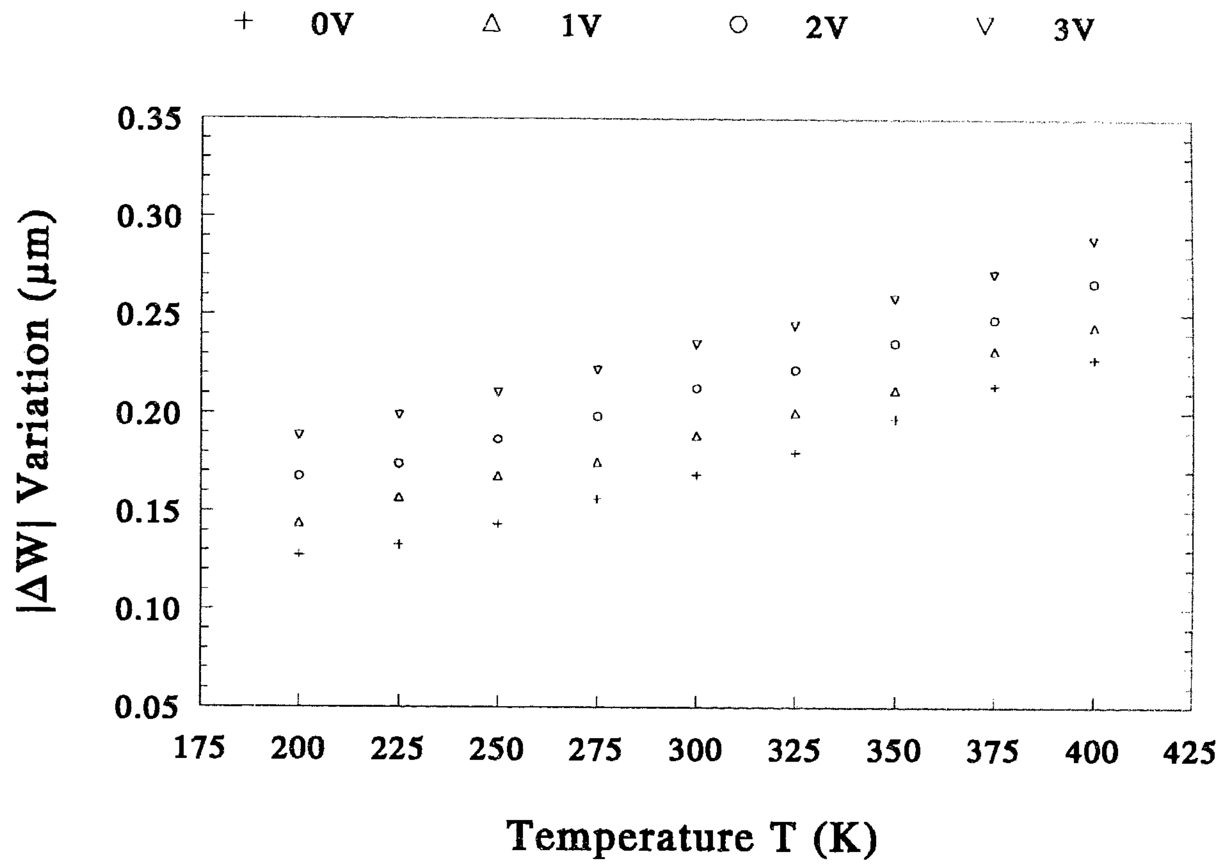


Figure 5.4.17. $|\Delta W|$ vs T for different V_{sb} at V_{ds} = 0.1 V.

Table 5.4.1. The effects of voltage biasing and temperature variation on the parasitic parameters. Note that the uparrow (↑) denotes an increase in value with respect to biasing and downarrow (↓) shows a decrease.

	R_p	ΔL	$\|G_p\|$	$\|\Delta W\|$
V_{gs} increase	↓	↓	↑	↑
V_{ds} increase	↑	↑	↑	↑
V_{sb} increase	↑	↑	↑	↑
T increase	↑	↑	↓	↑

5.5 MODELLING OF PHYSICAL PARAMETERS

The previous three sections present the results of all physical parameters which are important in the study of small geometry devices. The data were extracted from measured I_{ds}-V_{gs} data using the respective short-channel and narrow-width devices. Some of the extracted parameters used the parameter extraction scheme while the others were based on the equations which were described in Chapter 2. From the figures in Section 5.2 to 5.4, it is possible to show the modelling of individual physical parameters as a function of temperature, channel dimensions and voltage biasing. The simulation of I_{ds}-V_{gs} curve in the following section uses some of these equations. Table 5.5.1 shows some of the physical parameters as a function of temperature at V_{ds} = 0.1 V and V_{sb} = 0 V. Unless it is specified, the equations of the parameters are derived from data using either all varying channel-length or channel-width devices.

It has been shown in Chapter 2 that some physical parameters such as threshold voltage and subthreshold slope vary according to their channel dimensions. Table 5.5.2 shows the relationship of these parameters with their respective channel length and channel width at room temperature.

Table 5.5.1. Some of the physical parameters as a function of temperature. Note that the letter *l* in bracket denotes the equation is derived from a short-channel device with L = 1.2 μm and W = 20 μm while the letter *w* denotes the equation is derived from a narrow-width device with L = 10 μm and W = 2 μm.

Physical parameters	Function of temperature T
V_T (*l*)	$1.0379 - 1.14 * 10^{-3}T$
V_T (*w*)	$1.2213 - 8.26 * 10^{-4}T$
α_1	$0.8192 - 2.09 * 10^{-3}T + 8.07 * 10^{-6}T^2$
α_3	$0.0748 + 9.39 * 10^{-4}T + 4.29 * 10^{-6}T^2$
S (*l*)	$7.14 + 0.3433T$
S (*w*)	$28.08 + 0.186T$
μ_o (*l*)	$2.7015 * 10^6 T^{-1.5279}$
μ_o (*w*)	$2.1515 * 10^6 T^{-1.5019}$
θ_0 (*l*)	$0.5901 - 2.23 * 10^{-3}T + 2.42 * 10^{-6}T^2$
θ_0 (*w*)	$0.3574 - 1.43 * 10^{-3}T + 1.69 * 10^{-6}T^2$
θ_B (*l*)	$0.0228 + 5.9 * 10^{-5}T - 2.07 * 10^{-7}T^2$
θ_B (*w*)	$0.4509 + 1.98 * 10^{-3}T - 2.35 * 10^{-6}T^2$
R_p	$66.5249 + 4.31 * 10^{-2}T - 9.45 * 10^{-6}T^2$
ΔL	$0.0358 + 1.75 * 10^{-4}T + 3.27 * 10^{-8}T^2$
$\lvert G_p \rvert$	$1.7961 - 6.27 * 10^{-3}T + 5.51 * 10^{-6}T^2$
$\lvert \Delta W \rvert$	$0.0543 + 3.97 * 10^{-4}T + 1.08 * 10^{-7}T^2$

Table 5.5.2. Some of the physical parameters as a function of channel dimensions. The letter in bracket has the same meaning as in Table 5.5.1.

Physical parameters	Function of channel dimensions
V_T (*l*)	$0.7997 - \frac{0.1110}{L}$
V_T (*w*)	$0.9167 + \frac{0.1089}{W}$
S (*l*)	$86.5 + \frac{7.86}{L^2}$
S (*w*)	$81.5 + \frac{6.15}{W^2}$

The results in Section 5.4 show that the parasitic parameters can be altered by changing the biasing conditions at their terminals. Based on the results in Figs 5.4.1 to 5.4.17, it is possible to model the parasitic parameters in terms of biasing conditions and use these equations in the simulation of I_{ds}-V_{gs} curve. They can also be applied to modelling of smaller dimensions eventhough the results were extracted from devices of different channel dimensions. The following section will provide more details on modelling of I_{ds}-V_{gs}. Table 5.5.3 shows the equations of parasitic parameters with respect to voltage biasing at room temperature.

Table 5.5.3. Parasitic parameters R_p, ΔL, $|G_p|$ and $|\Delta W|$ as a function of gate, drain and substrate voltage biasing.

Physical parameters	**Function of voltage biasing**
R_p	$(146.81 + 8.2662V_{ds} + 3.1810V_{sb}) - (34.52 + 2.7454V_{ds} + 0.2214V_{sb})V_{gs} + (4.25 + 0.4463V_{ds} - 0.0503V_{sb})V_{gs}^2$
ΔL	$(0.2278 + 0.0869V_{ds} + 0.0556V_{sb}) - ((54.78 - 0.1911V_{ds} - 1.8606V_{sb})10^{-3})V_{gs} + ((34.29 - 0.2401V_{ds} - 5.8731V_{sb})10^{-4})V_{gs}^2$
$\lvert G_p \rvert$	$-((-7.7978 + 19.66V_{ds} - 0.1991V_{sb})10^{-3}) + ((-0.8354 + 3.9606V_{ds} + 0.4788V_{sb})10^{-2})V_{gs} + ((18.23 + 9.6576V_{ds} + 0.6030V_{sb})10^{-3})V_{gs}^2$
$\lvert \Delta W \rvert$	$((4.1289 + 0.0259V_{ds} + 3.4026V_{sb})10^{-2}) + ((40.56 + 3.1884V_{ds} - 7.6893V_{sb})10^{-3})V_{gs} - ((40.52 + 25.38V_{ds} - 91.73V_{sb})10^{-5})V_{gs}^2$

5.6 SIMULATION OF I-V CURVE

The important results and equations presented above will be utilized in this section. This section shows the modelling of I_{ds}-V_{gs} curves of a wide, short-channel device and a long, narrow-width device. The first part of this section shows the simulation of short-channel device and narrow-channel device and their results while the second part described the parameter extraction scheme can be apply to smaller dimensions. Some model equations of physical parameters from Section 5.5 were included in the simulation. In this research, the most crucial equations included in the simulation are the equations for R_p and ΔL of short-channel device and $|G_p|$ and $|\Delta W|$ of narrow-width device. They are used to model the behaviour of parasitics under different biasing conditions.

It will be shown that accurate analytical expressions of both R_p and ΔL are necessary for modelling I_{ds}-V_{gs} characteristics of short-channel LDD devices. As the channel length decreases, the parasitic resistance becomes increasingly important because the value of R_p is quite significant with respect to the intrinsic channel resistance. Fig 5.6.1 shows the comparison of three I_{ds}-V_{gs} data curves at room temperature, V_{ds} = 0.1 V, V_{sb} = 0 V and L_m = 1.2 μm. The solid line is the measured data of a short-channel device with L = 1.2 μm using the equipment setup described in Chapter 3. Analytic (V) shows the calculated I_{ds}-V_{gs} data using the model equations illustrated in Table 5.5.3 in which R_p and ΔL are functions of V_{gs}. Analytic (F) shows the calculated I_{ds}-V_{gs} data using fixed values to represent the parasitic parameters at V_{gs} = 7 V. From this figure, it shows that Analytic (V) fits better with the measured data than Analytic (F).

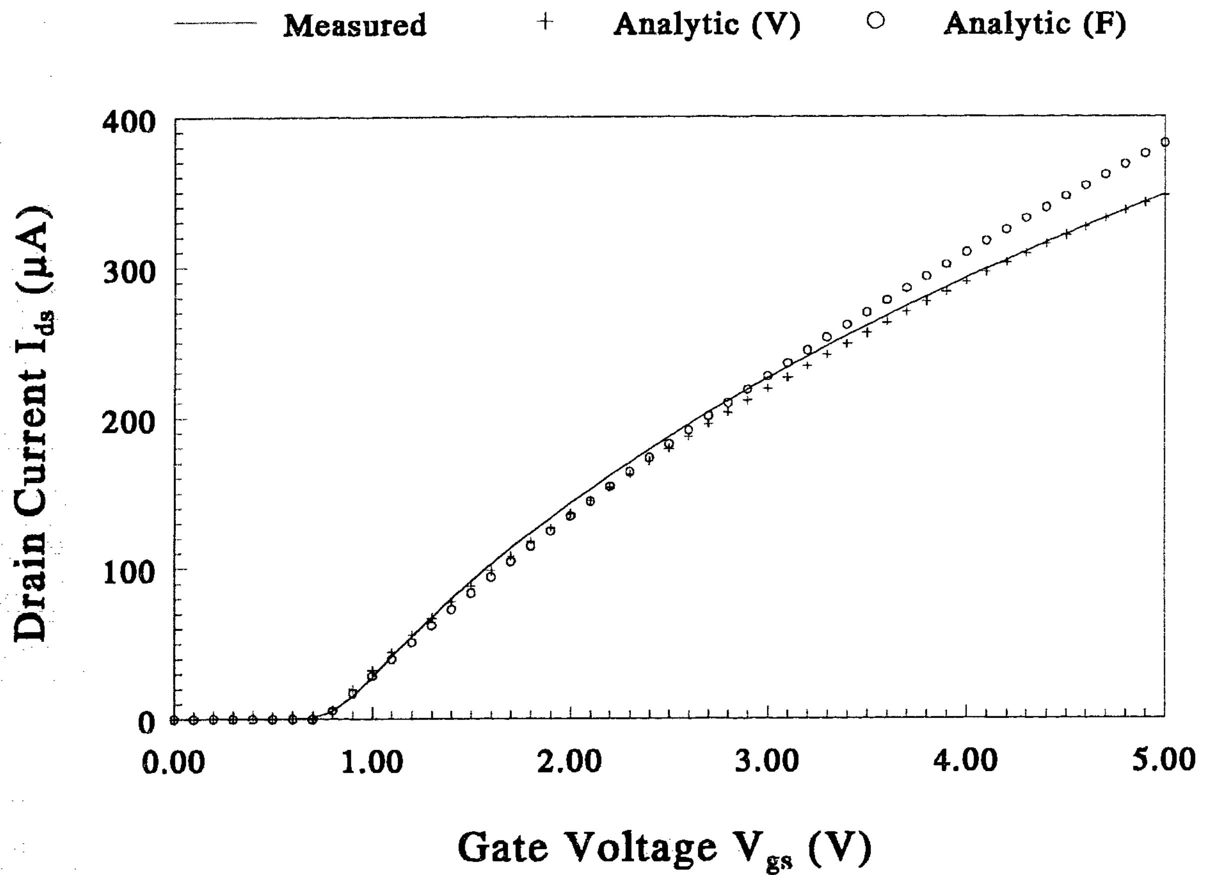


Figure 5.6.1. The comparison of I_{ds}-V_{gs} curves at V_{ds} = 0.1 V, V_{sb} = 0 V, T = 300 K and L_m = 1.2 μm. The solid line is the measured data of a short-channel device with L = 1.2 μm. Analytic (V) shows the calculated I_{ds}-V_{gs} data using the model equations. Analytic (F) shows the calculated I_{ds}-V_{gs} data using fixed values to repersent the parasitic parameters.

The average fitting error between the measured data and the calculated values can be found from the following expression [63]

$$Error = \frac{\sum_{i=1}^{n} \frac{|I_i^m - I_i^c|}{I_i^m}}{n} \tag{5.6.1}$$

where I^m_i is the *i*th measured data, I^c_i is the *i*th calculated data and N is the number of data points. The fitting error for Analytic (V) is less than 1 % while Analytic (F) has a fitting error of about 6 %. The values for R_p and ΔL in Analytic (F) were obtained at high V_{gs} biasing (V_{gs} = 7 V) to alleviate the geometrical effect in V_T determination. However, due to device down-scaling into submicron range, the maximum gate-to-source voltage supported will be reduced. Typically, the range of V_{gs} for most electronics application is between 0 and 5 V. Thus, previous methods that suggest high V_{gs} biasing will be avoided due to device reliability problem. To further illustrate the importance of parasitic parameters in modelling I_{ds}-V_{gs}, Fig 5.6.2 shows the SPICE simulation (SPICE (V)) of I_{ds}-V_{gs} data using piecewise values of parasitics R_p and ΔL from Figs 5.4.1 and 5.4.2, respectively fits better on the measured data than SPICE (F) using fixed parasitics.

For the simulation of narrow-width devices, the model equations for physical parameters G_p and $|\Delta W|$ will be used. It can be concluded, from Section 5.4, that the shape of the channel edge changes with biasing conditions. As the channel width shrinks, the edges on both sides of the channel becomes increasingly important because the device conductance is directly proportional to the channel width and a small change in these edges will significantly change their drive capability. By using the values of the extracted parameters and the equations of the parasitics, it is possible to show the modelling of

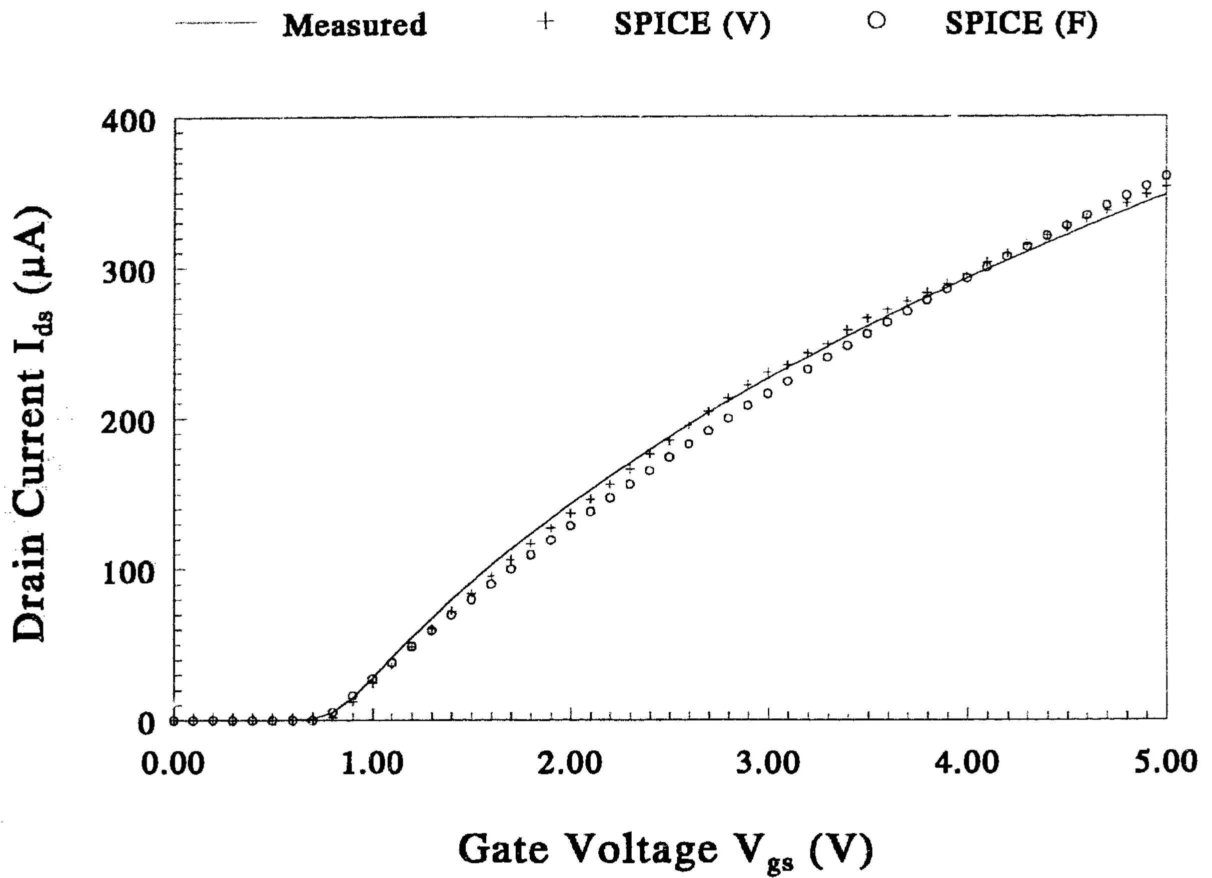


Figure 5.6.2. The comparison of experimental I_{ds}-V_{gs} data and SPICE simulation at V_{ds} = 0.1 V, V_{sb} = 0 V, T = 300 K and L_m = 1.2 μm.

I_{ds}-V_{gs} curve of a narrow-width device. Again, Fig 5.6.3 shows the comparison of I_{ds}-V_{gs} curves between the measured and the calculated data at room temperature, V_{ds} = 0.1 V, V_{sb} = 0 V and W_m = 2 μm. The calculated I_{ds}-V_{gs} data using analytical equations (Analytic (V)) of varying parasitics fits better on the measured data than the one using fixed parasitics (Analytic (F)). The fitting error for Curve 2 is less than 3 % while Curve 3 has a fitting error greater than 6 %. The values for $|G_p|$ and $|\Delta W|$ in Curve 3 were obtained at high V_{gs} biasing to avoid the geometrical effect in V_T determination. To further illustrate the importance of parasitic parameters in narrow-width device, Fig 5.6.4 shows the SPICE simulation (SPICE (V)) of I_{ds}-V_{gs} using piecewise values of $|G_p|$ and $|\Delta W|$ from Figs 5.4.3 and 5.4.4, respectively fits better than SPICE (F).

Since the devices are fabricated using the 1.2 μm process technology, the smallest device would have a channel length of 1.2 μm. One of the main objectives in this research is to show that this technique, which used in the 1.2 μm process devices, is also good for devices with smaller dimensions. In this study, the 1.2 μm process technology is provided only as a test vehicle for the parameter extraction scheme described in Chapter 4. The technique can also be applied to a set of varying channel length or width devices of different fabrication process because it does not take into account the process parameters during parameter extraction. In order to extract physical parameters, it requires a set of measured I_{ds}-V_{gs} data at different drain or substrate biasing for different channel length or width devices. Overall, the technique is fast, simple and easy to use. Before using the technique, one has to make sure that Eqn (4.1.5) will be satisfied for a set of varying length devices and Eqn (4.2.6) for varying width devices.

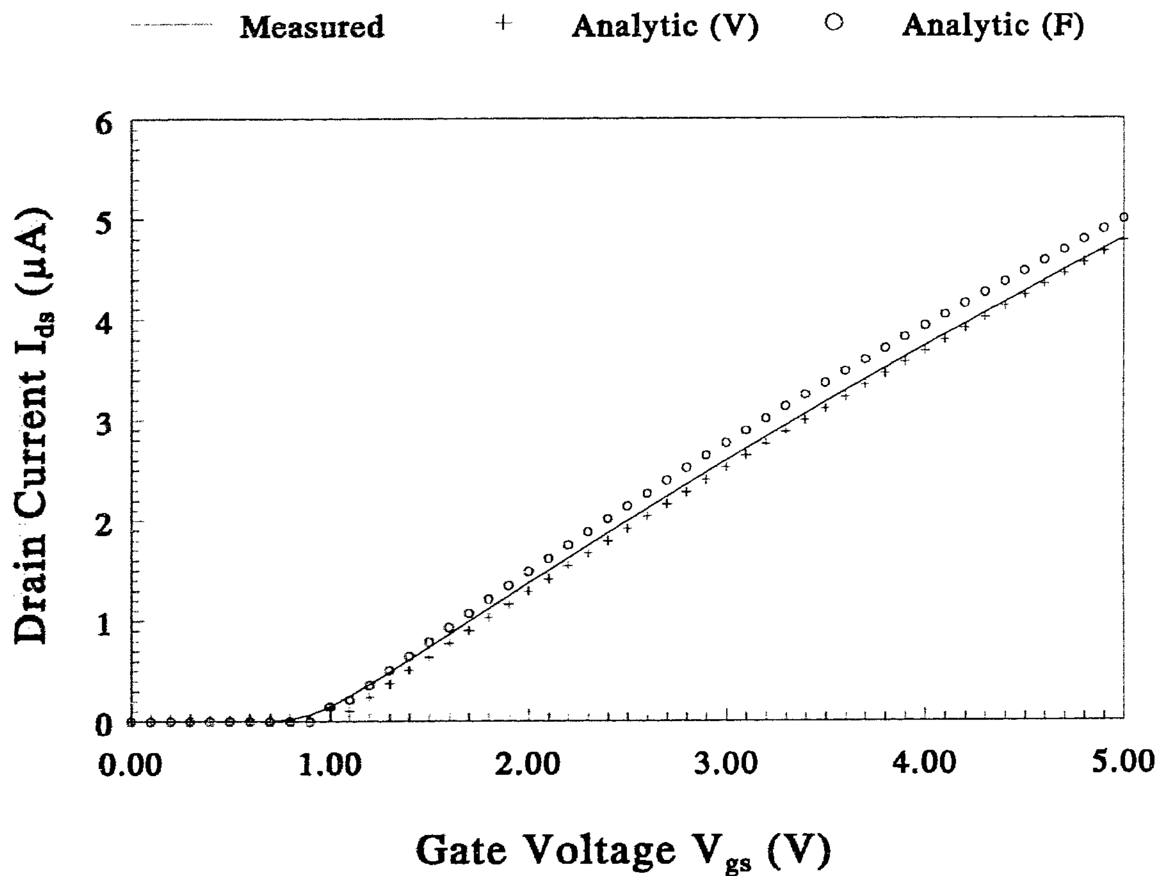


Figure 5.6.3. The comparison of I_{ds}-V_{gs} curves at V_{ds} = 0.1 V, V_{sb} = 0 V, T = 300 K and W_m = 2 μm. The solid line is the measured data of a short-channel device with L = 1.2 μm. Analytic (V) shows the calculated I_{ds}-V_{gs} data using analytical equations. Analytic (F) shows the calculated I_{ds}-V_{gs} data using fixed values to repersent the parasitic parameters.

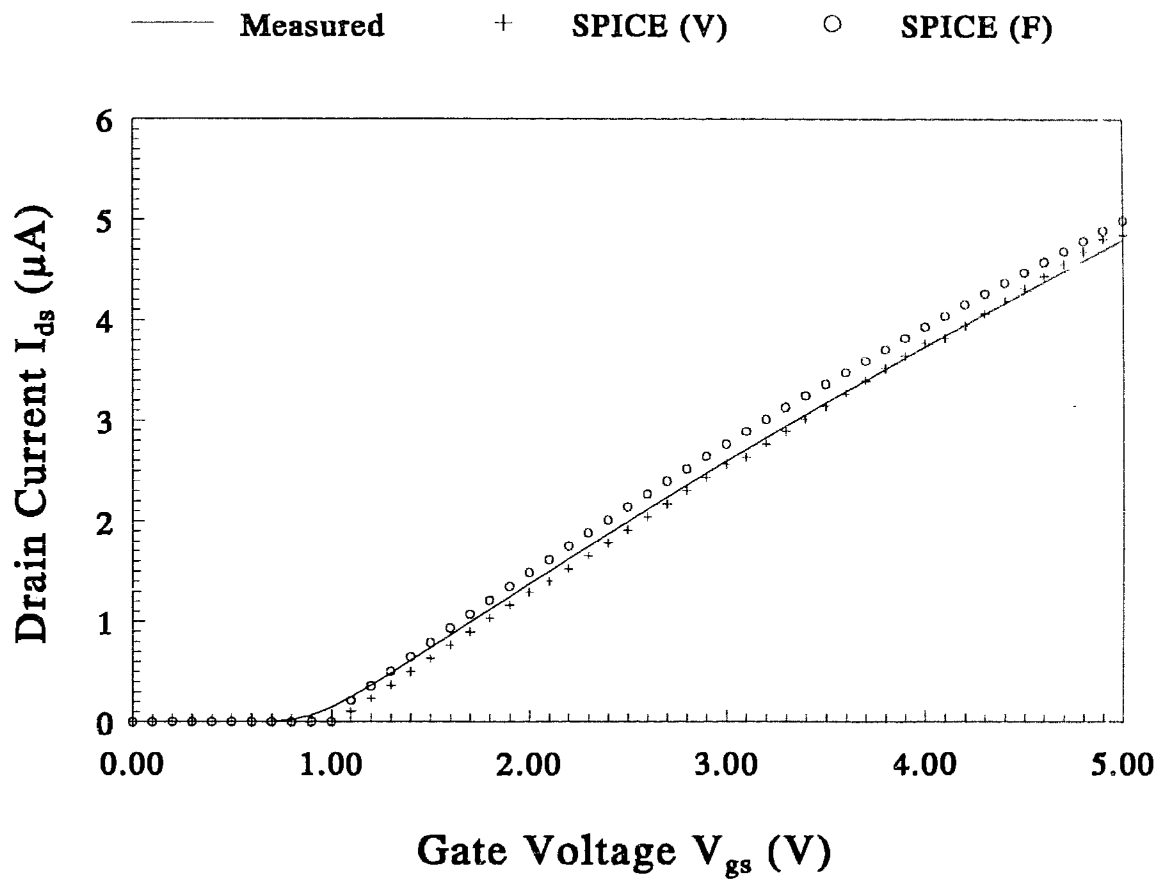


Figure 5.6.4. The comparison of experimental I_{ds}-V_{gs} data and SPICE simulation at V_{ds} = 0.1 V, V_{sb} = 0 V, T = 300 K and W_m = 2 μm.

Chapter 6 CONCLUSION

In this chapter, a summary of the results and a conclusion on the work completed will be given. The outcome of this research is important to device and circuit designers because they can provide an insight into how parasitic parameters and other parameters in the down-scaling of devices affect their drive capability in a circuit. Moreover, it can be used to approximately pre-determine the drain current of small geometry devices before actually making them.

The parameter extraction scheme described in Chapter 4 is also good for devices with smaller dimensions and for a set of devices with different fabrication processes. The equations presented in Chapter 5 can also be applied to future submicron devices without significant changes. The importance of parasitic parameters in device modelling is shown in Section 5.6 because a small percentage change of these parasitics can lead to a larger changes in the predictions of their terminal current-voltage characteristics. In this research, the dc characteristics below saturation of small-geometry LDD devices were studied in detail that include the effects of short-channel, narrow-width and temperature variations. The rest of this section gives a summary of the results presented in Chapter 5.

The study of short-channel effects include parameters such as V_T, S, μ_o, R_p and ΔL. Overall, short-channel effect is less significant at lower temperatures. This implies that devices can be made shorter without suffering much short-channel effects if they are operating at low temperature. However, the hot carrier effect and carrier freeze-out are stronger at lower temperatures. Because of reduced carrier scattering at lower

temperatures, the transconductance g_m and low field carrier mobility μ_o will be higher. V_T decreases with increasing temperature for all devices; short-channel effect is more pronounced when channel length is less than 2 μm. Subthreshold slope S is also affected by short-channel modulation at this channel length.

It has shown that both R_p and ΔL can be affected by either changing the biasing condition at one of the terminals or varying the operating temperature of the devices. It was found that, at a fixed temperature, R_p and ΔL decrease with increasing V_{ge}, increase with increasing V_{ds} and V_{sb}. At lower temperatures, the effective channel lengths of NMOS devices are longer than that at higher temperatures. It is due to the decrease in horizontal depletion widths at lower temperatures. R_p also increases with temperature due to an increase in ρ_{si}.

Narrow-width effect can be shown in V_T, S, μ_o, $|G_p|$ and $|\Delta W|$. V_T decreases with increasing temperature for all devices and the narrow-width effect occurs at channel width less than 3 μm. Since the channel length is long, the hot-carrier effect is not as severe as for short-channel devices. The transconductance g_m and mobility μ_o are higher at lower temperatures but they are lower than that for varying channel length devices. Similar to R_p and ΔL, $|G_p|$ and $|\Delta W|$ can also be varied by operating conditions of the device. The values of $|G_p|$ and $|\Delta W|$ increase with V_{ge}, V_{ds} and V_{sb}. For the effect of temperature, $|G_p|$ and effective channel width decrease with increasing temperature because the edges of the channel $|\Delta W|$ increases with temperature.

6.1 RECOMMENDATIONS

Since the results of this research is based upon in the linear region of device operation, a number of new areas can be explored and will be recommended here :-

1. the study of the saturation characteristics of these devices;
2. propose models for some important parameters in the saturation region; and
3. do stress-degradation test on these devices.

All of these recommendations can be continued at different biasing and temperature conditions.

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APPENDIX

This section lists the threshold voltages of the devices used in the linear regression.

```
vta = [7.0005e-01 6.8127e-01 6.7489e-01 6.7044e-01 6.6682e-01];
.....
vtg = [8.0292e-01 7.8732e-01 7.8604e-01 7.8584e-01 7.8562e-01];
```

This section obtains the measured resistance at different effective gate biasing.

```
for w = 1:5;
for i = 1:9;
for j = 1:100;
vga(i,w) = (i*0.4)+vta(w)+(w*0.05);
if (vga(i,w) >= a(j,1)) & (vga(i,w) <= a(j+1,1));
A(i,w) = (a(j+1,w+1)-a(j,w+1))*((vga(i,w)-a(j,1))...
/(a(j+1,1)-a(j,1)))+a(j,w+1);
aa(i,w) = (0.1*w)/A(i,w);
else
end
.....
vgg(i,w) = (i*0.4)+vtg(w)+(w*0.05);
if (vgg(i,w) >= g(j,1)) & (vgg(i,w) <= g(j+1,1));
G(i,w) = (g(j+1,w+1)-g(j,w+1))*((vgg(i,w)-g(j,1))...
/(g(j+1,1)-g(j,1)))+g(j,w+1);
gg(i,w) = (0.1*w)/G(i,w);
else
end
end
end
end
```

This section extracts the parasitic parameters from the respective slopes and intercepts.

```
for k = 1:8;
ma(k,w) = (gg(k,w)-aa(k,w))/8.6e-6;
```

```
mb(k+1,w) = (gg(k+1,w)-aa(k+1,w))/8.6e-6;
ca(k,w) = aa(k,w)-(ma(k,w)*1.2e-6);
cb(k+1,w) = gg(k+1,w)-(mb(k+1,w)*9.8e-6);
x(k,w) = (cb(k+1,w)-ca(k,w))/(ma(k,w)-mb(k+1,w));
y(k,w) = (mb(k+1,w)*x(k,w))+cb(k+1,w);
dlrp = [x y];
end
end
```