Current-Mode Signal Processing for Integrated Transducer Systems

by
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"Current-Mode Signal Processing for Integrated Transducer Systems"

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Abstract

The union of signal processing circuitry and transducers -- sensors, emitters and actuators -- forming integrated transducer systems may provide many benefits. These advantages include increased accuracy, dynamic range, noise immunity, reliability and ease of use in ways not otherwise attainable with discrete systems.

This thesis investigates some of the analog signal processing circuits that have applications in the development of integrated transducer systems. Specifically, small low-powered A/D converters using both algorithmic and time-domain conversion methods are presented. In order to achieve the size, power and dynamic range restrictions with a digital IC process, current-mode circuit techniques were employed.

One example of integrated transducer systems, known as the visual-to-thermal converter cell, was also implemented and evaluated. A single visual-to-thermal converter cell combines a photodetector and a thermal pixel along with a local algorithmic A/D converter operating in the current-domain. Arrays of these cells would convert a visual scene to a thermal scene with the same resolution.

Another integrated transducer system is proposed. This system integrates a MAGFET transducer with signal processing developed in this thesis. The design would provide a single digital signal with a duty cycle related to the incident magnetic flux. Due to the minimal size, power and interconnect requirements, the design has applications in systems requiring arrays of MAGFETs.

Acknowledgements

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1 Introduction

The most promising high-volume emerging markets for microelectronics in the coming decades include industrial process control, environmental monitoring and control, advanced automotive systems and health care [1]. Some of the required transducers for each of these markets do not exist or lack the precision, speed or reliability demanded by the application. However, integrated transducers manufactured using standard IC technologies may provide a solution to some of these problems.

Silicon as a transducer material is very promising, because it permits the integration of the sensing element and the signal-processing circuitry on one chip forming the so-called integrated or "smart transducer" [2]. An important characteristic of such integrated transducers is that their behavioral complexities may be dealt with internally and not impose themselves on the user. Another advantage is that the integrated transducer can perform the analog processing necessary to provide a digital interface. Such signal processing circuitry could extend the overall system accuracy, dynamic range, noise-immunity and reliability in ways not otherwise attainable.

1.1 Silicon Transducers

A number of thermal, mechanical, optical and chemical transducers can be realized by combining established integrated circuit technologies with a few additional processing steps specific to the transducer function and compatible with the integrated circuit process [3]. Digital CMOS IC technology is popular due to the availability and low cost of the IC process. These transducers can be loosely grouped into five signal domains: mechanical,

radiant, thermal, magnetic and chemical. Some typical examples are examined next.

An number of silicon or silicon dioxide mechanical structures can be constructed using silicon micromachining. These include suspended platforms and cantilevered beams which are useful for constructing miniature levers and accelerometers [4]. By diffusing piezoresistors or MOSFETs on different structures, a number of force and pressure sensors have been developed [5,6].

Silicon can be used to construct transducers for a wide spectrum of electromagnetic radiation, from gamma rays to infrared [2]. Photodiodes and phototransistors can be easily fabricated using digital IC technology without the need for post-processing [7]. Thermal emitting pixels are constructed using silicon micromachining to create a suspended platform with polysilicon resistors on top [3,8]. Low-cost solid state cameras based on charge-coupled devices (CCD) are now being introduced into the market [2].

Due to silicon's temperature dependency, a number of temperature measuring devices can be integrated on the chip. The devices may use two bipolar transistors with different emitter areas [9] or the subthreshold region of a MOSFET [10]. Another temperature sensing device can be obtained by integrating thermocouple-like structures [2] or ceramic capacitors on the substrate [11].

While silicon is non-magnetic, Hall plates and transistor structures sensitive to magnetic fields can be constructed [2]. With four-collector transistor structures, it is even possible to construct sensors capable of simultaneously measuring the magnitude and direction of the magnetic field. Other devices include magneto resistive elements and bipolar magnetotransistors [12].

Chemical transducers are required for biomedical, automotive and environmental applications. The ion-sensitive field-effect transistor (ISFET), manufactured using ion-selective gate insulators, is a well known device [2]. Other devices are constructed using thin-films of polymer or organic layers, sensitive to the desired chemical, applied to lateral capacitor finger electrodes [3,13] or interdigitated gate electrode field effect transistors (IGEFET) [14].

As shown by the preceding paragraphs, there is a large collection of useful silicon based transducers, many of which are already commercially available. The question that remains is which signal-conditioning and signal-processing circuits are appropriate for specific applications.

1.2 Transducer Interface Circuits

Signal formatting and conditioning is the most important task for the interface circuitry. Nearly all transducers generate or respond to analog signals. However, at present, most transducers will be used with digital systems such as microprocessors. Digital signals are much more noise immune than analog signals making their use desirable for long distance communication. This means some sort of A/D or D/A signal conversion must be performed as close to the transducer as possible.

As well, most transducers show some non-linearity, cross-sensitivity, offset and drift [2,10]. The interface circuitry could incorporate signal-processing concepts to correct some of the transducer's limitations using additional transducers, feedback control and/or look-up tables. For example, most silicon transducers show some cross-sensitivity to temperature [15]. Therefore, interface circuitry could use a temperature sensor integrated next to the transducer to null the effects of temperature change.

The final task of the interface circuitry could be performing special processing functions on the transducer's information. This may be as simple as low-pass filtering the transducer's output before signal conditioning and formatting. Other ideas include averaging the response of an array of transducers or perform some mathematical transformation on a number of different transducer signals. Some very interesting transducer concepts can be imagined depending on the desired application.

A number of integrated transducers devices have been developed such as pressure sensors [2,5,13], mass flowmeters [1,16], gas sensors [5,13,14], thermoelectric AC power sensors [3], humidity sensors [3,17], optical sensors [5,18], thermoelectric infrared sensor [3], strain gauges [19], thermal emitters [20], accelerometers [2], temperature sensors [9,10], radiation detectors [21] and biosensors [13]. While some of these systems have simple conditioning circuitry, others have attempted to implement intelligent chips that can be networked together [1,15,17,22]. Such a chip contains a few smart transducers with an intelligent controller that responds to computer requests for information over a databus. By networking of these chips together, a large number of transducers can be used over a wide area with minimal interconnect.

One approach to promote the use of integrated transducers is to develop standard transducer cells similar to the standard cell approach for digital circuitry [23]. The transducer cell would integrate one or more transducers with signal processing and control circuitry. A library of these cells would minimize the effort required by designers and aid in the promotion of transducers for new applications. The visual-to-thermal converter cell which emits thermal energy proportional to visible light intensity is a perfect example [24]. Arrays of these standard cells are attractive

as they can measure or generate a matrixes of energy such as mechanical, thermal or acoustic. For example, arrays of the visual-to-thermal converter cell would convert a visible image to a thermal image with the same resolution.

1.3 Current-Mode Signal Processing

By taking advantage of standard IC processes, these miniaturized transducers occupy less space and consume less power than traditional devices [23]. However, this advantage can put significant demands on the interface circuitry. For example, an integrated photodiode current output can vary over 6 decades of current ranging from 10pA to 10μA. As well, most capacitance based transducers, such as certain pressure or chemical sensors, have a nominal capacitance around 1pF. Therefore, the signal processing circuitry should be integrated beside the transducer to maintain the signal-to-noise ratio of these very small signals.

As well, applications using large number of transducers, such as arrays, put additional demands on the interface circuitry. With large numbers of these circuit blocks, low power consumption is require to minimize the chip dissipation. As well, the interface circuitry must be as small as possible in order not to compromise the packing density of the array. Finally, the desire to use relatively inexpensive digital CMOS IC processes, which are compatible with a number of transducers, may limit the accuracy and flexibility of analog circuit design.

Current-domain signal processing may be the answer to some of the design criteria of the transducer interface circuitry. Analog current-domain circuit design is compatible with digital CMOS IC technology [25,26] and, since a significant number of transducers are current controlled or generate current

signals, voltage-current converters are not required. Current-mode design can provide attractive and elegant solutions for many circuit and system problems.

In this thesis, we will examine current-domain signal processing techniques and their application to transducer signal processing. Two current-mode A/D converters are presented with their application to the visual-to-thermal converter cell. Alternative time-domain A/D conversion techniques using current-mode circuitry are also presented with a brief examination of their applications to transducer systems.

1.4 Organization of Thesis

Chapter 2 presents a general overview of digital CMOS compatible current-mode signal processing with guidelines for improving the performance of analog circuits. Chapter 3 describes current-mode A/D converters while Chapter 4 examines alternatives to A/D converters such as current-mode oscillators and sigma-delta modulators. Chapters 5 looks at two examples of integrated transducer systems. Chapter 6 provides some future research considerations and conclusions.

2 CMOS Current-Mode Techniques

Analog circuits will always be needed to perform a variety of critical tasks required to interface digital circuitry with the external world, such as amplification, prefiltering, demodulation, signal conditioning for line transmission, for storage, and for display. In addition, analog will retain its advantage over digital for at least the near future when very high frequency or very low power is required [26].

Analog design has historically been viewed as a voltage dominated form of signal processing. This has been apparent in analog integrated circuit design where current signals are generally transferred into the voltage domain before any analog signal processing takes place [25]. This approach does not make any sense especially when accompanied by significant suppression of dynamic range of the desired signal.

Current-domain or current-mode techniques offer a number of advantages. Generally, current-mode circuits do not require amplifiers with high voltage gains thereby reducing the need for high performance amplifiers [27]. At the same time, current-mode circuits generally do not require either high precision resistors or capacitors and, when capacitors are used to store the signal, the capacitors need not display either good ratio matching or linearity [25]. Thus, current-mode circuits can be designed to make them fully compatible with most digital processes.

This compatibility with digital processes makes current-mode circuitry very attractive for interfacing transducers to the digital world due to number of standard IC process compatible transducers that have been developed [3]. Standard commercial digital CMOS IC processes are popular due to the low

cost of fabrication and large availability. While developing high-performance CMOS analog circuitry is difficult with IC processes that are optimized for digital circuitry, a number of design techniques exist to simplify the task.

2.1 MOSFET as a Current-Mode Device

CMOS current-mode design requires a full understanding of the different MOSFET modes of operation and the effect of device mismatch due to the variations in IC process across the die. Unlike BJTs which possess an exponential current response, the MOSFET can operate with a quadratic, linear or exponential characteristic depending on the drain, source and gate voltages. Therefore, the effect of the IC process variations is dependent on which mode of operation the MOSFETs are operating in.

The first mode of operation is known as the constant-current or saturation region. The drain current of a MOSFET operating in this region is often expressed as [28]

$$I_D = \frac{\mu_o C_{ox} W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}), \quad 0 < (V_{GS} - V_T) < V_{DS} \qquad (2.1)$$

where V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, V_T is the threshold voltage, μ_o is the surface mobility of the MOSFET's channel, C_{ox} is the capacitance per unit area of the gate oxide, W is the effective channel width, L is the effective channel length and λ is the channel length modulation parameter. Although the drain current is this region mainly depends on V_{GS}, the current is considered constant because it does not change significantly with V_{DS} except for short channel devices. Thus the operation in this region is desirable for most current-mode circuitry, such as current-mirrors, where ideal current sources are required.

The second mode of operation is known as the linear region. The drain current of a MOSFET operating in this region is modeled as [28]

$$I_D = \frac{\mu_o C_{ox} W}{L}\left\{(V_{GS} - V_T) - \frac{V_{DS}}{2}\right\} V_{DS}\,(1 + \lambda V_{DS}), \qquad (2.2)$$

$$0 < V_{DS} < (V_{GS} - V_T)$$

In this region, the MOSFET acts as a resistor-like device with the drain current depending significantly on either V_{DS} or V_{GS}. Because of this resistor-like response, this region is not generally used for current-mode circuit design.

Modeling another MOSFET region of operation depends on the application. For digital circuitry, the MOSFET is said to be in cutoff when the gate-to-source voltage V_{GS} is less than the threshold voltage V_T. In reality, this is not the case. As V_{GS} approaches V_T, the I_D versus V_{GS} relationship changes from a square-law to an exponential response. The region where V_{GS} is less than V_T is called the subthreshold [29] or weak inversion region [26]. One model for this region is given as [29]

$$I_D = I_{DO}\frac{W}{L}\exp\left(\frac{V_G}{\eta U_T}\right)\left\{\exp\left(-\frac{V_S}{U_T}\right) - \exp\left(-\frac{V_D}{U_T}\right)\right\}, \quad V_{GS} < V_T \qquad (2.3)$$

where U_T is the thermal voltage, I_{DO} is the characteristic current and η is the subthreshold slope factor. The thermal voltage U_T is equal to kT/q where k is the Boltzmann's constant ($1.381\text{x}10^{-23}$ J/°K), q is the unit electron charge ($1.602\text{x}10^{-19}$ C) and T is the temperature. The characteristic current I_{DO} is a process-dependent parameter which is also dependent on V_{SB} and V_T [26].

Equation 2.3 can be simplified if we assume that V_{DS} is much greater than U_T and the V_{SB} is equal to zero. These assumptions yield

$$I_D \cong I_{DO}\frac{W}{L}\exp\left(\frac{V_{GS}}{\eta U_T}\right), \quad V_{GS} < V_T \text{ and } V_{DS} \gg V_T \tag{2.4}$$

Figure 2.1 shows the drain current I_D versus gate-to-source voltage V_{GS} for a MOSFET transistor manufactured using Northern Telecom's 3μm digital CMOS process. While the exponential response in this region can be useful for designing certain circuits, the region may be susceptible to minor defects. Figure 2.2 shows the response of a defective transistor that is well characterized in the strong inversion region, but does not exhibit the expected exponential response. While such a transistor will still function as a digital device, an analog circuit using the transistor in this region of operation would probably fail. The importance of this defect mechanism will depend on the circuit design and the IC process used.

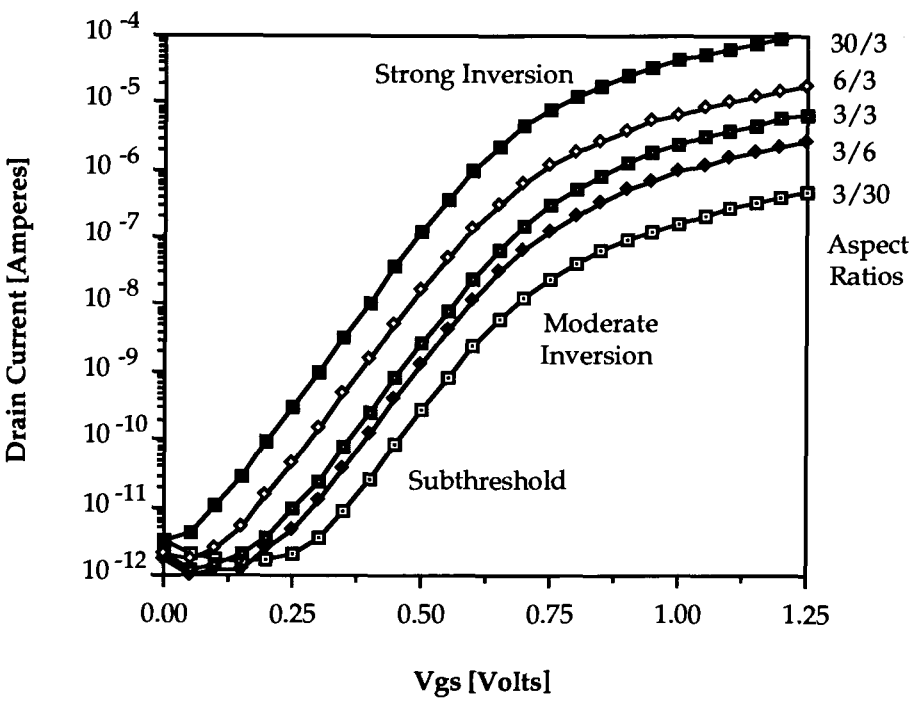

Figure 2.1: MOSFET Subthresold Response

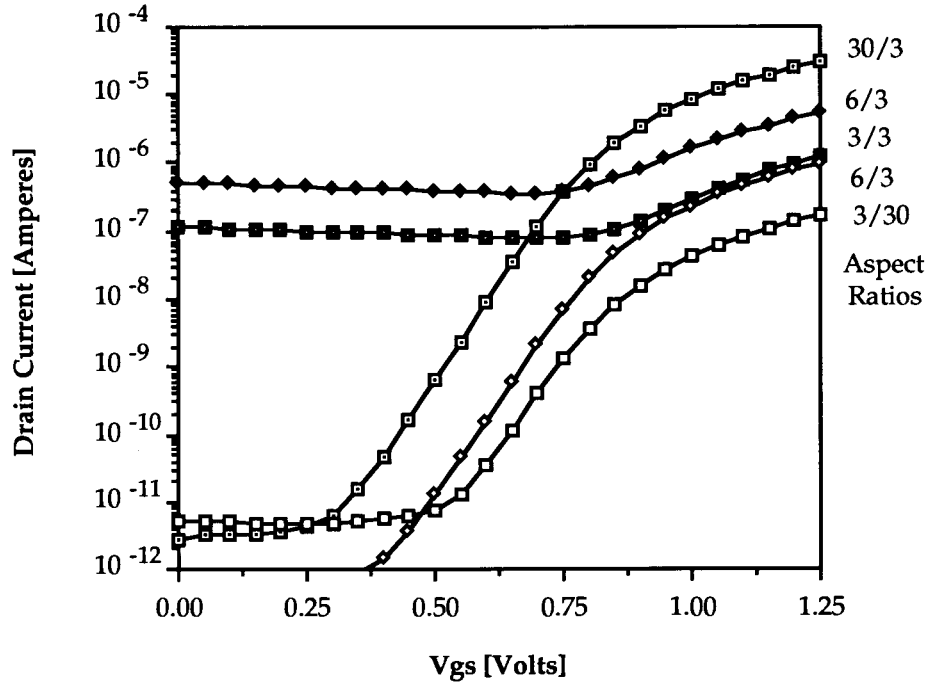

Figure 2.2: MOSFET Subthreshold Response with Defects

The above equations do not properly model the transition between the square-law and the exponential regions. This region, labeled in Figure 2.1, is called the moderate inversion since the drain current is a combination of the weak inversion and the strong inversion effects. A number of models have been developed in the literature for this region [28,30], but are not usually needed for designing current-mode circuitry.

2.2 Analog Circuitry Using Digital CMOS

Unlike digital circuits which operate with a set of fixed voltage levels, analog circuits operate using either voltage or current signals over a continuous domain. Therefore, their accuracy is fundamentally limited by unavoidable mismatches between components, and their dynamic range is limited by noise, offsets and distortions [26]. Unfortunately, digital IC

processes are not optimized to ensure the required matching between similar devices, but for size and speed.

There are two types of variations of device parameters to consider in an IC process. Global variation accounts for the total variation in the value of a device over a wafer or a batch. Local variation or mismatch reflects the variation in a device's value with reference to an adjacent devices on the same chip [31]. By designing analog circuits using component ratios rather than using absolute component values, the effect of global variations can be minimized. However, device mismatch will still effect analog circuit design.

The feasibility of using CMOS for analog circuitry has been researched with a focus on identifying the mechanisms behind component mismatch [26,31]. For MOSFETs, the problem is caused by the variation in device parameters such as the transistor's threshold voltage V_T and transductance K. The effect of these variations on the drain current can depend on the mode the transistor is operating in. For example, the saturation region is relatively insensitive to changes in threshold voltage when compared to the exponential sensitivity of the subthreshold region.

Some research has successfully modeled how the MOSFET parameters change depending on the structure of the device [31]. The transductance and threshold voltage of NMOS and PMOS transistors with varying aspect ratios were compared. The results found that the variation in threshold voltage and transductance was strongly related to the transistor's aspect ratio. This conclusion is significant for CMOS current-mode analog designs where the aim is to use component ratios to counter global parameter variations. Thus, using different aspect ratios to create circuit blocks, such as current amplifiers, could contribute to the local parameter mismatching degrading the block's performance.

A number of methods have been developed to solve the problem of device parameter variation. One method is to use floating gate MOSFET transistors similar to the structures found in EPROM and EEPROM circuits [32]. The device acts as a programmable analog storage that can be used to trim analog circuits. Another method is to use digitally trimmable multigate MOSFET structures which allow the user to modify the transconductance by 0.25% per step using a 4 bit digital word [33]. Other methods rely on laser trimmable structures such as resistor networks and fusible links [34]. However, such corrective techniques can be very time consuming for complex circuitry if each structure must be characterized and corrected.

Another approach to solve the mismatching problem is to use only one transistor. Dynamic current mirrors use one transistor for both the generation of the gate voltage as well as the output drain current [25]. A network of switches alternately connects the transistor in a diode and an output configuration. A capacitor connected to the MOSFET gate stores the gate voltage generated when the transistor is connected in the diode configuration. When the transistor is in the output configuration, the drain current set by the capacitor's gate voltage is routed to the next stage. The problem with this approach is that the mirror requires careful design to minimize charge sharing/injection from the switches [25] and Early voltage effects [35]. The approach also suffers from increased size and complexity.

An unique solution to the matching problem is to use MOSFETs in a lateral bipolar mode to form NPN BJTs [36]. The structure uses the MOSFET's gate to form the BJT's p-type base between two n-type diffusions. With the proper biasing of the MOSFET's gate, well connection (base) and one of the n-type diffusions (emitter), current flows between the two n-type diffusions in a purely bipolar operation. The characteristics of this BJT structure displays

much better matching than MOSFETs making them desirable for current mirrors [36]. However, a large current flows from the emitter to the CMOS substrate due to the formation of a second parasitic BJT structure. This wasted current could be significant when a large number of these devices are used or in low-power applications.

A desperate approach is to move to a new digital technology such as BiCMOS [37]. BiCMOS combines the best of both the CMOS and the bipolar processes with digital logic being performed by CMOS devices and the large current control handled by bipolar transistors. The availability of this process is increasing as more IC manufacturers need the improved performance and circuit density, but it is expensive. For analog design, better quality current mirrors may be constructed using the bipolar transistors [26]. However, like the lateral bipolar mode describe above, most BiCMOS processes do not have PNP bipolar transistor structures so purely bipolar circuits are hard to realize.

The use of BiCMOS and other new digital processes for analog circuits will be interesting as the trend for increased digital performance drives the power supply voltage from a typical 5 volts to 3.3 volts and lower. The lower power supply voltage decreases the voltage swing of the digital signals reducing the effect of load capacitance in the circuit. While BiCMOS processes may offer better quality components, such as large linear capacitors, than bulk CMOS processes, the components may have reduced maximum voltage ratings limiting their use. For example, the Northern Telecom 0.8μm BiCMOS process capacitors are rated for an absolute maximum voltage drop of 4 volts [38]. These reduced maximum voltages along with reduced power supply voltages could limit the possible analog circuit configurations, such as cascode current mirrors, unless the MOSFET's threshold voltages are also decreased [37]. However, decreasing the transistor's threshold voltage would

require reducing the gate oxide thickness and fixed oxide charges -- a very significant and difficult change to an IC process which may not be necessary for digital applications.

Even with all the above problems, MOSFETs will continue to play a role in analog designs using bulk CMOS IC processes for at least the near future. Fortunately, some steps may be taken to ensure the matching between similar components. These steps are described in the following section.

2.3 Design Guidelines For Analog CMOS Design

In order to minimize device mismatching, an understanding of the mechanisms that create these parameter variations is desirable. Interest in such research is apparent in the literature [25,26,31,39]. However, the method taken in solving the problem varies between an experimental identification of the best device structures [39] to modeling the expected variation based on standard deviations in device parameters [31].

Empirical methods involves measuring a series of different devices and identifying the structures that have the best matching characteristics. This measured data can be used to generate parameter means and standard deviations which can be useful in predicting the matching characteristics of the structures. While both of these methods are useful, a set of basic process-independent circuit and layout guidelines would be desirable as they could simplify the number of details the designer must consider.

A number of these guidelines for MOSFET structures have been presented in the literature [26,31]. Applying the guidelines to a design minimizes the variations in transconductance and threshold voltage due to aspect ratio and layout effects. Fortunately, a significant amount of the

variation in these parameters can be attributed to transistor's aspect ratio and overall size [31].

However, the design guidelines summarized below do not correct mismatching caused by random process variations. Therefore, the accuracy of the device matching will never be much better than 0.2% [31] to 1% [25]. If this accuracy is not precise enough, then more complicated methods explained previously must be used.

Same Structure. Devices to be matched should have the same structure [26]. For instance, a junction capacitor cannot be matched with an oxide capacitor. As well, while a MOSFET operating in the subthreshold region has an exponential response similar to a BJT, the two devices cannot be matched.

Same Temperature. Matched devices should be at the same temperature [26]. If the circuit is located near a hot spot, such as an integrated thermal pixel, matched devices should be located on the isotherm. Symmetric layout around the dissipative structures can ensure this. However, this guideline is usually not a problem if the chip dissipation is low.

Same Size and Shape. Matched devices must have the same size and shape [26,31]. For MOSFETs and other devices, this does not mean the same aspect ratio, but the identical length and width. This guideline also applies to passive devices such as capacitors and resistors.

For current mirrors, this means that all the transistors must be identical. For non-unity current gains of N/M, multiple transistors are used by paralleling them together in separate groups of N and M matched devices.

Minimum Separation. Minimum distances between matched devices is necessary to take advantage of spatial correlation of fluctuating physical

parameters [31]. Experimental results reported for one digital CMOS process has shown that these fluctuating physical parameters are periodic repeating every 100μm to 200μm [40]. This means that spacing matched devices even 30μm apart may make a significant difference in performance.

Common-centroid geometries should be used to cancel constant gradients of parameters [25,26,31]. This usually means that multiple devices positioned in a symmetric pattern and opposite devices are connected in parallel. For example, current-mirrors using two MOSFETs can be constructed using a quad configuration with opposite corner transistors connected in parallel.

Same Orientation. The same orientation on the chip is necessary to eliminate asymmetries due to anisotropic steps in the process, or to the anisotropy of the silicon itself [26]. This means that current paths, such as the source to drain current in MOSFETs, of matched device be strictly parallel. Layout methods for shrinking the circuit size that violate this guideline, such as meandering MOSFET gates, should be avoided.

Same Surroundings. Devices that are to be matched should have the same surrounding to avoid the effect of certain process steps that are affected by the chip's topology. For example, this guideline minimizes the end effect in a series of current sources implements as a line of transistors, or the street effect in a matrix of capacitors [26]. Since a purely symmetric circuit layout is impossible in most cases, this guideline can be followed by using dummy devices around matched devices. An example of this approach can be found in the implementation of polysilicon resistors for strain gauges [19].

Non Minimum Size. Large devices reduce the effects of edge fluctuations and can improve spatial average of fluctuating parameters [26,31]. However, there is a trade-off between these very large devices and using the

more complicated matching schemes mentioned above. Since matched devices should also be the same size and shape, increasing the overall size of the devices will result in a geometric increase in the overall circuit size.

Device Choice. For example, devices which use a compensating threshold adjust implant, such as PMOS transistors in the Northern Telecom 3μm digital CMOS technology, have a higher mismatch in threshold voltage [31]. While relying on only one type of transistor is unrealistic for most circuit designs, critical current paths should be handled using the more predicable devices.

Mode of Operation. Matching performance of devices that have more than one mode of operation, such as MOSFETs, may depend on the mode used. For example, MOSFETs operating in the saturation region are slightly temperature sensitive due to the change in threshold voltage. However, MOSFETs operating in the subthreshold region are exponentially sensitive to temperature [41]. Figure 2.3 shows how the MOSFET's drain current changes as the temperature is varied for both regions. The subthreshold region has been used for CMOS compatible temperature sensors [42,43]. Therefore, for applications where the temperature of the chip will vary, a good design decision may be to avoid this region of operation.

The saturation region of MOSFET may also be superior to the subthreshold region when large variations in threshold voltage are expected. The saturation region is dependent on the threshold voltage, but the effect of threshold voltage varying a few hundred millivolts can be minimized by using large gate voltages. On the other hand, large gate voltages limits the possible voltage swing of the MOSFET's drain as too low a drain voltage will force the transistor into the linear region. This problem can be solved using

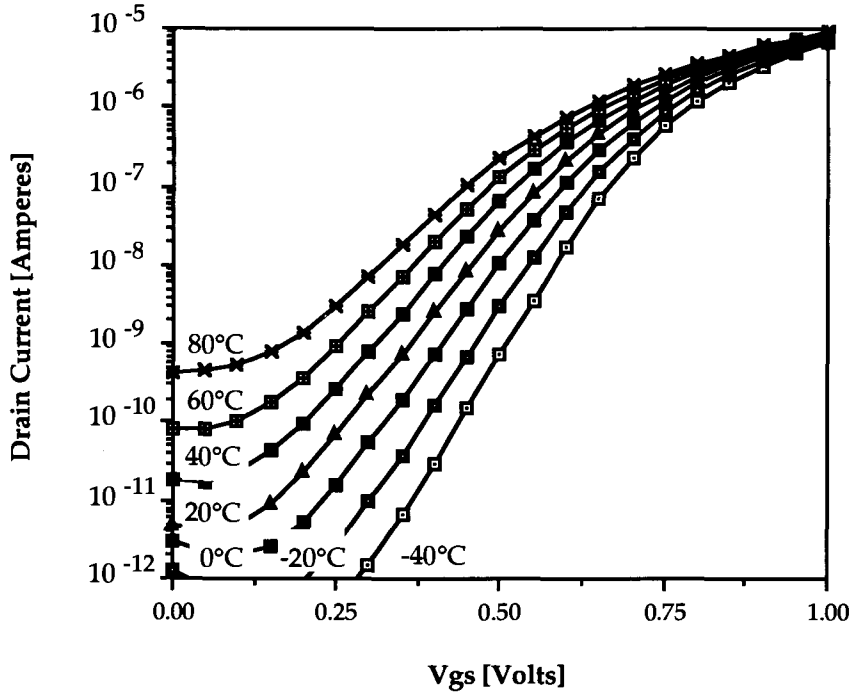

Figure 2.3: MOSFET Subthreshold Temperature Response

an active current mirror created from a basic current-mirror and an operational-amplifier [35] at the expense of increased complexity.

2.4 Design Examples

In order to evaluate the effectiveness of the above design rules, a number of current mirrors were constructed using the Northern Telecom 3μm digital CMOS process. The current mirror performance was measured using an HP 7574A Semiconductor Parameter Analyzer (SPA). The accuracy of the SPA is ±(1.11% + 5pA) for currents less than 10nA, ±0.6% for current between 10nA and 1μA and ±0.4% for currents greater than 1μA. The design goal was accurate and consistent current gains for input currents less than 1μA.

The first current mirror is made from two MOSFETs, shown in Figure 2.4 and 2.5, with aspect ratios of 3μm/3μm and 6μm/3μm to provide a gain of two.

Figure 2.6 shows the typical response of the current mirror for both NMOS and PMOS devices. As you can see, the current gain is neither linear nor predictable which is unacceptable for current-mode circuits.

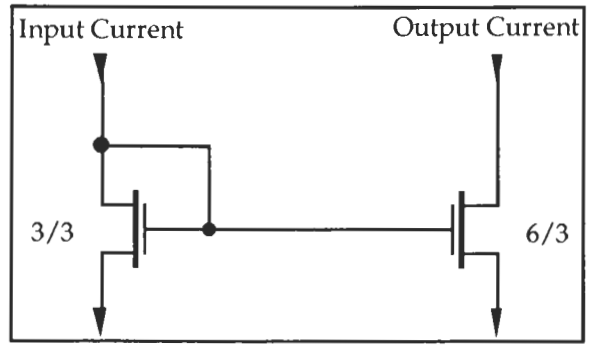

Figure 2.4: Minimum Geometry Current Mirror

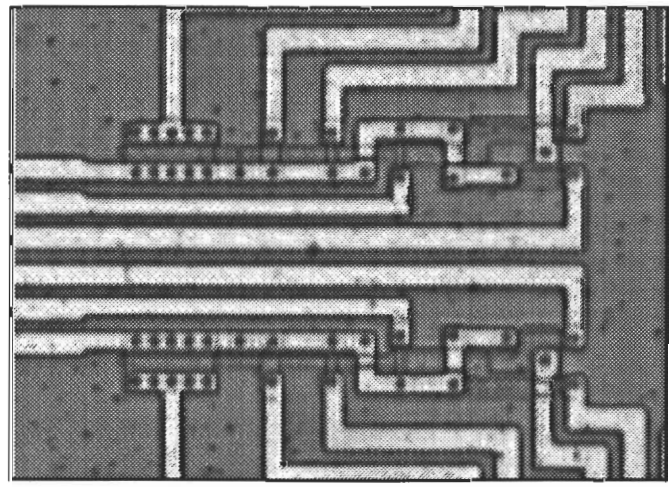

Figure 2.5: Microphotograph of Minimum Geometry Current Mirror

Another series of current mirrors were designed using the guidelines listed above. For these mirrors, three identical transistors are used to provide the gain of two as shown in Figure 2.7 and 2.8. The long transistor length ensures the transistor operates with as large as possible gate voltage. While

the width of the transistor is only a little larger than minimum size, it

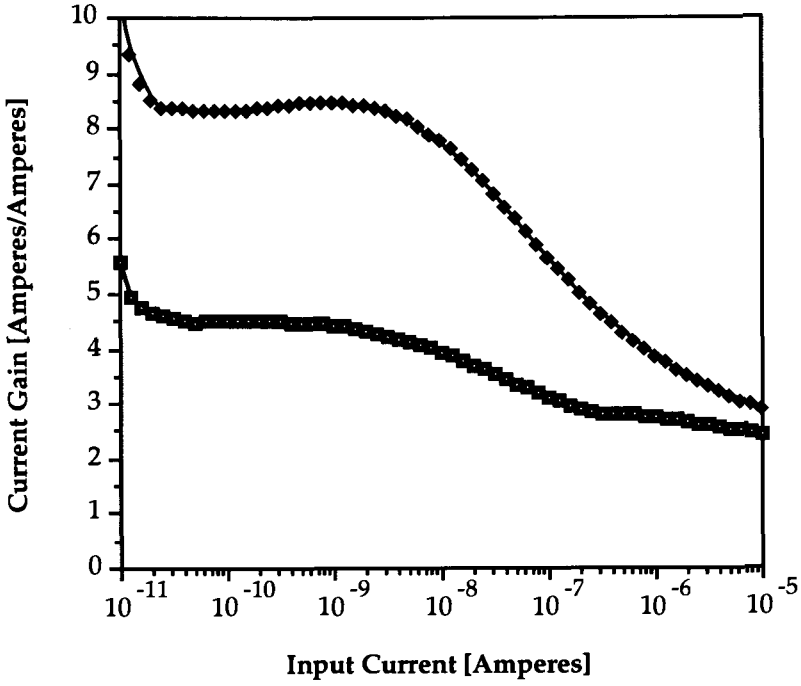

Figure 2.6: Gains of Current Mirrors using Minimum Geometry MOSFETs

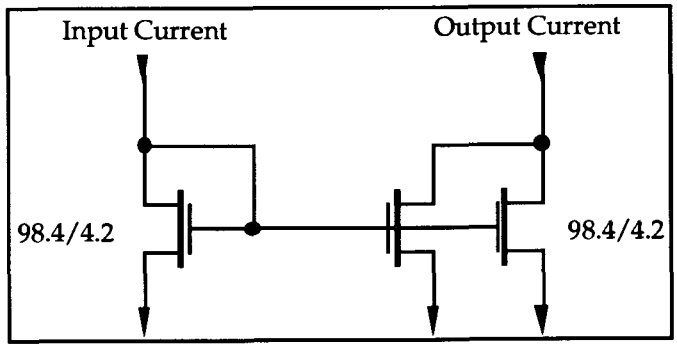

Figure 2.7: Optimized Geometry Current Mirror

represents a trade-off with the transistors length. Figure 2.9 shows very linear current gains from 1nA to 10μA for all the current mirrors.

The NMOS current mirror gains were measured over the desired region to be 1.99±2% using 4.2μm/98.4μm transistors and 1.98±7% using

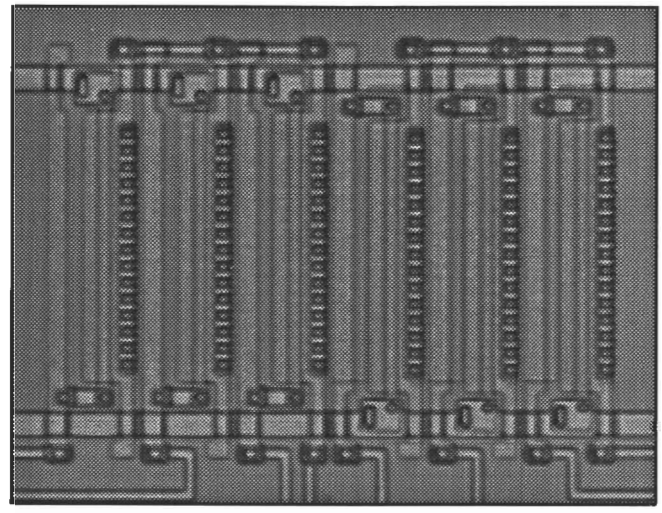

Figure 2.8: Microphotograph of Optimized Current Mirror

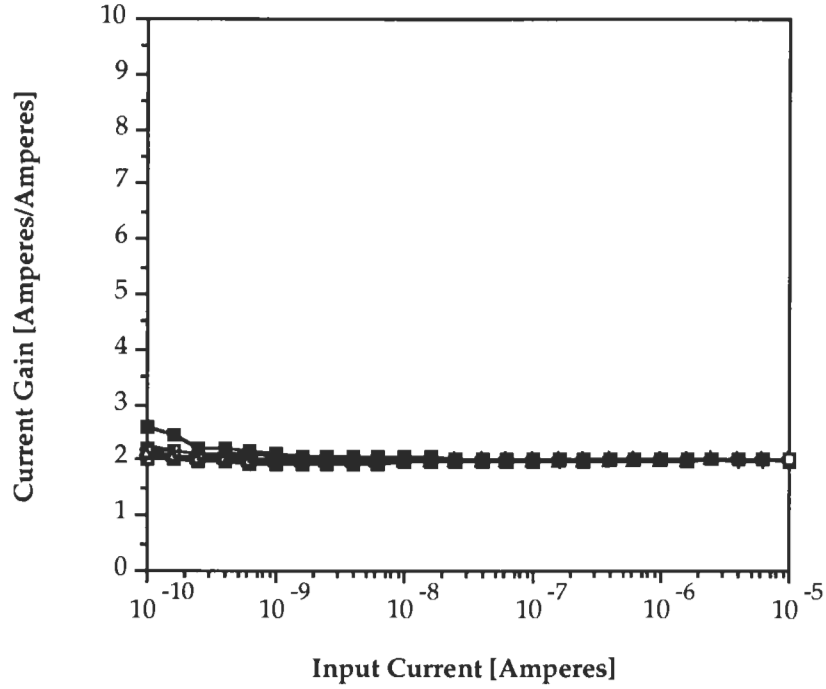

Figure 2.9: Gain of Optimized Current Mirrors

4.2μm/49.2μm transistors. The PMOS current mirror gains were 2.01±%4 using 4.2μm/98.4μm transistors and 2.05±6% using 4.2μm/49.2μm

transistors.. As expected, the larger transistors produced better quality current mirrors.

For a first attempt at designing precision current mirrors, these results display the usefulness of the guidelines for current-mode circuit design. The techniques learned here can now be applied to specific problems.

3 Current-Mode Multi-Bit A/D Converters

The need for mixed analog/digital VLSI systems will ensure the necessity for small sized, high speed analog-to-digital converters fabricated using commonly available digital processes. Since current mode circuits can be designed almost exclusively with transistors, they are fully compatible with most digital processes. While A/D converters may use current mode techniques [25], the choice of architecture for the A/D converter has a significant impact on the converter's size and performance.

Building efficient visual-to-thermal radiation converters, described in Chapter 5, to simulate an infrared scene from an optical image is one application that may require such A/D converters. Dynamic thermal scene simulators require rapid input of data for scene simulation. One method of accomplishing this is to input the data optically. By using CMOS compatible photodetector and micromachining, a CMOS compatible visual-to-thermal converter (VTC) can be realized [24].

An A/D converter operating in the current domain can convert the photodetector current directly to an usable digital form. However, a non-standard solution is required for the VTC due to the structure of the cell and the fact that thousands of VTCs must comprise a thermal scene simulator. In this section, the two A/D converters are presented for the integrated transducer applications such as the VTC.

3.1 A/D Signal Conversion Methods

A current mode A/D converter allows transforming a transducer current output directly to a usable digital form. However, the output of a

transducer may vary over a large dynamic range. For example, a CMOS compatible photodiode current output can vary over six orders of magnitude depending on the incident light intensity. This would require either an A/D converter with a large number of bits or a means of scaling the A/D converter's range of operation.

As well, the current generated by transducers, such as small photodetectors, can be much less than 1μA. Such signals are very sensitive to noise and would suffer degradation over long distances. For this reason, the A/D converter should be integrated very close to the transducer. The resulting digital form of the transducer's output can then be used anywhere on the chip.

In order to integrate the A/D converter into the VTC, a "smart" low power conversion method is desired. Incorporating this intelligence into the VTC reduces the number of external signal connections to the VTC, decreasing the area used by data buses. Since thousands of these VTC will be used in the final wafer-scale system, excessive current consumption by the A/D converter could cause power distribution problems on the silicon wafer. Careful design would simplify such implementation issues.

Commonly used conversion methods manufacturable in CMOS technology include: flash converters, successive-approximation converters, oversampling converters and algorithmic (cyclic) converters. The first approach, flash conversion, has extremely fast conversion rates, but fails to meet the low-power dissipation [44]. Both the flash conversion and the successive-approximation methods fail the die area requirements. The oversampling converters require capacitors and external clocking signals. Fortunately, the algorithmic method offers both small die area and low power dissipation making it desirable for VLSI systems [25,45].

For applications targeting thermal scene simulation which require dense arrays of VTC cells, the algorithmic conversion method offers a possible solution. By using current-domain techniques and algorithmic conversion methods, two small low power A/D converters have been developed for such applications using Northern Telecom's 3μm digital CMOS process.

3.2 Pipelined A/D Signal Conversion

The simplest A/D conversion using current-domain methods is performed in a bit-by-bit fashion using a number of stages each containing a current comparator and current subtraction circuitry [25]. Both the size and accuracy of the A/D converter can be easily scaled by adding additional stages.

In this design, each stage of the converter compares twice the input current from the previous stage to a reference current and outputs a digital bit as shown in Figures 3.1 and 3.2. Depending on the digital bit, the output current to the next stage is either twice the input current or the difference between twice the input current and the reference current. Thus, the sensitivity of the stage to a small current change depends on its current comparator, while the overall accuracy of the A/D converter's digital value depends on the precision of the current mirrors.

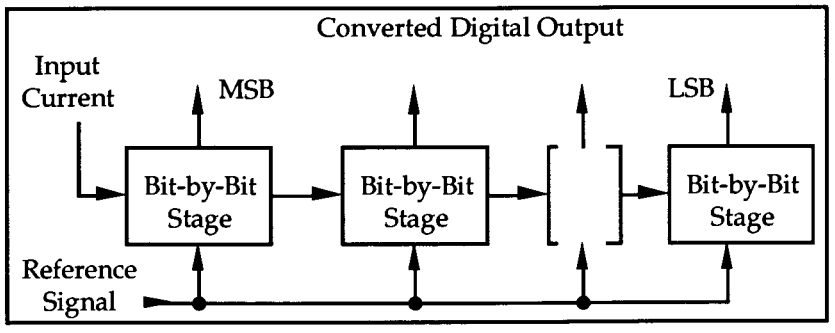

Figure 3.1: Block Diagram of a Pipelined A/D Converter

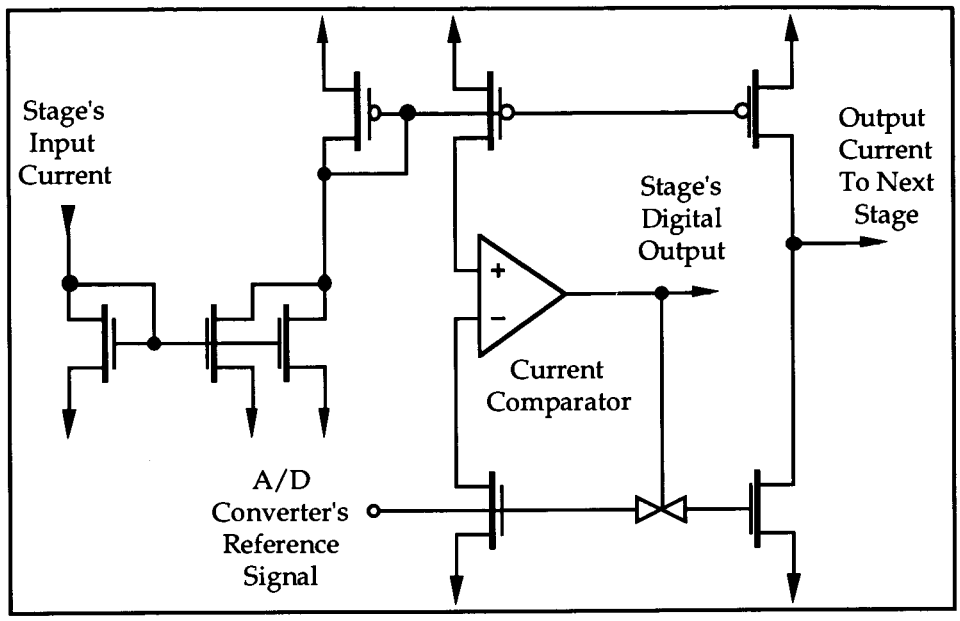

Figure 3.2: Schematic of a Pipelined A/D Converter Stage

The current comparator and transmission gate blocks shown in Figure 3.2 were designed for small size and low power consumption. The schematic in Figure 3.3 is the transmission gate which includes a transistor to ground the output. This transistor prevents the output from floating when the transmission gate is turned off. The current comparator described in Figure 3.4 uses two digital inverters to convert the output of two conflicting current mirrors into a digital value. Both blocks operate over a large dynamic range and are insensitive to device parameter variations.

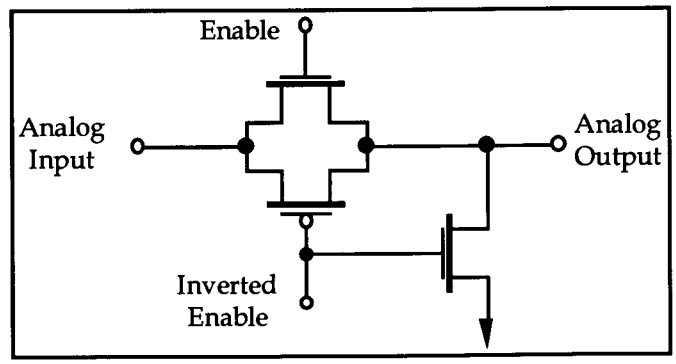

Figure 3.3: Transmission Gate Schematic

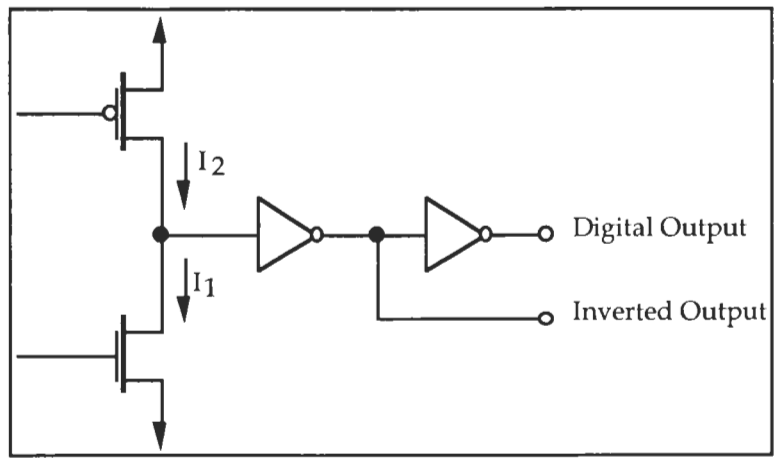

Figure 3.4: Current Comparator Schematic

A photomicrograph of one of the test A/D converter stages characterized is shown in Figure 3.5. Tests of a single A/D converter stage using a Hewlett-Packard Semiconductor Parameter Analyzer (SPA) showed very good linearity of the conversion within five decades of input current as shown in Figure 3.6. The upper operating range of the converter stage is limited by the current comparator while the lower operating range is limited by the current mirroring errors.

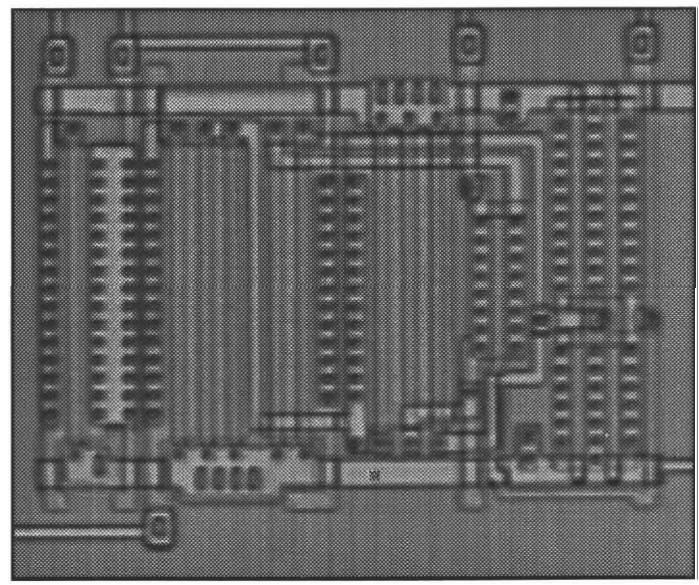

Figure 3.5: Microphotograph of a Pipelined A/D Converter Stage

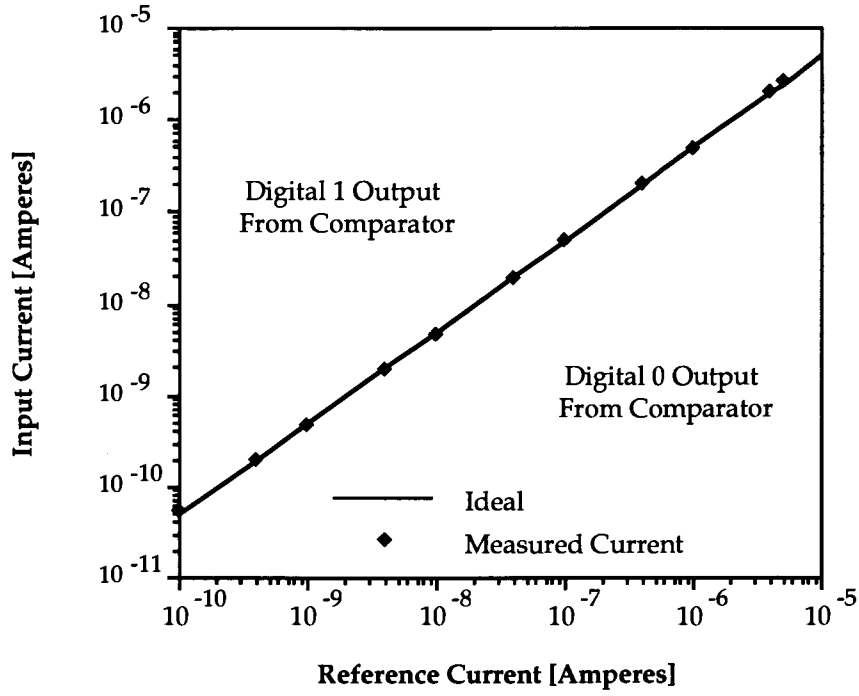

Figure 3.6: Linearity of a Single Pipelined A/D Converter Stage

Because of the sequential nature of this design, the mirroring errors in each stage accumulate throughout the entire A/D converter, limiting the overall size and performance. The non-linearity is most prominent when the A/D converter's most significant bit has gone active as the following stages must process an extremely small current. Evaluating the design using a four bit A/D converter displayed the most non-linearity when the output changes between 7, 8 and 9. In extreme cases, the A/D converter will miss some output values due to these accumulated mirroring errors. These results are consistent with similar designs using this conversion method published in the literature [35].

Another reason why we found this A/D converter not acceptable for the VTC is that the range of the converter's operation cannot be easily shifted. The reason for this difficulty is that the current subtraction circuitry will only function over a small range in order to ensure that all transistors operate in

the saturation region. To understand the problem with the current subtraction, a simplified circuit diagram shown in Figure 3.7 is analyzed. To ensure that the transistor Q_1 remains in the constant-current region described in Chapter 2, the drain voltage swing is limited by the gate voltage.

$$V_{DS1} > (V_{GS1} - V_T) \tag{3.1}$$

In this case, the drain voltage V_{DS1} is set by the following stage's input transistor Q_3 and the difference in the two currents:

$$I_2 - I_1 = K_3 (V_{GS3} - V_T)^2 \tag{3.2}$$

By combining equations 3.1 and 3.2 and setting V_{DS1} equal to V_{GS3}, a lower bound on the minimum current difference is given:

$$I_2 - I_1 > K_3 (V_{GS1} - 2V_T)^2 \tag{3.3}$$

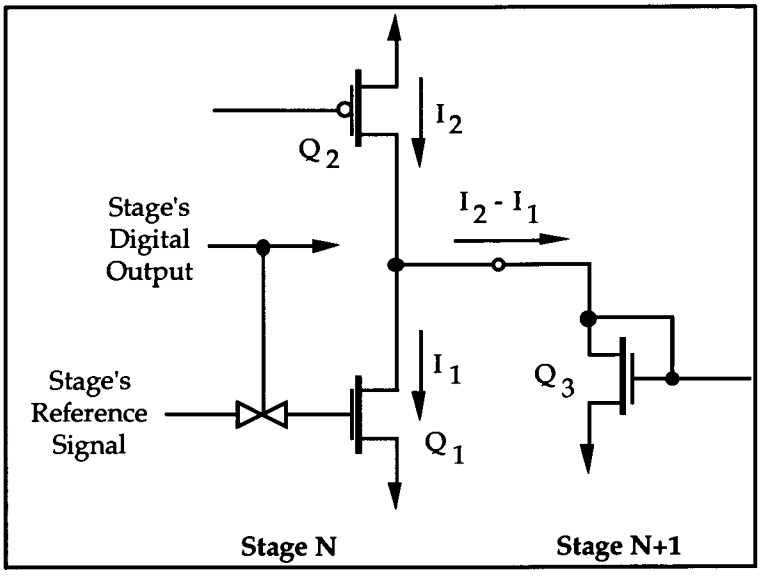

Figure 3.7: Schematic of the Pipelined A/D Converter Current Subtractor

The above equation states that to accurately subtract two equal current signals I_1 and I_2 and produce a zero output current to the next converter stage, the gate voltage V_{GS1}, determined by the converter's reference signal, must be equal to twice the transistor's threshold voltage V_T. Thus, attempting to operate the A/D converter outside this range increases the current mirroring errors and further degrades the converter's performance.

Figure 3.8 shows the measured upper and lower operating ranges of the 4 bit test A/D converter developed here. Measurement was performed using a Hewlett-Packard SPA. For this converter design, input currents ranging between approximately 35nA to 800nA may be converted to a 4 bit digital form using the appropriate reference signal. As described above, the most non-linearity can be seen as the converter output changes from 7 through 9.

A number of design modifications, such as optimizing the current mirror's performance and subtraction circuitry, were attempted in order to

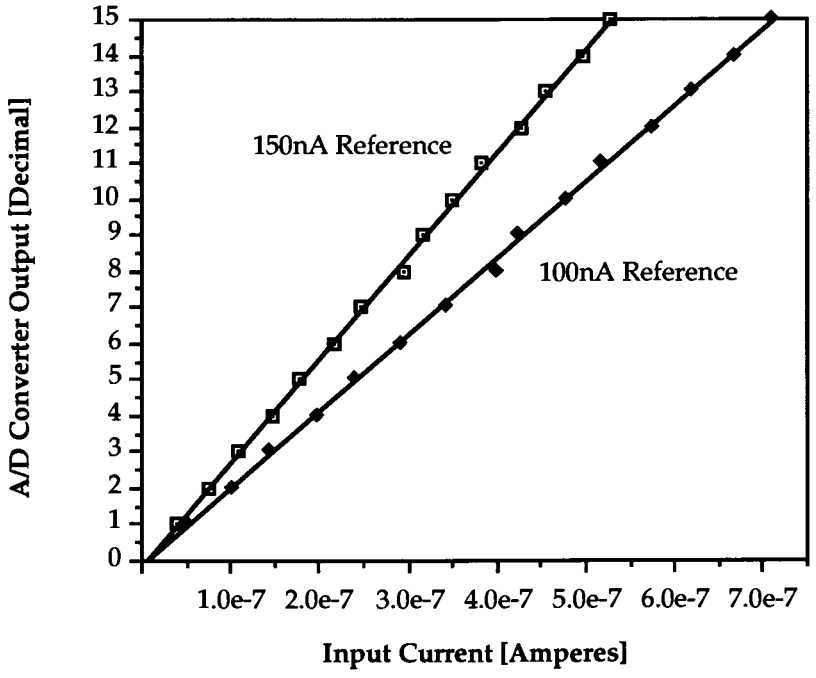

Figure 3.8: Response of a 4 Bit Pipelined A/D Converter

solve some of the problems with the pipelined conversion discussed. In most cases, solutions presented in the literature require variations of active current mirroring using switched capacitors or operational-amplifiers [25,36,45]. Unfortunately, switch capacitor based mirrors suffer from errors caused by charge injection/sharing by the switching circuitry which would become a significant source of noise for the small currents being converted. As well, current mirrors using operational-amplifiers would increase the size and current consumption of the design. We would like to take advantage of the algorithm nature of the conversion method to provide a simple, but effective solution.

3.3 Parallel A/D Signal Conversion

An alternate conversion method attempts to address some of the limitations of the pipelined conversion method. In order to reduce the cumulative effects of current mirroring errors, a sequential design can not be used. Also, replacing the current subtraction circuit would allow for a larger range of operation, a feature important for adding flexibility to the VTC design.

The technique is a parallel conversion method using current addition and comparing stages as shown in Figure 3.9. For each stage, a new reference current is generated using the previous bit values and geometrically aspect ratioed transistors. The reference current is then compared to the A/D converter's input current to determine the stage's digital output. This design improves on the linearity and input range of the pipelined converter by reducing the cumulative error from current mirroring and current subtraction errors [46]. However, small errors caused by device parameter

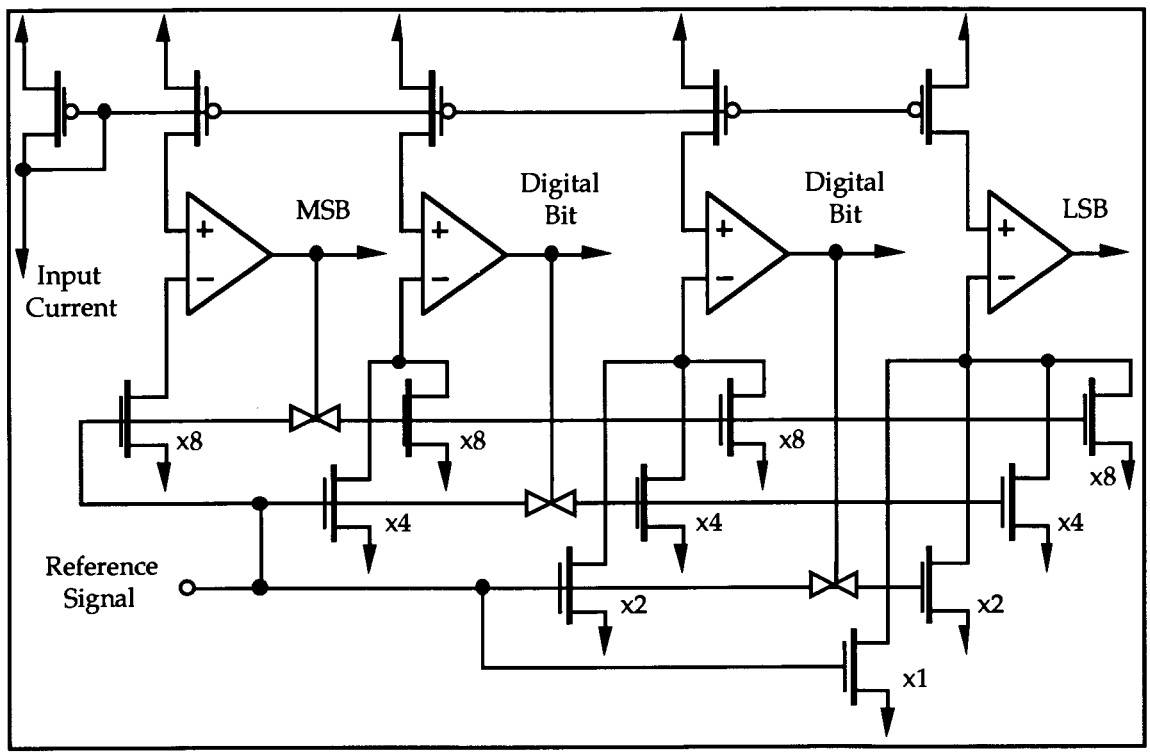

Figure 3.9: Schematic of a 4 Bit Parallel A/D Converter

variations still affect the converter's performance, but not as significantly asthe pipelined signal conversion method.

Current addition is easily implemented and does not limit the converter's range of operation. In this test design, shown in Figure 3.10, the converters linear operation ranged from approximately 1nA to 2.5μA and was limited by the current comparator for large input currents and current mirrors for small input currents. This range is large enough to cover the photodetector current range of interest. Figure 3.11 and 3.12 shows the upper and lower response of the test 4 bit A/D converter at two extreme points of its operation range. Another feature is the feasibility of implementing nonlinear conversion schemes, necessary to cover broad ranges of the input currents. By using each stage's reference current to generate a new nonlinear

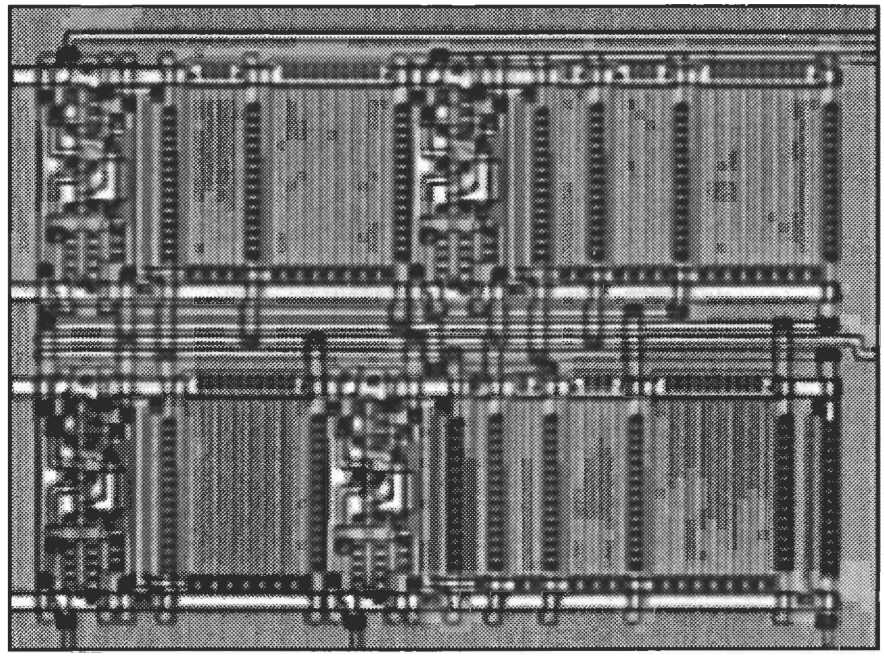

Figure 3.10: Microphotograph of a 4 Bit Parallel A/D Converter

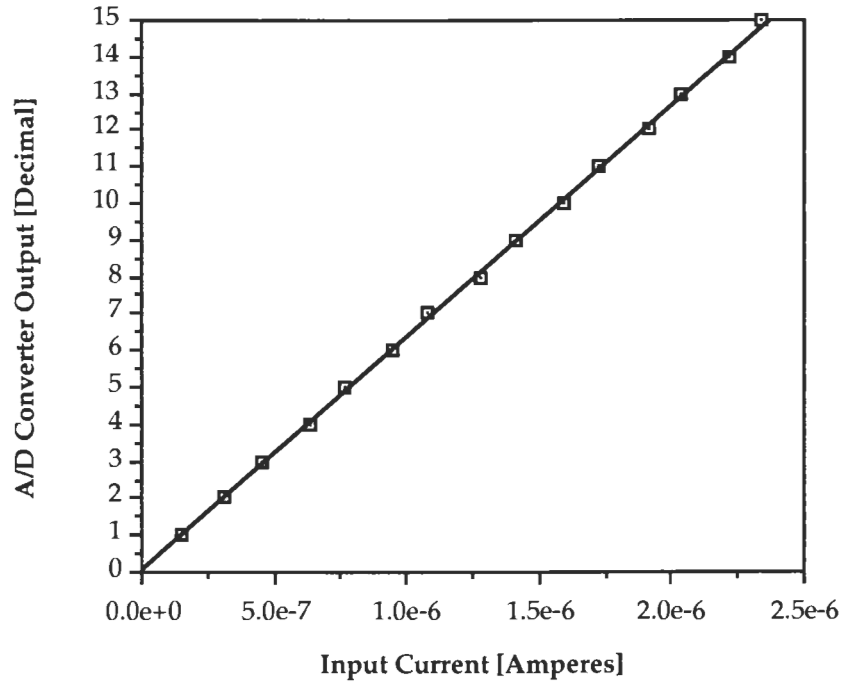

Figure 3.11: Large Input Response of 4 Bit Parallel A/D Converter

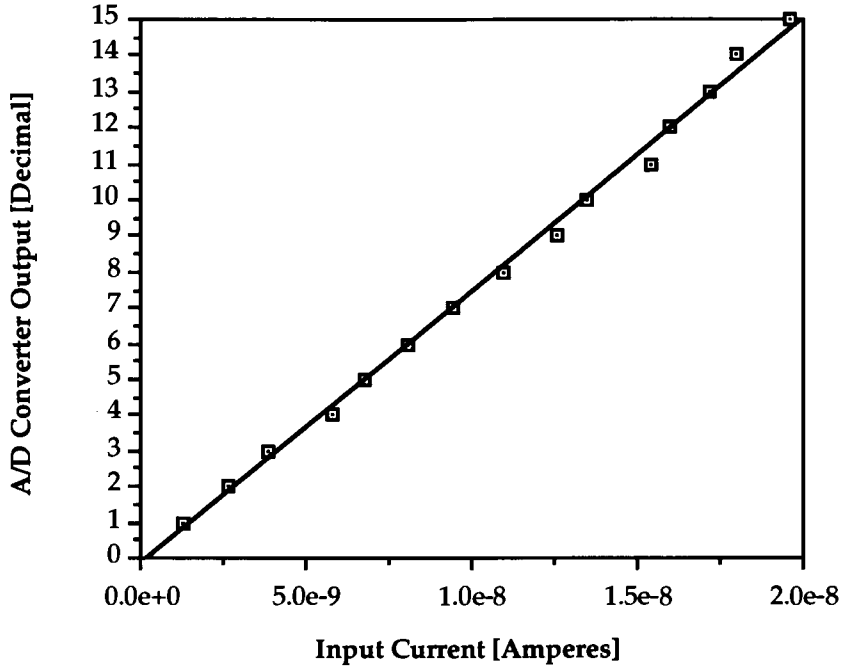

Figure 3.12: Small Input Response of 4 Bit Parallel A/D Converter

reference current for the stage, the converter will follow the inverse nonlinear function. This feature could become very important for many integrated transducers applications where the sensor signal varies non-linearly over a very broad range.

Unfortunately, the parallel method requires more area than the pipelined conversion due to the increase circuit complexity and the larger transistors. Since a stage's reference current is generated using geometrically increasing transistor aspect ratios, the size of A/D converter will increase geometrically as the number of bits increase. This may limit the useful size of the A/D converter for array applications with significant space limitations to 5 or 6 bits.

3.4 Comparison Summary

In this section, two algorithmic A/D converters were developed and tested. While a pipelined A/D converter may be implemented using a digital CMOS process, it's response is sensitive to current mirroring errors and cannot be shifted like the parallel A/D converter. However, the parallel A/D converter relies on geometrically sized transistors and thus requires additional chip area for implementations greater than 4 bits.

While both A/D converter designs are small when compared to one chip A/D solutions, they are sensitive to process variations and are still too large for some applications with significant space limitations. In the following chapter, alternative A/D conversion methods focusing on size are examined.

4 Time-Domain A/D Encoding

The communication of analog transducer signals in digital VLSI systems pose some special design problems. An analog signal is susceptible to noise and other degradation effects when transmitted over relatively long distances. Converting an analog signal to a set of digital signals multiplies the number of data wires that must be routed. For array applications where information must be transferred between array cells, the number of bus signals interconnecting the cells must be kept small to maximize the cell density.

A single digital bit can represent two values of information: a logical high and a logical low. Normally, an analog signal is converted to its respective base 2 value which is represented by a set of digital signals. In order to preserve the dynamic range of the analog signal, a large number of bits must be used. For example, an analog signal that varies over one order of magnitude may be represented by 4 digital bits. However, an analog signal that varies over 6 orders of magnitude, which is typical for a number of transducers, must be represented by 20 digital bits. Unfortunately, the area required for such a data bus as well as the required analog-to-digital converter is not acceptable for some applications. Obviously, new methods of transmitting analog signals must be devised to solve these design issues.

While a digital bit usually represents only two possible values, a single bit can represent an analog signal by using the transitions of the bit rather than the digital levels to encode the analog information. Thus, the current-domain or voltage-domain analog signal is communicated as a time-domain signal. Depending on the scheme used, analog information may be

represented by the digital signal's frequency or duty cycle or as a combination of digital pulses.

Time-domain signals still retain the same noise immunity that digital signals possess allowing them to be transmitted over long distances. Other advantages include one wire per analog signal as well as being readable by computer systems. However, analog signals are essentially low-pass filtered when represented in the time domain as rapid changes in signal level cannot be communicated between digital transitions. This is not a problem if sufficiently high frequencies are used.

In this section, current-mode frequency and sigma-delta encoding circuitry are developed with small size, low power and versatility being key design criteria. In order to meet these criteria, switched-current design techniques are used to provide the required time delay circuitry.

4.1 Switched-Current Circuit Design

Analog sampled-data signal processing has been dominated for the past decade by the switched-capacitor (SC) circuits. This technique, which uses switched-capacitor integrators to replace resistor-capacitor (RC) circuit structures, relies on precisely defined capacitance ratios (with a low voltage coefficient) to perform difference-equation algorithms on voltage samples. This manipulation is accomplished by transferring charges between floating capacitors during clocking pulses. For linear operation, these capacitors must also be linear. However, realizing precision floating linear capacitors with high ratio accuracy requires additional fabrication steps over standard digital CMOS processes [47]. Figure 4.1 shows a simple SC integrator.

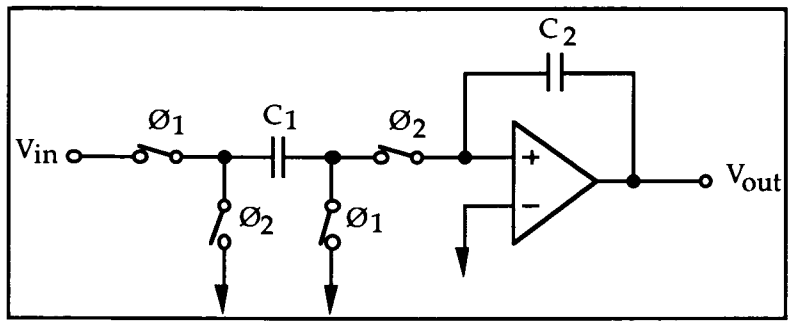

Figure 4.1: Schematic of a Simple Switched-Capacitor Integrator

A switched-current (SI) system may be defined as a system using analog sampled-data circuits in which signals are represented by current samples. Unlike SC circuits, SI circuits use MOS transistors as the storage elements to provide analog memory capability. Similar to the operation of dynamic logic circuits, a voltage is stored on the gate of the MOSFET and held using the gate capacitance. The held gate voltage generates a corresponding held current signal in the drain. Thus, linear floating capacitors are not required for SI circuits and, in principal, the voltage swings are not as large as the signals represented by currents, giving a potential for low supply voltage operation [25]. Since the voltage swings are less in SI circuits than in SC circuits, this approach results in increased speed [47].

Figure 4.2 shows an example schematic of a simple SI track and hold. In this design, the diode connected MOSFET operates as a nonlinear current-to-voltage converter generating the gate voltage for the output MOSFET. When the switch is on (track), the output current is the mirror of the input current. However, when the switch is off (hold), the output MOSFET acts as a nonlinear voltage-to-current converter generating a constant output current based on the voltage stored on its gate capacitance. Since the two converters are inverse functions of each other, the entire circuit operates linearly in the current domain.

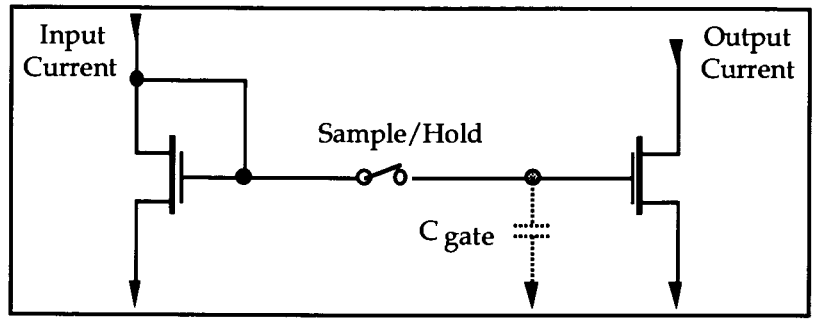

Figure 4.2: Schematic of a Simple Switched-Current Track and Hold

Thus the accuracy of the SI design is dependent only on the matching of MOSFET characteristics and not on the capacitance on the gate connections. While channel length modulation through drain voltage variations and charge injection/sharing into the storage capacitance from the switches produce errors in the output current, SI circuits do not suffer from the operation-amplifier limitations of SC circuits. Fortunately, all of these effects may be minimized with careful design [25,47,48].

A major design problem is a digitally controlled current switching circuit that will operate with currents less than 1μA. Typical current switching methods shown in Figure 4.3 were tested and found to have limitations with small currents. For example, current starved inverters are limited to a relatively small voltage swing and may suffer leakage effects between the two mirrors. Differential amplifier based switches suffer from offset currents due to poor current mirroring causing drift problems. In general, we are looking for a simple effective solution that is insensitive to device parameter variations.

The best solution to the problem may not be switching the current at all, but to shunted the current away from the output or turned off the current in the current mirror feeding the output. A number of methods are shown

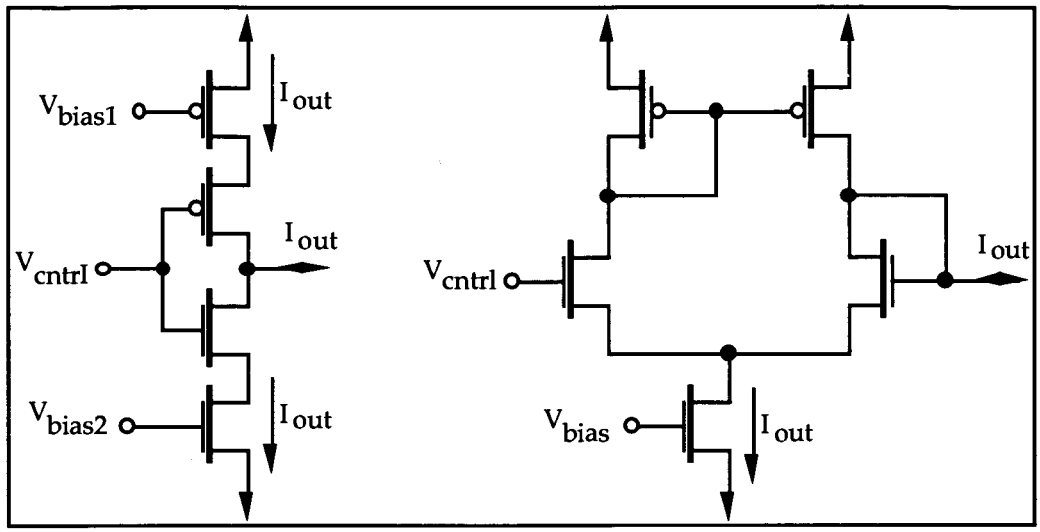

Figure 4.3: Popular Current Switching Circuitry

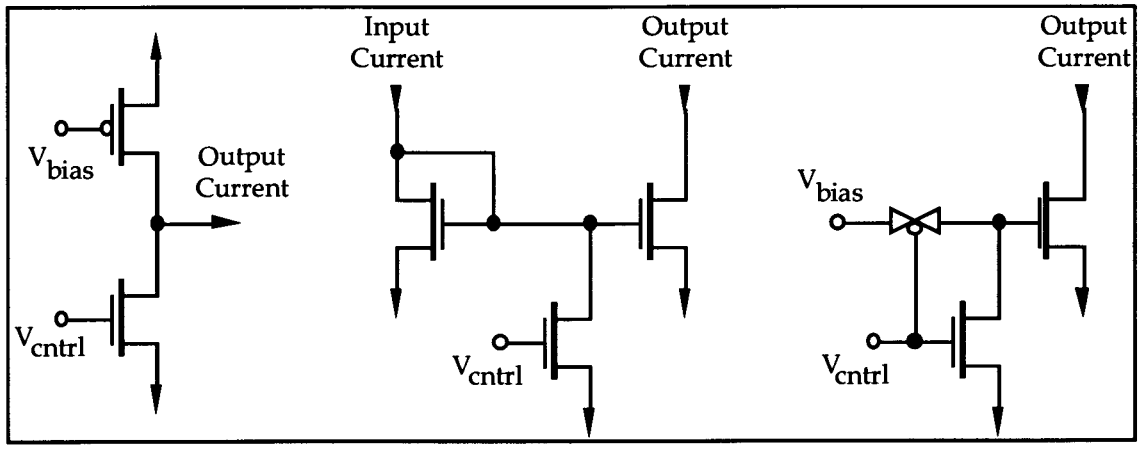

Figure 4.4: Alternate Current Switching Methods

in Figure 4.4. The first method switched the output from zero to a preset current limit. While this method may seem extreme, it can be used to ensure a capacitor, connected to the switch output, is fully discharged before a charging cycle is started. The other two methods control a current mirror depending on whether the input bias is a voltage or a current. An advantage of these methods is that all switching transistors are minimum geometry and

do not effect the current mirroring performance. All three methods were tested experimentally and found to operate over a large dynamic range .

In the following sections, SI techniques will be applied to the problem of designing variable time-delay circuitry for use in oscillators and sigma-delta encoders. While some of the designs do not operate strictly as SI circuits, they rely on the concepts presented in this section.

4.2 Current-Controlled Oscillator

A current-controlled oscillator (ICO) generates a fixed amplitude digital pulse signal with a frequency proportional to the input current signal. In other words, the current-domain analog signal has been moved into the time domain. The more popular form of oscillator is the voltage controlled oscillator (VCO) which converts an analog voltage signal to a corresponding frequency. While VCOs are more common and have been used in current-mode signal processing [49], the ICO will not require the extra current-to-voltage converter circuitry when interfaced to current based transducers.

Simple variable oscillators can be made from any odd number of inverter stages which have adjustable propagation delays. A number of such oscillators have been developed for transducer systems [9,43,50], but are optimized for power consumption and not for size. Most rely on the method similar to the design shown in Figure 4.5 [43] with the MOSFETs acting as matched pull-up resistors for each stage. These MOSFET resistors form crude RC networks that dominate the propagation delay of each stage. As well, such a design requires additional circuitry such as diode connected MOSFETs or set-reset flip/flops to prevent interaction between each stage.

The SI approach developed in the previous section may be used to design an ICO. Since the ICO must be very small, only one inverting stage is

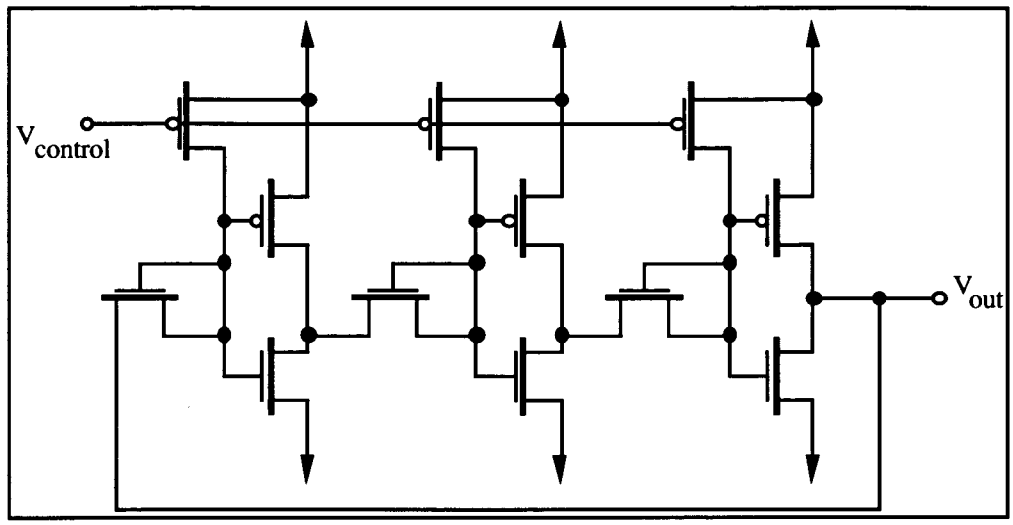

Figure 4.5: Voltage-Controlled Ring Oscillator

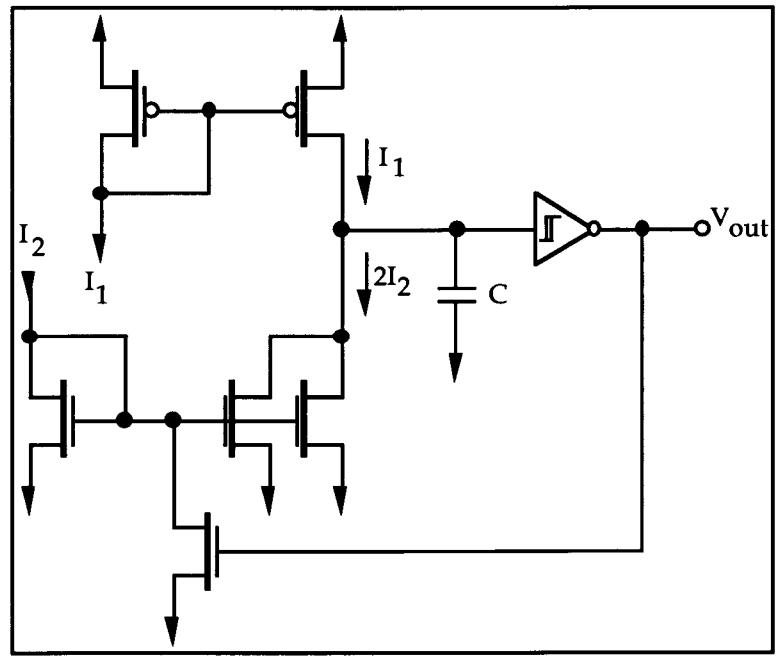

Figure 4.6: Two Input Current-Controlled Ring Oscillator

used as shown in Figure 4.6. A Schmitt trigger is used to control when the ICO output changes state. Unfortunately, this design was developed very late in the thesis and was not fabricated as a standard cell as shown in Figure 4.7.

However, a number of standard cells and current-mirror test structures fabricated using Northern Telecom's 3μm digital CMOS process were used to construct a circuit to test the ICO presented here.

The oscillator frequency response of the ICO is approximately

$$F = \frac{1}{C(V_+ - V_-)} \frac{I_1 (2I_2 - I_1)}{2I_2} \tag{4.1}$$

where V_+ and V_- are the upper and lower switching thresholds of the Schmitt trigger and C may be a fixed capacitor or the input capacitance of the Schmitt trigger. While the frequency is not a simple function, the duty cycle of the oscillator is given by

$$\text{duty cycle} = \frac{I_1}{2 I_2} \ 100\% \tag{4.2}$$

which is independent on the capacitor's value or its voltage swing. This feature is important as relative value of two analog signals can be communicated with one digital signal without the need to characterize the

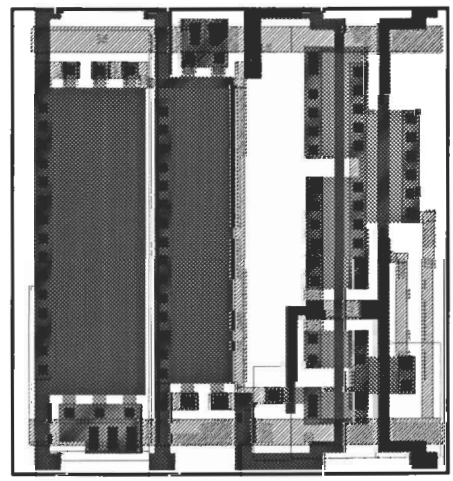

Figure 4.7: Layout of a Two Input Current-Controlled Ring Oscillator

oscillator. Figures 4.8 and 4.9 show the measured frequency and duty cycle response of the test circuit. However, due to the large stray capacitance from the chip package, the measured frequency is very low. HSpice simulations indicate that the output frequency for the same input current would be two to three orders of magnitude larger when designed as a standard cell.

From the above equations, the information about two analog signals, in this case I_1 and I_2, can be transmitted using one wire. However, the oscillator can be modified to accept only one input as shown in Figure 4.10. The output digital signal has a fixed duty cycle of 50% with a frequency given by

$$F = \frac{I}{2C(V_+ - V_-)} \tag{4.3}$$

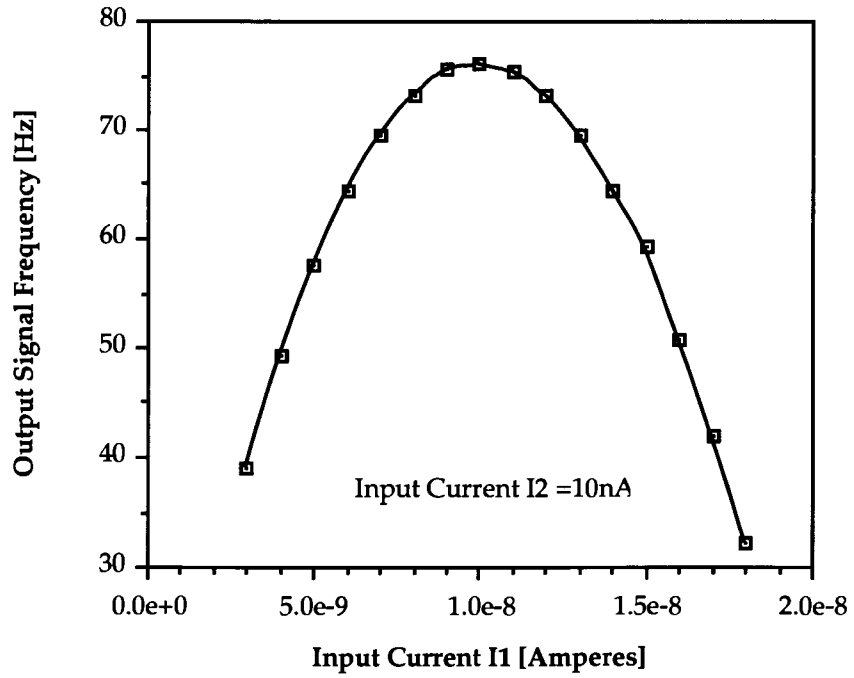

Figure 4.8: Frequency Response of Current-Controlled Ring Oscillator

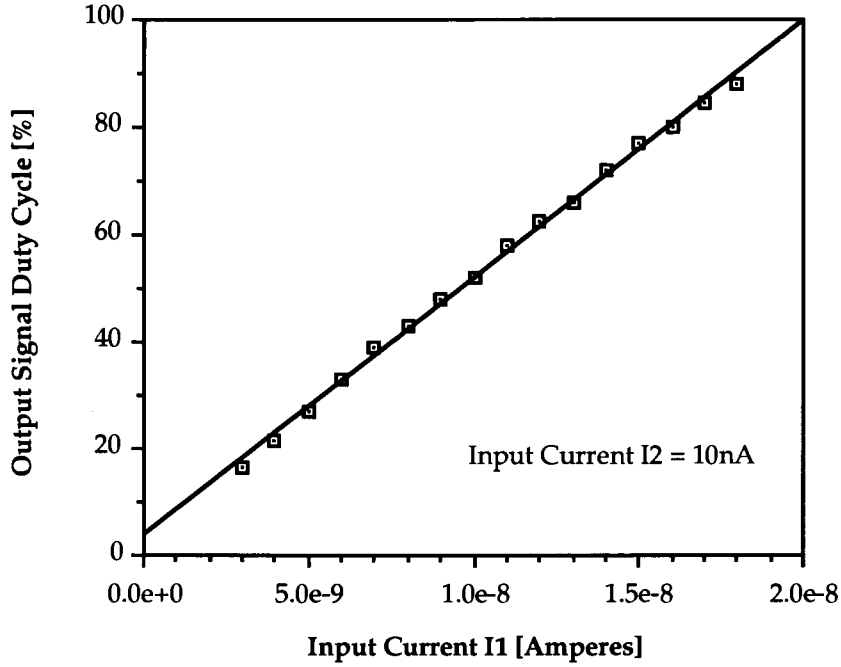

Figure 4.9: Duty Cycle Response of Current-Controlled Ring Oscillator

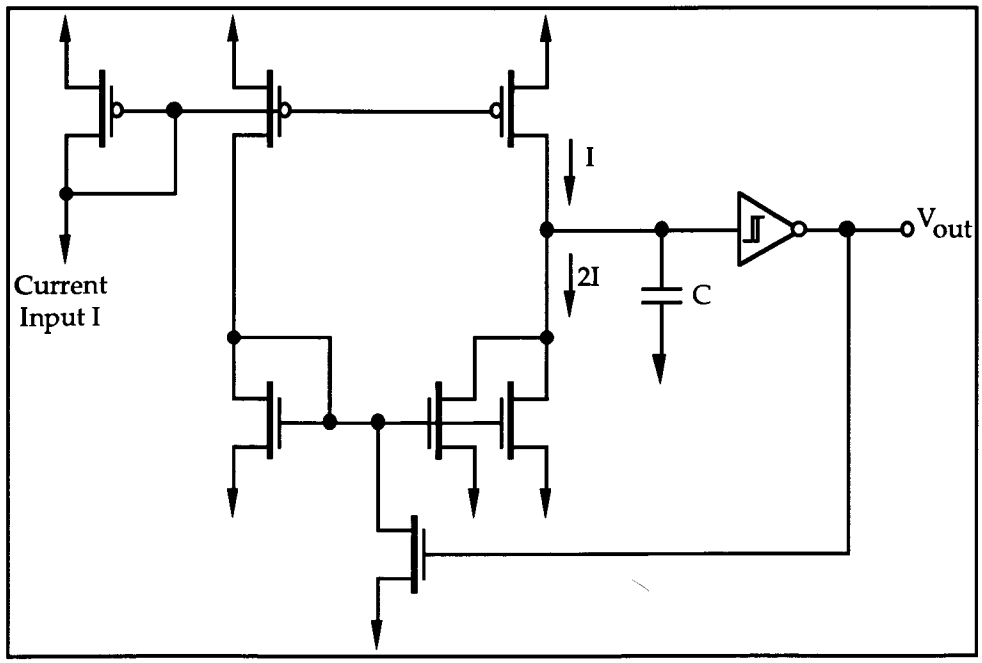

Figure 4.10: Single Input Current-Controlled Ring Oscillator

The measured characteristics shown in Figure 4.11 are very close to the expected linear response with the response rolling off at large currents due to the current mirroring limitations. A possible feature of this design may be to measure small or large changes in capacitance rather than current by replacing the fixed capacitor with a capacitance based transducer. Stray capacitance, such as the input gate capacitance of the Schmitt trigger, that affect the transducer measurement may be minimized using minimum geometry devices.

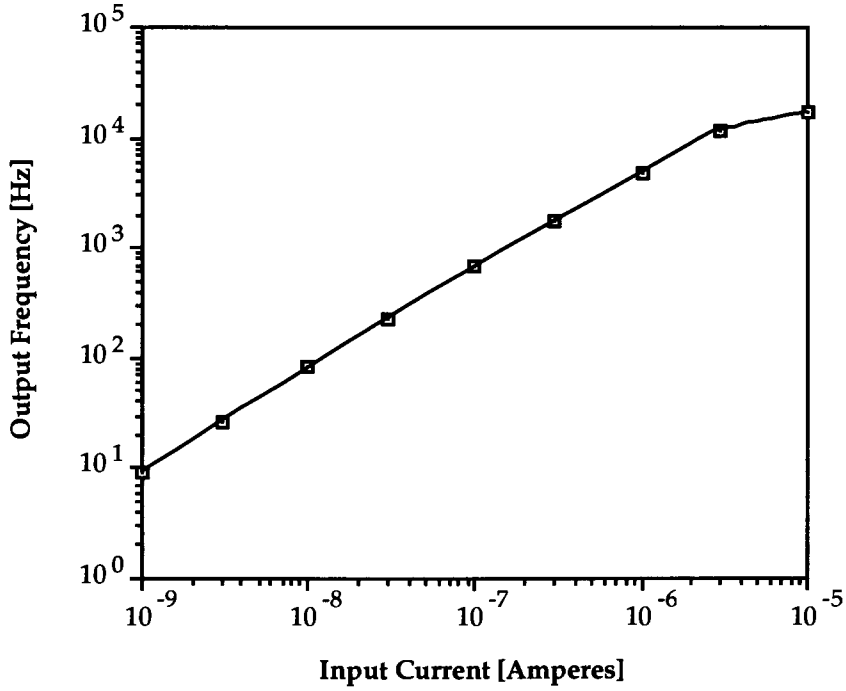

Figure 4.11: Frequency Response of One Input ICO

The above designs have a number of advantages over the standard ring oscillator designs. Firstly, the number of matched devices has been reduced or limited to matching between two devices. As well, most of the transistors except the current mirrors may be minimum size allowing for very small

designs. As well, the two-input ICO design has the ability to encode two analog signals into a single digital signal.

4.3 Sigma-Delta A/D Converters

A form of analog-to-digital conversion based on time-domain encoding is known as sigma-delta ($\Sigma\Delta$) modulation. Basically, a $\Sigma\Delta$ modulator digitizes an analog signal with a very low resolution (1 bit) at a very high sampling rate. By using oversampling and filtering techniques, the effective resolution of the A/D converter is increased. In general, these converters are insensitive to circuit imperfections and component mismatch since they employ only a simple one-bit quantizer [51,52,53]. For this reason, a large number of $\Sigma\Delta$ designs have been presented in the literature for various applications [19,54,55].

While the theory behind oversampling converters is complex, the basic concepts are not. By oversampling an analog signal, the noise energy generated by the digital quantization is spread out as shown in Figure 4.12. Therefore, most of the noise lies outside the bandwidth of the input analog signal, thus increasing the dynamic range of the converter. By employing feedback techniques, the noise spectrum may be shaped so that even more of the noise energy lies outside the desired bandwidth without increasing the sampling frequency. This noise shaping is precisely what a $\Sigma\Delta$ modulator does.

To recover the original signal from the $\Sigma\Delta$ modulator output, the digital signal must be low-pass filtered. This removes the quantization noise in the higher frequencies. Depending on the application, a low-order analog filter may be used. However, digital filtering techniques are now becoming

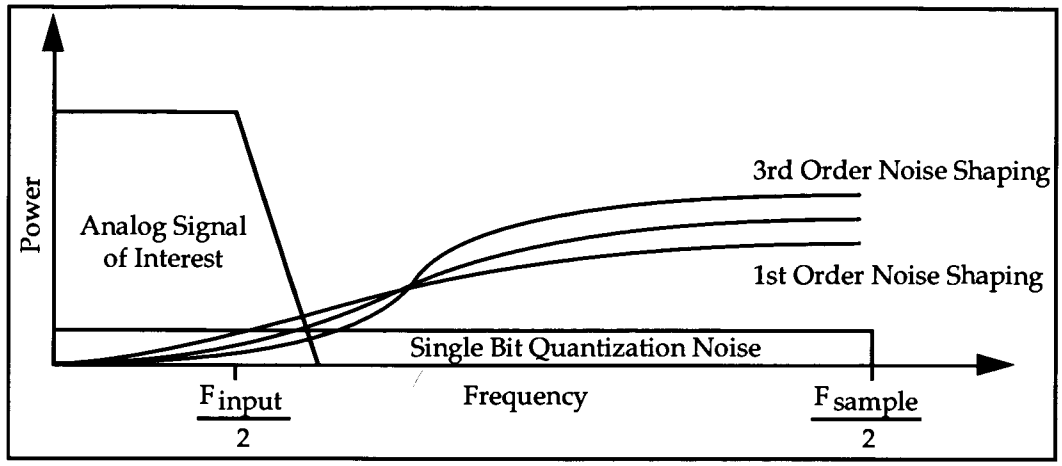

Figure 4.12: Simplified Oversampling Frequency Spectrum

popular as the resulting filtered signal remains in a form readable by a computer. A number of chips that perform these dedicated tasks exist on the market [56].

The simplest form of A/D converter uses a first-order ΣΔ modulator shown in Figure 4.13. However, most of the research presented in literature has been for higher-order modulators due to the large oversampling frequency ratios required for lower-order loops. For example, a dynamic range of 13 bits is achievable with a third-order modulator operating an oversampling frequency 32 times the input signal's bandwidth. A first-order

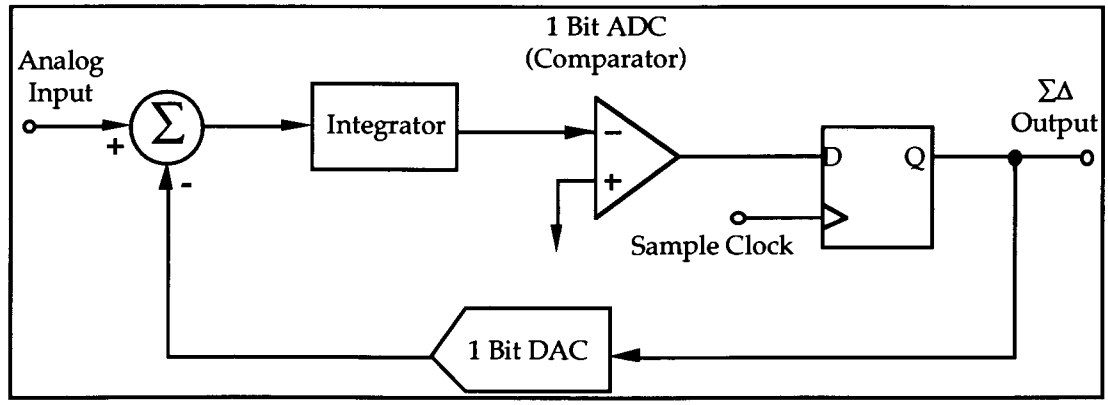

Figure 4.13: Block Diagram of a First Order ΣΔ Converter

modulator requires an oversampling frequency approximately 750 times the input bandwidth to achieve the same resolution. Unfortunately, higher-order modulators are difficult to design and suffer from stability problems [51].

While the higher-order $\Sigma\Delta$ modulators are useful for high-speed applications, lower-order modulators may be used for transducer systems as the input bandwidth requirement is relatively small. For example, a transducer, whose output bandwidth is less than 1kHz, may be oversampled at 1MHz or even 10MHz. Since this represents an oversample ratio greater than 750, a first-order $\Sigma\Delta$ modulator may achieve over 13 bits of dynamic range. Thus the first-order modulator is desirable over higher-order designs as it is easier to design and will occupy less chip area.

A very simple first-order $\Sigma\Delta$ modulator is proposed in Figure 4.14. While this design is similar to the circuits presented in the previous section, the function of the components are slightly different. The storage capacitor C acts as an integrator for the current difference at that node. The digitally controlled NMOS current mirror performs the 1-bit D/A conversion while the digital inverter is the 1-bit A/D converter. The modulator is designed so that the reference current represents the middle of the modulator's operating range. Therefore, if the input current is equal to the reference current, the output waveform of the modulator has a 50% duty cycle.

The exact performance of the circuit depends on the sampling rate, the integrator time constant and the reference current. The integrator time constant is set by the reference current and the value of the storage capacitor C. Thus the noise shaping function of the modulator will vary if the reference current is used to correct large variations in transducer

characteristics. While the sampling rate does not have to be accurate, it must be stable in order to prevent detrimental idling patterns and tones [56].

The circuit shown in Figure 4.14 was simulated using SPICE as the design has not be received from fabrication. Figure 4.15 shows a simulation of the circuit in operation. The maximum input current is twice the input reference current. Additional work must be performed to fully characterize the modulator and determine the limitations of the concept.

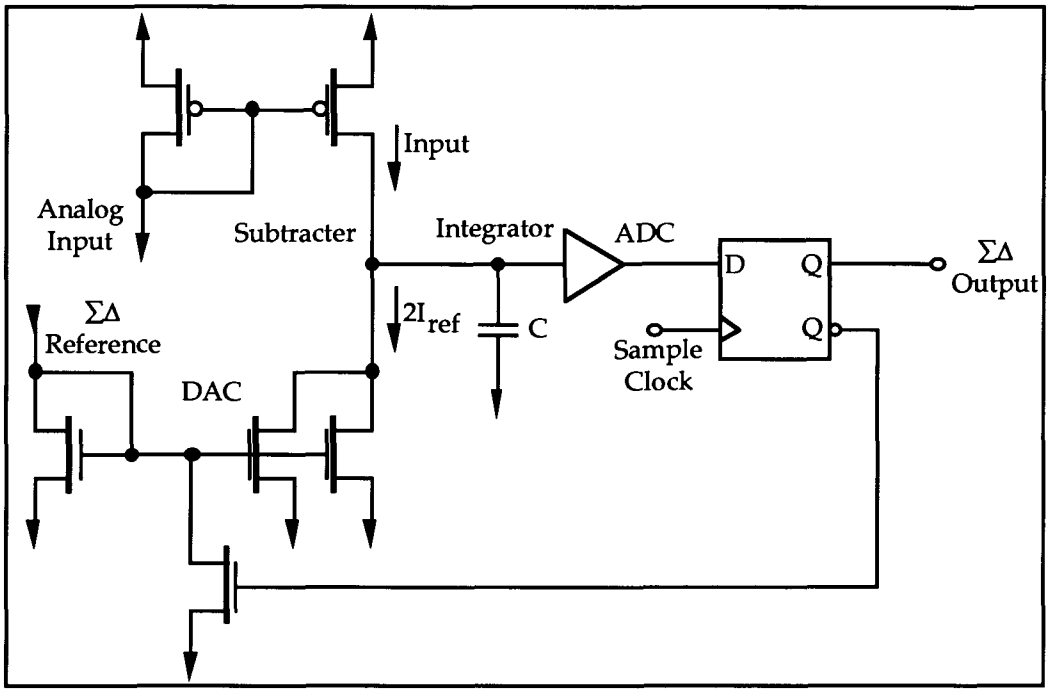

Figure 4.14: Proposed Current-Mode First-Order ΣΔ Modulator

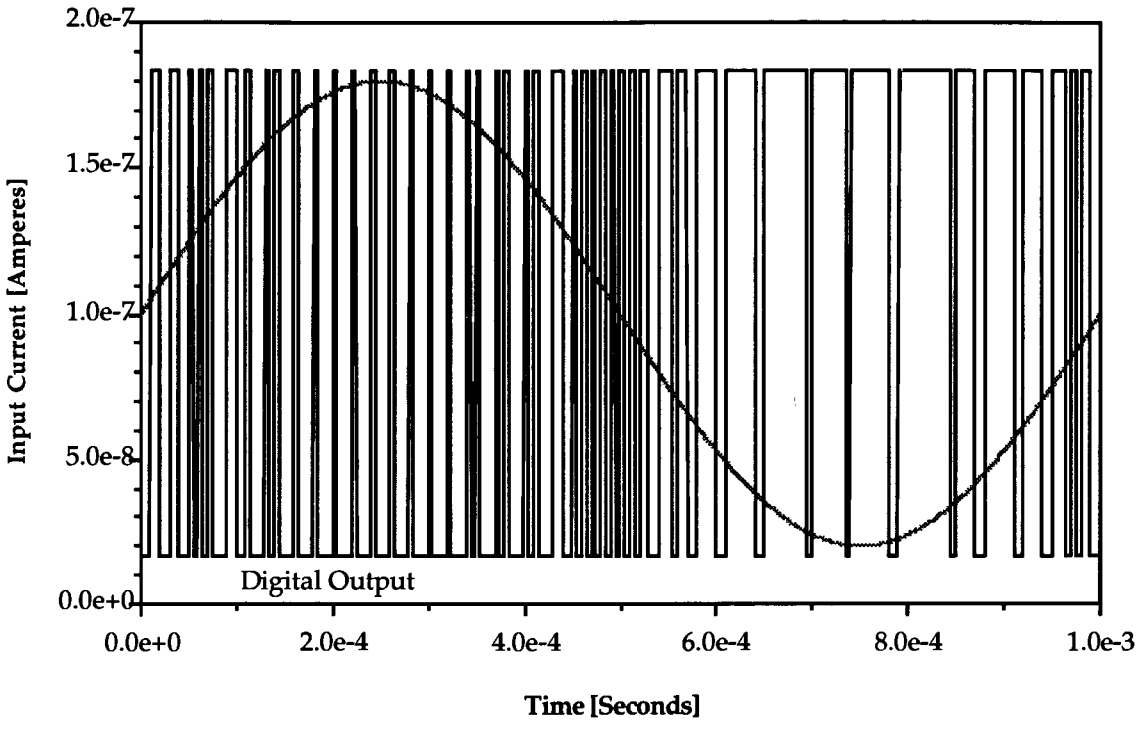

Figure 4.15: First Order $\Sigma\Delta$ Modulator HSpice Simulation Results

5 Examples of Integrated Transducer Systems

The circuits developed to date have been used in the design of integrated transducer systems. The first system is the visual-to-thermal converter (VTC) cell which integrates two transducers with the A/D converters presented in Chapter 3. The second system looks at using the ICO presented in Chapter 4 to convert the current output of a split-drain MOSFET magnetic sensor into digital form.

5.1 Visual-to-Thermal Converter Cell

A single VTC cell, which was introduced in Chapter 3, converts the incident visible light into a proportional amount of thermal radiation [24]. Its implementation in silicon integrates two different transducers plus associated electronic circuitry. The main components of the cell are: a photodetector sensitive in the visible light range, an A/D converter, memory and a thermal radiation emitter (thermal pixel) with its driver. Figure 5.1 shows the basic schematic of the VTC cell.

The photodetector produces a current proportional to the power density of the incident light. This current is converted by the A/D converter into a digital signal, which is stored in local memory. The digital signal controls the operation of the pixel driver, which controls the current through the thermal emitter, converting electric current into thermal energy. The amount of emitted thermal energy can be made proportional to incident visible light intensity. The possibility exists to use the A/D converter's reference signal to shift its linear range of operation over a few decades to

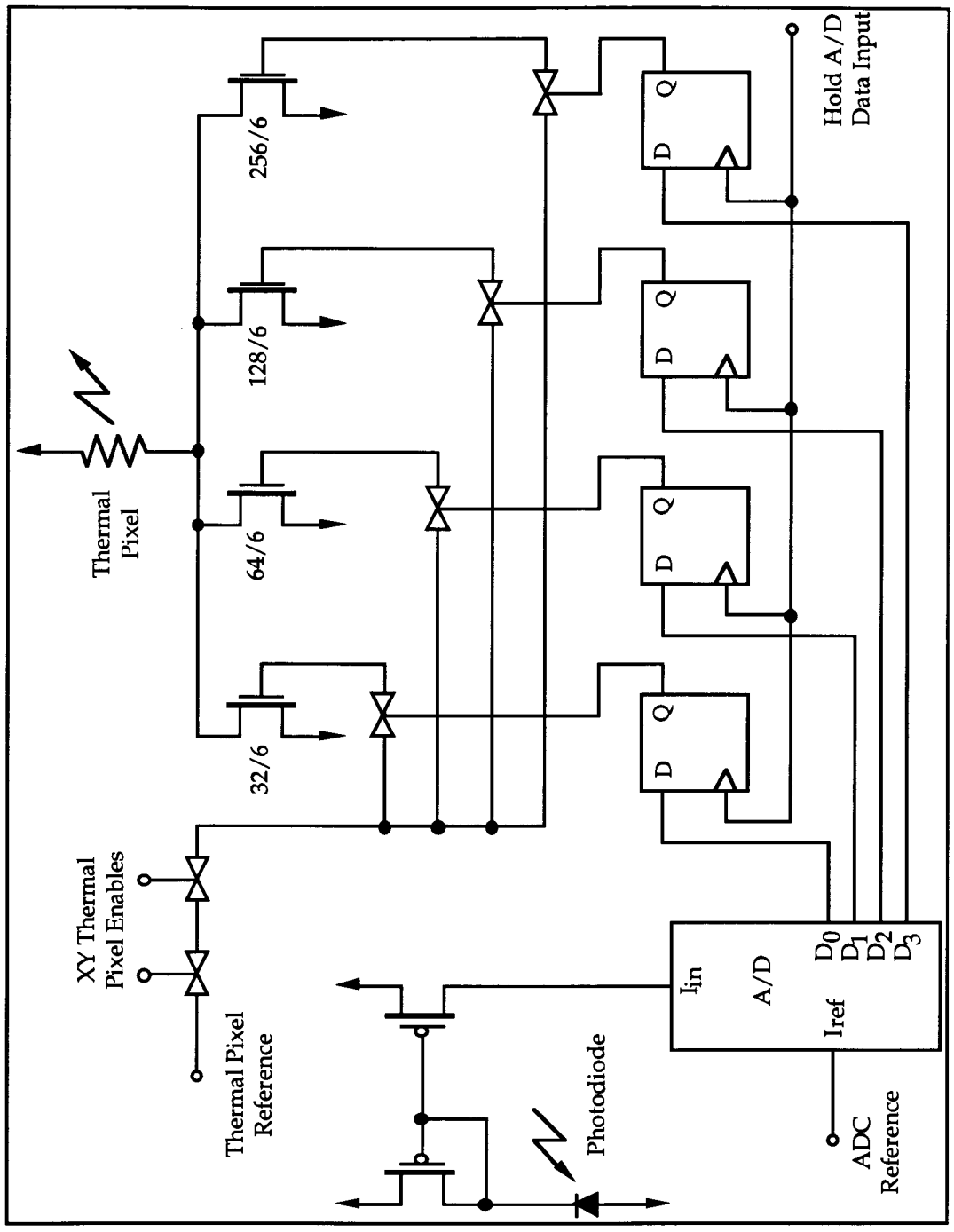

Figure 5.1: Visual-to-Thermal Converter Cell Schematic

select a desired range of light intensities and to compensate for non-uniformity of the photodetector response's in various VTC cells.

Many different types of CMOS photodetectors may be used such as photodiodes [57] and vertical phototransistors. Vertical phototransistors are more sensitive than diodes, but their characteristics are not as linear as those of diodes due to current drain degradation in the very low light intensity range. Variable-sensitivity photodetectors with a controllable mode of operation [7] can also be used for the VTC to cover a large light intensity range.

Both VTC cells presented here have been designed and fabricated using the digital 3μm CMOS process available from Northern Telecom. The CMOS fabrication process was followed by a CMOS-compatible anisotropic etching [8] that created a high thermal isolation necessary for thermal pixel operation. The circuits were then measured and their performance evaluated.

Figure 5.2 shows a photomicrograph of a 4 bit A/D converter using pipelined signal conversion integrated with a photodiode, thermal pixel and control circuitry. This design forms one VTC cell occupying 1400μm by 740μm and performs the image processing for a single pixel of an image.

Figure 5.3 shows a photomicrograph of the same visual-to-thermal cell except a 4 bit A/D converter using parallel signal conversion is used. This design forms one VTC cell occupying 1250μm by 740μm and also performs the image processing for a single pixel of an image.

Measuring the performance of the VTC cells was performed in a piece-wise manner in order to simplify the task. Instead of trying to illuminate the cell with a calibrated light source and measure the emitted thermal energy, each section of the VTC cell was measured separately. The photodiode used

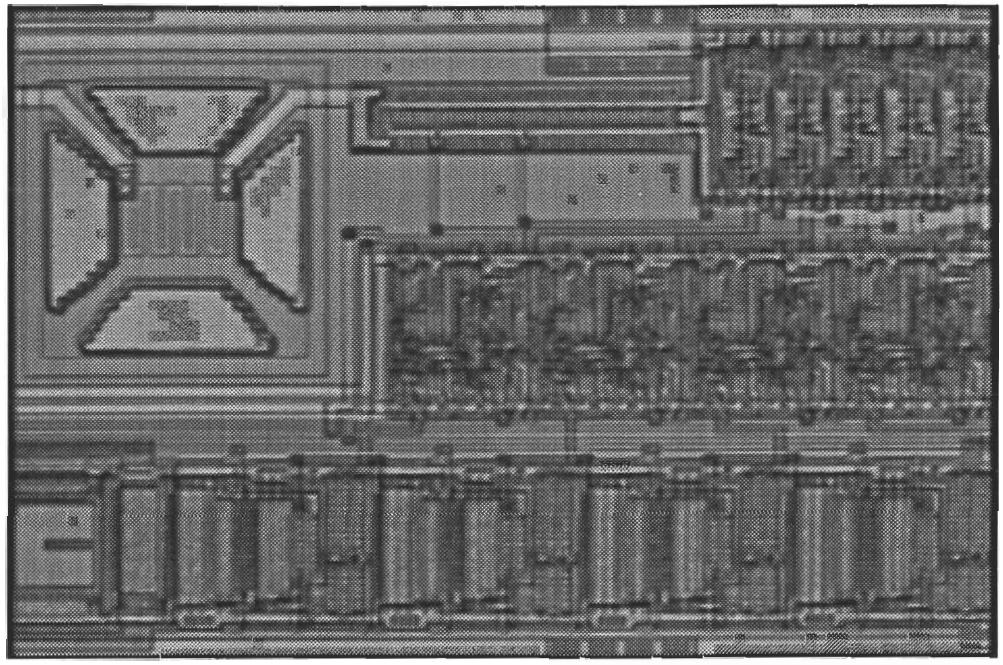

Figure 5.2: Visual-to-Thermal Converter Cell using Pipelined A/D Converter

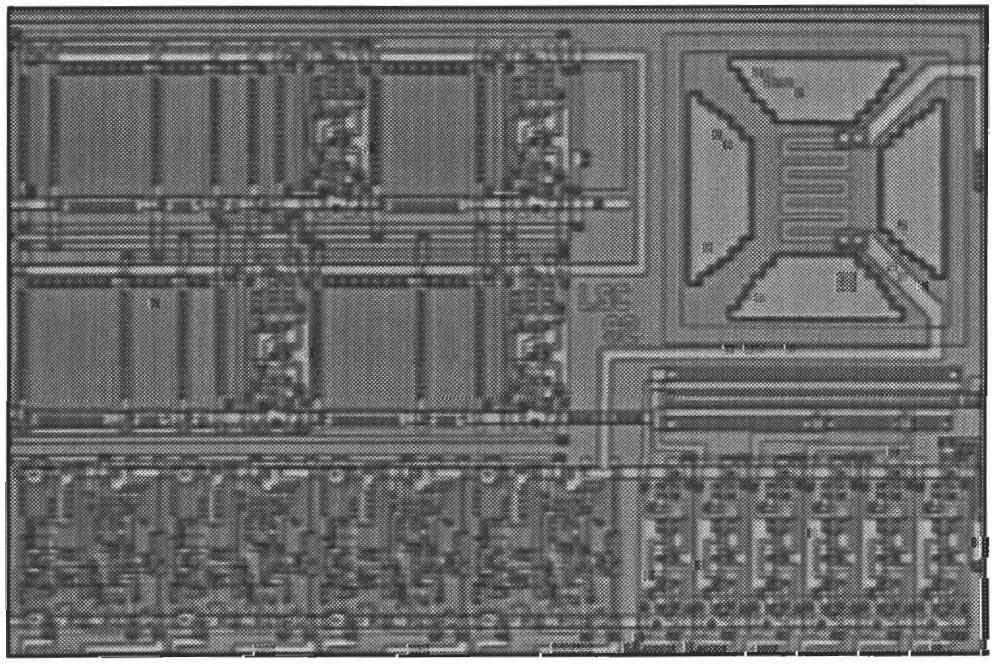

Figure 5.3: Visual-to-Thermal Converter Cell using Parallel A/D Converter

for these designs were characterized in the literature [7]. All circuitry was measured using a HP Semiconductor Parameter Analyzer (SPA).

The characterization of the thermal pixels were a problem as the equipment to measure them is not available at Simon Fraser University. However, their temperature can be estimated using the change in the polysilicon heater's resistance and the temperature coefficient of polysilicon [58]. Some experimentation was performed on thermal pixel test structures to characterize their uniformity and performance [59] using a donated Hammamastu infrared camera. Figure 5.4 shows an enhanced video capture, from the infrared camera, of an image generated using an 8x8 array of these test structures. Unfortunately, absolute temperature measurement of thermal pixel response was not possible with the camera.

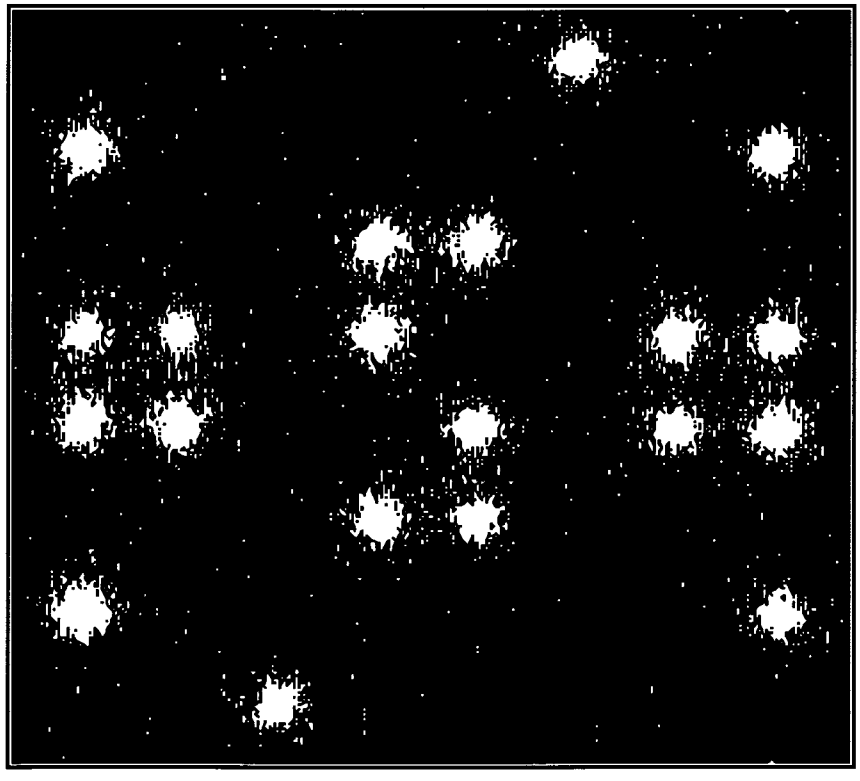

Figure 5.4: Infrared Camera Video Capture of Thermal Pixel Array

All the results were combined to form the estimated VTC cell response shown in Figure 5.5. The curve is not linear as the temperature is proportional to the resistive power dissipation, I^2R, resulting in the thermal radiation intensity varying approximately with $I^{0.5}$. In reality, thermal losses due to non-ideal thermal isolation between the polysilicon heater and the substrate make the above relationship more complex [60].

Arrays of VTC cells have been fabricated to explore thermal scene simulator design issues such as defect avoidance using redundancy to improve array yield and power distribution [24,61]. Figure 5.6 shows a photomicrograph of one such test array structure which uses laser links for defect avoidance. From the picture, we see that the data buses with their respective laser links, which connect the A/D converter to the data latches and thermal pixel controllers, take a significant amount of die area. In this

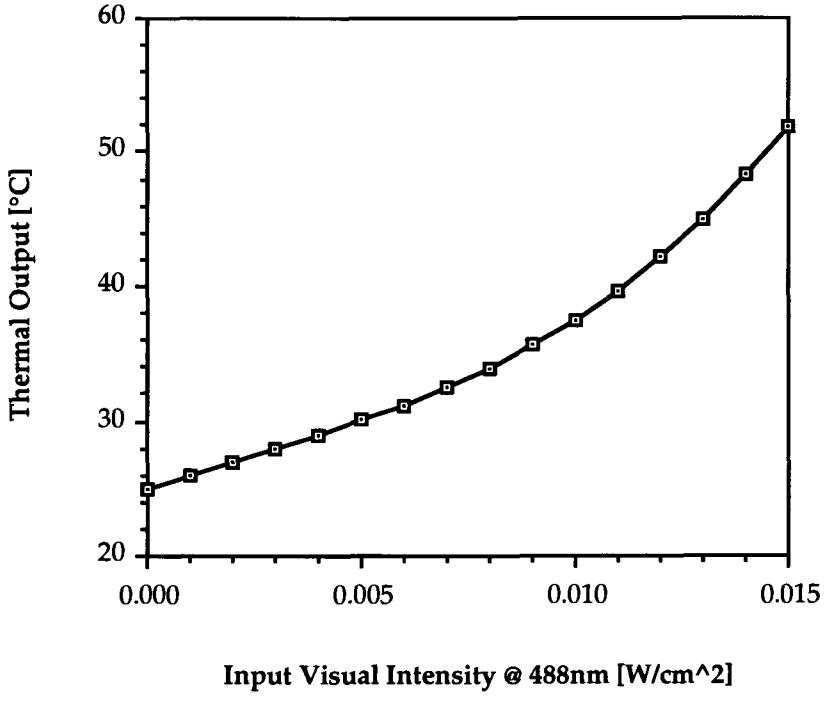

Figure 5.5: Visual-to-Thermal Converter Cell Response

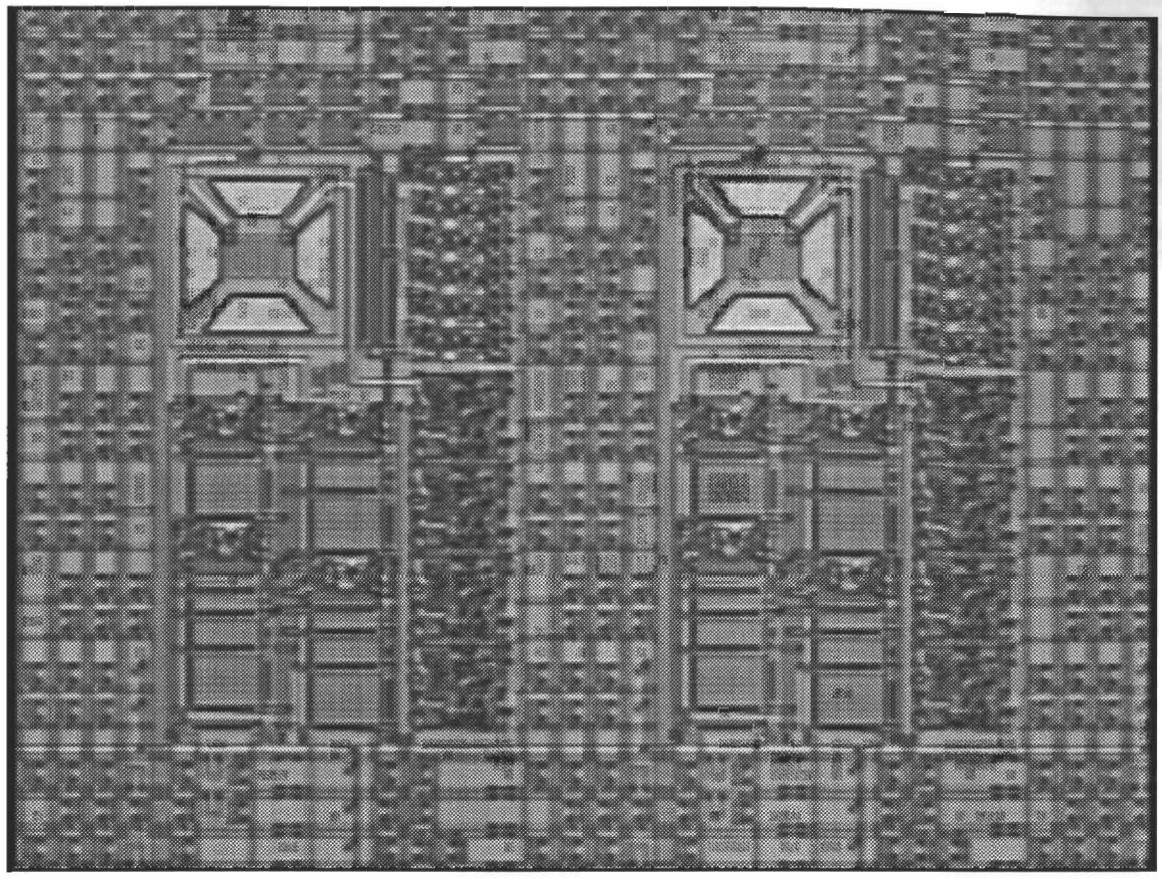

Figure 5.6: Test Array of Visual-to-Thermal Converter Cells

case, the VTC cell uses approximately 45% of the die area with the remaining 55% being used by the data bus/laser link structures.

While this test array was kept simple for easier debugging and experimentation of various redundancy schemes, it does point to a problem with the overall size of the VTC cell. With this design, a 140x40 array of VTC cells could be constructed on an 8 inch wafer. However, this does not take into account the die area required for defect avoidance. As well, we would expect that increasing the resolution of the A/D converters would increase the size of the VTC cell and the interconnection data buses, reducing the maximum array size.

A different approach to the implementation of the VTC cell may be required to solve some of the area requirements of the current designs. One method is to use some of the A/D conversion techniques presented in Chapter 4. Since the pixel's thermal inertia causes the thermal pixel to respond similar to a low-pass filter, the possibility exists that a form of pulse-width or $\Sigma\Delta$ modulation could be used to control them. Thus, a current-domain $\Sigma\Delta$ modulator combined with a photodetector, thermal pixel and additional circuitry would implement a smaller VTC cell with increased resolution. However, pulsing large currents through the thermal pixels may cause power distribution problems in VTC array applications. Further work must be done in this area.

5.2 Magnetic Field Sensor Cell

A CMOS compatible magnetic sensor is the split-drain MOSFET known as the MAGFET [62,63]. This device is a large rectangular channel MOS transistor with two separate drain connections. A magnetic field perpendicular to the silicon surface creates a difference in the two drain currents due to the Lorentz force effect on the charge carriers. This difference changes linearly with the magnetic field strength. The measured current difference can reach 0.3% at 800 gauss [62] or as high as 50μA [63] depending on the design.

An interface circuit which converts the current difference into useful digital information is desirable. However, calculating the two drain currents using current mirrors is not advisable due to subtraction errors as discussed in Section 3. These errors would limit the minimum magnetic field that could be measured using the MAGFET. On the other hand, converting each drain current into digital form would require two separate A/D converters

wasting chip area and power. Obviously, a method that processes the drain signals while converting them into a digital signal is desired.

The ICO presented in Chapter 4 provides a possible solution to this problem. The basic ICO design has two current-mode analog inputs which determine both the frequency and the duty cycle of the oscillator. Thus, both drain currents from the MAGFET may be used to control the oscillator. Figure 5.7 shows the proposed interface circuit connected to a split-drain MAGFET. This design uses very little analog circuitry as it combines the MAGFET with the ICO using only one current mirror and a capacitor.

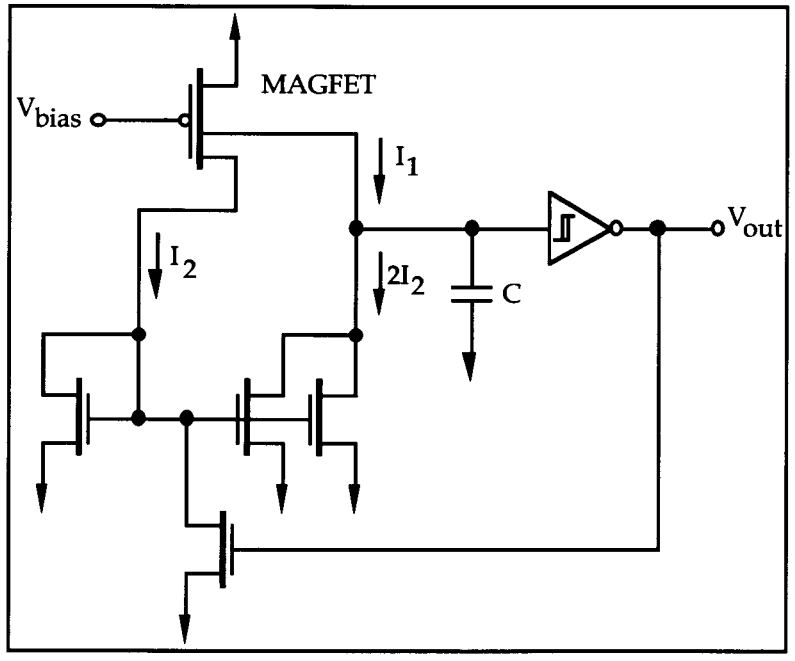

Figure 5.7: Schematic of Magnetic Sensor with Frequency Encoded Output

From the equation developed in Section 4, we see that the duty cycle of the oscillator would be dependent on the ratio of the MAGFET drain currents. If the MAGFET is not exposed to a magnetic field, the oscillator output should have a 50% duty cycle. Exposing the design to a magnetic field should cause the output duty cycle to increase or decrease. In order to relate the oscillator's

duty cycle to change in drain currents, the oscillator's input currents I_1 and I_2 are defined as I_{bias}-ΔI_{mag} and I_{bias}+ΔI_{mag} respectively where I_{bias} is the average MAGFET drain current and ΔI_{mag} is the change in MAGFET drain current due to the magnetic field. The oscillator's duty cycle can then be written as

$$\text{duty cycle} = \left\{\frac{1}{2} - \left(\frac{I_{bias}}{\Delta I_{mag}} + 1\right)^{-1}\right\} 100\ \% \qquad (5.1)$$

Therefore, the duty cycle would provide all the information necessary to calculate the ratio $\Delta I_{bias}/I_{mag}$ which is proportional to the magnetic field strength. Extracting the ratio from the duty cycle is a very simple task for a computer.

An important feature of using the duty cycle to calculate the magnetic field strength is that the duty cycle should be insensitive to circuit variations such as the MAGFET, capacitor or Schmitt trigger. This insensitivity should make the design perfect for array applications where such variations are expected. By adding an AND gate and a transmission gate to the design, the outputs of each ICO/MAGFET transducer cell could be multiplexed on a single bus wire. Further work must be done in this area.

Unfortunately, this design was developed very late in the thesis and exists only as a simulation. Hopefully, a design will be submitted in the next BiCMOS or CMOS fabrication run to verify the concepts presented here.

6 Conclusions

6.1 Summary

The research results presented in this thesis are the first steps towards the design and fabrication of integrated transducer systems. Among the many possible issues to be solved, we focused on the design of the signal conditioning/processing circuitry using current-mode design techniques.

Current-mode analog circuit design techniques were discussed with attention on using digital IC processes for analog signal processing. The modeling of MOS transistor characteristics were reviewed. A number of circuit alternatives to improve accuracy and dynamic range performance of analog circuits were presented. Finally, a review of the possible layout and circuit guidelines to improve device matching for analog design. A test of the effectiveness of the guidelines for current mirrors was presented.

Two different CMOS A/D converters for current-domain operation were developed and compared. They provide a simple, but effective A/D converter solution for use in applications where size and power consumption are important over a very wide range of input current from the transducer. A design allows for compensation of non-linearity of the transducer's characteristics. However, both designs suffer from potential problems with current mirroring due to limitations of the digital CMOS technologies.

Another approach of converting analog signals into digital form using time-domain encoding was explored. These methods allow the analog signal to be transmitted over a single wire with high resolution. Current-controlled

frequency and sigma-delta encoding circuits were presented with small size, low power and versatility being key design criteria.

Two examples of integrated transducer systems were presented. The first example was a CMOS-compatible visual-to-thermal converter cell which transforms input visual radiation to a corresponding output level of thermal radiation. The converter cell integrates two transducers: a photodiode and thermal pixel with an analog-to-digital converter and pixel driver circuitry. The other example proposed the application of a oscillator based interface circuit for a MAGFET based magnetic sensor. In this case, the design would perform subtraction and ratioing operations while remaining insensitive to process variations.

The ability to integrate interface electronics with CMOS compatible transducers on a single substrate is powerful. Combined with the emergence of new transducers and IC processes, this research should form a starting point in developing integrated transducer systems for unexplored applications.

6.2 Future Work

The potential of integrated transducer systems has not been ignored by industry. Researchers and manufactures such as Analog Devices and Dallas Semiconductor are starting to develop intelligent signal conditioners devices for use with sensors [22,56]. The circuitry in these devices include blocks such as amplifiers, signal multiplexers, A/D converters and small microprocessors. They provide functions such as data scaling, linearization and monitoring that can be controlled over a computer interface. However, they have not integrated transducers on the chips yet.

Efforts are underway by the National Institute of Standards and Technology (NIST) and the TC-9 Committee of the Institute of Electrical and Electronics Engineers (IEEE) to define the requirements and potential benefits of a smart-sensor interface standard [64]. The first phase of this project was a Smart Sensor Interface Standard workshop held the end of March of this year. Topics include the establishment of general communication-protocol and data-transfer formats, selection of several hardware implementations and development of a public-domain library for them. All final phases results in a completed standard are expected to be finished in the next few years.

The advantage of the research being performed at Simon Fraser University has been in the area of CMOS-compatible transducer technology. By exploring concepts such as transducer arrays and intelligent transducer system, the results may be marketable.

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