MODELING LEAKAGE IN SUB-MICRON CMOS TECHNOLOGIES

by

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ABSTRACT

As CMOS technology scaling continues, subthreshold leakage current increases dramatically. A significant percentage of the total chip power is due to leakage, also known as static power. Accurately estimating static power in early stages of design is an important step for developing power efficient products.

Leakage current is an important segment of total supply current (I_{DDQ}), which is used as a means to identify defective chips. I_{DDQ} value is determined by the sum of leakage currents of those transistors that can leak. Setting I_{DDQ} value too high or low will result in excessive shipment of defective chips or yield loss because of rejecting good parts, respectively.

The goal of this work is to investigate and model leakage mechanisms in submicron CMOS technology using SPICE circuit simulators. The main focus of this research will be subthreshold and reverse-bias p-n junction band-to-band leakage mechanisms and the effect of transistor parameters on them.

DEDICATION

To my love and husband, Ali, for his unconditional and never-ending love, support, and patience

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1 INTRODUCTION

The need for lower power consumption and higher circuit densities has made it necessary to scale down supply voltage in CMOS logic circuits. To maintain the circuit speed, threshold voltage should also scale down with the supply voltage. This results in leakage current increase (See Figure 1); and hence, the leakage power increases with each technology node. If this trend continues, leakage power will soon be in the same order as the dynamic power (See Figure 2). Estimating leakage power in early stages of VLSI circuit design is important for optimizing the total power dissipation [1].

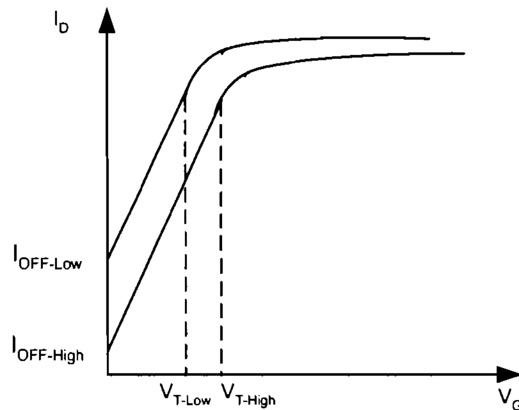

Figure 1: Threshold Voltage Scaling and Increase in OFF Current for a Given Technology [2]

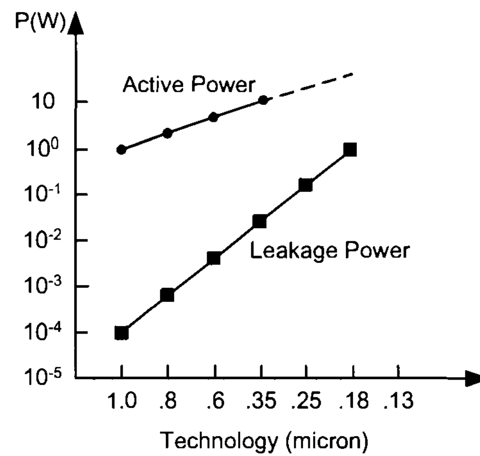

Figure 2: Technology Scaling and Leakage Power Increase [2]

Leakage current is also an important factor in setting total supply current (I_{DDQ}) value, which is used as a pass/fail threshold for testing chips. Setting this value too high would cause some defective chips to be considered non-defective; similarly if this value is set too low, functional chips may be considered defective. I_{DDQ} consists of two parts, the current due to parametric failure and the current due to catastrophic failure. The parametric failure results in increased power supply current flow. Increasing leakage current due to the technology scaling has reached or even passed the value of current associated with parametric failure; this makes it more difficult to identify defective chips [3].

All these have made researchers investigate ways to control and reduce leakage current in submicron CMOS technologies. Two major categories for reducing leakage are design-time, and run-time techniques. In [4] each of these techniques are explained. For Design-Time Technique, use of Dual-Threshold CMOS is described; where, transistors with low threshold voltage (V_{TH}) are used in critical paths and high V_{TH} transistors for

non-critical paths. For Run-Time technique, methods such as the use of transistor stacks, sleep transistors, forward and reverse body biasing, and dynamic V_{TH} scaling are depicted.

There are several leakage sources in a MOSFET. Based on the transistor feature size some of these leakage currents have higher values and therefore greater impact on circuit performance than others.

In this report a number of leakage mechanisms will be studied. The impact of important model parameters on leakage currents will be considered. SPICE simulation will be performed on a MOS transistor in 0.35, 0.18, and 0.13 micron technology generations. Leakage current comparison between a simulated transistor and a measured one will be conducted, where applicable, followed by the conclusion.

2 LEAKAGE MECHANISMS

There are several parameters influencing the off current of a MOS transistor. Threshold voltage, channel/surface doping profile, gate oxide thickness, channel physical dimensions, drain/source junction depth, and V_{DD} all have some effects on the OFF current. There are several leakage mechanisms contributing to the OFF current of a MOS transistor in short channel devices. The dominating leakage mechanism depends on device size, channel dimensions, operating conditions, technology node, and other transistor parameters.

As the transistor channel length shortens, power supply of transistors needs to be decreased and hence the threshold voltage. Since the weak inversion state leakage is a function of threshold voltage, the OFF current of transistor increases. Increasing drain voltage results in widening drain-channel depletion region and therefore drain current increases significantly. The increase of the OFF current is due to the current on the channel surface, which is caused by drain-induced barrier lowering (DIBL) or deep channel punch-through currents. The threshold voltage and OFF current are both dependant on the width of the transistor. As the width of the transistor decreases, these two parameters get modulated and this gives rise to narrow-width effect. These undesirable effects are called short channel effects (SCE).

To keep SCE under control, the gate oxide thickness needs to be reduced with channel length scaling, which will result in considerable amount of current flowing through the gate oxide of the transistor because of the high electric field. This means that

the input impedance of MOS transistors can't be considered infinite anymore and the circuit performance will be seriously degraded. The two major components of gate leakage current are injection of hot carriers from substrate to the gate oxide and gate oxide tunnelling.

Depletion of the carriers at the drain surface right below the gate-drain overlap causes another leakage current called gate-induced drain leakage (GIDL). All of the above leakage mechanisms are illustrated in Figure 3 [5].

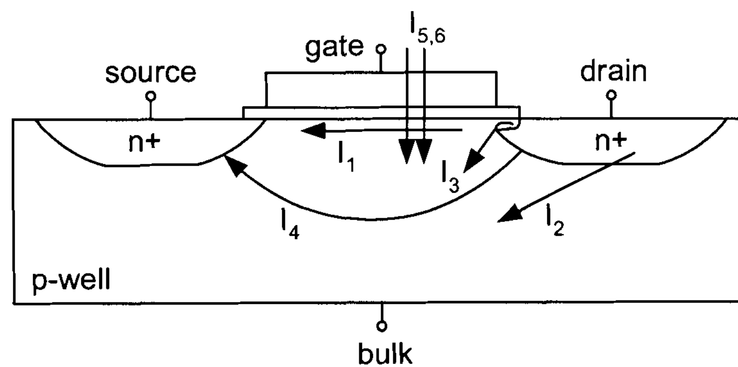

Figure 3: Leakage Mechanisms in Sub-micron CMOS Transistor [5]

I_1: Sub-threshold leakage

I_2: Reverse-bias pn junction leakage

I_3: Gate-induced drain leakage

I_4: Channel punch-through leakage

I_5: Oxide tunnelling leakage

I_6: Hot carrier injection gate leakage

In the following sections each one of these leakage mechanisms will be briefly explained.

2.1 Subthreshold Leakage

Subthreshold leakage in a MOS transistor is caused by several phenomena, which are described in the following sections.

2.1.1 Weak Inversion Effect

Weak inversion happens when the gate voltage is below threshold voltage. In this mode the minority carrier concentration in the conduction channel is low but not zero. The drain-substrate voltage drops entirely across the substrate-drain pn junction, which is reverse biased. Since both the longitudinal electric field and the number of mobile carries are small, the diffusion current dominates. This is one of the components of the subthreshold current [5].

2.1.2 Drain Induced Barrier Lowering (DIBL)

DIBL happens when source and drain depletion regions interact with each other close to the channel surface. High drain voltage in a short channel device lowers the source barrier height and hence decreases the threshold voltage. As a consequence the source injects carriers into the channel surface. Gate voltage does not have any effect on this phenomenon. As the channel length decreases and the drain voltage increases, DIBL effect becomes more and more significant [5].

2.1.3 Body Effect

When the well-source junction in a MOS transistor is reverse biased, the bulk depletion region widens and this increases the threshold voltage. The increase in threshold voltage causes the leakage current to decrease [5].

2.1.4 Narrow Width Effect

Narrow width of a MOS transistor modulates the threshold voltage and the leakage current in 3 different ways.

The fringing field of the gate causes the gate-induced depletion region to extend outside the channel width and consequently to increase the total depletion charge of the bulk region. This increases the threshold voltage.

The channel doping is higher along the width of the local oxide isolation gate. Because of the channel stop, the dopants invade under the gate. This means that there is need for higher voltage to invert the channel.

The third effect is called inverse-narrow-width effect. In this case the depletion layer cannot extend under the oxide isolation; so the depletion charge in the bulk doesn't rise. But, because of the field induced edge-fringing effect at the gate edge, an inversion layer at the gate edges forms at lower voltage than at the centre. And the overall gate capacitance increases because of the sidewall capacitance; and therefore, the threshold voltage decreases [5].

2.1.5 Effect of Channel Length

In short channel transistors, the drain and source depletion regions are in a near proximity of each other. They enter more into the channel length and as a result part of the channel gets depleted. Consequently, less gate voltage is needed to turn the transistor on. This means that the threshold voltage is lower for the short channel transistor and subthreshold current is higher [5].

2.1.6 Temperature

It has been observed that subthreshold leakage is temperature dependent. This is due to the linear increase of subthreshold slope and decrease of threshold voltage with temperature [5].

2.2 Reverse-bias pn Junction Leakage

There are two components in a reverse bias pn junction leakage current: Minority carrier diffusion/drift close to the depletion region, and electron-hole pair generation in the depletion region. Since source-to-well and drain-to-well junctions are usually reverse biased, the above leakage mechanisms are observed in the MOS transistors. This leakage current is dependant on doping concentration and junction area. If the doping concentration of both p and n regions are high, a leakage mechanism called Band-to-Band Tunnelling (BTBT) dominates the pn junction leakage.

BTBT occurs when electrons from the valance band of the p-region tunnel to the conduction band of the n-region when a high electric field is established across the pn junction. The electric field should be greater than 10^6 V/cm. High doping concentration and sharp doping profile in scaled devices increases BTBT current through the drain-bulk junction [5].

2.3 Gate-induced Drain Leakage (GIDL)

When the drain of the MOS transistor is at V_{DD} and the gate voltage is zero or negative, the n+ region below the gate can be depleted or inverted. This increases the electric field and therefore effects such as BTBT can occur. Minority carriers beneath the gate will be emitted into the drain. Lower potential of the substrate makes the minority

carriers in the drain depletion region below the gate to move to the substrate. Low oxide thickness and high V_{DD} increases the electric field and therefore GIDL. Moderate drain doping makes GIDL worse, since both the electric field and depletion width are significant [5].

It has been observed that temperature has also an affect on GIDL. This is due to the fact that the band gap (E_{gap}) is temperature dependent. Reduction in oxide thickness means that the electric field at the drain-gate overlap region increases, which results in an increase of GIDL. Also depletion layer width decreases as the drain doping concentration increases; so the electric field at the depletion layer is higher. This results in carrier generation (band-to-band tunnelling effect) and an increase in GIDL [6].

2.4 Channel Punch-through Leakage

Decreasing channel length causes the depletion regions of drain and source to get closer to each other. Increasing V_{DS} also forces the two depletion regions closer together. When the two depletion regions merge, punch-through has taken place. In this state, majority carriers in the source overcome the energy barrier and enter the substrate, where some of them get collected by the drain [5].

2.5 Oxide Tunnelling Leakage

Gate oxide thickness reduction with technology scaling has resulted in an increase in the electric field across the oxide. Electrons can tunnel through the oxide from gate to substrate or vice-versa. This leakage mechanism can be further divided to two parts: Fowler-Nordheim (FN) tunnelling where electrons tunnel to the conduction band of the oxide layer; and direct tunnelling, where electrons tunnel directly through the silicon

oxide layer. This happens when the thickness of oxide is less than 3-4 nm. There are three mechanisms for direct tunnelling: electron tunnelling from the conduction band (ECB), electron tunnelling from the valance band (EVB), and hole tunnelling from the valance band (HVB). Since holes have to overcome higher barrier height than electrons, the tunnelling current resulted from HVB is smaller. Hence, the gate leakage current in PMOS is lower than NMOS [5].

2.6 Hot Carrier Injection Gate Leakage

This leakage occurs due to the high electric field near the Si-SiO_2 interface. Electrons and holes can gain enough energy to overcome the potential barrier at the interface and enter the oxide layer. Electrons are more likely to enter the oxide since they have a lower effective mass and the barrier height for electrons (3.1 eV) is less than that for holes (4.5 eV) [5].

3 PARAMETER DEPENDENCE OF LEAKAGE

Looking at the definition of each of the leakage mechanisms discussed in the previous section, it is apparent that different leakage currents are dependent on one or several transistor parameters. Table 1 summarizes these mechanisms and the parameters they depend on. Altering each of these parameters will vary the value of one or more of these leakage mechanisms.

Table 1: Parameter Dependence of Leakage Currents

Leakage Current	Parameter
Subthreshold	V_{TH}, L, W, T, V_{GS}, T_{OX}
BTBT	n & p regions doping concentration, Junction area, V_{DD}
GIDL	T_{OX}, V_{DD}, Drain doping concentration, T, Band gap energy
Channel Punch-Through	L, V_{DS}
Oxide Tunnelling	T_{OX}
Hot Carrier Injection	V_G, T_{OX}

Among these parameters some have more influence on leakage currents than others. Also in deep submicron CMOS technologies, other parameters that are not listed

in Table 1 come into play, such as, V_{FB} and N_{pocket}. N_{pocket}, also known as halo doping, is a non-uniform p+ doping in the source-body and drain-body boundaries which is used in advanced MOSFETs to get better short channel effects [7]. In [8] it is shown that BTBT is more sensitive to N_{pocket} and V_{DD} variations and subthreshold current is more sensitive to V_{FB}, T_{OX}, and N_{pocket}.

In chip fabrication, the within-die process variation of 10-20% is nominal, this means that each of the above parameters may vary within 10-20% from batch to batch. In [9] it is shown how 10-20% variation in channel doping, oxide thickness, and effective channel length fluctuates the leakage current. This is very important observation that needs to be considered both at design stage for static power estimation and at test stage for setting I_{DDQ} value.

4 SPICE SIMULATION OF SUBMICRON LEAKAGE

For the simulation, Cadence™ software tool was utilized. The technology files were those of Taiwan Semiconductor Manufacturing Company (TSMC), with BSIM3 model files. Typical library model (TT) for n-channel devices was utilized. Simulations were performed in 0.35, 0.18, and 0.13 micron technologies. For simulations the following circuit was configured, as illustrated in Figure 4.

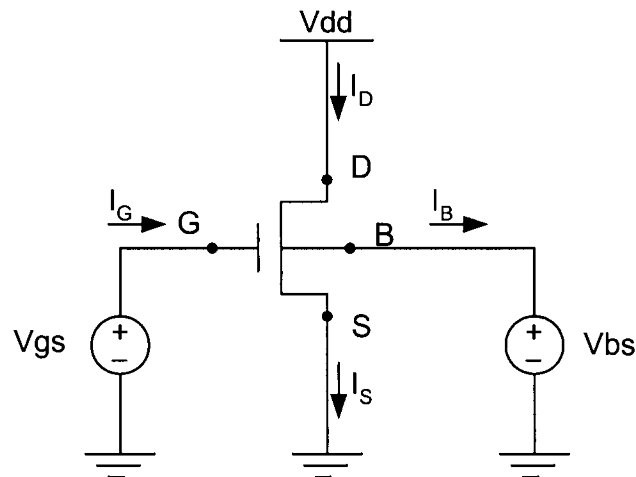

Figure 4: Circuit Schematic for Leakage Simulation

Based on the technology in use, proper transistor aspect ratio and supply voltage were selected. The focus of this simulation was mostly on drain and bulk currents. The gate current was ignored, because BSIM3 model considers gate as an open circuit [10] and also for $T_{OX} > 20$ Å, gate leakage current can be neglected compared to other main

leakage sources, such as subthreshold leakage [11]. Oxide thicknesses for each of the above technologies were above 20 Å.

Table 2: Gate Oxide Thickness in Submicron CMOS

Technology Node (micron)	Oxide Thickness (m)
0.35	7.50E-9
0.18	4.08E-09
0.13	3.15E-09

In [8] it is shown that T_{OX}, N_{pocket}, V_{DD}, V_{FB} are important parameters that major leakage currents are sensitive to their values. In BSIM3 there is no parameter for halo doping (N_{pocket}). There is also no specific parameter for V_{FB}, but since we know that threshold voltage and flat band voltage are related based on equation 1, threshold voltage has been varied in the simulations instead.

$$V_{TH0} = V_{FB} + \Phi s + K_T \text{ sqrt } (\Phi s) \qquad (1)$$

In the following sections parameters such as channel length, oxide thickness, channel doping concentration, threshold and supply voltages are varied by ±20%, one at a time, and their impacts on major leakage currents are observed.

4.1 BSIM3 MODEL

Here, it is worth to mention some of the important characteristics of BSIM3 model. Figure 5 illustrates the dc circuit equivalent that has been implemented by this model.

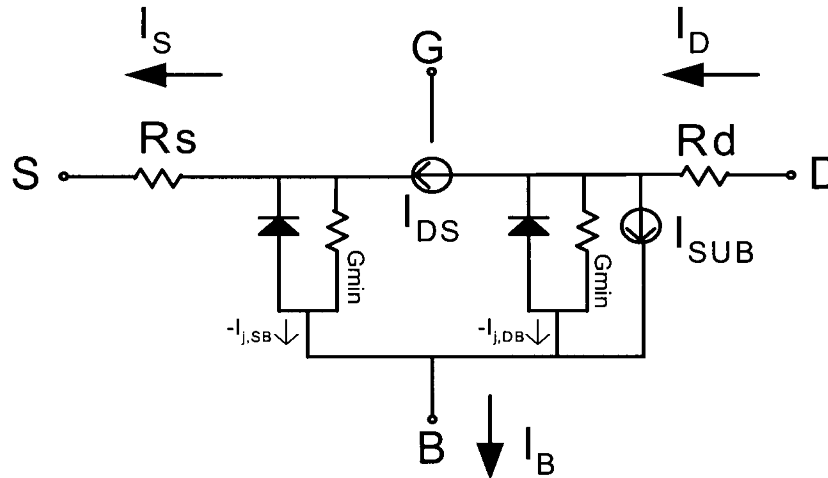

Figure 5: DC Circuit Equivalent of MOS Transistor in BSIM3 Model [10]

As previously mentioned and can be observed from the above illustration, the model doesn't include any of the gate leakage currents: neither tunnelling current through oxide nor hot carrier injection leakage. GIDL is not included in this model either. The only leakage currents accounted for in this model are drain-bulk and source-bulk junction leakages ($I_{J,DB}$ & $I_{J,SB}$), the substrate leakage (I_{SUB}), and subthreshold leakage current between drain and source (I_{DS}).

I_{SUB} is due to the impact ionization. This happens when an electron travels in the channel and gains energy from the electric field applied by V_{DS}. When this electric field is sufficient, the electron gains enough energy so that when it collides with a crystal atom

it generates an electron-hole pair. The generated electron will move towards drain, which has positive potential while the hole will move towards bulk, which is at lower potential. On their way they can collide with more crystal atoms and generate more electron-hole pairs, leading to avalanche multiplication of electron-hole pairs.

A summary of terminal currents and their relationships for this model is outlined in the following equations [10]:

$$
\begin{aligned}
&I_G = 0\\
&I_D = I_{DS} + I_{SUB} - I_{J,DB}\\
&I_S = - I_{DS} - I_{J,SB} \qquad (2)\\
&I_B = - I_{SUB} + I_{J,SB} + I_{J,DB}\\
&I_D = I_S + I_B
\end{aligned}
$$

Based on the above equations, the relationship between components of leakage current at drain, source, and bulk in BSIM3 model can be understood.

4.2 0.35-micron Technology

For this simulation circuit of Figure 4 was utilized. W/L of transistor was 0.8/0.35 with V_{DD} at 3.3 V.

4.2.1 I-V Characteristics

To have a better understanding of the range of OFF current of a transistor in 0.35-micron technology, the drain and bulk currents were plotted based on variations of V_{GS}

for several V_{BS} values. For this simulation V_{DD} was set at 3.3V while V_{GS} was swept from 0 to 5V with steps of 25mV and V_{BS} was varied from 0 to –1.5V by –0.5V steps. The result for drain and bulk currents are illustrated in Figure 6 and Figure 7.

As it can be observed from Figure 6, the OFF current of this transistor is in the range of several pA. As the bulk-source voltage decreases, higher voltage needs to be applied to the gate-source in order to turn the transistor on (body effect).

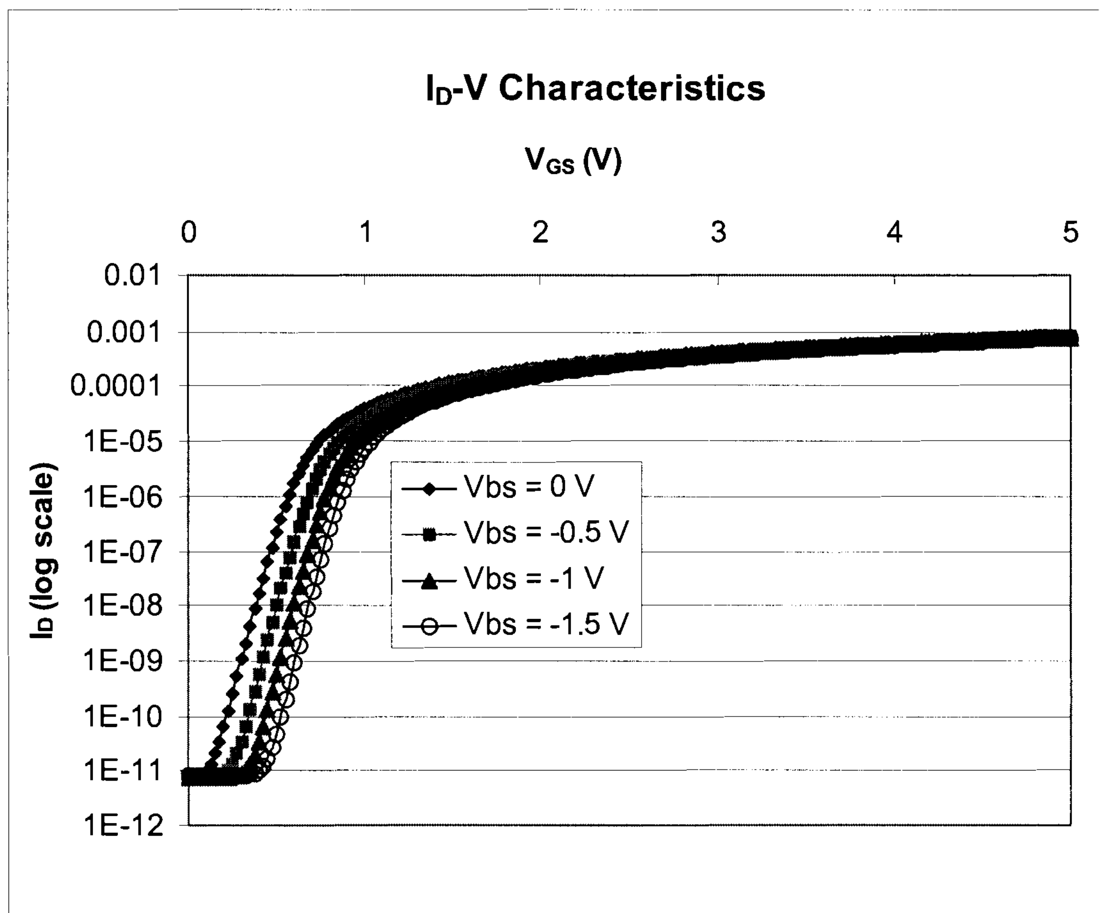

Figure 6: **I_D-V Characteristics of NMOS (W/L=0.8/0.35, V_{DD}=3.3V)**

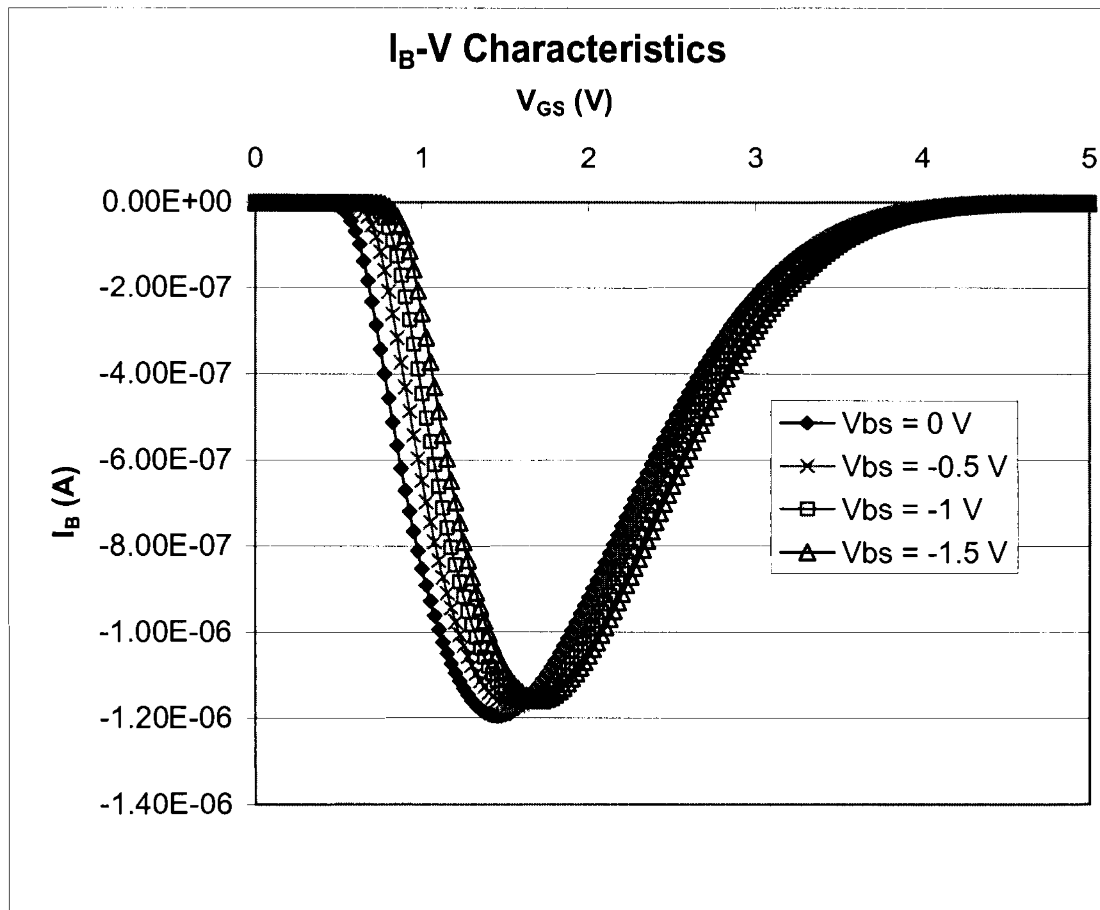

Figure 7: **I_B-V Characteristics of NMOS (W/L=0.8/0.35, V_{DD}=3.3V)**

If we assume that the junction currents are minute ($I_{J,SB}$ and $I_{J,DB}$), then the bulk current is same as the substrate current (Figure 5). When V_{DS} is large, the transistor operates in saturation. The electric field between the gate-drain terminals, close to where the channel pinches off, is large and therefore the substrate current due to impact ionization is large.

The bell shape graph of Figure 7 indicates that there are two factors influencing the value of impact ionization. One is the amount of the electron carriers (channel

current) and the second factor is the gate-drain junction electric field. When V_{GS} is small the channel is not strongly inverted, therefore the number of electrons present in the channel are small and hence the substrate current is small too. As V_{GS} increases, the inversion gets stronger and the number of electrons that can initiate impact ionization increases. This results in an increase in the bulk current (becomes more negative).

However this doesn't continue forever. After V_{GS} passes a certain value (V_{DS} remains constant) the voltage drop across the saturated region decreases. This means that the electric field and hence the amount of impact ionization decreases. If $V_{GS} - V_{DS} > V_T$ then the transistor starts operating in the linear region and the bulk current goes back to very small values [10].

4.2.1.1 A Case Study

A transistor with aspect ratio of 10 (W/L= 3.5/0.35), V_{DD} = 1.5V was tested and its bulk and drain currents measured [12]. V_{BS} was varied from 0 to -1.5V. Using Cadence™ tool the simulation in the same operating conditions was performed. The following graphs show the similarities and differences between measurement and simulation results.

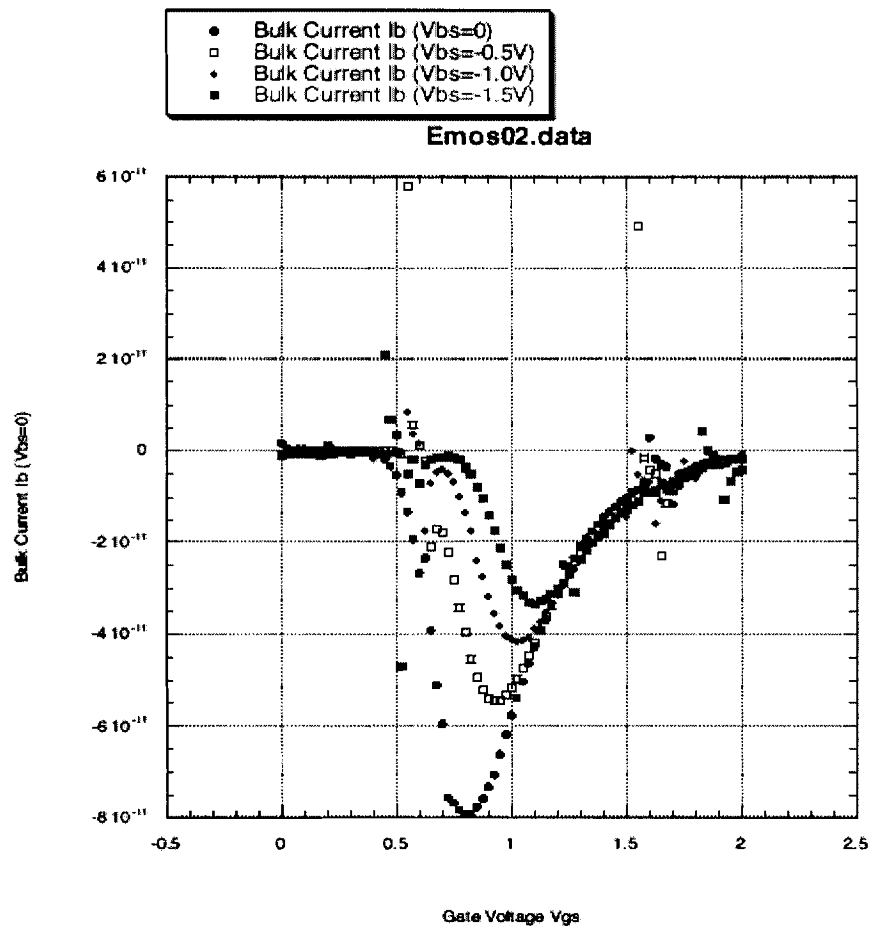

Figure 8: Measurement of Bulk Current vs. V_{GS} at Various V_{BS}, V_{DD}=1.5V [12]

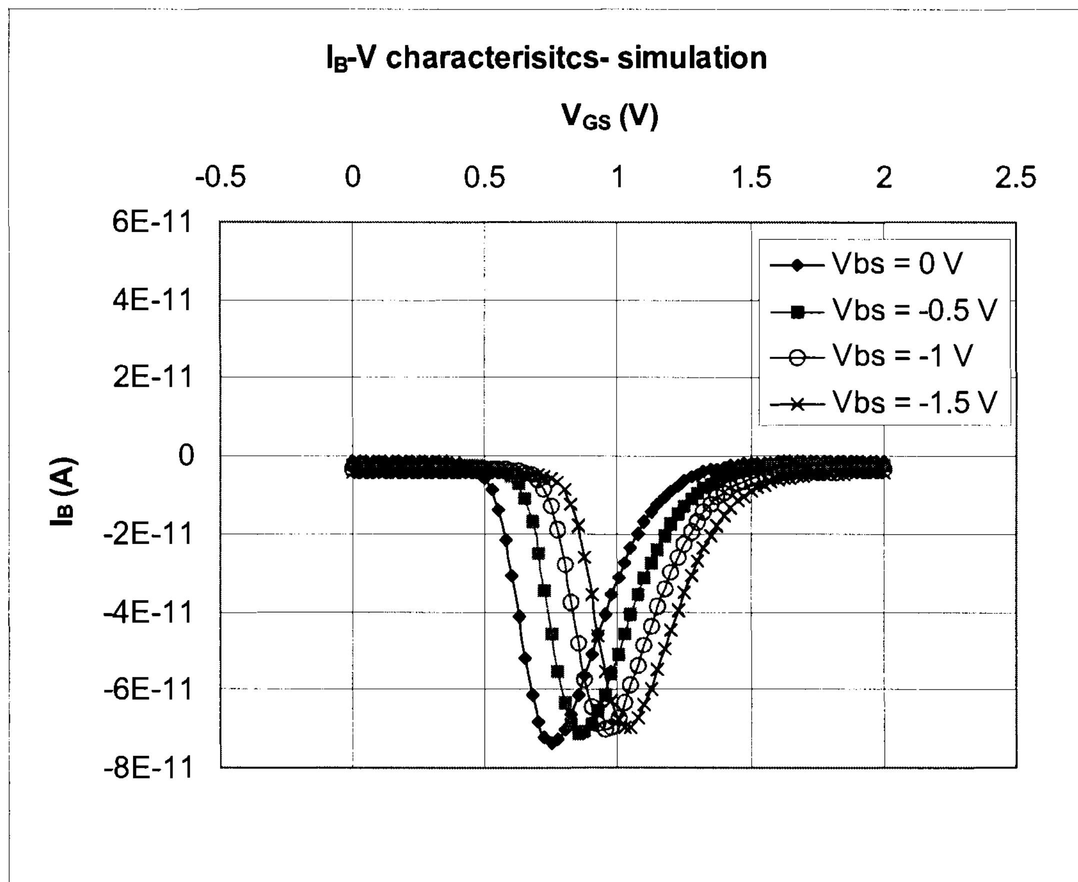

Figure 9: Simulation of Bulk Current vs. V_{GS} at Various V_{BS}, V_{DD}=1.5V

Comparing the measured and simulated data (Figure 8, Figure 9), it can be observed that in simulation the maximum absolute value of bulk current is around 70pA and the peak value has happened between 0.75 to 1.025V of V_{GS}. While in actual measurement the bulk current has a range between 35 to 80 pA and the peak has occurred between 0.8-1.1V of V_{GS}. Decrease of ~50pA of bulk current for different values of V_{BS} can be due to other leakage and parasitic sources that are not accounted for in the simulation model file.

The following graphs compare the test and simulation results for drain current.

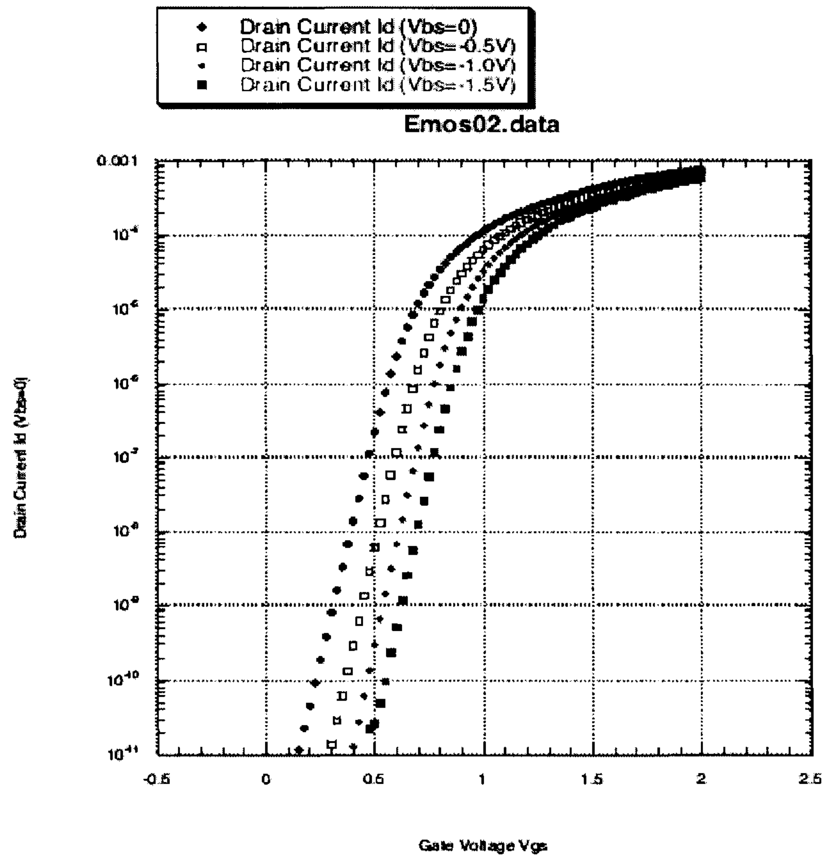

Figure 10: Measurement - Drain Current vs. V_{GS} at Various V_{BS}, V_{DD}=1.5V [12]

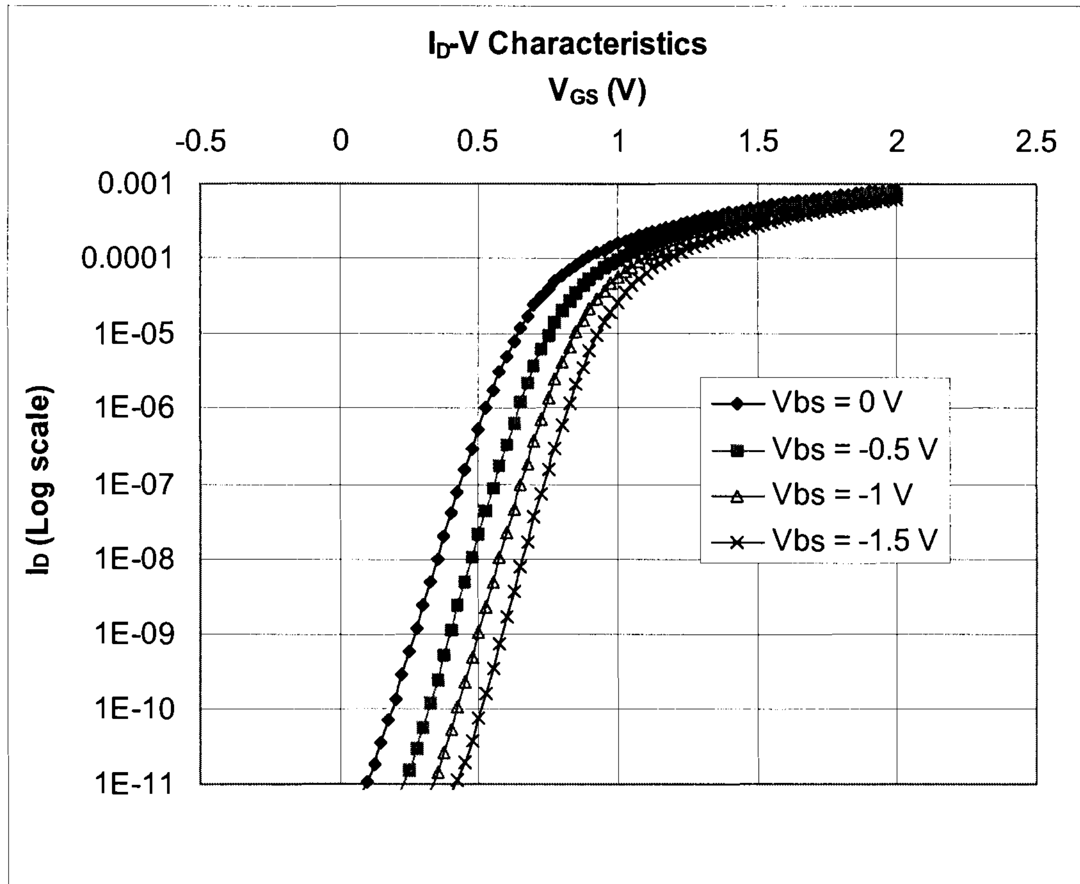

Figure 11: Simulation - Drain Current vs. V_{GS} at Various V_{BS}, V_{DD}=1.5V

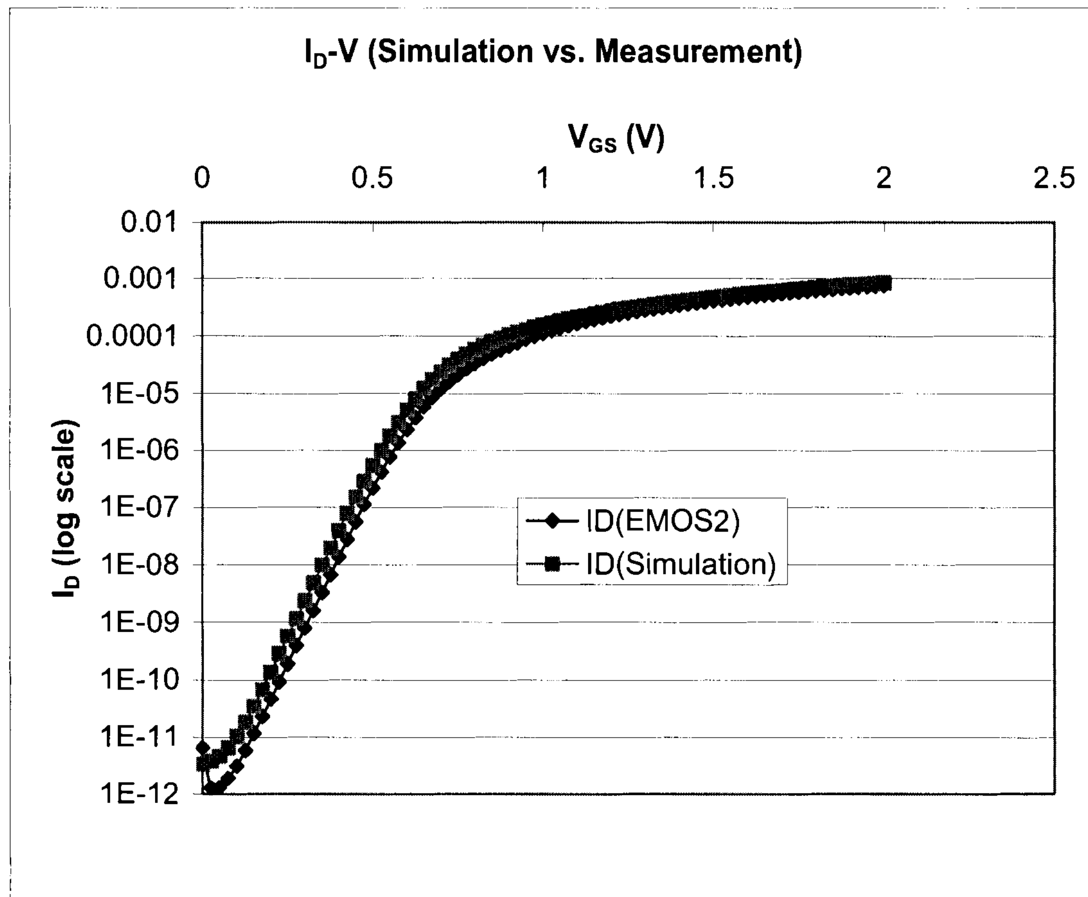

Figure 12: Drain Current Comparison for V_{BS}=0, V_{DD}=1.5V

As can be observed from the Figure 12, there is a 40-60% difference between the simulation and measurement results in subthreshold region, but this difference becomes less as the transistor enters the linear region of operation.

Figure 13 compares the measured and simulated results for the bulk current.

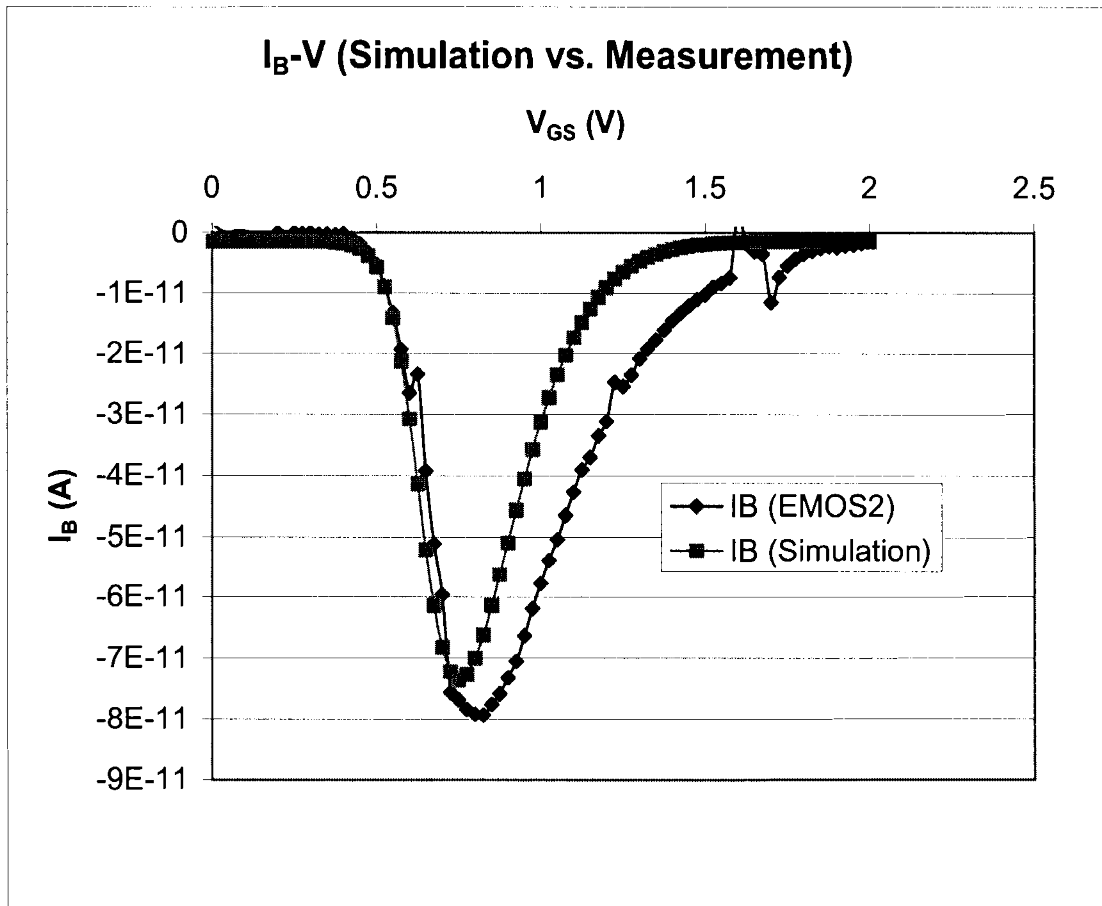

Figure 13: Bulk Current Comparison for V_{BS}=0, V_{DD}=1.5V

It can be observed that the measured bulk current does not follow the simulation as closely as the drain current does. This can be due to other factors that are not accounted for in the model file.

Another observation was the dependency of I_B on V_{DD}. Figure 14 shows that as drain voltage increases the absolute value of bulk current in OFF state increases as well. This has been confirmed with simulation as it is shown in Figure 15. When V_{DD} is small the transistor operates in the linear region independent of the gate source voltage. The

applied electric field close to drain is small and hence the amount of impact ionization is almost zero. As V_{DD} increases the transistor enters the saturation region. The channel pinches off and the electric field between gate and drain becomes large and so does the substrate current (impact ionization) [10].

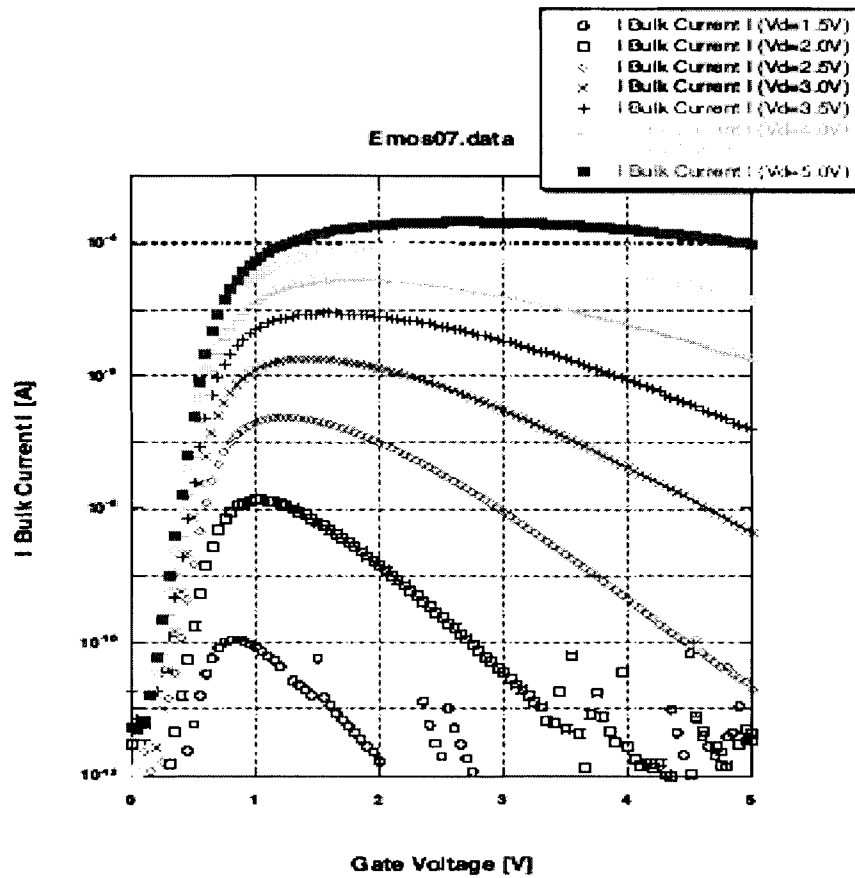

Figure 14: Measurement - log $|I_B|$ vs. V_{GS} at Various V_{DD} [12]

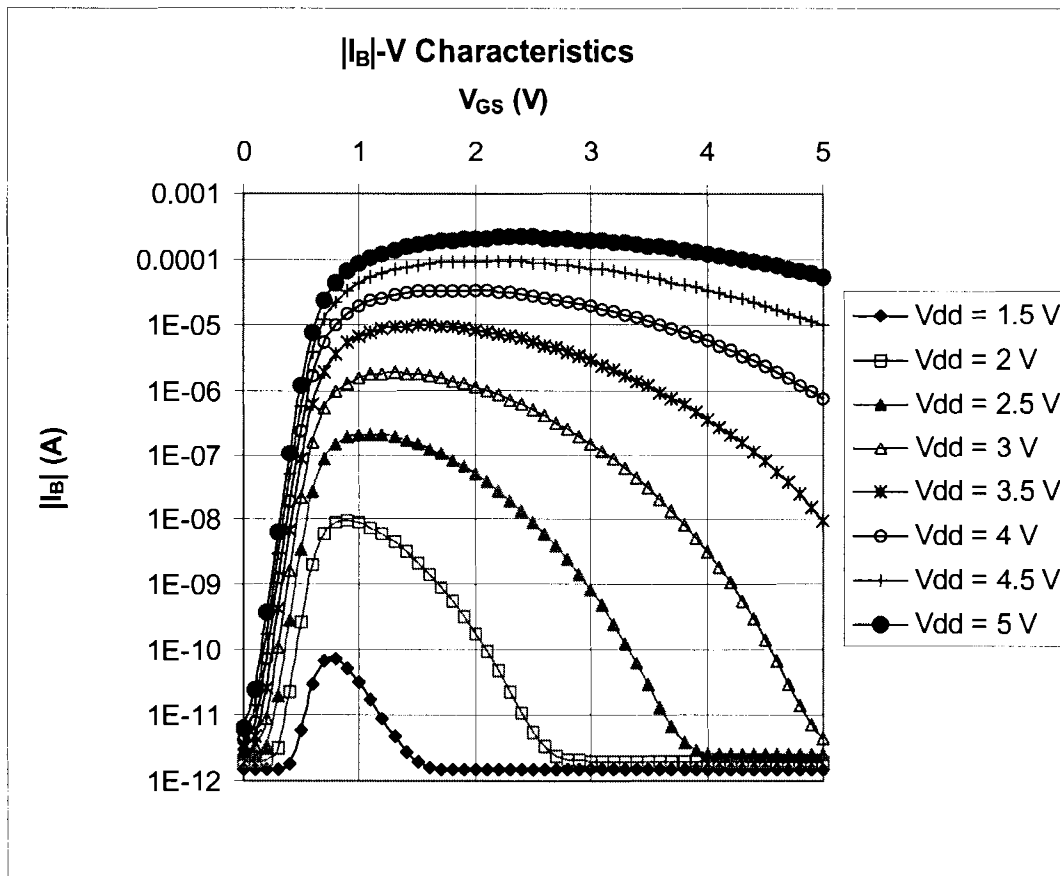

Figure 15: Simulation - log $|I_B|$ vs. V_{GS} at Various V_{DD}

Figure 16 compares measured and simulated bulk currents for couple of drain voltage values.

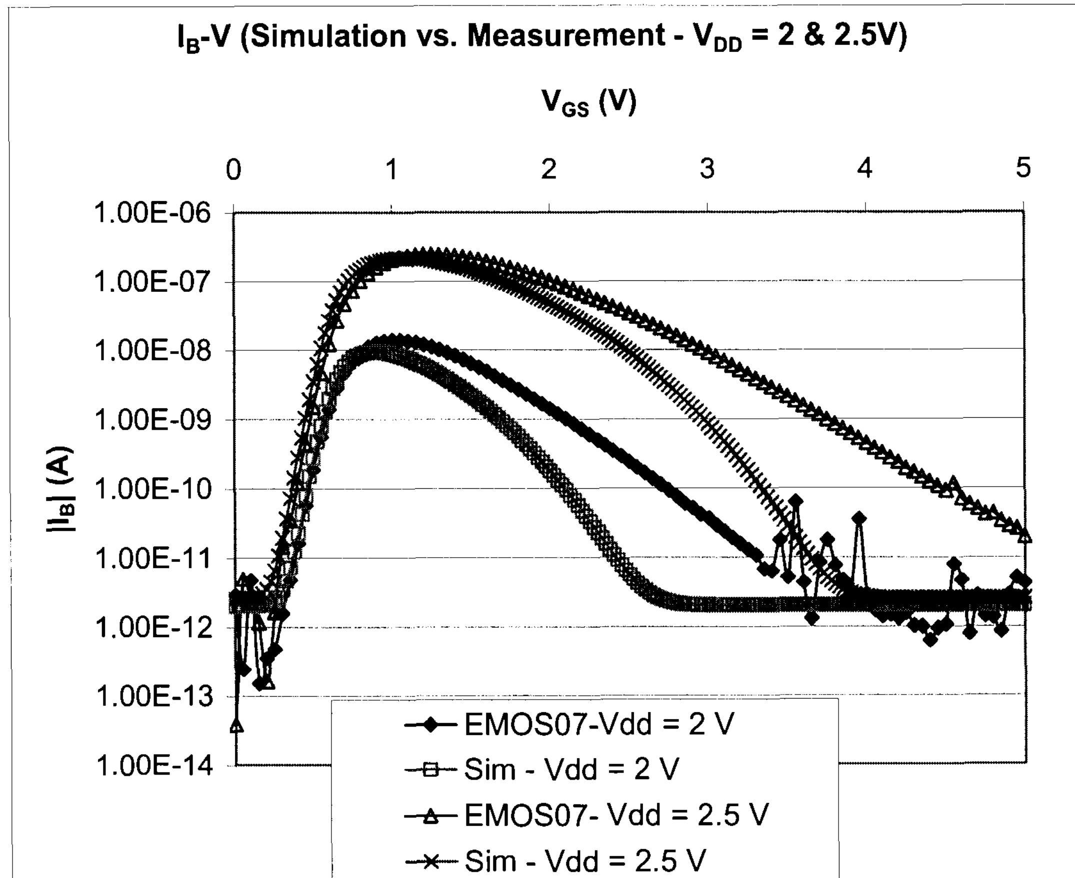

Figure 16: Comparison of Simulated and Measured Bulk Current (V_{DD}=2 & 2.5V)

4.2.1.2 Drain-Bulk Junction Current ($I_{j,DB}$)

In the previous sections, we neglected $I_{j,DB}$ and $I_{j,SB}$ (Figure 5), as a result the bulk and the substrate currents were considered equal. To find out if this assumption was correct, the following simulation was performed in the OFF state of circuit of Figure 4, ($V_{GS} = V_{BS} = 0$, $V_{DS} = V_{DD} = 3.3$V).

The drain diffusion area (AD) is one of the transistor parameters. Its default value for 0.35-micron technology is:

AD = 1 x Width of transistor (μm^2)

This value was increased until a significant change in the bulk current was observed (in the range of pA). By increasing the drain area by 10^4, an increase of 2.02pA was detected in the bulk current.

I_{B1} = -3.347pA Default value at AD = 1 x 3.5 (μm^2)

I_{B2} = -5.369pA New value at AD = 1 x 3.5 x 10^4 (μm^2)

The conclusion drawn was that $I_{j,\,DB}$ is about 4 orders of magnitude less than the bulk current, and therefore with AD at its default value, $I_{j,\,DB}$ will approximately be equal to:

$|I_{j,\,DB}| \approx 3.347E\text{-}16$ A (or 334.7 aA)

Therefore, our first assumption to neglect the reverse-bias p-n junction currents in respect to the bulk current is justified.

4.2.2 Channel Length Variations

In this section we observe the effect of channel length variation on transistor leakage currents. The circuit was in the OFF state ($V_{GS} = 0$, $V_{BS} = 0$, $V_{DD} = 3.3V$). L was varied by +20%. The default value was 0.35 micron. Figure 17 illustrates drain and bulk leakage. It has been observed that drain current varies about 0.3% while bulk current stays almost constant over the entire range.

4.2.3 Oxide Thickness Variations

The default value for T_{OX} of this model transistor is 7.5E-9 m. Oxide thickness was varied over a range of ±20% and the leakage currents were measured. Figure 18 illustrates the results. The outcome shows that for drain current ±20% variation in T_{OX} only changes it by 2.25% and 1.3% respectively and for bulk current by 0.21% and 0.12% respectively.

4.2.4 Channel Doping Variations

The default value for channel doping is 2.3579E+17 cm^{-3}. This value was changed by ±20% and the drain and bulk currents were plotted. The result showed that drain current varied by 0.8% and % 0.9 respectively while the bulk current changed by % 0.09. Figure 19 illustrates this.

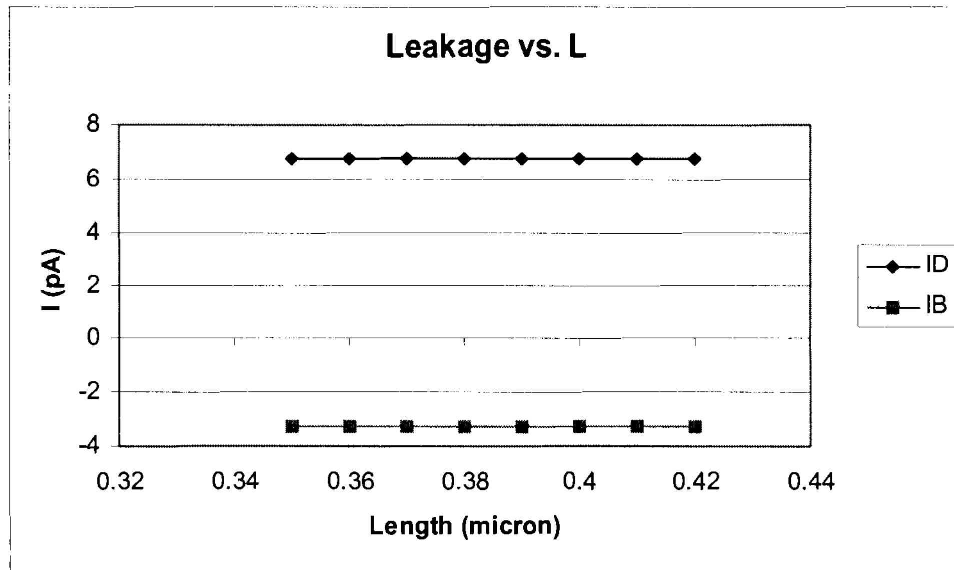

Figure 17: Leakage vs. Channel Length Variations (V_{GS}=V_{BS}=0, V_{DD}=3.3V)

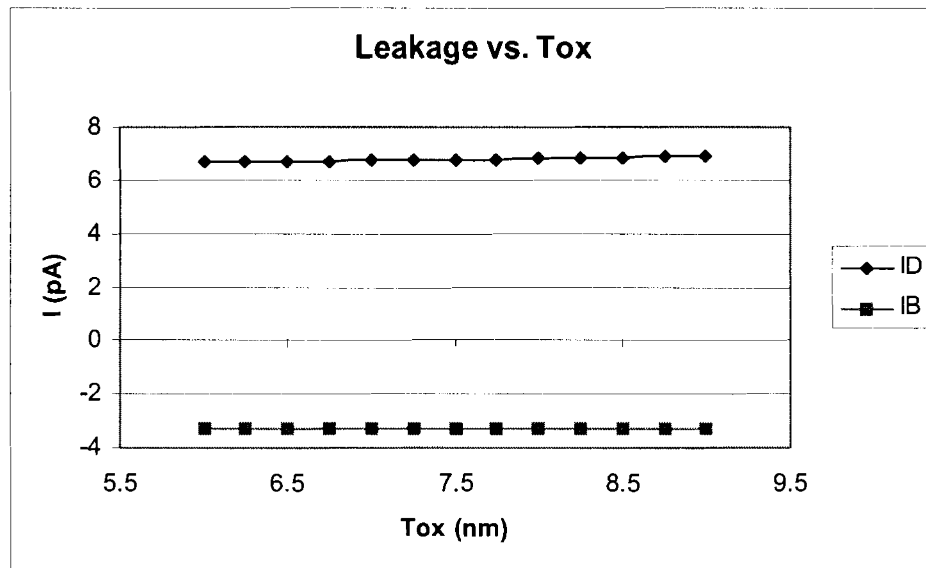

Figure 18: Leakage vs. Oxide Thickness Variations (V_{GS}=V_{BS}=0, V_{DD}=3.3V)

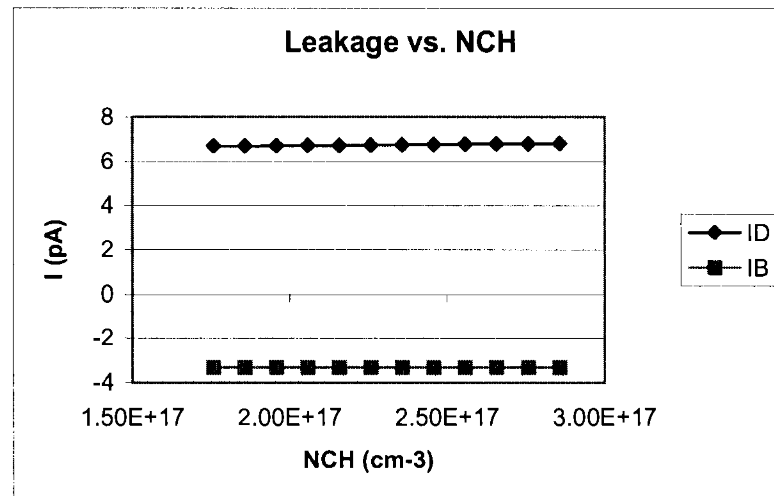

Figure 19: Leakage vs. Channel Doping Variations (V_{GS}=V_{BS}=0, V_{DD}=3.3V)

4.2.5 Threshold Voltage Variations

As described earlier, the goal was to vary flat band voltage, but since there is no such parameter available in the model file, and since it is known that flat band voltage and threshold voltage are related (Equation 1), V_{TH0} was varied over ± 20%. The default value for threshold voltage is 0.574607 V. The result showed that drain current was varied by 2.5% and 68% and bulk current by 0.24% and 6% respectively. Figure 20 illustrates this observation.

4.2.6 V_{DD} Variations

The value of V_{DD} was originally at 3.3 V. Varying it by ±20% caused both the drain and bulk current to vary by 20%, as illustrated in Figure 21.

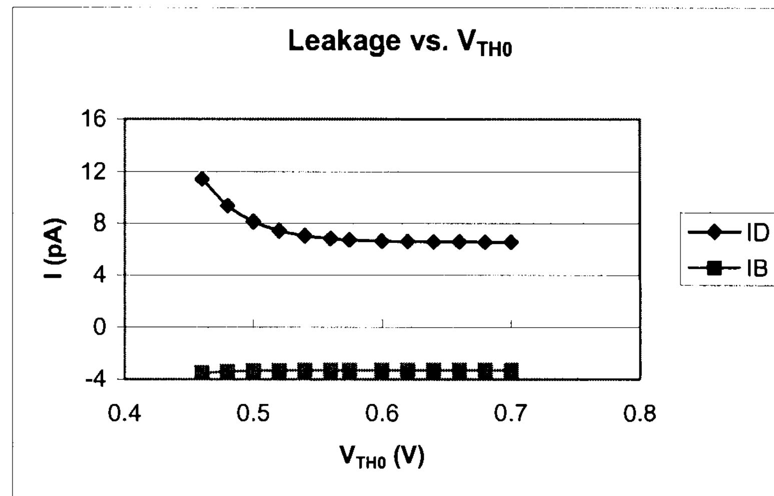

Figure 20: **Leakage vs. Threshold Voltage Variations (V_{GS}=V_{BS}=0, V_{DD}=3.3V)**

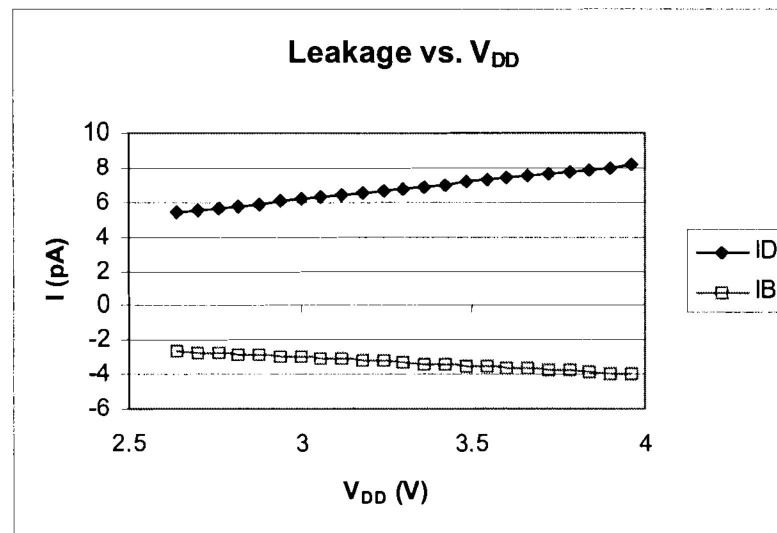

Figure 21: **Leakage vs. Supply Voltage Variations (V_{GS}=V_{BS}=0)**

4.2.7 Summary

The following table summarizes the impact of each parameter on drain and bulk leakage currents in 0.35-micron technology.

Table 3: Parameter Variation Summary for 0.35 micron Technology

Parameter	% Change	I_D % Change	I_B % Change
L	+20	0.3	0
T_{OX}	+20	2.25	0.2
	-20	1.3	0.12
NCH	+20	0.8	0.09
	-20	0.91	0.09
V_{TH0}	+20	2.5	0.24
	-20	68	6
V_{DD}	+20	20	20
	-20	20	20

From this table it can be concluded that variations of threshold voltage (flat band voltage) have the greatest impact on the drain leakage mechanism, while V_{DD} variations have the most impact on the bulk leakage current.

4.3 0.18-micron Technology

Circuit of Figure 4 was utilized for the following simulations. W/L of transistor was 0.5/0.18 with V_{DD} at 1.8 V.

4.3.1 I-V Characteristics

Similar to the previous section, the simulation started with observing I-V characteristics of the transistor. Drain and bulk currents were plotted while gate-source voltage was varied over a range of 0-5V with 25mV steps and V_{BS} from 0 to -1.5V with steps of -0.5V. Figure 22 and Figure 23 illustrate the simulation results.

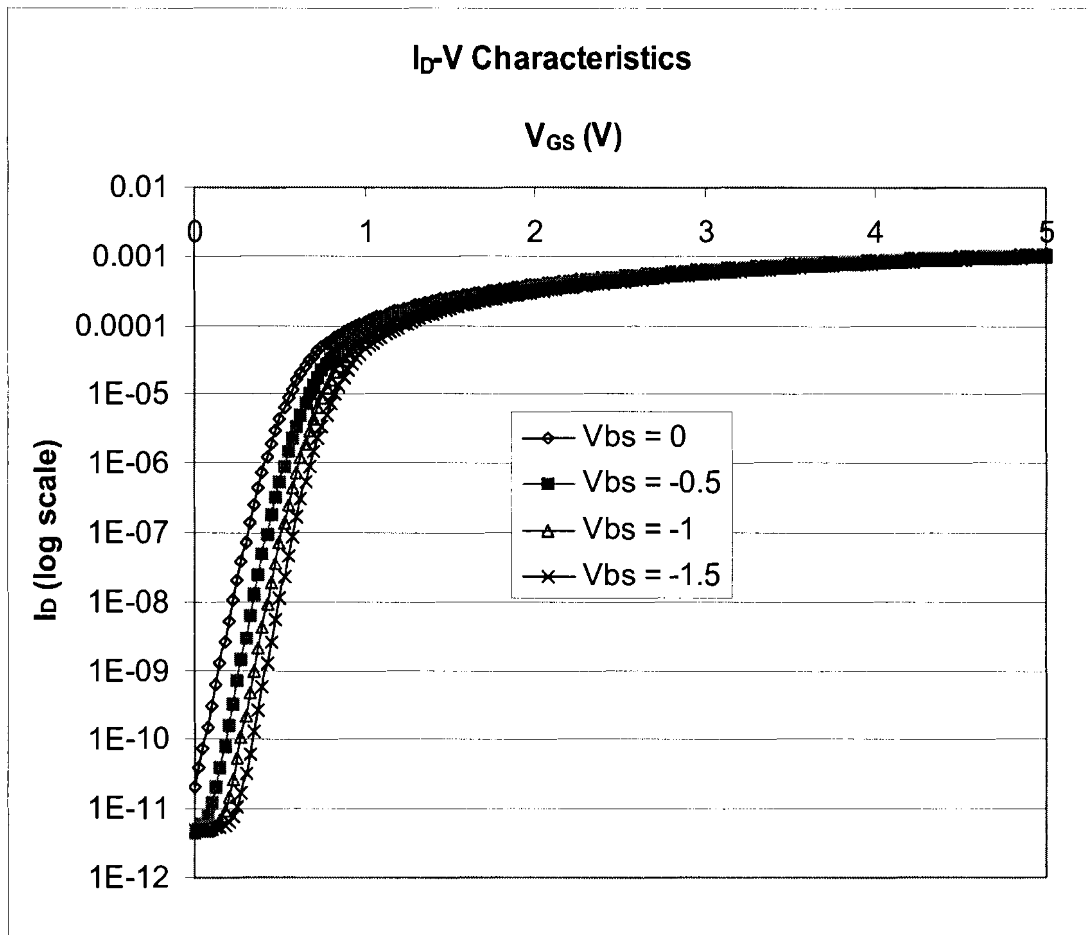

Figure 22: I_D-V Characteristics of NMOS (W/L=0.5/0.18, V_{DD}=1.8V)

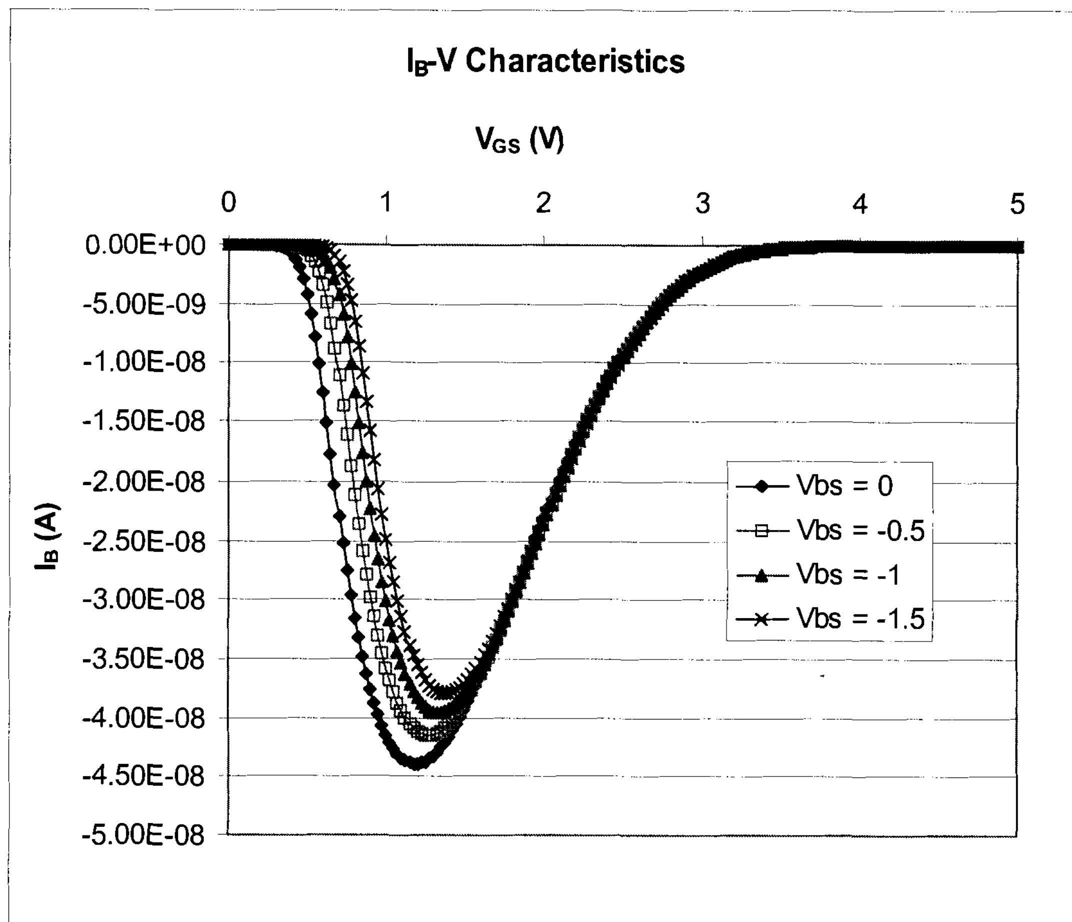

Figure 23: **I_B-V Characteristics of NMOS (W/L=0.5/0.18, V_{DD}=1.8V)**

As can be observed from Figure 22, the drain leakage decreases as the bulk-source junction becomes more reverse biased. This is due to body effect. For details, please refer to section 2.1.3.

The bell shape graph of Figure 23 is due to impact ionization, as discussed in section 4.2.1.

4.3.2 Channel Length Variations

The goal of this simulation is to find out the effect of channel length variations on the leakage current. The transistor was configured in the OFF state ($V_{GS} = V_{BS} = 0$, and $V_{DD} = 1.8V$). L was varied +20%. The default value was 0.18 micron. Figure 24 illustrates drain and bulk leakage currents. It has been observed that drain current varies about 34% while bulk current varies about 0.38%.

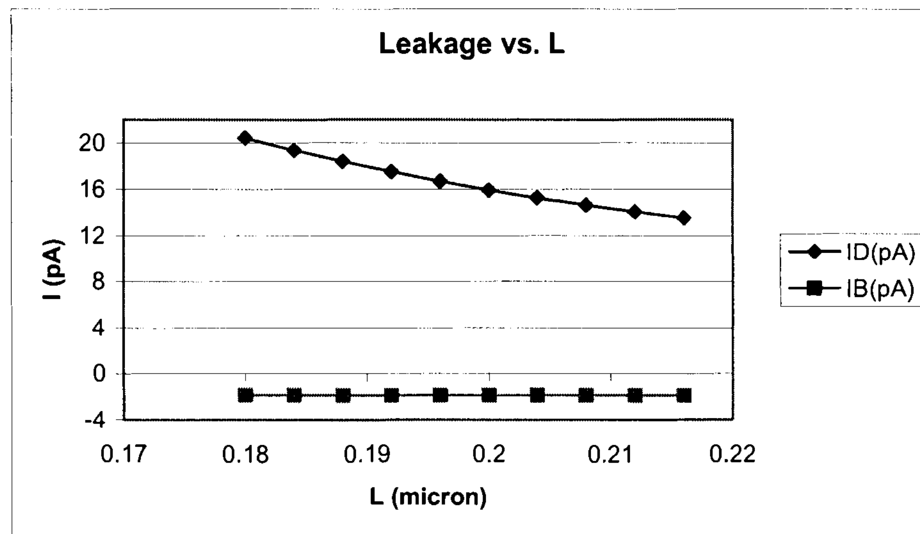

Figure 24: Leakage vs. Channel Length Variations ($V_{GS}=V_{BS}=0$, $V_{DD}=1.8V$)

4.3.3 Oxide Thickness Variations

The default value for T_{OX} of this model transistor is 4.08E-9 m. Oxide thickness was varied over a range of ±20% and the leakage currents were plotted. Figure 25 illustrates the results. It shows that ±20% variation in T_{OX} changes drain current by 53% and 35% and the bulk current by 0.66% and 0.44% respectively.

4.3.4 Channel Doping Variations

The default value for channel doping is 3.9E+17 cm^{-3}. ±20% variation of NCH changed the drain current by 22% and 20% and the bulk current by 0.27% and 0.22% respectively. Figure 26 illustrates this.

4.3.5 Threshold Voltage Variations

The goal was to vary flat band voltage, but since there is no such parameter available in the model file, and since it is known that flat band voltage and threshold voltage are related (Equation 1), V_{TH0} was varied over a range of ±20%. The default value for threshold voltage for this technology is 0.4736658 V. The drain current changed by 78% and 1185% and the bulk current by 0.93% and 14% respectively, as illustrated in Figure 27.

4.3.6 V_{DD} Variations

The original value of V_{DD} was 1.8 V. Varying it by ±20% caused the drain current to change by 15% and 14% respectively and the bulk current by 22% and 20% respectively, as illustrated in Figure 28.

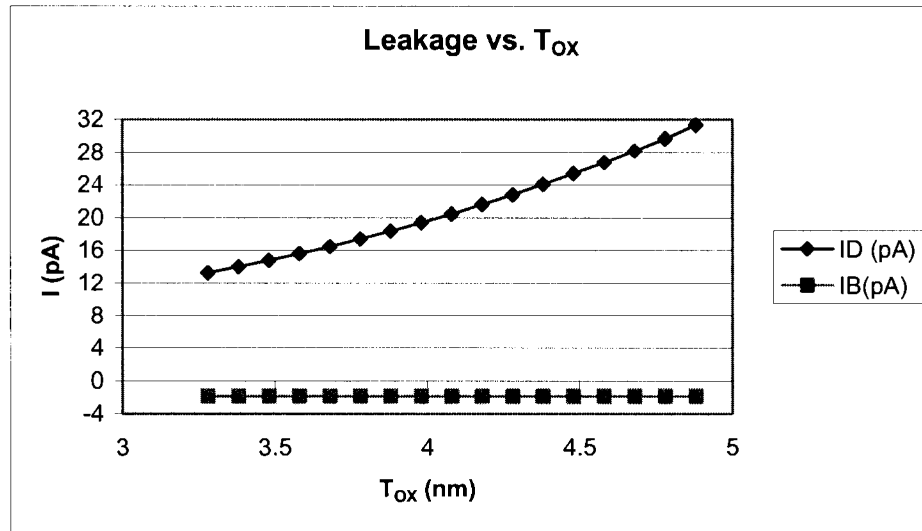

Figure 25: Leakage vs. Oxide Thickness Variations (V_{GS}=V_{BS}=0, V_{DD}=1.8V)

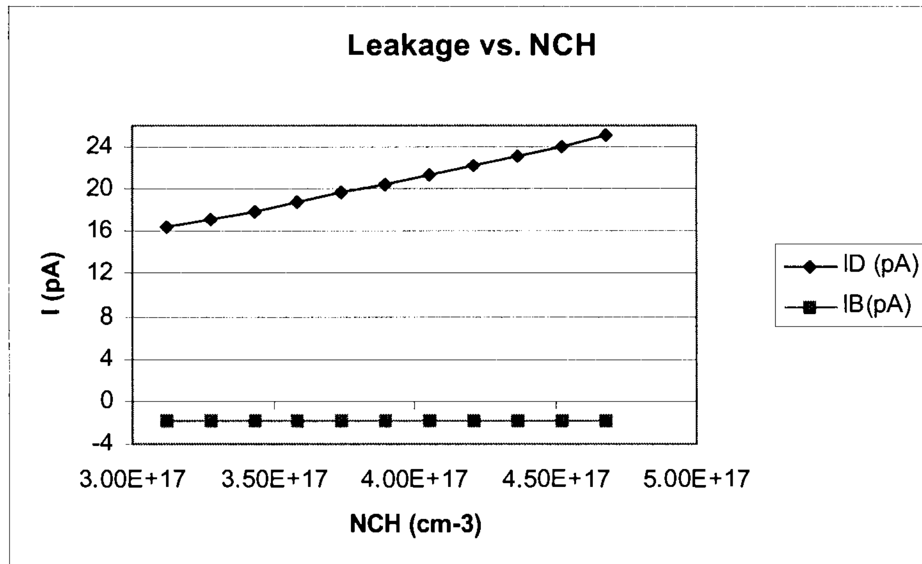

Figure 26: Leakage vs. Channel Doping Variations (V_{GS}=V_{BS}=0, V_{DD}=1.8V)

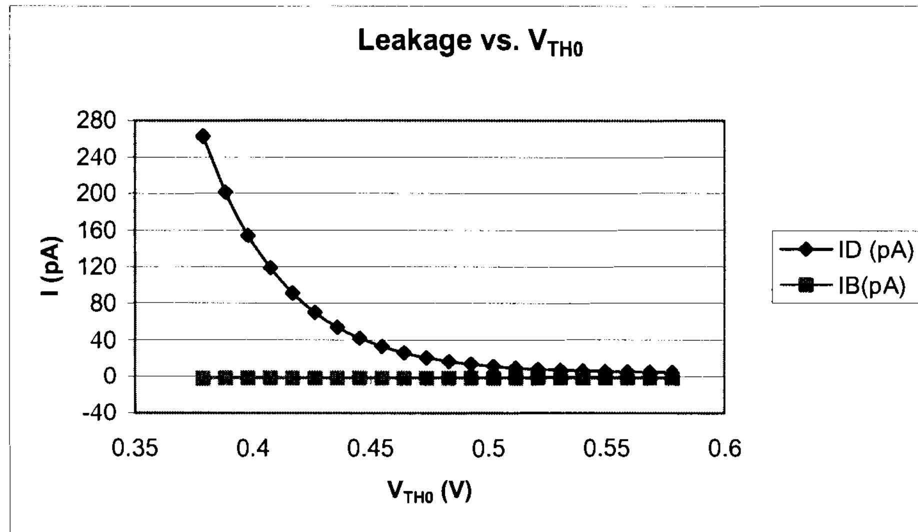

Figure 27: Leakage vs. Threshold Voltage Variations (V_{GS}=V_{BS}=0, V_{DD}=1.8V)

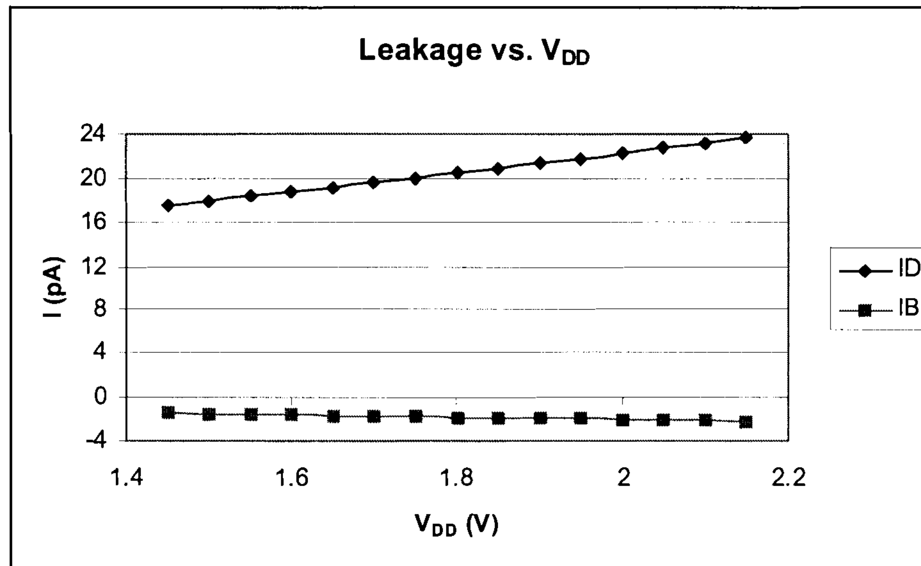

Figure 28: Leakage vs. Supply Voltage Variations (V_{GS}=V_{BS}=0)

4.3.7 Summary

The following table summarizes the impact of each parameter on drain and bulk leakage currents in 0.18-micron technology.

Table 4: Parameter Variation Summary for 0.18 micron Technology

Parameter	% Change	I_D % Change	I_B % Change
L	+20	34	0.38
T_{OX}	+20	53	0.66
	-20	35	0.44
NCH	+20	22	0.27
	-20	20	0.22
V_{TH0}	+20	78	0.93
	-20	1185	14
V_{DD}	+20	15	22
	-20	14	20

From this table it can be concluded that variation of threshold voltage (flat band voltage) has the greatest impact on the drain leakage mechanism while variation in V_{DD} has the maximum impact on bulk leakage current in 0.18-micron technology.

4.4 0.13-micron Technology

For this simulation circuit of Figure 4 was utilized. W/L of transistor was 0.6/0.13 and V_{DD} = 1.2V.

4.4.1 I-V Characteristics

To have a better understanding of the range of OFF current of the transistor, the drain and bulk currents of the transistor were plotted based on various gate-source voltages and bulk-source voltages. V_{GS} was swept from 0 to 1.2V with 25mV steps, and V_{BS} was varied between 0 to –0.75V with –0.25V steps. V_{DD} was at 1.2V. Figure 29 and Figure 30 illustrate the results obtained from these simulations.

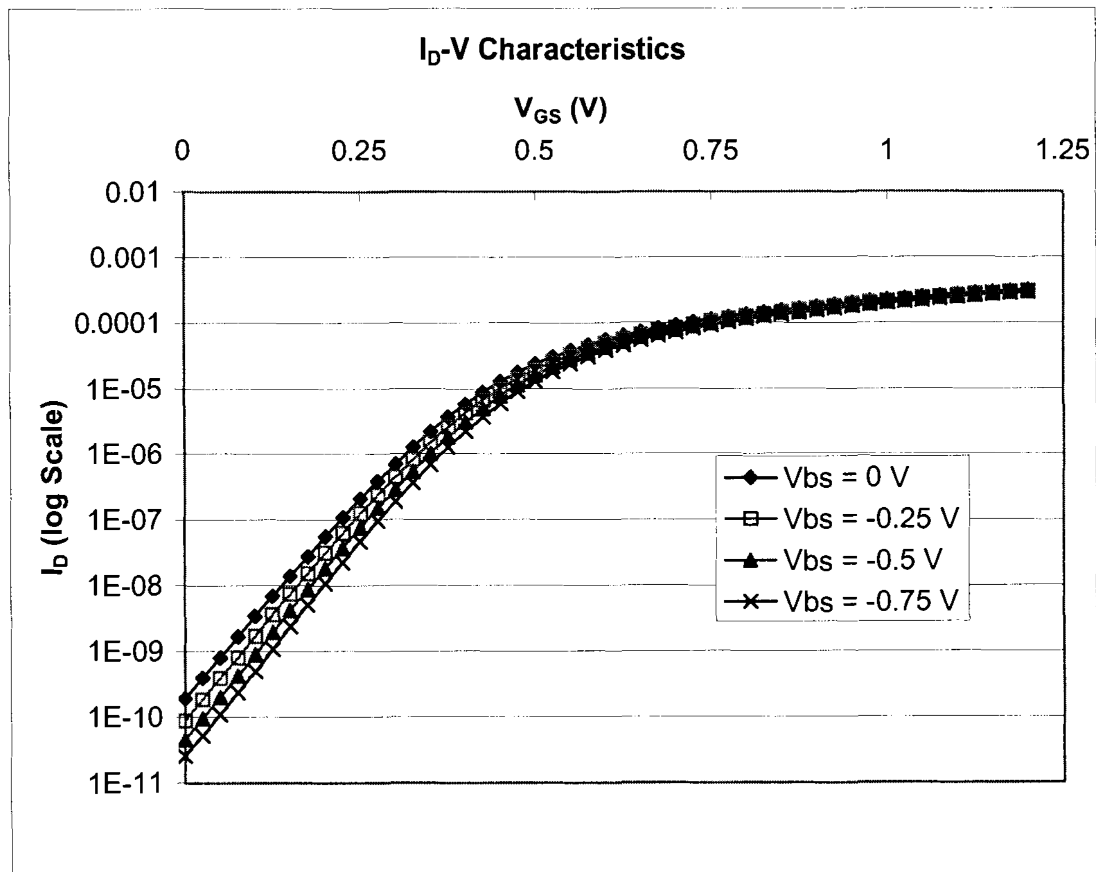

Figure 29: I_D-V Characteristics of NMOS (W/L=0.6/0.13, V_{DD}=1.2V)

As it can be observed from Figure 29, the OFF current of this transistor decreases as the bulk-source voltage becomes more negative (body effect). Also the value of the drain current in subthreshold region is more than those of the previous two technologies, which shows the impact of transistor scaling on leakage.

Figure 30 illustrates the bulk current of this transistor for the same V_{GS} and V_{BS} values.

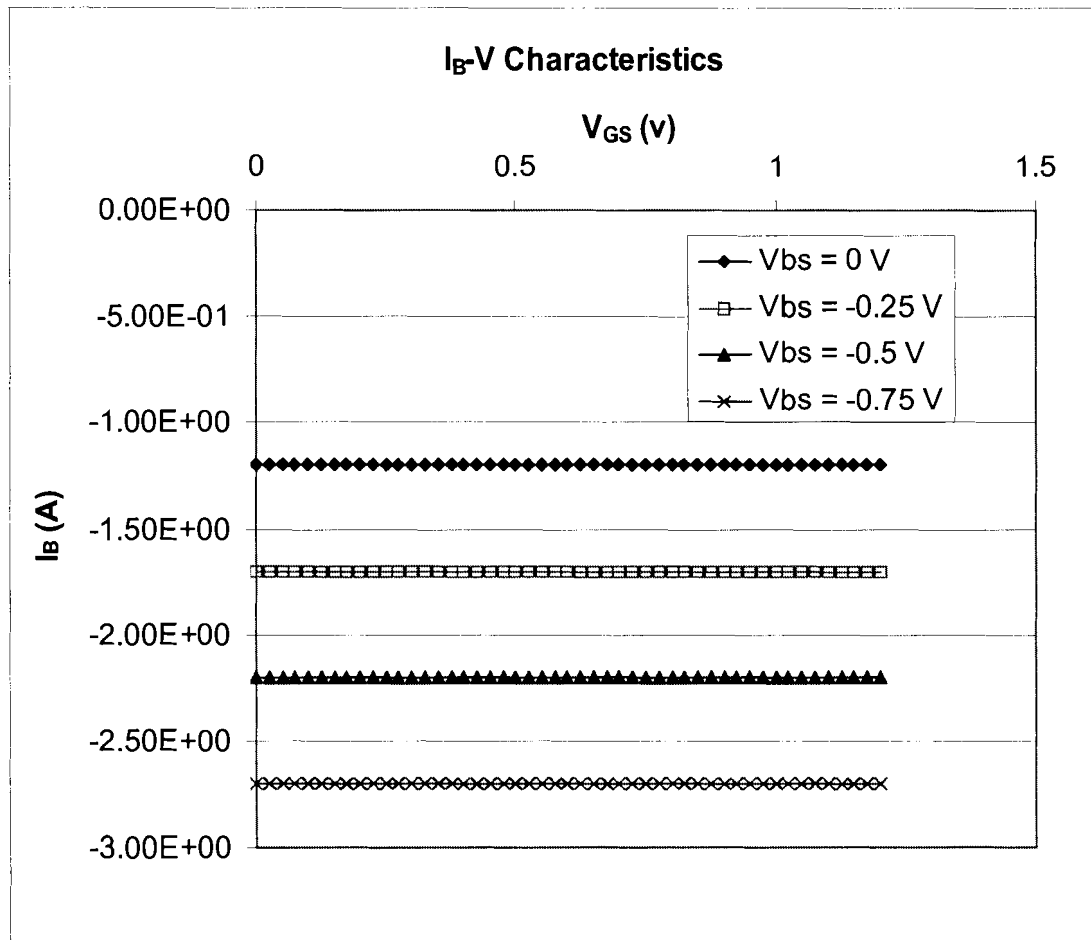

Figure 30: I_B-V Characteristics of NMOS (W/L=0.6/0.13, V_{DD}=1.2V)

Unlike the previous two technology nodes, the bulk current doesn't have a bell shape graph in 0.13-micron technology. It may be due to lack of accurate transistor modeling in the model file provided by Canadian Microelectronic Corporation (CMC). This area requires more investigation.

4.4.2 Channel Length Variations

In this section we observe the effect of channel length variations on the leakage current. The transistor was configured in the OFF state ($V_{BS} = V_{GS} = 0$, $V_{DD} = 1.2V$). L was varied by +20%. The default value was 0.13 micron. Figure 31 illustrates drain and bulk currents. It has been observed that drain current varies about 77% while bulk current remains almost constant over the entire range. This shows how dramatically the drain leakage current decreases as the length of the transistor increases.

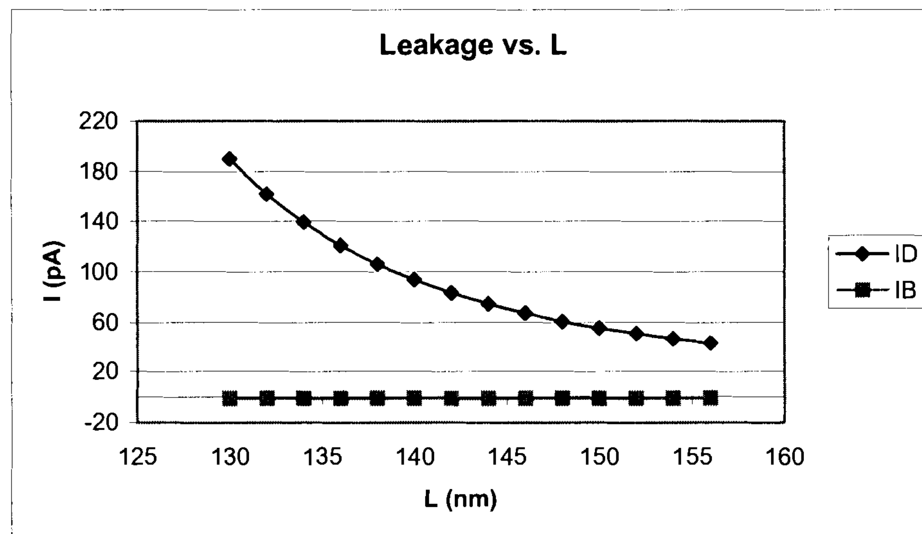

Figure 31: Leakage vs. Channel Length Variations (V_{GS}=V_{BS}=0, V_{DD}=1.2V)

4.4.3 Oxide Thickness Variations

The default value for T_{OX} of this model transistor is 3.15E-9 m. Oxide thickness was varied over a range of ±20% and the leakage currents were plotted. Figure 32 illustrates that +20% variation in T_{OX} changes drain current by 395% and –20% variation of T_{OX} changes it by 83%. Bulk current remains constant over the entire range.

4.4.4 Channel Doping Variations

The default value for channel doping is 2.7082E+17 cm^{-3}. This value was altered by ±20% and the drain and bulk currents were plotted. The result shows that drain current varies by 34% and 92% respectively while the bulk current remains constant, as illustrated in Figure 33.

4.4.5 Threshold Voltage Variations

In this part the threshold voltage was varied instead of flat band voltage, since we know that these two are related (Equation 1). This parameter was varied over ± 20%. The default value for threshold voltage for this technology node is 0.2330 V. The result was that drain current varied by 74% and 292% respectively while the bulk current did not change over the entire range. The result is illustrated in Figure 34.

4.4.6 V_{DD} Variations

The original value of V_{DD} was 1.2 V. Varying it by ±20% caused the drain current to vary by 76% and 10% respectively and bulk current by 20%, as illustrated in Figure 35.

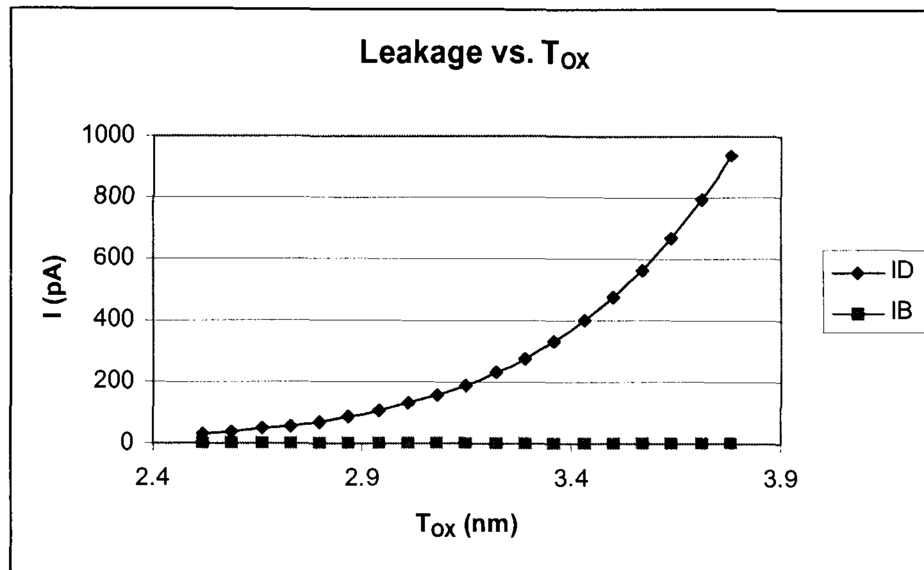

Figure 32: Leakage vs. Oxide Thickness Variations (V_{GS}=V_{BS}=0, V_{DD}=1.2V)

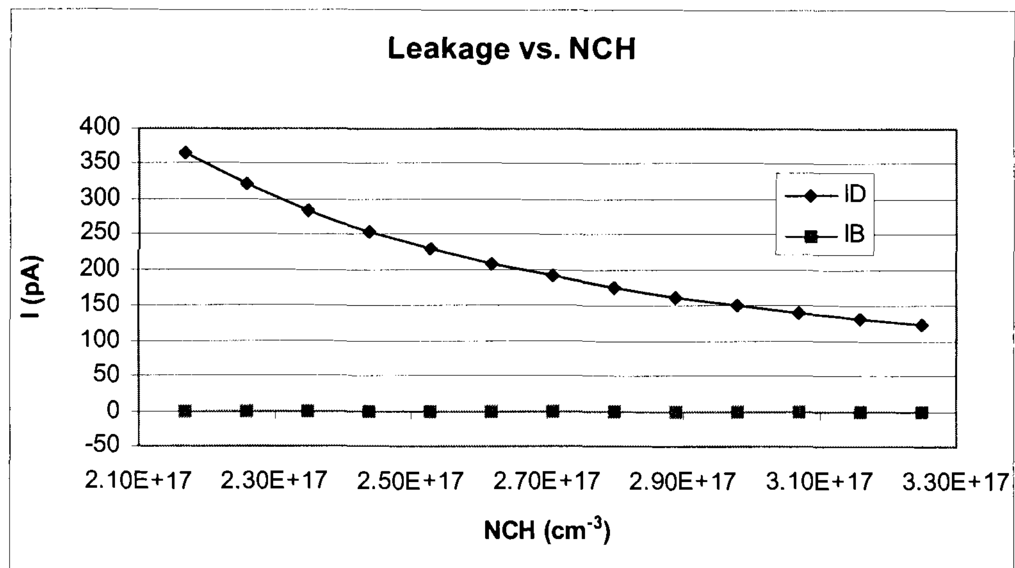

Figure 33: Leakage vs. Channel Doping Variations (V_{GS}=V_{BS}=0, V_{DD}=1.2V)

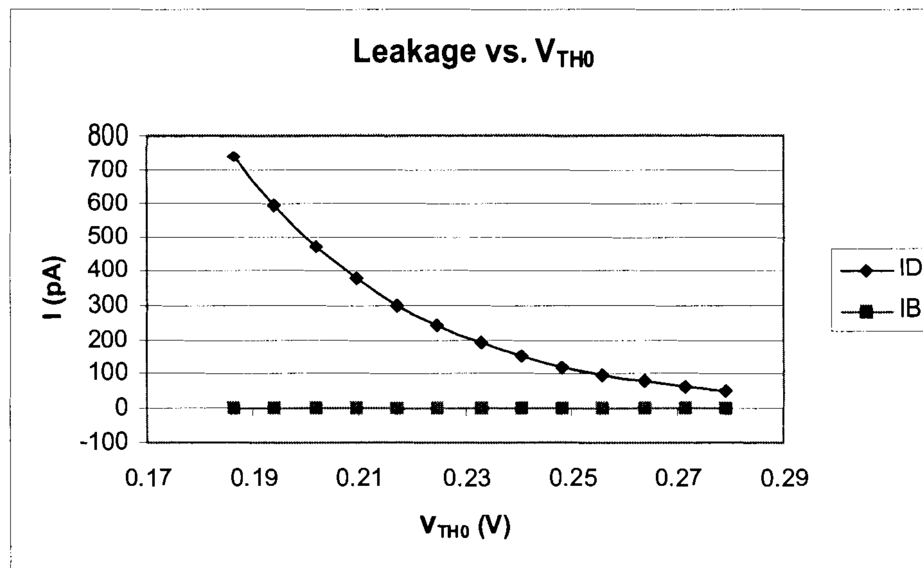

Figure 34: Leakage vs. Threshold Voltage Variations (V_{GS}=V_{BS}=0, V_{DD}=1.2V)

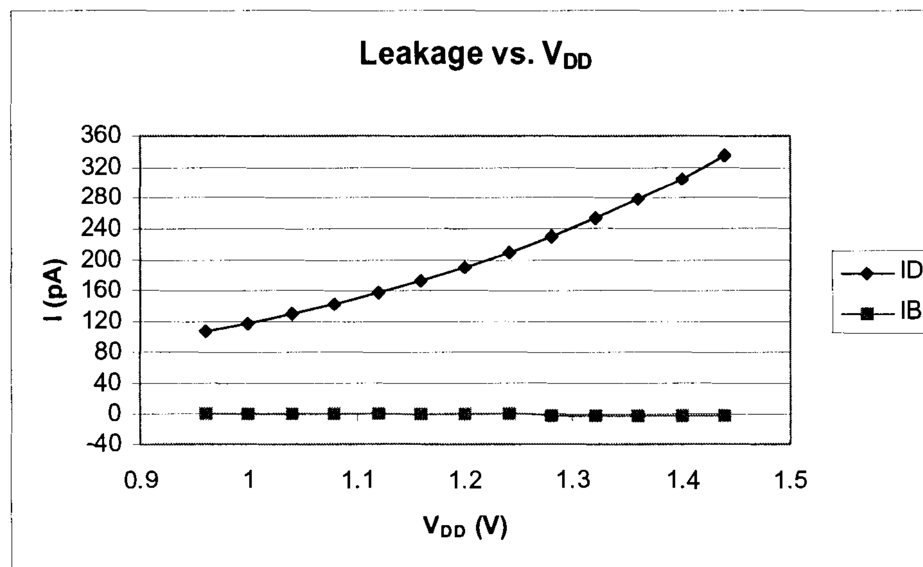

Figure 35: Leakage vs. Supply Voltage Variations (V_{GS}=V_{BS}=0)

4.4.7 Summary

The following table summarizes the impact of each parameter on drain and bulk leakage currents in 0.13-micron technology.

Table 5: Parameter Variation Summary for 0.13 micron Technology

Parameter	% Change	I_D % Change	I_B % Change
L	+20	77	0
T_{OX}	+20	395	0
	-20	83	0
NCH	+20	34	0
	-20	92	0
V_{TH0}	+20	74	0
	-20	292	0
V_{DD}	+20	76	20
	-20	10	20

From this table it can be concluded that increasing oxide thickness has the greatest impact on drain leakage current; Threshold voltage also has a large impact on the drain leakage. Variations in V_{DD} influences the bulk leakage current most. Here it is worthwhile to mention that the behaviour of bulk current was quite different in this technology node than the previous two (0.35 and 0.18 microns). This may be due to inaccurate modeling of bulk current in the OFF state of transistor in 0.13-micron technology. This area requires more investigation.

5 CONCLUSION

Based on the simulations performed, it can be concluded that subthreshold leakage is the dominant leakage in all three technologies. The most influential parameters on the subthreshold leakage current in 0.13-micron technology were oxide thickness and threshold voltage. For the other two technology nodes (0.18 and 0.35) threshold voltage had the greatest impact on the leakage current. Table 6 summarizes this observation.

Table 6: Dominant Leakage Parameter in CMOS Technologies

CMOS Technology (micron)	Leakage Parameter
0.35	V_{TH0}
0.18	V_{TH0}
0.13	T_{OX}, V_{TH0}

It was also observed that BSIM3 does not take into account all the leakage sources in the MOSFET model. This results in discrepancies between computer simulations and actual measurements on the device. IC designers should take this into account that the leakage current value of the fabricated chip would differ from that of the simulation.

This research project can be a starting point for identifying the I_{DDQ} values for building blocks of more complex integrated circuits. Same methodology can be utilized to simulate larger functional blocks in CMOS. Simulated leakage components can be efficiently controlled using such BSIM3 model parameters as V_{TH0} and T_{OX}.

As scaling in CMOS technology continues, leakage current and static power dissipation will increase. Many leakage reduction methods have been developed, but still more research needs to be done in this field. Carefully designing the integrated circuits and utilizing the circuit level techniques can effectively control leakage current mechanisms in submicron CMOS technologies.

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