HOT-CARRIER DEGRADATION STUDIES AT SILICON-SILICON DIOXIDE INTERFACE IN SHORT CHANNEL MOSFETS

by

Xiao Ming Li

B. Sc., Beijing University, 1984

M.Sc., Beijing Polytechnic University, 1987

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Name: Xiao Ming Li

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Examining Committee:

Committee Chairman:

Dr. J. Jones
School of Engineering Science, SFU

Senior Supervisor:

Dr M. J. Deen
Sc l of Engineering Science, SFU

Committee Member:

Dr. R. H. S. Hardy
School of Engineering Science, SFU

Committee Member:

Dr. S. Stapleton
School of Engineering Science, SFU

External Examiner:

Dr. S. R. Morrison
Department of Physics, SFU

Date Approved: April 23, 1991

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Author:

(signature)

Xiaoming LI

(name)

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(date)

ABSTRACT

It is well known that $Si-SiO_2$ interface states generated by hot-carrier-injection have played an important role in the degradation of short-channel MOSFETs. Theoretical and experimental researches were carried out in this project to examine the hot-carrier effects and characterize the $Si-SiO_2$ interface states. Among these researches, we proposed a new charge-pumping method and a physical model for formulating bias dependence of 1/f noise in the saturation mode, and compared hot-carrier-generated interface state densities with the DC parameter degradations. A computer software/hardware integrated microelectronic measurement system was built.

The charge pumping technique has proven to be a reliable probe of $Si-SiO_2$ interface states. However, for more than two decades since it was introduced, charge pumping measurements have been conducted by connecting the drain and source together. Here, we propose a new charge pumping method, which uses separate drain and source bias voltages. It allows us for the first time, to measure the $Si-SiO_2$ interface states density (N_{it}) near the drain and source independently without making any assumption. We can now determine the spatial distribution of N_{it} along the whole channel for short channel devices. N_{it} is found to be non-uniformly distributed along the channel even for unstressed devices, and peaks of N_{it} can be found at both the source and the drain side of the channel.

The trapping and detrapping of carriers by the interface states generated by hot-carrier-injection, and the mobility fluctuation caused by interface scattering have been known to be the source of low frequency or 1/f noise in MOSFETs. We proposed here a physical model to formulate the bias dependence of 1/f noise

for MOSFETs in the saturation mode. Good agreement has been obtained between the theoretical predictions and our experimental results.

DC parameters which are sensitive to hot-carrier effects were monitored and their degradations as a function of hot-carrier stressing time were also measured. Comparison was made between the degradation of maximum trans-conductance g_m and charge pumping measured N_{it}. As we expected, the degradation of g_m has shown to be a direct probe of N_{it} generated by hot-carrier stress in our short channel NMOS devices.

DEDICATION

To those who are pursuing democracy

for my homeland ——— *CHINA*

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Chapter 1 Introduction

As the basic element in VLSI circuits, MOSFETs have been extensively studied for various performance characteristics and technological improvements. Much effort has been expended on the reliability physics of MOSFETs. For example, hot-carrier-induced MOSFET degradation due to the $Si-SiO_2$ interface states has attracted a great deal of interest.

It has been shown that $Si-SiO_2$ interface states play an important role in the degradation of MOSFETs, and there has been many methods developed to determine this kind of degradation. However, these methods can be classified into two major categories: one is concentrated on the performance degradation of the devices by measuring, for example, the degradation of the maximum trans-conductance g_m, changing of the subthreshold properties and the shifting in threshold voltage. These performance degradation characterizations mostly concentrate on the DC parameters of the devices, hence we can call them the DC performance methods. The other category concentrates on the determination of the $Si-SiO_2$ interface state properties, such as the spatial and energy distributions of the interface state by using the charge pumping and 1/f noise measurements. The correlations between the DC measurement and the interface states were demonstrated by many authors. In my M.A.Sc. thesis project, I conducted the DC performance test, charge pumping measurements and low frequency noise measurements to study the hot-carrier-injection degradation in MOSFETs. The motivation for doing all these measurements was to find a reliable probe for $Si-SiO_2$ interface states and their characteristics. So that we can investigate the interface states generation as a function of the electrical stressing time, which is

important for understanding the failure mechanism of MOSFETs.

The significance of my thesis work is its contribution to the understanding of $Si-SiO_2$ interface states and the MOSFET degradation studies by introducing a new charge pumping method for determining the spatial distribution of the interface states, and a new physical model for the low-frequency noise of MOSFET in saturation.

The new spatial profiling charge-pumping technique provides a direct probe of the spatial distribution of $Si-SiO_2$ interface states. It allows us to detect interface states near the source and drain independently. No assumption on the interface state distribution is needed.

The physical model for low-frequency noise at saturation is based on the mobility fluctuation model. By introducing a two region distribution of the channel carriers along the channel, we formulated the 1/f noise as a function of the DC bias conditions. Very good agreements have been found between the theoretical predictions and our experimental results.

DC measurements have been taken to examine the hot-carrier-injection-induced degradations. As expected, our NMOS devices showed steady decrease in performance characteristics as the stressing time increases. For instance, a steady decrease of maximum trans-conductance g_m and a steady increase of the maximum substrate current were observed. That was a result of the increasing negative charge-trapping in the $Si-SiO_2$ interface, and the decreasing mobility as a result of increased interface scattering.

Chapter 2 Theoretical Background

In this chapter, the theoretical background to the techniques involved in our research is presented.

There are three major sections in this chapter dealing with theories about: (1) the Charge Pumping technique, (2) DC parameter measurements for hot-carrier-injection induced degradations, and (3) low frequency noise of MOSFETs. These are all related to properties of Si-SiO_2 interface states in MOSFETs, and hence are described together in this chapter.

The charge pumping technique has been proven to be a reliable probe of Si-SiO_2 interface states, such as the total number of states, the energy and spatial distributions, and the variation of these quantities as a function of hot-carrier-injection stress. There are many DC parameters which are sensitive to the interface states and they may also be used as probes of the interface state densities. The low frequency noise or 1/f noise in MOSFETs has basically been understood as a result of tunneling carriers trapping by the interface states and mobility fluctuations caused by interface state scattering. Therefore, it is possible to obtain Si-SiO_2 interface state information by studying the low frequency noise spectra.

§2.1 Charge Pumping Theory

The charge-pumping technique was developed by Brugler and Jespers in 1969 [Brug69]. They applied periodic square pulses to the gate of a MOSFET whose source and drain were connected to ground. The average substrate current was monitored. It was

Conventional Setup: $V_D = V_S$

New Setup: $V_D \neq V_S$

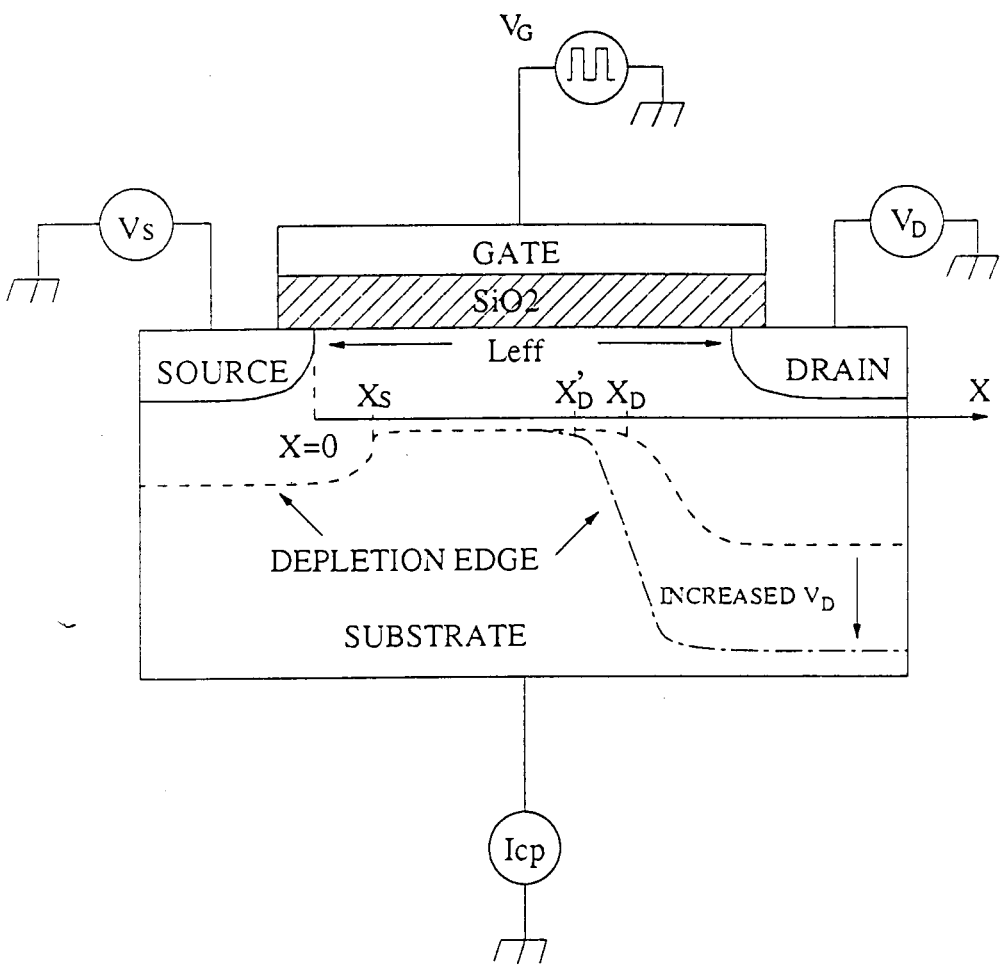

Figure 2.1 Schematic Diagram of Charge Pumping Test Circuit

observed that, in addition to the expected a.c. displacement current, an extra d.c. component of substrate current was present. This d.c. current is the so-called charge pumping current. The schematic structure of the test circuit is shown in figure 2.1.

There are two principal mechanisms proposed to explain the charge pumping substrate current effect, and they both involve the transfer of charge from the source and drain terminals to the substrate in the assistance of recombinations and generations. One of the proposed mechanisms is the charge pumping current associated with the $Si-SiO_2$ interface traps. This part of the charge-pumping current provides the information on the interface state which plays an important role in reliability physics of MOSFET. The other part of the charge pumping substrate current is from bulk recombination in the substrate, which is called geometry current and provides no information on the interface states.

When the channel is pulsed back and forth between inversion and accumulation, there will be either recombination of inversion-layer charges through bulk traps and recombination centers when the channel is in inversion, or recombination of interface state trapped charges with electrons or holes from source and drain when the channel is turned into accumulation.

The recombination through the bulk traps and recombination centers forms the geometric current which is not a desirable part of the charge pumping current. For example, in an n-channel MOSFET, if the gate voltage changes quickly from inversion to accumulation, the electrons, which temporarily remain at the surface, attract holes from the substrate in order to satisfy charge neutrality. The induced electrical field and

concentration gradient result in the transport of holes to the surface and electrons toward the substrate. The electron flow is due to recombination through either bulk traps or recombination centers at the ohmic substrate contact.

Because the amount of the inversion layer charge injected into the substrate through bulk recombination is a function of the channel length and width, this component of substrate current has been named as geometric current. The geometric current should be reduced as much as possible since it contains no information on the interface traps. There are many ways to reduce the geometric current. A simple way is to reduce the geometry of the substrate to reduce the current. Increasing the gate pulse frequency can also reduce the geometric current since the bulk recombination can not follow up the gate pulse at very high frequency, e.g. 50KHz or greater.

The recombination of the interface state trapped charge forms the other part of the substrate current. For instance, when the channel of an NMOS transistor is in accumulation mode, the interface trapped electrons will be recombined with the holes. This part of the substrate current is proportional to the interface trap density, the effective gate area and the a.c. pulse frequency. Knowing the effective gate area and pulse frequency, we can determine the trap density at the $Si-SiO_2$ interface which can be used to evaluate the degradation of the MOSFETs. By varying the drain and source bias voltage, we can change the effective channel length thereby obtaining information on traps in different parts of the channel. In this way, the spatial distribution of the interface trap density can be measured. The energy and time constant distribution of the interface trap can also be found by varying the gate pulse

amplitude and rise-fall times. There are two major methods developed to determine these distributions from the experimental charge pumping current. The earlier model was proposed by Groeseneken *et al* [Groe84]. In order to overcome the difficulty in determining the transient process during the rise-fall-time, Tseng [Tsen87] developed the Staircase Charge Pumping method in 1987.

A comprehensive study of charge pumping was carried out by Groeseneken and his co-workers in 1984 [Groe84]. Recombination through the interface traps during the rise and fall transitions was described by a transient ***Shockley-Hall-Read*** (SHR) recombination model developed by Simmons and Wei [Simm73a,b]. As an extension of the conventional ***SHR*** [Shoc52] theory, the transient ***SHR*** theory is capable of analyzing situations where the emission and capture of interface-trapped charge are not in steady-state conditions. Since the probability of occupancy of a particular trap is a function of time, the transient recombination parameters, such as electrons' and holes' capture cross sections, are required to determine the transient recombination during the rise-fall-time. However those parameters are not easy to determine. This is the principal drawback of the charge pumping technique described by Groeseneken [Groe84].

In addition to the above two sources of the charge pumping substrate current, the reverse current of the source and drain p-n junctions was found to be bothersome when we applied higher source and drain reverse bias voltages to reach the central part of the channel (at bias voltage ~ 6V for some of our test devices). This part of substrate current can be avoided by using smaller bias voltages, or by subtracting the DC leakage current

from the charge pumping current.

The charge pumping current without considering the transient recombination for a square wave pulse can be found from the basic Groeseneken equation [Groe84]. The total charge involved in the charge pumping process can be determined by the integration over the energy interval swept by the gate pulses, and is given by

$$Q_{ss} = A_{eff} \cdot q \cdot \int N_{it}(E) dE$$
$$= A_{eff} \cdot q^2 \cdot \overline{N}_{it} \cdot \Delta\psi_s \quad . \tag{2.1.1}$$

These charges are being moved at frequency f, and they form the charge pumping substrate current I_{cp} given by:

$$I_{cp} = f \cdot Q_{ss}$$
$$= f \cdot A_{eff} \cdot q \cdot \overline{N}_{it} \cdot q\Delta\psi_s \quad . \tag{2.1.2}$$

In the above equations A_{eff} is the effective area of the gate. It is better to use the effective gate area instead of the mask gate area because only the charges under the effective gate area participate the charge pumping process and f is frequency. The interface trap energy density and its average value are denoted by N_{it} *and* $\overline{N}_{it}$ respectively, and $\Delta\psi_s$ is the total sweep of the surface potential.

Considering the transient process, charge pumping current

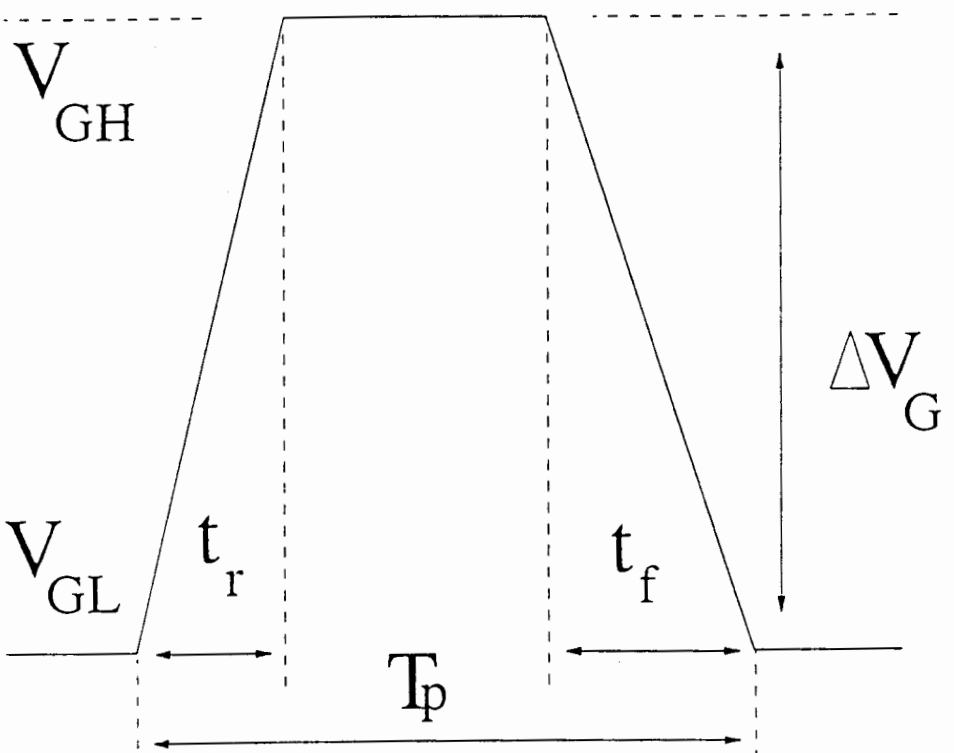

Figure 2.2 Square Pulse in Charge Pumping Measurement

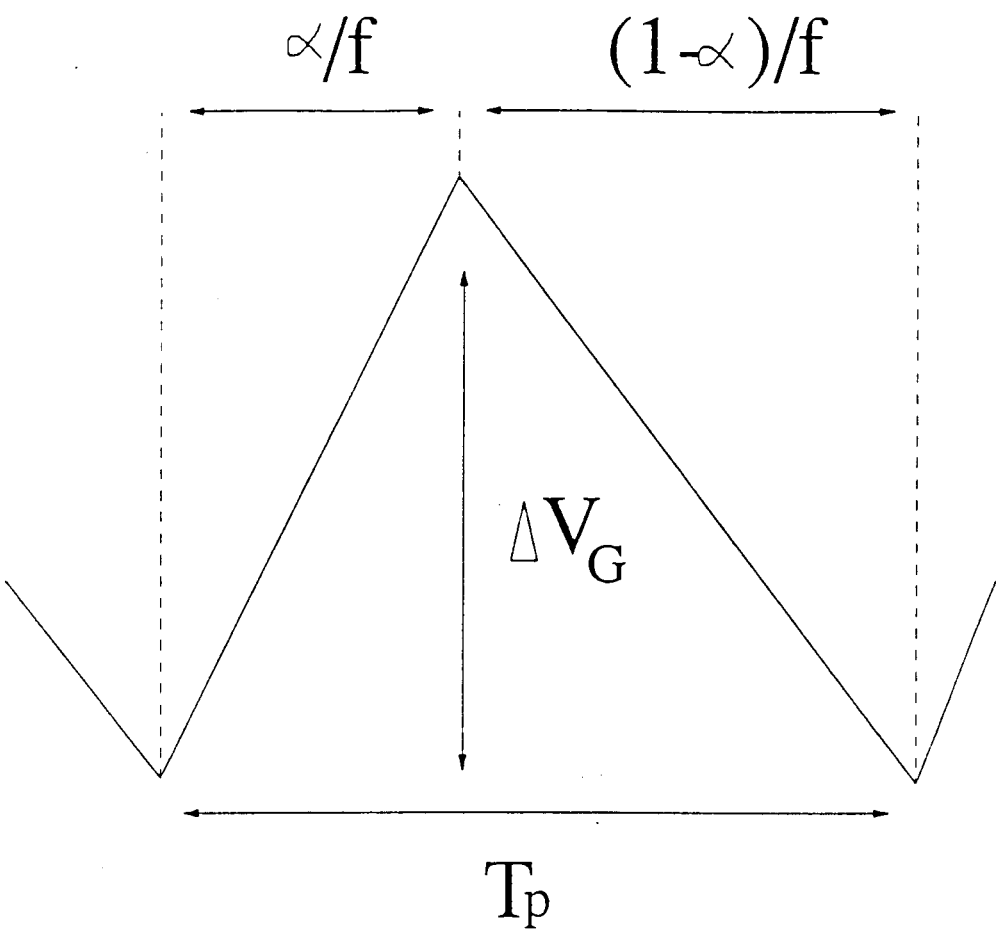

Figure 2.3 Saw-tooth Pulse in Charge Pumping Measurement

can be described by the following modified Groeseneken equations. For the square pulse shown in figure 2.2, the substrate current is:

$$I_{cp} = 2 \cdot q \cdot f \cdot A_{eff} \cdot \overline{N}_{it} \cdot KT \cdot \left\{ \ln(v_{th} \cdot n_i \cdot \sqrt{\sigma_n \cdot \sigma_p}) + \ln\left(\frac{|V_{FB} - V_T|}{|\Delta V_G|} \cdot \sqrt{t_f t_r} \right) \right\} \quad . \qquad (2.1.3)$$

For saw-tooth pulses in figure 2.3, the charge pumping current can be given by:

$$I_{cp} = 2 \cdot q \cdot f \cdot A_{eff} \cdot \overline{N}_{it} \cdot KT \cdot \left\{ \ln(v_{th} \cdot n_i \cdot \sqrt{\sigma_n \cdot \sigma_p}) + \ln\left(\frac{|V_{FB} - V_T|}{|\Delta V_G|} \cdot \frac{1}{f} \cdot \sqrt{\alpha \cdot (1-\alpha)} \right) \right\} \quad . \qquad (2.1.4)$$

The shape dependence of the pulse in I_{cp} is included in equations (2.1.3) and (2.1.4). These equations give better frequency dependency of I_{cp} than equation (2.1.2), especially for the saw-tooth pulses. However, the capture cross sections σ_n, σ_p for electrons and holes have to be determined before (2.1.3) and (2.1.4) can be used.

§2.1.1 Energy Profiling of Interface States

There are many ways to use the charge pumping technique to determine energy distributions of the interface states [Tsen87, Cili90, Saks91]. Recently, the stair-case charge pumping (SCP) method [Tsen87, Chun89, Saks91] has been used in many charge pumping measurements to get rid of the difficulty in parameter determination of transient processes. The stair-case charge pumping method also provides a way of determining the energy distribution of interface states and

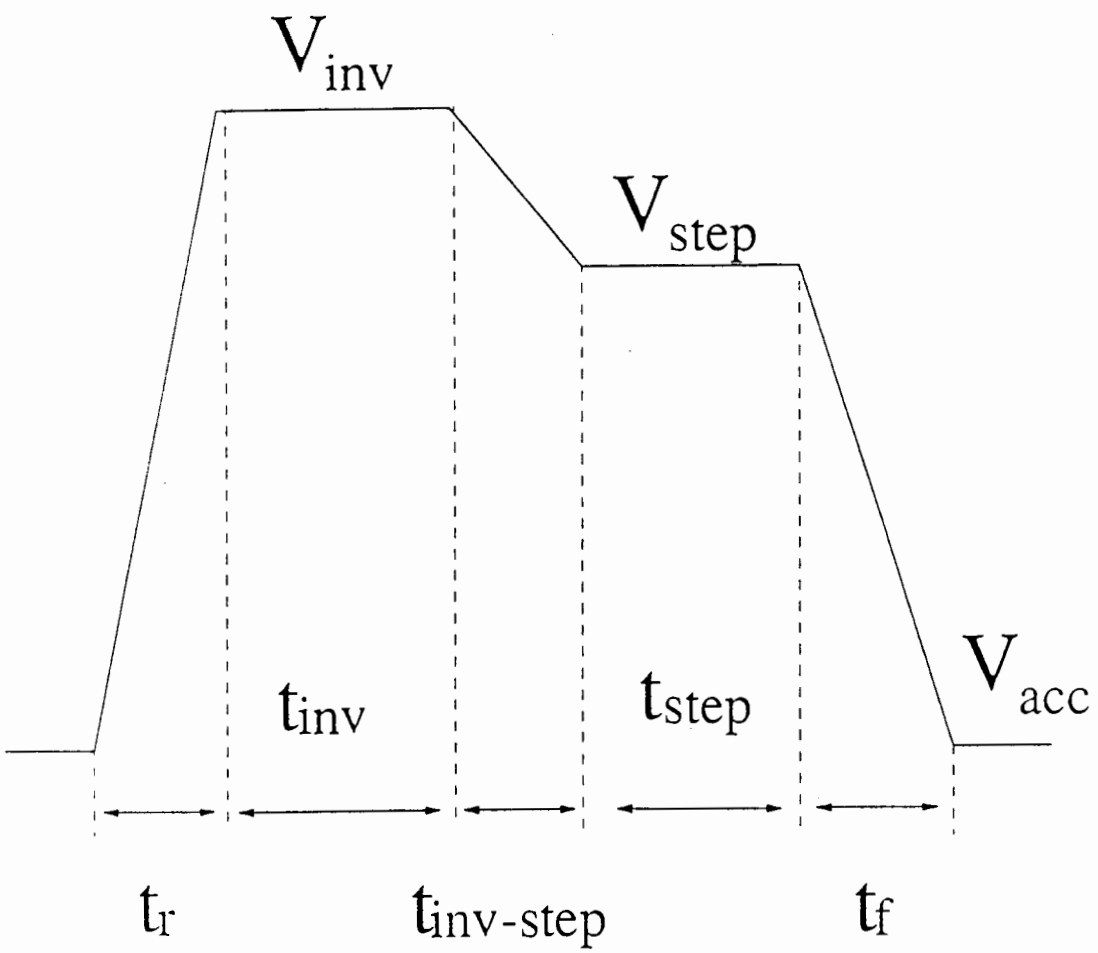

Figure 2.4 Stair-case Pulse in Charge Pumping Measurement

trap cross sections of electrons and holes [Saks91].

The basic idea of **SCP** [Tsen87, Chun89] is to perform the charge pumping measurement in the upper-half of the band gap for n-channel devices and the lower-half of that for p-channel devices without requiring complex modeling or the use of numerous fitting parameters. The **SCP** technique also gives a better physical understanding of the charge pumping mechanism. However, the **SCP** cannot be conducted in our lab now due to the lack of a required three-level wave function generator to produce the staircase pulses.

The staircase pulse employed in the **SCP** measurement is shown in figure 2.4. The timing parameters of the **SCP** pulse such as T_r, $T_{inv-step}$ and T_f are chosen to be much longer than the dielectric relaxation time to ensure that electrons and holes in the conduction and valence bands are in dynamic equilibrium with the gate bias at all time.

Assume that the device experienced two steps when the device changes from accumulation into inversion by the stair-case gate pulse, and assume there is a constant demarcation energy E_d level as well.

In the first step, when the gate bias increases, the interface traps will be filled by holes (the following discussion is for n-channel device, except otherwise specified) emitted to the substrate from the accumulation Fermi energy level E_{acc} to the demarcation level E_d, and in the second step the traps will be filled by electrons from source and drain from E_d to the inversion Fermi level $E_{F(inv)}$.

The charge pumping current of the staircase gate pulses can be found as:

$$I_{cp} = f \cdot Q_{sub.}$$

$$= f \cdot q \cdot A_{eff} \cdot \int_{E_d}^{q\psi_{step}} N_{it} dE \qquad (2.1.5)$$

Assume that E_d *is a constant* when $q\psi_{step}$ and $q\psi_{inv}$ changes, then the interface state density N_{it} can be found by the derivative of equation (2.1.5) as:

$$\frac{dI_{cp}}{d(q\psi_{step})} = f \cdot q \cdot A_{eff} \cdot N_{it}(E)|_{E=q\psi_{step}} \qquad (2.1.6)$$

from which, we have:

$$N_{it}(E)|_{E=q\psi_{step}} = \frac{1}{f \cdot q \cdot A_{eff}} \cdot \frac{dI_{cp}}{d(q\psi_{step})} \qquad (2.1.7)$$

Therefore, by varying $q\psi_{step}$, the energy band can be swept, and the energy distribution of the surface state density can be found from equation (2.1.7).

§2.1.2 Spatial Profiling of Interface States

The spatial profile of interface states along the channel is another major property of N_{it}. It is also important in the hot-carrier-injection degradation of MOSFETs. Many researchers are very interested in determining where most of the hot-carrier-injection stress damage is located in the device. Although there are many hypotheses and indirect evidences about the spatial distribution of N_{it}, no effective charge pumping technique has been available to probe N_{it}

spatially. Many authors have adapted the charge pumping technique for determining the N_{it} distribution along the channel [Maes82, Here89, Plos88, Saks90]. However, all these previous researchers used many assumptions on the distribution of N_{it} itself, because the source and drain are usually connected together. In my thesis project, we developed a new spatial profiling charge pumping technique to get rid of these assumptions on N_{it}, so that we can determine the spatial profile of N_{it}. We use separated source and drain bias voltages in the new method. More details about the new method can be found in Chapter §3.

The charge pumping can be performed by applying the simple square gate pulses shown in figure 2.2 to the test device. If we fix the amplitude ΔV_G ($|\Delta V_G| > |V_{FB}-V_T|$) of the pulse and change the base level of the pulses V_{GL}, we expect to get I_{cp} as a function of V_{GL} as shown on figure 2.5.

In the charge pumping process, the base level of gate pulses changes relatively to the threshold and flat band voltage as shown on the lower part of figure 2.5. When V_{GL} is so low that V_{GH} is lower than V_{FB}, the device stays in accumulation all the time and no electron from the source or drain can be trapped by interface states, therefore no charge pumping current can be measured. Similarly, when V_{GL} is higher than V_T, the device stays in inversion all the time, and no holes from the substrate can be attracted to the interface to recombine with the trapped electrons from the source or drain, therefore no charge pumping current can be measured either. I_{cp} can only be measured when the device can be pulsed back and forth between accumulation and inversion.

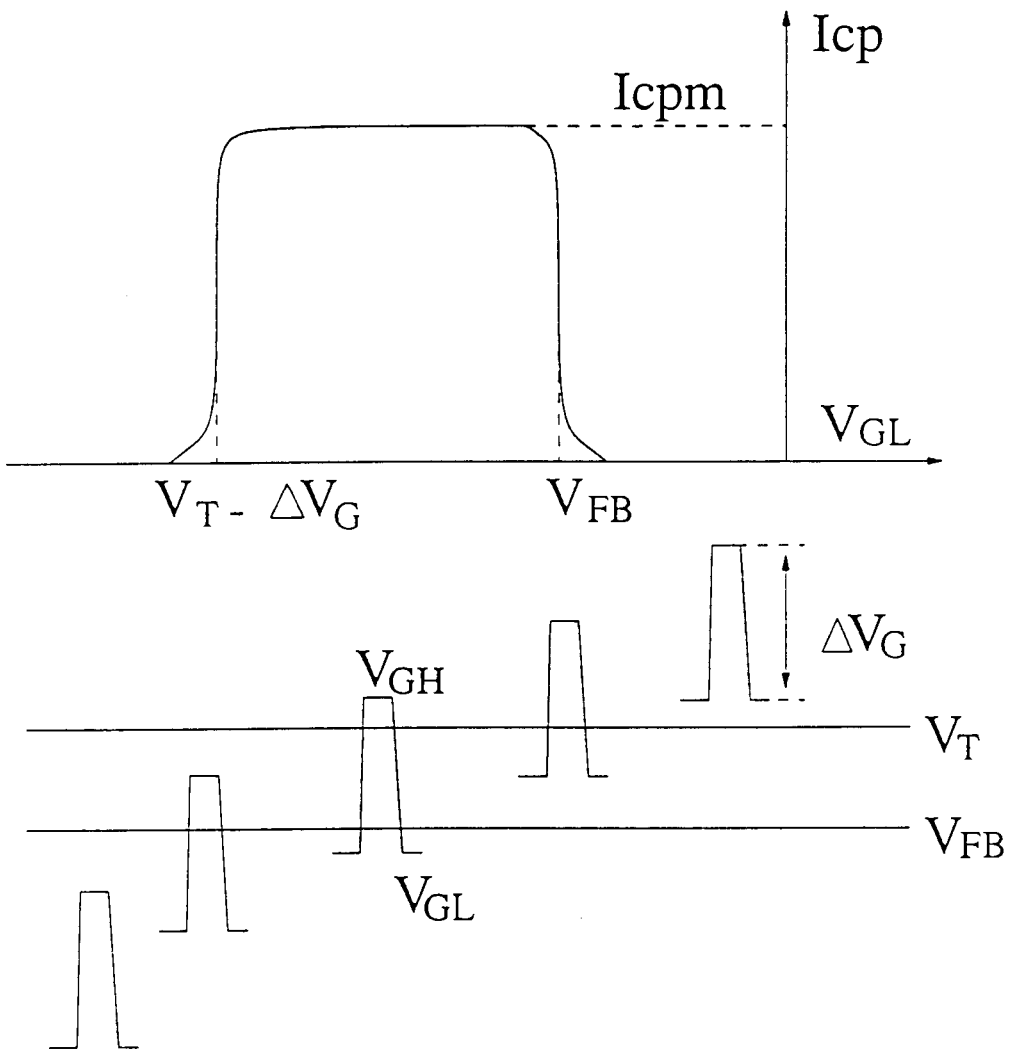

Figure 2.5 I_{cp} Dependence on V_{GL}

From equation (2.1.3), the maximum charge pumping current I_{cpm} on figure 2.5 can be used to obtain energy average of interface state density $\overline{N}_{it}$, and the shift along the V_{GL} axis on figure 2.5 can be used to determine the change of any fixed charge in the interface which can affect the flat band and threshold voltages.

During the period in which the device is pulsed between accumulation and inversion, we can reasonably assume that the change of surface potential is $\Delta\psi_s \approx 2\phi_F$, and use I_{cpm} in equation (2.1.2) to determine the energy average of interface state density. $\Delta\psi_s$ is a complicated function of the device bias conditions. However, if gate pulse amplitude ΔV_G is big enough to pulse the device between deep inversion and accumulation, $\Delta\psi_s$ will be close to $2\phi_F$.

It is known that in the depletion region, the carrier density is relatively low, and therefore the generation and recombination rate is low in the depletion layer. Interface states screened by the depletion layer will not contribute to the charge pumping substrate current. The basic idea of using the charge pumping technique to measure the spatial distribution of N_{it} is to apply different drain and source bias voltages to change the width of the drain and source depletion layer to screen different parts of the channel. Thus we can determine N_{it} contribution from different parts in the channel and therefore measure the spatial distribution of the interface states along the channel.

§2.1.3 Conventional Charge Pumping Technique

In this section, we will present a brief description of a typical conventional charge pumping technique for determining the spatial distribution of N_{it} and we will show the deficiency of the old method. To solve the problems associated with the old method, a new method will be discussed in Chapter §3. The old method conducts the charge pumping measurement with the drain and source connected together. Changing of drain and source reverse bias will result in a simultaneous change of depletion edges near both source and drain junctions.

We use I_{cp0} to denote the charge pumping substrate current of the 'virgin' device as a function of the reverse voltage at drain and source (V_S=V_D):

$$I_{cpo} = f \cdot q \cdot W \cdot q\Delta\psi_{so} \int_{-L(V_D)/2}^{+L(V_D)/2} N_{it}(X)dX \tag{2.1.8}$$

Note: the origin of the coordinate system is in the center of the channel.

Assume $N_{it}(X) = N_{ito} = const.$, then

$$\begin{aligned} I_{cpo} &= q \cdot f \cdot W \cdot q\Delta\psi_{so} \cdot L(V_D) \cdot N_{ito} \\ &= q \cdot f \cdot A_{eff} \cdot N_{ito} \cdot q\Delta\psi_{so} \end{aligned} \tag{2.1.9}$$

where $L(V_D) = L_{eff} - 2\sqrt{\frac{2\varepsilon_{si}}{qN_B}(V_D + 2\phi_F)}$ *and*

$$A_{eff} = W \cdot L(V_D) \tag{2.1.10}$$

are the effective channel length and effective gate area due to the change of depletion edges under the drain and source

bias voltage V_D.

After the hot-carrier-injection (HCI) stress, consider the interface state density to be a function of position along the channel, the charge pumping substrate current can be found as:

$$I_{cp} = q \cdot f \cdot W \cdot q\Delta\psi_{so} \int_{-L(V_D)/2}^{+L(V_D)/2} N_{it}(X)dX \qquad (2.1.11)$$

Assuming that the interface states density N_{it} near the source end of the channel remains in constant after the HCI stress, i.e.

$$N_{it}(-L(V_D)/2) = N_{ito} \qquad (2.1.12)$$

the derivative of the I_{cp} in equation (2.1.11) as a function of drain and source to substrate bias voltage V_D can then be obtained as:

$$\frac{dI_{cp}}{dV_D} = \frac{q \cdot f \cdot W \cdot q\Delta\psi_{so}}{2} \cdot \frac{dL(V_D)}{dV_D} [N_{it}(L(V_D)/2) + N_{ito}] \quad . \qquad (2.1.13)$$

The interface state density at the drain depletion edge can be solved from the above equation as follows:

$$N_{it}(L(V_D)/2) = \frac{2}{q \cdot f \cdot W \cdot q\Delta\psi_{so}} \cdot \frac{dI_{cp}}{dV_D} \cdot \left(\frac{dL(V_D)}{dV_D}\right)^{-1} - N_{ito} \quad . \qquad (2.1.14)$$

In the above procedure, two basic assumptions were used. One is that N_{it} is a constant along the channel for a virgin device. The other is that N_{it} near the source does not change after the hot-carrier-injection stress equation (2.1.12). We

will find out from our experiment results that those assumptions are not always valid. Therefore, we need a method without these assumptions.

§2.2 DC Measurement of Performance Degradation

The stress degradations of g_m was reported by many authors [Lo90, Kusa88, Here86, Hori87, Yang88]. The dependence of $\Delta g_m/g_{mo}$ was shown to be proportional to the stressing time t in logarithm scale as:

$$\Delta g_m/g_{mo} \sim t^{\alpha_{g_m}} \tag{2.2.1}$$

The trans-conductance degradation is mainly caused by the μ_{eff} degradation. The strong dependence of μ_{eff} on the distance between the interface charges and the carriers was discussed in [Chen74] and the positive fixed charges, and/or interfacial electron traps on μ_{eff} have stronger effects on μ_{eff} degradation than the oxide bulk trapped charges [Chen74, Schm88, Hsu84]. Therefore the degradation of g_m can be an indirect probe of the $Si-SiO_2$ interface properties.

The interface properties can also be detected by the degradation of subthreshold properties [McWh86, Saks87, Here86].

Hot carriers, high-field stress, ionizing radiation and many other conditions can lead to V_{th} shift in MOSFET. The change of interface trap density N_{it} is not the only cause of the V_{th} shifting. When using the shift of V_{th} as a probe of interface traps, one should notice that the trapped-oxide charge N_{ot} can also cause a shift in V_{th} [McWh86], *i.e.*

$$\Delta V_{th} = \Delta V_{N_{it}} + \Delta V_{N_{ot}} \tag{2.2.2}$$

V_{th} was found to increase as approximately the square root of the stress time in literature [Saks87] at both 77K and 300K. However, we can not conclude that the interface states also change with stress time in this way because there are other charge change may contribute to V_{th} shift.

A method to split the two major causes of V_{th} shifting was introduced in [McWh86], where they found that $|\Delta V_{N_{ot}}| > |\Delta V_{N_{it}}|$, and a decrease in V_{th} was found. That means the positive charge traps are dominant in the causes of V_{th} shifting. The same results were also found by P. Heremans [Here86] for the n-channel MOSFET. Because of the amount of trapped holes is much larger than the amount of the interface states which can trap electrons, in literatures [McWh86, Saks87, Here86], they all found that the shift of V_{th} is due to a net positive charge which is the trapped holes but not the interface state traps' contribution. So that V_{th} detection is not sensitive enough to be a probe of interface states unless we can split the two contributions to ΔV_{th} [McWh86].

In summary of the two DC methods, it has been shown that $\Delta g_m/g_{mo}$ is strongly correlated to the interface states generation [Lo90, Kusa88, Hori87, Yang88, Take83]. The experimental results in [Lo90, Take83] show that the following relationship

$$\Delta g_m/g_{mo} \quad \propto \quad (\Delta N_{it}/N_{ito})^{\alpha_{N_{it}}} \tag{2.2.3}$$

is well satisfied. This makes trans-conductance g_m degradation to be a powerful probe of the interface (surface) state generation in MOSFET degradation.

On the other hand, V_{th} change is not a direct indicator of

the interface states degradation. More work is needed to separate the contribution of the interface states from the trapped charge in the oxide [McWh86].

§2.3 1/f Noise Theory

There are many models and theories proposed to characterize the low frequency noise in MOSFETs [Ziel88b, Hung90]. Low frequency noise in MOSFETs is contributed from both the bulk and interface noise [Hoog81]. All the theories can be sorted into three categories. One is mobility fluctuation theory started from the well known Hooge's empirical relation [Hoog76] in describing the bulk origin of low frequency noise in metals and semiconductors. This theory is also known as the mobility fluctuation theory [Hoog76,81, Vand80a,b, Klei81, Ziel82, Ziel88b]. However, the mobility fluctuation theory now is no longer limited to the bulk mobility fluctuations, and more attention is paid to interface-scattering-caused mobility fluctuations. The second one is the number fluctuation theory based on the McWhorter's interface charge trapping model [McWh57, Chri68, Berz70, Hsu70, Klaa71, Fu72, Vand80b, Celi85, Sury86, Ziel88b, Klei90]; And the third one is the unified theory [Hung90, Grab89a,b, Ziel88b, Grab88, Sury88, Miko82] considering the fact that the number fluctuation and the mobility fluctuation are strongly correlated to each other.

For years, a huge amount of noise data have shown almost equal support to either one of the first two counterparts [Hafe89, Vand89, Grab88, Haya88, Hend88, Ziel88a, Clev87, Fang86a,b, Maes85, Uren85, Reim84, Steg84, Aoki82, Miko82, Park82a,b, Ziel82, Park81, Hoog81, Back80, Vand80a,b, Hoog78,

Aoki77, Hoog76, Klaa71, Chri68b]. It seems that none of them is superior to the other in describing low frequency noise behavior in MOSFETs. However, it is also quite clear that the Hooge's empirical relation cannot be used with its simple form. The physical meaning of Hooge's noise parameter as well as its spatial dependence have to be worked out to achieve better agreement with the experimental results. The lack of a physical explanation of Hooge's noise parameter has been an obstacle for further development of the Hooge's mobility fluctuation theory [Ziel88a]. On the other hand, the number fluctuation theory has plenty of room for further expansion because the physical concepts involved are much clearer. Even so, the number fluctuation theory alone is still not a universally accepted theory for 1/f noise in MOSFETs. Due to the above reasons, there emerges the third theory, an unified noise theory trying to combine the two noise theories [Hung90, Ziel88]. The unified 1/f noise theory is based on the knowledge that the carrier number fluctuation and the mobility fluctuation are so strongly correlated to each other that they can not be considered as separated in most cases.

§2.3.1 Mobility Fluctuation Theory

The bulk origin of low frequency noise in metal and semiconductors can be described by Hooge's empirical relation [Hoog76]:

$$S_V/V^2 = \alpha/fN \tag{2.3.1}$$

Where α is the 1/f noise parameter and N is the total number

of charge carriers in the homogeneous sample subjected to homogeneous field.

α has been found to be 2×10^{-3} for variety of materials [Hoog81]. The experimental accuracy was not enough to determine if there is any material dependence of α.

In order to practically measure the 1/f noise, carrier number $N < 10^{13}$ is desirable to measure 1/f noise above the thermal noise in the frequency range of 1 Hz to 10KHz without applying too much current to the sample [Vand89].

The validity of the empirical relation has been found for a large number of materials such as metal films, homogeneous GaAs crystal and etc. By considering effective concentration and thickness, the results of 1/f noise from an ion-implanted layer in Si can also be interpreted with Hooge's empirical relationship.

The typical procedure of applying Hooge's empirical relation to structures more complicated than homogeneous samples is to consider the structure to be a combination of small homogeneous volumes on which the empirical relation can be applied. The noise of the whole structure due to bulk mobility fluctuation can then be found by integrating all the small volumes over the whole sample. However, this procedure cannot be easily applied to MOSFETs, even though it gives good results for some other structures [Vand89].

There are many models for 1/f noise in MOSFETs utilizing the mobility fluctuation mechanism [Ziel88a,b, Ziel82, Hoog81, Klei81, Vand80a,b] as well as many experimental results in support of mobility fluctuation mechanism [Hend88, Hoog78, Hoog81, Park81, Park82a,b, Vand80a,b, Vand89, Ziel82, Ziel88a].

The ac short circuit, drain current noise spectral density can be found from the Langevin spatial cross spectral density:

$$S_{I_D}(f)=\frac{1}{L^2}\int\int_0^L S_H(x,x',f)dxdx' \tag{2.3.2}$$

where the Langevin spatial cross spectral density is given by:

$$\begin{aligned} S_H(x,x',f) &= \frac{I^2}{\mu^2(x)}S_\mu(x,x',f) \\ &= \frac{\alpha(x,E)I^2}{fn(x)}\delta(x-x') \end{aligned} \tag{2.3.3}$$

In the above equation, the Hooge's parameter α is considered as a function of position in the channel as well as a function of electric field.

This is a direct application of Hooge's empirical relation to the Langevin noise source term. For MOSFETs, the drain current noise spectral density can be written as [Ziel88]:

$$\begin{aligned} S_{I_D} &= \frac{\alpha I_D^2}{fL^2}\int_0^L \frac{dx}{n(x)} && (GeneralForm) \\ &= \frac{\alpha q \mu_D V_D}{fL^2} && (LinearForm) \end{aligned} \tag{2.3.4}$$

This equation is a simplified expression for Hooge's relation which contains the following assumptions:

1) the Hooge's parameter α is constant along the channel (both general form and linear form);

2) electron mobility μ and $d\mu/dE$ are constant along the channel (linear form);

The validity of equation (2.3.4) is limited by the above assumptions.

If we consider only the spontaneous fluctuation of mobility as the source of 1/f noise, taking into account the spatial dependence of Hooge's parameter and the mobility, the drain noise spectral density can then be worked out by substituting equation (2.3.3) into (2.3.2):

$$S_{I_D} = \frac{I_D^2}{fL^2}\int_0^L \frac{\alpha(x,E)dx}{n(x)} \tag{2.3.5}$$

It is very hard to compare the experimental results with noise predicted by equation (2.3.5) since the spatial dependence of $\alpha(x)$ is unknown. This problem can only be solved by determining the physical model for α. However, in some cases such as weak inversion, the field and spatial variation of mobility may be relatively small and a constant Hooge's parameter can be expected.

By putting different expressions for the drain current as a function the gate bias into equation (2.3.4), for different operating modes of the device, the drain current noise spectral dependence on gate bias has been experimentally verified by different authors. For example, in linear or ohmic region [Vand80a, Ziel82, Ziel88b], when V_D is small, substituting the well known drain current expression:

$$I_D = \frac{\mu W C_{ox}}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \tag{2.3.6}$$

and

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{\mu, V_D}$$

$$= \frac{\mu W C_{ox}}{L} V_D \qquad (2.3.7)$$

into equation (2.3.4), then the gate referred voltage noise spectra can be found as:

$$S_{VG}(f) = \frac{S_{I_D}(f)}{g_m^2}$$

$$= \frac{q\alpha}{fWLC_{ox}}\left(V_G - V_T - \frac{1}{2}V_D\right) \quad . \qquad (2.3.8)$$

Note that in equation (2.3.7), the gate voltage dependence of mobility was ignored.

Considering the simple gate voltage dependence of mobility with a none-zero surface mobility degradation factor θ:

$$\mu = \frac{\mu_o}{1 + \theta(V_G - V_T)} \quad , \qquad (2.3.9)$$

we can rewrite the equation of drain current and the expression of trans-conductance as following:

$$I_D = \frac{WC_{ox}}{L}\frac{\mu_o}{1 + \theta(V_G - V_T)} \cdot \left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \qquad (2.3.10)$$

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D}$$

$$= \frac{\mu W C_{ox}}{L} \cdot \frac{1 + \frac{1}{2}\theta V_D}{1 + \theta(V_G - V_T)} V_D \qquad (2.3.11)$$

and in turn the gate referred voltage noise spectra for MOSFETs in linear region can be rewritten as:

$$S_{VG}(f) = \frac{S_{I_D}(f)}{g_m^2}$$

$$= \frac{q\alpha}{fWLC_{ox}} \cdot \left(V_G - V_T - \frac{1}{2}V_D\right) \cdot \left[\frac{1+\theta(V_G - V_T)}{1+\frac{1}{2}\theta V_D}\right]^2 \qquad (2.3.12)$$

The validity of this equation is limited by the above drain current equation (2.3.10) which holds for small V_D, and also equation (2.3.8) which does not include the lateral electrical field effect on the mobility.

A similar bias dependence of $S_{VG}(f)$ was also found by Grabowski [Grab88] from a different approach where phonon density fluctuation was considered as the source of mobility fluctuation instead of Hooge's empirical relation. If the V_D term in g_m was not neglected in his equation (26), his results should be read as the following:

$$S_{VG}(f) = \frac{S_{I_D}(f)}{g_m^2}$$

$$= \frac{q^2 K (C_{ox}/q)^m (V_G - V_T)^m}{fWLC_{ox}^2 \mu_o^2 \ln(\tau_{\mu 2}/\tau_{\mu 1})} \cdot \left[\frac{1+\theta(V_G - V_T)}{1+\frac{1}{2}\theta V_D}\right]^2 \qquad (2.3.13)$$

where it was claimed that $m \approx 2.2$, and $\tau_{\mu 1}$, $\tau_{\mu 2}$ are the minimum and maximum relaxation time of mobility fluctuation. K is a function of several parameters, such as scattering center density in the interface, coefficient of phonon scattering, coefficient of transfer of phonon fluctuation to mobility fluctuation and the scattering center density per unit volume along the channel. All these parameters cannot be determined

easily.

It is amazing that if we let

$$m = 1 \quad \text{and} \quad \frac{K}{\mu_o^2 \ln(\tau_2/\tau_1)} = \alpha \quad , \tag{2.3.14}$$

then equation (2.3.13) will be exactly the same as equation (2.3.12), although they were derived from different approaches.

In the non-ohmic region, the bias dependence will be more complicated [Hoog81, Park81, Vand80b, Ziel88b]. In Chapter 4, a new model for the MOSFET 1/f noise in saturation mode is presented.

§2.3.2 Number Fluctuation Theory

Based on the original work of McWhorter [McWh57], it is widely known that the low frequency noise is partly caused by the random trapping and detrapping processes of charges in the oxide traps near the Si-SiO_2 interface [Chri68, Berz70, Hsu70, Klaa71, Fu72, Aoki77, Vand80b, Celi85, Sury86, Ziel88b, Klei90]. The latest theoretical work can be found in [Klei90]. The number fluctuation theory is widely supported by correlations between low frequency noise data and the interface state densities [Hsu70, Klaa71, Fu72, Miko82, Maes85].

It is hard to interpret the relation between interface trap density and the low frequency noise data if the interface trap is treated as the only origin of carrier number fluctuation. As a fact, when the charges in the channel are trapped and detrapped by the interface states through tunneling, the number of carriers will fluctuate. However,

that is not all. The charge number fluctuation will also result in a change in the potential along the channel. The potential fluctuation will, in turn, contribute to the number fluctuations. The modulation of potential fluctuations on the number fluctuations is also an important origin of low frequency noise of MOSFETs. Beyond the correlation between number fluctuation and potential fluctuation, the correlation between number fluctuation and mobility fluctuation is also significant and a unified noise model is needed to describe it. We will discuss unified models in next section.

The energy and spatial distribution of interface state density as well as the potential fluctuation modulation are responsible for different charge number dependence of low frequency noise under different operation mode of MOSFETs.

The classic formula for the 1/f noise in MOSFET associated with the number fluctuations was first discussed by Christensson et al. in 1968 [Chri68]. The gate referred noise spectra caused by electron tunneling from the interface traps can be found as [McWh57, Steg84]:

$$S_{VG}(f)=\frac{q^2kTN_{it}(E_F)}{fWLC_{ox}^2\ln(\tau_2/\tau_1)} \quad . \tag{2.3.15}$$

Where $N_{it}(E_F)$ stands for the *total* number of interface states near the Fermi level.

Please note that in the rest of this section, we will keep using N for *total number* and n for *number densities*.

Equation (2.3.15) is valid only for strong inversion, since it was assumed that the carrier number density fluctuation δn was equal to the trap density near the Fermi

level $n_{it}(E_F)$. It is impossible for the number fluctuation δn to be equal to the trap density $n_{it}(E_F)$ if the total number of carriers is less than $n_{it}(E_F)$ [Klei90]. The same expression was derived by Grabowski in 1984 [Grab84] from a slightly different approach.

While the input referred noise spectra were studied, the drain current noise spectra were also investigated. In 1984, Reimbold [Reim84] presented the normalized drain current fluctuation as:

$$\frac{S_{I_D}(f)}{I_D^2}=\frac{q^4\lambda N_{it}}{fkTLW(C_{ox}+C_d+C_{it}+C_n)^2} \tag{2.3.16}$$

where $\lambda=(\hbar\sqrt{8m^*\phi})^{-1}$ is the tunneling constant of electrons with effective mass m^* in the oxide, ϕ the energy barrier for tunneling electrons, and $\hbar$ the Planck's reduced constant. The capacitances in the denominator are capacitance per unit area of the gate oxide (C_{ox}), the depletion layer (C_d), the interface states (C_{it}), and the carrier charges ($C_n=(q^2/kT)(N/WL)$). N is the total number of carrier charge in the channel. This equation was claimed to be valid from weak to strong inversion.

It was in 1987, Ghibaudo [Ghib87] proved that the Reimbold's expression equation (2.3.15) was identical to the earlier derived gate referred spectra expression in the strong inversion region. A properly expressed trans-conductance in the ohmic operation [Ghib86] could make the connection, that is:

$$g_m = \frac{WC_{ox}}{L} \frac{C_n}{(C_{ox}+C_d+C_{it}+C_n)} \mu_0 V_D \tag{2.3.17}$$

The basic relation between the gate referred spectra and the drain current spectra [Gent81] was used. This work again made it clearer that both formula were good for the strong inversion region.

Considering the gate bias dependence of the effective mobility, the drain current noise spectra can then be written as [Hafe89, Ghib87]:

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{q^4 \lambda N_{it}}{fkTLW(C_{ox}+C_d+C_{it}+C_n)^2} \frac{\mu_{eff}^2}{\mu_0^2} \tag{2.3.18}$$

Substituting equation (2.3.9) into the above equation, and under the strong inversion condition:

$$C_n \gg (C_{ox}+C_{it}+C_d) \tag{2.3.19}$$

the drain current noise spectra then will be as:

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{q^2 \lambda kTN_{it}}{fLWC_{ox}^2(V_G-V_T)^2[1+\theta(V_G-V_T)]^2} \tag{2.3.20}$$

The latest theoretical work on the number fluctuation theory was done by Kleinpenning [Klei90]. In his work, the position dependence of the channel carrier capacitance was considered. He started with the Langevin equation for the noise source terms, and his results can be applied to the operating regions from linear to saturation.

Assuming that the interface trap density n_{it} and mobility μ_{eff} along the channel are constants, then the Langevin spatial cross spectral density source term for the number fluctuation is given by:

$$S_H(x,x',f) = \frac{I_D^2}{n^2(x)} S_n(x,x',f)$$

$$= \frac{\gamma^2 I_D^2 n_{it} \lambda}{f t_{ox} n(x)[\gamma n_{it} + n(x)]} \delta(x-x') \qquad (2.3.21)$$

where

$$\gamma = C_n/(C_d + C_{it} + C_{ox} + C_n) \qquad (2.3.22)$$

and the definition of capacitances are the same as before.

The a.c. short circuit drain current noise spectral density can be found from the above Langevin spatial cross spectral density source term as:

$$S_{I_D}(f) = \frac{1}{L^2} \int\int_0^L S_H(x,x',f) dx dx'$$

$$= \frac{I_D^2 n_{it}}{f L^2 t_{ox}} \int_0^L \frac{\gamma^2 dx}{n(x)(\gamma n_{it} + n(x))} \qquad (2.3.23)$$

Taking into account the position dependence of the channel carrier capacitance, the capacitance noise reduction factor γ in equation (2.3.22) can be rewritten as following:

$$\gamma(x) = \frac{C_n(x)}{C_n(x) + C_{it} + C_{ox} + C_d}$$

$$= \frac{n(x)}{n_0 + n(x)} \qquad (2.3.24)$$

where n_0 is defined as:

$$n_0 = WkT(C_d + C_{it} + C_{ox})/q^2 \tag{2.3.25}$$

The drain current noise spectra for the device can then be derived as:

$$S_{I_D} = \frac{I_D^2 \lambda n_{it}}{f t_{ox} L^2} \int_0^L \frac{dx}{[n_0 + n(x)]\,[n_0 + n_{it} + n(x)]} \quad . \tag{2.3.26}$$

So far, we have not made any assumption on the operating mode of MOSFET.

The integration can be easily worked out under the condition of strong inversion with:

$$n(x) = \frac{WC_{ox}}{q}(V_G - V_T) = \frac{I_D}{(q\mu dV(x)/dx)} \quad . \tag{2.3.27}$$

Therefore, we have:

$$S_{I_D} = \frac{I_D^2 \lambda n_{it}}{f t_{ox} L^2} \int_0^L \frac{dx}{[n_0 + n(x)]\,[n_0 + n_{it} + n(x)]}$$

$$= \frac{I_D^2 \lambda N_{it}}{f t_{ox} N^2 \eta (1 - \eta/2)} \ln\left[\frac{(1 - \eta/r)^{N_0/N_{it}}}{(1 - \eta/s)^{1 + N_0/N_{it}}}\right] \tag{2.3.28}$$

with

$$N_0 = n_0 L\,, \quad r = 1 + N_0/N\,, \quad s = 1 + (N_0 + N_{it})/N\,, \quad \textit{and} \quad \eta = V_D/(V_G - V_T). \tag{2.3.28'}$$

Equation (2.3.28) can be simplified under some typical device operating modes as follows:

$$S_{I_D} = \frac{I_D^2 \lambda N_{it}}{f t_{ox} N^2 \eta (1-\eta/2)} \ln\left[\frac{(1-\eta/r)^{N_0/N_s}}{(1-\eta/s)^{1+N_0/N_{it}}}\right]$$

$$= \begin{bmatrix} \dfrac{I_D^2 \lambda N_{it}}{f t_{ox}(N_0+N)(N_0+N_{it}+N)} & \text{ohmic region, with } \eta = \dfrac{V_D}{(V_G-V_T)} \ll 1 \\ \dfrac{2 I_D^2 \lambda N_{it}}{f t_{ox} N^2 \ln\left(\frac{N}{N_{it}}\right)} & \text{on-set saturation, with } \eta = \dfrac{V_D}{(V_G-V_T)} = 1, \text{ and } N \gg N_{it} \gg N_0 \\ \dfrac{2 I_D^2 \lambda N_{it}}{f t_{ox} N^2 \ln\left(\frac{N}{N_0}\right)} & \text{on-set saturation, with } \eta = \dfrac{V_D}{(V_G-V_T)} = 1, \text{ and } N \gg N_0 \gg N_{it} \end{bmatrix} \quad (2.3.29)$$

In the weak inversion region, with $V_D > kT/q$, the drain current will be dominated by diffusion current:

$$I_D = -qAD_n \frac{dn(x)}{dx} = qAD_n \frac{n(0)-n(L)}{L} \quad (2.3.30)$$

where the effective current flow cross section area A is equal to the channel width times effective inversion depth. Referred to Sze [Sze85], we have:

$$A = W \frac{kT}{qE_x} = \frac{WkT}{q\sqrt{2qN_A \psi_s/\varepsilon_{si}}} \quad (2.3.31)$$

The boundary conditions are:

$$n(0) = n_{po} e^{\beta \psi_s}, \quad \text{and} \quad n(L) = n_{po} e^{\beta \psi_s - \beta V_D} \quad (2.3.32)$$

The surface potential ψ_s is a function of gate bias voltage as follows:

$$\psi_s = (V_G - V_{FB}) - \frac{\alpha^2}{2\beta}\left\{\left[1 + \frac{4}{\alpha^2}(\beta V_G - \beta V_{FB} - 1)\right]^{1/2} - 1\right\} \tag{2.3.33}$$

The integration in equation (2.3.26) can be evaluated as:

$$S_{I_D} = \frac{I_D^2 \lambda n_{it}}{f t_{ox} L^2} \int_{n(0)}^{n(L)} \frac{(-qAD_n/I_D)\,dn(x)}{[n_0 + n(x)]\,[n_0 + n_{it} + n(x)]}$$

$$= \frac{I_D^2 \lambda n_{it}}{f t_{ox} L^2} \frac{(-qAD_n/I_D)}{n_{it}} \ln\left[\frac{n(L) + n_0}{n(0) + n_0} \cdot \frac{n(0) + n_0 + n_{it}}{n(L) + n_0 + n_{it}}\right] \tag{2.3.34}$$

§2.3.3 Unified 1/f Noise Theory

It is quite clear that the noise of MOSFET is a result of combination of the noise from mobility fluctuation and from number fluctuation. The strong correlation between the number fluctuation and the mobility fluctuation has been noticed, and this has led to the introduction of unified noise models. There are many papers published on this issue [Hung90, Grab89a,b, Ziel88b, Grab88, Sury88, Miko82].

The unified theory can be as simple as describing the noise as a sum of noise given by both mobility fluctuation and number fluctuation. For example, the combined formula given by Grabowski [Grab88], is simply a root-mean-square of equations (2.3.13) and (2.3.15):

$$S_{VG}(f) = \sqrt{\left[\frac{q^2 kT N_{it}(E_F)}{f WLC_{ox}^2 \ln(\tau_2/\tau_1)}\right]^2 + \left[\frac{q^2 K (C_{ox}/q)^m (V_G - V_T)^m}{f WLC_{ox}^2 \mu_o^2 \ln(\tau_2/\tau_1)} \cdot \left(\frac{1 + \theta(V_G - V_T)}{1 + \frac{1}{2}\theta V_D}\right)^2\right]^2} \tag{2.3.35}$$

However, one has to keep in mind that the first term in

right-hand-side of equation (2.3.35) is only good for the strong inversion mode, while the second one is only good for the ohmic region. Thus, equation (2.3.35) is valid only in the strong inversion ohmic region, i.e. $V_G - V_T > V_D \sim 0$. The equation cannot be used either subthreshold or saturation operating of MOSFETs.

A unified model from first principles was presented by Hung and his co-workers [Hung90]. Their result incorporated both the number fluctuation and surface mobility fluctuation mechanism, and is valid for both linear and saturation operating mode of the device. Considering the drain current fluctuation is due to contributions from the carrier number fluctuation and the mobility fluctuation, which are coupled by the interface scattering. The drain current noise spectra given by Hung [Hung90] is:

$$S_{I_D}(f) = \frac{kTI_D^2}{\gamma f W L^2} \int_0^L N_{it}(E_f) \left[\frac{1}{N(x)} \pm \alpha\mu \right]^2 dx \tag{2.3.36}$$

By making the following substitution:

$$N_{it}^*(E_f) = N_{it}(E_f)(1 + \alpha\mu_{eff} N)^2$$

$$= A + BN + CN^2 \tag{2.3.37}$$

and putting the drain current equation and bias dependence of carrier density into equation (2.3.36), the drain current noise spectra can then be written as:

$$S_{I_D}(f) = \frac{kTq^2 I_D \mu_{eff}}{a\gamma f L^2 C_{ox}} \left[A \ln \frac{N_0}{N_L} + B(N_0 - N_L) + \frac{1}{2} C(N_0^2 - N_L^2) \right] \tag{2.3.38}$$

where A, B, and C are fitting parameters related to the interface trap density around the Fermi level, and

$$N_0 = C_{ox}(V_G - V_{T0})/q \quad ,$$

$$N_L = C_{ox}(V_G - V_{T0} - aV_D)/q \quad . \tag{3.3.39}$$

The tunneling trapping constant γ is given by:

$$\gamma = \hbar\sqrt{8m^*\phi} \tag{2.3.40}$$

with m^* being the effective mass of electron in the oxide, ϕ the barrier height for tunneling electrons, and $\hbar$ the Planck's constant.

For devices in saturation mode, V_D in equation (2.3.39) should be replaced by V_{DSAT}.

By chosing proper fitting parameters A, B, and C, equation (2.3.38) was found by Hung et al [Hung90] to be in good agreement with their experimental results.

In the linear region, the gate referred noise spectra can be derived from equation (2.3.36) as:

$$S_{V_G} = \frac{kTq^2}{\gamma f WLC_{ox}^2}(1 + \alpha\mu N)^2 N_{it}(E_f) \quad . \tag{2.3.41}$$

This expression is similar to the unified empirical noise formula in linear region found by Mikoshiba [Miko82]. From his experimental results, Mikoshiba found the following bias dependence of gate referred noise spectra in linear region:

$$S_{V_G}(f) = \frac{1}{fLW}\left[K_1\left(\frac{q}{C_{ox}}\right)^m (V_G - V_T) + K_2\left(\frac{q}{C_{ox}}\right)^2\right] \tag{2.3.42}$$

where $m = 0.7 \sim 1.2$, and K_1, K_2 are empirical constants.

Equation (2.3.41) can be compared to (2.3.42) by ignoring the highest order term of N, setting $m = 1$, and

$$K_1 = \frac{kT}{\gamma} 2\alpha\mu N_{it}(E_f) \quad ,$$

$$K_2 = \frac{kT}{\gamma} N_{it}(E_f) \quad . \tag{2.3.43}$$

The equivalence between equations (2.3.41) and (2.3.42) provided more experimental support, in the linear region, to the unified theory derived from first principles by Hung et al.

Hung's unified theory was also found to be successful in the saturation region in comparison with Hung's experimental results. In Chapter 4, we will show that our model is also in good agreement with the unified noise theory in the saturation region for describing noise bias dependence.

Chapter 3 New Spatial Profiling Technique

In this chapter, we will introduce a new charge pumping method for determining the spatial distribution of interface states. The new method utilizes the charge pumping technique with separated source and drain biases. The advantage of this method is that it allows us to measure N_{it} distributions near the source and drain independently, and we call the new method the spatial profiling charge pumping (SPCP) technique. SPCP requires no assumption on the N_{it} distribution, and if it is combined with the stair-case charge pumping method, then we can determine the overall spatial and energy distributions of the interface state density along the channel. A formula for determining the spatial and energy distribution of N_{it} using the combined charge pumping technique will also be presented in this chapter.

§3.1 Configuration and Formula

The new charge pumping technique is proposed for measuring the spatial distribution of interface state density N_{it} in MOSFETs. Instead of connecting the source and drain together as is usually done, we apply different reverse bias voltages to the source and drain separately. The new method allows us to measure the distribution of N_{it} without making any assumption on it. With the new method, we can determine N_{it} distribution near the source and the drain independently. Our results show that the interface state distribution of a virgin MOSFET is not constant along the channel.

In general, the charge pumping current is given by equation (3.1) below if only the spatial distribution is considered.

$$I_{cp} = f \cdot q \cdot W \int_{X_S}^{X_D} N_{it}(x)dx \, q\Delta\psi_{so} \tag{3.1}$$

where

$$X_S = \sqrt{\frac{2\varepsilon_{si}}{qN_B}} \cdot [(V_S + 2\phi_F)^{1/2} - (2\phi_F)^{1/2}] \quad , \quad and$$

$$X_D = L_{eff} - \sqrt{\frac{2\varepsilon_{si}}{qN_B}} \cdot [(V_D + 2\phi_F)^{1/2} - (2\phi_F)^{1/2}] \tag{3.2}$$

are the well known pn-junction depth near the source and drain respectively. $\Delta\psi_{so}$ is the change of surface potential, f is the frequency of the gate pulses and W is the width of the device.

As pointed out in section §2.1.3, the assumptions in the conventional method limited its validity for measuring arbitrary N_{it} distributions. In order to obtain the actual spatial distribution along the channel, we proposed a new scheme to perform the charge pumping measurement, shown schematically in Figure 2.1. This new method does not require assumptions on N_{it} either for the virgin device, or for the source end of the device, and it is suitable for any N_{it} distribution along the channel.

Instead of connecting the source and the drain together, we apply different reverse bias voltages to the source and the drain independently. In figure 3.1, we show the coordinate system for the new CP scheme. The distribution of interface states in the drain region can be found by varying the drain bias voltage with fixed source bias. Since the source bias is fixed, the source end of the depletion region X_S in the channel is fixed. After measuring the charge pumping current in equation (3.1),

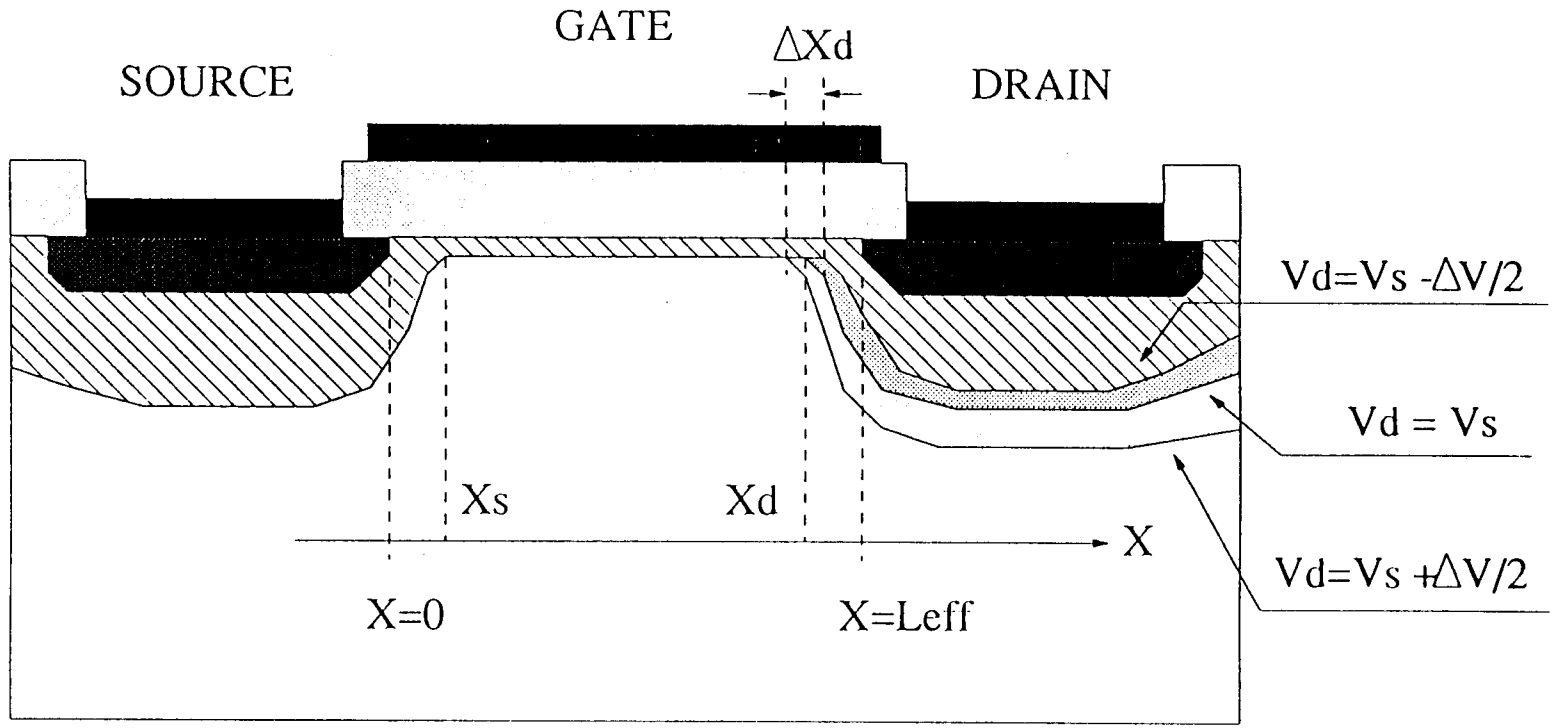

Figure 3.1 Coordinate System in Charge Pumping Measurement.

we can find the spatial distribution $N_{it}(x)$ near the drain end by a straightforward calculation, that is, taking derivative of equation (3.1) to get:

$$N_{it}(X_D)=\frac{1}{f\cdot q\cdot W\cdot q\Delta\psi_{so}}\cdot\left(\frac{dX_D}{dV_D}\right)^{-1}\cdot\left(\frac{dI_{cp}}{dV_D}\right)_{V_S=const.} \quad . \tag{3.3}$$

The distribution near the source region can similarly be measured by varying the source bias voltages with fixed drain reverse bias voltage to give:

$$N_{it}(X_S)=\frac{-1}{f\cdot q\cdot W\cdot q\Delta\psi_{so}}\cdot\left(\frac{dX_S}{dV_S}\right)^{-1}\cdot\left(\frac{dI_{cp}}{dV_S}\right)_{V_D=const.} \tag{3.4}$$

With equations (3.3) and (3.4), we can determine N_{it} around the drain and the source end of the channel independently without making any assumption on N_{it}.

In order to reduce the interference to I_{cp} from hot-carrier-injection induced substrate current, the drain and source bias voltages were chosen to be very close to each other, i.e. V_{DS} was small during the charge pumping measurement.

§3.2 Combination of SPCP and SCCP

The spatial distribution of N_{it} given in last section is an average of its energy distribution. In this section, a more general formula will be given to find spatial and energy distributions of N_{it}. It is a combination of the spatial profiling and stair-case charge pumping techniques.

Considering both the energy and spatial distribution of N_{it}, we can find the charge pumping current from:

$$I_{cp}=f\cdot q\cdot W\int_{E_d}^{q\Psi_{sp}}\int_{X_S}^{X_D}N_{it}(E,X)dE\cdot dX \tag{3.5}$$

The energy and spatial distribution near the drain can be measured by taking derivatives of I_{cp} respecting both drain bias and the surface potential to the step of the stair-case gate pulses. The calculations are straightforward.

$N_{it}(E,X_D)|_{E=q\Psi_{step}}$ distribution near the drain can be given by:

$$N_{it}(E,X_D)|_{E=q\Psi_{step}} = \frac{1}{f \cdot q \cdot W} \cdot \left(\frac{dX_D}{dV_D}\right)^{-1} \cdot \left(\frac{d^2 I_{cp}}{dV_D \quad d(q\Psi_{step})}\right)_{V_S = const.} \tag{3.6}$$

and the distributions near the source:

$$N_{it}(E,X_S)|_{E=q\Psi_{step}} = \frac{-1}{f \cdot q \cdot W} \cdot \left(\frac{dX_S}{dV_S}\right)^{-1} \cdot \left(\frac{d^2 I_{cp}}{dV_S \quad d(q\Psi_{step})}\right)_{V_D = const.} \tag{3.7}$$

The spatial and energy distribution of interface states can be used to evaluate the low frequency noise due to the number fluctuations and the correlation between the number fluctuation and mobility fluctuation. The spatial distribution can also be used in modelling the aging of interface states.

Chapter 4 1/f Noise Model of MOSFETs in Saturation

The mobility fluctuation theory of 1/f noise in MOSFET has previously been investigated by many researchers. To date, there exists both theoretical and experimental results on low frequency noise for the linear mode of operation in MOSFETs, and the agreement between the theory and experiment is good. However, improvements are needed for the existing low frequency noise models of MOSFETs in saturation. The intention of this chapter is to present a new low frequency noise model for saturated MOSFETs. A comparison of our theoretically predicted noise with our experimental results can be found in section §6.3.

The 1/f noise models for MOSFETs in ohmic region based on the mobility fluctuation have shown success by many authors [Hoog81, Hend88, Park81, Park82a, Vand80a, Ziel88b]. However, the evaluation of equation (2.3.4) in saturation mode is not as easy as that in the linear region.

In this chapter, we will present the gate-referred noise spectra based on the general form of equation (2.3.4) for MOSFETs in the saturation mode and will also consider the field dependence of mobility.

The channel lengths of most of our test devices were less than 4μm, and we are more interested in hot carrier effects in short channel devices, therefore we chose the short channel model in the following discussions.

The derivation starts with equation (2.3.4), Hooge's empirical relation as the Langevin source term of noise. Using this relation, the drain current noise spectra can be written in the usual way:

$$S_{I_D} = \frac{\alpha I_D^2}{fL^2} \int_0^L \frac{dx}{n(x)} \tag{4.1}$$

and for the linear region of MOSFET operation, equation (4.1) can be easily evaluated as:

$$S_{I_D} = \frac{\alpha q \mu I_D V_D}{fL^2} \quad . \tag{4.2}$$

However, in the saturation mode, the integration in equation (4.1) is not simple, and it has to be properly evaluated before a comparison with experimental results can be made. Here, we propose a physical model to evaluate equation (4.1) for the saturation mode of operation of NMOS devices. Similar results can also be obtained for PMOS devices.

The proposed model, called the two-region model, divides the channel into two parts as shown in figure 4.1. Note that the distance between L′ and L″ has been exaggerated to show their difference. Region I, the *linear region*, is the conductive channel from the source junction edge (X=0) to the pinch off edge (X=L′). Region II, the *velocity saturation region*, is the depleted part from the pinch off edge (X=L′) to the drain junction edge (X=L).

In region I, the carrier density is related to the gate capacitance charge which is a linear function of the position along the channel and is given as:

$$n(x) = WC_{ox}(V_G - V_T)(1 - x/L')/q \tag{4.3}$$

and

$$L' = L - \Delta L$$

$$= L - \left[\frac{2\varepsilon_{si}}{qN_a}(V_D - V_{Dsat})\right]^{1/2} \tag{4.4}$$

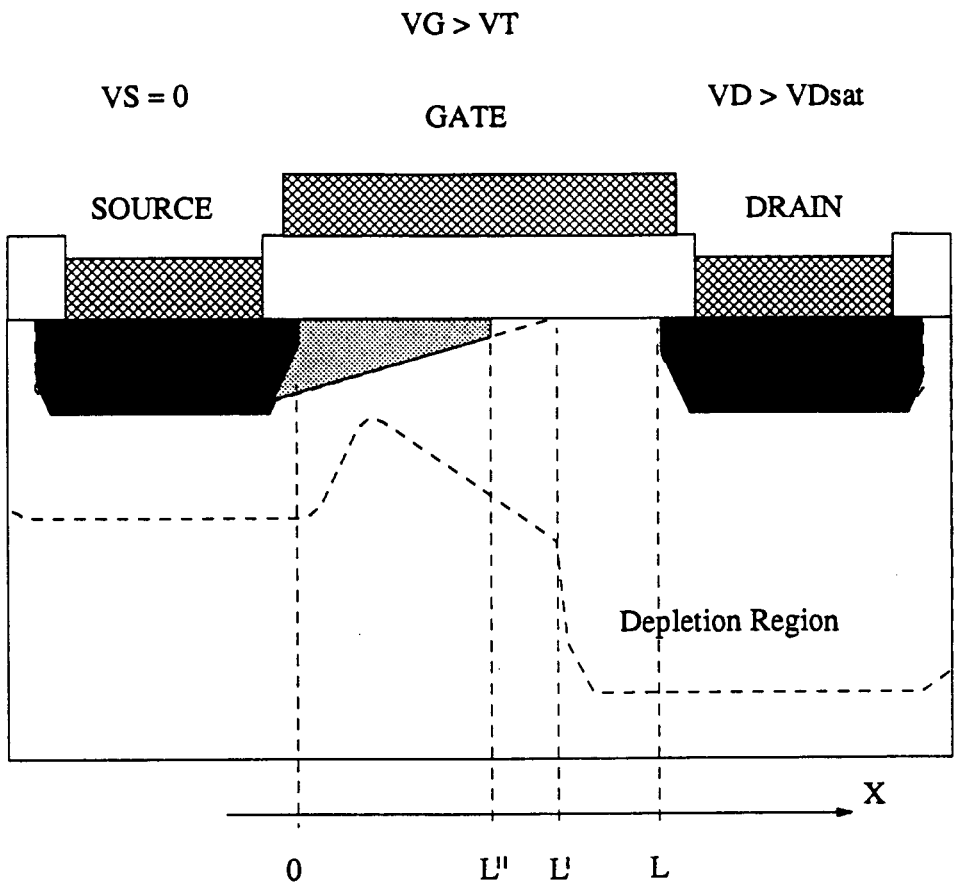

Figure 4.1 Coordinates in the Saturation MOSFET Noise Model

In region II, the carriers are considered to travel at the saturation velocity v_x. The carrier density, although very small $n(x \mid L \geq x \geq L'') = n_0$, is a constant and can be determined from:

$$I_D = q v_x n_o \quad . \tag{4.5}$$

The integration of equation (4.1) is carried out in two intervals: [0, L'] and [L'', L], and carrier continuity is maintained at L '' by the relation:

$$\begin{aligned} n(L'') &= WC_{ox}(V_G - V_T)(1 - L''/L')/q \\ &= n_o \end{aligned} \tag{4.6}$$

From the above model for the saturated MOSFET, we can write the carrier density distribution as:

$$n(x) = \begin{cases} WC_{ox}(V_G - V_T)(1 - x/L')/q & 0 \leq x \leq L'' \\ n_o = WC_{ox}(V_G - V_T)(1 - L''/L')/q & x = L'' \\ n_o = I_D/q v_x & L'' \leq x \leq L \end{cases} \tag{4.7}$$

Substituting this distribution into equation (4.1), the drain current noise spectra can be found by a straightforward calculation and is:

$$\begin{aligned} S_{I_D} &= \frac{\alpha I_D^2}{fL^2} \int_0^L \frac{dx}{n(x)} \\ &= \frac{\alpha q I_D^2}{fLWC_{ox}(V_G - V_T)} \left[\frac{L - \Delta L}{L} \ln\left(\frac{I_{max}}{I_D}\right) + \frac{\Delta L}{L}\left(\frac{I_{max}}{I_D}\right) \right] \end{aligned} \tag{4.8}$$

where ΔL was defined in equation (4.4), and I_{max} was defined as:

$$I_{max} = v_x WC_{ox}(V_G - V_T) \tag{4.9}$$

and the relationship between the drain current noise spectra and the input referred voltage noise spectra is known to be [Gent81]:

$$S_{VG}(f)=\frac{S_{I_D}(f)}{g_m^2} \tag{4.10}$$

In the following sections, we are going to consider two typical cases in the saturation mode of MOS device operation. And the gate referred noise spectra will be presented for both cases. The two cases are:

Case I (*slightly saturated short channel devices*): $V_D \sim V_{Dsat}=(V_G-V_T)$ for short channel devices with small V_G-V_T, we have $I_D \propto (V_G-V_T)^2$;

Case II (*deeply saturated short channel devices*): $V_D \geq (V_G-V_T) > V_{Dsat}$ for short channel devices with velocity saturation, we have $I_D \propto (V_G-V_T)$;

§4.1 Onset Saturation Model

In this section, we will deal with the onset of saturation case. The condition for onset saturation is:

$$V_D=V_G-V_T=V_{DSAT} \quad \textit{for small } V_G-V_T \textit{ in short channel devices.} \tag{4.11}$$

In order to determine the bias dependence of gate-referred noise spectra, we need to know the saturation current model.

Using the well-known expression of the drain current for the onset of saturation in short channel MOSFETs:

$$I_D=\frac{WC_{ox}}{2L'}\frac{\mu_0}{1+\theta(V_G-V_T)}(V_G-V_T)^2(1+\lambda V_D) \tag{4.12}$$

we can evaluate the trans-conductance g_m as:

$$g_m=\frac{2+\theta(V_G-V_T)}{1+\theta(V_G-V_T)}I_D(V_G-V_T)^{-1} \quad . \tag{4.13}$$

The gate-referred noise spectra for MOSFET at the onset of the

saturation mode is determined as:

$$S_{VG}(f) = \frac{\alpha q}{fLWC_{ox}}\left(\frac{1+\theta(V_G-V_T)}{2+\theta(V_G-V_T)}\right)\left[\frac{L-\Delta L}{L}\ln\left(\frac{I_{max}}{I_D}\right)+\frac{\Delta L}{L}\left(\frac{I_{max}}{I_D}\right)\right](V_G-V_T)$$

$$\approx \frac{\alpha q}{2fLWC_{ox}}\left[\frac{L-\Delta L}{L}\ln\left(\frac{I_{max}}{I_D}\right)+\frac{\Delta L}{L}\left(\frac{I_{max}}{I_D}\right)\right](V_G-V_T) \qquad (4.14)$$

where I_{max} was defined in equation (4.9).

Since $I_{max} \propto (V_G-V_T)$ and the drain current $I_D \propto (V_G-V_T)^2$, the second term in the right-hand-side of equation (4.14) will be approximately constant as V_G-V_T increases, while the first term will increase slightly. Therefore, we expect that the gate referred noise level will increase slightly as V_G-V_T increases at the onset of saturation region.

§4.2 Velocity Saturated Model

In this section, we will discuss an extreme situation in the saturation mode of MOSFET operation. In this case, the velocity of carriers in most of the channel is saturated to the maximum velocity v_x. This can be achieved by biasing the short channel device under the following condition: $V_D \geq (V_G-V_T) > V_{Dsat}$.

In case of the deep saturation, the drain current is the maximum possible drain current which can be written as:

$$I_D = v_x WC_{ox}(V_G-V_T) \qquad (4.15)$$

and therefore the trans-conductance is a constant as follows:

$$g_m = v_x WC_{ox} \qquad (4.16)$$

Substituting equations (4.8), (4.15), and (4.16) into equation (4.10), the input referred noise spectra in deep saturation can then be found as:

$$S_{VG}(f)=\frac{\alpha q}{fLWC_{ox}}\cdot\frac{\Delta L}{L}(V_G-V_T) \tag{4.17}$$

It will increase linearly as V_G-V_T increases.

Chapter 5 Experimental Systems

An automated microelectronics measurement system has been implemented for the microelectronics research group at school of engineering science, Simon Fraser university. This hardware and software integrated measurement system is capable of taking measurements on DC characterization, low frequency noise spectra and charge pumping of MOSFETs. It is very useful in studying the hot-carrier-induced effects and other short channel effects in short channel MOSFETs.

§5.1 Devices Studied

The devices used in our experiments were supplied by Northern Telecom Electronics, Ottawa. The effective channel length of those devices varies from 0.6μm to 3.0μm. All the devices have the same draw width of 10μm and the terminals of each device are separated. The effective channel doping is about $2x10^{16}cm^{-3}$, and the gate oxide thickness is 250 Å for all devices used.

§5.2 Charge Pumping Measurements

Our experimental setup is shown in figure 5.1. A HP4145B Semiconductor Parameter Analyzer (SPA) was programmed to provide both the source and the drain bias voltages, and to measure the substrate current in the charge pumping measurements. A Wavetek 178 wave function generator was programmed to supply the square pulses to the gate with a variable base level. All the equipment are automated by an IBM compatible personal computer.

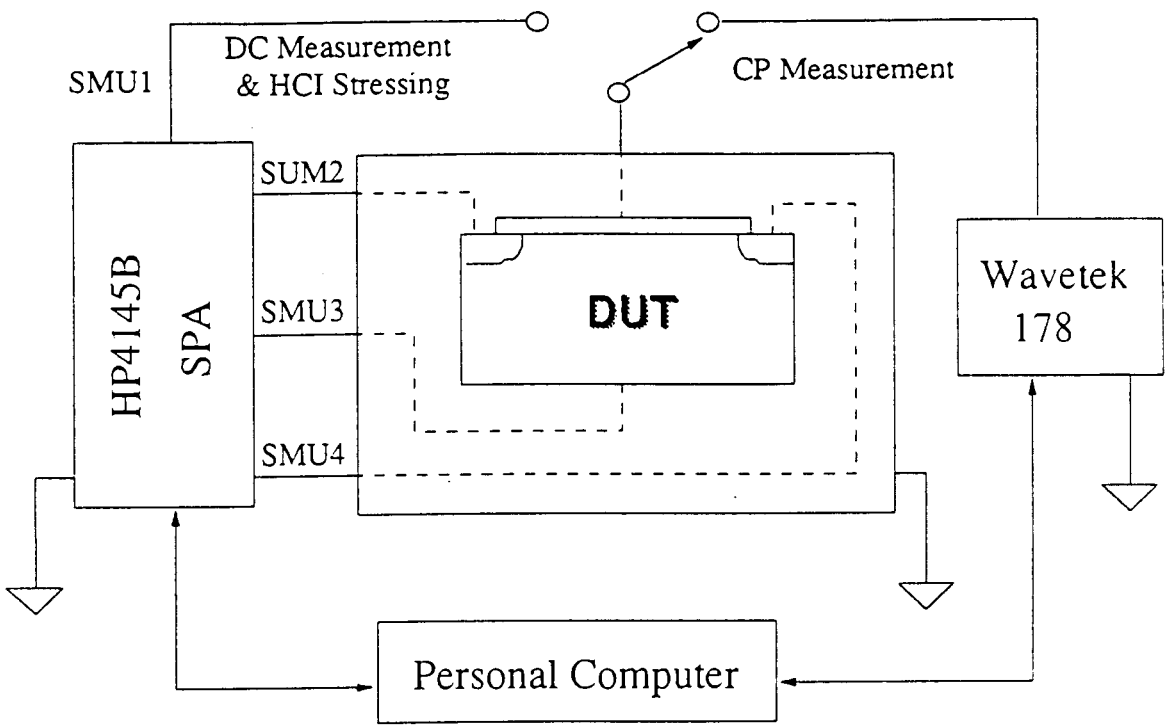

Figure 5.1 Charge Pumping Experimental Setup

The HP4145B Semiconductor Parameter Analyzer was also used to stress the MOSFET for hot-carrier-injection and monitoring the DC parameter degradations.

To measure the interface states distribution near the drain end, for each fixed source voltage V_s, two measurements were taken at drain bias voltages of $V_D = V_s \pm \frac{1}{2}\Delta V$. The difference of the drain bias $\Delta V_D = \Delta V$ and the change of charge pumping current ΔI_{cp} were used in equation (3.3) to calculate $(dI_{cp}/dV_D)_{V_s=const.}$ for $N_{it}(x)$ near the drain end. If we adjust the step of the source bias voltage to $\frac{1}{2}\Delta V$, then we can have the change of I_{cp} with fixed drain bias for different source bias at the same time. This changes can be used in equation (3.4) to determine the distribution near the source region.

In most of our measurements the gate pulse frequency is f=100KHz. The frequency is chosen to be high enough so that the bulk recombination in substrate cannot respond to it to reduce the geometric substrate current. The frequency dependence of charge pumping current has been investigated to find a proper gate pulse frequency. The amplitude of gate pulses is chosen to be 7.5V or 5.0V. Accordingly, the change of surface potential was established to be about $0.6V(\approx 2\phi_F)$.

Since the new charge pumping method modified the conventional charge pumping technique with different voltages applied to the source and drain, a question about effects on the charge pumping results caused by the voltage difference may be asked. Our experimental results showed that the effect can be eliminated by carefully selecting of the source and drain bias voltage difference. It was found that the bias voltage difference of $\Delta V = 100mV$ was most suitable for our test devices. There are two major factors involved in determining this bias

difference. Too large or too small ΔV will cause problems, and more details on this issue can be found in chapter 6.

A computer control program called ***CPSPA***, was developed to conduct the automated charge pumping measurements. The syntax of using ***CPSPA*** is:

CPSPA configuration_filename

Inside the file: *configuration_filename*, 8 parameters are specified. They are:

start, stop, and step values of gate pulse offset voltage V_{GL}, and drain bias voltage V_D; gate pulse frequency f and amplitude of gate pulse ΔV_G;

Table 5.1 shows a typical file of *configuration_filename* for a NMOS device.

Table 5.1 Configuration file of Program CPSPA

V_{GL}			V_D			f	ΔV_G
start	stop	step	start	stop	step	Hz	(V)
-8.0	2.0	0.1	0.05	5.0	0.05	1.0E5	7.5

The voltage difference between the drain bias and source bias is set to be the same of drain bias step value supplied by the configuration file, and ΔV of the derivative measurement in equation (3.3) or (3.4) is double of the drain bias step value supplied by the configuration file.

To run this program, one needs the following instrument:
A HP4145B Semiconductor Parameter Analyzer (SPA) and A Wavetek 178 wave function generator.

§5.3 DC Measurements and Stress Scheme

The DC parameter degradation measurements are performed by an automated HP4145B Semiconductor Parameter Analyzer. Computer control programs developed for the DC measurements and hot-carrier-injection stressing are ***SPA*** and ***STRESS***.

Program ***SPA*** is for taking DC characteristic measurements. The syntax of using this program is:

SPA configuration_filename <output_filename>

If *output_filename* was not provided, the default output file name *datafrom.spa* will be used.

Program ***STRESS*** is developed to stress the DUT for any given time interval under specified drain bias voltage. The program can automatically determine the gate bias voltage to achieve the maximum substrate current. To use program ***STRESS***, the syntax is:

STRESS P(N) (PMOS/NMOS) stress_time(Sec) <drain_bias_voltage>

If *drain_bias_voltage* was not supplied, the default *drain_bias_voltage* is 5V for NMOS with option ***N***, and -5V for PMOS with option ***P***.

As discussed in section §2.2, the trans-conductance g_m is a direct probe the hot carrier injection degradation in MOSFETs. The g_m was determined from derivative the DC I_D - V_G curve at $V_D = 50,\ 75,\ \text{and}\ 100mV$, with both the source and the substrate connected to ground. The g_m degradation as a function of the stressing time was monitored for NMOS devices with the effective channel length varying from 0.6μm to 3.0μm.

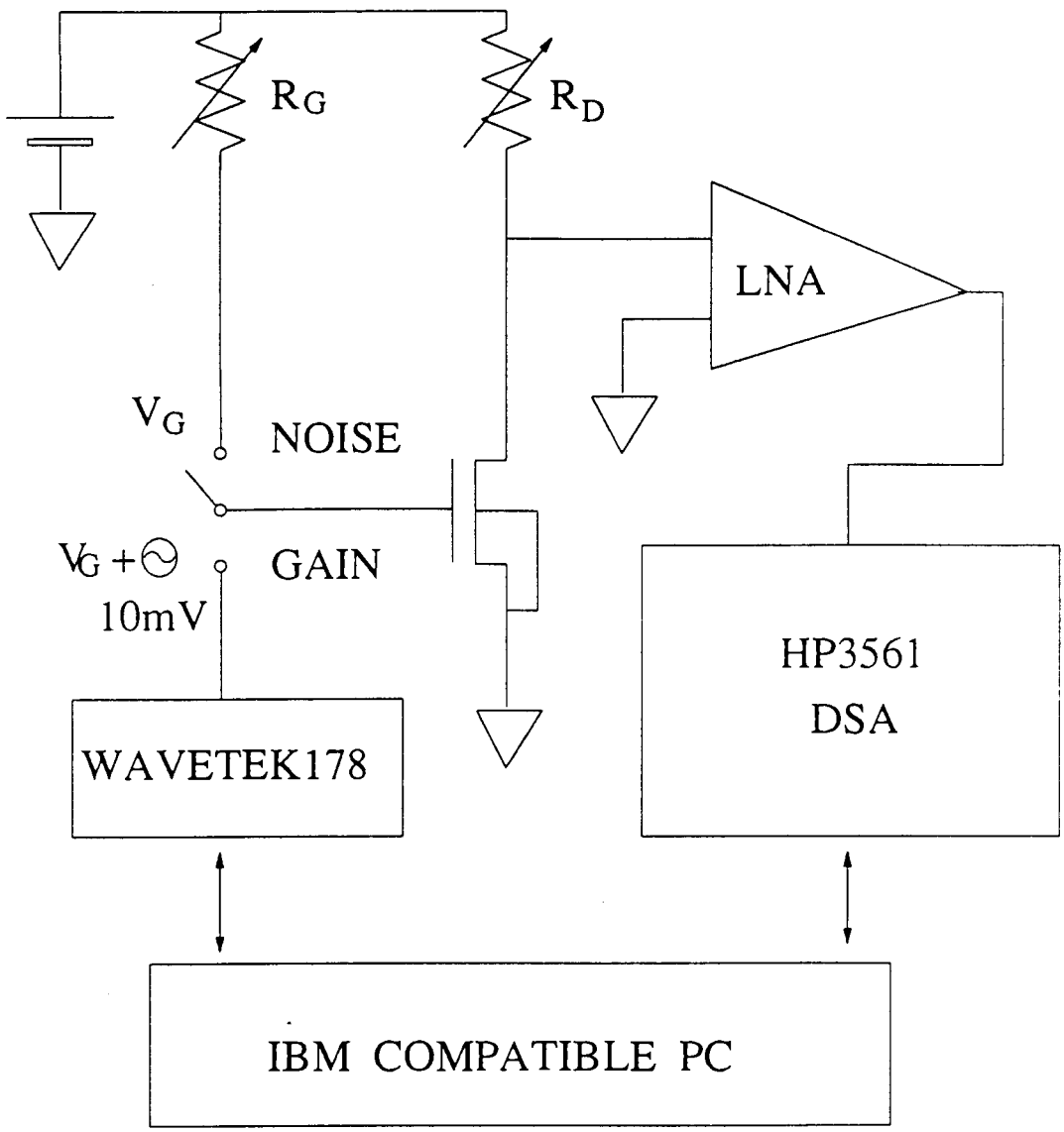

Figure 5.2 Schematic Diagram of Noise Test System

§5.4 1/f Noise Measurements

The low frequency noise spectra were measured for our test devices at saturation mode to verify the theoretically predicted bias dependence of 1/f noise introduced in Chapter §4.

A computer program for taking the noise measurement was developed. The program is called ***MOSNOISE***. This program is capable of controlling the automated measurement system to take the noise data as well as measure the gain data of device under test. The noise data will be stored in a file called ***n****xxxxxxxx.xxx*, and the gain data in ***g****xxxxxxxx.xxx*. In the output file names, *xxxxxxx.xxx* is a user supplied string (maximum 7 characters before the dot ".", and maximum 3 characters after it). To use this program, type:

MOSNOISE *xxxxxxx.xxx*

A HP3561 Dynamic Signal Analyzer, a Wavetek 178 wave function generator, and a low noise per-amplifier are needed to run this measurement. In order to reduce unnecessary system noise, we use a battery as our bias voltage supply. The program ***MOSNOISE*** was designed to be interactive for necessary inputs and bias adjustments. Figure 5.2 is a schematic diagram of our noise test system.

Chapter 6 Results and Discussions

Our experimental results showed that the proposed new spatial profiling technique is capable of determining the interface state density distribution in MOSFETs, and N_{it} is not uniformly distributed along the channel even for the virgin devices. Peaks of N_{it} can be found at both the source and the drain side of the channel. It was also found that the change of interface state is correlated to the original value, and the higher the original value, the larger the increase after hot carrier injection stress.

The experimental results of 1/f noise in saturation showed very good agreement with the two region model's predictions. Also, our DC measurement results confirmed that the maximum trans-conductance g_m is a consistent function of the hot-carrier injection stress (HCI) time for NMOS devices.

§6.1 Spatial Distribution of N_{it} in MOSFETs

As a test of our measurement system, the gate pulse offset dependence of the charge pumping current was measured and the results are shown in figure 6.1 which is same as we previously plotted in figure 2.5. In figure 6.1, we also show the source and drain bias dependence of I_{cp}. It is easy to understand that the charge pumping current is reduced when the source and drain reverse bias voltages increase. This is because the effective channel length for charge pumping is getting shorter and therefore, the amount of interface states involved in I_{cp} is reduced. The source and drain bias dependence of the charge pumping current is the foundation of spatial profiling technique.

The spatial interface state density distributions have been

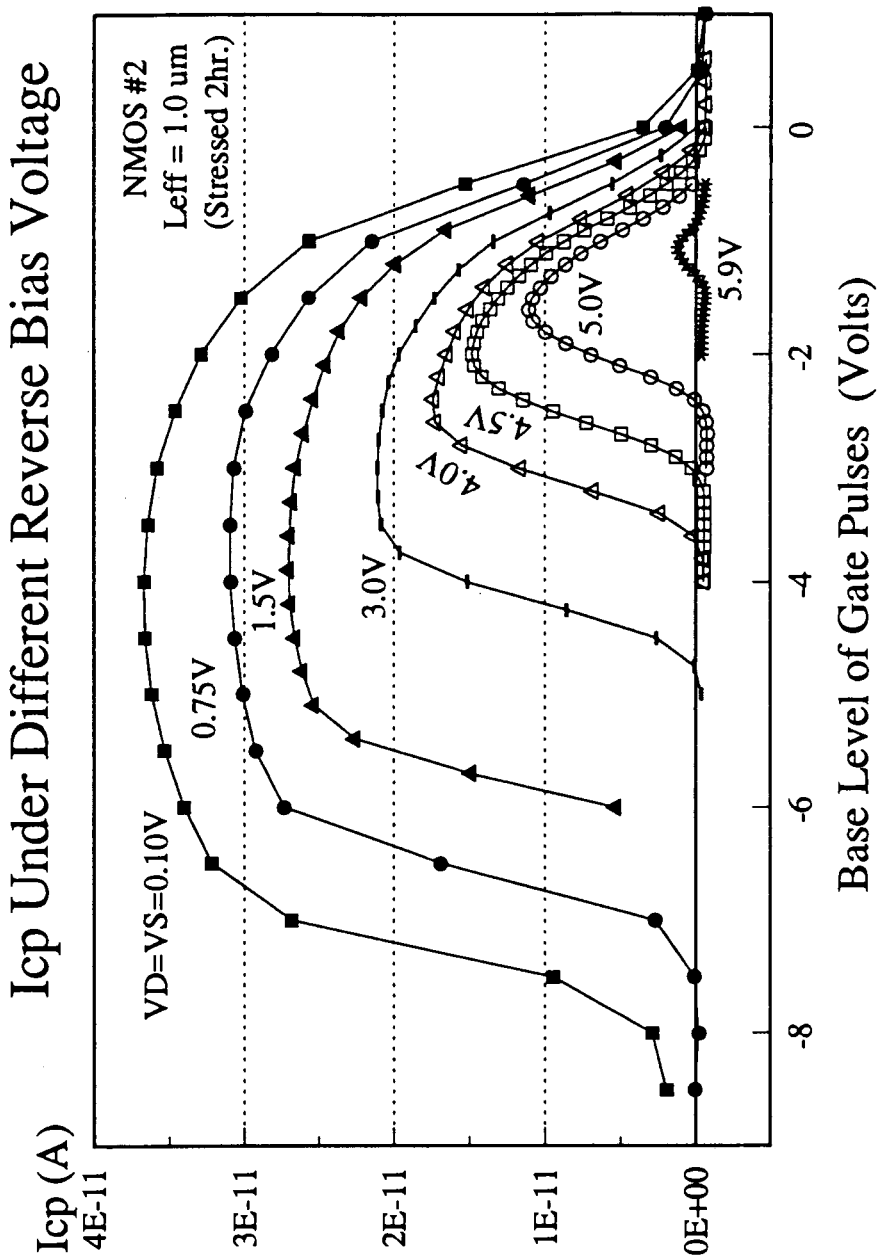

Figure 6.1 Bias Dependent of I_{cp}

measured by the proposed spatial profiling charge pumping method for our NMOS test devices. The effective channel length of the device is L_{eff} = 1.0μm. The variation of N_{it} under the hot-carrier injection stress time was also investigated.

The charge pumping measurements were performed under the following conditions: the gate pulse amplitude was $\Delta V_G = 5.0V$, at a frequency of $f = 100kHz$, the source and drain bias voltage were varied from 0.05V to about 4.0V, which allowed us to investigate the interface states down to the channel central region from both the source and the drain side.

In figure 6.2, we show our results of interface state distribution for a NMOS device with L_{eff}=1.0μm. The N_{it} profiles along the channel are similar for both the virgin (before hot-carrier injection stressing) and stressed device. We can see that the interface state has two peaks at both the source and the drain region. This result is in contrast to either the latest results reported in [Saks90], or the results in [Maes82]. The interface state density is not a constant for the virgin devices as assumed in [Maes82, plos88]. Peaks of N_{it} near the source and drain of a virgin device are found not always of the same height. This difference is believed due to the processing steps that affect the gate oxide near the source and drain, and possibly different overlap length of the gate oxide near the source and drain.

The changes in the interface state density near both the source and drain as a function of HCI stressing time are also shown in figure 6.2. We can see that the interface state density increased as a result of HCI stress. The device was stressed under the condition that the maximum substrate current was achieved at $V_D = 5.0V$ *and* $V_G \approx 1.8V$ for two hours. The interface

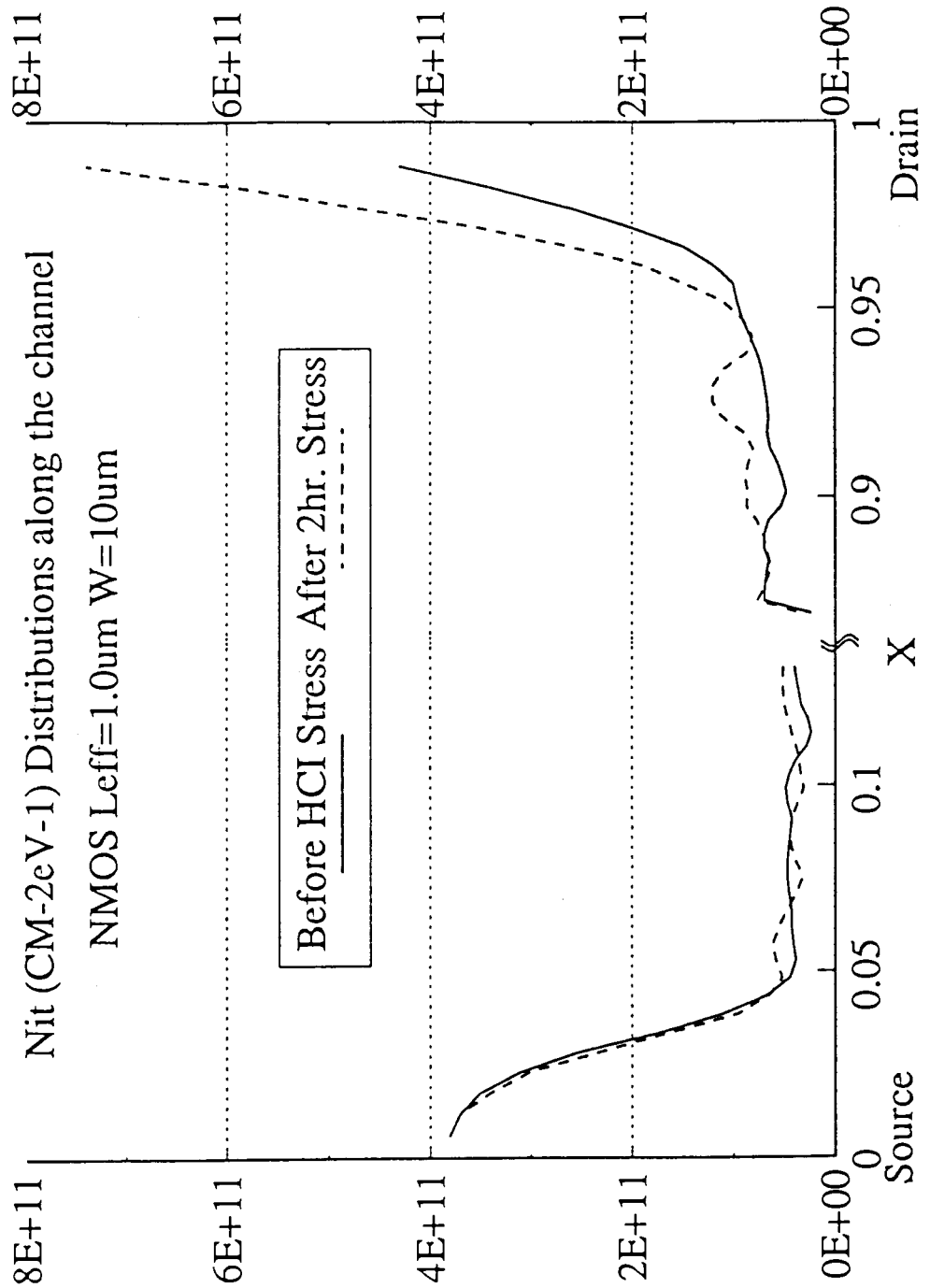

Figure 6.2 N_{it} Distribution Along the Channel

state density almost doubled near the drain while near the source it remained the same as for the virgin device. From figure 6.2, we can also see that the change in N_{it} is proportional to its original value. That is, the larger N_{it} was in the virgin device, the larger is its change after HCI stress. This proportional relationship was also reported by other researchers, such as [Fang86b]. Fang's results from 1/f noise in MOSFETs also showed that new traps were created in proportion to the existing trap densities. This result will be helpful in understanding and modelling the aging of interface states under HCI stress.

There are many factors that may affect the charge pumping results, such as: the gate pulse frequency, waveform, and amplitude dependences. However, all these problems have been extensively investigated both experimentally and numerically by many authors in last few years [Groe84, Here89, Ghib88, Ghib89]. For our system and test devices, the optimized parameters were given in section §5.2. In this section, we will address one particular issue associated with our new spatial profiling technique and another problem on which no paper has been written.

First of all, we want to discuss the substrate current caused by the bias difference between the source and drain. This is new to the charge pumping technique because different source and drain bias voltages are used in our spatial profiling method.

During the charge pumping process, the gate pulses the channel between inversion and accumulation, and there will be a current driven by the source and drain bias difference when the channel is in inversion. The substrate current has been known to be proportional to the drain current. Larger bias differences will result in higher drain currents and therefore larger

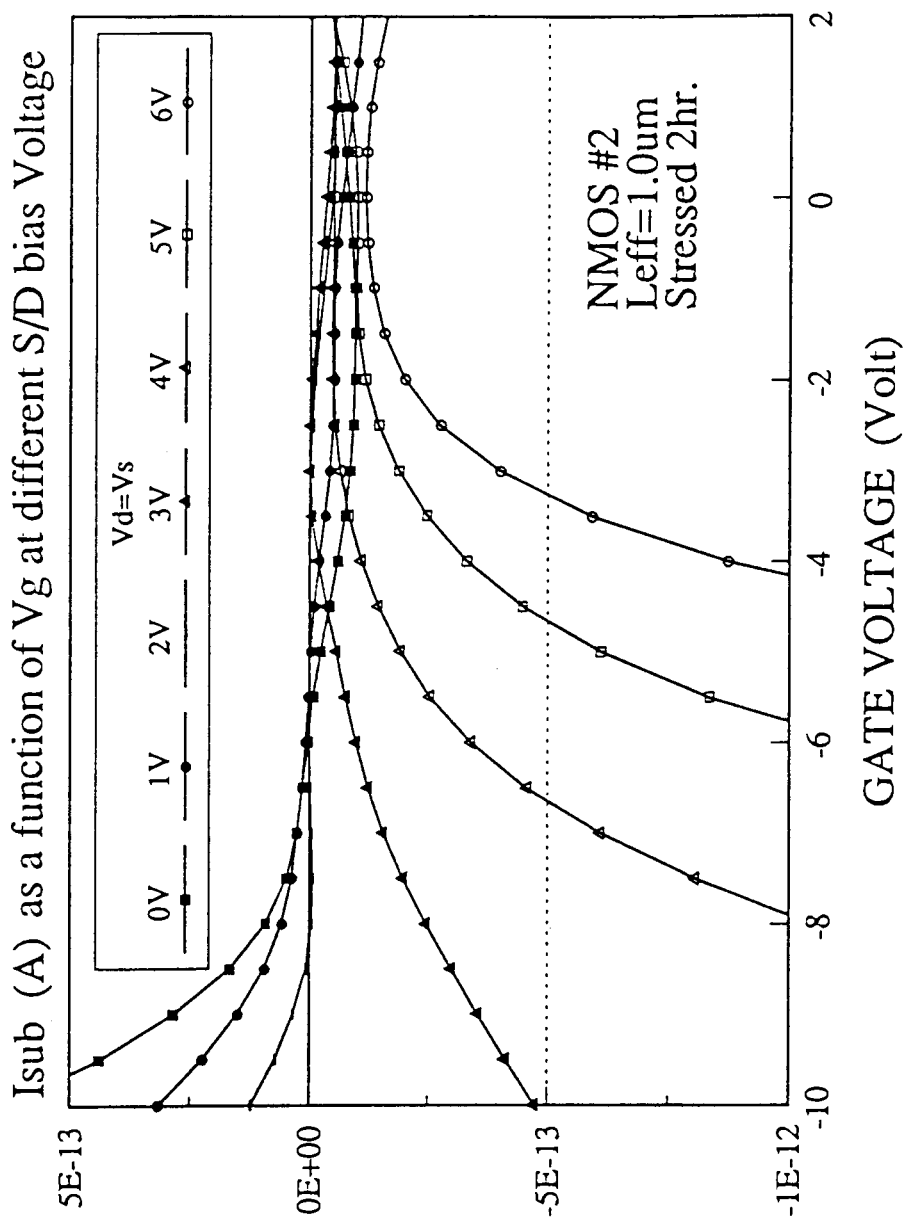

Figure 6.3 Bias Dependent of I_{sub}

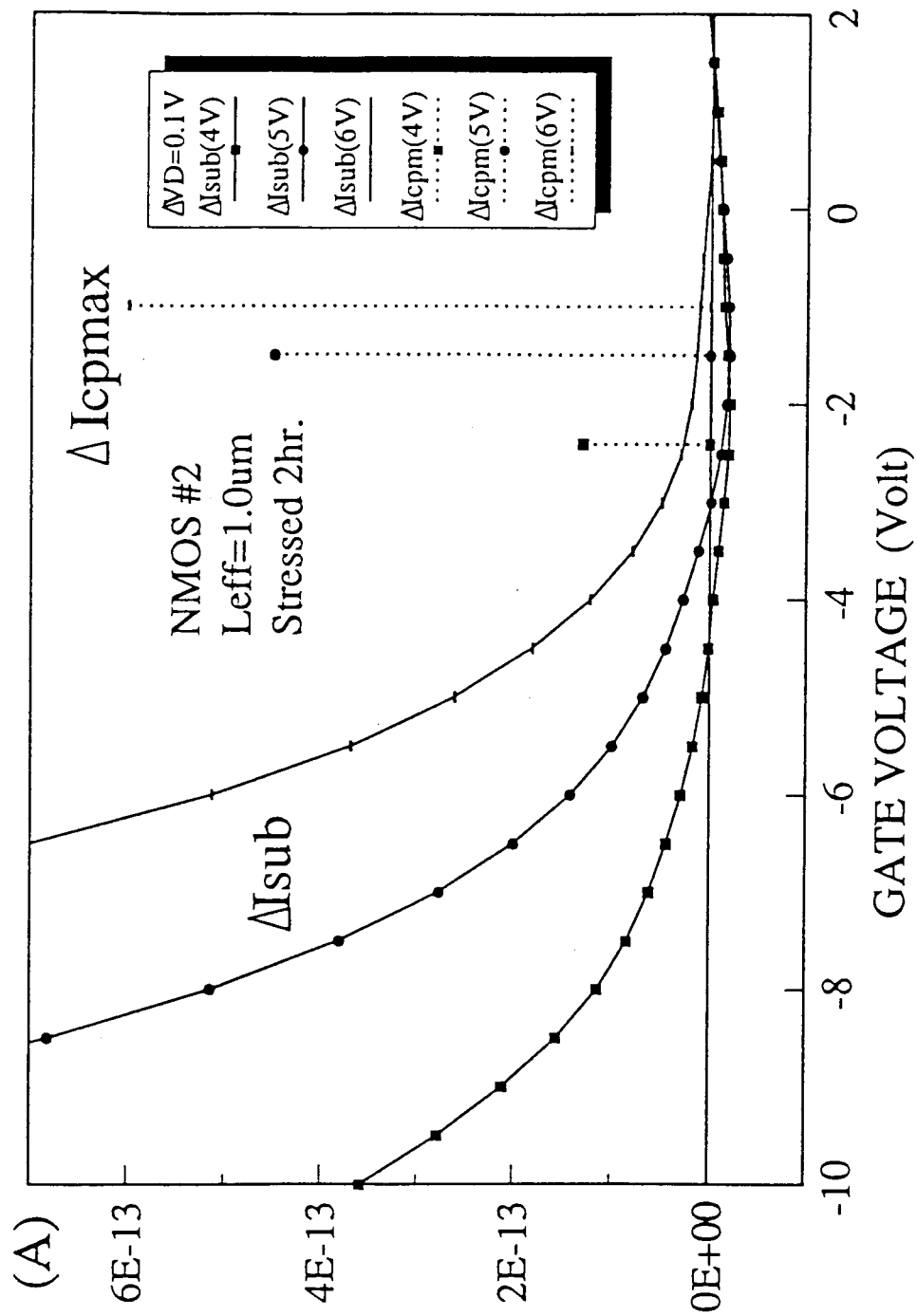

Figure 6.4 Bias Dependent of ΔI_{sub} and ΔI_{cpmax}

substrate currents. This substrate current may be large enough to interfere with the charge pumping current if the bias difference is too large or the effective channel length is too short. This part of the substrate current can be reduced by using smaller bias differences. However, the smallest value of the bias difference is limited by the accuracy of the charge pumping current measurement. The bias difference has to be large enough to make the change of charge pumping current measurable. For our system and test devices, the optimum choice of the bias difference is 50mV.

The second issue we are going to discuss is the source and drain p-n junction reverse leakage current which limits the depth into the channel that the charge pumping technique can probe. The leakage current dominates the substrate current when the source and drain reverse bias voltages are too large. For our device, this occurs at about 4.0V or 6.0V for different devices.

Figure 6.3 showed the source and drain p-n junction leakage current as a function of the reverse bias voltage. The substrate current increases dramatically when the reverse bias voltage exceeds 3 Volts and it is also a function of gate voltage. To see how much the substrate current can affect the N_{it} measurement, we plotted the change of substrate current ΔI_{sub} from DC measurements as well as the change of maximum charge pumping current ΔI_{cpm} in figure 6.4. For both measurements, V_s was set to 4.0V, 5.0V and 6.0V. The drain was biased at two voltages: $V_D = V_s - 0.05V$ and $V_D = V_s + 0.05V$ for each V_s, and the current difference was measured between the two drain biases. For ΔI_{cpm}, the position in the gate voltage axis represents the gate pulse offset value which yields the maximum charge pumping current. ΔI_{sub} showed rapid increase when the gate bias approached larger

negative values. However, at the gate voltages of maximum I_{cp}, ΔI_{sub} was much smaller than ΔI_{cpm}. Therefore for this test device, the substrate current caused by the junction leakages (up to 6.0V reverse S/D bias) and source and drain bias difference (0.05V) would not affect the determination of N_{it} which is proportional to ΔI_{cpm}. But some of our test devices require lower S/D reverse bias voltages in order to keep the change of leakage current much less than ΔI_{cpm}. The substrate current must therefore be monitored after each HCI stress to ensure that it would not affect the N_{it} measurement because it will change as a result of HCI stress.

§6.2 DC Parameter Degradation Under HCI

There are many DC parameters that can be used as probe of the hot-carrier effects. In this section, we will show our experimental results of changes of the maximum trans-conductance g_m, the substrate current I_{sub}, and the charge pumping current I_{cp} as functions of channel hot-carrier injection stress (HCI) time. The total number of interface states N_{it} is proportional to the charge pumping current as shown by equation (2.1.2). Comparison of N_{it} generation and the g_m and I_{sub} degradations will also be reported. All the results presented in this section are for NMOS only.

§6.2.1 Maximum Trans-conductance

The maximum trans-conductance g_m degradation has been demonstrated by many authors [Hu85, Chun90]. Steady decrease of g_m as a function of hot-carrier injection stress time was

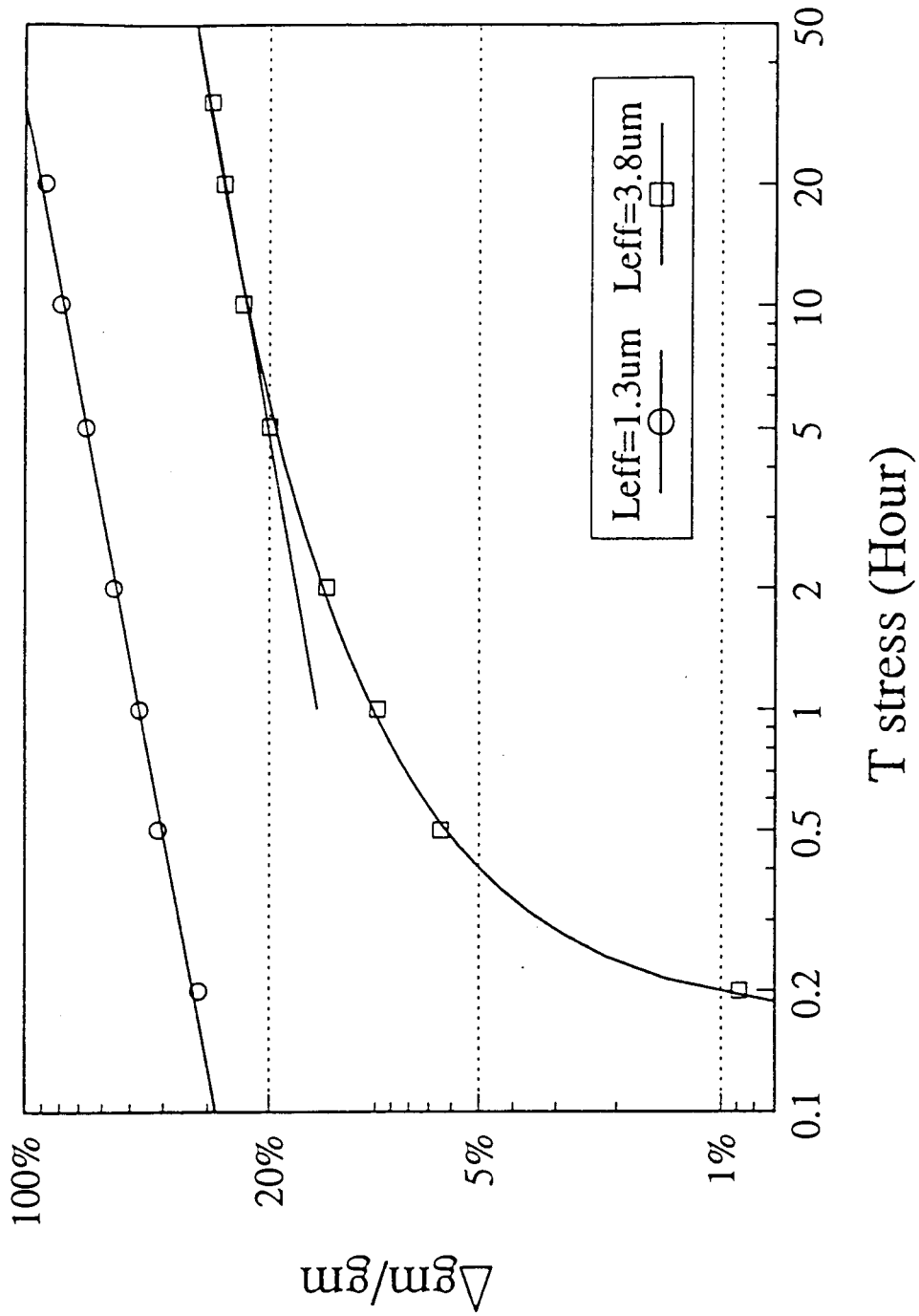

Figure 6.5 g_m Degradation Under HCI Stress

obtained from our NMOS test devices. In figure 6.5, we plotted a typical g_m degradation with $\Delta g_m/g_{mo}$ as a function of HCI stressing time. Note that $\Delta g_m/g_{mo}$ was defined as:

$\Delta g_m/g_m = (g_{m_0} - g_m)/g_{m_0}$,

since g_m declines when the device is stressed. The two test devices have the effective channel length of 1.3μm and 3.8μm respectively. Both of them were stressed under $V_D = 5.0V$, *and* V_G was chosen to be $V_G \approx 3.0V$ to achieve maximum substrate current.

The steady decrease of g_m can be understood as a result of a steady increase in the number of acceptor-type traps which trap the channel electrons, and therefore reduced the drain current [Hu85]. During the whole stress process for the shorter channel device and a few hours later for the longer device, a linear relationship in logarithm scale was obtained between the g_m degradation and HCI stress time. The linear relationship is in good agreement with equation (2.2.1), and the slopes are $\alpha_{g_m} \sim 0.22$, *and* 0.20 for the shorter and longer device respectively. Although they have the similar slope α_{g_m}, $\Delta g_m/g_{mo}$ is much smaller for the longer device than that for the shorter device, which means that the longer device was less susceptible to hot-carrier degradation. In other words, hot-carrier degradation is much severe for the short channel devices, which is in agreement with the result obtained for other test devices in our laboratory [Quon90].

§6.2.2 Substrate Current

Under the same HCI stress conditions described in §6.2.1, linear a relationship in logarithm scale was also observed between the substrate current degradation and the time of HCI

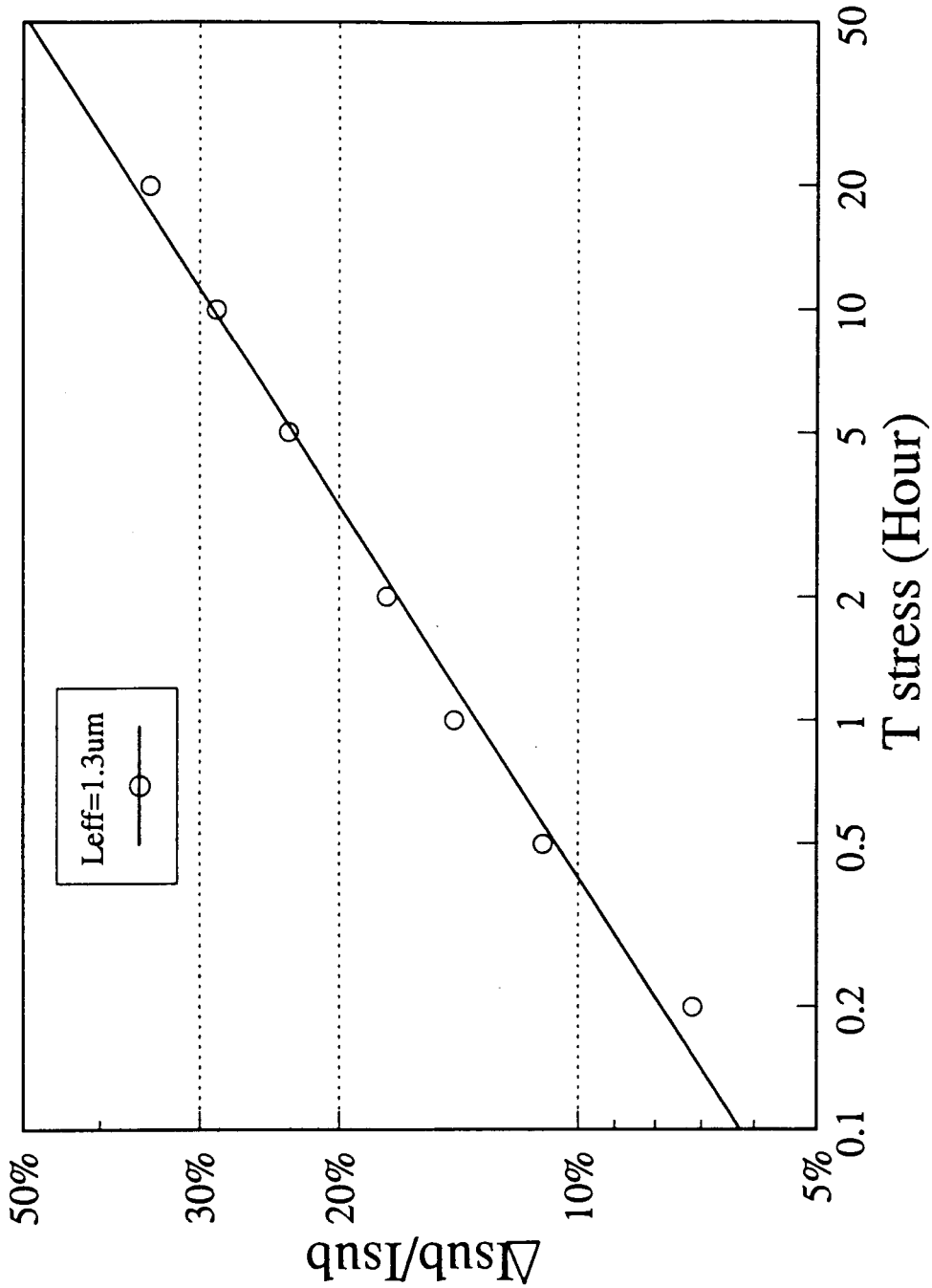

Figure 6.6 I_{sub} Degradation Under HCI Stress

stress. A typical result is shown in figure 6.6 for our test device with $L_{eff} = 1.3\mu m$. The relationship is:

$$\frac{\Delta I_{sub}}{I_{sub}} \sim t^{\alpha_{sub}}, \quad with$$

$$\alpha_{sub} \approx 0.33 \quad . \tag{6.2.1}$$

where the substrate current was measured under conditions of $V_D = 5.0V$, *and* V_G chosen to be $V_G \approx 3.0V$, which yield maximum substrate current. The t^{α} time dependence is a result of a continuous exponential increase of maximum substrate current under HCI stress. Our results are in good agreement with those reported in [Hu85, Chun90]. The substrate current can be expressed by its dependence on the effective electron temperature T_e as [Hu85, Tam83]:

$$I_{sub} \propto I_D e^{-\Phi_i / kT_e}, \tag{6.2.2}$$

where Φ_i is the minimum energy in electron-volts that a hot electron must have in order to create an impact ionization. However, so far there is no physical model available for the stress time dependent of I_{sub}. In next section, we will try to obtain an empirical HCI stress time dependent of effective electron temperature T_e, and therefore the time dependent of I_{sub}.

§6.2.3 Comparison with Interface State Generation

The t^{α} time dependence has been obtained form the degradations of both the maximum trans-conductance and the

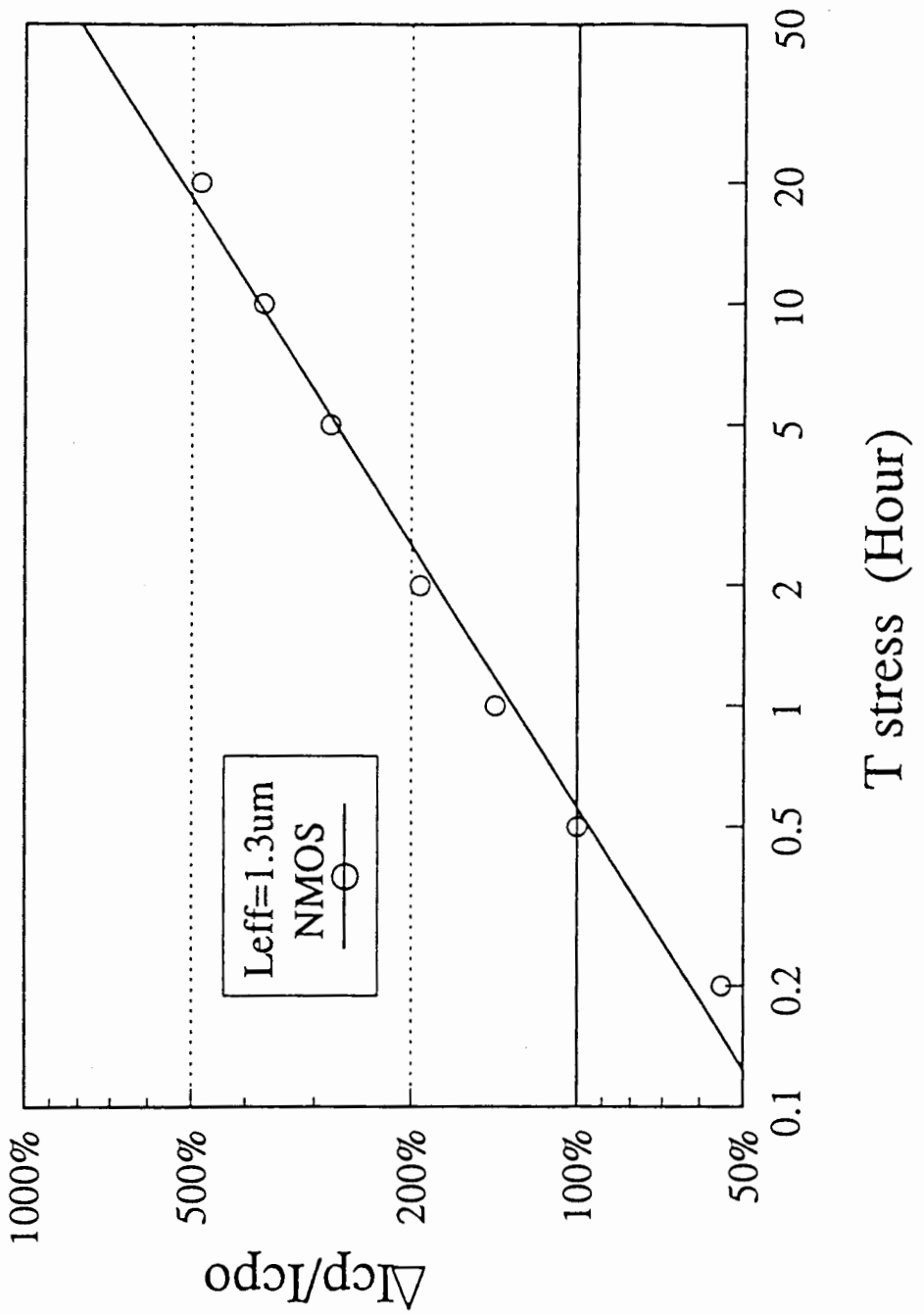

Figure 6.7 I_{cp} Degradation Under HCI Stress

substrate current degradation under HCI stress. Although we do not have a physical model for time dependence of I_{sub}, we have a physical model for the t^{α} time dependent of interface state generation [Hu85]. According to Hu's model, we have:

$$\Delta N_{it} \propto \left(I_D e^{-\Phi_{it}/kT_e}\right)^{\alpha_{it}} \cdot t^{\alpha_{it}} \quad . \tag{6.2.3}$$

where Φ_{it} is the critical energy for generating an interface trap. From the charge pumping theory discussed in section §2.1, we know that the change of interface states ΔN_{it} can be determined by taking the CP measurement. Using equation (2.1.2), we have:

$$\Delta N_{it} \propto \frac{\Delta I_{cp}}{I_{cpo}} \quad . \tag{6.2.4}$$

In figure 6.7, $\frac{\Delta I_{cp}}{I_{cpo}}$ was plotted against the HCI stress time for our test device with $L_{eff} = 1.3\mu m$. The t^{α} time dependent of $\frac{\Delta I_{cp}}{I_{cpo}}$ shown in figure 6.7 is:

$$\frac{\Delta I_{cp}}{I_{cpo}} \sim t^{\alpha_{cp}}, \quad with$$

$$\alpha_{cp} \approx 0.46 \quad . \tag{6.2.5}$$

Comparing equations (6.2.5) and (6.2.4), the time dependent exponent of interface trap generation can be determined as:

$$\alpha'_{it} \approx 0.46 \quad . \tag{6.2.6}$$

This value is very close to 0.5 as reported in [Hu85]. One may notice that α'_{it} was used instead of α_{it} in equation (2.6.3). This is because we expect t^{α} time dependence of ΔN_{it} to be:

$$\Delta N_{it} \propto \left(I_D e^{-\Phi_{it}/kT_e}\right)^{\alpha_{it}} \cdot t^{\alpha_{it}} \sim t^{\alpha'_{it}} \quad . \tag{6.2.7}$$

We now want to determine the HCI stress time dependence of the effective electron temperature T_e and/or that of Φ_{it} to evaluate the time dependent index α_{it} in equation (6.2.3). In order to

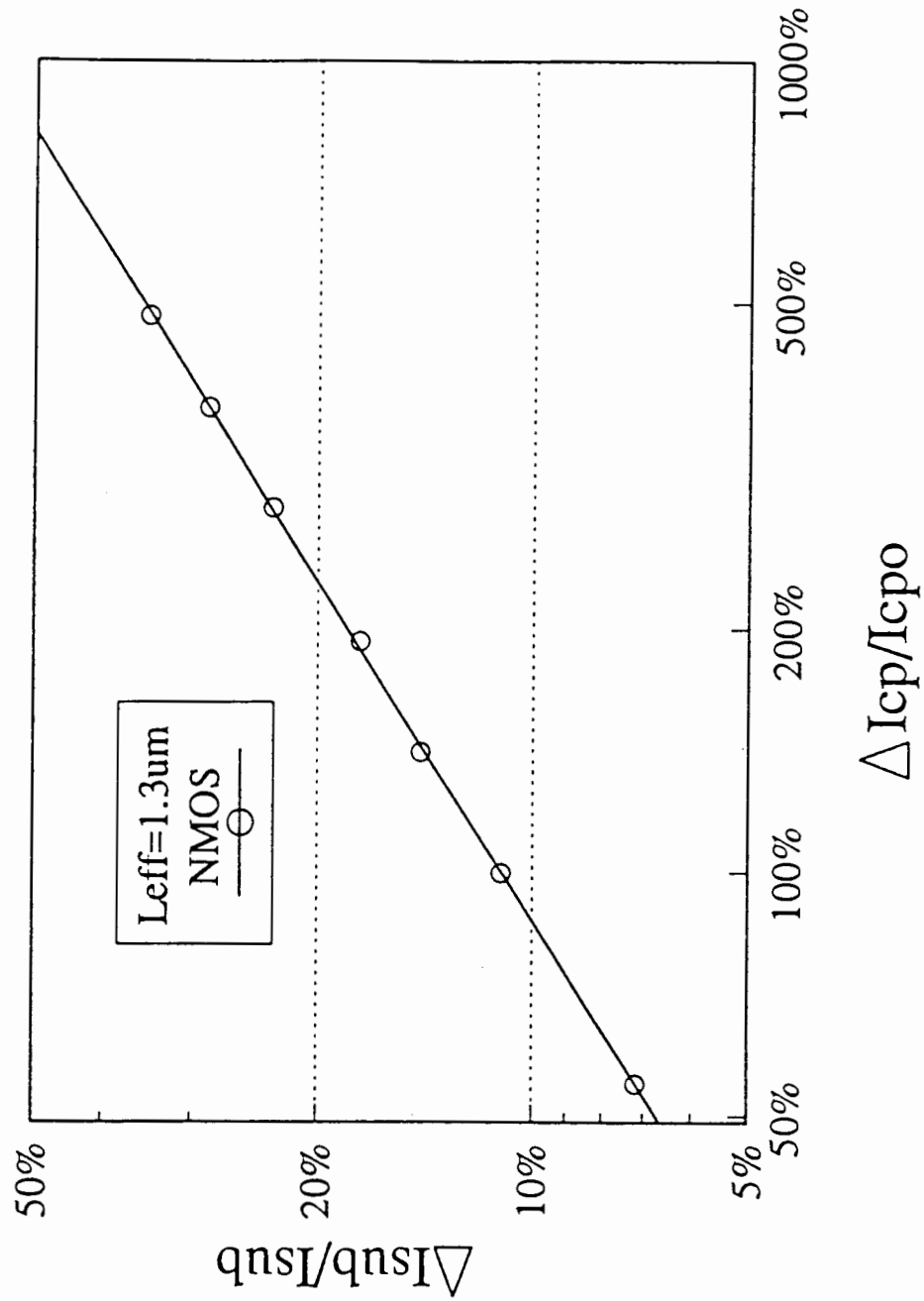

Figure 6.8 Relation between I_{sub} and I_{cp} Degradations

do this, we plotted $\frac{\Delta I_{sub}}{I_{sub}}$ against $\frac{\Delta I_{cp}}{I_{cp}}$ in figure 6.8. The slope of the line is found to be 0.72. Comparing equations (6.2.1), (6.2.2), and (6.2.7), we have:

$$\frac{\Delta I_{sub}/I_{sub}}{\Delta N_{it}} \sim I_D^{(1-\alpha_{it})} \frac{e^{-\Phi_i/kT_e}}{e^{-\alpha_{it}\Phi_{it}/kT_e}} t^{-\alpha_{it}} \sim \frac{t^{\alpha_{sub}}}{t^{\alpha'_{it}}} . \tag{6.2.8}$$

Considering the fact that under HCI stress, the change of I_D is relatively smaller. Then from the slope of 0.72 (in logarithm scale) in figure 6.8, we have:

$$\frac{\Phi_i/kT_e}{\alpha_{it}\Phi_{it}/kT_e + \alpha_{it}\ln t} \approx \frac{\alpha_{sub}}{\alpha'_{it}} \approx \frac{0.33}{0.46} \approx 0.72 \tag{6.2.9}$$

This is again an evidence of that both Φ_i/kT_e *and* Φ_{it}/kT_e are functions of HCI stress time, and their time dependence can be derived from equations (6.2.1), (6.2.2), and (6.2.7) as follows:

$$-\Phi_i/kT_e = \alpha_{sub}\ln t \tag{6.2.10}$$

and

$$-\alpha_{it}\Phi_{it}/kT_e = (\alpha'_{it} - \alpha_{it})\ln t \tag{6.2.11}$$

Assuming that $\Phi_i \approx 1.3eV$, *and* $\Phi_{it} \approx 3.3eV$ are constants [Chun90], and substituting them into the above equations, we have:

$$kT_e \approx \frac{-4.3}{\ln t} \tag{6.2.12}$$

and

$$\alpha_{it} \approx 0.26 . \tag{6.2.13}$$

However, the physical relation between the effective electron temperature and the interface state generation is unknown, and it is a very interesting topic for further investigation.

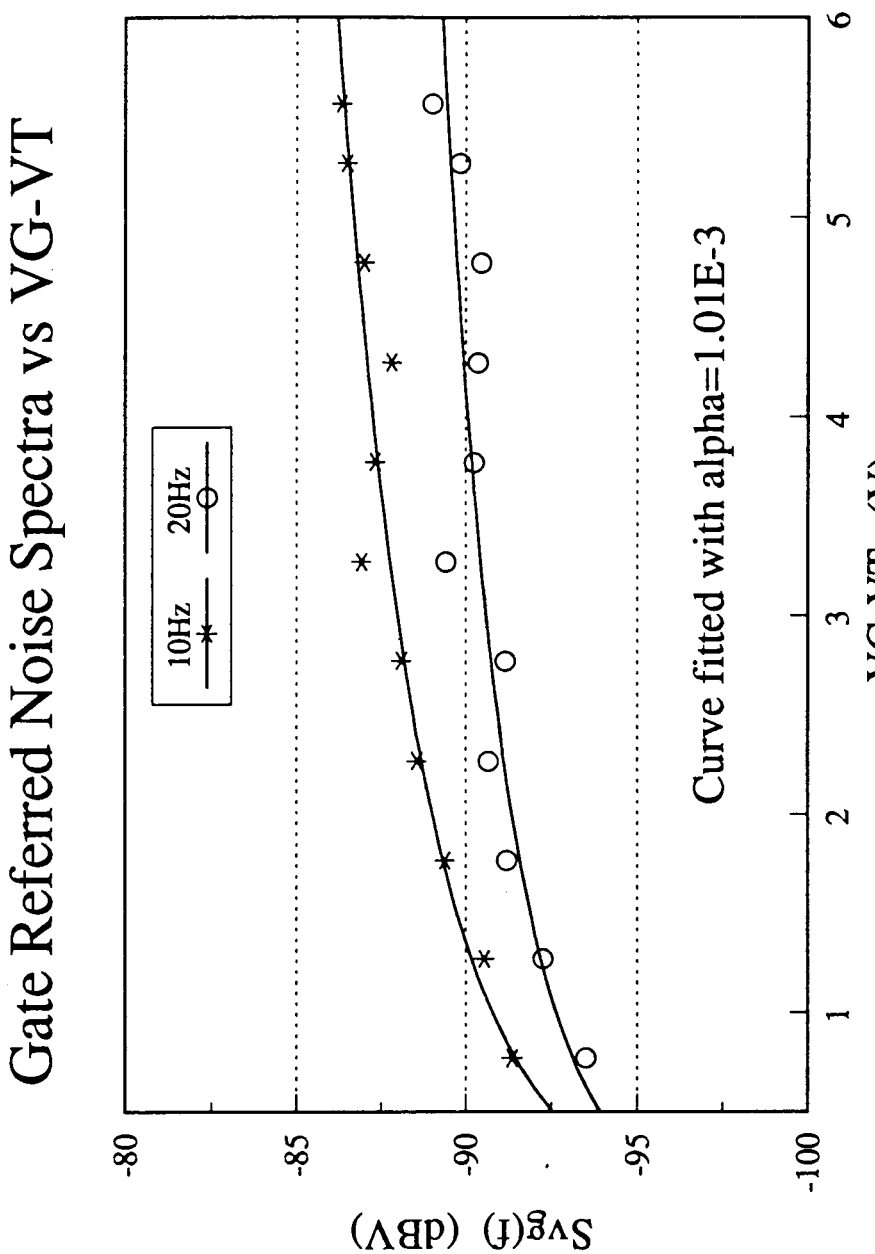

Figure 6.9 $S_{vg}(f)$ vs $V_G - V_T$

§6.3 Low Frequency Noise in MOSFETs

In figure 6.9, we showed a typical result of 1/f noise in short channel MOS device at frequencies of 10 and 20Hz. The bias points of the measurement were shown by solid black squares on figure 6.10. The effective channel length of the device is 1.4μm, the width is 10μm, and the oxide thickness t_{ox} is 250Å. From the DC curve in figure 6.10, we can find that the device was in the deep saturation region under the bias conditions. The solid lines in figure 6.9 were the theoretical predictions with $\alpha_H \approx 1.01E-3$. As we can see, the agreement is good. The experimental results at higher bias voltages were lower than predicted values, and this can be explained by the decrease of number of interface states due to the effective channel length shortening [Deen91].

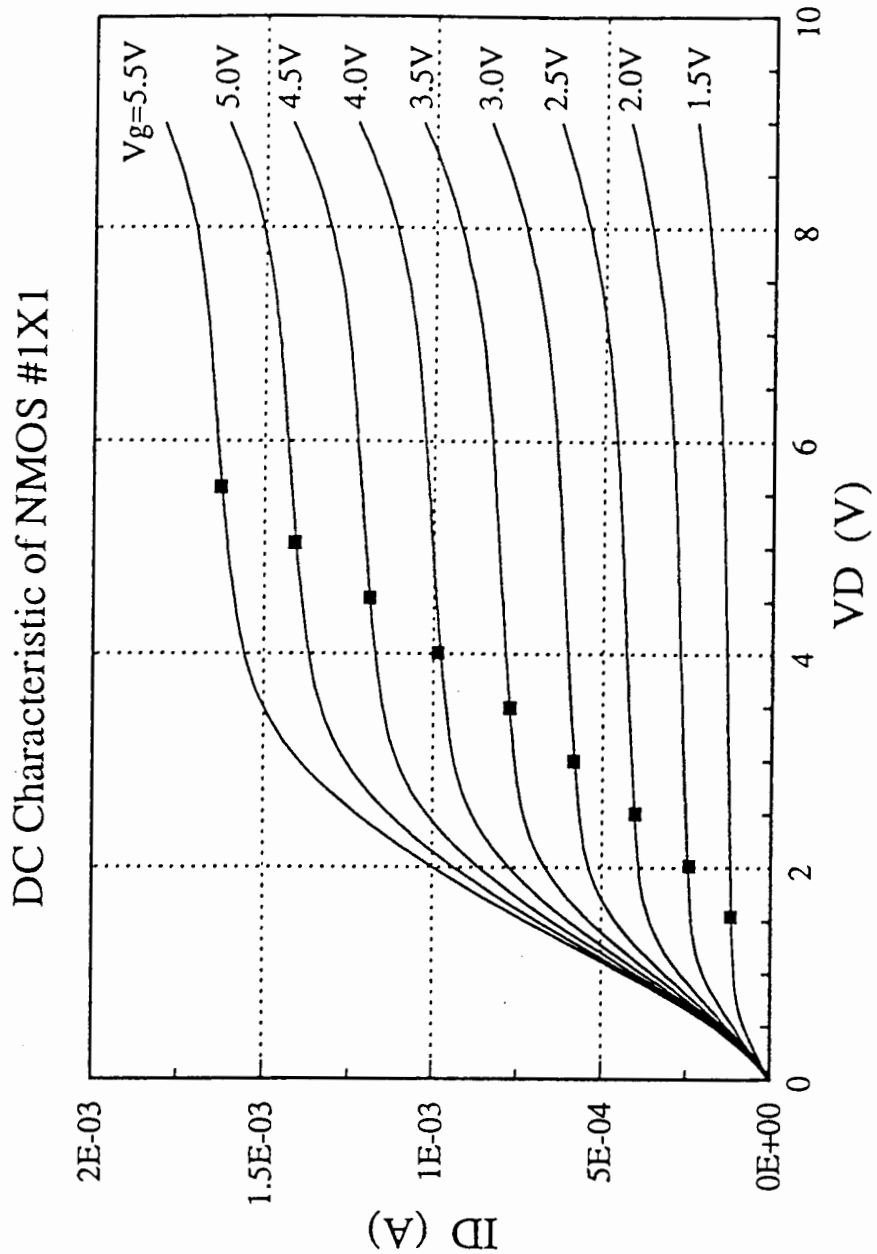

Figure 6.10 Bias Points of $S_{v_g}(f)$ Measurements

Chapter 7 Conclusions

Three major tools for investigating the hot-carrier effects in MOSFETs have been used and/or modified. A spatial profiling charge pumping (SPCP) method and a physical model for 1/f noise in saturation were proposed. The DC parameter degradation was monitored as a function of hot-carrier stressing time, and an empirical time dependent of effective electron temperature has been found.

The main advantage of SPCP method is that it allows us to measure arbitrary distribution of interface states without making any assumption on its distribution. The distribution near the source and the drain can be measured independently. It may cover any part of the channel, provided that the channel is not too long. The proposed method is also a powerful tool for investigating hot-carrier-injection effects, especially for the short channel devices.

N_{it} is found to be non-uniformly distributed along the channel even though in unstressed devices, and peaks of N_{it} can be found at both the source and the drain side of the channel. After the HCI stress, new interface states are mostly generated near the drain junction and there is almost no change in near the source junction.

The proposed low frequency noise model for MOSFET in saturation mode was compared with our experimental results, and good agreement has been found.

The DC parameter degradation due to hot-carrier effects was studied by examining the maximum trans-conductance g_m, the substrate current I_{sub} and the charge pumping current I_{cp} degradations under the hot-carrier stress. The t^{α} dependent has been observed for all of these DC parameters.

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