INVESTIGATION OF THERMAL MAPPING METHODS ON INTEGRATED CIRCUITS

by

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ABSTRACT

The reliability of an integrated circuit (IC) is a strong function of temperature. In this study, we developed computer-aided design tools to predict the temperature distribution of an IC die and compared it with thermal maps obtained by infrared (IR) imaging. A temperature sensor array fabricated on test chips was used to measure the actual surface temperature of an IC die.. This array was used to validate the data obtained by IR imaging.

DEDICATION

To my wife

ACKNOWLEDGEMENTS

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CHAPTER 1

TEMPERATURE DISTRIBUTION DETERMINATION: RELATIONSHIP TO RELIABILITY

1.1 THE SIGNIFICANCE OF THIS STUDY

In this section we discuss the relationship between temperature and reliability. We also overview completed and on-going research in the area of IC reliability related to temperature. We also point out the unique features of our research on IC thermal maps.

1.1.1 Temperature and Reliability

The reliability of an electronic component is a strong inverse function of temperature. A 1985 DOD (The U.S. Department of Defence) study grouped electronic failures according to environmental factors and found that problems caused to heat were the cause of more breakdowns than were any other such factors-including vibration and humidity. One of the most useful models relating component lifetime to temperature has for many years been the Arrhenius model. The rationale for this model is that the strength of degradation leading to component failure is governed by chemical and physical processes with the reaction rate:

$$r = A\ exp(-E_a/kT) \qquad (1.1)$$

where A is a constant; E_a is the activation energy for a certain mechanism of failure in Joules; k is Boltzmann's constant ($k=1.38\times10^{-23}$

joule/ ^0K) and *T* is the absolute temperature. If the reaction rate follows the Arrhenius model, the temperature-life time relationship will be

$$t = C \exp(E_a/kT) \qquad (1.2)$$

where *C* is a (temperature-independent) constant. In terms of failure rate this equation is

$$\lambda(T) = K \exp(-E_a/kT) \qquad (1.3)$$

Although there are many factors which cause electronic components to fail, most failures are temperature related. For example, time-dependent dielectric breakdown(TDDB) (also called oxide wearout) is a significant cause of failure in such integrated circuits as metal-oxide-semiconductor(MOS) devices [7]. During the process that results in TDDB, a device's oxide dielectric layer degrades due to the existence of hole-electron pairs in the oxide and a resultant accumulation of holes at the cathode. This accumulation increases the electric field at the cathode, eventually causing a destructive short circuit. This process occurs six times as fast at 70°C as at 20°C. Another cause of failure is even a slight contamination in the gold component of an aluminum-gold bond which causes the bond to separate. This is a deficiency that occurs twice as fast at 80°C as at 70°C. Solder joints also fail more often as operating temperatures rise[7]. The above-mentioned failure mechanisms frequently lead to catastrophic failure. Temperature also influences the device parameters. Virtually every transistor parameter is directly or indirectly affected by temperature because of the thermal dependence of

the electromechanical characteristics of the silicon crystal. Electrical properties of the material (such as conductivity and intrinsic carrier concentration) are strongly dependent on the effect of temperature on mobilities and band-gap energy. In addition, the mechanical properties of crystal lattices are temperature-sensitive, thereby influencing heat conductivity and capacity [64]. Fig.1.1 describes the relationship between the failure rates of electronic parts and system, and temperature [7].

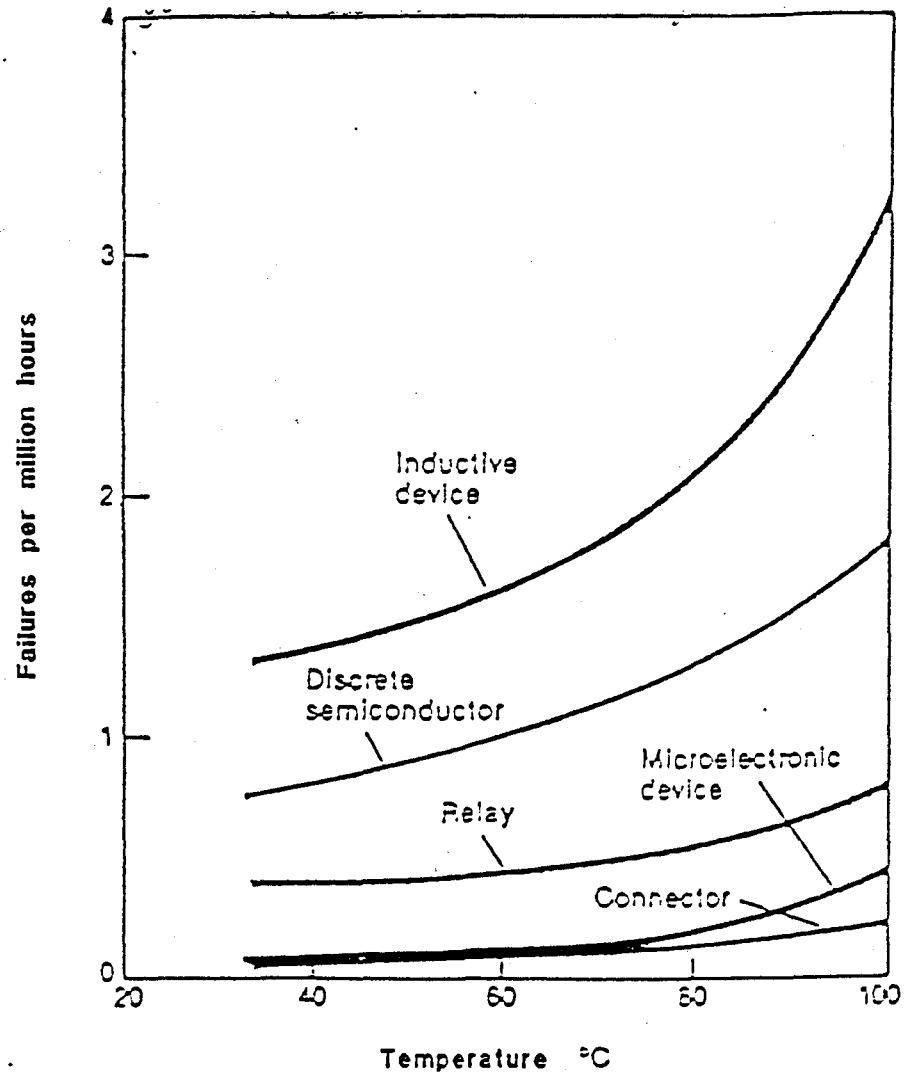

Fig.1.1 Failure rates of electronic parts and systems vs increases in temperature

Due to the strong relationship between temperature and electronic device reliability, a broad field of research is opening up with the purpose of carrying out thermal distribution studies on printed circuit boards and integrated circuits.

1.1.2 Overview on Research Work in The Area of IC Reliability Related to Temperature

Although we will focus our discussion on integrated circuits, it is worthwhile to review what has already been accomplished with regard to printed circuit boards. Since temperature is a critical factor in reliability prediction of PCBs and ICs, for many years research in this area has concentrated on determining temperature distribution on PCBs or IC capsules[2][6]. The method of temperature measurement takes one of two forms: direct (infrared image) and indirect. The most popular sensor used in indirect measurement is the thermocouple. Recently, the IR scanner has become an attractive tool for this application[3][7][31][41].

Using an IR camera,temperature variations as small as 0.1°C between points on the tested board can be detected and compared with a composite image from several functioning boards of the same type. Components operating either above or below the specified temperatures are highlighted: short circuits will appear hotter than normal, while breaks in circuits will appear cooler.

Powerful software which can access a component library including all parts specified on the Military Handbook (MIl-HDBK)-217e, and which can interface with an IR scanner to calculate the Mean Time Between Failure (MTBF), has been developed successfully at the School of Engineering

Science, Simon Fraser University [2]. This system is able to give the MTBF of a PCB of 100 ICs within a half hour from the taking of an IR image to the printing out of a hardcopy report.

Another direction of thermal analysis is simulation. The equations that govern heat transfer within a system are generally solved by a finite-difference technique employing a thermal model [81]. No more than 10 years ago, a model with 1000 nodes was considered too large for easy analysis of its thermal characteristics; now systems with as many as 50,000 nodes can be analyzed economically. This allows accurate prediction of the temperature of hundreds of parts mounted on printed-circuit-boards, including those parts with intricate copper cutouts linking the components.

Recently, because of the complexity of modern PCB designs consisting of hundreds of components, PCB layout, and, in particular, the placement of components, has become a task which is extremely time-consuming and which involves decision making which is often beyond the expertise of a design engineer. To help the design engineer, CAD techniques have been developed. For example, a number of programs are available which automatically place components on a PCB and which minimize the total wirelength. Unfortunately, such programs typically neglect placement based on other measures, such as reliability [16]. A recently developed system called TRP (Thermal reliability predictor) is taking into account placement based on reliability. Hughes Aircraft's Product Analysis Laboratory, EL Segundo, Calif., developed an automated system for printed-circuit boards (called Advanced CAD/R), one for hybrid microcircuits (Hybrid), and one for VLSI circuits (VLSI-D)[7]. The advantage of the above-mentioned software is that the results of thermal

analysis can be fed back quickly to the designers who may then immediately identify and correct unacceptable designs.

An infrared scanning system has been used for temperature verification of the hybrid microelectronic circuit design [43][59]. After a hybrid microelectronic circuit prototype has been built, and before its serial production, its thermal verification has proven very useful. The demands placed on microcircuits by MIL-STD-883 constitute the driving force behind thermal considerations in hybrid design. Many companies address junction-to-case and case-to-ambient thermal considerations after they build pilot units and before they can take temperature measurements. At this point in the design cycle, it is usually too late to redesign the circuit or to change package types in order to bring case and junction temperatures to within allowable limits. Therefore, it is critical to predict worst case junction temperatures in the early design stages. Early on, an engineer can add features to the design that will provide suitable power dissipation and hence avoid exceeding the maximum temperatures on specific devices, as dictated by process and material constraints. Thermal analysis should address device parameters, layout, package type, and reliability [59].

Recently, the thermal characteristics of ICs have been studied. Most published papers in this area concentrate on the thermal evaluation of VLSI packages [8][62][63][64]. Some papers discuss the thermal analysis of multiple-layer structures, the results of these analyses being applicable to IC structure [1][5][65].

1.1.3 Temperature Distribution on a Chip

In this study, we combined three different methods of determining

temperature on a VLSI die. These methods are theoretical analysis, infrared scanner, and "on – chip" temperature sensor[1], with special emphasis on the analytical method. Our study also involved three features which applied to all methods, as described below.

First, we interface existing CAD tools [63] with a temperature distribution (TD) program developed as part of this study. This program calculates the temperature distribution in an integrated circuit by analytical solution of Laplace's equation. For semi-custom IC design, the TD program extracts geometric parameters from the layout data base provided by designers. Another program, also developed in this study, extracts the power dissipation of each discrete device on the die from the output files of circuit simulation software. The geometry and power dissipation of discrete devices are used as input data to run the TD program. Thus this software enables design engineers to model alternative designs quickly and flexibly. Another program developed in this study enables printer or colour plotters to present results graphically to designers - an important feature, since hot spots can then be identified at a glance.

Second, due to the interactive capability of the TD program, our software package allows us to add reliability to the IC design. Thus, we can predict the MTBF of IC at the design stage. Discrete devices on an IC die under high electrical load can produce nonuniform junction temperature distribution on a chip. Since most failure mechanisms are temperature dependent a knowledge of precise junction temperature is essential for accurate reliability projection. The program TD solves Laplace's equation analytically with appropriate boundary conditions for giving the precise temperature distribution in a three-dimensional IC model,

including junction temperature of discrete devices on the IC die. The calculated temperature variation may be seen from device to device as well as within the same metal via region. Given that each device or region is at a different temperature, the implication for reliability is that different acceleration factors must be calculated. The resultant reliability calculation is more accurate than a calculation which assumes an average junction temperature for all discrete devices on the die. Also, the ability to predict temperature from a theoretical calculation greatly helps the reliability stress design. This kind of thermal analysis should also address device parameters, layout, and package type. The device parameters (semiconductor carrier concentration and mobility) are influenced by temperature, which degrades high frequency capability. The built-in emitter-base diode potential of bipolar transistors decreases with temperature. As more current is injected into the base, current distribution becomes non-uniform.

Layout: Circuit layout should avoid hot spots on the die. Power dissipation should be as uniform as possible. Since the thermal model neglects thermal coupling between adjacent devices, high power dissipating devices should be separated from each other so that thermal coupling does not significantly affect junction temperature . For circuits requiring the same temperature at first-stage transistors thermal analysis is especially useful.

Package type: The package case and die attachment materials particularly affect the temperature distribution on the die.

Third, since we combine three methods , the focus of this study is not only on thermal analysis, but also on other related fields, including emissivity study, IR camera calibration, IC defect and package study.

The TD program takes geometrical and thermal parameters from the IC structure model as input and produces a theoretical thermal map. Thus by changing the conductivity and thickness of the die attachment, we can achieve a number of different simulated thermal maps.

1.2 COMPUTER-AIDED ENGINEERING ON HEAT TRANSFER

In order to solve the heat conduction equation we use either Fourier transform or finite element analysis. Computer-Aided-Engineering, based on the algorithms obtained from the above mentioned methods, was used to speed up the calculation of results for the temperature distribution in ICs.

1.2.1 The Heat Conduction Equation

Based on the first law of thermodynamics and Fourier's law of heat conduction, we can obtain the General Heat Conduction Equation for an isotropic solid continuum

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) + \dot{q} = \rho c_v \frac{\partial T}{\partial t} \qquad (2.1)$$

Here k is thermal conductivity

ρ is material density

c_v is specific heat

q is heat generation

For constant k, ρ, and c_v, Eq. (2.1) simplifies to:

$$\frac{\partial T^2}{\partial x^2} + \frac{\partial T^2}{\partial y^2} + \frac{\partial T^2}{\partial z^2} + \frac{\dot{q}}{k} = \frac{1}{\alpha}\frac{\partial T}{\partial t} \qquad (2.2)$$

where $\alpha = k/\rho c$ is the material thermal diffusivity

Considering only steady heat flux ($\partial/\partial t=0$) with constant k, Eq. (2.2) reduces to

$$\frac{\partial T^2}{\partial x^2} + \frac{\partial T^2}{\partial y^2} + \frac{\partial T^2}{\partial z^2} = \nabla^2 T = -\frac{\dot{q}}{k} \qquad (2.3)$$

called Poisson's equation

In the case of no heat generation, q = 0:

$$\nabla^2 T = 0 \qquad (2.4)$$

called Laplace's equation

1.2.2 Different Techniques To Solve Heat Distribution Problem

There are exact analytical and numerical techniques to solve Laplace's differential equation. For regular geometries and simple boundary conditions, an analytical technique may be used. In such a case, Laplace's equation may be solved as a set of algebraic equations. For irregular geometries, complicated boundary conditions, or both, the basic differential equation may be solved approximately by numerical techniques. Two common numerical techniques are the finite-difference method and finite element analysis. These techniques make it possible effects to the

model.

a) **Finite-difference method**

The finite-difference method simulates an ordinary or partial derivative by an algebraic approximation equivalent to the quotient for which limits are taken in calculus derivations. The second derivative may be approximated by [82]:

$$\frac{\partial T^2}{\partial x^2} \simeq \frac{1}{\Delta x}\left(\frac{T(x + \Delta x) - T(x)}{\Delta x} - \frac{T(x) - T(x - \Delta x)}{\Delta x} \right)$$

$$\simeq \frac{T(x + \Delta x) - 2T(x) + T(x - \Delta x)}{\Delta x^2} \qquad (2.5)$$

From the Taylor series expansion, we can find that the error involved is of order $\Delta x^2(\partial^2 T/\partial x^2)$

b) **Finite-element method (FEA)**

Fundamentals of Finite Element Analysis

The flowchart in Fig.1.2 presents the basic steps of Finite Element Analysis.

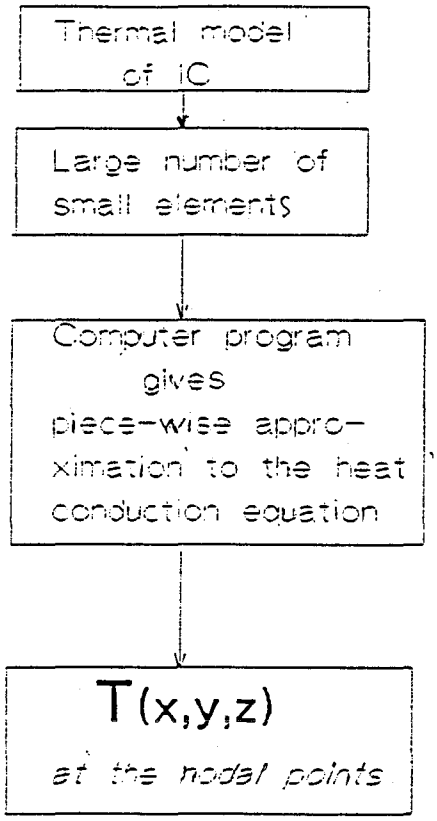

Fig.1.2 The basic steps of Finite Element Analysis

In this flowchart the thermal model is divided into a large number of small elements, interconnected at a discrete number of nodal points describing the geometry. A set of mathematical operations in the computer program give a piece-wise approximation to the heat distribution equations. The basic premise of FEA is that a solution can be analytically approximated by replacing it with an assemblage of simple

(low-order-polynomial) solution.

The main advantage of the TD program over FEA is its high spatial resolution. For the die (LA 253, one semicustom linear array by Genum corporation, Burlington Ontario; the chip size is 2338×2821 μm^2) used in this study, the TD program takes about 180 minutes on IBM AT (8 MHz) to achieve a 20×20×20 μm^3 spatial resolution thermal map. To achieve the same spatial resolution in FEA we need to divide the IC model into 1,000,000 elements. A problem with FEA is that it is CPU-intensive [72]. The model with 1,000,000 elements is not realistic for an FEA software package used on a personal computer. However, the TD program is not always useable. Whenever irregular boundary conditions, convection and/or radiation are involved, FEA is a useful numerical tool.

c) **Analytical technique**

Besides numerical analysis using finite element or finite difference methods, there are closed-form analytic solutions using Laplace and/or Fourier transforms, or Green's function methods for solving the heat flow equation [6]. It is the task of computer code users to ascertain which technique is most suited to the required job. In this study we use the model originally developed by Kokkas [81] in order to simulate the steady-state temperature distribution in the IC chip.

CHAPTER 2

ANALYTIC METHOD FOR TEMPERATURE DISTRIBUTION DETERMINATION ON IC

2.1 ANALYTIC SOLUTION OF LAPLACE'S EQUATION

If k, ρ, c_v and q are independent of temperature, then the heat conduction equation is linear and simple solutions can be combined in order to form more complex solutions. This is the basis for the Fourier series analysis used to solve Poisson's or Laplace's Equation .

2.1.1 Single Rectangular Layer

Consider uniform thermal conductivity in the form of a rectangular box of lateral dimensions L_x, L_y and thickness L_z. Assume no heat flow out of the lateral boundaries of the material, i.e.[5],

$$\frac{\partial T(x,y,z)}{\partial x}\Big|_{x=0,L} = \frac{\partial T(x,y,z)}{\partial y}\Big|_{y=0,L} = 0 \qquad (2.6)$$

Since the model for IC is rectangular, it is convenient to keep Laplace's equation in Cartesian coordinates. The Fourier transform is defined as

$$\tau(f_x,f_y,z) = \int_0^{L_x}\int_0^{L_y} T(x,y,z)exp(-2\pi i(xf_x + yf_y))dxdy \qquad (2.7)$$

where f_x, f_y are the Fourier transform variables which are conjugate to the variables x,y. The inverse Fourier transform is defined as

$$T(x,y,z) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\tau(f_x, f_y,z)exp(2\pi i(xf_x + yf_y))df_x df_y \qquad (2.8)$$

From boundary conditions specified in 2.6, one can deduce that the Fourier transform variable is of the form [5]

$$f_x = \frac{n}{2L_x} \tag{2.9}$$

Then 2.8 may be written as

$$T(x,y,z) = \sum_{n=0}^{\infty} \sum_{m=0}^{8} \frac{4\tau(n,m,z)\cos(n\pi x/Lx)\cos(m\pi y/Ly)}{(\delta_{n0}+1)(\delta_{m0}+1)LxLy} \tag{2.10}$$

where

m,n are integers

and $\tau(n,m,z) = \alpha\cosh(\gamma z) + \beta\sinh(\gamma z)$ (2.11)

where $\gamma = \left\{\left(\frac{n\pi}{L_x}\right)^2 + \left(\frac{m\pi}{L_y}\right)^2\right\}^{1/2}$ (2.12)

and the coefficients α and β are determined from the two z-dependent boundary conditions.

2.1.2 Three-Layer Rectangular Structure

A three-layer structure is assumed to have the geometric form presented in Fig 2.1. The three layers are characterized in terms of thermal conductivities and thicknesses Ki,Li(i = 1,2,3). In the case of an IC, the top layer is the semiconductor device, the middle layer is the die attachment and the bottom layer is the carrier . Power sources are

assumed to be on the surface of the semiconductor device.

$$k_1 \frac{\partial T_1(x,y,z)}{\partial z}\Big|_{z=0} = P(x,y) \qquad (2.12)$$

Where $P(x,y)$ is power density.

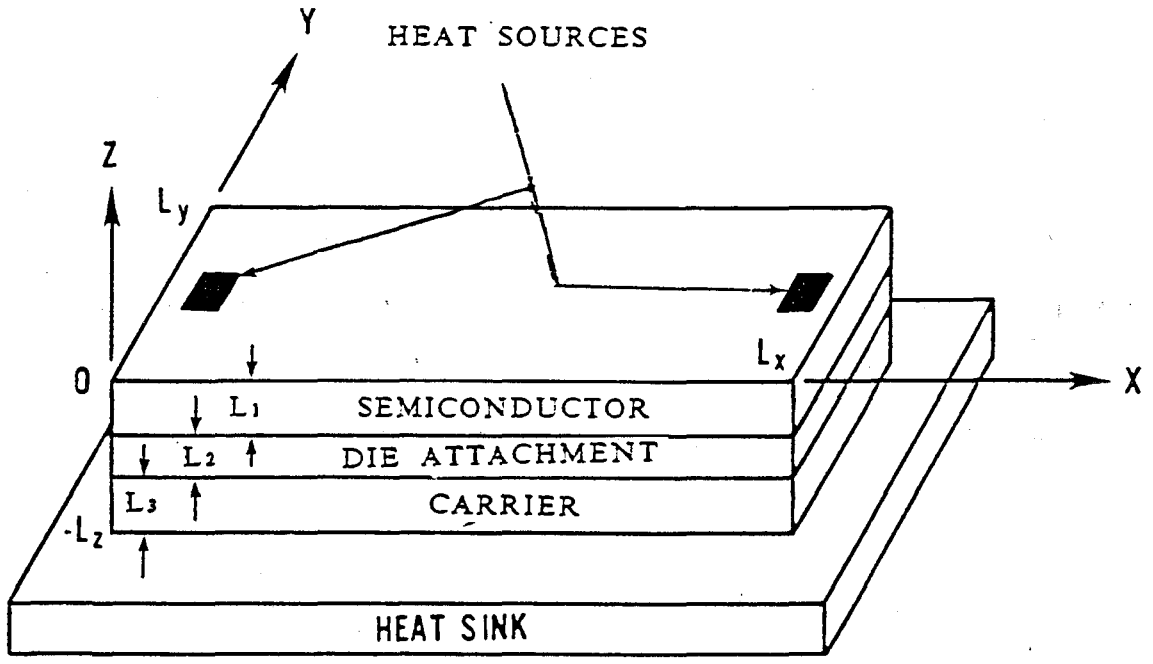

Fig. 2.1 The geometry of the IC three-layer structure

All three layers of the model are assumed to have the same lateral dimensions. It is assumed that there is no heat flow out of the lateral boundaries of the structure due to either convection or radiation. So

$$\left.\frac{\partial T_i(x,y,z)}{\partial x}\right|_{x=0,L_x} = \left.\frac{\partial T_i(x,y,z)}{\partial y}\right|_{y=0,L_y} = 0 \qquad (2.13)$$

The assumption that the temperature is continuous across the interfaces between the layers may be written as

$$T_1(x,y,z)\Big|_{z=L_1} = T_2(x,y,z)\Big|_{z=L_1} \qquad (2.14a)$$

$$T_2(x,y,z)\Big|_{z=-(L_1+L_2)} = T_3(x,y,z)\Big|_{z=-(L_1+L_2)} \qquad (2.14b)$$

The assumption that the heat flow is continuous across the interfaces between the layers is expressed by the conditions that

$$k_1\left.\frac{\partial T_1(x,y,z)}{\partial z}\right|_{z=-L_1} = k_2\left.\frac{\partial T_2(x,y,z)}{\partial z}\right|_{z=-L_1} \qquad (2.15a)$$

$$k_2\left.\frac{\partial T_1(x,y,z)}{\partial z}\right|_{z=-(L_1+L_2)} = k_2\left.\frac{\partial T_2(x,y,z)}{\partial z}\right|_{z=-(L_1+L_2)} \qquad (2.15b)$$

Finally, assuming that the heat sink, which is in contact with the bottom layer, is ideal and has a temperature equal to the ambient. This implies

$$T_3(x,y,z)\Big|_{z=-L_x} = T_a = 0 \qquad (2.16)$$

Solving Laplace's Equation with the stated boundary conditions, we obtain

$$T_i(x,y,z) = P_0 \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{4U(n,m)\tau_i(n,m,z)\cos(n\pi x/L_x)\cos(m\pi y/L_y)}{(\delta_{n0}+1)(\delta_{m0}+1)L_xL_yk_1} \qquad (2.17)$$

where $U(n,m)$ is power density function,

P_0 is the steady-state power density per unit area.

For i=1,2,3 to obtain the solutions in each of the three layers.

Here τ_i (i = 1,2,3) are Fourier coefficients

$$\tau_1(n,m,z) = \frac{\Omega(\gamma)\cosh(\gamma(L_1+z))}{\gamma\cosh(\gamma L_1)}\left(\tanh(\gamma L_3) + \frac{k_3}{k_2}\tanh(\gamma L_2)\right.$$

$$\left. + \tanh(\gamma(L_1 + z))\frac{k_2}{k_1}(\tanh(\gamma L_3)\tanh(\gamma L_2) + \frac{k_3}{k_2})\right) \quad (2.18)$$

$$\tau_2(n,m,z) = \frac{\Omega(\gamma)\cosh(\gamma(L_1 + L_2 + z))}{\gamma\cosh(\gamma L_1)\cosh(\gamma L_2)}\left(\tanh(\gamma L_3)\right.$$

$$\left. + \frac{k_3}{k_2}\tanh(\gamma(L_1 + L_2 + z))\right) \quad (2.19)$$

$$\tau_3(n,m,z) = \frac{\Omega(\gamma)\sinh(\gamma(L_1 + L_2 + L_3 + z))}{\gamma\cosh(\gamma L_1)\cosh(\gamma L_2)\cosh(\gamma L_3)} \quad (2.20)$$

Here $\Omega(\gamma)$ =

$$\frac{1}{\left(\tanh(\gamma L_3)\tanh(\gamma L_1) + \frac{k_3}{k_2}\tanh(\gamma L_1)\tanh(\gamma L_2) + \frac{k_2}{k_1}\tanh(\gamma L_3)\tanh(\gamma L_2) + \frac{k_3}{k_1}\right)} \quad (2.21)$$

2.2 Interactive Computer Program

We use a computer program based on equations 2.17 - 2.20 in order to calculate the temperature distribution on the surface of the top layer. Recently this program was modified to match the need for a practical number of heat sources with different power densities. The results of the calculation can be presented in a table or in a format which can be easily interfaced with graphic software tools . The temperature distribution also can be drawn using three dimensional graphics by a program which converts output data to a format compatible with the Matlab software used for visual printouts. (In this case, a function of Matlab that converts data from matrix form to three-dimensional graphics is used .) Another option for the output data presentation is the use of colour charts.

2.2.1. Interface With CAD Tools

When the computer program is used for temperature mapping of integrated circuits, we need to know the positions, sizes and powers of heat sources. For large-scale integrated circuits, to determine and to enter these parameters manually is tedious. To overcome this difficulty, we interfaced our computer program with existing software tools. The following is a diagram of the interfacing procedure:

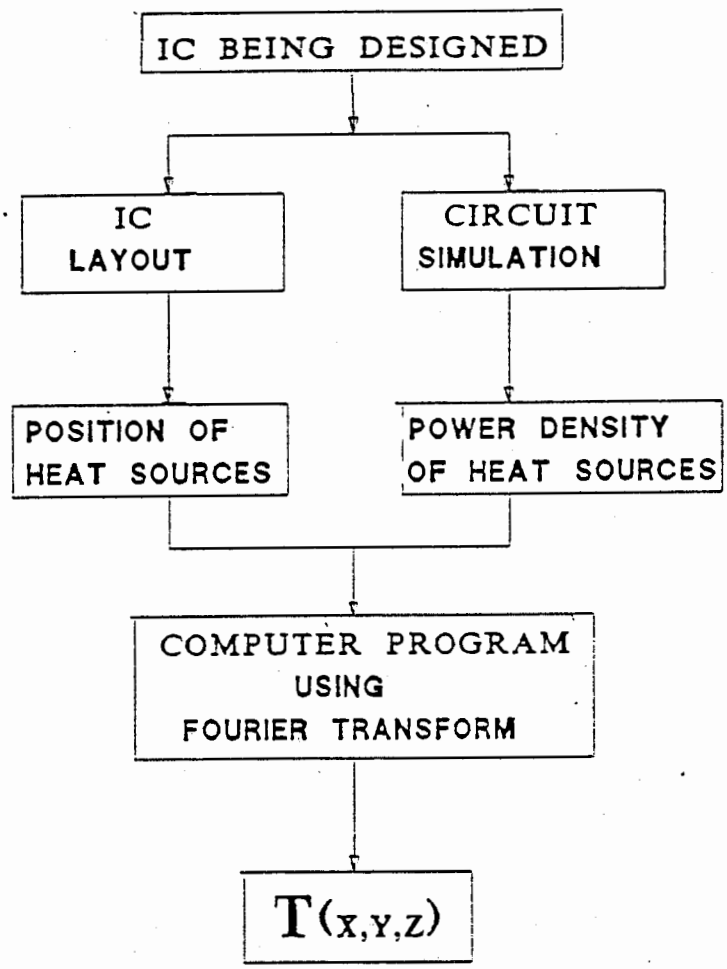

Fig. 2.2 Interface Temperature Distribution program with CAD tools

The purpose of interfacing our computer thermal simulation program with CAD tools is to help IC designers build reliability into the IC. Circuit simulation software plays an important role in studying the

performance of a designed circuit. In this sense, the simulation package can be called a software breadboard. But circuit simulation software does not analyse the power consumption of discrete components. In that situation, "worst case" has been used to quantify failure rates[57]. For example, the failure rate measured through the life testing of a worst case vehicle - in this particular case represented by a chip dissipating maximum power - was found to be 2 to 3 times higher than that measured on randomly selected product ICs, even after compensation for the differences in chip temperatures. To achieve reasonable failure rate estimation we have to consider power dissipation as a key variable that controls the IC reliability. Not only power dissipation, but also the relative positions of discrete components on the IC determine temperature distribution. After designers finish layouts, it is very valuable for semicustom IC design to use the results from circuit simulation and lay-out tools in order to calculate the temperature of each IC component. Thus the incorporation of reliability models into IC CAD tools will proliferate, thereby allowing for reliability to be "built - into" the product. The methods described in this section represent the beginnings of the evolution toward the incorporation of reliability into IC design.

a) Interface with PC-CARDS

We limit our discussion to semicustom chip design. In order to provide design support for various semicustom arrays we use a commercially available CAD software tool called PC-CARDS. This software package works on an IBM-AT microcomputer. In order to use the PC-CARDS PC board layout software from PCAD, the base array data must first be converted to the PCAD database format. First the physical layout information of a

particular base array (e.g. LA251, LA252, and LA253 from Genum Corporation) is obtained from the vendor. This information is supplied in Calma GDS-II format. The GDS-II data is then converted into CIF (CalTech Intermediate Form). The next step of the process is to convert from CIF to PDIF (PCAD Database Interface Format). This conversion is performed by a program called CIF_to_PDIF. The PDIF file is in an ASCII format similar in structure to the EDIF (Electronic Data Interchange Format). The PDIF description is independent of processor type, physical file structures and other machine specific factors. This makes it possible to bring up PDIF files and applications software on virtually any host-based environment. Also, since PDIF is in ASCII form, it can be transferred between systems and modified with any standard text/word processors. The final step of the conversion process is from PDIF to PCAD's internal database format and this is accomplished through the use of the standard PCAD utility PDIFIN. Figure 2.3 shows the LA253 array fully integrated into the PC-CARDS environment and ready for design inputs.

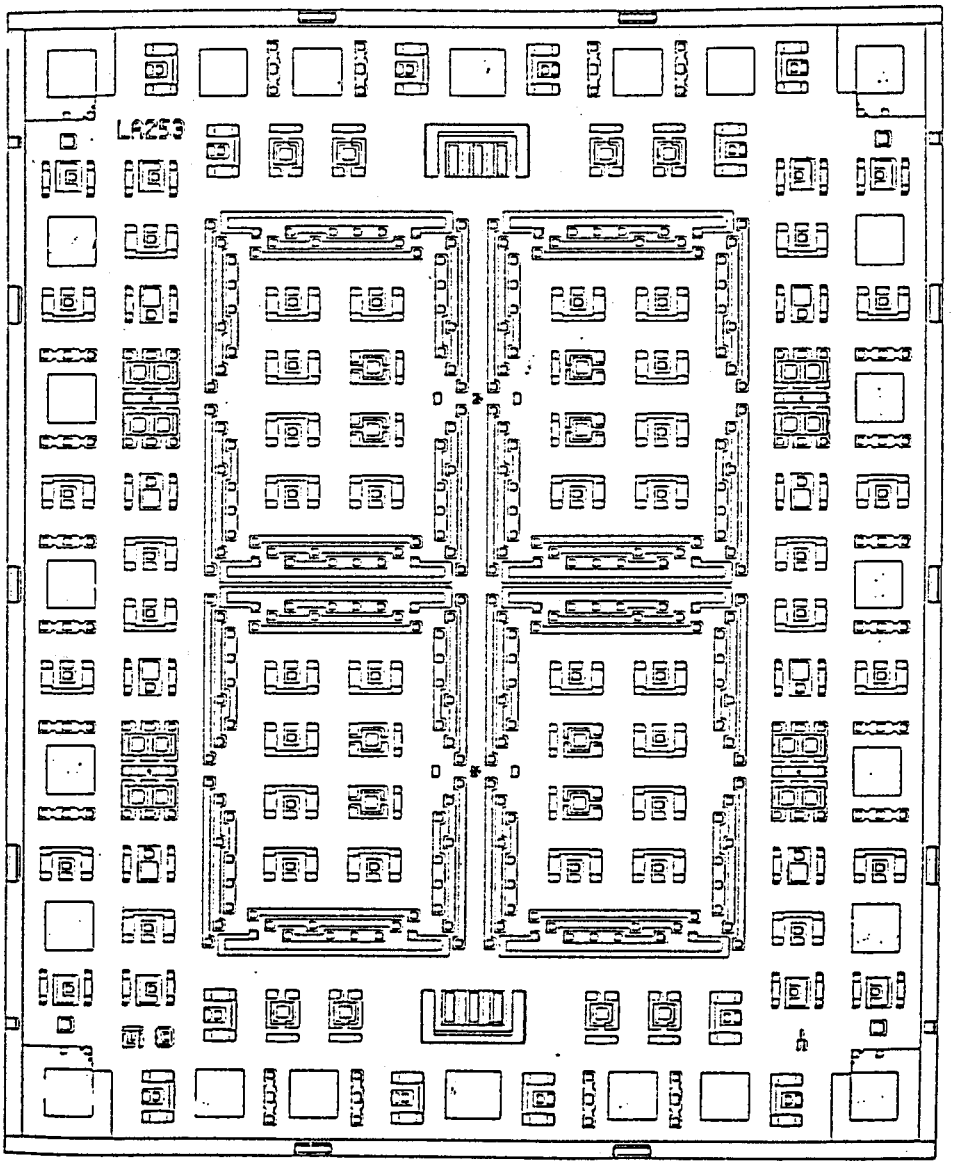

Fig. 2.3 The LA253 array fully integrated into the PC-CARDS environment and ready for design inputs

The design process is relatively simple as the designer is free to use all the human interface facilities (e.g. Zoom, Pan, Edit, etc.) provided by PC-CARDS to create the design file. Designs are created with the "Enter Wire" command. Wires of zero width are used to create arbitrarily shaped polygons. Wires of a given width are used to specify interconnections between various array elements.

After the design has been completed, we can start to work on labelling the heat sources. In the case of PC-CARDS, we use symbol mode to draw polygons around heat sources. These polygons can be saved as components. For the same kind of heat sources, we can use the "enter component" command to put the required polygon on them. This labelling has to be done on a layer which has not been used in the previous design. The labeling information that includes positions and sizes of heat sources is extracted from the PC-CARDS database using the standard PCAD utility PDIFOUT. The output of PDIFOUT provides the definition of various connections in the form of wires of various widths and x,y co-ordinates and is in the form of an ASCII file. This is further processed into a subset of CIF consisting of polygon definition.

P x_1 y_1 x_2 y_2 ..... $x_n y_n$

where

P x_1 y_1 x_2 y_2 ..... $x_n y_n$

is the vertex list from CIF. We achieve position and size of heat sources from the output of PDIFOUT to FORTRAN format data by using a program called P2TD.

b) **Interface with Pspice**

Pspice is a piece of circuit simulation software. One of the results of Pspice is the determination of the voltage at each node in the simulated circuit. We have developed a computer program called S2TD to calculate power dissipation of bipolar and MOS transistors based on the results mentioned above. In turn, the results of S2TD will be the input data for the main simulation program.

2.2.2 Display of Theoretical Thermal Map

Results of the temperature-mapping program can be presented in one of three forms: (1)Table, (2)pseudo-3-dimension graphics and (3)thermal map in colours. To display 3D graphics, we wrote a computer program called TD2GR in order to convert data in table form to a format which can be accepted by the software called Matlab. The displaying and printing out of a hardcopy of a colour thermal map required the modification of the existing software used in the "Thermal Reliability Scanner" system. We wrote a computer program called TD2MAP in order to convert the output data from the TD program to a format which matched the requirements of the scanner.

CHAPTER 3

METHODS OF EXPERIMENTAL DETERMINATION OF TEMPERATURE DISTRIBUTION WITHIN INTEGRATED CIRCUIT

3.1 ON-CHIP-TEMPERATURE SENSORS

We designed and fabricated test chips with temperature sensor arrays on them. These sensors were calibrated individually and were used to measure the actual surface temperature of ICs.

3.1.1 Overview

Different kinds of sensor are used to measure the temperatures of chips. The basic requirements for these sensors are that they be easy to integrate, small, and that they not affect the temperature distribution on the chip. Although temperature-sensitive resistors satisfy these requirements, the need for an external circuit makes them unpopular. Due to its stability and accuracy, the thermo-couple is one of the best choices. Although the size of this kind of sensor was reduced significantly, it nevertheless stays on the chip as an extra component. Diodes, or diode-configured transistors, on the other hand, are ideal temperature sensors as they can be built on the chip.

3.1.2 Design, manufacture, calibration

The flowchart in Fig.3.1 shows the main steps of obtaining on-chip sensors. Each step is explained as following.

a) Design and Fabrication

To detect the junction temperature on a chip, an array of diode-configured transistors has been designed and fabricated using the

LA253 semicustom chip. Power transistors work as heat sources. The coordinates and sizes of the sensors and heat sources are known from the data base LA253.

b) Calibration

Temperature measurements are made using a diode-configured transistor as the temperature-sensing element because its forward voltage changes in inverse linear proportion to its temperature. To obtain a temperature reading curve from a diode forward voltage it is necessary to have calibration curves for the diode voltage versus temperature. Temperature control during calibration was provided by a controlled-temperature oven. To ensure that the oven met the requirements of constant temperature we first tested its performance. Electronic display for temperature readout of the oven was compared with temperature readout from a thermometer. Fig 3.2 show the perfect matching between these two readouts of the temperature range from -20°C to 150°C. When the electronic temperature display showed stable

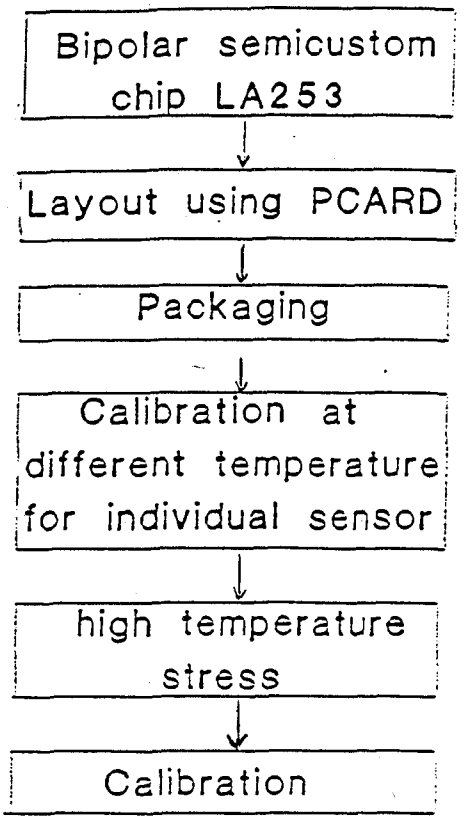

Fig.3.1 Procedure of obtaining on-chip sensor

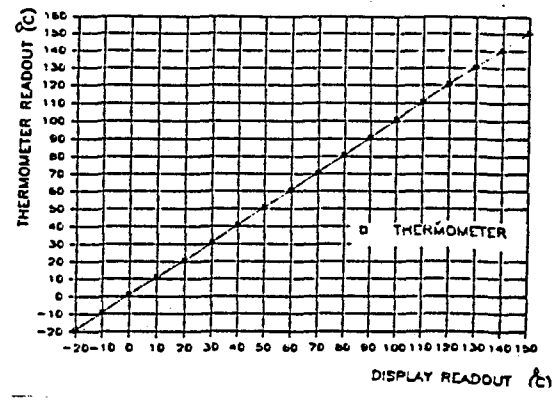

Fig.3.2 Comparison of readouts from thermometer and oven's display

values the thermometer was put in different positions inside the oven in order to measure temperatures. The results of this experiment showed that temperature differences at different positions inside a stable oven are less than 0.1°C.

We also studied the oven's transient characteristics. Fig 3.3 shows the transient time for the oven between room temperature and any other given temperature (60°C, in this experiment). From the curve it is clear that 5 minutes is enough time to get a stable temperature environment in this particular case.

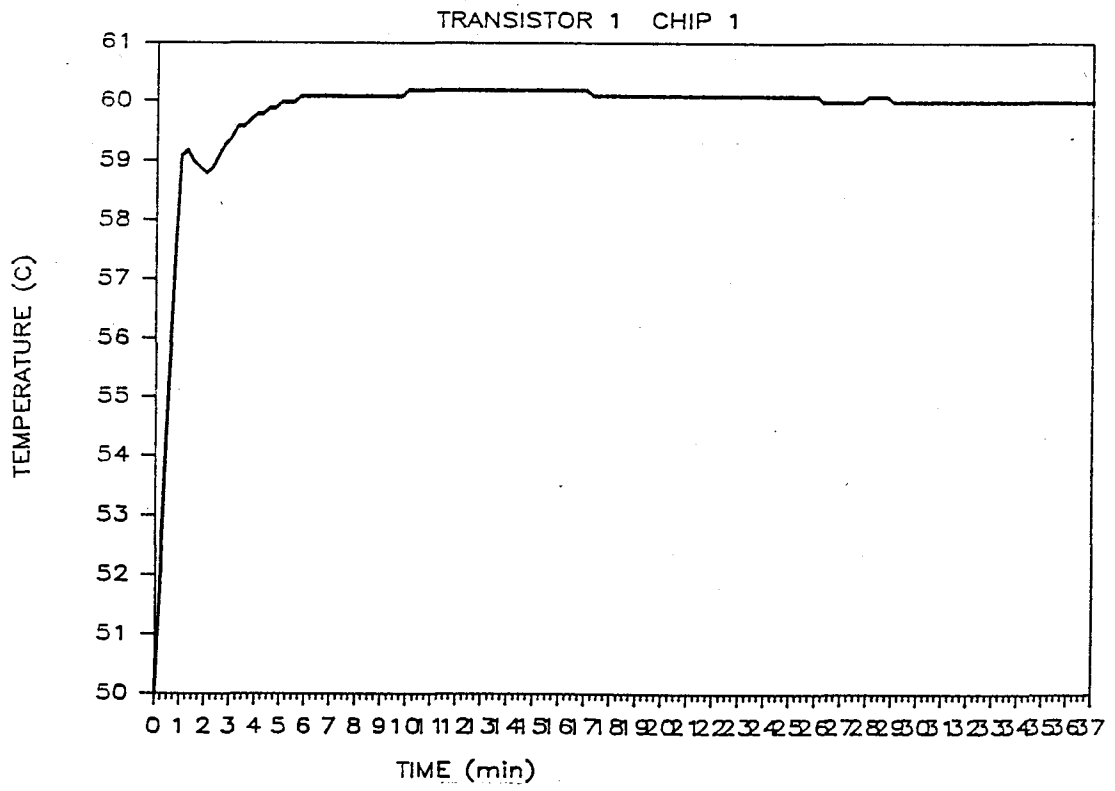

Fig. 3.3 Oven's temperature transient function

Six chips from a batch of 12 were used as test chips. The temperature sensors on each test chip were calibrated individually. Before taking calibration data, we performed an experiment in order to establish the minimum time required for the sensor to obtain the oven temperature in the case of each temperature change. Fig 3.4 shows that about 20 minutes were needed to obtain stable temperature in a PN junction following each change of oven temperature. (The temperature change step was ten degrees.) Each time the temperature in the oven was set to a new value, at least 30 minutes was spent to make sure that the temperature at the test PN junction was stable. On a day to day basis the stability of the temperature sensors was tested against the constant temperature environment in the oven. This experiment shows that 0.1°C accuracy is not difficult to achieve.

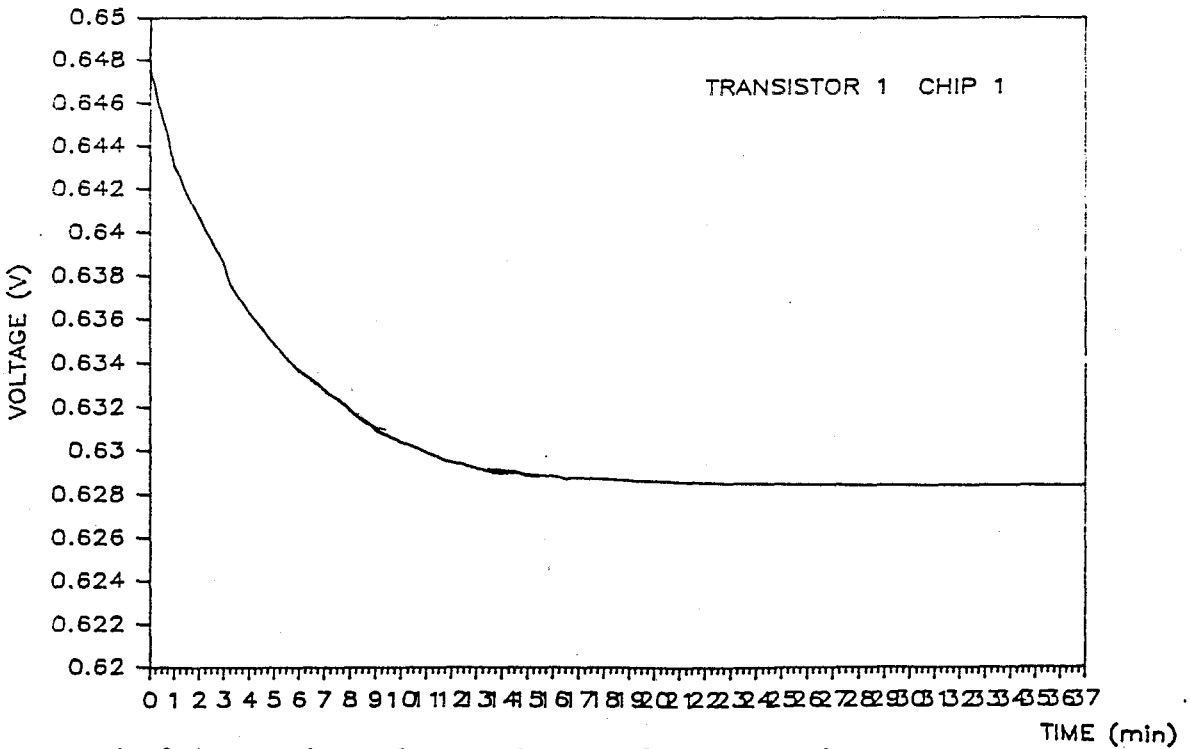

Fig.3.4 Transistor base-emitter voltage vs. time in constant oven temperature

The linearity of a temperature-voltage curve of a sensor is significantly dependent on the current passing through it. The calibrating curves for a diode on a different chip corresponding to a different current are shown in Fig.3.5 through to Fig.3.12. From these figures, we can accept 0.3 mA as the minimum current required in order to achieve good linearity.

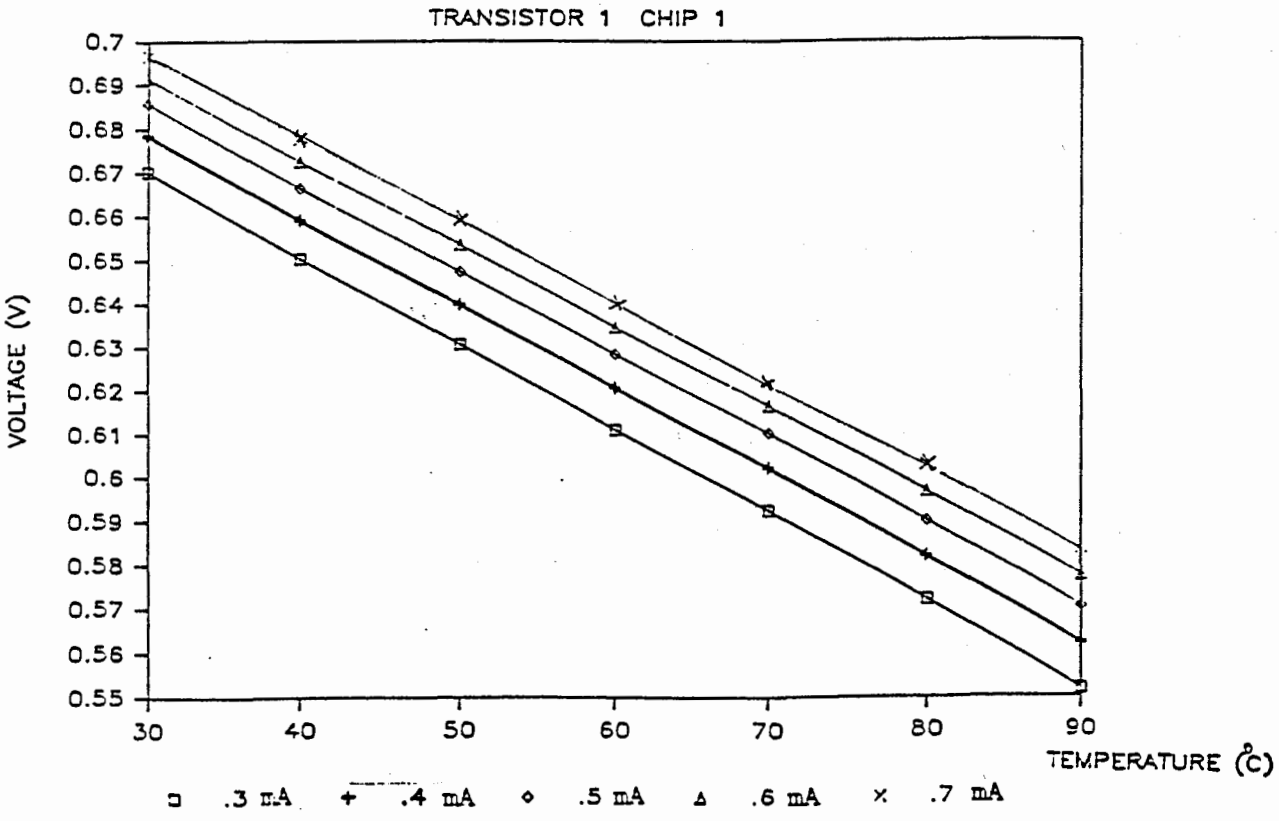

Fig. 3.5 Calibrating curves for transistor #1 on chip #1

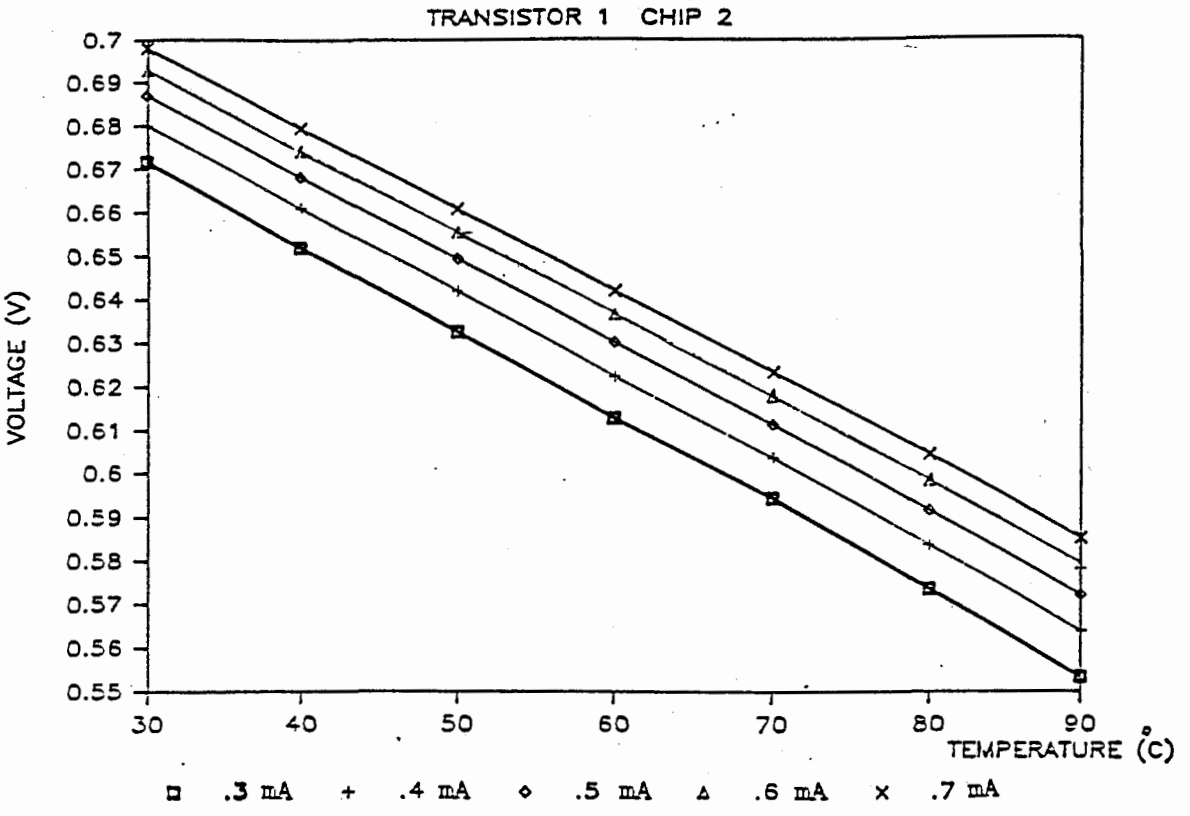

Fig. 3.6 Calibrating curves for transistor #1 on chip #2

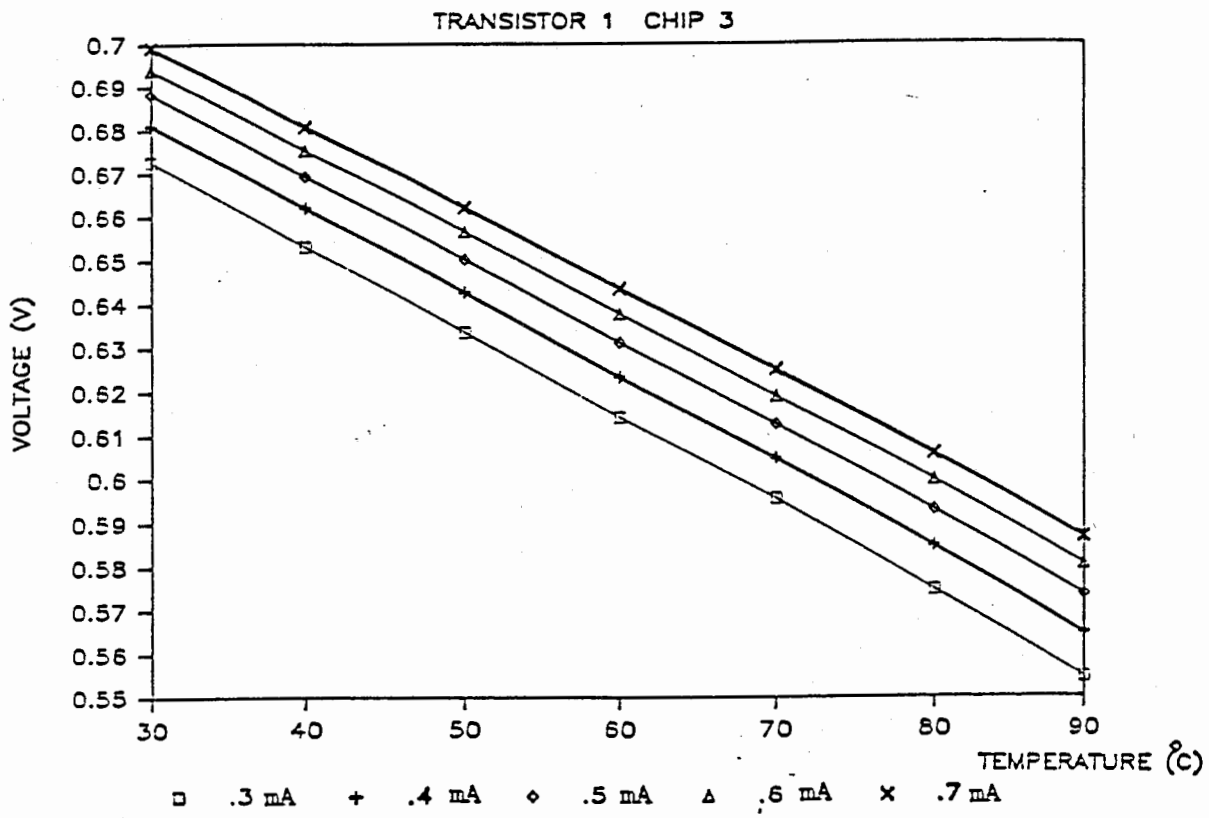

Fig. 3.7 Calibrating curves for transistor #1 on chip #3

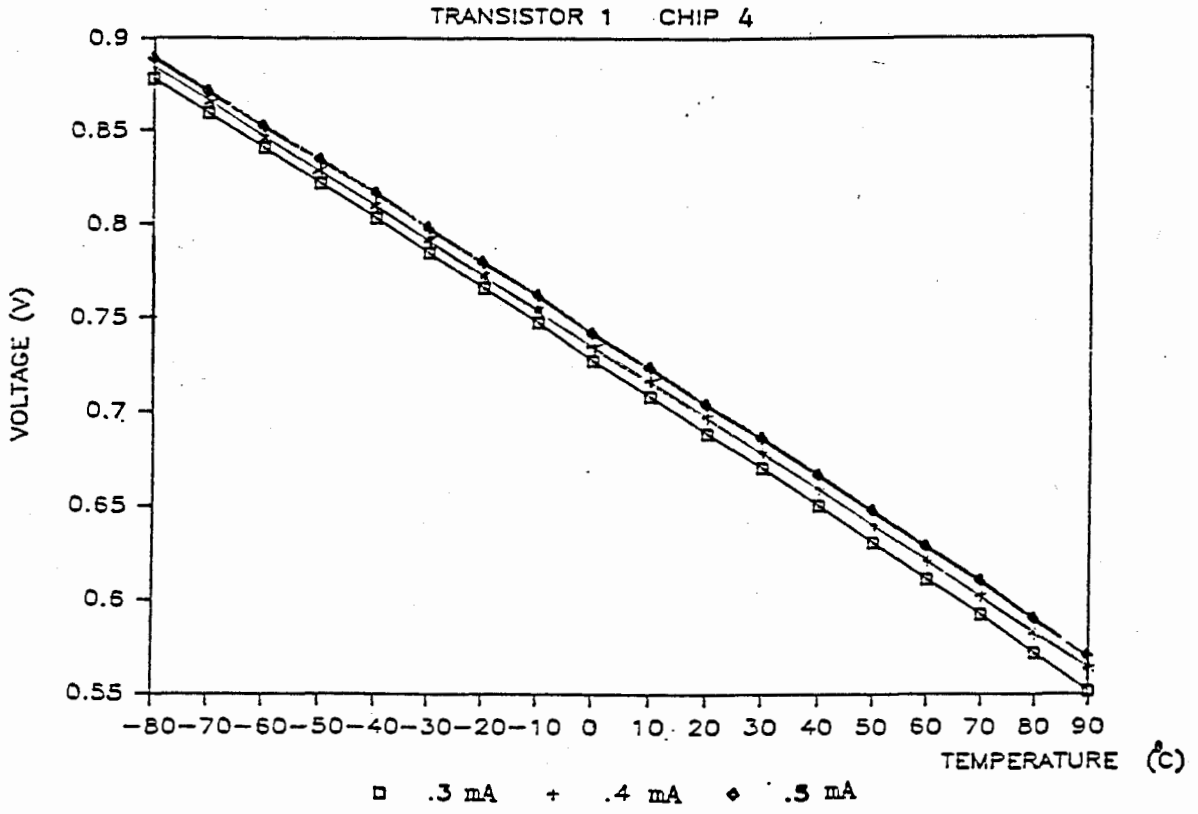

Fig. 3.8 Calibrating curves for transistor #1 on chip #4

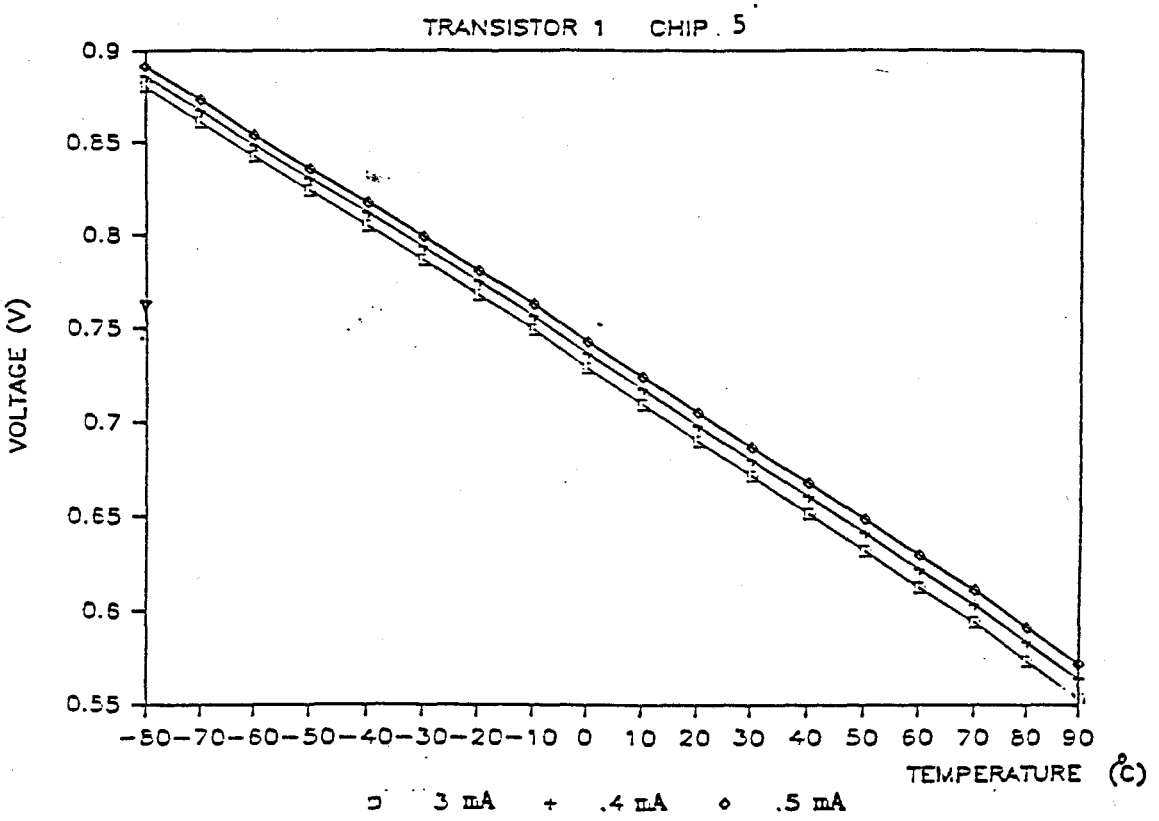

Fig. 3.9 Calibrating curves for transistor #1 on chip #5

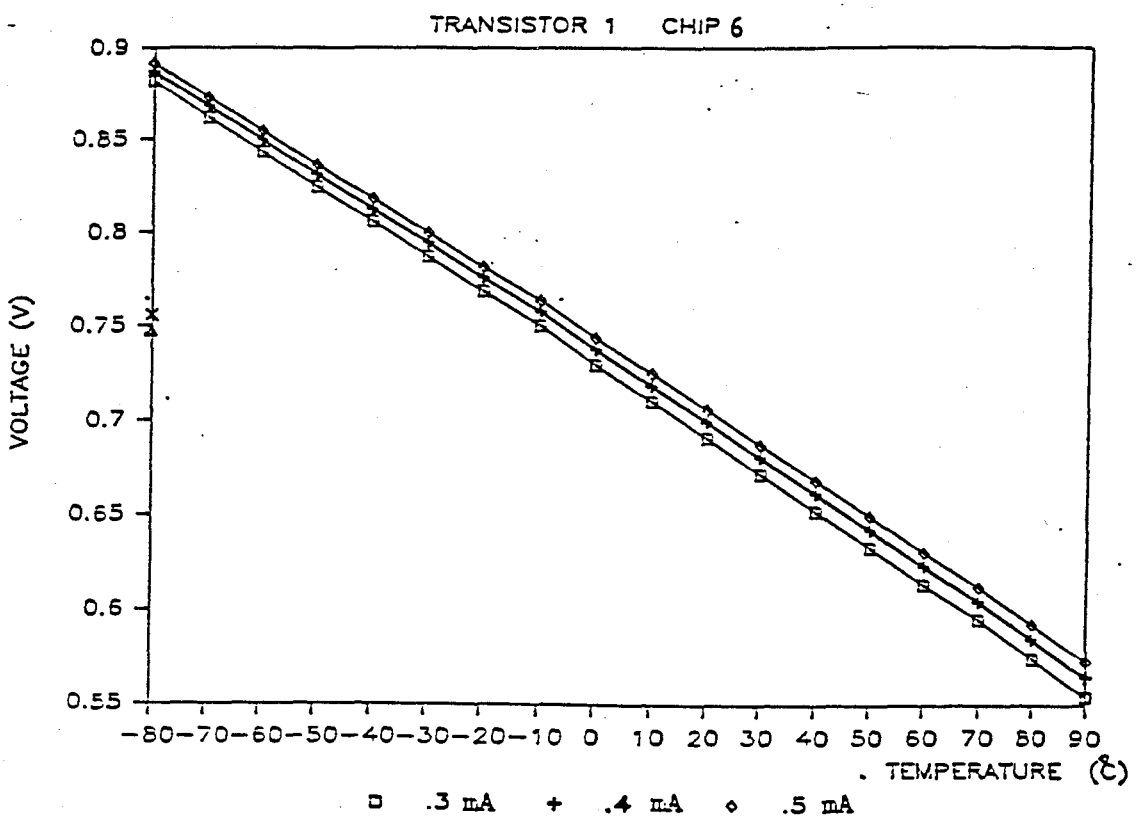

Fig. 3.10 Calibrating curves for transistor #1 on chip #6

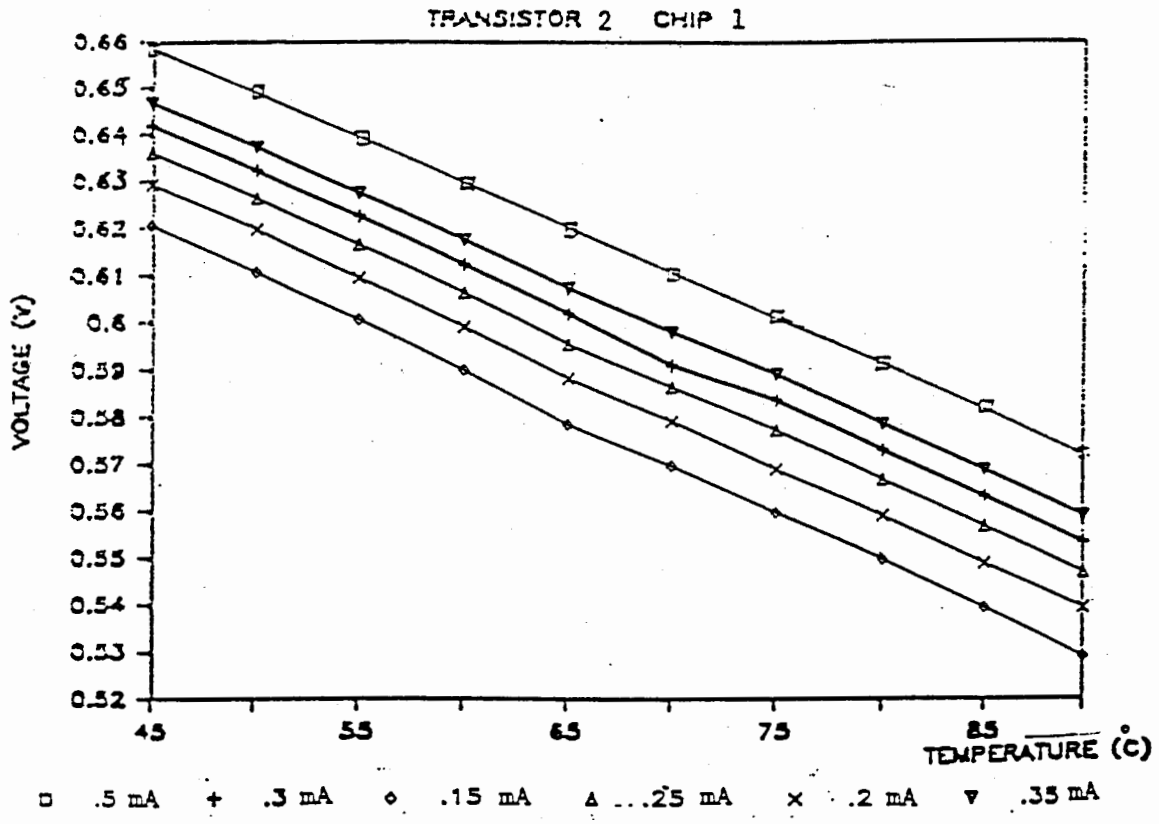

Fig. 3.11 Calibrating curves for transistor #2 on chip #1

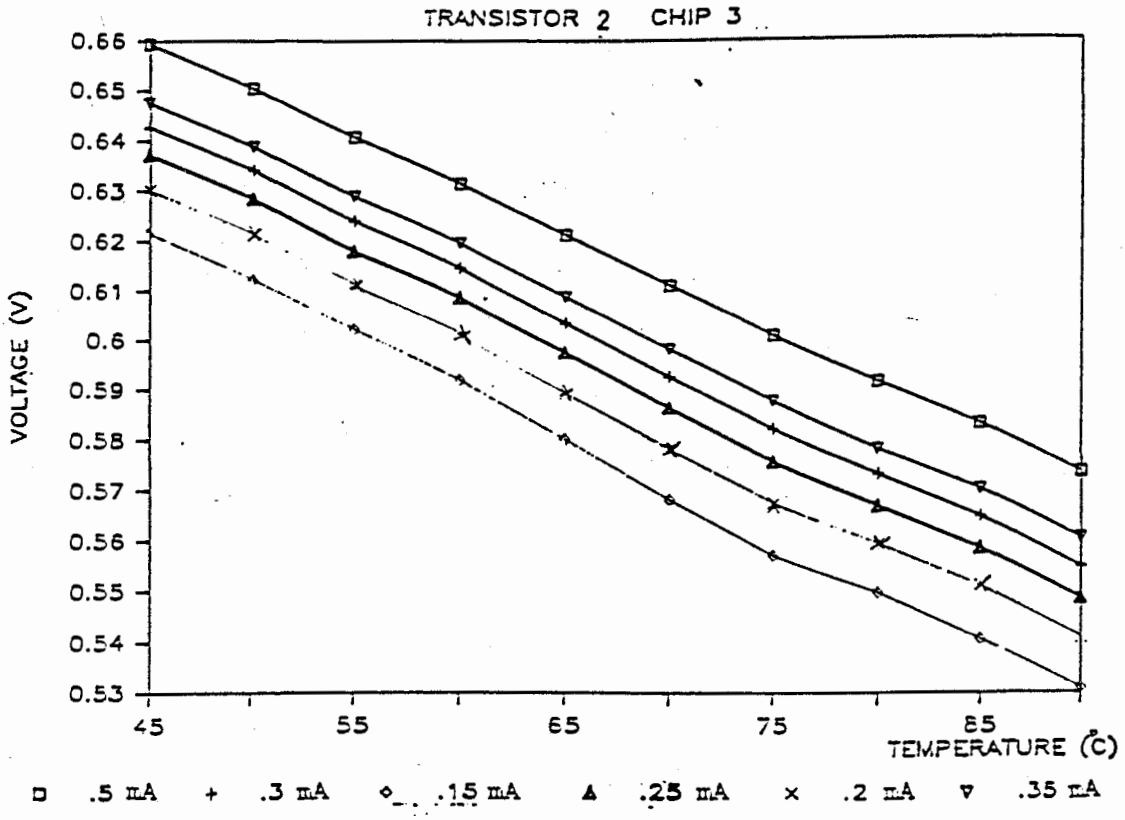

Fig. 3.12 Calibrating curves for transistor #2 on chip #3

To calculate error due to current changes through the diode we varied the current and measured the voltage drop through said diode. The result is shown in Fig.3.13. Higher junction temperatures produce higher errors. At 40°C, the calculation results show that one microampere shift of the current causes about a 0.04°C shift in temperature. To keep the accuracy of temperature measurement within 0.1°C we have to keep the current changes to less than 2 microamperes. In other words, a current source of 300 microamperes requires a current source accuracy of 0.7 per cent.

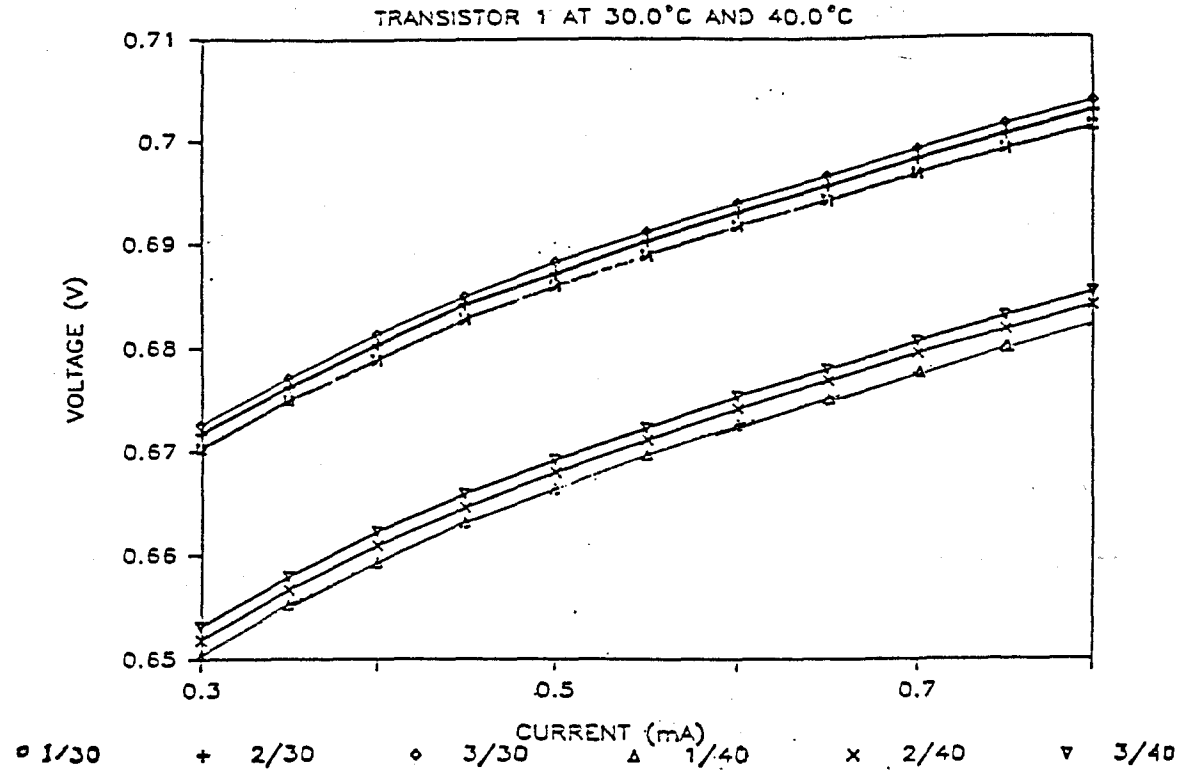

Fig. 3.13 Base-emitter voltages of on-chip transistors vs. various collector currents

(For transistor #1 on chip #1, chip#2, and chip#3; notation under the figure presents chip #/temperature)

3.2 INFRARED IMAGE METHOD

This section describes an Infrared Image System. We emphasize that the emissivity of an object plays an important role in determining the actual temperature from IR images.

3.2.1 Overview: Using IR Images for Reliability

Infrared Radiation

Infrared energy is energy that is propagated through space at the speed of light through the transfer of electromagnetic vibrations. The infrared portion of the spectrum covers the wavelengths from about 0.75×E-6 meters to about 1000×E-6 meters.

Infrared radiation is naturally emitted by all objects because of the thermal agitation of their molecules. The intensity, frequency, and wavelength of this electromagnetic energy are controlled by the temperature and size of the source and by a property known as the emissivity of the material. When the electromagnetic energy emitted by a source reaches another body, part may be reflected, part may be transmitted, and part may be absorbed and cause heating. If the total energy reaching the second object is represented by unity this relationship is:

$$t + r + a = 1$$

where t, r, and a are the object's fractional transmittance, reflectance and absorptance, respectively.

Infrared Cameras

Infrared Cameras contain a small infrared sensor which views an object through an optical system consisting of a high-speed rotating prism

or of an oscillating mirror that scans the entire field of view across the fixed sensor. The sensor's analog signal output then goes to a high-speed signal-processing system to be digitized, analyzed and displayed. In order to perform accurate, real-time temperature measurement, internal temperature reference sources must be incorporated into the scanner and viewed periodically by the detector for calibration. An infrared camera must incorporate lenses that efficiently transmit within the infrared spectrum. Materials such as germanium, silicon or zinc selenide are typically used. The relevant characteristics of the optical system, detectors and electronics will be reviewed briefly.

Optical System

The purpose of the optical system is to collect incoming radiation from the target and to concentrate it upon the detector. The major components of the optical system are those that focus target energy upon the detector. These elements may be either refractive or reflective or a combination of both. In addition to focusing components, the optical system very frequently employs one or more filters in order to limit the radiation reaching the detector to the spectral region of interest.

There are four major characteristics of all optical systems which affect the measurement being made: (1)focal ratio or f/number, (2)spectral transmission, (3)resolution and (4)field of view.

Focal ratio or f/number is the ratio of the focal length to the diameter of the telescope aperture. The lower the f/number the better the sensitivity.

Sometime the optical elements can be selected to provide just the desired pass-band. This property is referred to as the spectral

transmission characteristic of the camera.

Resolution is the capability of the optical system to form a sharp image of the target scene. The resolution of an infrared instrument is limited by the same aberrations as are visual optical systems, e.g. spherical, chromatic, coma, astigmatism, etc.

The collecting optic of an infrared camera produces an image of the scene in its focal plane. When an infrared detector is placed in the focal plane the only portion of the scene from which radiation is received is that portion which falls on the detector. The detector area, therefore, establishes the field of view of the instrument. If the scene is distant from the lens, the image will lie at the focal length of lens F and therefore, the horizontal and vertical angular field of view θ_x and θ_y will be:

$$\theta_x = \frac{X}{F} \qquad \theta_y = \frac{Y}{F}$$

where X and Y are the dimensions of the detector.

Infrared Detectors

The infrared detector converts radiation to a form that is convenient for either measurement or display. It is useful for measurement data evaluation to calculate the radiant power focused onto a detector.

We shall first assume a distant extended target of uniform radiance N (Watts/cm-ster) being viewed by a radiometer with a detector of dimension x, y and an entrance aperture of area A, as shown in figure 3.14.

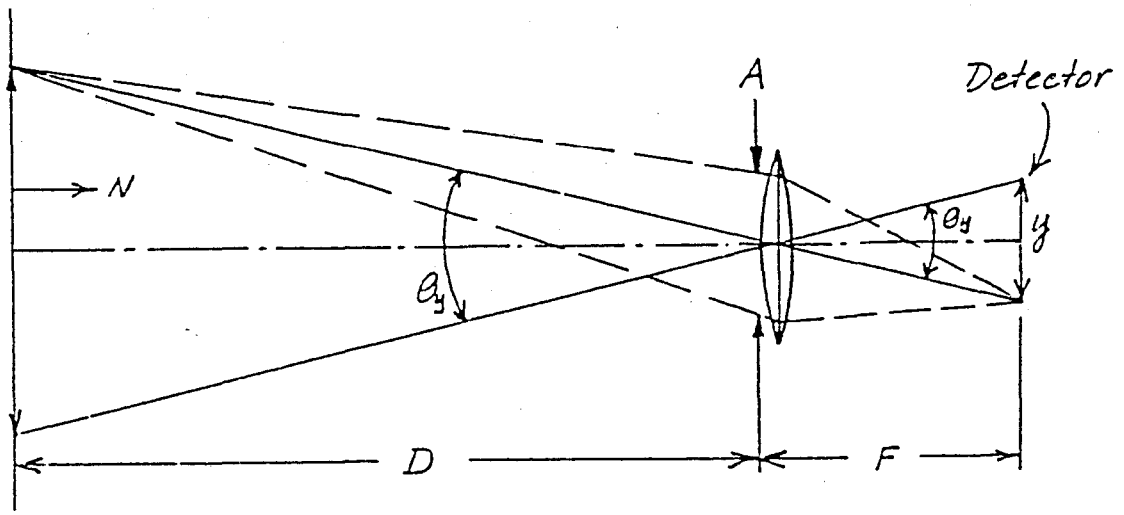

Figure 3.14 Calculation of radiation focused onto detector.

The angular field of view is

$\theta_x\theta_y = XY/F$

the spot size area at distance D is

$\theta_x\theta_y D^2$

The radiation collected by the system from unit area of the target is equal to the radiance of the target N times the solid angle subtended by the optical aperture N×A/D. The total power collected, P, will then be multiplied by the total area of target viewed or the spot size. The power

collected in the case of an extended source would be:

$$P = (N \times A/D)D^2 \times \theta x \times \theta y = N \times A \times D \times \theta x \times \theta y$$

Instead of an extended target, suppose the target were smaller than the field of view, having an area a. The energy collected would then be:

$$P = \frac{NAa}{D^2}$$

As conventional measuring methods for thermal studies of printed circuit boards involve direct contact with the material, they are both time consuming and unreliable with respect to searching for the exact location of the maximum temperature. Thus for determining the temperature measurement of the IC die, direct contact measurement is not ideal. For example, when the tester, usually a thermocouple, contacts the tested surface, it dissipates a part of the heat from the surface, and furthermore, the tested points are not necessarily the hottest spots on the surface. Consequently the infrared image method is used to obtain a visual display of the surface temperatures of integrated circuits because, compared with the use of a thermocouple, it allows measurement to be made noninvasively, quickly, and over a wider area.

3.2.2 Measurement and Results

Infrared images are constructed from measurements of the infrared radiation emitted from individual surface elements and they can be displayed in colour, recorded, or stored for subsequent analysis and data processing. A true temperature map can be displayed when proper techniques are used to compensate for the emissivity of the different materials that comprise microelectronics.

Emissivity is a measure of the ability, or ease, with which an

object, or surface, emits infrared radiation. Emissivity is the ratio of the radiant energy emitted by an object at a temperature T to the radiant energy emitted by a blackbody at the same temperature T. This may be written as

$$\epsilon = \frac{W_0}{W_{bb}}$$

where,

W_0 is equal to total radiant energy emitted by an object at a given temperature T,

W_{bb} is equal to total radiant energy emitted by a blackbody at the same temperature T.

The emissivity of a body depends, in general, on its material and surface texture. It can vary between zero (perfect reflector) and one (perfect emitter or "blackbody"). Knowledge of the emissivity of the object is crucial for correct temperature measurement by means of thermography. PCBs and ICs are, luckily, very often made of a high emissivity material. However, when looking at a die, at metal-covered components or at chips from which the cover has been removed, low and unknown emissivity may cause severe problems [65].

CHAPTER 4

IMPLEMENTATION OF THE METHODS USED TO DETERMINE TEMPERATURE DISTRIBUTION IN SEMICUSTOM IC

4.1 EXAMPLE OF APPLICATION AND LIMITATION OF TEMPERATURE MAPPING PROGRAM

As an example of the application of the temperature-distribution program and the programs interfacing with CAD tools and graphic systems, special chips have been designed and manufactured. Following is a detailed description of each step of the application of the TD program.

(1). Extract geometrical data of heat sources from physical layout

The physical layout of the test chip is shown in Fig.4.1.

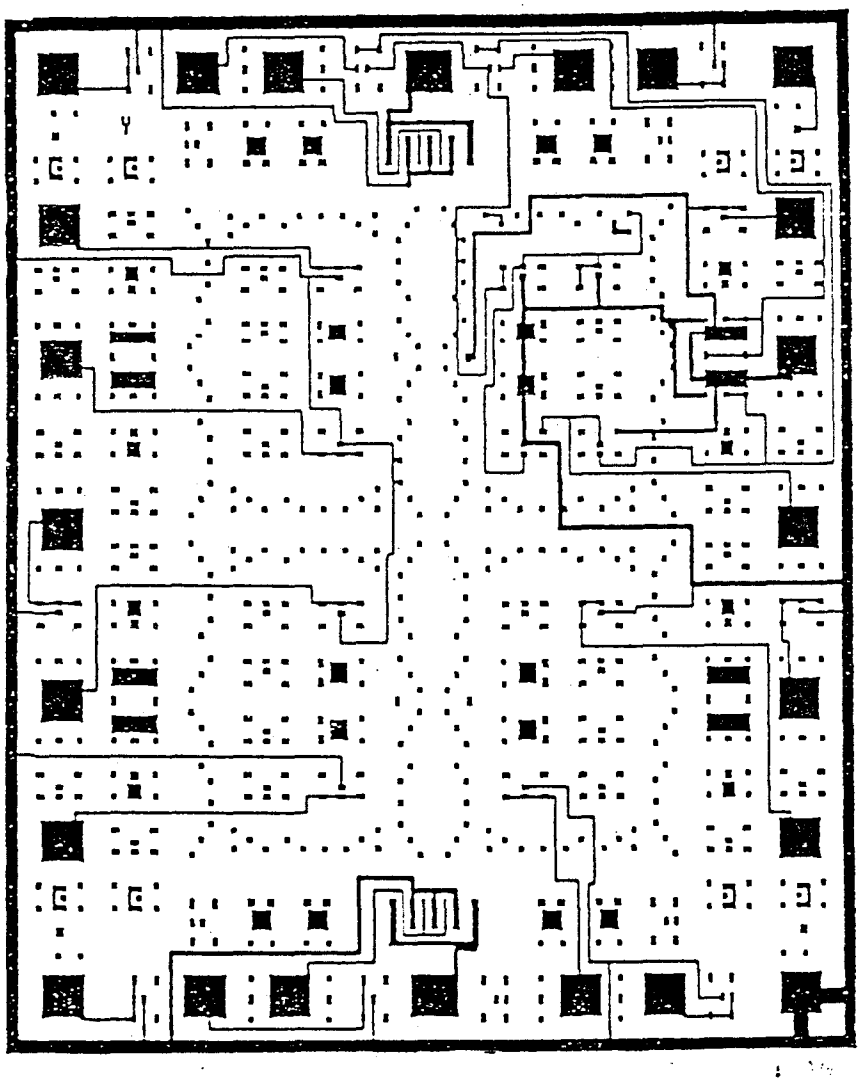

Figure 4.1 Physical layout of test chip

In the layout, boxes were drawn around the heat sources. The layout data was saved on a file named "Ther.msk"; PDIFOUT software converted the layout data to ASCII format; the P2TD program achieved the following geometrical data for the heat sources:

X ($\times 42\mu m$)	ΔX ($\times 42\mu m$)	Y ($\times 42\mu m$)	ΔY ($\times 42\mu m$)	P ($\times 5.67\times 10^{-4}$ w/μm^2)
002.5	0.2	008.0	0.2	0.180000
002.5	0.2	030.0	0.2	0.180000
002.5	0.2	045.0	0.2	0.180000
007.0	1.0	026.0	0.5	0.280000
015.0	0.2	019.0	0.2	0.180000
015.0	0.2	031.0	0.2	0.180000
026.0	0.4	005.0	0.5	0.180000
026.0	0.2	015.0	0.2	0.180000
026.0	0.2	031.0	0.2	0.180000
026.0	0.6	049.0	0.8	0.180000
035.0	0.2	014.0	0.2	0.180000
035.0	0.2	019.0	0.2	0.180000
035.0	0.5	026.0	0.6	0.180000
047.0	0.2	014.0	0.2	0.180000
047.0	0.2	019.0	0.2	0.180000
047.0	0.2	030.0	0.2	0.180000
051.0	0.2	007.0	0.2	0.180000
054.0	0.1	026.0	1.0	0.280000
054.0	0.2	008.0	0.2	0.180000
059.0	0.2	021.0	0.2	0.180000
059.0	0.2	030.0	0.2	0.180000
059.0	0.2	045.0	0.2	0.180000

This data is used as input data for the TD program.

(2). Power of heat sources

In this application, two heat sources are operated independently. The power of each heat source is controlled by an external circuit. Measuring collector current and voltage drop through emitter and collector, we recorded the power of each heat source.

(3). Modeling of chip layered structure

For the simulation of thermal distribution on a chip we used the geometry presented in Fig.2.1. The contact area between base and collector of the power transistor was measured and formed to be 1660 μm^2. So for 350mW the power density is 0.00021 $W/\mu m^2$. In this study we assumed the following parameters for the layered structure model:

Name of layer	Thickness (μm)	Conductivity ($W/\mu m^{\circ}C$)
Top layer	381	1.0512×10^{-4}
Middle layer	1143	3.9370×10^{-7}
Bottom layer	762	3.9331×10^{-4}

4. Results

The results of the TD program are presented in different forms by means of different software. Using TD2GR to convert data from table form to the format for MATLAB, we produced the 3-dimensional graphic presented in Fig.4.2

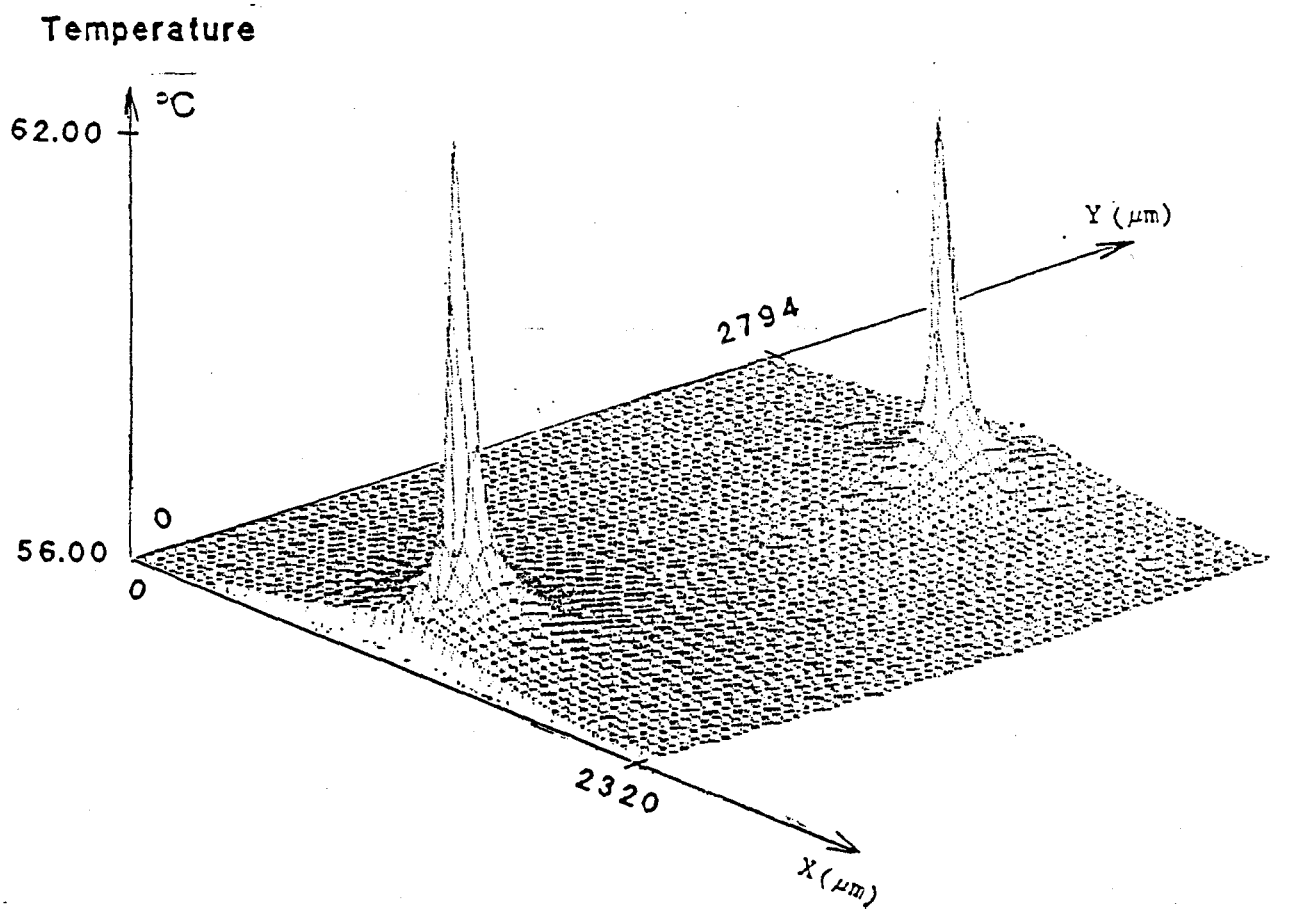

Fig.4.2 Temperature distribution of Integrated Circuit as result of TD program and CAD tools

The result of interfacing with the thermal Scanner system through the TD2MAP program was printed out in colour. The simulation thermal map is shown in Fig. 4.3. The thermal map of the same IC was obtained from the IR camera and software in the Thermal scanner and is presented in Fig.4.4 for purposes of comparison.

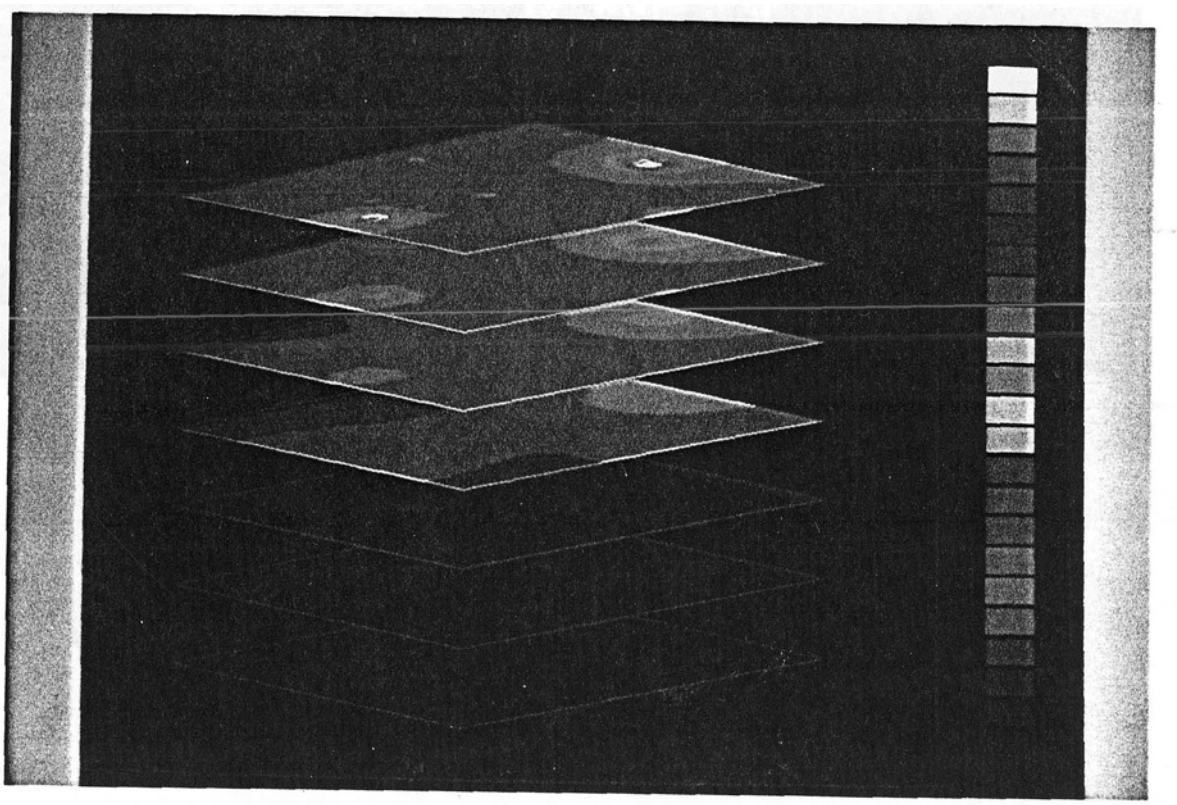

Fig.4.3 Simulation thermal map of IC

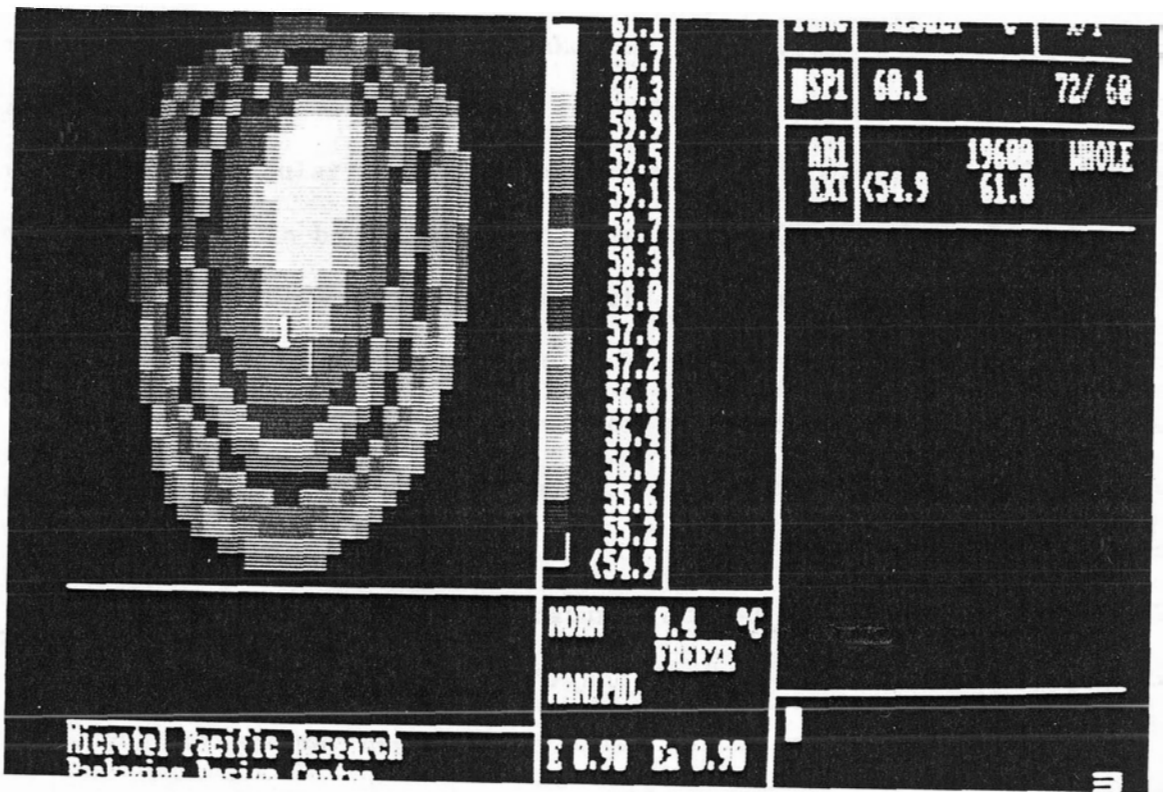

Fig. 4.4 Thermal map of IC obtained from IR camera with the heat source turned on

Following is discussion about accuracy of the results obtained from TD program: The number of Fourier series terms used influences the accuracy of calculation. From (2.17) we can derive the condition for the convergence of the sum. It was found that for large values of the argument

the power density function U(n,m) tends very slowly to zero. Also, as the arguments approach infinity the cos terms in eq.(2.17) do not tend to any limit. It is the Fourier coefficients $\tau_i(n,m,z)$ which are responsible for the convergence of the sum. Consequently, some discussion of the n and m behavior of the Fourier coefficients is necessary. It was pointed out that the Fourier coefficients are peaked at the origin of the n,m plane and approach zero as n and m become large. To make a quantitative analysis, we used a particular choice of parameters which required only the m=0 term in the sum to be retained while needing a large value of n terms in order to obtain the convergence of the sum [5]. The results of calculation are shown in figure 4.5. Curves A, B, and C show the temperature calculated at the center of the heat source to be a function of the number of terms in the sum, N, for the top of the first, second, and third layers, respectively. It is clear from curve 7a that the calculation of the surface temperature (at z=0) may require at least 350 terms in the sum while curves 7b and 7c indicate that the temperature below the surface may need only 20 terms in the sum. From the viewpoint of physics, this is a result of the fact that the number of terms needed to adequately represent a feature size of Δx (typical of the lateral size of a heat source) should be on the order of $Lx/\Delta x$ (with Lx being the lateral dimension of the structure). Deeper into the structure, the heat flow spreads out, the temperature gradient is smaller, and, therefore, fewer terms are necessary.

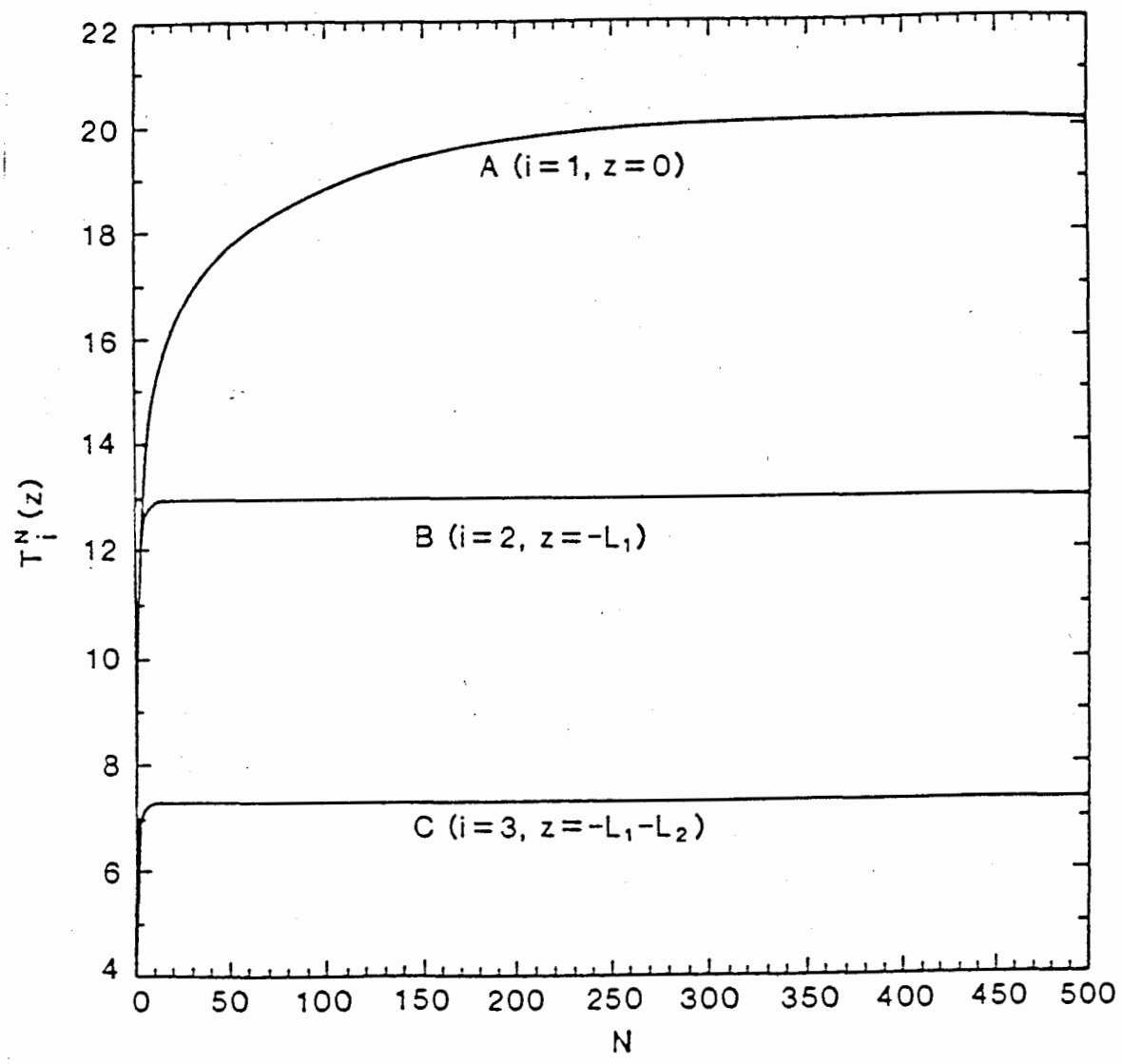

Fig.4.5 Convergence of the sum. Represented temperature as result of solving Laplace's equation by Fourier Transform. Curve A is for top layer. Curve B is for middle layer, and curve C is for bottom layer of the chip layered structure.

4.2 FINITE ELEMENT ANALYSIS (FEA)

Modeling of an Integrated circuit

The FEA model of an IC is shown in Figure 4.6. In this figure die and die attachment are each divided into 8×8×3 elements, the carrier is divided into 9×9×3 elements and the element of the carrier under the attachment itself is divided into 8×8×3 elements. This model is adequate for our case as die and attachment are opened.

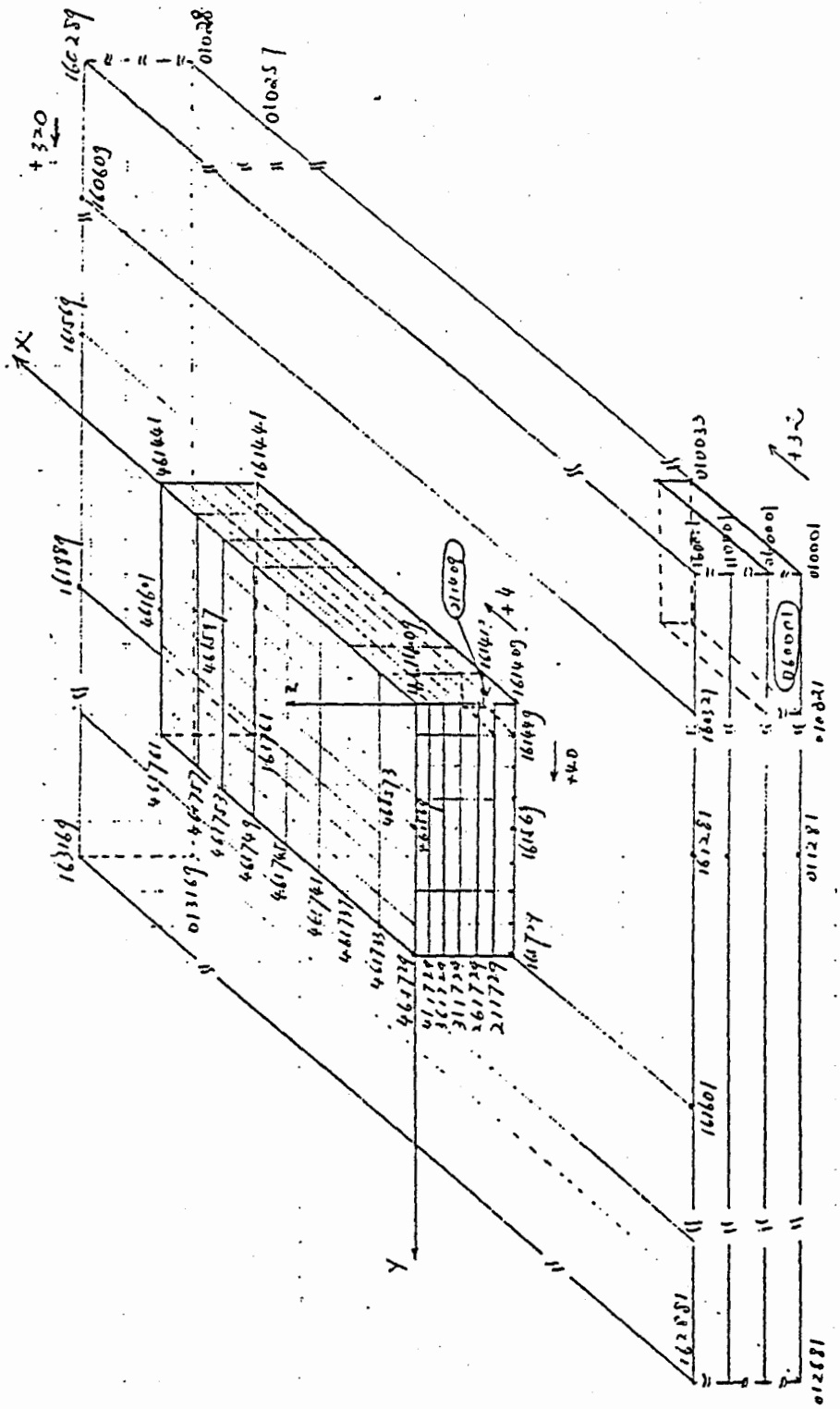

Figure 4.6 FEA model of a IC

Figure 4.6 FEA model of a IC

Setup of an input data file for FEA

We used a word editor to set up an input data file for the personal computer version of NISA - a FEA software package . The file includes element type, element connectivity, nodal coordinates, material properties, specified temperatures, power density of heat sources, and convection and radiation information.

In this study the power of each heat source is low (less than 1W) and the heat sink is thick. With that configuration heat sources are most efficiently cooled by diffusion into a thick heat sink and thus temperature is not critically dependent on convection or radiation, so we do not have to consider convection and radiation in the FEA. The input data file for NISA is in Appendix c.

Results

The result, with which this study is most concerned and which is shown in the output file after running NISA HEAT, is the temperature at each node. For this result,we have 9 thermal maps in Z direction. A thermal map for an IC surface is shown in figure 4.7.

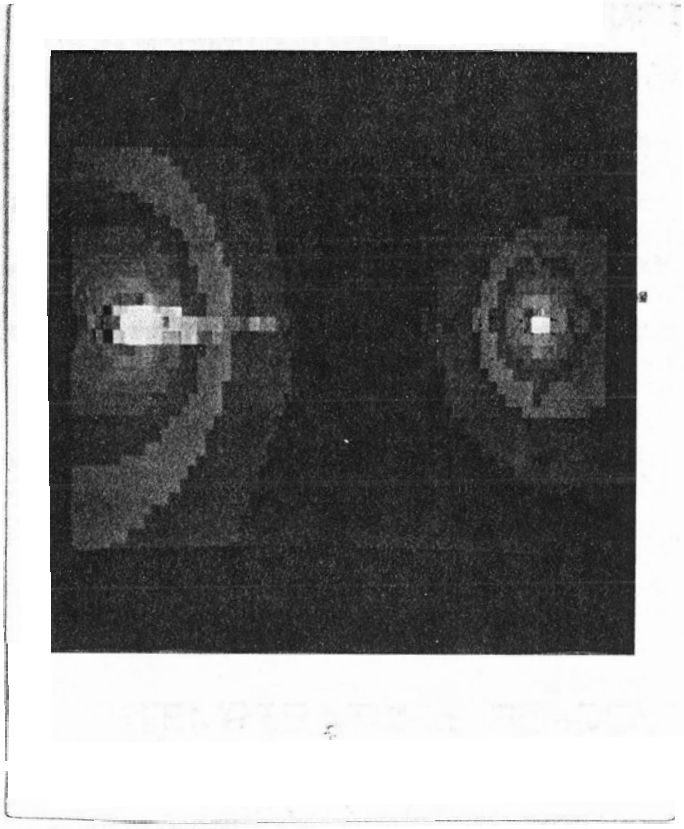

Fig. 4.7 Thermal map obtained from Finite Element Analysis

4.3 MEASUREMENT RESULT FROM ON-CHIP TEMPERATURE SENSORS

Four temperature sensors located along the X axis of each test chip were used. The power dissipated by the heat sources on each test chip was set at 450mW and 350mW respectively. The measurement results are shown in Fig.4.8. One of the six test chips was painted black and the test results compared with the results achieved by means of infrared image. In this latter case, the painted chip with known emissivity was used as a standard to find the unknown emissivity of the chip surface.

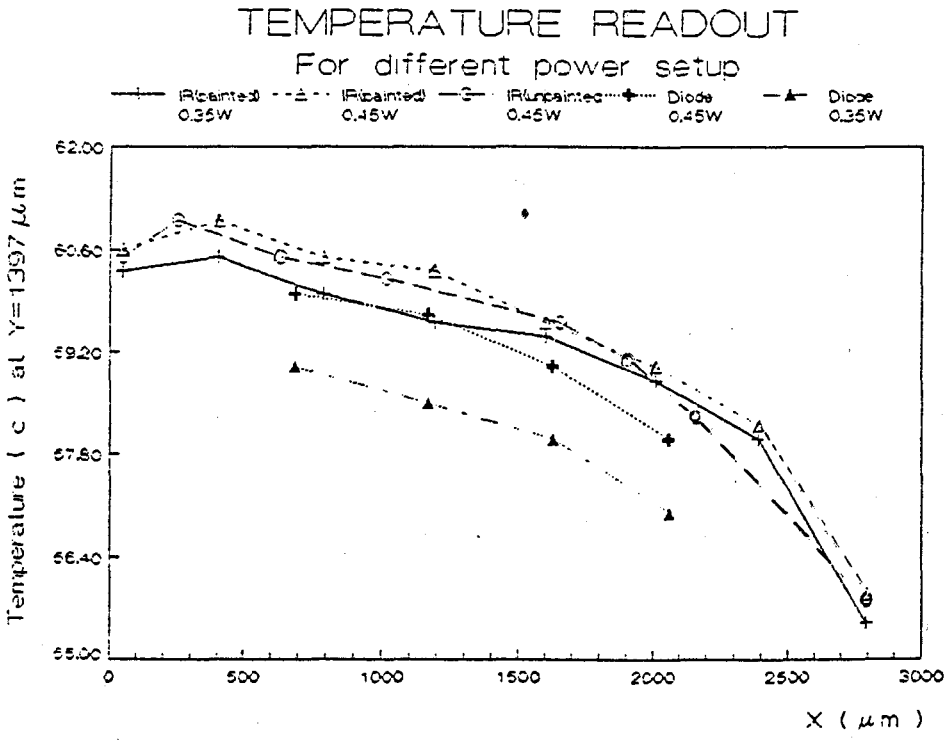

Fig 4.8 Temperature readout from on-chip-temperature sensors

4.4 INFRARED IMAGING RESULTS

In this study, we used the AGA 800 Infrared system in order to acquire thermal images of semicustom chips which we designed and manufactured ourselves. The system included an IR camera, an IBM XT, and our own personal custom software. With minor modifications of optics, this system has a spatial resolution of 20 microns and a temperature resolution of 0.1 degree Centigrade. Fabricated chips were prepared in two groups: painted black (with emissivity of 0.9 [76]) and unpainted. The goals of this experiment were to take thermal maps of microcircuits and to determine the emissivity of the die's surface. As the maximum energy that can be emitted from a body at any temperature is that of a blackbody the energy emitted by the latter uniquely determines the temperature of the former. In non-transmissive materials the fraction of incident energy absorbed by the body is equal to it emissivity, and, naturally, the percentage reflected is $(1-\epsilon)$. In other words, externally incident energy is either absorbed or reflected, and the absorptivity is equal to the emissivity. A scanning IR measuring system collects the energy from an area on the target and focuses it onto a detector using suitable optics. The energy detected is represented in terms of the radiance, or power per unit area per unit solid angle at the target. Each point, or "pixel", on the image represents a separate measurement. The radiance measured at each point represents the sum of the emitted and reflected contributions:

$$N_m = \epsilon N_t + (1-\epsilon)N_a \qquad (4.1)$$

Where:

N_m is the measured radiance;

ϵ is the emissivity;

N_t is the blackbody radiance corresponding to the unknown surface

temperature; and,

N_a is the blackbody radiance at ambient temperature.

Taking an infrared image of the painted die surface means measuring the radiance N_m at each point. We take the temperature of the room, and look up N_a in a table of blackbody radiances. Then, with ϵ known to be 0.9, we solve eq. 4.1 for N_t and find the absolute temperature in the table of blackbody radiances.

With the same power setup we take infrared images of the unpainted die surface and thus determine its N_a, N_m, and N_t. From Eq 4.1 we determine the emissivity ϵ of each observed point on the die surface.

In practice we know the emissivity of different features on die surfaces, particularly silicon and metallization. In principle we have to have emissivity and ambient temperature at each point to precisely calculate temperature from the use of infrared images according to Eq 4.1. It is simply not practical to enter the emissivity by hand for the thousands of points that make up an image. Even if one is only interested in a few points on the target, it is not always easy to find information on the emissivity of semiconductor materials, metals, alloys and coating [60]. To deal with this matter we use our computer-aided-design tools. From the IC layout database we set a look-up table of emissivities for the particular IC under design. Fig.4.8 presents our work on emissivity correction. The layout output file is in GDS-II format. The Quick-Chip format translator converts the GDS-II format into CIF. Our own software sets up an emissivity map from the layout output file in CIF. Then, the emissivity map merges with the IC IR image, indicating the actual temperature on the IC surface. Finally, the temperature distribution is presented in a color thermal map.

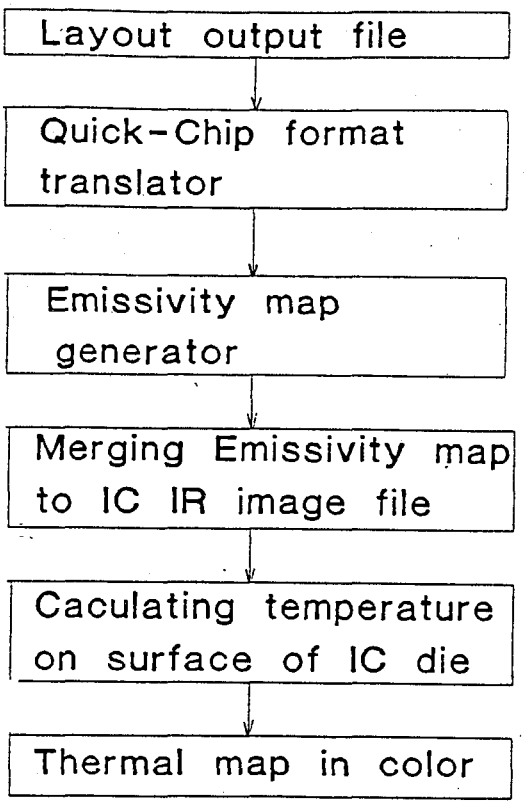

Fig.4.9 Emissivity correction for IC IR image

In the layout database we have all the geometrical information concerning the different materials on the surface of an IC die. The spatial resolution chosen depends on the feature size of IC devices and on the wire width of metallization. For the 6 μm CMOS technique we choose a space resolution of 2 μm. So for gate array IC with size of 4000μm × 4000μm we make an emissivity-look-up table corresponding to a geometrical map of 2000 × 2000 pixels. This table is used to correct emissivity at each pixel for true-temperature thermal imaging of the IC die.

Since emissivity of the IC die surface depends not only on its material but also on its surface texture, in order to improve the accuracy

of temperature measurement based on infrared image we made experimental corrections. The first measurement method, already mentioned in this section, is based on comparing, at the same power level, the image of an unpainted surface with an IC surface painted with paint of known emissivity.

The second method of emissivity measurement is based on measuring the radiance at two known temperature [68]. We heat up the die by powering the on-chip power transistor. With two measurements of radiance at constant temperatures, and with an unchanged ambient, we calculate the emissivity at each point.

$$N_{m1} = \epsilon N_{t1} + (1-\epsilon)N_a \qquad (4.2)$$

$$N_{m2} = \epsilon N_{t2} + (1-\epsilon)N_a \qquad (4.3)$$

Subtracting equation (4.4.3) from (4.4.2) and solving for ϵ:

$$\epsilon = (N_{m1} - N_{m2})/(N_{t1}-N_{t2}) \qquad (4.4)$$

According to equation (4.4) the error in emissivity measurement depends on the error in temperature measurement (N_t's) by the on-chip-temperature sensor and the error in ambient temperature measurement (N_m's). Ambient temperature can be measured with quite high accuracy compared with on-chip temperature. Thus the error of emissivity measurement in this method is mainly due to the error of temperature measurement by the on-chip-sensor. The error of on-chip-temperature measurement, as discussed in chapter 3, can be controlled within 0.1°. This assures that relative error of emissivity can be neglected.

While deriving equation (4.4) we assume that emissivity is constant at different temperatures. This is only an approximation, since emissivity depends on wavelength and therefore on temperature

$$\epsilon(T) = \frac{\int \epsilon(w)R(w)W(w,T)dw}{\int R(w)W(w,T)dw} \qquad (4.5)$$

where R(w) is the wavelength-(w)-dependent-transfer-function of the instrument, and W(w,T) is the Planck function.

For an indium-antimonide detector, the temperature dependence of emissivity for silicon-nitride passivated silicon is shown in Fig. 4.10. The resulting temperature error versus the target temperature for emissivity from figure (4.10) is shown in figure (4.11).

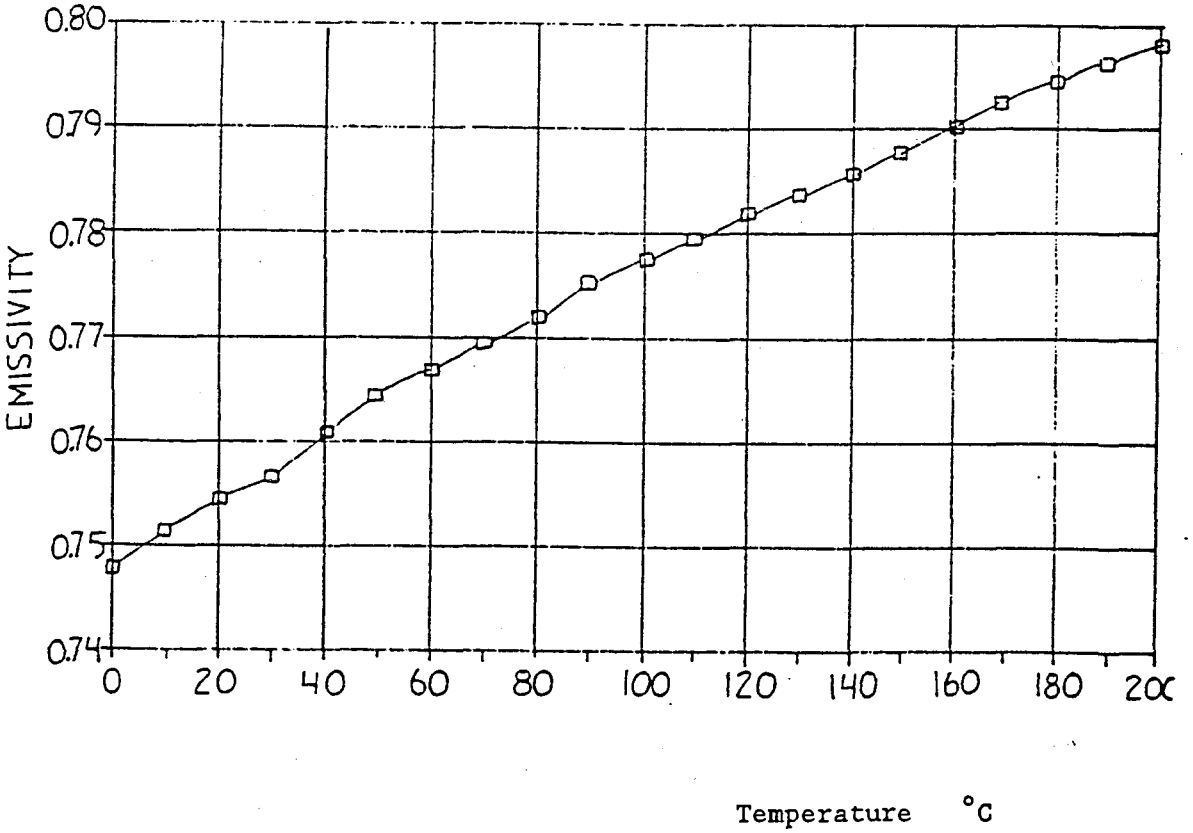

Figure 4.10 Temperature dependence of emissivity for silicon-nitride passivated silicon

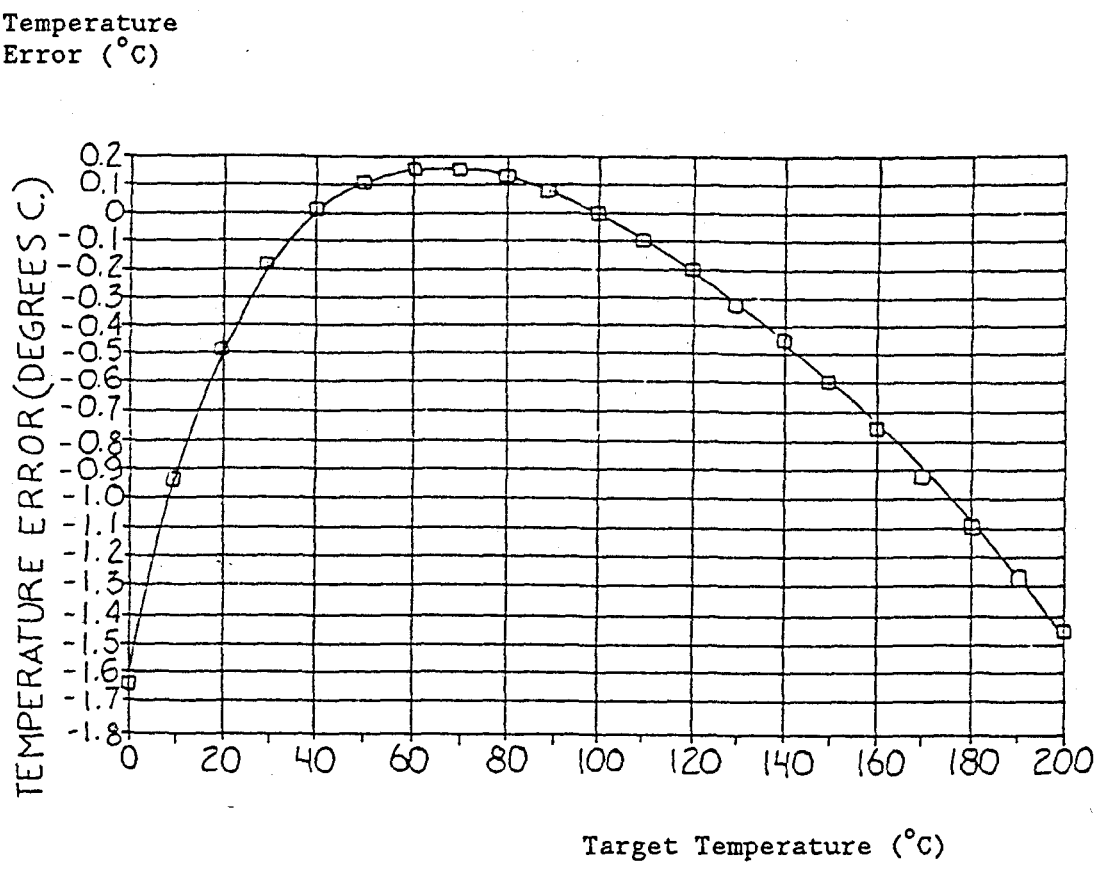

Figure 4.11 Resulting temperature error versus target temperature for emissivity from figure 4.10

CHAPTER 5
EVALUATION OF RESULTS FROM DIFFERENT METHODS USED AND FUTURE WORK

5.1. EVALUATION

This study concentrated on the analytical solution of Laplace's equation. We used Fourier transform and simplified boundary conditions in order to achieve an analytical solution to this equation, and we developed the computer program, TD, in order to evaluate this solution. The TD program is advantageous not only as a calculation tool, but as a very important element in the system, which also includes PC-CARDS, 3D graphics display, and the Thermal Scanner system. The following computer programs have been developed : S2TD which interfaces circuit simulation with TD; P2TD which interfaces IC layout tool with TD; TD2GR which interfaces TD with 3D graphics; and TD2MAP which interfaces TD with the Thermal Scanner System. The above mentioned programs work as a complete simulation tool in order to give thermal distribution information on ICs. These programs play important role in IC design when temperature is considered.

Infrared imaging and "on-chip" sensors are experimental methods which support computer simulation techniques for the study of the thermal behavior of integrated circuits.

We have fabricated twelve chips. After microscopic observation we choose six of them to package. All the sensors of the six chips were calibrated individually. We took infrared images of these six chips when the on-chip heat source was turned on. We also recorded the results from on-chip sensors for these six chips. Fig. 5.1 shows the results of

temperature read outs along an axis on the chip for all three methods when a top heat source was turned on.

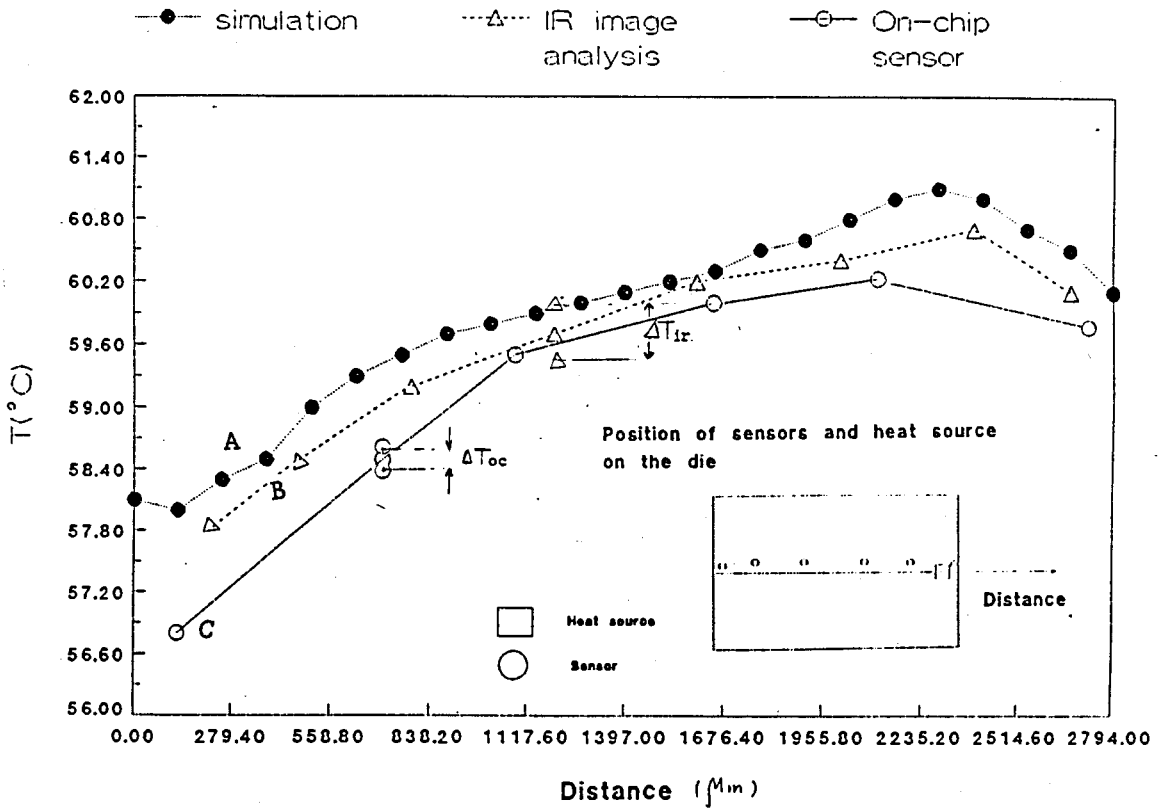

Fig 5.1 Temperature readouts along a axis on test chip

Curve a is the result of a computer simulation using Fourier transform. Curve b is the result after averaging the results received from infrared images taken from the six chips. ΔT_{ir} is an average error for this IR-imaging-temperature measurement. Curve c is also an averaging result from on-chip sensor for six chips. ΔT_{oc} is an average error for this on-chip-sensor temperature measurement.

The trends of changing temperature distribution along an arbitrarily chosen axis are almost identical for all three methods. The slight discrepancy of temperature read outs from different methods can be explained as follows.

To simplify the problem of the computer simulation of the chip thermal behavior we assumed that there is no heat outflow from the lateral boundaries of the chip and that there is no heat dissipation due to convection or radiation. This assumption is responsible for the higher theoretically calculated values of temperature than the temperature readouts obtained from the other two methods.

In the case of IR imaging application, the most important parameter necessary for absolute temperature determination of an object is its emissivity. The emissivity of a chip's surface is dependent on temperature, shape, flatness, texture, etc. For that reason the assumption of fixed emissivity for all chips is a very rough approximation. This reason also explains the error for curve b.

Whenever a hot spot on IC die is concerned infrared image analysis (direct measurement) is the fastest means of guiding IC designers toward the improvement of chip reliability.

The "on-chip" sensor is a reliable tool for determining the temperature of an IC chip. Whenever either computer simulation techniques

or infrared image analysis need to have a standard measurement for checking results, this sensor is useful. It is very difficult for an IR camera to determine absolute temperature. The results obtained from IR cameras are critically dependent on the emissivity of considered objects. For these results, "on-chip" sensors provide a standard temperature measurement and support experiments determining emissivity.

5.2. FUTURE WORK

1. Defect study, premanufacture reliability prediction

With the present speed of technological progress, the level of integration will increase from five million transistors per chip for VLSI circuits in the year 1988 to more than one hundred million transistors per chip for ultra large-scale integrated (ULSI) circuits in 1995 [66]. Several approaches may be utilized to ensure microelectronic product reliability. The conventional screening approach attempts to eliminate the infant mortality failures of fabricated parts. Such failures are highly material-and process-dependent. Substrate defects, process contamination and manufacturing equipment inaccuracy are common causes of failure. Elimination of high infant mortality ICs is an important task. Based on this study we can set up a procedure to screen out ICs with manufacturing defects . When the computer simulation techniques and the related experimental tools are mature, IC defect study based on the methods discussed in this paper becomes possible. The simulated thermal map from computer simulation techniques is supposedly a "healthy" thermal image. The experimental thermal map obtained by means of either IR camera or "on-chip" sensors should be the real thermal image of the IC studied. If

defects, such as mechanical, electronic, or dielectric breakdown exist, we will find a discrepancy between the two kinds of thermal maps. When the resolution of the thermal maps is high enough, we can locate the defect through the discrepancies. Thermal imaging is also particularly useful in comparing current production results with past performance. The ability to monitor the thermal performance characteristics of a production batch and compare them to the characteristics of a previous batch allows the production department to pinpoint variances within the manufacturing process itself. There are of course many factors that lead up to variations in dies from batch to batch. Thermal imaging is a rapid method of determining what differentiations truly exist.

Premanufacture reliability prediction

Normally, when failure rate information is desired, a number of devices, often as many as 1,000, are subjected to accelerated stress consisting of elevated temperature or a combination of elevated temperature and applied voltage. Failures are recorded as a function of time at different temperatures and an activation energy is determined which allows results to be extrapolated to rated stress level. The procedure is generally long and costly. Trend-analysis which may simulate years of operation in minutes of computer time, is being developed [14][66].

Key failure mechanisms in VLSI products are related to: hot-carrier damage, electromigration, radiation effects, electrostatic discharge, and time-dependent dielectric breakdown (TDDB) [66]. Recently, software modules to handle hot-carrier effects [66] and electromigration effects [14] have been developed. Software that can simulate all mentioned

failure mechanisms may be expected in the near future. As mentioned earlier in this study, the above-mentioned failure mechanisms are strongly temperature-dependent. Thus methods to determine temperature distribution on IC dies will play an important role in designing computerized simulation programs which allow designs to be checked for reliability prior to fabrication.

2. Self controlled chips

The temperature-measurement methods used in this study are reliable for on-chip diode and infrared image, if they are well-calibrated and suitable for use on IC die. There are many factors which produce overheating in operating ICs. Four cases that frequently occur are: (1). Some components on IC are faulty. (2). Some components need more current due to ageing. (3). Circuits that are connected to the IC require more current than usual. (4) Heat dissipation from the IC die is not adequate.

For certain ICs each of the aforementioned cases produces overheating at specific positions on the chip. It is possible to place temperature-sensitive diodes on different places on the chip and to build a circuit that will monitor temperatures through the sensors and will "think" about possible solutions to overheating, e.g. switch to redundancy circuit, shut off power, increase power voltage etc.

Some specially-designed IC dies require uniform thermal distribution on their surfaces. These chips consist of a matrix of polysilicon resistors distributed across the die [48]. Due to the changing of the material and/or components of the die such a distribution does not guarantee a constant uniform temperature. A suggested approach to obtaining uniform heat distribution is to place a matrix of heat sources

and temperature-sensitive diodes on the die. The power dissipation of each heat source should be adjustable so that if a non-uniform temperature distribution is detected by the sensors, the sensors can tell the control circuits to adjust the power dissipation of the heat source. Borrowing the name of auto-gain-control (AGC) we name this kind of circuit auto-temperature-control (ATC) .

3. Die attachment and package study

Since we have determined that junction temperature is important to the quality and reliability of a semiconductor device, in order to assure that the device operates within its thermal design limit its package and die attachment must be carefully analyzed and verified. A die attachment has three principal purposes: (1) physical restraint of the die, (2) heat transfer and (3) electrical connection (many power transistors). Virtually all of the heat generated at the junction is conducted to the outside of the package through the die bond or die attachment. Techniques commonly used for the production monitoring of die attachment evaluation include X-ray, die shear, scanning laser acoustic microscope (SLAM) and thermal impedance testing[66].

X-ray can be a relatively inexpensive way to evaluate die attachment; however, its drawbacks include the difficulty of interpretation and its secondary importance with respect to determining the thermal impedance of the bond. Die shear is the oldest method, however, because it calls for shearing the die from the header in order to examine the bond, it is both destructive and interpretive. SLAM assumes that heat and sound propagate in a similar manner and, although non-destructive, it is difficult to interpret.

Each method has its strengths with respect to specific applications but none is as effective in production as is thermal die attachment evaluation. We can use a combination of the theoretical and experimental methods mentioned in this study in order to carry out this procedure. For an integrated circuit, the die is heated up sufficiently to determine whether the thermal energy is being dissipated through the die bond at the proper rate. Using the computer program TD and finite element analysis we simulate different material and thicknesses of die attachment in order to evaluate its thermal characteristics. On-chip sensor and infrared image are good experimental methods for carrying out the thermal transient evaluation of die attachment.

Based on our research, I suggest using thermal pulse [37][38] as a research method for studying die attachments and packaging. This technique relies on the use of a short-duration heat pulse to produce an initial thermal gradient in a sample. Physical parameters such as thermal diffusivity, heat capacity, and thermal conductivity can be obtained by analyzing the shape of the temperature-time curve. As actual power-dissipating elements heat up in a matter of microseconds [48] we can use on-circuit-power-dissipating elements as heat pulse sources.

We can also use heat pulse sources to make on-chip cycling stresses in order to investigate the degradation of integrated circuits. Sometimes on-chip temperature sensors or heat pulse sources can be found in commercial ICs. For example, an on-chip sensor can be the input protection diode of an unused input on a real die (provided both anode and cathode are externally available), or it can be an imbedded diode on a specially-designed thermal die [48].

CONCLUSION

Three independent methods of determining temperature distribution on silicon chips has been presented. The results of temperature distribution obtained from these methods show good agreement. Infrared image analysis (direct measurement) should be the fastest means in guiding IC designers to the improvement of the reliability of chips. "On-chip" sensors should be used for the calibration of IR camera or for the continuous monitoring of the temperature of chips working in systems with high reliability requirements. The results obtained from any of these experimental methods may lead to more refined and accurate computer simulation techniques for studies of the thermal behavior of integrated circuits.

Taking advantage of interfacing with CAD tools, an emissivity map was made in order to make emissivity corrections for the IR image measurement. Therefore, the IR image of an IC can be used to find defects in the IC or to detect abnormal working conditions. Interfacing with CAD tools also allows fully automatic simulation. All parameters needed to run a program based on solving Poisson's equation are taken from the output files of CAD software. This makes simulation a good tool for IC designers concerned with analyzing the thermal characteristics of IC design and also provides early inputs with regard to effective lifetime prediction. Figure 5.2 describes the procedure for obtaining thermal maps and the interconnection between them. This figure also presents our efforts to add reliability parameters into IC design.

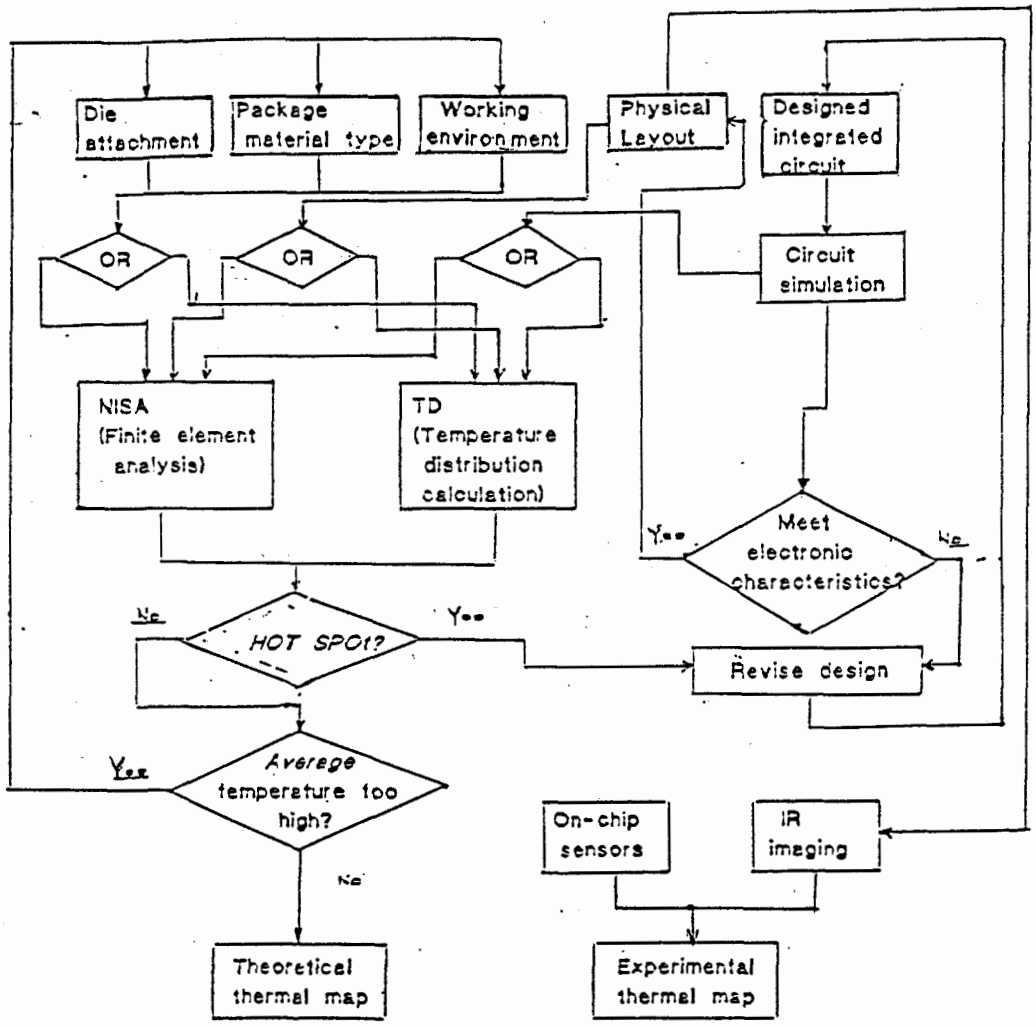

Fig. 5.2 Procedure for obtaining thermal maps and relationship between thermal maps and CAD

REFERENCES

[1] Zi Wei Xie, Andrew H. Rawicz "Methods for determining the temperature distribution at IC chip level ," IASTED , Los Angeles, December 12-14, 1988

[2] Andrew H. Rawicz "Thermal reliability System," final report to B.C. Science council, 1989

[3] Donald Q. Kern, Allan D. Kraus "Extended Surface Heat Transfer," 1972 by McGraw-Hill, Inc.

[4] Allan D. Kraus, "Extended Surface Thermal Systems," 1982 by Hemisphere Publishing Corporation.

[5] John Albers "TXYZ: A Program for Semiconductor IC Thermal Analysis," National Bureau of Standards, Washington, D.C. 20234

[6] Ericsson, "Thermal Studies of Printed Circuit Boards and IC Capsules" Application Report, AGEMA Infrared Systems Ltd. Jul. 19, 1985

[7] James M. Kallis, Landon A. Stranttan, and Thomas T. Bui, Hughes Aircraft Co."Programs Help Spot Hot Spots," IEEE Spectrum, March 1987, pp.36-41

[8] Kiyoshi Miyake, Hideto Suzuki, Shoichi Yamamoto, "Heat Transfer and Thermal Stress Analysis of Plastic-Encapsulated ICs," IEEE Transactions on Reliability, vol R-34, No.5, 1985, pp.402-409

[9] Herb Boulton, "Design Verification, Failure Analysis and Production Testing of Hybrids Using High-Sensitivity Thermography Systems," Uti Instruments Company, pp.85-89

[10] K. J. Russell and J.K. Dhiman, "Power GaAs FET RF Life Test Using Temperature-Compensated Electrical Stressing," IEEE/IRPS, 1986 pp.150-156

[11] T.R. Conrad, R.J. Mielnik, L.S. Musolino, "A Test Methodology To Monitor and Predict Early Life Reliability Failure Mechanisms," IEEE/IRPS, 1988, pp.126-130

[12] Xiaoguang Sun and Dwight L. Jaggard, "The Inverse Blackbody Radiation Problem: A Regularization Solution," J. Appl. Phys. 62(11), 1 December 1987, pp.4382-4386

[13] David F. Frost, Kelvin F. Poole, "A Method for Predicting VLSI-Device Reliability Using Series Models for Failure Mechanisms," IEEE Transactions on Reliability, Vol, R-36, No.2, Jun. 1987, pp.234-242

[14] J.W. Lathrop, M.A. Bridgwood, D.J. Dumin, J.W. Harrison, Jr. K.F. Poole, "VLSI Reliability Research," Fourth Annual Report, July 1988, Clemson University, pp.1-78

[15] T.M. Berlicki, E.L.Prociow, "Power-Temperature Dependence of Elements in Hybrid Circuits," Microelectronics Journal Vol 17 No 1 1986, pp.25-33

[16] Michael Pecht and B.T. Sawyer, "PCB design for Thermal Reliability,"

Printed Circuit Design, May 1987, pp.12-18

[17] J.M. Pimbley and D.M. Brown, "Current Crowding in High-Density VLSI Metallization Structures," IEEE Transactions on Electron Devices, Vol. ED-33, No.9, September 1986, pp.1399-1401

[18] John G.J. Chern, William G. Oldham, Nathan Cheung, "Electromigration in AL/Si Contacts-Induced Open Circuit Failure," IEEE Transactions on Electron Devices, Vol. ED-33, No.9, September 1986, pp.1256-1262

[19] H.R. Stirn, "Failure Analysis of Multilayer Printed Circuit Boards Using Thermography," pp.204-208,

[20] Brenda M. Clark, "Keeping an Eye on Hot Spots," December 1985 Circuits Manufacturing, pp.21-24

[21] Florin and Scherler AG, Kriens, "Thermographic Studies of Electronic Components," 1983, Agatronics Limited

[22] Steven S. Tung, "Combinatorial Analysis in Determining Reliability," 1982 Proceedings Annual Reliability and Maintainability Symposium, pp.262-266

[23] George S. Baird, "Economics of Thermographic Predictive Maintenance Inspections," SPIE Vol. 520 Thermosense VII 1984 pp.193-196

[24] P. Gregory, "Thermal Characteristics of a Hybrid Microcircuit," Microelectronics Journal Vol. 13 No.5 1982, pp.12-15

[25] Steven Groothuis, Walter Schroen, and Masood Murtuza, "Computer Aided

Stress Modeling for Optimizing Plastic Package Reliability," 1985 IEEE/IRPS, pp.184-191

[26] "Thermographie IR : Pour les Cartes E'lectroniques, Si...," Mesures-4 mars 1985, pp.51-54

[27] N. Khurana, T. Maloney, W.Yeh, "ESD on CHMOS Devices - Equivalent Circuits, Physical Models and Failure Mechanisms," 1985 IEEE/IRPS pp.212-222

[28] E.A. Weis, et al, "Investigating Reliability Attributes of Silicon Photodetectors," Microelectron. Reliab. Vol.26. No.6 1986, pp.1099-1110

[29] W.D. Brown, "Temperature Effects in The NOMOS Transistor," Microelectron. Reliab. Vol.26, No.6 1986, pp.1163-1172

[30] Torky I. Sultan, "Optimum Burn-in Time: Model and Application," Microelectron. Reliab. Vol 26, No.5 1986, pp.909-916

[31] Herbert Kaplan, "Marketplace Update: Commercial Infrared Imaging Systems," Photonics July 1987, pp.99-100

[32] IL Hyun Choi and Kensall D. Wise, "A Silicon-Thermopile-Based Infrared Sensing Array for Use in Automated Manufacturing," IEEE Transactions on Electron Devices, Vol. ED-33, No.1, January 1986, pp.72-79

[33] Eric Y. Chang and Andreas Acrivos, "Conduction of Heat from A Planar

Wall with Uniform Surface Temperature to a Monodispersed Suspension of Spheres," J. Appl. Phys. 62(3), 1 August 1987, pp.771-776

[34] Costas P. Grigoropoulos and Richard H. Buckholz, "Stability of Phase Boundaries on Thin Silicon Layers with Glass Substrates," J. Appl. Phys. 62(2), 15 July 1987, pp.474-480

[35] John M. Halley and John E. Midwinter, "Thermal Analysis of Optical Elements and Arrays on Thick Substrates with Convection Cooling," J. Appl. Phys. 62(10),15 November 1987, pp.4055-4064

[36] K. R. Grice, L.J. Inglehart, L.D. Favro, P.K. Kuo, and R.L. Thomas, "Thermal Wave Imaging of Closed Cracks in Opaque solids," J. Appl. Phys. 54(11), November 1983, pp.6245-6255

[37] W.P. Leung and A.C. Tam, "Techniques of Flash Radiometry," J. Appl. Phys. 56(1), 1 July 1984, pp.153-161

[38] Michel Egee, Robert Dartois, Jean Marx, and Christian Bissieux, "Analysis of Semitransparent Layered Materials by Modulated Photothermal Radiometry: Application to the Bonding and Thickness Control of Enamel Coatings," Can. J. Phys. 64, 1297 (1986), pp.1297-1302

[39] R.M. Sandfort, E.J. Charlson, "Calibration Curves for Gold-Nickel and Silvernickel Thin film Thermocouple," Solid-State Electronics Pergamon 1968 Vol.11, pp.635-637

[40] P. Cielo, R. Lewak, D.L Balageas, "Thermal Sensing for Industrial

Quality Control," SPIE Thermosense VIII Symposium, Cambridge, MA-Sept.15-20, 1985

[41] Chen Cheng Yu and Alexander J. Swinton, "Precision Temperature Profiling in Highly Accelerated VLSI Life Test," 1982 IEEE/PROC. IRPS, pp.140-143

[42] Nicholas M. Baran "Finite Element Analysis on Microcomputers,"1988 by R.R Donnelly & Sons Company

[43] Sedat Sirbegovic, Milan Mazalica and Ratko Krcmar, " Temperature Verification of Hybrid Microelectronic Circuit Design," Electrocomponent Science and Technology, 1983, Vol.10, pp.63-66

[44] A. Tsdaka, "A Resistor Matrix Simulating a Dynamic Infrared Target," App. Opt. 22, 1983, pp.187-194

[45] D.S.Peck & O.D.Trapp "Accelerated Testing Handbook,"1987 by Technology Associates

[46] "Handbook of Infrared Radiation Measurement," 1983 by Barnes Engineering Company, Stamford, Connecticut

[47] Mohamed Munaf Alli, Mali Mahalingam, "Thermal Characteristics of Plastic Small Outline Transistor (SOT) Packages," IEEE Trans. on Components, Hybrids, and Manufacturing Technology,Vol. CHMT-9, No.4, December 1986, pp. 353-363

[48] M. Aghazadeh, M. Kirschner, "Transient Thermal Characteristics of

VLSI Device - Evaluation and Application," 1986 International Test Conference, pp.428-434

[49] Birger Schneider, Gert Jorgensen, and Moogens Bo Christensen, "The Effects of Bacdrive Stressing Fast IC Technologies," 1986 International Test Conference, pp.452-464

[50] Charles F. Hawkins, Jerry M. Soden, "Reliability and Electrical Properties of Gate Oxide Shorts in CMOS ICs,"1986 International Test Conference, pp.443-451

[51] P. Cielo, "In Situ Laser Thermal Analysis of Bulk Materials," Journal of Thermal Analysis, Vol.30(1985), pp.3-42

[52] Richard W.Sherman, "Thermal Imaging,"Photonics Spectra July 1983, pp.57-60

[53] Jeanne s. Pavio, "Successful Alloy Attachment of GaAs MMIC's," IEEE Transactions on Electron Devices, Vol. ED-34, no. 12 December 1987, pp.2616-2620

[54] S.Holland, I.C. Chen, T.P. MA, and C. Hu, "On Physical Models for Gate Oxide Breakdown," IEEE Electron Device Letters, Vol. EDL-5, NO.8, August 1984, pp.302-305

[55] KiKuo Yamabe and Kenji Taniguchi, "Time-Dependent Dielectric Breakdown of Thin Thermally Grown SiO2 Films," IEEE Transactions on Electron Devices Vol. ED-32, NO. 2, February 1985, pp.423-427

[56] L. Richard Carley and Wojciech Maly, "A Circuit Breaker for Redundant IC Systems," Department of Electrical and Computer Engineering Carnegie Mellon University

[57] R. Radojcic, "Generic Qualification of Semi-Custom IC Product Families," Microelectron. Relia. Nov. 1985, pp.471-479

[58] Charles G.Masi, "Thermal Imaging in Electronics," Test & Measurement World, January, 1987

[59] Mark Basler, "Hybrid Thermal Analysis: a design tool," Hybrid Circuit Technology, September 1987, pp.79-84

[60] Jay W. Shepherd, "A discussion of emissivity correction and its application in infrared microimaging," An International Conference on Thermal Infrared Sensing for Diagnostics and Control, 18-20 May 1987 Orlando, Florida, pp.130-137

[61] Robert B. Mclntosh, "Justification for infrared microimaging in the design, manufacture, test, and screening of semiconductor microcircuits," An International Conference on Thermal Infrared Sensing for Diagnostics and Control, 18-20 May 1987 Orland. Florida, pp.148-152

[62] Achilles G. Kokkas, "Thermal Analysis of Multiple-Layer Structures," IEEE Trans. Electron Devices, vol.ED-21, November 1974, pp.674-681

[63] Frank F. Oettinger, "Thermal Evaluation of VLSI Packages Using Test Chips - A Critical Review," Solid State Technology/February 1984,

pp.169-178

[64] R. Frey and M. Kane, "Temperature Effects Examined for Microwave Power-Transistor Performance and Thermal-Design Considerations," Microwave Systems News, november 1985, pp.9-12

[65] Gordon, "The PCB Thermal Analysis Problem," Printed Circuit Design, October 1987, pp.27-30

[66] Binh J. Sheu, Wen-Jay Hsu, Vance C. Tyree, "Computer-Aided VLSI Circuit Reliability Assurance," pp. 77-81

[67] William A. Ribble, "Thermal transient testing out of the lab and into production production," Evaluation Engineering, November 1987, pp.150-151

[68] Robert W. Astheimer, "Determination of safe backdriving power for PC testing by infrared imaging," Presented at Semi-Therm I, Phoenix, Arizona, December 10-12, 1984, pp.1-22

[69] Albert M. Leung, "Quick Chip - a one-day turnaround IC fabrication resource," Final report submitted to the Science Council of British Columbia(Grant #70, RC-14).

[70] Y. Leblebici, S. M. Kang, C. T. Sah, T. Nishida, IEEE proceedings of International Conference on Computer-Aided Design, Santa Clara, CA, Nov. 1987, pp.252-255.

[71] David W. Jacobson, "Importance of accurate thermal analyses," 1989

Proceeding annual reliability and maintainability symposium, pp.465-469

[72] Richard Goering, "Mechanical CAD tools take on electronic packaging," Computer design, February 15, 1988, pp.26-28

[73] Paul R. Gray, "A 15-W monolithic power operational amplifier," IEEE J. Solid-State Circuits, vol. SC-7, Dec. 1972. pp.474-480

[74] A. Paul Brokaw, Michael P. Timko, "An improved monolithic instrumentation amplifier," IEEE J. Solid-State Circuits, vol. SC-10, Dec. 1975, pp417-423

[75] James E. Solomon, "The monolithic Op amp: A tutorial study," IEEE J. Solid-State Circuits, vol. SC-9, Dec. 1974, pp.314-332

[76] Robert C.Weast, "CRC Handbook of Chemistry and Physics," 68Th Edition, 1987-1988, CRC Press, Inc.

[77] D. P. Holcomb and J. C. North, "An Infant Mortality and Long-Term Failure Rate Model for Electronic Equipment," At&T Technical Journal, vol.64, No.1, January 1985, pp.15-31

[78] Douglas D. Burleigh, "Bibliography of the Application of Infrared Thermography to Electronic and Microelectronic Circuits," Spie vol.934 Thermosense Oct. 1988, pp.97-100

[79] V. Kadambi and N. Abuaf, "Numerical Thermal Analysis of Power Chip Packages," The 23rd. National Heat Transfer Conference, Denver,

Colorado, August 1985, pp.77-84

[80] Pang Ho, Tom Andrade, and Ed Johnson, "GaAs MMIC Reliability Analysis and its Impact on Microwave Systems," MSN & CT August 1987, pp.96-101

[81] A.D.Gosman, B.E.Launder,G.J.Reece "Computer-Aided Engineering, Heat Transfer and Fluid Flow," 1985 by Ellis Horwood Limited

[82] Frank M. White "Heat Transfer," 1984 by Addison-Wesley Publishing Company