11-BIT FLOATING-POINT PIPELINED ANALOG TO DIGITAL CONVERTER IN CMOS 0.18μm TECHNOLOGY

by

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Abstract

As the technology advances, larger volume of circuitry is included in one chip such as in integrated sensor systems. An essential component in such sensor systems is Analog to Digital Converter (ADC) that converts the sensor output into digital data suitable for memories and processors. This project discusses the design of an 11-bit floating-point pipelined ADC designed especially for such systems. Because of the large number of circuit components in sensor systems silicon area and power consumption are limiting factors. Also sensors such as optical sensors produce a wide range of signal levels. Therefore the named ADC was chosen and designed to meet a low power consumption of 50mW and small silicon area usage of 0.837mm^2 while having a large dynamic range of 90dB. The ADC circuit was designed and fabricated in 0.18μm CMOS technology that resulted in two fabricated chips.

Acknowledgements

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Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

As the micro-machining technology advances, more circuitry can be implemented on a chip. Especially in devices such as integrated sensor systems usually there is a large number of different circuitry included in one chip. Figure 1.1 shows a general diagram of such systems. The sensor or sensor array provides analog signals, which are amplified and converted to a suitable form of signal for further processing. This suitable signal is usually in digital format, which makes the data processing and storage more efficient through micro-controllers/processors and memories. Sometimes even some data processing is done on the signal in the same chip before sending the data out.

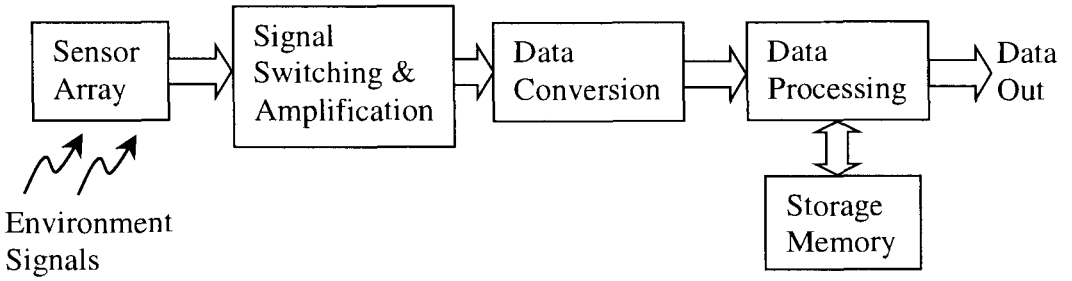


Figure 1.1: General block diagram of an integrated sensor system.

1.1 Analog to Digital Converter

A very important component of such sensor systems is the Analog to Digital Converter (ADC). As shown in Figure 1.1, data conversion block is the part where the ADC is used to convert analog signals coming from the sensors to digital signals. The digital signal is normally a binary number used commonly in digital circuits. Figure 1.2 shows a general block diagram of ADCs.

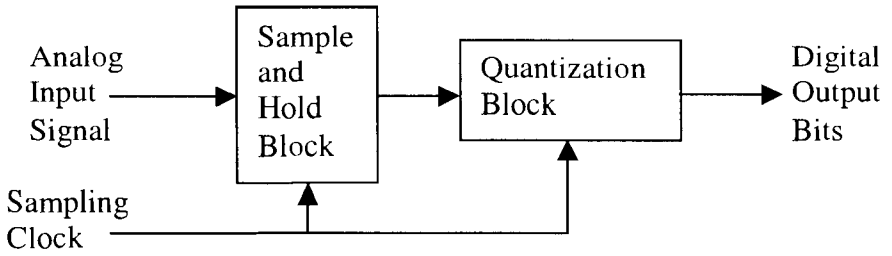


Figure 1.2: General block diagram of an Analog to Digital Converter.

The analog signal coming into the ADC is sampled with a specific clock frequency. According to the Nyquist's law [5, 14, 15] this clock frequency, which is the same as sampling rate, has to be equal or larger than twice the input signal frequency. Therefore the input signal frequency spectrum is sampled correctly and otherwise the high frequencies will be filtered out. The sampled analog data is then sent to a quantizer, where for every specific signal range that the input signal level falls within, a unique binary number is assigned to it. This number assignment is shown in Figure 1.3.

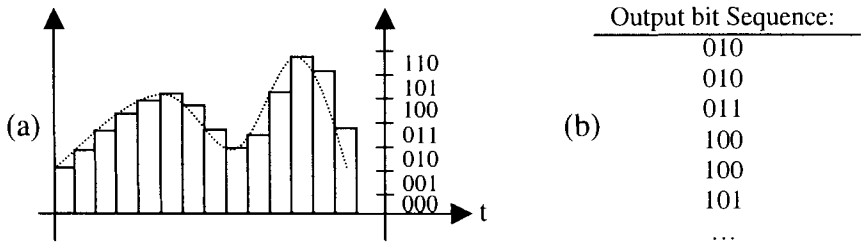


Figure 1.3: (a) Input signal (dashed line) and sampled data, (b) Example of output bit sequence corresponding to the sampled data levels in (a).

There are many different kinds of ADCs, which serve different purposes. A suitable ADC must be chosen carefully to provide features that help to optimise parameters required for a project. In the case of such integrated sensor systems, where normally a number of sensors are used along with electrical circuits as shown in Figure 1.1, two important parameters are the circuit area and the power consumption. It is very important to achieve a design with small silicon area usage along with a low power consumption to optimise the chip from the economical point of view. Therefore it is very important to choose a topology that not only meets the data

conversion requirements but also provides for the smallest silicon area and lowest power consumption possible.

Sensors such as photo sensors have analog signals with very large dynamic ranges as their output data. This means that not only we require to sample large signal levels with a suitable precision, but also very small signal levels require a high precision sampling to avoid the loss of the small signal data. Therefore a large dynamic range ADC is required for both large and small signals to be sampled with the required precision. There are two kinds of ADCs in general, uniform and non-uniform ADCs. Uniform ADCs are those of which divide the input signal range into equal sections and assign a unique binary number to each one of them. But the non-uniform ADCs divide the input signal range into non-equal signal sections. Two examples of non-uniform ADCs are logarithmic [13] and floating-point [2] ADCs.

In both named non-uniform ADCs, the divisions for smaller input signal levels are smaller compared to the divisions for the higher input signal levels. This means that the smaller signal levels are sampled more precisely. This has great advantages compared to uniform ADCs. In many cases, it is not required to sample higher input signal levels with a precision as high as smaller input signals. Using a uniform ADC causes the entire input signal range to be sampled with the same high precision and thus, the high input signals are sampled with an unnecessary precision. This causes a large inefficiency in conversion. Extracting extra data means having higher number of bits and extra circuitry to extract data. Using a non-uniform conversion instead, provides for a suitable precision for different input signal levels and thus saves in the number of bits. Saving in the number of bits usually means fewer components and thus smaller silicon area and power consumption.

1.2 Floating-Point ADCs

A floating-point ADC converts the input analog signal to a binary number in the floating-point format. Floating-point numbers are one of the most commonly used numbers in digital

processes. The floating-point concept is simply to keep only the required precision of a number to simplify the calculations and in the case of programming concerns, having smaller variable sizes to save in the memory usage of a program. As shown in Figure 1.4-a, instead of keeping a 10 digit decimal number, we can eliminate the extra precision and only keep a number of digits for required precision as the mantissa section of a floating-point number. The mantissa is multiplied by ten to the power of the exponent that here in Figure 1.4 is equal to the number of eliminated digits. In this example four digits are kept as the mantissa and the floating point is assumed to be at the end of this number. Therefore, the exponent is equal to 6. It can be seen from the Figure 1.4-a that not only the floating-point format simplifies the number, but also fewer digits (5 digits here) are required to be memorized.

This format is used especially in engineering calculations. The same thing can be done on binary numbers. The example in Figure 1.4-b shows a 15-bit binary number. If only 8 bits of precision are required, then 8 most significant bits are kept as the mantissa part of the number, which is multiplied by two to the power of exponent, which in this case is seven or $(111)_2$.

a) $1234567890 \rightarrow 1234 \times 10^6$

b) $(101110101010011)_2 \rightarrow (10111010)_2 \times 2^{(111)_2}$

Figure 1.4: Converting a number into the floating-point format: (a) a decimal number and (b) a binary number.

In floating-point ADCs, such a floating-point number is assigned to different input signal levels. Mantissa has a certain number of bits for a large range of input signal and therefore the sampling precision, which is the number of mantissa bits, is the same for large and small signals.

The ADC of this project is an 11-bit floating-point ADC. Same as the one shown in Figure 1.4-b, the 11-bit floating-point number consists of an 8-bit mantissa and a 3-bit exponent. Below, the advantage of using such an ADC compared to uniform ADCs is discussed.

1.2.1 Advantage of Using the Floating-Point Format

As mentioned before, we require sampling a high signal dynamic range especially in the case of integrated sensor systems. These sensors generate decades of analog signal, which even small signal levels require to be sampled with a high precision. Figure 1.5 shows the comparison between the Signal to quantization Noise Ratios (SNR) of three different ADCs.

Formula 1.2 is to calculate the signal to quantization noise ratio of an n-bit uniform ADC.

$$SNR[dB] = 20 \times \log\left(\frac{ISL}{MISL/2^n}\right) \tag{1.1}$$

ISL stands for Input Signal Level and *MISL* stands for Maximum Input Signal Level and n is the number of sample bits. The denominator in this formula is the amplitude of the quantization noise. Therefore the fraction in the parentheses is the Signal to Noise Ratio (SNR), which is converted into dB units.

In Figure 1.5, the bold dotted line is the SNR of an 8-bit uniform ADC. For the highest input signal this SNR is about 48dB and the SNR goes linearly to zero with the input signal level decreasing. The smallest signal level extractable by this ADC is about –48dB. Still we require sampling much smaller signals for sensor systems. One solution is to increase the number of sample bits for higher precision sampling, such as a 15-bit uniform ADC. As shown in Figure 1.5, SNR for such an ADC starts from 90dB for the highest input signal and a signal as low as -90 dB can be sampled. The dynamic range of this ADC is improved by 42dB compared to an 8-bit uniform ADC and is suitable for sampling sensor data. Yet, the very high number of bits demands a large circuitry. Therefore as a solution, the 11-bit floating-point ADC is proposed.

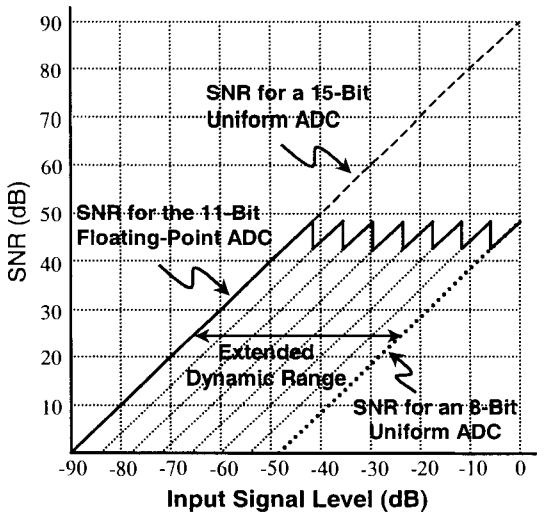


Figure 1.5: Signal to noise ratio of different ADCs

This ADC saves four bits in the sample binary number and yet provides for the same dynamic range as a 15-bit uniform ADC, as shown in Figure 1.5. The 15-bit ADC has a very high unnecessary SNR for input signal levels higher than –42 dB. The 11-bit floating-point ADC sacrifices this unnecessary precision using its 8-bit mantissa and 3-bit exponent. But why the SNR for such an ADC behaves like this?

For the highest input signal level, the mantissa has 8 bits of precision. Therefore the SNR for the highest signal is the same as the SNR for an 8-bit uniform ADC. There, the exponent is at its highest value which is seven or $(111)_2$. When the input signal level decreases, the SNR goes linearly down, until it drops 6dB to an SNR of 42dB. It means that the input signal level is going below half its maximum value and thus, the number of mantissa bits is decreasing by one. Therefore to keep the 8-bit mantissa, a least significant bit is added to the mantissa. The exponent decreases by one for the new range of input signal. Therefore again the sampling precision is 8 bits and the SNR jumps back to its maximum of 48dB. This keeps happening every 6dB dropping of the input signal level until the exponent value is zero. There, the mantissa value falls linearly to zero and results in the reduction of SNR to zero for the –90dB input signal level as shown in Figure 1.5.

1.3 Floating-Point ADC Circuit Blocks

The floating-point ADC presented here targets the same dynamic range as the ADC proposed in [2] but obtained having fewer number of output bits. The ADC investigated here is intended for applications in integrated sensor systems. A summary of features of this ADC and comparison of its performance with the ADC designed in [2] is brought in Section 3.1.

In general, there are two major blocks used to implement the floating-point ADC circuit. As shown in Figure 1.6, the first block is a Variable Gain Amplifier (VGA) and the second block is an 8-bit uniform pipelined ADC.

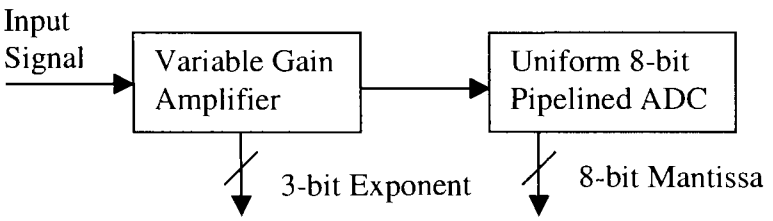


Figure 1.6: General block diagram of the floating-point ADC of this project.

The VGA block also generates the 3-bit exponent part and the 8-bit pipelined ADC generates the 8-bit mantissa part of the final floating-point number.

The concept of using these blocks is that we require keeping the 8-bit sampling precision for a wide dynamic range of the input signal, the same as in the floating-point format. The VGA makes this happen. The gain of the VGA is dependant on the input signal level. Lower input signal levels cause the VGA to have higher gains. The output of the VGA goes to the 8-bit pipelined ADC input. To use the entire 8-bit sampling precision of the pipeline, the signal at the input of the pipeline has to be higher than half its maximum input level. If the pipeline input signal goes lower than half its maximum value, it means that the 8-bit output number is going below half its maximum value, which will have a resolution equal to a seven bit number. The VGA amplifies the input signal to prevent the pipeline input to go below half its maximum value. Therefore, when the input signal level reduction causes the output of the VGA to reach to the half

point, the VGA gain will be increased to twice its previous value and therefore the VGA output will again jump to its maximum value for the pipelined ADC to sample the signal by its full 8-bit precision.

The VGA gain can be 1, 2, 4, 8, 16, 32, 64 or 128 (V/V) depending on the input signal level. Figure 1.7 shows the VGA transfer function. As it can be seen from this figure, for the highest input signal level the gain is equal to one and the VGA input and output reduce together to half the maximum value, where the gain increases to two.

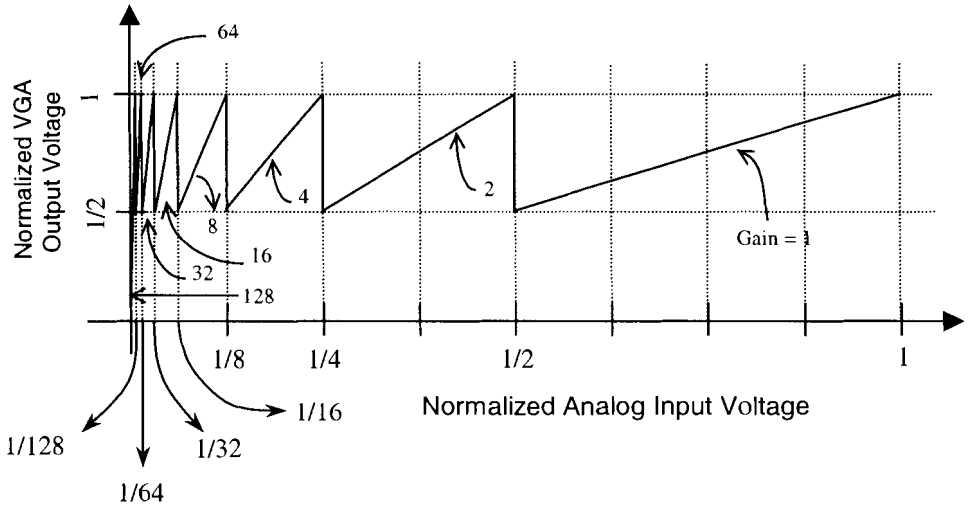


Figure 1.7: Output versus input of the VGA block.

The VGA output increases to the maximum value and goes down again by the input signal level reduction. This process repeats until the VGA gain is at its maximum 128 (V/V) after which the VGA output goes linearly to zero by the input signal level reduction. This process generates the 11-bit floating-point form that has the signal to quantization noise ratio shown in Figure 1.5.

Before going further into the circuit block details, it is necessary to know how flash ADCs function. Flash ADCs are used in different forms inside the blocks of the floating-point ADC. Section 1.3.1 below explains how a flash ADC functions.

1.3.1 Flash ADCs

Flash ADCs have a very simple structure and a small conversion delay. Figure 1.8 shows a general diagram of an n-bit flash ADC circuit. As shown in this figure, for an n-bit flash ADC, $m=2^n$ resistors and $m-1=2^n-1$ comparators are required. The resistor array generates 2^n-1 different DC levels between ground and V_{ref} voltage levels. Each DC level goes to one comparator.

The input signal to the flash ADC goes to all the comparators and is compared to all the DC levels. In a comparator if the input signal level is higher than its given DC value, the comparator output is one, otherwise it is zero. The outputs of the comparators are sent to a encoder, which generates an n-bit binary number. Therefore it is obvious that for an input signal between two adjacent DC voltage levels there is one unique binary number assigned to it.

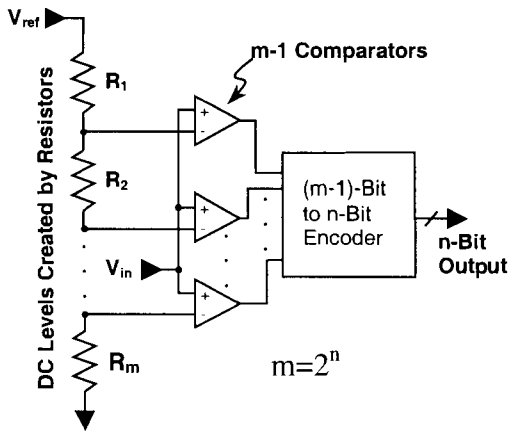


Figure 1.8: Circuit of an n-bit flash ADC.

As the resistor array generates the voltage ranges for the comparators, uniformity and non-uniformity of the flash ADC is dependant on the resistors values. When the values of the resistors are equal, there are equal voltage ranges and therefore the ADC is uniform. In contrast, when the resistor values are not equal, we can have any kind of non-uniformity. Table 1.1 shows the comparator outputs and the encoder outputs of a 3-bit flash ADC. In Table 1.1, V_{c1} to V_{c7} are the outputs of the comparators from the lowest to the highest input DC voltage respectively. V_{b0} to V_{b2} are the encoder outputs from the least to the most significant bit.

Table 1.1: Outputs versus the input signal of a 3-bit uniform flash ADC.

V_{c1}	V_{c2}	V_{c3}	V_{c4}	V_{c5}	V_{c6}	V_{c7}	V_{b2}	V_{b1}	V_{b0}
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	1	1
1	1	1	1	0	0	0	1	0	0
1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1

1.3.2 Variable Gain Amplifier

In this section, the block diagram of the VGA responsible to generate variable gains dependant to the input signal level is discussed. Figure 1.9 shows the general block diagram of the entire floating-point ADC. In the VGA block there are three Small Variable Gain Amplifiers (SVGA) in series, which generate the total gain of the VGA block.

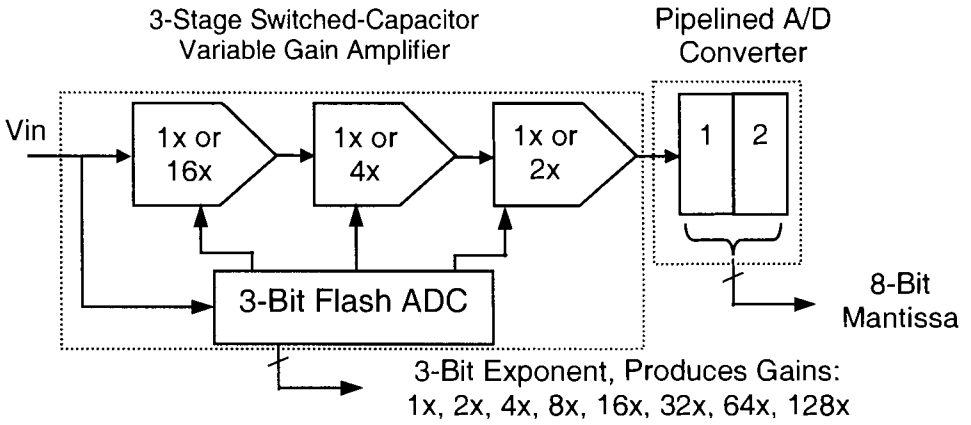


Figure 1.9: Block diagram of the Variable Gain Amplifier (VGA).

The loading effect of putting the SVGAs in series doesn't have any effect on their gain because of their properties. Therefore total gain is simply equal to the product of the gains of SVGAs. Every one of these SVGAs can have a gain equal to one or a higher gain as shown in Figure 1.9. The bits coming out from a non-uniform flash ADC control the gain of these SVGAs. The input signal goes to both the non-uniform flash ADC and the first SVGA. Three bits are generated through the flash ADC that adjust the gain of each SVGA and then, the input signal is

amplified through the SVGAs to receive the required amplification. The SVGAs are arranged from the highest gain to the lowest gain to reduce the cumulative noise of the VGA block.

As it was discussed before in Section 1.3.1 the non-uniformity of the flash ADC is generated using non-equal resistors in the resistor array. Table 1.1 shows different ranges provided by this resistor array, corresponding 3-bit binary numbers and gains for the VGA. A Logical one as an output bit of the flash ADC results in a gain of one for the corresponding SVGA and a logical zero results in the higher gain of that SVGA.

Table 1.2: Gain and binary output number for different signal ranges

Input Signal (x(t)) Ranges	Flash ADC Output	Gain
1/2< x(t) <1	111	1
1/4< x(t) <1/2	110	2
1/8< x(t) <1/4	101	4
1/16< x(t) <1/8	100	8
1/32< x(t) <1/16	011	16
1/64< x(t) <1/32	010	32
1/128< x(t) <1/64	001	64
x(t) <1/128	000	128

The three bits generated through the flash ADC of the VGA block are also buffered. delayed and sent out through a number of flip-flops as the exponent part of the final 11-bit floating-point number later shown in Chapter 2. The exponent number is delayed because in pipeline circuits, such as the one in this project, results are generated in different time intervals. Therefore each bit is delayed accordingly, so that all of which resulted from the same input signal arrive at the output at the same time. Detailed discussion about these delays is brought in Section 2.6.

1.3.3 8-Bit Pipelined ADC

As mentioned before in Figure 1.6 and Figure 1.9, the output signal of the VGA enters an 8-bit pipelined ADC. This uniform ADC is responsible for extracting the 8-bit mantissa of the

floating-point number. The number of stages for this pipeline ADC is chosen to be two due to the advantages gained. These advantages are discussed later in Section 3.1.

A general pipeline stage looks similar to the one of Figure 1.10. This stage extracts *n* bits of a final m-bit number. Therefore *m* should be dividable by *n* if the stages are assumed to extract equal number of bits and the number of stages would be equal to *(m/n)*. The input signal to the stage, V_{in}, will be sampled and hold through the S/H block. The S/H output goes to a subtracter circuit and an n-bit uniform flash ADC. This ADC converts the signal level to an n-bit binary number. This n-bit binary number is then converted back to an analog signal through an n-bit Digital to Analog Converter (DAC). As discussed in Section 1.3.1, a flash ADC compares its input signal level to a number of DC levels and assigns a binary number to it.

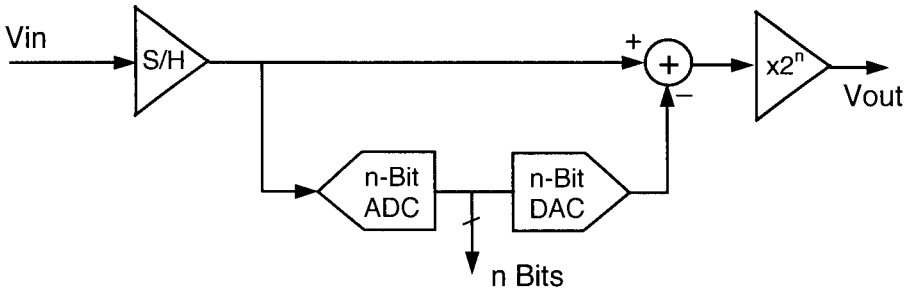


Figure 1.10: The block diagram of a general pipeline stage.

This binary number represents a specific range of signal, where the input level falls within. A DAC assigns a voltage level to a binary number to generate an analog signal. Therefore in the pipeline stage, the output of the DAC is not necessarily equal to the input of the flash ADC. There is a difference called quantization error. To extract this error, the input sampled signal and the DAC output signal are subtracted through a subtracter circuit. This error can be sent to other stages to be converted to digital for more sampling precision. As discussed in Section 1.3.1 in an n-bit flash ADC, the input range is divided into 2^n sections. Therefore the quantization error can't be larger than the size of these sections, meaning that the quantization error is equal or less than the maximum input signal divided by 2^n. Therefore, for the error signal to cover the entire input

range of the next stage, it is amplified by a gain of 2^n. The output of the stage is then ready to be sent to similar stages for further conversions.

The pipeline stages of this project extract 4 bits each. Therefore only two stages are required for an 8-bit conversion. The block diagram of the entire 8-bit pipelined ADC of this project is shown in Figure 1.11. The second stage doesn't have a Sample and Hold (S/H) block in it. A S/H block is required for the first stage to generate discrete time signals for the stage assuming that the input signal is continuous. But as you will see later in Chapter 2, the amplifier and subtracter blocks are made of switched capacitor circuits that also act like S/H circuits. Therefore the input to the second stage is already a discrete time signal. Also the S/H block in the first stage is hidden in the previous stage amplifier.

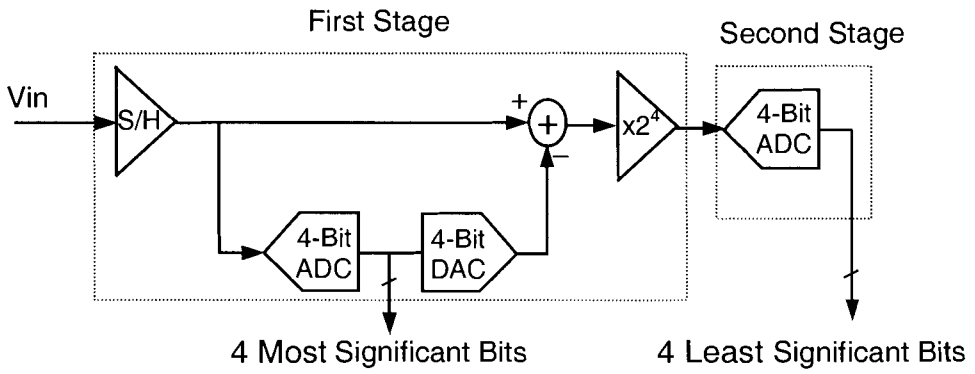


Figure 1.11: The block diagram of the entire 8-bit pipelined ADC

It can be seen that although the first stage is similar to a general pipeline stage, the second stage isn't required to have all the components. The reason is simply that the analog signal residue is not needed after the final 4 bits are extracted and therefore it can be discarded. Therefore only one 4-bit flash ADC suffices for the second stage. In some designs, the final stage is the same as other stages and the analog signal residue is sent out of the chip. This is done to enable cascading another ADC to the first chip to recover more bits out of the analog signal residue for more precision. But for the application of this project, not only chip cascading is not required, but also less power consumption and smaller silicon area usage demands eliminating any extra elements.

The advantages of using such a pipeline circuit is brought in Section 3.1. There you can see the parametric comparisons between this ADC and other ADCs.

1.4 Summary

An 11-bit floating-point pipelined ADC is proposed in this project as a solution to be used especially in integrated sensor systems. A number of improvements in the ADC characteristics were implemented to optimise the ADC to be used in such systems. These improvements include the smaller power consumption, smaller silicon area usage of the circuit and a high dynamic range sampling while having a small number of output bits.

In Chapter 2, the circuit and layout design of the components are discussed with all the component simulation measurements and results. At the end of this chapter a summary of the final circuit properties measured through simulations is provided. Chapter 3 provides the test results from the experiments done on two fabricated chips that include the essential components and the entire ADC circuit. These two chips were designed so that their measurements would help to verify the simulation results and advance the design of the circuits and components. The proposed ADC design is compared to some other ADC topologies and its performance is discussed. And finally the thesis conclusion is brought at the end of Chapter 3.

Chapter 2

Design of the Floating-Point ADC

2.1 Introduction

This chapter will discuss the circuit and layout design of the entire circuitry of the floating-point ADC. The design has been fabricated in CMOS 0.18μm technology, provided through Canadian Microelectronics Corporation (CMC). As mentioned in the previous chapter, the ADC of this project consists of two major blocks: VGA and 8-bit pipelined ADC. Each of these blocks contains a large number of smaller blocks. Further in this chapter, detailed design of every circuit component is discussed and then, they will be assembled to make larger components and blocks to finally achieve the entire ADC.

One of the major circuits used for analog signal processes is switched capacitor circuit. Switched capacitor circuits are used vastly in analog signal processing components of integrated circuits for their precise characteristics such as gain. The gain of amplifiers on boards can be adjusted using feedback resistors in general and usually a satisfactory result is achieved. But in integrated circuits, resistances are very dependant to the fabrication process. Where the ratio of resistances is important, resistance-matching techniques help to achieve a value close to the desired value. But resistor matching in integrated circuits is done with a poor quality. Unlike resistors, capacitors can be matched with a much higher precision. Therefore resistive circuits are mostly replaced with switched capacitor circuits to achieve much higher signal processing precision. Below, the switched capacitor circuits used in the ADC of this project are discussed.

2.2 Switched Capacitor Circuits

As mentioned above, switched capacitor (SC) circuits are used for the circuits where high precision signal processing is required. In the circuits of the ADC of this project, the most important thing is that the analog signal level passes through the stages with minimal error.

Therefore all the amplifier and subtracter stages are made of switched capacitor circuits. Figure 2.1 shows three mostly used basic switched capacitor circuits. Figure 2.1-a is a non-inverting SC circuit. There are two non over-lapping clock phases used: V_{p1} and V_{p2}. V_{p1} samples the input voltage level over the capacitor and V_{p2} sends the sampled voltage level out. Figure 2.1-b and c have the same configuration except for the clock phase arrangement that makes the first one inverting and the second one non-inverting. The difference between the circuit (a) and the other two is that in circuit (a), parasitic capacitances of the switches are parallel to the capacitor and affect the equivalent value of the capacitor. But in the other two circuits the effect of the parasitic capacitors are cancelled due to the topology used. In [5] these circuits are discussed in more details.

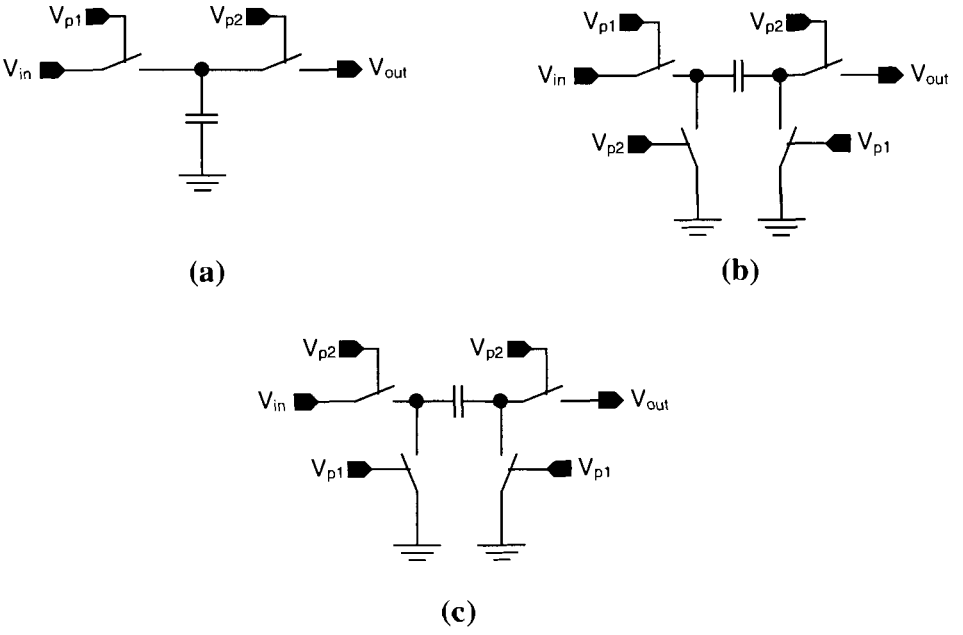


Figure 2.1: (a) non-inverting SC circuit, (b) inverting SC circuit and (c) non-inverting SC circuit.

As mentioned before, switched capacitors replace resistors in integrated circuits because equivalent circuit of a switched capacitor is similar to a resistor. Formula 2.1 shows that the ratio of the capacitor voltage changes and its current in every T seconds is equal to a constant value,

which is the equivalent resistor of the circuit. T is the switching period and c is the capacitor value. The value of the equivalent resistor is adjustable using the value of T or c.

$$R_{eq} = \frac{\Delta v_c}{i_c} = \frac{T}{c} \tag{2.1}$$

Similar SC circuits are used along with OpAmps to achieve subtracter and amplifier circuits. Before starting with these circuits, their components are discussed in details.

2.2.1 OpAmp for Switched Capacitor Circuits

An OpAmp suitable for SC circuits must have a high gain, high bandwidth and a high output current. High gain of the OpAmp helps to reduce the dependency of the total circuit gain to the OpAmp gain, and therefore reducing the total gain sensitivity to OpAmp parameters and conditions. Therefore the total gain of the circuit can be adjusted more easily by peripheral elements of the circuit such as the ratio of the feedback capacitors. High current and high bandwidth of the OpAmp together help to increase the speed of the stage the OpAmp is used in. High output current capability reduces the charge/discharge time of the capacitors and high bandwidth reduces the settling time of the stage. Below the circuit and layout design of such an OpAmp is discussed.

2.2.1.1 Circuit Design of the OpAmp

The topology of the OpAmp suitable for such application is a folded cascode OpAmp that uses gain-boosting technique [4]. Gain-boosting technique allows the OpAmp to have a high gain while maintaining a high gain bandwidth. Figure 2.2 demonstrates the gain boosting technique proposed in [4]. Figure 2.2-a shows a cascode gain stage with gain enhancement. Instead of supplying a DC biasing voltage for the gate terminal of *M1*, there is an additional single ended amplifier that is inserted in the circuit in the form of a negative feedback.

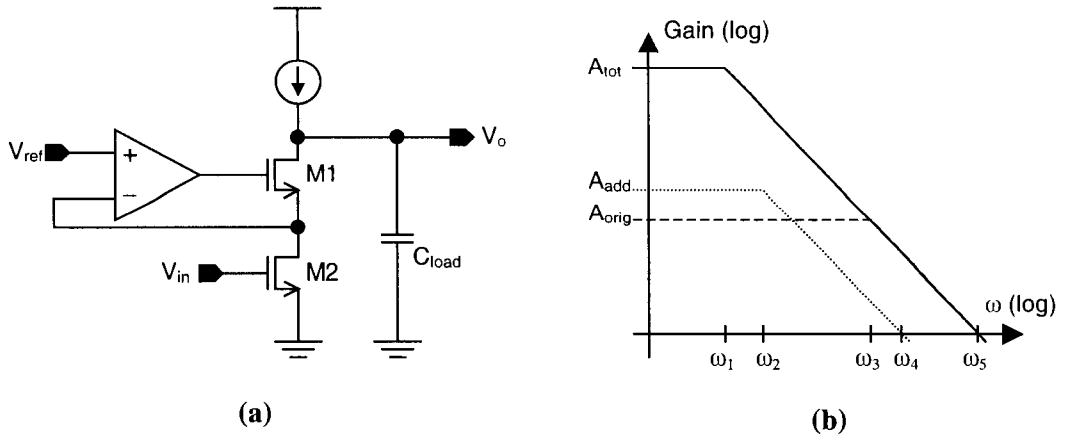


Figure 2.2: (a) Cascode gain stage with gain enhancement. (b) Gain Bode plots of the individual amplifiers and the total amplifier [4].

Figure 2.2-b shows the gain Bode plots of the original cascode stage (A_{orig}), additional amplifier (A_{add}) and the improved cascode circuit (A_{tot}). As it can be seen from this figure, the total gain of the circuit is boosted a lot while the unity gain of the improved circuit is the same as the original cascode amplifier. The amount of gain improvement from [4] is calculated from:

$$A_{tot} = g_{m1}r_{o1}(g_{m2}r_{o2}(A_{add}+1)+1) \qquad (2.2)$$

In this formula, g_{m1} and r_{o1} are *M1* parameters and g_{m2} and r_{o2} are *M2* parameters and A_{add} is the gain of the additional amplifier. The same technique was used to improve the gain of a folded cascode amplifier.

Figure 2.3 shows the circuitry for the high-gain, high frequency OpAmp of this project. I have modified the topology compared to the one presented in [4] to simplify the circuit as much as possible. Doing this I could design smaller circuit layout and therefore a smaller circuit in terms of silicon area usage is achieved.

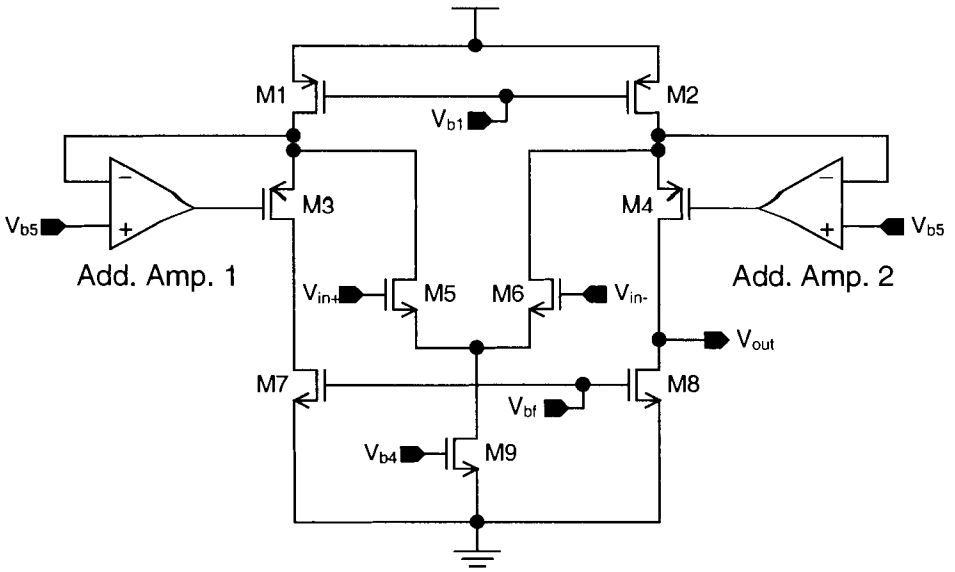


Figure 2.3: Schematic of the high-gain high-frequency OpAmp of this project

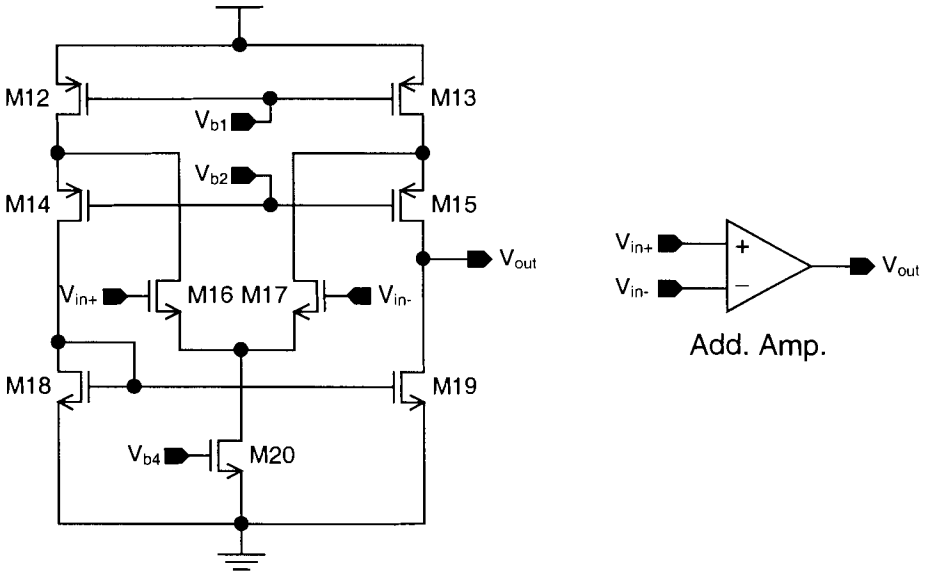


Figure 2.4: Additional single-ended folded cascode amplifier circuit and its symbol.

Two smaller additional amplifiers (Add. Amp.) are used as feedback amplifiers to boost the gain of a folded cascode amplifier as shown in Figure 2.3. These additional amplifiers also use folded cascode topology. Figure 2.4 shows the circuit of the additional amplifier used. Table 2.1 lists the transistors widths and lengths of both original and additional cascode amplifiers. As mentioned before, all designs are implemented in CMOS 0.18μm technology.

Table 2.1: List of widths and lengths of the transistors used in the OpAmp circuitry.

Main Stage Figure 2.3			Additional Amp. Figure 2.4		
Transistor Name	Width	Length	Transistor Name	Width	Length
M1 & M2	72 μm	0.35 μm	M12 & M13	2 μm	0.35 μm
M3 & M4	10 μm	0.35 μm	M14 & M15	5 μm	0.35 μm
M5 & M6	50 μm	0.35 μm	M16 & M17	1 μm	0.35 μm
M7 & M8	20 μm	2 μm	M18 & M19	1 μm	3 μm
M9	90 μm	2 μm	M20	3 μm	0.7 μm

There are a number of biasing voltages coming to the OpAmp circuit provided from DC biasing voltage generator circuits. The output DC bias voltage of the OpAmp is too sensitive to the transistor parameters and biasing voltages. A slight change in transistor parameters or biasing voltage levels can result in the saturation of the output transistors and damage the performance of the amplifier. Fabrication process always contains some amount of error and beside that, any change in the temperature of the chip can change circuit parameters. Therefore a special biasing method is used to eliminate the output bias point sensitivity to these parameters.

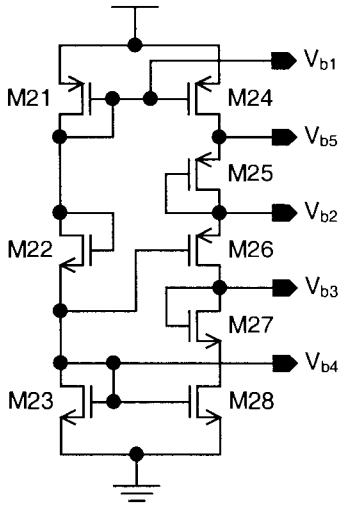


Figure 2.5: Initial biasing voltage generator circuit for the OpAmp.

First, a simple DC biasing voltage circuit is designed to create the initial biasing voltage levels. This circuit is shown in Figure 2.5 and the transistors widths and lengths for this circuit are provided in Table 2.2. Note that the V_{bf} biasing voltage seen in Figure 2.3 is not coming from this

circuit but as later shown, it is coming from an additional biasing circuit to avoid the output bias voltage of the OpAmp to saturate. The values of the biasing voltages generated through the circuit of Figure 2.5 are provided in Table 2.3 measured from the post-layout simulations.

Table 2.2: Transistors widths and lengths for initial biasing circuit.

Transistor Names	Width	Length
M21	3.5 μm	0.35 μm
M22	1 μm	1 μm
M23	2 μm	0.4 μm
M24	4 μm	0.35 μm
M25	4 μm	0.35 μm
M26	1.5 μm	0.4 μm
M27	0.8 μm	5 μm
M28	2 μm	0.4 μm

Table 2.3: Values of the biasing voltages.

Voltage Names	V_{b5}	V_{b1}	V_{b2}	V_{b3}	V_{b4}
Value (V)	3.214	2.415	2.343	1.679	0.915

In the circuit of Figure 2.3, there is a biasing voltage named V_{bf}. For any different circuit parameters, this voltage can be adjusted to bring the output bias voltage to the middle of the power rails. Looking in the OpAmp circuit, you can see that the output level is reversely proportional to the changes in V_{bf} with some gain.

Now if we supply the biasing voltages and send equal DC voltages to the input pins V_{in+} and V_{in-}, using a negative feedback shown in Figure 2.6 we can keep the output voltage level in the middle of the rails. The feedback includes a voltage source to shift the output voltage level down to the desired value, because the actual V_{bf} level is smaller than the output operating point. If for any reason, such as a change in temperature, the output level increases it causes the V_{bf} voltage level to increase. This forces the output voltage level to reduce and vise-versa. Therefore this negative feedback brings the output voltage level to the middle of the power rails for different conditions and parameters the OpAmp is working under.

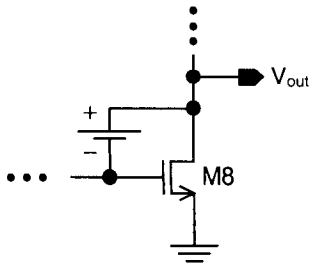


Figure 2.6: The negative feedback used to keep the output DC level in the middle of the power rails.

This feedback can't be used in the OpAmp circuit, because it damages its operation drastically. So what I did was that I copied the entire OpAmp circuit of Figure 2.3 and used the feedback in the copied one as shown in Figure 2.7. This secondary circuit is only used to generate the V_{bf} voltage level and doesn't have any other purpose. Yet generating V_{bf} is so effective in the OpAmp performance that it's worth it to design the circuit discussed above. Figure 2.7 shows the circuit of this additional component, the V_{bf} generator. All the circuit components and the biasing voltages are the same as the corresponding ones in Figure 2.3. Only a feedback circuit, which is basically a common drain, is added and V_{b3} biasing voltage is provided from the initial biasing circuit to bias the V_{bf} generator circuit input terminals. The common drain circuit provides the DC voltage difference between the output voltage level and V_{bf} such as the voltage source of Figure 2.6.

The V_{bf} biasing voltage goes to the OpAmp of Figure 2.3 and because both the OpAmp and the V_{bf} generator circuit are the same, the OpAmp output bias point would be the same as the V_{bf} generator circuit output voltage. These circuits are placed very close to each other in the layout to have the same characteristics and operation conditions such as the temperature. Therefore in any different condition they both change together and V_{bf} keeps adjusting the output bias point to hold it in the middle of the power rails. Table 2.4 shows the parameters of the feedback circuit.

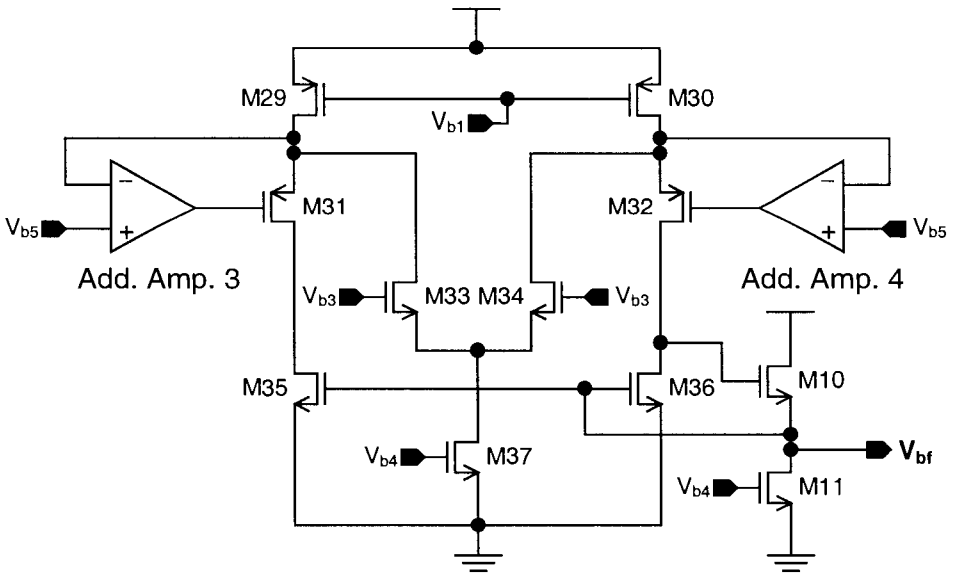


Figure 2.7: The V_{bf} generator circuit (similar to Figure 2.3 only with feedback).

Table 2.4: Transistor parameters of the feedback circuit.

Transistor Names	Width	Length
M10	12 μm	0.35 μm
M11	5 μm	1 μm

Figure 2.8 shows entire OpAmp circuit and Table 2.5 summarizes its parameters. To implement the OpAmp, there are some issues and sensitive points that have to be considered. Below the layout design of the folded-cascode OpAmp is discussed.

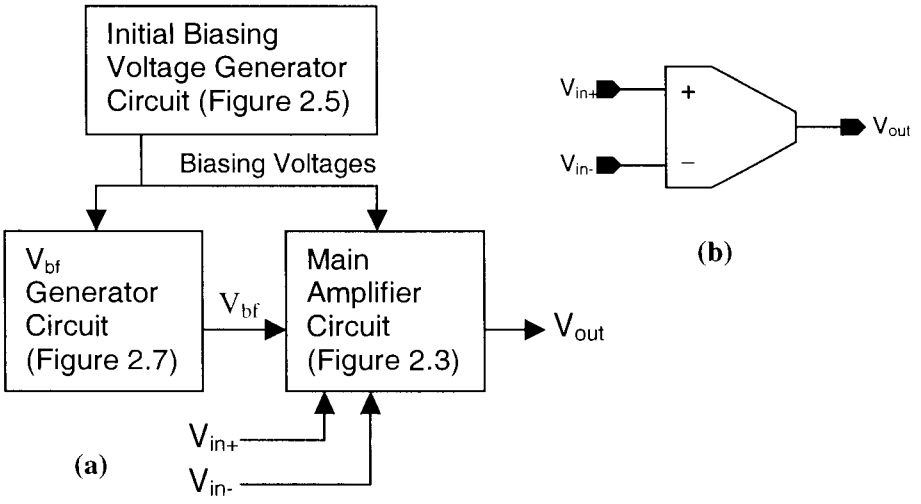


Figure 2.8: (a) Block diagram of the entire OpAmp Circuit. (b) Symbol of the OpAmp.

Table 2.5: Summary of the parameters of the folded-cascode OpAmp.

Parameter	Value	Unit
Gain	58.7	dB
CMRR	58.9	dB
Unity Gain Bandwidth	930	MHz
3dB Bandwidth	1	MHz
Phase Margin	71	Deg.
Output Current	70	μA

2.2.1.2 Layout Design of the OpAmp

There are a few issues that have to be considered in analog layout designs such as: using small silicon area, matching all related and corresponding components, considering parasitic elements, considering layout design rules and etc... Some of these issues are discussed below.

The software used for all the circuit and layout design is Cadence©. In Virtuso©, the layout design tool of Cadence©, there is a Design Rule Check (DRC) tool that takes care of checking all the design rules such as layer spacing, width and etc... It makes the layout design much easier and one shouldn't worry a lot about the rules while errors can be easily found and corrected. Layout Versus Schematic (LVS) tool is another useful tool in Cadence©, which compares the designed layout to the circuit schematic that is already designed and shows the possible differences. This is a great tool to design a circuit layout equal to the designed schematic.

Component matching and silicon area usage are kinds of issues that must be taken care of by a designer. Silicon area usage is important from the economical point of view for industries, and from the silicon area limitation point of view for the university research purposes where only a limited area is granted to each researcher. A designer should keep the components as close as possible within design rules for this purpose. But parasitic elements such as parasitic capacitors or leakage currents limit the minimum distance between components. In the case of parasitic capacitors, where passing layers above each other can easily generate a capacitor, it is very important not to pass different layers from the same area especially for the sensitive nodes.

Otherwise pass layers where there is a thicker isolator layer in between them to minimize the effect of parasitic capacitors.

Knowing these issues, it is time to discuss the OpAmp layout design. It is essential for some circuit elements such as transistors used in current mirrors or input or active loads of differential amplifier stages to have equal parameters or precise ratios. Otherwise currents and voltages in circuit branches will be different than their intended values and will cause properties different to what was initially intended or even failure in functionality of the OpAmp. Therefore matching important components, which in the case of OpAmps are transistors, is very important. Transistor matching is done mostly by breaking the transistor widths into smaller values to get a number of smaller transistors. Smaller transistors are put beside each other one by one and their terminals are connected in a way to form two similar transistors. The arrangement of the smaller transistors follows a common centroid model, meaning that the center of weight for two matched transistors is the same. Figure 2.9 shows two transistors and how they are matched.

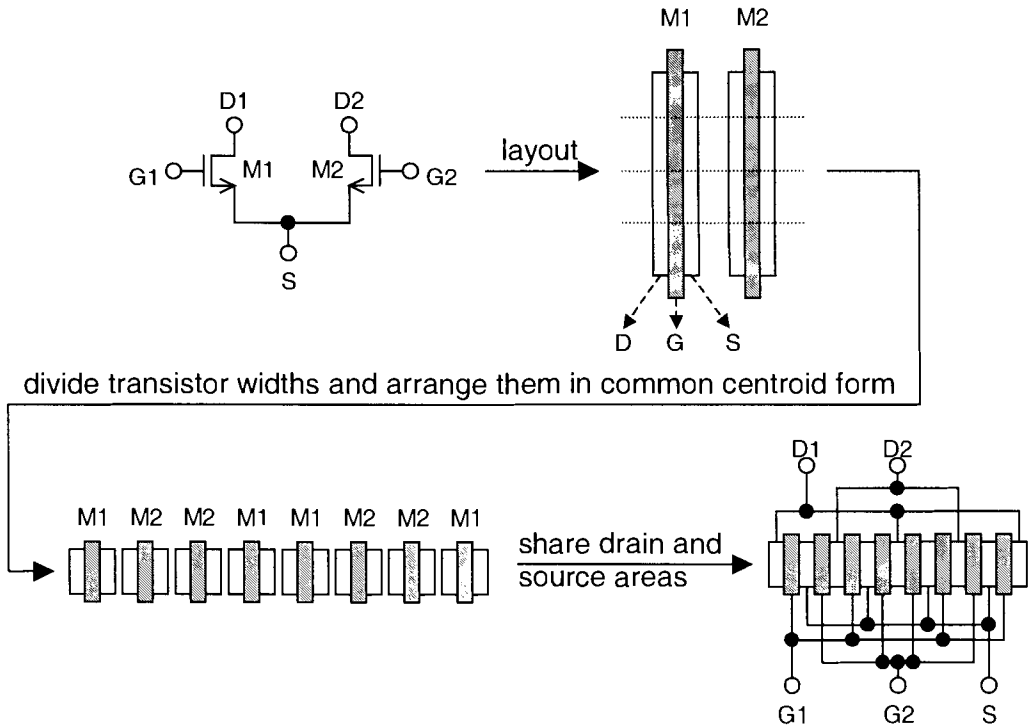


Figure 2.9: Matching of two transistors that their source terminals are connected.

As it is seen in this figure, where two transistors share their drain or source terminals in a circuit, they can share the same diffusion area. This matching method not only minimizes the differences caused by the fabrication process between two transistors, but also minimizes the parasitic capacitances of drain and source nodes [5, 6]. For all the layouts designed for this project, above issues are firmly considered. Figure 2.10 and Figure 2.11 show the layout of the parts and the entire circuit of the OpAmp. The layout of the V_{bf} generator circuit (Figure 2.7) is very similar to the layout of the main amplifier stage shown in Figure 2.10-a. Therefore it is not repeated here. But it is seen in the final OpAmp layout in Figure 2.11.

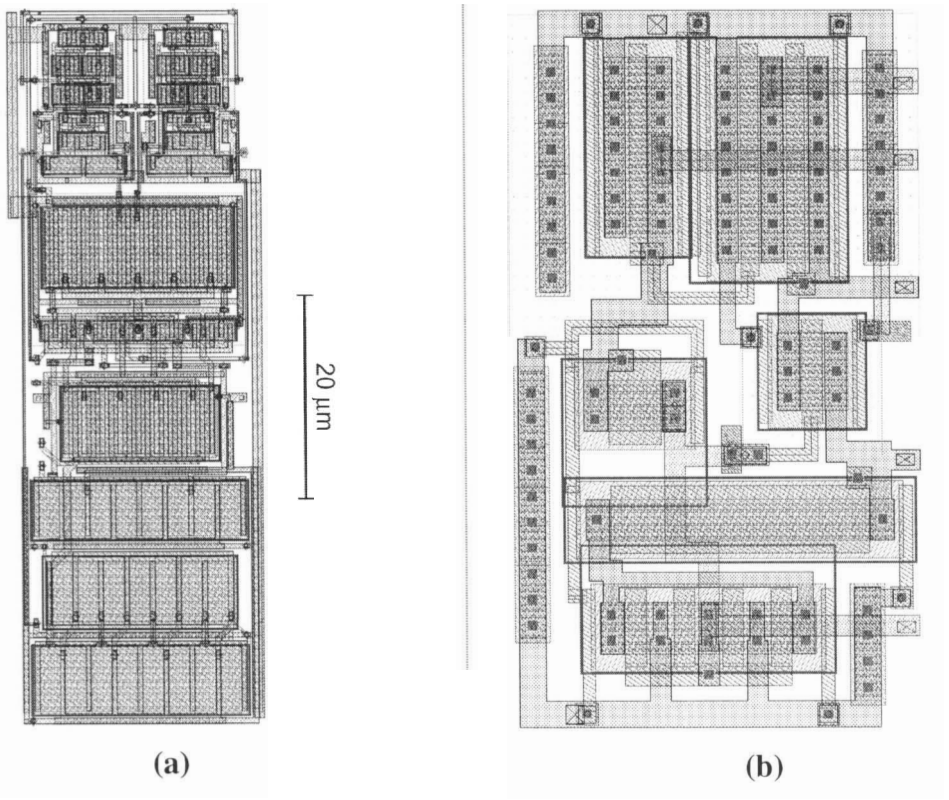


Figure 2.10: (a) Layout of the main amplifier section (Figure 2.3). (b) Layout of the initial biasing voltage generator (Figure 2.5).

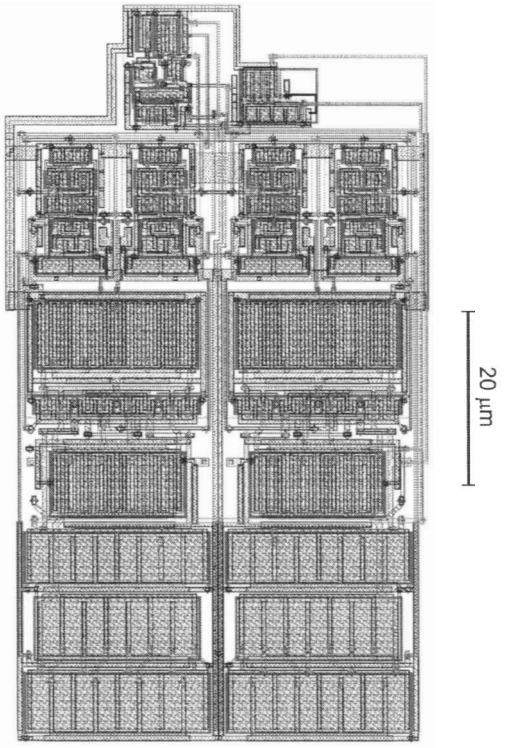
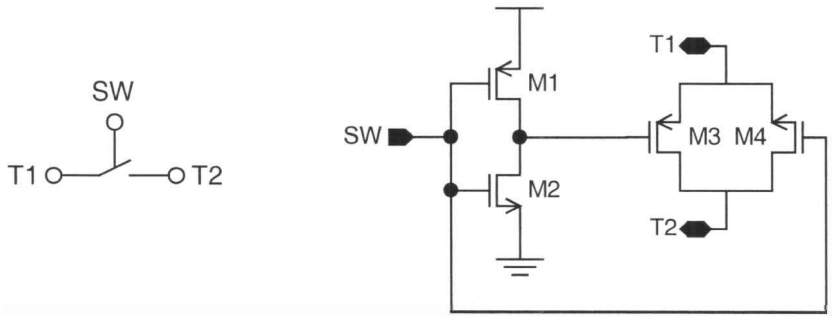


Figure 2.11: Layout of the entire OpAmp circuit (Figure 2.8).

2.2.2 Switches

The next component used in the switched capacitor circuits is the analog switch. A switch simply works as a contact, connecting two nodes together. An ideal switch has no resistance and current limitation. But analog switches always have some resistances that limit the current through them. This limitation can slow down the circuit especially where they are trying to charge/discharge capacitors. Therefore switches are designed to achieve a desired speed. Figure 2.12 shows the symbol of a switch and its general circuit topology. You can see that the switching part in Figure 2.12-b is basically an n-channel and a p-channel transistor in parallel. This is done to achieve rail-to-rail analog signal switching capability. When the transistors are on the switch is closed and otherwise it is open. A digital signal, *SW*, controls the close/open position of the switch. A digital inverter is used to invert the *SW* signal for the p-channel transistor. For these transistors to be operational at the same time, the gate signal of the p-channel should be reversed of the n-channel transistor. In the circuit of Figure 2.12, when the *SW* signal is high, the switch is

close and vise-versa. The same switch topology is used as the switches of this project. Table 2.6 lists the transistor parameters for the switch circuit. Also Figure 2.13 shows the layout of the switch circuit.



(a) **(b)**

Figure 2.12: (a) Symbol of a switch. (b) General circuit topology of an analog switch.

Table 2.6: Transistor parameters of the circuit and layout design.

Transistor Names	Width	Length
M1	1.3 μm	0.3 μm
M2	0.5 μm	0.35 μm
M3	3 μm	0.3 μm
M4	3 μm	0.35 μm

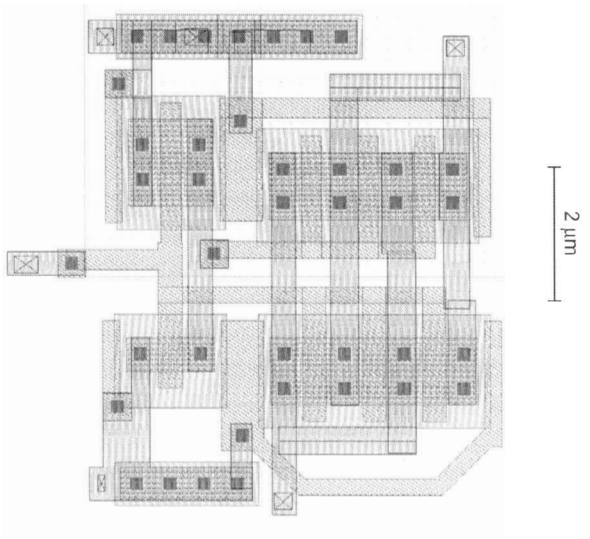


Figure 2.13: Layout of the switch circuit.

Below, the switch performance is tested to charge and discharge a 1pF capacitor. Figure 2.14 shows the schematic of the test circuit. Two non-overlapping clock phases, V_{p1} and V_{p2}, are used to control the switches. Figure 2.15 shows post-layout simulation results of the capacitor voltage V_{cap} and clock phases.

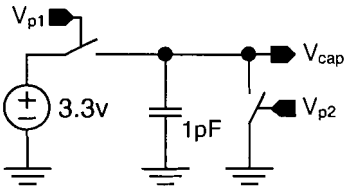


Figure 2.14: Schematic of the test circuit.

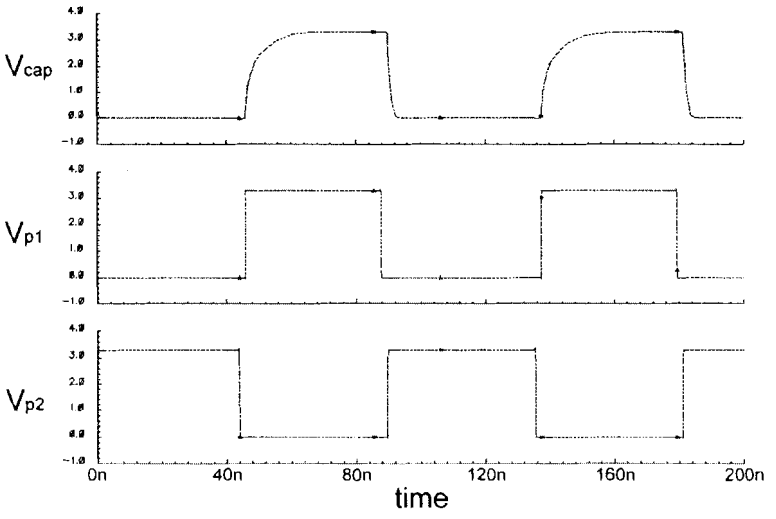


Figure 2.15: V_{cap} and clock phase waveforms versus time for the post layout test circuit.

2.2.3 Low Frequency OpAmp

In many cases in the circuit of the project, an analog buffer is required. High quality analog buffers are usually made of an OpAmp with its output connected to its negative input terminal as shown in Figure 2.16. The output in this case perfectly follows the input.

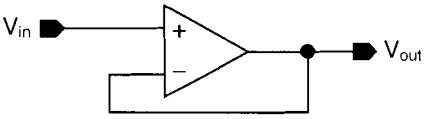


Figure 2.16: Schematic of an analog buffer using OpAmp.

Using the high-gain high-frequency OpAmp that is already designed in Section 2.2.1 a buffer can be designed. But using this OpAmp has two big disadvantages. First, this OpAmp consumes a lot of current intended for capacitor charge/discharge purposes. Second, it occupies a very large layout area. These two disadvantages leaded to designing a simple, more economical OpAmp. As mentioned, there are a lot of DC voltages in the entire ADC circuit that need buffering. Therefore a low frequency OpAmp with a simple topology is used for this purpose. The schematic of this OpAmp is shown in Figure 2.17.

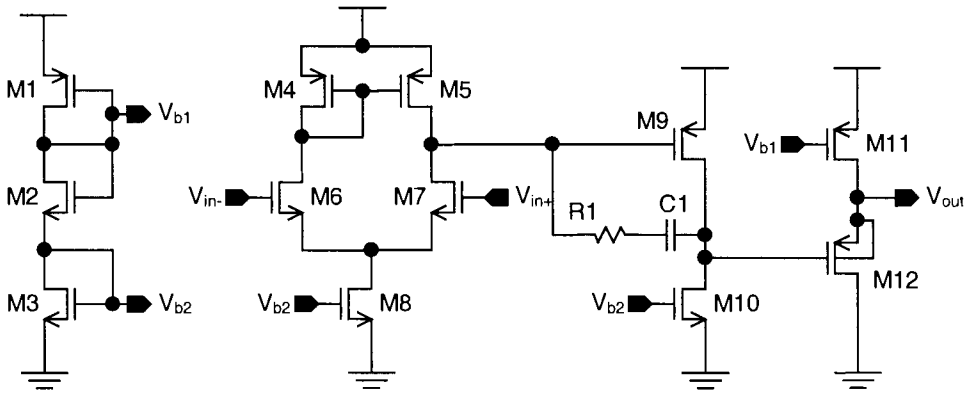


Figure 2.17: Schematic of the low frequency OpAmp.

Table 2.7 lists transistor parameters of this OpAmp. The most important parameter in this OpAmp is its gain. Higher gains are more desired to minimise the difference error between the input and the output of the buffer. Table 2.8 summarises the post-layout parameters of the low-frequency OpAmp. Figure 2.18 shows the gain versus frequency diagram of the OpAmp.

Table 2.7: Transistor parameters of the low-frequency OpAmp.

Component Names	Parameter Value		Component Names	Parameter Value	
	Width	Length		Width	Length
M1	5 μm	0.5 μm	M9	2 μm	1 μm
M2	0.4 μm	4 μm	M10	5.2 μm	1 μm
M3	5 μ m	0.5 μm	M11	10 μm	0.3 μm
M4 & M5	1 μm	1 μm	M12	50 μm	0.3 μm
M6 & M7	1 μm	0.35 μm	C1	100fF	
M8	5 μm	1 μm	R1	95 KΩ	

Table 2.8: Summary of low-frequency OpAmp Parameters.

Parameter	Value	Unit
Gain	83.4	dB
CMRR	84.5	dB
Unity Gain Bandwidth	32	MHz
3dB Bandwidth	2	MHz
Phase Margin	90	Deg.
Output Current	26	μA

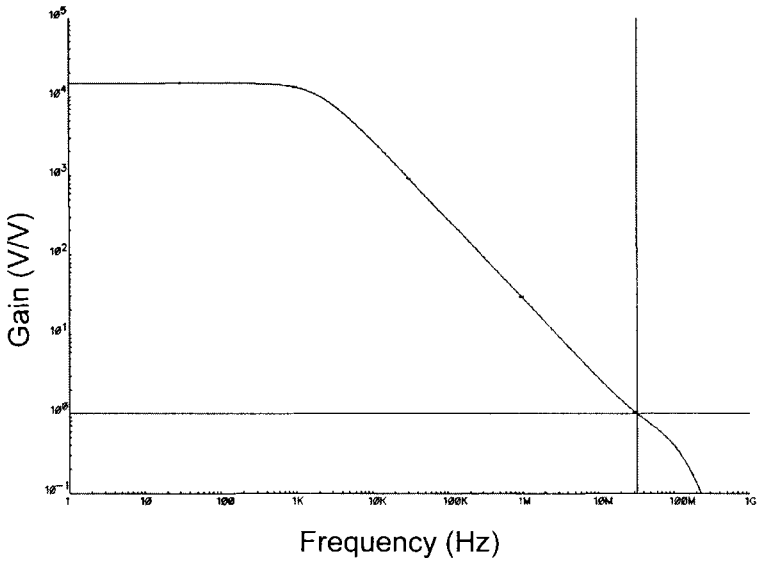


Figure 2.18: Gain versus Frequency of the OpAmp.

For the layout design of this OpAmp, new issues are the ones about the compensation resistor and capacitor. Because of the *Poly* layer linear resistance properties, all the resistors of this project are made of *Poly* resistors. Also to avoid a long resistor, resistors are broken into a series of resistors, placed parallel to each other. Extra *Poly* layer is repeated on both sides of the resistor as dummy components to provide similar fabrication process conditions for all parallel resistors. In the case of capacitors, to avoid consuming a large area for a capacitor, instead of two-layer capacitors, six layer capacitors designed from *Poly* to *Metal-5* layers for all the capacitors of this project. Figure 2.20 demonstrates a general diagram of the capacitor layout designed for the ADC circuit and Figure 2.21 shows the layout of the entire low frequency OpAmp circuit.

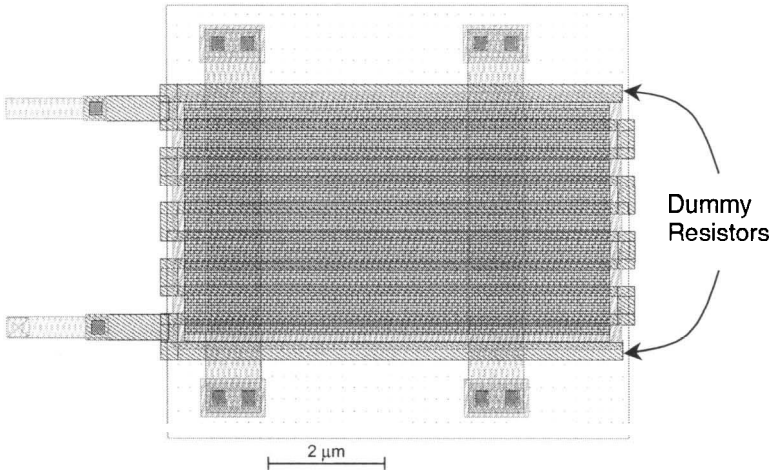


Figure 2.19: Layout of the OpAmp compensation resistor made of poly silicon (*Poly*) layer.

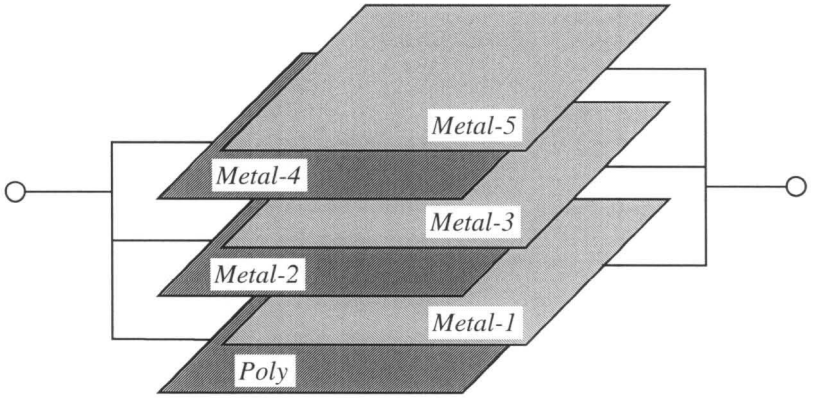


Figure 2.20: General layout of a capacitor designed for the ADC.

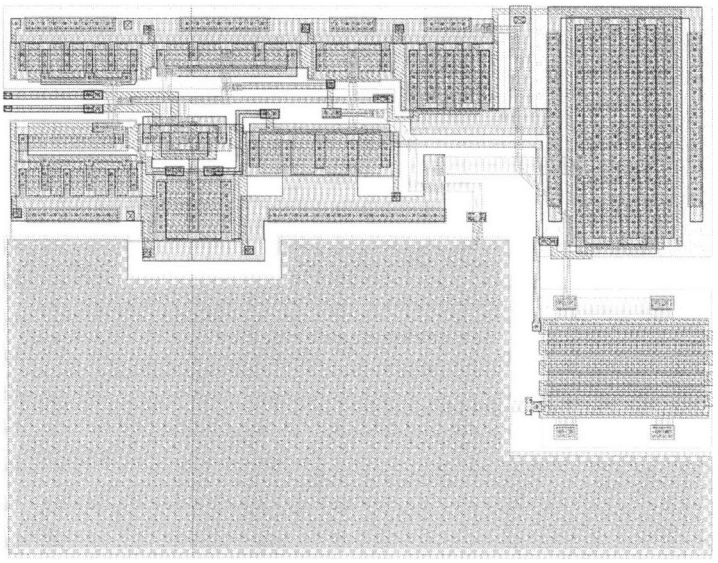


Figure 2.21: Layout of the low frequency OpAmp.

2.2.4 Switched Capacitor Variable Gain Amplifier

After discussing most of the basic components, it is time to discuss one of the most important components of the ADC. This component is the basic switched-capacitor variable gain amplifier. This component is used repeatedly in the ADC stages to amplify analog signal levels. The idea of this amplifier is to implement a circuit similar to the architecture shown in Figure 2.22. The gain of such an amplifier is $A_v = R_2/R_1 + 1$ when the switch is open. When the switch is closed, the gain A_v is equal to one.

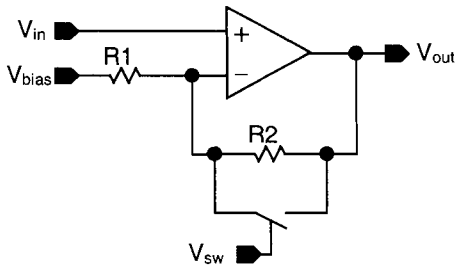


Figure 2.22: Schematic of a VGA using resistive feedback.

Therefore one of the two possible gains can be chosen by simply opening and closing the switch across R_2. As mentioned before in the beginning of Section 2.2, using resistors in layout especially for high precision circuits is not advantageous due to the high errors in the resistor values and their matching occur in fabrication processes. Therefore capacitors are used for their much higher value and matching accuracy. Also as mentioned in the same section, Switched Capacitor (SC) circuits can replace resistors in circuits. Therefore the schematic of Figure 2.22 can be implemented as the SC circuit shown in Figure 2.23. There are two non-overlapping clock phases used in this circuit named V_{p1} and V_{p2} shown in Figure 2.24 that are buffered through digital buffer inverters. These inverters are discussed later in Section 2.3.1. The clock signal shown in Figure 2.24 is the main clock generated from a clock generator circuit discussed in Section 2.3.5. The two clock phases used in the ADC circuit are generated using this clock signal. When the Gain Select signal, V_{gs}, has a logical low value, a high level on V_{p1} resets the circuit by discharging C_1 and C_2 capacitors to their initial values and samples the input voltage level over

C_3. Then a high level on V_{p2} sends the sample to the circuit where it is amplified using the feedback capacitors C_1 and C_2. In this case the circuit gain A_v is equal to $C_1/C_2 + 1$. A logical high on V_{gs} causes the output of the *OR* gate to be high all the time and therefore the switch *SW1* is closed and bypasses the capacitor C_2 and the gain of the stage will be equal to one.

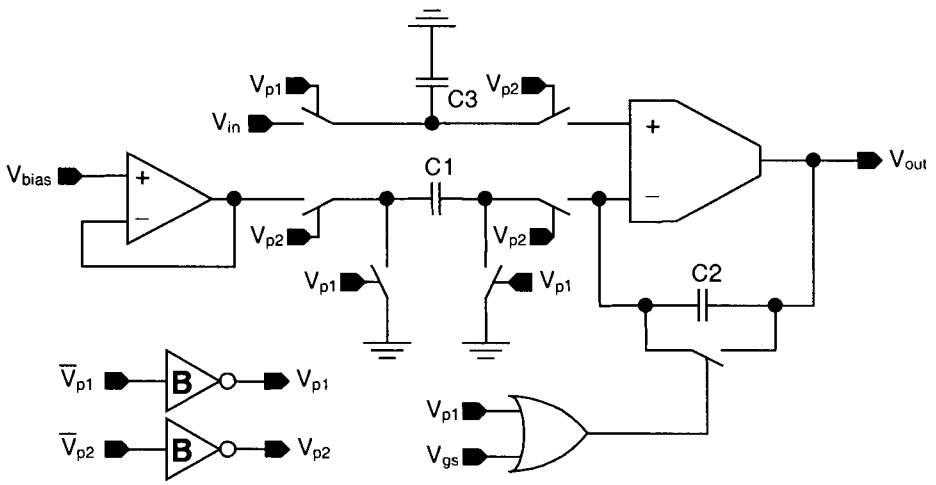


Figure 2.23: Schematic of the switched capacitor VGA.

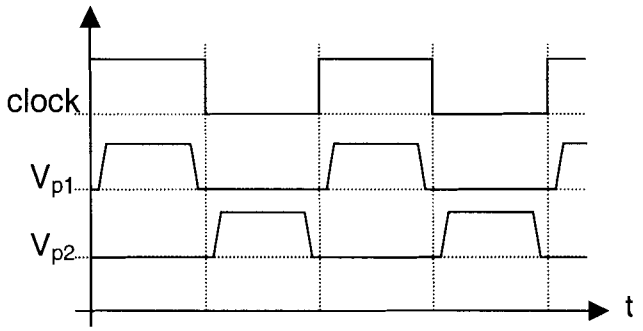


Figure 2.24: Clock signal and the clock phases used in the ADC circuit.

The *OR* gate is inserted in this circuit, so that a low on the gain select signal V_{gs} can provide normal switching operation of the capacitor C_2 for a gain of $C_1/C_2 + 1$. Otherwise a high continues level on V_{gs} causes a closed switch position to bypass C_2 for a gain of one. That's how the variable gain capability of the circuit is achieved. Also there are two inverters that are used to buffer the clock phases for the switched capacitor circuitry. The circuit and layout design of the *OR* gate along with other digital circuits used in this project are discussed later in Section 2.3.

In Figure 2.22, there is no resistance in series to the input voltage. But the switched capacitor circuit added in series to the input voltage made of C_3 capacitor in Figure 2.23 is absolutely necessary. Because normally the input to this circuit is coming from another switched capacitor circuit and in switched capacitor circuits the output is only valid for a specific period of time. Therefore input switch samples the valid data over C_3 by the clock phase V_{p1} and this correct signal level will be amplified through the circuit by the clock phase V_{p2}. Without this input sampling circuit, in the period of V_{p2} when the circuit amplifies, invalid input signals will be amplified and a wrong output signal will be generated.

All the gains of the amplifiers in the ADC are either one or are equal to a number that is a power of two. Therefore the basic VGA can have gains equal to two and one and from now on will be called the gain-of-2 VGA. To achieve this gain the value of C_1 must be equal to the value of C_2. To minimize the effect of parasitic capacitors on the gain of the amplifier, all capacitors are chosen to have values much greater than the parasitic capacitors. Simulations showed that the parasitic capacitors have values smaller than 50fF and therefore a good value for the capacitors of the circuit was chosen to be $C_1 = C_2 = C_3 = 1pF$. Capacitors larger than 1pF may give better results, but capacitors in a circuit consume very large silicon area from the layout design point of view. Therefore it is desired to keep capacitances as small as possible. Not only that, but also large capacitors drastically reduce the speed of the circuit. Therefore the best compromise was to choose the 1pF value for the capacitors.

In Figure 2.23, there is a buffer that sends the biasing voltage V_{bias} to the circuit. This DC voltage comes from a source that generates suitable biasing voltage. Because this biasing voltage goes to a large number of stages it is necessary for every stage to have such a buffer. Without this buffer, V_{bias} can become very noisy and unstable when each stage consumes a high volume of current out of this line to charge/discharge the stage capacitors. Inserting this buffer isolates the biasing voltage of stages and assures a much cleaner operation. The OpAmp used as the buffer, is

the low-frequency OpAmp discussed in Section 2.2.3. The reason for needing the V_{bias} voltage level is discussed in more details in Section 2.2.6.

From now on, the circuit shown in Figure 2.23 will be replaced with its symbol shown in Figure 2.25 for simplicity. This block is the basic block of all the switched capacitor amplifiers, used in the ADC circuit.

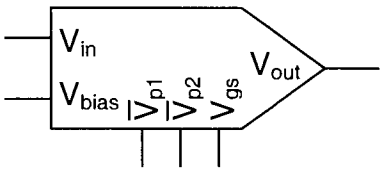


Figure 2.25: Symbol used for the gain-of-2 VGA of Figure 2.23.

As shown in Figure 2.26, to test the gain-of-2 VGA, its output is sampled over an extra capacitor using the clock phase V_{p2}, when the amplifier output is valid to get a cleaner signal only for the test purpose. In Figure 2.27, V_{gs} and I/O signals are shown. In this figure the change in the amplifier gain value depending on the V_{gs} signal value is visible.

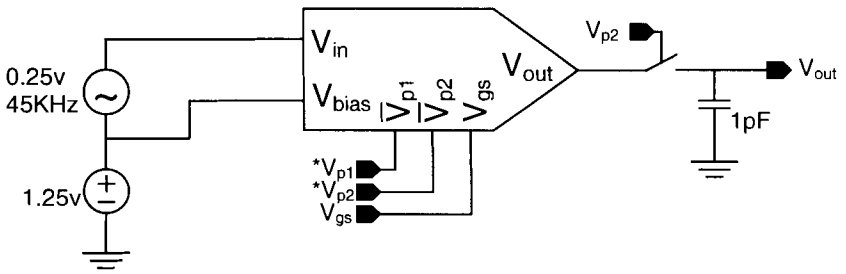


Figure 2.26: Schematic of the test circuit for the gain-of-2 VGA.

In the low state period of V_{p2} when the VGA is amplifying the signal, there is a delay until the output signal reaches its final valid value. This is the reason there are voltage spikes seen on the output voltage. Therefore the clock phase high state period has to be large enough to give time for the output voltage settlement. Therefore the clock phase period, which is half the clock period, can't be smaller than this settling time delay. From the simulation, the settling time is measured to be around 50 ns and therefore the clock speed can go as high as 10Mhz. This delay time is the dominant reason that slows the circuit speed. As you will see later, the rest of the ADC

circuitry functions in much higher speeds. Therefore increasing the switched capacitor amplifier speed increases the speed of the entire ADC.

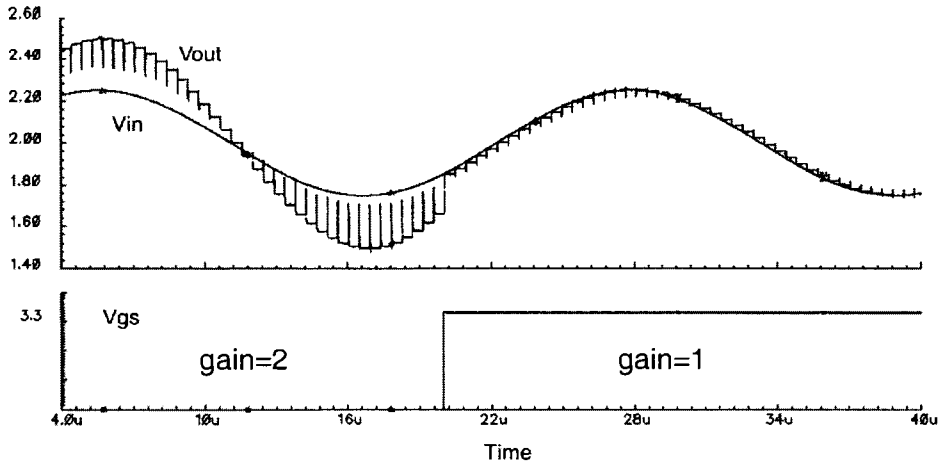


Figure 2.27: V_{gs} and I/O signals of the test circuit of Figure 2.23.

The layout design of the VGAs was done to achieve the minimum silicon area usage. One of the important issues was the ratio of feedback capacitors C_1 and C_2. For a precise ratio, matching between these two capacitors was done. Also to minimize the silicon area usage of all capacitors instead of using only two layers to create a capacitor, all layers from *Poly* to *Metal-5* were used so that in a smaller area a larger capacitor is generated, as shown previously in Figure 2.20. As a basic capacitor, a square shaped 0.25pF capacitor was designed. Then four of these capacitors where used for each 1pF capacitor. They are arranged in a common centroid manner and also dummy layers were put around them for best results. Figure 2.28 shows the dimensions of a 0.25pF capacitor and the matched C_1 and C_2 capacitors. Figure 2.29 shows the layout design of the entire switched capacitor circuit.

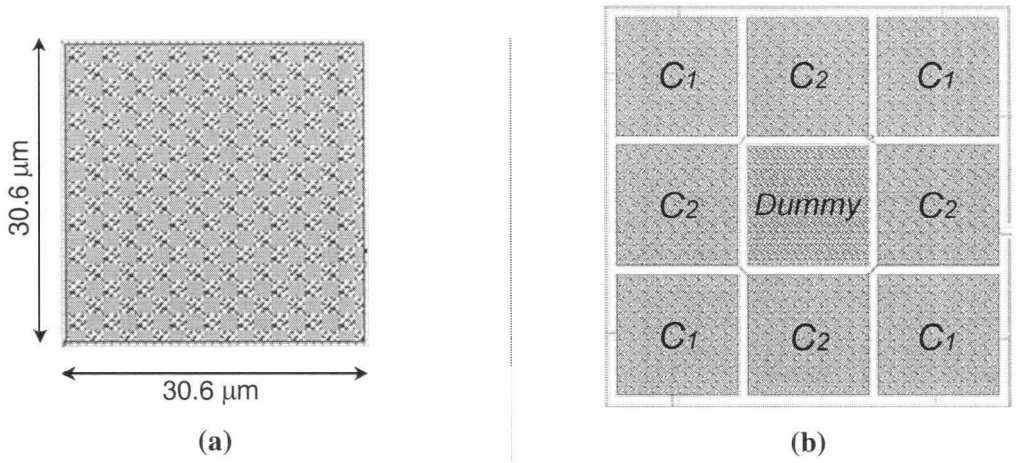


Figure 2.28: (a) Dimensions of a 0.25pF capacitor. (b) Matched C_1 and C_2 capacitors.

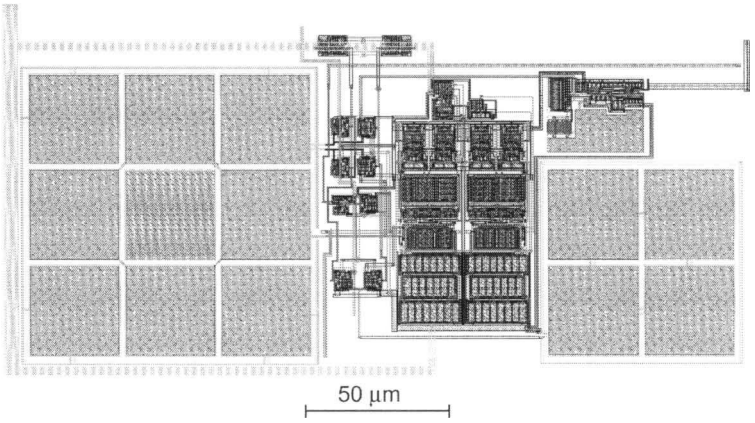


Figure 2.29: Layout of the entire switched-capacitor gain-of-2 VGA.

2.2.4.1 Gain-of-4 and Gain-of-16 Amplifiers

In the circuit of the ADC, there are two other kinds of SVGA (Small VGA), both feature two different gains: a low and a high gain. Both SVGAs have a low gain equal to one. But one has a high gain of four and the other one has a high gain of sixteen. Both these SVGAs are made of cascading the gain-of-2 VGA of Figure 2.23 because of a few reasons: first, amplifiers made of gain-of-2 VGAs in series have a higher bandwidth compared to a one-stage high-gain amplifier Because as shown in Figure 2.30, a one-stage high-gain amplifier has a low frequency pole, ω_2, that limits its bandwidth where a number of low-gain amplifiers in series have similar high frequency poles, ω_3.

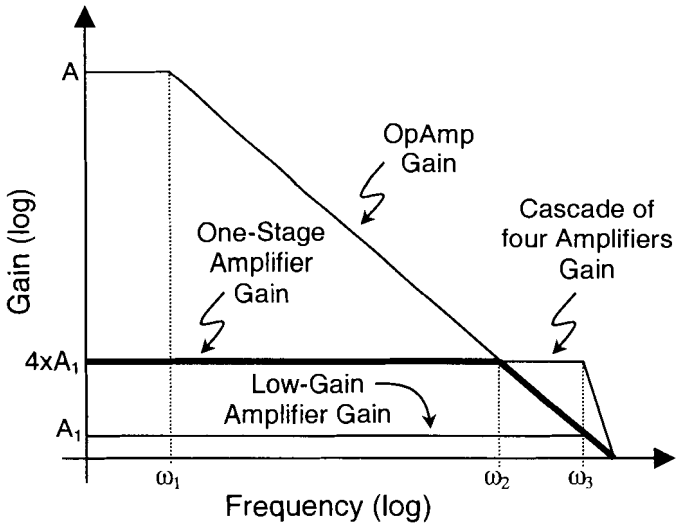


Figure 2.30: Comparison between bandwidth of different amplifier topologies.

Second, the total capacitance used to build switched capacitor amplifiers in the entire ADC circuit in the case of amplifiers in series is smaller than that of high gain amplifiers. Table 2.9 compares the value of total capacitances for these amplifiers.

Table 2.9: Comparison of total capacitor values for different amplifier topologies.

Kind of Amplifier	Capacitance Value for Amplifiers in Series	Capacitance Value for one High Gain Amplifier
Gain of Four	6pF	5pF
Gain of Sixteen	12pF	17pF

Referring to Figure 1.9 and Figure 1.11 that together show the general block diagram of the ADC, it is seen that the gain-of-16 amplifiers were used twice and the gain-of-4 amplifiers were used once in the entire ADC. This fact along with the data in Table 2.9 shows a 23% saving in the capacitor value. The silicon area used by a capacitor is proportional to the capacitor value. Therefore 23% saving means the same amount of saving in the layout area usage from the capacitor area point of view.

And third, the best matching between two capacitors can be done when they have equal values. Two equal capacitors can be broken into identical capacitor sections for matching. When

they are matched this way both will have very similar conditions and therefore very close values. In the gain of two amplifier of Figure 2.23 the gain is highly dependant on the ratio of C_1 and C_2. Therefore not only matching is necessary for these capacitors, but also it can be done perfectly due to their equal values (1pF). For a one-stage gain-of-16 amplifier, C_1 and C_2 would have values equal to 15pF and 1pF respectively. Assume that they are divided into 0.25pF subsections for matching. To achieve a common centroid model, an arrangement such as the one in Figure 2.31 can be used. It is obvious from the figure that the outer subsections of the 15pF capacitor shown with number 2 are very far from the ones of the 1pF capacitor shown with bold number 1 to have the same conditions. Therefore only a poor partial matching between these two capacitors can be done, which is not satisfactory for the required precision.

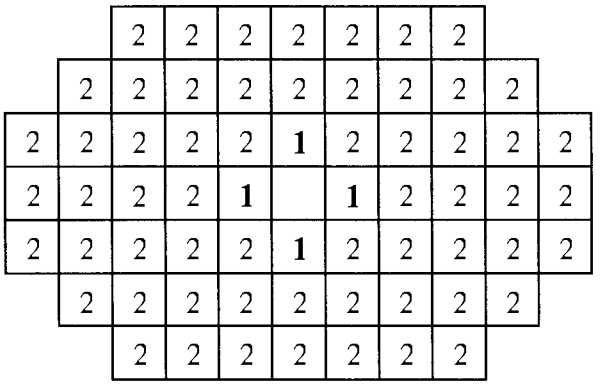


Figure 2.31: Matching between a 1pF and a 15pF capacitor.

The only disadvantage of using smaller amplifiers in series is that it increases the delay between when the input signal is sampled into the ADC to when the corresponding digital signal is produced, because simply the number of pipeline stages is increased. But it doesn't have any effect on the circuit speed and sampling rate will be the same.

Figure 2.32 shows a gain-of-4 VGA made of gain-of-2 amplifiers. When cascading the amplifiers, or more generally for the switched capacitor circuits of this project, it is very important to note the clock phase arrangement of the stages. All switched capacitor stages of the circuit use two non-overlapping clock phases. One phase resets the circuit and samples the signal

into the circuit and the other one processes the signal and sends it out. When cascading two stages, in the same clock phase when the signal is going out of the first stage, the second stage must be sampling the signal level using the same clock phase for the proper operation. Figure 2.33 shows this timing for two switched capacitor stages, where in every process box the same signal number stands for the process over the same input signal. Figure 2.34 shows the block diagram of a gain-of-16 VGA.

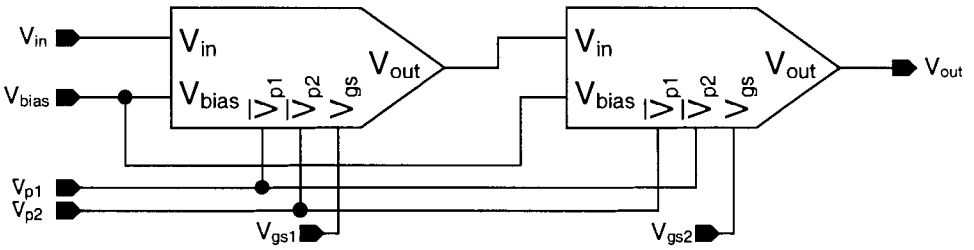


Figure 2.32: Diagram of a gain-of-4 VGA made of two cascading gain-of-2 VGAs.

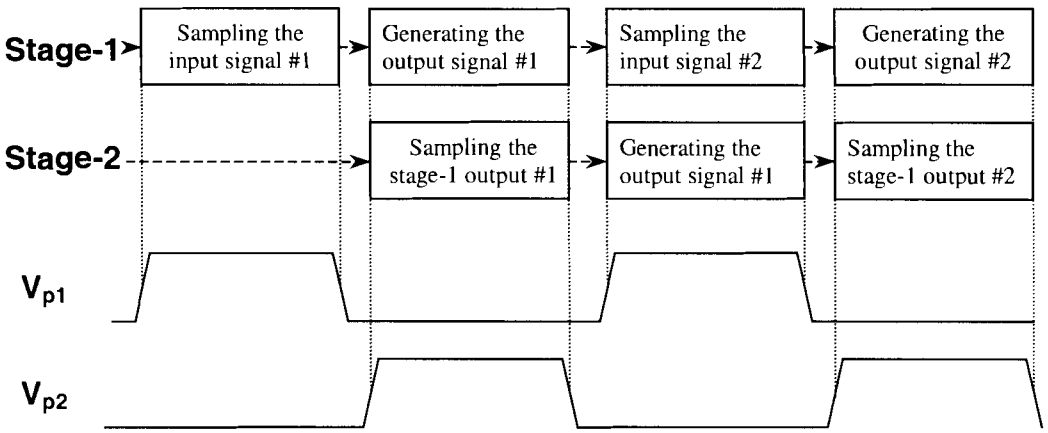


Figure 2.33: Timing arrangement of two switched capacitor stages in series.

As it can be seen from Figure 2.32, clock phase arrangement is reversed for every consecutive stage for the purpose mentioned. The V_{gs} signal for every stage is different. Remember that signal levels are processed in a pipeline manner and therefore, every stage of the amplifier can have a different gain suitable for the specific signal level it is carrying. But in other cases, if a constant gain amplifier is required, the V_{gs} signals of the stages are simply tied down to the ground.

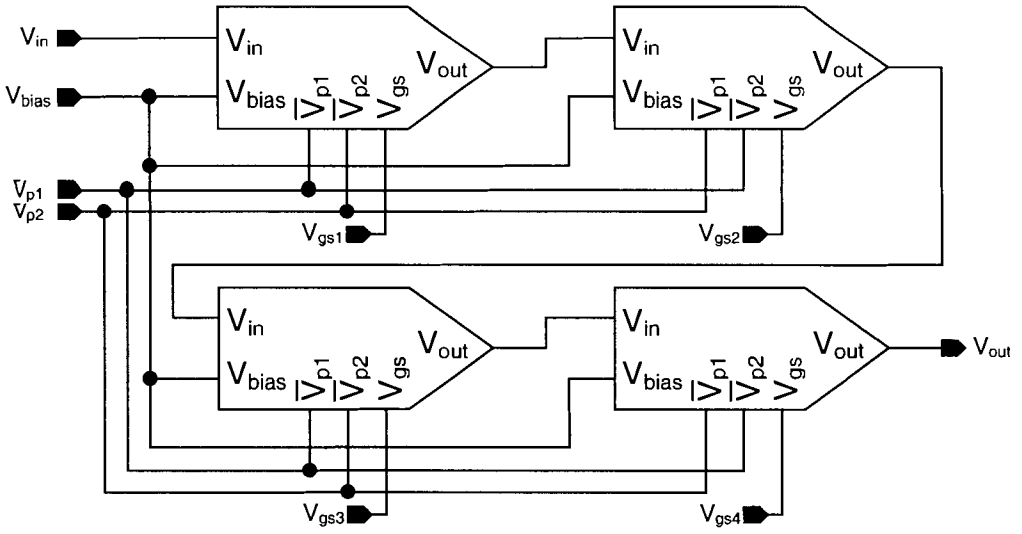


Figure 2.34: Block diagram of a gain-of-16 VGA.

Figure 2.35 shows the symbols that will be used for gain-of-4 and gain-of-16 amplifiers. In Figure 2.36 and Figure 2.37, the layouts of gain-of-4 and gain-of-16 VGAs made of gain-of-2 VGAs are demonstrated respectively.

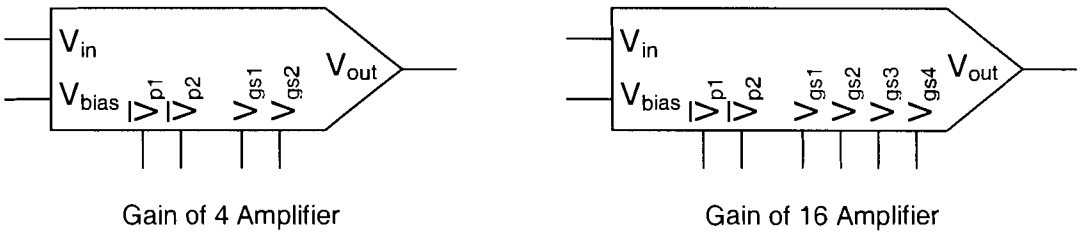


Figure 2.35: Symbols of gain-of-4 and gain-of-16 VGAs.

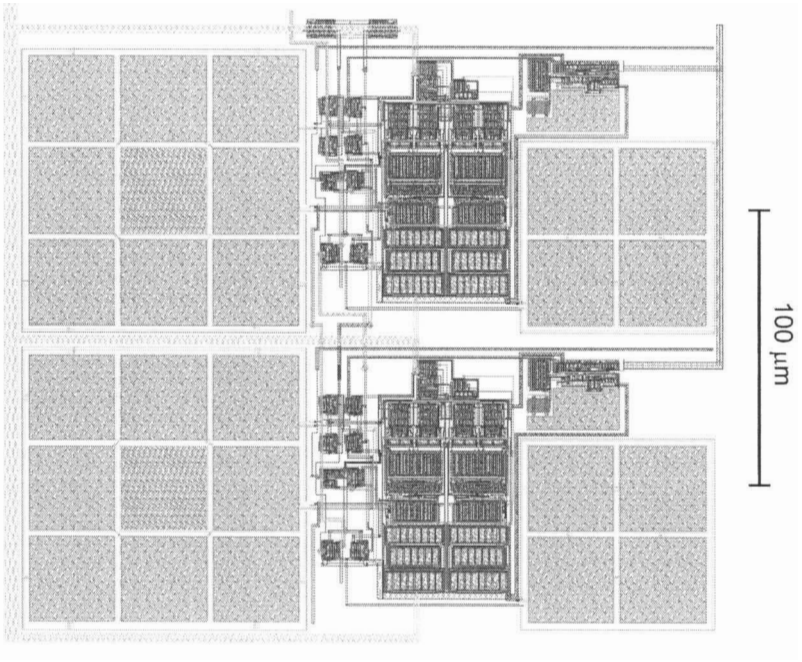


Figure 2.36: Layout of gain-of-4 VGA.

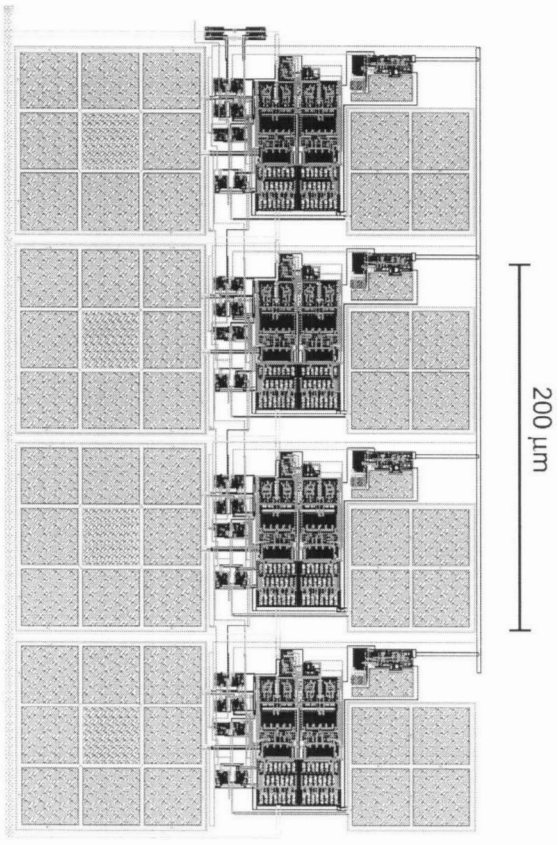


Figure 2.37: Layout of gain-of-16 VGA.

2.2.5 Switched Capacitor Subtracter

Figure 2.38 shows the schematic of a subtracter circuit using resistors. It has a circuit very similar to the amplifier discussed in the precious section. Only the equal input resistors R_3 and R_4 take two different input signals V_{in+} and $-V_{in-}$. Because the resistors are equal, the voltage on the OpAmp positive input is equal to $(V_{in+} - V_{in-})/2$. The rest of the amplifier has a gain of two ($R_1 = R_2$) and therefore the output signal of this stage is equal to $(V_{in+} - V_{in-})$. Here we assumed that the V_{in-} signal is already inverted. A similar circuit is used as a switched capacitor amplifier shown in Figure 2.39.

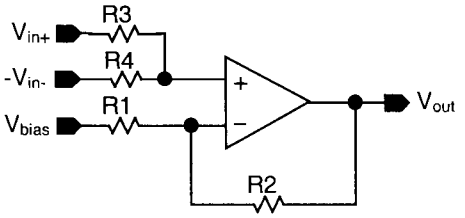


Figure 2.38: Schematic of a subtracter circuit using resistors.

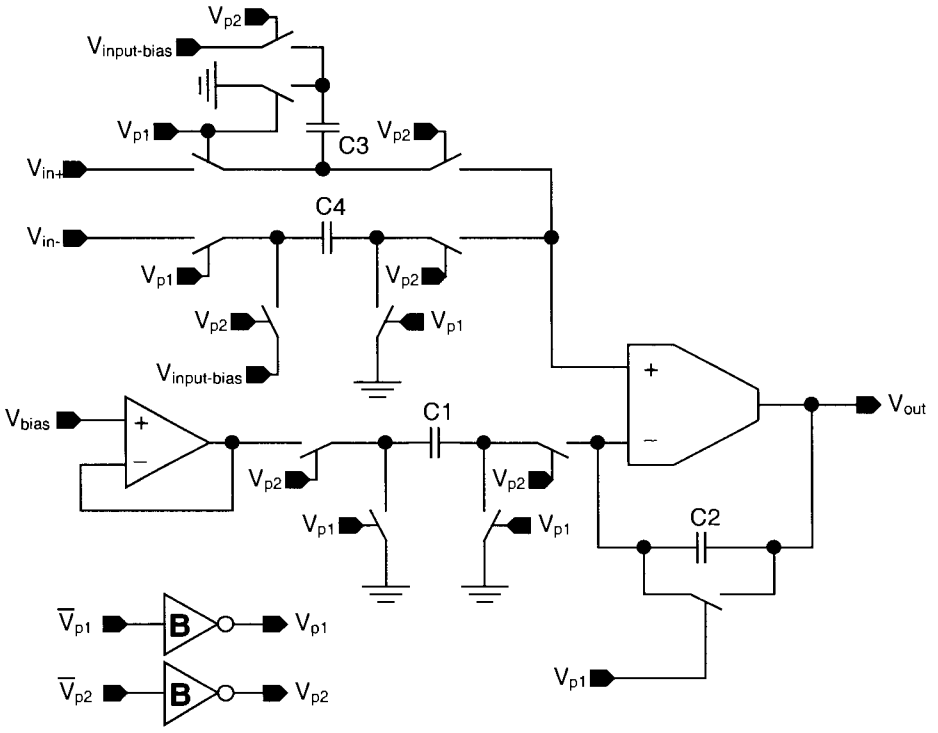


Figure 2.39: Switched capacitor implementation of the subtracter circuit of Figure 2.38.

The inputs to the circuit are V_{in+} and V_{in-} and an inverting switched capacitor circuit using C_4 inverts V_{in-} to make the subtraction process possible. The rest of the circuit is very similar to the VGA discussed in Section 2.2.4 and has a gain of two ($C_1 = C_2$). Only there is no *OR* gate or V_{gs} signal, because we want the gain to be always equal to two for the amplifier part of the subtracter. The equivalent capacitance values across two capacitors that sample the input signals are slightly different. This is caused due to different parasitic capacitors across these two capacitors. Therefore the subtraction will have some error. One can say that the non-inverting switched capacitor circuit of Figure 2.1-c could be used to cancel the parasitic elements and achieve similar switching behaviour. The problem with the circuit of Figure 2.1-c is that for the clock phase V_{p2}, the circuit is transparent and all the input changes of this circuit goes to its output. In contrast, the inverting switched capacitor circuit of Figure 2.1-b, also used in Figure 2.39, samples its input signal in a specific time. What we want is the subtraction of two signal levels from the same point in time. Using the circuit of Figure 2.1-c cancels the parasitic elements, but the subtraction result will be for signal levels from different points of time, which is wrong. Therefore instead of circuit of Figure 2.1-c, circuit of Figure 2.1-a is used so that both inputs are sampled in the same point of time. To cancel the effect of the parasitic capacitors, a very small capacitor $C_5 = 11fF$ (not shown in the schematic of Figure 2.39) is added parallel to C_4 so that there are equal total capacitances across both capacitors and the subtraction is done correctly. The *C3* and *C4* circuit is designed so that a biasing voltage, $V_{input\text{-}bias}$ is added to the voltage in the positive input of the OpAmp to bias the OpAmp for the correct operation.

Figure 2.40 shows the symbol used instead of the entire subtracter circuit and the test circuit used to test the subtracter. Same as the test circuit of Figure 2.26, the subtracter output is sampled over a capacitor and the simulation results are demonstrated in Figure 2.41. To test the subtracter as shown in Figure 2.40, square waves with different amplitudes are applied as input to

the subtracter. This is done to increase the visibility of subtraction operation in the final result of Figure 2.41.

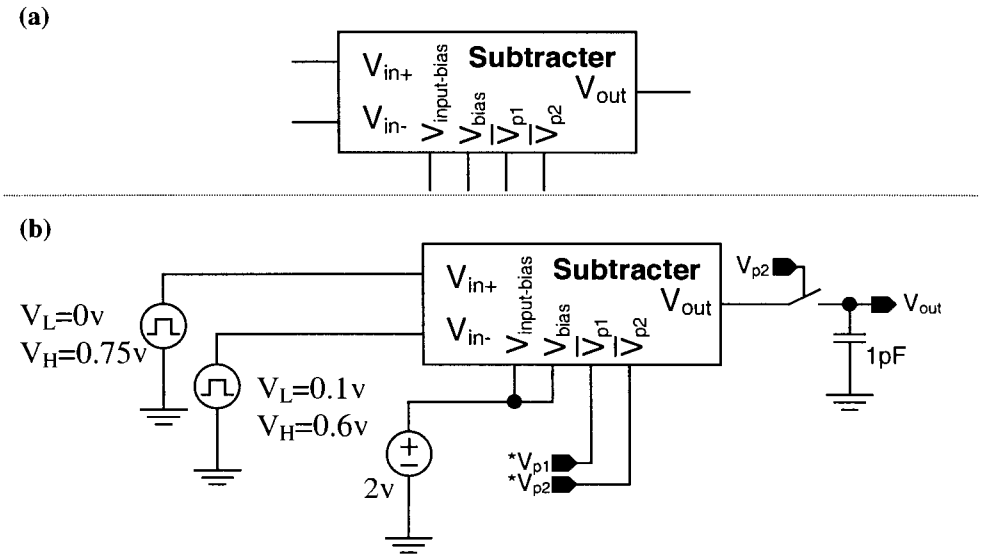


Figure 2.40: (a) Symbol of the subtracter circuit. (b) Test circuit of the subtracter.

In Figure 2.41 the output voltage level is the subtraction of input levels plus a 2V offset voltage and the subtracter output DC offset voltage. This offset is the same for all switched capacitor circuits and here is caused because $V_{input\text{-}bias}$ and V_{bias} are tied together. Later in Section 2.2.6 a special circuit is designed to eliminate the output DC offset of switched capacitor circuits. Also as you can see, there are different delays from when the inputs change to when the corresponding output is generated. The variable delay is due to the fact that the input signals are sampled during the high state of V_{p1}. Therefore depending on the point when the input change is happened within or outside this state, the delay can be different. For the layout design of the subtracter circuit, same cautions as the layout of the VGA circuit were considered. Another capacitor matching between C_3 and C_4 capacitors was done in the same way as mentioned for the VGA layout design to achieve the best results. Figure 2.42 shows the layout of the entire subtracter circuit.

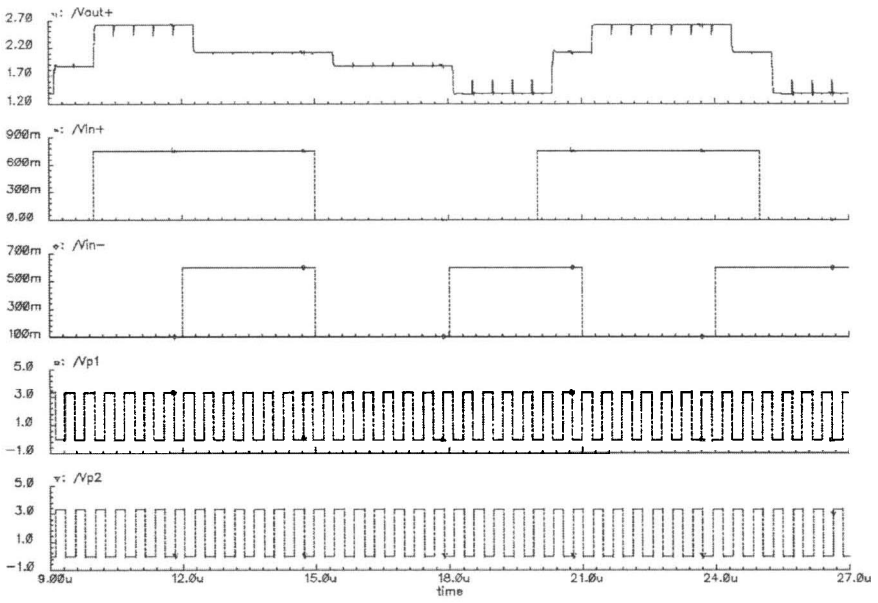


Figure 2.41: Simulation results of the switched-capacitor subtracter.

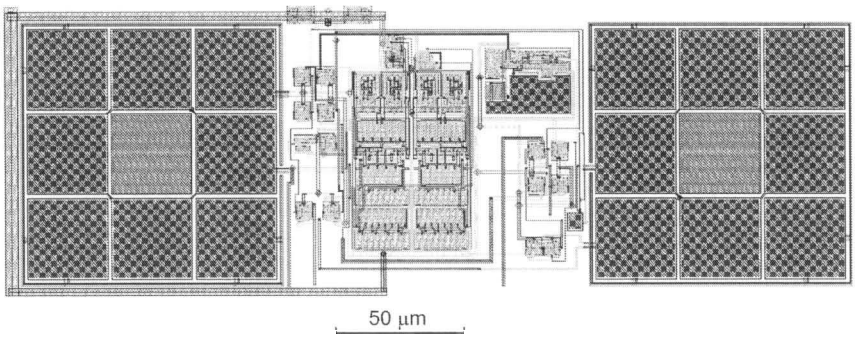


Figure 2.42: Layout of the entire subtracter circuit.

2.2.6 V_{bias} Voltage Level Generator

Because the chip is designed to have zero and 3.3v as its power supply, all the analog signals have to be biased over a DC voltage so that they are in the operating range of the analog circuits. This DC biasing voltage is added to all the sampled voltage levels inside the circuits.

There is a problem in the designed switched capacitor circuits, and that is a very small output DC offset voltage. The value of this output voltage is about 26mV. It seems like a very small voltage error, but it gets amplified and accumulated through many switched-capacitor amplifier stages in the ADC to a point where the analog signal level is completely useless.

Therefore eliminating this output offset is essential for the correct operation of the ADC. The schematic of a gain-of-2 VGA is repeated in Figure 2.43 for your convenience.

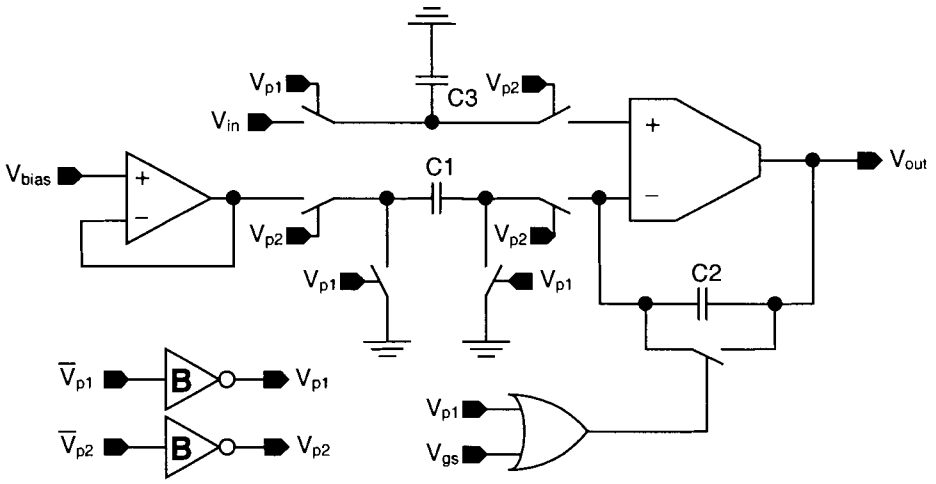


Figure 2.43: Schematic of a gain-of-2 VGA circuit.

If you look in the schematic of Figure 2.43, you can see that the best way to eliminate this offset voltage is to provide a V_{bias} voltage slightly different than the input DC biasing voltage so that the input and output have the same biasing voltages. In such circuit a change in V_{bias} is reflected to the output with a negative gain of one. Therefore, if for V_{bias} equal to the input biasing voltage the output is off by -2.6mV, it is sufficient to apply a voltage equal to (V_{bias} + 2.6mV) instead to correct the output. Because the switched-capacitor circuits of the ADC are similar, the same compensated V_{bias} voltage corrects the offset voltage of the entire circuit. To provide the exact V_{bias} a special circuit is designed. Figure 2.44 shows the schematic of this circuit.

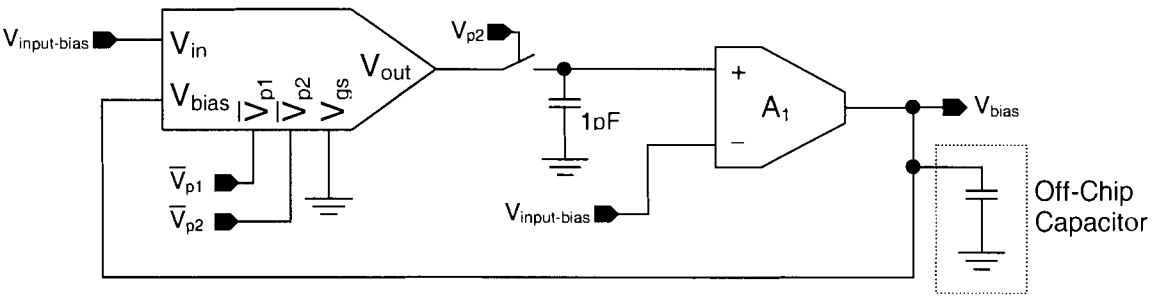


Figure 2.44: Schematic of the V_{bias} voltage generator circuit.

It is required to make the output DC voltage of a gain-of-2 VGA to be equal to its input DC voltage. To make the input and output bias voltages equal, OpAmp A_1 in a negative feedback mode is used as shown in Figure 2.44. In a negative feedback, two inputs of an OpAmp will have the same voltage. As you can see in Figure 2.44, the negative feedback includes a gain-of-2 amplifier. The desired biasing voltage, $V_{input\text{-}bias}$ is applied to both gain-of-2 amplifier and the A_1 OpAmp. The output of the gain-of-2 amplifier is sampled over a 1pF capacitor to eliminate the existing ripples over the output of this amplifier. The output of the OpAmp, V_{bias}, will change to a voltage so that the output of the gain-of-2 amplifier has the same value as $V_{input\text{-}bias}$. Therefore the V_{bias} voltage is the suitable voltage to bias all the switched capacitor stages and eliminate their output DC offset. To test this circuit, a 2V input as the $V_{input\text{-}bias}$ voltage was applied to the circuit. Simulation shows that in this circuit V_{bias} will have a value equal to 2.026V. The signals to the negative input of the switched capacitor amplifier will go out by a gain of one. Therefore a 26mV increase in the biasing voltage causes the output to reduce by 26mV and become the desired 2V voltage. This is why the test shows a V_{bias} equal 2.026V. Figure 2.45 shows the layout of the V_{bias} voltage generator circuit.

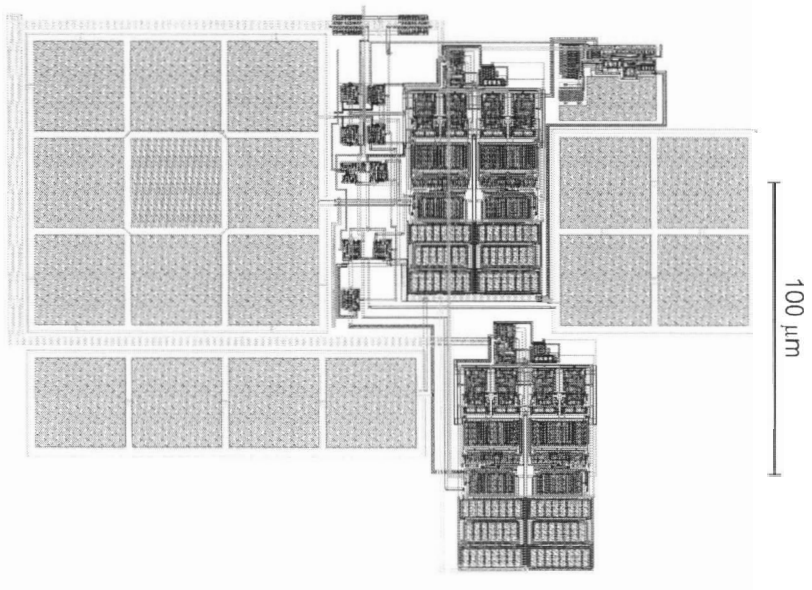


Figure 2.45: Layout of the V_{bias} voltage generator circuit.

2.3 Digital Circuits

There are a number of different basic digital circuits used in this project such as *AND* gates, *OR* gates or inverters and a few larger digital circuits are designed using this basic gates such as flip-flops and encoders. Compared to the clock speed of the switched-capacitor circuits, digital circuits designed for this project have very high speeds and very small delays. Therefore they are not considered as bottlenecks for the ADC speed and do not require special topologies. Usage of some of these gates such as inverter and *OR* gates has already been discussed for switched-capacitor circuits. In this section, the circuit and layout design of the digital circuitry used in the ADC along with their properties are discussed.

2.3.1 Inverters

An inverter has the simplest circuit. There are two different inverters used in this project. One is a simple low current one that is used among the digital circuitry and the other one is a high output current inverter, which is used especially to buffer the clock phases going to the switched-capacitor circuits, such as the ones shown in Figure 2.23. Figure 2.46 shows schematics and symbols of these inverters.

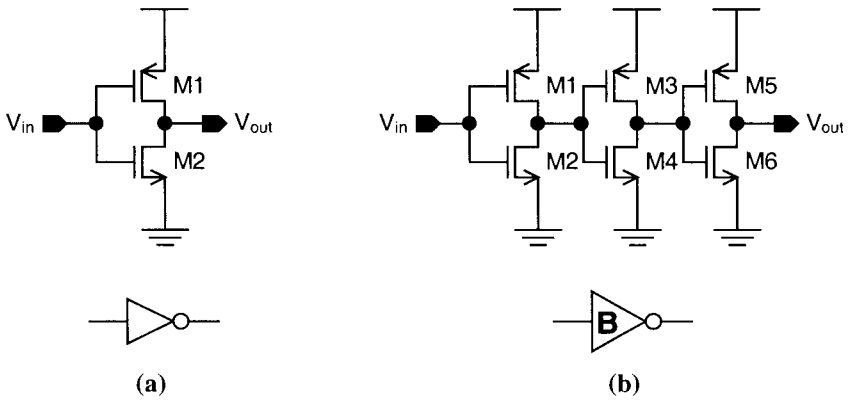


Figure 2.46: (a) schematic and symbol of the low current inverter and (b) schematic and symbol of the high current inverter.

As you can see in this figure, for the high current inverter three inverter stages are used instead of one. Such a topology allows the gradual current increase for each inverter stage.

Therefore a much smaller input capacitance is achieved for such an inverter compared to a one-stage high-current inverter. This increases the speed of digital circuits where small input capacitance and high output current is required. Table 2.10 provides transistor parameter values.

Table 2.10: Transistors width and length for both inverters.

Transistor Names	Low Current Inverter		High Current Inverter	
	Width	Length	Width	Length
M1	1.5 μm	350 nm	1.3 μm	300 nm
M2	0.8 μm	350 nm	0.5 μm	350 nm
M3			2.6 μm	300 nm
M4			1 μm	350 nm
M5			13 μm	300 nm
M6			5 μm	350 nm

Figure 2.47 demonstrates timing parameters in a digital circuit in general. t_{phl} and t_{plh} stand for propagation delay from the input to the corresponding output when output changes from high to low and low to high respectively. t_r stands for the output rise time and t_f stands for the output fall time. These parameters are measured using post layout simulations for both kind of inverters and are brought in Table 2.11. To test the inverters, a 50fF load capacitor is used for the low current inverter and a 1pF load capacitor is used for the high current inverter.

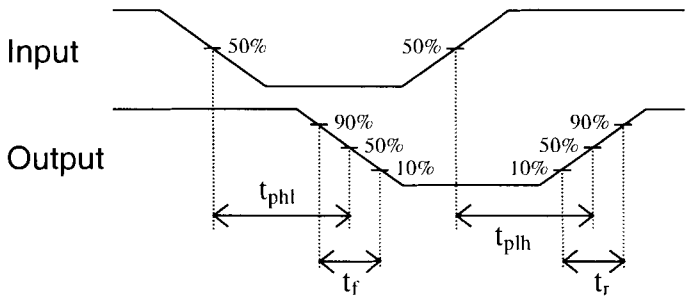


Figure 2.47: Digital circuit timings.

Table 2.11: Timings for both inverters.

Parameters	Simple Inverter	Buffer Inverter
t_{phl}	190 ps	1 ns
t_{plh}	270 ps	1 ns
t_r	545 ps	660 ps
t_f	340 ps	770 ps

In the layout design of digital circuits, the transistor matching is not as critical as it is in analog circuits. It is only done to reduce the drain and source parasitic capacitor values and to reduce the area used by the circuit on one or more transistors that share their drain or source.

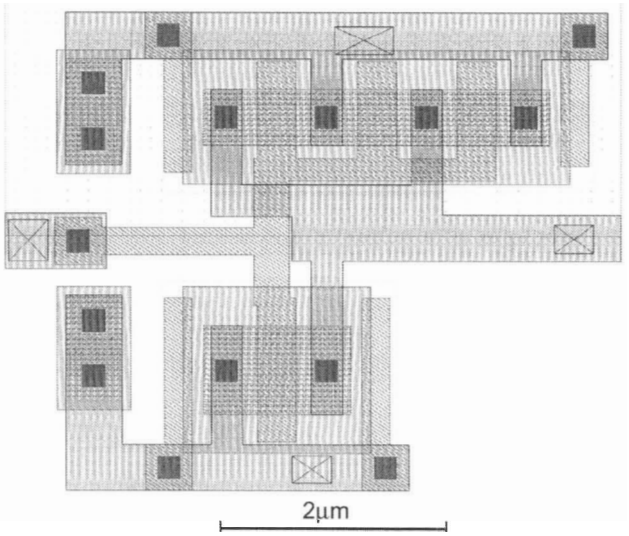


Figure 2.48: Low current inverter layout.

Common centroid matching is not used here to achieve a better transistor arrangement. Layouts of these inverters are shown in Figure 2.48 and Figure 2.49.

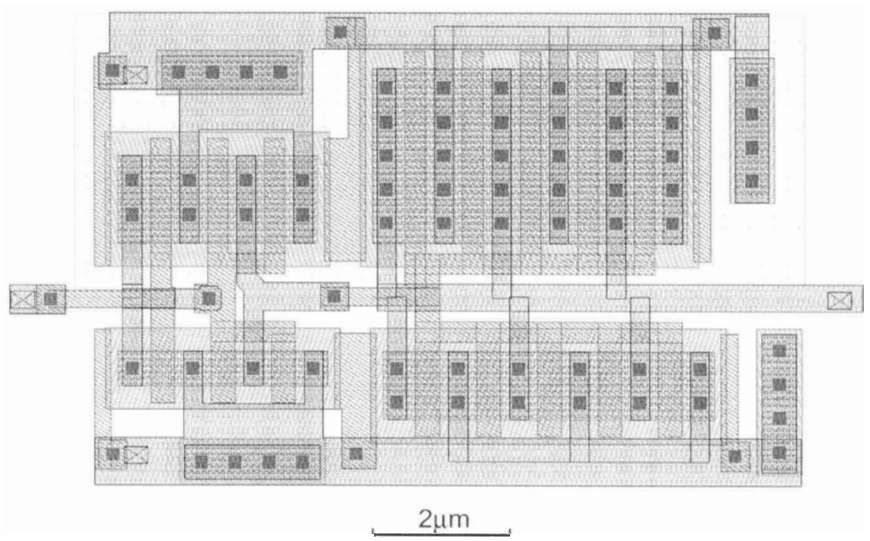


Figure 2.49: High current inverter layout.

2.3.2 Logical *AND* and *NAND* Gates

The *AND* and *NAND* gates used in the ADC are all two input gates. Figure 2.50 shows the schematic and the symbol of both these gates.

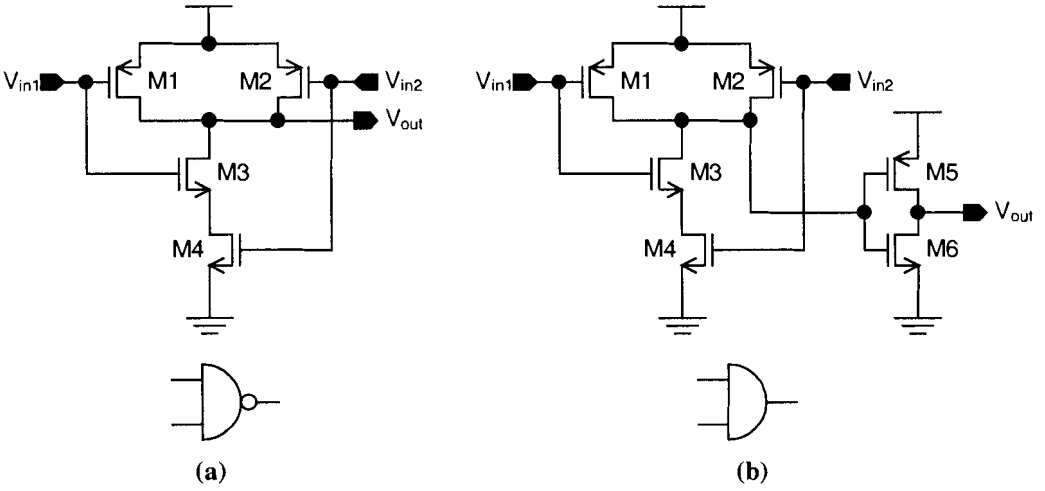


Figure 2.50: (a) Schematic and symbol of the *NAND* gate. (b) Schematic and symbol of the *AND* gate.

Table 2.12: Transistor parameters for *NAND* and *AND* gates.

Transistor Names	*NAND* gate		*AND* gate	
	Width	Length	Width	Length
M1	0.5 μm	350 nm	0.5 μm	350 nm
M2	0.5 μm	350 nm	0.5 μm	350 nm
M3	1 μm	350 nm	1 μm	350 nm
M4	1 μm	350 nm	1 μm	350 nm
M5			1.5 μm	350 nm
M6			0.5 μm	350 nm

As it can be seen from Figure 2.50, the *AND* gate uses the same circuit as the *NAND* gate, only one inverter circuit is added as its output stage. These gates are tested using a 50fF load capacitor. This load is higher than the input capacitor of the general digital CMOS circuits. Therefore used in actual circuits, these gates can demonstrate even higher speeds. Table 2.12 shows the transistor parameters for both gates and Table 2.13 summarises the timings for both these gates. Figure 2.51 and Figure 2.52 show the layout of the *NAND* gate and the *AND* gate respectively.

Table 2.13: Timings for *NAND* and *AND* gates.

Parameters	*NAND* Gate	*AND* Gate
t_{phl}	430 ps	530 ps
t_{plh}	1.6 ns	550 ps
t_r	790 ps	300 ps
t_f	220 ps	430 ps

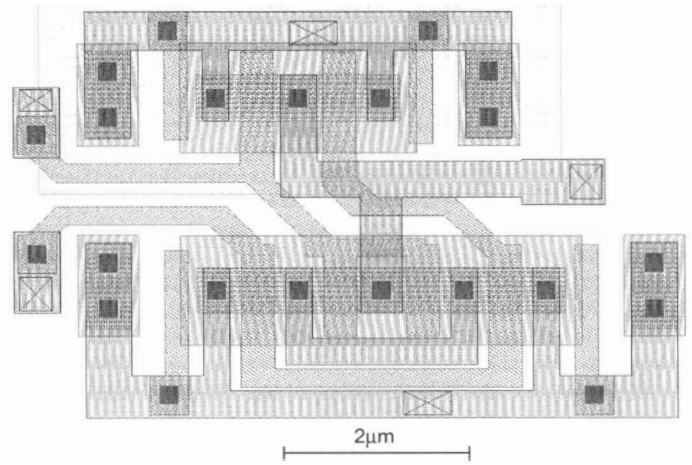


Figure 2.51: Layout of the *NAND* gate.

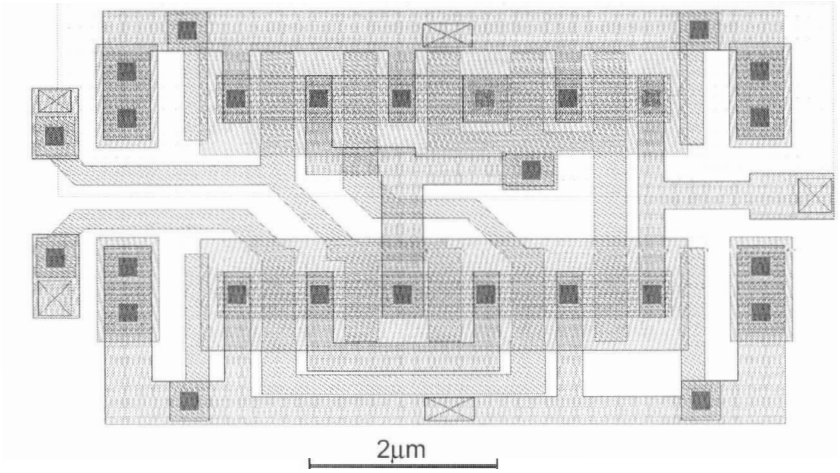


Figure 2.52: Layout of the *AND* gate.

2.3.3 Logical *OR* Gates

In the circuits of the ADC presented in this project, two kinds of *OR* gates are used: two and four input *OR* gates. Their circuits are the same as a *NOR* gate with an inverter circuit added

as their output stage. But because no *NOR* gates are used in the ADC, here I only concentrate on the *OR* gates. Figure 2.53 shows the schematic and the symbol of both kinds of *OR* gates.

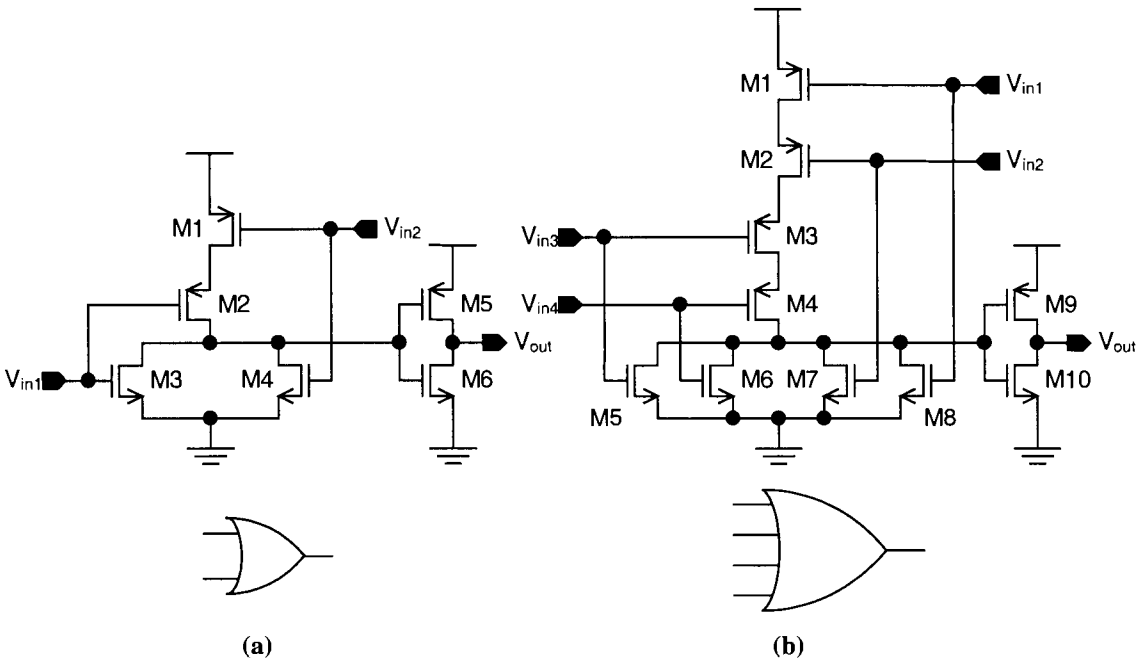


Figure 2.53: (a) Schematic and symbol of the two input *OR* gate. (b) Schematic and symbol of the four input *OR* gate.

Table 2.14 summaries the gates transistor parameters. Again, using the 50fF load capacitors, timings of both *OR* gates are measured using post layout simulations and the results are brought in Table 2.15. The layouts of the gates are shown in Figure 2.54 and Figure 2.55.

Table 2.14: Transistor parameters for two and four input *OR* gates.

Transistor Names	Two Input *OR* Gate		Four Input *OR* Gate	
	Width	Length	Width	Length
M1	1 μm	300 nm	1 μm	350 nm
M2	1 μm	300 nm	1 μm	350 nm
M3	0.5 μm	350 nm	1 μm	350 nm
M4	0.5 μm	350 nm	1 μm	350 nm
M5	1.5 μm	300 nm	0.5 μm	350 nm
M6	0.5 μm	350 nm	0.5 μm	350 nm
M7			0.5 μm	350 nm
M8			0.5 μm	350 nm
M9			1.5 μm	350 nm
M10			0.5 μm	350 nm

Table 2.15: Timings of both *OR* gates.

Parameters	Two Input *OR* Gate	Four Input *OR* Gate
t_{phl}	415 ps	676 ps
t_{plh}	283 ps	450 ps
t_r	470 ps	552 ps
t_f	530 ps	595 ps

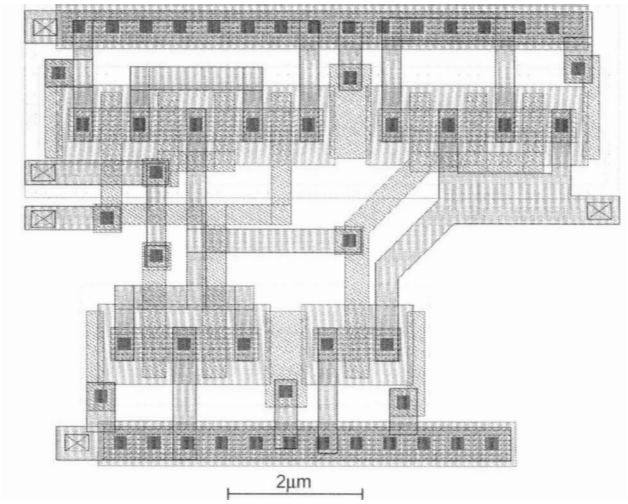


Figure 2.54: Layout of the two-input *OR* gate.

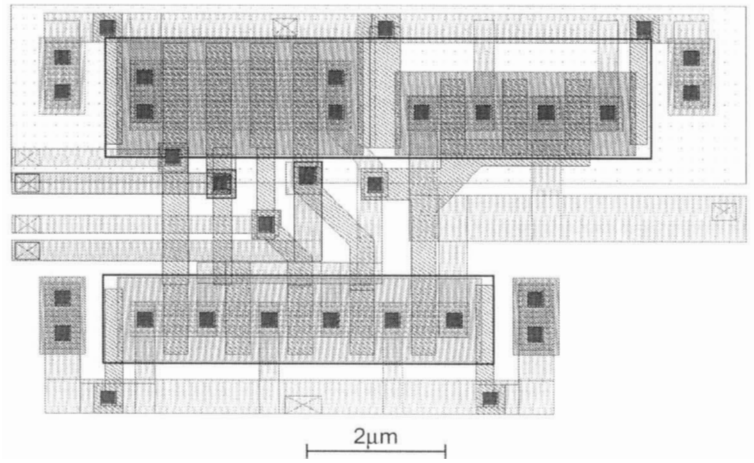


Figure 2.55: Layout of the four-input *OR* gate.

2.3.4 D-Flip-Flop

Using the above gates, an edge triggered d-flip-flop is designed. Figure 2.56 shows the schematic of an edge-triggered d-flip-flop and its symbol. In this flip-flop, on the rising edge of

the clock pulse C, the input signal D is sampled to the output Q. $\overline{Q}$ is the inversion of Q. $\overline{Q}$ signal is not used in this circuit and that's why it doesn't appear in the flip-flop symbol.

Table 2.16 summarises the flip-flop characteristics using the post layout simulation measurements. A 50fF load capacitor is used.

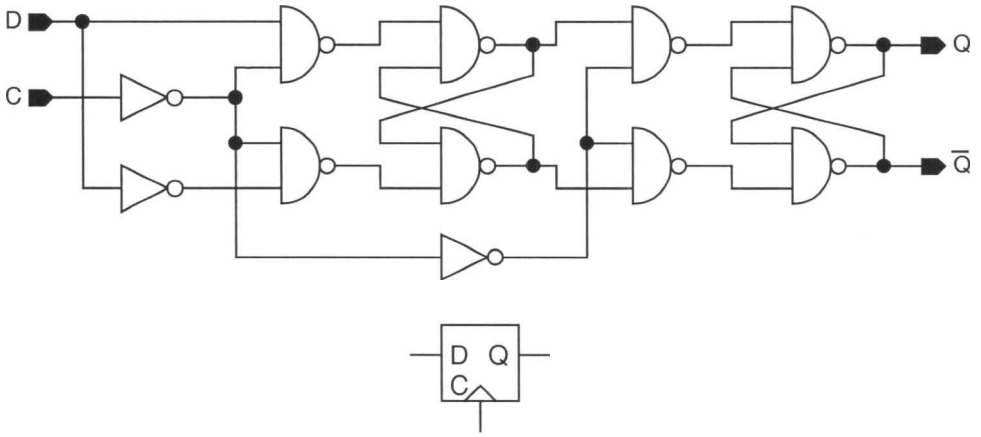


Figure 2.56: Schematic and symbol of an edge triggered d-flip-flop.

Table 2.16: Timings of the flip-flop.

Parameters	Value
t_{phl}	523 ps
t_{plh}	950 ps
t_r	1.15 ns
t_f	460 ps

For the layout design of the flip-flop, the layouts of gates were put together in a way to achieve the smallest area possible. Final layout of the flip-flop is brought in Figure 2.57.

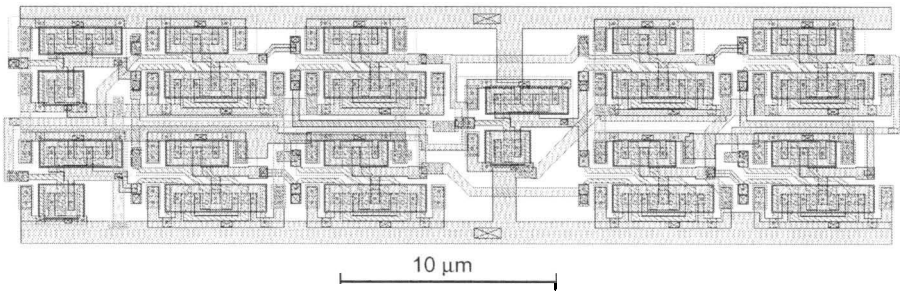


Figure 2.57: Layout of the flip-flop.

2.3.5 Clock Generator

The clock generator circuit is responsible for generating the inverted of the two clock phases used in the circuit, $\overline{V}_{p1}$ and $\overline{V}_{p2}$. These clock phases are buffered and used throughout the circuit using the high current inverter buffer discussed in Section 2.3.1. To generate a clock, first step done in this project was to use an Schmitt-triggered inverter. Adding a resistor parallel to the Schmitt-triggered inverter and a capacitor from its input to the ground causes this inverter to oscillate. Figure 2.58 shows the schematic of the entire clock generator circuit. Transistors M1 to M6 together make CMOS Schmitt-triggered inverter designed for the clock generator. After using this Schmitt-triggered inverter, its output is buffered through an inverter made of M7 and M8 transistors. The non-overlapping clock phases are generated using the circuit implemented after this inverter in Figure 2.58. As you can see from this figure, a 0.5pF capacitor is added to the output of the inverter. This capacitor slows the clock edges down. This is helpful to make a time distance between the clock phase edges to get suitable non-overlapping time.

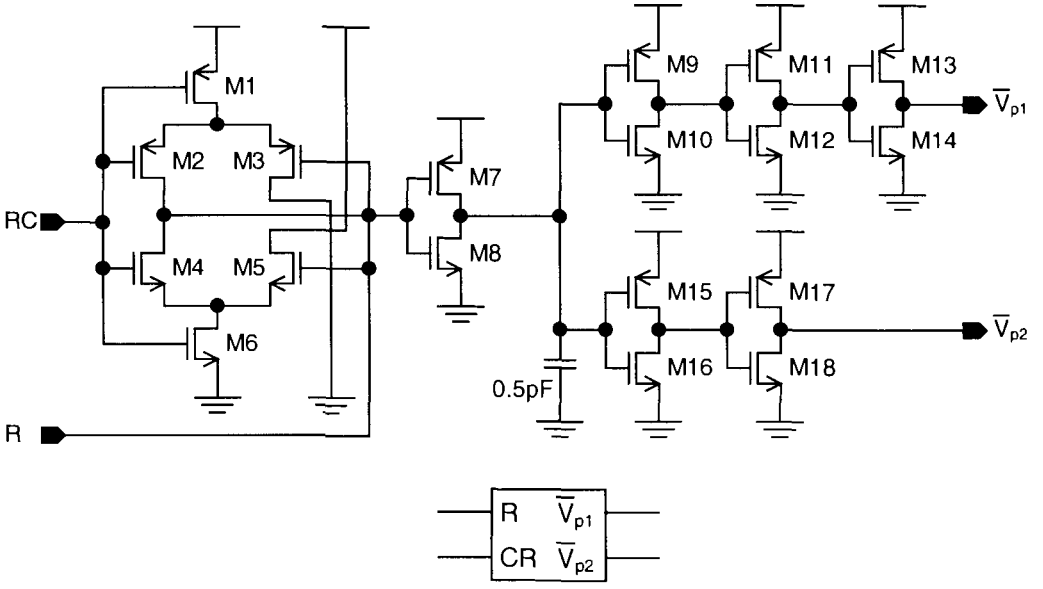


Figure 2.58: Schematic of the entire clock generator circuit and its symbol.

This signal first goes to imbalanced inverters. For the upper imbalanced inverter made of M9 and M10 transistors, the input threshold voltage is high. For the lower imbalanced inverter

made of M15 and M16 transistors, the input threshold voltage is low. Therefore their outputs change in different points of time for different voltage levels coming to their inputs. As shown in Figure 2.59, external resistor and capacitor are connected to the clock generator circuit to make it oscillate and generate the desired clock phases.

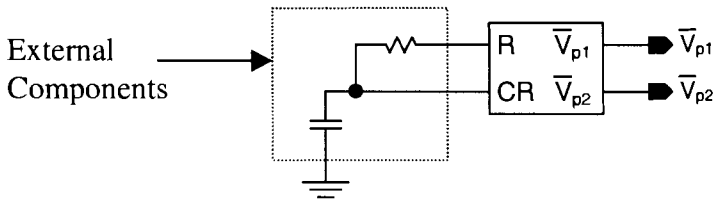


Figure 2.59: Schematic of the clock circuit using external resistor and capacitor.

Figure 2.60 shows the output of the Schmitt-triggered inverter and the imbalanced inverters. As seen in this figure, the circuit results in a 2 ns distance between the edges as a non-overlapping time.

Table 2.17: Transistor parameters of the clock generator circuit.

Clock Generator Circuit					
Names	Width	Length	Names	Width	Length
M1	1.3 μm	300 nm	M10	0.5 μm	350 nm
M2	1.3 μm	300 nm	M11	1.3 μm	300 nm
M3	1.3 μm	300 nm	M12	0.5 μm	350 nm
M4	0.5 μm	350 nm	M13	1.3 μm	300 nm
M5	0.5 μm	350 nm	M14	0.5 μm	350 nm
M6	0.5 μm	350 nm	M15	0.8 μm	300 nm
M7	1.3 μm	300 nm	M16	1 μm	350 nm
M8	0.5 μm	350 nm	M17	1.3 μm	300 nm
M9	9 μm	300 nm	M18	0.5 μm	350 nm

Having two clock pulses that have non-overlapping edges, we can generate non-overlapping clock phases. As shown in the schematic of Figure 2.58, a number of inverters are added after the imbalanced inverters to sharpen the clock edges and generate $\overline{V}_{p1}$ and $\overline{V}_{p2}$ pulses. Figure 2.61 shows these clock pulses along with their inversions, V_{p1} and V_{p2} for a frequency of about 33.5MHz. Also in the same figure the voltage of the pin R, the Schmitt-triggered inverter output, is included to show the relevance of the output pulses to this signal.

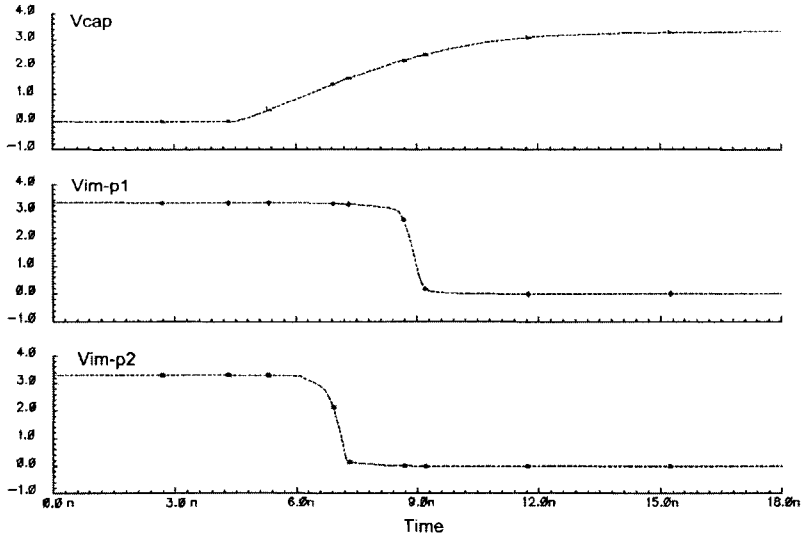


Figure 2.60: Output of the buffer inverter and the imbalanced inverters.

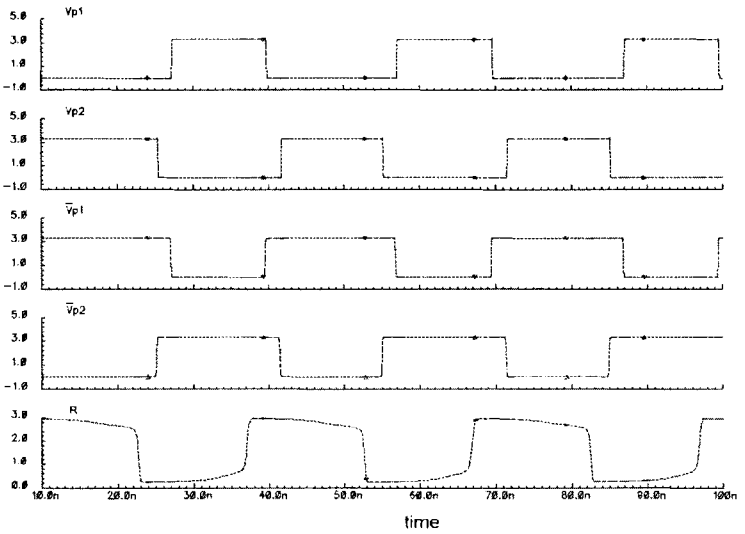


Figure 2.61: Clock phases generated using the clock generator circuit and their inversions.

Different combination of resistor and capacitor values can be used on the Schmitt-triggered inverter to generate different frequencies. Formula 2.3 can be used to calculate the frequency resulted from using different *R* and *C* values.

$$F \approx 1/(2RC) \qquad (2.3)$$

The layout of the clock generator circuit excluding the capacitor is shown in Figure 2.62 and the layout of the entire clock generator circuit is shown in Figure 2.63. As it is obvious from this figure, the 0.5pF capacitor takes a large area of the circuit.

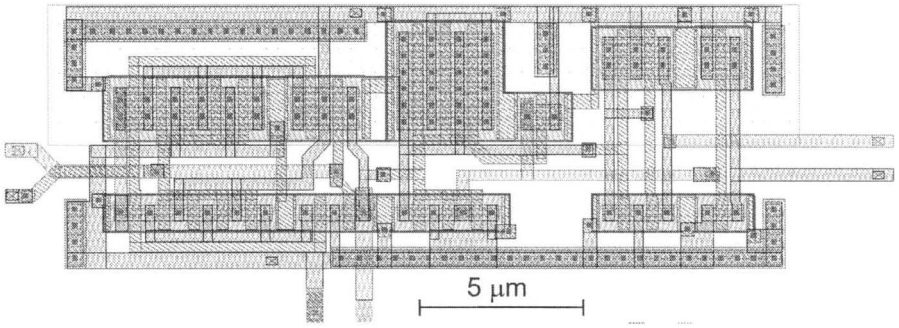


Figure 2.62: Layout of the clock generator circuit excluding the capacitor.

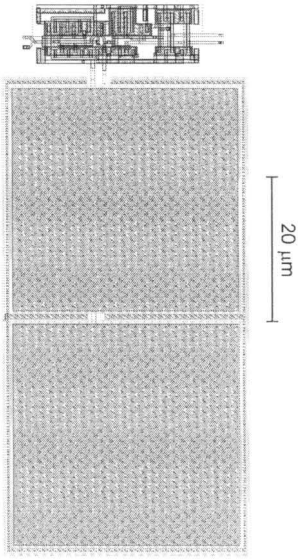


Figure 2.63: Layout of the entire clock generator circuit.

2.3.6 Encoders

Encoders are one of the components used in flash ADCs. As shown in Figure 1.8 in Section 1.3.1, the final stage of a flash ADC after the comparators is the encoder. There are two different flash ADCs used in this project. First one is a non-linear 3-bit flash ADC, which requires a 7-to-3-bit encoder and the other one is a linear 4-bit flash ADC, which requires a 15-to-4-bit encoder. Table 2.18 shows the truth table of a 7-to-3-bit encoder and Table 2.19 shows the

truth table of a 15-to-4-bit encoder. All a_n bits are inputs and all b_n bits are outputs in the tables below. In these tables, all inputs up to a point are one and the rest are zero. This is explainable knowing that these inputs come from the comparators of a flash ADC as described in Section 2.4.

Table 2.18: Truth table of a 7-to-3-bit encoder.

a_0	a_1	a_2	a_3	a_4	a_5	a_6	b_0	b_1	b_2
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	1	1
1	1	1	1	0	0	0	1	0	0
1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1	1	1

Table 2.19: Truth table of a 15-to-4-bit encoder.

a_0	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8	a_9	a_{10}	a_{11}	a_{12}	a_{13}	a_{14}	b_0	b_1	b_2	b_3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The digital circuit for encoders are designed using the pre-designed gates and their schematics are shown in Figure 2.64 and Figure 2.66. Table 2.20 summarises the properties and finally Figure 2.65 and Figure 2.67 demonstrate the layout of both encoders.

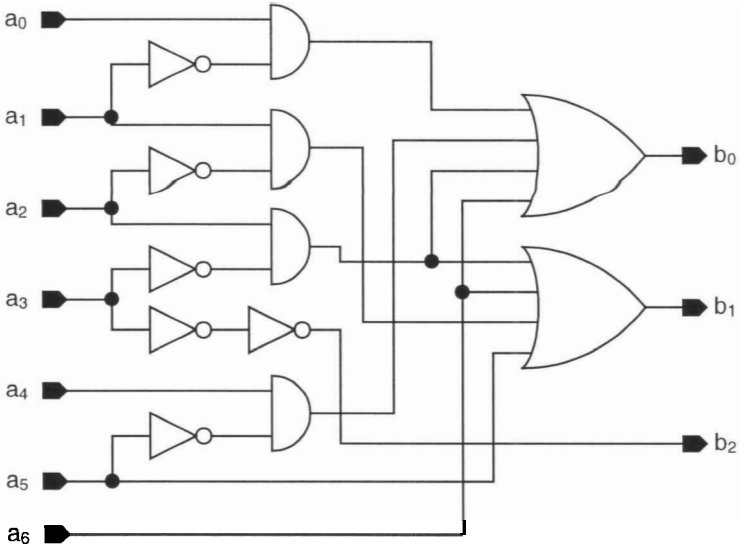


Figure 2.64: Schematic of the 7-to-3-bit encoder.

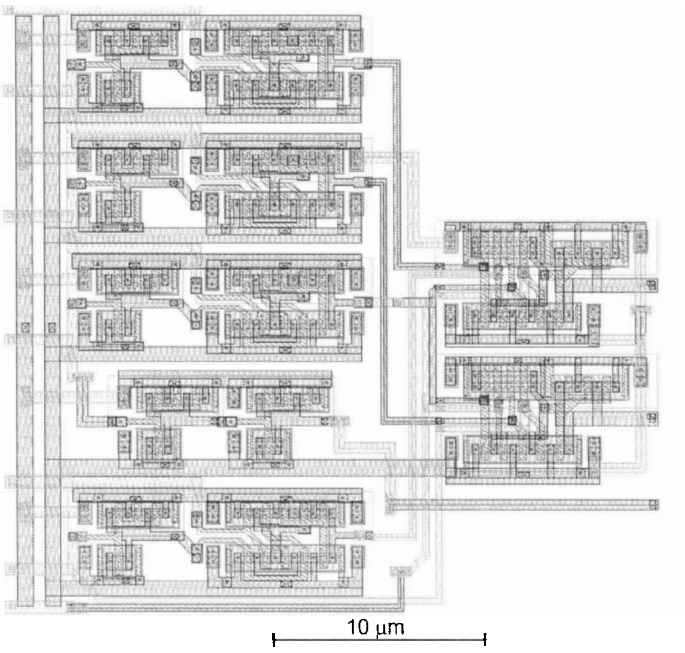


Figure 2.65: Layout of the 7-to-3-bit encoder.

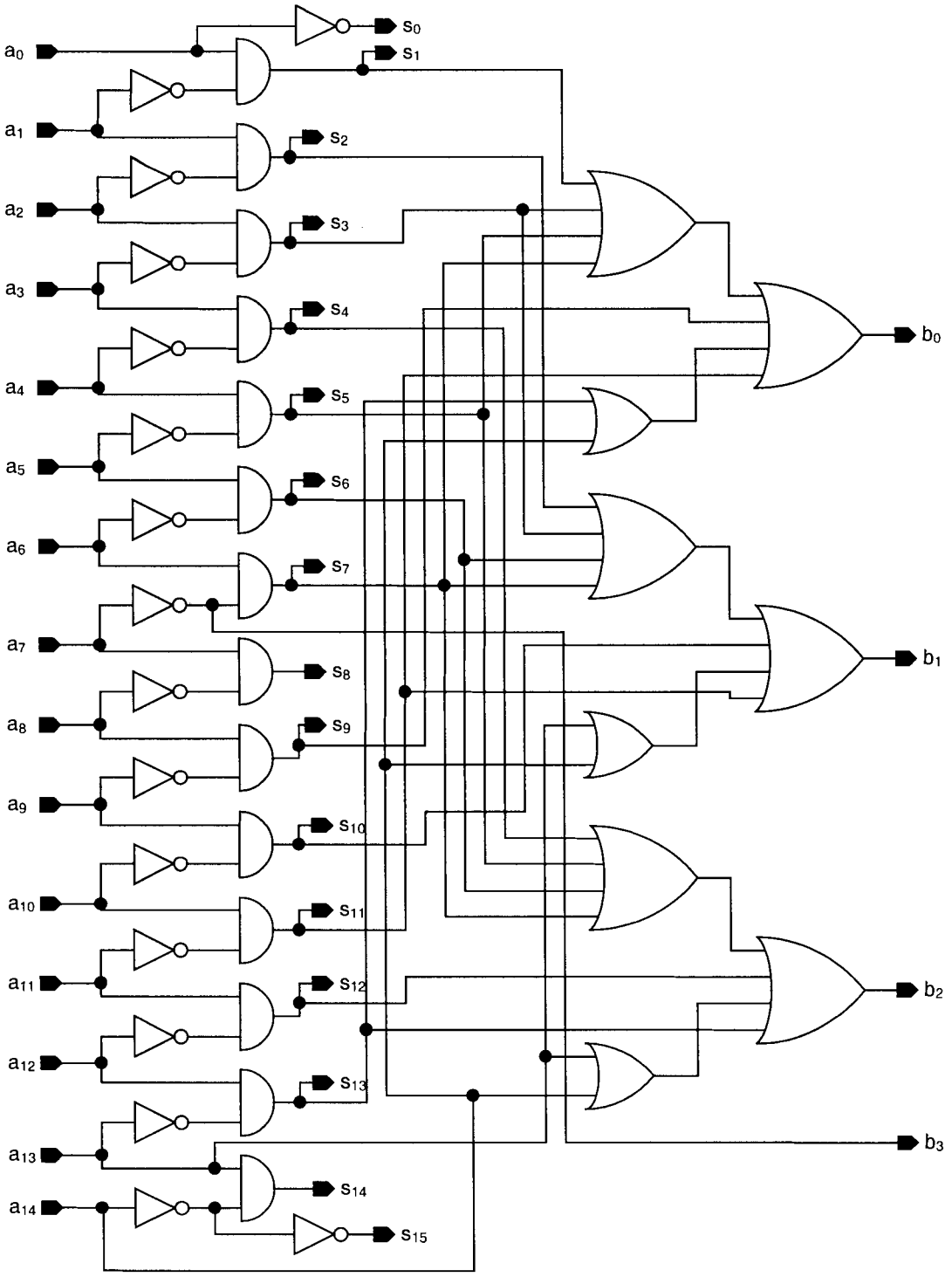


Figure 2.66: Schematic of the 15-to-4-bit encoder.

In Figure 2.66 there are sixteen S_n signals inside the 15-to-4-bit encoder circuit. These signals are later used to combine the ADC and DAC circuits together in Section 2.5. S_0 is a

logical one whenever a_0 is a logical zero. S_{15} is a logical one whenever a_{14} is a logical one and the rest of S_n signals are a logical one whenever a_{n-1} input is a logical one and a_n input is a logical zero. Knowing the formation of the encoder input bits as shown in Table 2.19, only one S_n bit can be high at a time. Therefore a high on an S_n bit represents the point where the series of logical ones at the input of the encoder stops. Later on, in Section 2.5 it is shown that this point also represents the whereabouts of the input signal of that flash ADC and is used to switch the corresponding DC voltage level as the output of the DAC circuit. But these bits are only used whenever a DAC is combined to a 4-bit flash ADC and otherwise S_n bits are not used. Figure 2.68 shows the symbols used for the 7-to-3-bit and 15-to-4-bit encoders used in flash ADCs discussed in Section 2.4.

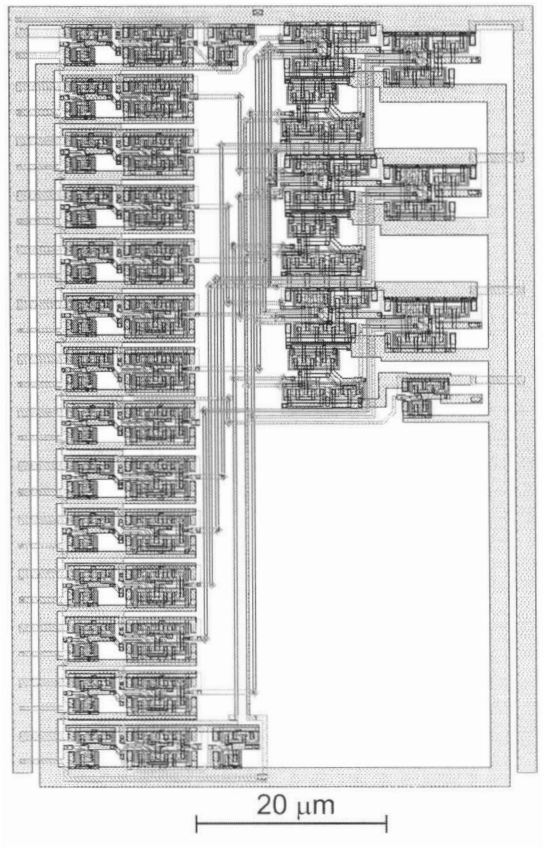


Figure 2.67: Layout of the 15-to-4-bit encoder.

Table 2.20: Timings of both encoders.

Parameters	7-to-3-bit Encoder	15-to-4-bit Enoder
t_{phl}	900 ps	1.24 ns
t_{plh}	463 ps	570 ns
t_r	560 ps	560 ps
t_f	600 ps	600 ps

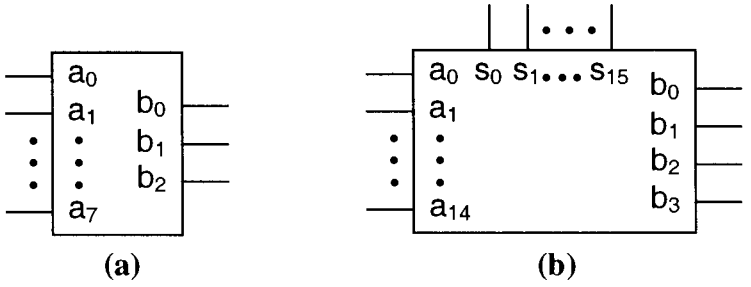


Figure 2.68: (a) Symbol of the 7-to-3-bit encoder. (b) Symbol of the 15-to-4-bit encoder.

2.4 Flash ADC Circuits

The functionality of flash ADCs has been described previously in Section 1.3.1. The schematic of a general flash ADC is repeated here in Figure 2.69 for your convenience. A set or resistors in series generate DC levels by simply dividing the voltage difference on the ends of the resistor array, which is equal to V_{ref} - V_{low} as shown in Figure 2.69. These DC levels connect to the negative inputs of comparators and the input signal connects to the positive input of the comparators. Therefore the output of comparators with DC reference levels higher than the input signal will be low and the rest will be high. Comparators outputs then enter an encoder that generates the n-bit output number. The conversion uniformity in flash ADCs depends on the resistor array. Equal resistors result in uniform conversion and vice-versa.

In circuits of this project, two kinds of flash ADCs are used. One is a 3-bit non-uniform flash ADC and the other one is a uniform 4-bit flash ADC. All the building blocks of these ADCs has been described before, except for the comparator that is discussed below.

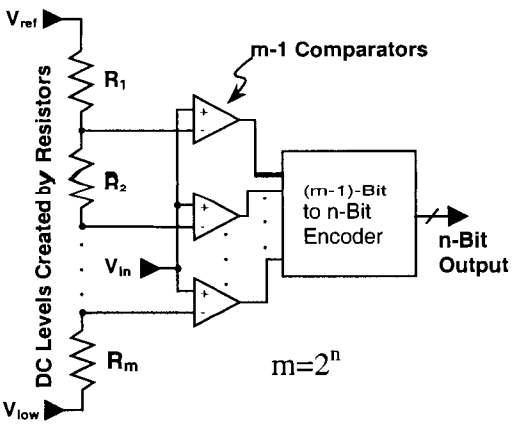


Figure 2.69: Circuit diagram of an n-bit flash ADC.

2.4.1 Comparator

Analog comparator is one of the circuits used to build flash ADCs. Unlike OpAmps, frequency compensation and linearity are not an issue in comparators because the output signal is always digital corresponding to saturation of amplifiers. The most important parameters in a comparator are gain, speed and input offset. High gain and speed together cause a fast output transition and low input offset reduces the comparison error. The circuit used as a comparator for this project is shown in Figure 2.70. There is a biasing voltage generator circuit that consists of M1, M2 and M3 transistors. The input signals go into the V_{in+} and V_{in-} pins. First stage of the comparator, which consists of transistors M4 to M10, is a low-gain high-bandwidth preamplifier stage. The output of this stage goes into a latch made of transistors M11 to M15. A latch circuit not only has a high gain, but also has a very fast output transition time and reduces the comparator delay. Next stage is a self-biased circuit that functions as a differential amplifier made of transistors M16 to M21. This stage has a high voltage gain and also is a very suitable stage to generate high output currents. Therefore it can charge or discharge the capacitive load of the next stage with a high speed. And finally the last stage is an inverter driver that drives output loads and also generates rail-to-rail output signal for the comparator, made of transistors M22 and M23. Transistor parameters of the comparator circuit are summarized in Table 2.21.

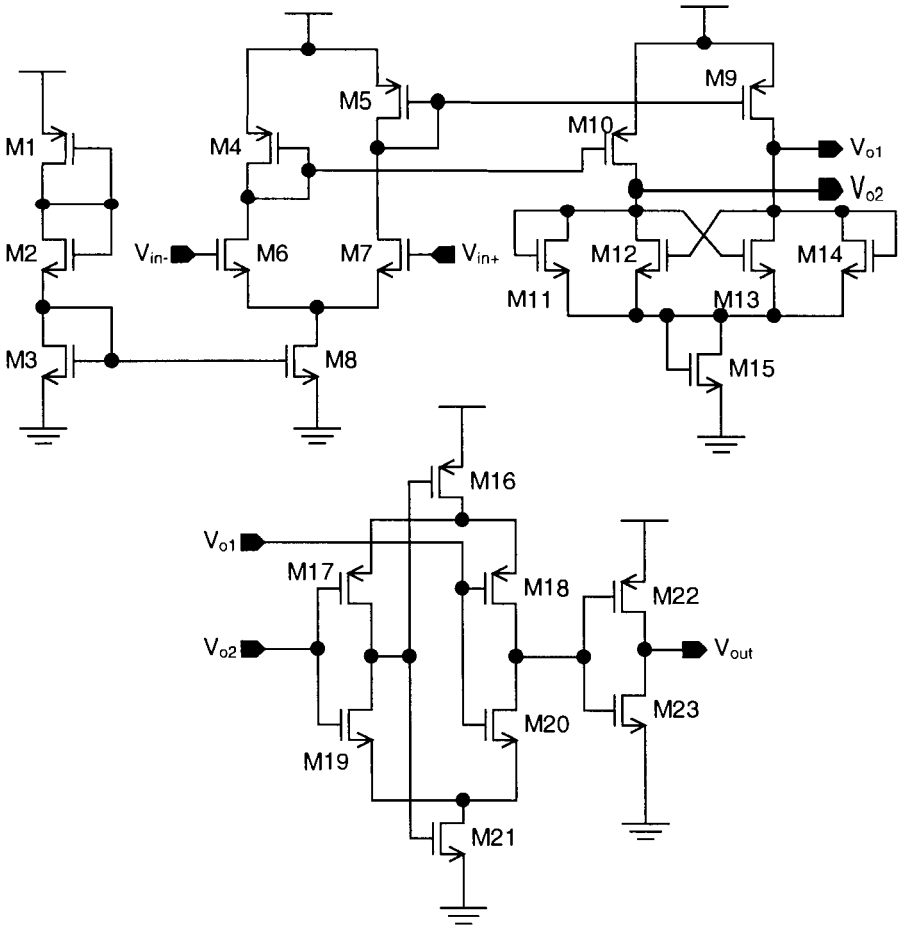


Figure 2.70: Schematic of the comparator circuit [5].

Table 2.21: Transistor parameters of the comparator circuit.

Comparator Circuit					
Names	Width	Length	Names	Width	Length
M1	4 μm	350 nm	M13	1 μm	500 nm
M2	800 nm	6 μm	M14	1 μm	500 nm
M3	2 μm	350 nm	M15	1 μm	350 nm
M4	1 μm	500 nm	M16	1.5 μm	500 nm
M5	1 μm	500 nm	M17	3 μm	350 nm
M6	4 μm	350 nm	M18	3 μm	350 nm
M7	4 μm	350 nm	M19	1 μm	350 nm
M8	7 μm	1 μm	M20	1 μm	350 nm
M9	3 μm	500 nm	M21	0.8 μm	2 μm
M10	3 μm	500 nm	M22	4.5 μm	500 nm
M11	1 μm	500 nm	M23	2 μm	500 nm
M12	1 μm	500 nm			

To test the comparator a 50fF output load is connected to the comparator that represents the input capacitance of other stages. This is the maximum load that the comparator has to drive in the circuits of this project, because it is always connected to the input of a digital circuit, which here is the encoder circuit. Some of the comparator parameters are also gathered in Table 2.22. The layout of the comparator is shown in Figure 2.71.

Table 2.22: Parameters of the comparator.

Parameters	Value
Low Frequency Gain (A_m)	115 dB
3dB Frequency	414 KHz
Unity Gain Frequency	980 MHz
Input Offset Voltage	0.5 mV
Input Common Mode Range	0.8v – 3.3v
Output Voltage Range	0v – 3.3v

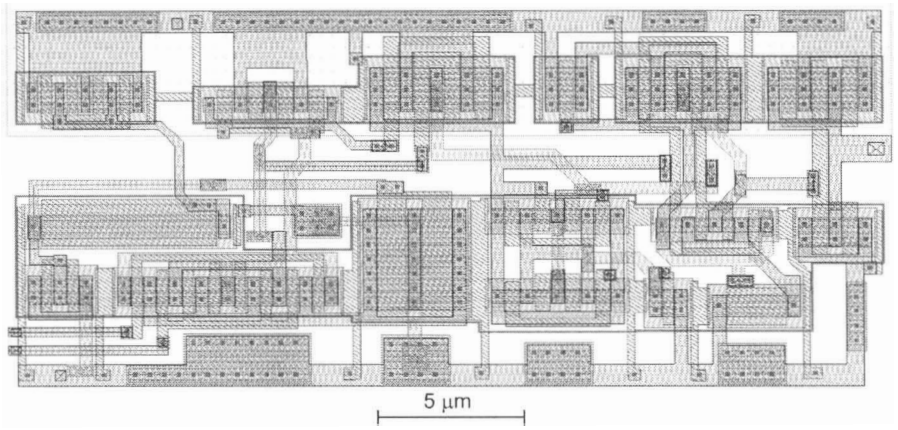


Figure 2.71: Layout of the comparator.

2.4.2 3-bit Non-Uniform Flash ADC

This flash ADC is used in the VGA block of the floating-point ADC of this project, as described before in Section 0. Table 2.23 shows the output of the 3-bit flash ADC for normalized input signal between non-uniform input signal ranges. For a 3-bit flash ADC 8 resistors, 7 comparators and a 7-to-3-bit encoder is required. As described before, these non-uniform ranges are generated using non-equal resistor values.

Table 2.23:Signal ranges and corresponding output bits of the 3-bit non-uniform ADC.

Input Signal (x(t)) Ranges	Flash ADC Output
1/2< x(t) <1	111
1/4< x(t) <1/2	110
1/8< x(t) <1/4	101
1/16< x(t) <1/8	100
1/32< x(t) <1/16	011
1/64< x(t) <1/32	010
1/128< x(t) <1/64	001
x(t) <1/128	000

The resistor values can be calculated using Table 2.24 where the targeted unity resistance R is equal to 350Ω. This resistor array along with the comparators and 7-to-3-bit encoder described in Section 2.3.6 are combined to make the non-uniform 3-bit flash ADC. The schematic of the flash ADC is shown in Figure 2.72.

Table 2.24: Resistor values of the 3-bit non-uniform flash ADC.

R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1
R	R	2xR	4xR	8xR	16xR	32xR	64xR

To show the performance of this flash ADC, V_{ref} = 3.3V and V_{low} = 1.3V are applied to the circuit along with a sinusoidal input voltage with an amplitude of 1V and an offset voltage of 2.3V to cover the entire input range. The simulation results are shown in Figure 2.73.

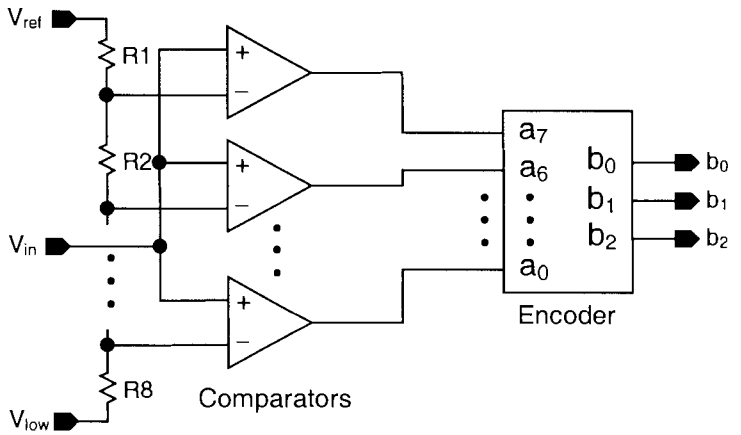


Figure 2.72: Schematic of the 3-bit non-uniform flash ADC.

The straight lines in the input signal diagram of Figure 2.73 represent reference DC voltage levels created through the resistor array of the 3-bit ADC. As you can see, due to non-equal resistor values in the resistor array of this ADC, DC lines are equal to ½, ¼, and so on of the input signal range. There is only one issue for the layout design of this flash ADC and that is the resistor array. As mentioned before, resistor values are affected drastically in the fabrication process. But in the flash ADC circuits the resistance ratio matters not the value of the resistor. Therefore resistors in the array are matched very carefully to obtain a very good ratio and therefore accurate DC levels. Figure 2.74 shows the matching diagram of the resistor array where rectangles with the same numbers stand for the divisions of one single resistor. Numbers are in correspondence with the ones in Figure 2.72. Figure 2.75 shows the layout of the resistor array.

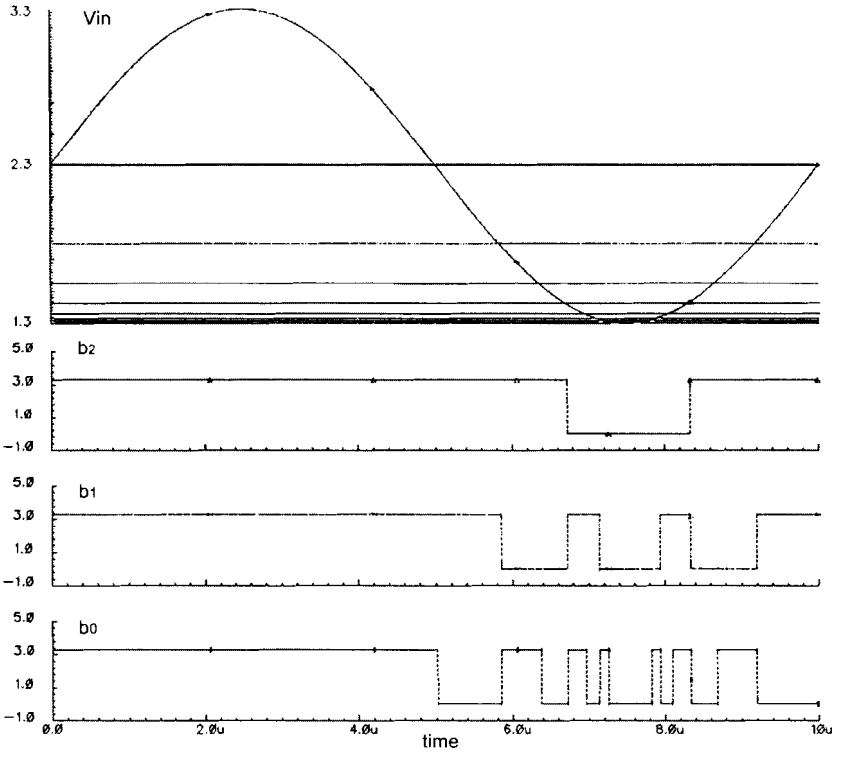


Figure 2.73: Simulation results of the 3-bit flash ADC circuit.

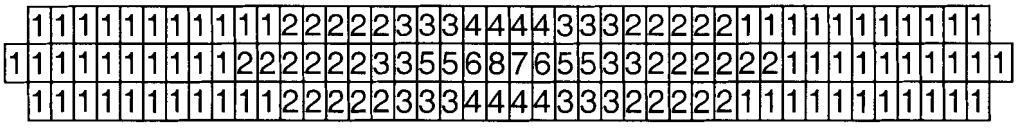


Figure 2.74: Matching diagram of the resistors in the resistor array.

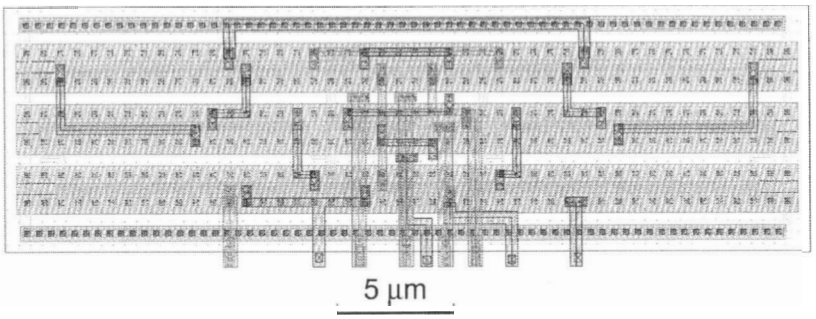


Figure 2.75: Layout of the resistor array.

All the components of the 3-bit flash ADC were wired together to generate the final layout shown in Figure 2.76.

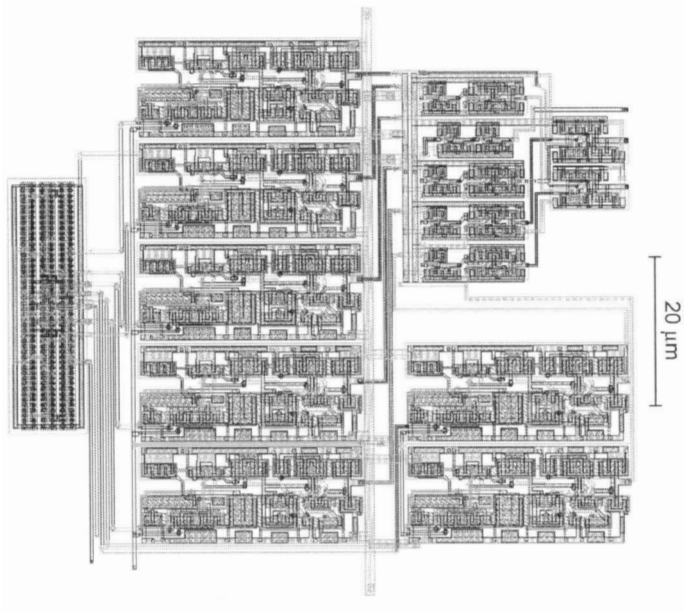


Figure 2.76: Layout of the 3-bit non-uniform flash ADC.

One important parameter of flash ADCs is their propagation delay from when the input signal goes into the circuit until the corresponding output digital number is generated. In the proposed flash ADC circuit, this delay is highly dependant on the input voltage frequency. Slower input signals cause the comparator outputs to react slightly slower and therefore cause the delay to increase. As simulations proved, the propagation delay of the 3-bit flash ADC for different input frequencies is somewhere between 4ns to 30ns. Not only that, but also the input to all the

flash ADCs are coming from switched capacitor circuits. Therefore no matter what the input signal frequency is, due to the voltage sampling, changes in the voltage level are done very fast. As mentioned before in Section 2.2.4, the switched capacitor amplifier delay is about 50ns. Therefore testing the 3-bit ADC with 50ns transient time results in a small 5.5ns propagation delay for this ADC.

2.4.3 4-bit Uniform Flash ADC

4-bit uniform flash ADCs are used in the stages of the pipeline ADC of this project. For a 4-bit flash ADC 16 resistors, 15 comparators and a 15-to-8-bit encoder is required. As it is a uniform ADC, all the resistors have the same values equal to about 1.2 kΩ. Figure 2.77 shows the schematic of the 4-bit ADC. To test the ADC, same signals as the ones used to test the 3-bit flash ADC of the previous section are used: V_{ref} = 3.3V, V_{low} = 1.3V and a sinusoidal input voltage with an amplitude of 1V and an offset voltage of 2.3V. The results of the simulation are shown in Figure 2.78. The straight lines shown in the input voltage diagram of Figure 2.78 are DC voltage levels generated from the ADC resistor array. When the input voltage passes one of these lines, output binary number changes accordingly.

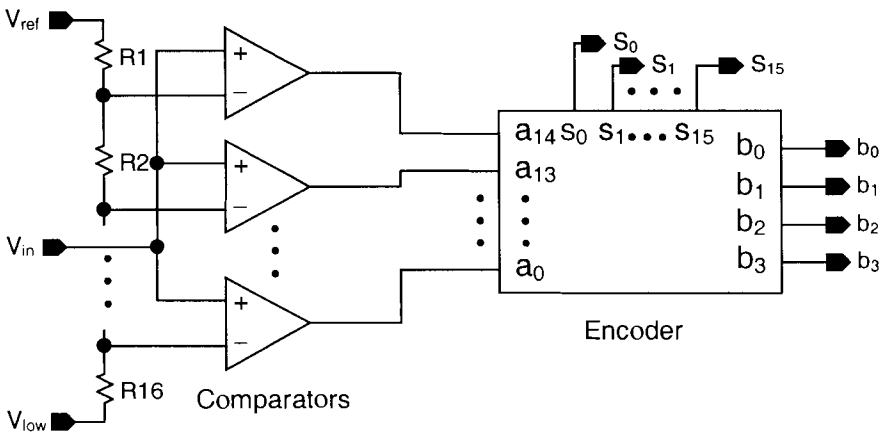


Figure 2.77: Schematic of the 4-bit uniform flash ADC.

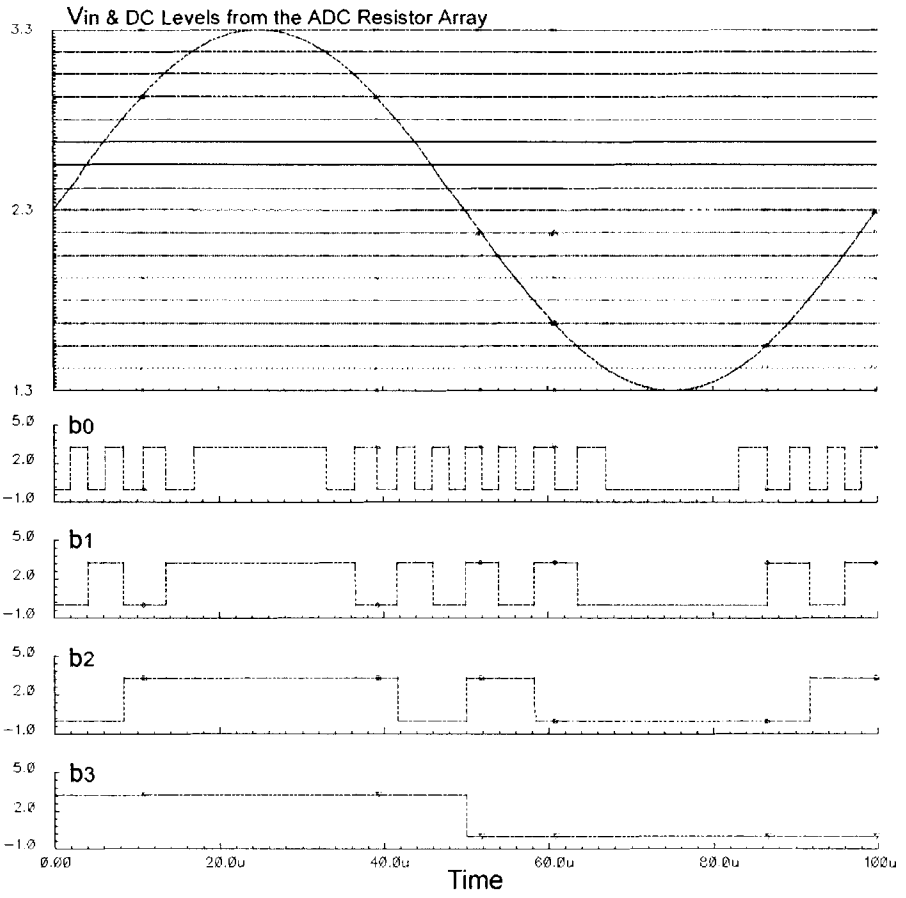


Figure 2.78: Simulation results of the 4-bit uniform flash ADC.

The usage of S_n signals is discussed in more details later in Section 2.5 for DAC and ADC combination. To measure the propagation delay of the 4-bit flash ADC it was tested for a 50ns transient time in the same conditions as the 3-bit flash ADC in the previous section. The result was a propagation delay of 6ns. In the layout design for the resistors to be in the same conditions, the poly resistors layouts were put in parallel of each other, as their values are the same. Then they were connected in series to form the resistor array of the ADC. Also dummy resistors were placed on the array sides to improve the layout result. The layout of the entire 4-bit flash ADC is shown in Figure 2.79.

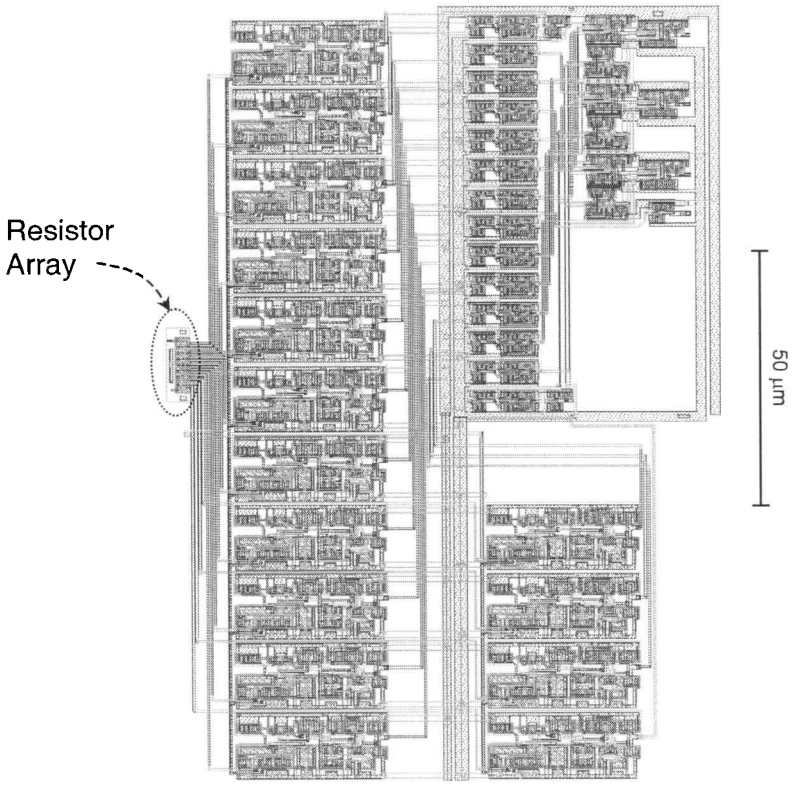


Figure 2.79: Layout of the entire 4-bit flash ADC.

2.5 DAC Circuit

As mentioned before in Section 1.3.3, Digital to Analog Converter (DAC) circuit is used in pipeline stages of the pipelined ADC block of this project. First the input signal of the pipeline stage is converted into digital signal using a flash ADC and the number will be converted back to analog using the DAC and goes to a subtracter to get the quantization error.

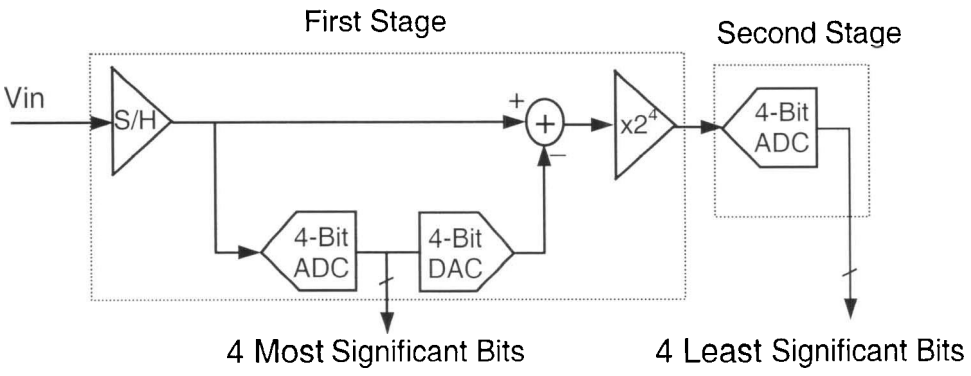


Figure 2.80: Block diagram of the pipelined ADC block of this project.

The block diagram of the pipelined ADC is repeated here in Figure 2.80. The first thing that comes into mind is to design a separate DAC and put it after the ADC of the pipeline stage. But one important issue is the matching between DAC and ADC circuits. As mentioned before, flash ADCs use a resistor array to generate DC levels to be compared with the input signal level. Also DAC circuits generate their own signal levels depending on their input digital value. DC levels in an ADC are not necessarily equal to the levels generated at the output of a DAC. Knowing that in fabrication processes resistor matching is not done accurately as desired, it is obvious that in two separate circuits there will be much greater mismatching. Therefore the output of the DAC will be different than the DC level of which the input signal is compared to inside the ADC. This will cause an error over the output signal level of the pipeline stage and next stages will not correctly recover the digital number.

What I did to avoid this problem was to combine the circuits of the ADC and the DAC. Basically in the designed circuit the DAC uses the same DC levels generated in the ADC to produce its output signal. This way the DAC output levels will be exactly the same as the ADC DC levels. Figure 2.81 shows the schematic of this combined circuit.

The ADC of this figure is the same 4-bit flash ADC discussed in Section 2.4.3. The DC levels generated in the ADC are buffered through low-frequency OpAmps with a unity gain feedback configuration. The low-frequency OpAmp was used here because it is only required to buffer DC voltage levels. The design of this OpAmp is discussed in Section 2.2.3. DC levels are going to be sent to a number of switches and switching can add noise to DC levels. Noise on DC levels could drastically damage the performance of both the ADC and the DAC. That's why buffers are used to transfer the DC levels to the switches to isolate them from the switching noise.

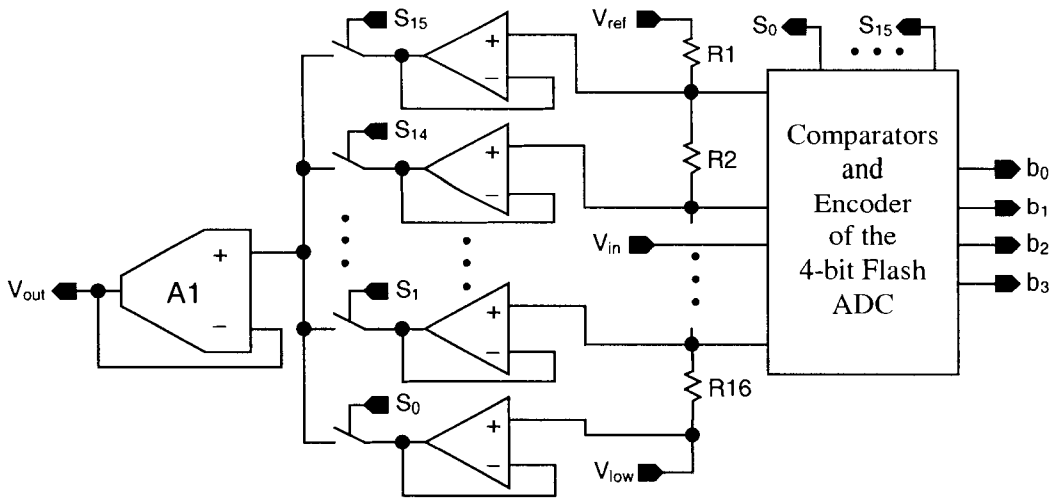


Figure 2.81: Schematic of the combined circuit of the ADC and the DAC.

There are sixteen switches that each one can switch one DC level and only one of them will be closed at a time. The outputs of the switches are all shorted together. Therefore this common connection can have different voltage values depending on which switch is closed. The switches are activated by the S_n signals made within the encoder of the ADC as discussed in Section 2.3.6. A high on a S_n signal shows that a_{n-1} is high and a_n is low. Because of the nature of the input signals of the encoder, which are the comparator outputs, only one S_n signal can be high at a time. V_{DCn} is defined as the n^{th} DC voltage coming from the ADC resistor array from low to high ($V_{DC0}=V_{low}$) Therefore when the input of the ADC is between V_{DCn} and V_{DCn+1}, S_n signal will be high that causes the buffered V_{DCn} signal to be switched to an output high-frequency buffer ($A1$). A high frequency OpAmp discussed in Section 2.2.1 was used as the output buffer of the DAC because the resulted signal from switches has the same properties as the input signal to the pipeline stage.

As the same DC levels of the ADC are switched out from the DAC, the mismatching problem between the 4-bit ADC and DAC of the first pipeline stage has been solved. This combined circuit is only used in the first stage of the pipelined ADC. The second stage only has one 4-bit flash ADC as discussed in Section 1.3.3. To test the DAC circuit, the combined circuit

is simulated. V_{ref} = 3.3V and V_{low} = 1.3V are applied to the circuit along with a sinusoidal input voltage with an amplitude of 1V and an offset voltage of 2.3V. The simulation results of this circuit are provided in Figure 2.82. V_{out} signal is the DAC output signal. Every level in this signal is the same as one of the DC levels of the 4-bit ADC resistor array as discussed before. Therefore as seen in Figure 2.82, whenever the input signal V_{in} passes one of these levels, the digital number and DAC outputs change to a new value.

The propagation delay time for the combined circuit from when the analog signal goes into the ADC until the corresponding DAC analog output is generated was measured simulating the circuit with an input signal with a 50ns transient time. Using such input signal was discussed before in Section 2.4.2 for the 3-bit ADC delay measurement. The measurement resulted in a propagation delay value about 8ns. The combined ADC and DAC circuit has the largest delay time among digital or mixed signal components.

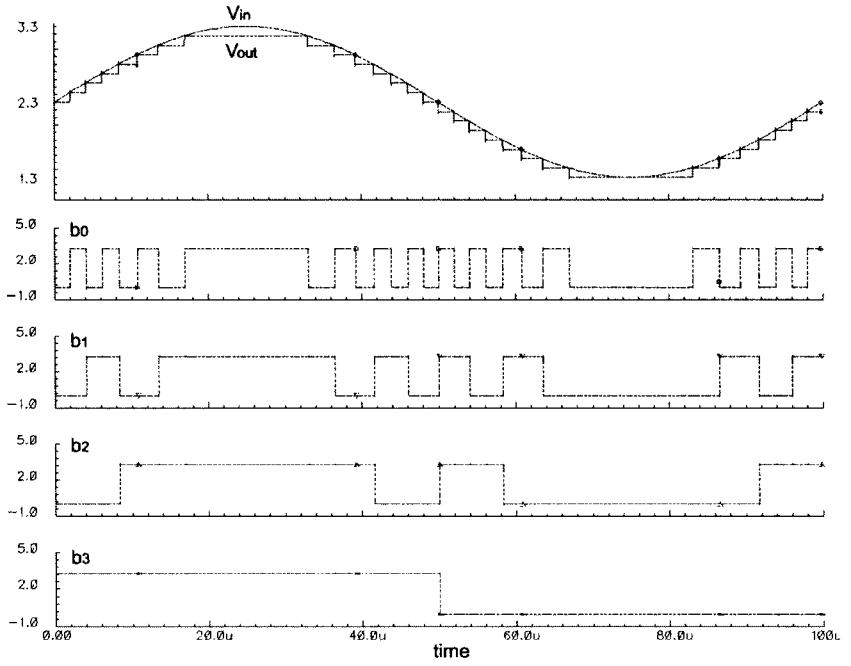


Figure 2.82: Post layout simulation results of the combined 4-bit ADC and DAC circuit.

Yet this delay is much smaller than the minimum pulse width of the clock phases used for analog stages, which is 50ns. The propagation delay of the ADC of the combined circuit is the

same as before, 6ns. The layout of the DAC is combined with the layout of the ADC shown previously in Figure 2.79. Figure 2.83 shows the layout of the combined circuit.

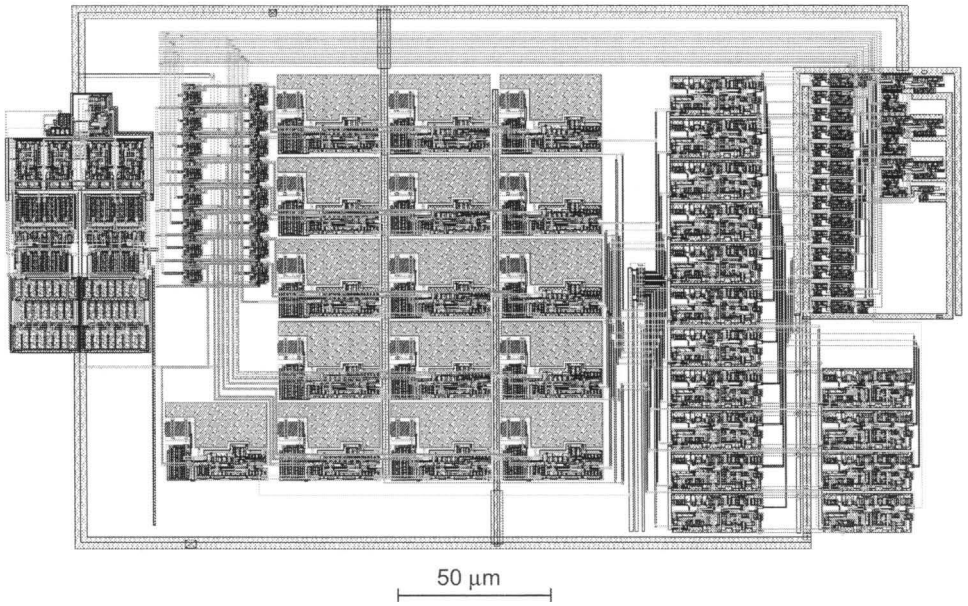


Figure 2.83: Layout of the combined DAC and ADC circuit.

2.6 Combining the Entire Floating-Point ADC Circuit

Now that the design of all the different circuit components of the floating-point ADC is discussed, it is time to put them together to get the final circuit. Putting the circuit blocks together is pretty straightforward. The only important and challenging issue is the clock phase and control signal distribution. As discussed in Section 2.2.4, all amplifiers of the ADC circuit are basically made of cascades of gain-of-2 VGAs. Therefore to make this issue more understandable, knowing the functionality of the gain-of-2 VGA circuit is essential.

As discussed before, every gain-of-2 VGA uses two clock phases. Also where a variable gain is required, a gain select control signal to V_{gs} input pin is also required. Otherwise the V_{gs} input is grounded for a fixed non-unity gain. The first clock phase resets the circuit and samples the input signal into the circuit and the second clock amplifies and sends the data out. When cascading two gain-of-2 VGA stages, the clock phase arrangement to the second stage is

switched. This way when the first stage is sending the data out, the second stage is sampling the data in. This is also shown in Figure 2.32 and Figure 2.33. Ignoring the rest of the ADC circuit and only considering the switched capacitor stages of the ADC, one can see that there are thirteen switched capacitor stages in series, as shown in Figure 2.84. They are either amplifiers or subtracters, which both have the same clocking method.

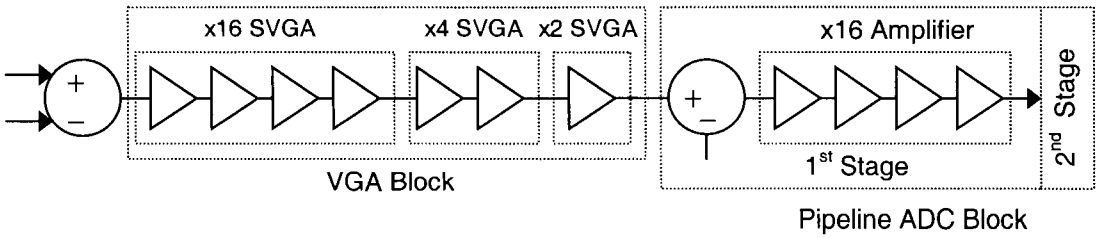


Figure 2.84: The series of switched capacitor circuits in the floating-point ADC.

As discussed in Section 1.3, two major blocks in series make the floating-point ADC: the VGA block and the uniform 8-bit pipelined ADC block. The VGA block includes three SVGAs in series as also discussed in Section 0: gain-of-16, gain-of-4 and gain-of-2 VGAs. After the VGA block, analog signal goes into the pipelined ADC where in the first stage of the pipeline there is a subtracter and a gain-of-16 amplifier. As also shown in Figure 2.84, to enhance the functionality of the ADC, another subtracter is added to the beginning of the circuit before the VGA block. This stage enables the designer to apply differential input to the floating-point ADC.

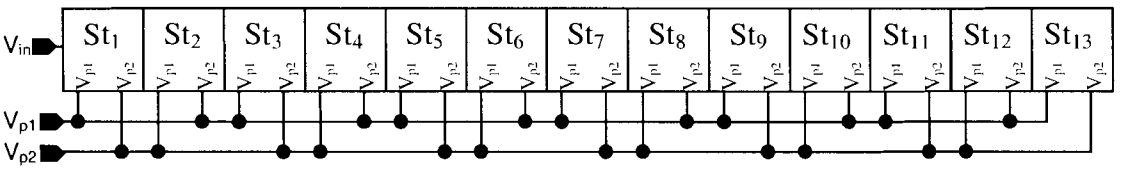


Figure 2.85: Function of the amplifier stages in series and their clock distribution.

Figure 2.85 shows the clock phase distribution between the switched capacitor stages. Every St_n block represents one switched capacitor stage corresponding to each stage of Figure 2.84. Clock phase distribution is done to achieve the correct functionality for the stages with the same fashion described before for cascading the gain-of-2 VGAs in Section 2.2.4.1. Therefore for

the switched capacitor stages, clock phases must be switched for each consecutive stage as shown in Figure 2.85. As there are thirteen stages, which use such clock phase distribution, one can see that it takes fourteen consecutive clock phases to pass the input signal to the output of the last stage. As each clock phase is half a clock period, it takes seven clock periods to recover the digital number from the analog input. But as the process is done in a pipeline manner, for every clock pulse a new output is generated. Therefore the output sample rate is the same as the clock frequency.

Knowing the clock distribution of the ADC, the assembly of the VGA block is discussed first. To understand the function of the circuit, one should keep the track of the clock phases. As described above, the first stage of the floating-point ADC is a subtracter. The subtracter is reading the signal in using the clock phase V_{p1} as also shown in the stage clock arrangements in Figure 2.85. Therefore it is sending the data out using the clock phase V_{p2} to the VGA circuit. As discussed in Figure 1.9 of Section 0, the VGA block consists of three gain stages in series (SVGA) and a non-uniform flash ADC and a number of d-flip-flops in between. Figure 2.86 shows the schematic of the VGA block in detail. Output digital bits of this block, e_{o0}, e_{o1} and e_{o2}, are exponent bits of the final output number and go out to chip pins. As the analog signal comes out of the subtracter by V_{p2}, it is sampled with the same clock phase into the first amplifier stage of the gain-of-16 amplifier (note the clock phase connections). Also it goes into the 3-bit non-uniform flash ADC. In Figure 2.86 there are three flip-flop arrays used to shift the output bits of the 3-bit flash ADC. The schematic of each of these flip-flop arrays is shown in Figure 2.87 (adjacent D and Q pins are connected). In the flip-flop array, clock phases $\overline{V}_{p1}$ and $\overline{V}_{p2}$ are each buffered through two buffer inverters in series and are sent to the clock input of each flip-flop as shown in Figure 2.87. Outputs of flip-flops corresponding to the first seven clock phases are used to adjust the gain of the three SVGAs of Figure 2.86, as they consist of a total of seven gain-of-2 VGAs in series in the VGA block.

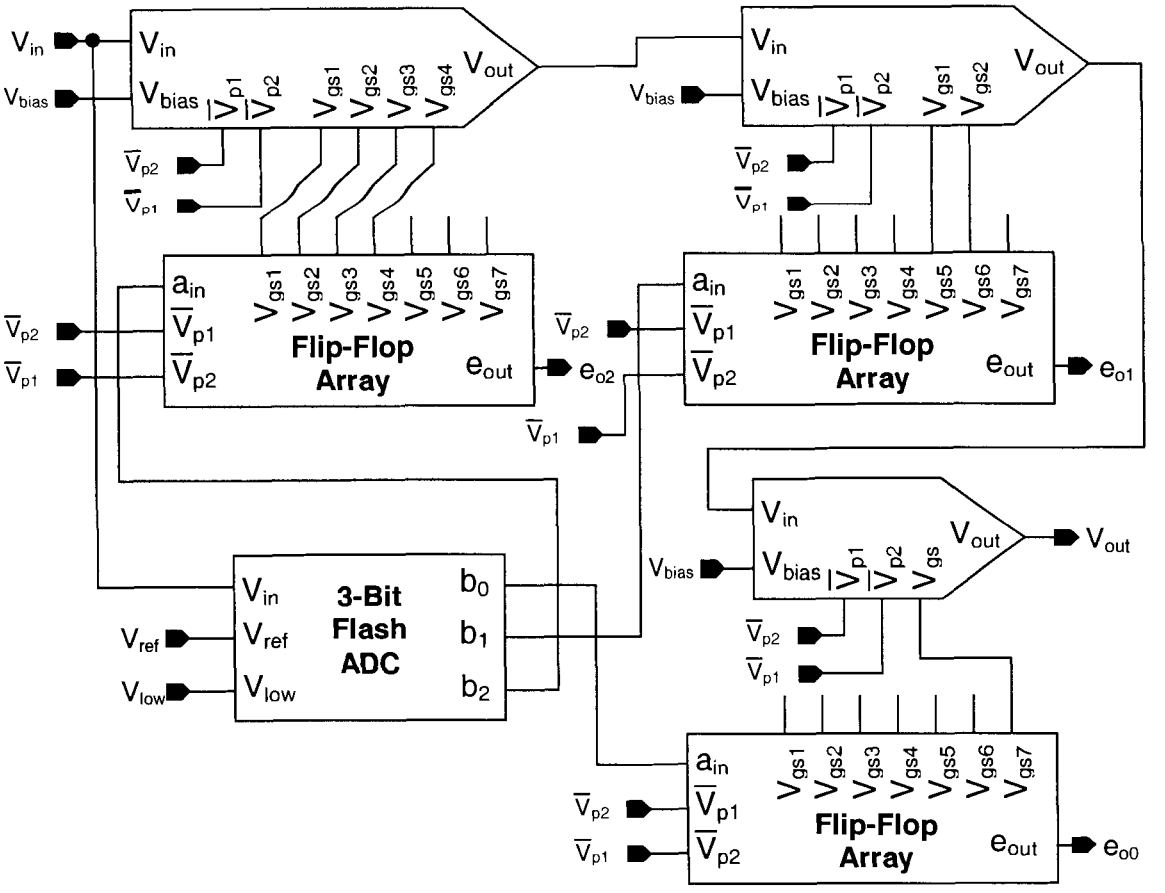


Figure 2.86: Schematic of the VGA block in detail.

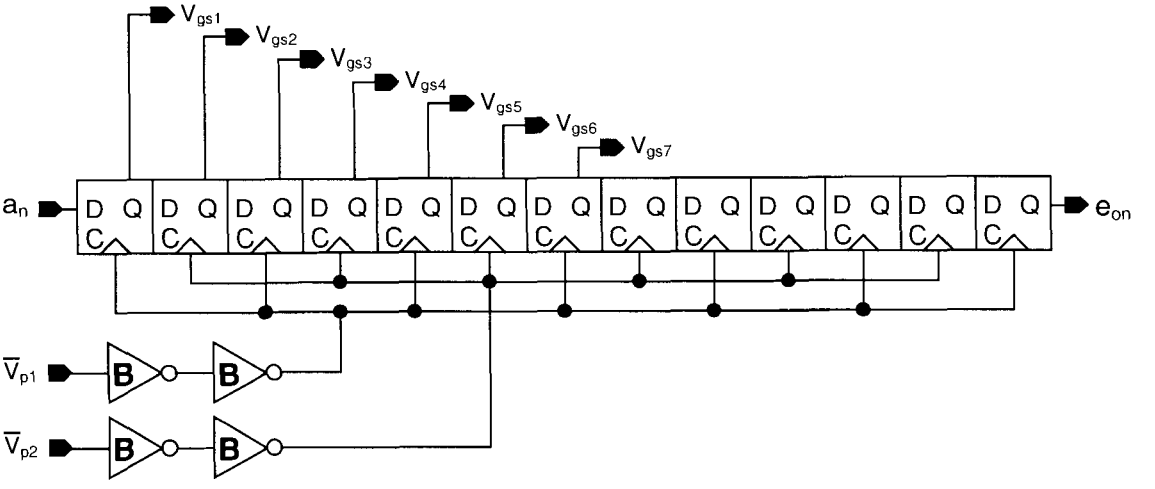


Figure 2.87: Schematic of the VGA block flip-flop array used for each 3-bit ADC output bit.

The reason to use the inverted clock phases as flip-flop clocks is that because analog signal processes are completed in a clock phase period, their outputs are valid for sure at the end

of that clock phase (falling edge). Therefore at the same time with the falling edge of the clock phase signal, flash ADC outputs will be valid and must be sampled into a flip-flop. Because flip-flops of this project sample their input on the rising edge of their input clock, the rising edge of the inverted clock phases is used to achieve the purpose mentioned.

There are thirteen flip-flops in series because as mentioned before, fourteen consecutive clock phases are used to generate the final floating-point number. Therefore after the subtracter at the beginning of the floating-point ADC, it takes thirteen consecutive clock phases to generate the output number. Because all different bits of the final floating-point number should be delivered to the output at the same time, every bit coming out of the 3-bit ADC of the VGA block must be delayed for thirteen clock-phase periods and that's why thirteen flip-flops are used.

The first, second and third bits of the 3-bit ADC, b_0, b_1 and b_2 are responsible for setting the actual gains of the gain-of-16, gain-of-4 and gain-of-2 VGAs respectively. The first control bit is the most significant bit, b_2. Again, it is only valid at the end of V_{p2} pulse, when the output of the subtracter is completely stable. Therefore at the falling edge of the V_{p2} pulse, this bit is sampled into the first d-flip-flop of the array used for the b_2 bit. The output of the first flip-flop, V_{gs1}, is ready at the beginning of V_{p1} and goes to the V_{gs1} pin of the first amplifier of the gain-of-16 VGA. For the same input signal level, all the V_{gs} signals of the same SVGA have to have the same value. But because the signal level arrives to each stage in a different time, the proper V_{gs} signal for that signal level has to be shifted though the flip-flops. Therefore the signal level and its corresponding V_{gs} signal will arrive at the same amplifier at the same time. After the first amplifier stage samples the data in by the V_{p2} clock phase, it processes the data and sends it out by the V_{p1} clock phase. At the same time, the second amplifier is sampling the signal level in using the V_{p1} clock pulse. Also it should have the correct V_{gs} signal. Therefore the output of the first flip-flop, V_{gs1}, which is the correct control signal for this signal level, is sampled at the end of V_{p1} by the rising edge of $\overline{V}_{p1}$ to become V_{gs2}. Using the same concept, as the signal level proceeds

into amplifiers: $\overline{V}_{p2}$ samples V_{gs2} over the third flip-flop as V_{gs3} to adjust the gain of the third amplifier stage and so on. Only four first flip-flops are used to adjust the gain of the gain-of-16 VGA amplifiers. The remaining nine flip-flops only delay and shift the b_2 bit to the output in the corresponding flip-flop array.

The second bit of the 3-bit ADC, b_1, is used only after five consecutive clock phases since when it has been generated. Therefore the outputs of the first four flip-flops in the flip-flop array of the b_1 bit are not connected. Then V_{gs5} is connected to the first amplifier and V_{gs6} is connected to the second amplifier of the gain-of-4 VGA. The seven remaining flip-flops of the second bit, b_1, will shift it to the output. And finally for the third least significant output bit of the 3-bit flash ADC, b_0, it takes seven consecutive clock phases until the signal level arrives at the input of the gain-of-2 VGA. Therefore the outputs of the six first flip-flops of the b_0 flip-flop array are not used. The output of the seventh flip-flop, V_{gs7}, is sent to V_{gs} pin of the gain-of-2 VGA. This is how the 3-bit flash ADC outputs are shifted to arrive at the correct inputs at the correct time.

After seven consecutive clock phases including the one used for the input subtracter circuit, the output of the VGA block is written into the first stage of the pipelined ADC using the eighth clock phase, V_{p1}. The detailed block diagram of the first stage of the 8-bit pipelined ADC of this project is provided in Figure 2.88. The output of the VGA block is sent out by the V_{p1} clock phase. At the same time, the signal level goes into the 4-bit flash ADC of the first pipeline stage, and the analog signal level is generated from the DAC of this stage. As mentioned in Section 2.5, the propagation delay of the DAC (8 ns) is much smaller than the V_{p1} pulse width (minimum 50 ns). Therefore the output of the DAC will be ready in the same clock phase and both the output of the VGA block and the output of the DAC will be sampled into the subtracter of the first pipeline stage by the V_{p1} clock phase. As discussed in Section 1.3.3, subtracter will generate the quantization error, which is the difference of the stage input signal and the DAC

output. Because every stage recovers four bits, the output of the subtracter is smaller than 1/16 of the maximum input level. Therefore it is amplified by a gain of sixteen to cover the entire input range of the next stage. A gain-of-16 amplifier with a fixed gain is used here. This means that the V_{gs} inputs of this amplifier are tied to zero as shown in Figure 2.88.

There are five switched capacitor stages in the first pipeline stage: one for the subtracter and four for the gain-of-16 amplifier. It means that a total of six clock phase pulses, one to input the signal to the subtracter and five to shift the signal out of SC stages, are required. Therefore the four output bits of the flash ADC are shifted out by six flip-flops in series for a suitable delay using the rising edge of $\overline{V}_{p1}$ and $\overline{V}_{p2}$ clock phases. The schematic of this flip-flop array that is used in Figure 2.88 is shown in Figure 2.89.

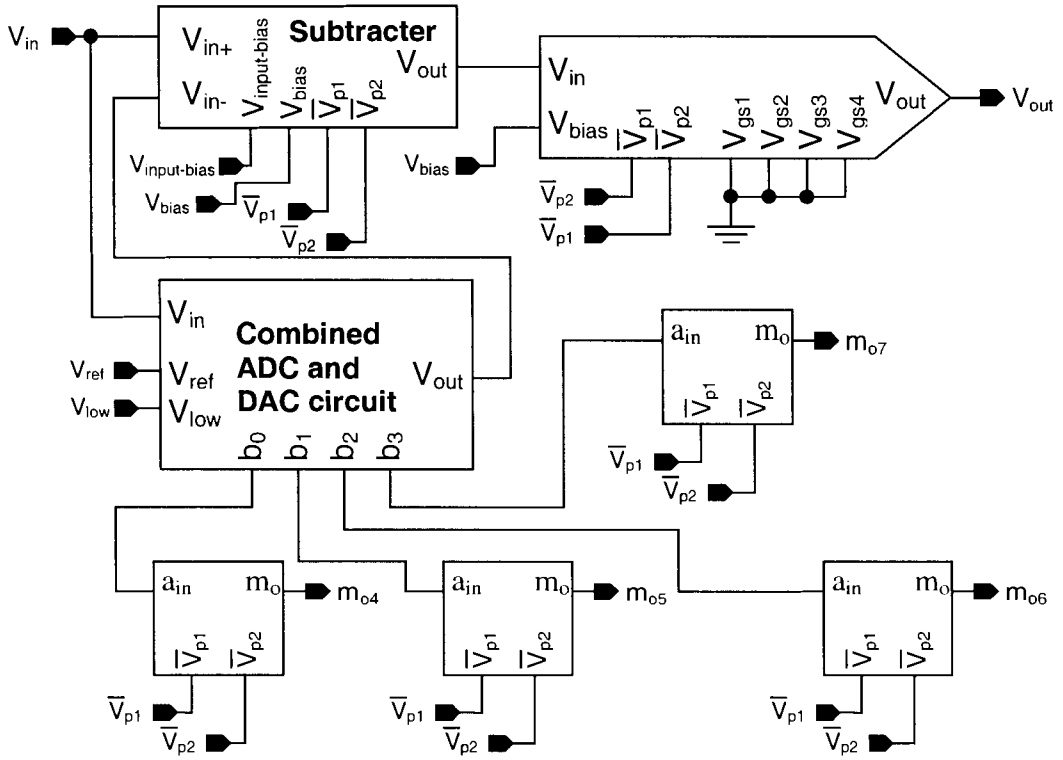


Figure 2.88: Detailed block diagram of the first stage of the 8-bit pipelined ADC.

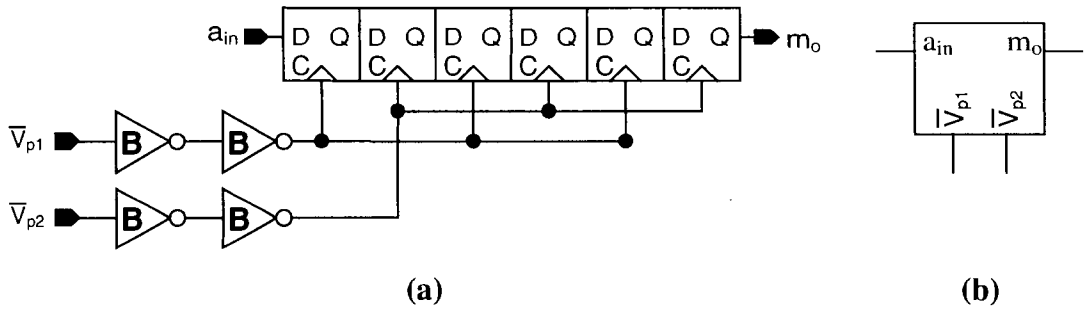


Figure 2.89: Schematic of the flip-flop array used in the first pipeline stage (a) and its symbol (b).

After five clock phases, using the sixth clock phase V_{p2}, the first pipeline stage sends its analog signal level out to the second pipeline stage. The second stage is only a simple uniform 4-bit flash ADC and four flip-flops as shown in Figure 2.90. Because the flash ADC is very fast (6 ns propagation delay), it generates the output digital numbers in the same clock phase, V_{p2}. Therefore at the end of V_{p2}, when the output of the flash ADC is stable, final four bits are sampled each into a flip-flop by the rising edge of $\overline{V}_{p2}$ as shown in Figure 2.90. And now all the eleven bits of the floating-point number for the same input signal level to the floating-point ADC arrive at the output of their corresponding final flip-flops together and form the output of the chip.

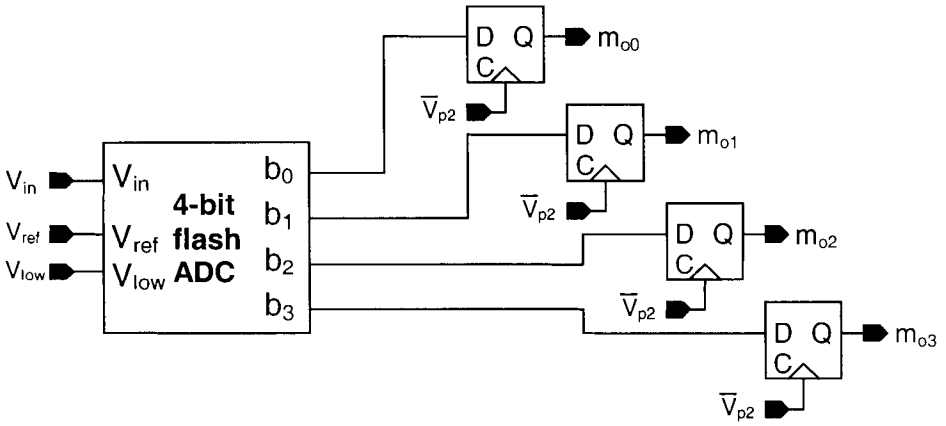


Figure 2.90: Detailed block diagram of the second stage of the 8-bit pipelined ADC.

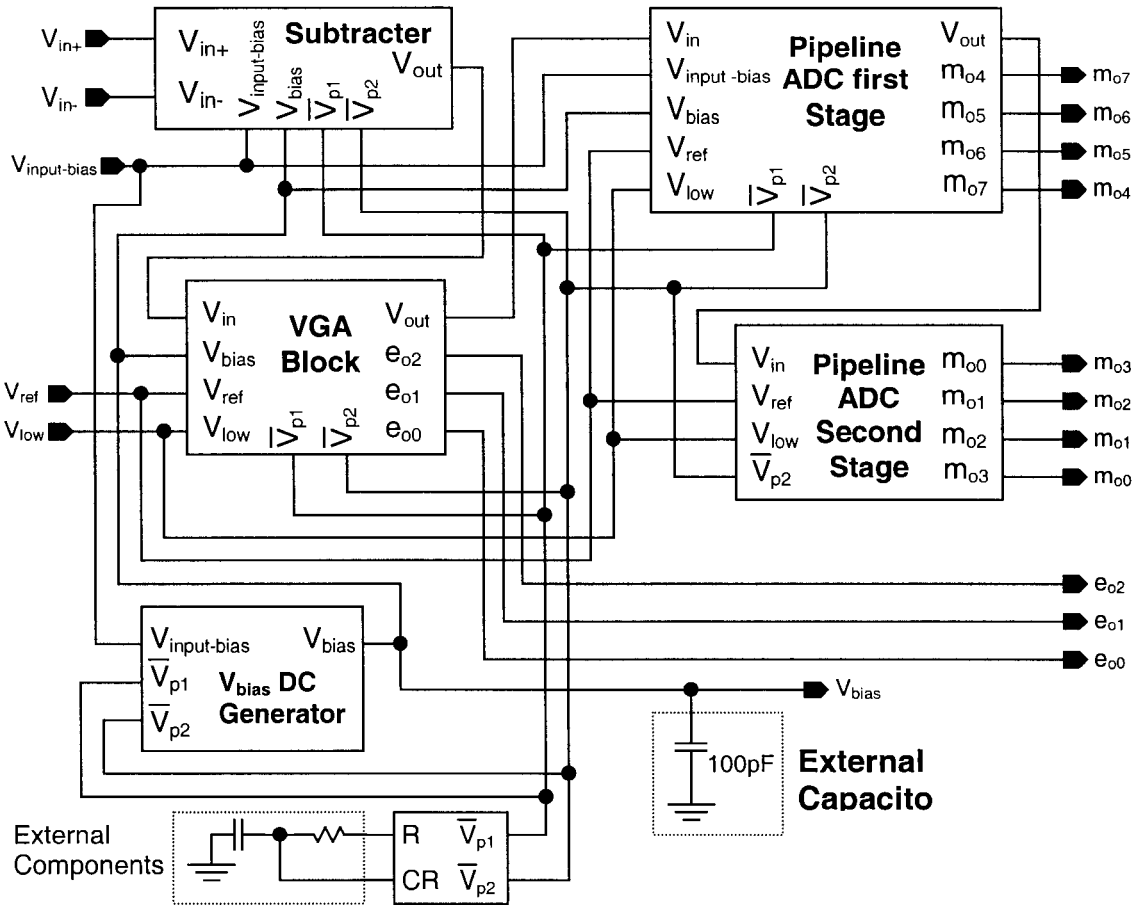


Figure 2.91: Schematic of the entire ADC of this project.

The final considerations are the biasing and reference voltages of the components. There are three input DC levels to the chip: $V_{input\text{-}bias}$, V_{ref} and V_{low}. V_{low} goes to all the V_{low} inputs and V_{ref} goes to all the V_{ref} inputs of the flash ADCs. These two together form the maximum input voltage range. For the differential input of the ADC, (V_{in+} - V_{in-}), the minimum value can be zero and the maximum value can be ($V_{ref} - V_{low}$). To achieve a normal operation for the chip, V_{low} and $V_{input\text{-}bias}$ must be tied together. This way the minimum signal of all stages will be the same. The $V_{input\text{-}bias}$ level goes to the input of the V_{bias} generator circuit discussed in Section 2.2.6. The V_{bias} output of this circuit goes to all the V_{bias} inputs of the switched capacitor circuits and adjusts their lower input margin to eliminate the output DC offset of the switched capacitor stages as discussed before in Section 2.2.6. V_{bias} is also sent out of the chip to a pin to be connected to the ground through a 100pF or higher capacitor. And finally, the $V_{input\text{-}bias}$ input level goes to the $V_{input\text{-}bias}$

input of all the subtracter circuits. The final block diagram of the floating-point ADC is presented in Figure 2.91.

2.6.1 An Example of the ADC Circuit Functionality

Now to understand how an analog signal level is transformed into a floating-point digital number, an example is provided here. Assume that the following signal levels are provided to the floating-point ADC inputs: $V_{input\text{-}bias} = V_{low} = 1.2V$, $V_{ref} = 3.2V$, $V_{in+} = 1.2V$ and $V_{in-} = 0.3V$. The input signal range for the input signal level is equal to $(V_{ref} - V_{low}) = 2V$. The differential input value is equal to $(V_{in+} - V_{in-}) = 0.9V$. As discussed before, a DC level equal to $V_{input\text{-}bias}$ is added to the input signal level to bring it into the operating range of the blocks. But here to simplify the calculations, we don't consider this value and also assume that all the stage ranges are from zero to $(V_{ref} - V_{low}) = 2V$. Therefore the 0.9V input level enters the VGA block. The 2V range is divided over the non-uniform resistor array of the 3-bit flash ADC. The generated DC levels are: 1V, 0.5V, 0.25V, 0.125V, 0.0625V, 0.03125V and 0.015625V. The 0.9V input level falls between the 0.5V and 1V range. Therefore the 3-bit flash ADC output will be $e_{o2}e_{o1}e_{o0} = (110)_2$. This is the exponent part of the floating-point number and also adjusts the gain of the VGA block to be 1x1x2 = 2. Therefore the input signal level, 0.9V, is amplified by a gain of two to be 1.8V. This signal goes to the first pipeline stage. The ADC of this stage divides the 2V signal range over its resistor array. Because the resistors have equal values, the voltage across each resistor is equal to 0.125V. Therefore the generated DC levels are equal to: 1.875V, 1.75V, 1.625V, 1.5V, 1.375V, 1.25V, 1.125V, 1V, 0.875V, 0.75V, 0.625V, 0.5V, 0.375V, 0.25V and 0.125V. The 1.8V input falls between the 1.75V and 1.875V range. Therefore the output of the ADC is $m_{o7}m_{o6}m_{o5}m_{o4} = (1110)_2$. Also the DAC output level will be equal to the lower voltage of the range, 1.75V. It will be subtracted from the input signal level, 1.8V, and the subtracter output will be 0.05V. Then the subtracter output will be amplified 16 times to get a 0.8V signal level. It goes in the second pipeline stage, which is another 4-bit flash ADC. The 0.8V signal level falls

between the 0.75V and 0.875V range. Therefore the ADC output number is equal to $m_{o3}m_{o2}m_{o1}m_{o0} = (0110)_2$. Now we have the entire floating-point number for the 0.9V input signal: $(110)_2$ exponent and $(11100110)_2$ mantissa.

To verify the result, we calculate the corresponding voltage for this number. So first we transform this number to a linear scale digital number. It is calculated to be two to the power of exponent times mantissa:

$$Linear\ Scale\ Number = (11100110)_2 \times 2^{(110)_2} = (11100110000000)_2 = (14720)_{10}$$

The maximum linear scaled digital number we can get out of this ADC is a 15-bit number. A 15-bit number can go up to $(32767)_{10}$. Therefore it is like we are dividing our 2V signal range by 32767. So each segment will be about:

$$Segment\ Size = 2V / 32767 = 6.103515 \times 10^{-5} V$$

Because the output number is equal to 14720, we have 14720 times one of these segments. So the voltage corresponding to the output digital number will be:

$$Corresponding\ Voltage = 6.103515 \times 10^{-5} V \times 14720 = 0.8984V$$

As you can see, this value is very close to the original value of 0.9V.

Again we mathematically calculate the binary number here to verify that eliminating extra bits of data is the cause of the difference between the 0.9V input and resulted 0.8984V output. Our input is 0.9V out of the 2V range, which is 45% of the maximum input range. Also we can say that it is 45% of the maximum 15-bit number, 32767, which is 14745. If we convert this number to the binary base we get $(111001100111001)_2$. It is obvious that the eight most significant bits of this number are the same as the ones we got from the calculations using the ADC topology as the mantissa bits. The difference between the seven least significant bits is simply due to the elimination of these bits and use of exponent number instead. Therefore from

this example, it is seen that by combining the floating-point ADC circuit as mentioned, the correct result will be achieved for this circuit.

2.6.2 Layout and Package of the Chip

For the layout design of the circuit, all the components are put together as described above. The final chip was sent to CMC for fabrication. The space allocated by CMC for this project was 1mm x 1mm. This area was very small and the layout had to be squeezed into this area along with the bonding pads. Figure 2.92 shows the final layout of the circuit showing the circuit blocks. The rest of the circuits in between the blocks are flip-flop arrays. The tight area of the chip not only is the cause of strange arrangements in pad locations but also disabled me to add more test features to the circuit to analyse the performance of the blocks. Fortunately, as CMC staff claimed, it was possible to wire the chip die to the package. But it would be almost impossible to find where the problem is if the chip doesn't function properly. Diagram shown in Figure 2.93 demonstrates how the chip die was packaged.

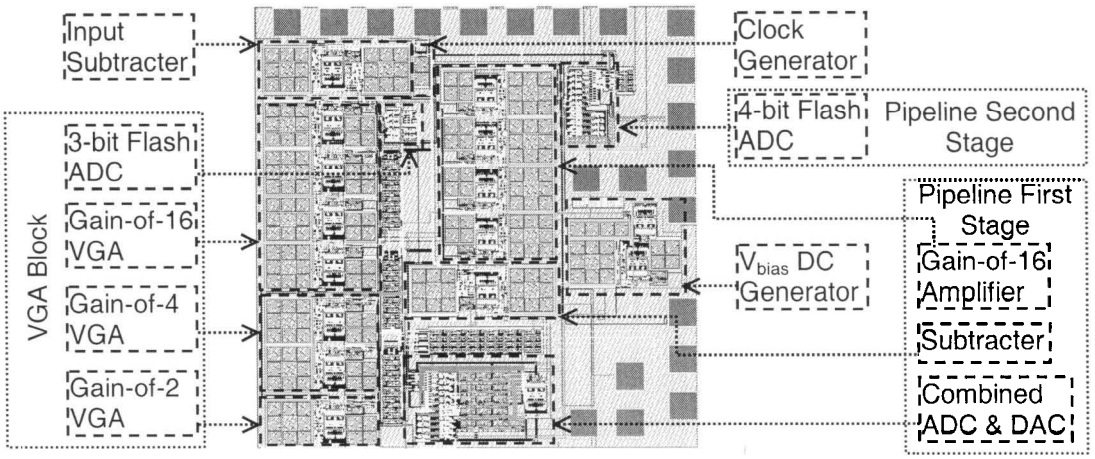


Figure 2.92: Final layout of the entire floating-point ADC in 1mm x 1mm area.

The package used for the final chip was 44CQFP. Referring to CMC website [16], this package can be used for frequencies not exceeding 1.5GHz. Of course the circuit of this ADC doesn't use such high frequencies. But using this package is advantageous compared to low frequency packages. Using this package, 44CQFP, the edges of the output digital pulses won't be

affected by the parasitic capacitors of the package. In the next chapter, results of the tests and measurements for two fabricated chips are discussed. Table 2.25 below shows the pin-out of the chip along with the description of the pins. As seen in this table, 21 pins are used for the chip and the remaining ones are not connected.

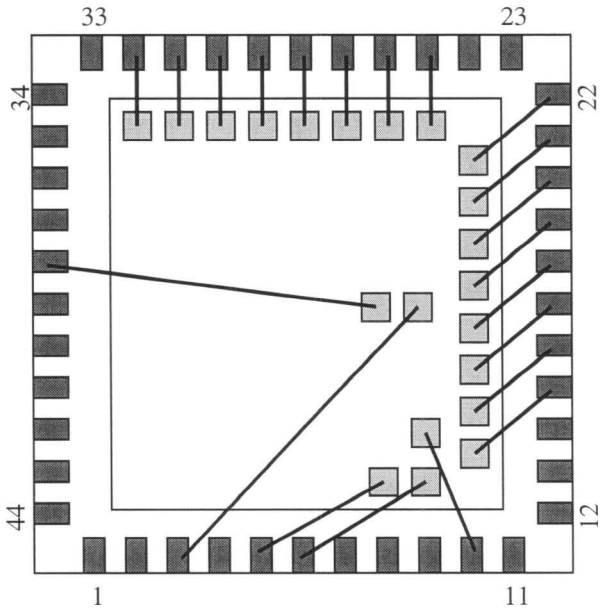


Figure 2.93: Packaging of the ADC chip to the 44CQFP package.

Table 2.25: Pin-out of the floating-point pipelined ADC.

Pin Numbers	Pin Names Respectively	Pin Description
3, 38, 17	e_{o0}, e_{o1}, e_{o2}	Exponent number bits (e_{o2} = MSB)
16, 15, 6, 5, 26, 25, 22, 21	$m_{o0}, m_{o1}, m_{o2}, m_{o3}, m_{o4}, m_{o5}, m_{o6}, m_{o7}$	Mantissa number bits (m_{o7} = MSB)
10	V_{bias}	Internally generated biasing voltage, this pin must be connected to the ground by a 100pF or higher capacitor.
18	$V_{input\text{-}bias}$	Biasing voltage input
19	GND	Chip ground pin
20	VDD	Chip VDD pin
27	V_{ref}	Reference voltage input pin
28	V_{low}	Low biasing voltage input pin
29	R	Resistor connection pin of the clock generator
30	CR	Capacitor and resistor connection of the clock generator
31	V_{in-}	Negative input voltage to the ADC
32	V_{in+}	Positive input voltage to the ADC
Other pins	N/C	Not Connected

2.7 Circuit Electrical Parameters

After putting the entire ADC circuit together, some important parameters of the ADC can be measured using simulations. All the circuits of this project were designed for the 3.3V supply voltage of the CMOS 0.18μm technology. As mentioned before in Section 2.2.4, the circuit speed is mostly limited by a slow settling time of the switched capacitor circuits. As measured in that section, the settling time delay for the output signal of designed circuits is about 50ns. All other circuits designed for this project have much smaller delays than 50ns. As mentioned before, there are two clock phases, each in every half a clock period. As the output analog signal process of the switched capacitor circuits is done in one clock phase, the clock phase period must be longer than 50ns. This gives a minimum clock period of 100ns or a maximum frequency of 10MHz. The sampling rate for the ADC of this project is equal to the clock speed and therefore the maximum sampling rate is 10Msamples/second.

As described in Section 1.2.1, the maximum sampling precision of the floating-point ADC of this project is equal to 8 bits for a wide range of the input signal to the ADC simply because it has an 8-bit mantissa. Therefore using Formula 1.2 the peak signal to quantization noise ration of this ADC is calculated to be 48dB. Also due to the use of the 11-bit floating-point output number, the circuit has a maximum resolution same as a 15-bit uniform ADC. Thus the dynamic range of the ADC will be equal to 90dB. The maximum input range of the analog stages defines the differential input range of the ADC. The lowest input range among the circuits is for the switched capacitor stages and is equal to 2v.

The power consumption of the circuit was measured using the simulation results. For a 3.3V supply voltage the measured power consumption was equal to a low value of about 50mW for the entire circuit. Table 2.26 Summarizes the circuit parameters. In the next chapter, first the circuit used for this project will be compared to some other topologies to show the advantages of the proposed circuit. Then measurements done on two fabricated chips are provided. These

measurements will be used to show the circuit performance and to verify the simulation results provided in this chapter. Table 2.27 shows the number of elements used inside the ADC circuitry.

Table 2.26: Summary of the floating-point ADC electrical parameters.

Parameter	Value
Sampling Rate	10 Msample/sec
Peak SNR	48 dB
Dynamic Range	90 dB
Differential Input Range (V_{in+}-V_{in-})	0v to 2v
Supply Voltage	3.3V
Power Dissipation	~50mW
Technology	CMOS 0.18 μm
Chip Area	1mm x 1mm
Active Area	0.915mm x 0.915mm

Table 2.27: Number of elements used in the ADC.

Element	Number
Transistor	6055
Capacitor	76
Resistor	70

Chapter 3

Comparisons, Measurements and Conclusion

3.1 ADC Circuit Comparison

In Chapter 2 the entire deign of the floating-point ADC of this project along with simulation results was discussed. These designs and simulation results here are compared to the properties of other circuit topologies, especially the ADC presented in [2]. As mentioned in the previous chapter, the circuit consists of two major blocks: the VGA block and the 8-bit pipelined ADC block.

The ADC circuit presented in [2] has the same topology except it has a 10-bit mantissa number and a 5-bit exponent number. The dynamic range of this number is the same as the range of a 15-bit uniform ADC. Also this dynamic range is similar to the range of the 11-bit output number of the ADC presented in this thesis. This is because the 5-bit exponent number generated in [2] is not coded. Therefore to show a number using these bits, the exponent bit corresponding with the exponent number is a logical one and the rest are zero. The disadvantage of such output number is having a higher number of bits such as 15 bits for the circuit presented in [2]. This 5-bit exponent number could be coded into three bits to show numbers from zero to four as five possible exponent values.

What I did here to save even more in the number of bits was first use a topology that already codes the exponent number into three bits in the VGA block as mentioned in Section 2.6. Second I used the entire range of the three bit exponent number and instead eliminated two bits in the mantissa number. This way I could have the same dynamic range as the ADC of [2] and yet reduce the output to eleven bits. The elimination of two mantissa bits is also helpful to reduce the required circuit for the pipelined ADC block and therefore saves more in the silicon area usage and power consumption.

The other consideration I did was the design on the 8-bit pipelined ADC block. In this block I used stages that extract four bits each instead of any other topology. Here I compare the topology used for this block to two other possible topologies. One possible uniform 8-bit ADC topology is an 8-bit flash ADC. For such an ADC it is required to have 256 resistors in the resistor array, 255 comparators and a large digital circuit for the encoder. Another possibility was to use a pipeline ADC with stages that each extracts only one bit, such as the one presented in [2]. For such an ADC 8 stages will be required. Table 3.1 shows the comparison between mentioned 8-bit ADCs. The values shown in this table are calculated using the power consumption and silicon area of the components design in this thesis.

Table 3.1: Comparison between different ADC topologies as the 8-bit ADC block.

ADC Topology	Number of Comparators	Other Components	Power Consumption	Silicon Area Usage
Two Stage 8-bit ADC	30	4	~10mW	~0.24mm^2
8-bit Flash ADC	255	Large Encoder	>34mW	~0.16mm^2
8-Stage 8-bit ADC	8	28	~17mW	~0.7mm^2

From the above table it is obvious that using an 8-Stage 8-bit pipeline ADC is completely disadvantageous as it consumes 70% more power and has almost three times the area of the two stage pipeline ADC of this project.

Table 3.2: Parameter comparison between the ADC of this project and the one proposed in [2].

Parameter	ADC Reported in [2]	ADC of This Project
Sampling Rate	20 Msample/sec	10 Msample/sec
Peak SNR	60 dB	48 dB
Dynamic Range	90 dB	90 dB
Supply Voltage	5v analog, 4.5v digital	3.3V
Power Dissipation	380 mW	~50 mW
Technology	CMOS 0.5 μm	CMOS 0.18 μm
Active Area	4.3 mm x 3.2 mm	0.915 mm x 0.915 mm

Also although the 8-bit flash ADC consumes about half the silicon area, it is a very power hungry circuit and consumes a much higher power more than three times the power consumption of the 2-stage ADC. From Table 3.1 one can see the advantage of using the 2-stage pipeline ADC proposed in this project.

Table 3.2 shows the comparison between the ADC of this project and the one in [2]. As seen in this table, much smaller power consumption and silicon area usage was achieved while having the same dynamic range by sacrificing the peak SNR for the ADC.

3.2 Measurements of Fabricated Chips

Two chips were submitted for fabrication to Canadian Microelectronics Corporation (CMC). First one was submitted while designing components of the ADC. This chip consisted of essential components of the ADC such as the flash ADC and switched capacitor VGA. This chip was used to verify the functionality of the blocks and confirm the design. After testing this chip, the ADC design was completed and a chip with the entire ADC circuit was prepared and submitted for fabrication as the second chip. Testing this chip showed the functionality of the entire ADC circuit and some of the ADC components. Below each chip and its measurements are discussed in detail.

3.2.1 First Chip: Essential Components

As mentioned above, this chip consisted of the most essential components of the circuit. Two large blocks, a gain-of-2 switched capacitor VGA and a 3-bit uniform ADC, along with some of their components, comparators, clock generator and high-gain high-bandwidth OpAmp, were included in the chip. Testing the large components confirmed the functionality of these blocks as they worked as they were supposed to. This also confirmed the functionality of all their sub-circuits. As you will see later, the provided information helped to improve the speed of the switched capacitor. Unfortunately the chip was packaged in a 68PGA package. This package is good for frequencies up to 50 MHz [16]. Therefore although there was no problem testing he

functionality of the blocks, output transient characteristics of digital signals could not be measured as they exceed 50 MHz. Below the test results of two major blocks of this chip are discussed. Figure 3.1 below shows the layout of the first chip.

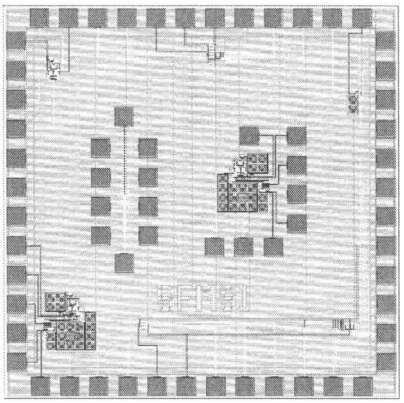


Figure 3.1: Layout of the first chip.

3.2.1.1 Switched Capacitor Amplifier

There is a difference between the switched capacitor VGA in the first chip and the one designed in Chapter 2 for the second chip. This difference is for the OpAmp used in this VGA. The OpAmp used here has the same topology and structure as the one designed previously in Section 2.2.1. Only the old design had slower characteristics and as you will see later in the VGA test, it resulted in slower operation frequency of 2.5MHz. Table 3.3 below shows the improved parameters of the new OpAmp designed in Chapter 2 compared to the old OpAmp.

Table 3.3: Improved characteristics of the new OpAmp compared to the old OpAmp.

Parameter	Old OpAmp	New OpAmp	Unit
Gain	58.2	58.7	dB
CMRR	54.4	58.9	dB
Unity Gain Bandwidth	870	930	MHz
Output Current	62	70	μA

The low operation speed of the VGA (2.5MHz) is why the OpAmp was modified to be able to provide better characteristics as shown in Table 3.3 to achieve a higher operation speed of 10MHz.

Figure 3.2 shows the test circuit of the gain-of-2 VGA and the pin numbers of the terminals. The structure of this circuit is the same as discussed in Section 2.2.4. To test the VGA circuit, a clock generator circuit was included in the circuit and all the necessary pins were connected to the package from pin number 3 to 5 and 61 to 65 as shown in Figure 3.2.

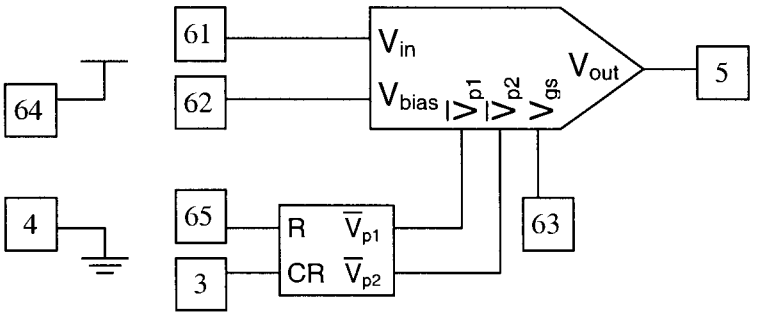


Figure 3.2: Switched capacitor amplifier test circuit.

The circuit was biased with a 3.3V power supply. To test the circuit an external resistor and capacitor were connected to the clock generator circuit and a frequency of about 680KHz was generated. This clock generator circuit was discussed in Section 2.3.5. The V_{gs} signal was controlled externally to change the VGA gain. Then a DC voltage equal to 1.5V was supplied to the V_{bias} input and a sinusoidal signal with 0.3V amplitude and 1.5V DC offset was supplied as the input signal of the stage. Below Figure 3.3 and Figure 3.4 were recorded from the oscilloscope and they show the VGA output waveform for V_{gs}=0 and V_{gs}=1 respectively.

The ripples on the output waveform are due to the switching and also the probe load over the output of the circuit. As shown with dotted lines on the output waveform, in the output clock phase period where the output is valid, it perfectly follows a sinusoidal waveform amplified with a gain according to the V_{gs} signal. It is obvious that V_{gs} effectively changes the stage gain and the gain is accurate for the corresponding V_{gs}. There is only an output offset for the gain equal to two that as mentioned before in Section 2.2.6, is due to the equal values of the V_{bias} and input signal DC offset. Adjusting the V_{bias} value eliminates this output offset.

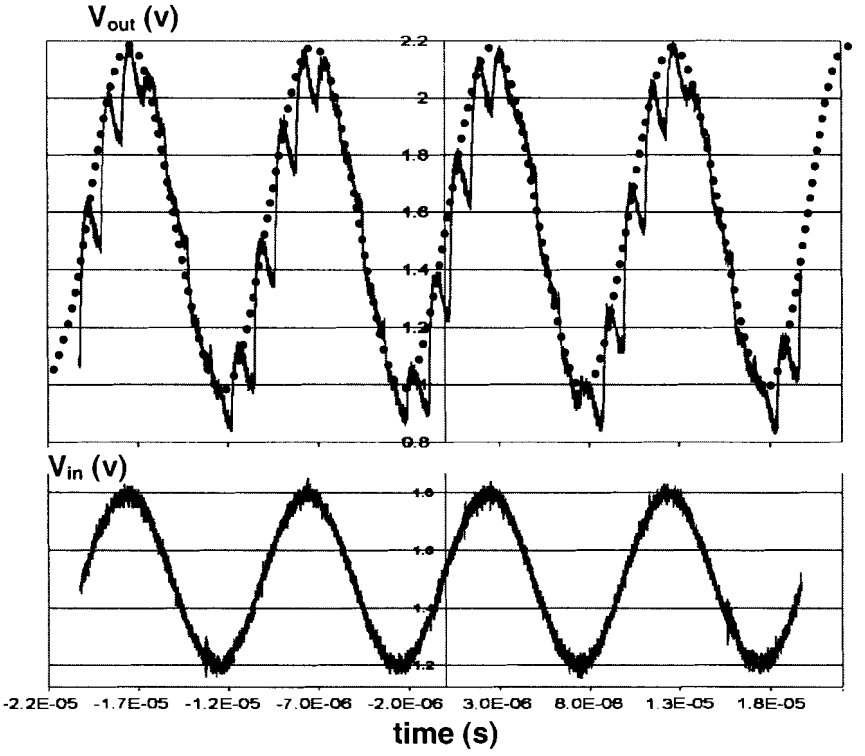


Figure 3.3: Measurement result of the VGA test circuit for V_{gs}=0 (Gain=2).

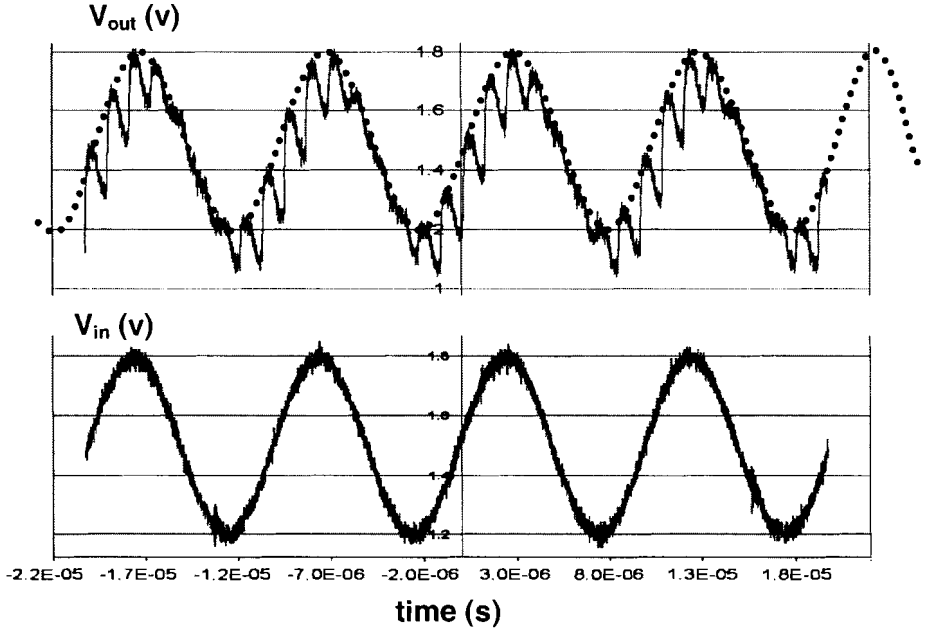


Figure 3.4: Measurement result of the VGA test circuit for V_{gs}=1 (Gain=1).

Another useful information to measure was the operation speed. Zooming in the output voltage of the VGA can show the circuit response delay of the circuit, as shown in Figure 3.5. In

this figure that is captured when the circuit was operating in about 400KHz, the operation delay was measured to be 200ns.

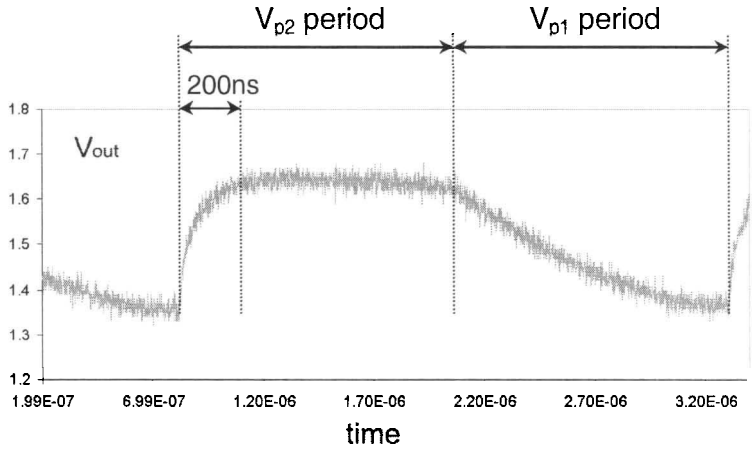


Figure 3.5: Output waveform of the VGA used to measure the delay.

This 200ns delay means that the clock phase periods can be as small as 200ns, which results in a 2.5MHz clock frequency. As mentioned, the OpAmp was modified to achieve better properties and as discussed before in Section 2.2.4 post layouts simulations confirm a delay of 50ns, which resulted in a 10MHz clock frequency. Below in Figure 3.6 the output of the pin named *R*, the clock generator Schmitt-triggered inverter output, is shown. The measurement frequency was about 400MHz.

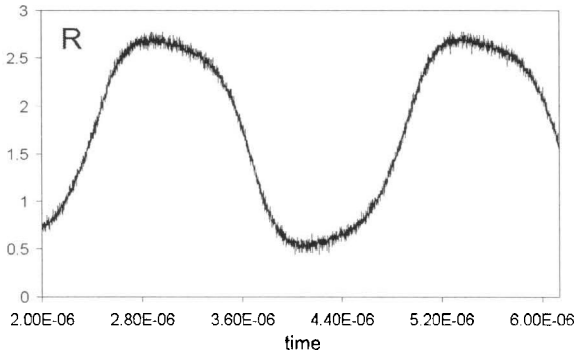


Figure 3.6: The Schmitt-triggered inverter output waveform, *R*.

From the VGA test it was confirmed that the circuit and all its components function properly including hi-frequency and low-frequency OpAmps, switches, digital gates and the clock circuit. Also the OpAmp was modified to achieve higher operation speed.

3.2.1.2 3-bit Uniform Flash ADC

The other major block designed for the first chip was a 3-bit uniform flash ADC. As shown in Figure 3.7 the flash ADC is connected between pins 39 to 46 of the package. Testing the flash ADC not only confirmed its functionality, but also the functionality of all its sub-circuits.

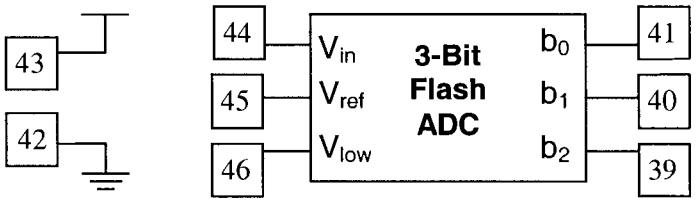


Figure 3.7: The test circuit of the 3-bit flash ADC.

The circuit was biased with a 2.2V power supply. This power supply voltage showed that the flash ADC circuit is even functional for voltages other than 3.3v. V_{low}=0 and V_{ref}=1.8v were supplied to the circuit. The input signal was a triangular waveform so that the output change could be better visible. The output of the flash ADC was recorded from the oscilloscope and shown in Figure 3.8. To avoid a crowded diagram, only the input and the least significant output are shown in this figure. But all the outputs worked perfectly as they were supposed to and correct output digital numbers were generated for different input signal levels. As mentioned at the beginning of this section, this flash ADC is a uniform ADC. Therefore the voltage ranges of the ADC are equal and the DC voltage levels generated from the resistor array of this ADC are shown in Figure 3.8. In this figure it is completely visible that exactly when the input passes one of the generated DC levels within the ADC, the output of the ADC changes to its new value. The edges of the output signal are not as fast as they were measured in Section 2.4.2 due to the low-frequency package. Yet the rise and fall times are measure to be 46ns and 40ns respectively. The

correct performance of this flash ADC also confirmed the functionality of its sub-circuits: the encoder block, comparators, digital gates, and the resistor array.

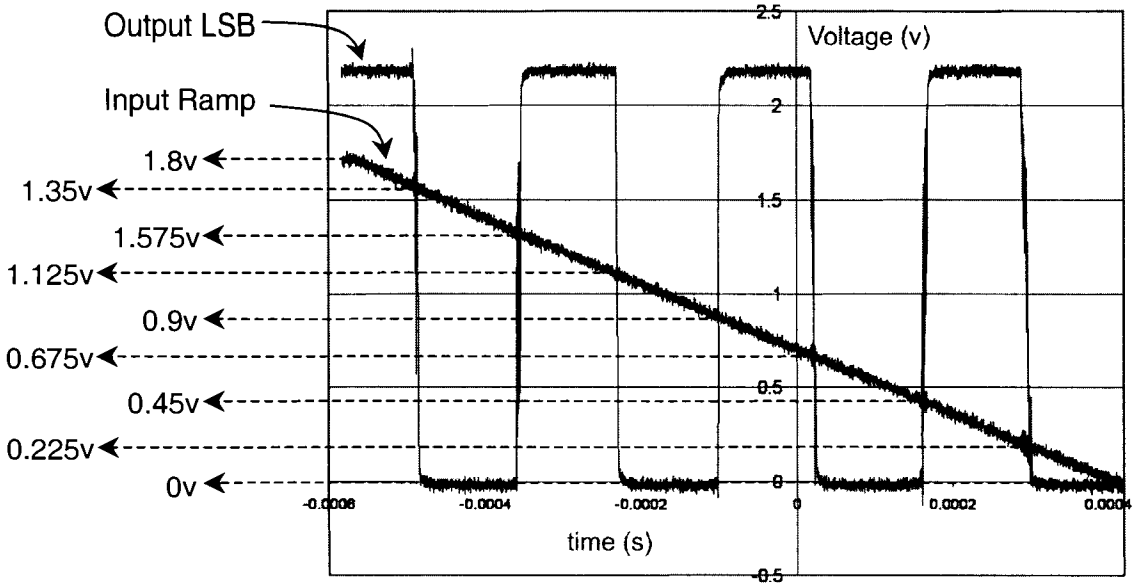


Figure 3.8: Least significant bit transition by the input voltage level.

3.2.2 Second Chip: The Entire ADC

This chip consists of the entire floating-point ADC of this project designed in the previous chapter. The 44CQFP package used for the second chip is good for operation frequencies up to 1.5 GHz [16].

First approach to test the chip was DC measurements. This means that besides biasing the chip for a correct performance, DC levels were provided to V_{in+} and V_{in-}. Performing such a test technique, one can take the output floating-point number and compare it to the expected result according to the biasing voltages of the chip. To do so and also to make the test and measurements easier, a test board was designed as shown in Figure 3.9.

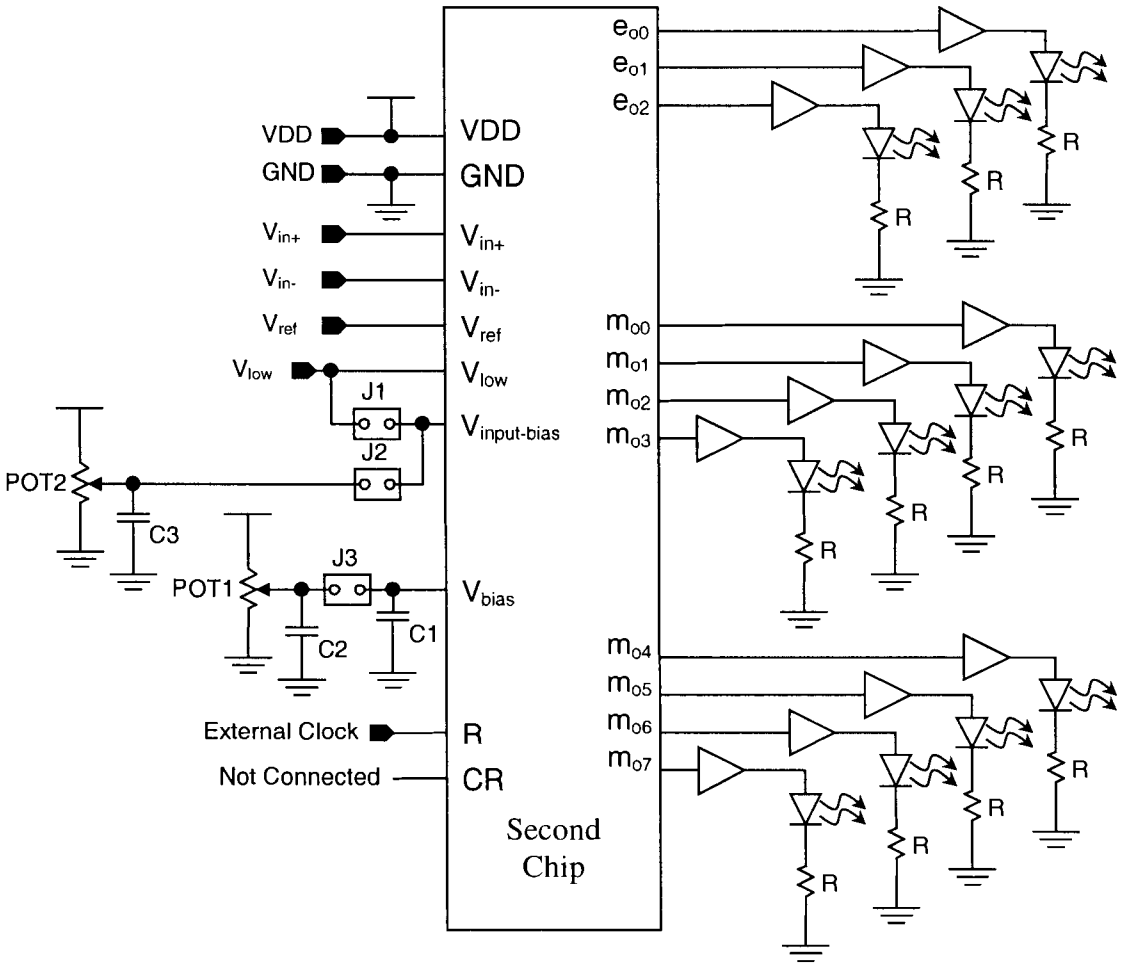


Figure 3.9: Schematic of the test board.

The Semiconductor Parametric Analyser (SPA) was used to provide DC voltages to the inputs of the chip as it can generate very accurate voltage levels. For the normal operation of the chip V_{low} and $V_{input\text{-}bias}$ have to be tied together. This has become possible by closing the jumper J1. But also to enhance the testability of the chip it is a good idea to have different voltage levels for these two pins. As the SPA can only provide six output channels, for extra signal levels voltage dividers were implemented using potentiometers for variable levels. These levels are filtered through capacitors for noiseless DC signals. POT2 potentiometer provides a DC level that can be fed to the $V_{input\text{-}bias}$ pin by closing the J2 jumper and opening the J1 jumper. V_{bias} is a pin that has to be connected to the ground through a capacitor (C1) so that the V_{bias} DC level is generated from the V_{bias} level generator circuit (Section 2.2.6). Also to enhance the testability of

the circuit, an external DC level generated through POT1 and C2 can be forced over V_{bias} by closing the J3 jumper. This way an external V_{bias} voltage level can be adjusted for the circuit in case of V_{bias} level generator circuit malfunctioning. Also to be able to more easily change the operation frequency of the chip, the clock generator circuit was bypassed. A clock signal was generated externally using a function generator and fed into the *R* pin of the chip.

As you can see in the test board above, all the output pins are buffered to light up an LED diode each. Three green LEDs and eight red LEDs were used to indicate exponent and mantissa bits respectively. Other components used are brought in Table 3.4.

Table 3.4: Components used in the test board.

R	POT1	POT2	C1	C2	C3	Buffers
220Ω	1KΩ	1KΩ	33μF	100μF	100 μF	HCF4050B

To start testing in the normal operation of the ADC, jumpers were set to J1 closed and J2 and J3 opened. The first thing tested was the V_{bias} level generator circuit (Section 2.2.6). This circuit is independent to the rest of the ADC circuits and therefore its characteristics are easy to measure.

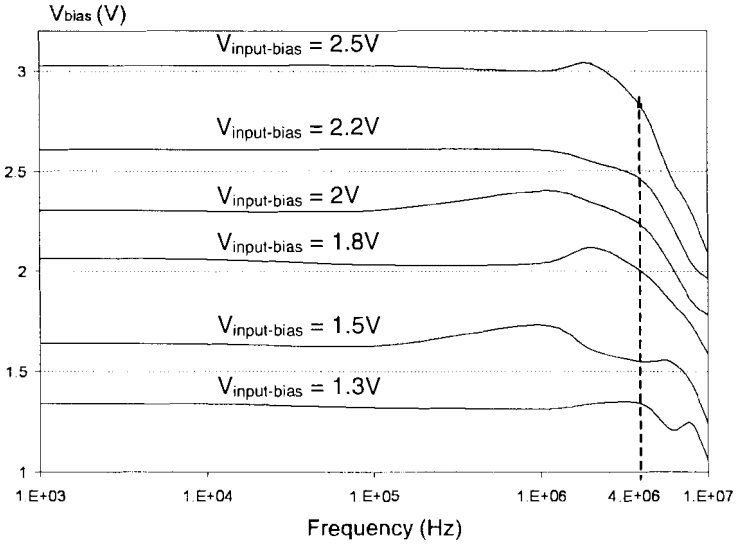


Figure 3.10: V_{bias} voltage generated for different $V_{input\text{-}bias}$ voltage and clock frequencies.

Therefore the circuit was powered up by VDD = 3.3V and GND = 0V and different $V_{input\text{-}bias}$ voltages and input clock frequencies were provided to this circuit. The V_{bias} voltage resulted from this measurement is provided in Figure 3.10. It is seen that the V_{bias} voltage generator is functional as the output V_{bias} voltage follows the input $V_{input\text{-}bias}$ voltage closely. Yet the resistive contacts between the chip and the test fixture could be affecting the outcome of the measurements. Unfortunately further measurements on this circuit along with many other measurements were not possible due to the limitations caused by the lack of test features and circuits in the chip. This issue is discussed in more details later in Section 3.2.3. From Figure 3.10 it is seen that the V_{bias} voltage level closely followed the $V_{input\text{-}bias}$, especially for lower $V_{input\text{-}bias}$ voltages and frequencies lower than 4MHz. This confirmed the proper functionality of the sub-circuits of the V_{bias} level generator circuit, hi-frequency and low-frequency OpAmps, Switches and digital components.

Testing the entire ADC circuit in its normal mode of operation didn't result in any kind of functionality. Observations showed that for different input signal levels (V_{in+} and V_{in-}) between zero and 3.3V output bits retained their values, which were all zero for exponent bits and all one for mantissa bits. Therefore to enhance the measurements the jumpers were rearranged to J1 opened and J2 and J3 closed. This allowed adjusting different values for V_{bias} and $V_{input\text{-}bias}$ using external bias network. Again the input signal levels to V_{in+} and V_{in-} didn't have any effects on the output bits. As mentioned before in Section 2.6, the input to the entire ADC circuit is a subtracter. The output of the subtracter goes directly to the non-uniform flash ADC of the VGA block, which generates the exponent bits. As the flash ADC circuit was previously tested in Section 3.2.1.2 and the circuit along with all its digital gates worked, the assumption is that the circuit is functional in the second chip too. Therefore the most probable source of circuit malfunctioning is in the input subtracter circuit. For some unknown reason the subtracter output doesn't react to any input signals, what suggests that it might be stuck at a constant voltage level.

Non-functioning of the input subtracter paralysed the functionality of the entire circuit. Yet using the method described below I was able to test 4-bit flash ADCs and their flip-flops. The general circuit for a flash ADC is repeated here for your convenience in Figure 3.11. The resistor array in the ADC generates reference voltages between V_{ref} and V_{low}. These references vary depending on the V_{ref} and V_{low} voltages. In the case of the 4-bit flash ADC of the pipeline, which has 16 equal resistors, there are 15 reference levels and 16 voltage ranges.

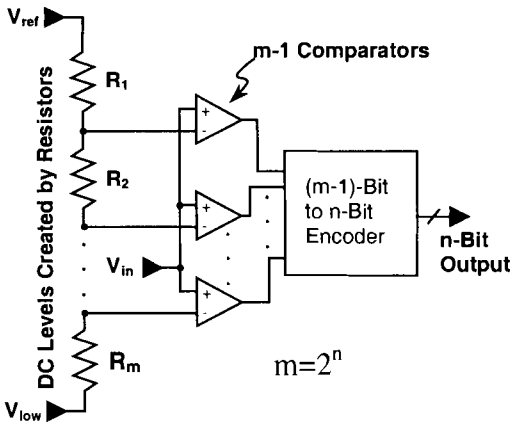


Figure 3.11: General flash ADC circuit.

As I mentioned before, all the mantissa bits remained high. It showed that the inputs to the 4-bit flash ADCs of the pipeline had values higher than the largest DC level generated through the flash ADC resistor arrays. There was no way to change the inputs of the flash ADCs. Therefore instead, I kept the flash ADCs input constant by giving constant voltages to the switched capacitor circuits. Then I set V_{ref} to 3.3V and swept V_{low} from zero to 3.3V. Figure 3.12 shows the result achieved by the sweeping of the V_{low} voltage. As I mentioned, the flash ADC input, V_{in}, is somewhere in the highest range of the flash ADC as shown in Figure 3.12. Sweeping V_{low} raises the reference levels too and they will pass V_{in} one by one. Passing every one of them over the V_{in} voltage results in a specific output binary number as shown in Figure 3.12.

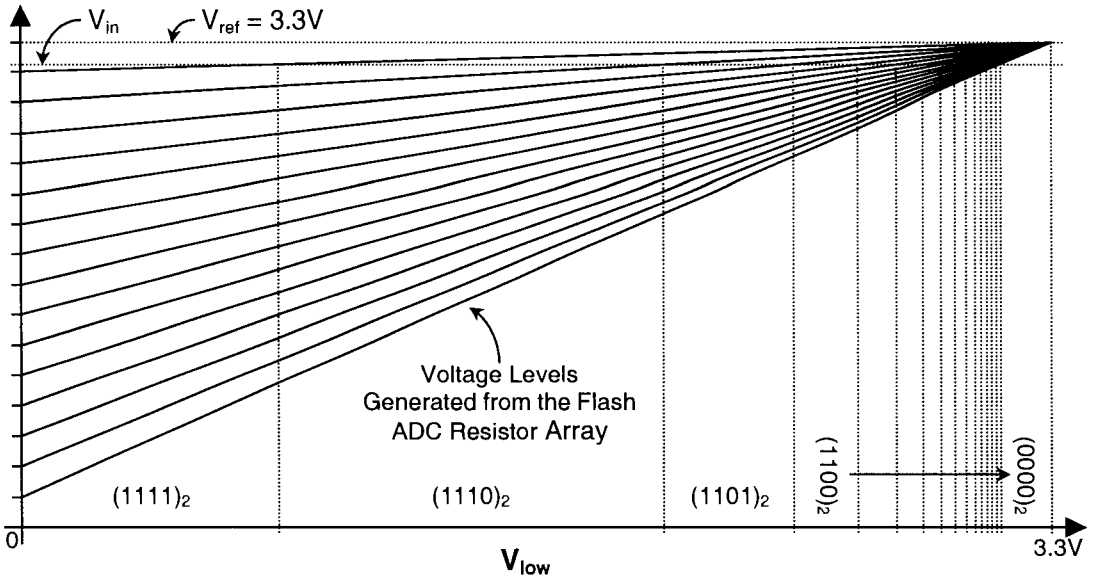


Figure 3.12: The change in the resistor array DC levels of the 4-bit flash ADC and its output resulted from the sweeping of the V_{low} voltage.

Testing the pipeline circuit as discussed above resulted in the same behaviour at the output mantissa numbers as shown in Figure 3.12. Therefore the functionality of the 4-bit flash ADCs and their relative flip-flops were tested. Also this confirmed the functionality of all the related sub-circuits of these components.

Clock Generator Test

In addition to the above tests, the clock generator circuit was also tested. As I mentioned above, for the ease of testing the circuit in many different frequencies, the clock generator circuit was bypassed. Actually this circuit is functional and applying external resistor and capacitor to the circuit resulted in the clock generation. Figure 3.13 shows the output waveform of the clock generator, the *R* pin, for a frequency of about 420KHz. Although the clock frequency is functional, it operates between 2 to 5 times slower than the post-layout simulation results indicate. Not only that, but also the clock generator doesn't work for frequencies higher than 1MHz.

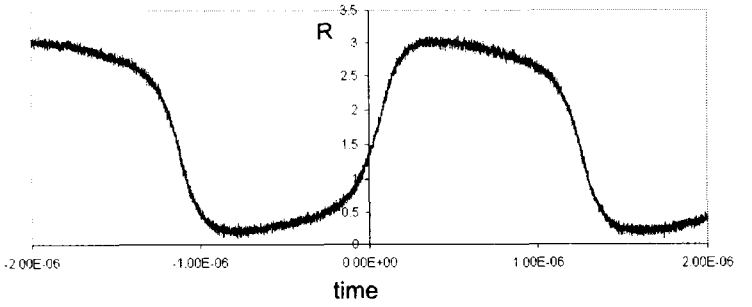


Figure 3.13: The *R* pin of the clock generator circuit.

Below in Table 3.5 clock frequencies resulted from the chip measurements are compared to the ones from the post layout simulations for C = 5pF and different resistor values.

Table 3.5: Comparison of the clock frequencies between chip measurements and post layout simulations for C = 5pF.

R	Clock Frequency	
	Chip Measurements	Post Layout Simulations
200KΩ	233KHz	514KHz
100KΩ	420KHz	1.1MHz
55KΩ	553KHz	2MHz
33KΩ	710KHz	3.5MHz
10KΩ		40MHz

This low frequency functionality of the clock generator is mostly due to the test fixture and probe parasitic capacitances. They were not included in the simulations because they were not supposed to be present in the circuit. All measurements were done using a Tektronix© active probe which features about 1pF and 1MΩ output load suitable for measuring frequencies up to 1GHz. Measurements showed putting this probe on the clock generator circuit alone reduces the frequency by at least 20% for frequencies around 300KHz. Adding a digital buffer to the circuit of the clock generator could make the parasitic capacitances less effective on the frequency, as shown in Figure 3.14. Adding the non-inverting buffer as shown in the figure above can significantly increase the output current of the Schmitt-triggered circuit.

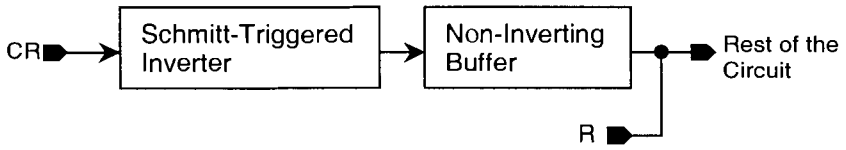


Figure 3.14: Adding a digital buffer to the Schmitt-triggered clock generator.

Therefore the effect of the parasitic capacitors will be reduced and the circuit will be capable of working in high frequencies as the post-layout simulation results suggested.

3.2.3 Test Results Discussion

Although the entire ADC circuit didn't operate, testing the second chip proved the performance of a few blocks such as the V_{bias} generator circuit, 4-bit flash ADC and its flip-flops and the clock generator circuit. These sub-circuits include the circuits of the V_{bias} generator circuit: high-frequency high-current OpAmp (Section 2.2.1), low-frequency OpAmp (Section 2.2.3), switches (Section 2.2.2) and inverter buffers (Section 2.3.1) and therefore the gain-of-2 switched capacitor amplifier (Section 2.2.4). Also the functionality of the sub-circuits of the 4-bit flash ADC and d-flip-flop was tested. They include: all the digital gates including inverters (Section 2.3.1), 2-input *AND* and *NAND* gates (Section 2.3.2), 2-input and 4-input *OR* gates (Section 2.3.3), d-flip-flop (Section 2.3.4) and 15-to-4-bit encoder (Section 2.3.6). Also the clock generator circuit (Section 2.3.5) was tested. Knowing that the 7-to-3-bit encoder was tested previously in the first fabricated chip, all the digital components of Section 2.3 were tested.

I was unable to test the non-uniform 3-bit flash ADC in the second chip. Yet testing a uniform 3-bit flash ADC circuit in the first chip in Section 3.2.1.2 proved the operation of the 3-bit ADC. The components that were not tested due to the limited testability include the gain-of-4 and gain-of-16 VGAs, subtracters and 4-bit DAC circuit.

The limited testability of the chip is caused by the very small chip area (1mm x 1mm) granted by CMC instead of my initial request of 2mm x 2mm area. As it is obvious from the layout and package wiring of the chip shown previously in Figure 2.92 and Figure 2.93, not only

the area of the chip has been used almost completely, adding even one extra pad would be extremely challenging. This was the reason I was unable to add any extra testing features to the chip. In case of having enough area I could add the following features to the chip to enhance the testability:

First, circuit components could be added separately to the chip so that they could be tested alone. This way the functionality of all the components could be tested and information would be provided on their performance and how to improve them to work better in the ADC circuit.

Second, instead of one solid ADC circuit, switches could be added to the circuit as shown in Figure 3.15. Setting the *Test* signal to a logical high disconnects both the input and output of a specific block and connects them to the output pins of the chip. Setting the *Test* signal to zero returns the block in its position in the ADC circuit, which enables the test of the entire ADC circuit as one circuit. Analog buffers maybe required for achieving the full speed operation of different blocks. Therefore all major blocks such as VGAs, amplifiers, subtracters, flash ADCs and DAC could be tested separately using this method.

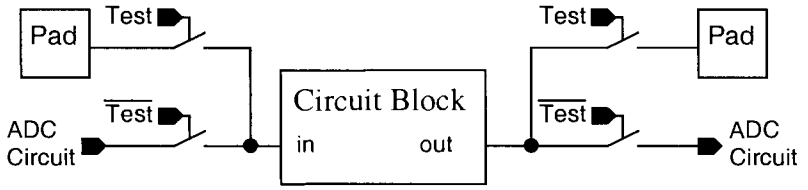


Figure 3.15: Increasing the testability of the blocks by adding switches and pads.

Third, adding multiplexers to digital circuits, many output digital signals could be sent to on output pin as shown in Figure 3.16. In this figure the select bits can select a specific input to be sent to the output for measurement. This is a great way to test many digital signals by adding a few more pins. But as the functionality of the digital components were tested in the first chip this option was not necessary and would be used in case of having an adequate silicon area.

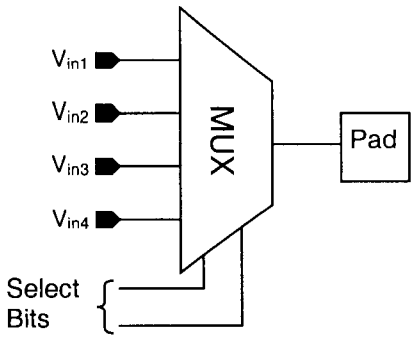


Figure 3.16: Multiplexing digital signals to measure them separately on one output pin.

Having the option of adding the above test features to the chip could allow very efficient tests of the components. To enable such features in the chip adding many pads along with more circuitry was required, which would consume an area much larger than $1mm^2$ granted to me by CMC. Yet as described before, in spite of having testing limitations, many of the circuit components were tested and their operations were confirmed.

3.3 Conclusion

An 11-bit floating-point pipelined ADC was presented in this project. This ADC was designed to have low power consumption and silicon area usage while having a high dynamic range to be integrated with other mixed signal components, especially in integrated sensor systems. To design the ADC circuit, first of all a suitable topology was chosen: an 11-bit floating-point pipelined ADC. One of the advantages of this topology is the saving in the number of output bits while keeping a high dynamic range. Because a high dynamic range was required to convert the sensor signals, a uniform ADC would have more output bits and therefore more circuitry to generate those bits. Instead, a floating-point ADC only samples the input signal with a required precision (here with a peak of 48dB). Therefore eliminating the extra precision resulted in smaller circuit and thus much smaller power consumption and silicon area usage.

To design the circuit after choosing the topology, circuit was divided into major blocks: the VGA block and the 8-bit pipelined ADC block. To achieve the required performance for each

block, they were further divided into smaller blocks. The VGA block was divided into three VGAs in series as mentioned before in Section 0: gain-of-16, gain-of-4 and gain-of-2 VGAs. These VGAs were controlled by the output bits of a non-uniform 3-bit flash ADC and flip-flop arrays. The pipeline block was an 8-bit uniform ADC that was divided into two stages that each would extract 4 bits of data. The VGA block extracts the 3-bit exponent number and the pipelined ADC extracts the 8-bit mantissa number of the final 11-bit floating-point number. After breaking the circuit into the required blocks, all sub-circuits were designed in 0.18μm CMOS technology. The analog components designed include high and low frequency OpAmps, comparator and analog switch. Designed digital components include inverters, *AND* and *NAND* gates and *OR* gates which also combined to produce d-flip-flop and encoders. Also a clock generator was designed to produce the clock phases required for the ADC circuit. These sub-circuits were combined further to generate larger components such as switched capacitor VGAs and subtracter, biasing DC generator, 3-bit non-uniform ADC and 4-bit uniform ADC. And at the end all the components were put together to become the floating-point ADC of this project.

The comparison between the properties of the designed ADC and the one presented in [2] has shown promising results, as seen in Table 3.1. The power consumption was reduced by 7.6 times and the silicon area usage was reduces by 16.4 times for the designed ADC of this project. To achieve these properties the peak SNR and sampling rate of the circuit were compromised and yet both circuits have the same dynamic range of 90dB. Therefore it is concluded that the designed floating-point ADC of this project is much more suitable to be integrated along with other mixed signal components within the integrated sensor systems.

Beside the circuit designs, all the circuits were also fabricated into two chips. First one included the essential components of the ADC such as the gain-of-2 VGA and 3-bit flash ADC. Testing this chip confirmed the operation of these components and their sub-circuits. In the second chip the entire ADC didn't function as one unit and some of the circuit components

remained untested. This was due to the limited testability resulted from the small area of $1mm^2$ granted by CMC. Yet the second chip measurements successfully confirmed the functionality of many of its sub-circuits and components.

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