NOISE ANALYSIS OF A CURRENT MEDIATED ACTIVE PIXEL SENSOR FOR DIGITAL IMAGING

By:
Alireza Nezamzadeh
B.Sc. in Electrical Engineering, Kerman University, Kerman, 1991

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Name: **Alireza Nezamzadeh**

Degree: **Master of Engineering**

Title of project **Noise Analysis of a Current Mediated Active Pixel Sensor for Digital Imaging**

Chair: **Dr. Bonnie Gray**
Assistant Professor
School of Engineering

Examining Committee:

Dr. Karim S. Karim
Assistant Professor
Senior Supervisor, School of Engineering, SFU

____

Dr. Ash M. Parameswaran
Professor
Supervisor, School of Engineering, SFU

____

Date Defended/Approved: November 30, 2004

ABSTRACT

Crystalline silicon active matrix imagers have gained prominence due to their highly integrated nature in digital imaging applications ranging from star trackers to monolithic integrated circuit cameras. In this project, the operation and noise performance of a pixel with current mediated readout (C.M.APS) is investigated. The total output noise power spectral density (PSD) is theoretically calculated using small signal analysis to obtain the noise contribution of each pixel component as well as the overall pixel noise transfer function. The theoretical work is compared to results obtained from a circuit simulated in state-of-the-art complementary metal-oxide-semiconductor (CMOS) 0.35μm technology using the Cadence integrated circuit design environment. Signal gain, noise, noise bandwidth and frequency response results are presented. Results indicate that, in contrast to a C.M.APS pixel operating in Direct Mode, a C.M.APS pixel operating in Difference Mode allows suppression of fixed pattern noise components without causing an increase in random noise components.

DEDICATION

This work is dedicated to my family

for their unconditional love and support

in all aspects of my life

ACKNOWLEDGEMENTS

I would like to thank my senior supervisor Dr. Karim, S. Karim for his encouragement, guidance, feedback and direction throughout the duration of my research and for his constant belief in my potential during the last fifteen months as a researcher. Without the initiative, perseverance and sound leadership of Dr. Karim this project would never happened.

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ABBREVIATIONS AND ACRONYMS

AC	Alternative Current
APS	Active Pixel Sensor
CCD	Charge Coupled Devices
CMOS	Complementary metal-oxide-semiconductor
C.M. APS	Current Mediated Active Pixel Sensor
CMOSP35	CMOS 0.35μm fabrication technology
DC	Direct Current
FPN	Fixed Pattern Noise
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field Effect Transistor
PSD	Power Spectral Density
PRNU	Photo-response non-uniformity
V.M. APS	Voltage Mediated Active Pixel Sensor

CHAPTER ONE
INTRODUCTION

Crystalline silicon active matrix imagers have gained prominence due to their highly integrated nature in digital imaging applications ranging from star trackers to monolithic integrated circuit cameras. They offer the advantages of small area and being highly integrated which makes them simple to operate [1]-[5].

Integrated image sensor technology offers the benefits of cost effective, imaging and on-chip signal processing functions leading to higher image quality. These days, CMOS imagers compete with CCDs (Charge Coupled Devices) in industry for low cost, low power applications with on-chip signal processing.

CCDs have a simple architecture consisting of a MOS photosensitive capacitor, a parallel shift register, a serial CCD shift register, and a signal sensing output amplifier [6]. Photon charge captured by photo capacitor is shifted along a row of pixels to a charge sensitive read out amplifier. The charge on each row is shifted one row down, as shown in Figure 1-1, and then readout through the serial shift register.

Image acquisition using CCDs is performed in three steps:

1) Exposure, where light is converted into an electronic charge at discrete sites, called pixels.

2) Charge transfer, which moves the packages of charge within the silicon substrates from pixel to neighboring pixel.

3) Charge to voltage conversation at the output amplifier.

The charge storage and transfer operation in a CCD is shown in Figure 1-2. Circles represent the electric charges stored in the pixel potential wells. The charge is stored in MOS capacitors at each pixel and is transferred in between adjacent potential wells at or near a Silicon Dioxide interface. The charges

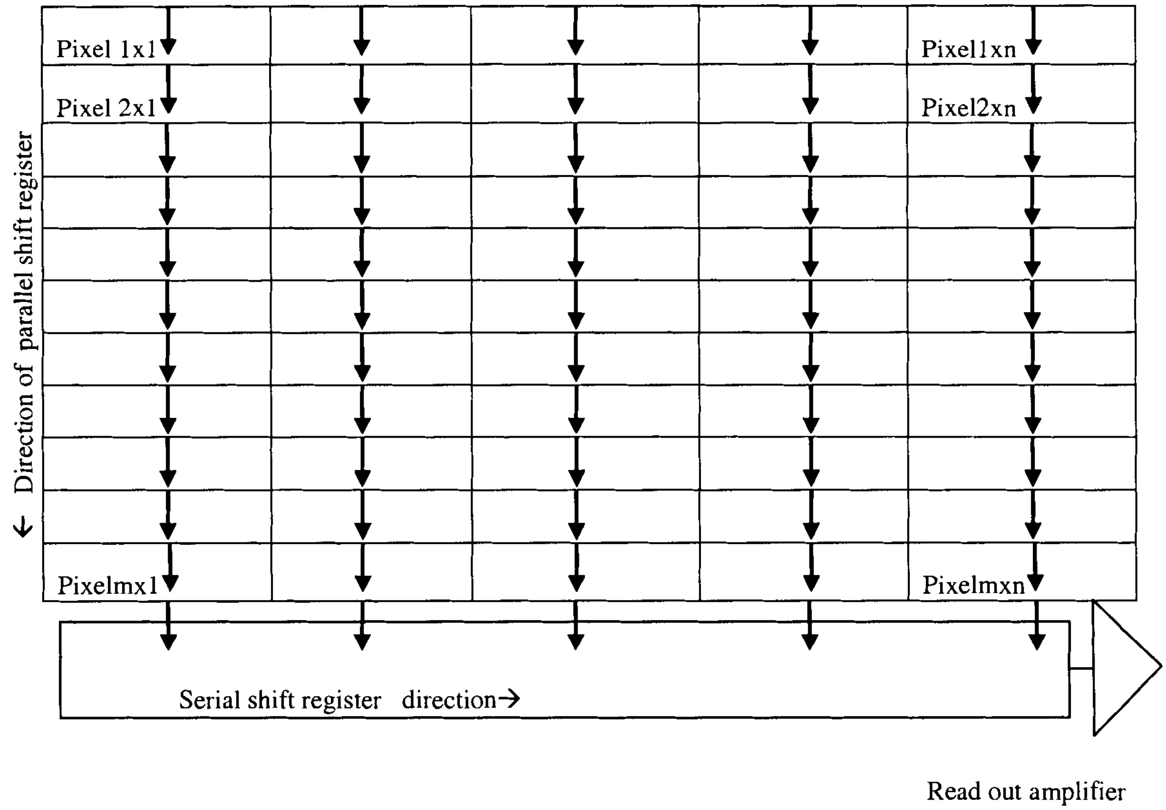

Figure 1- 1: Charge transfer in a CCD

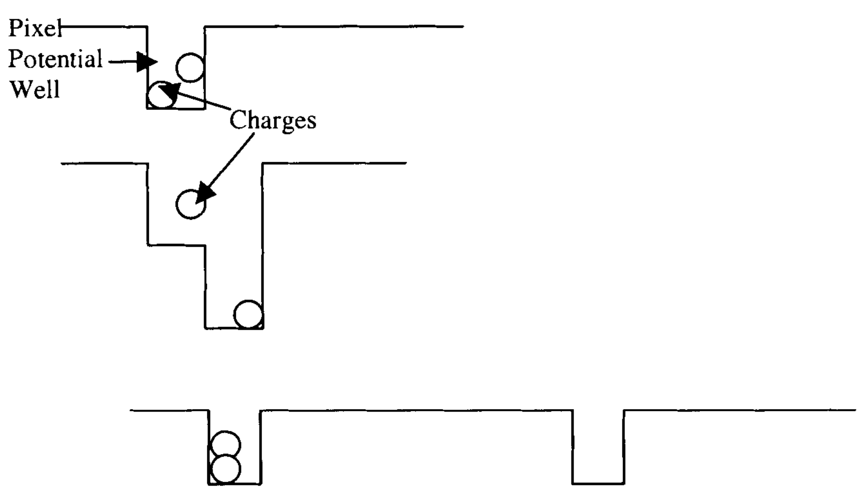

Figure 1- 2: Charge storage and charge transfer in adjacent potential wells pixels in CCDs

filled in the wells can be transferred to the adjacent wells by clocking the adjacent gate. In this fashion, readout of pixels is possible sequentially.

A drawback of CCDs is that they are manufactured in select foundries using a specialized process. In contrast, CMOS foundries are more common. Also, unlike CCDs CMOS technology offers highly integrated image sensors with on chip signal processing to designers.

A CMOS image sensor usually consists of an active matrix array of pixels where the photo charge is transferred out by row select logic. A block diagram of a CMOS imager is shown in Figure 1-3. Here column parallel readout is performed by reading out each row simultaneously via the column readout circuits.

CCDs transfer packages of charge sequentially within the silicon substrates from pixel to neighboring pixel (serial output), but in CMOS, output pixel signals are readout in parallel through bus lines, hence eliminating the signal

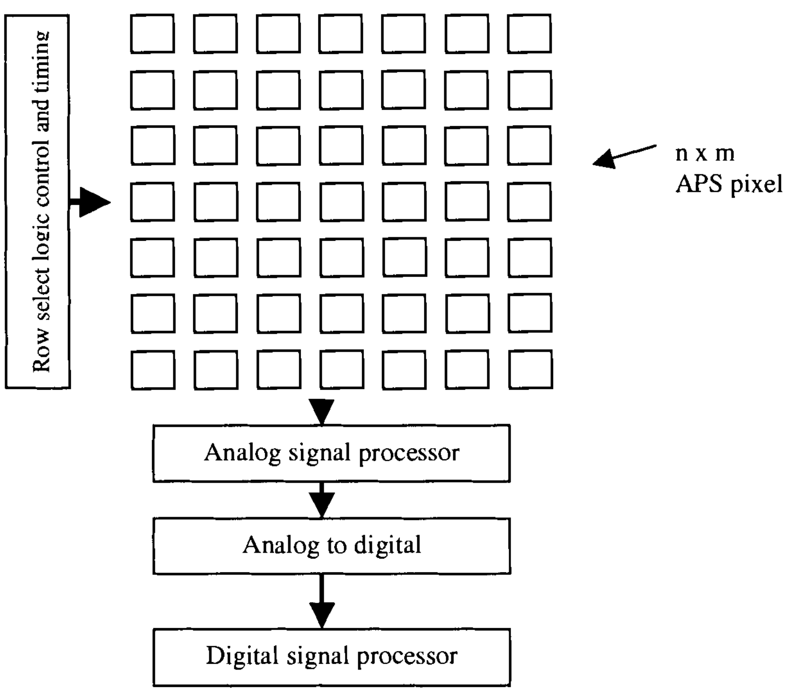

Figure 1- 3: CMOS image sensor architectural block diagram

degradation due to CCD charge transfer inefficiency within the silicon substrates. This allows fast and selective column readout.

Differences between CCD and CMOS image sensors lie in their sensitivity, power consumption and their cost. CMOS imagers have more transistors and therefore can have less fill factor and less sensitivity. Therefore, CMOS sensors have the ability to integrate timing control units, analog and digital signal processors on a single chip. The integration of all these support circuits leads to low cost and more reliable products compared to CCDs [6].

In this report, we will investigate the noise properties of a CMOS sensor for digital imaging application. In Chapter 2, we introduce some common pixel architectures in CMOS technology. In Chapter 3, we perform a noise analysis of a current mediated active pixel sensor that has the potential to suppress fixed pattern noise. In Chapter 4, we summarize and conclude our work.

CHAPTER TWO

Active Pixel Sensors in CMOS Technology

An active pixel sensor (APS) is a pixel containing one or more transistors acting as amplifiers within the pixel unit cell.

2- 1 Voltage Mediated Active Pixel Sensor (V.M. APS)

The basic form of one of the most popular V.M. APS employs a photosensor and a readout circuit consisting of three transistors [1] as shown in Figure 2-1.

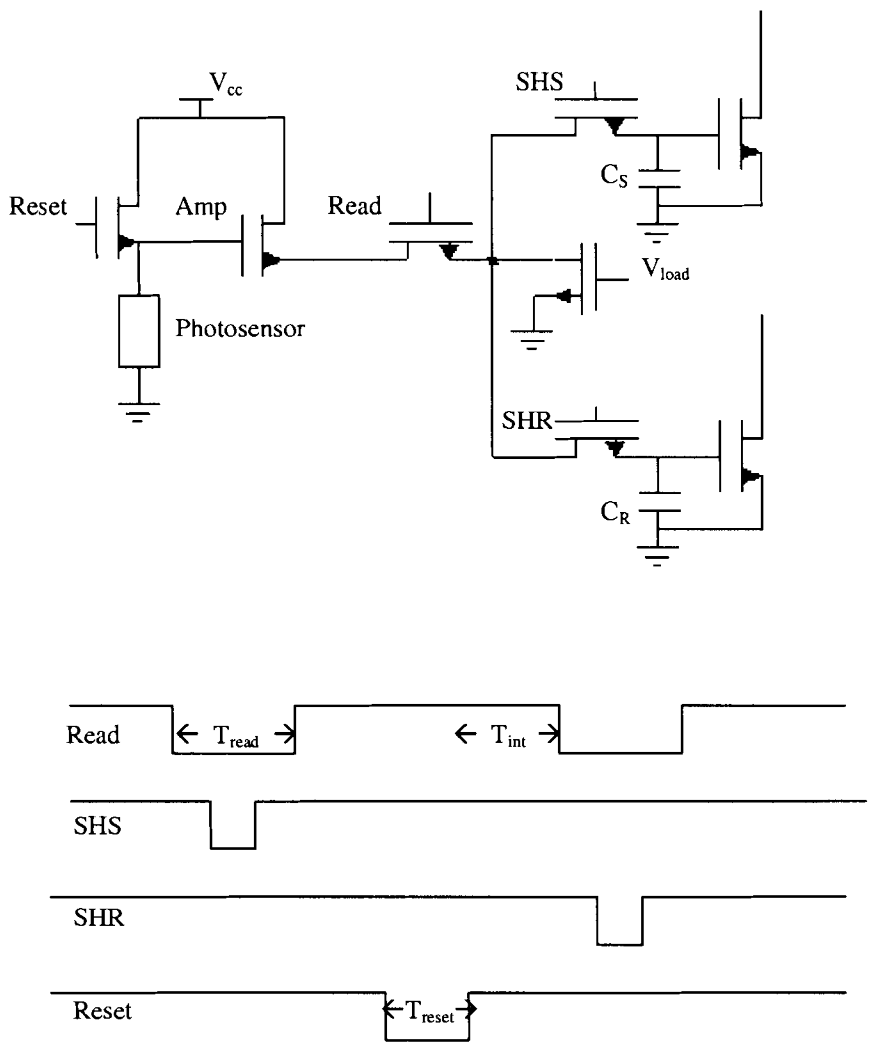

Figure: 2- 1: Schematic and timing diagram of sample and hold read out circuit for Voltage Mediated APS

The circuit operates in three phases: charge integration, read and reset. In the integration phase, the reset and read transistor is switched off for the integration period T_{int} (integrate time). During reset, the reset and read transistor is on and in the read out phase, only the readout transistor is on.

If a photogate is used as a photosensor, the pixel is called a photogate pixel, and if a photodiode is used, the pixel is called a photodiode pixel. During the reset phase, the reset transistor is switched on and the photosensor charges to V_{DD} -V_{Treset}. For the read out phase the read transistor is switched on for a sampling time T_{read}, and photosensor charge is relayed via read transistor to the output.

The Amp transistor acts as a voltage buffer to drive the output independent of the diode. The Read transistor allows random access to each pixel enabling selective readout. In a V.M. APS the output voltage signal is proportional to photosensor voltage (V_{sense}) subtracted by threshold voltage of Read transistor.

$$V_{out}=V_{sense} - V_{Tread} \quad (2\text{-}1)$$

Therefore, the output signal changes linearly with the photosensor's voltage.

Sampling the signal level permits correlated double sampling (CDS), which can suppress pixel noise and threshold voltage variation in transistors due to CMOS process non-uniformity [8].

Each sample and hold circuit consists of a sample and hold switch, a capacitor and a column source follower to buffer the capacitor voltage. Pixel out put signal is sampled at two different times and the resulting output is the difference of two samples. The first sample is the data signal, then the pixel is reset and the second sample occurs which corresponds to the reference signal. This pseudo differential sampling removes the correlated noise between the reference and the data signal. Reference capacitor (C_R) holds the reset value, and signal capacitor (C_S) holds the signal added to the new value of noise, as shown in Figure 2-2. Note that additional components can add further noise to the signal such as kTC Noise from sample and hold capacitors and Flicker Noise from the transistors [8]. However, the added noise is usually less than the pixel noise.

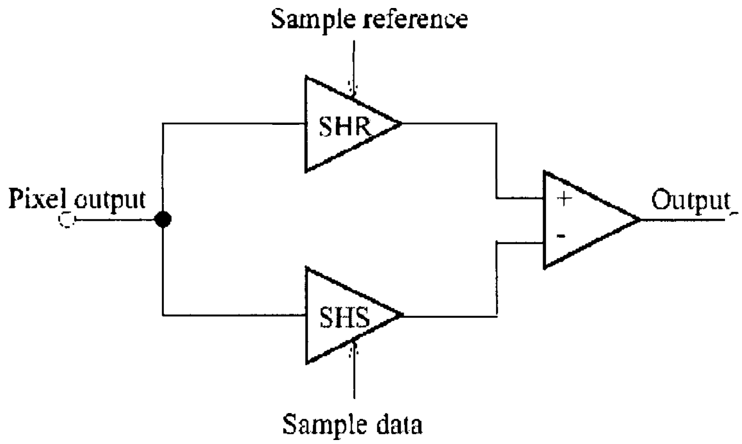

Figure 2- 2: Correlated double sampling block diagram

2- 2 Photodiode Pixels

The basic form of a photodiode pixel is a reverse biased p-n junction coupled

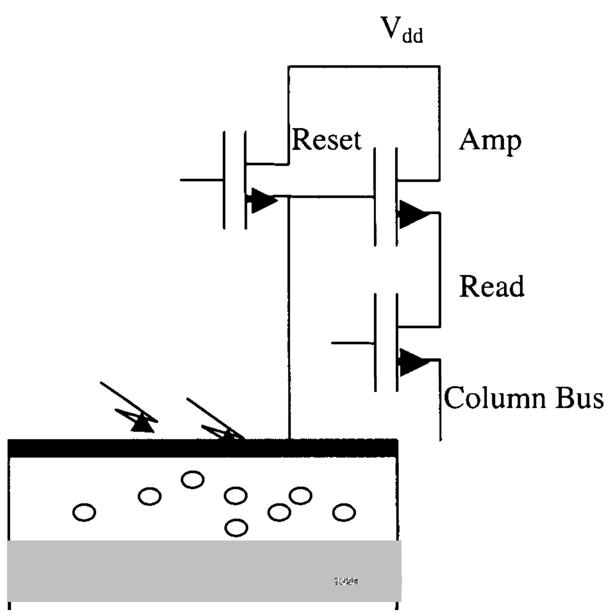

Figure 2- 3: Photodiode APS

to an APS circuit. Photodiodes are the most common detector used in APS CMOS circuits. They convert light to current and transfer it to a high input impedance common drain amplifier, as shown in Figure 2-3. A typical fill factor is 20-35% [14], and the peak quantum efficiency of photodiode pixel is about 40% at green wavelength, which is low compared to CCDs [14], and the photogate pixel discussed next.

2- 3 Photogate Pixels

A CMOS photogate APS is shown schematically in Figure 2-4. This APS sensor consists of a photogate, biased positively, which creates potential well and provides storage for the photo generated charge.

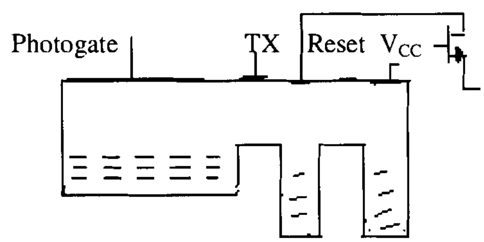

Figure 2- 4: Photogate APS

A transmission gate, *TX*, is DC biased during integration. When the photogate is pulsed to 0*V*, charge is transferred under the *TX* gate to the floating diffusion (*FD*) output node. The structure and operation of the CMOS photogate APS is more complex than the photodiode APS, but photogates offer an improvement in noise suppression and greater quantum conversion gain. A disadvantage is poor quantum efficiency that almost offsets the higher gain [13].

2- 4 Current Mediated Active Pixel Sensor (C.M. APS)

The C.M. APS offer the advantages of compact size and simple design [5]. In the 700nm process, the pixel occupies a 15x15 μm area, allowing almost

400,000 pixels to be placed in 1-*cm* die. The nonlinear photon-to-output signal transfer function of this pixel, however, must be considered [2].

A C.M. APS pixel is displayed in Figure 2-5 and the timing diagram is shown in Figure 2-6

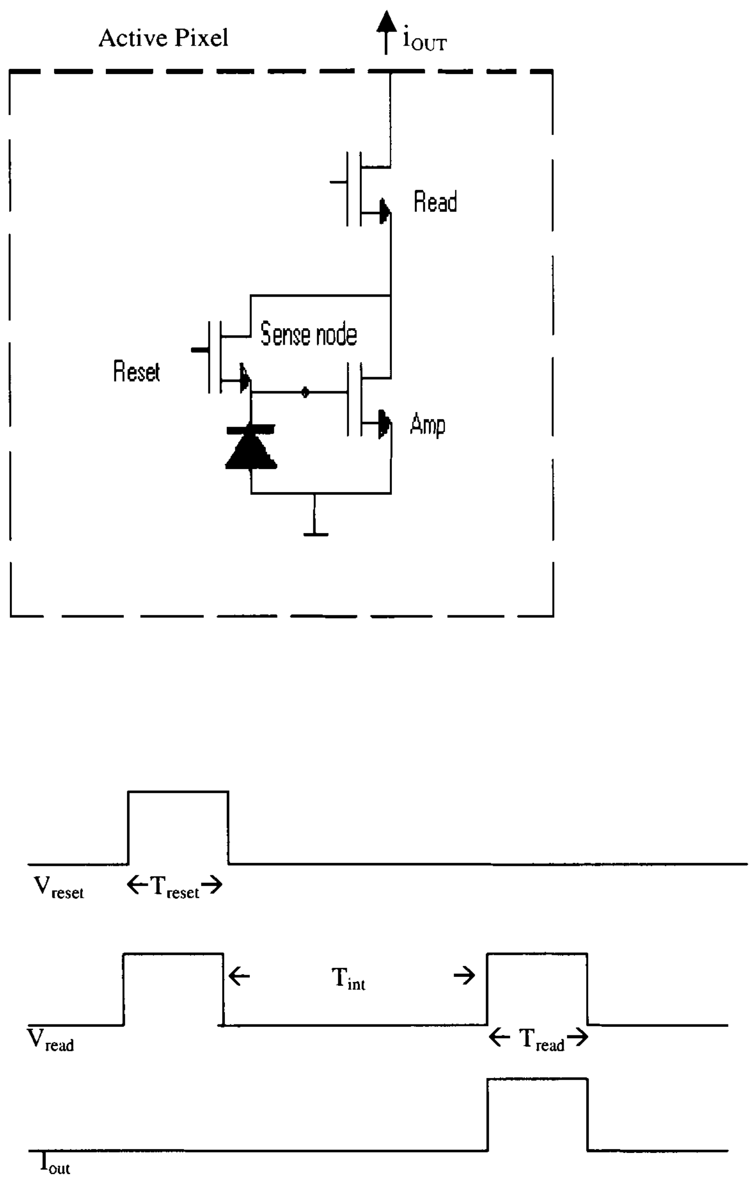

Figure 2- 5: C.M. APS schematic and timing diagram

The output signal appears as a current proportional to the square root of sense node voltage and threshold voltage of Read transistor. Therefore, output current is highly sensitive to threshold voltage, and the spatial noise in C.M. APS is higher than V. M. APS.

The current of Read (Select) transistor is determined by:

$$I_D = \frac{K^{'}}{2}(V_s - V_{TAmp})^2 \quad (2\text{-}2)$$

Where:

$$K^{'} = \frac{\mu C W}{L} \quad (2\text{-}3)$$

W is width of T_2,

L is Length of T_2,

μ is Mobility,

and C is capacitance per unit area of Silicon Dioxide.

The sense node capacitance (C_S) is composed of both the gate capacitance of the active device and the voltage dependent photodiode depletion capacitance. A calculation based on the pixel layout over the range of voltage expected in normal operation, (0.8 to -2.0 *V*), shows that it varies between 27.2*fF* and 23.5*fF*, with an average value of 26.1*fF* [5].

Neglecting the variation of this capacitance, the sense node voltage at time *t*, $V_s(t)$, can be written as [10]:

$$V_s(t) = \mathrm{V_s}(0) - \frac{1}{\mathrm{C_s}}\mathrm{I_{ph}}.\mathrm{t} = V_s(0) - q\frac{\mathrm{N_e}}{\mathrm{C_s}} \quad (2\text{-}4)$$

Where N_e is the number of electrons integrated onto the sense node and I_{ph} is the photo current of photosensor.

As shown in Figure 2-6 the C.M. APS can be used in Direct Mode (without a reference current) and Difference Mode (with a reference current) [5]. Reference current can be injected to pixel by an external switch.

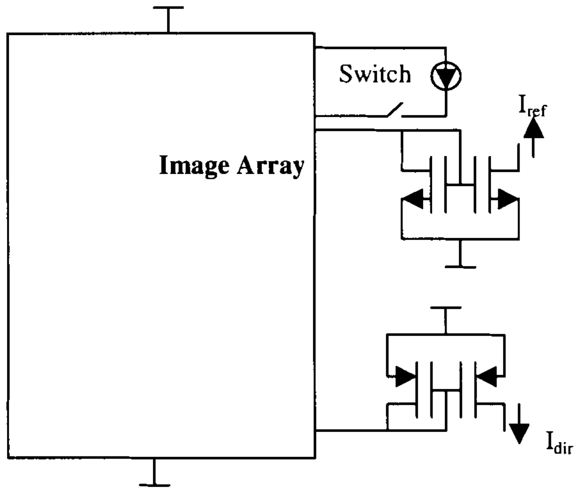

Figure 2- 6: C.M. APS in Difference Mode and Direct Mode

2- 5 C.M. APS in Direct Mode

In Figure 2-7 the pixel output current is applied to current mirror directly. This readout method is called Direct Mode.

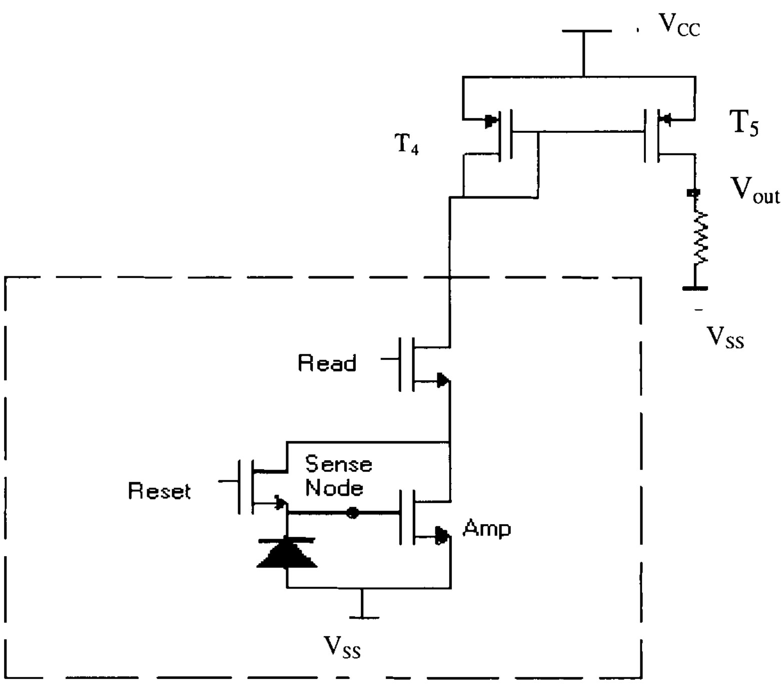

Figure 2- 7: C.M. APS in Direct Mode series with current mirror

Transistor T_2 of C.M. APS in Direct Mode operates in saturation region. Drain Source current of T_3 transistor, output current, is identical to drain current of the T_2 transistor.

When C.M. APS operates in reset mode, all T_1, T_2, T_3 and T_4 switches are closed. The drain current flowing through T_3 is equal to the current that flow to Drain Source of T_2. The gate voltage of T_2 at sense node is then reset to a value proportional to the current that flow through Drain Source of T_2.This voltage is stored on the sense node capacitance. Thus the pixel output signal is independent of the threshold voltage of the active transistor, T_3.

During signal integration T_1 and T_3 are open, and photo generated current reduces the voltage of reverse-biased diode at the sense node. Readout can be done nondestructively by closing the row-select switch. Thus the operational sequence is reset, integration and readout.

In order to amplify the drain source current of T_3, drain of T_3 is connected to the current mirror T_4 and T_5, which have different aspect ratio. In other words the circuit works in Direct Mode with a current multiplication factor *n*, proportion to width and length of the transistors, *W* and *L*:

$$I_5 = I_4 \frac{W_5 L_4}{W_4 L_5} \qquad (2\text{-}5)$$

When incident photons on the photo sensor, electron-hole pairs are created leading to a change in the charge at the integration node. The change, due to a sensor input, in the charge detection node bias voltage (V_G) is:

$$\Delta V_G = \frac{\Delta Q_P}{C_{pix}} \qquad (2\text{-}6)$$

Where ΔQ_P is the change in the input signal charge of the sensor node, capacitor C_{pix}, due to incoming photons and V_G is the corresponding change in the integration.

During small signal operation, the change in the output current respects to change in the gate voltage of T_2, ΔV_G, i.e. $\Delta I_{out}=n.g_m\Delta V_G$, where n is the current mirror multiplication factor and g_m is transconductance of the transistor T_2 and T_3.

2- 6 C.M. APS in Difference Mode

Another approach to read out of the output pixel current is shown in Figure 2-8. A current source is used to inject current to drain of select transistor, T_3. Then the difference of I_{ref}-I_{pix}, is steered to NMOS current mirror. The external set-switch enables the pixel signal current to be read in one of two out put modes. In Direct Mode readout, the column reference current sources are disabled and the pixel current is directed to a PMOS current mirror.

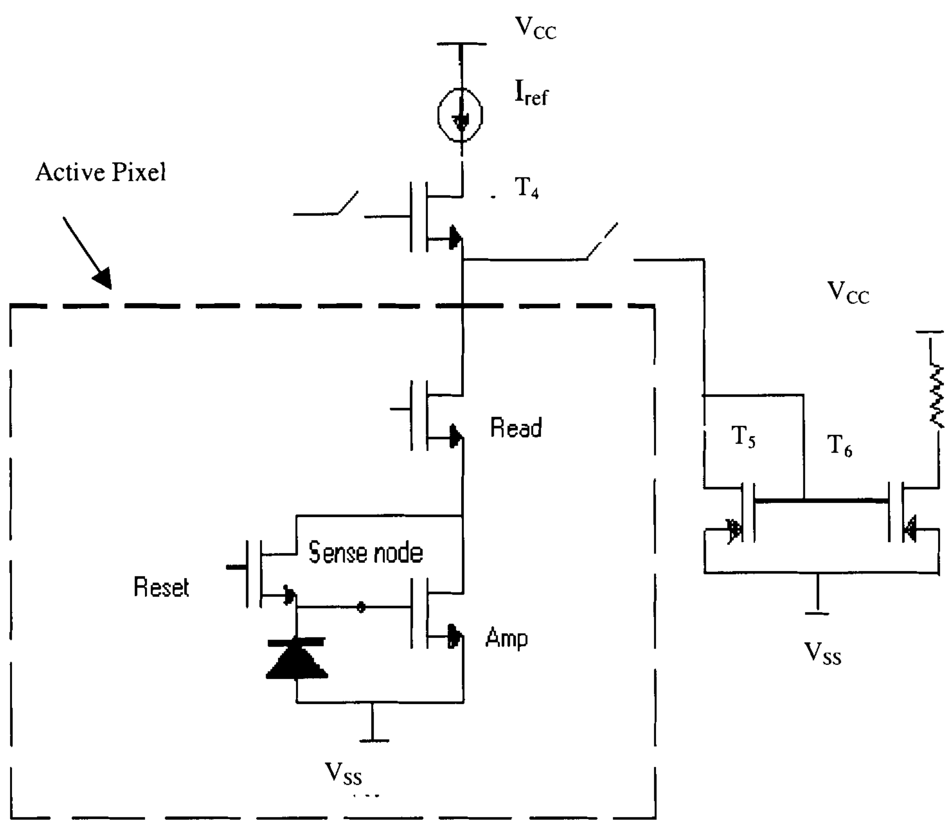

Figure 2- 8: C.M. APS in Difference Mode series with a current mirror

In Difference Mode, the switch is turned on and the difference current between the reference and the pixel signal current is directed to an NMOS current mirror. In Direct Mode the switch is off and the current source is not used. Difference Mode read out reduces fixed pattern noise due to mismatches in the column current sources [2], because the sense node voltage in reset mode is proportional to I_{ref}.

CHAPTER THREE
NOISE ANALYSIS OF C.M. APS

3- 1 Outline

The overall performance of each system is limited by noise that is added by the system to signal. In order to know the sensitivity of a pixel and minimum signal that can be detected, we have to know the total input noise of the pixel. In this chapter, the random noise and sensitivity of both C.M. APS in Difference Mode and Direct Mode is calculated and compared to simulation results.

In order to analyze these APS circuit, an AC equivalent circuit for each APS must be generated. Small signal circuit analysis is performed to extract the pixel transfer function, which is used to yield the output Power Spectral Density (PSD). Each circuit is simulated in Cadence to extract its electrical parameters, calculate the input current noise of each component, and finally calculate and plot the output noise.

3- 2 Noise in CMOS Imaging Pixels

CMOS image sensors suffer from noise more than CCDs due to the additional pixel and column amplifier transistors that generate Thermal and Flicker Noise. The overall performance of the sensor is ultimately limited by the noise that is added to signal. In this sense, the actual implementation of the system is limited by noise. Noise comes from numerous sources and its minimization requires optimization of many individual parts of the system. Our analysis will not consider external noise source, such as electrical pick-up. Noise in image sensors comes from typically either spatial noise or random noise sources.

3- 3 Spatial Noise

Mismatches in electrical characteristics of the pixels' components, such as those in the current mirror ratio and the component providing a threshold voltage drop, result in a fixed pattern output current variations at flat-field illumination.

Pattern noise is effectively a spatial noise and does not change significantly from frame to frame. Basically, it is non-uniform across the array; e.g. differences in the signal generated by individual pixels to uniform illumination. Spatial noise is divided into two components, fixed pattern noise (FPN) and photo-response non-uniformity (PRNU).

- FPN is the component of pattern noise measured in the absence of illumination and it is mainly due to variations in detector dimensions, doping concentrations, contamination during fabrication and characteristics of MOSFETs (doping, threshold voltage, gain, *W* and *L*). Fixed pattern noise is due to pixel-to-pixel variations in the absence of illumination and the main cause of FPN in CMOS imagers is variations in threshold voltage between MOSFETs (in the pixel and in the column). Also irregularities in the array clocking can cause the FPN.
- PRNU, photo response non-uniformity, depends on p-n diode detector dimensions, doping concentrations, thickness of over layers and wavelength of illumination. PRNU is signal dependent [9].

3- 4 Random Noise

Random Noise is expressed in terms of parameters, which describes the statistical distribution of signal voltage or current. Random noise is a phenomenon caused by small fluctuations of the analog signal. The average of this signal is zero.

Noise results from the fact that electrical charge is not continuous but the result of quantized behavior and is associated with fundamental processes in a semiconductor component. In other words, it is due to the fact that electrical charge is not continuous, but is carried in discrete amount equal to the charge of an electron. In essence, noise acts like a random variable and is often treated as one [4]. If there are n samples of the signal, then the mean is:

$$X = \frac{X \ + X_2 + X_3 + \ldots + X_n}{n} \tag{3-1}$$

However, the mean for many noise sources is zero (leaving the DC level of the signal unaffected). So, a more useful description of the noise is either the variance or the standard deviation. Standard deviation is given by:

$$< X >= \sqrt{< X_1^2 > + < X_2^2 > + < X_3^2 > + ... < X_n^2 >} \qquad (3\text{-}2)$$

When noise voltages are produced independently and there is no relationship between the instantaneous values of the voltages, they are uncorrelated. Two waveforms that are in identical shape are said to be 100%

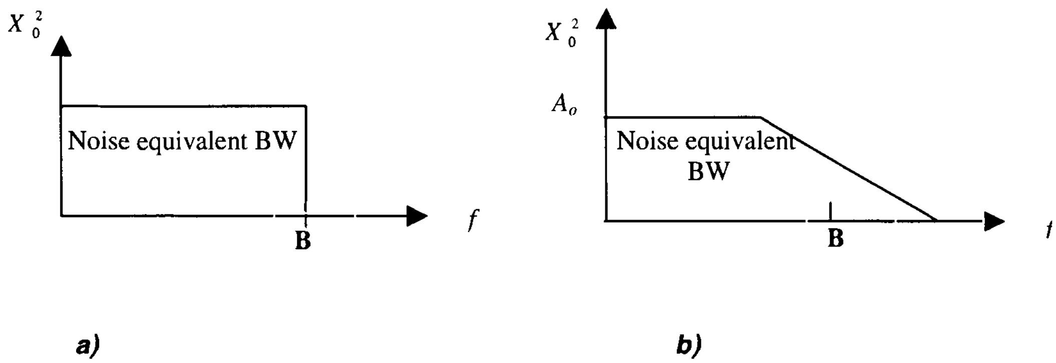

Figure 3- 1: Spectral bandwidth a) ideal circuit b) ieal circuit

correlated even if their amplitudes differ. An example of correlated signals would be two sine waves of the same frequency and phase. Another important factor is the noise equivalent bandwidth as shown in Figure 3-1. This is defined as the voltage gain-squared bandwidth of the circuit. The ideal case (Figure 3-1-a) is that the gain is constant A_0 up to the bandwidth of *B*, and after *B* is zero. But, the behavior of a real circuit is not abrupt. *B* is chosen to estimate the whole area of under the curve.

3-4- 1 Thermal Noise

Thermal Noise is due to random thermal motion of the electrons and is independent of the DC current flowing in the component. i_n is the mean square value of the Thermal Noise current as in formula (2-7) [6]:

$$i_n^2 = \frac{4KTB}{R} \qquad (3\text{-}3)$$

Where:

K is Boltzmann's constant, $1.38\text{x}10^{-23}$ *Joules/K*;

T is absolute temperature *Kelvin*;

and R is the resistor or equivalent resistor in which the thermal noise is occurring.

3-4- 2 Flicker Noise

Flicker or 1/f Noise is an important source of noise for a CMOS transistor. This noise is associated with carrier traps in semiconductors, which capture and release carriers in a random manner [6].

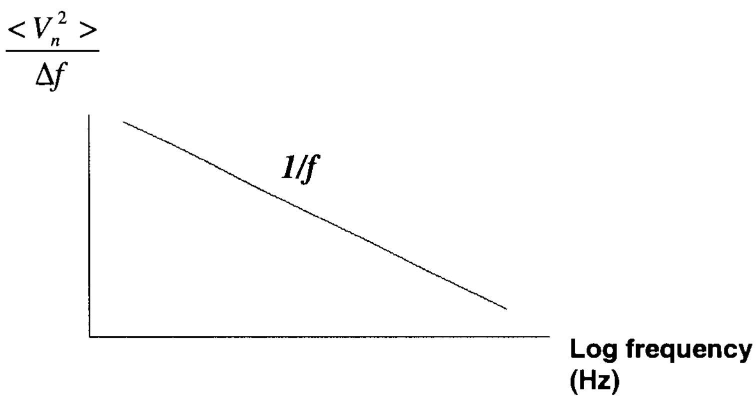

Figure 3- 2: Flicker Noise

$$i_n^2 = K_F \frac{I_D}{fC_{ox}L^2} B \tag{3-4}$$

Where K_F =Flicker noise coefficient is 10^{-28} for $0.8\mu m$ technology and 10^{-23} for 0.6 μm technology, f is frequency in *Hertz*, C_{ox} is Silicon Oxide capacitance per unit area, B is the band width, L is the oxide thickness and I_D is the drain current. The noise_ current spectral density for typical *1/f* is shown in Figure 3-2.

3-4- 3 Shot Noise

Another source of white noise is Shot Noise, which is associated with DC current flow across a p-n junction. This is the result of random generation of carriers within a depletion region either by thermal generation, i.e. shot noise or random generation of electrons causes by incident photons. i_n is the mean square value of the shot noise current with the form :

$$i_n^2 = 2qIB \qquad (3\text{-}5)$$

Where $q=1.6x10^{-19}C$ is the charge of electron;
I is the average DC current of the p.n. junction;
and (B)Δf is the bandwidth in *Hertz.*

The noise current spectral density can be found by dividing i_n by Δf and is denoted as [4]:

$$S_i = \frac{i_n^2}{\Delta f}$$

3-4- 4 Reset Noise

The circuit in Figure 3-3 resents a transistor acting as a switch in series with a capacitor C. The switch transistor is represented by a resistor R in series with an ideal switch, where R is the ON resistor of the transistor.

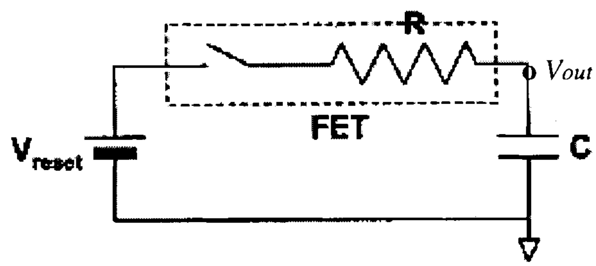

Figure 3- 3: RC equivalent circuit of CMOS transistor

The capacitor C can be charged and discharged through the switch resistor R with a time constant of *RC.* The switching generates a noise called Reset Noise (KTC Noise) that is given by [9]:

$$< i_{out} = \sqrt{KTC} > \qquad (3\text{-}6)$$

3- 5 MOSFET Noise

Noise can be modeled by a current source connected in parallel with the drain source current as shown in Figure 3-4. The noise current source represents two noises, Thermal Noise and Flicker Noise. The mean square current noise source is defined as [6]:

$$i_n^2 = i_{thermal}^2 + i_{1/f}^2 = [\frac{8KTg_m}{3} + \frac{(KF)I}{fCL^2}]B \quad (3\text{-}7)$$

Where K is Boltzmann's constant, C is Dioxide capacitance, T is Kelvin degree, I is drain current, g_m is transconductance, f is operating frequency, $\Delta f(B)$ is the noise bandwidth and KF is flicker coefficient with typical value of 10^{-28}F-A [6].

The mean square voltage noise is:

$$S_{eN} = \frac{i_n^2}{g_m^2} \quad (3\text{-}8)$$

And the Power Spectral Density is:

$$S_e^2 = \frac{e_{eq}^2}{\Delta f} \quad (3\text{-}9)$$

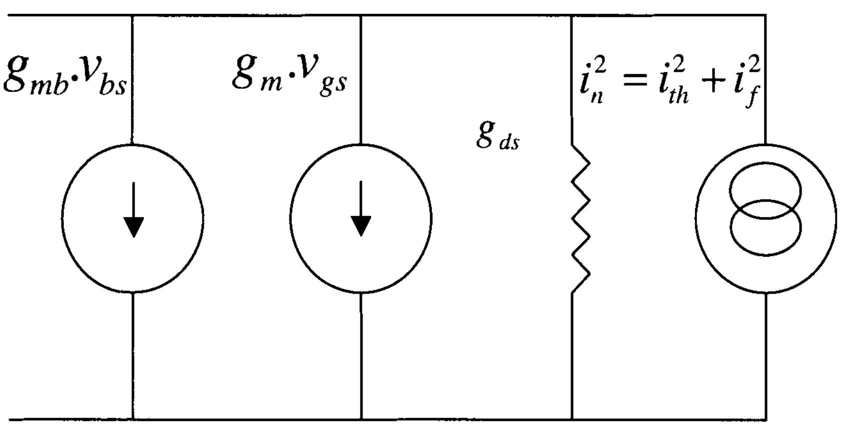

Figure 3- 4: CMOS Small Signal circuit

Where:

$$g_m = \frac{\delta i_d}{\delta V_{gs}}$$

$$g_{mb} = \frac{\delta i_d}{\delta V_{bs}}$$

$$g_{ds} = \frac{\delta i_d}{\delta V_{ds}}$$

3- 6 Noise in C.M. APS

Each component of the APS is responsible for different noise sources and affects the performance of the system. The noise generated in each component is the input noise for the next stage and may be even amplified [5].

$$< i_n >= \sqrt{i_1^2 + i_2^2 + i_3^2 + \ldots + i_n^2} \tag{3-10}$$

The components' noise source is displayed in Table 3-1.

Component	Noise added
T_1	Reset, FPN
Photodiode	PRNU,FPN, (dark and photon) Shot
T_2	FPN, Thermal, *1/f*
T_3	Thermal and *1/f* (T_3 noise <<T_2 noise)

Table 3- 1: Noise contribution of pixel in C.M. APS

Where i_{N1}, i_{N2}, i_{N3} and i_{Nn} are the uncorrelated random inputs of a linear system having a $H(\omega)$ system transfer function. The total output PSD is given by:

$$S_{Vn} = \left|H_1(\omega)^2\right|.S_{iN1} + \left|H_2(\omega)^2\right|.S_{iN2} + \ldots + \left|H_n(\omega)^2\right|.S_{iNn} \tag{3-11}$$

S_{iN1}, S_{iN2}, S_{iN3}, and S_{iNn} denote the PSD noise of each corresponding input current.

3- 7 Noise simulation of C.M. APS

To simulate the circuit shown in Figure 2-8, a photo sensor was replaced with a capacitor, where the voltage on the capacitor was varied. Photo current Shot Noise and dark current Shot Noise were obtained from the following equation:

$$I_D = I_{SAT}(e^{\frac{qv}{KT}} - 1) \quad (3\text{-}12)$$

$$I_{sn} = \sqrt{2q(I_p + I_D)\Delta f} \quad (3\text{-}13)$$

Where:

I_D =Photo sensor dark current,

$q = 1.6 \times 10^{-19}$

$I_{P=}$ Photo generated current,

and T is Kelvin temperature.

The photo current and dark current cause a change in the charge on capacitor $\Delta Q = C\Delta V$ or $\Delta Q = nq = i.\Delta t$. (3-14)

$$I_{sn} \times \Delta t = nq$$

$$I_{sn} = \frac{nq}{\Delta t} = \frac{C.\Delta V}{t} = \frac{26\times10^{-15}\times0.6}{10^{-6}} = 15.6\times10^{-9}$$

$$\frac{i_{sn}^2}{\Delta f} = 2qI_{sn} = 0.5\times10^{-27}$$

Where C= $26\text{x}10^{-15}$ [8] and t is the period of readout mode (assuming read out frequency is 1MHz).

Flicker Noise can be calculated by equation (3-15) [17], which W, L, g_m and g_{mbs} may be extracted from the electrical parameters [10].

$$(i_N)^2 / \Delta f = \frac{1}{f}\frac{KF}{2CoxWLK'} = \frac{1}{f}\frac{KF}{2C_{ox}WL\mu C_{ox}} = \frac{1}{f}\frac{KF}{2C_{ox}WL\frac{g_m}{g_{mbs}}C_{ox}} \quad (3\text{-}15)$$

Parameters K for P channel and N channel transistors are different in the technology used; for example K_P=0.5x10^{-23} and K_N=10^{-23} in 0.6 μm CMOS technology, also C_{ox} is capacitance per unit area of the gate oxide *(Farad/cm²)*. All noises were calculated at a frequency of 10 *MHz.*

3- 8 Small Signal Model for C.M. APS in Direct Mode

APS circuit was run in Cadence and set the desirable DC operating points for each components, electrical parameters (such as transconductances, capacitances, voltages, currents, etc) corresponding to different bias condition and device geometric can be obtained. These values can be used to calculate the power spectral density noise for each transistor. The DC operating points for C.M. APS in Direct Mode are displayed in Table 3-2. For a complete list of DC operating points, see Appendix D.

	V_{gs} (V)	V_{ds} (V)	W (μm)	L (μm)	I_d (μA)	V_T (V)
Reset	-1.4	0.56	0.8	0.35	0	0.50
Amp	1.4	1.963	0.8	0.35	2.1	0.42
Read	1.18	0.11	0.8	3.6	2.1	0.65
T_4	-1.22	-1.22	0.8	0.35	-2.13	-0.59
T_5	-1.22	-3.23	10	0.35	-70.42	-0.47

Table 3- 2: DC operation points for C.M. APS in Direct Mode

An AC equivalent circuit and Small Signal model of C.M. APS is shown in Figure 3-5 and Figure 3-6. The Small Signal equivalent circuit of the circuit is shown in the read out mode, i.e. gate of transistor T_1 is grounded, gate of transistor T_3 is connected to V_{cc}, which in AC equivalent circuit is grounded. The analytical expression for the total noise of the read out mode obtained from the small signal equivalent circuit of the CMOS transistor was developed. The various parameters of the small signal model are all related to the large signal

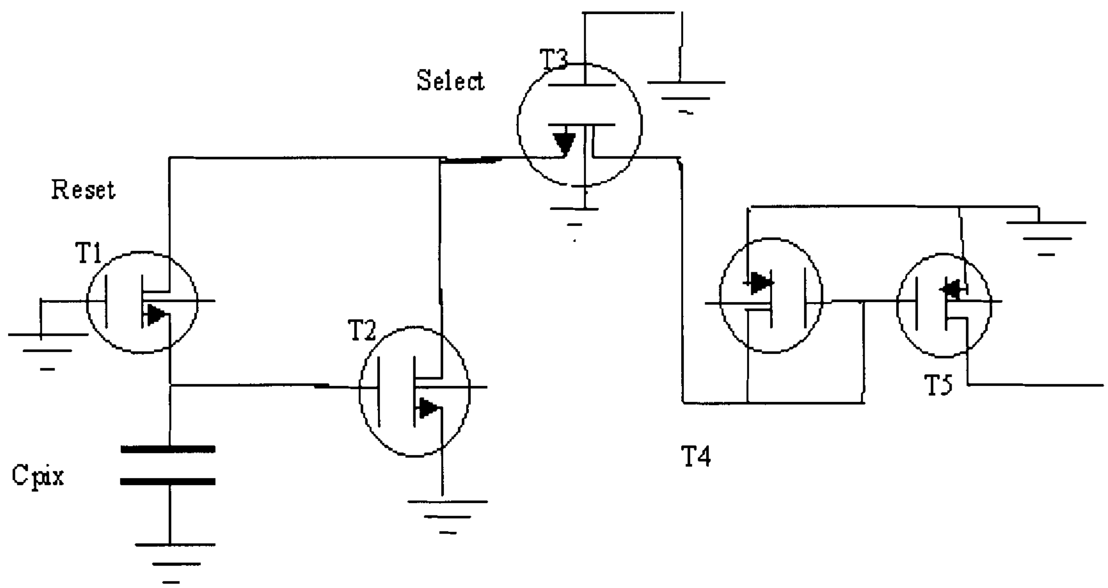

Figure 3- 5: AC equivalent circuit of Figure 2-7 – C.M. APS in Direct Mode series with current mirror

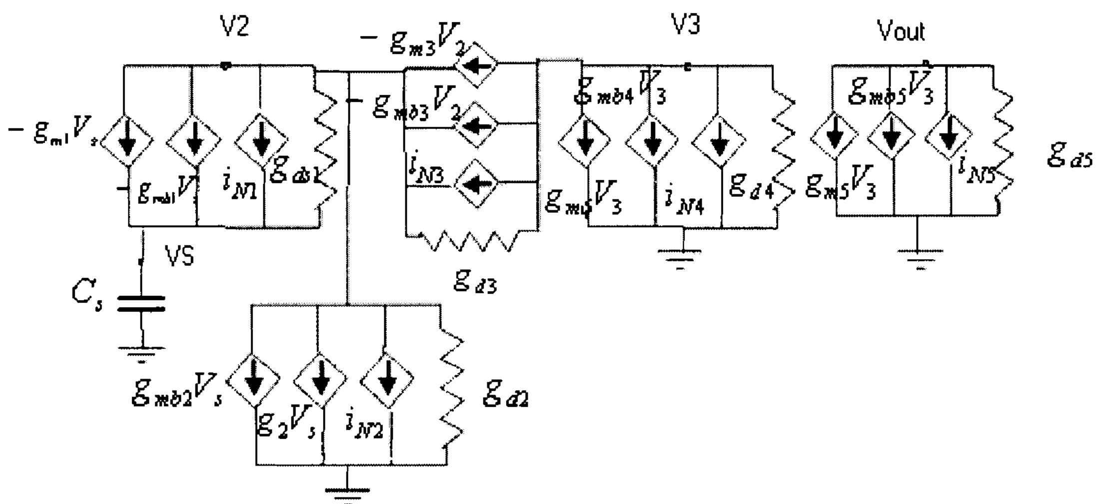

Figure 3- 6: Small Signal Circuit of Figure 3-5 - C.M. APS in Direct Mode series with current mirror

model parameters and DC variables, e.g. g_{bd} and g_{bs} are conductance for the bulk to drain and bulk to source junctions. Since these junctions are normally reverse biased, the conductance is very small. For simplification, the small parameters are deemed negligible to the larger parameters; for instance g_{mbs}, transconductance of bulk source, is much smaller than transconductance of the CMOS, g_m.

It should be noted that noise was determined in the steady state condition only. During normal CMOS active pixel sensor operating the signal and the noise levels reach their stationary or equilibrium level at the sampling instant. In other words, the signal and noise transients no longer vary.

A nodal analysis in the frequency domain $\omega=2\pi f$ leads us to find the relation for the output noise level. By using nodal analyses, the following small signal equivalent circuit was obtained.

$$i_{N1} - g_{m1}V_s + (V_2 - V_s)g_{d1} - SCV_s = 0 \tag{3-16}$$

$$V_2 \cdot g_{d2} + i_{n2} + g_{m2}.V_s + V_s.Sc + g_{m3}V_2 + g_{mb3}V2 + i_{n3} + (V_2 - V_3)g_{d3} = 0 \tag{3-17}$$

$$g_{m4}V_3 + i_{n4} + V_3 g_{d4} = -g_{m3}V_2 - i_{n3} + (V_3 - V_2)g_{d3} = 0 \tag{3-18}$$

$$g_{m5}V_3 + g_{mb5}V_3 + i_{n5} + V_{out}(g_{d5} + g_L) = 0 \tag{3-19}$$

$$V_{out} = X_1.i_{N1} + X_2.i_{N2} + X_3.i_{N3} + X_4.i_{N4} + X_5.i_{N5} \tag{3-20}$$

Where i_{N1} i_{N2}, i_{N3}, i_{N4} and i_{N5} are the un-correlated random inputs of a linear system having V_N as output the total Power Spectral Density of the circuit is given by:

$$S_N = \left|X_i(\omega)\right|^2.S_{iN} = \left|X_1(\omega)\right|^2.S_{iN1} + \left|X_2(\omega)\right|^2.S_{iN2} + \left|X_3(\omega)\right|^2.S_{iN3} + \left|X_4(\omega)\right|^2.S_{iN4} + \left|X_5(\omega)\right|^2.S_{iN5} \tag{3-21}$$

Where:

$$X_1 = \frac{g_{m5}+g_{mb5}}{g_{d5}} f_1; X_2 = \frac{g_{m5}+g_{mb5}}{g_{d5}} f_2; X_3 = \frac{g_{m5}+g_{mb5}}{g_{d5}} f_3;$$
$$X_4 = \frac{g_{m5}+g_{mb5}}{g_{d5}} f_4; X_5 = \frac{1}{g_{d5}+g_L}$$

For a detailed derivation see Appendix A.

Since we have obtained the total spectral density of the APS circuit, we need the electrical parameters of each component to calculate the output voltage noise. This information was obtained from the SpectreS models. In order to obtain the output noise, the circuit was simulated with SpectreS models in Cadence. After reset noise the major noise concern for an APS circuit is when it is in read out mode, since the propagation of the signal from input to output is crucial. To observe this operation, transistor T_1 was off, transistor T_3 was in linear region (active mode), and transistors T_2, T_4 and T_5 were in saturation region. The circuit was simulated in $0.35\mu m$ CMOS (CMOSP35) technology. V_{cc} was 1.65 and V_{ss} was -1.65 to ground. Since transistor T_1 was off, it did not affect the readout circuit noise. The photo sensor was replaced with a capacitor which its voltage was increasing toward the forward diode voltage responding photon interaction.

As mentioned previously, the sense node voltage (voltage gate of T_2) depends on the DC operation of circuit during reset. The voltage at the gate of T_2 adjusts itself to the current that flows to T_2 via T_3 and T_4.

The sense node voltage was varied from reverse to forward depending on the number of photon interacting with the photo sensor and depletion layer capacitance. The photo sensor is simulated by a capacitor in parallel with a voltage source, where the voltage on the capacitor was varied over time. This specified time was a read out period, $1\mu s$. The output load was $1k\Omega$ to obtain the lowest possible noise, and so that the output current can be driven off chip by the resistor. The resistor noise was calculated separately.

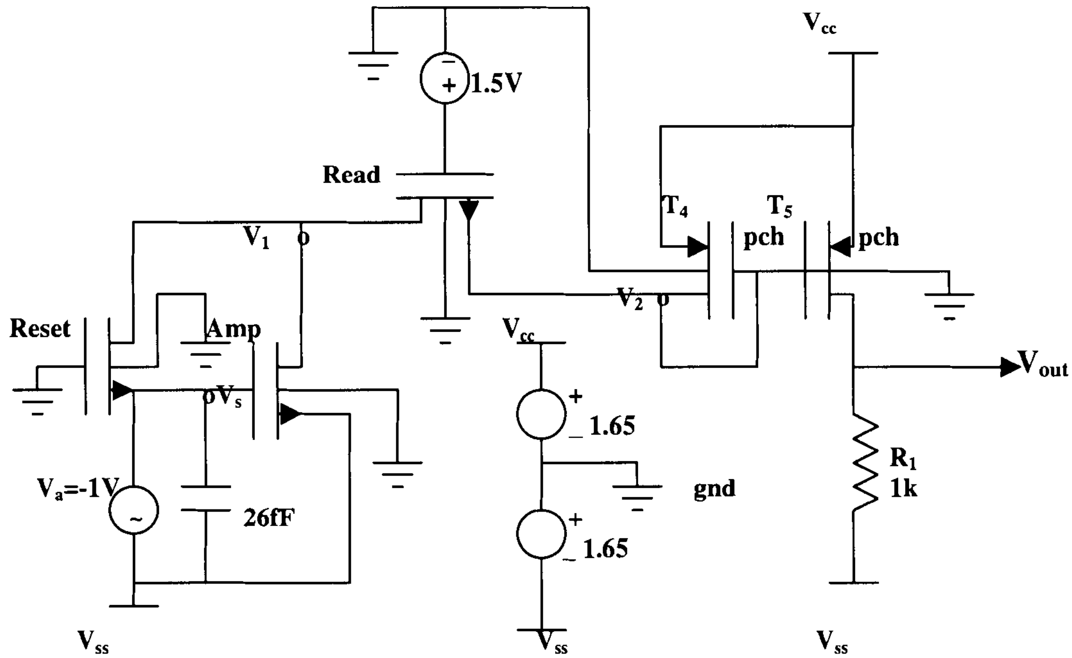

Figure 3- 7: C.M. APS in Direct Mode simulated in Cadence

To minimize the charging time on the drive side, the current mirror transistors were given a large *W* and a small *L* to provide a high transconductance at the output. The aspect ratio and DC bias voltages were chosen to obtain the desired operating points. C.M. APS in Direct Mode is simulated in Cadence as shown in Figure 3-7.

Since every $1\mu s$ the photo sensor is read, the period of signal is $1\mu s$. The noise bandwidth of the circuit measured in Cadence was 87*MHz* (Δf=87*MHz*).

3- 9 Noise Transfer Function of APS

The output PSD of the circuit was obtained by extracting the electrical parameters for the circuit after simulation. The electrical parameters for the above APS circuit were printed out in Cadence and are presented in Appendix D.

The operating frequency was f<100 *MHz,* neglecting the parasitic capacitors the transconductance of photo sensor obtained:

$$Y_c = \frac{1}{X_c} = 2\pi fC = 2\pi \times 85 \times 10^6 \times 26 \times 10^{-15} = 13.8\mu \tag{3-22}$$

The transfer functions were calculated from the electrical parameters. These transfer functions are difficult to handle analytically, unless simplifying them by doing some very reasonably assumption and calculations. Using the multiplication factors of the transfer function in Appendix A and B, we obtain:

$$S_{V_{out}} = (\tfrac{1}{364\mu})^2 S_{iN1} + (\tfrac{1}{40.63\mu})^2 S_{iN2} + (\tfrac{1}{2694.8\mu})^2 S_{iN3} + (\tfrac{1}{43.61\mu})^2 S_{iN4} + (\tfrac{1}{1015\mu})^2 S_{iN5} \quad (3\text{-}23)$$

3- 10 Output Current Noise of C.M CMOS APS in Direct Mode

In order to calculate output PSD noise, S_{VN}, the PSD of each corresponding input component (S_{iN1}, S_{iN2}, S_{iN3}, S_{iN4}, S_{iN5} and $S_{iNRload}$), are constant for white noise and inversely proportional to the frequency for the Flicker Noise, are calculated.

Transistor T_2 operates in saturation region, transistor T_3 operates in linear region, transistor T_4 operates in saturation region and transistor T_5 operates in saturation region and also bring the current noise of the load resistor into account, the output PSD of each component is demonstrated in Table 3-3 (for details, see appendix B).

If we exclude the noise of load resistor, the total active components noise becomes:

$$S_{V_{Total}} = S_{V1} + S_{V2} + S_{V3} + S_{V4} + S_{V5} = (0 + 218 + 0.04 + 101 + 4.53) \times 10^{-18} = 324 \times 10^{-18} V^2 / Hz$$

The contribution of each signal noise to form the total PSD noise is calculated in Table 3-4.

If we add the load resistance noise ($16a\,V^2/Hz$) to active component noise ($324a\,V^2/Hz$) the total output PSD noise becomes $340a\,V^2/Hz$.

Source	PSD (A^2/Hz)
S_{iN1}	$3.07x10^{-36}$
S_{iN2}	$3.6x10^{-25}$
S_{iN3}	$3.05x10^{-25}$
S_{iN4}	$1.92x10^{-25}$
S_{iN5}	$4.67x10^{-24}$
$S_{iNRload}$	$1.65x10^{-23}$

a)

Source	PSD (V^2/Hz)
S_{v1}	0
S_{v2}	218.12×10^{-18}
S_{v3}	0.04×10^{-18}
S_{v4}	101×10^{-18}
S_{v5}	4.53×10^{-18}
S_{vRload}	1.60×10^{-17}

b)

Table 3- 3: a) input b) output - PSD noise of C.M. APS in Direct Mode

Source	S_{V1}	S_{V2}	S_{V3}	S_{V4}	S_{V5}
Contribution %	0	67.35	0.01	31.24	1.4

Table 3- 4: Contribution of each component in total PSD noise in Direct Mode

The output noise waveform plotted by Cadence in Figure 3-8 shows that the total out put PSD noise of APS circuit in Direct Mode is $327aV^2/Hz$.

Signal waveforms, frequency response, transient response and noise response of APS in Direct Mode plotted by Cadence in Appendix C. The noise bandwidth was *87MHz*, total output noise at V_2 was $1.75fV^2/Hz$, and output spectral noise density at V_1 was $4.07fV^2/Hz$. Gain of the circuit at sense node was 1, and at V_1 was 2.85.

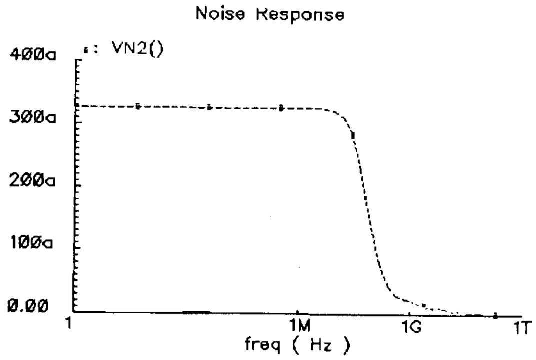

Figure 3- 8: Total output PSD noise of C.M. APS in Direct Mode

3- 11 Small Signal Model for C.M. APS in Difference Mode

Another approach to read out of the output pixel current is to use a current source to inject current to drain of select transistor, T_3. Then the difference of I_{ref}-I_{pix}, is steered to NMOS current mirror. An AC equivalent circuit of the C.M. APS and its small signal circuits in Difference Mode are shown in Figure 3-9 and Figure 3-10. This Small Signal equivalent circuit of the circuit is shown in the read out mode, i.e. gate of transistor T_1 and T_4 is grounded, gate of transistor T_3 is connected to V_{cc}, which in AC equivalent circuit is grounded. The analytical expression for the total noise of the read out mode obtained from the small signal equivalent circuit of the CMOS transistor was developed. The various parameters of the small signal model are all related to the large signal model parameters and DC variables, e.g. g_{bd} and g_{bs} are conductance for the bulk to drain and bulk to source junctions. Since these junctions are normally reverse biased, the conductance is very small. For simplification, the small parameters are deemed negligible to the larger parameters; for instance g_{mbs}, transconductance of bulk source, is much smaller than transconductance of the CMOS, g_m.

A nodal analysis in the frequency domain $\omega=2\pi f$ leads us to find the relation for the output noise level.

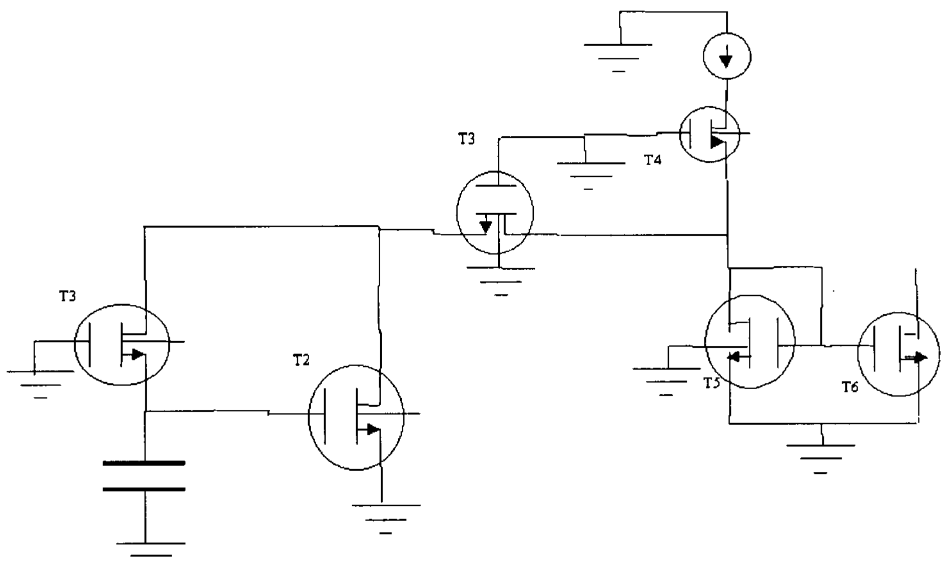

Figure 3- 9: AC equivalent circuit of Figure 2-8 - C.M. APS in Difference Mode series with a current mirror.

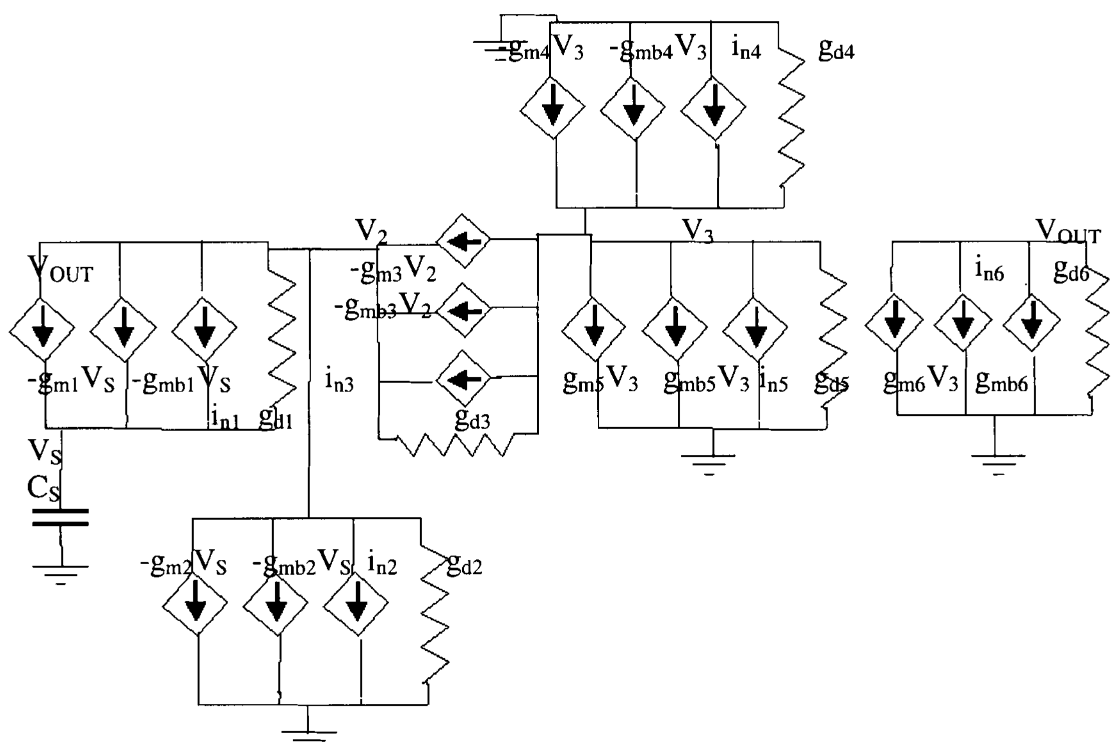

Figure 3- 10: Small Signal circuit of Figure 3-9 - C.M. APS in Difference Mode series with a current mirror.

Using nodal analyses, following small signal equivalent circuit for noise was obtained:

$$i_{N1} - g_{m1}V_s + (V_2 - V_s)g_{d1} - SCV_s = 0 \tag{3-24}$$

$$V_2.g_{d2} + i_{N2} + g_{m2}.V_s + V_s.Sc + g_{m3}V_2 + g_{mb3}V_2 + i_{N3} + (V_2 - V_3)g_{d3} = 0 \tag{3-25}$$

$$g_{m6}V_3 + g_{mb6}V_3 + V_{out}(g_{d5} + g_L) + i_{n6} = 0 \tag{3-26}$$

$$g_{m6}V_3 + g_{mb6}V_3 + V_{out}(g_{d5} + g_L) + i_{n6} = 0 \tag{3-27}$$

$$V_{out} = X_1.i_{N1} + X_2.i_{N2} + X_3.i_{N3} + X_4.i_{N4} + X_5.i_{N5} + X_6.i_{N6} \tag{3-28}$$

For a detailed derivation see Appendix A.

As i_{N1}, i_{N2}, i_{N3}, i_{N4}, i_{N5} and i_{N6} are the un-correlated random inputs of a linear system having V_N as output voltage noise the total output APS noise in Difference Mode circuit is given by:

$$S_{VN} = \left|X\ (\omega)\right|^2.S_{i\,N1} = \left|X_1(\omega)\right|^2.S_{iN1} + \left|X_2(\omega)\right|^2.S_{iN2} + \left|X_3(\omega)\right|^2.S_{i\,N3} + \left|X_4(\omega)\right|^2.S_{i\,N4} + \left|X_5(\omega)\right|^2.S_{iN5} + \left|X_6(\omega)\right|^2.S_{iN6} \tag{3-29}$$

The total spectral density of the circuit was simulated to determine the electrical parameters. C.M. APS in Difference Mode is simulated in Cadence and displayed in Figure 3-11.

The electrical parameters determined during simulation as shwon in Table 3-5. The DC operating points are displayed in Table 3-5. For a complete list of DC operating points, see Appendix D.

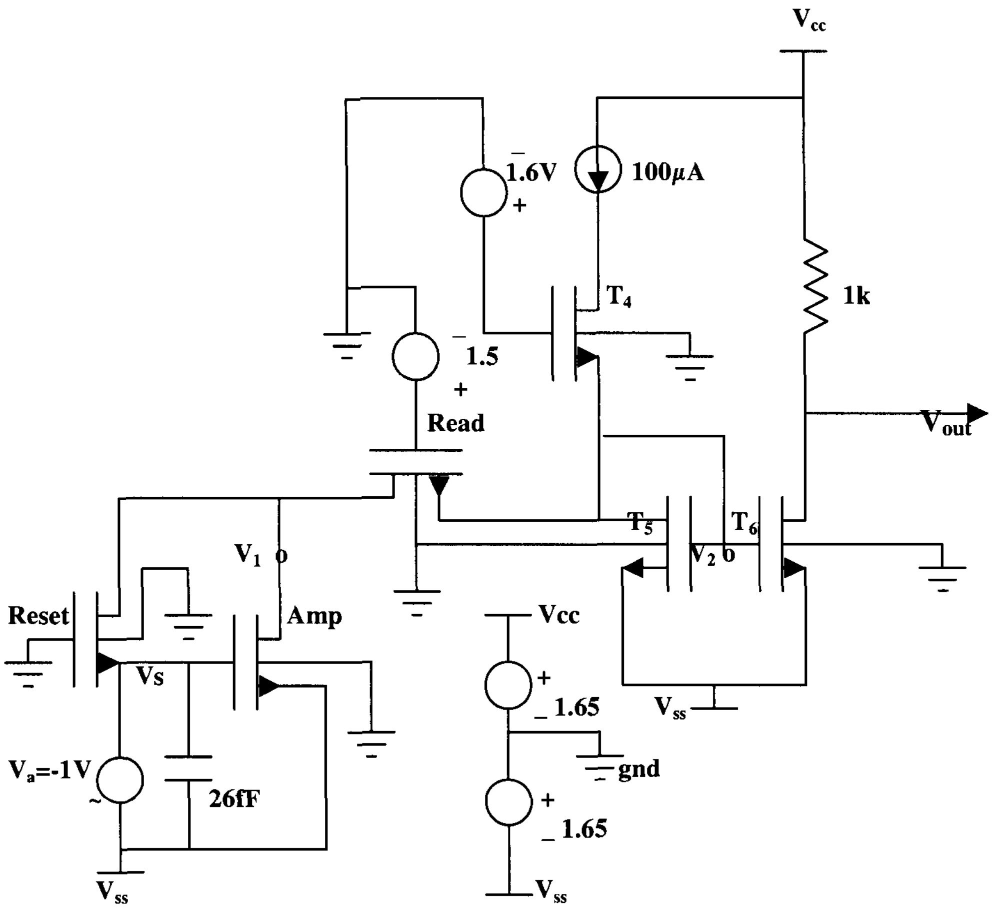

Figure 3- 11: C.M. APS simulated in Cadence in Difference Mode

	V_{gs} (V)	V_{ds} (V)	W (μm)	L (μm)	I_d (μ A)	V_T (V)
Reset	-1.4	0.64	0.80	0.35	0	0.54
Amp	1.4	2.04	0.80	0.35	2.15	0.42
Read	1.10	0.15	0.80	3.50	2.15	0.62
T_4	1.10	0.18	0.8	3.5	100	0.70
T_5	2.19	2.19	0.80	0.35	97.84	0.42
T_6	2.19	1.96	10.00	0.35	0.41	0.41

Table 3- 5: A typical DC operation points for C.M. APS in Difference Mode

Using these electrical parameters and using the same methods to calculate the transfer function of the system, we obtain the folowing equation:

$$S_{V_{out}} = (\tfrac{1}{361\mu})^2 S_{iN1} + (\tfrac{1}{77.12\mu})^2 S_{iN2} + (\tfrac{1}{4.73m})^2 S_{iN3} + (\tfrac{1}{445m})^2 S_{iN4} +$$
$$+ (\tfrac{1}{961\mu})^2 S_{iN5} + (\tfrac{1}{1073\mu})^2 S_{iN6}$$

In order to calculate the output PSD noise, S_{VN}, the PSD of each corresponding input component (S_{iN1}, S_{iN2}, S_{iN3}, S_{iN4}, S_{iN5}, S_{iN6} and $S_{iNRload}$, which are constant for white noise and inversely proportional to the frequency for the Flicker Noise, was calculated.

Transistor T_2 operates in saturation region, transistor T_3 and T_4 operate in linear region, transistor T_5 and transistor T_6 operate in saturation region and also bring the current noise of the load resistor into account, the output PSD noise of each component is demonstrated in Table 3-6 (for more details see appendix B). Total output PSD noise of the circuit excluding load resistance noise is:

$$S_{V_{Total}} = S_{V1} + S_{V2} + S_{V3} + S_{V4} + S_{V5} + S_{V6} = (0 + 61.2 + 0.01 + 0.00021$$
$$+ 225 + 21.8) \times 10^{-18} = 307 \times 10^{-18} V^2 / Hz$$

The contribution of each signal noise to form the total PSD noise is calculated in Table 3-7.

If we add the load resistance noise ($14.3aV^2/Hz$) to active components' noise ($307aV^2/Hz$) the total output PSD noise becomes $321.3aV^2/Hz$

$$S_{V_{Total}} = S_{V1} + S_{V2} + S_{V3} + S_{V4} + S_{V5} + S_{V6} + S_{VRLoad} =$$
$$= 307 \times 10^{-18} + 14.3 \times 10^{-18} = 321 \times 10^{-18} V^2 / Hz$$

The output noise waveform plotted by Cadence shows that the total output PSD noise of APS in Difference Mode is $301.3aV^2/Hz$ (as shown in Figure 3-12). Signal waveforms, frequency response, transient response and noise response, of APS in Difference Mode plotted by Cadence are shown in Appendix C. The noise bandwidth was $98MHz$, total out put noise at V_2 was $71aV^2/Hz$ and output spectral noise density at V_1 was $2.2fV^2/H_z$. The voltage gain of circuit at the sense node was 1, at V_1 was 2, and at $V_{difference}$ was 0.4.

a)

Source	PSD (A^2/Hz)
S_{iN1}	3.07×10^{-36}
S_{iN2}	3.64×10^{-25}
S_{iN3}	2.35×10^{-25}
S_{iN4}	4.25×10^{-24}
S_{iN5}	1.87×10^{-24}
S_{iN6}	2.15×10^{-23}
$S_{iNRload}$	1.65×10^{-23}

b)

Source	PSD (V^2/Hz)
S_{v1}	0
S_{v2}	61.2×10^{-18}
S_{v3}	1.05×10^{-20}
S_{v4}	2.1×10^{-23}
S_{v5}	2.25×10^{-16}
S_{v6}	1.87×10^{-17}
S_{vRload}	1.43×10^{-17}

Table 3- 6: a) input b) output- PSD noise of C.M. APS in Difference Mode

Source	S_{V1}	S_{V2}	S_{V3}	S_{V4}	S_{V5}	S_{V6}
Contribution %	0	20.17	0	0	73.7	6.1

Table 3- 7 Contribution of each component in total PSD noise in Difference Mode

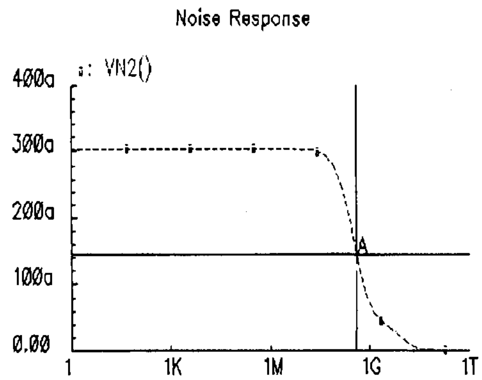

Figure 3- 12: Total output PSD noise of C.M. APS in Difference Mode

3- 12 Noise Results Summary

The total noise for the circuit obtained from Cadence in Direct Mode was $327aV^2/Hz$. The noise measure includes resistor noise. The resistor noise was determined through calculation, $16aV^2/Hz$, and added to the other APS noise sources, $324aV^2/Hz$, and obtained a value of $340aV^2/Hz$. This result is close to the simulated waveform obtained in Cadence. There is a less than a 4% difference between the calculation and Cadence results. Note that the formula considered the small signal parameters as negligible as compared to large signal values. These discrepancies accounted for the variation.

As we expected, transistor T_2 is the major generator of noise (67.3% of the total noises) followed by T_4 and T_5, because these devices all operated in the saturation region. The second largest noise source is T_5, which was the first transistor of the current mirror. Transistor T_1 (which operates in the cut off region) and T_3 (which operates in the linear region) do not contribute significant noise to the system, and their cumulative contribution can be approximated to be zero.

Revisiting the AC response of the system and moving backward from V_{direct} to V_1, we see the de-amplification of signal to 25% of its original value- from 2.82 to 0.72. This means the noise created by T_2 also degraded while crossing other active components. Also output noise plotted at V_1, V_2 and V_{direct}, noise changes from 4 to 2 and to 0.7 respectively. This confirms by itself that transistor T_2 has the largest noise contribution. The bandwidth of the circuit is 87*MHz*.

Assuming the signal level at V_{sense} is 1; the signal level was amplified by a factor of 2.8 by transistor T_2, and de-amplified to 1.75 at V_2. It is then again de-amplified to 0.72 at output, V_{direct}. These signals are plotted in Appendix C. V_{sense} drops from –250*mV* to -320*mV* (towards forward bias) within the *1 μs* period of time. The signal at V_1 starts to increase from *310mV* to 470*mV*. It decreases from 410*mV* to 530*mV* at V_2, and at V_{direct} it drops from –1.5*mV* to –1.62*mV*.

Voltage signal, voltage noise, voltage signal gain and voltage noise gain of CM CMOS APS is brought in table 3-8.

		V_s	V_1	V_2	V_{out}	V_{out}/V_S Gain	V_{out}/V_1 Gain	V_{out}/V_2 Gain	V_2/V_s Gain	Noise BW MHz
Direct Mode	**Signal**	**1 V**	**2.8 V**	**1.75 V**	**0.7 V**	**0.7**	**0.25**	**0.4**	**1.75**	**87**
	Noise	**X=2.18 *f* V²/Hz**	**4.05*f* V²/Hz**	**1.750*f* V²/Hz**	**327*a* V²/Hz**	**0.15**	**0.08**	**0.19**	**0.80**	
Difference mode	**Signal**	**1 V**	**1.92 V**	**0.182 V**	**0.34 V**	**0.34**	**0.18**	**1.87**	**0.18**	**97**
	Noise	**X=1.21 *f* V²/Hz**	**2.22*f* V²/Hz**	**71*a* V²/Hz**	**301*a* V²/Hz**	**0.24**	**0.13**	**4.23**	**0.03**	

Table 3- 8: Signal and noise performance for C.M. APS

The width and length for the transistors in Direct Mode and Difference Mode were chosen to be the same value in order to have a better compare of their overall circuit performance. The goal was not to optimize the noise performance of the circuit or to amplify the signal level, but to analyze and calculate both modes of the circuit.

In Difference Mode we have an extra component that works in the linear region, and does not add a significant noise to the system. Consequently, it is not expected to have too much of a difference in total output noise. Also transistor T_4 and T_5 were changed from P-channel to N-channel which inherently creates more noise due to the fabrication process [4].

In Difference Mode, transistors T_1, (which works in the cut off region) T_3 and T_4, (which work in the linear region), do not generate significant noise to the system, and their contribution is approximately zero. Transistors T_2, T_5 and T_6 are the major noise sources, as they operate in the saturation region.

The total noise is calculated to be $321aV^2/Hz$, and it is 2.3% less than what we calculated in Direct Mode, $327aV^2/Hz$. Total noise obtained in Cadence was $301aV^2/Hz$, which is 6.5% less than the noise obtained from Cadence in Direct Mode, 321 aV^2/Hz. Signal level and AC response of the circuits were plotted by Cadence and displayed in Appendix C. In Difference Mode, the bandwidth of the system is a bit more than direct mode and changed form $87MHz$ to $97MHz$.

In Difference Mode, the noise generated at V_1 is almost half that of the noise in Direct Mode, as it changes from $4fV^2/Hz$ to $2.2fV^2/Hz$. This is because T_3 is parallel to transconductance of the new transistor T_4, and the $H_2(\omega)$ drops from $1/40\mu$ (in Direct Mode) to $1/77\mu$ (in Difference Mode) and noise voltage gain was decreased.

In Direct Mode total output noise obtained in Cadence is $321aV^2/Hz$ and with signal noise gain 0.15, input noise becomes $2.18fV^2/Hz$. It is sensitivity of this APS. Other words the minimum signal level that APS can detect at sense node is $2.18f$ and the input signal should be more than that. In Difference Mode the total output noise obtained in Cadence was $311aV^2/Hz$ and with signal noise gain 0.13, input noise became $2.31fV^2/Hz$. Other words the minimum signal level that APS can be detected at sense node was $2.31fV^2/Hz$, and the input signal should be more than that. It means the total output noise of Difference Mode was less than Direct Mode, and the sensitivity of Difference Mode was more than Direct Mode.

3- 13 Power Consumption

Power consumption of the circuit in Direct Mode measured by Cadence was 245.9mW, and in Difference Mode was 245.8mW.

CHAPTER FOUR
CONCLUSION AND SUMMARY

Current Mediated APS offers the advantages of compact size, simple operation, and low power supply and threshold voltage, but their performance is limited by noise due to their sensitivity to mismatches in device threshold voltage. These features encourage designers to find a solution with these components, while seeking ways to overcome their disadvantages.

A C.M. APS can operate in two modes. These modes have been characterized and their performances were analyzed. Small signal analysis was used to calculate the total output noise C.M. APS and Contribution of each component in total output noise and sensitivity were calculated. Both circuit modes were simulated in Cadence and electrical parameters and signal waveforms were extracted. It was shown the largest noise source was transistor T_2. Bandwidth, signal gain and noise gain were also calculated.

The total output noise that was extracted from the theoretical analysis was not exactly identical to the Cadence simulation, because of the assumptions were made in the hand analysis. However, the figures for both were fairly close. One of the reasons for the discrepancy was the use of a fixed value of R_{ON} in Thermal Noise calculations $((i_N)^2 / \Delta f = 4KT / R_{ON})$. It should also note that some circuit parameters (ex. parasitic capacitance) were not included in the analysis, creating some variation between the calculated and measured quantities. Power consumption for both circuits was almost identical.

The objective of this project was to analyze, calculate and compare the noise performance of both C.M. APS in Difference Mode and Direct Mode. We showed that the FPN is reduced in Difference Mode. Also voltage noise in Difference Mode at V_1, V_2 and V_{out} is less than Direct Mode for identical components. Although the C.M. APS design was not optimized in this project, it is possible to improve the gain and noise performance of the C.M APS by detailed circuit and layout design.

APPENDICES

Appendix A - Transfer Function of APS

For a C.M. APS in Direct Mode the small signal input equations are as below:

$$i_{N1} - g_{m1}V_s + (V_2 - V_s)g_{d1} - SCV_s = 0$$

$$V_2 = \frac{g_{m1} + g_{d1} + SC}{g_{d1}}V_S + \frac{i_{N1}}{g_{d1}} \longrightarrow V_S = \frac{g_{d1}}{K_2}V_2 + \frac{i_{N1}}{K_2}(1) Where: K_2 = g_{m1} + g_{d1} + SC$$

$$V_3 = K_5V_2 + \frac{i_{N4}}{K_3} + \frac{i_{N3}}{K_3}$$

$$V_2 = \frac{g_{d3}}{K_1}.V_3 - \frac{g_{m2} + SC}{K_1}V_S + \frac{i_{n2}}{K_1} + \frac{i_{n3}}{K_1}(2) Where: K_1 = g_{d2} + g_{m3} - g_{d3}.$$

$$K_4 = 1 + \frac{g_{m2} + SC}{g_{m3}} \times \frac{g_{d1}}{k2}$$

$$V_2.g_{d2} + i_{n2} + g_{m2}.V_s + V_s.Sc + g_{m3}V_2 + g_{mb3}V2 + i_{n3} + (V_2 - V_3)g_{d3} = 0$$

$$2 \xrightarrow{1} V_2 = -\frac{g_{m2} + SC}{g_{m3}}\left(\frac{g_{d1}}{k_2}V_2 + \frac{i_{N1}}{k_2}\right) + \frac{i_{n2}}{k_1} + \frac{i_{n3}}{k_1} + \frac{g_{d3}}{k_1}$$

$$V_3 \longrightarrow V_2 = A.i_{N1} + B.i_{N2} + C.i_{N3} + DV_3(5)$$

Using (1) in (2), we obtain the relation between *V2* verses *V3*.

$$V_2(g_{d2} + g_{m3} + g_{mb3} - g_{d3}) + i_{n2} + i_{n3} - V_3g_{d3} + V_s(SC + g_{m2}) = 0$$

$$A = -\frac{g_{m2} + SC}{g_{m3}} \times \frac{1}{K_1K_4} B = \frac{1}{K_2K_4} +; C = \frac{1}{K_1K_4}; D = \frac{g_{d3}}{K_1K_4}$$

$$V_3(g_{m4} + g_{d4} + g_{d3}) + i_{N4} = V_2(-g_{m3} - g_{d3}) + i_{N3}$$

$$V_3 = -\frac{g_{m3}+g_{d3}}{g_{m4}+g_{d4}+g_{d3}}V_2 + \frac{i_{N4}+i_{N3}}{g_{m4}+g_{d4}+g_{d3}}$$

$$3 \xrightarrow{5} V_3 = K_5(Ai_{N1} + Bi_{N2} + Ci_{N3} + DV_3) + \frac{i_{N4}}{K_3} + \frac{i_{N3}}{K_3}(6)$$

$$Where.K_3 = g_{m4} + g_{d4} + g_{d3}$$

$$K_5 = -\frac{g_{m3}+g_{d3}}{g_{m4}+g_{d4}+g_{d3}}$$

$$V_3(1-K_5D) = K_5Ai_{N1} + K_5Bi_{N2} + K_5Ci_{N3} + \frac{i_{N4}}{K_3} + \frac{i_{N3}}{K_3}$$

$$f_1 = \frac{K_5A}{(1-K_5D)}; f_2 \frac{K_5B}{(1-K_5D)}; f_3 = \frac{K_5C-\frac{1}{K3}}{(1-K_5D)}; f_4 = \frac{1}{(1-K_5D)K_3}$$

$$V_3 = f_1i_{N1} + f_2i_{N2} + f_3i_{N3} + f_4i_{N4} \quad (7)$$

$$g_{m5}V_3 + g_{mb5}V_3 + g_{d5}V_{out} + i_{n5} = 0(8)$$

By placing (7) in (8), we get:

$$V_{out} = \frac{i_{n5}}{g_{d5}} + \frac{(g_{m5}+g_{mb5})}{g_{d5}}V_3 = \frac{i_{n5}}{g_{d5}} + \frac{(g_{m5}+g_{mb5})}{g_{d5}}(f_1i_{N1} + f_2i_{N2} + f_3i_{N3} + f_4i_{N4})$$

$$V_{out} = X_1.i_{N1} + X_2.i_{N2} + X_3.i_{N3} + X_4.i_{N4} + X_5.i_{N5}$$

Where:

$$X_1 = \frac{g_{m5}+g_{mb5}}{g_{d5}}f_1; X_2 = \frac{g_{m5}+g_{mb5}}{g_{d5}}f_2; X_3 = \frac{g_{m5}+g_{mb5}}{g_{d5}}f_3$$

$$X_4 = \frac{g_{m5}+g_{mb5}}{g_{d5}}f_4; X_5 = \frac{1}{g_{d5}+g_L}$$

Since g_{d5} is 15μ and g_L is equal to 1000μ, the transconductance was obtained:

$$X_5 = \frac{1}{g_{d5}+g_L} = \frac{1}{1015\mu}$$

By calculating all multiplication factors, we obtain:

$$S_{V_{out}} = (\frac{1}{364\mu})^2 S_{iN1} + (\frac{1}{40.75\mu})^2 S_{iN2} + (\frac{1}{2694\mu})^2 S_{iN3} + (\frac{1}{43.61\mu})^2 S_{iN4} + (\frac{1}{1015\mu})^2 S_{iN5}$$

As i_{N1}, i_{N2}, i_{N3}, i_{N4}, i_{N5}, and i_{N6} are the un-correlated random inputs of a linear system having V_N as output, the total spectral density of our circuit is given by:

$$S_N = \left|X\ (\omega)\right|^2.S_{i\ N} = \left|X_1(\omega)\right|^2.S_{iN1} + \left|X_2(\omega)\right|^2.S_{iN2} + \left|X_3(\omega)\right|^2.S_{i\ N3} +$$
$$+\left|X_4(\omega)\right|^2.S_{i\ N4} + \left|X_5(\omega)\right|^2.S_{iN5}$$

The same method leads us to calculate the out put power spectral density noise for Current Mediated APS in Difference Mode:

$$i_{N1} - g_{m1}V_s + (V_2 - V_s)g_{d1} - SCV_s = 0$$

$$V_2 = \frac{g_{m1} + g_{d1} + SC}{g_{d1}} V_S + \frac{i_{N1}}{g_{d1}} \& V_S = \frac{g_{d1}}{K_2} V_2 + \frac{i_{N1}}{K_2}$$

$$Where K_2 = g_{m1} + g_{d1} + SC$$

$$V_2(g_{d2} + g_{m3} + g_{mb3} - g_{d3}) + i_{n2} + i_{n3} - V_3 g_{d3} + V_s(SC + g_{m2}) = 0$$

$$V_2 . g_{d2} + i_{n2} + g_{m2}.V_s + V_s.Sc + g_{m3}V_2 + g_{mb3}V2 + i_{n3} + (V_2 - V_3)g_{d3} = 0$$

$$V_2 = \frac{g_{d3}}{K_1}.V_3 - \frac{g_{m2} + SC}{K_1} V_S + \frac{i_{n2}}{K_1} + \frac{i_{n3}}{K_1} (2) Where.K_1 = g_{d2} + g_{m3} - g_{d3}$$

$$2 \xrightarrow{1} V_2 = -\frac{g_{m2} + SC}{g_{m3}} \left(\frac{g_{d1}}{K_2} V_2 + \frac{i_{N1}}{K_2}\right) + \frac{i_{n2}}{K_2} + \frac{i_{n3}}{K_1} + \frac{g_{d3}}{K_1}$$

$$V_3 \longrightarrow V_2 = A.i_{N1} + B.i_{N2} + C.i_{N3} + DV_3$$

$$K_4 = 1 + \frac{g_{m2} + SC}{g_{m3}} \times \frac{g_{d1}}{K_1}$$

$$V_3(g_{m4} + g_{d4} + g_{d3} + g_{d5}) + i_{N4} + i_{N5} + V_2(-g_{m3} - g_{d3}) + i_{N3} = 0$$

$$A = -\frac{g_{m2} + SC}{g_{m3}} \times \frac{1}{K_4 K} B = \frac{1}{K_4 K} +; C = \frac{1}{K_4 K}; D = \frac{g_{d3}}{K_4 K_1}$$

$$V_3 = \frac{g_{m3} + g_{d3}}{g_{m4} + g_{d4} + g_{d3} + g_{d5}} V_2 + \frac{i_{N4} + i_{N5} + i_{N3}}{g_{m4} + g_{d4} + g_{d3} + g_{d5}}$$

$$Where.K_3 = g_{m4} + g_{d4} + g_{d3} + g_{d5}$$

$$K_5 = -\frac{g_{m3} + g_{d3}}{g_{m4} + g_{d4} + g_{d3}}$$

$$V_3 = K_5.V_2 + \frac{i_{N4}}{K_3} + \frac{i_{N3}}{K_3}$$

$$g_{m6}V_3 + g_{mb6}V_3 + g_{d5}V_{out} + i_{n6} = 0$$

$$V_{out} = X_1.i_{N1} + X_2.i_{N2} + X_3.i_{N3} + X_4.i_{N4} + X_5.i_{N5} + X_6.i_{N6}$$

Appendix B - Power Spectral Density in Direct Mode and Difference Mode

In order to calculate the output noise, the output current noise of each component was calculated.

Transistor T_1 turns off in read out mode:

$$S_{iN1} = (i_{N1})^2 / \Delta f = 4KT / R$$

$$S_{iN1} = (i_{N1})^2 / \Delta f = 4\times1.38\times10^{-23}\times300/5.39Y = 3.07\times10^{-36}$$

Transistor T_2 operated in saturation region the output current noise was:

$$S_{iN2} = (i_{N2})^2 / \Delta f = 4KT /(3/2g_{m2})$$

$$(i_{N2})^2 / \Delta f = 8\times1.38\times10^{-23}\times300\times32.78\times10^{-6}/3 = 3.6\times10^{-25}$$

Transistor T_3 operated in linear region and the output current noise was:

$$S_{iN3} = (i_{N3})^2 / \Delta f = 4KT / R$$

$$(i_{N3})^2 / \Delta f = 4\times1.38\times10^{-23}\times300/54.3K = 3.05\times10^{-25}$$

Transistor T_4 was in saturation region:

$$S_{iN4} = (i_{N4})^2 / \Delta f = 4KT /(\tfrac{3}{2g_{m4}}) + K\tfrac{I^a}{f^b}$$

$$(i_{N4})^2 / \Delta f = 8\times1.38\times10^{-23}\times300\times17.64u/3 = 1.92\times10^{-25}$$

Transistor T_5 was in saturation region:

$$S_{iN5} = (i_{N5})^2 / \Delta f = 4KT /(\tfrac{3}{2gm_5}) + K\tfrac{I^a}{f^b}$$

$$(i_{N5})^2 / \Delta f = 8\times1.38\times10^{-23}\times300\times425.3u/3 = 4.67\times10^{-24}$$

Current noise of the load resistor was calculated to be:

$$(i_{NRLoad})^2 / \Delta f = 4KT / R = 4KT / 1K = 1.65\times10^{-23}$$

We have:

$$S_{V_{out}} = (\tfrac{1}{364\mu})^2 S_{iN1} + (\tfrac{1}{40.63\mu})^2 S_{iN2} + (\tfrac{1}{2694.8\mu})^2 S_{iN3} + (\tfrac{1}{43.61\mu})^2 S_{iN4} + (\tfrac{1}{1015\mu})^2 S_{iN5}$$

From the output current noise, the total output Power Spectral Density was:

$$S_{V1} = (\tfrac{1}{364u})^2 Si_{N1} =\sim 0$$

$$S_{V2} = (\tfrac{1}{40.63u})^2 Si_{N2} = \tfrac{3.60\times10^{-25}}{(40.63u)^2} = 218.12\times10^{-18} V^2 / Hz$$

$$S_{V3} = (\tfrac{1}{2694u})^2 Si_{N3} = \tfrac{3.05\times10^{-25}}{(2694u)^2} = 0.04\times10^{-18} V^2 / Hz$$

$$S_{V4} = (\tfrac{1}{43.61u})^2 Si_{N4} = \tfrac{1.92\times10^{-25}}{(43.61u)^2} = 1.01\times10^{-16} = 101\times10^{-18} V^2 / Hz$$

$$S_{V5} = (\tfrac{1}{1015u})^2 S_{iN5} = \tfrac{4.67\times10^{-25}}{(1015u)^2} = 4.53\times10^{-18} V^2 / Hz$$

$$S_{V_{Rload}} = (\tfrac{1}{1015u})^2 S_{iNRLoad} = \tfrac{1.65\times10^{-23}}{(1015u)^2} = 1.60\times10^{-17} V^2 / Hz$$

If we exclude the noise of load resistor, total noise becomes:

$$S_{V_{Total}} = S_{V1} + S_{V2} + S_{V3} + S_{V4} + S_{V5} =$$
$$= (0 + 218 + 0.04 + 101 + 4.53)\times10^{-18} =$$
$$= 324\times10^{-18} V^2 / Hz$$

Contribution of each signal noise to form the total noise PSD is calculated as follows:

$$S_{V1} = 0\%.;.S_{V2} = 67.3\%.;.S_{V3} = 0.01\%.;.S_{V4} = 31.2\%.;.S_{V5} = 1.4\%$$

The output noise waveform plotted by Cadence shows that the total out put noise Power Spectral Density of APS circuit is:

$$S_{V_{out}} = 327\times10^{-18} V^2 / Hz$$

This noise includes the load resistance noise.

Excluding the load resistance noise, the simulation gives us 327-16 = 301 aV^2/Hz.

In Difference Mode the input current noise can be calculated as folow.

Transistor T_1 turns off in read out mode:

$$S_{iN1} = (i_{N1})^2 / \Delta f = 4KT / R$$

$$S_{iN1} = (i_{N1})^2 / \Delta f = 4\times 1.38\times 10^{-23}\times 300/5.39Y = 3.07\times 10^{-36}$$

$$S_{iN2} = (i_{N2})^2 / \Delta f = \frac{4KT\times 2g_{m2}}{3} = 8\times 1.38\times 10^{-23}\times 300\times 33.1\times 10^{-6}/3 = 3.64\times 10^{-25}$$

$$S_{iN3} = (i_{N3})^2 / \Delta f = 4KT/R = 4\times 1.38\times 10^{-23}\times 300/70.16k = 2.35\times 10^{-25}$$

$$S_{iN4} = (i_{N4})^2 / \Delta f = \frac{4KTx2g_{m4}}{3} = \frac{4KTx2}{3}\times 387.2u = 4.25\times 10^{-24}$$

$$S_{iN5} = (i_{N5})^2 / \Delta f = \frac{4KTx2g_{m5}}{3} = \frac{4KTx2}{3}\times 170.5u = 1.87\times 10^{-24}$$

$$S_{iN6} = (i_{N6})^2 / \Delta f = \frac{4KTx2g_{m6}}{3} = \frac{4KTx2}{3}\times 1.96m = 2.15\times 10^{-23}$$

$$(i_{NRLoad})^2 / \Delta f = 4KT/R = 4KT/1K = 1.65\times 10^{-23}$$

Now the output Power Spectral Density of each corresponding input constant to white noise is calculated as below:

$$S_{V1} = 0$$

$$S_{V2} = (\tfrac{1}{77.12u})^2 S_{iN2} = \frac{3.64\times 10^{-25}}{(77.12u)^2} = 61.2\times 10^{-18} V^2/Hz$$

$$S_{V3} = (\tfrac{1}{4.73m})^2 S_{iN3} = \frac{2.35\times 10^{-25}}{(4.73m)^2} = 1.05\times 10^{-20} V^2/Hz$$

$$S_{V4} = (\tfrac{1}{444.5m})^2 S_{iN4} = \frac{4.15\times 10^{-24}}{(444.5m)^2} = 2.1\times 10^{-23} V^2/Hz$$

$$S_{V5} = (\tfrac{1}{91.16u})^2 S_{iN5} = \frac{1.87\times 10^{-24}}{(91.16u)^2} = 2.25\times 10^{-16} V^2/Hz$$

$$S_{V6} = (\tfrac{1}{1073u})^2 S_{iN6} = \frac{2.15\times 10^{-23}}{(1073u)^2} = 1.87\times 10^{-17} V^2/Hz$$

$$S_{VRload} = (\tfrac{1}{1073u})^2 S_{iNRload} = \frac{1.65\times 10^{-23}}{(1073u)^2} = 1.43\times 10^{-17} V^2/Hz$$

Total noise power spectral density of the circuit excluding load resistance noise is:

$$S_{V_{Total}} = S_{V1} + S_{V2} + S_{V3} + S_{V4} + S_{V5} + S_{V6} =$$

$$= (0 + 61.2 + 0.01 + 0.00021 + 225 + 21.8)\times 10^{-18} =$$

$$= 307\times 10^{-18} V^2/Hz$$

$$S_{V1} = 0\%; S_{V2} = 20.19\%; S_{V3} = 0\%; S_{V4} = 0\%; S_{V5} = 73.08\%; S_{V6} = 6.85\%$$

If we include the resistor load noise we obtain:

$$S_{V_{Total}} = S_{V1} + S_{V2} + S_{V3} + S_{V4} + S_{V5} + S_{V6} + S_{VR\_Load} =$$
$$= 307 \times 10^{-18} + 14.3 \times 10^{-18} =$$
$$= 321 \times 10^{-18} V^2 / Hz$$

Appendix C- Signal waveforms of C.M. APS in Direct Mode and Difference Mode

Signal waveforms of APS in Direct Mode plotted by Cadence in Figure 4-1 to Figure 4-9. As mentioned before its noise bandwidth was 87*MHz*. Total out put noise at V_2 was 1.75 and out put spectral noise density at V_1 was 4.07.

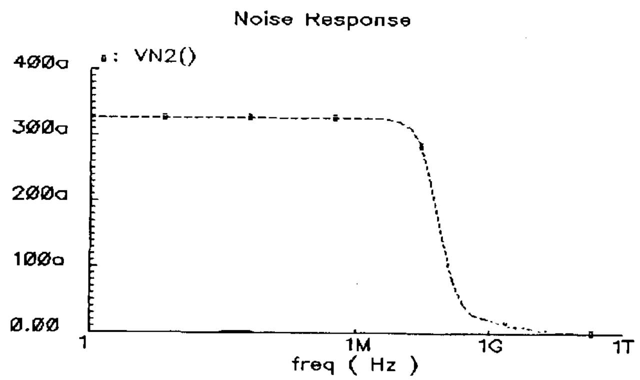

Figure 4-1: Total output noise at V_{direct}

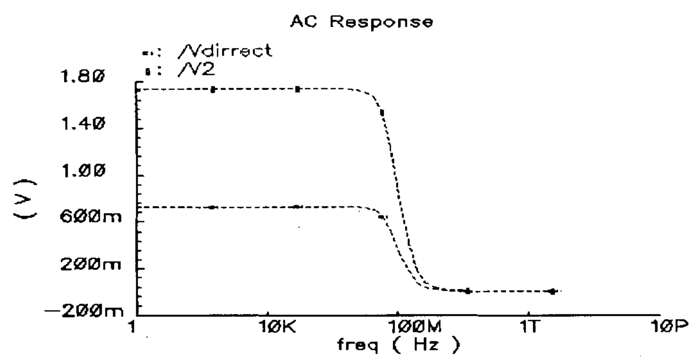

Figure 4-2: Transient voltage at V_{direct} and V_2

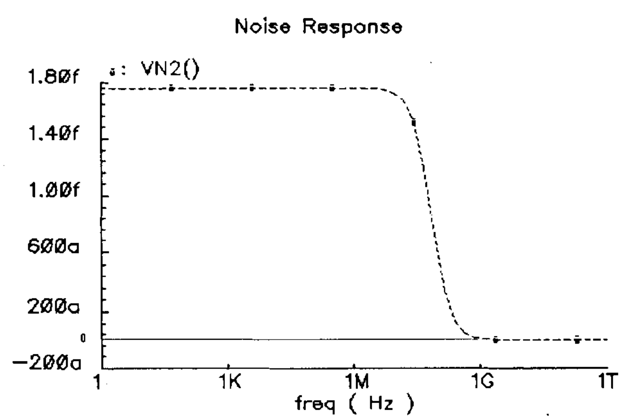

Figure 4-3: Output noise at V_2

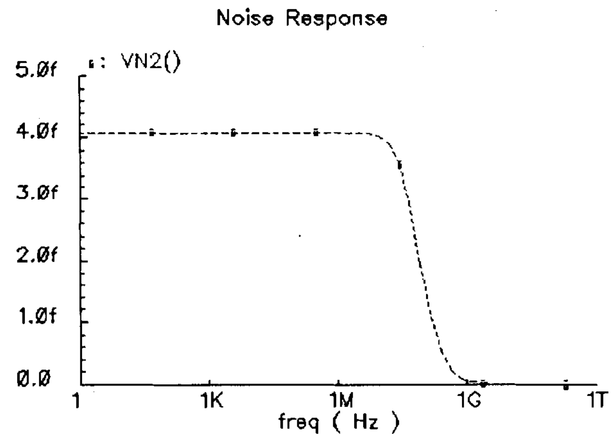

Figure 4-4: Output noise at V_1

Frequency response at V_{sense} and V_1 and transient response is plotted in Figures 4-5 to 4-9. At the sense node gain of circuit was 1 and at V_1 gain of circuit was 2.85.

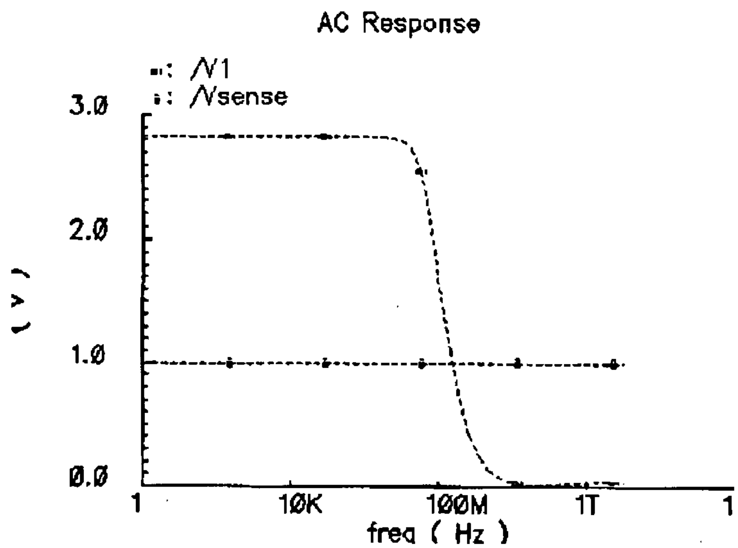

Figure 4-5: Frequency response at V_1 and V_{direct} in Direct Mode

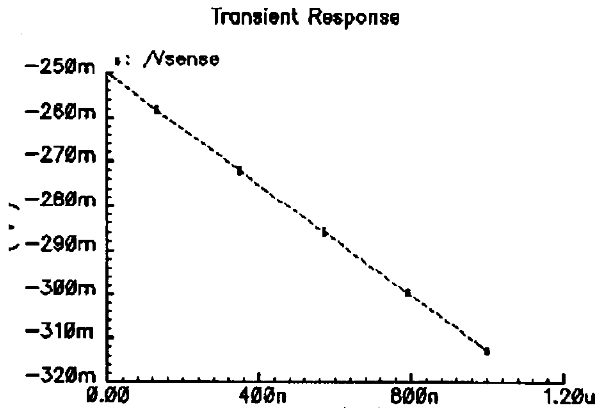

Figure 4-6: Sense node voltage in Direct Mode

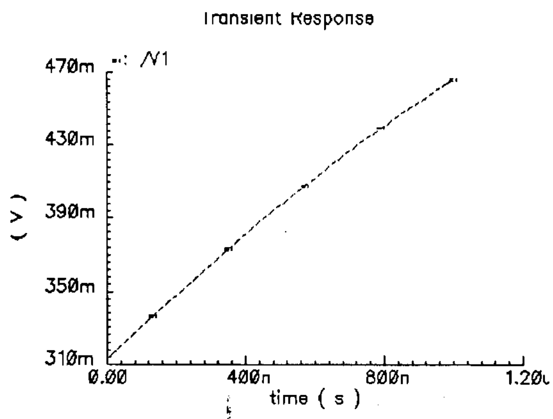

Figure 4-7: Transient response at V_1 in Direct Mode

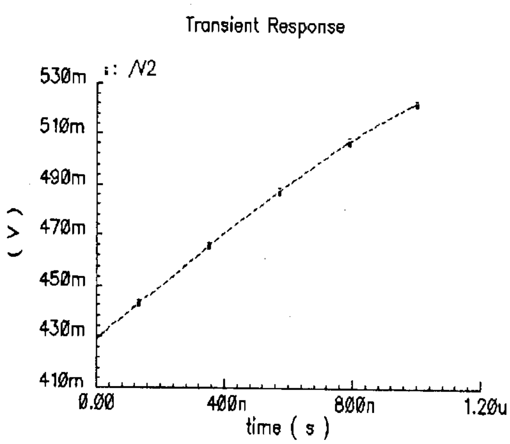

Figure 4-8: Transient response at V_2 in Direct Mode

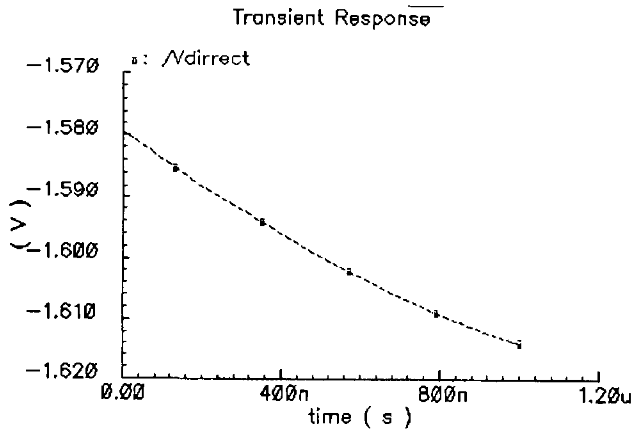

Figure 4-9: Transient response at V_{direct} in Direct Mode

Noise, transient and AC response for the APS operating in Difference Mode simulated in Cadence is plotted in Figure 4-10 to Figure 4-20.

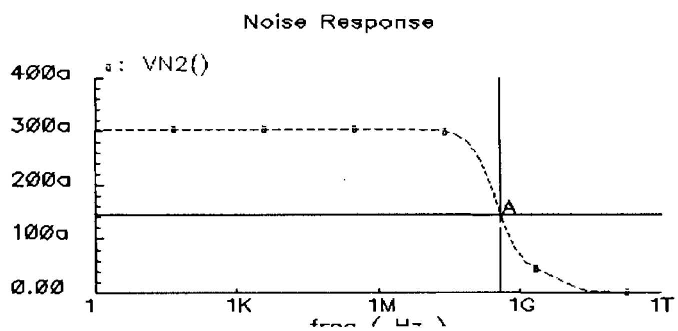

Figure 4-10: Total output noise in Difference Mode

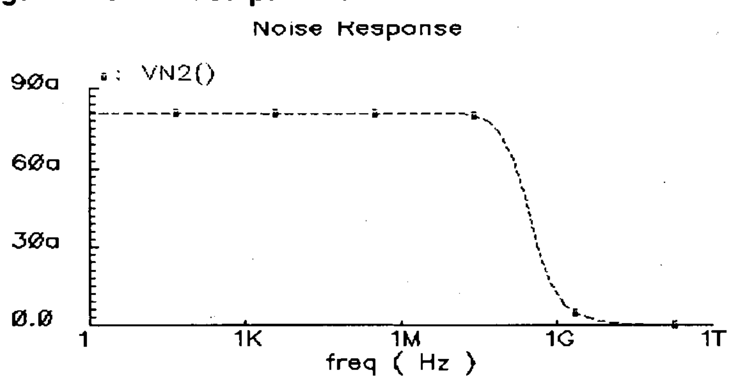

Figure 4-11: Output noise at V_2 in Difference Mode

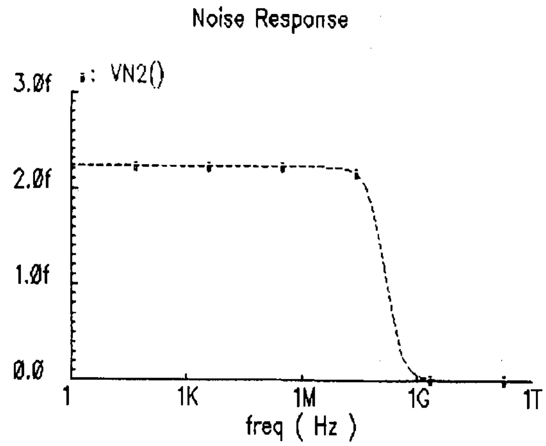

Figure 4-12: Output noise at V_1 in Difference Mode

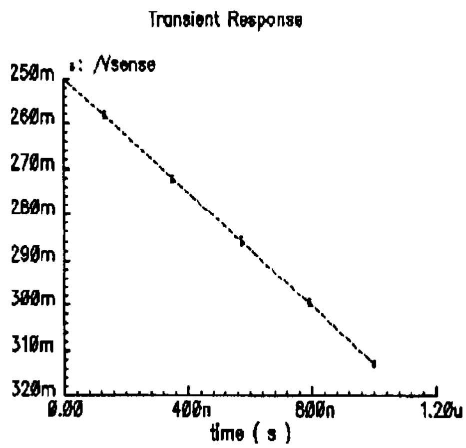

Figure 4-13: Transient response at sense node in Difference Mode

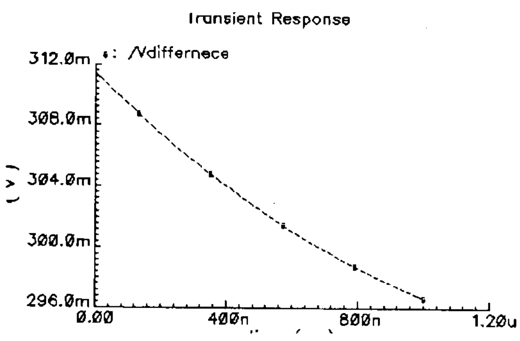

Figure 4-14: Transient response at output in Difference Mode

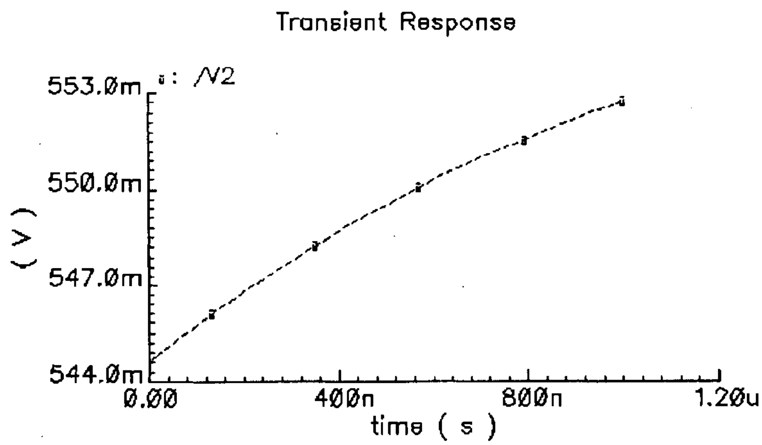

Figure 4-15: Transient response at V_2 in Difference Mode

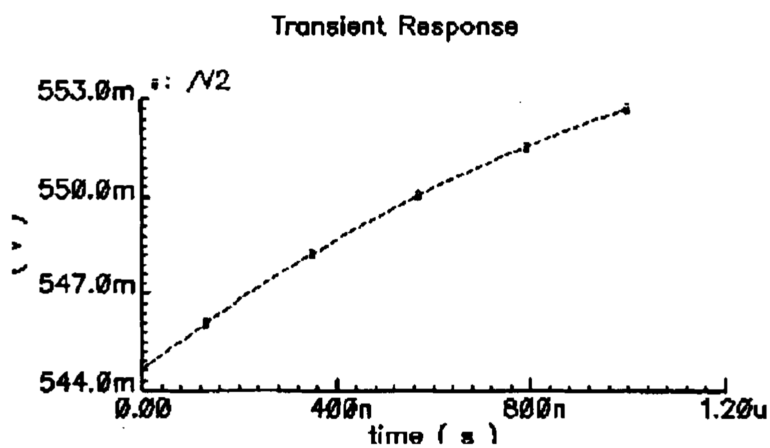

Figure 4-16: Transient response at V_1 in Difference Mode

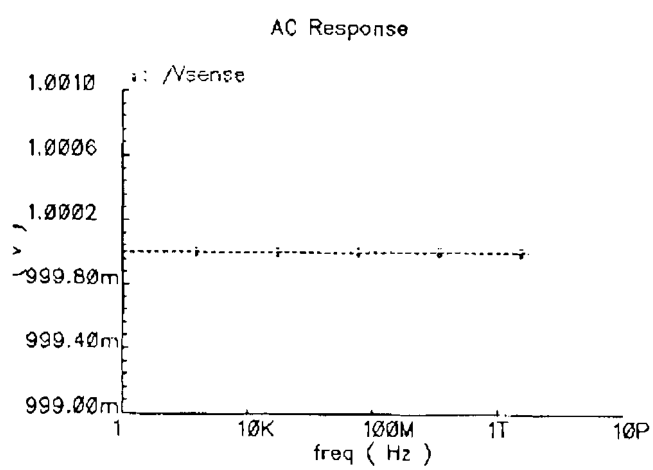

Figure 4-17: AC response at sense node in Difference Mode

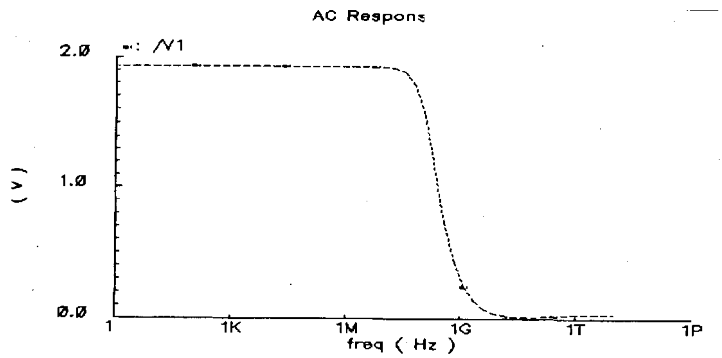

Figure 4-18: AC response at V_1 in Difference Mode

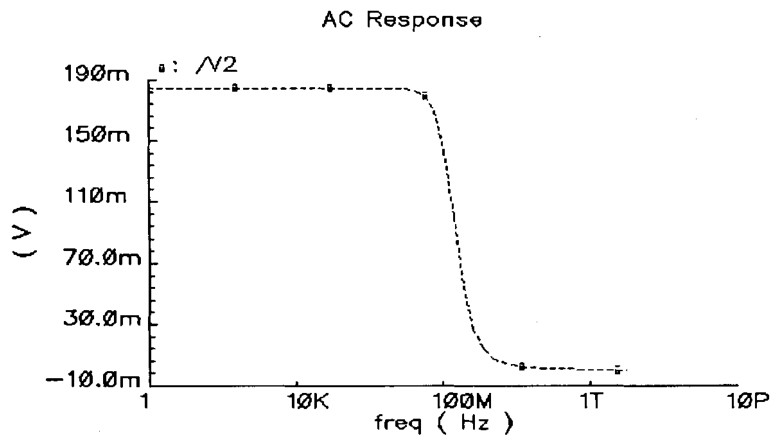

Figure 4-19: AC response at V_2 in Difference Mode

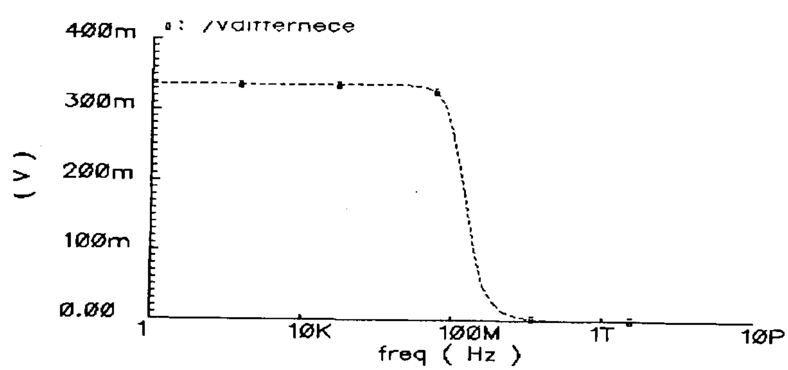

Figure 4-20: AC response at out put in Difference Mode

Appendix D - Electrical Parameters of C.M. APS in Direct Mode and Difference Mode

signal	OP("mt1" "??")
betaeff	427.8u
cbb	832.5a
cbd	0
cbg	-1.312f
cbs	479.7a
cdb	0
cdd	179.5a
cdg	-179.5a
cds	0
cgb	-832.5a
cgd	-179.5a
cgg	1.671f
cgs	-659.2a
cjd	1.565f
cjs	1.876f
csb	0
csd	0
csg	-179.5a
css	179.5a
gds	28.52e-27
gm	0
gmbs	-13.03e-27
gmoverid	0
ibulk	46.95p
id	2.978f
ids	104.4e-27
pwr	11.74p
region	0
reversed	0
ron	5.393Y
type	0
vbs	250m
vds	563.3m
vdsat	40.41m
vgs	-1.4
vth	504.6m

signal	OP("/T2" "??")
betaeff	425u
cbb	237.8a
cbd	0
cbg	-310.3a
cbs	72.57a
cdb	0
cdd	179.5a
cdg	-179.5a
cds	0
cgb	-131.3a
cgd	-179.5a
cgg	1.47f
cgs	-1.16f
cjd	1.565f
cjs	2.519f
csb	-106.4a
csd	0
csg	-980.6a
css	1.087f
gds	351.2n
gm	32.78u
gmbs	3.802u
gmoverid	15.39
ibulk	8.678m
id	2.13u
ids	2.13u
pwr	14.32m
region	2
reversed	0
ron	921.9K
type	0
vbs	758.2m
vds	1.963
vdsat	98.06m
vgs	1.4
vth	420.7m

signal	OP("/T3" "
betaeff	37.17u
cbb	4.364f
cbd	-2.023f
cbg	-1.283f
cbs	-1.057f
cdb	-1.48f
cdd	12.81f
cdg	-7.011f
cds	-4.314f
cgb	-1.278f
cgd	-6.574f
cgg	15.41f
cgs	-7.558f
cjd	1.529f
cjs	1.565f
csb	-1.606f
csd	-4.209f
csg	-7.115f
css	12.93f
gds	16.19u
gm	3.946
gmbs	1.071
gmoverid	1.853
ibulk	-5.956
id	2.13u
ids	2.13u
pwr	246.3n
region	1
reversed	0
ron	54.31K
type	0
vbs	-313.5m
vds	115.6m
vdsat	528.6m
vgs	1.187
vth	605.8m

signal	OP("mt4"
betaeff	96.99u
cbb	179.7a
cbd	0

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cbg	-284.8a
cbs	105.1a
cdb	-6.163e-33
cdd	155.5a
cdg	-155.5a
cds	6.163e-33
cgb	-128.9a
cgd	-155.5a
cgg	1.307f
cgs	-1.023f
cjd	2.889f
cjs	5.281f
csb	-50.83a
csd	0
csg	-867.1a
css	917.9a
gds	593.2n
gm	17.64u
gmbs	907n
gmoverid	8.274
ibulk	-2.28m
id	-2.13u
ids	2.132u
pwr	3.765m
region	2
reversed	0
ron	572.7K
type	1
vbs	1.213
vds	-1.221
vdsat	-204.9m
vgs	-1.221
vth	-592.9m
signal	OP("mt5" "??")
betaeff	1.393m
cbb	776a
cbd	0
cbg	-2.265f
cbs	1.489f
cdb	-98.61e-33
cdd	1.839f
cdg	-1.839f
cds	98.61e-33
cgb	-113.5a
cgd	-1.839f
cgg	14.36f
cgs	-12.4f
cjd	11.5f
cjs	48.6f
csb	-662.6a
csd	0
csg	-10.25f
css	10.91f
gds	15.36u
gm	425.3u
gmoverid	6.04
ibulk	-26.12m
id	-70.42u
ids	70.42u
pwr	43.32m
region	2
reversed	0
ron	45.86K
type	1
vbs	1.249
vds	-3.23
vdsat	-273.8m
vgs	-1.221
vth	-479.1m

Figure 4-21: Electrical parameters of C.M. APS in Direct Mode

signal	OP("mt1" "??")
betaeff	427.8u
cbb	832.5a
cbd	0
cbg	-1.312f
cbs	479.7a
cdb	0
cdd	179.5a
cdg	-179.5a
cds	0
cgb	-832.5a
cgd	-179.5a
cgg	1.671f
cgs	-659.2a
cjd	1.539f
cjs	1.876f
csb	0
csd	0
csg	-179.5a
css	179.5a
gds	28.13e-27
gm	0
gmbs	-13.35e-27
gmoverid	0
ibulk	46.95p
id	2.978f
ids	106.7e-27
pwr	11.74p
region	0
reversed	0
ron	6.028Y
type	0
vbs	250m
vds	643.3m
vdsat	40.41m
vgs	-1.4
vth	504.4m

signal	OP("mt2" "??")
betaeff	425u
cbb	237.8a
cbd	0
cbg	-310.3a
cbs	72.57a
cdb	-12.33e-33
cdd	179.5a
cdg	-179.5a
cds	12.33e-33
cgb	-131.3a
cgd	-179.5a
cgg	1.47f
cgs	-1.16f
cjd	1.539f
cjs	2.519f
csb	-106.4a
csd	0
csg	-980.6a
css	1.087f
gds	348.7n
gm	33.1u
gmbs	3.833u
gmoverid	15.34
ibulk	8.678m
id	2.157u
ids	2.157u
pwr	14.32m
region	2
reversed	0
ron	947.1K
type	0
vbs	758.2m
vds	2.043
vdsat	98.14m
vgs	1.4
vth	420.5m

signal	OP("mt3" "??")
betaeff	37.32u
cbb	4.251f
cbd	-1.891f
cbg	-1.301f
cbs	-1.059f
cdb	-1.396f
cdd	12.13f
cdg	-6.896f
cds	-3.837f
cgb	-1.289f
cgd	-6.256f
cgg	15.35f
cgs	-7.806f
cjd	1.497f
cjs	1.539f
csb	-1.566f
csd	-3.983f
csg	-7.153f
css	12.7f
gds	11.35u
gm	5.224u
gmbs	1.352u
gmoverid	2.421
ibulk	-5.956f
id	2.157u
ids	2.157u
pwr	326.6n
region	1
reversed	0
ron	70.16K
type	0
vbs	-393.5m
vds	151.4m
vdsat	447.5m
vgs	1.107
vth	626.2m

signal	OP("m4" "??")
betaeff	2.309m
cbb	1.291f
cbd	-1.393f

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cbg	-209.4a
cbs	311.7a
cdb	-500.6a
cdd	5.751f
cdg	-3.119f
cds	-2.131f
cgb	-138.8a
cgd	-2.707f
cgg	6.917f
cgs	-4.071f
cjd	4.98f
cjs	5.152f
csb	-651.3a
csd	-1.651f
csg	-3.588f
css	5.891f
gds	349u
gm	283.6u
gmbs	61.03u
gmoverid	2.836
ibulk	-16.17f
id	100u
ids	100u
pwr	18.74u
region	1
reversed	0
ron	1.874K
type	0
vbs	-546.8m
vds	187.4m
vdsat	319.9m
vgs	1.105
vth	701.3m
signal	OP("m5" "??")
betaeff	445.4u
cbb	223.3a
cbd	0
cbg	-310.3a
cbs	87.06a
cdb	0
cdd	179.5a
cdg	-179.5a
cds	0
cgb	-116.8a
cgd	-179.5a
cgg	1.47f
cgs	-1.174f
cjd	1.499f
cjs	2.519f
csb	-106.5a
csd	0
csg	-980.6a
css	1.087f
gds	5.627u
gm	170.5u
gmbs	14.97u
gmoverid	1.743
ibulk	8.589m
id	97.84u
ids	97.84u
pwr	14.39m
region	2
reversed	0
ron	22.43K
type	0
vbs	757.5m
vds	2.195
vdsat	543.2m
vgs	2.195
vth	420.4m
signal	OP("m15" "??")
betaeff	6.246m
cbb	1.485f
cbd	0
cbg	-2.3f
cbs	815.6a
cdb	0
cdd	2.077f
cdg	-2.077f
cds	0
cgb	-202.8a
cgd	-2.077f
cgg	15.73f
cgs	-13.45f
cjd	13.45f
cjs	24.07f
csb	-1.282f
csd	0
csg	-11.35f
css	12.63f
gds	73.14u
gm	1.963m
gmbs	145.3u
gmoverid	1.466
ibulk	100.4m
id	1.339m
ids	1.339m
pwr	168.2m
region	2
reversed	0
ron	1.465K
type	0
vbs	814m
vds	1.961
vdsat	545.2m
vgs	2.195
vth	417.5m

Figure 4-22: Electrical parameters of C.M. APS in Difference Mode

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