A HIGH EFFICIENCY EER-BASED TRANSMITTER

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ABSTRACT

The efficiency and linearity of a Power Amplifier (PA) is critical for a transmitter in most wireless communication systems. A lot of research has been done to improve these two parameters in transmitters. This project focuses on the highly efficient Radio Frequency Power Amplifier (RF-PA) implementation using Envelop Elimination and Restoration (EER) architecture with dynamic drain voltage supplier. The transmitter has been designed and implemented the entire transmitter in MATLAB/SIMULINK. Each individual component is implemented to include envelop and phase extraction, digitally controlled DC-DC converter, E-class power amplifier and phase shifter. In this report, simulation results have been presented along with an analysis of results, showing that limitations in the performance of some of the components affect the overall system performance.

Keywords:

Power Amplifier; Envelop Elimination and Restoration architecture; wireless communication systems; transmitters; digitally controlled DC-DC converter; E-class power amplifier

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1. INTRODUCTION

In a battery-powered system, especially in mobile communication, managing power consumption has recently attracted more and more attention. Power efficiency is becoming a very important part of the system design. Since the Radio Frequency Power Amplifier (RF-PA) is usually the most significant power-consuming component, a lot of research and studies have been done in this area, with several power management schemes been proposed to minimize its power consumption. This project is based on a system-level power management scheme, which applies a series of approaches to reduce the power consumption of the front-end transmitter.

First, a high efficiency E-class PA is deployed with Envelope Elimination and Restoration (EER) operation architecture. The input baseband signal is decomposed into the envelope and phase paths. The phase component is used to modulate the local oscillator output (RF carrier signal) to generate a phase modulated RF signal with a constant envelope. This signal is the input to an E-class RF-PA. The envelope of the baseband signal modulates the power supply voltage of the PA. Such a modulation restores the envelope of the RF output.

The system uses a dynamic controlled DC-DC converter as a voltage supplier. The adjustable drain voltage senses the average power level of the received signal and improves

the RF-PA efficiency. The input voltage of DC-DC converter is in a range of 2V to 6V, depending on the usage of the battery. The output voltage is tightly regulated in an assigned level, such as 3V for the load components in normal operational situation. The entire system also has different modes of operation. For example, it is typically in the "on" status or the heavy-load mode in normal operational condition, and in the "stand-by" or the light-load mode which needs low-level voltage supply. Through detecting the output voltage level of the load component, the digital controlling system compares sensing signal with the referenced command signal, and regulates the new output following the request of the command signal. In the steady-state of operation, the controller keeps the output inside a small regulation window around the command signal. If errors are found between sensed signal and command signal, the voltage output adjusts to follow the command signal. A digital controller (FPGA or IC Processors based) is designed for DC-DC converter working in high frequency switch-mode to improve the power efficiency over the wide range of power [1].

This project is to study the previous research [1], [2] and implement a complete RF front-end system based on a FPGA controller, using Matlab simulation. The system contains an E-class RF-PA with EER operation architecture, a dynamic digitally controlled DC-DC Converter, and a FPGA-based digital controller. The simulation results and relevant analysis provide a prototype and basis for further design.

This report is organized as follows: Chapter 1 is a brief introduction. Chapter 2 gives the background information related to the project, such as E-class Power Amplifier, EER architecture and digital PID control theory, etc. The system block diagram, on which the simulation is based, is also shown. Chapter 3 presents the simulation process of the E-class PA with EER architecture. Chapter 4 describes detailed module design and implementation for digitally controlled converter in both CCM mode and DCM mode. Chapter 5 shows the simulation results and the necessary analysis of the entire system.

2. TRANSMITTER USING EER ARCHITECTURE

2.1 EER Architecture-Based Transmitter

Figure 1 shows a system level block diagram of an EER-based transmitter [1].

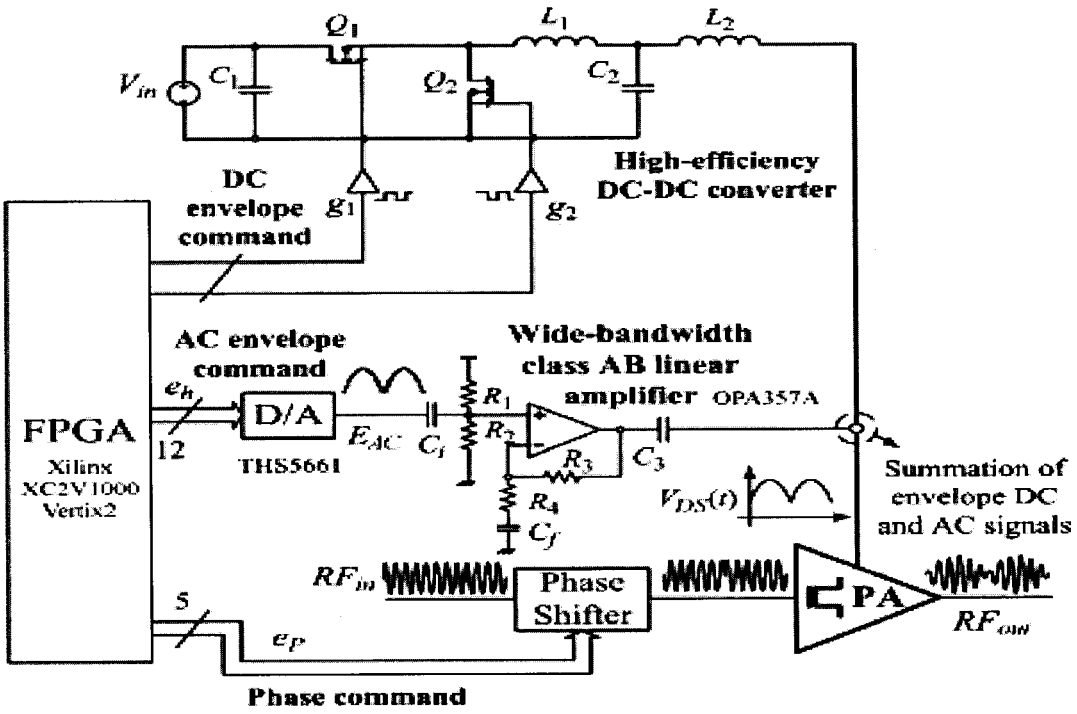

Figure 1 Top-Level System Block Diagram for Simulation

The system contains three key components: The first one is a high efficiency buck DC-DC converter, which provides steady voltage supply to RF-PA. Its dual switching control pulses come from an FPGA-based digital controller. The second part is the FPGA-based digital controller which receives the feedback error signals, transmits them to

two complementary 1MHz pulse signals with dynamic duty cycles, and then provides switching control signals to turn-on or turn-off the MOSFET in DC-DC converter. Another function of this part is to split the RF signals to envelope and phase paths. The envelope path is further discomposed to DC component and AC component. The AC envelope and phase paths are output in forms of 12-bit and 5-bit digital signals respectively. The DC component of the envelope acts as a referenced command signal to regulate the output of the DC-DC Converter. The third key component is an E-class PA with EER operation architecture. It receives a phase modulated RF input and its drain supply voltage is an envelope modulated signal. The output is the RF signal with the restored envelope.

Other components in the system include the phase shifter, DA converter, linear pre-amplifier, and summation circuit which combines DC and AC components in the envelope. The phase shifter performs phase modulation on the RF carrier signal. An off-the-shelf digitally controlled phase modulator can be used. The 5-bit digital signal is driven by the FPGA. The output of the phase shifter is simply a constant envelope, phase modulated RF carrier. The 12-bit envelope signal generated by the digital controller (FPGA) is converted to a base-band analog signal by a Digital-Analog Converter (DAC). After passing through a low-pass filter, the base-band signal is linearly amplified and then mixed with the DC voltage offset from DC-DC converter. This signal, which contains envelope information, will be the drain voltage supply of the E-class PA.

The entire system for the simulation is introduced primarily from two sections, one is E-class PA with EER architecture in chapter 3, and another is digitally controlled DC-DC converter in chapter 4. Functions of the FPGA-based digital controller will be described in these two chapters along with these two sections.

2.2 E-class Power Amplifier

The E-class Power Amplifier which is one of the key components in an EER-based transmitter was first introduced by N. O. Sokal in 1975 [3]. The E-class PA uses a single active device driven as a switch and a specially designed passive load network. The use of a single device in a switching amplifier eliminates the requirement for a complex designed passive load network, such as complex (Band-Limiting) transformer structures, thus reducing the overall complexity.

The schematic for the basic E-class amplifier topology is illustrated in Figure 2. A typical E-class PA consists of an active device, a RF choke and surrounding passive elements that form the load network.

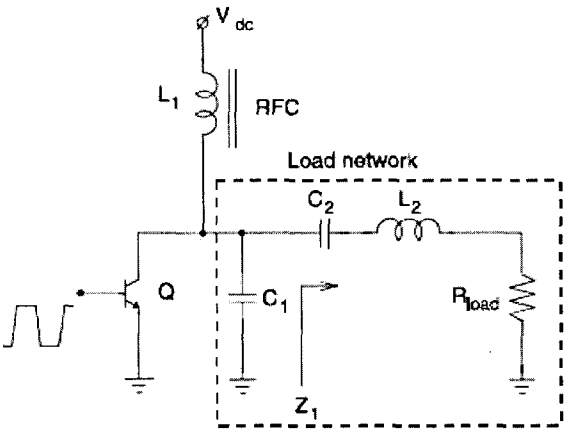

Figure 2 Basic E-class Power Amplifier

The transistor operates as a switch: in the ON state it is heavily overdriven by the input signal, and in the OFF state it is in the cut-off state. It alternately opens and closes at operating frequency, and the duty cycle can be arbitrarily chosen. The sinusoidal output voltage is obtained as a result of the switching action of the device and the transient response of the load network. To achieve maximum output power capability, the duty cycle of the switch is assumed to be 50% [4]. In the ideal situation mentioned above, the efficiency of an E-class amplifier is 100%. However, in practice, the switch has a finite on-resistance, and the transition times from the off-state to the on-state and vice-versa are not negligible. Among all the power amplifier topologies, the E-class amplifier has the highest ideal efficiency along with the smallest number of components. It presents an attractive solution for mobile communication and portable radio devices.

2.3. Envelope Elimination and Restoration (EER) Architecture Using E-class PA

The envelope elimination and restoration (EER) technique was first proposed by Kahn in 1952. It is essentially a high-level modulation technique.

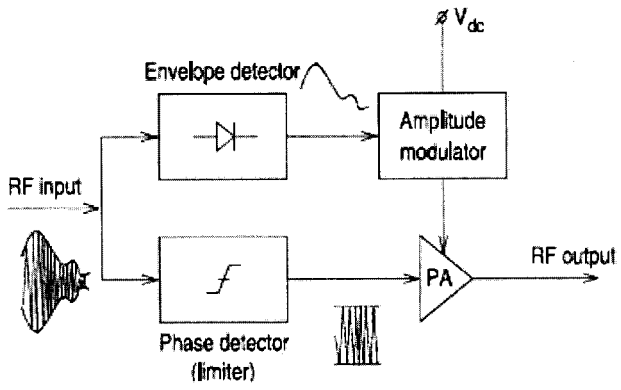

Figure 3 Basic Block Diagram of EER Concept

The input signal, shown in Figure 3, which may contain both the amplitude and phase modulation, is split into a baseband path containing the envelope of the input signal and an RF path containing a constant-envelope phase modulated carrier signal [5]. The constant-envelope, phase-modulated carrier is then amplified by a high-efficiency RF amplifier. The drain voltage of the PA is already modified by the baseband envelope path. This high-level, and high-power modulation results in the restoration of the input signal if the delays of both paths are suitably equalized.

The amplitude of the phase-modulated signal is kept fixed at a large enough value and drives the PA to ensure optimal PA saturation and high efficiency at the peak envelope level. But for lower envelope levels, a smaller drive signal is sufficient to cause saturation and high efficiency. Therefore, by regulating the RF drive amplitude in proportion to the signal envelope, the efficiency of the Kahn method can be optimized over all envelope levels.

Previous research [6] has shown that the design of low voltage, high efficiency E-class PA, can be used with either of the modulation schemes described previously. In the case of E-class PAs, it is difficult to discuss linearity, since the circuit does not really perform the amplification. The input signal is seen just as information to trigger the active device (i.e. the switch). The amplitude of the output voltage is entirely determined by the supply voltage and load network elements. Consequently, the best method to linearize an E-class amplifier is the EER technique [6]. On using this technique, the amplitude variations in the signal are initially canceled. The resulting constant envelope signal is then amplified in the high efficiency saturation power amplifier, and the amplitude variations are added at the final stage restoring the envelope of the signal. Thus, the information contained in the phase of the input signal is preserved in the output signal, and the envelope is reconstructed through modulation of the supply voltage.

2.4 DC-DC Converter and its two operating modes

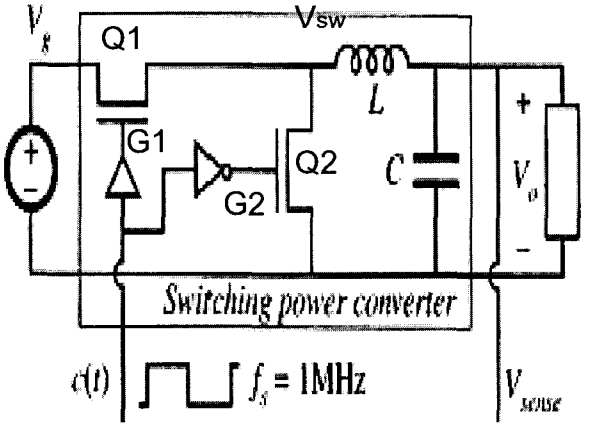

Figure 4 A Typical Buck DC-DC Converter

The second critical component in this projectis the DC -DC converter. A simple buck DC-DC design is shown in Figure 4. In steady state, the DC-DC converter is driven by gate control switched-pulses G1 and G2 which are complementary to each other. When G1 is high, the MOSFET Q1 is turned on and Q2 is turned off As a result, current of the inductor L ramps up and the capacitance C is charged. The switching voltage also goes high. On the other hand, when G1 becomes low, G2 turns high, Q1 is turned off and Q2 gets turned on. Consequently, C is discharged thru L and Q2. This cycle repeats. The duty cycle of the control signal determines the output voltage.

The efficiency of the PWM mode DC-DC drops when the load is light [2]. To improve efficiency at the light load, a dual-mode operation is proposed. The constant-frequency continuous conduction mode (CCM) described above is applied for the

high-load operation mode. In this working mode, two control switching pulses are complementary and their combined duties occupy almost the whole switching cycle. But when the load is light, most of the power is not consumed in driving the load, but wasted in turning on and off the MOSFET transistors. In contrast to the CCM mode, the Discontinuous Conduction Mode (DCM) is used for the light-load operation mode, in which the converter operates in a discontinuous conduction mode at a variable switching frequency. In this mode, two control switching pulses do not cover the entire duty cycle. Instead, G1 goes high for a period of time followed by G2. G2 goes low when the output voltage exceeds certain level. There will be a 'silent period' when both switches are off. G1 is turned on when the output voltage drops under a threshold.

DC-DC converter for a battery-powered system usually has a range of input voltage (for example, the output voltage of a single-cell Li-Ion battery range from 2V to 5.5V), but needs a tightly regulated output voltage. Based on its load, the system operates between the following two modes: CCM mode for heavy-load mode which working in a high power level; and DCM mode for a light-load in a low power level.

2.5 Digital PID-Control and Compensation Topology

The control loop of the DC-DC converter compares the output (V_{out}) to the reference voltage (V_{ref}) and uses the difference of the two signals to modulate the duty cycle of the control signal (PWM modulation) in CCM mode.

Typically in such a control loop, Proportional-Integral-Derivative (PID) Algorithm is used to reduce the output fluctuation (noise). A typical PID Control moduleis shown in Figure 5.

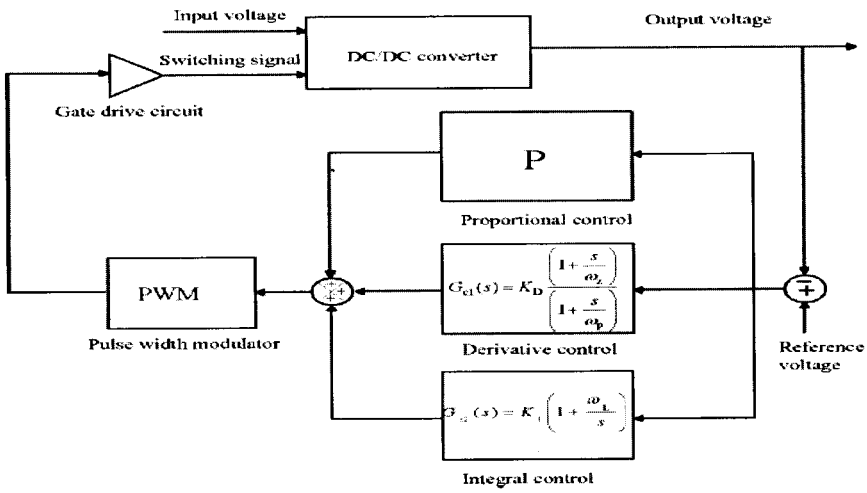

Figure 5 A Basic PID Controller

The transfer function of the continuous time control for a buck DC-DC converter is given as follows [2], [8] and [9]:

$$G_{vd}(s) = \frac{V_{in}}{1 + \frac{s}{Q\omega_0} + (\frac{s}{W_0})^2}; \quad \text{where: } Q = R\sqrt{\frac{L}{C}}, and \omega_0 = 2 * \pi * f_0 = \frac{1}{\sqrt{LC}} \qquad (1)$$

Based on the above transfer function, the continuous-time PID regulator described in time domain is as follows:

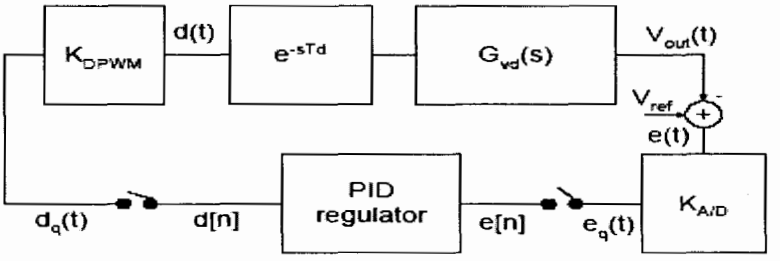

Figure 6 PID Controlling-Loop Block Diagram

Here, $K_{A/D}$, K_{DPWM} and e^{-sT_d} respectively represent transfer coefficients of the AD converter, Pulse-Width-Modulation module and entire loop-delay. So,

$$d(t) = k\left(e(t) + \frac{1}{T_i}\int e(t)dt + T_d \frac{de(t)}{dt} \right) \qquad (2)$$

where, k is total gain of all components in the loop except PID regulator, T_i and T_d are the integral and differential constants. Its LapLace transform is:

$$G_{comp}(s) = \frac{d^*(s)}{v_e(s)} = K_c \frac{1 + \frac{s}{Q_{comp}\omega_z} + \frac{s^2}{\omega_z^2}}{s} \qquad (3)$$

The digital PID compensator has the following form:

$$d(n) = d(n-1) + a * e(n) + b * e(n-1) + c * e(n-2) \qquad (4)$$

d(n) is the current digital duty-cycle command, d(n-1) is from the previous cycle, and e(n) is the digital error signal obtained from comparing the output voltage V_{out} with the reference V_{ref}, and e(n-1), e(n-2) are from e(n) delayed one or two cycles respectively. These three error items create the cycle correction command.

The compensator coefficients a, b, c can be found from the PID transfer function by pole-zero matching method.

$$r = \exp\left(-\frac{\pi * f_z}{Q_{comp} f_{sw}}\right), \text{ and } b = -a * 2r * \cos\left(2\pi * \frac{f_z}{f_{sw}}\right), \text{ and } c = a * r^2 \qquad (5)$$

The value of a is determined such that the magnitude corresponding to the discrete-time implementation approximately matches the magnitude corresponding to the continuous-time compensator at the desired crossover frequency. In our case, the DC-DC converter works at the switching frequency of 1 MHz, and we use the following parameters for the discrete components:

$R = 50\Omega, L = 10\mu H, and C = 10\mu F$; and for the compensator,

$Q_{comp} = 1.27, f_z = \omega_z / 2\pi = 10.4kHz, k_c = 38krad/s$

Here, we consider the input voltage V_{in} = 5V, the delay of the digital control part from the output of the DC-DC converter to the duty cycle of the switching control pulse as $T_s / 2$, and AD convert gain $1/V_q$ = 1/30mV.

The computed coefficients are: a=0.29199; b=-0.56787; and c=0.27734 (6)

Based on formula (4) and the above compensator coefficients a, b and c in (6), we implement a digital compensator for the digital controller used in our system.

3. DESIGN AND SIMULATION OF E-CLASS PA WITH EER ARCHITECTURE

This chapter provides the implementation details of the transmitter. We initially provide the design of the individual components. The top-level design is given later.

3.1 Design and Implementation of E-class PA

Based on the E-class PA diagram shown in Chapter 2.2, the basic E-class PA module in Matlab is implemented as shown Figure 7.

The ideal E-class amplifier block built consists of a MOSFET Q which acts as a switch, a bias choke RFC, a capacitor C_q, a tuned circuit L-C, and a resistive load R_{load}. The transistor switch Q is 'on' for half of the period, and 'off" for the other half. When Q is 'on', the voltage across Q is zero; and when it is 'off', the current through Q is zero.

The capacitor C_q includes the parasitic capacitance across the transistor. The L-C circuit resonates at the fundamental frequency of the input signal and only passes a sinusoidal current to the load R_{load}.

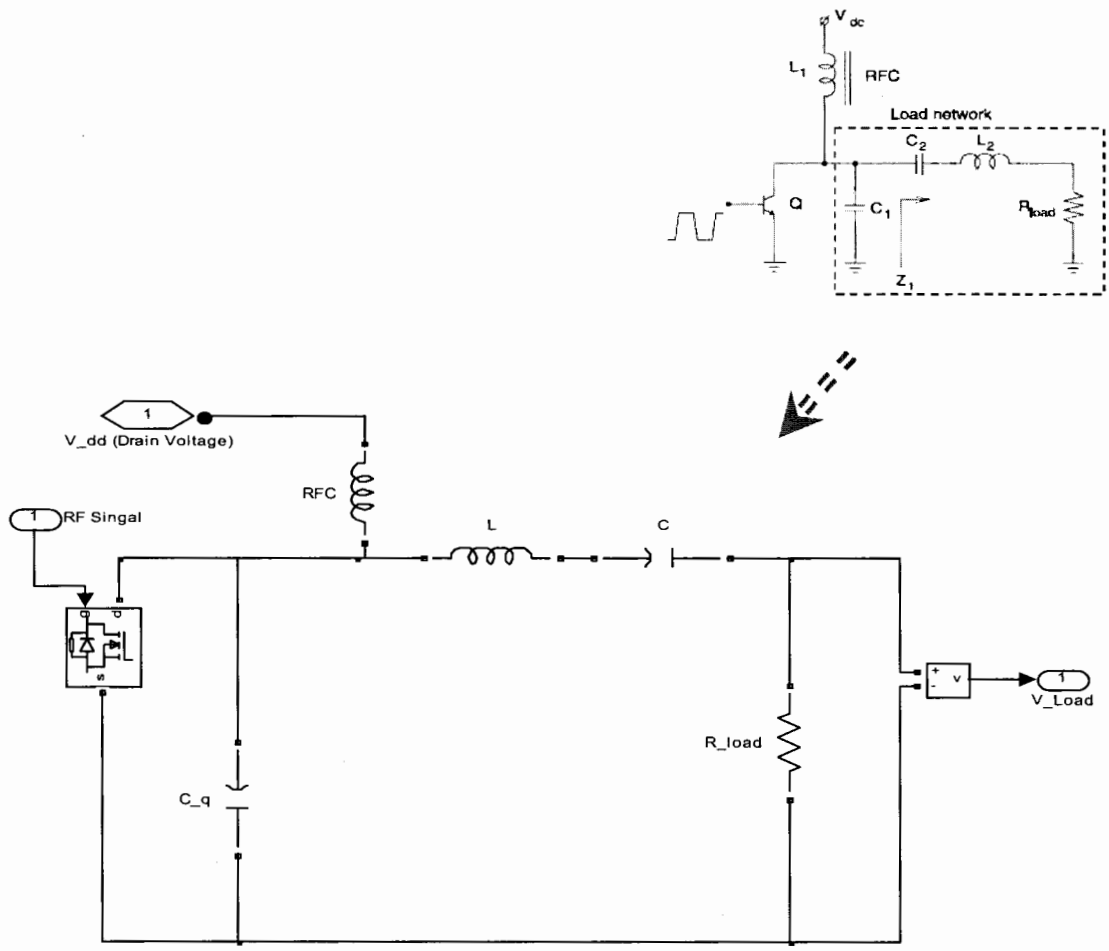

Figure 7 Implementation Block Diagram of E-class Amplifier

The following formulas give the computation of the parameters of the components in the E-class PA design [10], [11]. When the switch Q is off, the voltage V_q is given by solving the equation:

$$C_q \frac{dV_q}{dt} = I_d(1 - a\sin(w_s t + \phi)) \qquad (7)$$

where w_s is the signal frequency, I_d is the dc portion of the drain current, and constants a and □are constants that are yet to be calculated. Then,

$$V_q(t) = \frac{I_d}{w_s C_q}(w_s t + a(\cos(w_s t + \phi) - \cos\phi)) \qquad (8)$$

To avoid power dissipation due to either shorting of the capacitor C_q while there is a voltage drop across it during the switching or ensuring a "soft" turn-on condition for the switching device, the other two conditions listed below for the E-class operation are:

$$V_q(\frac{T_s}{2}) = 0 \quad \text{and} \quad \frac{dV_q}{dt}(\frac{T_s}{2}) = 0$$

Using these two conditions, constants a and ϕ are calculated to be:

$$a = \sqrt{1 + \frac{\pi^2}{4}} \approx 1.862 \qquad \text{and} \qquad \phi = -\arctan(\frac{2}{\pi}) \approx -32.48^o$$

The capacitor voltage V_q and its current i_q are known in the whole range as:

$$V_q(t) = \frac{I_d}{w_s C_q}((w_s t) + a(\cos((w_s t) + \phi) - \cos\phi)) \quad \text{in} \quad 0 \le w_s t \le \pi \qquad (9)$$

$$V_q(t) = 0 \qquad \text{in} \quad \pi \le w_s t \le 2\pi \qquad (10)$$

$$i_q(t) = 0 \qquad \text{in} \quad 0 \le w_s t \le \pi \qquad (11)$$

$$i_q(t) = I_d(1 - a\sin(w_s t + \phi)) \qquad \text{in} \quad \pi \le w_s t \le 2\pi \qquad (12)$$

From equations(8) to (11), the Load Z *l* at the fundamental frequency is:

$$Z_l = \frac{V_{ql}}{i_{ql}} = \frac{0.28}{w_s C_q} e^{j49^o} \qquad (13)$$

To simplify the analysis, the load network can just be treated as a RLC series [12]. Input impedance of this simple load network is given as:

$$Z_{load} = jw_s L_{load} + \frac{1}{jW_s C_{load}} + R_{load} \qquad (14)$$

The load component values are obtained by matching the real and imaginary parts of the equations (13) and (14), [12]:

$$C_q = \frac{1}{2\pi f_s R(\frac{\pi^2}{4}+1)(\frac{\pi}{2})} \qquad \text{and} \qquad L_{load} = \frac{Q_L R}{2\pi f_s}$$

For the bias choke RFC, we have $L_{RFC} = \frac{1}{(kw_s)^2 C_q}$ where factor k is the resonant ratio. To obtain the higher power output and drain efficiency, we choose:

$Q_L = 2.5$ and $k = 1.412$

Using a carrier with center frequency of 850 MHz, a typical PA designed as above is simulated with a constant drain voltage of 3V. The simulation waveforms are shown in Figure 8. As seen in the waveforms, the transistor works only in half cycle of the input signal. The capacitor C_q charges and discharges with the load when Q is "off", and its voltage reduces to zero when Q is "on". The output waveform is still a sinusoidal wave due to the switch transistor and its transient response from the load circuit. The transistor can be clearly seen as 'on' in half cycle, and 'off' in another half.

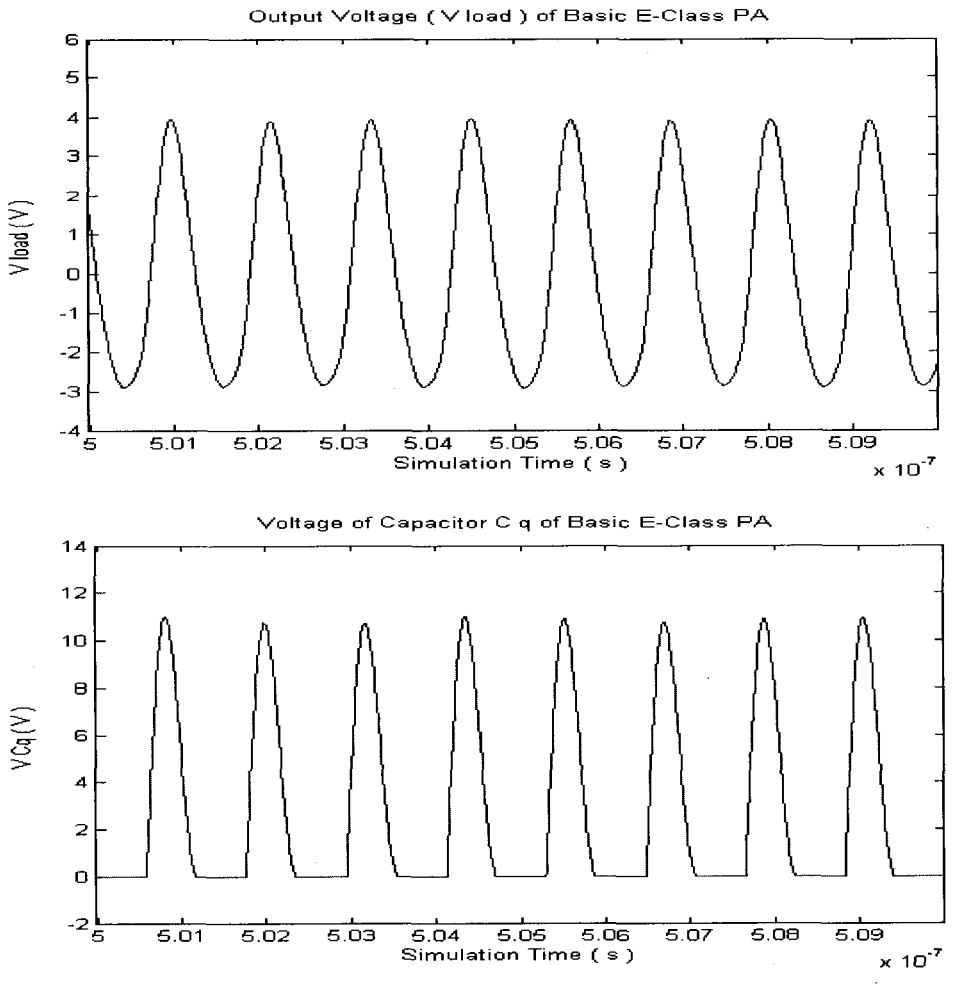

Figure 8 **Simulation Results for basic E-class PA Module:**
a. Output Voltage: Vload; b. Voltage of Capacitor Vq;

The drain voltage supply is then replaced from a fixed source to a dynamic source, which in the EER transmitter corresponds with the envelope of the input signal. We can see that the output voltage V_{load} changes with both input control signal and drain voltage in Figure 9. This change keeps the frequency (and phase) characteristic as a basic E-class PA, but its envelope as linear modulated by the dynamic drain voltage source. This

characteristic is as expected as an E-class PA in the EER-based transmitter described in section 2.3. The dynamic drain source used here is $V(t) = 3 + 2\sin(2\pi * 38.4e6)$ (V).

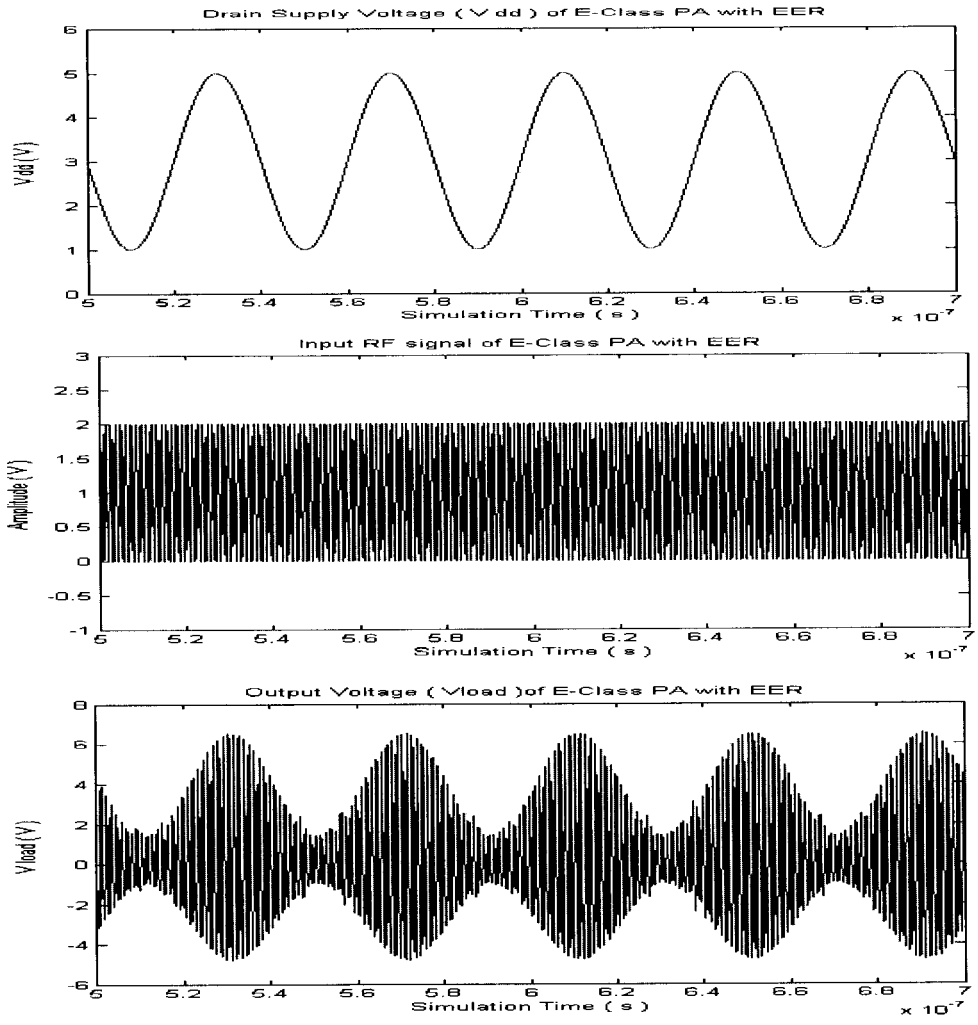

Figure 9 **E-class PA operated in EER mode**
a. Dynamic Drain Voltage Vdd; b. Constant envelope input;
c. PA output

3.2 Phase and Envelope Extraction

After converting the received I/Q samples to envelope and phase, the envelope is further discomposed to high frequency and low frequency components. The low frequency component of the envelope drives the DC-DC converter. And the high frequency component is amplified by an A/B-class amplifier. The outputs are mixed and applied to the E-class PA power supply.

The basic concept of EER architecture has been introduced in section 2.3. The received signal can be split into phase and envelope, and the RF phase-modulated (high frequency RF signal modulated by the phase path) signal, while passing through the E-class PA, is modulated again by the envelope component. Hence, we need to pre-treat the input signal once it is received. Here the input is a complex signal consisting of I (in-phase) and Q(quadrature-phase) The digital processor (FPGA) converts each I/Q sample into envelope and phase samples. The envelope signal is converted back into analog domain using a Digital-to-Analog Converter (DAC) The digital phase data drives a digital phase-shifter. The number of bits determines the quantization error. It has been shown that to maintain an acceptable signal-to-noise ratio at the transmitter, 12-bit is adequate for envelope and 5-bit for phase signal [1]. For this project, a WCDMA waveform with a 10x over sampling of 38.4MHz is used. Figure 10 shows the envelope path and phase path corresponding to the input I/Q sample of the first 1000 samples after processing.

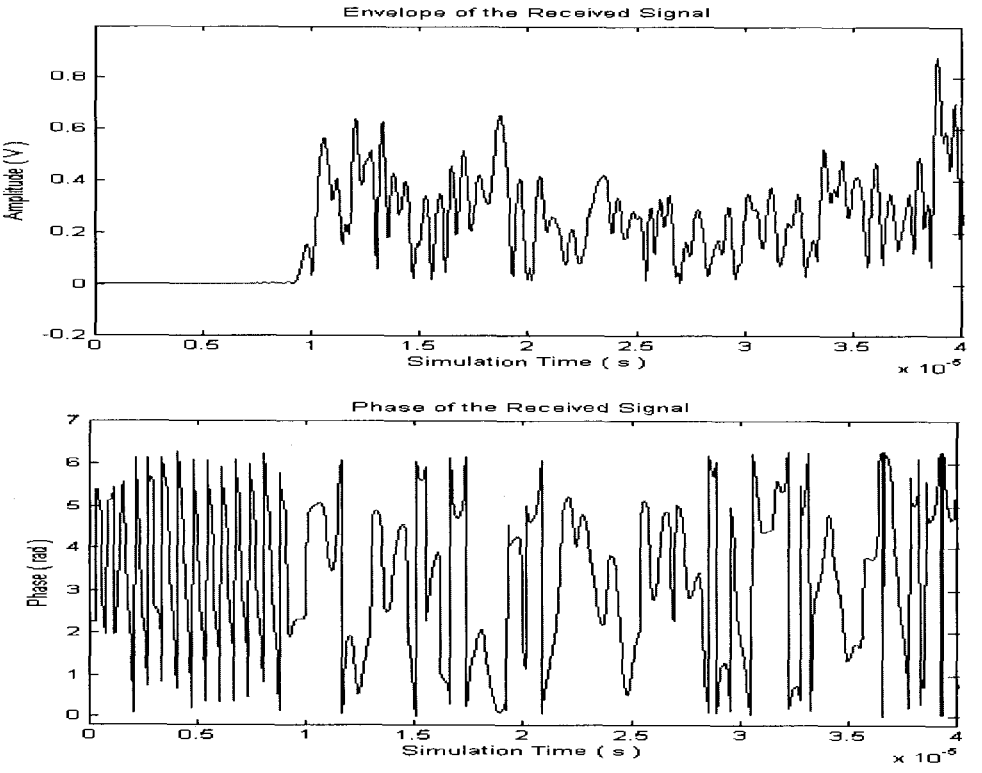

Figure 10 The Envelope and Phase of the Received Signal

The FPGA based digital controller processes the envelope and the phase of the sample input separately, and outputs 12-bit and 5-bit long discrete bit sequence. For the phase, the angle of each sample is mapped from $0 \sim 2\pi$ to $0 \sim 31$, which gives a phase resolution of $\pi/16$. The angle is rounded to the closest integer, then converted to a 5-bit binary sample and stored in the processor.

For example, $0.7356 \rightarrow 0.7356/\pi * 31 \rightarrow 7.2586 \rightarrow 7 \rightarrow 00111$.

The envelope is dealt with in the same way. The only difference is thatthe processor scales the envelope based on the peak power of the received signal, and then scales each sample to 0 ~ 4095 (2^12-1). If the peak power of the received signal is 1 (111111111111), we have

0.7235 → 0.7235*4095 → 2962.7235 → 2963 → 101110010011.

3.3 Regeneration of the Phase and Envelope Sample Sequences

The 5-bit phase and 12-bit envelope sample sequences are sent to the DAC and Phase-Shifter separately. The outputs of DAC and phase-shifter are inputs to the E-class PA. The envelope and phase restoration can be considered as a reverse process of the extraction.

The phase-shifter (shown in Figure. 11) has two inputs. One is the 5-bit phase sample, and the other is the RF signal with carrier frequency and unit amplitude. The phase-shifter first calculates the phase offset for the RF signal in each sample period, and then shifts the RF phase based on the calculated result. The relation between the sample phase code and the phase-shifter is provided in Table. 1.

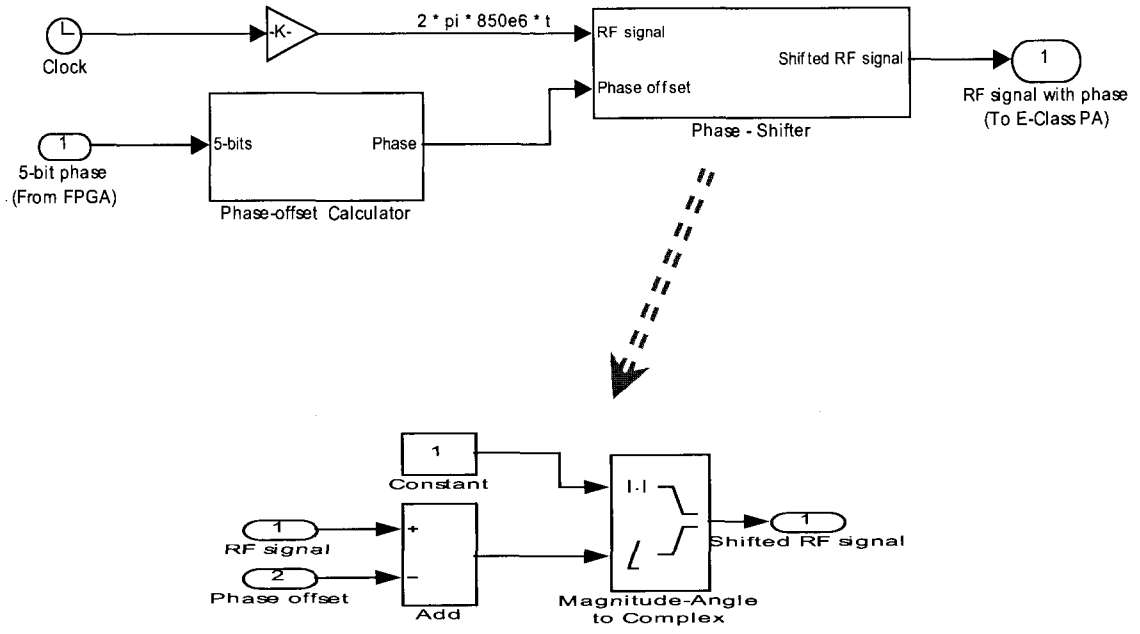

Figure 11 Block Diagram of Phase-Shifter

Table 1 The Relationship of the Coded Phase Sample with the Pin-Input Phase Shifter

Relative Phase(degree)	5-bit code	Shift -180' with input	Shift -90' with input	Shift -45' with input	Shift -22.5' with input	Shift -11.25' with input
0	00000	0	0	0	0	0
11.25	00001	0	0	0	0	1
22.5	00010	0	0	0	1	0
33.75	00011	0	0	0	1	1
45	00100	0	0	1	0	0
56.25	00101	0	0	1	0	1
67.5	00110	0	0	1	1	0
78.75	00111	0	0	1	1	1
90	01000	0	1	0	0	0
101.25	01001	0	1	0	0	1
112.5	01010	0	1	0	1	0

Relative Phase(degree)	5-bit code	Shift -180' with input	Shift -90' with input	Shift -45' with input	Shift -22.5' with input	Shift -11.25' with input
123.75	01011	0	1	0	1	1
135	01100	0	1	1	0	0
146.25	01101	0	1	1	0	1
157.5	01110	0	1	1	1	0
168..75	01111	0	1	1	1	1
180	10000	1	0	0	0	0
191.25	10001	1	0	0	0	1
202.5	10010	1	0	0	1	0
213.75	10011	1	0	0	1	1
225	10100	1	0	1	0	0
236.25	10101	1	0	1	0	1
247.5	10110	1	0	1	1	0
258.75	10111	1	0	1	1	1
270	11000	1	1	0	0	0
281.25	11001	1	1	0	0	1
292.5	11010	1	1	0	1	0
303.75	11011	1	1	0	1	1
315	11100	1	1	1	0	0
326.25	11101	1	1	1	0	1
337.5	11110	1	1	1	1	0
348.75	11111	1	1	1	1	1

Through offsetting the phase of the RF signal with an assigned angle in each sample period, a phase-modulated RF signal is obtained. The simulation results of the phase offset (see Figure 12) show that it is in the same phase as the input signal (see Figure 10).

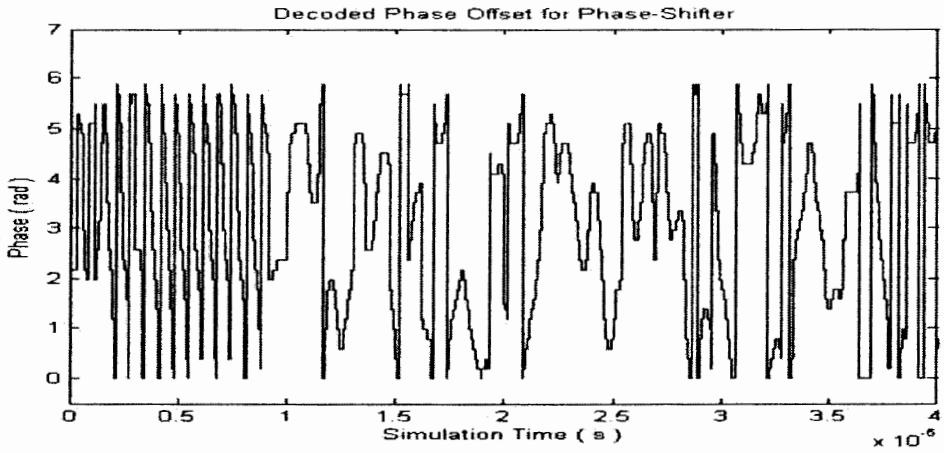

Figure 12 Phase Offset after Decoding the 5-bit Phase Sequence

The jump of the phase between the two sample periods can be found in Figure 13.

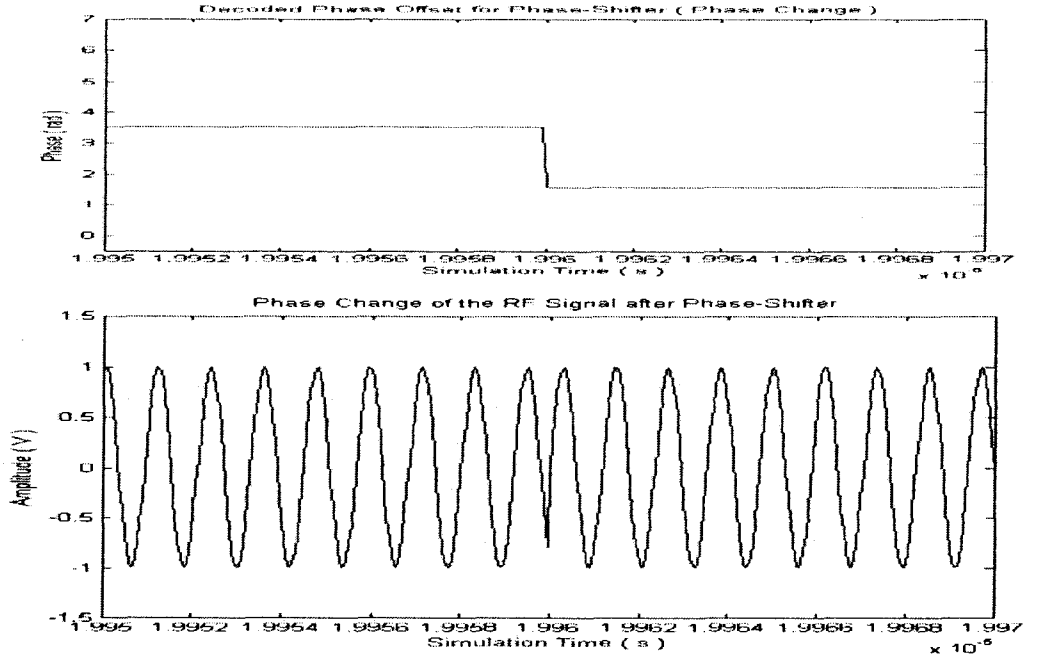

Figure 13 **Phase-Modulated RF Signal:**

a. Phase Change of the 5-bit sample;

b. Phase Jumping of the RF signal

In the envelope restoration path, the 12-bit envelope signal is fed into the DAC and a low-pass filter which convert it back to an analog envelope. The process diagram (Figure 14) and simulation results (Figure 15) are provided.

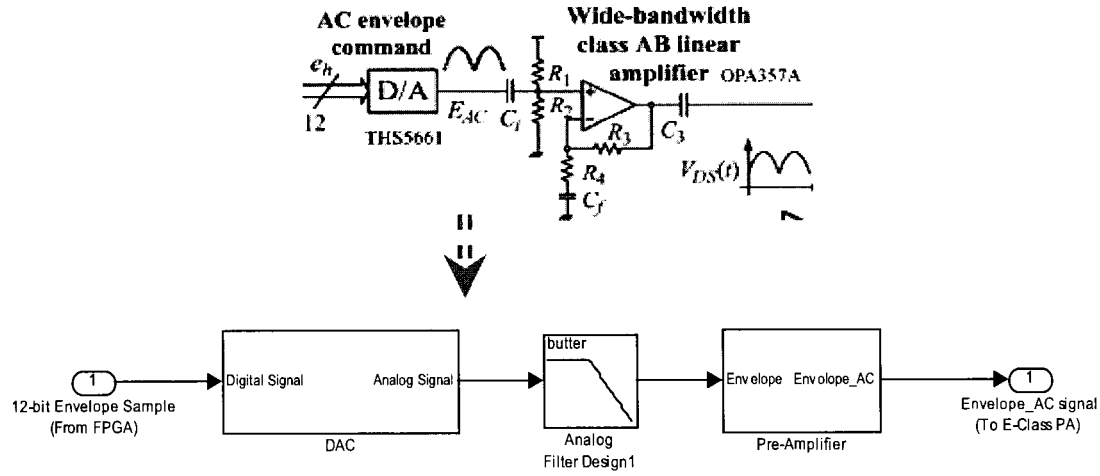

Figure 14 Decoding Process of 12-bit Envelope Sequence

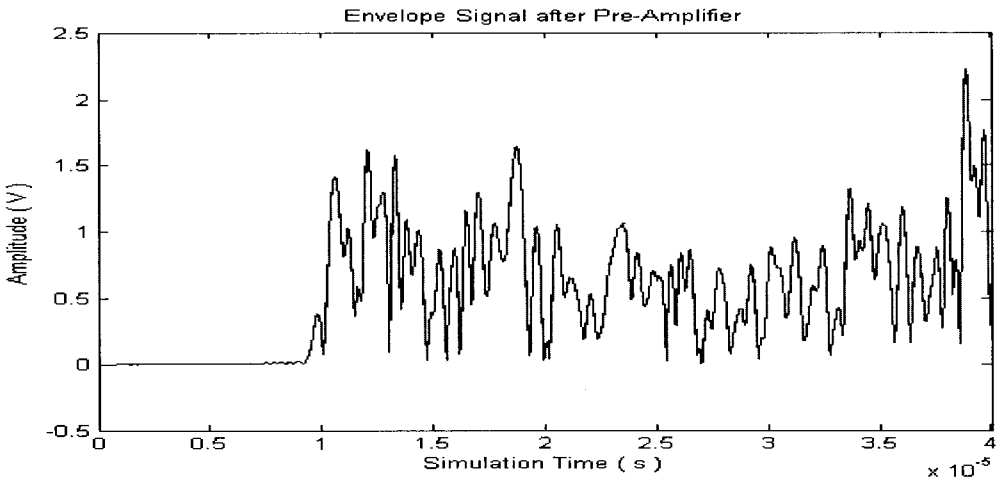

Figure 15 Decoding of 12-bit Envelope Sequence

On amplification by a linear Power-Amplifier, the digital signal is transformed into an AC power driving signal with the same envelope shape as the input sample signal.

3.4 Implementation of the E-Class PA with EER Operation Architecture

The E-class PA with EER architecture is implemented following the diagram as shown in Figure 16. For the drain voltage of the E-class PA, the envelope signal is used as drain voltage supply for modulation, which is already pre-amplified to provide the basic power amplification ability. The envelope signal is an AC voltage with an envelope modulation function. The input signal of the E-class PA is the phase-modulated RF signal from the phase-shifter.

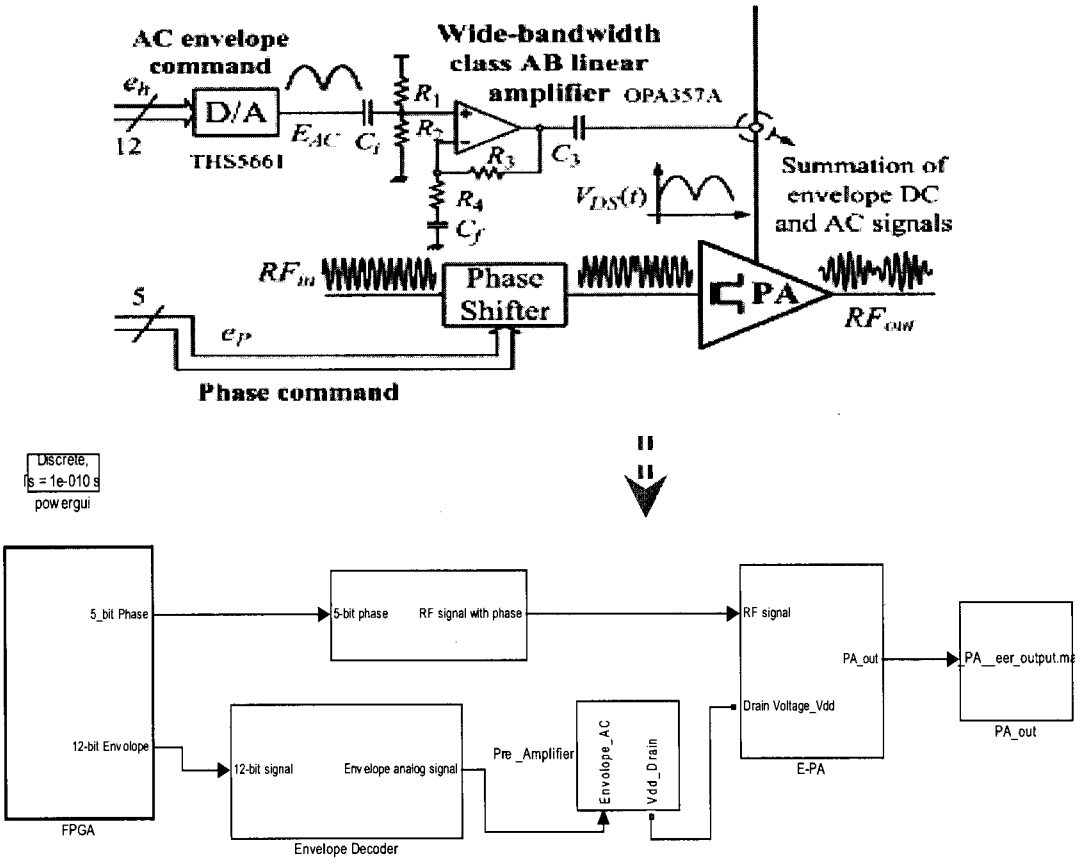

Figure 16 System Implement Diagram of RFPA with EER Architecture

The simulation results are shown in the Figure. 17. On comparing the simulation results with the received signal (Figure 15 for envelope modulation, and Figure 13 for phase modulation), it is observed that the EER operation architecture improves the linearity of the PA.

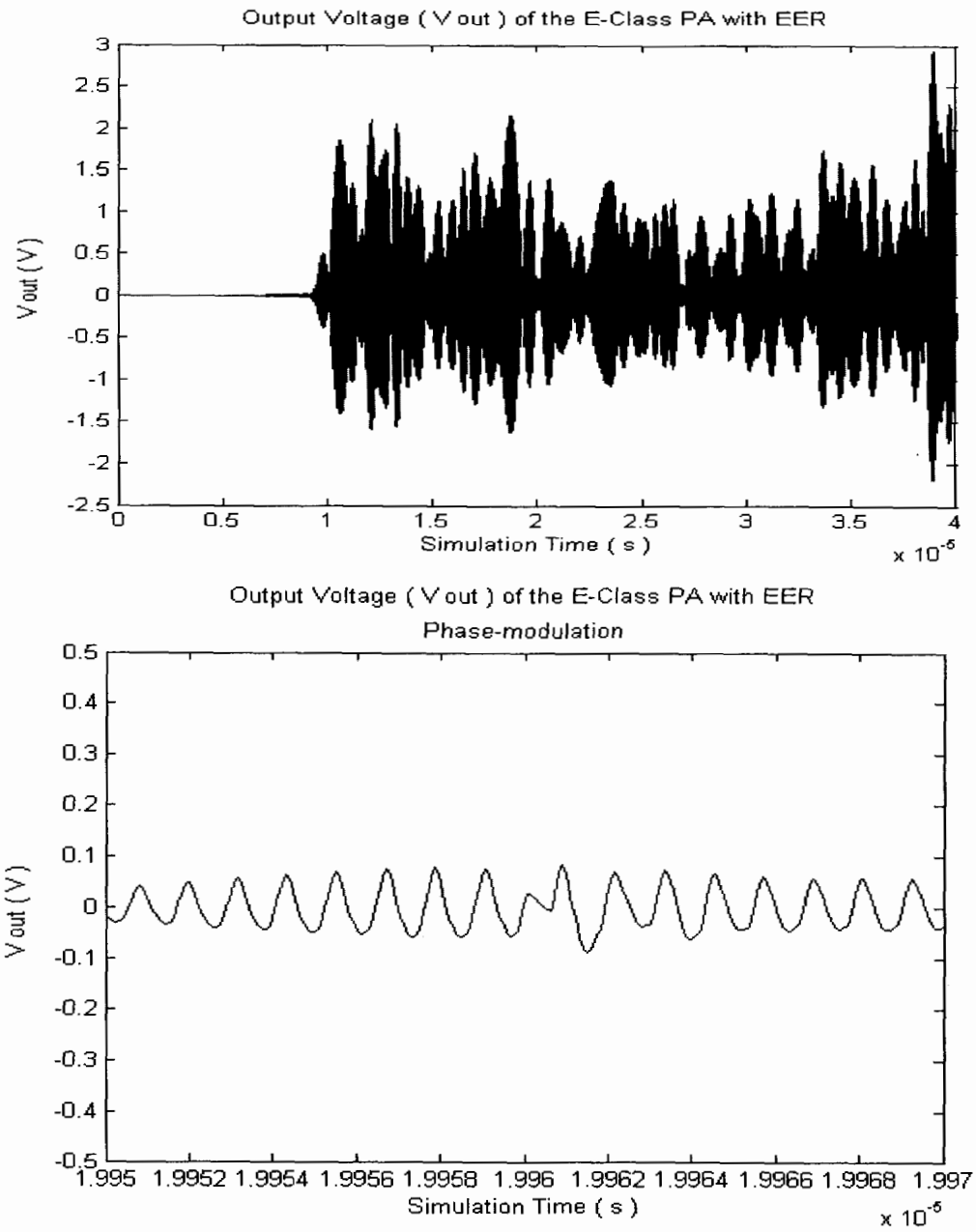

Figure 17 **Output RF Signal after EER E-class PA:**

a. Output of the E-PA with EER

b. Observation of the phase jump

4. SIMULATION OF DIGITALLY CONTROLLED DC-DC CONVERTER

As discussed in Chapter 2, the system requires the DC-DC converter working in a steady-state to provide a tight-regulated output voltage when in high load working mode (CCM mode), and turning to power-saving state when in light load working mode (DCM mode). To achieve the goal of regulating and adjusting the output of the converter, a dynamic process is used to supervise and control its working status.

The experimental block diagram (Figure 18) shown below demonstrates a power management scheme with multiple operation modes [2].

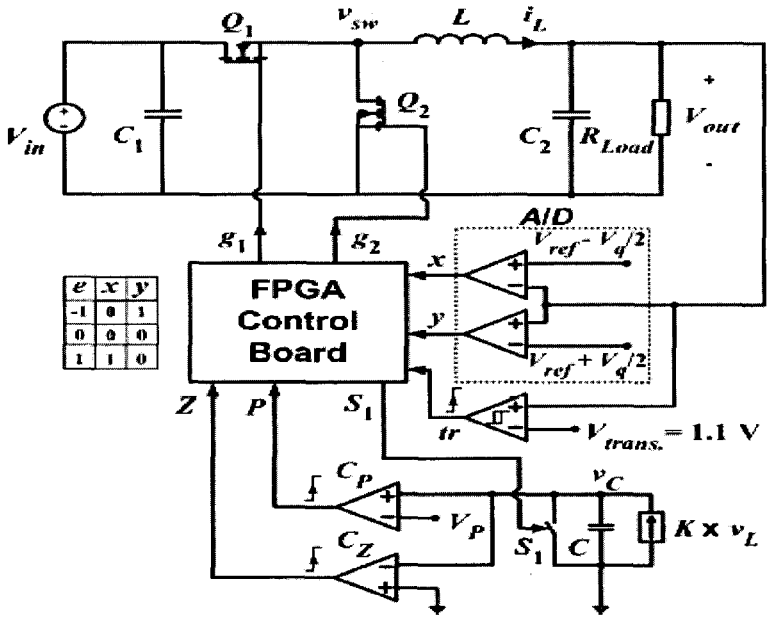

Figure 18 System diagram of Digitally Controlled DC-DC Converter

The system contains three parts. The first part is a basic switch-mode Buck DC-DC converter which was introduced in section 2. The second one is a Signal-Generation component which collects samples from the output of the DC-DC converter (or the entire system) and generates error signals in CCM mode and control signals in DCM mode. The working mode transition signal is created here as well. The final component is a FPGA based microprocessor which manages the converter's working status by adjusting the duty of each switching control pulse for the DC-DC converter according to the input error signals, or adjusting the interval between two switching cycles (Frequency Adjustment) based on the charge-discharge circuit and current calculated in the converter'sin ductor. We use a constant load resistance replacing the RF-PA. The following figure (Figure 19)

shows the entire system-level block diagram of the digitally controlled DC-DC converter as implemented in Simulink.

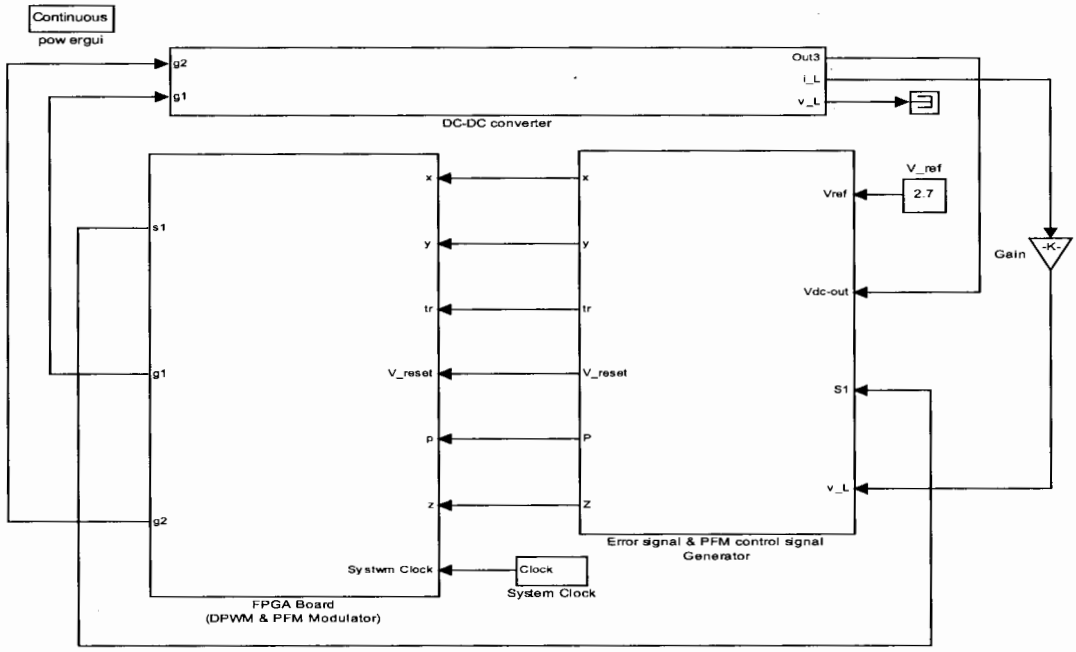

Figure 19 Implementation Diagram of Digitally Controlled DC-DC Converter

Based on the basic Buck DC-DC Converter diagram shown in Figure 4, we created a module as shown in Figure 20.

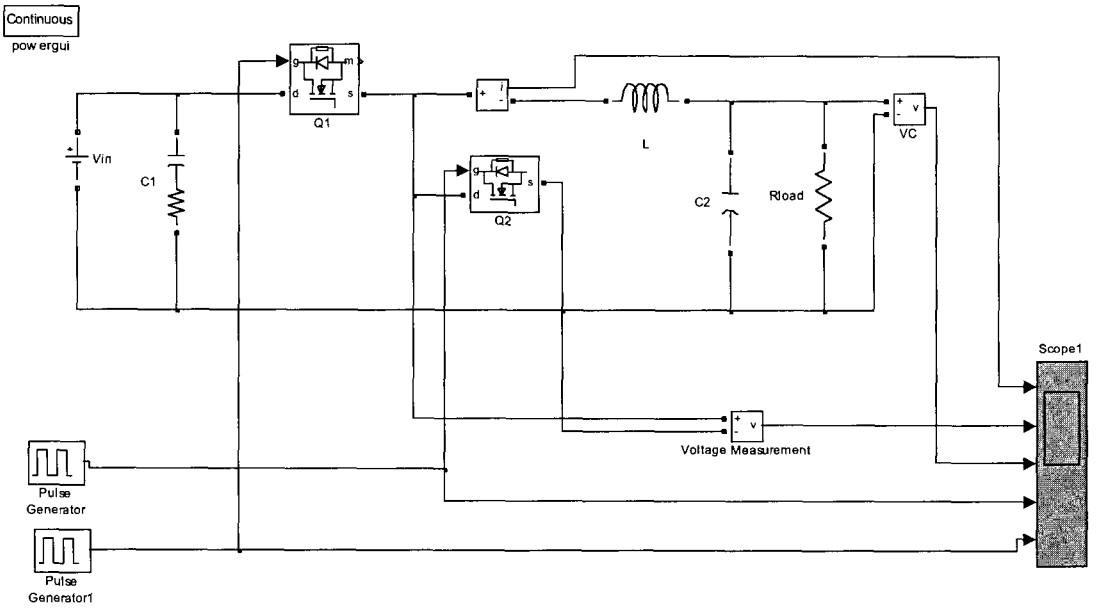

Figure 20 Block Diagram of DC-DC Converter

The simulation is processed based on the CCM mode with V_{in} = 5V, L = 10 uH and C_2 = 10 uF. The switching pulses we used at 1MHz are 50%-50% and 70%-30% fixed duties in each switching pulse respectively.

It can be seen that the converter reaches the steady state after about 1ms (this value varies with loop bandwidth). The final output voltage depends on the duty cycle of two switch-control pulses. Figure 21 presents the comparison of two duty-cycles with different voltage outputs. As the duty-cycle becomes large, the output voltage increases.

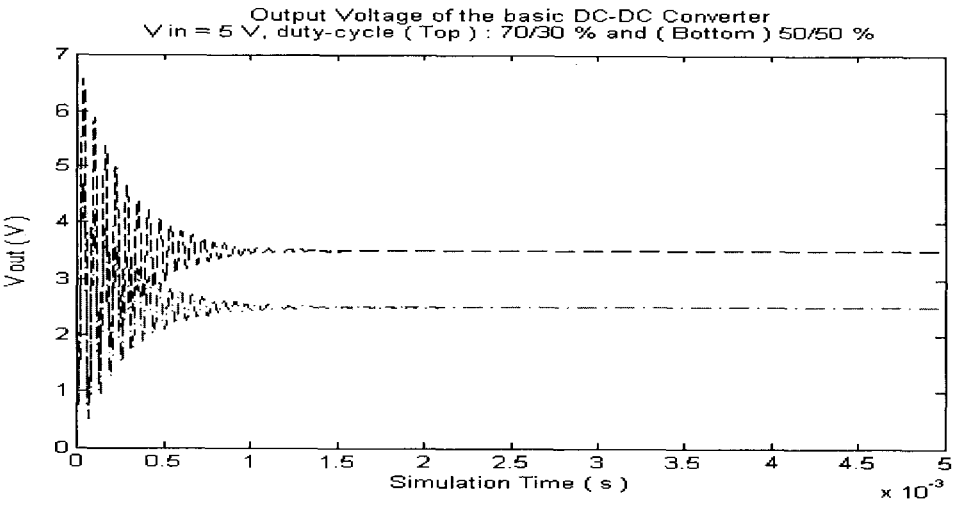

Figure 21 Voltage Output of DC-DC Converter with no control

4.1 CCM WORKING MODE

This section examines in detail the Simulink implementation and results of the digital control process in CCM working mode (Figure 22).

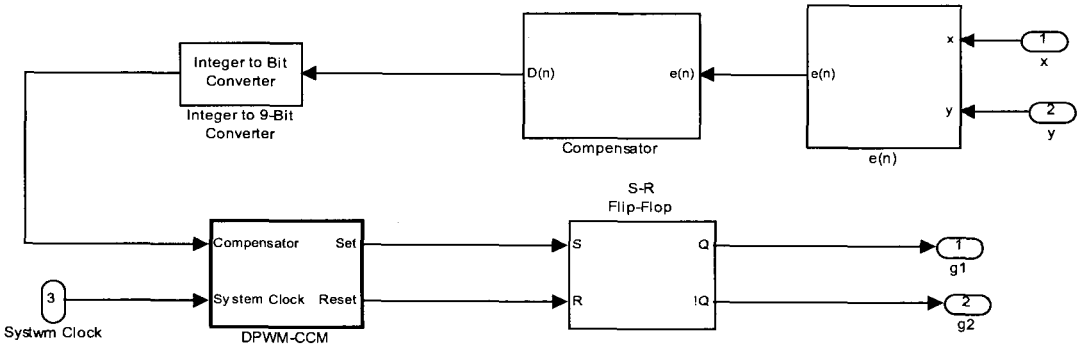

Figure 22 Diagram of Digital Controller for CCM mode (inside FPGA)

4.1.1 AD Converter and Error Signal e(n) Generation

An Analog- to-Digital Converter (ADC) senses and tracks the output voltage signal of the DC-DC converter V_{out} (Shown in Figure 23). When both the output voltage V_{out} and reference voltage V_{ref} are above the threshold V_{tr}, the digital controller works in the CCM mode. For this case, the threshold is set at 1.1V.

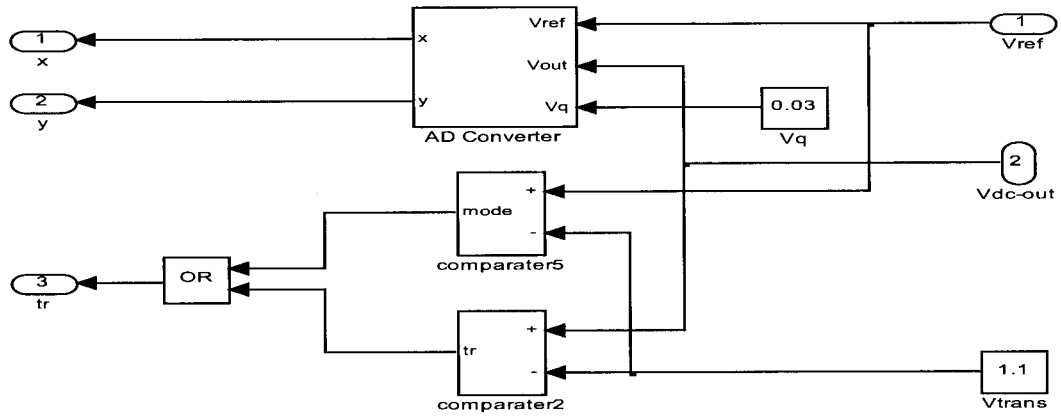

Figure 23 Diagram of Digital-Analog Converter (DAC)

The ADC samples of V_{out} are compared with the reference voltage (V_{ref}) and the digital error signal e(n) is generated. In general, the sensed voltage (V_{sense}) is a scaled version of the output of DC-DC converter, i.e. $V_{sense} = K*V_{out}$. K is assumed to be unity. For the error signal e(n), n is the index of the sample sequence, and is based on the duration T_s of each switching cycle of DC-DC converter. The V_{out} is sampled once in each switching period T_s. The 3-value ADC is built using just two comparators. Since the output voltage V_{out} should be regulated around the reference V_{ref}. If the regulation window size

is set to Vq centered at Vref, Vout should compare with Vref – Vq/2 and Vref + Vq/2 respectively. The output error has 3 discrete values as shown in Figure 24.

e(n)	x	Y
-1	0	1
0	0	0
1	1	0

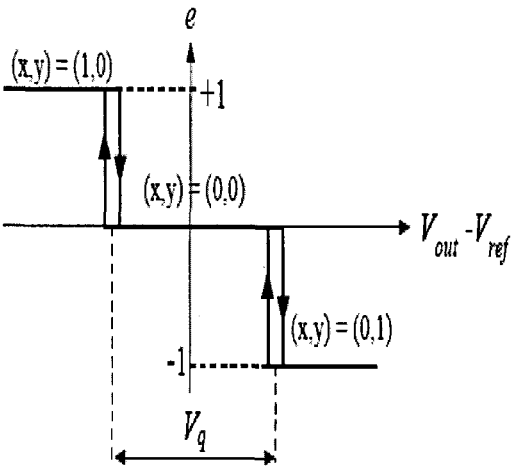

Figure 24 Concept of Error Signal Generation

The output error e(n) =0 implies that the DC-DC output Vout is inside the regulation window, and stays in the steady-state. The error +1 or -1 indicates that the Vout is above or below the window. Since the regulation system requires the output Vout to be close in value to the reference Vref, the static and dynamic voltage regulation capabilities depend on the characteristics of the DAC.

4.1.2 PID compensator implementation and its look-up table design

As explained in the background analysis in section 2.5 [8], [9], a digital compensator module can be designed based on the PID controlling scheme which is shown in Figure 25.

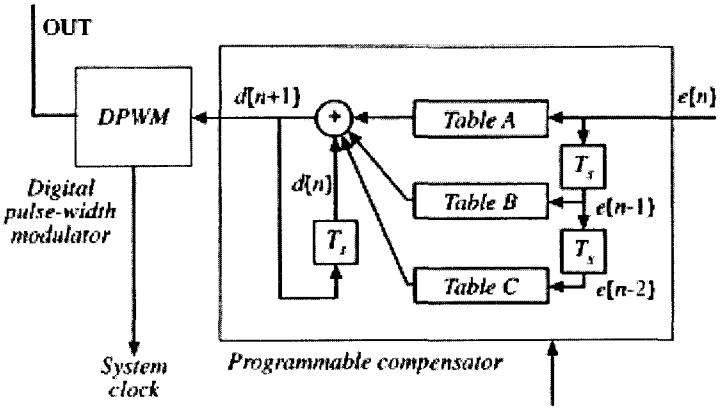

Figure 25 Concept of PID Compensator

A look-up table for the cycle correction command of the digital compensator can be created as well. The table entries are 9-bit values, giving e(n) with three error signal levels, -1, 0 and 1, and its two delay errors, e[n-1] and e[n-2]. There are a total of 27 possible values for the duty cycle correction command $d_c(n)$. Due to the first sign bit, the 8 bits of correction values are calculated based on the formula (4) to (6). After scaling by 256 (2^8, 8 bits except the sign bit), the values are round off to the closest integer in order to fit in the 9-bit entries. The values for the 9-bit compensator entry are presented in Table 2. It can be seen thatthe table is symmetr ical about the centre (index 14). Furthermore, for the indices 3, 7-8, and 12, since the corresponding error sequence ('-1 to 1' or '1 to -1' which crosses the reference window directly) would never occur during the transient sample period, the

values are forced to zero instead of being computed from the formula. It is the same for the indices 16, 19-21 and 25. The implementation diagram is shown in Figure 26.

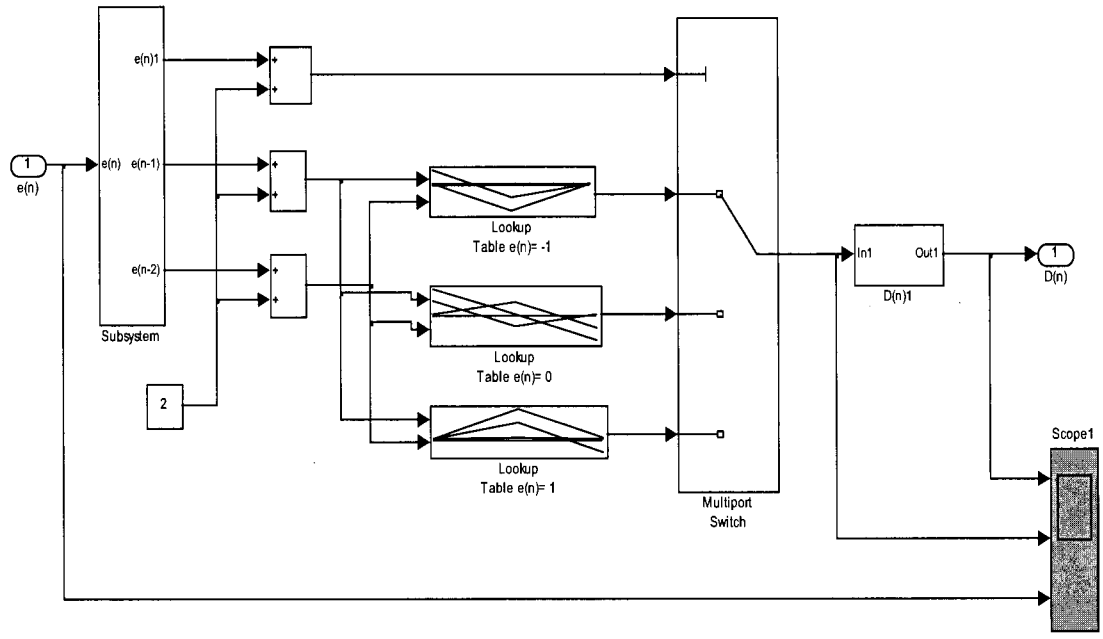

Figure 26 Implementation Diagram of PID Compensator

Table 2 9-bit Compensator Entry for Digital PID Compensator

Table index	e(n)	e(n-1)	e(n-2)	dc(n) *256 with sign (resolution=512)	9-bit duty-correction with sign
1	-1	-1	-1	-0.3738	-1
2	-1	-1	0	70.6253	71
3	-1	-1	1	141.6243	0
4	-1	0	-1	-145.7485	-146
5	-1	0	0	-74.7494	-75

Table index	e(n)	e(n-1)	e(n-2)	dc(n) *256 with sign (resolution=512)	9-bit duty-correction with sign
6	-1	0	1	-3.7504	-4
7	-1	1	-1	-291.1232	0
8	-1	1	0	-220.1242	0
9	-1	1	1	-149.1251	0
10	0	-1	-1	74.3757	74
11	0	-1	0	145.3747	145
12	0	-1	1	216.3738	0
13	0	0	-1	-70.9990	-71
14	0	0	0	0	0
15	0	0	1	70.9990	71
16	0	1	-1	-216.3738	0
17	0	1	0	-145.3747	-145
18	0	1	1	-74.3757	-74
19	1	-1	-1	149.1251	0
20	1	-1	0	220.1242	0
21	1	-1	1	291.1232	0
22	1	0	-1	3.7504	4
23	1	0	0	74.7494	75
24	1	0	1	145.7485	146
25	1	1	-1	-141.6243	0
26	1	1	0	-70.6253	-71
27	1	1	1	0.3738	1

4.1.3. Implementation of Digital Pulse-Wide-Modulator

The key aspect for the digitally controlled DC DC converter is to transfer the duty cycle correction d(n) from the given error signals with 3 possible values and their 27 possibilities to a set of the discrete duty ratios. As shown in Figure 27, a regulator of 9-bit resolution is used to obtain a scheme to transfer the digital input (from 1 to 511, decimally) to the duty ratio from 0.2% to 99.8% proportionally. The Digital Pulse-Width-Modulator (DPWM) can be structured by using fast-clocked counters and digital comparators, which work in high frequency environment.

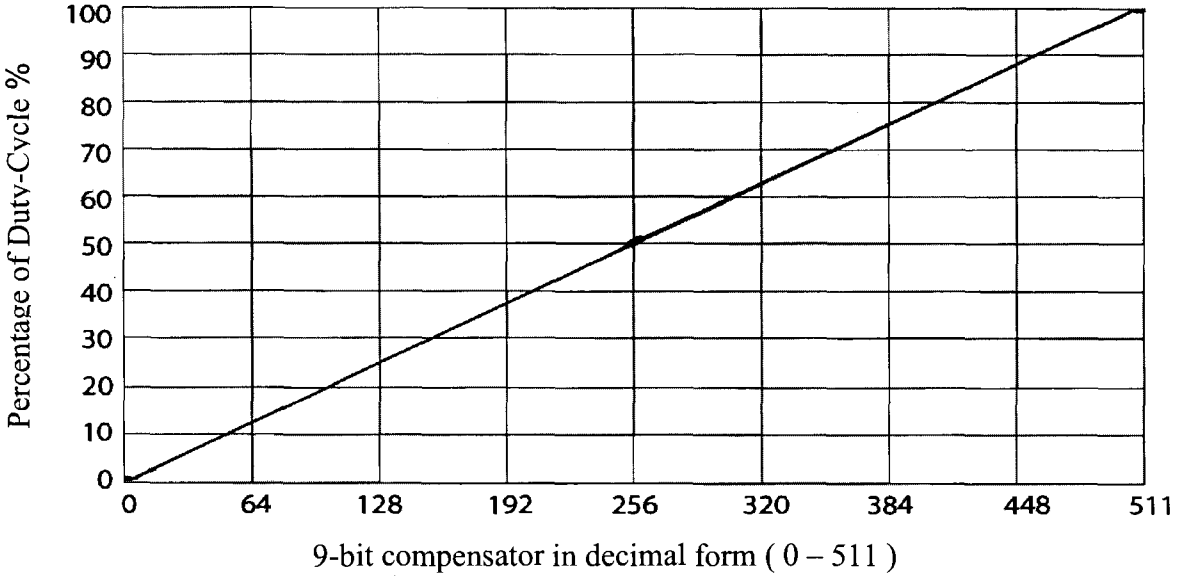

Figure 27 Relationship between the 9-bit compensator and the duty-cycle of the switching control pulses

To achieve n-bit resolution DPWM that can provide waveforms at frequency fs, the required system clock for the DPWM is 2^n * fs [8]. This means that a 512 MHz clock

frequency is needed to get the 9-bit resolution, thus resulting in tighter timing constraints and higher power consumption.

The tapped delay-line scheme can achieve the function of fine time resolution with lower system frequency. This scheme contains a ring of fixed-time delay units to form a ring oscillator and a counter, and works at the required switching frequency. However, this needs a large number of delay units and a multiplexer for function implementation.

If N-bit resolution is required, a N_c-bit counter ($N_c < N$) is used for the higher N_c bits of the N-bit resolution, and another N_d-bit ($N_d = N - N_c$) fixed-time delay ring is deployed to obtain the resolution for the remaining lower N_d bits. Since the delay ring splits the system clock T_s into N_d (decimal) parts and therefore increases to some extent the working frequency to $2^{N_d} * f_s$, the DPWM can work only at the frequency of $2^{N_c} * f_s$.

Here, a 4-bit DPWM is presented for example. We assume that f_s is 1MHz, and we use a 4-bit DPWM to get a 0 – 15 duty cycle resolution. The scheme consists of a 2-bit counter (N_c=2) and a 2-bit ring-oscillator which has four resettable flip-flops as delay units (N_d=2). Only f_{sys}=4 MHz ($2^{N_c} * f_s$) serves as a system clock, not 16 MHz anymore. The scheme achieves the target of reducing the clock frequency. Additionally, one counter, two comparators and a couple of logical gates give the function a whole resolution counting and produce the duty of the control signal from the input d(n), based on the percentage of the resolution from the PID regulator. Figure 28 depicts a simplified 4-bit resolution DPWM to show the working of the scheme.

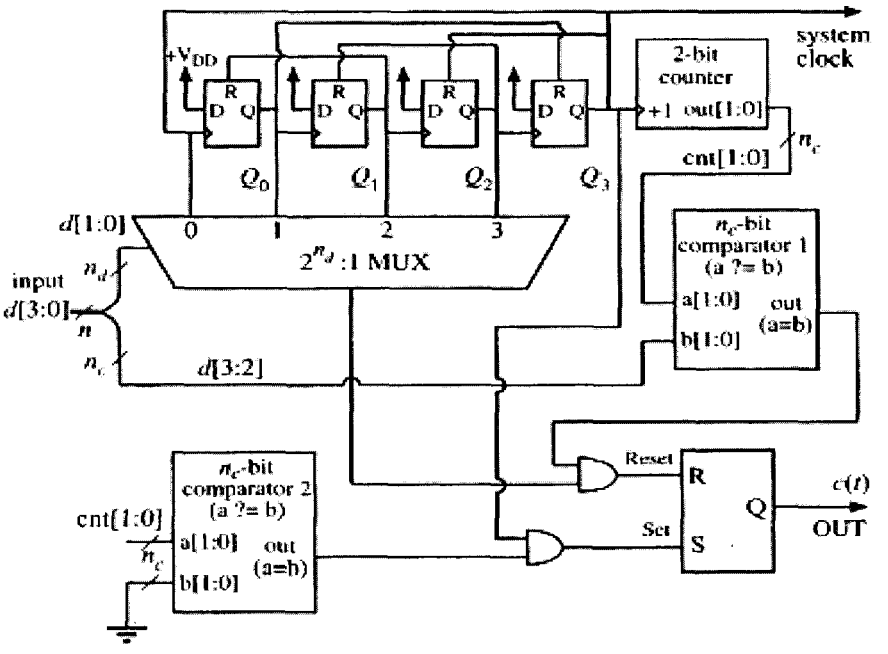

Figure 28 Scheme of Generating the DPWM Pulse Signal

It can be seen that the resettable delay ring splits the system clock into 4 continuous pulses with equal pulse width. In split pulse, it counts from 0 to 3 (2^Nd -1), and outputs to Q0 – Q3. The last split pulse (still working at f_{sys} = 4 MHz) is sent to the Nc-bit counter to complete a counting cycle in each 4 system clock cycles.

An S-R flip-flop is used for the control signal creation. At every assigned sampling point, we sample the outputs of the each delay-unit, convert them to a Nd-bit signal, and then compare it with the lower Nd-bit part of the d(n). At the same time, the output of the Nc-Bit counter is also compared with the higher Nc-bit of the d(n).

At the beginning of the switching time cycle, the output of the S-R flip-flop is set by checking the time when the counter is 0 and the last delay-unit is 0. The switching

pulse-cycle is then set to high. When the counter matches the upper two bits, N_c, and the delay ring matches the two lower bits, N_d, a true input value is sent to the Reset-Pin of the S-R flip-flop. This implies that the duty ratio of the switching control pulse has been matched with the duty correction command d(n), and then the switching pulse-cycle is reset to 0. Atthe next set-signal, which occurs every 4 system clock-cycles, the switching pulse-cycle is set to high again. Then a switching clock-cycle is completed at $f_s = 1$ MHz. This process can be examined in Figure 29.

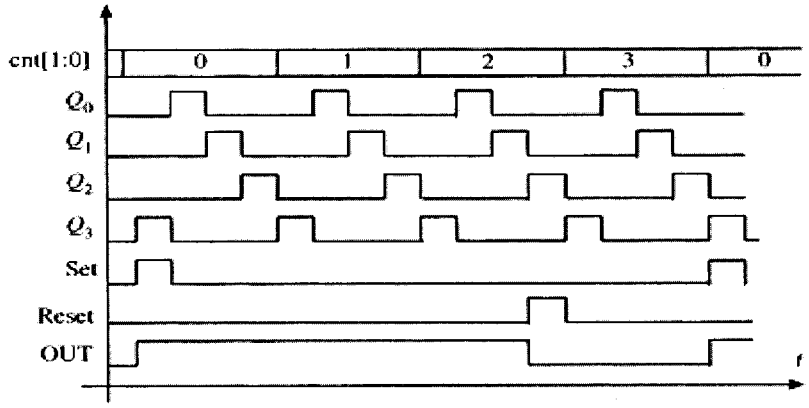

Figure 29 Waveforms of the DPWM Signals

A resettable 1-bit counter and a delay-unit are used to build a fixed-time delay unit in our simulation. 16 delay units set up a ring delay line to achieve the functionality of a ring oscillator and obtain the output waveform as required. The switching control pulses G1 and G2 need to be at the frequency f_s=1 MHz, and a 9-bit resolution DPWM is used (N = 9, 512 in decimal) in this project. The 9-bit regulation input d(n) and the DPWM are split into two separate sections - a 5-bit higher part (N_c=5) and 4-bit lower part (N_d=4). The

DPWM works at the system frequency of f_{sys}=32 MHz (2^Nc). The following models in Figure 30, 31 and 32 show in detail the implementation approaches thatexpand the approach of a 4-bit resolution DPWM to a 9-bit one.

a. Achievement of the internal 9-bit (512 decimal) (Figure 30)

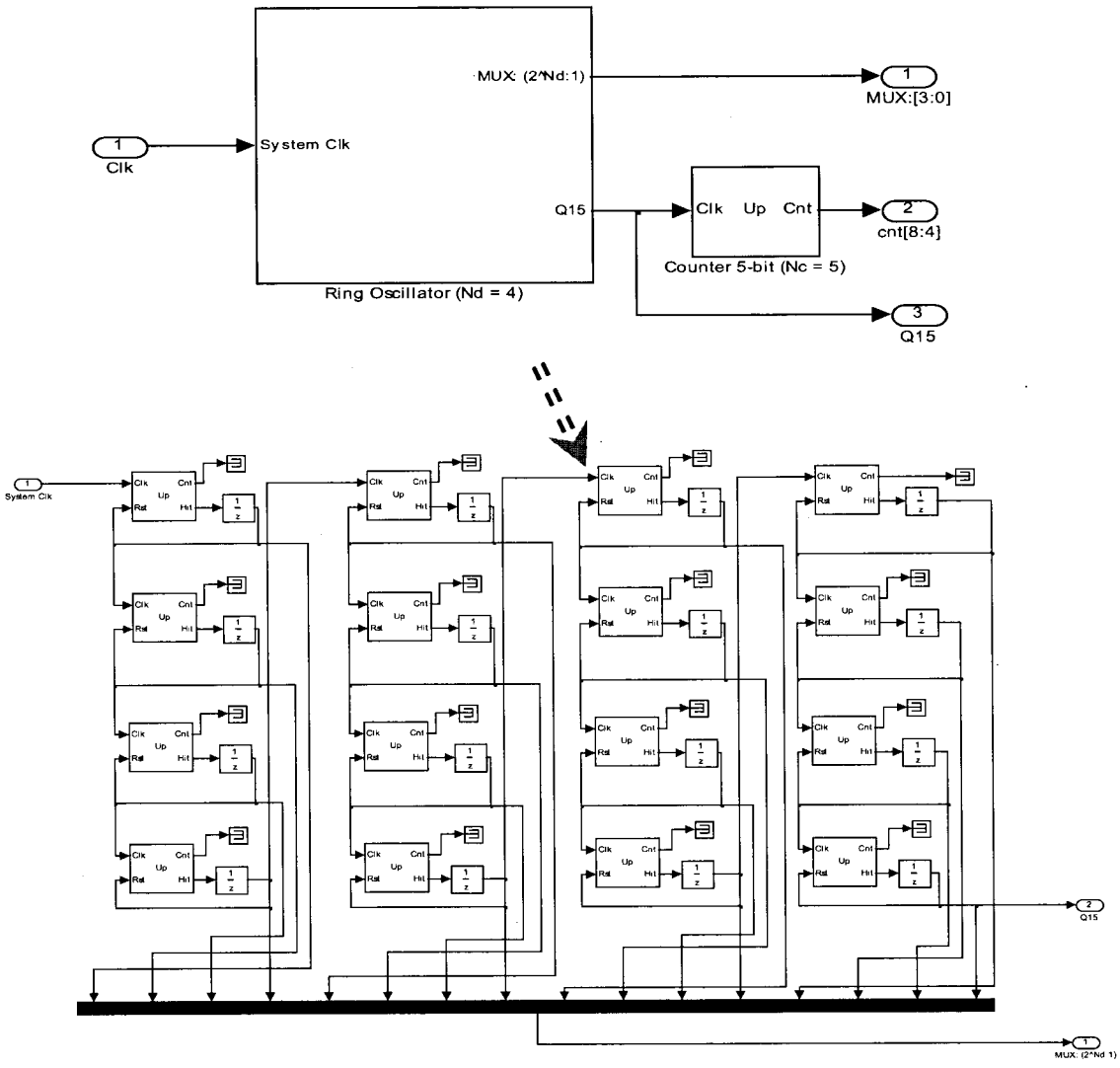

Figure 30 Implementation Structure of 9-bit fixed-time delay unit

b. Generation of two control signals of set and reset for switching pulse duty-ratio control (Figure 31)

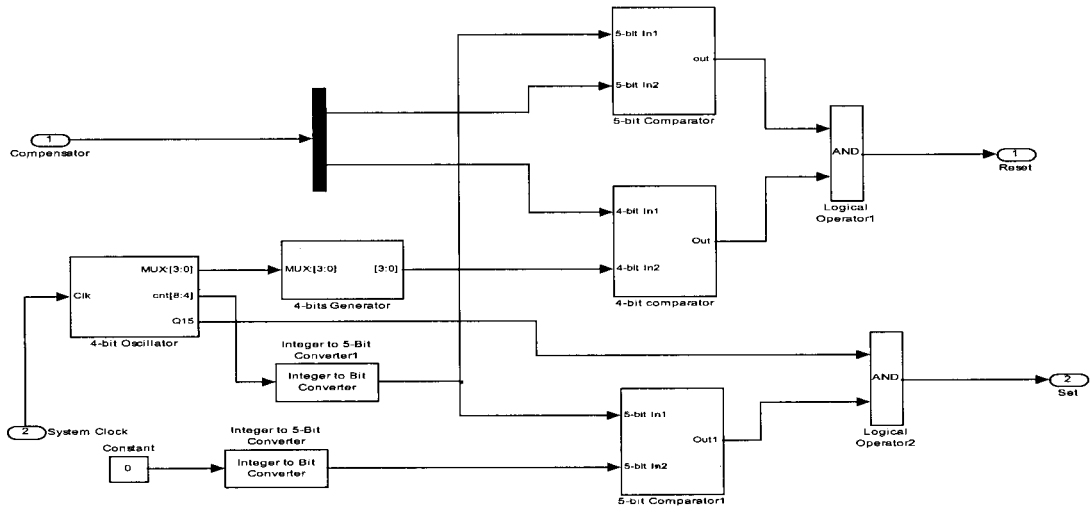

Figure 31 Logic Circuit of the DPWM Control Signal Generation

c. Output signal waveform (Figure 32)

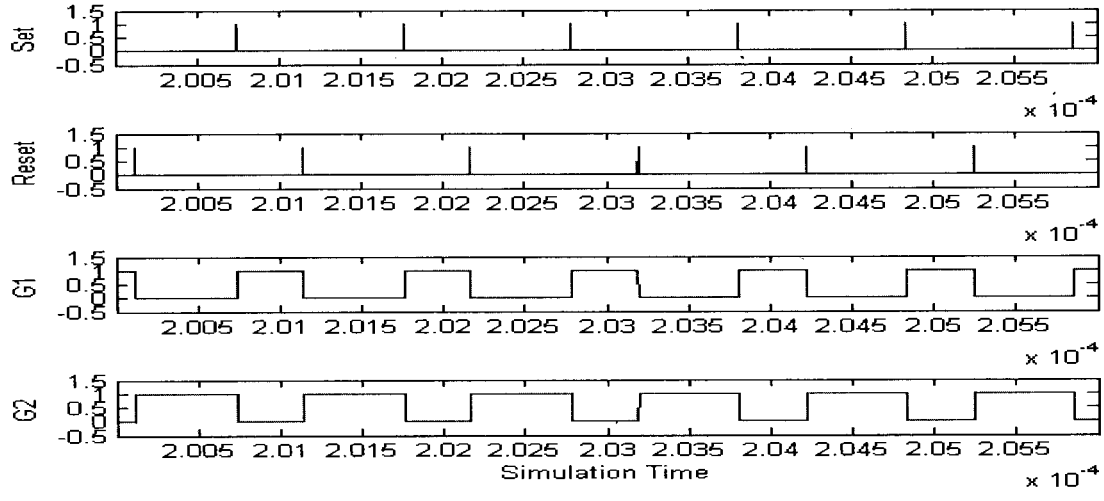

Figure 32 Relationship of the Set-Reset Signals with Switching Pulses

4.1.4 Simulation results for CCM Mode

This section provides the simulation results of the Digital PWM controlled DC-DC converter model thatworks in the continuous conduction mode (CCM).

The input voltage of the DC-DC converter, V_{in}, is set to 5V. Parameters of other components in the converter are: L =10 uH, C_2 =10 uF, load resistance R_{load} is = 50 ohm, and switching pulse frequency f_s = 1 MHz for G1 and G2. The digital control system deploys a 9-bit compensation with reference voltage V_{ref}= 3V, and error window size V_q = 30mV. The following waveform shows V_{out} (Figure 33).

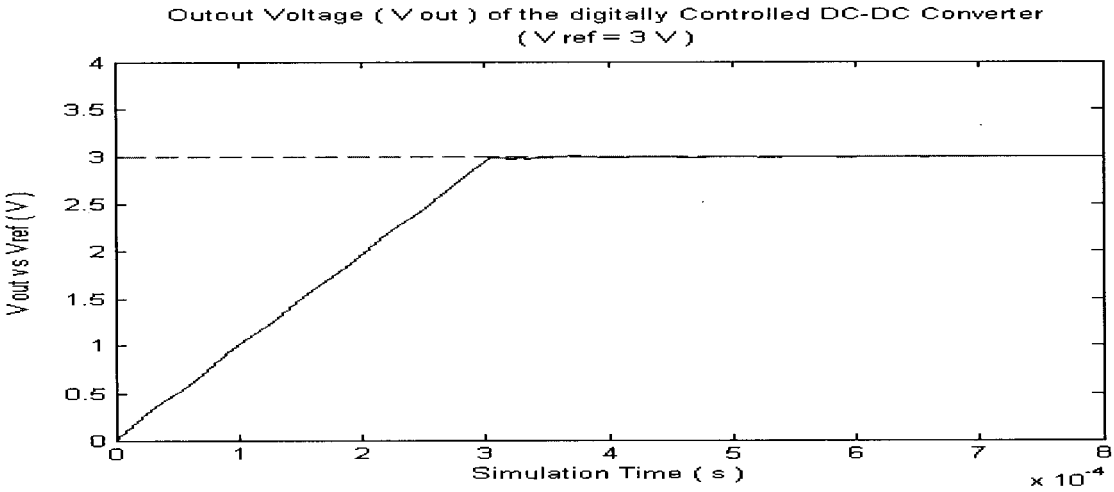

Figure 33 Simulation Result of Digitally Controlled DC-DC Converter in CCM Mode

It can be observed that the system has a soft-start feature, does not oscillate like the system without digital control, and reaches the steady state fast and resolutely. Compared to the results in Figure 21, the digitally controlled DC DC converter takes almost 5 times faster (about 3e-4 s) than the normal converter (about 1.5e-3 s) to reach the steady state. Changes in the error signal e(n), the duty-cycle correction $d_c(n)$ and the duty_cycle ratio

command d(n) give a regulation to the output voltage Vout. The waveforms in Figure 34 show changes in e(n), $d_c(n)$ and d(n) during the whole process. This figure shows the change in error signal and compensator to limit the Vout.

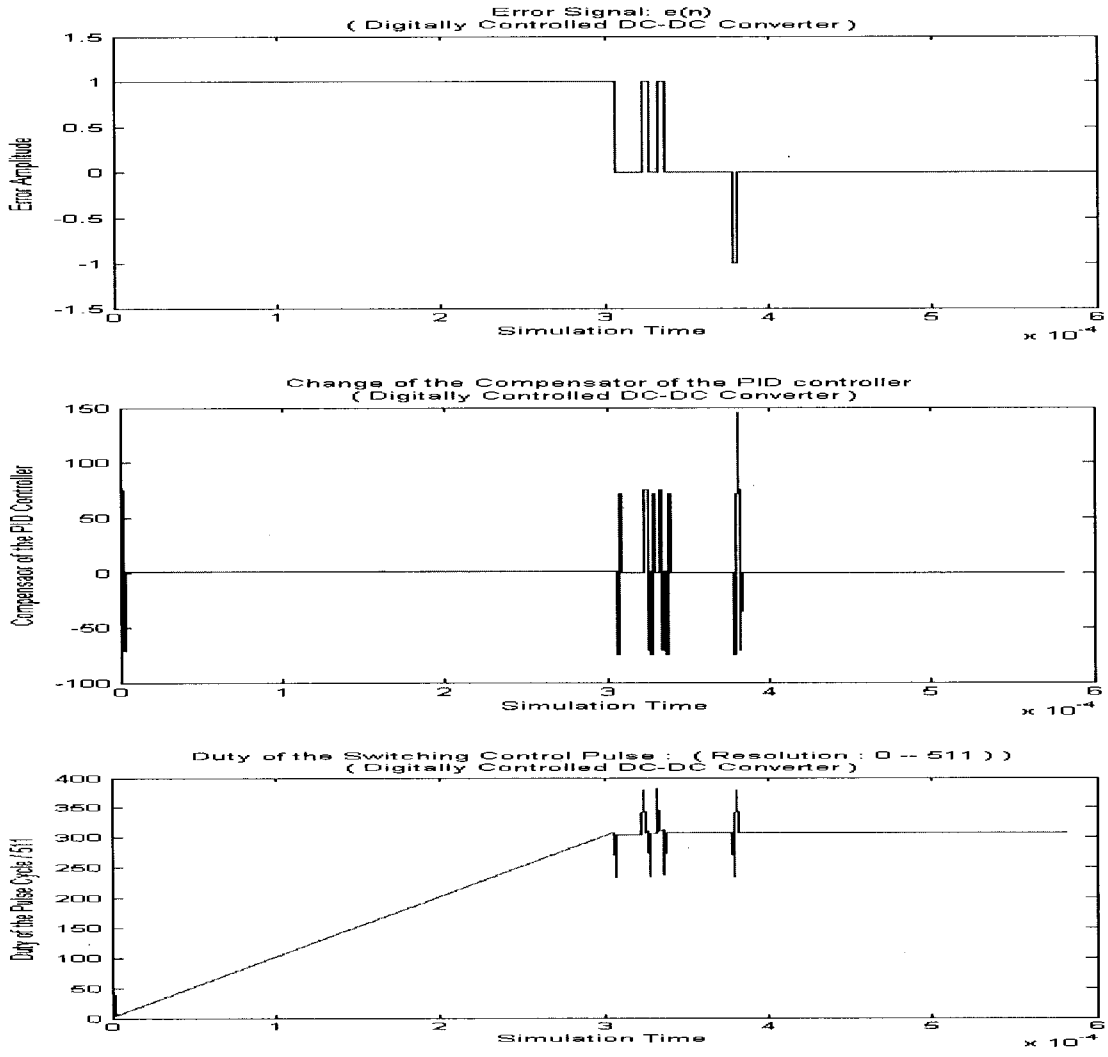

Figure 34 Changes of the Error, PID Compensator and Duty Command Signals

The error voltage between Vout and Vref is quite large at the start-up and the error e(n) = +1. The compensator increases correspondingly by one step in the switching cycle and gradually gets closer to the steady-state value. This process is pretty smooth.

The error voltage gets smaller while V_{out} reaches closer to V_{ref}. After a short oscillation, the output is then limited to being within the V_q range. Even though V_{out} goes over or under the regulation window bond by the charge-discharge inertia, the digitally-controlled system keeps it within the range by detecting the error and changing the duty-cycle ratio.

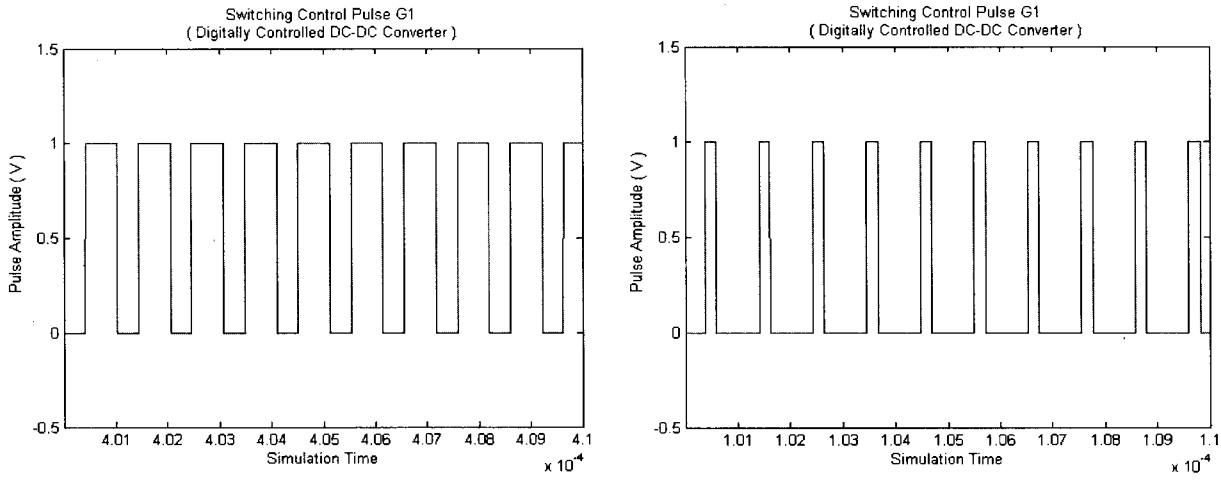

Figure 35 Change of the Duty-cycle in CCM mode

The changes of two switching control pulses can be observed in Figure 35. The DPWM controls two pulses to increase the charge time and reduce the discharge time apart from the simulation time. This control enables the voltage output $V_{out\ to}$ increase following the increase in duty-cycle. Comparing the change in the duty cycles of two switching pulses at different times, it can be seen that the duty cycle increases with the duty command and finally reaches a steady value.

4.2 DCM Operation Mode

Previous research and experiments [2], [6] have shown that the system power efficiency drops significantly when the converter's load becomes light. An analysis of the power consumptions in light-load mode of the converter clearly showsthat the switching loss of the power elements such as MOSFET take the most percentage of the total consumption.

It is proposed to decrease the switching frequency such as the discontinuous current mode (DCM) in order to reduce the power consumption. Pulse Frequency Modulation (PFM) method is a main technique to do so. The peak current of the inductor is regulated to a constant level in DCM mode. By detecting the constant peak current, the digital controller can drive the DC-DC converter to work at a variable frequency, making the current through the inductor discontinuous.

4.2.1 Implementation of DCM-Mode DC/DC Converter

The entire DCM-PFM approach in the digital controller consists of three sub-circuits for this experiment as shown in Figure 36. When the output voltage of the DC-DC Converter, V_{dc_out}, drops below the transition level V_{tr}, the switch turns the digital controller to DCM mode, and the switching control pulses are generated by the PFM module. The PFM module is shown in Figure 36.

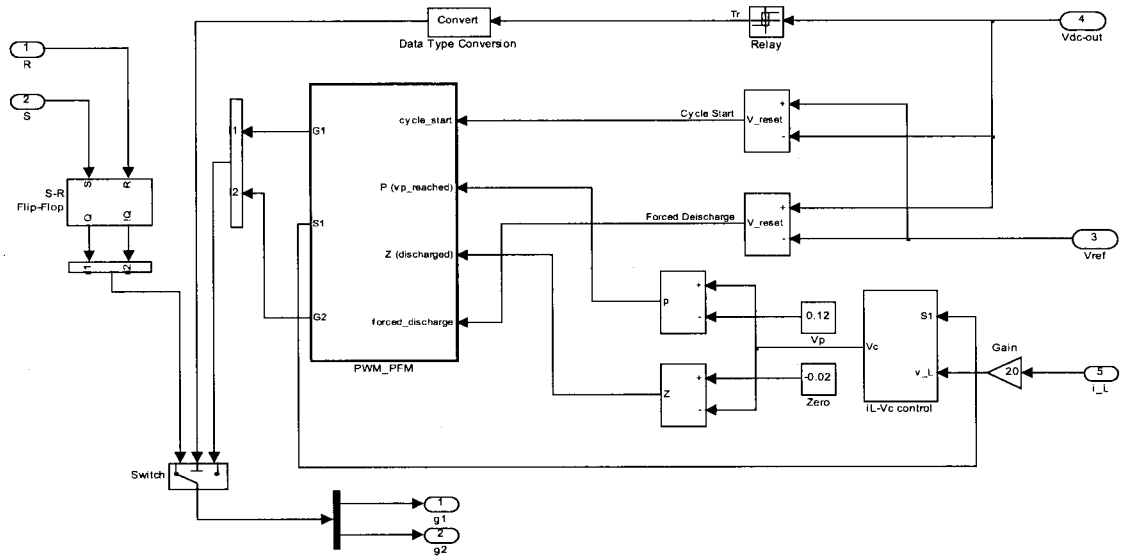

Figure 36 Implementation Diagram of PFM Module inside FPGA

The first sub-circuit is the current-controlled charge-discharge circuit which is named "iL_Vc control" module in Figure 36, and is also shown in Figure 37 in detail.

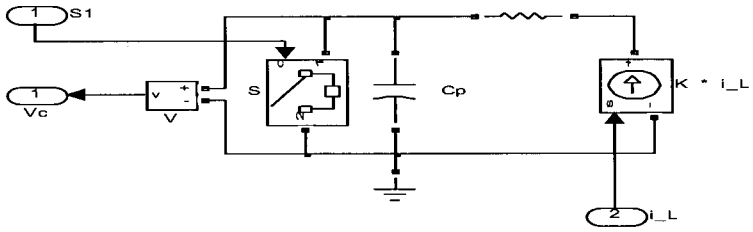

Figure 37 Current Controlled Charge-Discharge Circuit

The current of the inductor L of the DC-DC converter is sensed as an input to the charge-discharge sub-circuit. The current source in this circuit is linearly controlled by this sensed current signal. A capacitor and a digitally controlled switch S are parallel to the

current source. The signal-controlled switch S resets the capacitor to "zero" status. Once the control signal is received, the capacitor C is forced to zero. The circuit converts the ramp-up and down current of the inductor L in DC-DC converter to a voltage signal by integrating the capacitor C. The peak of this voltage signal is proportional to the peak of the sensed current signal.

The second sub-circuit is to generate the signals for pulse generator (Figure 38).

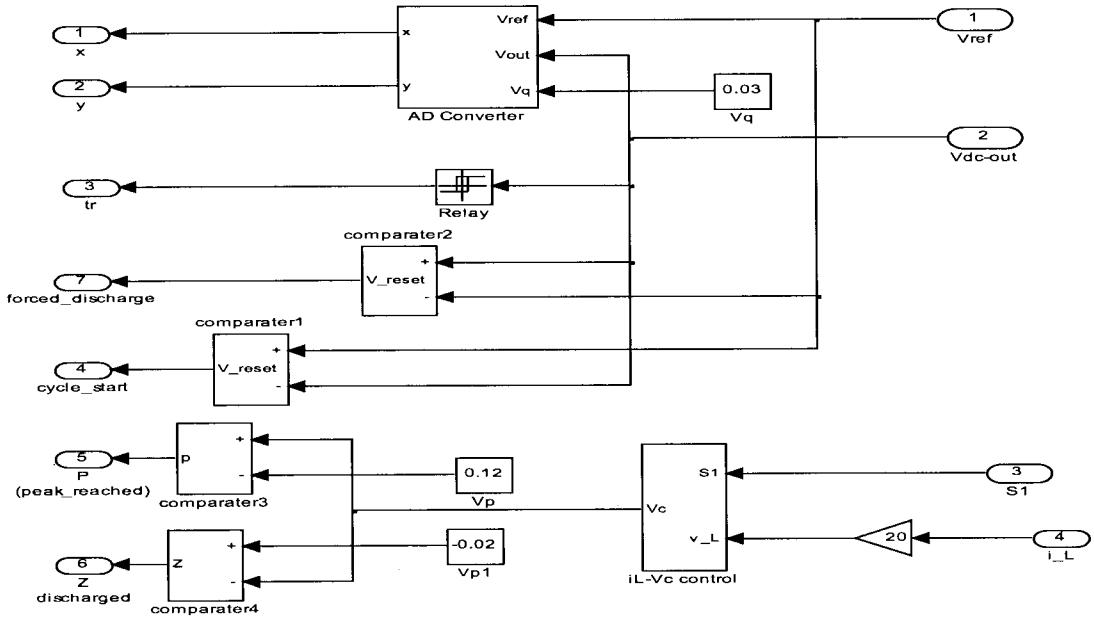

Figure 38 Generation of the Control signals for PFM Module

Two kinds of control signals are created apart from the operation mode signal Tr. One signal is to create a control cycle or pulse frequency by comparing the output voltage of a DC-DC converter V_{dc_out} and the reference V_{ref}. The output signal is cycle_start, which turns to high when V_{dc_out} is lower than the reference. The second control signal is to generate the cycle duty by comparing the voltage V_c from the Charge-Discharge

sub-circuit with the constant peak reference V_p and zero-level V_z respectively. The results of the two comparators, Z (waiting period and the charge-discharge reset circuit) and P (peak current), are sent to the digital pulse generator. It is found that V_{dc_out} can not reach V_{ref} during the experiment, and large difference appears between them if the reference drops down too fast. To avoid the occurrence of such a situation, a control signal is created by comparing the gap between V_{dc_out} and V_{ref}. This signal forces the capacitor C of the charge-discharge sub-circuit to be discharged and turn the DC-DC converter to discharge phase in spite of the peak voltage not being reached.

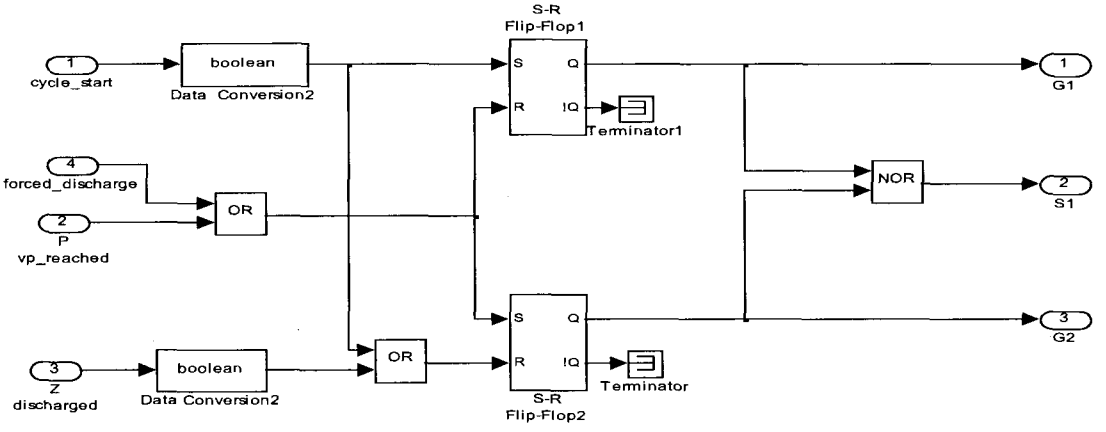

Figure 39 Switching Pulses Generation in PFM Module

The final sub-circuit is a Digital Pulse Generator as shown in Figure 39. This generator has two R-S flip-flops and some logical gates, and processes the control signals from the second sub-circuit, and creates the switching control pulses. Control signal S is also created to open-close the Digital switch S. It can be seen that there is no system clock involved in the DCM mode.

4.2.2 Simulation results

The system is assumed working in light-load environment once the output of the DC-DC converter V_{out} and the reference voltage V_{ref} are found to be lower than transition standard. The digital controller then sets the transition control signal V_{tr} to high and changes the DC-DC converter from CCM mode to DCM mode. The switching control pulses are sent out from the Digital Pulse Generator instead of from the DPWM. The implementation diagram is shown in Figure 36. Here, we set the transition voltage V_{tr} = 1.1V, and the light-load reference V_{ref} = 1V.

It is assumed that, at the beginning of a switching pulse, the control pulse G1 is set to high by the digital pulse generator, the transistor Q1 is turned on, the control signal S1 is set to low, and the controlled switch in charge –dicharge sub-circuit is open. As a result, the current of the inductor L ramps up, and the output voltage V_{out} increases. Meanwhile, in the charge-discharge sub-circuit of the digital controller, the capacitor C is charged by the current source which is controlled by the sensed inductor current. When the inductor current i_L reaches the peak, correspondingly, the output voltage of the capacitor C, V_c, reaches the peak V_p, the control signal P turns to high, the G1 is reset to low, and the G2 is set to high. At the same time, this results in the transistor Q1 getting turned off and the transistor Q2 getting turned on. Then, the inductor current ramps down, and the output V_{out} decreases. When the voltage of the capacitor C, V_c, drops to zero, the control signal Z turns to high. This resets G2 to low and turns off transistor Q2. Meanwhile S1 is set to high. With

the controlled switch S1 closed, the capacitor C is forced to zero. The output voltage V_{out} drops freely until it crosses the reference V_{ref}. Then the switching cycle is repeated by the control signal V_{reset} going low, the G1 being set to high and the digital switch S1 being opened.

Figures 40 and 41 are the simulation results of the DC-DC converter in DCM operation mode. From the output voltage waveform, it can be seen that V_{dc_out} moves above the reference V_{ref}, and changes within a small range, and the switching control pulses are discontinuous.

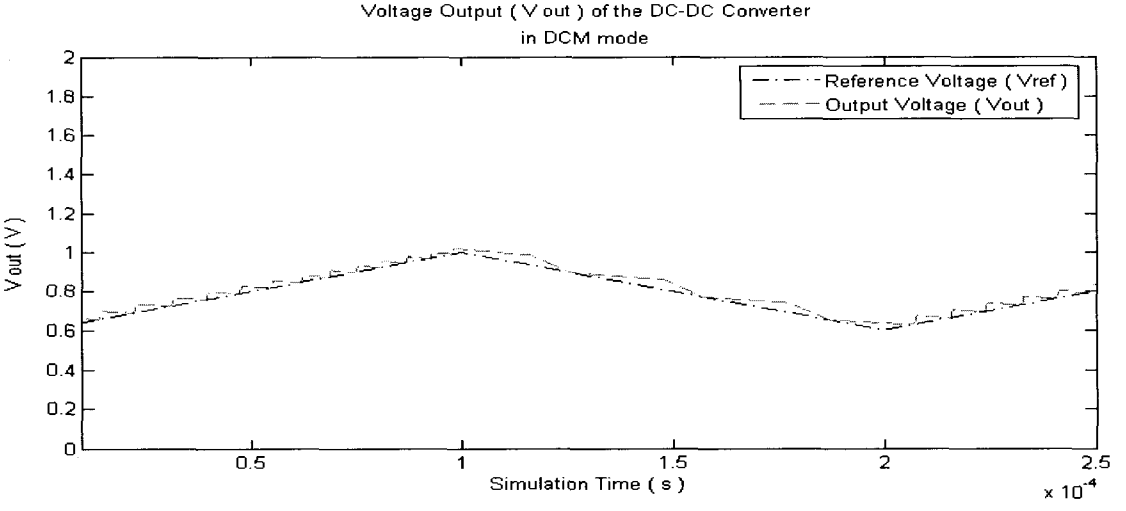

Figure 40 Voltage Output in DCM-PFM Mode

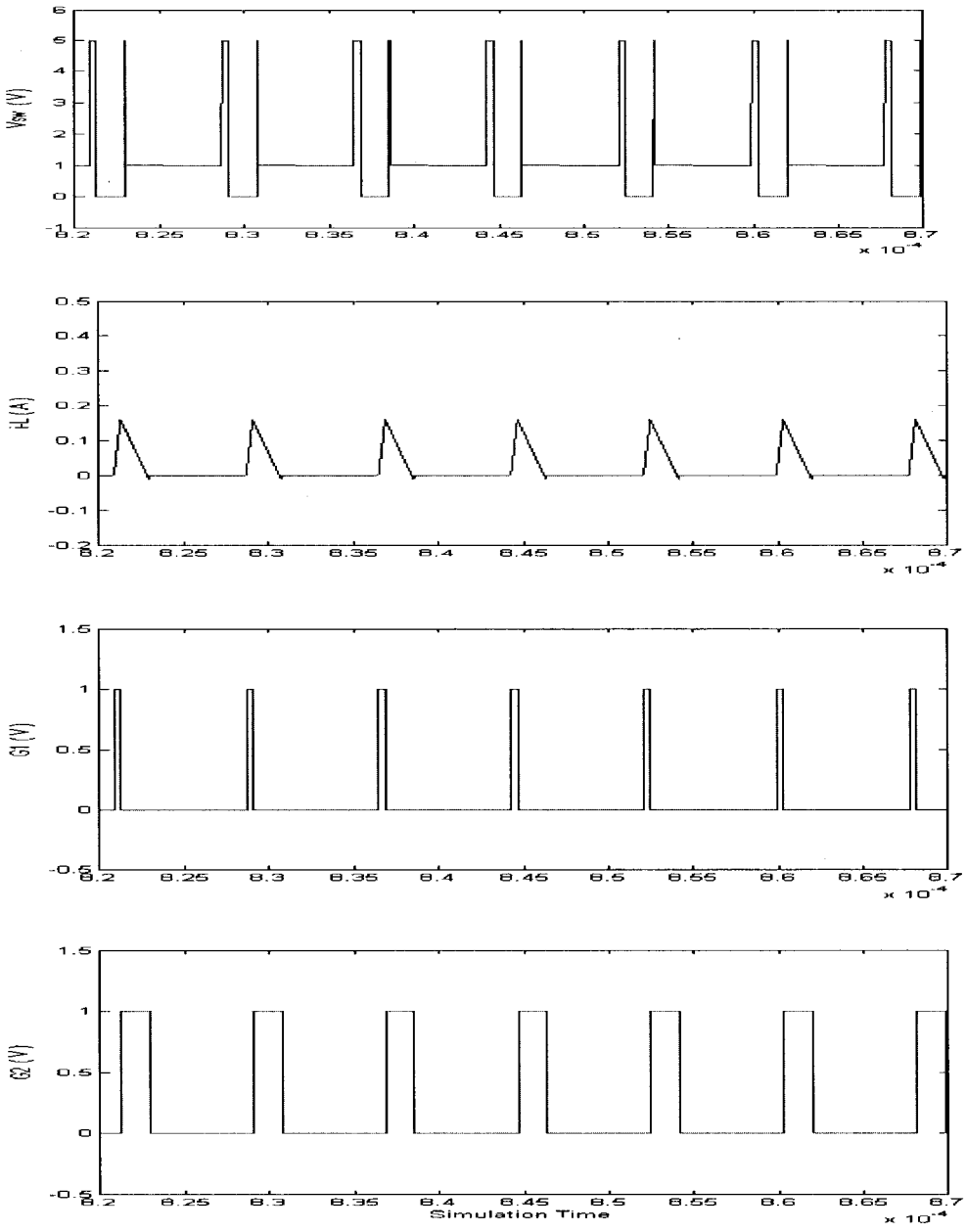

Figure 41 **Controlling Process in DCM Mode:**

a. Switching Voltage between two transistors Vsw;

b. Inductor's Current i_L;c&d. Switching Control Pulses G1&G2

4.3 Transition between CCM mode and DCM Mode

It can be seen that the reference voltage is obtained from the incoming sample signals from the system diagram in Figure 1.The output voltage V_{out} is always regulated around the reference voltage V_{ref} in the digitally controlled DC-DC converter as discussed previously.

The DC-DC converter changes its operation mode between the CCM and DCM when the output voltage V_{out} moves with the reference V_{ref} and crosses the transition threshold V_{tr}.

The DC-DC converter works in the DCM mode when the output level of V_{out} is less than V_{tr}. The current of the inductor is sensed and the switching pulses are generated in PFM modulation by detecting the peak values of inductor and capacitor as described in section 4.2. The Operation mode is switched to the CCM mode once the output V_{out} crosses the threshold V_{tr}. The digital controller changes the duty cycle of the switching pulses G1 & G2 by sampling the output voltage V_{out} and generating the error signals as discussed in section 4.1. The transition of the mode can be observed by the waveforms shown in Figure 42. From the current of the inductor, it is seen that the converter changes operation mode from DCM to CCM. The percentage of the duty cycle for the two switching control pulses increases and occupies the entire switching cycle.

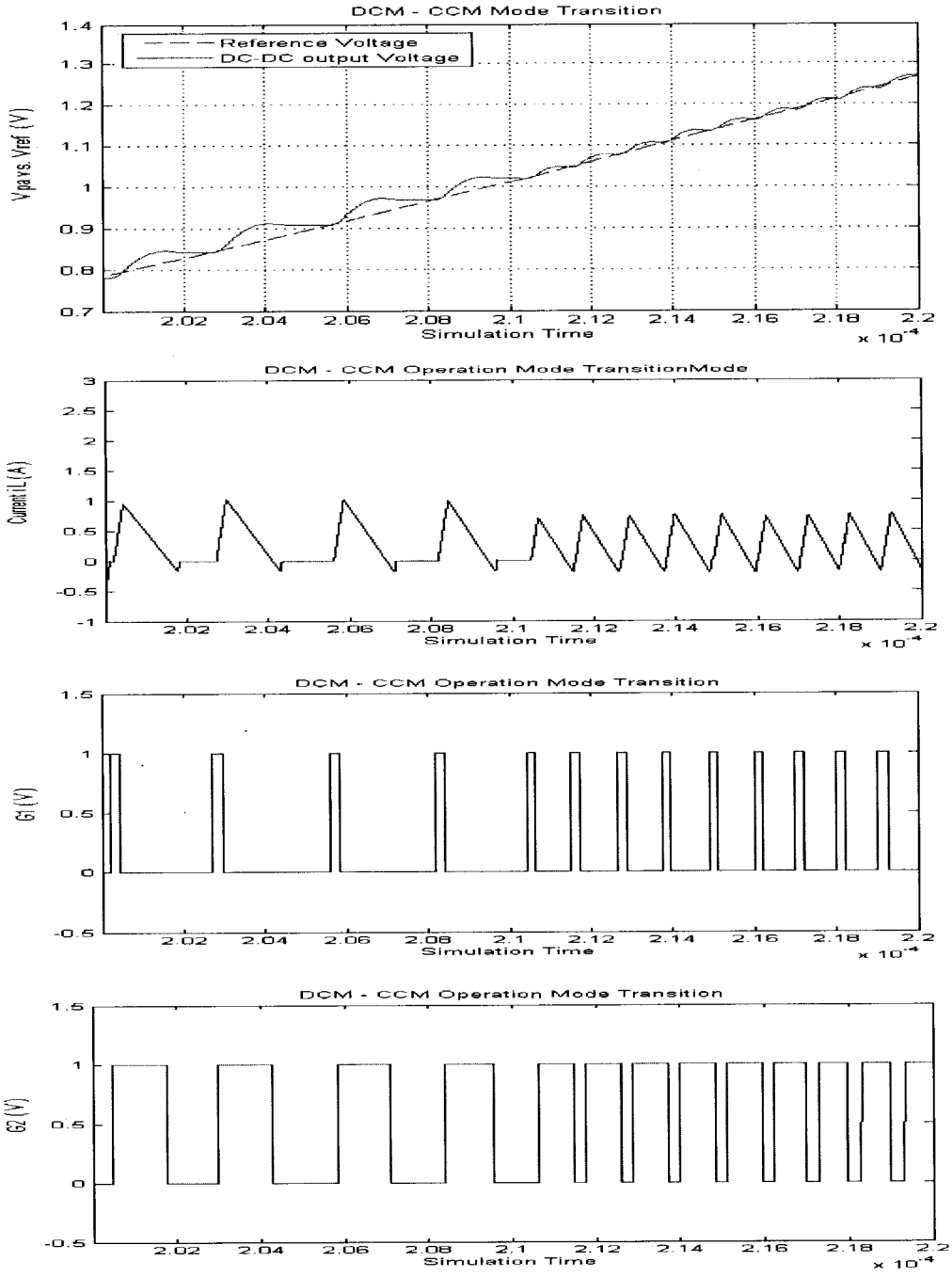

Figure 42 **Transition between DCM-CCM:**

a. Vout vs. Vref;

b. Inductor's Current i_L;

c&d. Switching Control Pulses G1&G2

5. SYSTEM SIMULATION AND ANALYSIS

The simulation diagram of the entire system can be set as follows (Figure 43) based on the system diagram shown in Figure 1, and all the modules discussed in the previous sections.

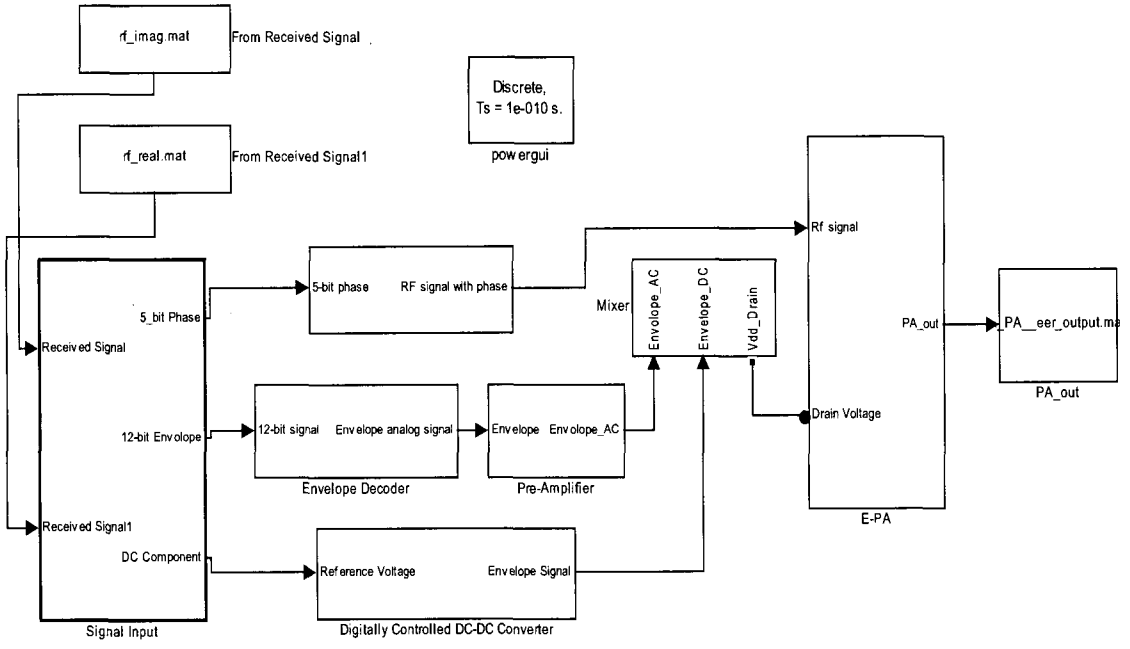

Figure 43 Diagram of Entire Simulation System

The system extracts the reference voltage from the low frequency component (DC path). After converting the received I/Q samples to envelope and phase, the envelope is further decomposed to high frequency and low frequency components. The low frequency component of the envelope drives the DC-DC converter (Figure 44), and the high

frequency component is amplified by the A/B-class amplifier. The AC component is extracted by subtracting the DC signal from the total envelope signal. The outputs are then mixed and applied to the E-class PA.

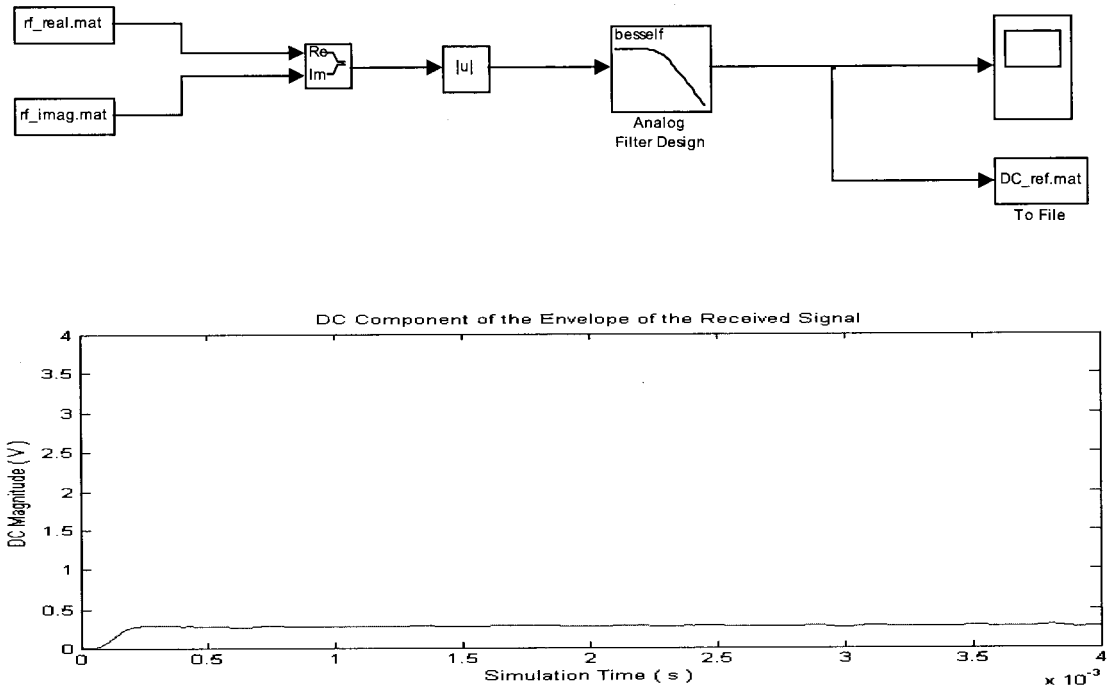

Figure 44 Extraction Diagram of DC reference Command

The System operation process is as follows; the system receives sample RF signal and passes it to the FPGA based processor. The processor then converts the received I/Q signal to phase and envelope paths. The envelope path is further decomposed to high-frequency AC component and low-frequency DC component. The drain supply of E-class PA is created by combining the pre-amplified AC-envelope component and the output from the Digitally Controlled DC-DC Converter thatfollows the change of DC-envelope component. The input of E-Class PA is generated from phase envelope.

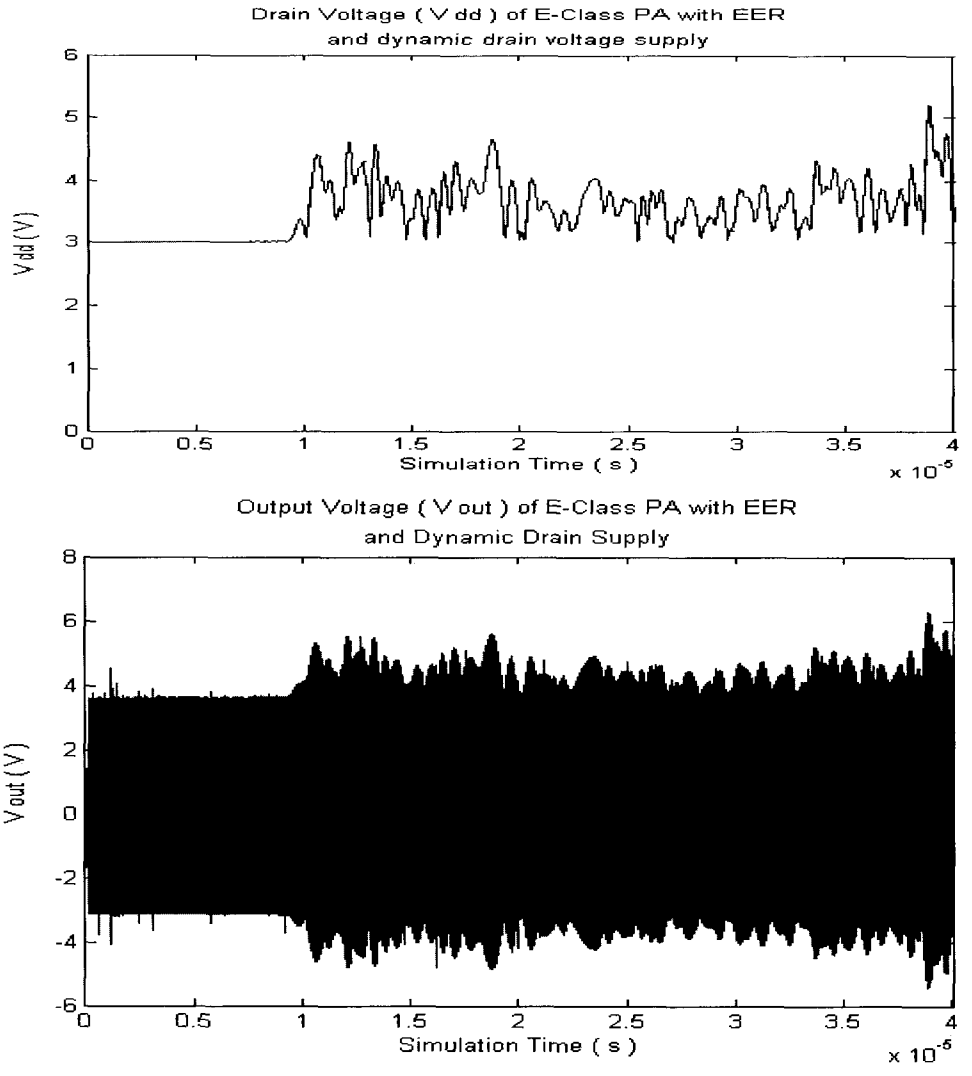

Figure 45 **System Simulation Results with Carrier RF at 850 MHz:**
a. Pre-Amplified Envelope Signal;
b. Output of Digitally Controlled DC-DC Converter

The output of the E-Class PA is an envelope and phase modulated RF signal as shown in Figure 45.

The system performance can be simply verified by comparing the output of the E-Class PA with the received signal in both time domain and frequency domain. We

demodulate the output RF signal (shown in Figure 45.b) of the E-Class PA according to the scheme shown in Figure 46.

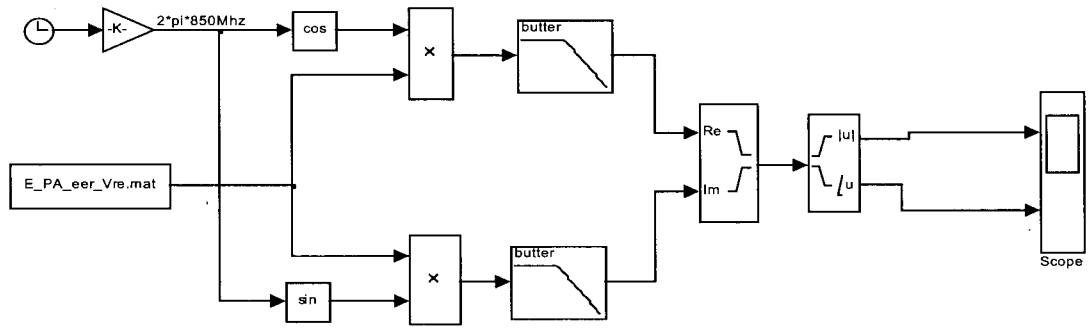

Figure 46 Diagram of Demodulation Module

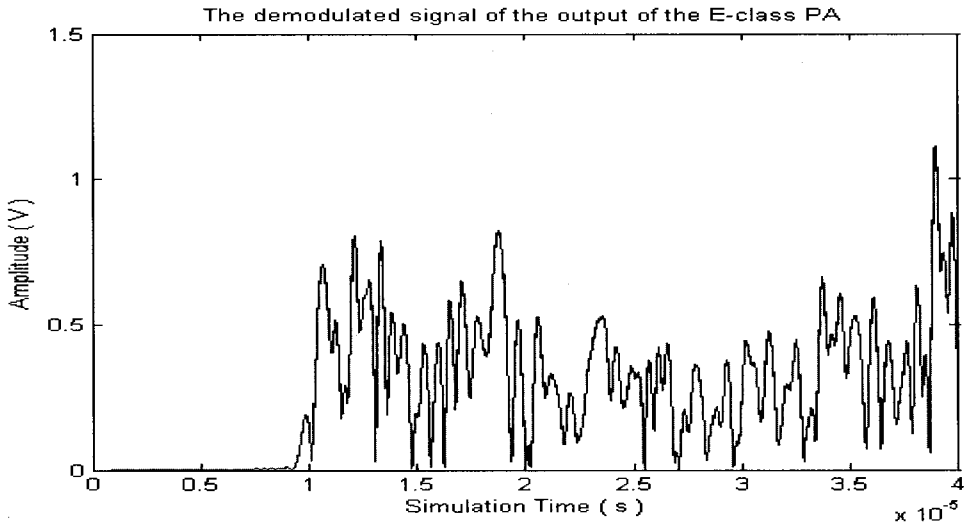

Figure 47 Envelope Component of Demodulation Signal

The demodulation signal is shown in Figures 47 and 48 in envelope and phase separately.

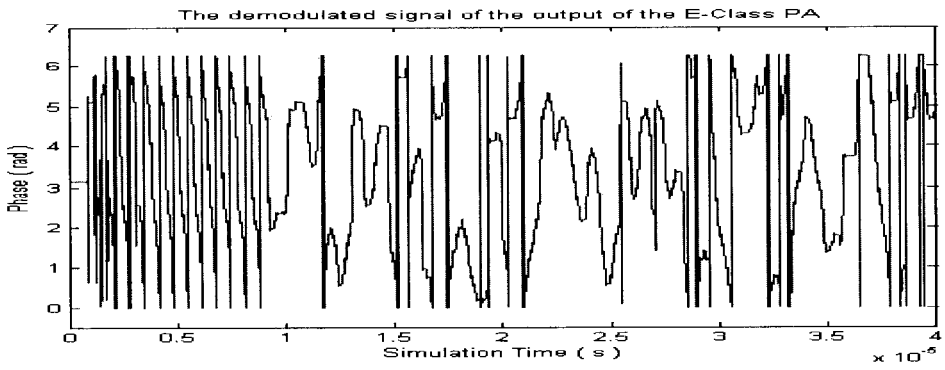

Figure 48 Phase Component of Demodulation Signal

Comparing these two figures with the received signal shown in Figure 10, it can be seen that the output demodulated signal has the same shape as the received signal. We can further compare them by tracking the error between them. To obtain the correct comparison results, we have to eliminate the influence of the delay of phase path and envelope path in EER operation mode, and also the delay of the E-Class PA. After considering the gain from the system, the error between the original signal and the output of the E-Class PA can be obtained by simply subtracting one from the other and taking the absolute value. The comparison of the envelope and the phase are shown in Figure 49.

We can also calculate the relative error of the envelope by the following formula

$$AverageError(\mathrm{Re}lative) = Average(\frac{ABS(Output - Input))}{Input}).$$

The relative error of envelope in the simulation duration is

AveError(Envelope) = 0.04787 (V).

The average phase error is,

$$AverageError(\text{Re}lative) = Average(Abs(Output - Input)) = 0.2319 \text{ (rad)}$$

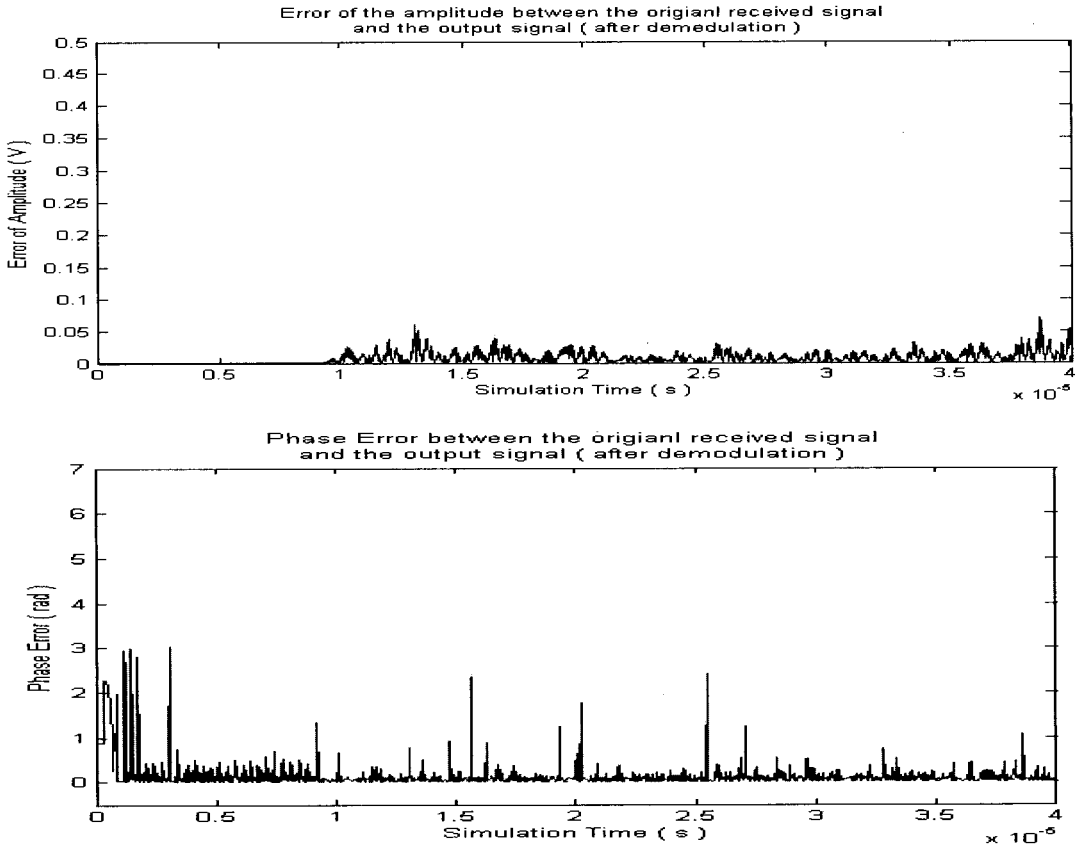

Figure 49 Error between the demodulation Signal and the Received Signal

It can be verified that the system is able to work normally and obtain a recognized output from the input by comparing the results in time domain. The implemented system in Simulink lacks accurate models for most components. Hence, we can only examine the system performance byobtaining the difference between the output and the input. Further analysis, such as more accurate error or power efficiency analysis can not be done.

The output RF signal and the demodulated signal are converted to frequency domain by FFT (Discrete Fast Fourier transform) in Simulink/Matlab. The frequency spectrum of the RF output of the E-class PA at 850 MHz is shown in Figure 50.

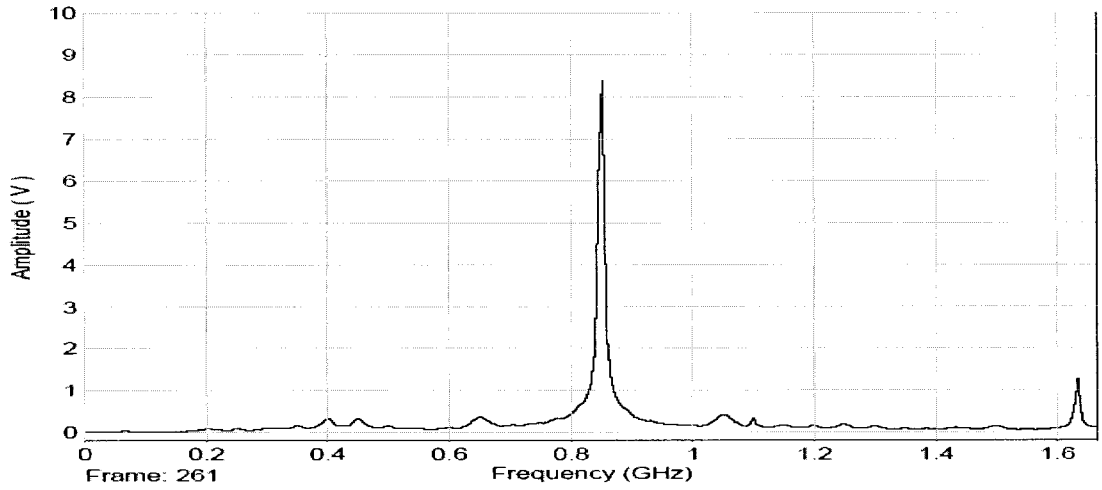

Figure 50 Frequency Spectrum of the output RF Signal

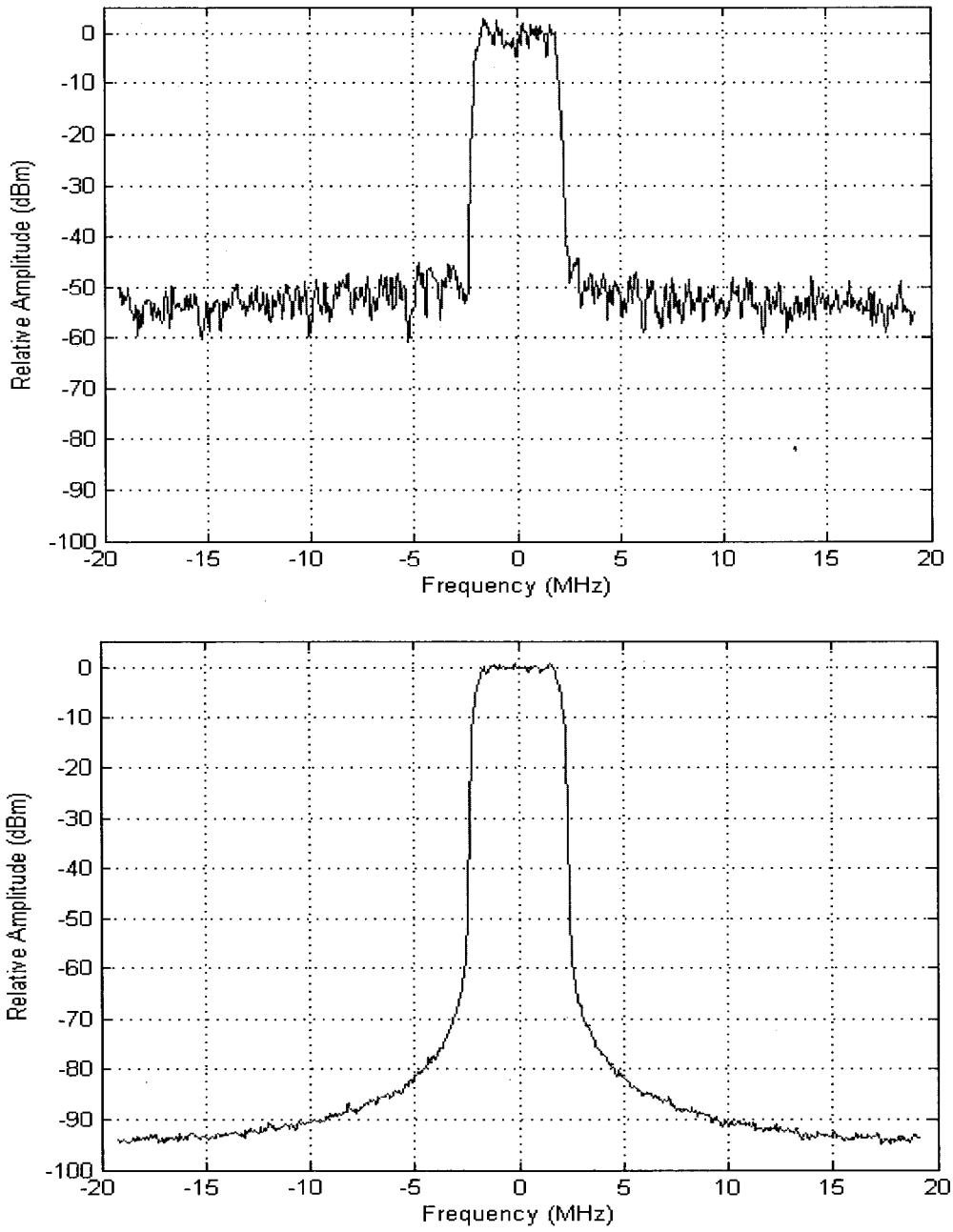

Figure 51 **Frequency Spectrum in Baseband:**
a. Received Signal,
b. Output demodulated Signal

We check the frequency spectrum of both signals in baseband (Figure 51) to compare the output with the input.

It can be seen that the bandwidth of the output demodulated signal is almost same in the range from 0 dBw level to -40 dBw level with about 10 MHz width after reshaping two signals to the same relative amplitude. Even though most of the components implemented in our system are ideal, and no noise is introduced either from extension or within devices, some noise still exists in the system, thus affecting the output signal. The noise comes from the resolution of DAC of envelope path, Phase-Shifter, response of the DC-DC converter, delay of two paths of EER operation mode and delay of E-Class PA. The signal to noise ratio of the output signal in baseband is much lower than the received signal.

CONCLUSION

Any input signal can be decomposed to polar form in baseband instead of I/Q form. Atthe RF transmitter end, this allows us to increase the power efficiency by using switch-mode high efficiency E-Class PA. It also improves the linearity by implementing the EER operation mode. To provide a dynamic drain voltage, a digitally controlled DC-DC converter is deployed. An FPGA based digital controller allows programmability of mode transition, digital compensation, etc. Through detecting the output with reference, the system can operate in CCM and DCM mode separately. The digital controller samples the output voltage, changes the duty cycle of the switching control pulses by DPWM modulation in CCM mode, detects the peak inductor current, and adjusts the pulse frequency by PFM modulation in DCM mode. This dynamic management scheme adjusts the power output according to the system operation status, thus further improving the system power efficiency. This operation architecture is also easy to implement. However, more attention needs to be paid to synchronize the phase and envelope paths.

Another advantage in our system is that the reference command comes from the DC component of the received signal. This reduces the bandwidth requirement of the DC-DC converter.

It has been possible to design and simulate most of the components in detail in SIMULINK environment. Compared to a straight forward PA design, the complexity of this design increases drastically with additional components such as DAC and digital logic. It is difficult to estimate the power consumption of the entire design. Fortunately, most of the complexity added is digital circuitry. We can take complete advantage of the advanced VLSI technology for its low power, high density, high speed, and low cost. There are some components in the system which are very difficult to simulate due to the lack of accurate models. For the system level simulation, we used ideal models for them. The overall system performance can only be evaluated accurately with these components specified.

The system runs only for a short duration due to the limitation of the processing power of the computer used for the simulation. In addition, some complex modules, such as Digitally Controlled DC-DC Converter, are simulated separatelywith the simulation results saved in a file and then passed to E-Class PA for further simulation. This increases the difficulty of quantitative analysis for system power efficiency.

FUTURE WORK

The next step for this project is to implement the entire system in hardware. Most of the digital logic can be transferred into an FPGA.

The conversion from simulink block diagram to FPGA implementation is fairly straightforward using tools provided by the FPGA venders. Other components such as the E-Class PA, DC-DC converter can be built using discrete components.

The system performance can then be evaluated in a real hardware implementation.

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