LOW NOISE HIGH DYNAMIC RANGE PIXEL ARCHITECTURE IN AMORPHOUS SILICON TECHNOLOGY FOR DIAGNOSTIC MEDICAL IMAGING APPLICATIONS

by

Golnaz Sanaie-Fard
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Name: Golnaz Sanaie-Fard

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Examining Committee:

Chair: **Dr. John Jones**
Professor of the School of Engineering Science

Dr. Karim S. Karim
Senior Supervisor
Assistant Professor of the School of Engineering Science

Dr. Ash M. Parameswaran
Supervisor
Professor of the School of Engineering Science

Dr. Andrew H. Rawicz
Internal Examiner
Professor of the School of Engineering Science

Date Defended/Approved: Apr. 11/06

ABSTRACT

The vast majority of commercially available flat panel digital x-ray imagers are based on flat panel amorphous silicon (a-Si) thin film transistor (TFT) switch pixels that are derived from active matrix liquid crystal display (AMLCD) technology. In this thesis, we develop on-pixel analog-to-digital converters (A/D's) as alternate pixel architectures for large area digital x-ray imagers to incorporate off-panel components into the on-panel integrated circuit. The higher level of integration can lead to lower complexity and costs, higher speeds and better imager performance. Different voltage controlled oscillators (VCOs) were considered in this thesis including an LC tank oscillator, a relaxation oscillator, and a ring oscillator. Ring oscillators became the choice for on-pixel A/D's in this thesis due to their compact nature and higher frequency output for amorphous silicon thin film transistor based circuits. Measured results for voltage to frequency gain and estimations of phase noise and metastability are presented.

Keywords: Medical x-ray imaging, flat panel detector, thin film transistor, amorphous silicon, high dynamic range

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GLOSSARY

A/D: Analog-to-digital

a-Si: Amorphous Silicon

a-Si:H: Hydrogenated Amorphous Silicon

AMFPI: Active Matrix Flat Panel Imager

AMLCD: Active Matrix Liquid Crystal Display

CAPS: Current Mediated Amplified Pixel Sensor

CVD: Chemical Vapour Deposition

HAPS: Hybrid Active Pixel Sensor

LCVCO: LC tank Voltage Controlled Oscillator

PECVD: Plasma Enhanced Chemical Vapour Deposition

PPS: Passive Pixel Sensor

RIE: Reactive Ion Etching

TFT: Think Film Transistor

VCO: Voltage Controlled Oscillator

V_T: Threshold voltage

CHAPTER 1: INTRODUCTION

Flat panel digital x-ray imagers provide benefits such as tele-diagnosis, immediate viewing of the radiograph, convenient computer storage and portability due to the compact and light nature of flat panel technology. These imagers started appearing as commercial products in 2003 and offer an alternative to film and chemicals in radiography, image plates in computed radiography, and bulky image-intensifiers in fluoroscopy with smaller, lighter, and more portable devices. The backbone of flat panel digital imagers stems from amorphous silicon active matrix liquid crystal display (AMLCD) technology of the mid-80s. The challenge in designing medical x-ray imagers comes from the fact that x-rays are not easily focused and the imager needs to be necessarily on the scale of the object being imaged; therefore, designing large area detectors is needed. CCD's and CMOS imagers found in digital cameras and video recorders are usually on the order of one to two centimetres in area and, therefore, not suitable for medical imaging applications [1]. Amorphous silicon (a-Si[1]) technology, however, offers benefits of uniform deposition over large area, low capital cost, and tolerance to x-ray radiation and subsequently there is motivation for research in advancing flat panel x-ray imager capabilities.

In designing a flat-panel x-ray imager, the specifications are based on the clinical needs of a particular diagnostic imaging modality, e.g. mammography, chest radiography,

[1] In this thesis a-Si technology refers to the field of amorphous silicon in general and a-Si:H refers to hydrogenated a-Si where hydrogenation is used for all TFTs to improve their characteristics

or fluoroscopy. Fluoroscopy, for example, is real-time x-ray imaging of the patient body and is used in many types of examinations and procedures, such as barium meal x-rays, cardiac catheterization, and placement of intravenous catheters – a technique that requires insertion of hollow tubes into veins or arteries. In catheterization, the catheter is guided through an artery using a real-time x-ray imager and, therefore, the patient is continuously exposed to radiation during the operation. The continuous exposure is what necessitates low x-ray dosage to reduce patient exposure and subsequently, the input signal to the imaging electronics becomes very small and challenging to detect. Using industry standard, a-Si switch based pixels [3], the signal-to-noise ratio (SNR) at the low fluoroscopic exposure levels can result in blurred images. In contrast, current-mediated a-Si pixel amplifier circuits have been reported [3], [4] to give an improved SNR for real-time low dose imaging. However, for imaging modalities that require larger doses to the patient, and consequently result in large x-ray input signals, the pixel amplifier output becomes non-linear, thus limiting the upper end of the pixel dynamic range. To address this challenge, a dual mode type pixel architecture, the hybrid active pixel sensor (HAPS) [5], [6], [7], [10] was investigated that exhibited both small and large signal linearity.

The trend for electronics and in particular, digital imagers is to incorporate greater complexity in the integrated circuits because it allows lower costs, higher speeds and potentially better image quality. The focus of this thesis lies in transferring off-panel readout circuit complexity into on-pixel intelligent integrated circuits in a-Si:H TFT technology. We achieve this objective by developing on-pixel analog-to-digital (A/D) converters [11], the main focus of this thesis, to improve pixel integration and possibly obtain better SNR.

This thesis investigates the feasibility of on-pixel A/D conversion using various VCO circuits in TFT technology. In this document, first we begin with an overview of medical x-ray imaging in various modalities using flat panel x-ray imaging technology, starting from passive pixel sensor (PPS), followed by current-mediated active pixel sensors (CAPS) and our investigations on the hybrid active pixel sensor (HAPS) in Chapter 1. In Chapter 2, various VCOs are investigated to obtain the suitable circuit that is both adoptable in a-Si:H fabrication technology and is suitable for high dynamic range x-ray imaging. Chapter 3 will focus on our investigations on Hartley and Colpitts LC tank oscillators. Finally, simulation and fabrication results of Relaxation and Ring oscillators are presented in Chapter 4 followed by conclusions in Chapter 5.

1.1 X-ray Imaging Requirements

The pixel, forming the fundamental unit of the active matrix, consists of a detector and a readout circuit, whose configuration in practice differs with the detection scheme. Two schemes [4] are prevalent in literature: the first is direct-detection which uses an x-ray photoconductor as the detector (for example, amorphous selenium (a-Se)) and the second is an indirect detection scheme, which employs a scintillation layer (CsI phosphor for example) coupled with an a-Si:H p-i-n photodiode sensor. Figure 1 depicts the components in the indirect detection method.

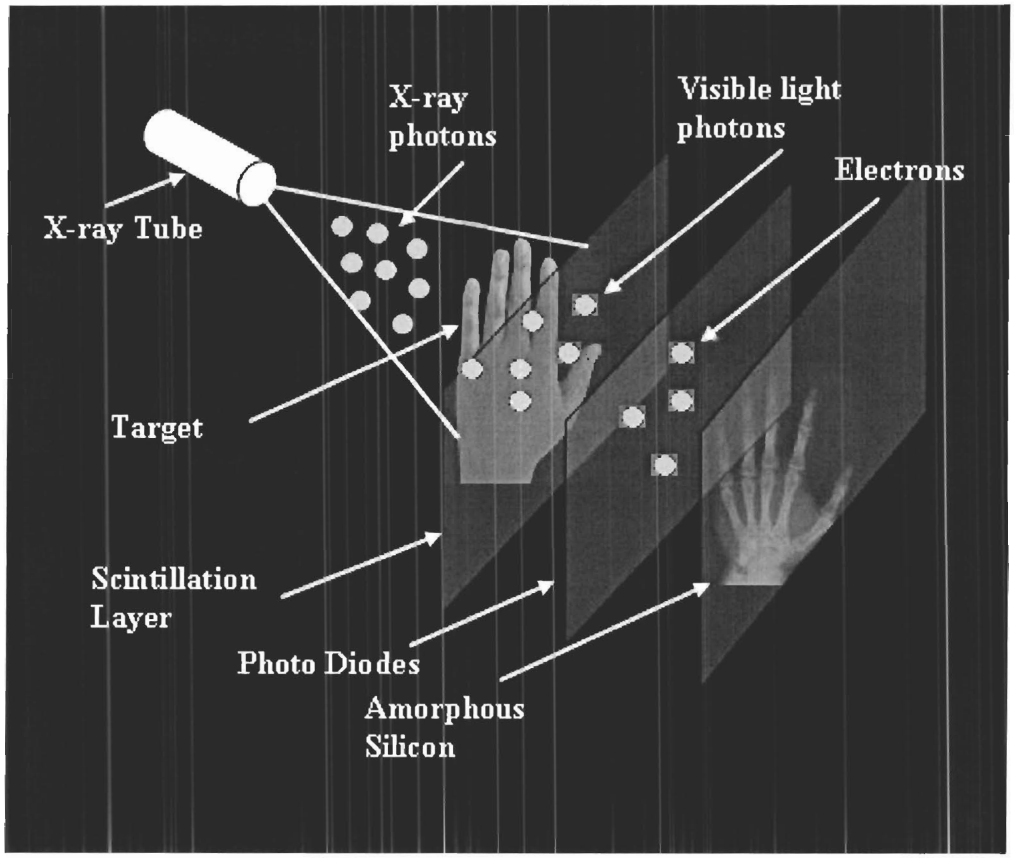

Figure 1. Components in flat panel x-ray imaging (indirect detection method)

Regardless of the detection scheme, the detector needs to be coupled with an appropriate on-pixel readout circuit to efficiently transfer the collected electrons to external off-panel electronics for data processing. A sample array of active[2] matrix flat panel imager (AMFPI) architecture is illustrated in Figure 2. The AMFPI architecture is used for a-Si digital x-ray imaging applications. A gate driver sequentially addresses every row in the array. Pixel outputs are connected to charge amplifiers and the columns are read out in parallel when a row of TFTs is enabled. The amplifier outputs are then

[2] The word active comes from pixel switching using active devices or TFTs.

multiplexed to an analog-to-digital (A/D) converter, which sends the digital output to a computer for image signal processing.

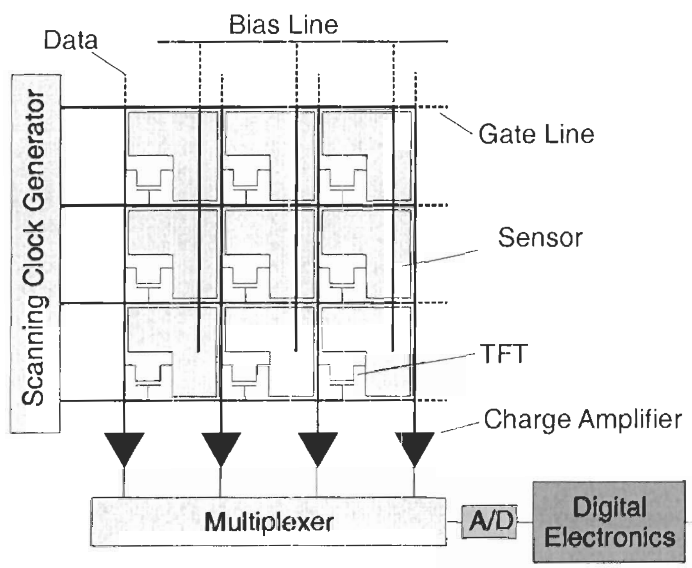

Figure 2. Active matrix flat panel imager (AMFPI)

The requirements on x-ray spectrum and exposure for a direct detection imager using a-Se are shown in Table 1. for diagnostic fluoroscopy and chest radiography. The primary differences between the two modalities lie in the real-time nature of fluoroscopy and the different amounts of charge collected per pixel area. The pixel capacitance for a-Se photoconductors where dielectric constant $\varepsilon_{a\text{-}Se}$=6.3 and thickness $t_{a\text{-}Se}$=500μm is calculated to be in the fF range and therefore the pixel capacitance is dominated by TFT parasitic capacitances in this case. Smaller pixel capacitance will give larger voltage swing and therefore better detection.

Table 1. Requirements for a digital flat panel x-ray imager for a-Se [1]

	Chest Radiography	Fluoroscopy
Imager size (cm)	35 x 43	25 x 25
Pixel area (μm^2)	200 x 200	250 x 250
Pixel count	1750 x 2150	1000 x 1000
Image readout time (s)	< 5	0.033/frame (for 30Hz)
X-ray spectrum (kVp)	120	80
Exposure range (mR)	0.03 – 3	0.0001 – 0.01
X-ray fluence (photons/mm^2/mR)	2.30 x 10^5	1.98 x 10^5
Image charge per pixel (e-/pixel/mR)	3.45 x 10^6	4.91 x 10^6
Image charge per pixel (in pC)	0.016 – 1.6	0.00008- 0.008
Voltage at pixel (for Cpix=0.2pF)(V)	0.08 – 8	0.0004-0.04

As evident, more than two orders of magnitude of charge can accumulate on a pixel during x-ray exposure. In the following sections, we will discuss the dynamic range limitations of the industry standard, switch based, amorphous silicon passive pixel sensor (PPS) and the recently reported current mediated amplified pixel sensor (CAPS) architecture, which led us to the design of hybrid active pixel sensor (HAPS).

1.2 Passive Pixel Sensor (PPS) Architecture

PPS is the workhorse of the imaging industry and consists of a sensor element (e.g. p-i-n photodiode) and an integrated readout TFT. There are three modes of operation for the PPS depicted in Figure 3.

- **Integration Mode:** Signal charge accumulates on C_{PIX} (sum of sensor and parasitic capacitances at node V_G) proportional to the amount of x-ray radiation.

- **Readout/Reset Mode:** Following integration, the READ TFT is turned ON thereby transferring the signal charge accumulated on C_{PIX} during integration to the feedback capacitance, C_{FB}, of the column charge amplifier. The readout step also causes pixel to reset since the charge transfer is a destructive process. Also, since readout is essentially a charge transfer process, the gain of the PPS is limited to being ≤1 and the operation is inherently linear.

Charge accumulated on C_{PIX} is read out through the TFT ON resistance and converted to a voltage via the column charge amplifier. During readout, the READ TFT is biased in the linear region to provide a low ON resistance for quick readout. When the TFT is OFF, it is biased to be non-conducting. Previous studies [3], [4] have shown that the PPS may be used for real-time imaging. However, the readout charge amplifiers add a large external noise component to the PPS (~1700 electrons at the detector input [1]), which drowns out the lower range of fluoroscopic input signal.

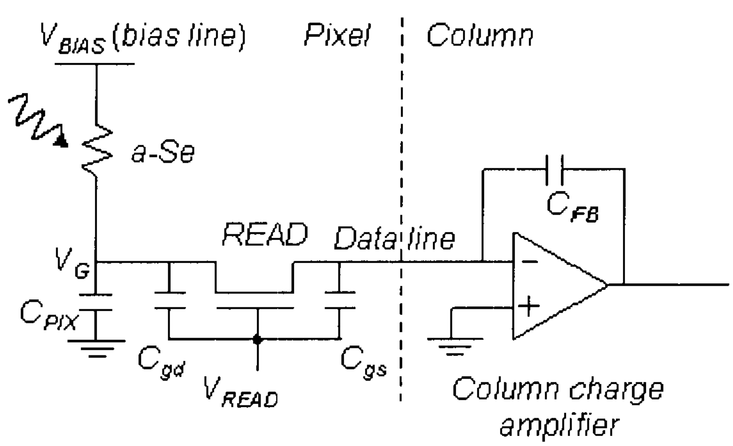

Figure 3. Schematic of a PPS using a-Se photo detector. C_{gs} and C_{gd} are the parasitic gate-source capacitances of the READ TFT switch [4]

1.3 Current-mediated Active Pixel Sensor (CAPS)

To achieve quantum noise limited x-ray imagers for fluoroscopy, signal amplification can be incorporated at either the x-ray detector or at the pixel readout circuit. The former alternative requires the use of high gain x-ray detectors such as HgI_2, PbO or CdZnTe, all of which are still in their experimental stages [8]. The second alternative of using a-Si on-pixel amplifiers to improve the fluoroscopic SNR is promising [3], [4]because it does not require a departure from either the well-established x-ray detector technologies or the mature a-Si thin film transistor (TFT) technology. Central to the current-mediated active pixel sensor CAPS illustrated in Figure 4 is a source follower circuit which produces a current output to drive an external charge integrating amplifier. The CAPS operates in three modes [4]:

Reset mode: The RESET TFT switch is pulsed ON and the pixel capacitance, C_{PIX} charges up to Q_P through the TFT's on resistance and the potential at C_{PIX} becomes V_G. In direct detection, C_{PIX} is usually defined by an on-pixel storage capacitor since the a-Se photoconductor capacitance is very small as explained earlier.

Integration mode: After reset, the RESET and READ TFT switches are kept OFF. During the integration time, the input signal, $h\nu$, generates photo-carriers discharging C_{PIX} by ΔQ_P and decreases the potential on C_{PIX} by ΔV_G.

Readout mode: After integration, the READ TFT switch is turned ON for a sampling time, T_S, which connects the APS pixel to the charge amplifier and an output voltage, V_{OUT}, is developed across C_{FB} proportional to T_S.

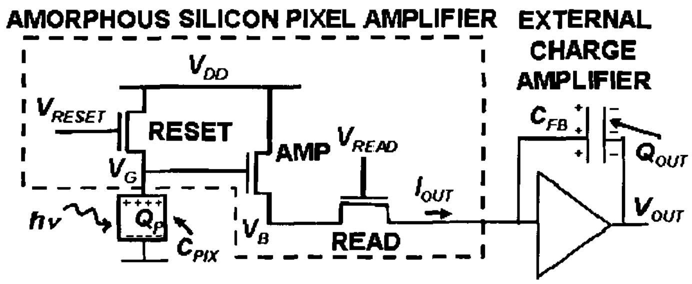

Figure 4. Current mode active pixel architecture [4]

Current-mediated a-Si pixel amplifiers have been reported to give a good SNR for fluoroscopy at low x-ray inputs [4]. However, since the drain current of the AMP TFT (denoted as I_{OUT} in Figure 4) has a quadratic relationship with the voltage at the gate of the AMP TFT (i.e. V_G), the charge amplifier output, V_{OUT}, changes non-linearly with changes in V_G. This nature of the quadratic relationship can be determined by examining the behaviour of ΔI_{OUT} with respect to ΔV_G. Here, we note that the AMP TFT is operating in the saturation region while the READ TFT is in the linear operation region during pixel readout. Taking into account the non-idealities of a-Si, where $(W/L)_{AMP}$ is the aspect ratio of the AMP TFT, μ is the electron band mobility, C_I is the insulator capacitance per area, K_t is the temperature constant, x_S is the channel length modulation, and V_{T0} is the threshold voltage, the current relationship of AMP TFT is given as [4],

$$(I_{DS})_{AMP} = K_{AMP}(V_G - V_B - (V_{T0})_{AMP})^{2/K_t} x_S, \quad (1)$$

where,

$$x_S = [1 - V_{DS}/\lambda]^{-1} V_{DS}^{(2-2/K_t)/2}, \text{ and } K_{AMP} = (W/L)_{AMP} \mu C_I x_S \quad (2)$$

Based on a nominal channel temperature T = 300ºC and setting $(I_{DS})_{AMP}$ to I_{OUT}, and neglecting channel length modulation equation (1) can be simplified as following,

$$I_{OUT} = K_{AMP}(V_G - (R_{ON})_{READ} I_{OUT} - (V_{T0})_{AMP})^2 \tag{3}$$

where,

$$(R_{ON})_{READ} = 1/(\mu C_I (W/L)_{READ}(V_{READ} - (V_{T0})_{READ})) \tag{4}$$

The pixel's charge gain and voltage gain are defined as,

$$G_i = |\Delta Q_{OUT} / \Delta Q_P| = (\Delta I_{OUT}.T_S)/\Delta V_G C_{PIX} = g_m T_S / C_{PIX} \tag{5a}$$

$$A_V = |V_{OUT} / V_{in}| = (Q_{OUT}.C_{PIX})/(Q_{PIX} C_{FB}) = g_m T_S / C_{PIX} \tag{5b}$$

where,

$$g_m = \delta I_{OUT} / \delta V_G \tag{6}$$

In equation (3), as long as the change in V_G is kept small [4],

$$\Delta V_G << 2(V_G - (V_{T0})_{AMP}), \tag{7}$$

the current I_{OUT} in (3) will change linearly with changes V_G and therefore g_m will be a constant number which results in linear charge gain and voltage gain[3]. Figure 5 illustrates simulation results for CAPS charge gain linearity. Here, the circuit in Figure 4 was simulated using $V_G = V_{DD}$, V_{READ} = 20V, $(V_{T0})_{AMP} = (V_{T0})_{READ}$ = 3.2V, C_I = 250µF/m^2, μ = 0.8cm^2/V.s, $(W/L)_{AMP}$ = 280µm/30µm, $(W/L)_{READ}$ = 200µm/10µm, x_S = 450, C_{FB} = 10pF, and C_{PIX} = 1pF. The TFT model was implemented in Verilog-A and was based on the static and dynamic behaviour reported in [9].

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[3] Further details of the above calculations can be found in [10].

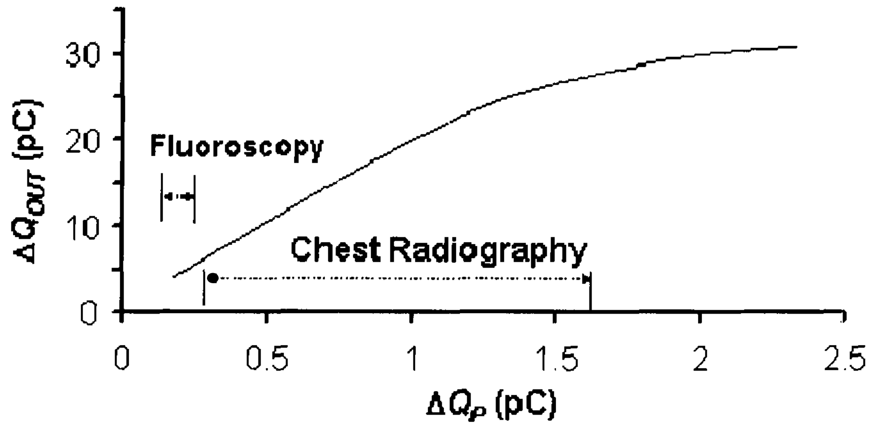


Figure 5. Simulation results for the linearity of the CAPS charge gain, G_i (Fluoroscopy and chest radiography range are shown for comparison)

The primary consequence of a non-linear pixel transfer function is that standard correlated double sampling[4] mechanisms cannot be implemented in hardware as is typically done with active matrix imaging arrays. There are a couple of alternatives to overcome the inherent non-linearity in the CAPS readout circuit at higher x-ray input levels. A possible solution to the non-linearity issue is to implement a frame memory in software to store each CAPS pixel's transfer characteristic curve so that the x-ray input could be extracted by interpolation. This is not however, an attractive option because longer frame times are required to process the imager output than if the basic non-uniformity correction was primarily implemented in hardware. In addition, the instability of a-Si transistors in the CAPS pixel will cause the pixel transfer characteristics to shift [12]. Unstable pixel transfer characteristics would require repeated characterization of the

[4] Double sampling [4] is required to correct for the effect of process non-uniformities (in the form of offsets) and in the case of a-Si technology, transistor instability on pixel circuit performance.

pixel transfer functions at regular intervals which would further slow down the imager readout making it challenging to switch instantaneously from fluoroscopic to radiographic mode. X-ray imagers targeting chest radiography can have up to 4 million pixels per imager which would make rapid readout times with a software frame memory challenging. In the following section, we present a hybrid pixel architecture, based on the PPS and CAPS architectures, which offers a pixel-level solution to achieve high dynamic range capabilities.

1.4 Hybrid Active Pixel Sensor (HAPS)

Based on PPS and CAPS architectures, the hybrid active pixel architecture exhibits real-time readout, amplification, large signal linearity, and consequently higher dynamic range x-ray imaging. A circuit schematic of hybrid active pixel sensor (HAPS) architecture is shown in Figure 6. In this circuit, by switching between PPS architecture for radiographic mode and CAPS for low-noise fluoroscopy we can produce high dynamic range flat panel imager. During fluoroscopic mode, the RDC transistor is operated while the RDP TFT (i.e. the PPS switch) is kept OFF, and the circuit would essentially behave as the CAPS circuit shown in Figure 4. In CAPS operation, the pixels send their outputs on column (n). For radiographic operation, however, the RDP pixel transistor is operated while the RDC and RESET transistors are OFF and the circuit operates as a PPS sending its output on column (n-1). Linearity and gain, transient behaviour, metastability, and noise performance of HAPS will be discussed in the following sections.

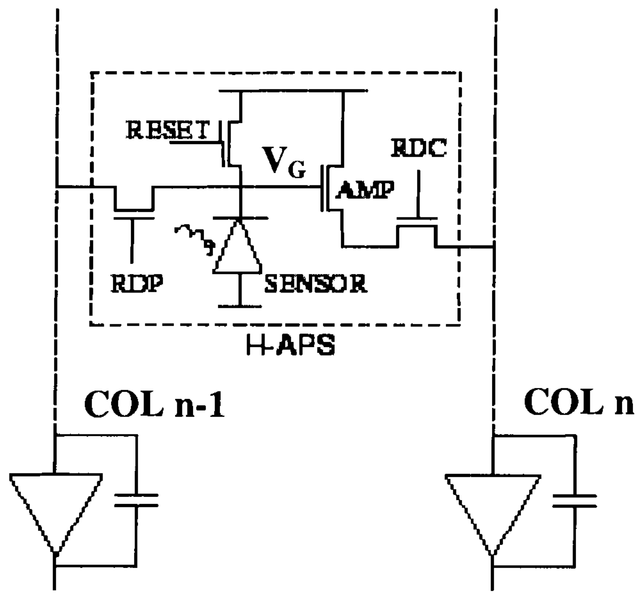


Figure 6. Hybrid APS (HAPS) pixel schematic [10]

1.4.1 Linearity and Gain

Since HAPS architecture contains both CAPS and PPS architectures, the pixel will yield a linear output for both fluoroscopy and chest radiography level signals as long as the appropriate mode is chosen. However, there is a slight difference between the charge gain, G_i, for the CAPS and HAPS pixel since capacitance at sensor node, C_{PIX} is increased due to the additional line capacitance added by the extra RDP TFT. Based on equation (5a), increasing C_{PIX} will reduce G_i, while reset noise, the largest noise component in the CAPS circuit, becomes larger with increasing pixel capacitance. However, the increase in C_{PIX} due to RDP TFT can be minimized by appropriate choice of the RDP TFT aspect ratio, and layout. For example, using a $(W/L)_{RDP} = 50\mu m/10\mu m$ introduces an additional parasitic of only 20fF which will reduce the charge gain by only 2% and still can achieve a PPS readout time of less than 3μsec for a $C_{PIX} = 1pF$, $V_{READ} = 20V$, $(V_{TO})_{RDP} = 3.2V$, $C_I = 250\ \mu F/m^2$, and $\mu = 0.8 cm^2/V.sec$ [10].

1.4.2 Transient Behaviour

Charge injection and feed-through from the additional RDP TFT can affect the steady-state voltage at the signal integration node for the HAPS pixel. When transistors turn OFF, charge injection occurs by two mechanisms. The first is due to the channel charge, which must flow out from the channel region of the transistor to the drain and source regions [10]. It can be estimated using the following equation,

$$\Delta V_G = (1/2)\frac{(V_{ON} - V_T)C_{OX}WL}{C_{PIX}} \tag{8}$$

The second error, which is typically smaller than the feed-through error is due to the overlap capacitances between the gate and the source/drain junction and can be ignored unless the gate voltage is very small or TFT dimensions are small. It can be estimated using the following equation,

$$\Delta V_G = \frac{(C_{gs})}{(C_{gs}) + C_{PIX}}(V_{ON} - V_{OFF}) \tag{9}$$

The feed-through and charge injection errors are only significant when the RESET TFT turns OFF (since the error voltage will determine the voltage at V_G on the AMP TFT during the next readout cycle). The transient error voltages are summarized in Table 2 and it should be noted that since these voltages are deterministic and repeatable, standard doubling sampling mechanisms can mitigate their effect [10].

Table 2. **Transient voltage errors at V_G for $(W/L)_{RESET}=(W/L)_{RDP}=50\mu m/10\mu m$, $(W/L)_{AMP}=280\mu m/30\mu m$, $(W/L)_{RDC}=200\mu m/10\mu m$, $V_{RESET} = 20V$, $V_{T0} = 3.2V$, $(C_{OL})_{RESET,RDP} = 0.02pF$, $(C_{OL})_{AMP} = 0.1pF$, $(C_{OL})_{RDC} = 0.08\ pF$, $C_I = 250\mu F/m^2$, $C_{PIX}=1pF$.**

Type of Error	Value
Feedthrough error when RESET TFT turns OFF	1.05V
Overlap error for RESET TFT turn OFF	0.38V
Overlap error at V_G (When RDP turns ON)	0.38V

1.4.3 Metastability

There are four TFTs in the HAPS pixel architecture and they will be affected by the bias-induced shift in TFT threshold voltage [4]. In diagnostic medical imaging applications, a factor aiding the metastability concerns is the significantly reduced TFT duty cycle. For example, in a 1000x1000 pixel real-time fluoroscopic imager, the TFTs are clocked 33μs every 33msec (i.e. a duty cycle of 0.1%). Experiments on TFT V_T shift, ΔV_T in the AMP and READ TFTs in the CAPS pixel to extract the x-ray imager lifetime at various duty cycles yielded a model that estimated a change in gm (and thus G_i) of less than 2% over 10,000 hours of operation [4]. Also, if a large V_{RESET} around +15 V is chosen, the T_{RESET} becomes relatively insensitive to ΔV_T. A similar argument applied to the RDP TFT [4], [10].

1.4.4 Noise Performance

Low frequency thermal and flicker noise for the READ and AMP TFTs, reset noise for the RESET TFT and the amplifier noise have been characterized in the past for the CAPS circuit [4]. The RDP TFT causes low frequency thermal and flicker noise during PPS operation which is expected during the normal operation of a PPS pixel. Based on models developed for the different noise sources in the CAPS pixel, [10] lists the input referred noise equivalent electrons (NEQ) for the CAPS pixel and the HAPS pixel operating in CAPS mode. The primary difference between the two pixel circuits is the additional parasitic capacitance added by the RDP TFT to C_{PIX} in the HAPS pixel and to C_{LINE}. Here, based on the TFT parameters listed in Table 2, a nominal 20fF gate-drain parasitic capacitance is estimated to be added to C_{PIX}. Also, based on a 1750 x 2150 pixel chest radiography x-ray imager and a nominal metal overlap capacitance of 10fF for a state-of-the-art a-Si TFT process, the increase in column line capacitance, C_{LINE}, is expected to be around 20pF. As shown in Table 3, the additional capacitance increases the reset noise, decreases the charge gain and due to the relationship of double sampling to uncorrelated random noise sources, increases the impact of the thermal and flicker noise components of the HAPS pixel. However, the net increase in noise is small and the HAPS pixel can be theoretically designed to give less than 1000 input referred noise electrons which is less than the quantum noise limit for digital fluoroscopy systems.

Table 3. Input referred noise of the CAPS compared to the HAPS operating in CAPS mode. Circuit parameters same as Table 2 and a nominal value of 1500 electrons is assumed for the external charge integrator noise.

	NEQ (electrons) CAPS (C_{PIX} = 0.98pF, C_{LINE} = 76pF)	NEQ HAPS (C_{PIX} = 1.0pF, C_{LINE} = 96pF)	Difference (%)
Charge Gain	27.2	26.7	1.8
Thermal	171	195	14.0
Flicker	698	751	7.6
Reset	562	568	1.1
Total Noise	913	962	5.3

To obtain the gain and noise performance shown in in Table 3, we need a pixel area of $170x170\mu m^2$ using a state-of-the-art a-Si TFT process with a minimum dimension of $10\mu m$.

1.4.5 HAPS Summary

HAPS architecture provides high dynamic range digital x-ray imaging. As discussed in the noise performance of HAPS in 1.4.4 the total input referred noise is slightly increased but this increase is within the maximum tolerable quantum noise limit for digital fluoroscopy systems. The HAPS pixel architecture is of particular relevance to the development of advanced x-ray imagers that can switch instantly between low exposure, fluoroscopic imaging and higher exposure radiographic imaging modes that can yield higher x-ray image quality as well as lower patient x-ray dosage to the patient. However, as discussed in the next chapter, further integrated and high dynamic range x-ray imager design with lower SNR may be possible if x-ray detection and analog-to-digital conversion is performed on-pixel.

CHAPTER 2: VOLTAGE CONTROLLED OSCILLATORS

The analog-to-digital (A/D) conversion, as shown in Figure 2, is performed off-panel in the existing active matrix flat panel imager (AMFPI) technology [1]. Increasing on-pixel intelligence using voltage controlled oscillator (VCO) for x-ray signal detection is investigated in this chapter. This method will help reduce the off-panel complexity and possibly provide benefits in noise and dynamic range. On-pixel frequency readout also eliminates the need for external column charge amplifiers, which can lead into signal to noise ratio (SNR) improvements. The proposed pixel architecture including the VCO and the column readout is depicted in Figure 7. It is assumed that x-rays are detected by either direct or indirect detection methods as explained in chapter 1 at node V_{pix}, and the VCO converts this voltage to frequency. This chapter will discuss various VCO circuits and determines a suitable circuit for medical x-ray imaging.

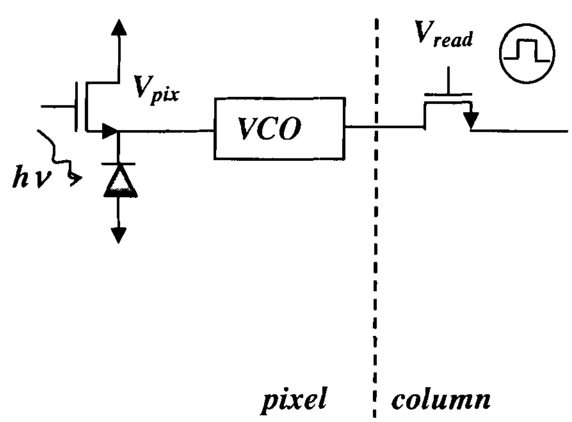


Figure 7. Pixel architecture and column readout

2.1 Voltage Controlled Oscillator Categories

The role of a VCO here is to read the input voltage, which is proportional to the amount of x-ray radiation detected per pixel, and convert it to frequency. A frequency counter converts this frequency to digital format. As shown in Figure 8, VCOs can be categorized by the method of oscillation into resonator-based oscillator, waveform-based oscillator (using logic gates), and OP Amp-RC oscillators. Primary examples of each category are shown below [15].

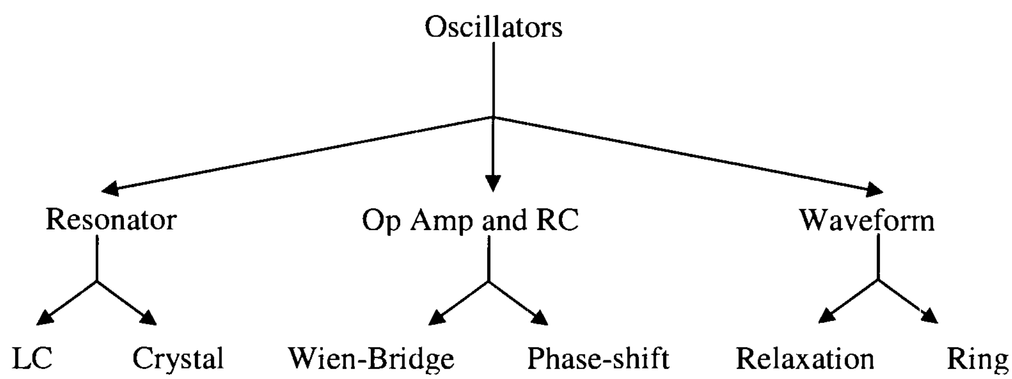


Figure 8. Various Voltage Controlled Oscillators

2.2 Oscillator Design Theory

An oscillator is basically a circuit used for the purpose of generating a signal or a clock. Many types of oscillators exist, but they all operate according to the same basic principle: an oscillator always employs a sensitive amplifier whose output is fed back to the input, in phase. Thus, the signal regenerates and sustains itself i.e. feedback is required for oscillations to produce periodic or AC output with DC power as the only input. We know that with negative feedback, the equation for closed-loop gain in terms of open-loop gain will be,

$$A_{CL}(j\omega) = A_{OL}(j\omega)/(1+\beta(j\omega).A_{OL}(j\omega)) \tag{10}$$

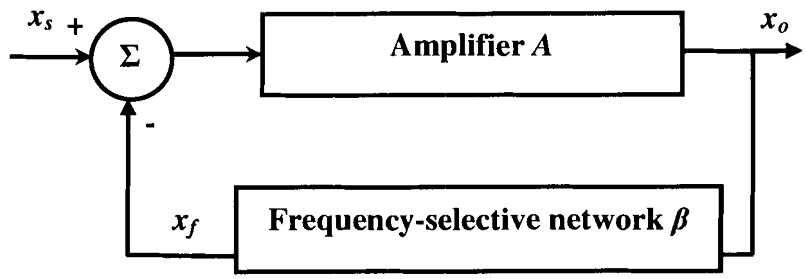


Figure 9. Feedback circuit block diagram

Here, the loop gain $L(j\omega) = \beta(j\omega).A_{OL}(j\omega)$ is a complex number represented in polar form as,

$$L(j\omega) = \beta(j\omega).A_{OL}(j\omega) = |\beta(j\omega).A_{OL}(j\omega)|e^{j\varphi(w)} \tag{11}$$

The frequency at which the loop phase angle, $\phi(w)$ becomes 180° the loop gain becomes a real and negative number and if the loop gain at this frequency is less than unity, then $A_{CL}(j\omega)$ will be greater than $A_{OL}(j\omega)$. On the other hand if at 180° phase shift, the loop gain is equal to unity, it follows that $A_{CL}(j\omega)$ will be infinity. In other words, there will be an output for zero input and, therefore, oscillations start [14].

2.3 VCO Architecture Comparison

Ideally, in designing a VCO we want to have, low noise, low power consumption, wide tuning range, small area, and high frequency of oscillations [17]. Though, as will be discussed below, it is unlikely that either the ring VCO (ring oscillator VCO) or LCVCO

(LC tank VCO) topologies can meet all of these conditions. Through a comparison of ring VCO and LCVCO, the following advantages and disadvantages may be formulated.

Ring VCO advantages:

- Highly integrated i.e. no need for inductor design on-pixel
- Low power consumption
- Small area consumption
- Wide tuning range

Ring VCO disadvantages:

- As frequency increases phase noise degrades

LCVCO advantages:

- Outstanding phase noise at high frequency

LCVCO disadvantages:

- Contains an inductor and a varactor (variable capacitor) which are large area components

2.4 Selection of a VCO circuit for TFT based medical imaging

In this section, we will discuss the various oscillators that were considered for the VCO design. First, referring to the three main categories of oscillators as shown in Figure 8, it should be noted that Op Amp-RC oscillators were not considered here due to the fact that a-Si based TFTs have low mobility, low on-current, and low gain; thus are not qualified for Op Amp design. A piezoelectric crystal, such as quartz, exhibits electromechanical-resonance characteristics that are very stable (with time and temperature) and highly selective (high Q). Crystal oscillators were not considered either since their oscillation frequency is fixed (not controllable for VCO application). The only suitable oscillators for x-ray imaging are therefore resonator oscillators and waveform oscillators as discussed in the following chapters.

CHAPTER 3: LC TANK OSCILLATORS

LC tank oscillators are reported to have outstanding phase noise performance at high frequencies [20] but their disadvantages include space requirements. This chapter covers our studies on application of LC oscillators in TFT based VCOs. An introduction on LC oscillators is given here.

An LC oscillator can be thought of as two 1-port networks connected together. One 1-port represents the frequency selective tank where oscillations occur. But the oscillations die through RI^2 losses in the circuit (through g_{tank} as shown below). If energy could be pumped back into the tank as fast as it were being dissipated, it would ring forever and this is the basic idea of an LC resonant oscillator. Therefore, the other 1-port represents the active circuit (represented with g_{active}) that cancels the losses in the tank [20].

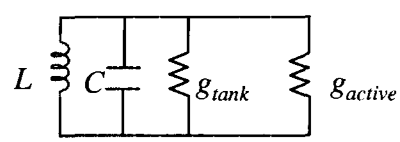


Figure 10. LC oscillator block diagram

In this view of LC oscillators we can have oscillations when both of the following conditions are satisfied:

- The negative conductance of the active network cancels out the positive conductance (loss) of the tank
- The closed loop gain has zero phase-shift

Therefore, the closed loop gain should be real with a magnitude greater than or equal to unity according to oscillation condition explained in chapter 2. Two commonly used LC oscillator circuits are Colpitts and Hartley oscillators as shown in Figure 11.

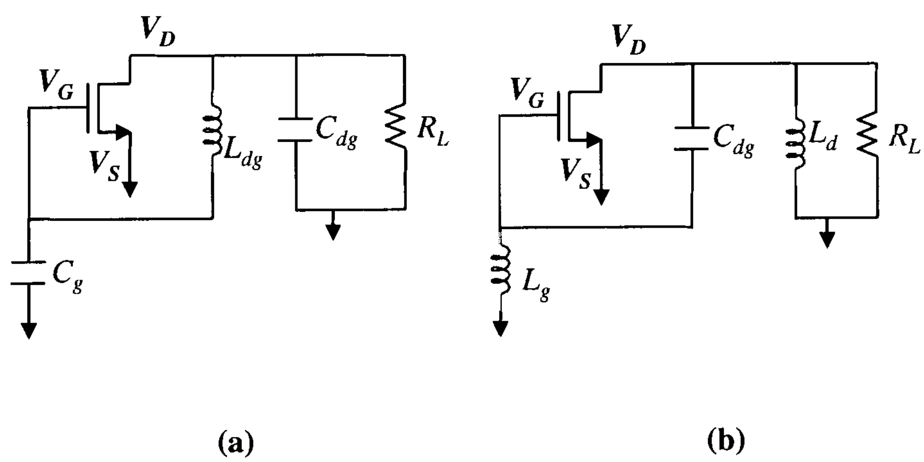


Figure 11. (a) Colpitts oscillator and (b) Hartley oscillator

The circuit performance of Hartley and Colpitts oscillators are quite similar in terms of oscillation frequency and LC sizes. Therefore, we will explain Hartley oscillator performance here to generally explore feasibility of LC oscillators in TFT technology.

3.1 Small signal analysis of Hartley oscillator

To analyze the Hartley oscillator circuit since the oscillation frequency is sufficiently low and the TFT parasitic capacitances are small, they can be neglected in our analysis. The frequency of oscillation can therefore be determined by the resonance frequency of the parallel-tuned circuit (LC tank) as explained below. Referring to Figure 12, the small signal analysis is performed as following where R_L includes the TFT output resistance.

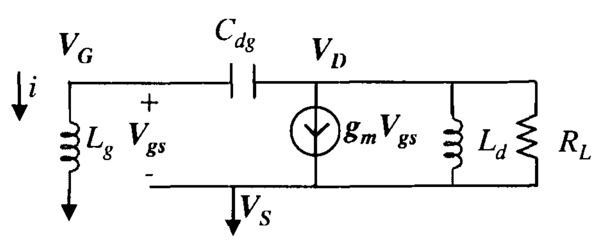


Figure 12. Small signal analysis of Hartley oscillator

To analyse this circuit for oscillations, one method is to find the loop gain and set the loop gain to greater than unity and the phase shift to zero. Another method [14] is to perform a nodal analysis at node V_D which will result in the circuit governing equation as following,

$$1/sL_g + g_m + (sL_d + R_L)(1 + 1/s^2 L_g C_{dg})/sL_d R_L = 0 \quad (12)$$

For oscillations to start, both the real and imaginary parts in the governing equation (12) should be equal to zero. Replacing s with $j\omega$ and equating the imaginary part to zero, the frequency of oscillation is found to be,

$$\omega_0 = 1/\sqrt{(L_d + L_g)C_{dg}} \quad (13)$$

And for the oscillations to start the real part should be greater than zero which results in,

$$g_m > L_d /(L_g . R_L) \tag{14}$$

Equation (14) has this physical interpretation: for oscillations to start the gain from gate to drain ($g_m R_L$) must be greater than the voltage ratio provided by inductive divider which will result in a gain of greater than unity for the oscillation condition.

3.2 Hartley oscillator simulation results in a-Si technology

The Hartley oscillator circuit including biasing is shown in Figure 13. The design feasibility here includes space calculations for inductors, and capacitors, and the required TFT sizes.

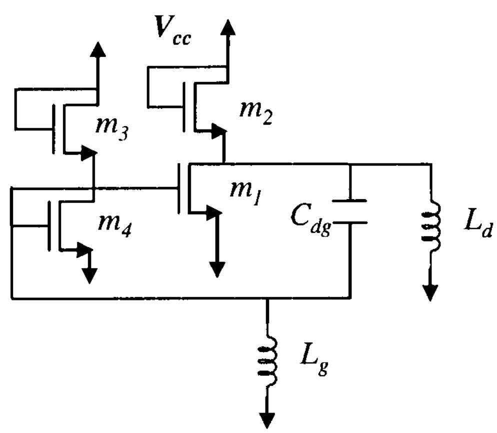


Figure 13. Hartley oscillator configuration including biasing

We first start with design for pixel space limitations of about 200x200μm^2 and calculate frequency of oscillations. Based on equation (13) frequency of oscillation is inversely proportional with L_d, L_g, C_{dg}. Since TFT unity gain frequency is in the 1MHz neighbourhood, therefore starting with a C_{dg}=1.6pF will require L_d=L_g=7500μm for 1MHz oscillation frequency.

For V_{cc}=30V, m_1=100μm/5μm, m_2=m_3=m_4=10μm/5μm the circuit will oscillate at a frequency of 980 kHz. The major problem with this circuit, however, is the large size of inductors with high quality factor. We used ASITIC software [21] for simulating planar inductors and calculating their quality factor. In the next section we determine the maximum inductor size that can fit in the 200x200μm^2 pixel area.

3.3 Inductor design

The following figure depicts a one layer planar spiral inductor with four sides. Planar thin film inductors can have different design parameters which are in the form of spiral with four or more number of sides. Also, number of layers, number of turns, area, line width, line pitch as well as line thickness should be considered in designing planar inductors. As can be expected, we need large inductors with low losses.

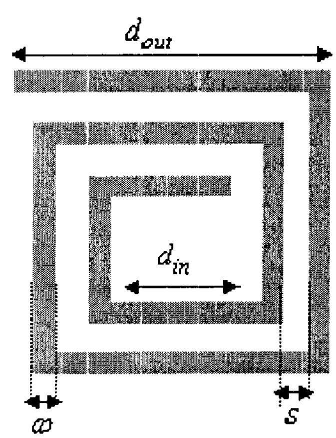


Figure 14. Planar inductor

In reality, the inductor has parasitic components other than the series resistance associated with it such as parasitic capacitances and Eddy current. Capacitance to grounded substrate sets inductor self-resonance frequency. Semiconductor materials are non-magnetic and the flux uniformly surrounds the inductor which penetrates into the substrate. This flux induces Eddy currents in the substrate, which dissipates in the form of V^2/R. Eddy currents also lower self-inductance and need to be taken into account when designing inductors [22]. A vertical-stacked planar inductor structure can produce inductors in a small area and high quality factor. Active research has been focusing on achieving high inductance value (L) and high quality factor (Q) IC inductors, typically using stacked planar structures or MEMS techniques. However, the large inductor sizes, typically a few hundred by a few hundred microns, and non-standard-process structures, result in large silicon consumption, intolerable capacitive effect and increased costs, making them unrealistic to design. Here this feasibility can be studied by modelling the inductor. Using ASITIC software simulator we can model the multi-layer planar inductor considering the parasitics associated with the inductor, with an equivalent as following [23].

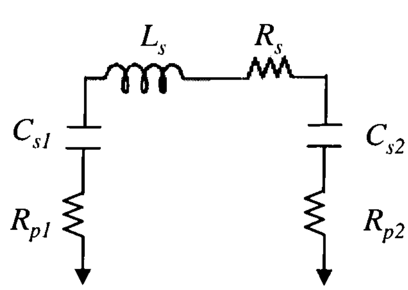


Figure 15. Inductor model

The general form of the one-layer planar spiral inductor based on the Wheeler formula is as following,

$$L = k_1 \mu_0 . n^2 d_{avg} / (1 + k_2 d_{avg}) \tag{14}$$

where μ_0 is the permeability, n is the number of turns , ω is the turn width, s is the turn spacing , k_1 and k_2 are layout dependent coefficients, d_{out} and d_{in} are the outer and inner diameters respectively, $d_{avg} = (d_{in} + d_{out})/2$ is the average diameter, and $\rho = (d_{in} - d_{out})/(d_{in} + d_{out})$ is the fill ratio [23].

Based on ASITIC simulations, two inductors were simulated with 200μm outer diameter, metal width=10μm, metal spacing=1μm, and number of turns n=9. The following is a graphical representation of the fabrication file used in ASITIC.

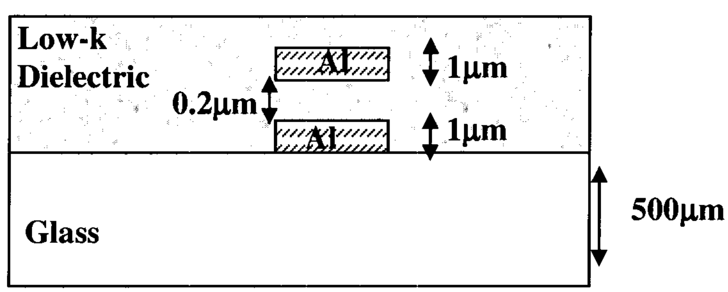


Figure 16. Fabrication file used in ASITIC simulations

The following table is the results for one-layer and double layer square inductors.

Table 4. Comparison between one-layer and double layer inductors

	Inductance	Parasitic series resistance
1-layer square inductor	7nH	10Ω
2-layer square inductor	26nH	19Ω

Based on the above results we observed that the inductance grows quadratically with the number of layers and therefore the two-layer inductor results in a more compact design. For the pixel area limitations of $200x200\mu m^2$ the maximum inductance was in the range of 30nH-50nH. We fabricated one-layer planar spiral inductors in-house to investigate the quality factor of Aluminium sputtered inductors.

3.4 Inductor Fabrication

The first mask for building planar spiral inductors consisted of Mylar masks with the minimum resolution of $50\mu m$. The inductors were one-layer four-sided and with various number of turns and diameters. The process for building the planar spiral inductors consisted of Aluminium deposition on Corning glass wafer and therefore the inductor dielectric is air in this case.

The Aluminium deposition had the following conditions:

Base pressure $1.5(10^{-6})$Torr

Sputtering pressure 3.0 mTorr

Ar flow 5.7 sccm

Substrate bias 70 V

DC current 0.26 A

Power 100 W

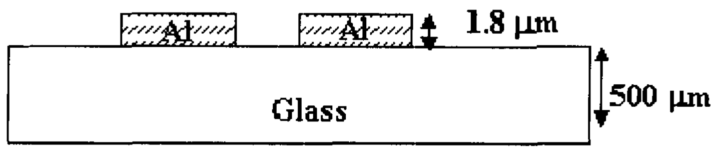


Figure 17. Aluminium inductor on glass

The results of the 1.8μm deposition are shown below. The resistively of Aluminium film in the case of 1.8μm was measured to be around 94mΩ/sq.

Table 5. Various sizes of one-layer, four-sided (square) inductors

Inductance measured (nH)	Inductance calculated (nH)	Inductance error (%)	R_{series} (Ω)	Outer diameter (μm)	Number of turns
1161	1238	-6.6	305.2	10000	17
159	165.6	-4.15	71.3	5000	8
23	23.66	-2.87	17.0	2500	4
5.7	5.672	0.49	6.1	1500	2

As can be observed from the above values, the measurement results are in proximity of expected values by ASITIC simulator. The small errors are mostly due to the actual sizes of inductor dimensions due to error originated from Mylar mask prints. Better results are possible by using more accurate mask prints, e.g. chrome on glass. To characterize the impact of the series resistance the quality factor (Q) is commonly used.

Q is the ratio of an inductor's reactance to its series resistance. For tuning purposes, this ratio should be as high as possible. From the definition of quality factor as following,

$$Q = E_{stored} / E_{dissipated} \mid_{percycle} \tag{16}$$

the quality factor Q can be calculated as following [24],

$$Q = \omega_0 L / R_s \tag{17}$$

where R_s is the inductor parasitic series resistance.

For the above inductances the maximum achievable quality factor at 500MHz was 12. Higher quality factors up to 20 (required for LC oscillators) can be achieved by designing double layer planar inductors [24]. This is due to the fact that inductance increases quadratically with number of layers but series resistance increases only linearly in that case [25].

3.5 LCVCO Summary

Our fabrication results showed that it is possible to fabricate inductors with suitable quality factor ~12 for designing LC oscillators. As was shown in Table 4, it is possible to design inductors of up to~30nH range which can fit in the pixel are using double layer technology. However, the oscillation frequency for this range of inductance will be in the ~500MHz which is well beyond the a-Si TFT unity gain frequency. On the other hand, high frequencies are achievable in poly silicon TFTs and can be investigated further for VCO design which is beyond the topic of this research. Further research is then required for frequency sensitivity analysis, phase noise, and metastability calculations.

Designing LC oscillator suitable for a-Si TFT speed (~1MHz) requires inductors in the range of >1000μH which will not meet the pixel area limitations of 200x200μm^2. For example, AIM Spice simulations for Hartley oscillator circuit in Figure 13 with TFT dimensions of m_1= m_2=m_3 =m_4=10μm/5μm, C_{dg}=1.6pF, and inductors of ~3mH resulted in frequency of oscillation of 1.3MHz. The area requirement for such size inductors is estimated ~35mm^2 based on planar spiral inductance measurement methods in [13]. Although too large for a-Si x-ray imaging, there maybe other applications for double layer inductors which can be easily adopted in TFT technology.

CHAPTER 4: WAVEFORM OSCILLATORS

Ring and relaxation oscillators fall under the waveform oscillators' category which will be discussed in this chapter. A background on the theory of operation of each oscillator is provided followed by circuit simulations using AIM Spice Software based on a-Si TFT Model ASIA2 (level 15) with parameters from our in-house TFT fabrication results. Circuit fabrication results are then compared with the expected simulation results. First, oscillation frequency requirements for suitable x-ray imaging are given in 4.1 followed by the maximum operation frequency of TFT based circuits in 4.2.

4.1 Oscillation frequency requirements

In this section we study the factors that control f_{osc} and calculate its maximum for better dynamic range performance while keeping the circuit dimensions at minimum due to area restrictions. As was described in chapter 1, in various imaging modalities, the pixel voltage can vary from 0.4mV to 8V. Since for real-time imaging a frequency of 30Hz (T_{frame} =33 msec) is required, for a 1000x1000 pixel array, which is read one row at a time, the read time T_o will be,

$$T_0 = (1/1000) \times (0.33 m\sec) = 33 \mu\sec \tag{18}$$

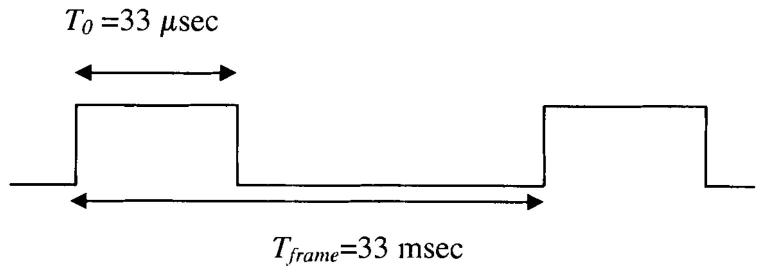


Figure 18. Readout time in a 0.1% duty cycle

The following table represents the dynamic range provided by increasing f_{osc} for 30Hz and 10Hz frame rates.

Table 6. Number of counts in 33μsec and 99μsec for a 1000x1000 pixel array

f_{osc}	T_{osc}	# of counts in T_0=33 μsec (30Hz frame rate)	# of counts in T_0= 99 μsec (10Hz frame rate)
10KHz	100μsec	N/A	1
100KHz	10μsec	3.3	9.9
500KHz	2μsec	16.5	49.5
1MHz	1μsec	33	99

As can be expected, the oscillator f_{osc} should be high enough to be detected in the T_0 read time window. From Table 6 we can see that the higher the frame rate, the smaller the read time, T_0, and the higher the required f_{osc}. Higher f_{osc} necessitates a more sensitive detection system, which will result in more accurate pixel A/D conversion. However, frequency operation of TFTs is limited due to low mobility of a-Si technology. Therefore, an optimization of the frequency of oscillation for the detection system in a-Si technology should be done. The following section discusses maximum operation frequency of our TFTs.

4.2 TFT maximum frequency of operation (f_T)

Unity gain frequency (f_T) is the frequency at which the short-circuit current gain of the current source configuration becomes unity. In the following figure where the TFT frequency response of a TFT is shown, we find f_T as the point where current $Gain = \frac{i_{Vcc}}{i_{Vin}}$ is unity [14].

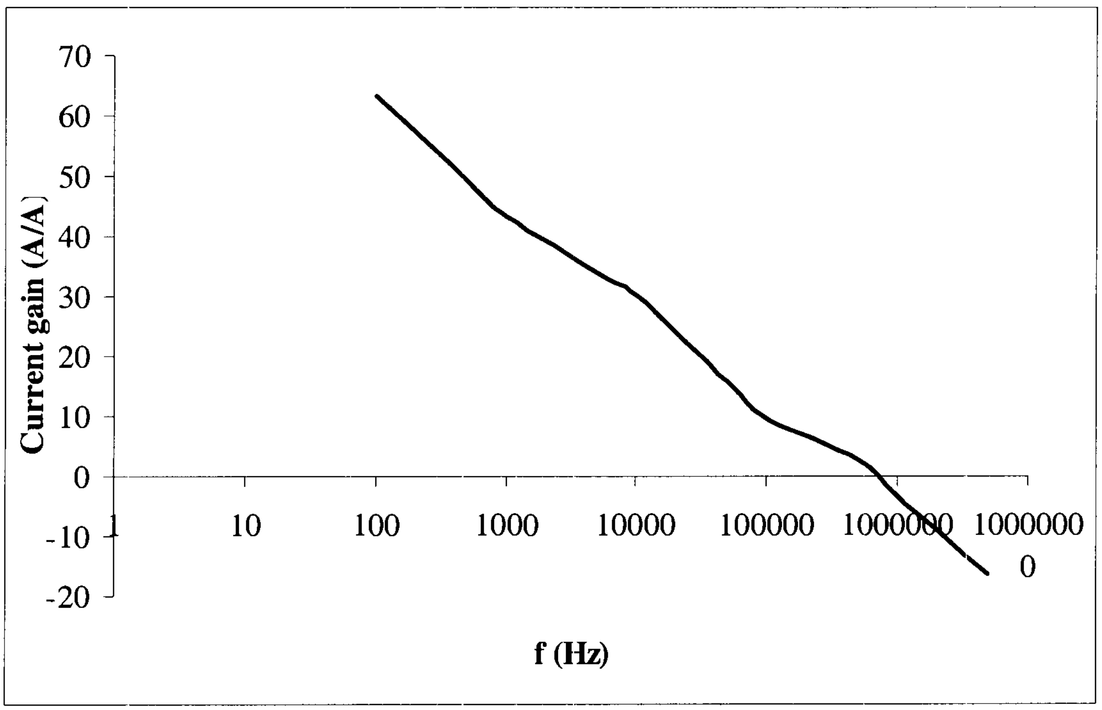


Figure 19. TFT frequency response based on W/L=100μm/5μm, V_T=5V, t_{ox}=350nm.

From the above graph, f_T is around 700kHz; therefore, the range of frequencies that we can choose for our circuit optimization should be below this frequency. The formula for f_T can be approximated by [14],

$$f_T = \frac{\mu(V_{GS} - V_T)}{2\pi L^2} \tag{19}$$

From the above formula we can observe that increasing f_T is possible by decreasing the TFT channel length (L). Higher frequencies of >1MHz can be designed using channel lengths of 2μm [15]. In the following sections, we study relaxation and ring oscillator and select the suitable circuit based on oscillation frequency performance.

4.3 Relaxation oscillator

One common type of waveform oscillators is the relaxation oscillator which is an astable circuit composed of an RC network combined with negative feedback. The circuit configuration is shown in the following diagram.

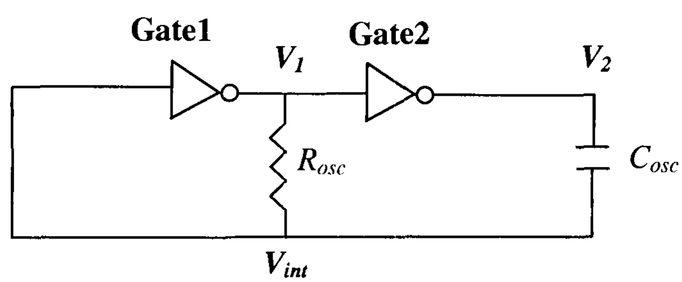


Figure 20. Block diagram of relaxation oscillator

Assuming that the inverters have a switching threshold $V_M = V_{DD}/2$, the gate delays are negligibly small with respect to the RC time-constant, and the output voltage of the gates change instantaneously when the input voltage crosses V_M, the following will result [16].

At time t=0, we assume V_{int} is rising. When crossing V_M, it causes gate1 and gate2 to toggle to low and high respectively. The abrupt change in V_2 is capacitively coupled to V_{int} node, to jump from V_M to $V_M+V_{DD}=3V_{DD}/2$ all of which occurs at time t=0. The voltage at node V_{int} then starts to decay exponentially towards ground with an RC time constant. After some time, it crosses V_M again, this time in the falling direction, toggling gates 1 and 2. V_1 and V_2 go to high and low respectively and V_{int} jumps to $-V_{DD}/2$ due to the capacitor C_{osc}. V_{int} starts to decay towards V_{DD} with a time-constant RC until it reaches V_M once more and the complete cycle is repeated again. As explained in [16] this circuit oscillates with a period of T_{osc} as below,

$$T_{osc} = 2(\log 3)R_{osc}C_{osc} \tag{20}$$

4.3.1 Relaxation oscillator design

For space saving reasons, active load TFTs are used for inverters' load transistors as well as for R_{osc} in place of resistive load. Circuit simulations for V_T = 5V, μ_{band} = 0.6cm^2/V.s and circuit dimensions of $m_{load(1,2)}$ =350μm/5μm, $m_{drive(1,2)}$ =550μm/5μm, m_{osc}=50μm/5μm, C_{osc}=2pF, and V_{cc} =30V resulted in f_{osc}= 25 kHz.

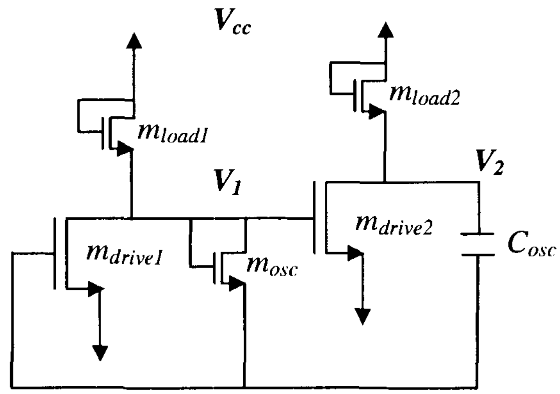


Figure 21. Circuit configuration of relaxation oscillator

For this circuit configuration, the formula for frequency of oscillations based on (18) will become,

$$f_{osc} = \frac{g_{m-osc}}{2(\log 3)C_p} \tag{21}$$

Where, $g_{m\text{-}osc}$ is the transconductance of m_{osc} and C_p is the total capacitance seen at V_2 node which includes the parasitic capacitances of the TFTs. Increasing frequency of oscillations based on the above formula can be achieved by increasing $g_{m\text{-}osc}$ which can be achieved by decreasing C_p which means lower TFT dimensions. But circuit area and f_{osc} still need further optimization. However, the main problem with this circuit is its low frequency of oscillation which results in low circuit sensitivity. Also, relaxation oscillators generally suffer from low frequency stability and higher phase noise [19]. In this work, we did not further pursue relaxation oscillators due to their low oscillation frequency in a-Si technology and decided to investigate ring oscillators as shown in the next section.

4.4 Ring oscillator

The ring oscillator configuration is formed by connecting an odd number of inverter stages in a loop. Although usually at least five inverters are used to ensure oscillations will start, it is possible to start oscillations with a minimum of three inverters. Smaller number of inverters results in higher oscillation frequency as discussed later in this chapter. The rising edge at node V_1 in Figure 22 propagates through gates V_2 and V_3 to return inverted after a delay of $3t_p$. This falling edge then propagates and returns with the original (rising) polarity after another $6t_p$ interval. It follows that the circuit oscillates with a period of $6t_p$. The feedback is negative and creates an initial bias equilibrium at the transition voltage for the gates. For a general case of N stages, 180° of phase shift is provided by the chain and sufficient gain (the overall gain >1) should be provided at oscillation frequency f_{osc}. This criterion means that the gain of each stage should be greater than 1. Similar to relaxation oscillator, inverter stages can be designed with either resistive or active loads. The following figure is a ring oscillator using resistive loads.

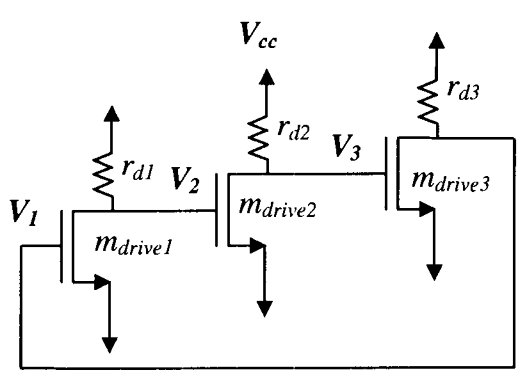


Figure 22. Ring oscillator with resistor loads

As will be shown in 4.4.5 high oscillation frequencies of ~200 kHz are achievable using ring oscillator circuit simulations. Therefore, we decided to pursue the ring oscillator design and fabrication as the focus of this thesis.

As shown in Figure 22, three inverter stages are used and each inverter stage is realized using an n-channel drive TFT and a load resistor as in Figure 23. At each inverter stage, higher load resistance is required to increase the gain according to,

$$Gain = V_o / V_{in} = g_m (r_o \parallel r_d) \tag{22}$$

For simplicity r_o, which is in the GΩ range, can be ignored compared to r_d. Therefore, the gain requirement will be as following,

$$Gain \cong g_m r_d \geq 1 \tag{23}$$

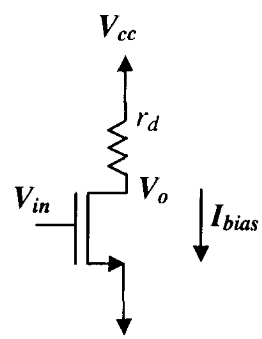


Figure 23. Inverter stage

Here we present an example of space requirements for ring oscillator with resistive load. In our fabrication, we used inverters with TFT dimensions of W/L=300μm/50μm and overlap= 30μm, which theoretically results in $g_m = \partial i_d / \partial V_g \big|_{V_g=10V}$ =3.15x10^{-7} A/V at V_{cc}=25V, for I_{bias}=0.8μA. Therefore, the inverter requires an r_d of greater than 3.17MΩ to get a gain of greater than unity according to equation (22). Thus, to ensure oscillations will start, we take r_d=10 MΩ. An example of a simulated inverter response with r_d of 10MΩ is shown below where we can observe the fully inverted V_o compared with V_{in} and the negligible time delay between the two signals.

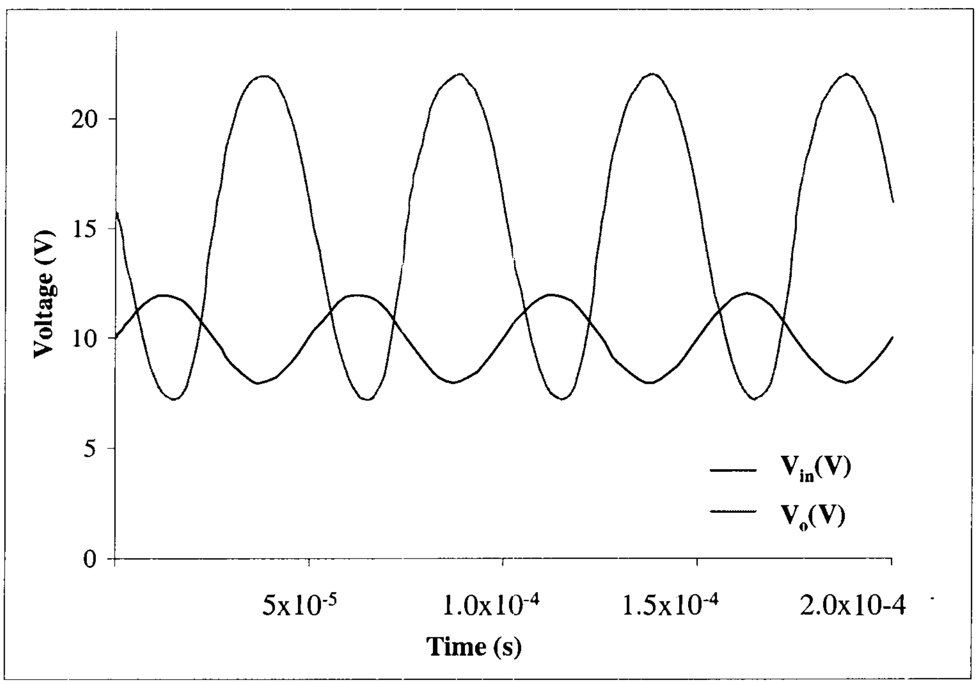


Figure 24. Inverter response with r_d =10MΩ

For the case of a TFT with dimensions W/L=300μm/50μm and r_d =10MΩ. The area for the 10MΩ resistor is calculated from the following formula where W,L, t are width, length, and thickness of the resistor,

$$r_d = \rho.L / A = \rho.L / (W.t) \tag{24}$$

The resistor is fabricated using PECVD n+ deposition which has a conductance in the range of 0.01S/cm (or resistivity of 10Ω.m) [26]. For the 10MΩ resistor, if we choose an n+ layer of 50nm thickness, according to our fabrication process, a width of 1mm is required which will be impractical. Comparing this result with the case where the n+ resistance is replaced with an active saturated TFT load, described in the next section, leads us to the preferred design.

Using active TFT loads for inverter stages, ring oscillator circuit will be as shown in Figure 25. The frequency of oscillation is a function of biasing as will be shown later but since controlling this frequency is required for our application (x-ray detection), an external control node $V_{pix\text{-}ctrl}$ is added here. V_{out} is the output node.

The size of the load TFTs is defined by the following requirements:

1. The biasing should be I_d= 1 μA, V_{cc}=25V, where V_T=5V.
2. Voltage gain can be calculated as[5], $Gain = |V_o / V_{in}| = \sqrt{\frac{(W/L)_{drive}}{(W/L)_{load}}} > 1$

According to first requirement and the simplified current formula for saturated TFTs as following, where μ is mobility, C_{ox} is the gate capacitance, and W/L is drive TFT dimensions,

$$I_d = (1/2).\mu.C_{OX}.(W/L)_{drive}.(V_{GS} - V_T)^2 \quad (25)$$

Starting with $(W/L)_{drive}$=300μm /50μm, for m_{drive} minimum dimensions of W/L of 50μm/50μm will satisfy both conditions. These dimensions are chosen for ease of fabrication due to in-house equipment limitations. Therefore, active TFT loads option

[5] Simplified gain formula for MOSFET based inverter [14].

will result in 20 times area savings and hence is the preferred choice. The only disadvantage, however, will be the possibility of increased metastability effect (since more TFTs are used). This effect will be discussed later in this chapter in 4.4.7.

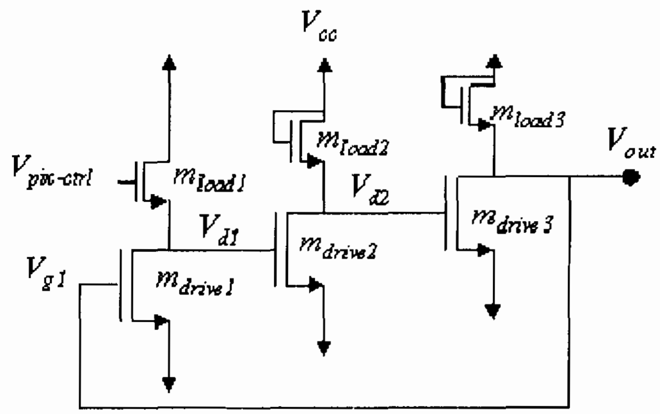


Figure 25. Ring oscillator with active loads

4.4.1 Propagation delay (t_p)

Calculating propagation delay, t_p is important in our design since the ring oscillator frequency is inversely proportional to this term [15],

$$f_{osc} = 1/(2.N.t_p) \tag{26}$$

where N is an odd number which is the number of inverter stages. The minimum N depends on f_T (unity gain frequency) and t_p according to the TFT technology as will be explained later in this chapter. Larger propagation delay (t_p) is expected due to the additional parasitic capacitances of the TFT loads compared to the case where resistor loads were used. A single stage of the inverter is shown below in Figure 26 and dynamic behaviour of this circuit is discussed in the next section in order to discuss propagation delay and frequency of oscillation of the ring oscillator circuit.

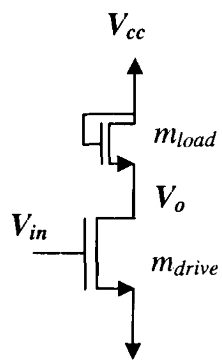


Figure 26. Inverter stage with active load

In addition to setting the frequency of oscillation, the propagation delay, t_p also controls the amplitude of oscillations according to,

$$V_{osc} = I_{bias} . t_p / C_p \tag{27}$$

The following figure shows the voltage response of the first inverter cascaded with the next 2 stages for $(W/L)_{load}$=50μm/50μm, $(W/L)_{drive}$=300μm/50μm, overlap=30μm, and V_{cc}=25V connected to a sine input voltage. As can be observed the V_o (shown as V_{d1} here) has a delay with respect to V_{in} which is referred to as $t_p \cong 7.9\mu$sec here. And $f_{osc}=1/6t_p$=21kHz which is good estimation for the f_{osc}=20kHz of the ring oscillator based on AIM Spice simulations.

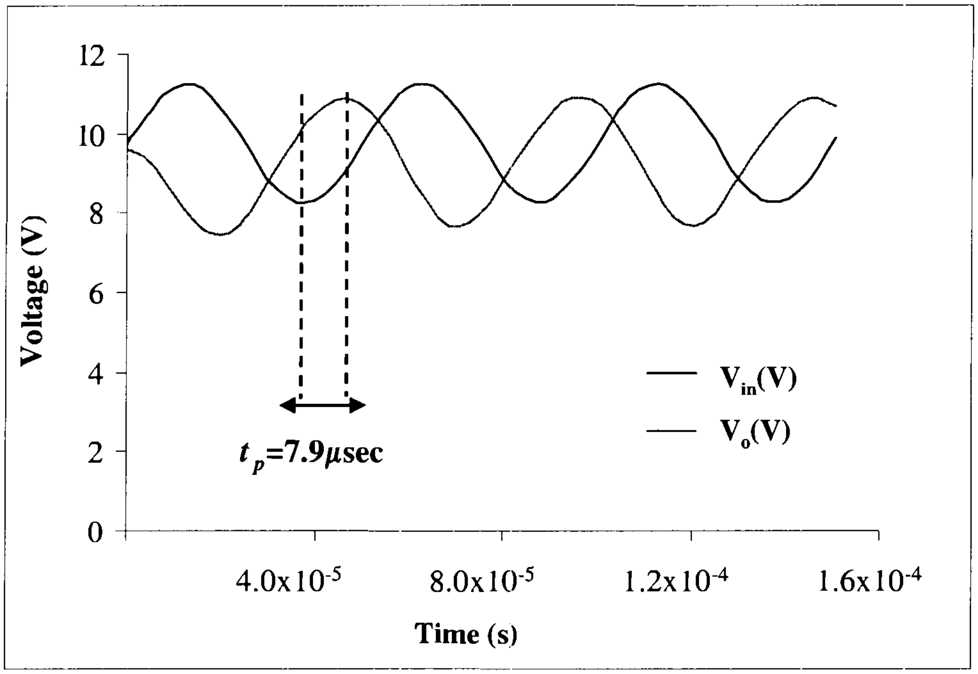


Figure 27. Inverter stage voltage response (sine input)

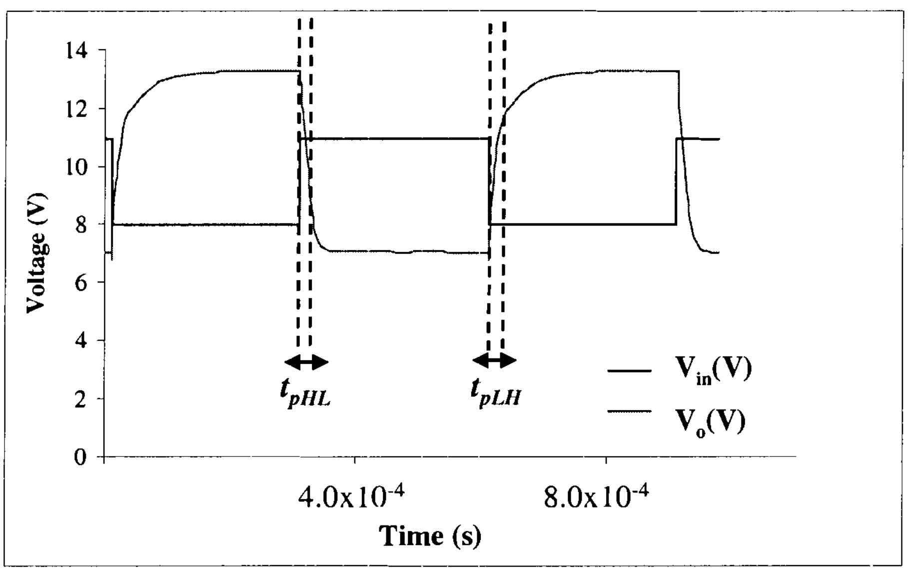
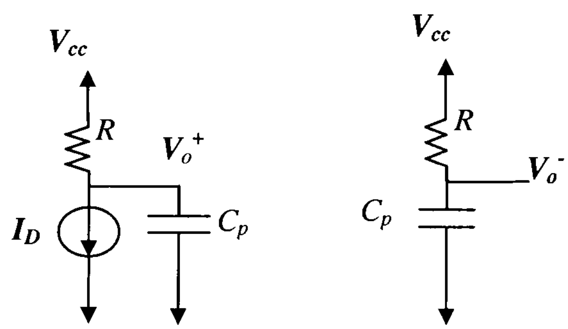


Figure 28. Inverter stage voltage response (switch input)

The value of t_p is the average of rise time (t_{pLH}) and fall time (t_{pHL}) and small signal analysis of each stage is required to calculate its value. During the low input cycle, the circuit looks like Figure 29 (a) and the capacitance C_p (the parasitic capacitance at the output stage) is charged up to $V_o = V_{cc} - R.I_D$. During the high input cycle Figure 29(b) C_p is discharged to $V_o = V_{cc} - V_T$. The overshoots observed at the transitions are due to transient behaviour of TFTs from channel feedthrough or overlap capacitances [4].



(a) Positive cycle **(b) Negative cycle**

Figure 29. Inverter stage small signal analysis

To find t_p for simple hand calculations we require calculating the effective C_p at the output of each stage in the cascaded inverters. $C_{gd\text{-}drive}$, $C_{gs\text{-}drive}$, and $C_{gs\text{-}load}$ refer to the overlap parasitic capacitances of m_{load} and m_{drive} in Figure 26. C_p is estimated by,

$$C_p \cong (3/2)C_{gs-drive} + C_{gs-load} \tag{28}$$

Here, each overlap capacitance is estimated by,

$$C_{ov} = (6.5).\varepsilon_0.W.ov/t_{ox} \tag{29}$$

For $W_{gd\text{-}drive}$=300μm, $W_{gd\text{-}load}$=50μm, t_{ox} =350nm, overlap=30μm,

$C_{gd\text{-}drive}$= $C_{gs\text{-}drive}$= is 1.48pF and $C_{gs\text{-}load}$= $C_{gd\text{-}load}$=0.24pF and therefore C_p will be 2.5pF.

Time delay t_{pHL} is estimated as the time it takes for the output to reach from maximum to 50% of its minimum and similarly for t_{pLH}. The charge-discharge time for an RC network from maximum to 50% is $t_{pHL} = 0.69RC$ [27]. Assuming both rise and fall times are equal, propagation delay $t_p = t_{pHL}\, t_{pLH}$.

$$t_p = \frac{0.69C_P}{g_{m-load}} \tag{30}$$

When V_{cc}=25V the load transconductance, $g_{m-load}=3.3\times10^{-7}$A/V which results in t_p=5.2μsec, which is a close estimation for the propagation delay observed in Figure 27. Optimization of f_{osc} will be discussed in explained in 4.4.5. The amplitude of oscillations is expected to be 5V according to (25) which is a close estimation for the AIM Spice results of 3V where I_{bias}=2.3μA.

4.4.2 Ring oscillator frequency-voltage gain

From oscillation frequency formula (24) and propagation delay formula (25) we can calculate the ring oscillator frequency-voltage gain as following.

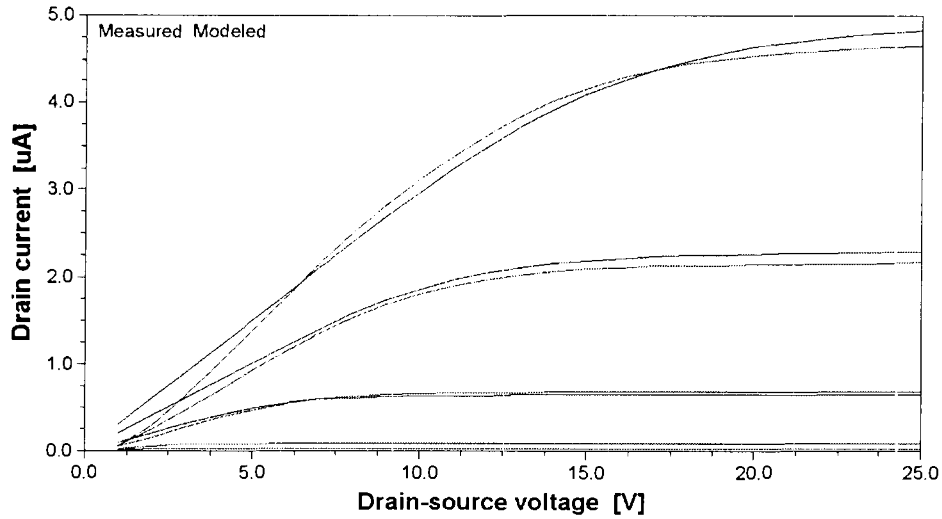
$$\Delta f_{osc} = \frac{\Delta g_{m-load}}{6\times 0.69C_P} = \frac{\mu.C_{OX}.(W/L)_{load}.\Delta V_{pix-ctrl}}{4.14C_P} \tag{31}$$

4.4.3 In-house TFT results

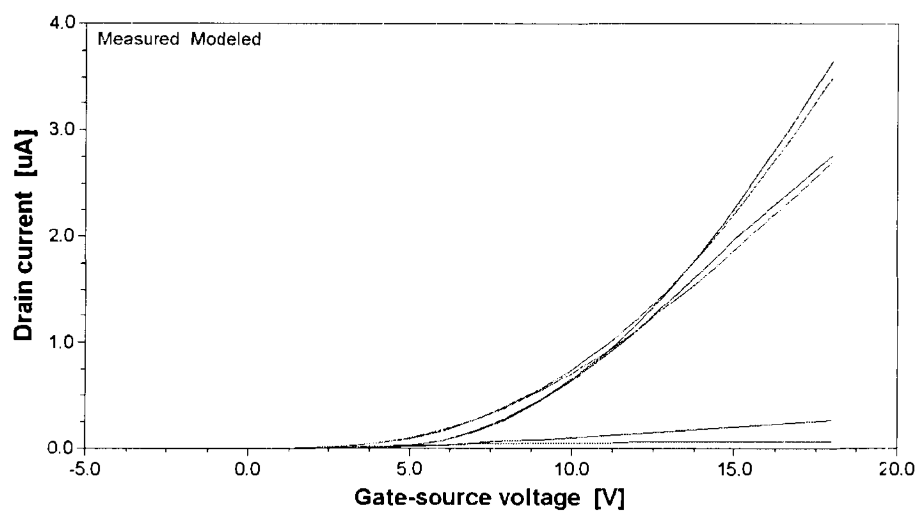
Since our design was for in-house fabrication, initially we used our previously in-house fabricated TFT characteristics for designing circuits. These characteristics were used as input files in AIM Extract simulator to obtain the TFT parameters for circuit simulations. And the process parameters were as following.

GAMMA=0.235, SIGMA0=2.5×10^{-14}A, LABDA= 0.001, M=5, VGSL=8V, VDSL=8V, IOL=3×10^{-14}A, VT0=5V, ALPHASAT=1, VAA=10000000V, ALPHA=0, V0=0.2V, VFB=-4V.

The following two figures demonstrate the extraction of modelled parameters from the measured values; close match between the measured and modelled graphs shows adequate parameter extraction.



(a)



(b)

Figure 30. TFT parameter extraction

4.4.4 Circuit design for in-house fabrication

In our in-house TFT fabrication we were able to achieve a mobility of μ=0.6cm^2/V.s, and for the ring oscillator we started with a channel length of 50μm for fabrication flexibility as mentioned earlier. Two ring oscillators with different aspect ratios were simulated and fabricated. Each configuration was also built with two different gate overlap values to observe its effect on f_{osc}. As can be observed from Table 7, decreasing overlap decreases f_{osc} since parasitic drain/source resistances will increase. And increasing both load and drive TFT dimensions at the same time will keep f_{osc} constant since the increase in f_{osc} due to increased load TFT dimensions is cancelled with the increase in C_p due to the increased m_{drive} dimensions.

Table 7. Fabricated circuits- R_{s,d_ld} and R_{s,d_dr} are parasitic drain/source resistances

	Overlap=10μm	Overlap=30μm
Case 1: m_{load}=50μm/50μm m_{drive} =300μm /50μm	R_{s,d_ld} =830kΩ R_{s,d_dr} =140kΩ f_{osc} =21.8kHz	R_{s,d_ld} =276kΩ R_{s,d_dr} =46kΩ f_{osc} =26kHz
Case 2: m_{load} =100μm /50μm m_{drive} =600μm /50μm	R_{s,d_ld} =415kΩ R_{s,d_dr} =69kΩ f_{osc} =21.9kHz	R_{s,d_ld} =138kΩ R_{s,d_dr} =23kΩ f_{osc} =26kHz

In terms of sensitivity analysis we analysed the ring oscillator shown in Figure 25 for Case 1 in Table 7 with overlap=30μm and V_{cc} ranging from 20V to 40V. As can be seen from Figure 31, as V_{cc} increases the range of sensitive $V_{pix\text{-}ctrl}$ increases but V_T shift then becomes an issue at higher voltages. In the case of V_{cc} =30V this range is only 2V whereas in the case of V_{cc}=40V it is increased to 6V and in the case of V_{cc} =20V it is only 1V. As seen in Figure 31, the frequency-voltage gain of the ring oscillator is ~1kHz/V at V_{cc}=40V which can also be calculated from equation (31).

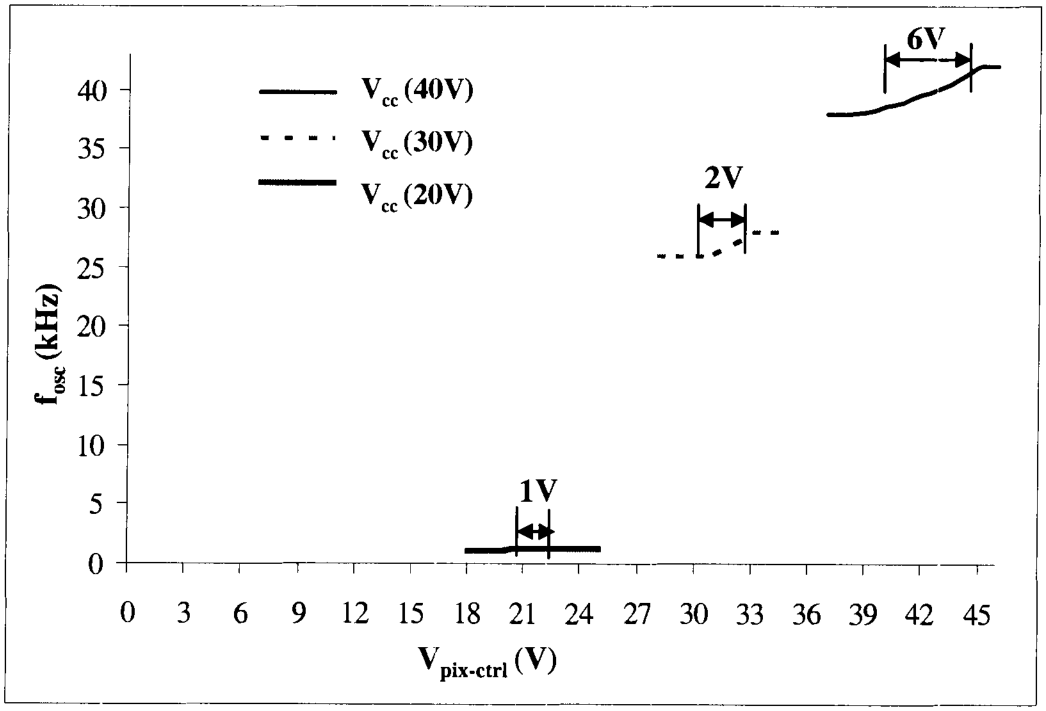


Figure 31. Ring oscillator sensitive range

4.4.5 Optimized circuit-theoretical

As mentioned in the previous sections, high f_{osc} and high sensitivity in the range of operation are desirable and in this section we aim to optimize the ring oscillator circuit shown in Figure 25. From equations (26) and (29) we can estimate that increasing f_{osc} can be achieved by decreasing the number of stages, decreasing parasitic capacitance at the output of each stage C_p, and increasing $g_{m\text{-}load}$.

Parasitic capacitance, C_p was calculated in (23) where we see that decreasing C_p can be achieved by using smaller devices.

For $g_{m\text{-}load}$ we have,

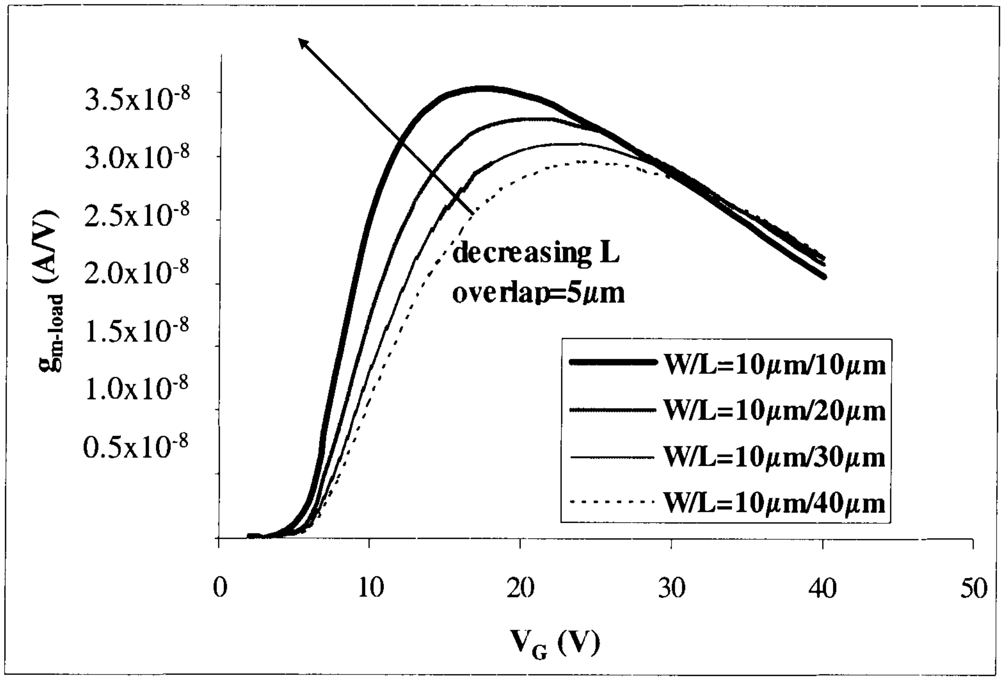
$$g_{m-load} = \partial i_d / \partial V_g \big|_{V_g = V_G} = \mu . C_{ox} .(W / L)_{load} .(V_G - V_T) \qquad (32)$$

Therefore, increasing W_{load}, decreasing L_{load}, and increasing V_G (bias voltage) all can improve $g_{m\text{-}load}$. Voltage V_G may be increased; this increases both the frequency of the oscillation and the power consumed, which is dissipated as heat. The heat dissipated limits the speed of a given oscillator and varies the threshold voltage V_T. Also, $g_{m\text{-}load}$ is decreased at higher V_G biases due to effect of drain/source resistances. The reason for the $g_{m\text{-}load}$ incline-decline behaviour as V_G is increased can be explained by a more precise bias current formula where the drain/source parasitic resistances are included [4]. Assuming the drain and source parasitic resistances are equal and called $R_{s,d}$ we have,

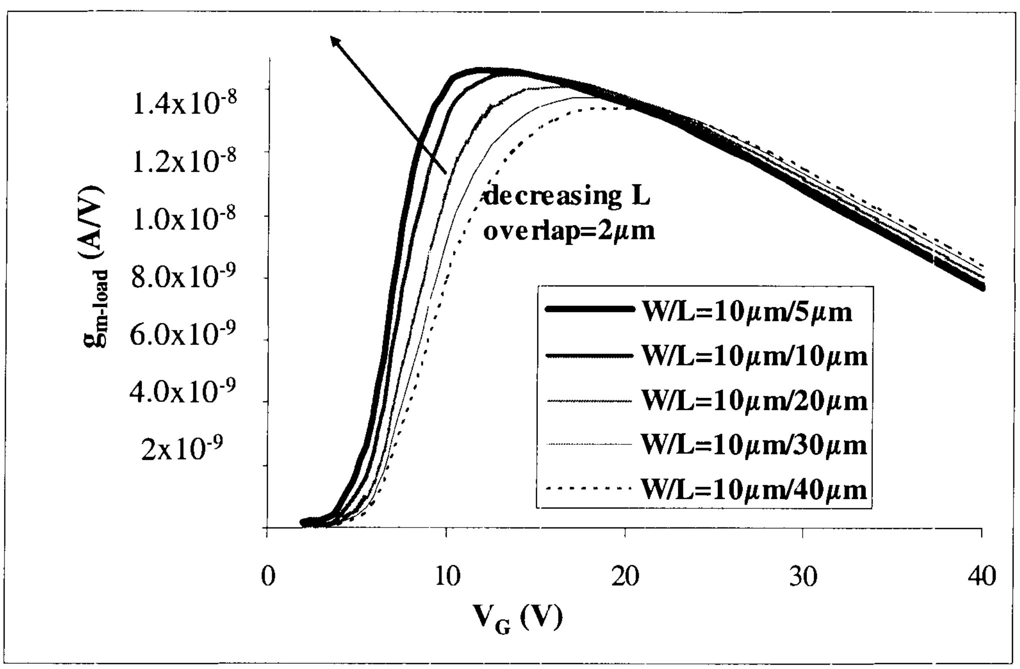
$$I_D = \mu C_{ox}(W/2L)[(V_{GS} - 2R_{s,d}.I_D) - V_T]^2 \tag{33}$$

The above feedback behaviour of I_D with increasing V_{GS} in the above formula, together with the original definition of $g_{m-load} = \partial i_d / \partial V_g \big|_{V_g = V_G}$ explain that $g_{m\text{-}load}$ can only increase to an optimum point at a specific V_G bias.

Figure 32 (a) and (b) show the load $g_{m\text{-}load}$ variation with increasing V_G and decreasing channel length L from 40μm to 10μm. Width of the TFTs is kept constant at 10μm; first graph is for overlap of 5μm and the second one is for 2μm.



(a)



(b)

Figure 32. Increasing V_G and decreasing L_{load} on $g_{m\text{-}load}$ for (a) overlap=5μm, (b) overlap=2μm

A few observations can be made from the above graphs:

1. Decreasing L_{load} increases $g_{m\text{-}load}$ but at higher voltages the effect is opposite (L=5-10μm is optimal)
2. Increasing V_G increases $g_{m\text{-}load}$ to an optimum value (20-25V seems optimal in Figure 32(a))
3. Increasing overlap decreases the parasitic drain/source resistances and increases $g_{m\text{-}load}$ for the same bias.

The maximum W_{load} can be chosen with area consideration as well as keeping C_p at minimum. Therefore, optimization is made by increasing W_{load} up to the point where the effect of C_p becomes noticeable.

From the above analysis, an optimized ring oscillator is proposed with the following parameters (simulated in AIM Spice ASIA2-level 15):

m_{load} =10μm/5μm, m_{drive} =100μm/5μm, R_{s,d_ld}=8.3MΩ, R_{s,d_dr}=0.83 MΩ, V_T=5V, t_{ox}=350nm, overlap=5μm.

As can be seen from Figure 33, f_{osc} is ~200kHz and the sensitive range is increased to about 10V. For application in medical imaging, the linear region of $f_{osc}/V_{pix\text{-}ctrl}$ is selected. In the case of V_{cc}=25V the range of $V_{pix\text{-}ctrl}$ 14 to 24V behaves linearly as seen below. The frequency voltage gain of the ring oscillator is ~6 kHz/V from (29) and can be observed below in the linear range. Further optimization can be made using the state of the art TFTs with channel lengths of 2μm.

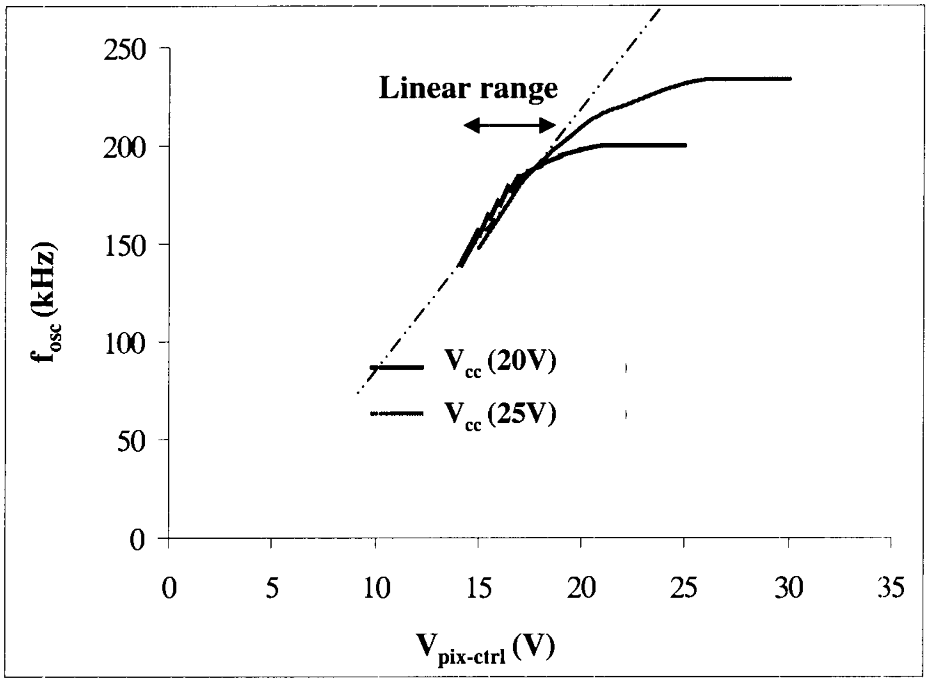


Figure 33. Optimized ring oscillator sensitive range

The area for the proposed optimized circuit will be mostly occupied by m_{drive} TFTs where each m_{drive} =100μm/5μm and using finger layout techniques the circuit can easily fit in the pixel area of 200x200μm^2 used for fluoroscopy application. In terms of dynamic range, this circuit generates Δf_{osc} from 3Hz to 50kHz for $\Delta V_{pix\text{-}ctrl}$ inputs ranging from 0.4mV to 8V and as long as a frequency counter with less than 3Hz frequency resolution (running at ~200kHz) is used at each column, the dynamic range of ring oscillator will cover from fluoroscopy to chest radiography application. Commercial frequency counters (e.g. Instek GFG-3015) can count from 0.01Hz to 15MHz with 10mHz resolution. As shown in Table 1., the voltage range of 0.4mV to 8V is based on using C_{pix}=0.2pF and Q_{pix} ranging from 0.08 fC to 1.6 pC from fluoroscopy to chest radiography.

4.4.6 Phase Noise Analysis

Phase noise is an important figure of merit in oscillator design. Based on the phase noise characteristics of the oscillator, it can be decided whether the design is suitable for a specific application. In the case of VCO used for A/D conversion in medical imaging applications, phase noise can be the limiting factor in x-ray detection in low-dose modalities. In this section, first a background on phase noise analysis is given based on [28] followed by phase noise estimation for the ring oscillator circuit discussed in 4.4.5.

If the power spectral density (power as a function of frequency) is measured at the output of an oscillator, it is observed that that rather than all the power being concentrated at the oscillation frequency, some of the power is distributed in frequency bands on both sides of the oscillator frequency. These unwanted frequency components are referred to as oscillator noise.

Let us assume the oscillator output *S(t)* can be expressed by,

$$S(t) = V(t).\cos(\omega_c t + \theta(t)) \tag{34}$$

where *V(t)* describes the amplitude variation as a function of time and $\theta(t)$ is the phase variation. $\theta(t)$ is referred to as oscillator phase noise. Assuming the oscillator is high-quality and therefore amplitude-stable, *V(t)* can be considered constant and thus all oscillator noise will be due to $\theta(t)$. A carrier signal of amplitude *V* and frequency f_0, which is frequency modulated by a sine wave of frequency f_m, can be represented by,

$$S(t) = V.\cos(\omega_c t + \frac{\Delta f}{f_m}.\sin(\omega_m t)) \tag{35}$$

Where Δf is the peak frequency deviation and $\theta_p = \frac{\Delta f}{f_m}$ is the peak phase deviation. The above equation can be simplified assuming θ_p <<1 to,

$$S(t) = V.\left\{\cos(\omega_c t) - \frac{\theta_p}{2}.[\cos(w_0 + w_m)t - \cos(w_0 - w_m)t]\right\} \tag{36}$$

This equation shows for small peak phase deviation, the phase deviation results in frequency components on each side of the carrier of amplitude $V.\theta_p/2$ at frequencies $f_0 \pm f_m$. Let us take V_N as the peak noise voltage; therefore, we have,

$$\frac{V_N}{V} = \frac{\theta_p}{2} \tag{37}$$

$S_\varphi(f_m)$ is defined as the ratio of the single sideband power of phase noise in a 1-Hz bandwidth f_m hertz away from the carrier frequency to the total signal power.

$$S_\varphi(f_m) = (\frac{V_N}{V})^2 = (\frac{\theta_p}{2})^2 = \frac{\theta_{rms}{}^2}{2} \tag{38}$$

The total noise is the noise in both sidebands and will be denoted by Sθ. That is,

$$S_\theta(f_m) = \theta_{rms}{}^2 \tag{39}$$

The above equations and analysis shown in [29], predict a phase noise expression as following.

$$S_\varphi(f_m) = \frac{f_0}{f_m{}^2}.(\frac{\Delta T_{rms-VCO}}{T_0})^2 \tag{40}$$

Assuming that in the oscillator each delay cell is buffered from the next stage,

$$t_d = \frac{C_L V_{SW}}{I_{ss}} \tag{41}$$

And therefore,

$$\frac{\Delta t_{d-rms}}{t_{d-rms}} = \frac{\Delta V_{n-rms}}{V_{n-rms}} \tag{42}$$

From noise analysis as explained in [29],

$$\overline{V_n^{\ 2}} = \frac{kT}{C_L}(\gamma_{drive}.a_v + \gamma_{load}) \tag{43}$$

Let us define,

$$\xi^2 = (\gamma_{drive}.a_v + \gamma_{load}) \tag{44}$$

One method to measure phase noise is to relate the spectral density of the normalized frequency fluctuations to the instantaneous error in the period of oscillations i.e. $\Delta T_0/T$. First, with the value of f_{osc} for ring oscillators in equation (26) and modelling circuit noise induced timing jitter for ring oscillators as explained in [29] we have,

$$(\frac{\Delta T_{rms-VCO}}{T_0})^2 = \frac{kT}{I_{SS}}.\frac{a_v \xi^2}{2(V_{GS} - V_T)}.\frac{1}{T_0} \tag{45}$$

Here, a_v is the voltage amplification in drive TFT, I_{ss} is the drain current and V_{GS} is gate-source current of drive TFT. And using (38) we have,

$$S_\varphi(f_m) = \left(\frac{f_0}{f_m}\right)^2.\frac{kT}{I_{SS}}.\frac{a_v \xi^2}{2(V_{GS} - V_T)} \tag{46}$$

Therefore, at a given frequency offset from carrier, the phase noise improves with higher inverter cell supply currents. Based on these expressions, the phase noise of a single-ended ring oscillator is found to be independent of the number of stages for a given power dissipation and frequency of operation. On the first pass noise analysis [29], noise sources are assumed constant for simplification so that basic path from current noise to the output voltage noise to timing jitter can be illustrated. Further analysis can be done with effects of time varying noise sources, and considering inter-stage amplification for complete analysis but in this document we assume first pass analysis.

The minimum voltage change due to x-ray exposure is 0.4mV based on Table 1. in Chapter 1. Based on our optimized circuit results in 4.4.5, we have γ_{load}=1 and γ_{drive}=2/3, I_{ss}=0.36μA, V_{GS}=5.57V, V_T=5V, a_v=1.006V/V and the following figure shows the phase noise in dB versus frequency.

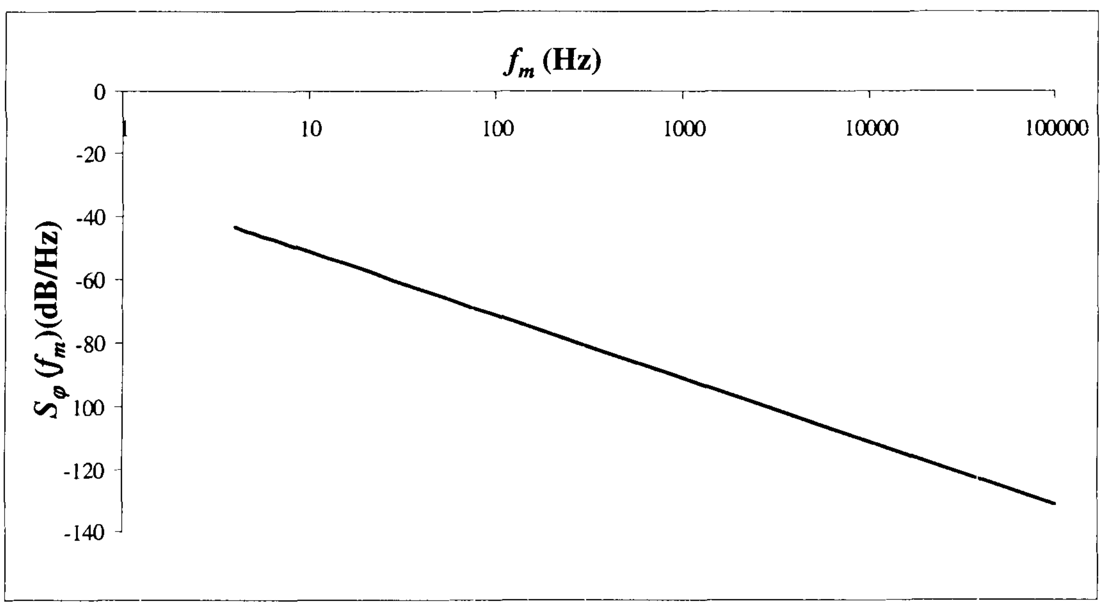


Figure 34. Phase noise $S_\varphi(f_m)$ versus f_m

As can be observed from the above graph, the further f_m is increased the more the noise is improved. The value of $S_\varphi(f_m)$ can further be improved by using high quality

TFTs with lower power consumption. $S_\varphi(f_m)$ is in dB units i.e. $(10.\log\lfloor S_\varphi(f_m)\rfloor)$. To calculate the input referred noise, we need to find the relation between the output phase noise and input voltage change. From equation (38) and the definition of Δf as the peak frequency deviation we have,

$$\Delta f = 2f_m\sqrt{S_\varphi(f_m)} = 2f_0\sqrt{\frac{kT}{I_{SS}}(\frac{a_v\xi^2}{2(V_{GS} - V_T)}} \tag{47}$$

For our optimized ring oscillator circuit, the value of Δf is 0.03Hz i.e. the smallest detected voltage which is 3Hz has only 1% peak frequency deviation. And based on the frequency-voltage gain of the circuit (6kHz/V) the input voltage change is $8.3\text{x}10^{-6}$V which when converted to charges (for C_{pix}=0.2pF) is ~$10.9\text{x}10^{-19}$C or <10 electrons that contribute to negligible error.

4.4.7 Metastability

First a background on the effect of V_T shift on TFTs is presented here which will be followed by the study of its effect on the ring oscillator circuit.

4.4.7.1 Background

The threshold voltage (V_T) of a-Si TFT shifts under prolonged gate bias stress, and TFTs show different threshold voltage shift behaviour under positive and negative gate bias stress. This anomalous behaviour is attributed to two main mechanisms (i) charge trapping and (ii) defect state creation [4] Charge trapping takes place due to the trap sites in the gate insulator/a-Si:H interface or in the gate insulator layer. The state creation is related to the breaking of the weak bonds, which increases the density of dangling bonds in the a-Si:H. Charge trapping generally dominates at higher gate bias and/or longer duration of bias stress. In contrast, increase in the defect density takes place predominantly at lower gate fields and/or shorter duration of bias stress.

The threshold voltage increases with respect to the positive stress voltage as well as the stress duration. However, a turn-around effect exists for negative bias stress. This effect was reported in [4], that V_T of transistor increases for a short bias stress duration and/or small negative stress voltages and decreases for a long bias stress duration and/or large negative stress voltages. This positive V_T shift at smaller negative voltage stress and/or shorter duration of bias stress is ascribed to the increased defect density states in the band gap near the conduction band by the negative gate bias. The turn-around effect can be explained by taking the hole-trapping into account which dominates at large negative voltages and/or for longer bias stress, and offsets the effect of increased defect density by lowering the threshold voltage. A lower hydrogen concentration in the a-Si:H films causes a reduction in created defect states and the threshold voltage decreases monotonically after an application of negative voltage stress.

In addition, a-Si:H TFTs exhibit different behaviour for pulsed positive and negative stress voltages. The V_T shift (ΔV_T) due to positive pulse bias stress is almost independent of frequency of operation but, for negative pulse bias stress, the ΔV_T decreases in magnitude with increasing frequency [4]. In summary, a positive pulse serves to increase the ΔV_T and a large negative pulse can reverse this shift; therefore, applying negative pulses to the TFT during OFF state can reverse the shift. In general, smaller duty cycles induce less ΔV_T shift since the effective stress time is decreased. This allows the created defect states to relax and/or charges can de-trap during the OFF cycles.

Therefore, increasing frequency of operation and decreasing the duty cycle at the same time will result in small ΔV_T shift.

4.4.7.2 Effect of V_G bias, frequency, and duty cycle on ΔV_T

Based on Powell Jackson [12] defect state creation is characterized by a power law dependence of ΔV_T over time. Here, A is a process dependent term as a fitting parameter, V_{GS} is the gate/source voltage, t is time for positive stress. Let us take A=0.0115 α=1, β=0.3 [4].

$$\Delta V_T = A(V_{GS} - V_T)^{\alpha} t^{\beta} \tag{48}$$

Also, for short effective stress time $t \ll \tau$ (τ is effective hole accumulation time) the above relation follows similar power law as following for negative stress. Again let us take B=0.12x10^{-3}, α=2.49, β=0.28 [4].

$$\Delta V_T = B|V_{GS}|^{\alpha} t^{\beta} \tag{49}$$

For a signal with a duty cycle of T_{on}/T_{per} where T_{per} is the period, ΔV_T can be summarized by the following relation.

$$\Delta V_T = A(V_{GS} - V_T)^{\alpha}(t.T_{on}/T_{per})^{\beta} - B|V_{GS}|^{\alpha}\left[t.(1 - T_{on}/T_{per})\right]^{\beta} \tag{50}$$

In all ΔV_T equations above, t is time in minutes.

4.4.7.3 Metastability of ring oscillator circuit

Regarding the oscillator design, the TFT metastability problem can lead into aging and change in f_{osc} over time. According to the ring oscillator frequency voltage gain in equation (31) and assuming the parasitic capacitance C_p stays constant with bias voltage variations, $g_{m\text{-}load}$ will be the determining factor in f_{osc} changes. Also, each inverter stage in the ring oscillator should have unity gain condition for the m_{drive} TFT, to keep the oscillations running. Therefore, changing both $g_{m\text{-}load}$ and $g_{m\text{-}drive}$ with ΔV_T are considered and the effect on f_{osc} shift is calculated over time. The calculation for the case of our optimized circuit in 4.4.5 was done for a duty cycle of 0.1% (which is the case in a 1000 x 1000 pixel array) and a bipolar bias of +25/-5 is considered on the TFT gates.

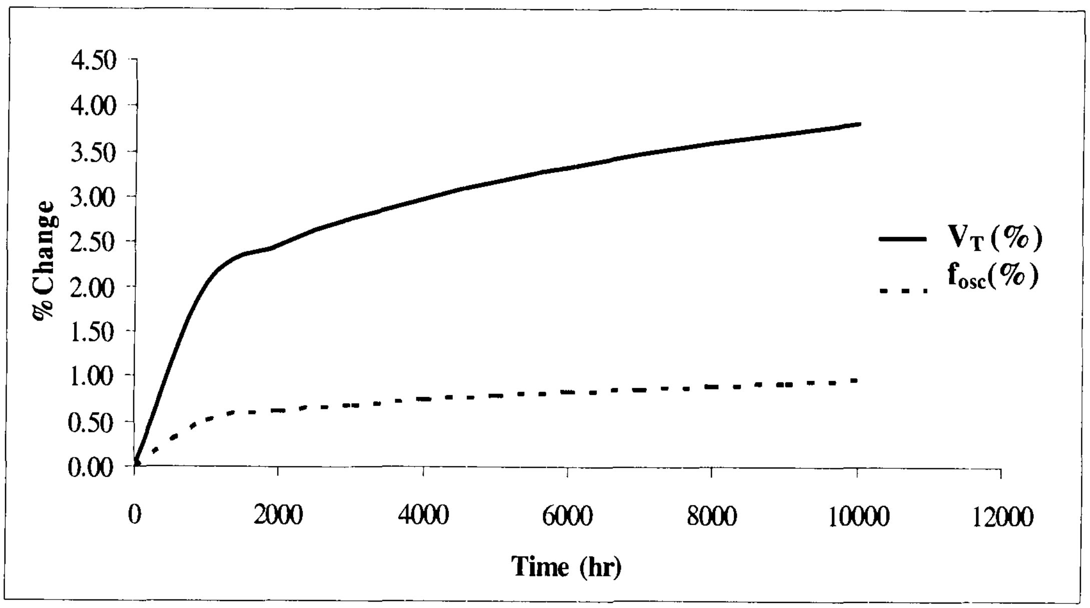


Figure 35. Effect of metastability on f_{osc} shift in ring oscillator circuit

As can be see from the above graph the f_{osc} variation is less than 1% over 10,000 hours of operation and the low duty cycle is an advantage since the change in V_T value during positive cycles is compensated during the negative cycles.

4.4.8 Ring oscillator readout

On-pixel analog-to-digital (A/D) conversion using ring oscillator as a VCO will require a frequency reader such as a counter, or a Schmitt trigger comparator and a counter. As shown in Figure 36, at the beginning of each cycle V_{reset} is set to V_{cc} and therefore $V_{pix\text{-}ctrl}$ will be ~ V_{cc}-V_T and as the x-rays hit the pixel (only pin diode is shown here as the detector), $V_{pix\text{-}ctrl}$ starts to drop and as a result the output of the VCO starts to drop as well. Therefore, the change in the input is reflected as change in frequency output. Readout can be done using a read TFT with sufficient drive. Also, a buffer can be placed between VCO output and the read TFT so the oscillations are not disturbed. C_{line} is estimated ~10pF, assuming read TFT is 10μm/5μm. The frequency counter will be placed at each column and needs to have frequency resolution of at least 3Hz based on the discussion in 4.4.5.

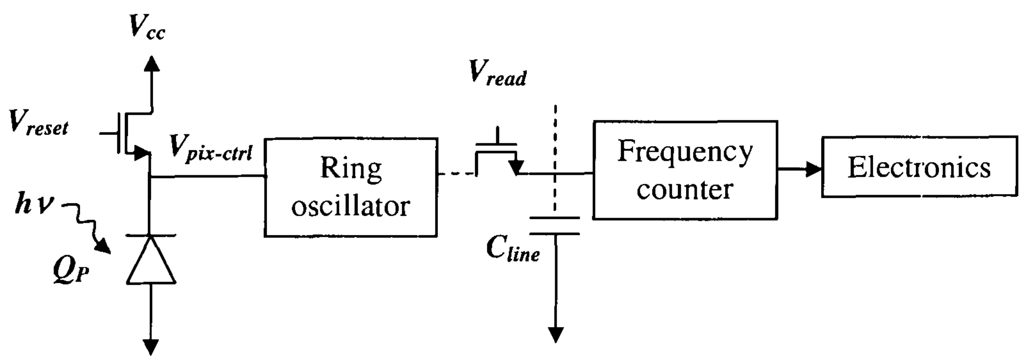


Figure 36. On-pixel frequency readout

4.4.9 Ring oscillator fabrication results

In the following we first present the TFT characteristics followed by circuit performance results. Then using AIM Extract, the TFT parameters are extracted and used in AIM Spice circuit simulations to analyse the results.

4.4.9.1 TFT characteristics and fabrication steps

Our TFTs were deposited using top-gate TFT deposition method. All our TFT depositions were made using the in-house multi-chamber load locked ultra high vacuum cluster tool for plasma enhanced chemical vapour deposition (PECVD). The TFT structure is as shown below. The thicknesses of a-Si:H and SiN_x were 100nm and 250nm respectively. Drain/Source is Aluminium with thickness of 70nm followed by n+ layer (not shown) with a thickness of 50nm. And for Gate we used Aluminium with thickness of 700nm.

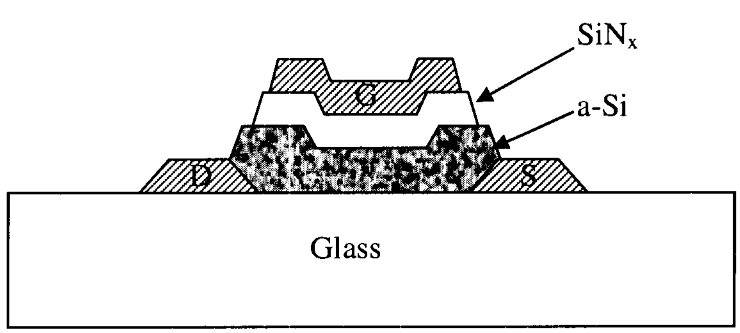


Figure 37. Top gate amorphous silicon TFT

A layer of SiN_x was first deposited on glass (not shown) as passivation layer. The deposition steps and conditions are as following.

SiN_x deposition which includes NH_3=150sccm, SiH_4=2.7sccm, H_2=100sccm, deposition pressure was 500mTorr with 1Watt power at 350°C for 30min followed by Aluminium sputtering. Then n+ is deposited using PECVD with SiH_4=1sccm, PH_3=1sccm, H_2=200sccm, deposition pressure was 1900mTorr with 1W power at 350°C for 30min followed by and drain/source photo lithography. Then a-Si:H is deposited using SiH_4=30sccm at 200mTorr at 210°C for 30min followed by SiN_x deposition using NH_3=150sccm, SiH_4=2.7sccm, H_2=100sccm at 500mTorr and 1Watt power at 350C for 30min.

The above steps are for TFT deposition and in the following we describe the step-by-step fabrication procedure using our 4-mask process:

1. Deposit SiNx (300nm), Aluminium (70nm), n+ (50nm).
2. Spin photoresist and UV expose using Mask1 (builds drain/source). Develop the photoresist.
3. RIE etch n+ layer, wet etch Aluminium, strip photoresist.
4. Deposit a-Si:H (300nm), SiN_x (350nm), and Aluminium (300nm).
5. Spin photoresist and UV expose using Mask2 (builds gate). Develop the photoresist.
6. Wet etch Aluminium to define gate and perform a RIE step to remove any film not protected by drain, source and gate. Strip photoresist.
7. Deposit SiN_x (600nm) for device isolation.
8. Spin photoresist and UV expose using Mask3 (builds vias). Develop the photoresist.
9. Wet etch SiN_x and strip photoresist.
10. Deposit Aluminium ($1\mu m$)
11. Spin photoresist and UV expose using Mask4 (builds top metal connections). Develop the photoresist.
12. Wet etch Aluminium. Strip photoresist.

In the following, we present the fabrication results for the ring oscillator from Table 7, where m_{load} =50μm/50μm, m_{drive} =300μm /50μm, and overlap=10μm. A micrograph of this circuit including TFT contact labels is shown in the following figure.

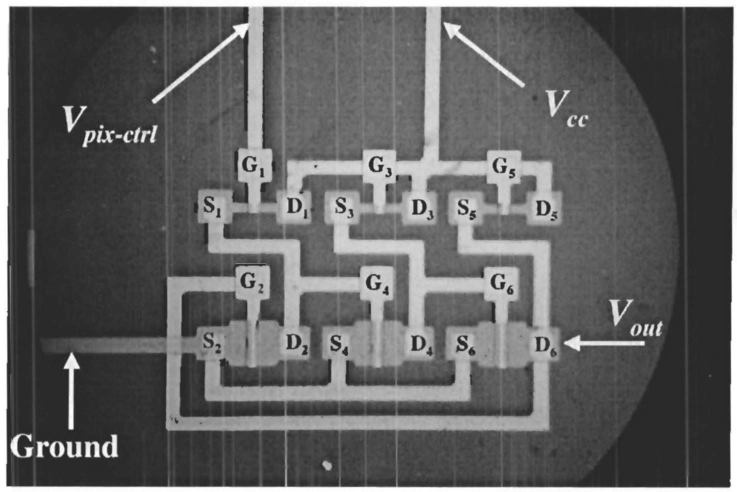


Figure 38. Micrograph of in-house fabricated ring oscillator m_{load}=50μm/50μm, m_{drive} =300μm /50μm, and overlap of 10μm

For comparison of the layout as observed in the micrograph with ring oscillator circuit schematic we have repeated Figure 25 including contact labels here.

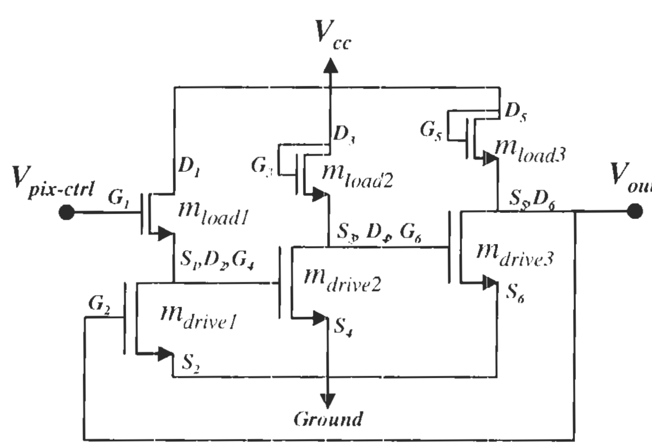


Figure 39. Ring oscillator schematic including contact labels

Before we discuss the circuit results, first we analyse TFT characteristics for the case of 300μm/50μm and 50μm/50μm as shown in the following two figures.

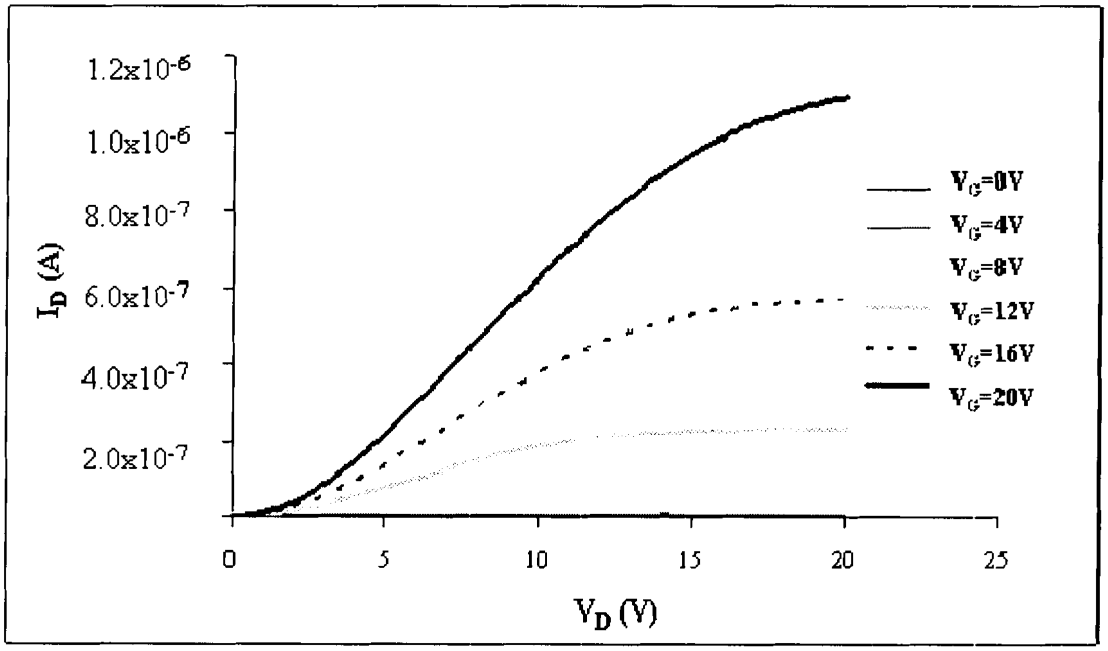


Figure 40. Current-Voltage characteristics for 50μm/50μm TFT

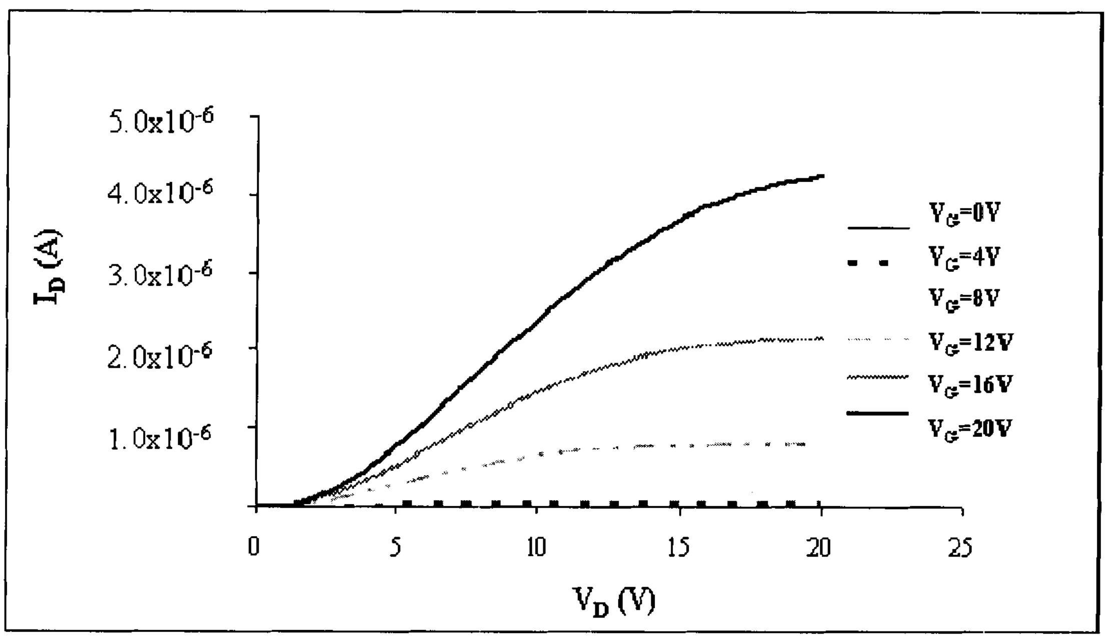


Figure 41. Current-Voltage characteristics for 50μm/50μm TFT

Using AIM Extract the following parameters were extracted.

For $50\mu m/50\mu m$ TFT:

GAMMA=0.235, SIGMA0=2.5×10^{-14}A, LABDA= 1×10^{-3}, M=5, VGSL=8V, VDSL=8V, IOL=3×10^{-14}A, VT0=6V, ALPHASAT=1, VAA=10MV, ALPHA=0, V0=0.2V, VFB=-4V.

And for the $350\mu m/50\mu m$:

GAMMA=0.235, SIGMA0=2.4×10^{-14}A, LABDA=1×10^{-3}, M=5, VGSL=8V, VDSL=8V, IOL=2.8×10^{-14}A, VT0=5V, ALPHASAT=1, VAA=10MV, ALPHA=0, V0=0.2V, VFB=-4V.

A channel mobility of $0.5cm^2/V.s$ was observed, which was slightly lower than our expected results.

The drain and source parasitic resistances are calculated from,

$$R_{S,D} = \frac{\rho . t_{n+}}{overlap.W} \tag{49}$$

Here, t_{n+} is the n+ thickness and $\rho=8.3e^3\Omega.m$ which resulted in $R_{S,D\text{-}load}=300k\Omega$, $R_{S,D\text{-}drive}=50k\Omega$.

4.4.9.2 Test apparatus

In this section we introduce our test apparatus as following. An Agilent 4156C precision semiconductor parameter analyzer was used for data collection, with a GPIB interface connected to a PC which had a user-friendly program for IC analysis. The probing station was a Signatone s-10-60R base with four Signatone S-725 probes. To monitor voltages of parameter analyzer, a Tektronics TDS 3024B Oscilloscope was used.

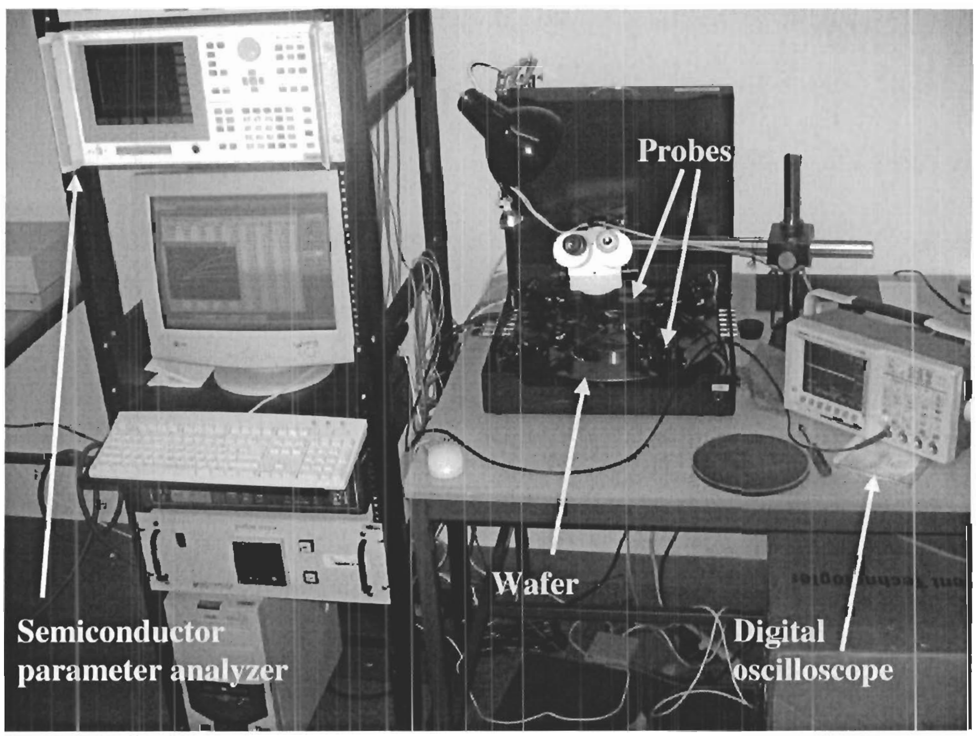


Figure 42. Test Apparatus

4.4.9.3 Circuit results

For the ring oscillator circuit mentioned in 4.4.9.1, we observed a 20kHz frequency of oscillations at 26V bias. This was calculated by the average period of 5 consecutive oscillations (52μsec). Increasing/decreasing the bias by 1V increases/decreases the oscillations by ~0.6kHz and therefore a sensitivity of 0.6kHz/V is observed. This voltage/frequency sensitivity value is observed from 22V to 26V.

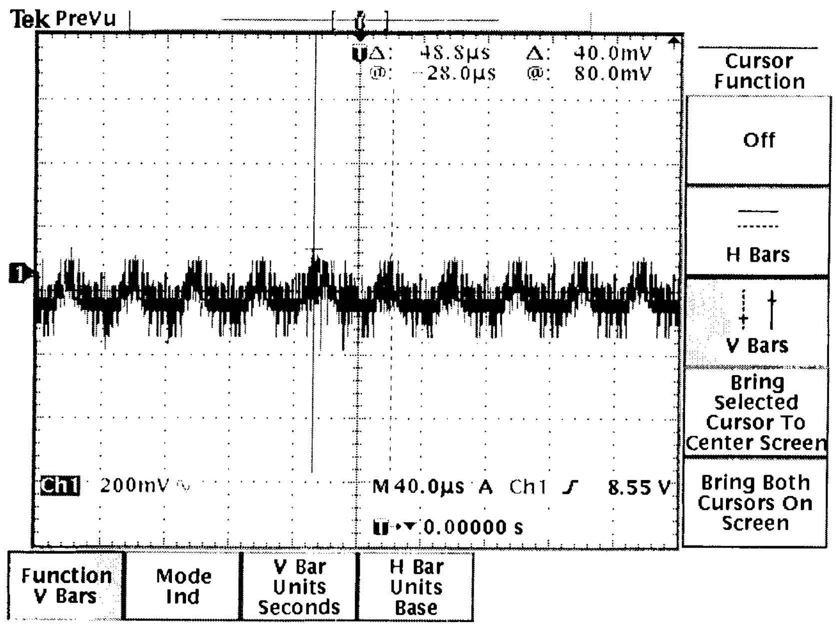


Figure 43. Ring oscillator oscillations at 26V DC bias

Our results show satisfactory agreement with the expected frequency of oscillation according to AIM Spice simulator. This is however slightly deviated from what was initially designed. The reason for this deviation is the fact that Mylar Masks prints were stretched in length (~7μm error) which decreased the channel length. This error increased the TFT aspect ratios by ~16% e.g. $(W/L)_{drive}$=300μm/43μm instead of 300μm/50μm and therefore a higher frequency of oscillations was expected. However, other errors such as the smaller channel mobility of 0.5cm^2/V.s and possibly higher parasitic capacitances due to mask error resulted in V_T of 6V instead of 5V. Thus forth, when new TFT parameters were entered in AIM Spice overall the frequency of oscillation remained close to what was originally expected. Our sensitivity is ~0.6kHz/V and this is in good agreement with AIM Spice simulations according to the new TFT parameters.

Regarding the oscillation amplitude, however, the measurements showed smaller than designed values. The reasons for this deviation include many factors such as following. The 1MΩ resistance and 15pF capacitance at the input probes of the Tektronics oscilloscope can decrease our signal amplitude; the output resistance of the ring oscillator is ~2MΩ and therefore can form a voltage divider. Also, the large input capacitance to the oscilloscope slows down the output charge time and that can also contribute to further decreasing the output amplitude. Other errors such as cable resistances and capacitances can contribute in this error as well. We simulated the effect of the 1MΩ resistance and 15pF capacitance at the oscillator output and the results are as following which is very close to our fabrication results.

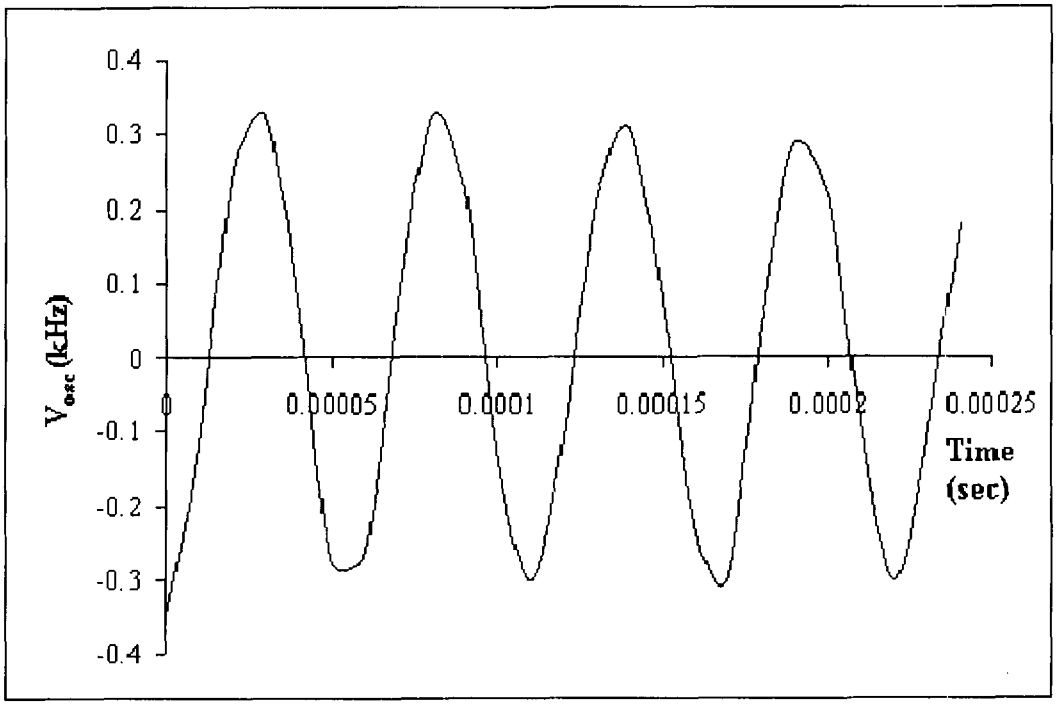


Figure 44. AIM Spice simulation of output observed by Tektronics oscilloscope

Overall the frequency of oscillations and frequency sensitivity of the ring oscillator were close to the expected values. All the circuit testing recorded here were done using the probe station and therefore our test results can significantly improve if the wafer is scribed and individual circuits are placed, wire-bonded, and tested inside DIP packages. Also, this circuit should be followed by a buffer which can significantly improve output signal distortion.

CHAPTER 5: CONTRIBUTIONS AND CONCLUSION

In this thesis work we mainly focused on on-pixel amplifiers to reduce pixel complexity and integrate off-panel components to on-panel and thus achieve higher signal-to-noise ratio (SNR) for low-exposure, real-time digital fluoroscopy. Towards this goal, we investigated methods for increasing on-pixel intelligence to reduce off-panel readout circuit complexity. A ring oscillator was fabricated, simulated in AIM Spice, tested, and analysed. Estimations of the phase noise and metastability of the ring oscillator were performed. Brief analysis of relaxation oscillator and LC tank oscillators were provided. Detailed analysis of charge gain and linearity of hybrid active pixel sensor (HAPS) architecture for increasing x-ray imaging dynamic range was performed. An in-house planar spiral inductor was fabricated on glass. Also, ASITIC simulations of the inductor concluded that high quality in-house inductors can be designed in TFT process at Simon Fraser University.

Future work in this area includes adding a buffer at the output of the ring oscillator, by placing an additional inverter stage to reduce output signal distortion. Further optimization of TFT characteristics and testing of metastability and phase noise are needed. Based on the circuits fabricated and tested in this thesis, ring oscillator in a-Si:H technology can be implemented for application in large area high dynamic range medical x-ray imaging. Also, based on simulations results, the ring oscillator phase noise performance appears to be excellent and the low metastability indicates long life-time for this application.

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