Phase Noise Analysis of a 0.18μm CMOS Fractional-N PLL for 802.11 a/b/g/n Applications

by

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ABSTRACT

In integrated CMOS 802.11 a/b/g/n direct conversion transceivers a key performance characteristic is the RMS value of RF clock phase noise at offsets between 1kHz and 20MHz. Phase noise analysis concepts related to fractional-N PLLs are presented and an optimization exercise determining PLL characteristics for a 0.18μm CMOS fractional-N PLL in an 802.11 a/b/g/n RF frequency generation application is described. For fractional-N PLLs, modelling fractional-N phase noise effects and optimizing PLL characteristics to mitigate fractional-N effects is a major part of the PLL implementation process. Other major phase noise sources such as VCO noise must also be considered in optimizing PLL characteristics; considerations for other noise sources are discussed. Matlab is used to model fractional-N phase noise effects and to model overall PLL phase noise performance in the frequency domain. PLL characteristics are optimized with consideration for RMS phase noise at the PLL output and with consideration for PLL stability. Analysis is also performed to investigate the effect of variations in IC characteristics on PLL performance.

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GLOSSARY

CMOS	Chemical Metal Oxide Substrate
IC	Integrated Circuit
LPF	Loop Filter
PD-CP	Phase Detector and Charge Pump
PLL	Phase Locked Loop
RF	Radio Frequency
Spectre/SpectreRF	Circuit simulator tools
VCO	Voltage Controlled Oscillator

1 INTRODUCTION

1.1 General

This report presents the design optimization process for a PLL used in an 802.11 a/b/g/n RF clock generation application. The PLL is implemented in a 0.18μm CMOS process. Basic concepts related to PLL phase noise are presented; the modelling concept used to predict the phase noise effects of fractional-N PLL activity is also provided. The design target for the PLL is 1^{o} RMS phase noise at the RF frequency output within offsets from the RF frequency of 1kHz to 20MHz (while 10MHz is the upper bound for critical phase noise in a/b/g applications, RMS phase noise over offset frequencies up to 20MHz is critical for the forthcoming 802.11 n standard). The design target is achieved through optimizing PLL characteristics with attention to fractional-N noise effects and other inherent noise effects within the PLL. Phase margin for the PLL is also required to exceed 45^{o}.

1.2 Report Outline

A very basic summary of PLL theory is provided in Section 2.

The concept of frequency multiplication and the fractional-N PLL are presented in Section 3. An analysis method for determining the phase noise input associated with fractional-N activity is presented and demonstrated.

In Section 4, noise models for major PLL noise contributors are presented and concepts related to PLL output phase noise response are presented.

In Section 5, the process of optimizing PLL characteristics using Matlab is presented; PLL optimization is performed with consideration for RMS phase noise on the PLL output and with consideration for PLL stability. Analysis is also performed to determine the effect of changes in PLL characteristics due to variations in CMOS process characteristics and operating conditions.

2 PLL THEORY

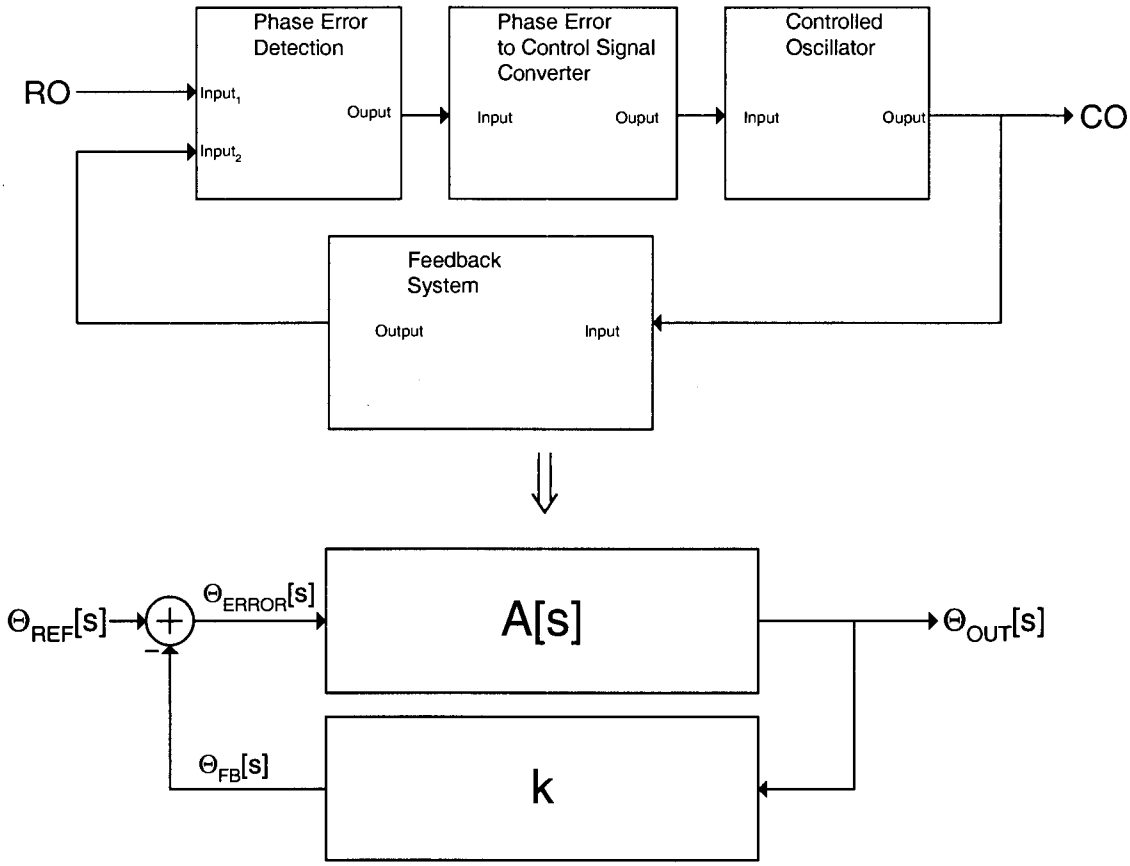
A brief summary of PLL architecture and modelling concepts is presented in this section to form a foundation for the discussion on fractional-N PLL noise modelling in Section 3 and for the general PLL noise theory and PLL phase noise optimization presented in Sections 4 and 5. Detailed discussion of PLL concepts is included in many graduate-level analog circuit design textbooks ([1] and [2]). As indicated in the following subsections and sections, portions of the discussion are specific to charge pump PLLs, specifically a class of charge pump PLLs referred to as third order charge pump PLLs.

2.1 PLL Concept

A PLL is a feedback control system that uses the phase argument of a periodic Reference Oscillator (RO) signal as its input (the concept of a periodic signal's phase argument is discussed in the Appendix) and controls the phase argument of a Controlled Oscillator (CO) signal. The feedback control system detects the difference between the phase argument of the RO signal and the phase argument of the feedback signal (the phase argument of the feedback signal is the phase argument of the CO signal scaled by a positive constant). The detected phase difference is used to generate a control signal for the CO.

A PLL that is at or near the phase locked condition can be approximately modelled as a Linear Time Invariant (LTI) system. $\Theta_{REF}(t)$ is the phase argument of the RO signal, $\Theta_{OUT}(t)$ is the phase argument of the CO signal, $\Theta_{FB}(t)$ is the phase argument of the feedback signal, and the difference between the feedback phase and the input signal phase is the detected phase error $\Theta_{ERROR}(t)$.

Figure 2-1 Functional diagram of PLL, block diagram of phase-domain control system model



At steady state, the control loop acts to ensure that $\Theta_{OUT}(t) * k$ is made to track $\Theta_{REF}(t)$, where k is the positive feedback constant. When the PLL is able to cause the

feedback signal's phase argument to track the RO signal's phase argument with no phase error ($\Theta_{ERROR}(t)=0$), the system is said to be phase locked. The forward gain of the system, $A[s]$, and the feedback coefficient k must be implemented with consideration for stability of the feedback control system.

2.2 Practical Third Order Charge Pump PLL Implementation and Sub-Block Modelling

The four main sub-blocks of a third order charge pump PLL are described briefly in following subsections. Continuous time LTI models of the four sub-blocks are presented. The four sub-blocks are:

1) Phase Detector and Charge Pump (PD-CP)

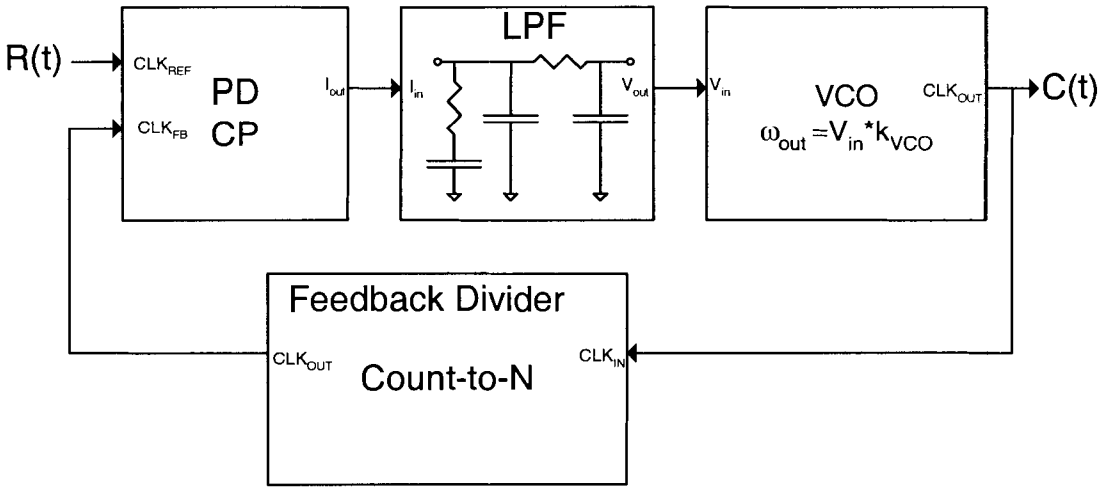
2) Low Pass Filter or Loop Filter (LPF)

3) Voltage Controlled Oscillator (VCO)

4) Feedback Divider

The interconnection of the four sub-blocks is shown in the following figure.

Figure 2-2 Four sub-blocks of the third order charge pump PLL



2.2.1 PD-CP

The PD-CP structure used in typical integrated CMOS PLLs is a mixed digital-analog circuit. Common architectures for phase-detection and charge-pumps are provided in [1]; for these common PD-CP structures (and if the PLL is at or near the phase locked condition) the phase difference between the reference clock and the feedback clock may be considered to be sampled once every reference clock period. The phase difference is measured by detecting the time delay between the rising edge of the feedback clock and the rising edge of the reference clock. Over each reference clock period the average output current of the CP will be proportional to the phase difference measured by the PD during that reference clock period.

This phase detection operation and adjustment of CP output current is not a continuous time process. However, the PD-CP transfer function is typically modelled as if phase detection and the resulting output current were continuous time processes (for

the sake of modelling, it is assumed that the instantaneous output current of the CP is proportional to the instantaneous phase difference detected by a continuous time phase detection operation). PLLs are generally implemented with a bandwidth at least one decade below the reference clock frequency, so the sampling operation of the PD-CP at the reference clock frequency is fast enough that the phase detection can be approximated as continuous time operation with respect to monitoring input phase variations near or below the PLL bandwidth. This concept becomes less accurate for fast input phase variations, but the approximation is necessary in order to facilitate modelling of the PD-CP frequency-domain response.

The PD-CP operation is modelled as a system with an instantaneous current output ($I_{CP\_OUT}(t)$) proportional to the phase difference at its input ($\Theta_{ERROR}(t) = \Theta_{REF}(t) - \Theta_{FB}(t)$); the constant of proportionality is the PD-CP gain (k_{PDCP}). k_{PDCP} has units of Amps per radian. The transfer function of the PD-CP ($H_{PDCP}[s]$) is given by

$$I_{CP\_OUT}(t) \approx k_{PDCP} * [\Theta_{REF}(t) - \Theta_{FB}(t)] = k_{PDCP} * \Theta_{ERROR}(t)$$

$$\Downarrow$$

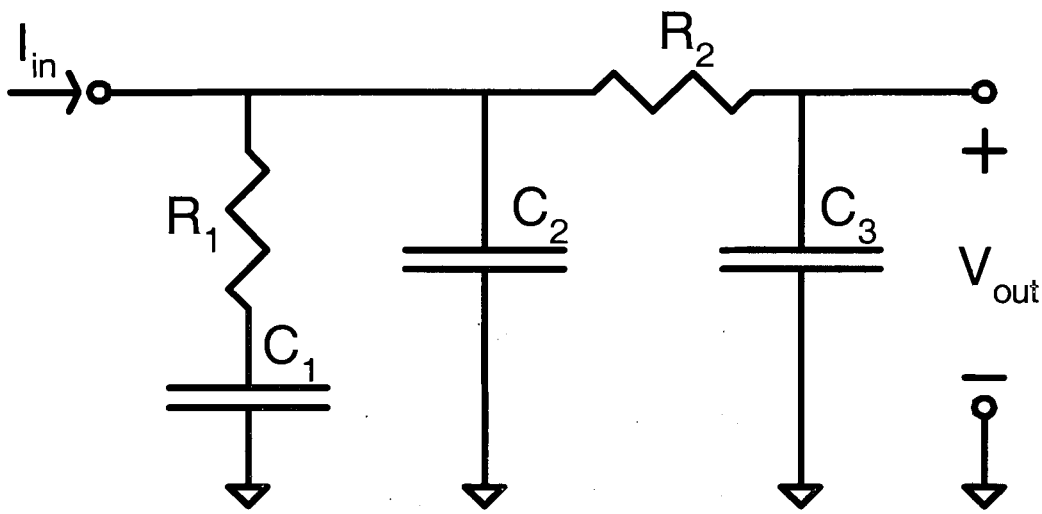
$$H_{PDCP}[s] = \frac{I_{CP\_OUT}[s]}{\Theta_{ERROR}[s]} = k_{PDCP}$$

2.2.2 Loop Filter

The loop filter is a network of resistors and capacitors; it stores the charge driven into it by the CP to produce a control voltage for the VCO. Since the loop filter input is the modelled current output of the PD-CP ($I_{CP\_OUT}(t)$), and the loop filter output must be

a voltage ($V_{LPF\_OUT}(t)$), the transfer function of the loop filter is simply the trans-impedance from the loop filter input port to its output port. The loop filter structure used in third order charge pump PLLs is provided in the following figure.

Figure 2-3 Third order charge pump PLL loop filter architecture



The sizing of C_1 is typically on the order of 10x larger than C_2, and the pole frequency associated with C_3 is typically on the order of 10x higher than the pole frequency associated with C_2. Under these conditions the trans-impedance of the loop filter can be approximated as a pole at DC, a zero at $\omega_Z \approx 1/R_1C_1$, a higher frequency pole at $\omega_{P1} \approx 1/R_1C_2$, and an even higher frequency pole at $\omega_{P2} \approx 1/R_2C_3$. The approximate s-domain model for the loop filter ($H_{LPF}[s]$) is given by

$$H_{LPF}[s] = \frac{V_{LPF\_OUT}[s]}{I_{CP\_OUT}[s]} = Z_{LPF\_IN-OUT}[s] \approx \frac{1}{C_1 s} * \frac{1 + sR_1C_1}{(1 + sR_1C_2)(1 + sR_2C_3)}$$

The loop filter transfer function provided above is an approximation because it assumes that the poles and zero associated with the loop filter capacitors are completely independent of each other. A more accurate transfer function for the loop filter can be calculated by explicitly determining the trans-impedance of the entire RC network shown in Figure 2-3.

2.2.3 VCO

The VCO is a circuit that generates a periodic output signal with an angular frequency ($\omega_{VCO}(t)$) that is proportional to the control voltage provided by the loop filter ($V_{LPF\_OUT}(t)$). The angular frequency and control voltage are related by a proportionality constant called the VCO gain (k_{VCO}) with units of radians per second per Volt.

$$\omega_{VCO}(t) = k_{VCO} * V_{LPF\_OUT}(t)$$

The VCO accepts the loop filter voltage ($V_{LPF\_OUT}(t)$) as its input and, for the purpose of modelling the phase response of the PLL, the VCO model should have the VCO output signal's phase argument ($\Theta_{VCO}(t)$) as its output.

Angular frequency of an oscillator is the derivative of the phase argument of the oscillator ($\omega = \Delta\Theta/\Delta t$) and conversely the phase of the oscillator can be considered to be the result of integrating the angular frequency of the oscillator with respect to time.

Using this relationship the VCO output phase can be related to the VCO control voltage by an integration operation.

$$\Theta_{VCO}(t) = \int_0^t \omega_{VCO}(t)dt = k_{VCO} * \int_0^t V_{LPF\_OUT}(t)dt$$

Given this relationship, the VCO s-domain model ($H_{VCO}[s]$) can be written as

$$H_{VCO}[s] = \frac{\Theta_{VCO}[s]}{V_{LPF\_OUT}[s]} = \frac{k_{VCO}}{s}$$

2.2.4 Feedback Divider

The feedback divider can be considered to be a simple fixed Count-to-N digital counter; the feedback circuit outputs a single output clock cycle once every N VCO clock cycles.

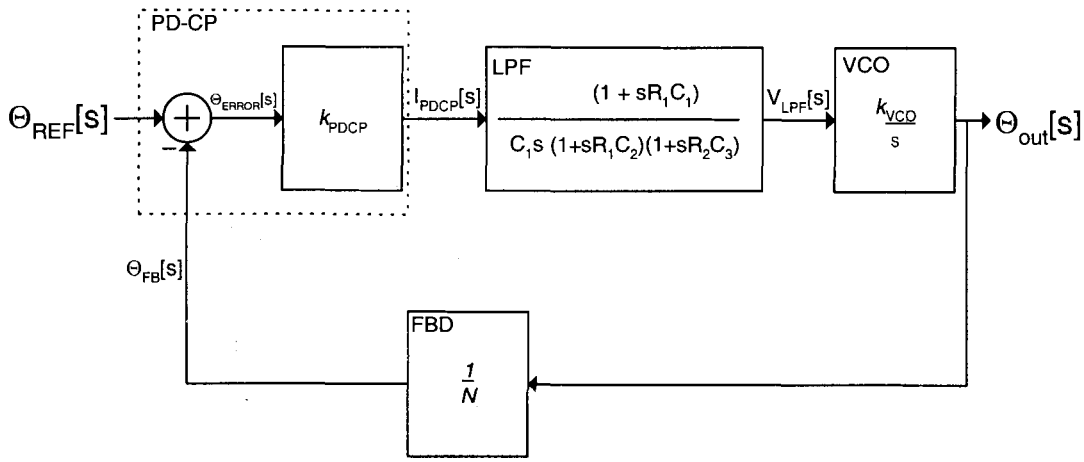
As discussed in the Appendix, the phase argument of the Count-to-N circuit's output clock ($\Theta_{FB}(t)$) is equal to $\frac{1}{N}$ times the phase argument of its input clock ($\Theta_{VCO}(t)$). The transfer function of the feedback system ($H_{FB}[s]$) implemented using a Count-to-N counter is therefore given by

$$H_{FB}[s] = \frac{\Theta_{FB}[s]}{\Theta_{VCO}[s]} = \frac{1}{N}$$

2.3 Linear Third Order Charge-Pump PLL Model

The four sub-block models discussed in the preceding section make up the components of the LTI model for the input phase to output phase transfer function of a third order charge pump PLL near the phase locked condition. The block diagram of the model is provided in the following figure.

Figure 2-4 Third order charge pump PLL linear model



The feed-forward gain of the PLL, $A[s]$ in Figure 2-1, is given by

$$A[s] = \frac{\Theta_{OUT}[s]}{\Theta_{ERROR}[s]} \approx k_{PDCP} \frac{(1+sR_1C_1)}{sC_1(1+sR_1C_2)(1+sR_2C_3)} \frac{k_{VCO}}{s}$$

The overall PLL transfer function is

$$H_{PLL}[s] = \frac{\Theta_{OUT}[s]}{\Theta_{REF}[s]} = \frac{A[s]}{1+\frac{A[s]}{N}}$$

2.3.1 Third Order Charge Pump PLL Transfer Function Example

In the following figure the loop gain magnitude response, loop gain phase shift, and closed loop transfer function magnitude are shown for illustration purposes for a third order charge pump PLL with the following characteristics:

$$k_{VCO} = 200MHz * 2 * \pi / Volt$$

$$k_{PDCP} = 200\mu A / 2 * \pi \ radians$$

$$R_1 = 3k\Omega$$

$$R_2 = 300\Omega$$

$$C_1 = 5nF$$

$$C_2 = 10pF$$

$$C_3 = 0.5pF$$

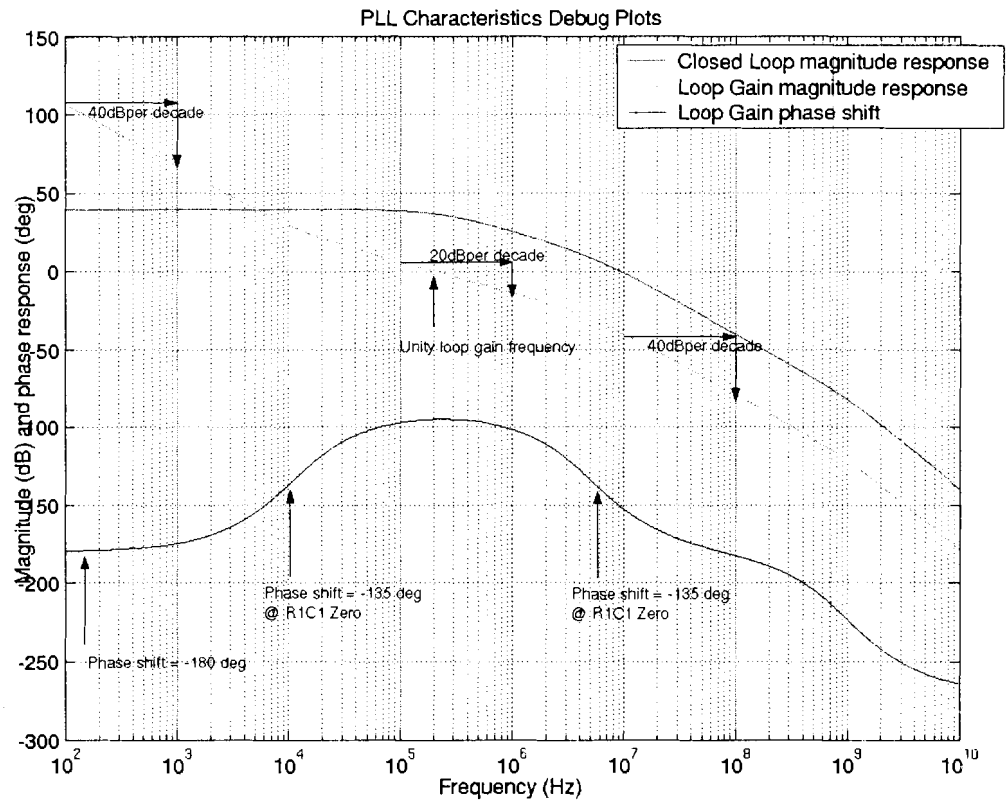
$$N = 90$$

$$\omega_Z \approx 2\pi(10.6kHz)$$

$$\omega_{P1} \approx 2\pi(5.3MHz)$$

$$\omega_{P2} \approx 2\pi(1.06GHz)$$

Figure 2-5 Third order charge pump PLL response sample characteristics



$A[s]$, the PLL's forward gain, has two poles at $s = 0$, correspondingly Figure 2-5 shows a loop gain phase shift of -180^o and a loop gain magnitude decay of 40 dB per decade at low frequencies. In order to meet the Nyquist stability criterion, the phase shift of the loop must be greater than -180^o at the unity magnitude loop gain frequency. To achieve this, the zero in $A[s]$ at $\omega_z \approx {}^{1}\!/_{R_1 C_1}$ is positioned at a frequency below the unity magnitude loop gain frequency so that the phase shift at the unity magnitude loop gain frequency will be greater than -180^o. In cases where it is necessary to improve high frequency attenuation of the PLL closed loop response, an additional pole or poles may be introduced above the unity gain

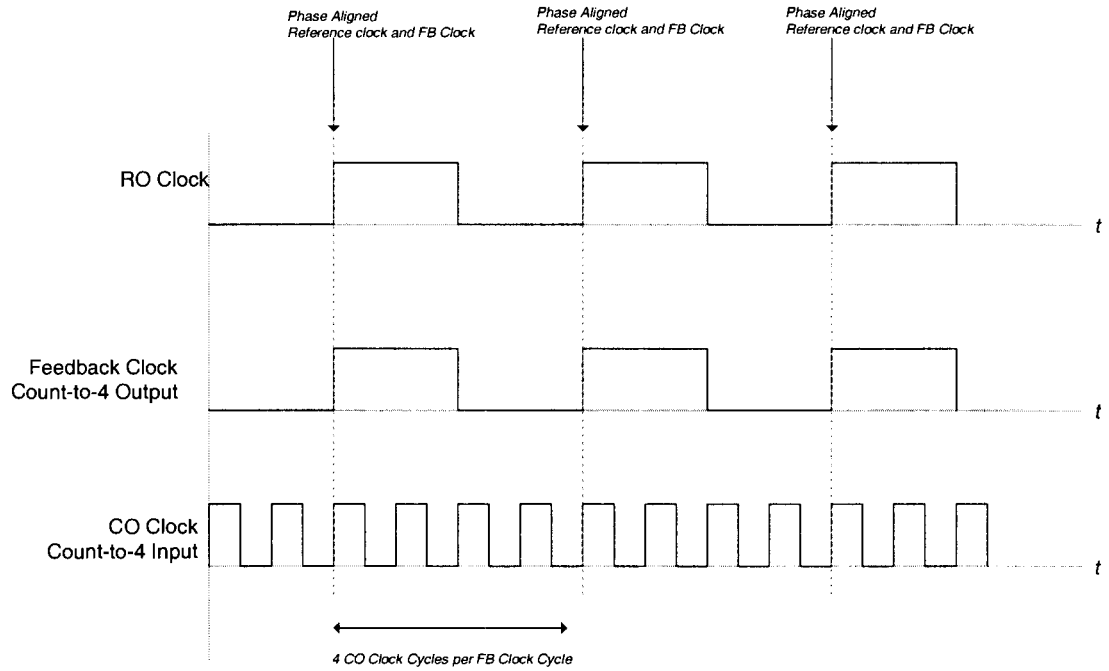
frequency (for a third order charge pump PLL poles are introduced at $\omega_{P1} \approx 1/R_1C_2$ and $\omega_{P2} \approx 1/R_2C_3$). The poles can't be placed close to the unity magnitude gain frequency because their corresponding reductions in the loop gain phase. Generally the lower frequency ω_{P1} pole is introduced at a frequency at least one decade above ω_Z.

3 INTEGER AND NON-INTEGER PLL FREQUENCY MULTIPLICATION

3.1 Integer Frequency Multiplication

The transient operation of a phase locked PLL with a fixed Count-to-N digital counter in the feedback path can provide an intuitive description of how a phase locked PLL acts as a frequency multiplier. When a PLL is phase locked, the feedback clock phase tracks the reference clock phase. If feedback clock remains in phase with the reference clock, the periods of these two clocks must be equal. Because the Count-to-N circuit outputs one feedback clock period for every N CO clock periods, the reference signal's oscillation period must therefore be N times greater than the CO oscillation period when the PLL is in phase lock. A timing diagram showing the CO output clock, the reference clock, and the feedback clock are shown in the following figure for a PLL in phase lock with a Count-to-4 circuit in the feedback path.

Figure 3-1 Transient behaviour of PLL output clock, feedback clock, and reference clock in a phase-locked PLL using a Count-to-4 feedback circuit



The concept of $N\times$ frequency multiplication is also apparent from the linear PLL model. Given that $\Theta_{REF}(t) = \Theta_{FB}(t) = {}^{1}\!/_{N}\,\Theta_{OUT}(t)$ for the case where the PLL is in phase lock, the relationship between the angular frequency of the reference oscillation ($\omega_{REF}(t)$) and the angular frequency of the output CO oscillation ($\omega_{OUT}(t)$) can be derived.

$$\Theta_{REF}(t) = {}^{1}\!/_{N}\,\Theta_{OUT}(t) \quad \Rightarrow \quad N\frac{d\Theta_{REF}(t)}{dt} = \frac{d\Theta_{OUT}(t)}{dt} = N\omega_{REF}(t) = \omega_{OUT}(t)$$

3.2 Fractional-N Frequency Multiplication Concept

The integer frequency multiplication capability is a useful PLL characteristic; it allows a PLL to generate a high frequency oscillation signal from a much lower

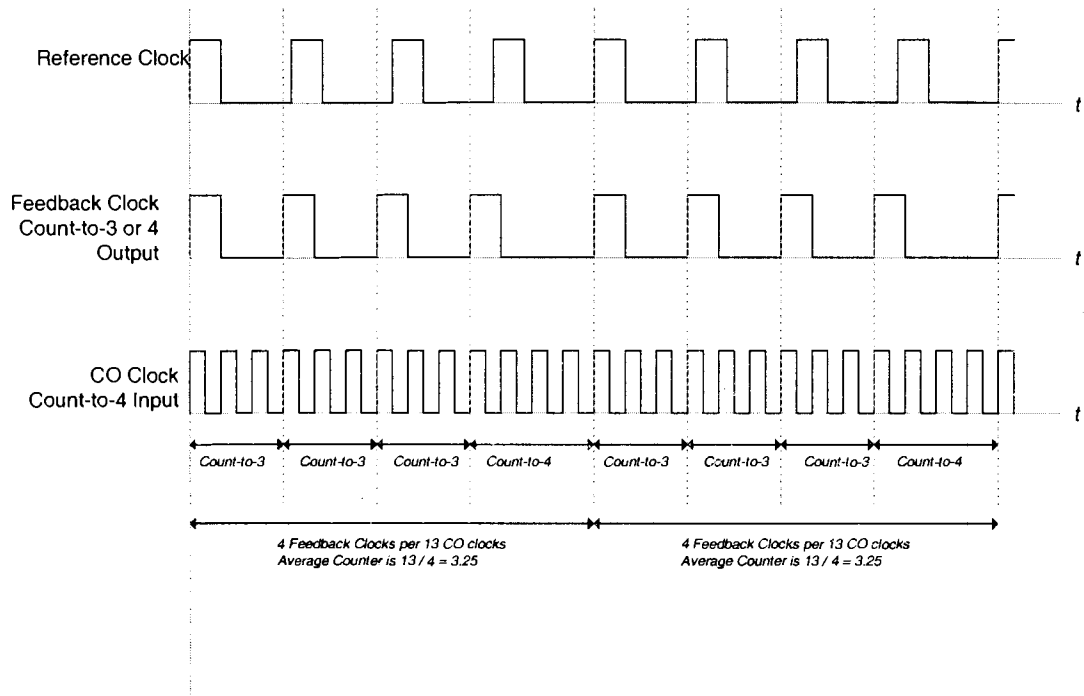
frequency reference oscillation signal. However, using a fixed function Count-to-N circuit in the feedback path only allows the phase locked PLL to generate an output oscillation signal at integer multiples of the reference signal's frequency. For cases where it is necessary to generate a non-integer multiple of the reference signal frequency, the fixed function Count-to-N circuit can't be used in the feedback path.

If it were possible to build a circuit that would generate an single output clock pulse for every $N+f$ (N is a positive integer, $0 \leq f < 1$) input clock cycles, the discussion in Section 3.1 and the feedback divider phase domain modelling concepts discussed in Section 2.2.4 could be extended to show that a PLL using such a circuit in the feedback path would cause the CO oscillation frequency to be scaled from the reference oscillation frequency by $N+f$ when the PLL is in phase locked condition.

It is not possible to build a rising-edge sensitive digital state machine that is clocked by a single binary clock and counts to a non-integer number of input clock cycles (e.g. Count-to-$N+f$). However, it is possible to build a simple digital state machine that acts as a flexible digital counter that can be dynamically reconfigured to count to different numbers of integer clock cycles. By dynamically switching such a digital counter between the configuration for count-to-N and count-to-$N+1$ operation it would possible to ensure that on average a single output clock cycle is generated by the counter for every $N+f$ input clock cycles. To illustrate this concept, the following figure shows the transient behaviour of a counter that counts to either 3 or 4, such that on average an output clock period is completed for every 3.25 input clock periods.

Additionally, a reference clock signal is plotted that has an oscillation frequency 3.25x less than the flexible counter's input clock frequency.

Figure 3-2 Transient operation of a Count-to-3 or 4 system with an average count value of 3.25



If this type of flexible count-to-N or $N+1$ circuit is placed in the feedback path of a PLL, and if the PLL characteristics are designed properly, the PLL will produce an output oscillation signal with an average frequency that is $N + f$ greater than the reference oscillation frequency. The modelling and simulation of this type of PLL system will be presented in the following subsections and sections.

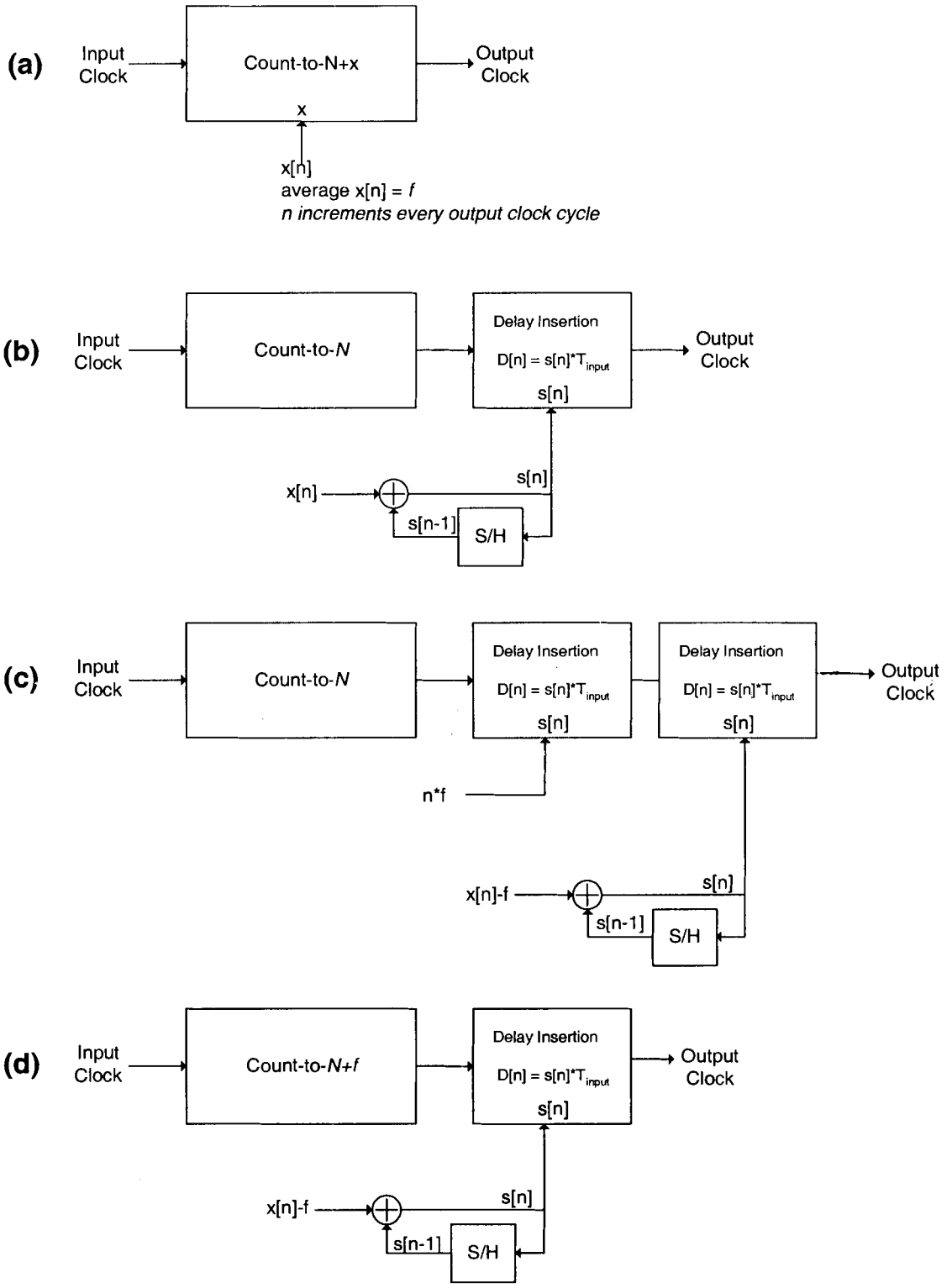
PLLs that implement fixed-function Count-to-N circuits in the feedback path are referred to as integer-N PLLs, and circuits that dynamically adjust the feedback counter

in order to get an average non-integer feedback counter value are referred to as fractional-N PLLs.

3.3 Fractional-N Feedback Noise Modelling

In order to analyze the affect of a feedback path in the PLL being implemented using a counter that is configured to count to a dynamically changing number of input clock cycles (for example, N or $N+1$), it is necessary to develop and alternative description for the transient operation of this type of flexible counter. The evolution of an alternative description for the flexible counter is presented in the following figure and subsections.

Figure 3-3 Alternative transient descriptions of Count-to-N+x[n] systems



3.3.1 Figure 3-3.a

Figure 3-3.a shows a flexible counter that outputs a single output pulse for every $N + x$ input pulses. x is an integer control input to the flexible counter (equal to 0 or 1 in the case where the counter is configured to count to either N or $N+1$). This control input is driven by a discrete sequence of integers, $x[n]$, where the value of the index n is incremented each time an output clock pulse is generated by the system. The resulting behaviour of the system is that the n^{th} output clock period from the system will be generated after the counter counts $N + x[n]$ input clock pulses following the $(n-1)^{th}$ output clock pulse. If the system is intended to generate an output pulse on average every $N + f, 0 < f \leq 1$ input clock cycles, then the average value of $x[n]$ must be f.

The sequence $x[n]$ is equivalent for each of the representations Figure 3-3.a-d.

3.3.2 Figure 3-3.b

The system in Figure 3-3.b is intended to reproduce the same transient relationship between the input and output clock as the system in Figure 3-3.a; Figure 3-3.b shows a system using a fixed count-to-N counter followed by a controllable delay cell. The controllable delay cell shown in Figure 3-3.b acts to delay the n^{th} output clock pulse from the count-to-N counter by a time amount $D[n]$ where $D[n]$ is determined by the following relationship:

$$D[n] = T_{input} \sum_{k=0}^{n} x[k]$$

T_{input} *is the input clock period to the Count – to – N counter*

$D[n]$ *is the delay added to the* n^{th} *output pulse from the Count – to – N counter*

For example, in the case where the system in Figure 3-3.a implements either count-to-N or $N+1$, the system in Figure 3-3.b increments the delay inserted by a single input clock period during each output clock cycle where the Figure 3-3.a system implemented count-to-$N+1$. The timing relationship between input clock pulses and output clock pulses is equivalent for the systems shown in Figure 3-3.a and Figure 3-3.b.

3.3.3 Figure 3-3.c

Figure 3-3.c shows a system that splits up the insertion of delay shown in Figure 3-3.b into two parts. The insertion of delay shown in Figure 3-3.b can equivalently written as

Figure 3 – 3.*b* *Figure* 3 – 3.*c*

$$D[n] = T_{input} \sum_{k=0}^{n} x[k] \quad \Leftrightarrow \quad D[n] = T_{input} \sum_{k=0}^{n} (x[k] - f) + T_{input} \sum_{k=0}^{n} f$$

$$= T_{input} \sum_{k=0}^{n} (x[k] - f) + T_{input} nf$$

The two-part delay insertion splits the delay insertion from Figure 3-3.b into an addition of $nT_{input} f$ to the n^{th} output clock pulse plus a zero-mean delay term.

given that $E[x[k]] = f$

$$E\left[\sum_{k=0}^{n} (x[k] - f)\right] = \sum_{k=0}^{n} (E[x[k] - f]) = 0$$

The timing relationship between input clock pulses and output clock pulses is equivalent for the systems shown in Figure 3-3.a and Figure 3-3.c.

3.3.4 Figure 3-3.d

Figure 3-3.d takes advantage of the fact the a Count-to-N circuit followed by a cell that incrementally adds an additional $T_{input} f$ delay for every output clock pulse is behaving like a circuit that generates a single output clock pulse for every $N + f$ input clock pulses (i.e. a Count-to-$N + f$ circuit).

The timing relationship between input clock pulses and output clock pulses is equivalent for the systems shown in Figure 3-3.a and Figure 3-3.d. Thus the Count-to-$N + x[n], (E[x[n]] = f)$ system acts like an ideal count to $N + f$ counter followed by a zero mean delay insertion term.

3.4 Phase Domain Model of Count-to-N+x[n] system

The system in Figure 3-3.d includes a zero-mean time shift term, given by

$$D[n] = T_{input}\left(\left(\sum_{k=0}^{n} x[k]\right) - n * f\right)$$

The ideal output of the count-to-$N + f$ counter in Figure 3-3.d exhibits an oscillation period of $(N + f) * T_{input}$. A time shift (Δt) applied to an oscillation signal (with an oscillation period T) is equivalent to a phase shift ($\Delta\Theta$) given by

$$\Delta\Theta = 2\pi\frac{\Delta t}{T}$$

Therefore the zero-mean time shift modelled in Figure 3-3.d can be represented as a zero mean phase shift ($\Theta_{FRAC\_NOISE}[n]$) applied to the n^{th} feedback clock signal:

$$\Theta_{FRAC\_NOISE}[n] = \frac{2\pi}{N}\left(\left(\sum_{k=0}^{n} x[k]\right) - n * f\right).$$

In the following subsection, a digital circuit structure for generating the sequence $x[n]$ is presented and sample $x[n]$ and $\Theta_{FRAC\_NOISE}[n]$ sequences are provided. In Sections 4 and 5, the impact of the discrete phase error sequence $\Theta_{FRAC\_NOISE}[n]$ on the PLL output phase will be discussed and a PLL optimization process considering $\Theta_{FRAC\_NOISE}[n]$ will be presented.

3.5 Fractional-N Control Sequence Generation

Fractional-N PLLs require a digital state machine to generate the sequence $x[n]$ that obeys $E[x[n]] = f$. $x[n]$ generation is typically performed using a Delta Sigma Modulator (DSM); DSM circuits are a type of analog to digital converter generally used in highly over-sampled analog to digital conversion. They are useful structures in part because the resulting quantization noise power spectral density at the DSM output has little low frequency content; this is achieved at the expense of adding quantization noise at higher frequencies. DSM circuits were subject to rigorous analysis beginning in the late 1980s as discussed in [3]. The fractional-N PLL operation of generating a sequence

of discrete $x[n]$ values that have a average value f can be considered to be an over-sampled analog to digital conversion, and the concept of using a DSM to generate the sequence $x[n]$ for a fractional-N PLL was first introduced in 1993 in [4].

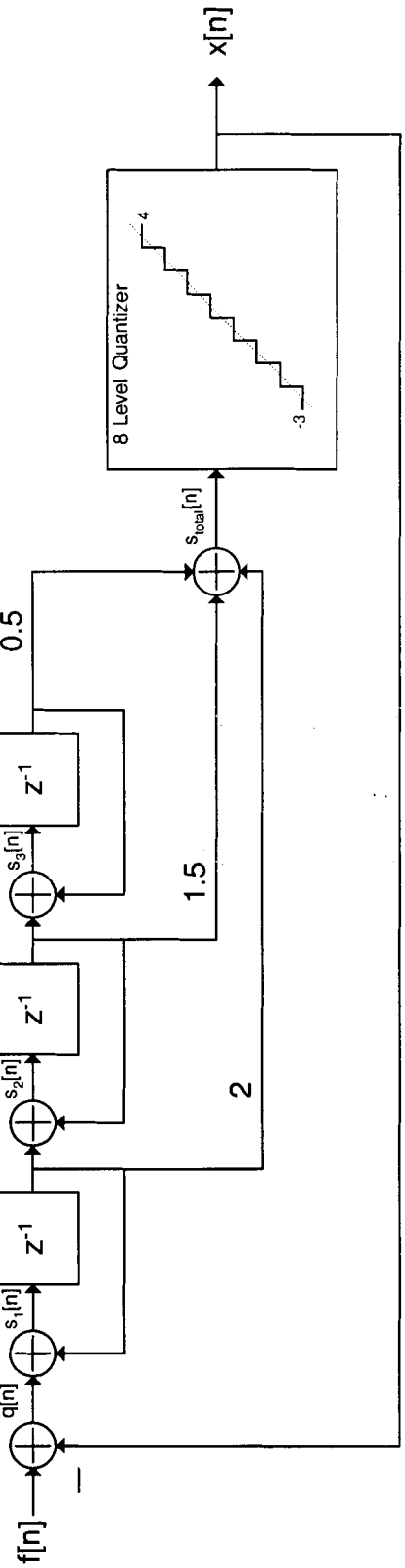
A number of different DSM structures currently find applications in fractional-N PLLs, often third order DSM structures are employed in fractional-N PLLs with tight constraints on spurious output phase noise content and overall close in RMS phase error requirements. Considerations related to DSM implementations in fractional-N PLLs are summarized in [5].

3.5.1 Third Order DSM Structure

Numerous DSM structures have been proposed and implemented to control fractional-N PLL feedback counters; two major DSM characteristics that vary between different DSM architectures are the spectral shaping of quantization noise and the potential for repetitive behaviour at the DSM output for certain input fractions resulting in spurious quantization noise power concentrations.

The $x[n]$ generation circuit used in the PLL implementation discussed in Section 4 and 5 was taken from [6]. The DSM structure is shown in the following figure. This DSM structure was selected following an initial investigation into numerous standard DSM structures that are commonly used for fractional-N PLL applications.

Figure 3-4 Third order DSM structure



The DSM structure shown in Figure 3-4 is described by the following equations

$$x[n] = \begin{cases} 4 \; if \; s_{total}[n] \geq 3.5 \\ 3 \; if \; 3.5 > s_{total}[n] \geq 2.5 \\ 2 \; if \; 2.5 > s_{total}[n] \geq 1.5 \\ 1 \; if \; 1.5 > s_{total}[n] \geq 0.5 \\ 0 \; if \; 0.5 > s_{total}[n] \geq -0.5 \\ -1 \; if \; -0.5 > s_{total}[n] \geq -1.5 \\ -2 \; if \; -0.5 > s_{total}[n] \geq -1.5 \\ -3 \; if \; -0.5 > s_{total}[n] \geq -1.5 \end{cases}$$

$$s_{total}[n] = 2 * s_1[n] + 1.5 * s_2[n] + 0.5 * s_3[n]$$

$$s_1[n] = q[n] + s_1[n-1]$$

$$s_2[n] = s_1[n] + s_2[n-1]$$

$$s_3[n] = s_2[n] + s_3[n-1]$$

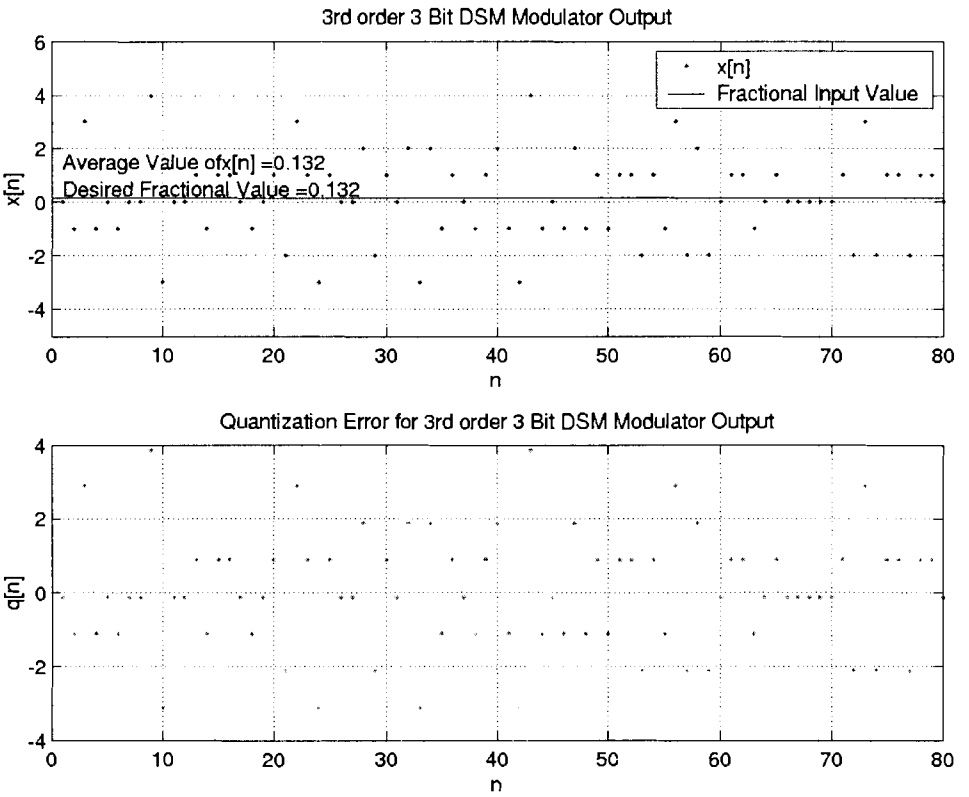
$$q[n] = f[n] - x[n]$$

As discussed in [6], the DSM structure shown in Figure 3-4 has been verified through simulation to generate valid output sequences $x[n]$ for constant values of $f[n] = f$ beyond the range $0 \leq f \leq 1$.

3.5.2 Demonstration Plots of Figure 3-4 DSM Operation

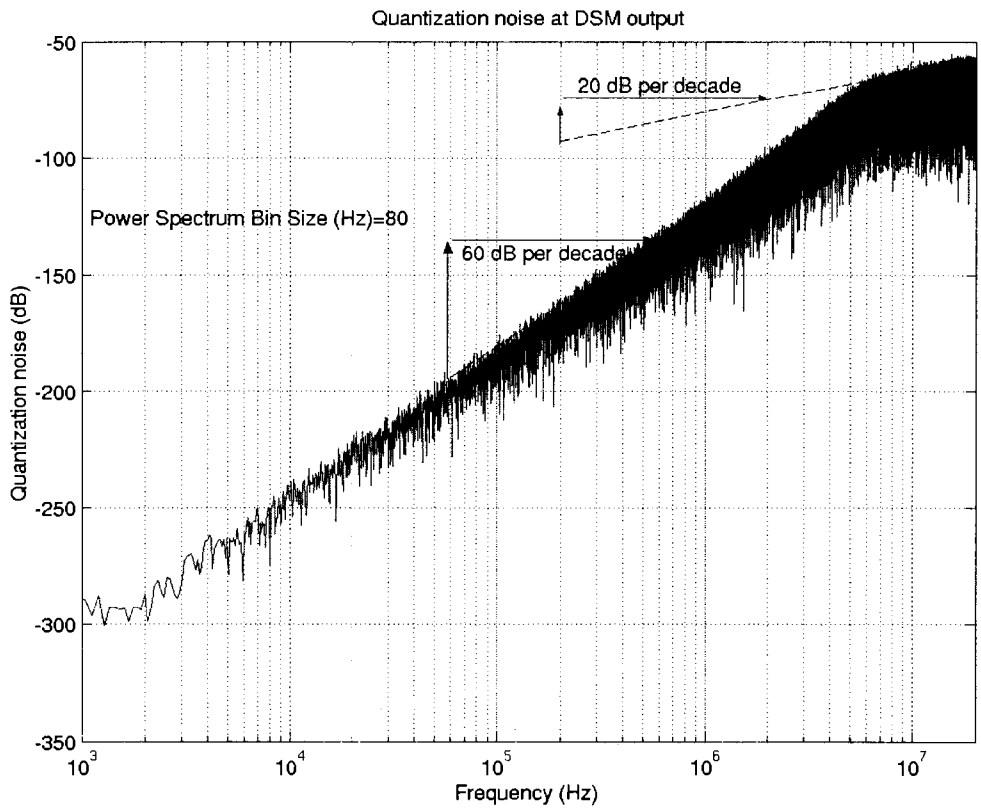
In order to pursue PLL phase noise analysis, the DSM structure shown in Figure 3-4 was implemented as a Matlab procedure and long $x[n]$ sequences were generated. A sample plot of the $x[n]$ sequence is provided in the following figure.

Figure 3-5 Third order DSM sample output modulation sequence generated in Matlab



Under the assumption that the DSM uses a sampling rate of 40MHz, power spectral density of the quantization error sequence ($q[n]$) is plotted in the following figure for the bandwidth 1kHz to 20MHz. $q[n]$ is simply the difference between $x[n]$ and f.

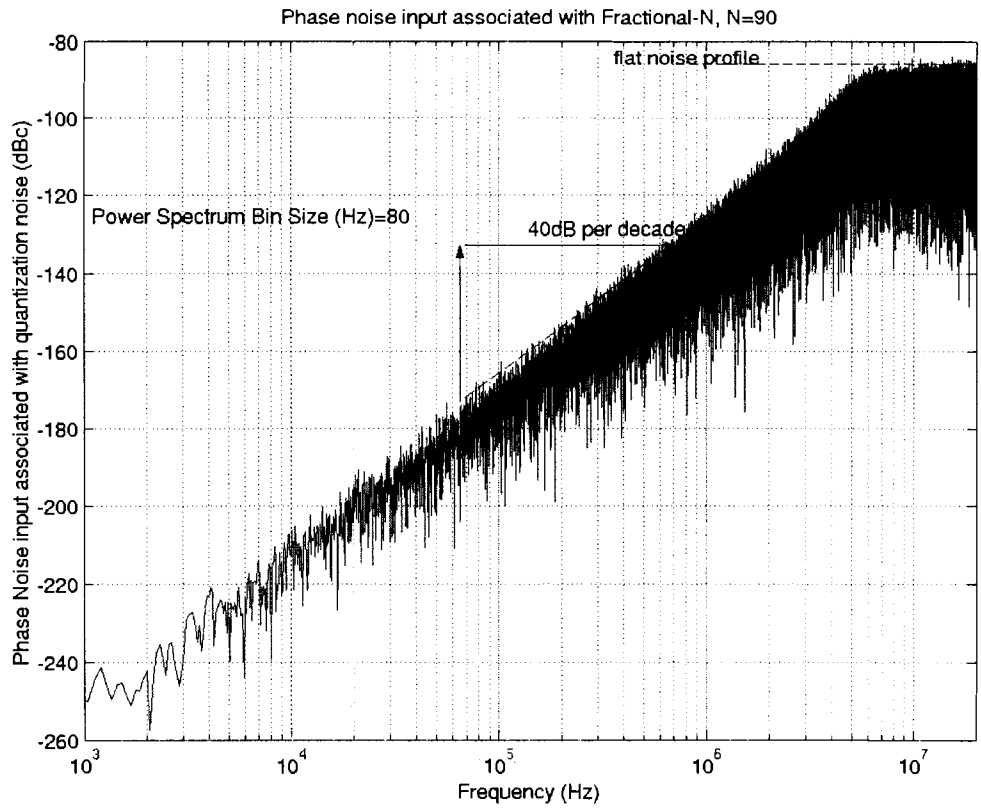
Figure 3-6 Third order DSM sample quantization noise spectrum (error between $x[n]$ and f)



While there is some relationship between the value of f and the quantization noise, the quantization noise represented in the figure above is representative of the quantization noise observed for most fractional input values.

If the $x[n]$ sequence with quantization noise shown above is used to control a flexible feedback counter and a value $N = 90$ is assumed, the power spectrum of the zero mean phase shift error term ($\Theta_{FRAC\_NOISE}[n]$ as discussed in Section 3.4) can be plotted. The power spectrum shown in the following figure plots the power spectrum in dBc within bin sizes of 80 Hz.

Figure 3-7 Third order DSM input phase noise power spectrum (N=90)



Due to the accumulation operation discussed in Section 3.4 that is used to model the input phase error term cause by DSM quantization noise, the power spectrum of $\Theta_{FRAC\_NOISE}[n]$ is shaped to emphasize lower frequency content by a shaping characteristic of 20 dB per decade relative to the power spectrum of quantization noise shown in Figure 3-6.

4 PLL NOISE THEORY, INTEGRATED 0.18 μm CMOS PLL NOISE SOURCES

RF clock phase noise is a critical characteristic for 802.11a/b/g/n transceivers; one key aspect of RF clock phase noise that is relevant for 802.11 a/b/g communications is the total phase noise power within offsets from the RF frequency of 1kHz to 10MHz (however, for the forthcoming 802.11 n standard, RMS phase noise out to 20MHz is also relevant, so the bandwidth considered in this analysis is 1kHz to 20MHz). Integrated 0.18μm CMOS 802.11 a/b/g frequency synthesizers typically exhibit RMS phase error within this bandwidth of approximately 1^{o}(e. g. [7] and [8]). While contributions to PLL output phase noise from fractional-N activity could be a significant portion of total phase noise power at offsets between 1kHz and 20MHz, there are a number of other major noise sources in a realistic integrated 0.18μm CMOS PLL that must also be considered. The PLL implementation that would minimize output phase noise power related to fractional-N effects would not be the minimum total phase noise power implementation. This section includes discussion of overall PLL noise sources and noise transfer functions to the PLL output.

4.1 PLL Implementation Considerations

The third order charge pump PLL model presented in Section 2 has eight parameters, k_{VCO}, k_{PDCP}, $R_1 / R_2 / C_1 / C_2 / C_3$, and N.

4.1.1 k_{VCO}

Generally k_{VCO} is a fixed parameter for a particular design, dictated by the required VCO functionality. Over variations in IC characteristics (including fabrication process variations, temperature variations, and power supply voltage variations), the nominal operation frequency of the VCO will shift significantly. The VCO must have sufficient frequency tuning range to achieve the desired PLL operation frequency; this dictates the lower bound on the value of k_{VCO}. Generally lower k_{VCO} is desirable because lower phase noise VCO designs are achievable with a low k_{VCO} and a low k_{VCO} also minimizes the gain from loop filter output noise to the PLL output. Therefore k_{VCO} is set to the minimum value that allows the VCO to be tuned to the desired operating frequency over variations in IC characteristics. For PLL implementation discussed in Section 5 the nominal k_{VCO} value is $(2\pi)150MHz/V$.

4.1.2 $R_1 / R_2 / C_1 / C_2 / C_3$

$C_1 / C_2 / C_3$ are adjustable parameters to consider in PLL implementation. An upper bound on the total amount of capacitance is necessary in an integrated PLL due to silicon area required for integrated capacitors. 1.5nF of capacitance in a typical 0.18μm CMOS process requires approximately 0.3 mm^2 of silicon area, which is a reasonable maximum size of area to dedicate to loop filter capacitance (overall area for the PLL design is discussed in this report is approximately 1.0 mm^2).

R_1 and R_2 are also adjustable parameters to consider in PLL implementation. Reasonably accurate resistance smaller than $100\,\Omega$ and above $100\,k\Omega$ can be achieved in a typical 0.18μm CMOS process. This range covers the useful loop filter resistor magnitudes for the PLL implementation discussed in Section 5.

4.1.3 k_{PDCP}

k_{PDCP} can be considered to be an adjustable parameter in PLL implementation. CP structures can be implemented with charge pump output current magnitudes as low as $50\,\mu$A and higher than 2mA, yielding k_{PDCP} in the range $50\mu A/2\pi$ to $2mA/2\pi$. The low side of this range is dictated by charge pump noise considerations; the upper side of the range is limited by concerns about the large switching currents that can be introduced in the integrated circuit by large charge pump output circuitry.

4.1.4 N

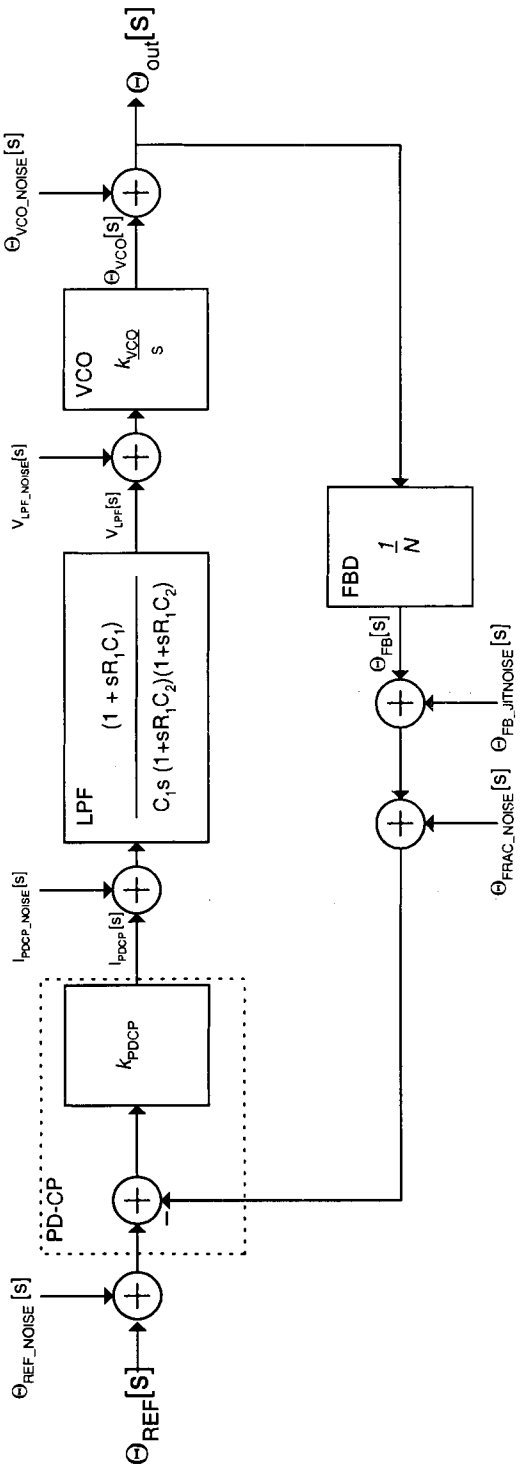
The reference frequency to the PLL can be generated at frequencies roughly at or below 40MHz (the upper limit on the reference frequency is related to the method used to generate high quality reference signals). Noise sources in the feedback path, reference input, and PD-CP are transferred to the PLL output with a power gain proportional to N^2 (as shown in Sections 4.3.2), so in 802.11 a/b/g/n RF frequency generation applications the maximum practical value of reference frequency, 40MHz, is often used to minimize the value of N. 40MHz is the reference frequency for the PLL implementation discussion in Section 5.

Furthermore, the PLL phase noise implementation doesn't necessarily have to operate with a PLL output frequency at the RF frequency. For the PLL implementation exercise discussed in Section 5, the underlying PLL structure generated output frequencies at 2/3 the RF channel rate for 802.11 a/n RF channels between 5GHz and 6GHz, and the PLL generated output frequencies at 4/3 the RF channel rate for 802.11 b/g/n RF channels between 2.4 and 2.7GHz. Following the PLL, a frequency translation circuit is used to generate the RF frequency from the 2/3 or 4/3 RF frequency generated by the PLL. The resulting range of required PLL output frequencies is 3.2GHz to 4.0GHz, which in conjunction with a fixed 40MHz reference frequency corresponds to N values of 80 to 100. A nominal N value of 90 is used in the PLL phase noise optimization exercise in Section 5; the considerations for PLL implementation over the full range of N are also discussed.

4.2 Third Order Charge Pump PLL Model with Noise Sources

The following figure shows the third order charge pump PLL model presented in Section 2 with the addition of six noise sources: VCO phase noise, reference oscillator phase noise, fractional-N phase noise, PD-CP output current noise, loop filter output voltage noise, and feedback divider timing jitter. The noise sources are discussed in further detail in the following subsections.

Figure 4-1 Third order charge pump PLL model with noise sources

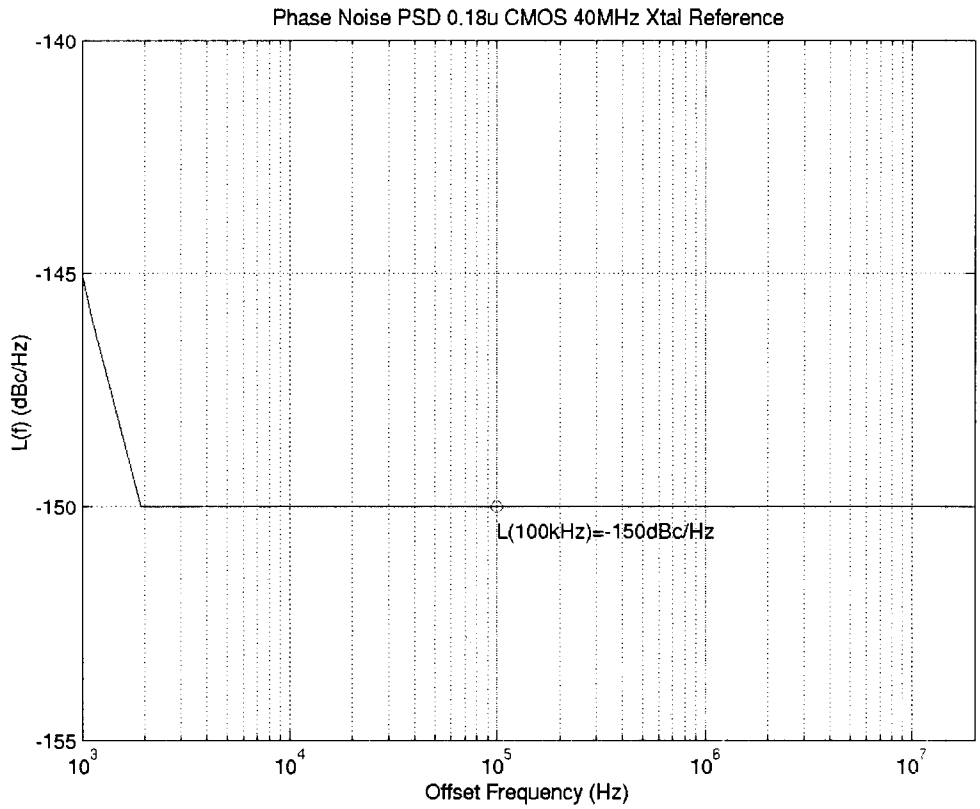


4.2.1 Reference Phase Noise

In fractional-N frequency synthesizing PLLs for 802.11a/b/g/n applications, the reference oscillator signal is typically generated using a 20MHz or 40MHz crystal oscillator circuit. Such circuits take advantage of the extremely high quality LC tanks provided by an external quartz-based component and provide a very low close in phase noise characteristic ([9]).

The phase noise performance of the 40MHz reference oscillator used for the 802.11 a/b/g/n PLL implementation presented in Section 5 is provided in the following figure. The phase noise profile is based on the results of SpectreRF phase noise simulations of a 0.18μm CMOS crystal driver circuit and an external crystal component model simulated under typical conditions.

Figure 4-2 40MHz 0.18μm CMOS crystal oscillator reference phase noise

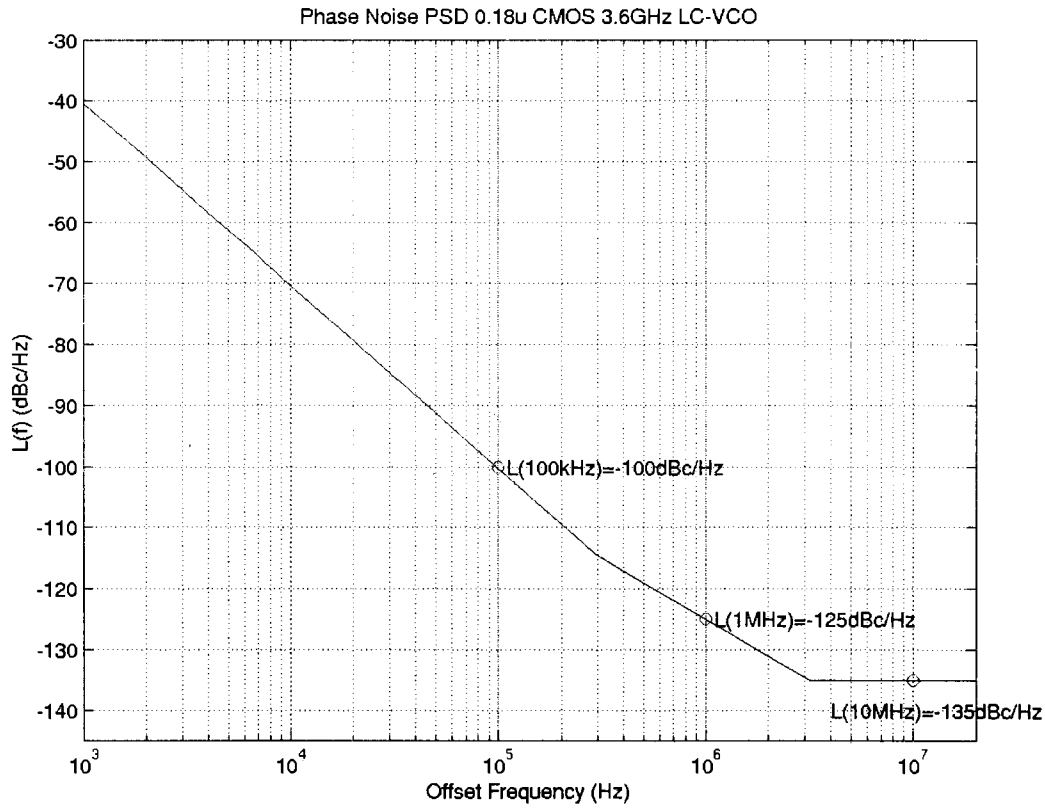


4.2.2 VCO Phase Noise

Integrated 802.11 a/b/g/n synthesizers typically use LC VCO structures such as those discussed in [7] and [8]. CMOS LC oscillator phase noise characteristics and the underlying causes of CMOS LC oscillator phase noise are discussed in [10]. Practical LC VCO structures generally exhibit a phase noise decay proportional to $1/f^3$ at low offset frequencies, followed by a region where phase noise decays at $1/f^2$, followed by a flat noise floor.

The phase noise of the 3.6GHz 0.18μm CMOS LC VCO with a noiseless control voltage input is presented in the following figure, this is the VCO phase noise used to determine the PLL implementation presented in Section 5. The phase noise profile is based on SpectreRF phase noise simulations of a 3.6GHz 0.18μm CMOS LC VCO.

Figure 4-3 3. 6GHz 0.18μm CMOS LC VCO phase noise



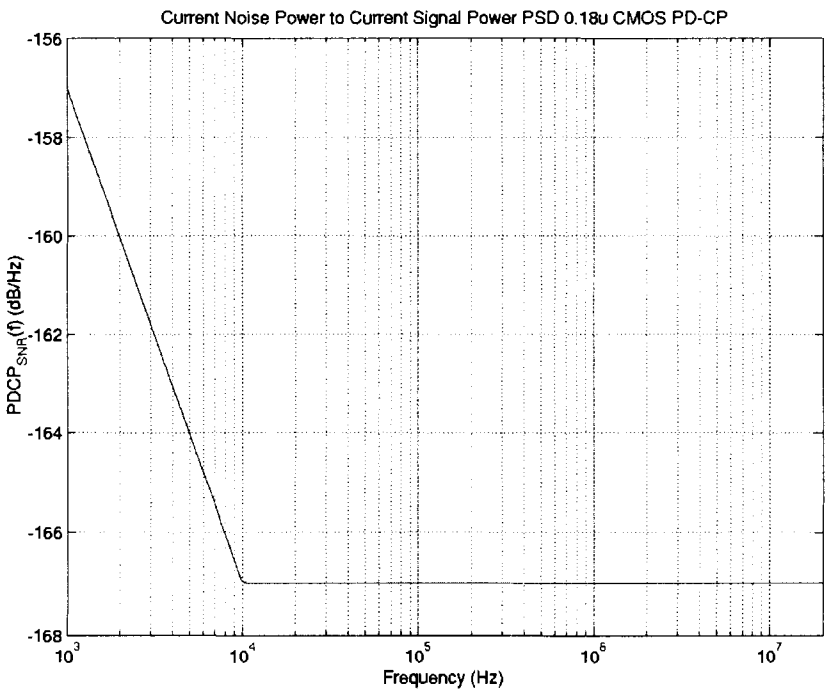
4.2.3 PD-CP Output Current Noise

A number of affects within the PD-CP add together to create the affect of PD-CP output current noise. The dominant source of PD-CP noise is typically the flicker noise and thermal noise of the actual MOS devices in the current sink and current source of the

CP output driver stage; when the PD-CP gain is adjusted by scaling up the number of parallel output stages, these noise sources' power is scaled up proportional to the number of output stages.

PD-CP output current noise power for a $200\mu A$ CP is plotted in the following figure, scaled by $1/(200\mu A)^2$. For PLL implementations considered in Section 5 with CP current magnitudes other than $200\mu A$, noise power is assumed to scale relative to the CP current magnitude. The PD-CP current noise profile is based on SpectreRF noise simulations of the average level of PD-CP output current noise simulated over a typical PD-CP activity period.

Figure 4-4 PD-CP output current noise scaled by $1/(200\mu A)^2$

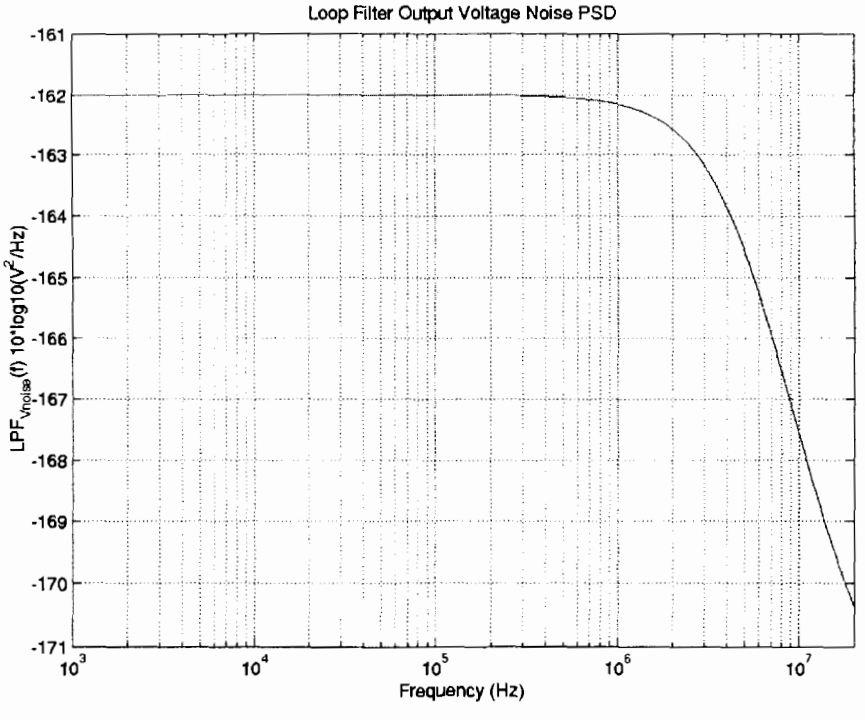


4.2.4 Loop Filter Output Voltage Noise

The loop filter for a third order charge pump PLL ideally consists of only passive resistive and capacitative elements. In this scenario, loop filter output voltage noise is simply the result of thermal noise present in the loop filter resistors.

The two loop filter resistors each exhibit equivalent white thermal voltage noise of $< v_{noise1}^2 >= 4kTR_1\Delta f$ and $< v_{noise2}^2 >= 4kTR_2\Delta f$. Each of these white voltage noise contributors is shaped by the loop filter and can be calculated as an equivalent loop filter output voltage noise term. For the demonstration loop filter component values used in Section 2.3.1, and assuming a temperature of 75°C, loop filter equivalent output voltage noise is plotted in the following figure.

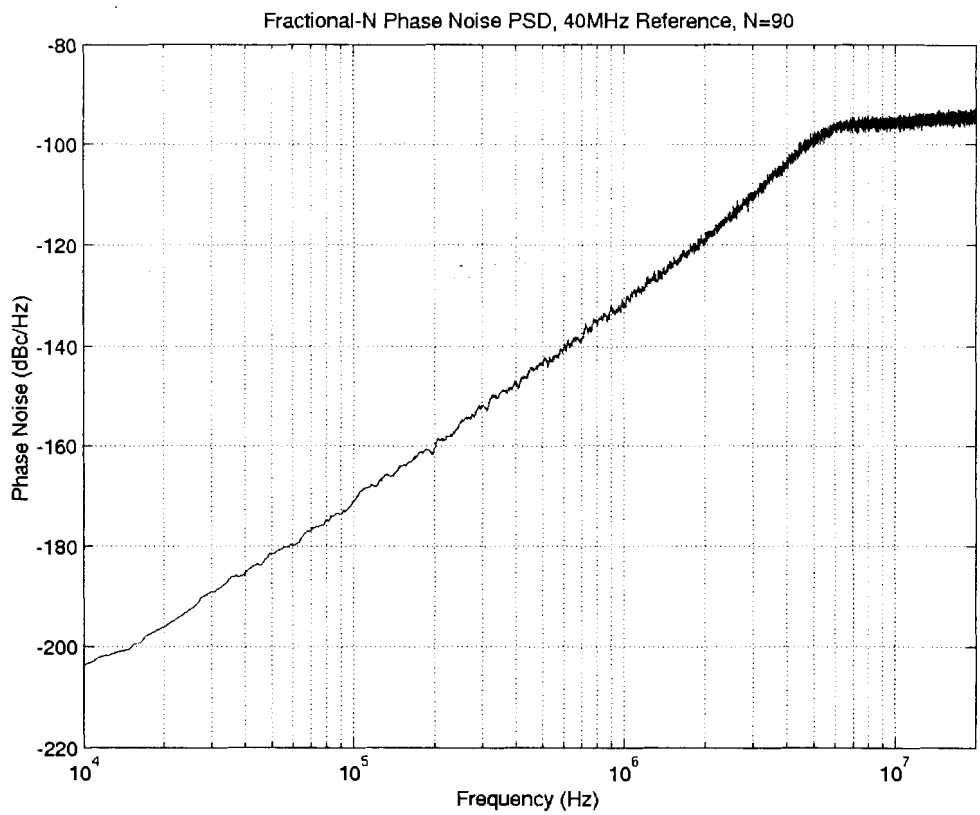
Figure 4-5 LPF output voltage noise spectrum for sample loop filter resistor characteristics



4.2.5 Fractional-N Phase Noise

Fractional-N phase noise modelling was discussed in Section 3. Fractional-N phase noise input depends on the value of N and the fractional-N feedback modulation method. The fractional-N feedback phase noise spectrum assumed for the PLL optimization presented in Section 5 is based on the DSM modulator discussed in section 3.5.

Figure 4-6 Fractional-N input phase noise



The fractional input phase noise profile plotted in the figure was calculated using significant PSD smoothing operations and was scaled to present noise power in units of

dBc per Hz. In order to calculate total output PLL phase noise power, the average spectral distribution of noise power is the information required, this is not affected by the smoothing operations performed.

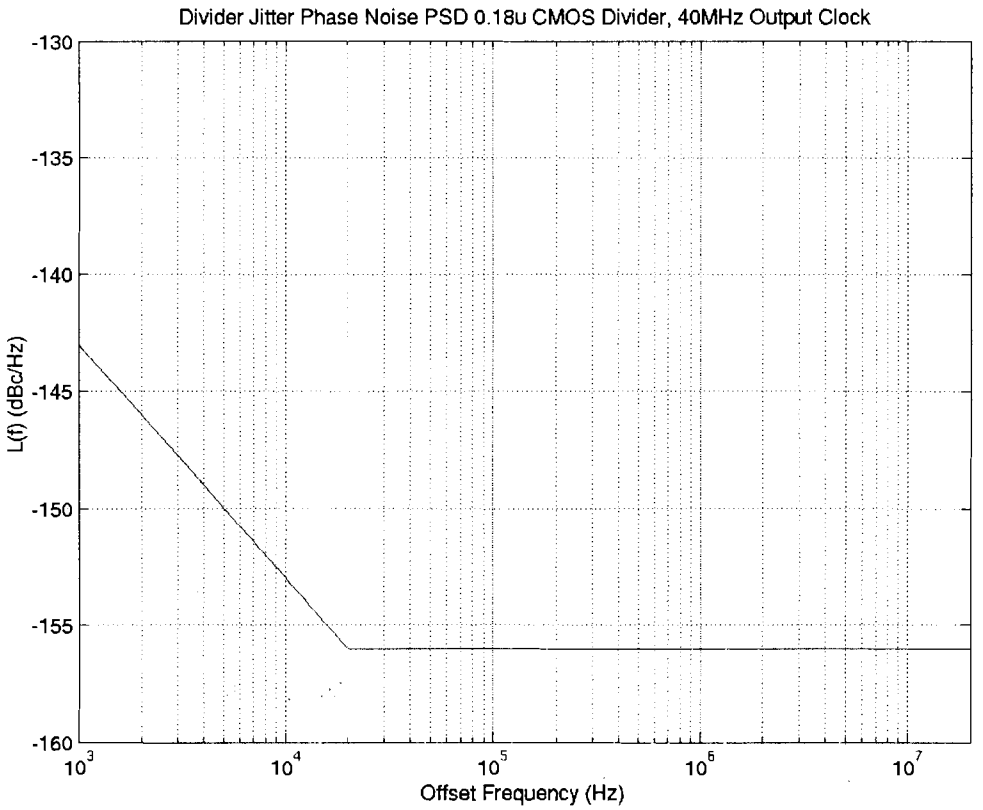
Although it is outside of the scope of this discussion, the maximum power of any phase noise spur is also a critical specification in 802.11 a/b/g/n applications, and fractional-N phase noise must be analyzed to ensure that spurious behaviour from the fractional-N activity doesn't violate maximum spur magnitude specifications. In order to investigate the maximum spur power associated with fractional-N activity it would not be acceptable to apply artificial smoothing operations during PLL noise analysis.

4.2.6 Feedback Divider Timing Jitter

Aside from the phase noise effects associated with switching the feedback counter between different values (e.g. N or $N+1$), there is also a timing jitter effect at the feedback divider output. If the feedback counter is in a fixed configuration, and if the counter is used to generate a fixed 40MHz output clock, the 40MHz output clock will still include a small amount of phase noise due to device noise within the counter circuit. The divider jitter considered during the PLL optimization exercise of Section 5 is provided in the following figure.

The feedback divider timing jitter phase noise profile is based on SpectreRF phase noise simulations of a 0.18μm CMOS configurable feedback divider operating in a fixed Count-to-N configuration.

Figure 4-7 Feedback divider output clock phase noise



4.3 Third Order Charge Pump PLL Noise Transfer Functions

Each of the six noise sources described in Section 4.2 experiences a particular transfer function from the addition point of the noise source to the PLL output. The transfer functions from each of the six noise sources to the PLL output are presented in the following subsections.

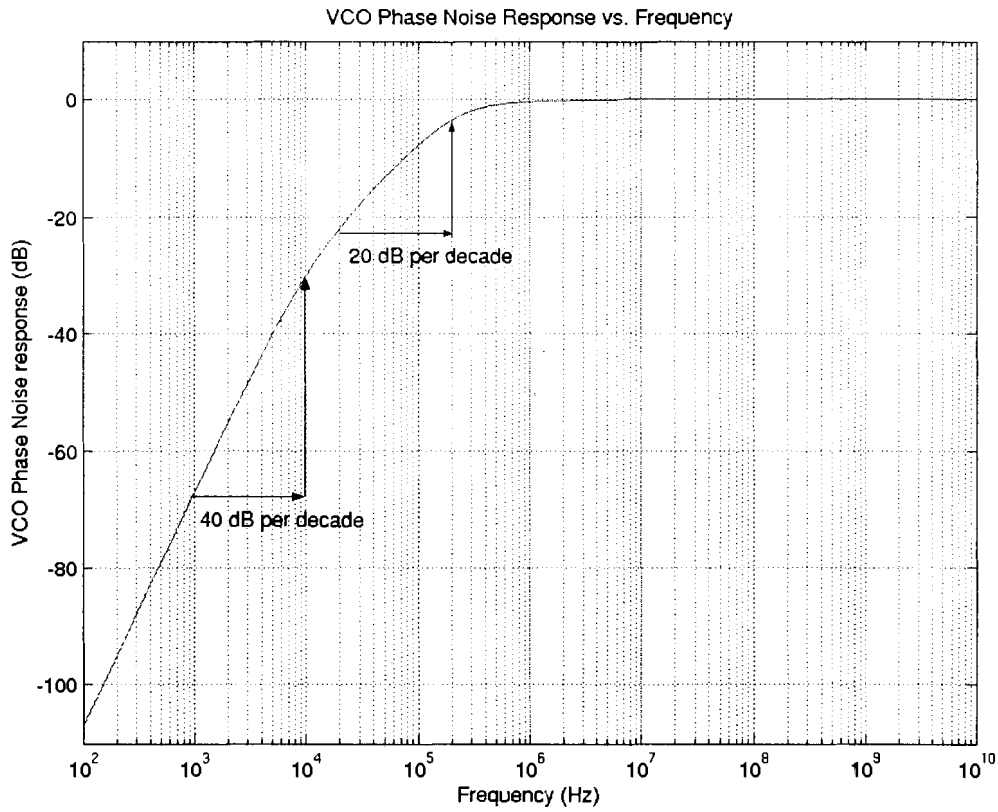
4.3.1 VCO Phase Noise Transfer Function

The transfer function from the VCO phase output ($\Theta_{VCO}[s]$) or the VCO phase noise ($\Theta_{VCO\_NOISE}[s]$) to the PLL output ($\Theta_{OUT}[s]$) is given by

$$G_{VCO}[s] = \frac{\Theta_{OUT}[s]}{\Theta_{VCO}[s]} = \frac{1}{1 - \frac{H_{PDCP}[s] * H_{LPF}[s] * H_{VCO}[s]}{N}} = \frac{\Theta_{OUT}[s]}{\Theta_{VCO\_NOISE}[s]}$$

For the test case PLL characteristics discussed in Section 2.3.1, the magnitude of the transfer function $G_{VCO}[s]$ is plotted in the following figure.

Figure 4-8 VCO output phase to PLL output transfer function magnitude



The $G_{VCO}[s]$ transfer function exhibits a high pass characteristic; attenuation decreases at 40 dB per decade at frequencies below the zero at ω_z and decreases at 20 dB

per decade at frequencies above ω_z but below the PLL bandwidth. At higher frequencies the VCO phase noise is passed directly to the PLL output with a gain of 0 dB.

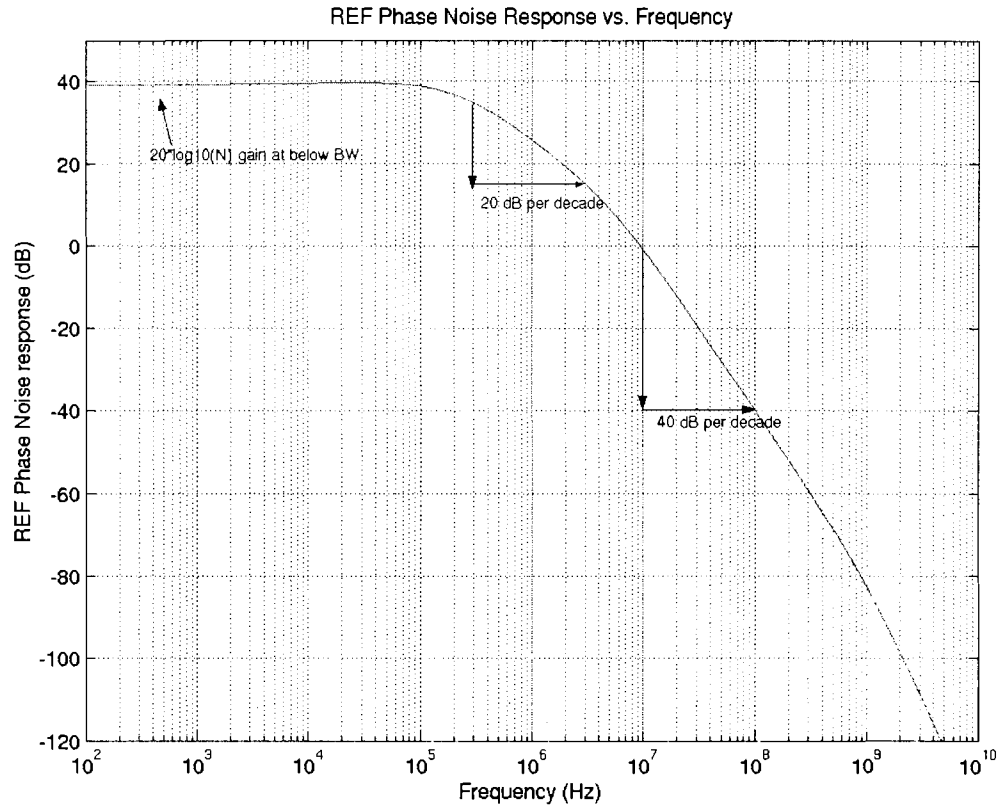
4.3.2 Reference Phase Noise Transfer Function

The transfer function from the reference phase input ($\Theta_{REF}[s]$) or the reference phase noise ($\Theta_{REF\_NOISE}[s]$) to the PLL output ($\Theta_{OUT}[s]$) is given by

$$G_{REF}[s] = \frac{\Theta_{OUT}[s]}{\Theta_{REF}[s]} = \frac{H_{PDCP}[s] * H_{LPF}[s] * H_{VCO}[s]}{1 - \frac{H_{PDCP}[s] * H_{LPF}[s] * H_{VCO}[s]}{N}} = \frac{\Theta_{OUT}[s]}{\Theta_{REF\_NOISE}[s]} = H_{PLL}[s]$$

For the test case PLL characteristics discussed in Section 2.3.1, the magnitude of the transfer function $G_{REF}[s]$ is plotted in the following figure.

Figure 4-9 Reference phase to PLL output transfer function magnitude



The transfer function $G_{REF}[s]$ exhibits a low pass characteristic; reference phase noise below the PLL bandwidth is passed directly to the PLL output with a gain of $20\log_{10}(N)$ dB. For frequencies above the PLL bandwidth and below the pole at ω_{P1}, attenuation increases at 20 dB per decade. Gain rolls off at 40 dB per decade at frequencies between the poles ω_{P1} and ω_{P2}. At frequencies above the ω_{P2} pole, attenuation increases at 60 dB per decade.

4.3.3 Fractional-N Phase Noise or Feedback Divider Jitter Phase Noise Transfer Function

The transfer function from the feedback phase ($\Theta_{FB}[s]$) to the PLL output ($\Theta_{OUT}[s]$) is given by

$$G_{FB}[s] = \frac{\Theta_{OUT}[s]}{\Theta_{FB}[s]} = \frac{-H_{PDCP}[s]*H_{LPF}[s]*H_{VCO}[s]}{1-\frac{H_{PDCP}[s]*H_{LPF}[s]*H_{VCO}[s]}{N}} = -G_{REF}[s]$$
$$= \frac{\Theta_{OUT}[s]}{\Theta_{FB\_JITTER}[s]} = \frac{\Theta_{OUT}[s]}{\Theta_{FRAC\_NOISE}[s]}$$

This is also the transfer function from the fractional-N phase noise ($\Theta_{FRAC\_NOISE}[s]$) or feedback divider jitter ($\Theta_{FB\_JITTER}[s]$) phase noise to the PLL output.

For the test case PLL characteristics discussed in Section 2.3.1, the magnitude of the transfer function $G_{FB}[s]$ is plotted in Figure 4-9 ($G_{FB}[s] = -G_{REF}[s]$), and the characteristics of the transfer function are discussed in Section 4.3.2.

4.3.4 PD-CP Noise Transfer Function

The transfer function from the PD-CP output current ($I_{PDCP}[s]$) or the PD-CP output current noise ($I_{PDCP\_NOISE}[s]$) to the PLL output ($\Theta_{OUT}[s]$) has units of radians per amp. The gain is given by

$$G_{PDCP}[s] = \frac{\Theta_{OUT}[s]}{I_{PDCP}[s]} = \frac{H_{LPF}[s]*H_{VCO}[s]}{1-\frac{H_{PDCP}[s]*H_{LPF}[s]*H_{VCO}[s]}{N}} = \frac{G_{REF}[s]}{H_{PDCP}[s]} = \frac{\Theta_{OUT}[s]}{I_{PDCP\_NOISE}[s]}$$

Given that the transfer function of the PD-CP ($H_{PDCP}[s]$) is simply a constant value ($H_{PDCP}[s] = k_{PDCP}$), the transfer function from the PD-CP output to the PLL output is equal to the gain from the reference input to the PLL output ($G_{REF}[s]$) scaled by $\frac{1}{k_{PDCP}}$. For the test case PLL characteristics discussed in Section 2.3.1, the magnitude of the transfer function $G_{REF}[s]$ is plotted in the Figure 4-9, and the characteristics of the transfer function are discussed in Section 4.3.2.

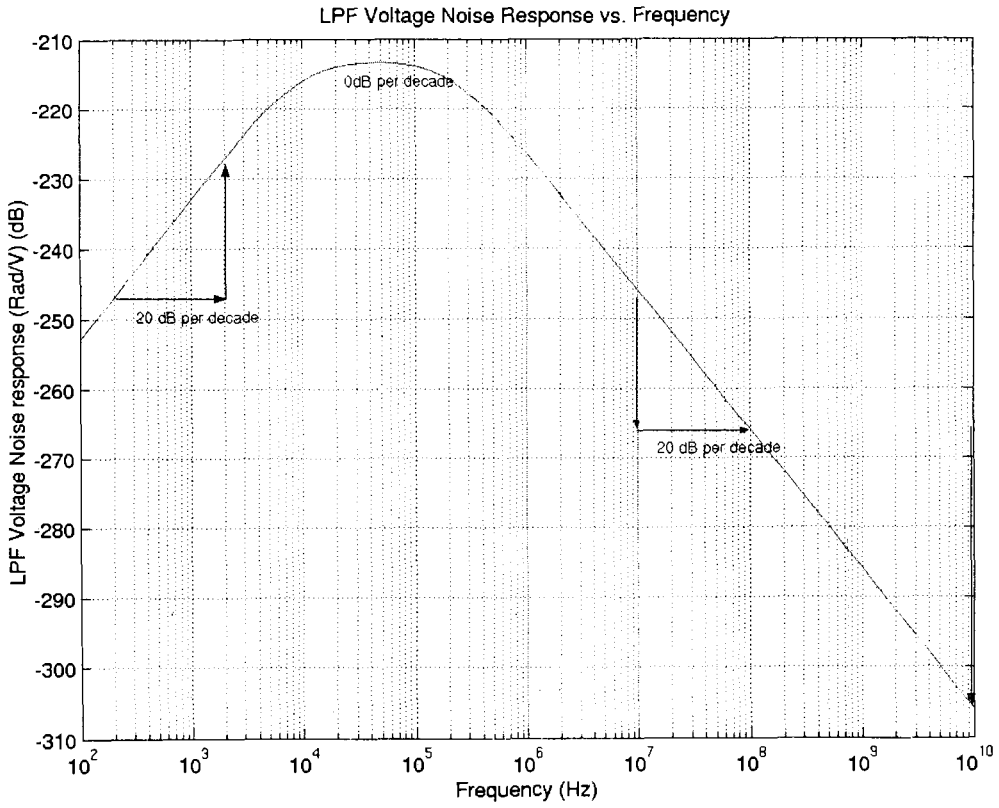
4.3.5 LPF Noise

The transfer function from the loop filter output voltage node ($V_{LPF}[s]$) or the loop filter output voltage noise ($V_{LPF\_NOISE}[s]$) to the PLL output ($\Theta_{OUT}[s]$) has units of radians per volt. The gain is given by

$$G_{LPF}[s] = \frac{\Theta_{OUT}[s]}{V_{LPF}[s]} = \frac{H_{VCO}[s]}{1 - \frac{H_{PDCP}[s] * H_{LPF}[s] * H_{VCO}[s]}{N}} = \frac{\Theta_{OUT}[s]}{V_{LPF\_NOISE}[s]}$$

For the test case PLL characteristics discussed in Section 2.3.1, the magnitude of the transfer function $G_{LPF}[s]$ is plotted in the following figure.

Figure 4-10 Loop filter output to PLL output transfer function magnitude



The transfer function $G_{LPF}[s]$ exhibits a band pass characteristic; loop filter output voltage noise below the zero at ω_Z experiences attenuation that decreases at 20 dB per decade as frequency increases. At frequencies between the zero at ω_Z and the PLL bandwidth, loop filter output voltage noise experiences a constant gain that is proportional to k_{VCO}. For frequencies above the PLL bandwidth, attenuation increases at 20 dB per decade.

5 OPTIMIZATION

As discussed in Section 4.1, the variable parameters in PLL implementation are the loop filter components $R_1 / R_2 / C_1 / C_2 / C_3$ and the PD-CP gain k_{PDCP}; the nominal value of $k_{VCO} = 2\pi * 150 MHz/V$ is a fixed parameter determined by VCO design considerations and the nominal value of $N = 90$ will be the nominal feedback coefficient considered. In this section the process of determining ideal values for the variable PLL parameters is presented.

5.1 Optimization Target

The key performance characteristic used to determine optimal PLL implementation is the RMS phase noise at the PLL output at offsets between 1kHz and 20MHz from the PLL output frequency. This characteristic is a key performance metric for 802.11 a/b/g/n RF clock signals. The targeted performance is less than 1° RMS phase noise at offsets from the RF frequency between 1kHz and 20MHz.

As discussed in Section 4.1.4, the PLL doesn't directly generate the RF clock frequency, it generates either 2/3 the RF frequency for channels between 5GHz and 6GHz or 4/3 the RF frequency for channels between 2.4GHz and 2.7GHz. As discussed in the Appendix, an ideal analog multiplier frequency scaling from 2/3RF to RF will increase the clock phase noise by a factor of 1.5x (similarly, frequency scaling from 4/3RF to RF will decrease phase noise by a factor of 1.25x). To achieve the maximum 1°

RMS phase noise target on the RF clock signal for the 5GHz to 6GHz channels the PLL output phase noise must be less than 0.67° RMS within offsets between 1kHz and 20MHz from the PLL output frequency.

Furthermore, the final PLL is expected to maintain 45° phase margin over variations in IC characteristics due to manufacturing variations and a range of operating conditions.

The noise source magnitudes considered in PLL optimization are provided in Section 4.2. The transfer functions between each of the noise sources and the PLL output phase were described in Section 4.3.

5.2 General Optimization Strategy Summary

5.2.1 Determining k_{PDCP}

In the PLL noise analysis considerations of Sections 5.3 and 5.4 the value of k_{PDCP} will be set at the value that provides the maximum possible PLL phase margin. For any particular setting of the variable loop filter parameters ($R_1 / R_2 / C_1 / C_2 / C_3$), k_{PDCP} will be adjusted to ensure the PLL loop gain's unity magnitude frequency will occur at approximately the same frequency as the PLL loop gain's maximum phase shift. The purpose of this constraint is to ensure that over variations in IC characteristics, the maximum degradation in PLL phase margin is well controlled. The assumption will be discussed further in Section 5.6.

5.2.2 Determining $\omega_Z / \omega_{P1} / \omega_{P2}$ Before Determining $R_1 / R_2 / C_1 / C_2 / C_3$

If loop filter resistor noise power is neglected and if the loop filter resistances are considered temporarily fixed, it is possible to consider the loop filter as having three independent parameters ($\omega_Z / \omega_{P1} / \omega_{P2}$) instead of five independent parameters $R_1 / R_2 / C_1 / C_2 / C_3$.

$$H_{LPF}[s] \approx \frac{1}{C_1 s} * \frac{1 + sR_1C_1}{(1 + sR_1C_2)(1 + sR_2C_3)} = \frac{\omega_Z R_1}{s} * \frac{1 + s/\omega_Z}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}$$

In Section 5.3 loop filter noise is neglected and fixed loop filter resistance values of $R_1 = 3k\Omega, R_2 = 0.8k\Omega$ are used. In Section 5.4, loop filter resistor noise is introduced and the magnitudes of $R_1 / R_2 / C_1 / C_2 / C_3$ are determined using the identified $\omega_Z / \omega_{P1} / \omega_{P2}$ values determined in Section 5.3.

5.2.3 Noise Filtering Tradeoffs for $\omega_Z / \omega_{P1} / \omega_{P2}$ and PLL Bandwidth

Neglecting loop filter noise, there are three noise inputs that are added at the PD input ($\Theta_{FRAC\_NOISE}[s], \Theta_{FB\_JITTER}[s], \Theta_{REF\_NOISE}[s]$) and one noise input that can be referred to the PD input by a constant scaling factor ($I_{PDCP\_NOISE}[s]$). The noise terms that are presented at the PD input experience low pass filtering with increased attenuation if the PLL bandwidth is reduced and/or if the loop filter poles ($\omega_{P1} / \omega_{P2}$) are moved to lower frequencies. The VCO phase noise term experiences high pass filtering, with improved attenuation at low frequencies if the PLL bandwidth is increased and/or if the

loop filter zero frequency (ω_Z) is increased. However as ω_Z is increased and ω_{P1}, ω_{P2} are decreased the maximum phase shift of the PLL loop gain will be reduced, reducing the maximum achievable phase margin for the PLL.

Final determination of $\omega_Z / \omega_{P1} / \omega_{P2}$ frequencies will be a compromise between the output noise of noise sources that experience low pass filtering by the PLL and the VCO noise that experiences high pass filtering by the PLL. Also the minimum acceptable phase margin will limit the minimum distance between ω_Z, ω_{P1} and ω_{P2}.

5.3 Determining the $\omega_{P1}:\omega_Z$ and $\omega_{P2}:\omega_{P1}$ Ratios

5.3.1 With Fixed $\omega_{P2}:\omega_{P1}$=10, Investigate the Affect of $\omega_{P1}:\omega_Z$ Ratio and ω_Z, ω_{P1} Frequencies

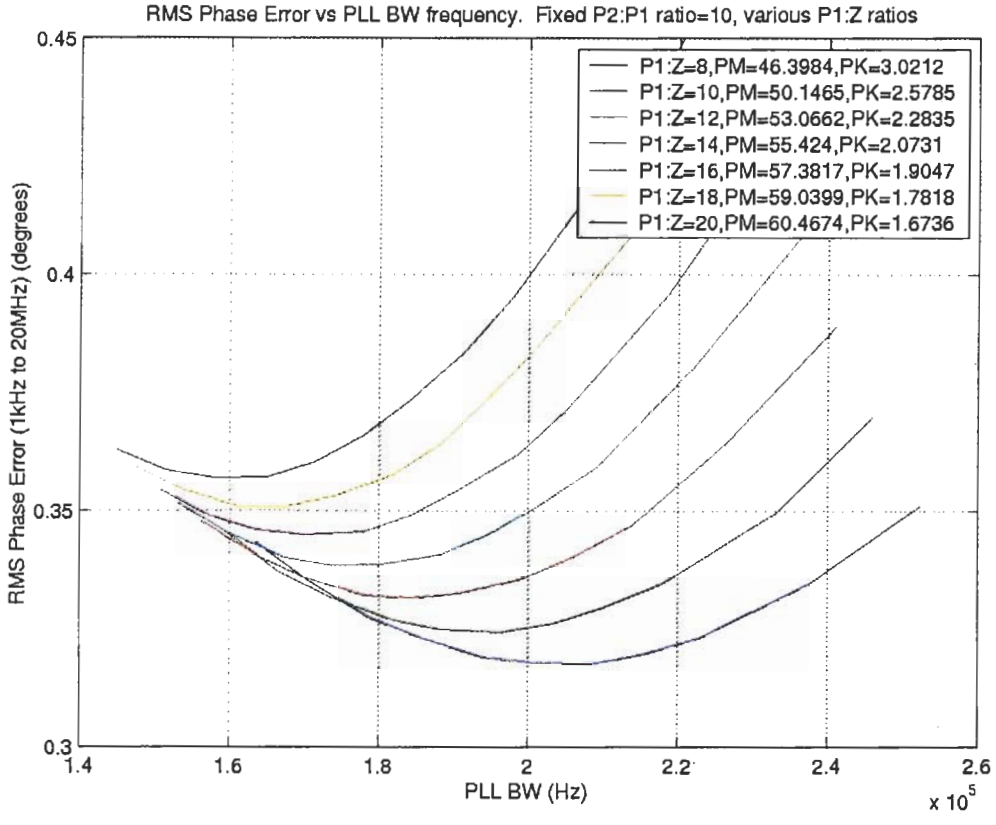
The following assumptions are made for the analysis presented in this subsection:

1. $\omega_{P2}:\omega_{P1}$ fixed at 10
2. $R_1 = 3k\Omega$ $R_2 = 0.8k\Omega$, both are noiseless
3. k_{PDCP} is adjusted to ensure maximum phase margin for any particular $\omega_Z / \omega_{P1} / \omega_{P2}$
4. $k_{VCO} = 2\pi * 150MHz/V$, $N = 90$
5. Noise source magnitudes are provided in Section 4.2

Given these assumptions, the remaining independently variable PLL parameters are the frequencies for ω_Z and ω_{P1}. For large $\omega_{P1}:\omega_Z$ ratios, the maximum phase shift of the PLL's loop gain will approach -90° and by appropriately setting k_{PDCP} as described in point 3 a PLL could be realized with phase margin approaching 90°. However, a small $\omega_{P1}:\omega_Z$ ratio is preferable because the improved roll-off in noise transfer functions associated with lower ω_{P1} (see Figure 4-9) and higher ω_Z (see Figure 4-8).

While keeping a fixed $\omega_{P2}:\omega_{P1}$ ratio of 10, various ratios of $\omega_{P1}:\omega_Z$ are set while the frequencies of ω_Z is swept over a large range. By adjusting k_{PDCP} for each considered group of $\omega_Z/\omega_{P1}/\omega_{P2}$ frequencies the maximum possible phase margin is maintained. For each of the $\omega_{P1}:\omega_Z$ ratios that is considered the phase margin is constant as the frequency of ω_Z is swept; this is because the PLL loop gain's maximum phase shift is constant for each particular fixed $\omega_{P1}:\omega_Z$ ratio. For each $\omega_{P1}:\omega_Z$ ratio we find a particular ω_Z frequency yields optimal output phase noise characteristics.

Figure 5-1 PLL output RMS phase noise (w/o loop filter noise) vs. PLL bandwidth for a range of $\omega_{P1}:\omega_Z$ ratios



In the plot above, the RMS phase noise at the PLL output is plotted for a series of $\omega_{P1}:\omega_Z$ ratios as ω_Z is swept over a range of frequencies; at each ω_Z frequency the PLL bandwidth is calculated and used as the horizontal coordinate. The output RMS phase noise at the optimum ω_Z frequency is improved monotonically as the $\omega_{P1}:\omega_Z$ ratio is swept from 20 down to 8. Additionally the phase margin achieved using the k_{PDCP} adjustment (described in point 3) decreases monotonically as the $\omega_{P1}:\omega_Z$ ratio is swept from 20 down to 8 (phase margin achieved at each $\omega_{P1}:\omega_Z$ ratio is annotated in the legend of the preceding figure).

While reductions in phase noise are realized by pushing ω_{P1} and ω_Z close together (and consequently reducing the maximum achievable phase margin), the reductions in phase noise are not large. The minimum RMS phase noise for a $\omega_{P1}:\omega_Z$ ratio of 14 is 0.34° and a phase margin of 55.4° is achieved. The RMS phase error is reduced only by 0.02° to 0.32° RMS for a $\omega_{P1}:\omega_Z$ ratio of 8 with the achieved phase margin reduced to approximately 46°.

In Section 5.6, justifications are provided to show that a reasonable lower bound on nominal PLL phase margin is ~55° in order to safely ensure that the design target of maintaining 45° phase margin is achieved over variations in IC characteristics. In order to achieve 55° phase margin with a $\omega_{P2}:\omega_{P1}$ ratio of 10, the ratio $\omega_{P1}:\omega_Z$ would be approximately 14 and the optimum PLL bandwidth value taken from Figure 5-1 is approximately 180 kHz.

5.3.2 Remove Restriction of $\omega_{P2}:\omega_{P1}$=10, Consider Other $\omega_{P1}:\omega_Z$, $\omega_{P2}:\omega_{P1}$ Ratios that Yield 55° Phase Margin

Accepted PLL design practices dictate that the pole at ω_{P2} is introduced at a frequency well above ω_{P1}. This ensures that ω_{P2} is at a frequency much higher than the loop gain's maximum phase shift frequency and therefore variations in ω_{P2} have little affect on PLL phase margin. Effects that can cause variations in ω_{P2} are discussed in Section 5.5. This accepted design practice drove the initial restriction $\omega_{P2}:\omega_{P1}$= 10, but it is useful to confirm that this design restriction didn't significantly increase the minimum achievable RMS phase error. If the restriction $\omega_{P1}:\omega_{P2}$=10 is removed,

different $\omega_{P1}:\omega_Z$ and $\omega_{P2}:\omega_{P1}$ ratio pairs that yield PLLs with achievable 55° phase margin can be considered.

For the analysis of this section the following assumptions are made:

1. $\omega_{P2}:\omega_{P1}$ and $\omega_{P1}:\omega_Z$ should be set such that the maximum phase shift of the PLL loop gain is approximately 55°. For a particular $\omega_{P1}:\omega_Z$ ratio, there is a corresponding $\omega_{P2}:\omega_{P1}$ ratio that yields ~55° maximum phase shift in the PLL loop gain.

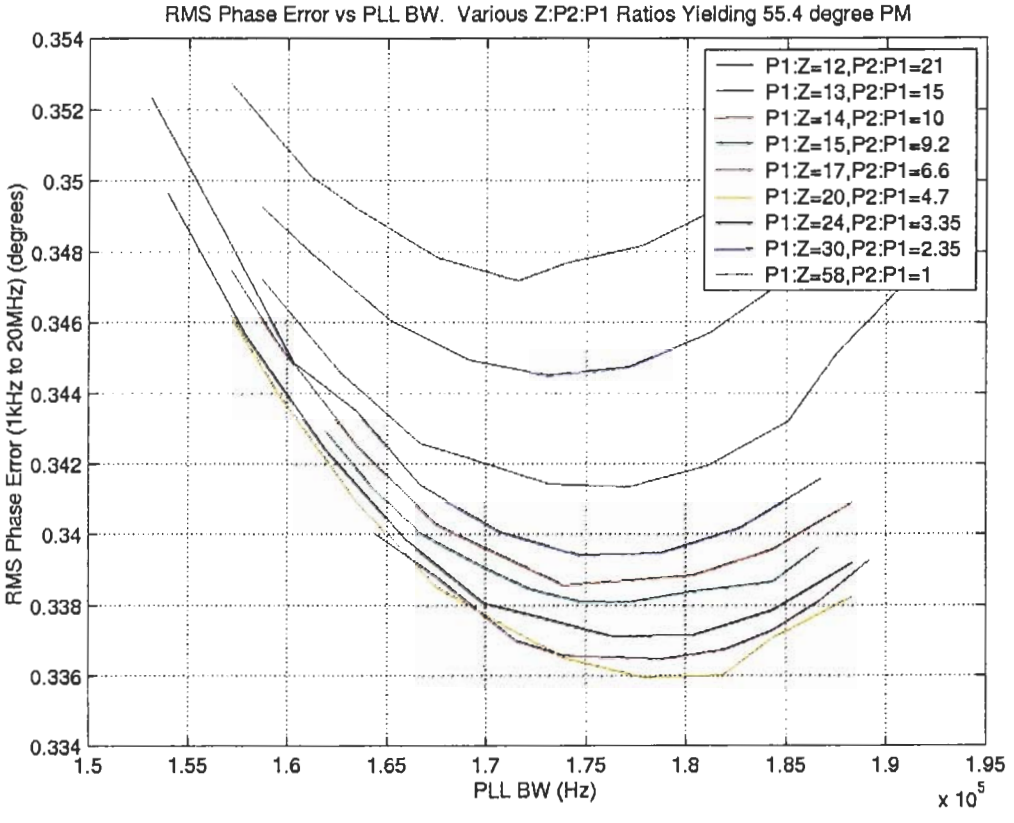
2. $R_1 = 3k\Omega$ $R_2 = 0.8k\Omega$, both are noiseless

3. k_{PDCP} is adjusted to ensure maximum phase margin for any particular $\omega_Z / \omega_{P1} / \omega_{P2}$

4. $k_{VCO} = 2\pi * 150MHz/V$, $N = 90$

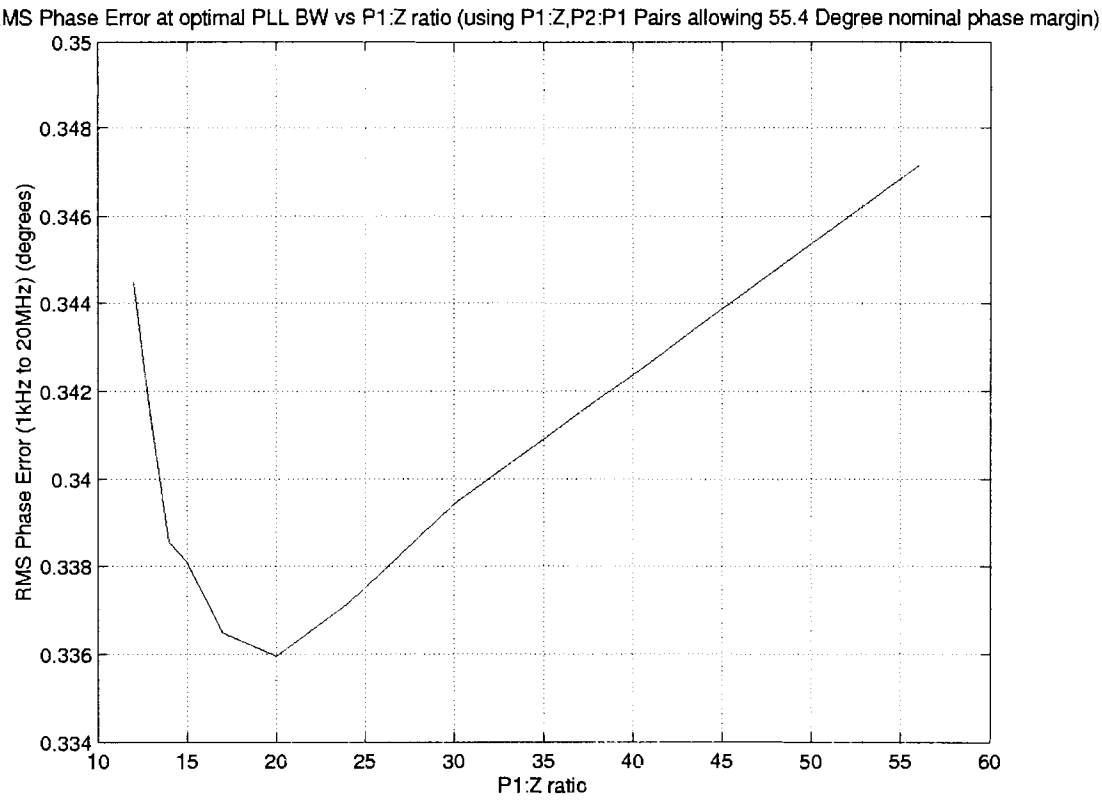
5. Noise source magnitudes are provided in Section 4.2

Figure 5-2 Figure of RMS phase noise (w/o loop filter noise) vs. PLL bandwidth for various sets of $\omega_{P1}:\omega_Z$, $\omega_{P2}:\omega_{P1}$ ratios yielding 55° phase margin



The preceding plot shows that over the ranges of $\omega_{P1}:\omega_Z$ and $\omega_{P2}:\omega_{P1}$ considered in this analysis, output phase noise at the optimal ω_Z value is slightly dependent on the ratio $\omega_{P1}:\omega_Z$. In the above plot, the horizontal axis is the PLL bandwidth achieved as ω_Z is swept. The relationship between the $\omega_{P1}:\omega_Z$ ratio implemented in this analysis and the RMS phase error at the optimal PLL bandwidth is plotted in the following figure.

Figure 5-3 Optimum RMS phase noise for PLL implementations achieving 55° phase margin



RMS phase noise in this analysis is optimized by setting the $\omega_{P1}:\omega_Z$ to approximately 20 and the $\omega_{P2}:\omega_{P1}$ ratio to approximately 4. However, these nominal ratios of loop filter characteristic frequencies results in a PLL where errors in ω_{P2} have a significant effect on loop gain maximum phase shift and therefore the achievable PLL phase margin. The achieved improvements in RMS phase noise by reducing $\omega_{P2}:\omega_{P1}$ from 10 to 4 are less than 1% (decreases from 0.339° to 0.336°), so the restriction $\omega_{P2}:\omega_{P1}$ = 10 is determined to not significantly impact output phase noise performance.

5.3.3 Selection of $\omega_{P1}:\omega_Z$, $\omega_{P2}:\omega_{P1}$ Ratios

The ratio of $\omega_{P1}:\omega_Z$ =14 and the $\omega_{P2}:\omega_{P1}$ =10 along with ω_Z =35kHz are choices for loop filter characteristic frequencies that yield reasonable nominal phase margin of 55° and achieve a near optimum RMS phase error without introducing high PLL phase margin sensitivity to the ω_{P2} frequency.

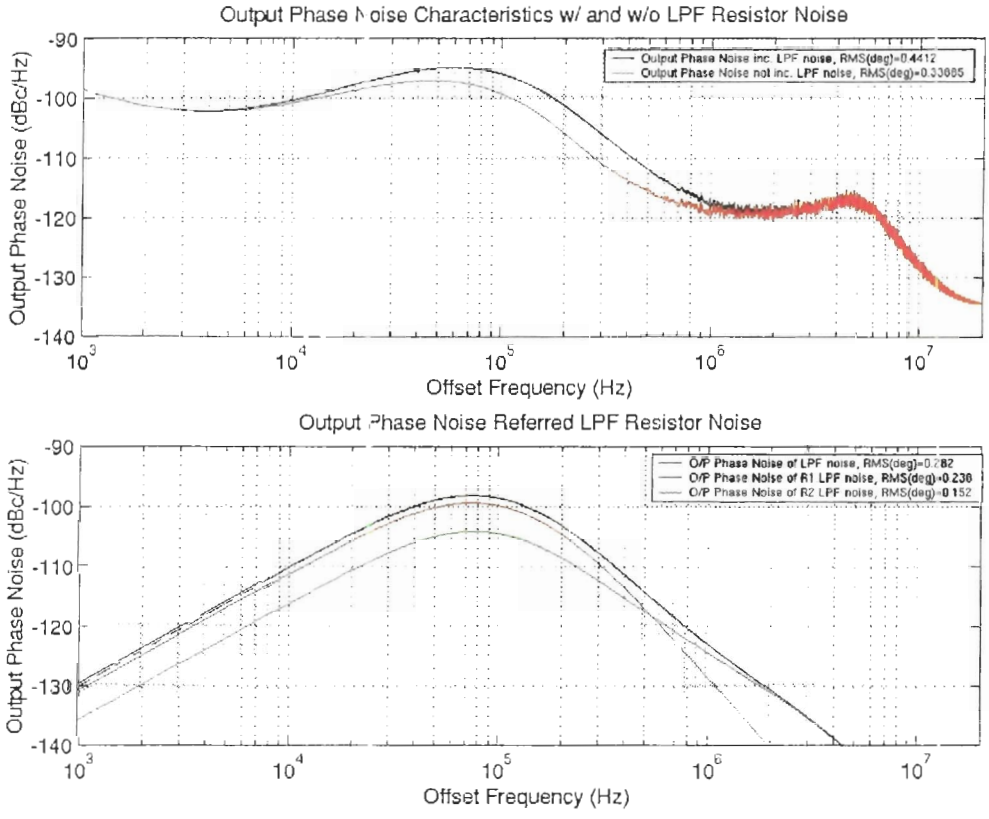
The value of k_{PDCP} is $160\mu A/2\pi$ and the resulting PLL bandwidth is approximately 180kHz.

5.4 Considerations for Loop Filter Resistor Noise

The analysis discussed in Section 5.3 used noiseless loop filter resistors with magnitudes of $R_1 = 3k\Omega$ $R_2 = 0.8k\Omega$. The following figure plots phase noise characteristics under the following assumptions:

1. $\omega_{P2}:\omega_{P1}$=10, $\omega_{P1}:\omega_Z$=14, ω_Z=35kHz
2. $R_1 = 3k\Omega$ $R_2 = 0.8k\Omega$, resistor noise is included, temperature is 75°C
3. k_{PDCP} is adjusted to ensure maximum phase margin, which means $160\mu A/2\pi$ for this case
4. $k_{VCO} = 2\pi * 150MHz/V$, $N = 90$
5. Noise source magnitudes are provided in Section 4.2

Figure 5-4 Output phase noise spectrum with and without resistor noise



For a particular set of $\omega_{P2}, \omega_{P1}, \omega_Z$ frequencies, loop filter output noise power from each of the resistors can be shown to be proportional to the value of that resistance. In order to reduce the contribution of each resistor while not affecting the $\omega_{P2}, \omega_{P1}, \omega_Z$ frequencies, the magnitude of the respective resistor must be decreased while inversely increasing the associated capacitance to maintain the $\omega_{P2}, \omega_{P1}, \omega_Z$ frequencies.

R_2 is set at 800Ω and the resulting contribution of R_2 to the PLL output phase noise power is approximately 10 % of the total output noise power (see RMS phase error values in the preceding figure annotation). Reduction of R_2 is not pursued because due to loop filter programmability (not shown in Figure 2-3) part of R_2 is implemented using

a CMOS switch that has variable resistance. Reducing R_2 below 800Ω would cause the value of R_2 to be too dependent on the highly variable switch resistance.

R_1 is set to $3k\Omega$ and the corresponding loop filter output noise power produces a significant portion of PLL output phase noise power (approximately 25%). However, if loop filter phase noise power from R_1 was to be halved while maintaining the same $\omega_{P2}, \omega_{P1}, \omega_Z$ frequencies, the value of C_1 would need to increase from 1.5nF to 3nF and the PLL area would grow by approximately 30% in order to accommodate the increased C_1 value. Total output RMS phase noise would decrease by only about 10% as a result. The trade off between PLL phase noise and PLL silicon area dictates that the noise introduced by the $R_1 = 3k\Omega$ resistor is acceptable.

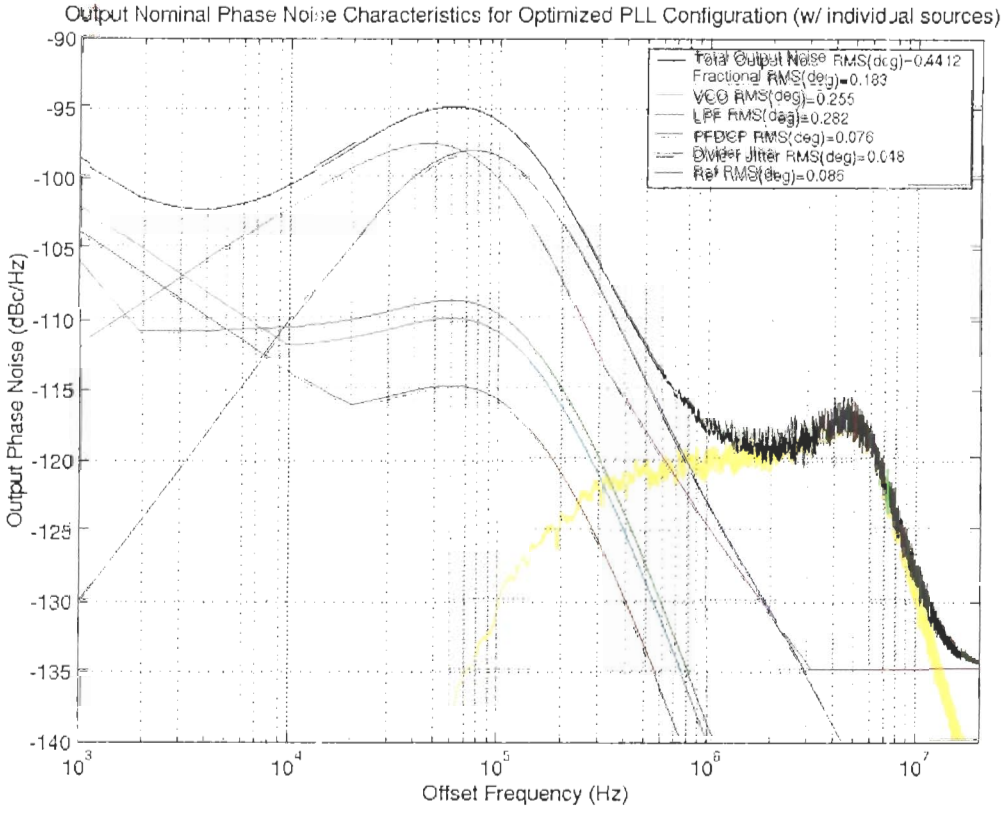
5.5 Summary Nominal PLL Phase Noise Profile

The discussion in Sections 5.3 and 5.4 yielded the following PLL characteristics:

$k_{VCO} = 2\pi * 150MHz/Volt$ *fixed parameter*
$N = 90$ *fixed parameter*
$k_{PDCP} = 160\mu A/2*\pi$ *radians*
$R_1 = 3k\Omega$
$R_2 = 800\Omega$
$C_1 = 1.52nF \quad \Leftrightarrow \quad \omega_Z \approx 2\pi * 35kHz$
$C_2 = 109pF \quad \Leftrightarrow \quad \omega_{P1} \approx 2\pi * 486kHz$
$C_3 = 40pF \quad \Leftrightarrow \quad \omega_{P2} \approx 2\pi * 4.86MHz$
$N = 90$

With the PLL noise contributions provided in Section 4.2, the PLL output phase noise power spectrum can be determined for this PLL.

Figure 5-5 Nominal output phase noise spectrum for optimized PLL, including summary of individual contributors



The power spectrum of phase noise at the PLL output shows the 3 major noise sources, fractional-N noise, loop filter noise, and VCO noise, dominating the PLL output phase noise.

If further reductions in RMS phase noise are required, the most attractive design modification is to reduce loop filter output voltage noise by reducing loop filter resistance and increasing loop filter capacitance to compensate. The next most attractive design improvement would be to reduce VCO phase noise through VCO design modifications; a

lower noise VCO would allow a lower bandwidth PLL to be used, which would also help increase attenuation of fractional-N noise above the PLL bandwidth.

5.5.1 Consideration for Variation in N

As described in Section 4.1.4, the value of N required to achieve all necessary PLL frequencies for this application covers the range N=80 to N=100. If the nominal PLL characteristics described in this section were maintained while the value of N scaled from 80 to 100, the PLL loop gain unity magnitude frequency would scale significantly (because loop gain magnitude is proportional to $1/N$) while the loop gain maximum phase shift frequency would remain unchanged (because the loop gain phase shift is unrelated to N). This scenario would result in significant phase margin reduction for extreme values of N.

To avoid this problem, the CP is designed with finely programmable charge pump output strength. This allows the PLL to be controlled to ensure that k_{PDCP}/N remains constant as N varies so that the PLL loop gain unity magnitude gain frequency remains constant and the PLL's phase margin is maintained over the range of N values.

As N is varied and k_{PDCP} is varied to compensate, PLL noise considerations are affected by the following issues:

1) The transfer function from noise present at the PD inputs to the PLL outputs is proportional to N

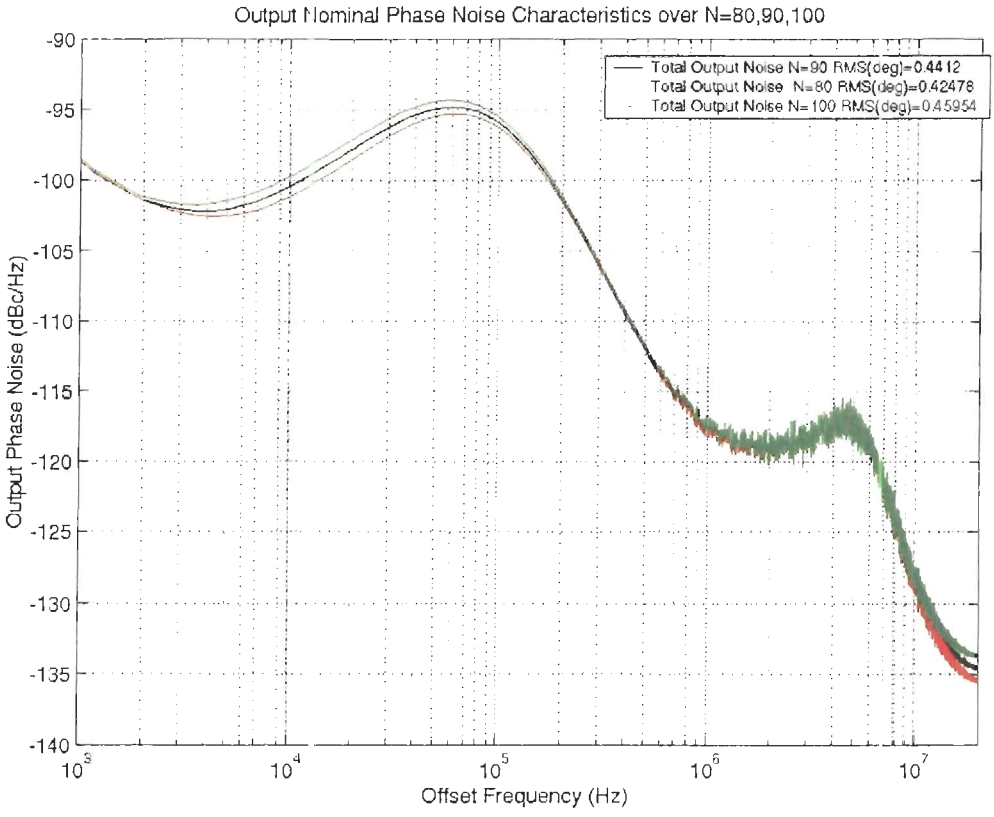
2) The magnitude of Fractional-N noise is proportional to $1/N$, as shown in Section 3

3) The magnitude of PD-CP output current noise is related to the value of k_{PDCP}, which is being adjusted to compensate for N

4) The VCO phase noise is slightly affected by VCO operating speed. The VCO speed scales proportional to N, and VCO noise magnitude is similarly approximated as scaling proportional to N.

Accounting for these affects, the following plot shows the phase noise power spectrum for the PLL configurations for values of N =80,90,100. As the plot shows, the output phase noise RMS value of the PLL is not significantly affected by variations in N.

Figure 5-6 Output phase noise spectrum for optimized PLL configuration with N =80,90,100



5.6 Considerations for IC Variations

Based on the nominal IC characteristics, nominal values are selected for $R_1 / R_2 / C_1 / C_2 / C_3$, k_{PDCP}, and k_{VCO}. However a realistic integrated CMOS PLL will be subject to significant variations in a number of important parameters. Critical IC variations include:

1) Loop filter capacitors are implemented using metal–metal capacitance and MOS devices. Changes in MOS and metal layer characteristics due to CMOS fabrication variations affect the loop filter capacitance values.

Variations in loop filter voltage also affect the capacitance of the MOS devices used to implement capacitors in the loop filter.

2) Loop filter resistors are implemented as poly-silicon resistors. Conversely the charge pump current magnitude is generated using a reference current through a poly-silicon resistor with a fixed voltage reference applied across it; as a result the PD-CP gain scales inversely with poly-silicon resistor variations. Poly-silicon resistors experience significant variations due to CMOS fabrication process variations

3) The VCO gain is affected by MOS device characteristics and metal processing characteristics (which affect the inductance in the VCO LC tank).

To investigate the affect on PLL performance due to these variations, the optimized nominal PLL characteristics described in Section 5.5 were simulated over +/-30% error in capacitance, +/-20% error in resistance, and +/-30% variations in k_{VCO}. The magnitude of these scaling factors is roughly consistent with the variations that are expected to be present across IC fabrication variations and changes in IC characteristics over the range of valid operating conditions.

This analysis is a rough investigation only to evaluate the robustness of the nominal PLL implementation proposed in Section 5.5 to variations in IC characteristics. This rough analysis must also be performed more formally by executing PLL stability and phase noise simulations in a Spice/Spectre based simulation environment using models for devices and device variations provided by the IC fabrication company.

5.6.1 Results Summary of PLL Characteristics over R, C, k_{VCO} Variations

The table below provides the nominal PLL characteristics and the PLL characteristics over R, C, and k_{VCO} variations. This analysis does not take into account the potential correlations between variations in R, C, and k_{VCO}.

Table 5-1 PLL Characteristics over IC variations

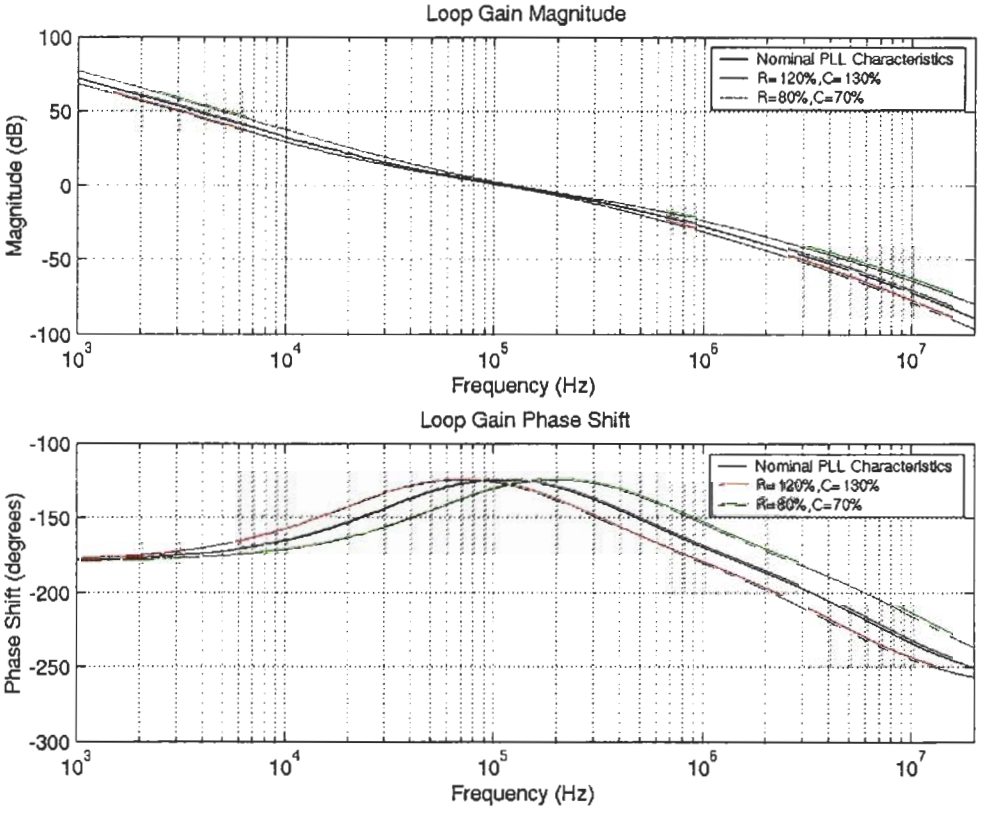
C Factor	R Factor	kvco Factor	Phase Margin (degrees)	RMS Phase Error (degrees)	Maximum Phase Frequency (kHz)	Unity Gain Frequency (kHz)	BW Frequency (kHz)
1	1	1	55.4032	0.4359	110.72	115.52	180.12
1	1	0.7	54.4719	0.4267	110.72	85.12	136.32
1	1	1.3	54.482	0.4806	110.72	144.32	241.92
0.7	1	1	54.4905	0.4782	158.72	121.92	194.72
1.3	1	1	54.501	0.4298	85.12	110.72	185.92
1	0.8	1	55.1223	0.4379	138.72	119.52	192.32
1	1.2	1	54.9089	0.4565	92.32	112.32	186.72
0.7	0.8	1	52.7537	0.5156	197.92	126.72	199.52
1.3	1.2	1	53.1014	0.4671	71.52	107.25	181.92
0.7	0.8	0.7	48.5441	0.4485	197.92	95.52	149.12
0.7	0.8	1.3	54.6936	0.6136	197.92	157.12	251.52
1.3	0.8	0.7	54.6725	0.413	106.72	84.32	135.52
1.3	0.8	1.3	54.2253	0.4467	106.72	143.52	241.12
0.7	1.2	0.7	53.1523	0.4421	132.32	87.52	138.72
0.7	1.2	1.3	55.2423	0.5348	132.32	148.32	245.12
1.3	1.2	0.7	55.2558	0.4613	71.52	79.52	131.52
1.3	1.2	1.3	50.1355	0.5165	71.52	133.12	226.72

5.6.2 Effects Causing PLL Phase Margin Degradation

Table 5-1 shows that the worst-case condition for phase margin is for minimum R, minimum C, and minimum k_{VCO}, the second worst condition is for maximum R, maximum C, and maximum k_{VCO}. If R and C values are both at their minimum levels,

ω_Z, ω_{P1}, and ω_{P2} are increased and the loop gain maximum phase shift frequency is increased as a result. The loop gain unity magnitude frequency remains relatively unchanged due to R and C variations. The following figure shows the affect of R and C variations moving the maximum phase shift frequency without significantly affecting the unity magnitude frequency.

Figure 5-7 Variations in PLL phase margin due to R, C shifts

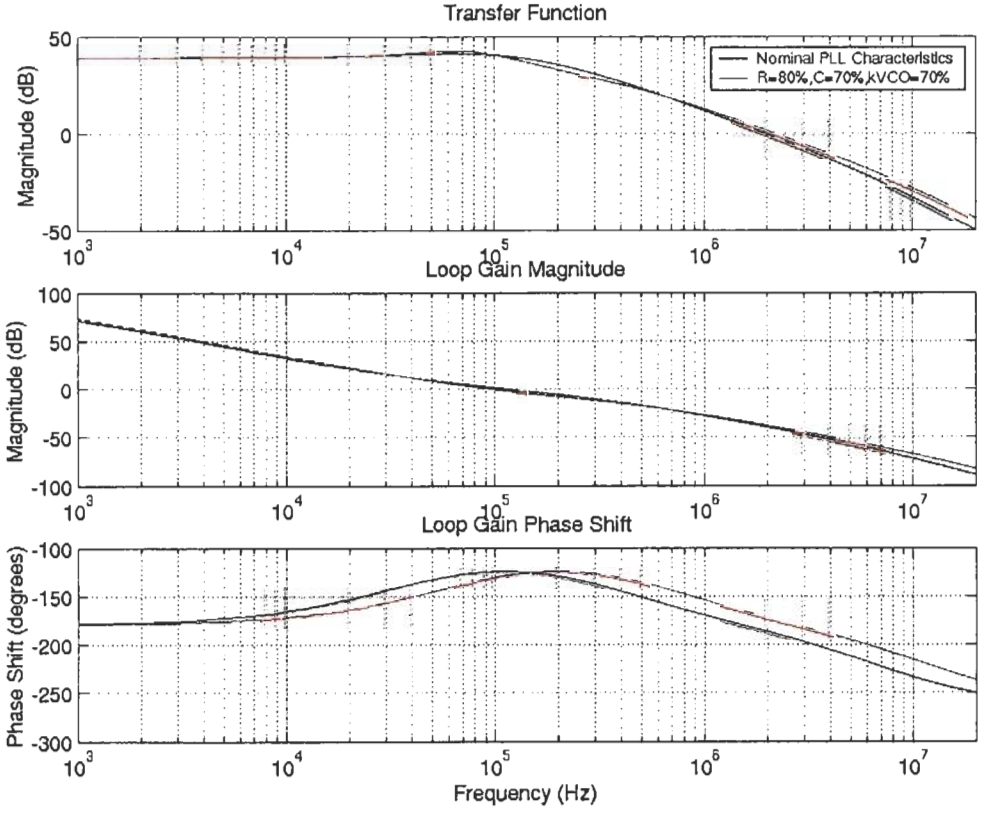


If k_{VCO} varies in the same direction as R and C then the variation in k_{VCO} will shift the unity magnitude frequency still further from maximum phase shift frequency,

increasing the phase margin degradation relative to the case where only R and C were varied.

The following figure shows the nominal case PLL transfer characteristics and the case where R, C, and k_{VCO} are all reduced to their minimum values. The minimum R, C, and k_{VCO} condition yields 48° phase margin, which is slightly better than the minimum acceptable 45° phase margin target.

Figure 5-8 Nominal and worst-case combination of R, C, k_{VCO} variations in terms of PLL phase margin



Conversely the case where R, C, and k_{VCO} are all at their maximum values is the second worst phase margin condition, yielding 50° phase margin.

Over the considered R, C, and k_{VCO} error range, similar phase margin degradation occurs in cases where the unity magnitude frequency is higher than the maximum phase frequency (maximum R, C, and k_{VCO}) and in cases where the unity magnitude frequency is lower than the maximum phase frequency (minimum R, C, and k_{VCO}). This justifies the decision to adjust nominal k_{PDCP} to ensure that the unity magnitude frequency occurs at the maximum phase shift frequency under nominal conditions; this nominal configuration allows for the smallest possible spacing between ω_Z and ω_{P1} while minimizing phase margin degradation in the presence of variations away from nominal R, C, and k_{VCO}.

5.6.3 PLL RMS Phase Error Variations

In the presence of R, C, and k_{VCO} variations that move loop filter characteristic frequencies and PLL bandwidth, some components of PLL RMS phase error are improved while others are made worse. Some R, C, and k_{VCO} variations cause a reduction in PLL bandwidth, resulting in improvements for noise source filtering to some noise sources but also reduction in attenuation of VCO phase noise. Alternatively some R, C, and k_{VCO} variations cause increase in PLL BW, which improves attenuation of VCO phase noise but degrades the attenuation of most other noise sources. Overall, the nominal solution is shown to exhibit near optimal RMS phase error and the increase in RMS phase error is generally small over small variations in IC characteristics.

The largest RMS phase error occurs for the case where R, C are at their minimum values and k_{VCO} is at its maximum value, which also corresponds to the maximum PLL bandwidth condition. The underlying cause of the increase in RMS phase error in this condition is a significant increase in the output phase noise related to fractional-N activity due to the increased PLL bandwidth. The RMS phase error increase in this condition is significantly worse than any other condition considered, so it is likely that improvements in the worst-case phase margin could be realized by shifting the nominal unity gain frequency and maximum phase shift frequency down by a small amount so that the maximum PLL bandwidth in the presence of R, C, and k_{VCO} variations is reduced. This type of adjustment would worsen the phase noise output under nominal conditions in order to improve the phase noise performance in the presence of the worst case R, C, and k_{VCO} variations.

Over the R, C, and k_{VCO} variations considered the output phase noise remains below the target maximum design limit of 0.67 degrees.

6 CONCLUSIONS

Fractional-N PLL implementation for 802.11 a/b/g/n RF frequency generation is a process involving tradeoffs between a number of different noise sources. While fractional-N noise affects are a challenge to model, the PLL output phase noise due to fractional-N activity is not a major contributor to PLL output phase noise in the final PLL implementation.

By optimizing PLL characteristics to ensure minimal sensitivity to loop gain errors due to uncertainty in IC characteristics, PLL performance meets the specification both under nominal conditions and in the presence of variations in capacitance, resistance, and VCO gain. While the lowest RMS phase noise solution for the PLL tended to be for PLL implementations with low phase margin and high sensitivity to IC variations, it is possible to select a slightly less aggressive PLL implementation while still meeting the RMS phase noise target. Through careful selection of PLL design parameters, the targeted maximum allowable RF clock signal RMS phase noise output level of 1° is satisfied while the PLL exceeds 45° phase margin across a range of R, C, and k_{VCO} variations.

APPENDICES

Phase Argument

Consider the reference sinusoidal signal $R_{\sin}(t)$:

$$R_{\sin}(t) = \sin(\Theta(t))$$

The quantity $\Theta(t)$ is referred to as the "phase argument" of $R_{\sin}(t)$. The phase argument terminology is meaningful if $R_{\sin}(t)$ is written using a term $e^{i\Theta(t)}$.

$$R_{\sin}(t) = \mathrm{Im}ag[e^{i\Theta(t)}]$$

A binary clock signal can also be written using polar notation so that the concept of a binary clock signal's phase argument is meaningful. For example consider the square wave signal $R_{square}(t)$

$$R_{square}(t) = S\left(\arg(e^{i\Theta(t)})\right)$$

$$S(x) = \begin{cases} 1, when\ 2n\pi \le x \le 2[n+\Delta]\pi \\ 0, when\ 2[n+\Delta]\pi \le x \le 2[n+1]\pi \end{cases}, \quad n = 0,1,2,3,\ldots,\infty, \Delta < 1$$

Generally binary clocks are used to drive digital phase detector circuits to clock rising edge sensitive circuits so the phase of the clock is only detected when the clock transitions from 0 to 1.

Effect of Count-to-N Digital Counter on Clock Phase

Practical PLL implementations often involve driving a binary clock signal into a Count-to-N digital counter and measuring the phase of the output clock from the Count-to-N counter.

Such a system can be seen as producing an output square wave with a phase argument increasing by 2π for every $N*2\pi$ increase in the phase argument of the input binary clock. Thus the Count-to-N system is producing an output phase argument that is $1/N$ x the input phase argument.

Concept of Phase Noise

An ideal oscillation signal with a frequency f_{OSC} would have a phase argument that is an ideal ramp in time given by

$$\Theta_{IDEAL}(t) = 2\pi f_{OSC} t$$

Practical oscillation signals deviate from the ideal oscillation behaviour. Often amplitude error is neglected, and the oscillation signal is modelled as having a phase argument given by

$$\Theta(t) = 2\pi f_{OSC} t + \Theta_{NOISE}(t)$$

$\Theta_{NOISE}(t)$ is a zero mean small error term, $\Theta_{NOISE}(t) << 2\pi$.

PLL phase noise can be characterized using units of dBc, which is a measure of the noise signal power to the carrier power.

Assuming that the magnitude of the oscillator is A, the error vector is simply $A*\Theta_{NOISE}(t)$ (assuming the phase noise is in Radians) and the power of the noise term is $[A*\Theta_{NOISE}(t)]^2$. The ratio of the noise power to the signal power is $[\Theta_{NOISE}(t)]^2$, and taking the relationship $10*\log_{10}[\Theta_{NOISE}(t)]^2$ provides phase noise in dBc.

Phase Noise Following 1.5x Frequency Conversion

A frequency conversion circuit follows the PLL discussed in this report; the PLL generates 2/3 or 4/3 the required RF frequency and the frequency conversion circuit generates the RF frequency. The case where 2/3 the RF frequency is translated to the RF frequency is discussed here for illustration.

Following the PLL a mixer is used to multiply a half PLL frequency (1/3RF) and the PLL frequency (2/3RF) to generate a frequency at RF and an unwanted tone at 1/3RF.

In order to consider the phase noise impact of this translation, the mixing operating can be considered to be ideal analog multiplication and the two input frequencies can be considered to be ideal sinusoids.

$$x_1(t) = \sin(\tfrac{2}{3}\omega_{RF}t + \Theta_{PLL\_NOISE}(t)) = \sin(\Theta_1(t))$$

The 1/3RF tone is generated using a divide-by-2 circuit; this divides the phase argument of the PLL output by 2 and consequently halves the phase noise.

$$x_2(t) = \sin(\tfrac{1}{3}\omega_{RF}t + \tfrac{1}{2}\Theta_{PLL\_NOISE}(t)) = \sin(\Theta_2(t))$$

The multiplication of these 2 tones yields the following output signal.

$$y(t) = x_1(t) * x_2(t) = \tfrac{1}{2}((\cos(\Theta_1(t) - \Theta_2(t)) - (\cos(\Theta_1(t) + \Theta_2(t))))$$
$$= 1/2(\cos(\tfrac{1}{3}\omega_{RF}t + \tfrac{1}{2}\Theta_{PLL\_NOISE}(t)) - \cos(\omega_{RF}t + \tfrac{3}{2}\Theta_{PLL\_NOISE}(t)))$$

If the 1/3 RF tone is removed through high pass filter the mixer output, the RF tone is produced and has a phase noise magnitude scaled by 1.5x from the original PLL output phase noise.

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