

Mid-IR Waveguides and Grating Couplers for 2.7-2.9 μm

by

Timothy Richards

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Approval

Name: Timothy Richards

Degree: Master of Science (Physics)

Title: Mid-IR Waveguides and Grating Couplers for 2.7-2.9 μm

Examining Committee: **Chair:** Malcolm Kennett
Associate Professor

Stephanie Simmons
Senior Supervisor
Assistant Professor

Michael Thewalt
Supervisor
Professor

Jeffrey McGuirk
Examiner
Associate Professor

December 4, 2018

Date Defended:

Abstract

Integrated silicon photonics strip waveguides and grating couplers are developed for mid-infrared (mid-IR) wavelengths at 2.7 μm and 2.9 μm . Waveguide loss is measured as a function of width for 2.7 μm light in the vicinity of a prominent OH absorption band, and a loss of less than 2 dB/cm is recorded for the 1.0 μm width waveguide. A fabrication bias metric is determined for accurately developing grating couplers at 2.9 μm on a 500 nm silicon-on-insulator (SOI), 3 μm buried-oxide substrate. A high resolution measurement scheme is motivated and measurements indicate that these devices will be capable of studying the Se^+ donor spin qubit cavity coupling platform proposed by researchers at Simon Fraser University.

Keywords: mid-IR silicon photonics; waveguides; grating couplers; quantum information

Dedication

To my parents,

This all started long ago. Thank-you for working so hard to give me the opportunities that got me here. I love you both.

Grr.

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I am immeasurably indebted to my Senior Supervisor, Dr. Stephanie Simmons, for her thoughtful guidance, expert knowledge, constant encouragement, and incredible patience.

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Chapter 1

Introduction

1.1 Overview

This work is concerned with guiding mid-infrared (mid-IR) light with nanoscale structures made of silicon. It is motivated primarily by a competitive quantum computing platform in silicon in development at Simon Fraser University (SFU). The results discussed in this thesis add to the body of mid-IR photonics research and contribute to the combined efforts of SFU researchers in the Silicon Quantum Technology group. In this introduction section, we first motivate the pursuit of quantum computing technology and introduce the unique quantum platform being developed at SFU. We show why mid-IR silicon photonics is the perfect complement for this system. Finally, we will explore the current state of mid-IR photonics literature and place this project firmly within its appropriate niche in the broader field.

1.2 Quantum information

The main goal of this work is to contribute to the efforts of other researchers at Simon Fraser University to create and study a particular physical system that can be used as a platform for quantum computing. A quantum computer is a device that takes advantage of the laws of quantum physics to perform calculations in a manner that is not possible with conventional, or classical, electronics [1, 2].

The fundamental building block of such a device is the quantum bit, or ‘qubit’ [2]. In a classical computer, calculations are performed by applying logical operations to classical bits. A classical bit has one instantaneous value: either a 0 or 1. A qubit is a two-level quantum system that is able to take one of two values, also labeled 0 and 1. However, unlike a classical bit, a qubit can also be a superposition of both 0 and 1 simultaneously [3]. In addition, when multiple qubits interact they can become entangled [4]. In the entangled state, the qubits act as a single entity, and cannot be described independently. These phenomena, superposition and entanglement, allow quantum computers to function using logic that is substantially different than that of a classical computer [2].

By harnessing these unique properties of qubits, quantum computers will be able to solve a variety of problems that are intractable using only modern, classical computers [5, 6, 7]. Direct applications include the use of quantum algorithms in chemistry to simulate and calculate the properties of molecules [8, 9], where the dimension of the calculation grows exponentially with the size of the system and makes the task infeasible for classical computation [5]. Problems in chemistry have already been solved using a small-scale (2-6 qubits) quantum computing device [10], demonstrating the vast potential for quantum devices on a larger scale. Chemical simulations such as these enable the efficient design of new medicine and materials [7].

The potential for these applications, and many more [11, 12, 13, 14], are driving quantum computing research globally, including many academics, corporations such as Google and IBM, and governmental agencies such as the U.S. Department of Energy [15]. There is a great variety of systems under development: superconducting qubits [16], spin qubits [17], photons [18, 19], trapped ions [20, 21, 22], quantum dots [23], nitrogen-vacancy centers in diamond [24], and more. The race to build a large-scale, universal quantum computing device is well underway. A competitive system must have qubits with favorable properties [25], be able to control and measure individual qubits, and facilitate qubit-qubit interactions to entangle and perform quantum logical operations. In addition, all of these criteria must be met in a system that is also scalable, meaning that it is able to be built up into ever-larger device networks to increase computational power.

1.3 Donor qubits in silicon

A promising qubit candidate has recently been proposed by researchers at Simon Fraser University [26]. The authors propose implanting single atoms of selenium (Se) into silicon. In silicon, Se is a substitutional double donor defect: it replaces a single Si atom in the silicon lattice and has two unpaired electrons. The Se defect can singly ionize to form Se^+ . The Se^+ system has one remaining unpaired electron which exhibits a helium-like two-level ground state energy structure based on the electron's spin state. The result is a donor spin qubit. The system has been shown to have a long lifetime (the system is very stable) as well as other favorable qualities that make it a good qubit [26]. The advantage of the Se^+ qubit that motivates this thesis work is that the qubit can be manipulated and measured optically using mid-infrared (mid-IR) light at a wavelength of $2.9\ \mu\text{m}$.

Part of the proposal [26] is to implant the Se^+ donor qubit into the center of an optical cavity, or resonator. This takes advantage of cavity quantum electrodynamics (c-QED) to greatly increase the light-matter interaction and allow for the manipulation and readout of the qubit using $2.9\ \mu\text{m}$ mid-infrared (mid-IR) light. This requires the development of an optical cavity in silicon resonant at $2.9\ \mu\text{m}$, along with a method of delivering and retrieving

mid-IR signals to and from the qubit. Such a system must also be scalable. Integrated silicon photonics is a natural solution to these requirements.

1.4 Silicon photonics

The field of integrated silicon photonics is concerned with the design and fabrication of devices on the micrometer scale that confine and guide light within the plane of a thin layer of silicon. Integrated photonics using the silicon-on-insulator (SOI) platform to create devices is already a well-established field in industry, particularly telecommunications [27]. The high refractive index contrast between silicon and either air or silica facilitates the confinement of light modes to create devices such as waveguides and resonators. Most significantly, the SOI platform uses tried-and-true complementary metal oxide semiconductor (CMOS) fabrication processes that allow for cost-effective batch-production of low footprint devices on photonic chips [28].

However, current telecommunications photonics technology has predominantly been designed for light with wavelength $1.3\ \mu\text{m}$ or $1.55\ \mu\text{m}$ [29]. The Se^+ donor qubits require an SOI photonics platform designed for $2.9\ \mu\text{m}$ wavelength, in the mid-IR ($\approx 2\text{-}20\ \mu\text{m}$ [30]). Relative to the telecommunications wavelengths, interest in mid-IR photonics research is a younger field [29]. Part of the delay in mid-IR interest was due to waiting for high-power, room-temperature sources and sensitive detectors in the mid-IR to be developed [30]. Mid-IR integrated photonics is now generating significant interest to create “lab-on-chip” sensors for chemical and biological measurements [29]. Integrated photonic devices may be able to replace bulky, laboratory-bound mid-IR spectroscopy devices, allowing sensing in-field [31].

To use integrated photonics for the Se^+ donor qubit platform, it is necessary to first develop the basic photonic building blocks for complex networks involving qubits. The basic components are: the waveguide, used for routing the light in-plane across the chip, and the grating coupler [32], used for coupling out-of-plane light into the plane of the chip, and then out again for measurement. The qubit-cavity coupling scheme for use with the Se^+ donor qubits requires the creation of cavities with a high quality factor (high-Q) at $2.9\ \mu\text{m}$. One specific challenge facing the development of $2.9\ \mu\text{m}$ integrated SOI photonics is the optical absorption of mid-IR light in silicon dioxide (SiO_2) in this wavelength region [33, 34]. If we are able to make strip waveguides on a particular substrate that demonstrate low loss, then this indicates that high-Q cavities may be possible. Conversely, high loss in waveguides suggests that high-Q cavities may not be feasible. As an initial step towards high-Q cavities, the loss characteristics of simple strip waveguides are studied in this work.

By developing waveguides and grating couplers designed for a wavelength of $2.9\ \mu\text{m}$, this work aims to achieve two goals: (1) begin to develop the basic components necessary for coupling Se^+ donor qubits to integrated photonic cavities in an SOI environment, and (2) add to the body of knowledge and interest in mid-IR photonics waveguides (and in-

put/output methods in the form of grating couplers) for their own sake, by measuring loss at a specific wavelength. The results are a calculation of the loss (in dB/cm) of strip waveguides in this wavelength region, and the performance of grating coupler designs over a range of wavelengths.

To achieve these goals, in this work we have used numerical simulation methods to design strip waveguides and grating couplers for 2.9 μm wavelength. Simulations are used to predict the losses in waveguides from multiple loss mechanisms, and these loss mechanisms are shown to be dependent on the width of the waveguide. Numerical simulation was used to optimize the grating coupler design. A photonic chip layout was designed and fabricated with hundreds of devices with varying waveguide length and width, and loss versus waveguide width was measured. Because of fabrication error in the widths of the grating couplers, the peak transmission actually occurs near 2.7 μm , and so we have measured loss at this wavelength. However, a number of grating couplers were fabricated with varying levels of width bias to account for error, and we have achieved at least one design that operates at 2.9 μm . A new measurement apparatus was also motivated and developed that will be useful for future work.

Chapter 2

Fundamental properties of waveguides and grating couplers

2.1 Photonic strip waveguides

The basic substrate of silicon photonics is shown in Figure 2.1 and is comprised of a thin (100–500 nm) layer of silicon on top of a few microns of oxide, commonly SiO_2 , called the buried oxide or BOX layer. These two layers rest on top of a thicker silicon substrate which makes up the rest of the wafer. Photonic devices are made by etching into the silicon device layer and leaving a pattern of silicon that can confine and guide light within the plane of the device layer. A common technique to perform this fabrication process is through electron-beam lithography (EBL), in which a resist is first applied on top of the device layer, exposed to electron beam radiation and developed [35]. The remaining mask material protects the silicon that is to remain unetched [35]. Often, a chemical etch is used to strip away unprotected silicon and leave the user-defined pattern [35].

After etching, a layer of oxide, such as SiO_2 , may be deposited on top of the wafer by chemical vapour deposition, with a thickness typically on the order of 1–3 μm [36]. This top layer is called the cladding and serves to protect the devices on the chip from physical damage. However, the devices in this work will be air-clad (no cladding). It will be discussed in Section 2.2 that a significant source of loss in our system may be due to OH group impurities in the SiO_2 . Because the oxide of the BOX layer and the oxide grown as a cladding may have different parameters, such as amount of impurities, we decided to keep the devices unclad so that there is only one type of SiO_2 present.

One of the most important and simple structures that can be created in silicon is the photonic waveguide [37]. Waveguides confine light to propagate along their length and are used to route light across a photonic chip. A 2D cross section of a basic rectangular waveguide, called a strip waveguide, is shown without cladding in Figure 2.2. The waveguide height is determined by the device layer of the wafer substrate, but the width is a free



Figure 2.1: Silicon-on-insulator (SOI) substrate with silicon (Si) device layer ($\approx 100\text{--}500$ nm), silica (SiO_2) buried-oxide (BOX) layer ($\approx 1\text{--}3\ \mu\text{m}$), and silicon substrate ($> 500\ \mu\text{m}$).

variable for design. At certain wavelengths, light will be confined to move orthogonally to the page in Figure 2.2, being confined in directions parallel to the plane of the page.

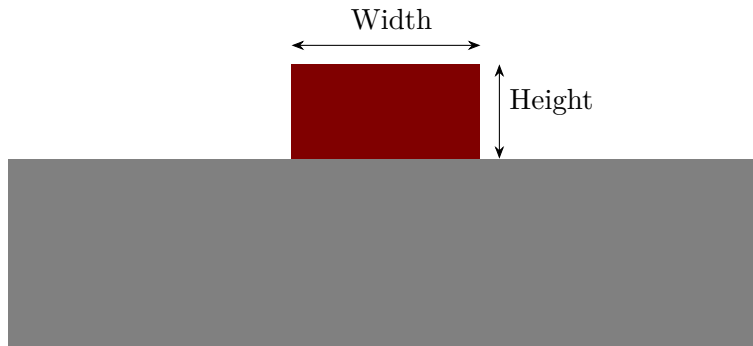


Figure 2.2: Strip waveguide geometry, 2D cross section. Light propagation is normal to the plane of the page. Note that there is no cladding in this diagram (air clad). Height is determined by the device layer thickness. In this work the height is 500 nm and widths vary between $0.6\text{--}1.2\ \mu\text{m}$.

A mixed-dielectric geometry such as that shown in Figure 2.2 generates an eigenvalue problem which can be solved according to Maxwell’s equations [37]. Solutions that are confined and guided along the waveguide, called guided modes, have fields that are standing waves inside the silicon core of the waveguide in the 2-dimensional cross-section of the waveguide normal to the direction of propagation, and decay exponentially in the air and BOX layer [37]. The mode with the greatest proportion of light within the silicon is called the fundamental mode of the waveguide.

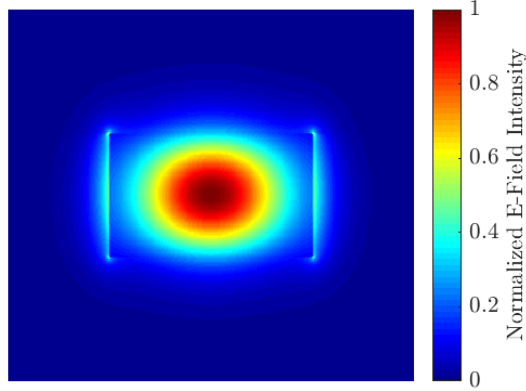


Figure 2.3: Electric field intensity of the fundamental waveguide mode confined by a strip waveguide with a rectangular cross section. Light propagation is normal to the page. Calculated using Lumerical MODE Solutions FDE solver.

Figure 2.3 shows the electric field intensity of the fundamental transverse electric (TE) mode for a rectangular strip waveguide. The light is TE polarized, meaning that the light polarization is parallel to the wafer plane (the horizontal in Figure 2.2). The majority of the field energy is concentrated in the center of the waveguide, but as can be seen in Figure 2.3, fields also extend above and below, and at the sidewalls, of the waveguide. This is very important, as the shape of the mode will dictate the degree to which the fields interact with the waveguide walls or the substrate beneath the waveguide.

2.1.1 Effective index

Confined light modes in a strip waveguide propagate with an effective index that differs from the natural refractive index of the silicon core, the BOX layer, or the cladding (in some cases, air). The solutions to the eigenvalue problem have the form

$$E(x, y, z, t) = E(x, y)e^{-\omega t + \beta z}, \quad (2.1)$$

where (x, y, z) are the spatial coordinates with z in the direction of propagation, ω is the angular frequency, t is time, and β is the propagation constant [38]. The square of the propagation constant, β^2 , is the eigenvalue of the eigenvalue problem and is solved for numerically [39]. The effective index is then

$$n_{\text{eff}} = c \frac{\beta}{\omega}, \quad (2.2)$$

where c is the speed of light [38]. In the mid-IR region of interest to this work, the refractive index of silicon is approximately 3.47 and that of silica (SiO_2) is 1.44 [40]. As the effective index increases, the proportion of light guided in the silicon also increases. When the effective

index approaches the index of the cladding and/or BOX layer, the mode becomes unconfined and unguided by the waveguide. Figure 2.4 shows the simulated effective index for the fundamental mode of 2.9 μm wavelength light in strip waveguides of varying width on a 500 nm SOI, 3 μm BOX substrate. Below $\approx 1 \mu\text{m}$ width, the waveguide is single-mode, meaning that no other solutions are confined. The fit to the simulated effective index data is used for simulating waveguide losses in Section 2.2.

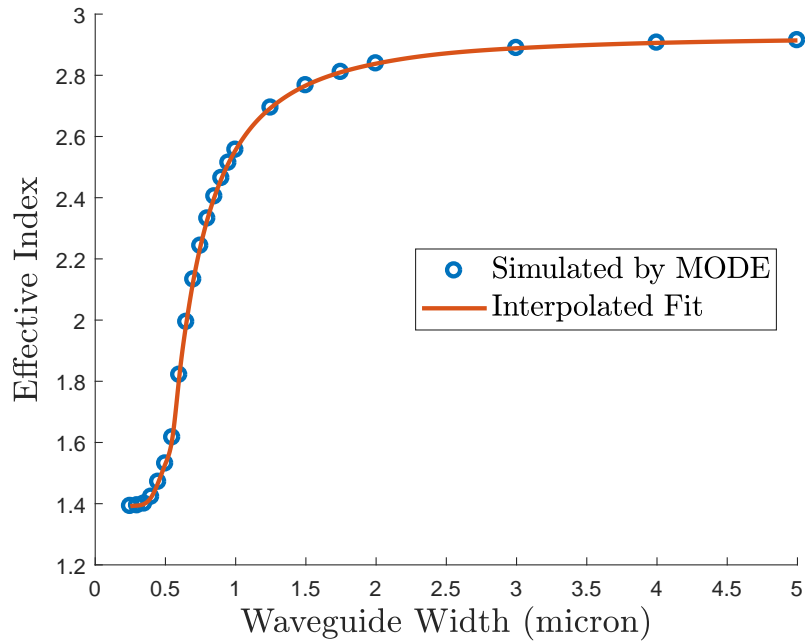


Figure 2.4: Simulated effective index at 2.9 μm wavelength as a function of waveguide width for strip waveguides on 500 nm Si device layer, 3 μm BOX layer. Calculated using Lumerical MODE finite difference eigenmode (FDE) solver. The refractive index of silicon at 2.9 μm is approximately 3.47 and for SiO_2 it is 1.44.

2.1.2 Mode profiles

As mentioned previously, it is important to note that the shape of the fields for the fundamental confined mode in a strip waveguide changes as the width of the waveguide changes. Figure 2.5 shows the fundamental mode of three separate waveguides, all with the same height, but varying width. Note that as the waveguide gets more narrow, the fields at the sidewalls become stronger. This will make the fields interact more significantly with any roughness in the sidewalls, and affect the propagation loss due to scattering from those imperfections [41, 42]. This is discussed in Section 2.2. In addition, as the fields extend further into the substrate, these evanescent fields will excite radiating modes within the substrate, leading to substrate leakage [43].

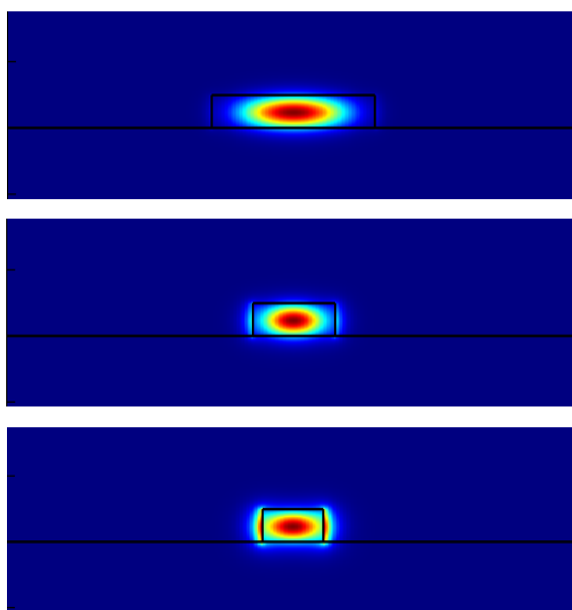


Figure 2.5: Normalized E-Field intensity for the fundamental waveguide modes of waveguides with equal height and varying width.

2.2 Waveguide loss

Three primary mechanisms of loss in photonic strip waveguides are substrate leakage [43], sidewall scattering [44, 45], and material absorption. Substrate leakage depends on waveguide geometry, dimensions, and materials [45], as well as on the thickness of the BOX layer. Sidewall scattering arises due to roughness of the waveguide sidewalls caused during the fabrication process [41, 42, 46]. Absorption depends on the materials or impurities in the materials that make up the waveguide structure. Silicon is transparent in much of the mid-IR, and the material used in the buried oxide of our devices will be SiO_2 , which only becomes absorptive for wavelengths greater than $3.5 \mu\text{m}$ [29]. However, OH group impurities

are common in SiO_2 , which have an optical absorption band near $2.72\ \mu\text{m}$ [33]. Formation of OH bond impurities are affected by the fabrication conditions, such as temperature and the presence of water, and may be on the surface or in the bulk of the oxide [33]. Substrate loss and absorptive losses due to OH impurities are both related, because each depends on the amount of overlap between the guided light mode of the waveguide and the BOX layer itself.

To study the loss of waveguides built on a given substrate (with a particular Si device layer thickness and SiO_2 BOX layer thickness) we use the fact that both the losses due to scattering and substrate leakage (and so also OH absorption) depend differently on the width of the waveguide, as defined in Section 2.1. We design, simulate, fabricate, and measure the loss in waveguides of varying width. We compare the loss vs width behaviour of our waveguides to the model and simulation, which allows us to distinguish between substrate and sidewall loss contributions. Following this work, future wavelength dependent studies can then distinguish between broadband evanescent and OH-specific loss mechanisms. These techniques could be used as a standard way to assess the suitability of a given substrate for use with the Se^+ cavity-qubit platform.

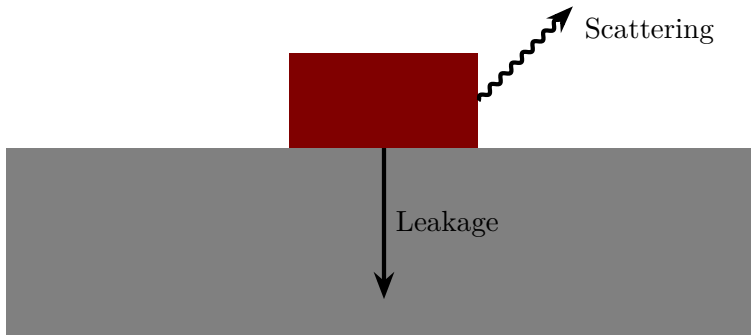


Figure 2.6: Two mechanisms of strip waveguide loss: substrate leakage and radiative sidewall scattering.

2.2.1 Substrate leakage

Substrate leakage is energy loss from the propagating modes of the waveguide due to coupling to other modes within the BOX layer and silicon substrate [37, 43, 47]. As seen in Section 2.1.2, the fundamental mode of a strip waveguide is not fully contained within the silicon (or high-index) portion of the waveguide. The propagating fields also extend into the surrounding cladding and down into the buried oxide layer. These fields excite modes within the substrate and lead to undesired power transfer to these modes [47].

The parameters that affect the amount of substrate leakage are then: (1) the index contrast between the waveguide core and the BOX layer, (2) the geometry of the waveguide, (3) the thickness of the BOX layer itself [45], and (4) the chemical composition of the BOX

layer (e.g. OH impurities in SiO_2). Parameters (1) and (2) are captured by the waveguide’s effective index (Section 2.1.1) and determine how well the fundamental mode of the waveguide is confined to the high-index core. Parameter (3) determines how well isolated the waveguide is from the silicon substrate. Parameter (4) affects the amount of absorptive losses due to evanescent fields present in the BOX layer. Parameters (1), (3) and (4) are determined by the wafer’s materials and dimensions, and the waveguide height is also fixed by the device layer thickness, so for a single wafer study we are confined to consider the effect of varying waveguide width on the amount of leakage loss.

Simulation

There are multiple possible methods for simulating substrate leakage. The most direct approach would be to create a fully 3D finite-difference time-domain (FDTD) simulation [48, 49] to propagate light along a strip waveguide and monitor the field strength along the length of the waveguide. However, this approach requires the simulation geometry to be large enough to observe the loss (> 1 mm of waveguide length). Losses on the order of 1–10 dB/cm require a simulation geometry which is prohibitively large due to either the memory requirements or the duration, or both, of the simulation. The use of periodic Bloch boundary conditions in 3D or a 2D solver such as the eigenmode expansion (EME) method requires significantly lower computational resources than 3D FDTD simulations.

In this work we have used Lumerical’s bidirectional eigenmode expansion (EME) solver to propagate light along strip waveguides of different widths and track the energy loss of the fields. The solver separates a small length of waveguide into sections over which the fields are decomposed into a basis set of modes, and then calculates scattering matrices between adjacent sections. In the case of the strip waveguide, the sections are identical. The scattering matrices capture the decay of fields to modes in the substrate. In this manner, the simulation can be extended to a great distance (50 mm) and the loss per unit length can be calculated.

The simulation results are shown in Figure 2.7. For waveguides with widths greater than 700 nm, projected substrate loss is negligible. Below a width of 700 nm width, the substrate loss increases exponentially as width decreases. Compare to the effective index in Figure 2.4 to see that this increase in leakage corresponds to the effective index approaching a minimum index of 1.4. To fit to the simulated data, an exponential fit plus a constant loss parameter is applied and produces a good fit to the data, suggesting that we can use an exponential to represent substrate leakage loss when analyzing real data.

The results in Figure 2.7 suggest that even at low effective index (Figure 2.4) the substrate leakage loss is quite low (on the order of 10^{-3} dB/cm). We believe that the actual loss will be much higher. Only a finite number of modes, in the waveguide or substrate, can be included in the simulation, and so not all the coupling between guided and unguided modes may be included, leading to lower projected loss. It is possible that a 3D simulation

that takes advantage of periodic boundary conditions may provide more reliable results, and this will be the subject of future study.

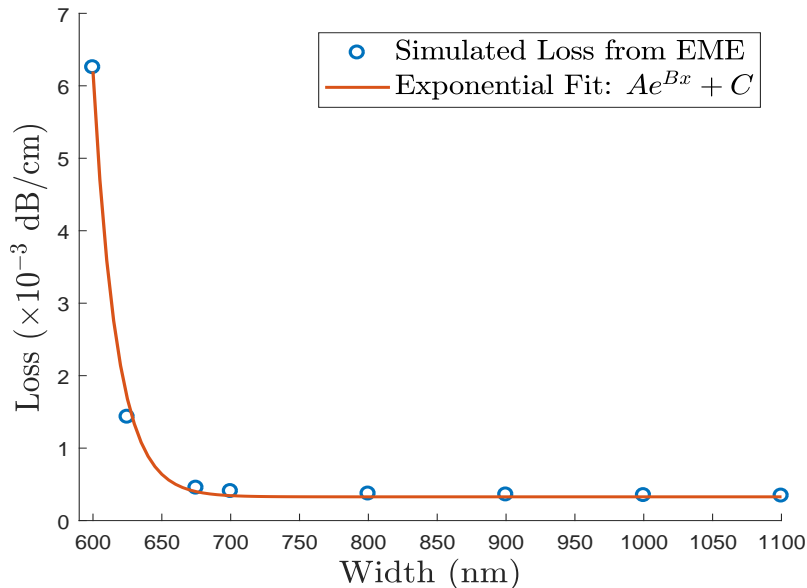


Figure 2.7: Results of substrate leakage loss EME simulation for 2900 nm wavelength on 500 nm SOI with 3 μm BOX layer thickness and no cladding. Note the scaling factor of 10^{-3} on the y-scale.

Note that the simulated loss does not tend to zero as the waveguide width continues to increase. One reason for this is non-zero material absorption in the material model. The material model gives the index of refraction as a function of wavelength, and in the Lumerical simulation software this model is obtained from a fit to complex-valued material data obtained from Palik [40], producing an ‘intrinsic’ waveguide loss that is not due to substrate leakage, but instead absorption by the materials. To check, we repeated the simulation for a waveguide width of 1000 nm using perfectly lossless material data (see Section 2.2.1). The result was a 12% reduction in the simulated loss at this waveguide width. Some non-zero substrate leakage loss is still to be expected, since an “infinitely” wide waveguide, called a slab waveguide, still does not have perfect confinement in the vertical (out-of-plane) direction. Therefore as the width increases, the waveguide loss will tend towards the loss of a slab waveguide with the same device layer thickness.

Complex refractive index

A material's optical characteristics are described by its refractive index, which is a complex-valued function of wavelength (λ) and can be written

$$\tilde{n}(\lambda) = n(\lambda) + ik(\lambda), \quad (2.3)$$

where the real part $n(\lambda)$ is commonly referred to as the index of refraction and the imaginary part $k(\lambda)$ is an attenuation coefficient that determines the amount of material absorption at a given wavelength. Since n and k are the real and imaginary parts of a complex function, they are highly connected by the Kramers-Kronig relations [50]. This means that both refractive index and loss are integral parts of describing a material's optical response and are not readily separated. It is possible to perform the simulation by taking a data set of (n, k) values and arbitrarily discarding k to get a lossless material, however, this is not recommended by Lumerical as it can make obtaining a fit of the material data difficult (n and k are necessarily fit at the same time) and create results that are difficult to interpret [38]. This means that although it is tempting to use lossless materials to simulate coupling to substrate modes for substrate leakage losses, it is better to keep the material absorption to have an accurate refractive index model.

2.2.2 Sidewall scattering

Another significant loss mechanism in photonic waveguides is radiative scattering from imperfections in the sidewalls, or sidewall roughness. These imperfections are due to fabrication processes.

Model

A commonly used model to predict and describe the loss due to sidewall scattering is known as the Payne and Lacey model [44]. The radiation loss coefficient due to scattering from sidewall roughness, α (dB/cm), is given by

$$\alpha = \frac{\sigma^2}{\sqrt{2}k_0d^4n_1}g(V)f_e(x, \gamma), \quad (2.4)$$

where σ^2 is the mean square deviation from a flat surface, $k_0 = 2\pi/\lambda$ is the wavenumber in vacuum, d is half of the waveguide width, and n_1 is the index of refraction of the waveguide core (silicon) [44]. The function $g(V)$ is defined in Equation 2.5 and depends on the wavelength, waveguide dimensions, and materials. $f_e(x, \gamma)$ is defined in Equation 2.7 and relates to an integral over a spectral density function [44].

$$g(V) = \frac{U^2V^2}{1+W}, \text{ where} \quad (2.5)$$

$$U = d\sqrt{n_1^2 k_0^2 - \beta^2}, \quad V = k_0 d \sqrt{n_1^2 - n_2^2}, \quad W = k_0 d \sqrt{\beta^2 - n_2^2 k_0^2}, \quad (2.6)$$

n_2 is refractive index of the cladding material, and $\beta = k_0 n_{\text{eff}}$, where n_{eff} is the effective index of the propagating mode [47]. Finally, we have

$$f_e(x, \gamma) = \frac{x \left[\left((1+x^2)^2 + 2x^2\gamma^2 \right)^{1/2} + 1 - x^2 \right]^{1/2}}{\left[(1+x^2)^2 + 2x^2\gamma^2 \right]^{1/2}}, \quad (2.7)$$

where

$$x = W \frac{L_c}{d}, \quad \gamma = \frac{n_2 V}{n_1 W \sqrt{\Delta}}, \quad \Delta = \frac{n_1^2 - n_2^2}{2n_1^2}, \quad (2.8)$$

and L_c is the correlation length of the sidewall roughness.

Simulation

To simulate the loss due to sidewall roughness, most of the relevant parameters are fixed by the waveguide dimensions and the wavelength, leaving only σ and L_c to be chosen. However, one of the parameters set by the geometry is deceptively complex – the effective index, n_{eff} , is in fact a function of the waveguide width ($2d$), and one without a known form. To simulate the scattering loss as a function of waveguide width, first the effective index for each width must be determined separately. Using the FDE solver in Lumerical’s MODE, we simulated the effective index for a set of waveguide widths of interest, and then applied an interpolated fit. This fit is then used to determine the value of n_{eff} for each waveguide width in the definition of W in Equation 2.6.

Results are shown in Figure 2.8 for $L_c = 50$ nm and $\sigma = 2$ nm, where these values are “typical” values based on atomic force microscopy (AFM) measurements of similar strip waveguides [46] and are used in several articles investigating scattering loss modeling [47, 51]. We can see that as the waveguide width decreases from a value of 1.2 micron, the scattering losses increases, attributable to an increase in the interaction with the sidewalls [47]. A maximum is reached at approximately 0.62 micron width. For waveguides narrower than this, scattering losses are predicted to decrease by the model. This has been attributed to the decrease in effective index, which describes a decrease in mode confinement (increase in mode diameter) and reduction in the intensity of the electric fields interacting with the sidewall roughness [42, 47, 51]. In the simulations performed by Gillot et al. [47] for square strip waveguides at 1550 nm wavelength, an increase in mode diameter is seen to coincide with a decrease in scattering losses for waveguide widths narrower than the width of maximum loss. This supports the idea that, as the waveguide mode becomes less confined (mode diameter increases), there is less interaction with sidewall roughness and so less loss due to radiative sidewall scattering.

To use this model to fit measured data, it is not possible to include the effective index as a fitting parameter because it is not a constant for varying waveguide width. The effective index is calculated for each width by numerical simulation, and it is an unknown function of the width. It is possible to measure the effective index by measuring the group velocity of the light for each waveguide width, but this is outside the scope of this work. Therefore, in order to apply the model to the data, an interpolated fit of the simulated effective index values is used for $n_{\text{eff}}(d)$ when fitting with the model. This leaves L_c and σ as the only constant fitting parameters.

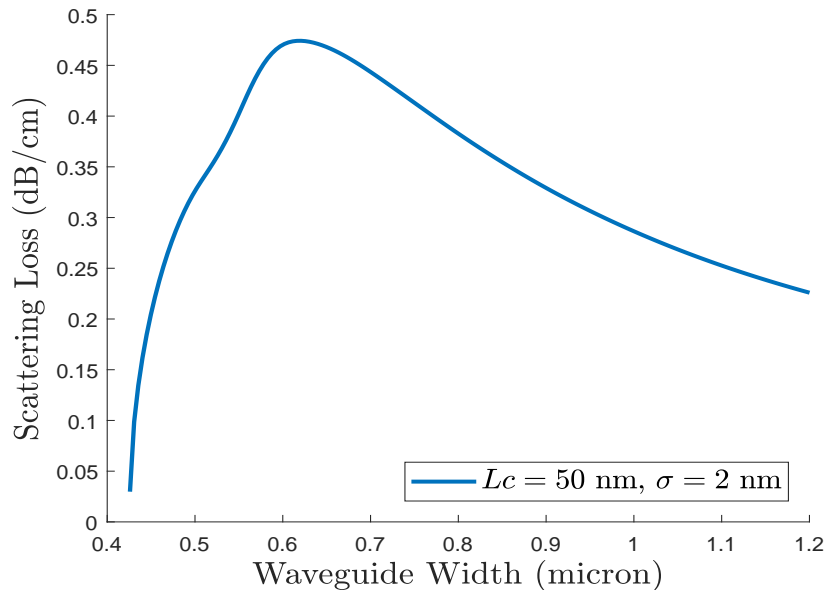


Figure 2.8: Results of scattering loss simulation for 2900 nm wavelength on 500 nm SOI, no cladding, with $L_c = 50$ nm and $\sigma = 2$ nm.

2.2.3 Combined loss

Figure 2.9 shows both simulated sources of loss on the same set of axes, as well as their sum. We see that according to the models, scattering losses should dominate until the waveguide width approaches around 0.6 micron. Previous to the submission of the design of the chip for fabrication, an erroneous implementation of the scattering loss model was used. This led to a mistake – as seen in Figure 2.9, and as will be seen in the analysis of the data, it would have been helpful to include waveguide widths less than 0.6 micron. Using the model with the error, however, did not initially suggest this, and the mistake was caught after the chip was fabricated. Study of this chip still proved to be edifying and a broader sweep of the parameters will be included in future work. In principle, the loss curve will change for different wavelengths. This will allow for future measurements at different wavelengths to further study the wavelength-dependent OH absorption contributions.

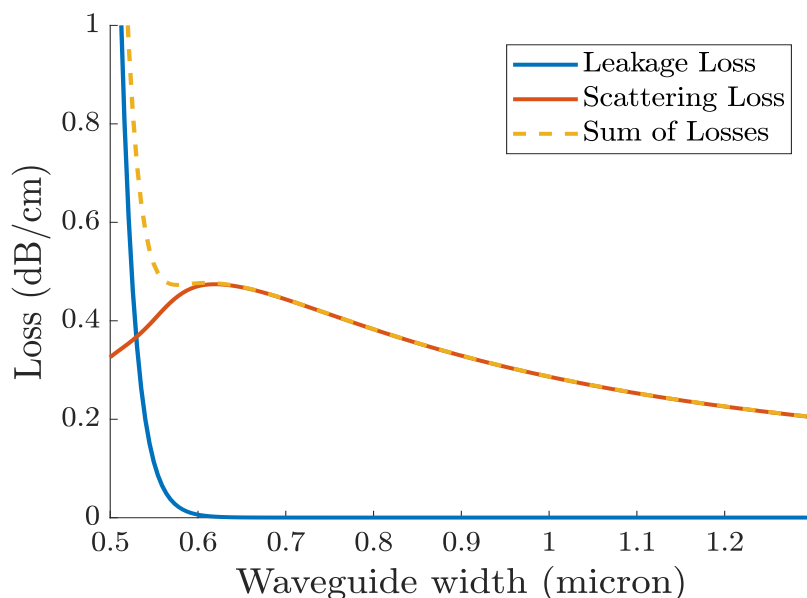


Figure 2.9: Both the simulated substrate leakage and simulated scattering loss are shown, as well as the sum of both. Simulations were performed at $2.9\ \mu\text{m}$ wavelength and on 500 nm SOI, 3 micron BOX, with no cladding.

2.3 Grating couplers

The completion of this experiment requires the automated measurement of hundreds of photonic devices with in-plane, waveguide-coupled light. The large number of devices makes an edge-coupling approach too space-inefficient for use [52]. One solution is to use a type of device called a focusing subwavelength grating coupler [53]. A scanning electron microscope

(SEM) image of a grating coupler is shown in Figure 2.10. Grating couplers couple out-of-plane light to in-plane light modes, and vice versa. The grating coupler is made up of a periodic diffraction grating and a tapered section of unetched silicon that ends at a waveguide. The grating is curved to focus diffracted light into the taper and couple to the waveguide. This allows for optical fibres to be placed above the chip to measure devices. A single fibre array containing multiple optical fibres can be held above the surface of the chip and moved from device to device to take measurements. This allows for input/output locations all over the chip, efficiently using the available space and allowing for automated measurement schemes (Section 3.4).

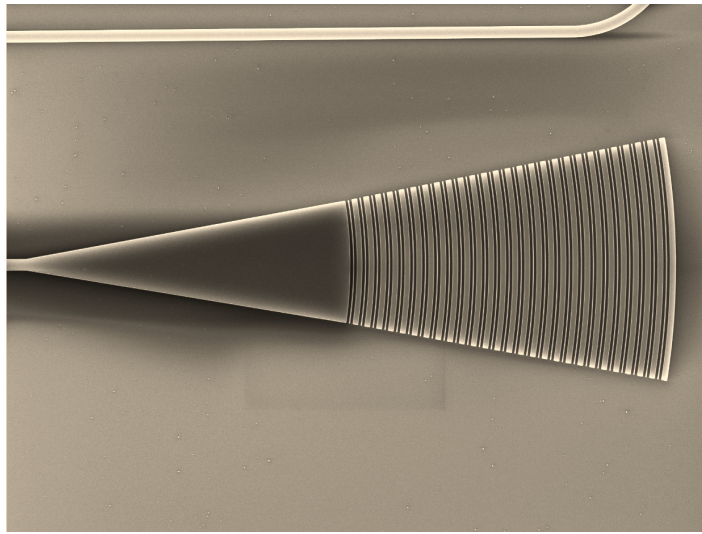


Figure 2.10: SEM image of printed grating coupler. Image supplied by the manufacturer, Applied Nanotools [36].

2.3.1 Theory

Figure 2.11 shows the 2D cross-sectional geometry of the chosen grating coupler design. The grating is made up of a periodic lattice of fully etched regions and regions of unetched silicon. This creates a repeating pattern of high and low effective index. Light propagating to the right in Figure 2.11 scatters off this grating upwards at an angle from the normal known as the insertion angle. Conversely, out-of-plane light incident on the grating at the insertion angle scatters and, if the design parameters are chosen correctly, couples into the confined modes of the waveguide, propagating away along the waveguide.

2.3.2 Design and optimization

The function of a grating coupler depends on the effective index contrast between high- and low-effective-index regions in the grating, as well as the periodicity of the grating [32]. Figure 2.12 shows the parameters that define the grating coupler geometry. The grating is a

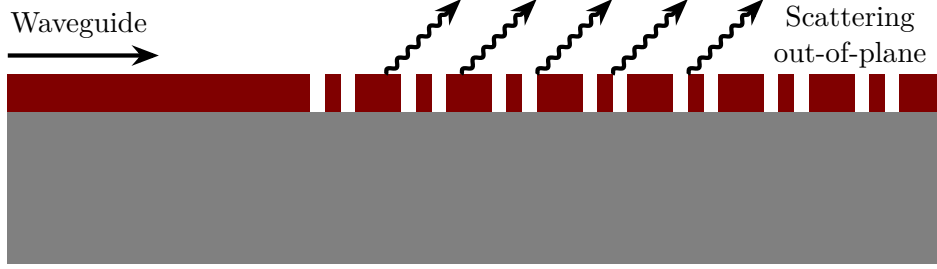


Figure 2.11: 2D geometry of a subwavelength grating coupler.

periodic structure that uses diffraction to couple the light modes of an out-of-plane optical fibre with the in-plane waveguide modes [54]. The directions of diffraction are determined by the associated Bragg condition for the grating, which can be expressed as [37, 55]

$$n_{\text{eff}} - n_c \cdot \sin(\theta) = \frac{\lambda}{P}, \quad (2.9)$$

where n_{eff} is the average effective index of the grating (not the waveguide), n_c denotes the index in the cladding ($n_c = 1$ for air), θ is the diffraction angle (insertion angle), λ is the wavelength, and P is the period of the grating.

For a given insertion angle, the grating period P , major grating width (Δ_h), and minor grating width (Δ_l) can be optimized to maximize transmission for a particular wavelength. The major grating width (Δ_h) determines the width of the high-effective-index regions of the grating, which is all silicon. The low-effective-index regions have length ($P - \Delta_h$) and are partially etched to lower the effective index of the region. The minor grating width (Δ_l) determines the effective index of the low-effective-index region of the grating. Together these regions determine the average effective index, n_{eff} , of the grating. It is possible to design a grating coupler with $\Delta_l = 0$, however this means that there is no control over the effective index of the low-index region, and so a high index-contrast between the waveguide and grating causes high back reflections [55].

Insertion angle may also be included in the optimization, though this is constrained by the available fibre array dimensions. The tip of the fibre array must be polished so that the array face can be parallel to the plane of the chip while the fibres are at the desired angle. Depending on the materials of the fibres and the array itself, only certain polish angles may be possible. In the case of this work, the available insertion angle was 8° and the grating couplers are optimized for this angle. It is possible to tilt the polished fibre array to adjust the insertion angle by $\approx 1\text{--}2^\circ$. Parameters that are fixed include the device layer thickness, cladding thickness, and the buried oxide layer thickness. The wafer substrate was 500 nm SOI with a 3 micron BOX layer. The grating coupler transmission was optimized for a wavelength of 2.9 micron.

Optimization proceeds by simulating the device performance in 2D using Lumerical's 2D FDTD solver. Figure 2.13 shows the basic simulation geometry. A pulsed source of

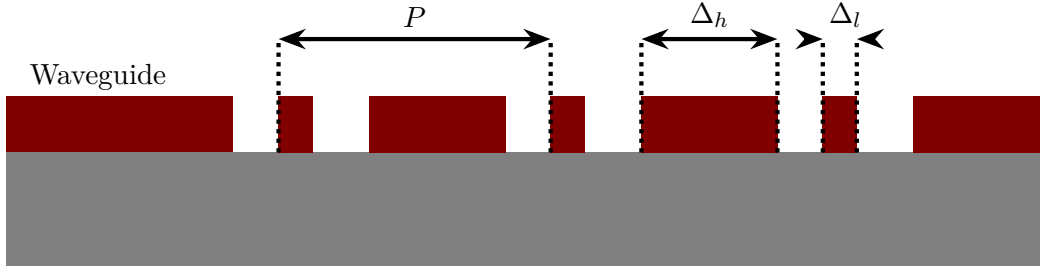


Figure 2.12: Design parameters of a sub-wavelength grating coupler, with the grating period P , major grating width (high-index region) Δ_h , and minor grating width (low-index region) Δ_l . The height of the grating is determined by the device layer thickness.

broadband light centered at $2.9\mu\text{m}$ is input at the selected insertion angle, and the simulation propagates the light over time until the total energy within the simulation region falls reaches below a cutoff threshold. The spatial mode of the input pulse is Gaussian. Simulation objects called “mode expansion monitors” use previously calculated waveguide mode data to record the amount of energy coupled into the fundamental waveguide mode over the course of the simulation, relative to the power of the source.

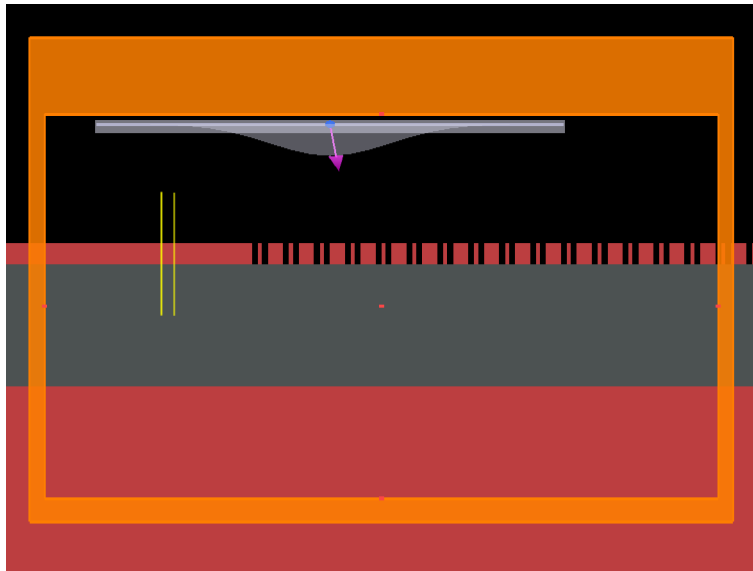


Figure 2.13: Screenshot of the Lumerical FDTD 2D-FDTD simulation set-up for optimizing grating coupler parameters. A Gaussian source pulse was input (indicated by the grey distribution and purple vector) from above with some insertion angle. Red layers indicate silicon, dark grey indicates SiO_2 , black is air. The orange region defines the simulation boundary, with “perfectly matched layer boundaries” that absorb scattered fields with minimal reflections [38]. A pair of “monitors” (yellow) measures the proportion of light coupled into the fundamental mode of the waveguide (propagating left).

To optimize transmission, a particle swarm optimization method is used as described in [56], which proceeds iteratively: for the first iteration, 50–100 points, called particles, are

randomly selected within the 3D parameter space (P, Δ_h, Δ_l) . The values of $(P, \Delta_h, \Delta_l)_n$ are each particle’s “position” coordinate in the space, called x_n for the n th particle. The simulation is run for each particle, where the particle’s x_n values determine the geometry of the device for that simulation. For each simulation the figure of merit (FOM) is recorded. The FOM is the property being optimized. In our case the FOM is the amount of optical energy coupled to the waveguide mode relative to the energy injected by the source, expressed as a transmission coefficient at $2.9\ \mu\text{m}$. We are aiming to maximize the FOM and so a numerically greater FOM is “better”.

Once the FOM has been calculated for each particle, the position with the best FOM of the collection is called the global best, g_{best} . Each particle will also have its own personal best position, p_{best} , which is the position of the best FOM yet calculated for that particular particle. To proceed with the next iteration, each particle’s position needs to be updated. This is done by assigning each particle a velocity in the parameter space and then calculating the next position for the particle by

$$x_n = x'_n + v_n, \quad (2.10)$$

where x'_n is the particle’s previous position, v_n is the particle’s velocity in the parameter space. To calculate velocity:

$$v_n = c_1 \cdot v'_n + c_2 \cdot A \cdot (p_{\text{best}} - x_n) + c_3 \cdot B \cdot (g_{\text{best}} - x_n), \quad (2.11)$$

where v'_n is the particle’s previous velocity, A and B are random numbers between 0 and 1 that introduce some noise to the movement, and (c_1, c_2, c_3) are constants throughout the simulation and set the level of inertia, the pull of the particle’s p_{best} , and the pull of the global best g_{best} , respectively. The coefficients (c_1, c_2, c_3) were left at the defaults of Lumerical’s FDTD software, which are discussed in the literature to converge well with photonics design problems [38, 56].

The simulation is then run for each particle using the new positions in parameter space, and so on. The result is a “swarm” of particles which move throughout the parameter space, and are drawn to increasing levels of the FOM. With enough iterations, the points will collect at the global maximum for the FOM within the parameter space. The position of the global maximum will be considered the best values of (P, Δ_h, Δ_l) for the design.

As the simulation must be run for each set of parameter values, it is inconvenient to perform this simulation in 3D FDTD, due to the long duration (hours) of each simulation. Therefore, the 2D approximation available in Lumerical FDTD Solutions is a good approximation for this application. After an optimized design is obtained in 2D simulations (Figure 2.14), a much longer 3D simulation was performed to further verify the design.

The 3D simulation results of the optimized grating coupler geometry are shown in Figure 2.15 along with the 2D results. The optimal parameters were $P = 1.19\ \mu\text{m}$, $\Delta_h = 0.581\ \mu\text{m}$,

and $\Delta_l = 0.149 \mu\text{m}$. We can also simulate the grating coupler by injecting light in the mode of the waveguide and monitoring the propagation of light out of the coupler into free space. The far-field projection of the diffracted light is approximately Gaussian, and so it is able to be matched to the Gaussian mode of an optical fibre.

The wavelength range for the 3D transmission simulation is constrained to keep the simulation time more manageable. Note that the 2D results do not agree with the 3D results, though nearly perfect agreement is possible (see [53]). The size of the 3D simulation is the likely cause, for several reasons: simulation boundaries that are too close to the source may cause higher loss, not enough of the grating may be contained in the simulation, and a simulation boundary in close proximity to the BOX-substrate interface will cause artificial loss of otherwise reflected fields. This is supported by observing an increase in agreement when increasing the simulation volume of the 3D simulation. Due to the length of the simulation time, convergence testing was not possible on the size of the 3D simulation. It is possible the 3D result may converge to agree with the 2D simulation given a large enough simulation. In light of limited resources, the 2D results are the best approximation to use. The results in Figure 2.15 represent the largest possible 3D simulation size with available hardware and realistic timescales.

The simulated transmission efficiency by 3D FDTD is approximately 38%, or -4.2 dB, while the 2D simulation suggests 60% or -2.2 dB, with back reflections of 4% when light is injected through the waveguide into the coupler. This range is comparable to telecommunications coupler designs, for which simulations have indicated -3.6 dB transmission at $1.55 \mu\text{m}$ [53].

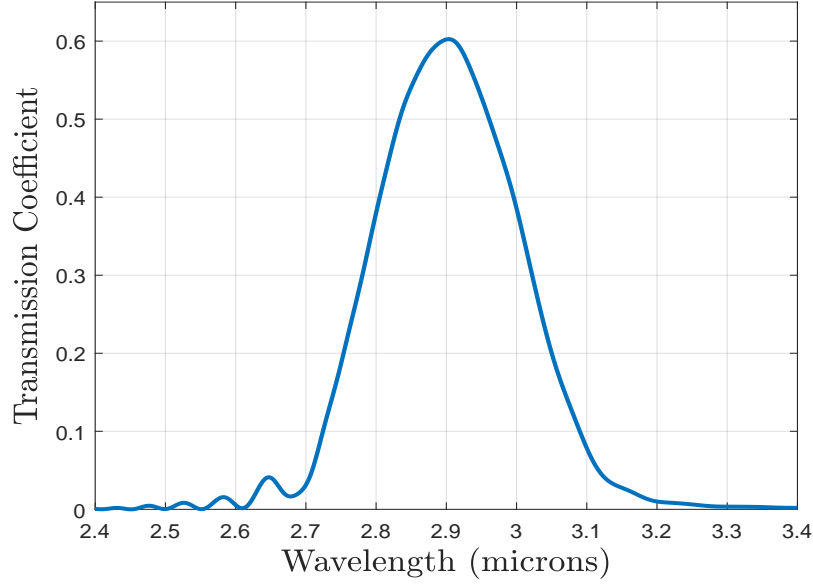


Figure 2.14: 2D FDTD simulation of the optimized grating coupler design for 500 nm SOI, 3 μm BOX layer, with $P = 1.19 \mu\text{m}$, $\Delta_h = 0.581 \mu\text{m}$, and $\Delta_l = 0.149 \mu\text{m}$.

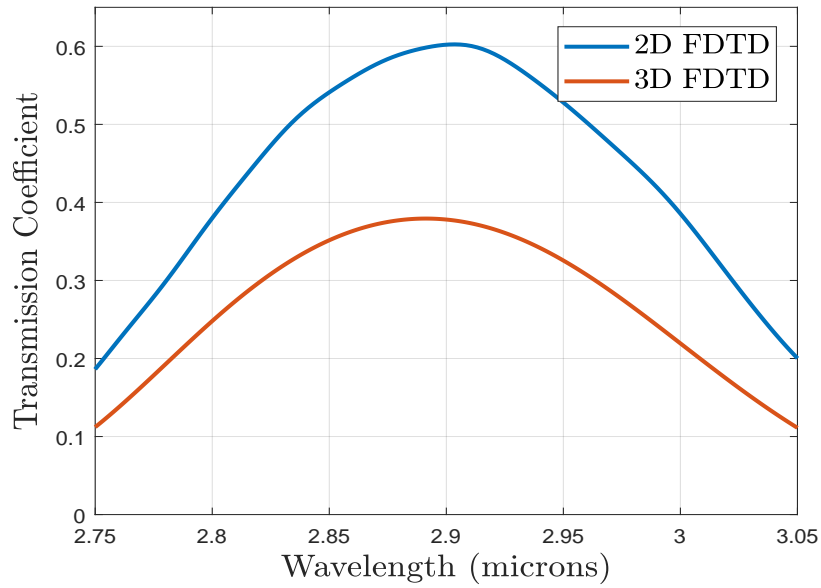


Figure 2.15: Results of both the 2D FDTD and 3D FDTD simulations of the optimal 2D grating coupler design for 500 nm SOI with a 3 μm BOX layer. The wavelength range of the 3D simulation is smaller to make the simulation time manageable.

Chapter 3

Experimental methods

3.1 Substrate

The wafer substrate used was produced by the manufacturer SOITEC part #G6P-024-01. This consisted of a 500 nm silicon device layer on top of a 3.0 micron SiO₂ BOX layer. The total wafer thickness was 626 μm , and the silicon orientation was (100) with 14–22 $\Omega\text{-cm}$ resistivity.

3.2 Layout

The goal of the overall chip layout is to allow for the measurement of waveguide loss for a number of different waveguide widths. The layout design accounts for possible spatial trends in the substrate parameters (device and BOX layer thickness) as well as fabrication quality. This is achieved by (1) randomizing the spatial distribution of device parameters within each section, and (2) including calibration structures throughout the chip.

3.2.1 Drawing in KLayout

The “GDS layout” is a 2D schematic describing the positions and geometry of the devices on the chip in the GDSII file format used by electron beam foundries. Our layouts were drawn with KLayout, a program for viewing and editing GDS file formats [57], by using the built-in Python scripting interface. We made extensive use of the “SiEPIC EBeam PDK & Library, for SiEPIC-Tools and KLayout” developed by Dr. Lukas Chrostowski at the University of British Columbia, which is available on GitHub [58].

3.2.2 Calibration structures

Every device on the chip is accompanied by a calibration device within close proximity (within 100 micron). A calibration device consists of two grating couplers with identical orientation, spaced by the fibre array spacing (127 micron). These calibration structures are joined by a short length of strip waveguide with width matching the associated device.

During data analysis, measurement of a device will be normalized to the signal measured via its associated calibration structure. This allows for two devices that are spatially separated on the chip to be compared directly, since any local variation of substrate or fabrication quality affecting the grating coupler efficiencies will be evident in the calibration device data, and are expected to shared with their corresponding device.

3.2.3 Waveguide switchbacks

The primary device measured in this experiment is a waveguide switchback. This device consists of two grating couplers with identical orientation and separated by the fibre array spacing ($127\ \mu\text{m}$) and connected by a strip waveguide. The basic design is shown in Figure 3.1. Beginning at the “input” coupler, the waveguide extends in a straight line away from the coupler to approximately $1/4$ of the desired length. The waveguide then is turned 180° towards the output coupler with a curvature radius of $20\ \mu\text{m}$. A total of 3 turns is made for all devices, with the waveguide ending at the output coupler. The distinctions of “input” and “output” are arbitrary, as the device is completely symmetric.

The waveguide curvature of $20\ \mu\text{m}$ is a conservative value to avoid excess loss due to the curvature, based on the minimum recommended value of $10\ \mu\text{m}$ determined by simulation in conjunction with our collaborator at UBC, Prof. Lukas Chrostowski. In addition, every switchback device has the same number of turns, regardless of waveguide length. Therefore any loss due to the curvature will be common to all switchback devices and will not affect the calculation of loss per unit length of the waveguides.

The total length of the switch-back device is easily varied, as well as the width of the strip waveguide. Each waveguide width selected on the chip has a number of devices with varying length, in order to extract a loss vs length for the waveguide. By use of the calibration structure normalization and a fit of the signal vs waveguide length, we can effectively ignore the insertion loss of the couplers themselves. See Section 3.5 for more details regarding data analysis.

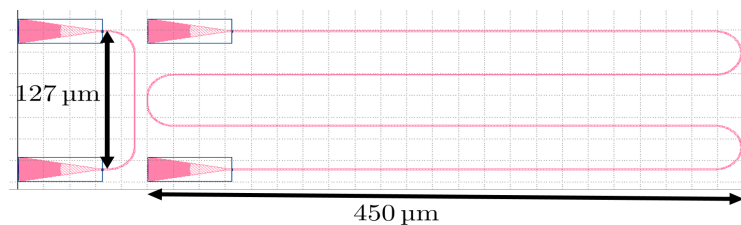


Figure 3.1: GDS layout of the unit cell of the waveguide switchback chip design, as viewed within KLayout. The two grating couplers on the left make up the calibration device and the switchback device is on the right.

3.2.4 Organization

The chip layout is organized into “blocks” (see Figure 3.2). Each block consists of 15 waveguide switch-back devices with their 15 calibration structures (see Figure 3.1). Each device has a different waveguide width, spread between 0.6 to 1.08 μm . All the switch-back devices in a block have the same total waveguide path length. There are a total of 7 different path lengths with a minimum of 1777 μm and maximum of 17 516 μm . Within each block, the order the waveguide widths are laid out is randomized, to prevent any spatial trends from appearing in the data.

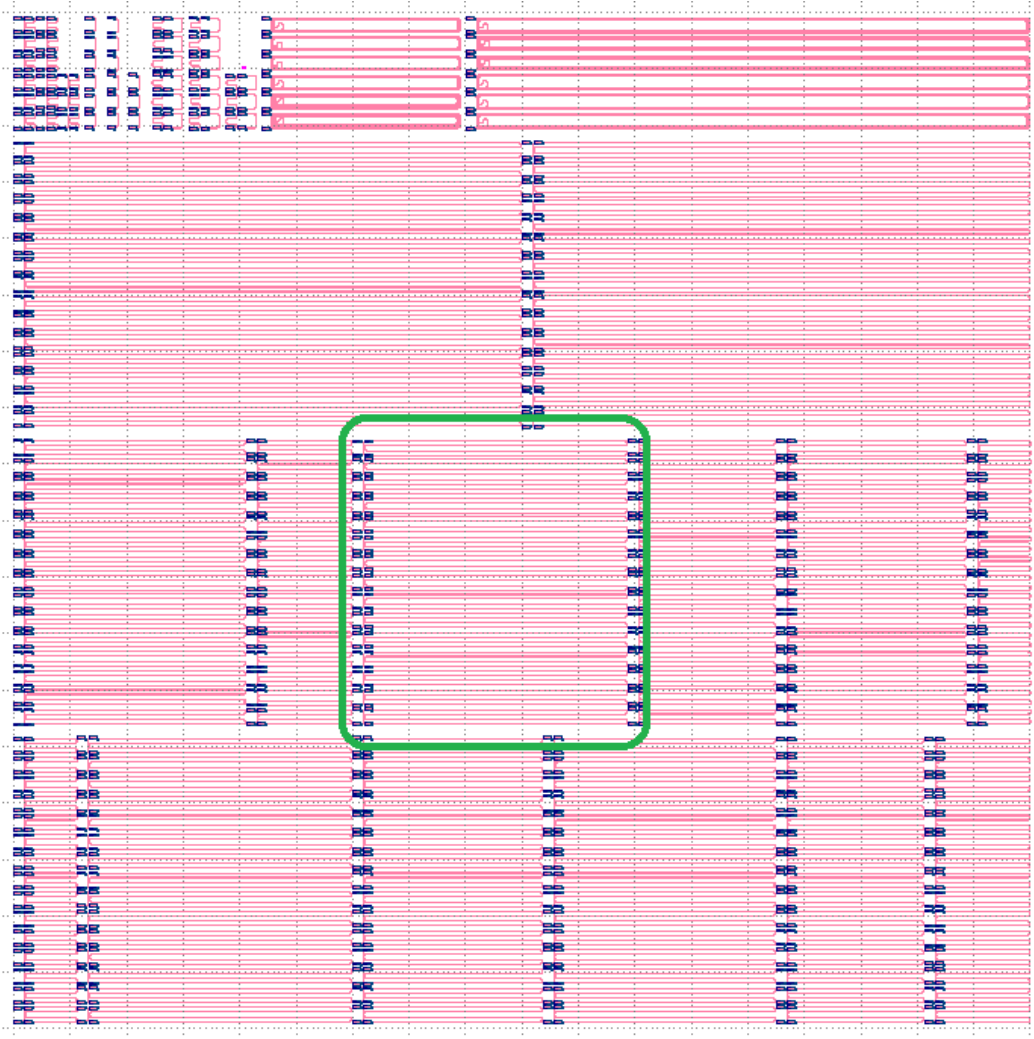


Figure 3.2: GDS layout of the chip as viewed with the KLayout program. The area bounded by the green rectangle contains a single “block” of the chip design; all of the switchback devices within this area are the same length but with varying waveguide width. The order the widths appear is randomized for each block to avoid trend effects in the wafer substrate.

In addition to the waveguide switchbacks and calibration structures, the layout shown in Figure 3.2 includes a collection of short waveguides connected with grating couplers in the top left and long waveguides in the shape of rectangular loops in the top right. These devices are intended to measure waveguide cross-talk (coupling, or light transfer, between waveguides in close proximity) and bend radius effects. Study of these devices will be used to inform future chip designs and will not be included in the discussion of waveguide loss.

3.3 Fabrication

3.3.1 Foundry

The chip layout design was sent to Applied Nanotools Inc. [36] for fabrication via a process of electron beam lithography (EBL) and inductively-coupled plasma reactive ion-etching (ICP-RIE) [36]. Specific parameters such as the EBL dose, resist recipe, and etch chemistry are proprietary and were not disclosed. In the EBL process, the device designs are drawn into an electron-beam-sensitive material spin-coated onto the wafer, called the e-beam resist. The areas of the resist that have been exposed to the e-beam become resistant to a chemical developer, which strips away the unexposed resist only. The result is a patterned layer on top of the silicon that is called the mask. Then the RIE process etches away the locations of silicon device layer that are left exposed until the underlying BOX layer is reached [36]. At the last step, the rest of the mask is chemically dissolved away, leaving behind the patterned (non-etched) silicon which makes up the devices.

3.3.2 Fabrication bias

An etch process can be isotropic or anisotropic. Isotropic etching removes material not protected by the mask in all directions at once. Isotropic etching has significant undercutting, where material is removed from beneath the mask at the edges of areas that are openly exposed to the etch. The width of features that result are narrower than the pattern on the mask, and the sidewalls are not vertical. In contrast, a purely anisotropic process cuts into the silicon in one direction, perpendicular to the plane of the silicon device layer, resulting in steep sidewalls and feature widths more closely matched to the patterns in the mask.

The ICP-RIE process used for our devices is anisotropic, but not perfectly, so there are still non-zero sidewall angles that contribute to the final width of features such as strip waveguides and gratings. With a Si device layer height of 500 nm, even a sidewall angle of 85° is significant. This means that the final, average width of the fabricated devices may be significantly different from the intended design. Depending on the duration of the ICP-RIE etch, the device widths may be either narrower or wider than desired. It is possible to partially compensate for this by introducing a fabrication bias to the design. The widths of features on each device are increased or decreased by the fabrication bias, with the intent that the resulting fabricated width of each feature will be approximately equal to the desired width. The choice of fabrication bias is based on recommendations and SEM data from the selected foundry.

The selection of bias proved difficult for this design, as the 500 nm 3 micron BOX substrate was new for the foundry and there was no available data for their process on this substrate. Based on their recommendations, and results from the standard 220 nm 2 micron BOX SOI usually used at Applied Nanotools, we chose a fabrication bias of -60 nm. This means that in our layout submitted for fabrication all device features were drawn

with widths 60 nm smaller than the optimal designs. Calibration structures also share the same fabrication bias as all other couplers on the chip.

3.3.3 Fabrication bias study – one more chip

In addition to the waveguide switch-back chip we have described, another layout was designed and printed as part of a batch run at the foundry. This chip was part of the same 25 mm x 25 mm wafer as the switch-back chip and was exposed to all the same fabrication conditions before dicing into separate pieces.

This second chip contains several thousand devices that are grating couplers attached by a short waveguide, similar to the calibration structures discussed in Section 3.2.2. The purpose of this chip is to study grating coupler performance over a large range of their parameters, including period, duty cycle, and fill-factor. Some devices were the optimal design but had varied fabrication bias applied. At the time of writing, only a selected subset of these devices had been measured. Devices that have different fabrication biases applied to them were and will be discussed in Section 4.5. This will allow us to find what the best fabrication bias to apply will be for future fabrication.

3.4 Experimental setup

The hardware and software for measuring the fabricated devices was developed by my colleagues Camille Bowness and Alex Kurkjian. I played a minor role in the overall design and wrote some Python-based interfacing for a lock-in detector.

The overall apparatus consisted of a system of motorized stages for positioning of the chip, a fibre array assembly to deliver light to or receive light from the chip, a laser assembly coupled into the fibre array, and a detector network including a lock-in detector. The custom software program written by my colleagues used a system of coordinates extracted from the GDS layout to move to the position of a specific device, optimize the position of the fibre array over the device for maximum measured signal through the device, and instruct the laser to perform a wavelength sweep.

3.4.1 Room-temperature infrared (photonics) testing apparatus (RITA)

The photonic chip was placed on an aluminum sample holder spin-coated with PMMA which dried to hold the chip in place. This sample holder was screwed into the top of a rotation stage mounted onto the top of two Micronix VT-50L linear stages coupled perpendicular to one another, allowing for 2D linear and rotational motion within the plane of the chip. A third identical linear stage is mounted above and holds another rotation mount, which in turn holds the fibre array assembly. This allows for the array tip to be lowered to within 50-100 micron of the chip surface, and for the insertion angle (see Section 2.3) to be adjusted.

Two computer-integrated microscopes were used to observe the array tip close to the chip surface for alignment and to prevent the array from making contact with the chip surface.

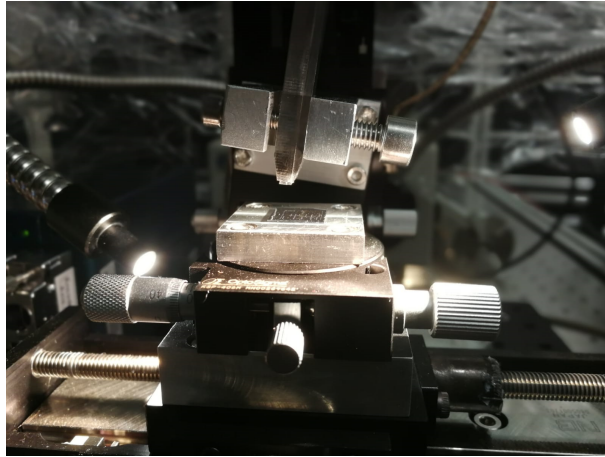


Figure 3.3: Picture of the fibre array tip above the chip, mounted on a sample holder and on top of the linear stages. Photo courtesy of Camille Bowness, Simon Fraser University.

3.4.2 Laser

The laser used to measure the devices was a multimode IPG Photonics model CLT mid-IR Cr:ZnSe/S laser fed by an IPG Photonics ELR-20-1587 pump laser. Output was continuous wave, multimode, linearly polarized, and tunable over 1.9 - 3.0 micron range with a linewidth of less than 0.5 nm, as quoted by the manufacturer [59]. The output wavelength is modified by moving the position of an internal stepper motor, with approximately 0.6 nm being the smallest wavelength step size used to take the data in this experiment. The laser power was too great for direct coupling into the fibres of the fibre array, and so a CaF₂ pick-off was used to select a small percentage of the laser output (≈ 25 mW) for coupling into the array. The rest of the beam terminated in a Thorlabs S310C thermal power sensor head connected to a Thorlabs PM100D meter to measure the power.

3.4.3 Fibre array

To couple light into/out of the chip, a custom-built FiberTech Optica Inc. fibre array was used. The array consists of a quartz linear v-groove array that holds four ZrF₄ mid-IR single-mode fibres with a core-to-core spacing of 127 micron. The array is held within a brass ferrule and polished to a 5 degree angle to obtain the desired grating-coupler insertion angle (see Section 2.3). The fibres end in FC/APC connectors for coupling via reflective collimators (Thorlabs RC04FC-P01).

3.4.4 Readout

Before entering the input collimator of the fibre array, the laser signal is passed through a chopper to modulate the delivered power and allow the use of a lock-in detector to isolate the signal coming out of the chip. Signal exiting the output collimator of the fibre array is measured by a Teledyne Judson Technologies indium arsenide (InAs) detector (TJ-420112). Current output from this detector is amplified by a DL Instruments Model 1212 current amplifier before being passed into an Ametek 5210 lock-in amplifier. Measured signal and sensitivity from the lock-in were polled by the computer via GPIB. It was important to record the sensitivity as the measurement software often changed it to select an appropriate range for a given device and wavelength. The laser’s output power was also recorded using a separate power meter, as described in Section 3.4.2.

It was found that the laser power was not a constant function of wavelength setting, and therefore it was important to normalize to the power measured by the power meter for each measurement. The final “signal” was then taken to be

$$\text{signal} = (\text{lock-in signal}) \times \frac{(\text{lock-in sensitivity})}{(\text{laser power after pick-off})}. \quad (3.1)$$

3.5 Data analysis

3.5.1 Wavelength sweep data

Typical wavelength sweep results for a calibration device on the chip are shown in Figure 3.4. Significant absorption lines are evident in the spectra, due to water absorption in the air. The approximate air path length was 35 cm. These absorption lines can be seen using a Fourier-transform infrared spectroscopy reference scan, as shown in Figure 3.5. The spectrum is measured using a supercontinuum laser source, which produces a highly broadband, “white light” laser beam [60]. The absorption peaks are too narrow to be properly resolved by the IPG laser, which is a limitation of its resolution. The amount of water vapour in the air is also a function of time as the temperature of the lab environment changes. This time dependence and the limited resolution of the laser make it so that the amount of water absorption differs between measurements of different devices.

In addition to the narrow absorption lines, significant fringing (a periodic modulation of the measured signal) in the IPG power spectrum is also observed. An example is displayed in Figure 3.6. These fringes in the grating coupler spectrum are not removed by normalization to the power spectrum, and we suspect that this is due to the shape of the laser mode changing as a function of wavelength. The laser is coupled into the fibre array via a reflective collimator in free space, and so a wavelength-dependent spatial mode affects this coupling and impacts the measured data. The portion of the laser beam that is terminated in the power meter will not be affected by the change in spatial mode to the same extent, and

so normalization to the measured power of the laser will not eliminate this effect from appearing in the data. The change in spatial mode of the laser as a function of its output wavelength will be characterized by future measurements.

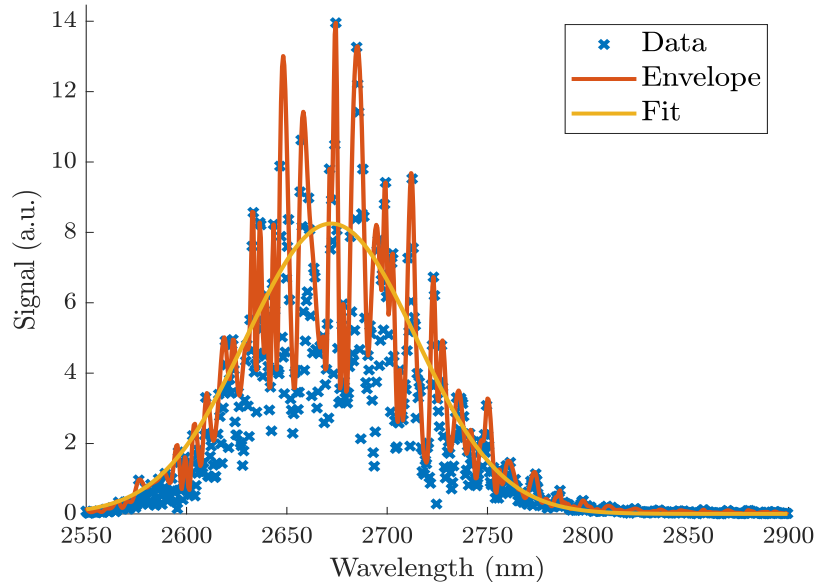


Figure 3.4: Wavelength sweep data for a typical calibration device on the chip.

These factors make it so that we cannot compare the measured signal at a specific wavelength between devices. This means that determining the loss at specific wavelengths is unreliable, preventing OH-specific substrate loss from being deduced and also prohibiting the use of the maximum of the spectrum to locate the peak transmission wavelength. Instead, statistical methods are used to capture the overall response of the grating coupler and smooth out the effects of the air path and IPG power fringing and result in a more repeatable measurement. We applied Matlab’s “`envelope()`” function with the peaks option selected, which uses a spline interpolation of local maxima to return the upper envelope of the signal. An upper envelope of the signal is appropriate because absorption or fringing can only decrease the response of the grating coupler, not enhance it. This envelope is then fit with a Gaussian to capture the overall magnitude, peak wavelength, and bandwidth of the grating coupler response.

The resulting fit is used to determine the signal by integrating under the fitted curve to obtain the level of signal, which will also be referred to as “integrated throughput”. The wavelength of the transmission peak of the device is determined by the location of the maximum of the Gaussian fit. To determine the signal for a particular waveguide switchback device, the integral under the curve fitted to the switch-back data was divided by (normal-

ized to) the integral under the curve fitted to the associated calibration structure, which is located nearby.

While the methods described above will allow useful information to be extracted from this data, the limitations of the experiment due to the IPG laser and absorption lines in the air are clear, as will be discussed in Section 4.5. To solve these issues, a new experimental apparatus was developed after the main experiment and used to measure a select few devices as proof of concept. The measurement apparatus consists of using the supercontinuum laser source as described above to create an extremely broadband input signal that is coupled into the fibre array and through the devices. The optical path from the output of the laser and into the input fibre of the array was minimized, contained, and purged with nitrogen. The output from the devices was coupled via fibre array directly into the FTIR spectrometer, which was evacuated. This setup takes advantage of the high resolution capability of the FTIR system and seeks to reduce the air absorption as much as possible. The results of these measurements are discussed in Section 4.5.

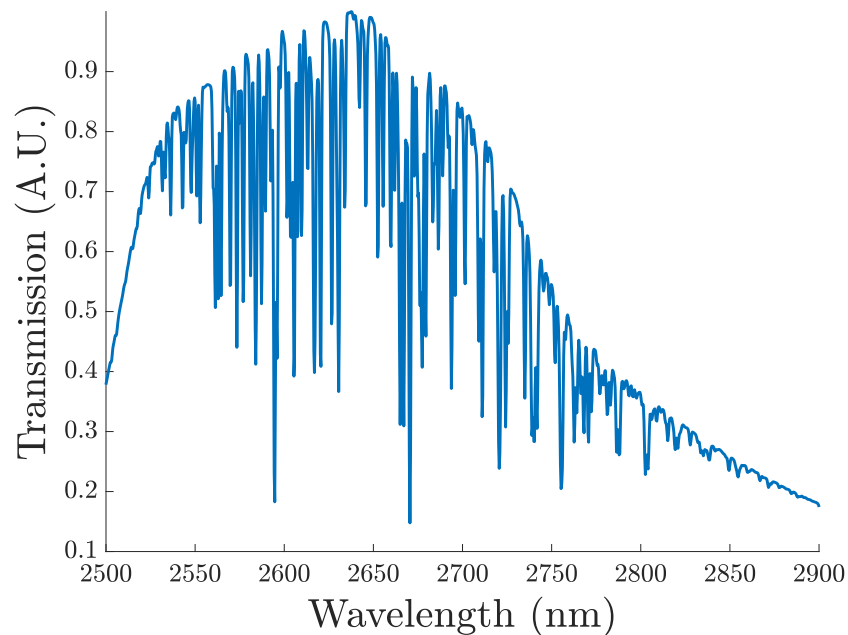


Figure 3.5: The results of a reference scan using a supercontinuum broadband laser source coupled into a Bruker FTIR spectrometer. The reference scan was taken by bypassing the fibre array and devices by directly connecting the input collimator to the output collimator with a length of optical fibre. The approximate air path length was 35 cm.

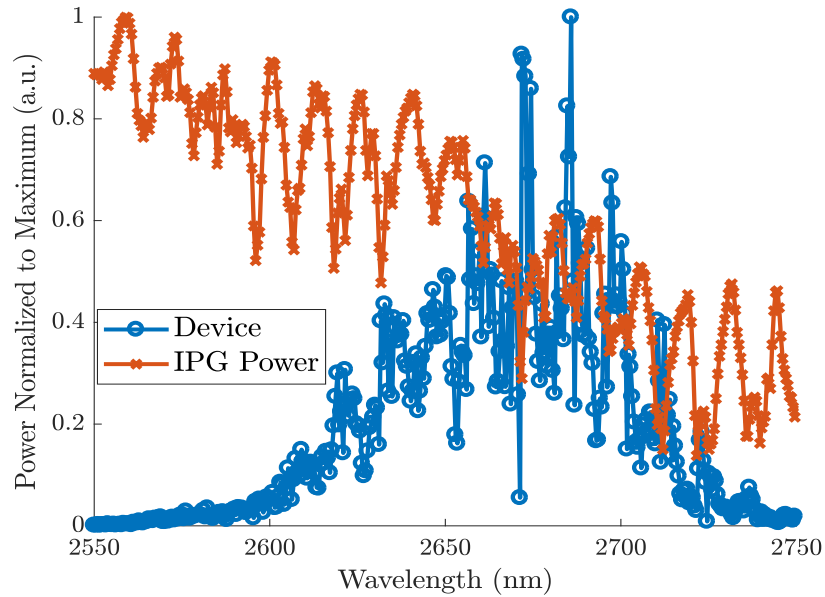


Figure 3.6: Wavelength scan of a calibration device plotted along with the power of the IPG as measured by the main beam passing through the CaF_2 pick-off. Both sets of data are normalized to their respective maximum.

Note that the device in Figure 3.4 was designed for peak operation at $2.9\ \mu\text{m}$, but has a peak between $2.65\text{-}2.7\ \mu\text{m}$. Two possible causes of this are a feature width error of the gratings due to the fabrication bias (Section 3.3.2) not matching the actual width error due to fabrication, and the fibre array not being at the insertion angle that is optimal (the couplers are designed for 8° insertion angle). The results of simulating these situations are shown in Figure 3.7 and Figure 3.8.

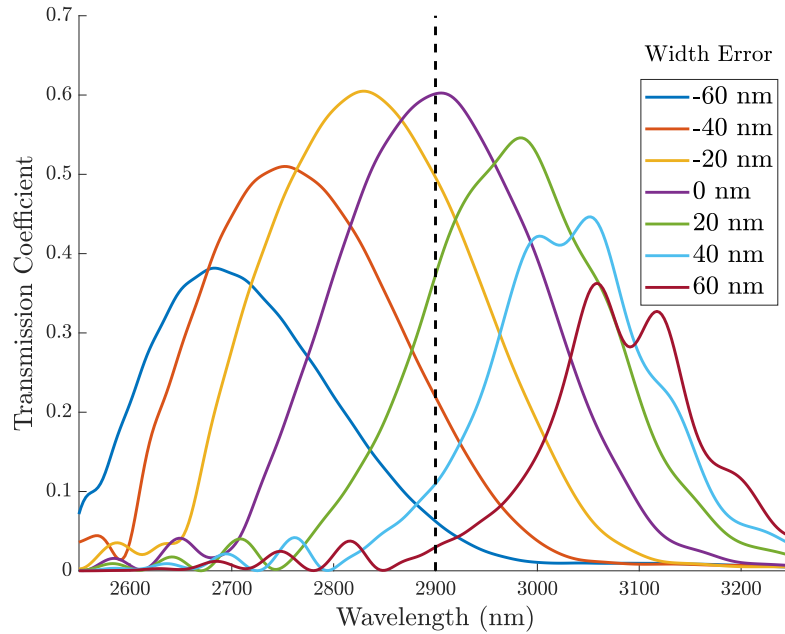


Figure 3.7: Simulated grating coupler spectra with varying grating width error. Simulations performed in 2D FDTD.

Figure 3.7 shows the results of simulating the optimal grating coupler design with various amounts of width error. As discussed in Section 3.3.2, the devices were printed with a -60 nm bias, anticipating a 60 nm increase in width from slanted sidewalls. If the actual increase is actually 0 nm (perfect sidewall angle), then our devices will have a bias error of -60 nm. Figure 3.7 shows that this would result in a spectrum similar to the device data shown in Figure 3.4. This suggests that the actual error in the fabrication process is possibly much less than a 60 nm increase. The peak position is also affected by insertion angle, as shown in Figure 3.8.

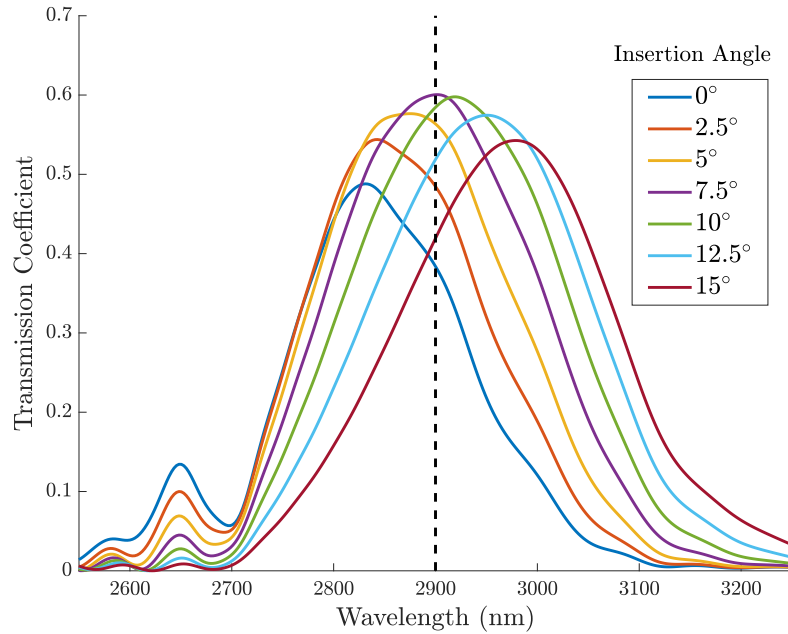


Figure 3.8: Simulated grating coupler spectra with varying input insertion angle. Simulations performed in 2D FDTD.

Figure 3.8 shows the effect on grating coupler peak transmission of changing the insertion angle away from the optimal angle of 8° . Decreasing the angle shifts the transmission peak towards smaller wavelengths. This suggests that the measurements were possibly taken with less than an 8° insertion angle. In conjunction with a possible fabrication error of much less than 60 nm, these two effects may be the cause of the shift from the design wavelength peak of $2.9\ \mu\text{m}$ to around $2.7\ \mu\text{m}$. Other effects, such as device layer thickness, may have also contributed.

As discussed previously, there is a high absorption band of OH groups present in silica in the vicinity of $2.72\ \mu\text{m}$, and so this shift presents a good opportunity to study the waveguide losses at this region. It will be edifying to compare this loss to a future study at $2.9\ \mu\text{m}$, which will be available once the actual width error and appropriate fabrication bias is determined for this substrate and process.

3.5.2 Loss vs length fitting

For each waveguide width, a dataset of normalized signal versus waveguide length is obtained. To extract the loss of the waveguide in dB/cm, the dataset is fit to

$$S(L) = Ae^{-BL}, \quad (3.2)$$

where S is the normalized signal, A and B are fitting constants, and L is waveguide length in metres. $L = 0$ indicates zero waveguide length and we can consider $S(0) = A$ to be the signal through a pair of grating couplers if they were connected directly and normalized to a calibration structure. The transmission through a length L of waveguide is then defined by

$$T(L) = S(L)/A = e^{-BL}. \quad (3.3)$$

The fitting parameter, B , gives the loss by

$$\text{Loss (in dB/cm)} = -\frac{10B}{\ln(10)} \times \frac{1 \text{ m}}{100 \text{ cm}}. \quad (3.4)$$

After fitting to the data, Equation 3.4 calculates the loss in dB/cm. Using this procedure, a new dataset of loss per unit length vs waveguide width is obtained.

3.5.3 Post-selection rules

Before the data is fitted, a post-selection process takes place that attempts to eliminate damaged or “dead” devices from contaminating the data. Physical damage to the surface of the chip (e.g. a scratch), or dust and other material deposits, may result in devices which function poorly or not at all, and do not accurately reflect the performance of the designed device geometry. The first condition for elimination was if the position of the peak of the wavelength scan (see Section 3.5.1) was greater than 2800 nm. This condition was chosen by visually inspecting the data sets: a peak above 2800 nm was, in every case, indicative of a dead device (low or no signal above the noise).

The second condition confines the dataset to only using devices for which both the device peak position and the calibration structure peak position fall within two standard deviations of the mean of all peak positions. This approach is chosen to identify outliers from the dataset in a consistent way. The set of all peak positions includes all devices and calibration structures, but excludes those points already eliminated by the first post-selection condition. The separate distributions of calibration structures and switchback devices may differ due to material absorption, and so more analysis of the remaining dataset is needed. A detailed discussion of the statistics of the distributions of peak positions is included in Section 4.2.3.

The third condition compared the normalized signal, or integrated throughput, of the device to the average of all the devices with the next greatest length. If the signal of the device was more than 40% less than this average, the device was ignored. This is because shortening the length of the switchback implies an increase in signal, so any serious deviation from this trend suggests a damaged device (which performs unreasonably poorly). Figure 3.9 is an example of one of the signal versus length plots of the dataset after the post-selection rules have been applied. The plots for other waveguide widths are similar.

Finally, any device with an integrated signal greater than its associated calibration structure was eliminated, because this indicates that the calibration structure is damaged or performing poorly. Section 4.3 looks at the spatial distribution of excluded points in the data.

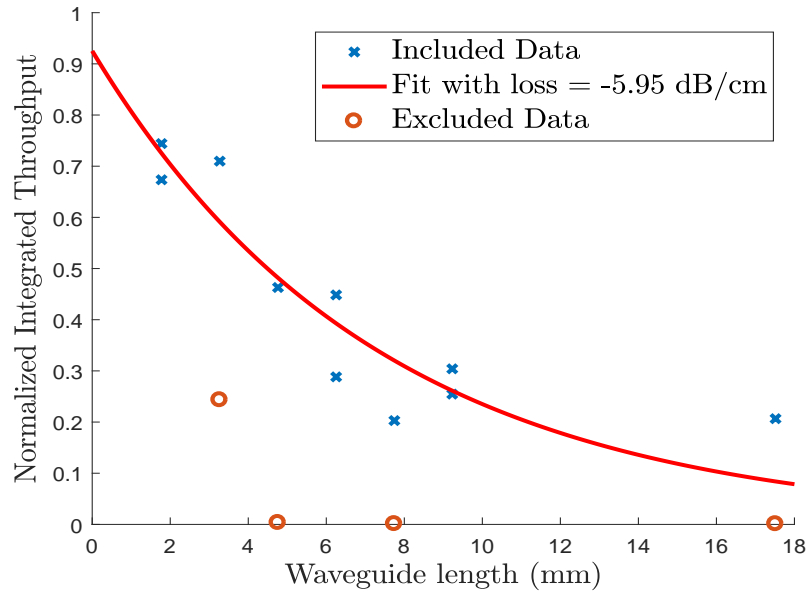


Figure 3.9: Integrated throughput signal normalized to calibration structure vs the length of waveguide switchback for waveguide width of $0.615\ \mu\text{m}$. The three rightmost excluded data points were eliminated due to having a wavelength-scan peak position $> 2800\ \text{nm}$. The leftmost excluded point was excluded due to being more than 40% lower than the point after it (and therefore it is likely damaged).

Chapter 4

Results

4.1 SEM and optical images

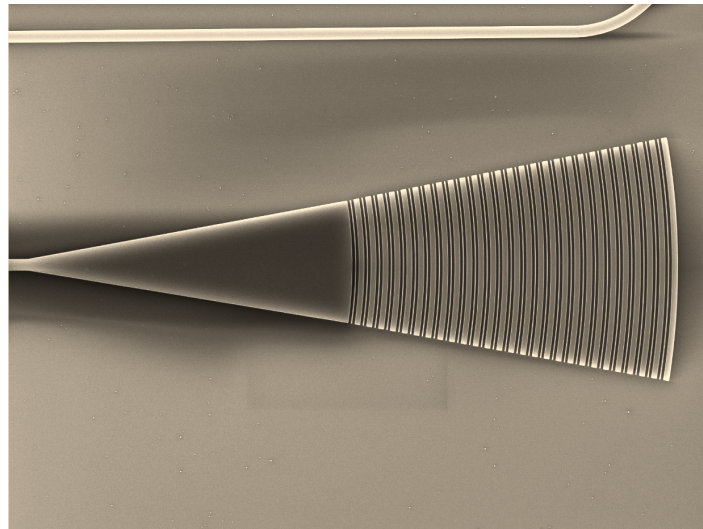


Figure 4.1: SEM image of printed grating coupler. Image supplied by the manufacturer, Applied Nanotools [36].

Figure 4.1 shows a scanning electron microscope (SEM) image of one of the subwavelength grating couplers that were fabricated. Analysis of the metrology structures such as the one shown in Figure 4.2 and performed by Applied Nanotools [36] indicate that the average error in feature widths was approximately +19 nm (corresponding to a 84.5 degree sidewall angle). This is good because the etching process produced steeper sidewalls than expected for the 500 nm SOI. However, the devices on the chip were biased for +60 nm error (that is, made 60 nm smaller), and so it can be expected that the resulting structures (especially grating coupler gratings) will be 41 nm narrower than the intended design, or a -41 nm error. This is in agreement with the discussion in Section 3.5.1, that used simulations to suggest that a negative width error could account for some of the observed shift of the transmission peak away from 2.9 μm for the grating couplers.

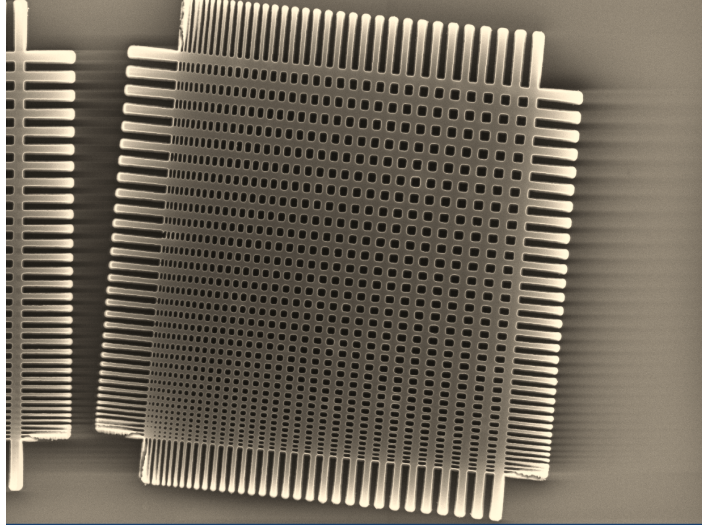


Figure 4.2: SEM image of metrology structure. GDS design supplied by Dr. Lukas Chrostowski at the University of British Columbia. The cross-hatch pattern has varying feature width and spacing. Image supplied by the manufacturer, Applied Nanotools [36].

4.2 Grating couplers

4.2.1 Wavelength sweep data

The analysis of the data taken in this experiment relies on the use of calibration structures to normalize the signal from each switchback device and attempt to remove spatial trends such as fabrication etch quality, device layer thickness, or physical damage to the grating couplers (discussed in Section 3.2.2). Figure 4.3 and Figure 4.4 show the wavelength sweeps and fits for two switchback devices with equal width (width = 0.615 micron) but different length (1.777 mm compared to 17.516 mm, respectively). The nearby calibration structure data is also shown for each device.

First we compare the signal of the calibration structures in both sets of data in Figures 4.3 and 4.4, and note that they differ by approximately 20% in maximum signal, but appear to have similar bandwidth. This suggests that the fabrication conditions at the location of the device in Figure 4.4 result in grating couplers with less efficiency. The device signal in Figure 4.3 is similar to the calibration device, whereas for the longer, 17.516 mm waveguide the device signal is much lower, as expected. Importantly, we note that the wavelength of the peak for the device and calibration fits differs in both cases. In order to support the validity of our calibration-normalization approach, we must analyze the statistics of peak positions for the data, which is the topic of Section 4.2.3.

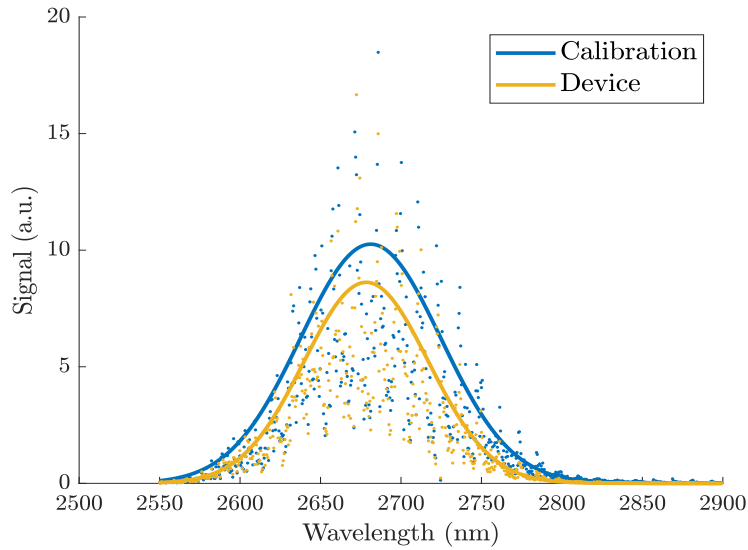


Figure 4.3: Wavelength sweep data of a waveguide switchback device with $0.615\ \mu\text{m}$ waveguide width, and $1.777\ \text{mm}$ waveguide length, and its nearby calibration structure.. Signal is normalized by Equation (3.1). Curve is the Gaussian fit to the upper envelope (see Section 3.5.1).

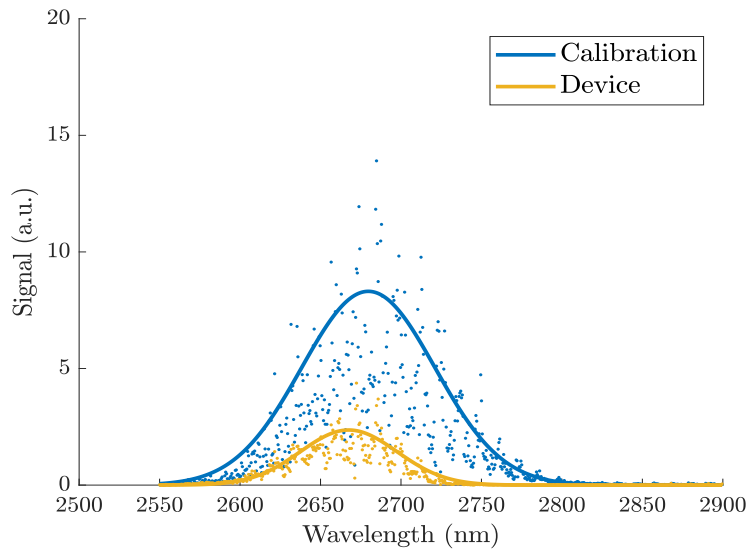


Figure 4.4: Wavelength sweep data of a waveguide switchback device with $0.615\ \mu\text{m}$ waveguide width, and $17.516\ \text{mm}$ waveguide length, and its nearby calibration structure. Signal is normalized by Equation (3.1). Curve is the Gaussian fit to the upper envelope (see Section 3.5.1).

4.2.2 Calibration heat-map

Figure 4.5 shows the spatial distribution of the calibration structures across the chip. The colour of the points is determined by the peak wavelength of their wavelength sweep data, and we can see that there are no apparent spatial trends across the chip that affect peak wavelength. The relative size of the points in Figure 4.5 shows the relative strength of the signal for each calibration device. Aside from a few devices which are weaker (possibly damaged), we can also note that there appears to be no spatial trends across the chip that affect the throughput of the grating couplers.

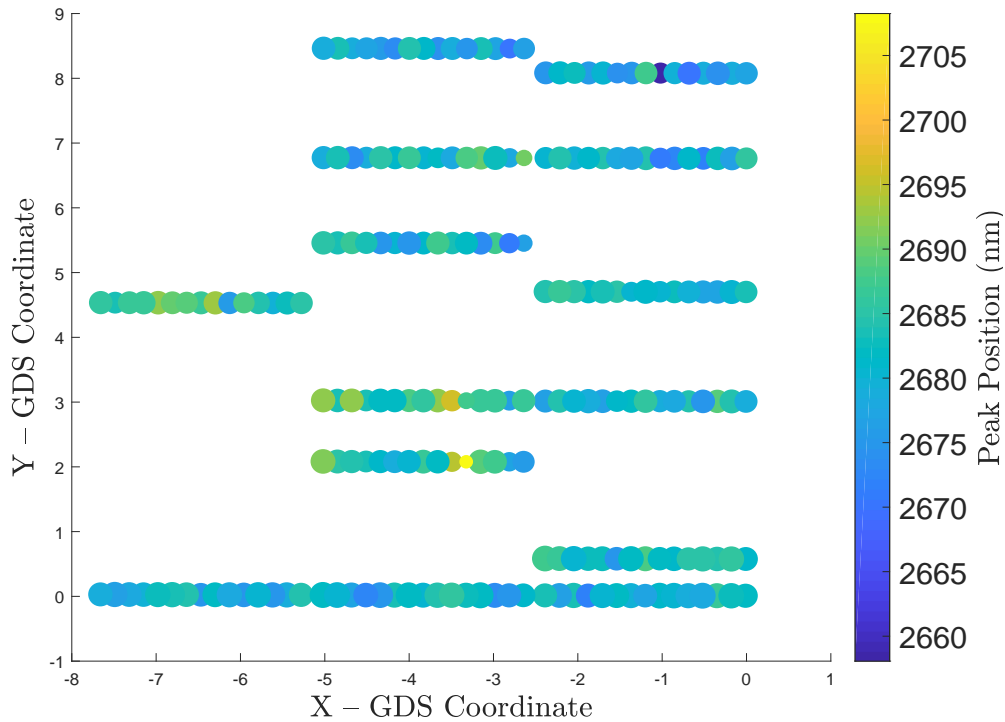


Figure 4.5: The spatial distribution of calibration structures across the chip, as a function of the design GDS coordinates. The peak wavelength is shown by the colour of each point (colour bar on the right), and the relative size of each circular point is determined by its integrated throughput signal (normalized to the max of the dataset). Note that this plot is rotated 90° counter-clockwise relative to the GDS pattern shown in Figure 3.2.

4.2.3 Peak position

Histograms

Because we are using an integral approach for determining the “signal” metric used for the loss calculation (Section 3.5.1), it is important to consider the distribution of the peak wavelengths of the Gaussian fits to the data. If the positions of these peaks are spread too widely, we would not be able to compare devices directly to calculate loss. In addition, if device grating couplers have peaks that differ too greatly from their associated calibration structures, then normalization is inappropriate. Ideally, the peak position distributions should be narrow enough that we can calculate and consider our loss results to be for a relatively narrow wavelength region.

Figure 4.6 shows two histograms of peak positions for the data, separated into two groups: devices (waveguide switchbacks), and calibration structures. For the switchback devices the distribution mean is 2677 nm with a standard deviation of 10 nm, and standard deviation of the mean of 0.7 nm; for calibration structures the mean is 2681 nm with standard deviation of 6 nm, and standard deviation of the mean of 0.4 nm. There is significant difference between the distributions. Figure 4.7 shows the distribution of peak wavelength differences between devices and their nearby calibration structures. The average difference is 5 nm, with a standard deviation of 10 nm, and standard deviation of the mean of 0.8 nm.

One possible reason for these observed differences in peak wavelength between calibration structures and their waveguide switchback devices is material absorption. Wavelength-dependent absorption due to OH impurities may be shifting the observed peak wavelength of the grating couplers. This shift would be dependent on the amount of absorption, and so we expect that this effect will be more pronounced for longer switchback devices and smaller waveguide widths. A more detailed investigation of the peak wavelength differences will be edifying, but is not included in this work.

For normalization of the switchback measurements, the desired method is to normalize for each measured wavelength, point-by-point. However, as discussed in Section 3.5.1, we do not have a reliable signal measurement for specific wavelengths. We do require normalization, and so we choose to use the overall response, or integrated throughput, as discussed in Section 3.5.1.

The overall distribution (including all peak positions of both types) has a mean of approximately 2680 nm, and this will be considered the center of the wavelength range for which we have calculated waveguide losses. The results of the post-selection described in Section 3.5.3 are shown in Section 4.2.3. These couplers were designed for operation at $2.9\ \mu\text{m}$, so this is a significant shift away from the design peak transmission wavelength. Section 4.1 shows that the width error of the devices is approximately -41 nm. As we have seen, this error, plus an insertion angle less than 8° , may account for some of this shift.

Additional parameters that may shift the peak locations include the slanting of the grating sidewalls, and variation in the Si device layer height or BOX layer depth.

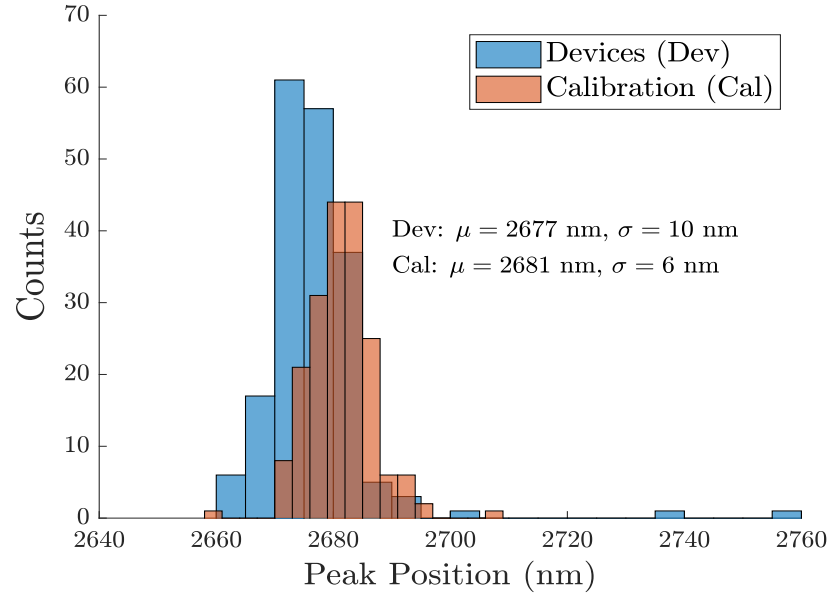


Figure 4.6: Histograms showing the distributions of Gaussian fit peak position for the device and calibration structure wavelength sweep data. The figure text indicates the mean (μ) and standard deviation (σ) of the data.

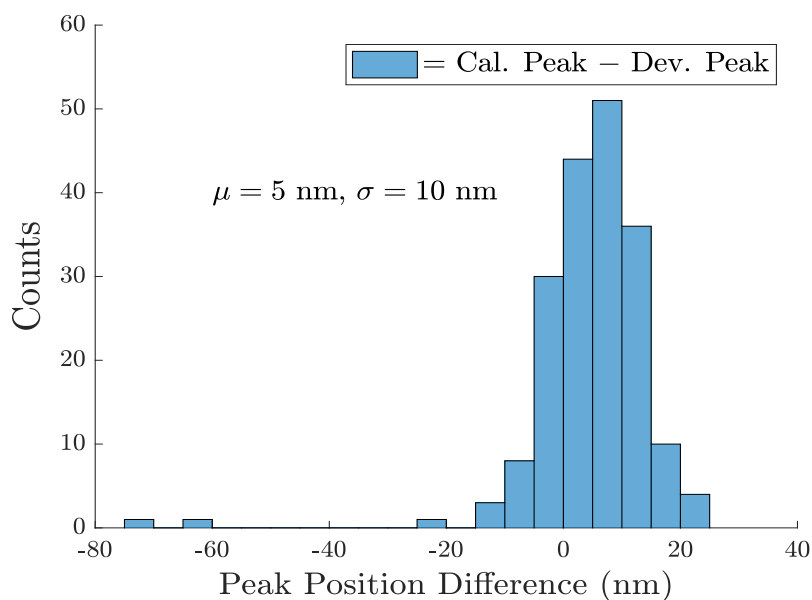


Figure 4.7: Histogram showing the distribution of the wavelength difference between device and associated calibration structure peaks, which are spatially correlated. The calculation is (Difference = Calibration Peak – Device Peak). The figure text indicates the mean (μ) and standard deviation (σ) of the data.

Figure 4.8 shows the spatial distribution (as a function of the design GDS coordinates) of the devices. The colour bar indicates the difference between the device peak wavelength and the peak wavelength of the nearby calibration structure. The points share a common, arbitrary size. Some devices have been removed since their peak positions were greater than 2800 nm and were suspected to be damaged (see Section 3.5.3). We see that there are no spatial trends to this difference data, aside from the two ≈ -60 nm outliers which appear in close proximity to one another near coordinates $(X, Y) = (-6, 0)$.

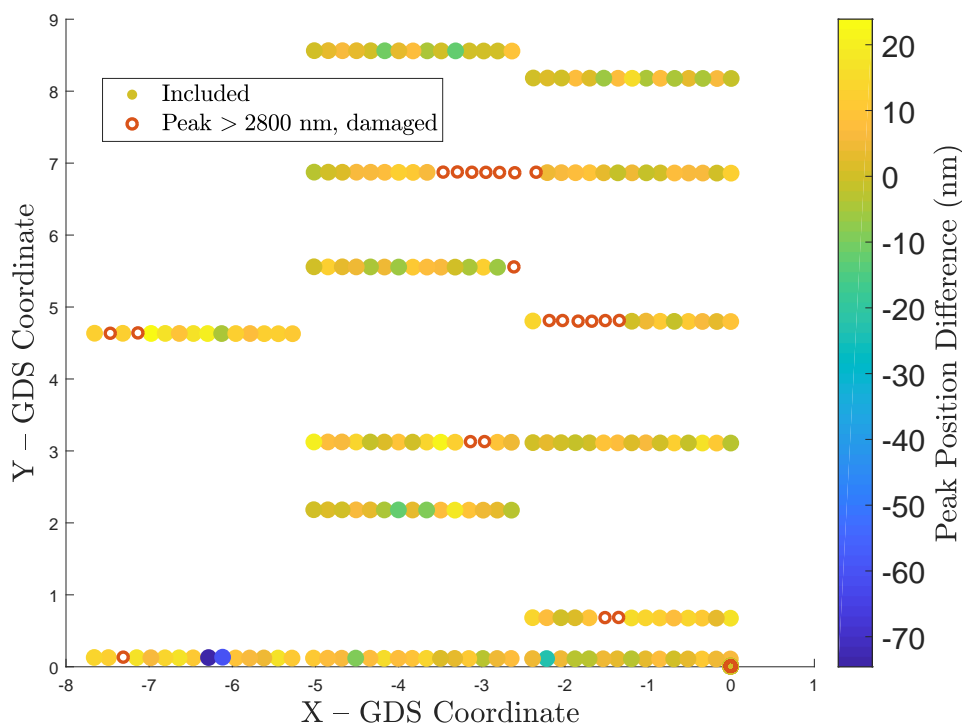


Figure 4.8: This 2D heat-map plot shows the peak wavelength difference for devices and their calibration structures across the chip. X and Y axis are the GDS coordinates from the layout design (in mm). The points share a common arbitrary size. Note that this plot is rotated 90° counter-clockwise relative to the GDS pattern shown in Figure 3.2.

Peaks Post-Selection

As described in Section 3.5.3, one of the post-selection rules eliminates any devices for which the device peak wavelength or its nearby calibration structure’s peak wavelength differed from the average peak wavelength by more than two standard deviations. To visualize how each set of devices, organized by waveguide width, may be affected by this rule, Figure 4.9 groups the wavelength peak data by waveguide width. We see that, at most, only 2 devices have been eliminated from any one set of waveguide widths by this rule.

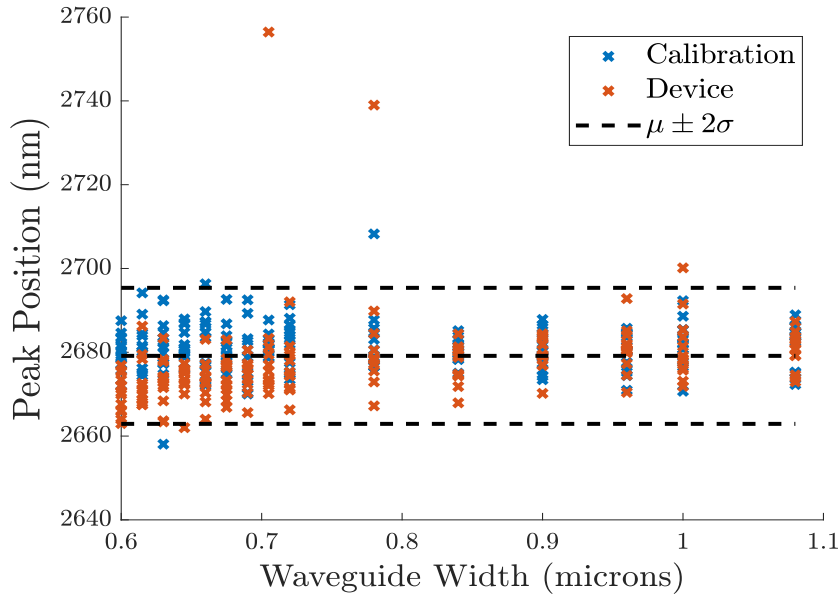


Figure 4.9: The $2\text{-}\sigma$ peak position post-selection rule for device and calibration peak wavelength. Points that fall outside the range $(\mu - 2\sigma, \mu + 2\sigma)$ are eliminated, where μ is the mean and σ is the standard deviation of the data.

4.3 Device yield

Figure 4.10 shows the spatial distribution of devices across the chip as a function of the chip design's GDS coordinates (in mm). The orange circles indicate points that have been excluded by the post-selection rules described in Section 3.5.3. We can see that excluded points appear across the chip, with only two rows of devices that have every point included. There are two locations, specified by GDS coordinates $(X, Y) \approx (-3, 7)$ and $(X, Y) \approx (-1.5, 5)$, that show a long group of 6+ devices that are excluded. These locations are likely sites of localized damage or interference, such as a physical scratch or the presence of dust particles.

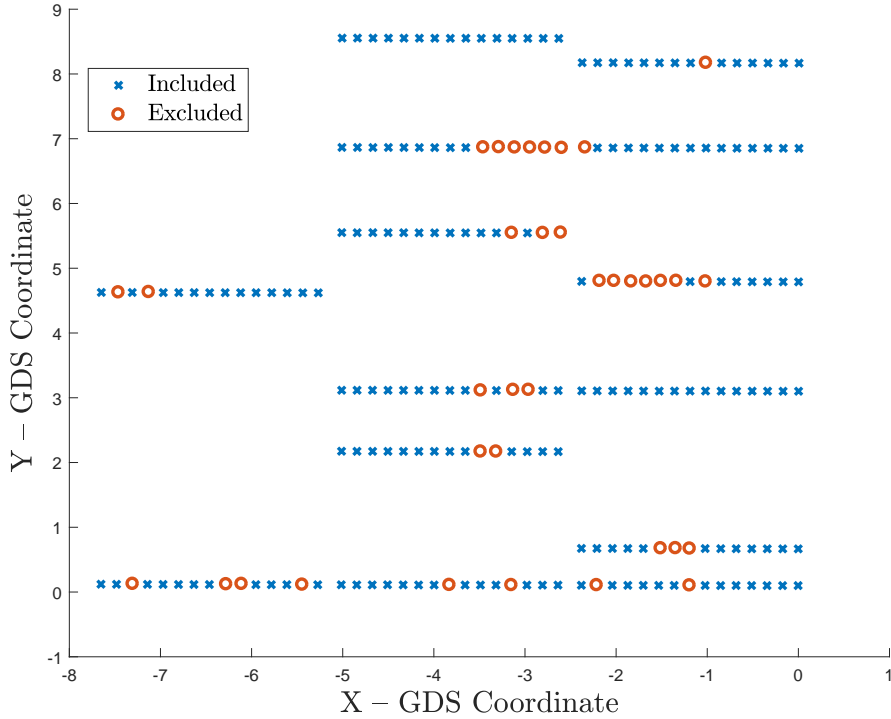


Figure 4.10: This plot shows the spatial distribution of devices across the chip as a function of the chip design’s GDS coordinates (in mm). The plot indicates which devices are included in the analysis and which have been excluded by the post-selection rules as defined in Section 3.5.3.

4.4 Waveguide loss as a function of width

Figure 4.11 shows the final results of the data analysis process carried out on all the measurements as described in Sections 3.5.1 and 3.5.2. Each data point is the calculated loss based on a fit of a signal versus waveguide length dataset for each waveguide width. The error bars displayed on Figure 4.11 represent the $1-\sigma$ intervals for the calculated loss. When fitting the loss versus width data in Figure 4.11, data points are weighted inversely to the size of their 68% confidence interval, to make points with smaller error more significant when fitting.

Fitting using the Payne-Lacey model for scattering losses necessarily uses an interpolated fit of simulated effective index values, leaving only L_c and σ as fitting parameters. The results depicted in Figure 4.11 show that the scattering loss model poorly describes the data. The exponential substrate leakage loss fit appears to do better, but ultimately neither fit produces meaningful fit parameters or a significant R^2 value. It is clear that more data points are required in the $0.70 - 0.85 \mu\text{m}$ width range.

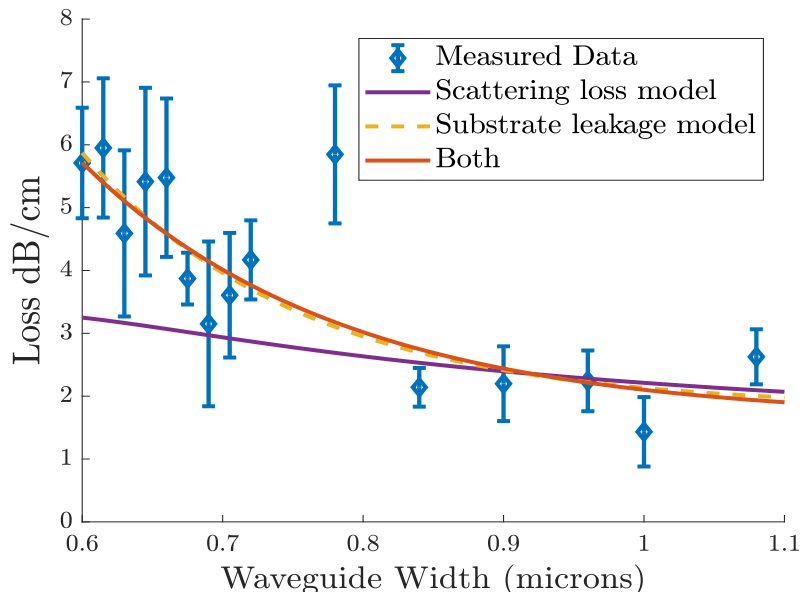


Figure 4.11: Waveguide loss (dB/cm) vs waveguide width at 2680 nm wavelength. Three attempts at fitting are shown. The curve indicated as “Both” fits the data using the sum of the Payne-Lacey scattering loss model and an exponential fit. All fits include a constant term to capture additional sources of loss.

The results suggest that losses are dominated by substrate leakage, and may be chiefly due to OH absorption. To determine if OH absorption is the primary factor, we need to study the loss at $2.9\ \mu\text{m}$ as well, since the OH absorption band is weaker there. As we will discuss in Section 4.5, other measurements will allow for couplers to be designed successfully at $2.9\ \mu\text{m}$ in the future.

We have measured waveguide loss at $2.7\ \mu\text{m}$ to be on the order of 1-2 dB/cm for $1.0\ \mu\text{m}$ waveguide width. This level of loss is almost compatible with cavities with the quality factor of $Q = 10^5$ required for the Se^+ proposal [26]. This loss is expected to decrease at $2.9\ \mu\text{m}$ wavelength, since OH absorption is less in that region, though this remains to be seen in future work.

4.5 Fourier-transform infrared spectroscopy

As discussed in Section 3.3.3, a second photonics chip was fabricated with devices to study grating coupler parameters. We have used the supercontinuum laser and FTIR apparatus described in Section 3.5.1 to measure a number of devices that are equivalent to calibration structures. The grating coupler parameters of these devices are the optimal values for operation at $2.9\ \mu\text{m}$ based on simulation, but have varying amounts of fabrication bias. The

data in this section allows us to (1) evaluate the improvement offered by the FTIR measurement scheme, and (2) identify the correct fabrication bias for this fabrication process and substrate.

Figure 4.12 shows the results of one of the devices, along with an asymmetric gaussian fit used to identify its peak transmission wavelength. The asymmetric model is based on Aaron et al 2008 [61] and was chosen by inspection. Note the absence of sharp absorption lines. This shows that the nitrogen purging of the input and evacuation of the FTIR system (Section 3.5.1 for description) effectively eliminates the absorption lines, indicating that the source of these lines was optical path length in air, as suspected.

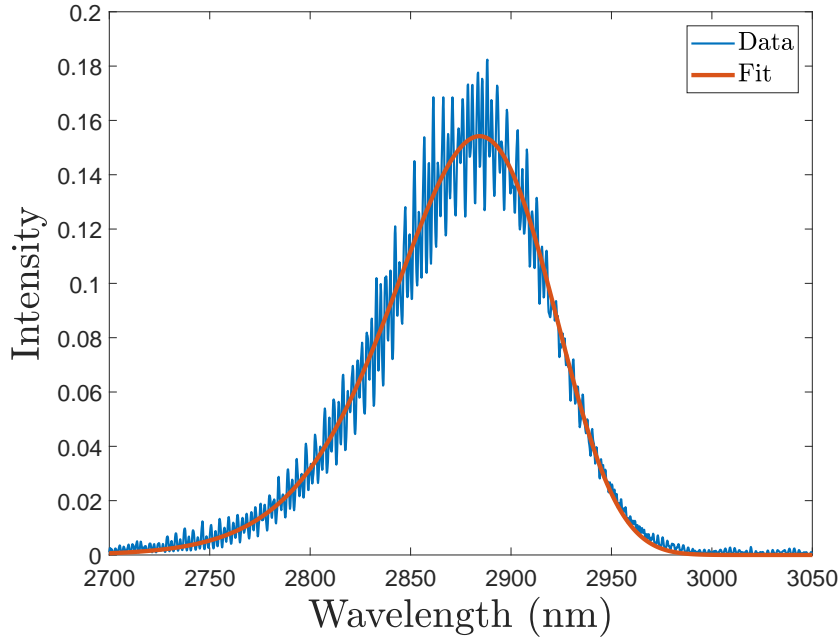


Figure 4.12: FTIR spectrum of a calibration device with 0 nm fabrication bias using a supercontinuum broadband laser source with a fully purged/evacuated free space beam path. The spectrum is fit using an asymmetric Gaussian model [61].

The source laser is the highly broadband supercontinuum, and so the periodic modulation in signal is not due to the power spectrum of the laser. The frequency of these fringes correspond to length scales on the order of 10-100 μm , which suggests they are caused due to interference from reflections between grating couplers in the devices. In addition to the distance between the gratings of each grating coupler along the connecting waveguide, the distance from fibre tip to chip surface also matches this length scale. Further study is required to confidently identify the source. However, the modulation is regular and the fit model is able to match the data with an adjusted $R^2 > 0.90$. Figure 4.12 clearly shows that

the FTIR system will be superior for measuring wavelength-dependent loss in the mid-IR at this wavelength, as well as photonic cavities for the Se^+ qubit scheme.

Figure 4.13 shows the spectra of several devices with varying fabrication bias, normalized to their respective maxima. We see that approximately 0 nm of fabrication bias achieves operation at the target wavelength of 2.9 μm . This suggests that fabrication resulted in steep sidewalls with very little feature width error. For future device fabrication, this suggests that an appropriate bracket (a set of three copies of each device with different biases) for fabrication biases would be on the order of -10 nm, -5 nm, and 0 nm to achieve operation at 2.9 μm . Having a range of biases accounts for the next fabrication run having slightly different error, and any changes in insertion angle, which has a less significant effect on the peak transmission (Section 3.5.1).

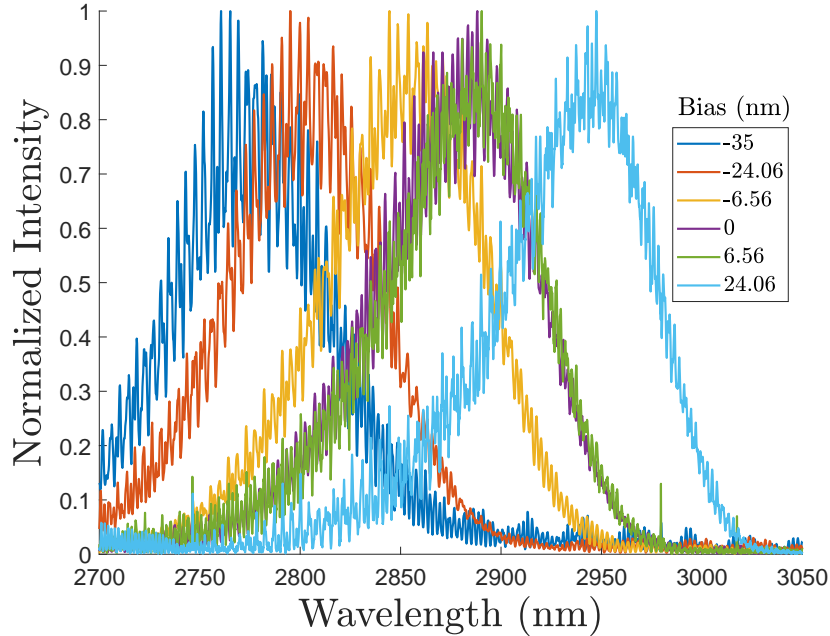


Figure 4.13: FTIR spectra of calibration devices with varying fabrication bias using a supercontinuum broadband laser source. The devices have different amounts of fabrication bias, and so will have different feature width error of their gratings.

Figure 4.14 shows the transmission peak wavelengths as a function of the width error, which is the actual width difference between the physical device gratings and the desired optimal design. The width error for measured devices is calculated as (error) = (bias) + (assumed fabrication error). This is so that, for example, a device that is biased by -19 nm for which the fabrication error is +19 nm will result in a device with 0 nm width error from the design width. We have plotted the measured data for an assumed fabrication error of both 0 nm, based on the discussion above, and +19 nm based on the SEM measurements (Section 4.1). The figure data suggests that the actual fabrication error present for these devices is between 0 nm and 10 nm. It is still unclear what the insertion angle error is for the measurements, and there are other factors which may affect the trend such as the sidewall angle and device layer thickness variation, which have not been explored in this work.

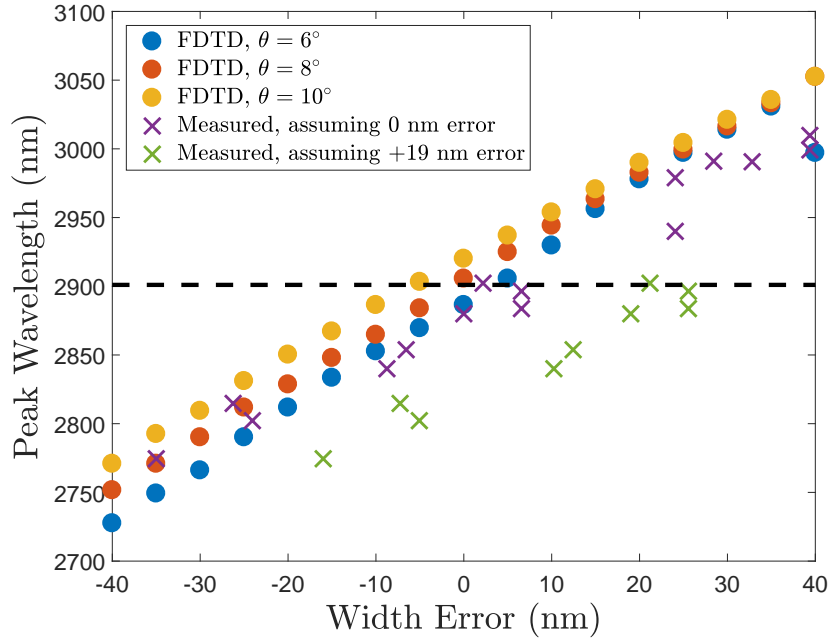


Figure 4.14: The wavelength of the transmission peaks for simulated and measured grating couplers is shown as functions of the width error. Simulated data is plotted with various values of the insertion angle, θ .

Chapter 5

Conclusion

This work has demonstrated the measurement of silicon photonic waveguide loss as a function of waveguide width in the mid-IR range near 2680 nm, near a significant OH-group absorption band in silica. Measurement used basic strip waveguide switchbacks and sub-wavelength grating couplers, which were developed for this wavelength range. The approach is suitable for integration with an automated measurement apparatus. In addition to the measurement of loss, grating couplers that operate at 2.9 μm were achieved for use with the promising Se^+ donor qubit platform. The approximate feature width error for fabrication on the 500 nm, 3 μm BOX substrate is now better known and will allow for grating couplers to be designed and fabricated at their target wavelength with higher accuracy.

For the waveguide loss study, it is clear that increasing the number of copies of each device (beyond only 2) would provide better statistics for determining the loss per unit length for a particular waveguide width, and further mitigate any lack in device yield. This could lead to more accurate width vs loss data and a better fit to the models. Second, a denser list of waveguide widths (specifically between 0.7 and 0.8 micron) would also improve the results. Furthermore, extending the the waveguide widths used to smaller than 0.6 micron may reveal more of the scattering loss model behaviour.

Due to the strong presence of structure in the spectra taken of the devices using the experimental set-up described in Section 3.4, the results of this work also motivated a new measurement scheme using an FTIR spectrometer and broadband source, described in Section 4.5. This method of measurement was able to eliminate absorption due to optical path in air, as well as provide high resolution spectra of the device transmission. These techniques will be directly applicable to the development of the Se^+ donor qubit platform proposed at SFU.

Future directions to take this work include another waveguide loss study at 2.9 μm using the improved measurement apparatus and parameters described above, and using our successful design for couplers at 2.9 μm . In addition, we are now equipped with the necessary input/output and routing devices to begin to investigate designs of photonic crystal cavities, on the SOI platform and for 2.9 μm .

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