

Design and Fabrication of High-Performance Capacitive Micro Accelerometers

by

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Abstract

This thesis presents the development of capacitive high-performance accelerometers for sonar wave detection. The devices are intended to replace the existing sensors based on hydrophones in towed array sonar systems. Two different designs of in-plane and out-of-plane accelerometers are developed, micro-fabricated, and experimentally tested.

The out-of-plane accelerometer is designed based on a continuous membrane suspension element. In comparison to beam-type suspension elements, the new design provides uniform displacement of the proof mass, lower cross-axis sensitivity, and lower stress concentration in suspension elements which could result in higher yield in the fabrication process. The out-of-plane accelerometer is fabricated using a novel microfabrication method which facilitates developing continuous membrane type suspension elements and full wafer thick proof mass for accelerometers. The designed accelerometer is fabricated on a silicon-on-insulator wafer with an 8 μm device layer, 1.5 μm buried-oxide layer, and 500 μm handle wafer. The developed accelerometer is proven to have resonance frequency of 5.2 kHz, sensitivity of ~ 0.9 pF/g, mechanical noise equivalent acceleration of less than 450 $\text{ng}/\sqrt{\text{Hz}}$, and an open loop dynamic range of higher than 130 dB while operating at atmospheric pressure.

The in-plane single-axis accelerometer is designed based on a proposed mode-tuned modified structure. In this modified structure, the proof mass is substituted with a moving frame which also provides the area for increasing the number of sensing electrodes. This substitution contributes to widening the bandwidth of the accelerometer by locating the anchors and elastic elements both inside and outside of the moving frame. The designed accelerometer is fabricated on a silicon-on-insulator wafer with a 100 μm device layer and high aspect ratio capacitive gaps of ~ 2 μm . The sensitivity of the accelerometer is measured as ~ 0.7 pF/g with the total noise equivalent acceleration of less than 500 $\text{ng}/\sqrt{\text{Hz}}$ in the flat band region of the bandwidth. The resonance frequency of the devices is 4.2 kHz while maintaining a linearity of better than 0.7%. The open loop dynamic range of the accelerometer, while operating at atmospheric pressure, is higher than 135 dB, and the cross-axis sensitivity is less than -30 dB.

Keywords: Accelerometer; MEMS; Low-Noise; Wide-Bandwidth; High-Performance;

To my beloved

MOM and DAD

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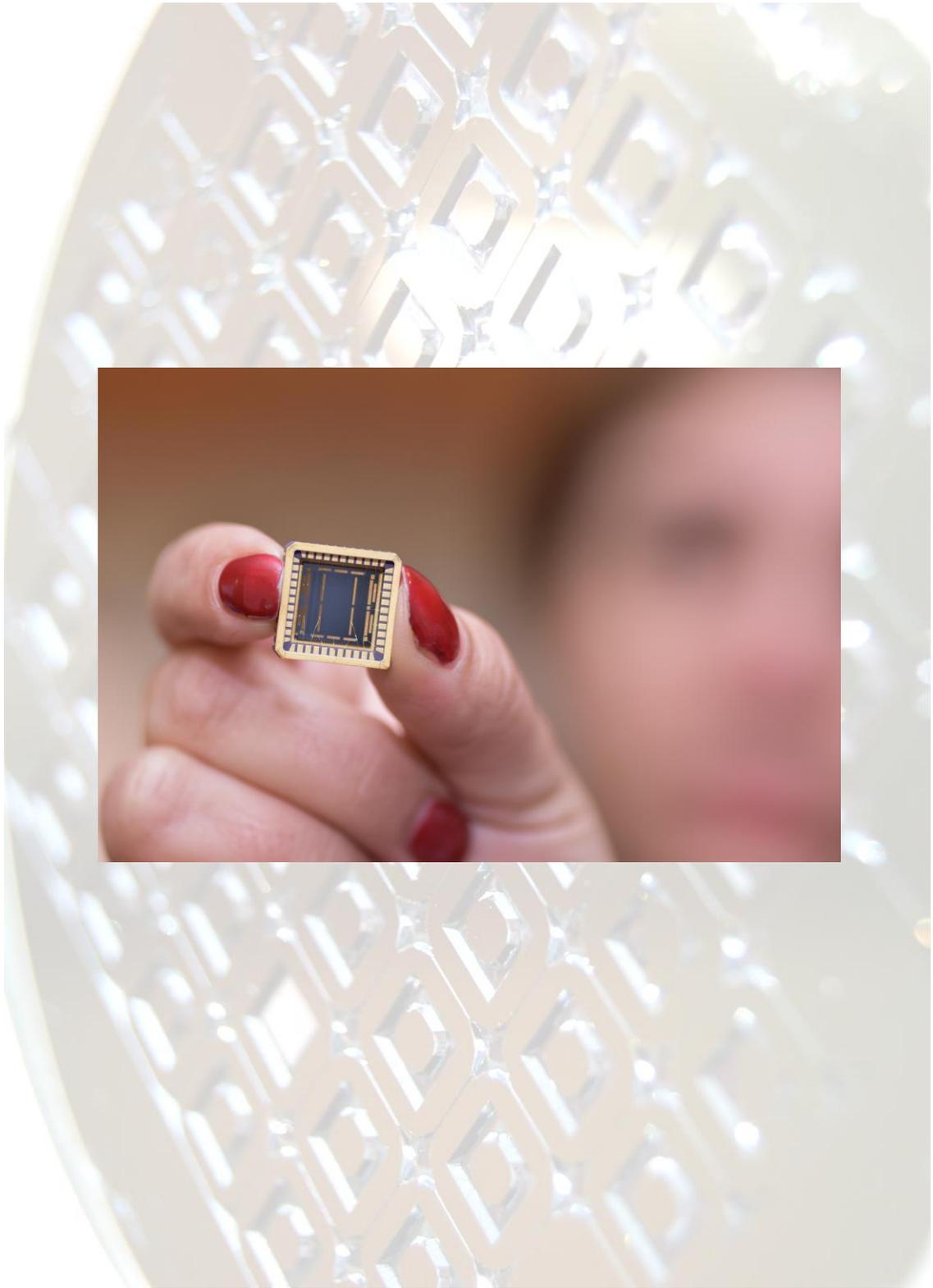
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List of Acronyms

AC	Alternative Current
CLP	Chip Level Packaging
CPP	Circular Proof mass Process
DC	Direct Current
DRIE	Deep Reactive Ion Etching
IA	In-Plane Accelerometer
MEMS	Micro-Electro-Mechanical Systems
MTSP	Mode Tuning Structural Platform
OA	Out-of-Plane Accelerometer
PECVD	Pressure-Enhanced Chemical Vapor Deposition
PT	Prototype
RIE	Reactive Ion Etching
SCNMT	Spectral Coherence Noise Measurement Technique
SEM	Scanning Electron Microscope
SFU	Simon Fraser University
SOI	Silicon on insulator
SPP	Square Proof mass Process
TDoA	Time Difference of Arrival
TMAH	Tetra Methyl Ammonium Hydroxide
TNEA	Total Noise Equivalent Acceleration
VHF	Vapor Hydrofluoric Acid
WLP	Wafer Level Packaging



Chapter 1. Introduction

1.1. Research Motivation

The term 'sonar' refers to the methods and equipment for detecting, locating, and determining the nature of underwater objects using acoustic waves [1]. Sonar wave detection is exploited in several applications. These applications include seabed mappings, oil and gas explorations, pipeline inspections, marine life studies, underwater threat detection, and search-and-rescue missions. Sonar Systems can be categorized under passive and active systems [2]. Passive sonar systems silently listen to the acoustic signals generated by various sources in the environment, while active sonar systems, emit acoustic signals and then listen for echoes in addition to the potential signals generated by the objects.

The principal measurement devices used for underwater acoustic wave detection are hydrophones. Hydrophones are omnidirectional transducers which measure the local strength of an incoming acoustic pressure wave reflected by or emitted from a distant object or surface [3]. Hydrophones are arranged in a linear array with known regular intervals inside an elastomeric hose in order to determine the location of the incoming acoustic waves. In some mobile applications, the hydrophone array is towed behind a ship or submarine. Such a system, which is shown in Figure 1.1, is known as towed array sonar system. The towed array arrangement causes the sound waves arriving from a distant source to reach each hydrophone at a slightly different time. Therefore, by using the Time Difference of Arrival (TDoA) method, the location of the sound can be estimated [4].

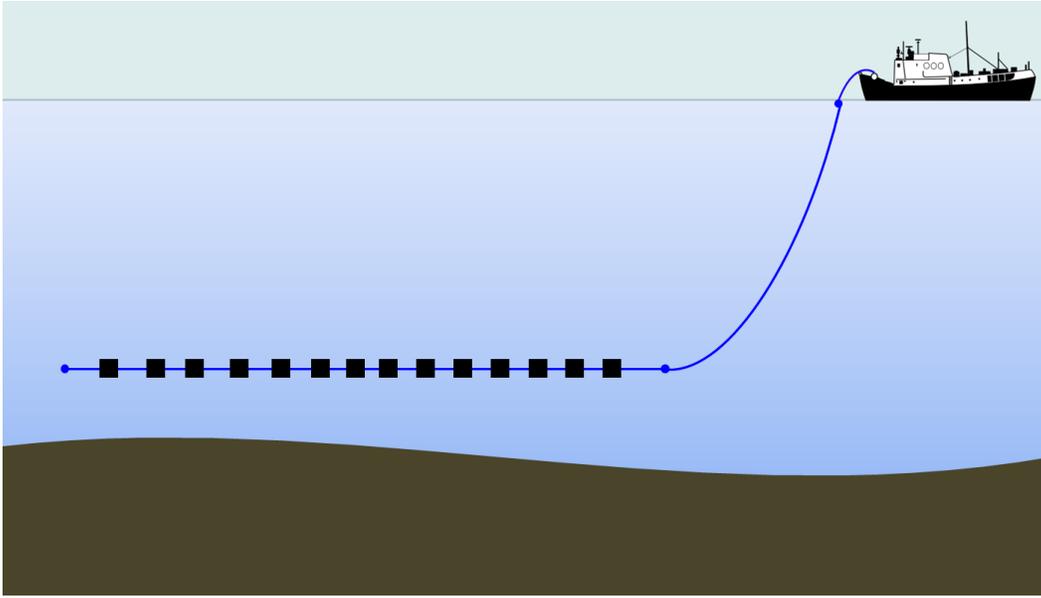


Figure 1.1 – Schematic of a towed array sonar system

The issue with a linear array of hydrophones is the left-right ambiguity in the recognition of the sound source location due to the inverse trigonometric function operation. In other words, there are two valid solutions for the location of the sonar source, one on the left side of the array and its mirror on the right side. In order to resolve this ambiguity issue in linear arrays, every single hydrophone at each node is replaced with an array of four hydrophones. So that, the direction of the signal is determined through time difference between hydrophone signals. Consequently, the diameter of the array should be large enough that the time differences in the output signals between the hydrophones in a single node become measurable to resolve the ambiguity issue [5]. The placement of multiple hydrophones at each node imposes limitations on the minimum diameter of the array. A typical towed array hose is about 10cm in diameter, several hundred meters in length with 200 to 300 sensing nodes, and filled with a liquid to make it neutrally buoyant in the water. Therefore, it can weigh more than a ton [6].

The towed array system is stored in a drum on the ship's surface and is deployed behind the vessel whenever required. However, the limitation on the minimum achievable radius of the towed array cable places stringent requirements on the power, size, and speed of the winch used to deploy or retrieve the array. Consequently, a major portion of the final cost of the towed array systems, typically more than 70%, is spent on winches that can meet such requirements. Moreover, the size and power requirements

for such winches are only met by large vessels which subsequently limits the applicability of towed array sonar systems on small ships. It is desirable to decrease the final cost of the towed array systems, enable their usage on smaller ships, and consequently serve new markets such as smuggling detection by coast guards. Therefore, it is required to significantly reduce the diameter of the hydrophone arrays.

An alternative method for detecting acoustic waves is to utilize neutrally buoyant particle acceleration sensors, i.e., accelerometers. A neutrally buoyant object that is small compared to the acoustic wavelength has similar acceleration characteristics to the acoustic wave [8]. According to Newton's second law applied to the fluid particles, the pressure gradient in a fluid is proportional to the acceleration of the fluid's particles [5]. Therefore, a single 2-axis particle acceleration sensor or two stacked single-axis accelerometers can substitute the quad hydrophone module at each node. Upon this substitution, the diameter of the carrier hose in the towed array could be decreased down to the diameter of a single micromachined accelerometer which is less than an inch.

However, the detection of sonar waves places rather challenging requirements on the performance of the required accelerometers. The noise floor of the accelerometer should be less than $0.5 \mu\text{g}/\sqrt{\text{Hz}}$ to be able to operate down to the quiet ocean ambient levels, where g is the gravitational acceleration [9]. The dynamic range of the accelerometer should be more than 130 dB (within a 1 Hz bandwidth) to enable it to listen to weak echoes while the ship transmitter is operating. Moreover, the accelerometer needs to cover a fairly wide frequency range, typically between 50Hz and 4 kHz plus DC. The combination of these requirements presents a multitude of challenges and trade-offs for the design of accelerometers usable in sonar applications. Although several high-performance accelerometers have been developed for various applications over the past few decades, the majority of them trade noise performance with bandwidth [10]–[12]. To the author's best knowledge, no accelerometer that could meet all of these requirements in a single device is designed, fabricated, and characterized so far.

1.2. Research Objectives

The current Ph.D. thesis aimed to accomplish the design, fabrication, and characterization of MEMS accelerometers with a combination of unprecedented performance characteristics including:

- Diameter of less than 25 mm.
- Cross-axis sensitivity of less than -30 dB
- noise floor of less than $0.5 \mu\text{g}/\sqrt{\text{Hz}}$;
- dynamic range of 130 dB;
- working frequency bandwidth of 50 Hz to 4 kHz plus DC;

The design of the accelerometer consists of three parts: 1) Design of the micro-mechanical structure, 2) development of microfabrication process, and 3) design and development of the associated interface electronics. The major focus in this thesis was on the micromechanical design and micro-fabrication of the MEMS accelerometer. Meanwhile, the interface electronic design and manufacturing were performed by other researchers at the Intelligent Sensors Laboratory in parallel to this project. Since the characteristics of the mechanical structure and the electronic interface affected the final performance of the accelerometer system, both research parties effectively communicated about the requirements over the course of this project. Finally, the designed electronics interface was used to characterize the accelerometer MEMS device in this thesis. The following steps were taken in this project:

- Acquiring fundamental understanding of MEMS accelerometers
- Choosing transduction techniques to meet the requirements of the project
- Developing proper mechanical designs to meet the requirements of size, noise, bandwidth, and dynamic range
- Manufacturing of the devices using microfabrication techniques
- Characterization of the devices

1.3. Thesis Organization

This thesis is divided into six chapters.

Chapter 1 describes the motivation of the thesis by introducing towed array sonar systems and discussing the need for replacing hydrophones with high-performance accelerometers. At the end of chapter 1, the objectives of this thesis work are also explained.

Chapter 2 provides an overview of accelerometer working principles. Subsequently, the common transduction methods for MEMS accelerometers are introduced and a survey of the literature on high-performance accelerometers is presented. Chapter 2 is finalized by proposing two accelerometer designs including in-plane and out-of-plane accelerometers.

Chapter 3 presents a thorough study on the design process of accelerometers. In the first section of chapter 3, the design objectives are explained and rationalized regarding the specific application of accelerometers. In the next section of chapter 3, a few diagrams are used to correlate the performance requirements to the physical characteristics of devices based on the governing equations in capacitive accelerometers. Finally, in the last section of chapter 3, the design procedure and the final proposed designs for the out-of-plane and in-plane accelerometers are presented.

Chapter 4 is dedicated to the micro-fabrication process development for materializing the designed accelerometers. In chapter 4, the developed fabrication process for out-of-plane and in-plane accelerometers are elaborated, and the associated problems during the course of the micro-fabrication process as well as relevant solutions are discussed.

Chapter 5 presents the accelerometer characterization results. In chapter 5, the experimental setups, test procedure, and experimental results of the developed accelerometers are discussed. The experimental results are compared with the simulation studies and any discrepancies are argued.

Chapter 6 concludes the thesis by identifying the achievements, contributions, and novelties of this research work. Furthermore, possible improvements on this project as well as recommended future work is explained.

Chapter 2. Literature Survey

Microelectromechanical inertial sensors are among the most widely-used devices in consumer electronics, automotive, and industrial applications. The first batch-fabricated MEMS accelerometer was reported back in 1979 [13]. Micro accelerometers are still among the top five MEMS devices by sales volume [14].

MEMS accelerometers are used in a wide variety of applications ranging from mobile devices to automotive industry. Many more new applications such as structural health monitoring, geophysical surveys, inertial navigation, seismic imaging, acoustic pressure sensing, etc., are also emerging. Such new applications are more demanding in the context of noise floor, dynamic range, and bandwidth. According to the available market studies, the high-performance MEMS accelerometer market is rapidly expanding and can open up new opportunities for technology developers [15].

In this chapter, an overview of the working principles of an accelerometer is presented. Furthermore, various kinds of transduction methods in accelerometers are elaborated and the advantages and disadvantages of each method are summarized in a table. Finally, a review on high performance accelerometers as reported in the literature is presented and their performance based on noise floor and bandwidth is visualized through a graph.

2.1. Working Principle

An accelerometer is a sensor that measures the physical acceleration experienced by an object due to the inertial forces. The operating principle of an accelerometer can be explained by a simple mass (m) attached to a spring of stiffness (k) and a damper with damping factor (c), as illustrated in Figure 2.1. The mass used in accelerometers is often called the seismic-mass or proof-mass.

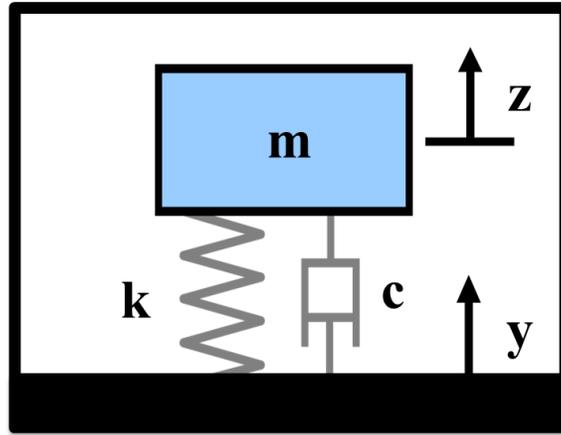


Figure 2.1- Conceptual Schematic of an Accelerometer

As indicated in Figure 2.1, z is the absolute motion of the proof mass and y is the absolute motion of the structure on which the accelerometer is mounted. Writing a balance of forces on the proof mass (m) yields[16]:

$$m\ddot{z} = -c(\dot{z} - \dot{y}) - k(z - y) \quad (2.1)$$

If the motion of the proof mass relative to the base is denoted by $x(t)$, which is equal to $z(t)-y(t)$, then equation (2.1) can be written in terms of the relative displacement as:

$$m\ddot{x} + c\dot{x} + kx(t) = -m\ddot{y} = ma(t) \quad (2.2)$$

Using the Laplace transform and considering the natural frequency as " $\omega_0 = \sqrt{\frac{k}{m}}$ ", the damping ratio as " $\zeta = \frac{c}{2\sqrt{km}}$ ", and the quality factor as " $Q = \frac{\sqrt{km}}{c}$ ", the mechanical transfer function from the Laplace transform of the output (proof-mass displacement) to the Laplace transform of the input (acceleration) can be obtained as:

$$H(s) = \frac{X(s)}{A(s)} = \frac{m}{ms^2 + cs + k} = \frac{1}{s^2 + 2\zeta\omega_0s + \omega_0^2} = \frac{1}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (2.3)$$

Under steady-state conditions, the displacement of the proof mass (x) is given by:

$$x = \frac{F}{k} = \frac{ma_{in}}{k} = \frac{a_{in}}{\omega_0^2} \quad (2.4)$$

where a_{in} is the applied acceleration along the sense axis. As evident from equation (2.4), low-frequency proof-mass displacements are quadratically proportional to the inverse of the resonance frequency. In accelerometers, the resonance frequency is typically the upper limit for the operating frequency band of the system. If DC to fundamental resonance frequency is considered as the operating bandwidth of the sensor, equation (2.4) implies that having a wide bandwidth causes small proof-mass displacements due to the input accelerations.

Assuming a voltage output, the sensitivity is defined as the rate of change of the output voltage (V_{out}) to the input acceleration signal (a_{in}). Considering equation (2.4) for an accelerometer, the sensitivity is given by [17]:

$$S_{a_{in}}^{V_{out}} = \frac{\partial V_{out}}{\partial a_{in}} = \frac{\partial V_{out}}{\partial x} \cdot \frac{\partial x}{\partial a_{in}} = \frac{\partial V_{out}}{\partial x} \cdot \frac{1}{\omega_0^2} \quad (2.5)$$

Equation (2.5) explains why achieving a wide working frequency band along with a high sensitivity in a single device, is one of the main challenges in designing high performance accelerometers. In other words, for a specific fundamental resonance frequency of the structure, which is typically the upper limit of the device's bandwidth, the proof-mass displacement is limited. Therefore, to improve the overall sensitivity of the device, the only way is to improve the rate of voltage change per unit displacement of the proof-mass. This, however, will bring up significant challenges on the interface circuit design where typically noise and gain of the circuit are related.

Another significant aspect in designing high performance accelerometers is achieving low noise floors. The noise floor is the total noise generated at the sensor output in the absence of real signal (i.e. acceleration). The noise sources can be categorized into mechanical and electrical.

The main source of mechanical noise in accelerometers is due to the Brownian motion of the gas molecules surrounding the mechanical structure. The mechanical noise leads to random fluctuations in the energy transfer between the structures and the damping gas. This phenomenon is based on the Fluctuation-Dissipation theorem [18]. That theorem states that the existence of a dissipation mechanism in a system assures the presence of a component of fluctuation which is directly related to that dissipation. This is due to the fact that any energy dissipating mechanism within the system causes all random motions to be decayed. Hence, there should be an associated fluctuating force in order to bring the system to equilibrium with the environment. In mechanical systems this is called the thermomechanical noise (Brownian noise). In an accelerometer, which can be modeled by a mass-spring-damper system, the energy is dissipated through the damper. The spectral density of the input fluctuating force which compensates the dissipation force can be determined using the Nyquist Relation [18]:

$$F = \sqrt{4k_b T c} \quad \left[\frac{N}{\sqrt{Hz}} \right] \quad (2.6)$$

where k_b is the Boltzman constant in N.m/K, T is the absolute temperature in K, and c is the damping coefficient in N.s/m. Equation (2.6) applies to any mechanical system that can be modeled as a simple mass-spring system.

Using Equation (2.6), the displacement of the mass due to the fluctuating force can be estimated by the following equation:

$$X_n = \frac{\sqrt{4k_b T c}}{k} \quad \text{in } m/\sqrt{Hz} \quad (2.7)$$

Considering the displacement of the proof mass due to the input acceleration as equation (2.4), the signal-to-noise ratio can be calculated as follows:

$$SNR = \frac{X_s}{X_n} = a_{in} \sqrt{\frac{MQ}{4k_b T \omega_0}} \quad (2.8)$$

Equation (2.8) implies that increasing the mass and the quality factor along with decreasing the natural frequency of the system boosts the signal-to-noise ratio.

Electrical noises are dependent to the interface electronics and the sensor's transduction method. They could have different sources such as temperature-induced fluctuations in carrier densities, random production and eradication of electron–hole pairs in semiconductors, variable trapping and release of carriers in any conductors, etc. [19]. During the characterization of the developed sensors' noise sources in Chapter 5, a brief discussion on the electrical noise sources is presented.

Assuming that the mechanical and electrical noise sources are uncorrelated, the total noise equivalent acceleration (TNEA) of the accelerometer system is the square root of the summation of the mechanical noise equivalent acceleration (MNEA) square and electrical noise equivalent acceleration (ENEAE) square [20]:

$$TNEA = \sqrt{MNEA^2 + ENEAE^2} \quad (2.9)$$

where MNEA is calculated from spectral density of the input fluctuating force, equation (2.6) over the mass of the structure.

2.2. Transduction Methods

Accelerometers can be classified based on how the proof mass displacement are sensed. Such techniques include capacitive, piezoresistive, piezoelectric, tunneling, optical, heat transfer, Hall Effect, thermal, and interferometric. In this section, a summary of the most common transduction methods is provided.

2.2.1. Piezoresistive Accelerometers

Piezoresistive effect is a change in the resistivity of a material due to a mechanical strain. The first bulk-micromachined accelerometer was also a piezoresistive one which was developed by Roylance et al. at Stanford university [13]. As shown in Figure 2.2, a piezoresistive accelerometer, in its simplest form, is a proof-mass which is anchored to a substrate using a cantilever beam. In this accelerometer, a piezoresistive element is embedded close to the fixed end of the cantilever. An input acceleration

displaces the proof mass and bends the cantilever beam. The induced strain due to the bending in the cantilever beam changes the resistance of the piezoresistive element. Using a Wheatstone bridge, for instance, the change in the resistance is interpreted as a measure of the input acceleration.

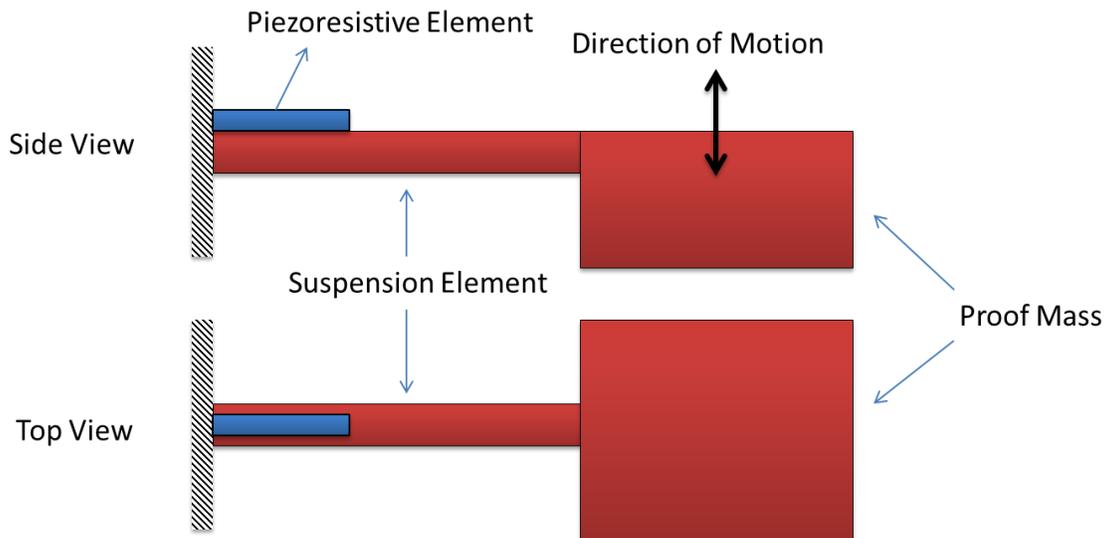


Figure 2.2 - Schematic of a piezoresistive accelerometer, side and top views

The advantage of piezoresistive accelerometers is the simplicity of their structural design and fabrication process. Moreover, because of the resistive bridge that makes a low output-impedance source, piezoresistive accelerometers have simple readout circuitries [21]–[24]. However, the dependence of the piezoresistive coefficient on temperature, sensitivity drift, and thermal noise caused by the resistors limits the applicability of piezoresistive accelerometers in high performance applications.

2.2.2. Piezoelectric Accelerometers

The piezoelectric effect is a property of certain materials in developing electrical charge in response to applied mechanical stress. This effect is reversible, meaning that when a piezoelectric material is subjected to an externally applied electric field, an internal stress is developed within the material [25].

A schematic of a typical accelerometer utilizing the piezoelectric principle is illustrated in Figure 2.3. In this schematic, the piezoelectric material is sandwiched between two conducting layers which are deposited on a suspension beam. As

acceleration is applied, the proof-mass moves, causing the beam to deflect. The created strain induces charge deposition on the surfaces of the piezoelectric material. The deposited charge is a measure of the applied acceleration.

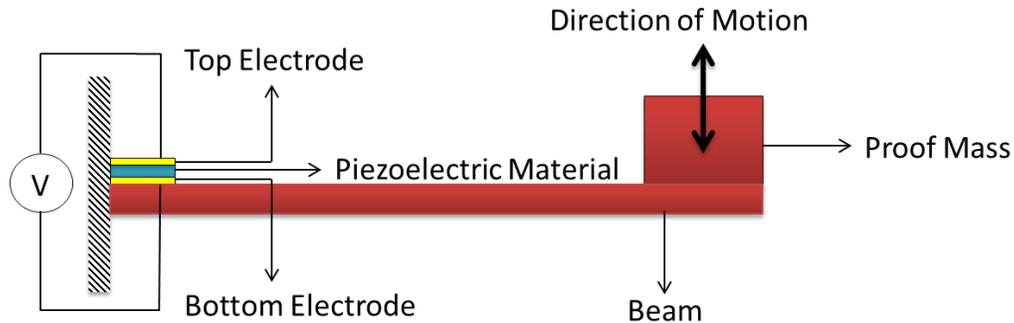


Figure 2.3 - Schematic of a piezoelectric accelerometer structure

Piezoelectric accelerometers have the advantage of high bandwidths, low power consumption, high shock survival, and temperature stability [26]. However, due to the parasitic effects of small DC leakage currents, piezoelectric accelerometers can only be used to sense vibratory motions.

2.2.3. Optical Accelerometers

Optical accelerometers primarily rely on distinguishing the changes in the characteristics of optical waves in response to input accelerations. The characteristics of the electromagnetic wave that can be altered include intensity, phase, wavelength, spatial position, frequency, and polarization [25].

A schematic of an optical accelerometer which uses the intensity modulation is shown in Figure 2.4. This accelerometer constitutes of a proof-mass which is attached to the substrate using suspension elements. The proof mass has a bulge which is located in-between the input optical fibers, the ones in which the light enters, and the output optical fibers, the ones from which the light exits. Based on the amount of the proof-mass displacement, the intensity of the transmitted light changes, providing a measure of the applied acceleration.

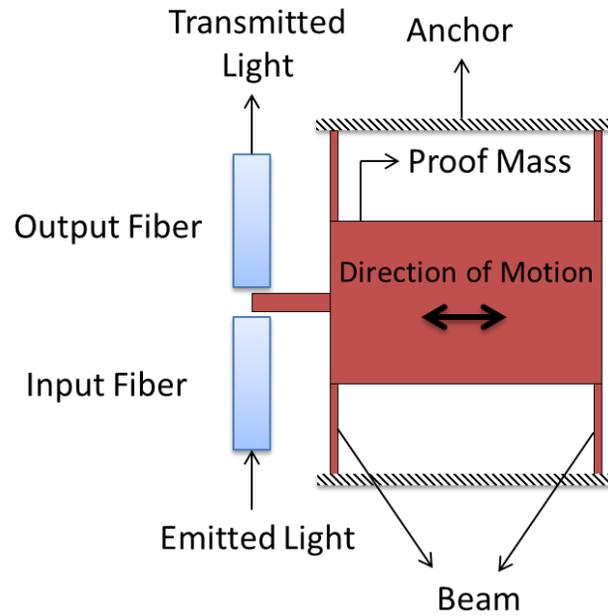


Figure 2.4 - An example of an optical accelerometer

Optical accelerometers have high electromagnetic interference noise immunity with very high sensitivity for the detection of proof mass displacement. Additionally, optical accelerometers can operate in high temperatures [21], [27]. However, the complex fabrication and packaging process as well as the complex detection circuitry are the two major drawbacks of optical accelerometers [28].

2.2.4. Tunneling Accelerometers

Tunneling accelerometers exploit changes in tunneling current between a tip and a counter-electrode attached to the moving structure. A schematic of a tunneling accelerometer is shown in Figure 2.5. When the separation gap between the tip and its counter-electrode is within a few angstroms, a tunneling current is established. As long as the tunneling voltage and the separation gap are constant, the tunneling current does not change. As the proof mass moves due to the applied acceleration, the distance between the tunneling tip and the electrode changes, resulting in tunneling current alteration [21]. Since the tunneling current and the tip-electrode separation have an exponential relationship, a tunneling accelerometer is required to work in closed loop to reduce nonlinearities [29].

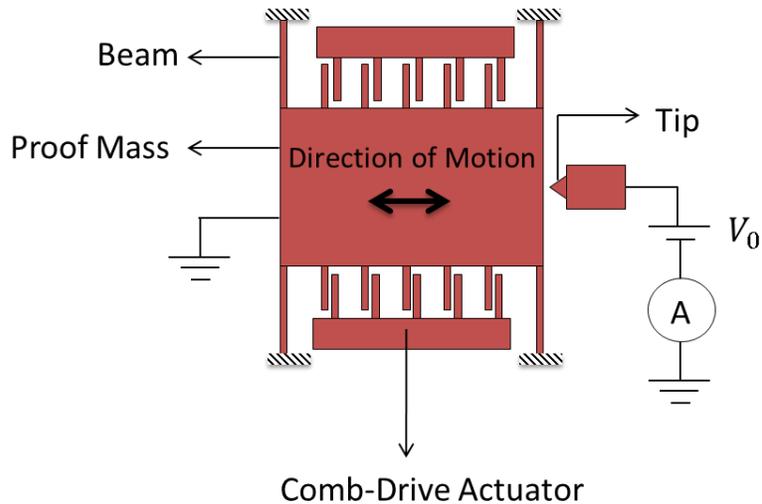


Figure 2.5 - Schematic of a tunneling accelerometer

Due to the fact that the tunneling current is highly sensitive to the variation in tunneling gap, tunneling accelerometers have extremely high sensitivities [21]. However, since the tunneling current changes with temperature, the accelerometer performance exhibits a strong temperature dependence [26]. The main issues with tunneling accelerometers which limits their application include fabrication challenges, maintaining linearity, and the required high supply voltage[21].

2.2.5. Resonant Accelerometers

Resonant accelerometers exploit the shifts in the resonant frequency of a resonator to measure the applied acceleration. Resonant response can be obtained in two ways. The first and the most conventional type of resonant accelerometers is based on mechanical coupling between the proof-mass and a resonator, shown in Figure 2.6. In these types of sensors, the inertial force of the proof mass due to the applied acceleration is transferred to the mechanically-coupled resonator through an axial force. Due to the geometric effects, the developed axial force in the resonator leads to a shift in the natural frequency of the resonator [30].

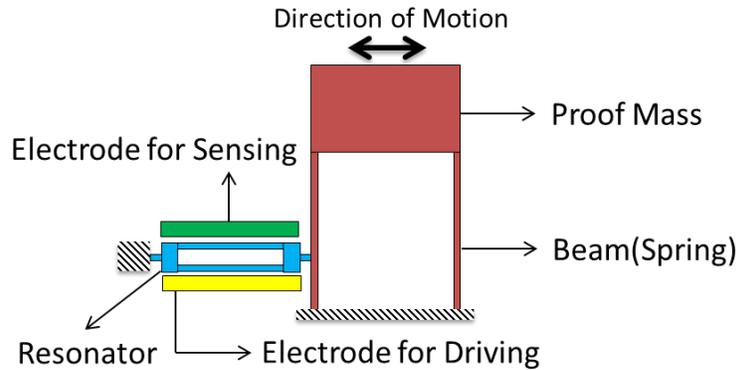


Figure 2.6 - Schematic of a resonant accelerometer

The other group of resonant accelerometers operates based on the electrostatic coupling of the proof-mass and the resonator. In this kind of accelerometers, the proof-mass movements modify the electrostatic gap within the proof-mass. This gap variation causes a change in the electrostatic spring constant of the resonator which results in a change in the resonance frequency of the resonator [31].

The main advantage of resonant sensing is the accuracy and precision of measuring a frequency signal compared to a typical voltage or current signal. The quasi-digital frequency output also simplifies interfacing with digital systems by demodulating the signal using frequency counting techniques. However, this mechanism can only be applied in acceleration signals that slowly vary with time where the frequencies are in the order of several hundred Hertz [32].

2.2.6. Thermal Accelerometers

Thermal accelerometers work based on the disturbance induced to a thermodynamic system due to an applied acceleration. To thermally measure acceleration, one possible technique is to use a heated plate as a proof-mass. As shown in Figure 2.7, the heated plate is placed between two heat sinks located within a small gap within the heated plate. As the proof-mass moves due to an input acceleration, the gap between the proof mass and the heated plates changes. The change in the separation gap leads to the heat flux change between the heater and the heat sinks, which induces temperature alteration between the plates. Using a thermopile, the temperature of the plates as a measure of the applied acceleration is measured [33], [34].

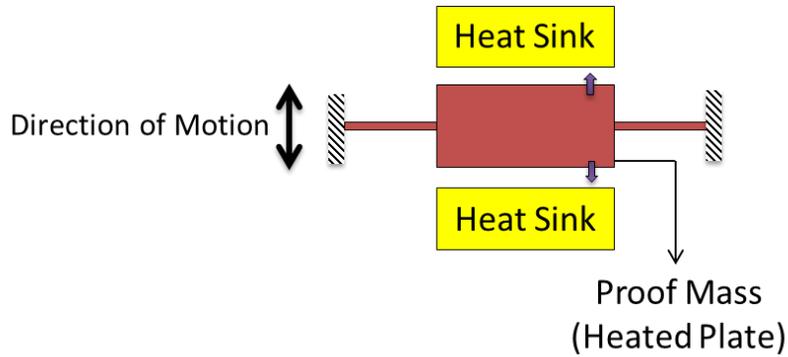


Figure 2.7 - Schematic of a thermal accelerometer based on a moving proof mass

Another technique of thermal acceleration measurement is to measure the acceleration based on the natural convection of fluid in a sealed chamber [35], [36]. A schematic of an accelerometer working based on convection heat transfer is shown in Figure 2.8. The device consists of three resistor strips and a cavity etched in a silicon substrate under the strips in order to provide proper thermal isolation. The middle strip acts as a heater and the side strips are used as temperature sensors. When no acceleration is applied, the heater produces a symmetric temperature distribution and the differential output would be zero. When acceleration is applied, the temperature distribution around the middle strip changes due to convection. The resulting temperature difference is related to the applied acceleration.

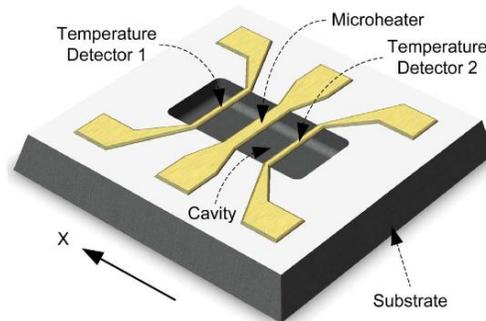


Figure 2.8 - Schematic of a thermal accelerometer without moving structure © 2012 IEEE [36]

The main advantage of convective heat bubble accelerometers is their lack of moving components. However, thermal accelerometers are temperature-dependent due to the nature of their sensing method, and they have low sensitivities; a few millivolts per g [37]. Therefore, they need appropriate packaging. Moreover, the operating bandwidth of thermal accelerometers is less than a few tens of Hertz, which makes them inappropriate for the intended application in this thesis [37].

2.2.7. Capacitive Accelerometers

Capacitive accelerometers use a variable capacitor as the transducer for measuring the proof-mass displacements caused by an input acceleration. The three most common configurations of capacitive sensing methods are based on parallel plate electrodes, transverse comb electrodes, and lateral comb electrodes. The parallel plate capacitor configuration is shown in Figure 2.9. In this configuration, the capacitor is formed between the two parallel plates. In the parallel plate capacitor configuration, the moving electrode is connected to the proof-mass and the fixed electrode is fixed to the substrate. As the proof-mass moves, the gap between the moving and the fixed electrodes changes. Consequently, the capacitance value between the two electrodes varies, providing a measure of the input acceleration. This configuration is generally used to measure out-of-plane accelerations. However, large displacements, i.e., more than a few percentage of the gap, make the transduction nonlinear, limiting the open-loop dynamic range of the accelerometer.

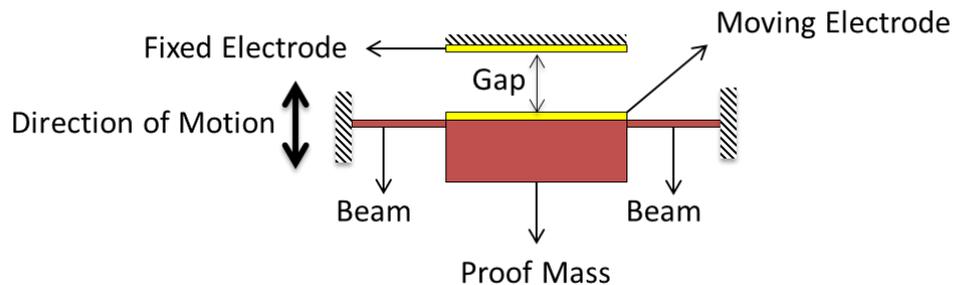


Figure 2.9 -Parallel plate capacitor configuration

Transverse and lateral comb configurations are shown in Figure 2.10, a and b. The transverse comb capacitance configuration is composed of a moving electrode on the proof-mass, which is parallel to a fixed electrode. As the proof-mass displaces, the capacitance value between the two parallel plates changes.

The lateral comb configuration has an almost similar layout to the transverse comb configuration. Their difference is in the proof-mass direction of motion. In the lateral comb configuration, the variation in the capacitance value is due to the change in the effective area between the comb electrodes. As such, this configuration generally has a poor sensitivity relative to the transverse comb configuration. However, the displacement-capacitance relationship is linear.

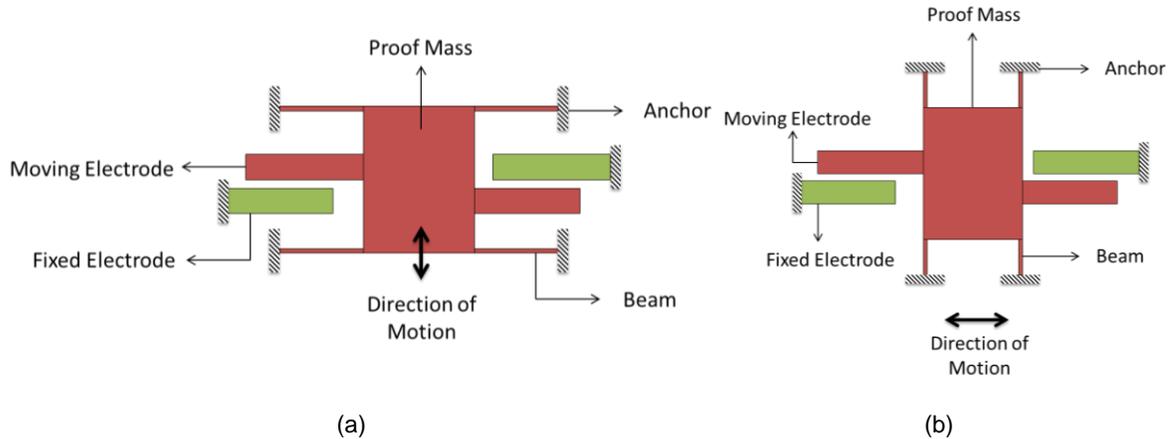


Figure 2.10 – a) Schematic of a transverse comb capacitance configuration, and b) schematic of a lateral comb capacitance configuration

Capacitive accelerometers have a simple structure, low drift, and low temperature sensitivity. Their relatively good noise performance makes the capacitive accelerometers suitable for high performance applications. However, capacitive accelerometers cannot be utilized in strong electromagnetic fields, since their sense nodes have high impedances.

2.2.8. Transduction Methods Summary

Table 2.1 summarizes the typical performance of accelerometers with different transduction mechanisms and interface electronics. The criteria considered in making this table are the ones that influence the applicability of the accelerometer in the defined high performance application. The plus (or negative) sign in each box means that the specific type of accelerometer has (or has not) an acceptable performance under that criterion. The dot sign means the performance is neither very good nor very bad. From Table 2.1, it is concluded that accelerometers with capacitive interfaces are the most promising types for the desired high performance application. Capacitive accelerometers can provide DC response. In addition, they are relatively simple to fabricate and have fairly simple interface electronics. Therefore, capacitive accelerometers were selected for the implementation of accelerometers in this thesis.

Table 2.1 - Comparison of different accelerometers based on their transduction methods

Transduction Method \ Criteria	Optical	Capacitive	Piezoresistive	Piezoelectric	Thermal	Resonant	Tunneling
DC Performance	+	+	+	-	+	+	+
Noise Performance	+	+	●	+	-	+	+
Interface Electronics	-	+	+	+	+	●	●
Open-loop Dynamic Range	+	●	●	+	●	+	●
Fabrication	-	+	+	+	+	+	-
Packaging	-	+	+	+	●	-	-

2.3. Reported High-Performance Accelerometers

Several high-performance accelerometers have been developed for various high-end applications over the past few decades. However, the majority of them traded noise performance with bandwidth [10]–[12].

Levinzon reported an ultra-low noise seismic grade piezoelectric accelerometer with a frequency range of 0.1 to 200 Hz and a noise floor of less than $600 \text{ ng}/\sqrt{\text{Hz}}$ [38]. However, the accelerometer has about 7 inches of diameter and 6 inches of height.

PCB Piezotronics Inc. has commercialized ceramic high performance accelerometers with 3 kHz bandwidth and resonance frequencies of more than 40 kHz. The noise level of these sensors is less than $11 \text{ } \mu\text{g}/\sqrt{\text{Hz}}$ for signals with frequencies of more than 10 Hz [39]. However, such accelerometers cannot be employed for DC measurements.

Vohra et. al. reported a high performance fiber optic accelerometer with less than $1 \text{ } \mu\text{g}/\sqrt{\text{Hz}}$ of noise at 1 kHz as well as a broad frequency response ranging from 100 Hz to 14 kHz [40]. The working principle of the reported accelerometer was based on the path length change of a fiber interferometer integrated into a proof-mass.

Krause et. al. reported an opto-mechanical accelerometer that employs optical displacement read-outs. In this device, acceleration is measured using a planar

photonic-crystal nano-cavity monolithically integrated with a high Q-factor mass-spring system. The noise level and bandwidth of the accelerometer were reported as $10 \mu\text{g}/\sqrt{\text{Hz}}$ and 20 kHz, respectively. However, the dynamic range of the accelerometer is limited to 40 dB [41].

Zandi et al. proposed an optical accelerometer composed of optical fibers and a MEMS structure [42]. In their device, the emitted light from a laser source is transmitted into a multimode SOI channel waveguide through a single mode optical fiber. The light, then, is split into the sensing and reference arms. The emitted light from the sensing arm is compared with the emitted light from the reference arm after hitting a movable Bragg mirror which was attached to the proof-mass. Measuring the output power, the magnitude of the applied acceleration is found. The resonance frequency, noise floor, and dynamic range of the accelerometer were reported as 4 kHz, $111 \mu\text{g}/\sqrt{\text{Hz}}$, and ~ 70 dB, respectively [42].

A wide bandwidth along with a sub- $\mu\text{g}/\sqrt{\text{Hz}}$ noise floor was reported for an opto-mechanical accelerometer developed by Cervantes et al. [43]. This optical accelerometer is a combination of a mechanical fused-silica oscillator and fiber-optic micro-mirror cavities. The noise floor of this device was reported to be $100 \text{ ng}/\sqrt{\text{Hz}}$ for frequencies between 1.5 kHz and 10 kHz. However, similar to the previous optical accelerometers, optical transduction is still not a viable candidate for most applications due to the complex packaging and interface requirements.

Rockstad et al., followed by Liu et al., progressively developed electron tunneling accelerometers aimed at underwater acoustics applications [10], [44]–[46]. The most recent version of such accelerometers operated at a low pressure of 1.3 Pa to achieve a noise level of $20 \text{ ng}/\sqrt{\text{Hz}}$ [46]. The mechanical bandwidth of the system was increased from its resonance frequency of 100 Hz to above 1 kHz using a feedback controller. This device, however, required a complicated manufacturing process and a sophisticated controller for the highly nonlinear tunneling transduction.

Zou et al. reported a seismic grade resonant accelerometer which included a proof mass connected to two double-ended tuning fork resonator sensing elements using a leverage mechanism that amplified the inertial forces [47], [48]. Due to the leveraging mechanism, the scale factor of the device was enhanced to 9408 Hz/g. The

dynamic range of the device was also reported as 130 dB. The measured noise level of the device was $144 \text{ ng}/\sqrt{\text{Hz}}$ over 1 to 50 Hz.

Gannon et al. developed a capacitive analog servo accelerometer [49]. The noise level of the accelerometer was $100 \text{ ng}/\sqrt{\text{Hz}}$ at 200 Hz with a bandwidth and dynamic range of 200 Hz and 115 dB, respectively. The sensor was a 3-terminal capacitive accelerometer which used a parallel plate capacitor configuration. It consisted of four silicon wafers, where the 2 centre wafers were fusion-bonded to form the 2-wafer-thick proof-mass and centre electrode. The outer two wafers acted as top and bottom electrodes which were bonded to the middle mass support frame using metal thermo-compression bonding. Some lower-performance versions of the reported accelerometer were commercialized and later sold by Colibrys [50].

Walmsley et al. developed a two-axis in-plane capacitive MEMS accelerometer using the surface electrode technology [51]–[53]. The accelerometer was fabricated from three silicon wafers including the cap wafer, rotor wafer, and stator wafer. These three wafers were bonded together and singulated into a small vacuum encapsulated die. The proof-mass and elastic elements were etched through the rotor wafer, and the variable capacitor was formed between the MEMS wafer and the stator wafer surface electrodes. Due to the applied acceleration, the proof mass displaced laterally and the overlapped area of the surface electrodes changed. Therefore, the capacitance value between the electrodes changed. The noise level of the accelerometer was measured to be $10 \text{ ng}/\sqrt{\text{Hz}}$ at a full bandwidth of 200 Hz with a dynamic range of 120 dB.

Laine et al. developed a capacitive low-noise accelerometer with an 800 Hz closed-loop bandwidth [54]. The accelerometer had a reported noise level of $10 \text{ ng}/\sqrt{\text{Hz}}$ at 70 Hz with a dynamic range of 130 dB. The sensor, which used a transverse comb capacitance configuration, was commercialized as part of a land seismic acquisition system [55].

2.4. Summary

Figure 2.11 compares the high-performance accelerometers reported in the literature in terms of the noise and resonance frequency of their mechanical structure specifications.

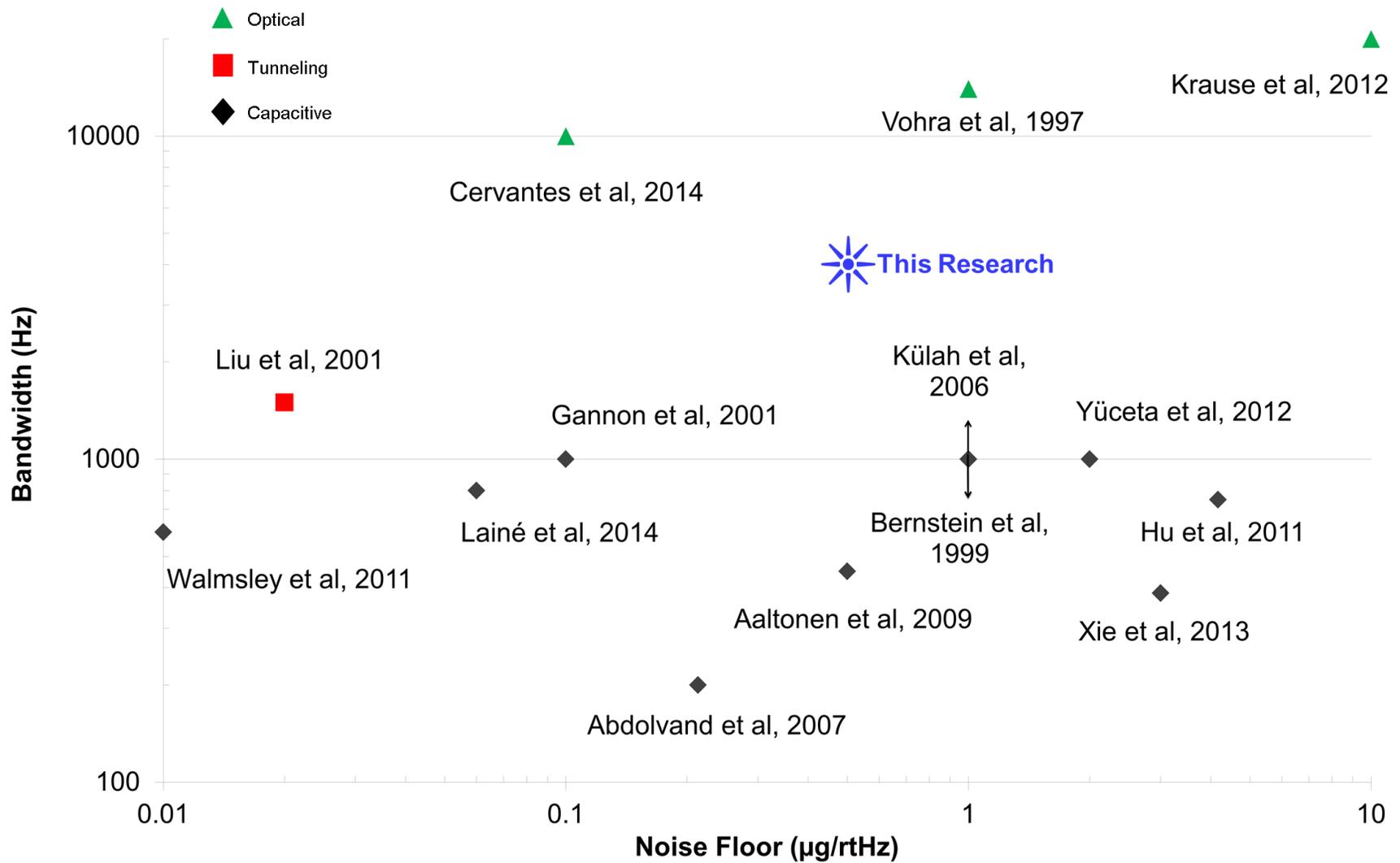


Figure 2.11 - Comparison of micro-accelerometers based on reported performance of bandwidth and noise floor [11], [20], [40], [41], [43], [46], [52], [54], [56]–[61]

As evident from Figure 2.11, despite the ongoing interest and efforts in this field, there is yet no high-performance accelerometer that can meet all the requirements for sonar wave detection, except optical accelerometers. As mentioned before, due to the stringent requirements on packaging, optical accelerometers are not viable candidates for sonar wave detection. This thesis is a study to fill the gap for a single-axis capacitive accelerometer with sub- μg noise floor, wide bandwidth, and high dynamic range for sonar wave detection. However, since all of these requirements are correlated to each other, meeting all of them in a single device is a real challenge. Figure 2.12 shows these correlations through a graph. The main limiting factor in the accelerometer is the size of the device. The MEMS device size limits the maximum achievable mass. Yet, mechanical noise of the device is related to the mass value. Furthermore, the bandwidth of the device has a lower limit which is identified by the required performance of the project. On the other side, bandwidth limits the sensitivity of the device, which mainly affects the electrical noise level of the system. In addition to all of these limitations and couplings between the requirements, the microfabrication also put strict limitation on the achievable features. In the following chapters, it is tried to address all of these issues by suggesting the optimized designs and microfabrication methods.

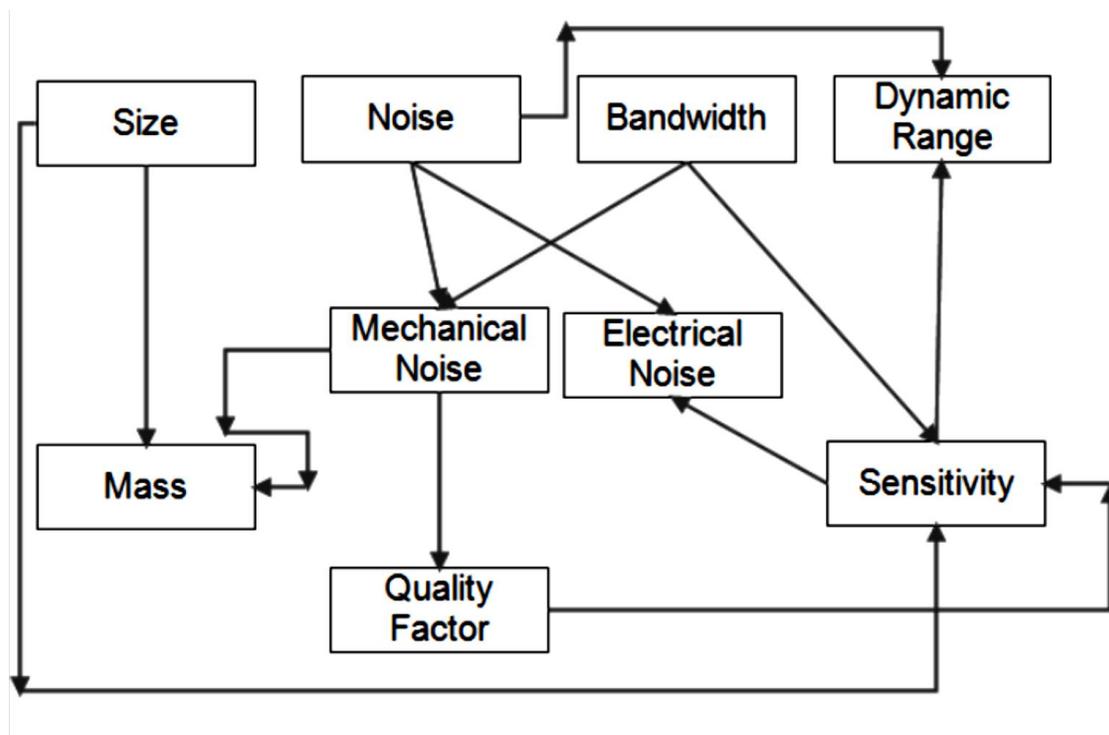


Figure 2.12 – Correlation of the high performance accelerometer design factors

Chapter 3. Device Design

Considering the various capacitive accelerometers reviewed in the previous sections, and after preliminary calculations, parallel plate and transverse comb configuration were selected as the two configurations which could meet the requirements of this project. However, there are some limitations associated with each of these configurations.

The parallel plate and transverse comb configurations lead to out-of-plane and in-plane accelerometers, respectively. In this Chapter, in the first section, the design objectives and the rationale for the objectives would be explained. Following that in Design Specifications section, by reviewing the metrics in capacitive accelerometers, the performance requirements of the accelerometer is correlated to the device characteristics. Finally, in the last section, the design procedure and final designs for the out-of-plane and in-plane accelerometers are elaborated.

3.1. Design Objectives

The design objectives for the capacitive accelerometer are defined based on the sonar wave detection application that was explained in Chapter 1. The objectives include the size of less than 1 inch, noise floor of less than $0.5\mu\text{g}/\sqrt{\text{Hz}}$, dynamic range of more than 130 dB, and working frequency band of 50 Hz to 4 kHz. In this section, the rationale for each of the requirements is elaborated.

The main requirement for this project is on the size of the sensors which return to the main motivation of this research work. The diameter of the accelerometers should be less than an inch to reduce the diameter of the carrier hose in the towed array systems.

Furthermore, the accelerometer noise floor should be less than the ambient acoustic noise in the ocean to be able to pick up the signals. Ambient noise levels in the ocean depend on the sea state. Sea state is a simple scale which can be used to give the general condition of the sea. Depending on the height of the waves, sea states goes from 0 to 9, where 0 is for a calm sea and 9 is for a sea with waves up to 14 meters. Wenz curves are a group of curves which shows the measured average ambient noise

spectra for different sea states and shipping traffic [9]. Figure 3.1 shows a simplified Wenz curve. According to sea state 1 line in Figure 3.1, the minimum amplitude of the pressure spectral density at 5 kHz is equivalent to 43.1 dB re 1 μ Pa.

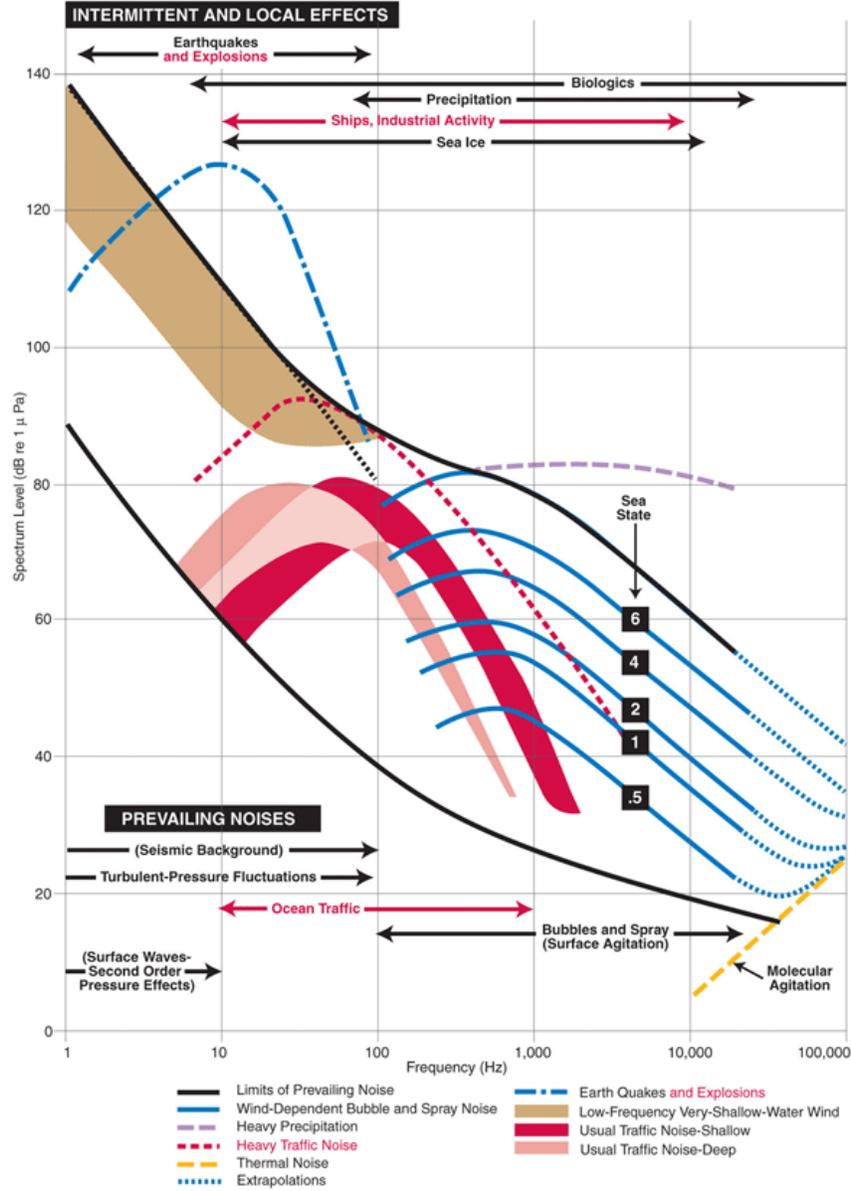


Figure 3.1 - The curves representing deep-water ambient-noise spectra [62]

Using equation (3.1), the RMS of the acoustic pressure is calculated:

$$Pressure\ Level(dB\ re\ 1\ \mu Pa) = 20\log\ \frac{P}{1 \times 10^{-6}} \rightarrow P = 1.43 \times 10^{-4}\ Pa \quad (3.1)$$

Acoustic pressure (P) is related to acoustic particle velocity (\vec{v}) through:

$$\vec{v} = \frac{p}{Z_0} \vec{n} \quad (3.2)$$

where \vec{n} is the vector indicating propagation direction and Z_0 is the characteristic acoustic impedance of the medium which is found from:

$$Z_0 = \rho c \quad (3.3)$$

where ρ is density of water, and c is sound velocity in the water. Acoustic particle acceleration can be calculated by derivation from the acoustic particle velocity:

$$\vec{a} = j\omega \vec{v} \quad (3.4)$$

Considering $\rho = 1030 \text{ kg/m}^3$ and $c = 1470 \text{ m/s}$, the characteristic acoustic impedance of the water would be $Z_0 = 1.5 \text{ MRayl}$. Therefore, the RMS value of the acoustic particle acceleration for sea state 1 at 5000 Hz would be $0.3 \text{ } \mu\text{g}$. As a result, by having an accelerometer with the noise floor of less than $0.5 \text{ } \mu\text{g}/\sqrt{\text{Hz}}$, the signals with magnitude of between the ambient noise level of sea state 1 and 2 would be detectable.

Another requirement of the accelerometer is dynamic range of better than 135 dB within 1 Hz bandwidth. This requirement implies that the accelerometer should be able to pickup the range of $0.5 \text{ } \mu\text{g}$ to 3 g signals linearly. Towed array transmitter emits signals with 3g amplitude in the active mode of operation.

The working frequency band of the devices should be DC plus 50 Hz to 4 kHz. DC signal detection capability of the accelerometers is for orientation identification. In other words, the accelerometer should be able to detect the gravity to identify its orientation. In addition, the range of 4 kHz bandwidth for detection is due to the sonar transmitter working frequency range.

3.2. Design specification

In this section, the performance requirements of the accelerometer are correlated to the device characteristics through the metrics in capacitive accelerometer design.

The fundamental resonance frequency for an accelerometer along the sense axis is given by:

$$\omega_0 = \sqrt{\frac{K_{eff}}{M_{eff}}} \quad (3.5)$$

where K_{eff} and M_{eff} are the effective stiffness and mass of the mechanical structure, respectively. Regarding equation (3.5) with a fixed value for resonance frequency, stiffness is linearly proportional to mass of the moving structure with the coefficient of ω_0^2 . The displacement of the proof mass at frequencies far below the resonance frequency or in the static situation is given by:

$$y_{static} = \frac{M_{eff} a_{in}}{K_{eff}} = \frac{a_{in}}{\omega_0^2} \quad (3.6)$$

where a_{in} is the applied acceleration along the sense axis. Figure 3.2 shows the value of static displacement of the proof mass relative to resonance frequency of the accelerometer in response to $1 \mu g$ input acceleration. As it is evident from Figure 3.2 due to the inverse quadratic relation of displacement and resonance frequency, displacement of the proof mass is reduced drastically as the bandwidth increases. For a mechanical system with resonance frequency of 5 kHz, displacement is about 10 femto-meters.

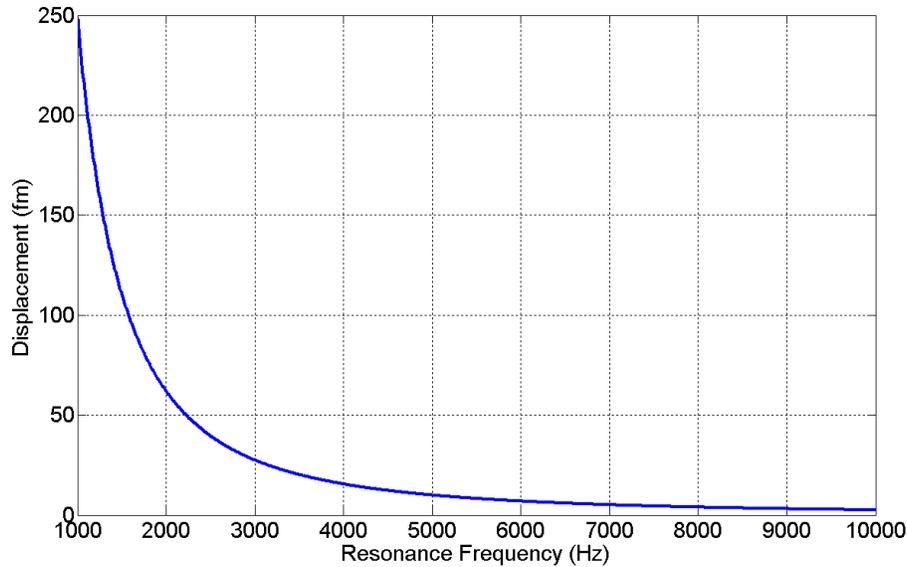


Figure 3.2 - Quasi-static displacement of a proof mass in a 1DOF mass-spring-damper system versus various resonance frequencies in response to $1 \mu g$ acceleration

Another fundamental metrics in designing high-performance accelerometers is the total noise equivalent acceleration (TNEA) of the accelerometer, which is the summation of mechanical noise equivalent (MNEA) and electrical noise equivalent (ENEAE):

$$TNEA = \sqrt{MNEA^2 + ENEA^2} \quad (3.7)$$

Mechanical noise equivalent acceleration is given by (in $m/s^2/\sqrt{Hz}$):

$$MNEA = \sqrt{\frac{4k_B T \omega_0}{Q M_{eff}}} \quad (3.8)$$

where k_B is Boltzmann constant and T is the working temperature. As it is evident from equation (3.8) the MNEA can be practically reduced by increasing mass of the moving structure (M_{eff}) or increasing the quality factor (Q). Increasing mass of the moving structure requires thicker wafer and/or larger surface area. On the other hand, increasing quality factor needs minimizing energy dissipation in the accelerometer system. Various dissipation mechanisms such as air damping, anchor loss, thermo-elastic damping, intrinsic material damping and surface damping contribute to energy losses in MEMS devices [63]. Each mechanism can individually limit the Q-value of the structure. However, air damping and anchor losses are known to be the dominant loss mechanisms that limit quality factor for MEMS accelerometers. Anchor losses can be reduced by proper design of support and anchor structures of the MEMS devices. Besides, air damping can be reduced by operating the accelerometer under the vacuum. Figure 3.3 shows the relationship between noise level and mass of an accelerometer with 5 kHz resonance frequency within different quality factors. According to this figure, for a system with Q-factor of 1, considering the assumption of negligible value for ENEA, the mass of the moving structure should be more than 2 milligrams for noise requirement to be met.

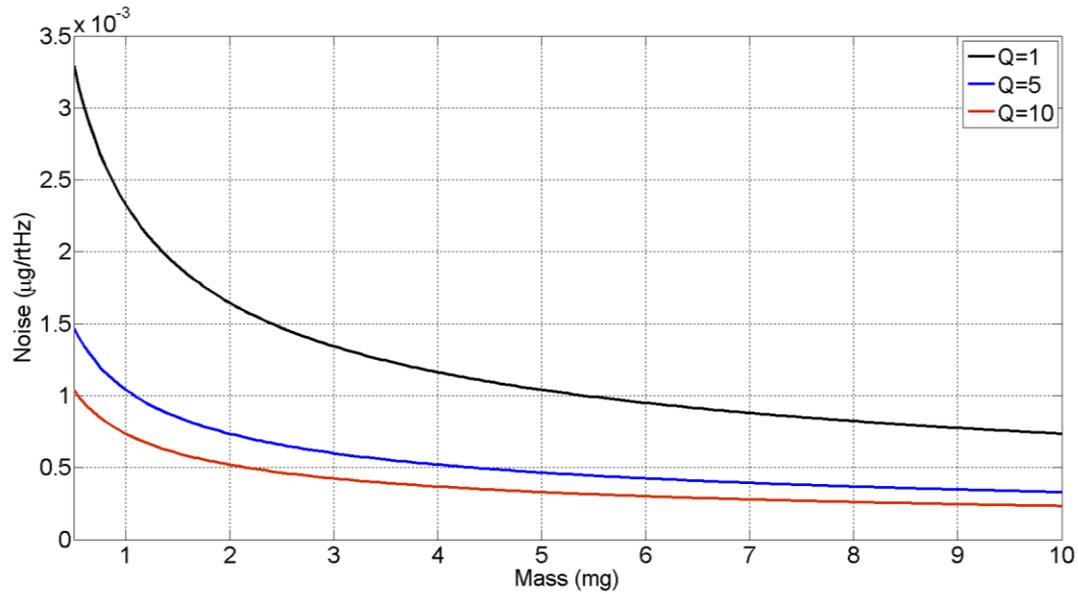


Figure 3.3 - Noise graph of mechanical system with 5 kHz resonance frequency versus mass within three different quality factors

In order to find the required area for achieving the required noise levels, the proof mass dimension with various thicknesses from 100 µm to 500 µm is plotted in Figure 3.4. It is evident that for a 2 mg mass, the proof mass dimension is changing from 4 mm to 9 mm for various thicknesses.

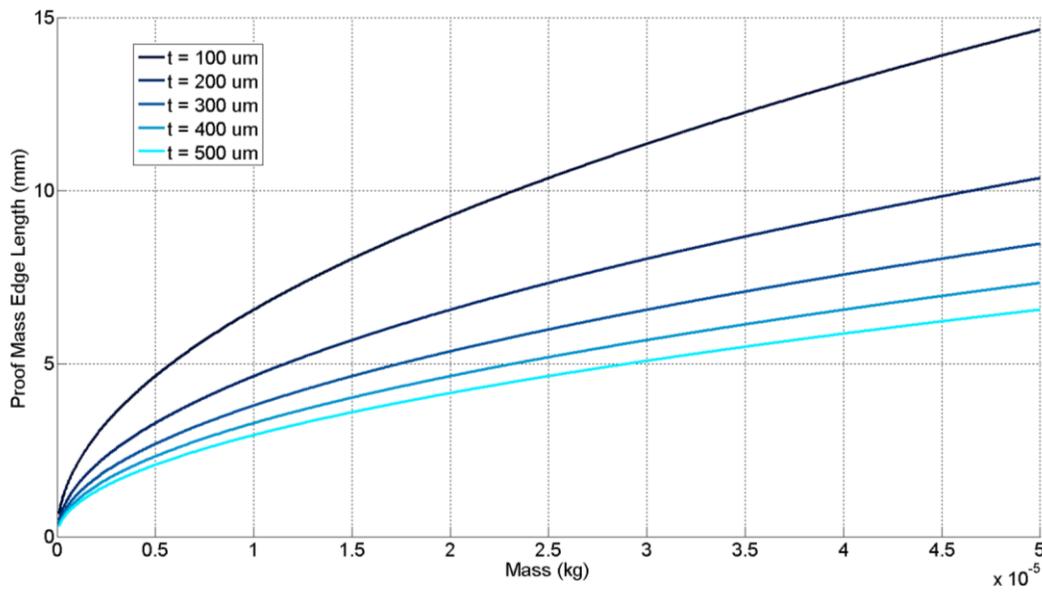


Figure 3.4 - Accelerometer's proof mass dimension versus to the required mass considering various wafer thicknesses

The three graphs, presented above, represent the main mechanical design graphs for the MEMS accelerometer. The last design graph is associated with the capacitive transduction method. The capacitance of a capacitor is calculated by:

$$C = \varepsilon \frac{A}{d} \quad (3.9)$$

where A is capacitive area, d is the capacitive gap, and ε is permittivity coefficient of dielectric material between two capacitive plates. Figure 3.5 - a indicates the capacitance value versus capacitive gap with different capacitive area.

Rate of the capacitance change per unit displacement for lateral displacement of the proof mass is obtained by taking the derivative of equation (3.9) with respect to the lateral displacement of the capacitor's plates (d):

$$\frac{\partial C}{\partial x} = \varepsilon \frac{A}{d^2} \quad (3.10)$$

The total sensitivity of the accelerometer is the function of the sensitivity of the proof mass displacement with respect to the input acceleration, and sensitivity of the capacitance change with respect to the proof mass displacement. Sensitivity of the proof mass displacement with respect to the input acceleration is inversely proportional to the square of resonance frequency of the system, and it is a fixed value. Therefore, the total sensitivity is mainly dominated by the capacitance area and capacitance gap:

$$S_{a_{in}}^{\Delta C} = S_{\Delta x}^{\Delta C} \cdot S_{a_{in}}^{\Delta x} = \frac{\partial C}{\partial x} \cdot \frac{\partial x}{\partial a_{in}} = \frac{\varepsilon_0 A}{d^2 \cdot \omega_0^2} \quad (3.11)$$

Figure 3.5 shows $S_{a_{in}}^{\Delta C}$ versus capacitive gap values with various capacitive areas. As evident from Figure 3.5, by decreasing capacitive gap and increasing capacitive area, sensitivity of the accelerometer system increases.

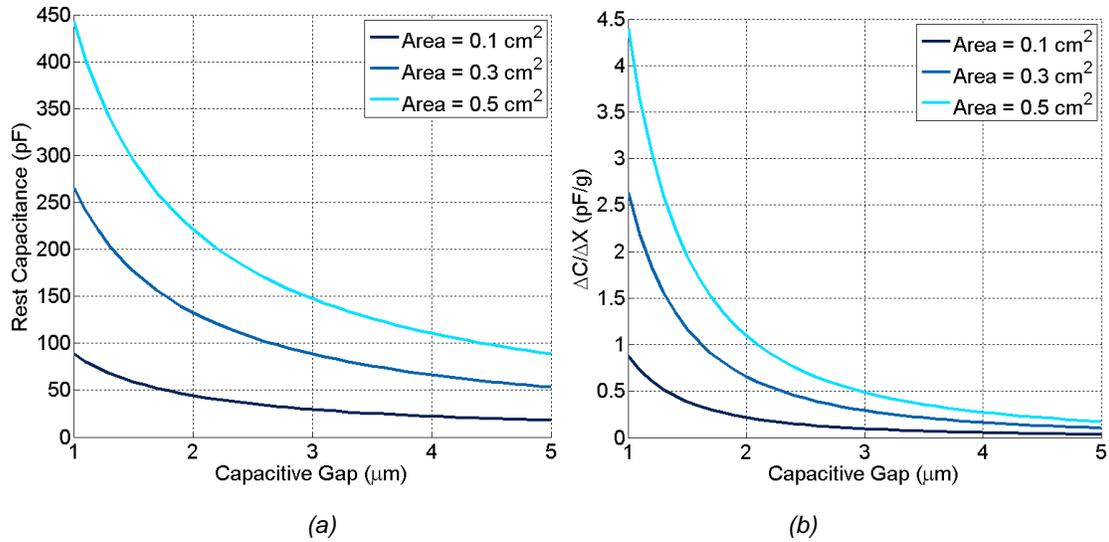


Figure 3.5 – a) capacitance value of an accelerometer versus capacitive gap with various capacitive area b) sensitivity of the accelerometer versus capacitive gap with various capacitive areas

The sensitivity of an accelerometer impacts the total noise equivalent acceleration. Otherwise, the gain of the interface circuit should be increased in a way to make any signal detectable. Increasing gain typically leads to increasing the noise of the circuit. Accordingly, it is required to maximize the sensitivity of the output capacitance to the input acceleration.

Considering all the design metrics, various capacitive accelerometers with high-performance characteristics and industry standard levels were designed, fabricated and evaluated. In light of the available fabrication resources at Simon Fraser University, the design and fabrication process was started with the out-of-plane accelerometers. The out-of-plane fabrication methodology proved economically inefficient due to the low yield. That, in turn, was because of the complications related to the micro-fabrication method. Therefore, the in-plane accelerometer was developed which delivered a higher yield as a result of using a simpler fabrication method. However, a part of the fabrication process needed to be outsourced. In the next section, the theoretical model and simulation results on the out-of-plane and in-plane accelerometers are presented.

3.3. Device Structure

In this section, the designs of the out-of-plane and in-plane accelerometers are elaborated. Furthermore, the accelerometer performance based on theoretical calculations and finite element simulations are depicted.

3.3.1. Out-of-Plane Accelerometer

The basic idea for designing out-of-plane accelerometers was using a continuous membrane which is anchored over its outer perimeter as a spring, with a bulky proof mass in the middle, shown in Figure 3.6. The proof mass and membrane could be of square or circular shapes. Upon applying acceleration; the proof mass oscillates normal to the membrane plane. The fixed plate within the specific gap on top of the membrane forms a capacitor with the top layer of the proof mass. As the proof mass displaces, the capacitive gap between the fixed plate and the moving plate changes. This change leads to a change in the capacitance value between the moving and fixed plates. The change in the capacitance value is a measure of the input acceleration.

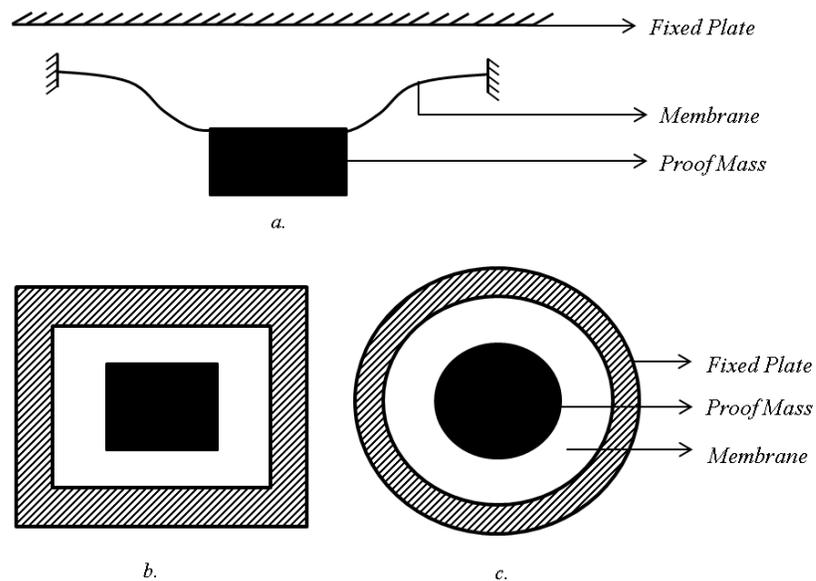


Figure 3.6– Schematic of out-of-plane accelerometer design

Considering the existing fabrication facilities and resources at the time, the first generation of accelerometers consisted of square membranes. Upon progress in the process development, the final design of the out-of-plane accelerometers altered to the circular membrane types. In this section, the final design which was a circular membrane accelerometer is elaborated. However, in Fabrication chapter, a complete discussion over the square membrane generation and then its alteration to the circular membrane generation would be presented.

According to the basic structure shown in Figure 3.7 three structures with various resonance frequencies and consequently various membrane widths were designed and

analyzed, referred to as Designs A1, A2, and A3. The design parameters are represented in Figure 3.7, and the assigned values for each parameter are summarized in Table 3.1.

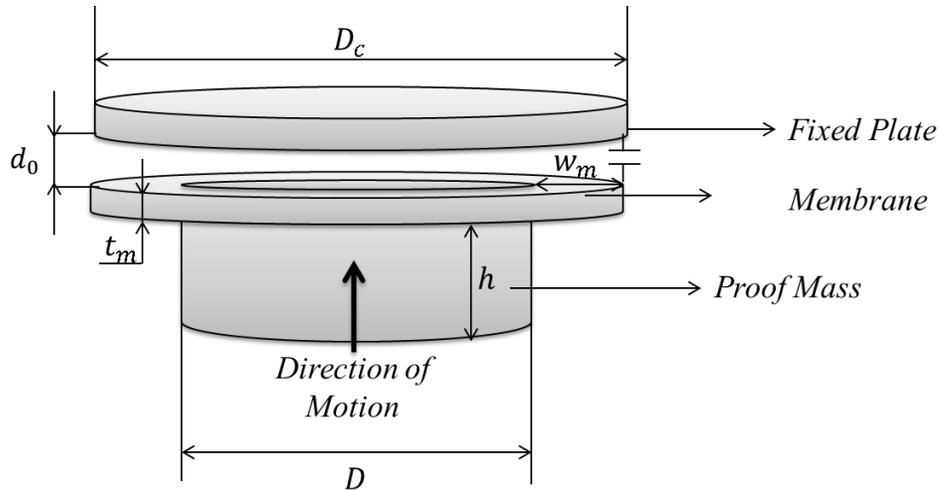


Figure 3.7 - Design parameters representation for an out-of-plane capacitive accelerometer

Table 3.1 – Out-of-plane accelerometer dimensions in μm

	Design A1	Design A2	Design A3
<i>Diameter of the Proof Mass (D) [μm]</i>	6650	6300	5400
<i>Width of the Membrane (w_m) [μm]</i>	175	350	800
<i>Height of the Proof Mass (h) [μm]</i>	510		
<i>Thickness of the Membrane (t_m) [μm]</i>	8		
<i>Diameter of the Capacitive Plate (D_c) [μm]</i>	7000		
<i>Gap between Capacitive Plates (d_0) [μm]</i>	2		

The accelerometer designs presented here were studied both theoretically and through numerical simulations. For static analysis of the accelerometer, theoretical formulas were extracted from [64]. The extracted formulas are based on the following assumptions:

“(1) The plate is flat, of uniform thickness, and of homogeneous isotropic material.

(2) The thickness is not more than about one-quarter of the least transverse dimension, and the maximum deflection is not more than about one-half the thickness.

(3) All forces which include loads and reactions are normal to the plane of the plate.

(4) The plate is nowhere stressed beyond the elastic limit.” [64]

Except the first assumption about the isotropicity of the material, the remaining conditions are applicable to the case of the out-of-plane accelerometer design. The accelerometer membrane and proof mass are made out of silicon which is an anisotropic material. However, the author still uses the theoretical formula with acknowledging of the probable discrepancy specifically in larger membrane deflections. The orthotropic material model properties for standard silicon 100 are summarized in Table 3.2.

Table 3.2 - Material properties for silicon (100)

Young Modulus(E) [GPa]	E_x 169	E_y 169	E_z 130
Poisson Ratio (ν)	ν_{yz} 0.36	ν_{zx} 0.28	ν_{xy} 0.064
Density [kg/m ³]	2330		

The employed model was derived for an annular plate with a uniform annular line load w at radius r_0 from the center of the membrane shown in Figure 3.8-a. The circular membrane accelerometer is considered as an annular membrane with a uniform annular line load w , which is equal to the mass of the proof mass distributed along the circular edge of it. The outer edge of the proof mass is fixed and the inner is considered as guided. The assumption of the guided inner edge is valid since the proof mass is a rigid bulk mass which acts as a guided support. Figure 3.8-b represents the parameters which are used in the theoretical deflection formula.

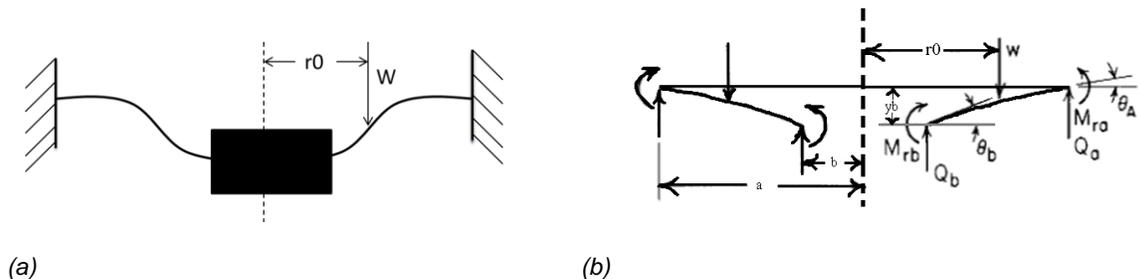


Figure 3.8 - a) Parameters representation for an annular plate with a uniform annular line load w at radius r_0 , b) representation of the specific case, outer edge fixed, inner edge guided[64]

Equation (3.12) is the general formula for deflection of an annular plate with a uniform annular line load w at r_0 .

$$y = y_b + \theta_b r F_1 + M_{rb} \frac{r^2}{D} F_2 + Q_b \frac{r^3}{D} F_3 - \omega \frac{r^3}{D} G_3 \quad (3.12)$$

where r is the radius at where we want to calculate the deflection, w is the applied force per unit length. D is the plate constant represented by $D = \frac{-Et^3}{12(1-\nu^2)}$ which E is module of elasticity, t is the plate thickness, and ν is the Poisson's ratio. The other parameters including y_b , θ_b , M_{rb} , Q_b , F_1 , F_2 , F_3 , and G_3 are the case specific parameters which are defined based on the boundary conditions. For our specific case, which is outer edge fixed, inner edge guided, these parameters are defined using the following equations [64]:

$$y_b = \frac{-\omega a^3}{D} \left(\frac{C_2 L_6}{C_5} - L_3 \right) \quad (3.13)$$

$$M_{rb} = \frac{-\omega a}{C_5} L_6 \quad (3.14)$$

$$C_2 = \frac{1}{4} \left[1 - \left(\frac{b}{a} \right)^2 \left(1 + 2L_n \frac{b}{a} \right) \right] \quad (3.15)$$

$$C_5 = \frac{1}{2} \left[1 - \left(\frac{b}{a} \right)^2 \right] \quad (3.16)$$

$$L_3 = \frac{r_0}{4a} \left[\left(\left(\frac{r_0}{a} \right)^2 + 1 \right) L_n \frac{a}{r_0} + \left(\frac{r_0}{a} \right)^2 - 1 \right] \quad (3.17)$$

$$L_6 = \frac{r_0}{4a} \left[\left(\left(\frac{r_0}{a} \right)^2 - 1 + 2L_n \frac{a}{r_0} \right) \right] \quad (3.18)$$

$$F_2 = \frac{1}{4} \left(1 - \left(\frac{b}{r} \right)^2 \left(1 + 2L_n \frac{r}{b} \right) \right) \quad (3.19)$$

$$G_3 = \frac{r_0}{4r} \left(\left(\left(\frac{r_0}{r} \right)^2 + 1 \right) L_n \frac{r}{r_0} + \left(\frac{r_0}{r} \right)^2 - 1 \right) \quad (3.20)$$

$$\theta_b = 0 \quad , \quad Q_b = 0 \quad (3.21)$$

where a is the radius of the proof mass plus the width of the membrane, b is the radius of the proof mass, and r_0 is the load application radius which in our case is equal to b . Upon applying 1 g acceleration, the diagram of the membrane deflections calculated from equation (3.12) for the three designs of the circular membrane are shown in Figure 3.9.

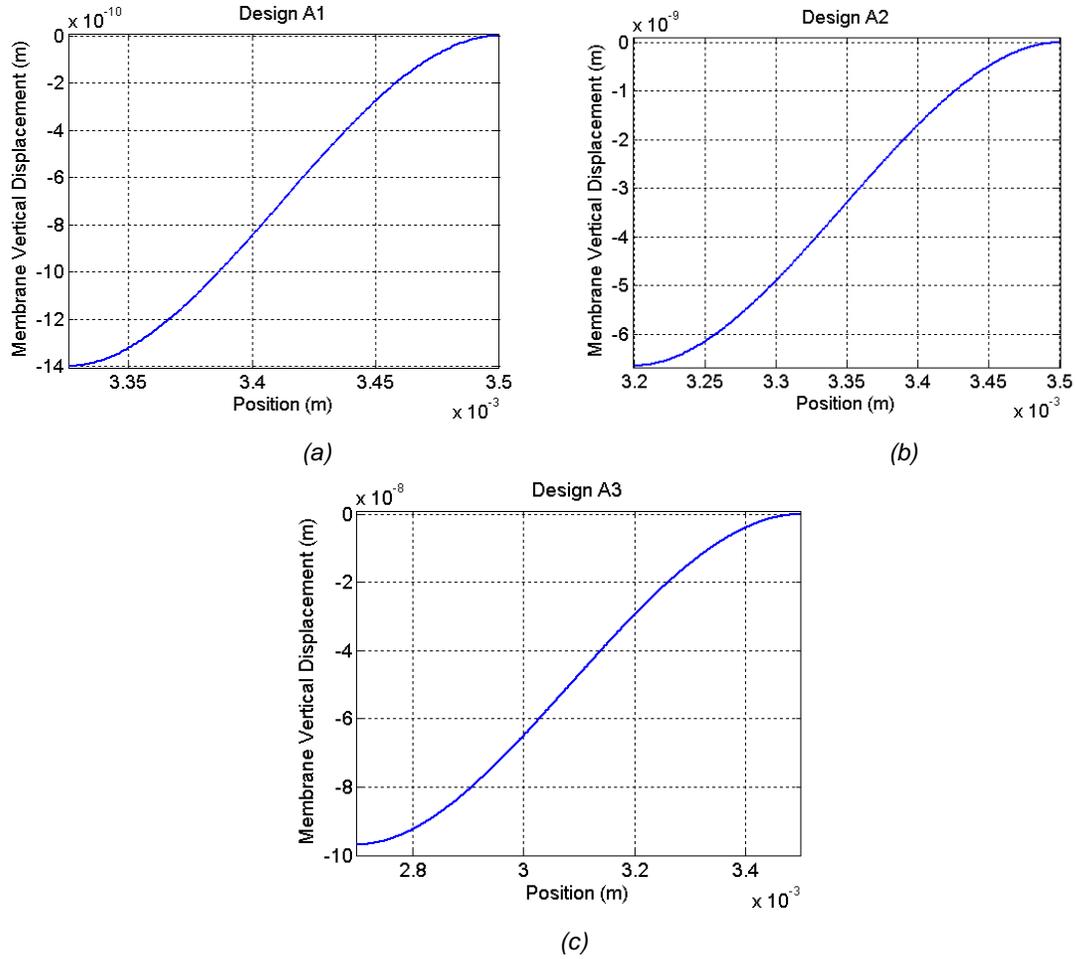


Figure 3.9 - Displacement across the membrane from the edge of the membrane to the edge of the anchor with the input of 1g

Once the proof mass displacement in response to an applied acceleration is identified, the resonance frequency can be estimated using equation (3.22).

$$\omega = \sqrt{\frac{k}{m}} = \sqrt{\frac{F/y}{m}} = \sqrt{\frac{mg/y}{m}} = \sqrt{\frac{g}{y}} \quad (3.22)$$

In equation (3.21), k is the spring constant of the membrane, m is the mass of the proof mass, g is the gravity acceleration, and y is the displacement of the proof mass due to an input acceleration of 1 g. The modal analysis study was also performed using ANSYS. Figure 3.10 shows the first four mode shapes for Design A1.

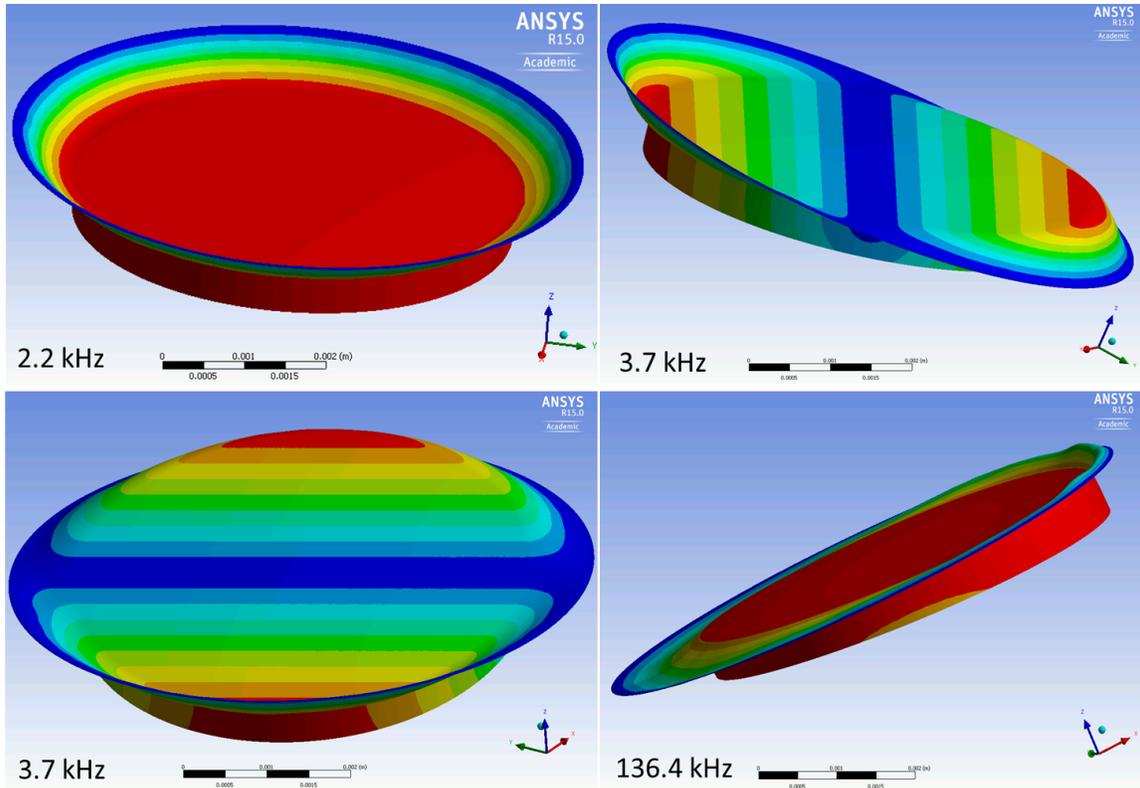


Figure 3.10 - The first four resonance frequencies of the out-of-plane accelerometer, Design A1

Table 3.3 summarizes the mechanical properties of the designed out-of-plane accelerometers. In this table, the theoretical and simulated resonance frequencies for the designs A1, A2, and A3 are shown. The discrepancy between theoretical and experimental results for designs A1, A2, and A3, are 10, 10, and 27 percent, respectively. The discrepancies have various root causes such as isotropicity assumption of Silicon and non-normality of the load relative to the membrane plane due to deformation of the membrane. Considering the resonance frequencies derived from the ANSYS simulations, the MNEA of the accelerometers are calculated using equation (3.8) for two values of quality factors. The results are shown in Table 3.3. As shown in this table, Design A2 could meet the requirements of the project regarding noise and resonance frequency criteria.

Table 3.3 - Theoretical and Simulated Resonance Frequencies for Out-of-Plane Accelerometer

		Design A1	Design A2	Design A3
Theoretical Resonance Frequency [kHz]		13.3	5.1	1.6
Simulated Resonance Frequency [kHz]		14.8	5.7	2.2
Noise [ng/\sqrt{Hz}]	Q = 1	623	452	309
	Q = 10	197	122	98

To test the accelerometer and measure the change in capacitance through an electronic interface, the electrical specifications of the accelerometer should be calculated. These properties include the bulk capacitances and the sensitivities are summarized in Table 3.4.

Table 3. 4 - Accelerometer's Electrical Properties

	Design A1	Design A2	Design A3
Bulk Capacitance (pF)	170		
Sensitivity (pF/g)	0.11	0.72	6.56

After specifying required dimension to meet the desired performance criteria, a proper microfabrication process was developed. In the next chapter, the fabrication process will be explained in detail.

3.3.2. In-Plane Accelerometer

In this section, the design procedure for development of the in-plane accelerometers is explained. The design process was started with a low bandwidth accelerometer called prototype I which mainly utilized for verification of the fabrication capabilities. Then, the design was modified using a proposed platform to achieve a high bandwidth and high sensitivity accelerometer, called prototype II. Following that, due to the fabrication yield issues, a few modifications was performed on the in-plane design and the final design, called prototype III, was developed.

Prototype I

The first in-plane designed accelerometer was a typical in-plane comb finger accelerometer, indicated in Figure 3.11-a [65]. The designed accelerometer was mainly intended for developing the test procedures and identifying the fabrication limitations. As shown in Figure 3.11-b, the accelerometer layout constitutes a proof mass, moving

electrodes which are attached to the proof mass, fixed electrodes which are attached to the substrate, suspension beams, and one pair of control electrodes. As the accelerometer is subjected to acceleration, the external force is transferred to the proof mass through the suspension elements. Accordingly, the proof mass and the moving comb fingers displaces relative to the stationary comb fingers which are fixed to the substrate. The displacement changes the capacitance between the moving and fixed electrodes. Capacitance change is measured differentially using an electronic interface.

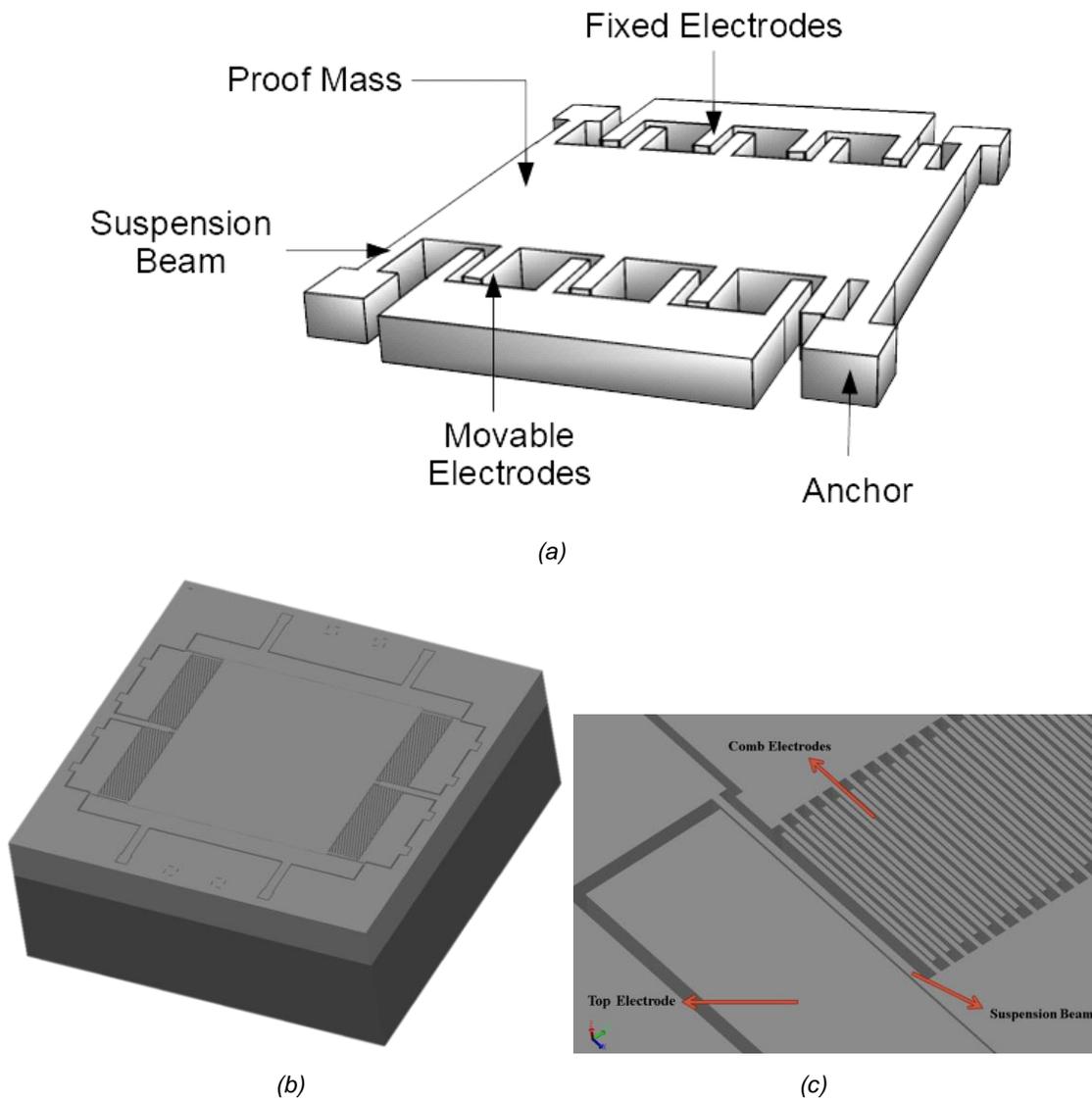


Figure 3.11 - a) Schematic of an in-plane capacitive accelerometer, b) prototype I, and c) enlarged view of comb fingers, suspension beam and top control electrode

The accelerometer has 4 clamped-guided suspension beams. The dimension of the accelerometer along with its mechanical properties is shown in Table 3.5.

Table 3.5 – Prototype I mechanical properties

Die Size [mm^2]		10 × 10
Proof Mass Dimension [μm^3]		5000 × 5000 × 100 μm^3
Suspension Beams Dimension [μm^3]		1000 × 25 × 100
Mass (mg)		5.8
Resonance Frequency (kHz)		2.1
MNEA (ng/Hz)	Q=1	624
	Q=10	198

The in-plane accelerometers have the typical transverse capacitive comb configuration shown in Figure 3.12. In this configuration, with only one routing layer available, each stationary comb finger is located between two moving fingers with two different gap values, d_0 , and dd_0 , which comprise 2 parallel capacitors. As the proof mass moves, the total capacitance changes are dominated by the variations in the smaller gap. In order to decrease the adverse effect of the large gap on the capacitance change, it is desirable to increase the larger gap as much as possible. Additionally, it is desired to increase the number of sensing elements as it increases the total capacitance change per unit change in proof mass displacement. However, the chip area, where the capacitors can be located, is limited. Hence, in order to achieve maximum sensitivity, a compromise should be established between the number of combs (n) and the dd_0/d_0 ratio.

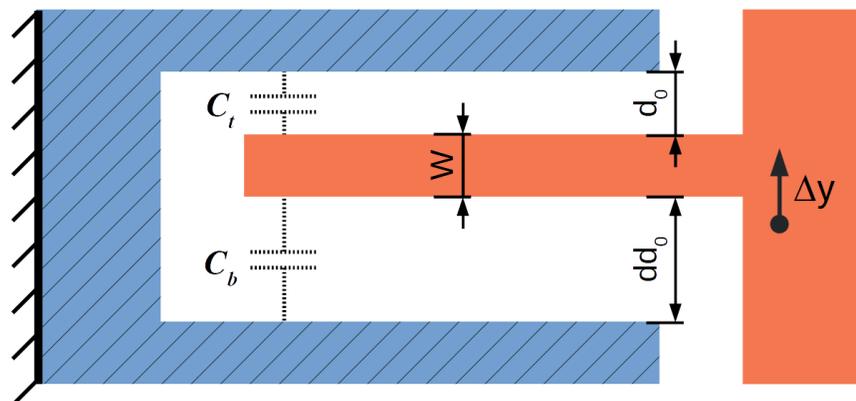


Figure 3.12 - Interdigitated Capacitive Comb Finger

The relation between changes in capacitance value (ΔC), small gap value (d_0), comb width (w), gap ratio ($\alpha = \frac{dd_0}{d_0}$), and the number of combs (n), is as follows:

$$\Delta C = n \frac{2\epsilon y A (d_0^2 - (\alpha d_0)^2)}{(d_0^2 - y^2)((\alpha d_0)^2 - y^2)} \quad (3.23)$$

where y is the relative displacement of the combs. By considering the maximum achievable aspect ratio, which is the thickness of the structural layer over the minimum achievable gap between electrodes, an optimized value for α could be achieved. According to the length of the proof mass, the number of electrodes that can be located on the edge is derived from the following formula:

$$n = \text{int} \left[\frac{L}{2w + d_0(1 + \alpha)} \right] \quad (3.24)$$

where L is the length of the proof mass and w is the width of the comb fingers. By plugging in equation (3.24) into equation (3.23), the graph of changes in capacitance value versus gap ratio is achieved. Figure 3.13 shows these graph for different values of the small capacitive gap, i.e. d_0 .

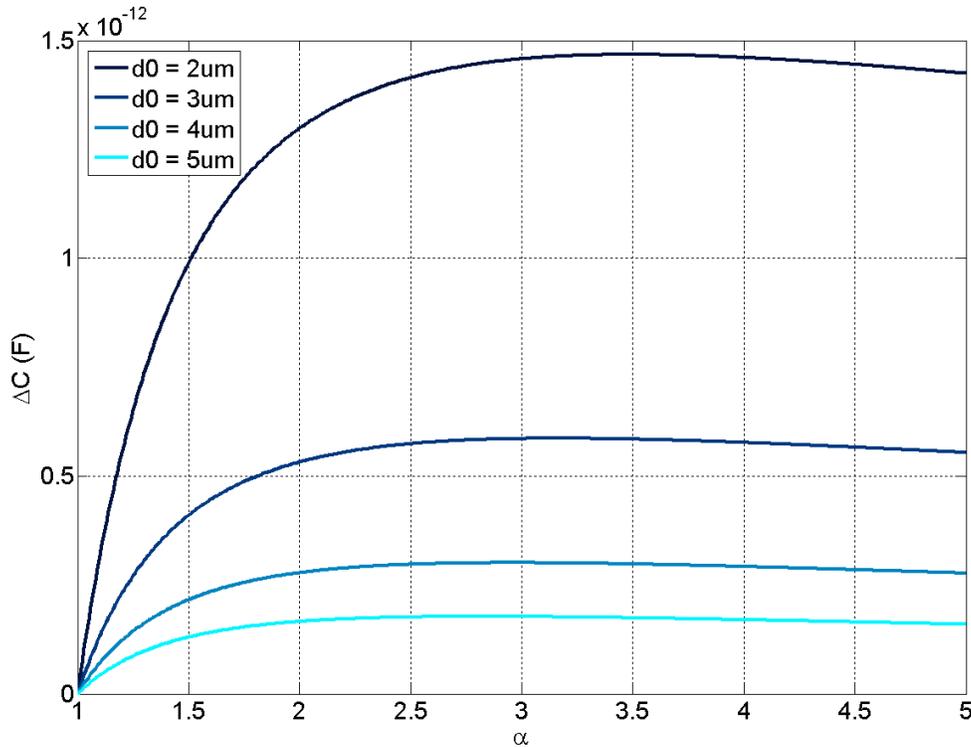


Figure 3.13 - Change in capacitance versus the ratio of the capacitive gaps on the two sides of each comb finger

As evident from Figure 3.13, graph of capacitance change versus α is maximized in the specific gap ratios associated with the value of the small gap. Figure 3.14 shows α maximum versus the small gap value.

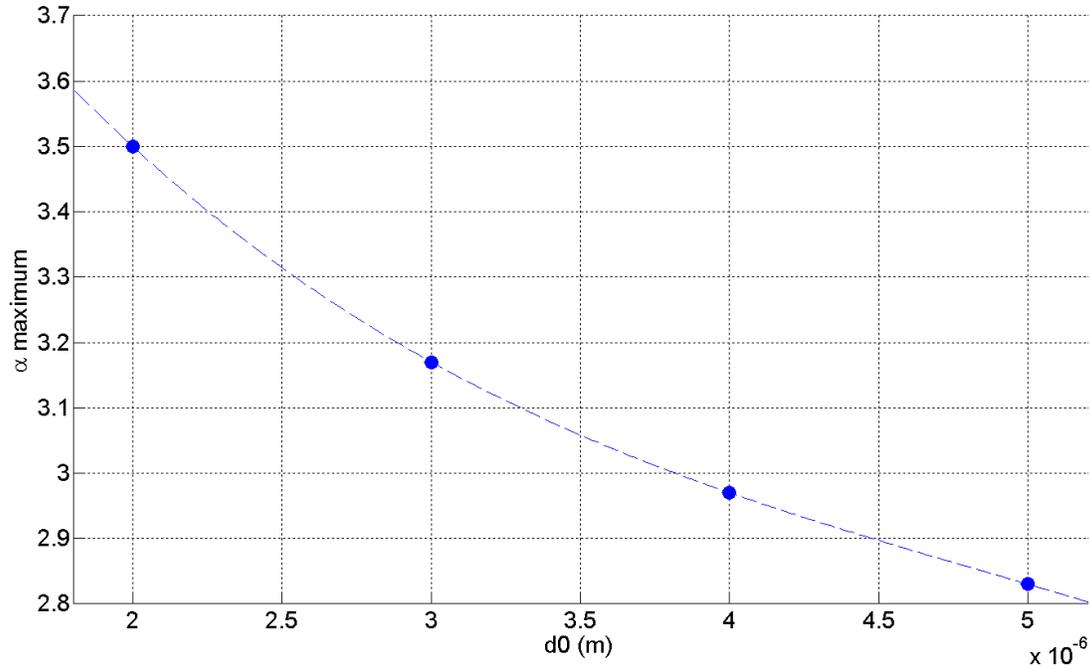


Figure 3.14 - Maximum change in capacitance versus the initial small gap value.

Considering Figure 3.14, it is concluded that for the case of prototype I with the small gap of 5 μm , the large gap should be 2.83 times of the small gap. According to these values, thickness of the structure, comb fingers length, the capacitive characteristics of the sensing electrodes are calculated. On the final mask layout, two different gap values of 5 μm and 7 μm were designed. The calculated characteristic values for large gap devices (7 μm gap) and small gap devices (5 μm gap) are summarized in Table 3.6.

Table 3.6 - Capacitive characteristics of in-plane accelerometer- Prototype I

	LG*	SG*
Bulk Capacitance (pF)	12	17
Sensitivity (pF/g)	0.14	0.28
Pull-In Voltage (v)	111	41

LG: Large Gap
SG: Small Gap

In order to verify the theoretical results, the accelerometer mechanical structure was simulated in CoventorWare. The results for modal analysis are shown in Figure 3.15. The first resonance frequency is an in-plane mode shape with 2.1 kHz frequency which is in good agreement with theoretical results.

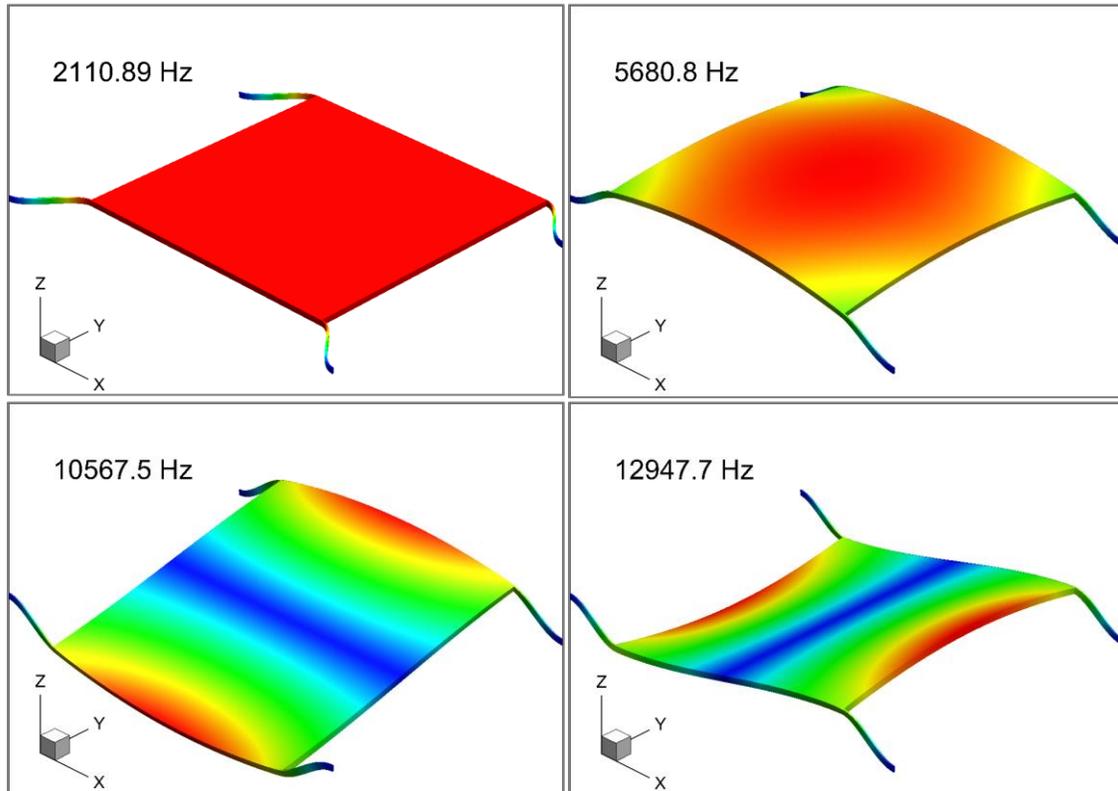


Figure 3.15 - The first four mode shapes of the in-plane accelerometer, prototype I

The issue with prototype I was that the resonance frequency was limited and could not meet the requirements of the project. Moreover, the sensitivity of the accelerometer could not meet the requirement for electronic noise level. In order to achieving low noise level in the electronic circuit, the sensitivity should be at least 0.7 pF/g as dictated by the interface electronic designer of the team. Otherwise, the output signal of the accelerometer should be amplified, and amplification is equivalent to introducing more noise into the system. Consequently, it was required to increase the bandwidth and also sensitivity of the accelerometer design. This requirement led to the second prototype in-plane accelerometer design which is elaborated in the next section.

Prototype II

In order to comply with the design objectives, prototype I design was required to be modified in a way to have wider bandwidth. Meanwhile, to meet the noise floor requirements, the sensitivity of the device should be increased. In order to get the desired bandwidth, in the first try, the suspension beams stiffness was increased. The first four mode shapes of the modified design are shown in Figure 3.16. The sensing axis in this accelerometer was supposed to be in y-direction. As evident in Figure 3.16, the out-of-plane mode, which constitutes the second mode of the modified design, got pretty close to the first vibration mode. This means that any input vibration in z-axis can deteriorate the sensitivity of the accelerometer in its main axis, i.e., y-axis. Hence, it was required to still modify this design to push the second mode far from the main mode.

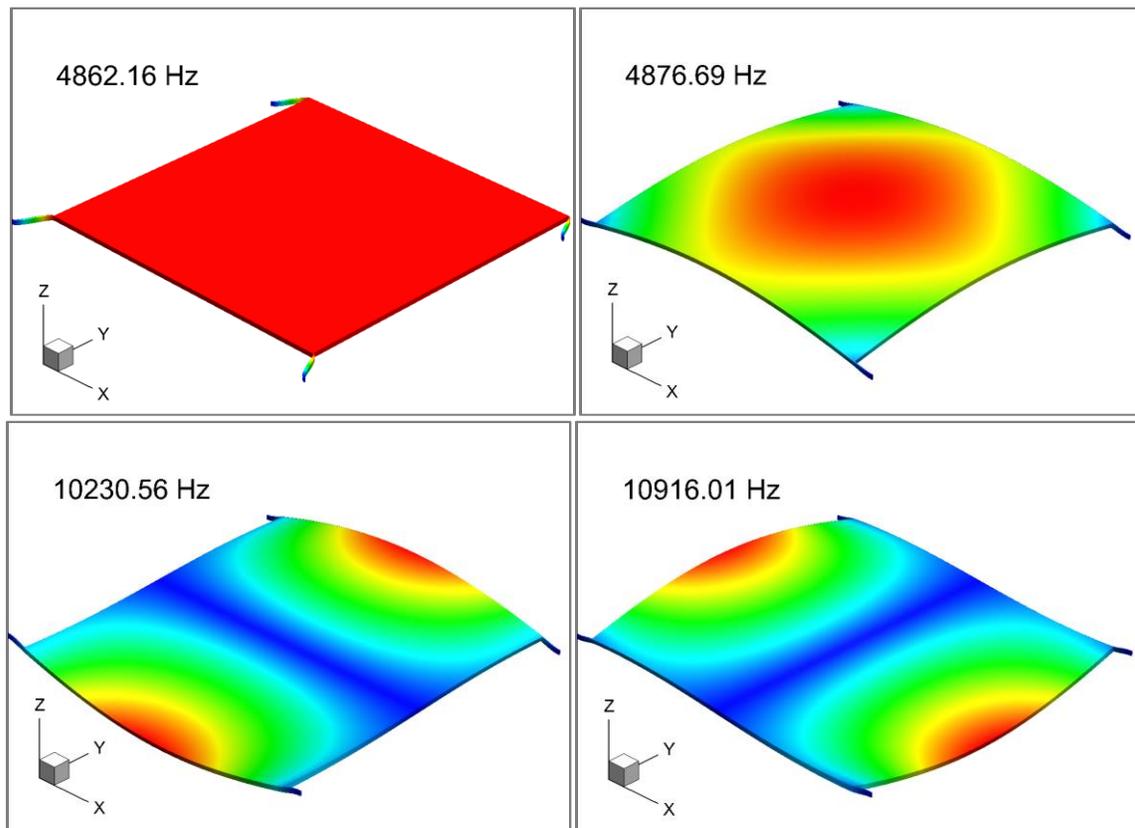


Figure 3.16 - The first four mode shapes for the first modified in-plane accelerometer for higher bandwidth

Apart from the proximity of the first and second modes of the modified accelerometer design, the attainable sensitivity in this design could also not fulfil the design requirements. As mentioned earlier, low-frequency proof mass displacements are

quadratically proportional to the inverse of the resonance frequency, equation (3.6). Taking DC to fundamental resonance frequency as the operating bandwidth of the accelerometer, the proof mass displacement due to an input acceleration is limited by the bandwidth of the device. As a result, increasing the bandwidth while keeping the same setup for sensing electrodes, i.e. sensing gap value and number of electrodes, is translated as decreasing the total sensitivity quadratically. In order to address the issue of sensitivity, it is required to increase the value of capacitance change per unit displacement of the proof mass. Decreasing the sensing gap and increasing the number of sensing electrodes are the two methods for increasing the capacitance change per unit displacement of the proof mass. The main issue in decreasing the sensing gap is fabrication limitation, i.e. etching aspect ratio. Etching aspect ratio is the ratio of the thickness of the wafer over the minimum gap width. For fabrication of prototype I, the required aspect ratio was 20, i.e. etching a capacitive gap of 5 μm on a 100 μm wafer. In Deep Reactive Ion Etching (DRIE) process, aspect ratio of 20 is not a critical value and it is achievable in a proper MEMS foundry. Since, we need more sensitivity in our process; we pushed the etching aspect ratio to 50, i.e. etching a capacitive gap of 2 μm on a 100 μm wafer. This aspect of the fabrication process would be explained in more details in fabrication chapter. Keeping the same number of sensing elements while increasing the aspect ratio, still does not deliver the required sensitivity. In order to address this issue, it was required to increase the number of sensing elements. For increasing the number of sensing elements, it was proposed to substitute a moving frame in place of the continuous solid body proof mass. The moving frame provides more internal and external edges for stacking sensing electrodes which leads to increasing the sense area and therefore increasing the sensitivity. Since changing the proof mass structure results in changes in dynamic response of the accelerometer, an initial simulation was performed to identify the possible problems. As shown in Figure 3.17, due to snipping the areas inside the proof mass, the unwanted flexural modes are introduced to the working bandwidth of the device.

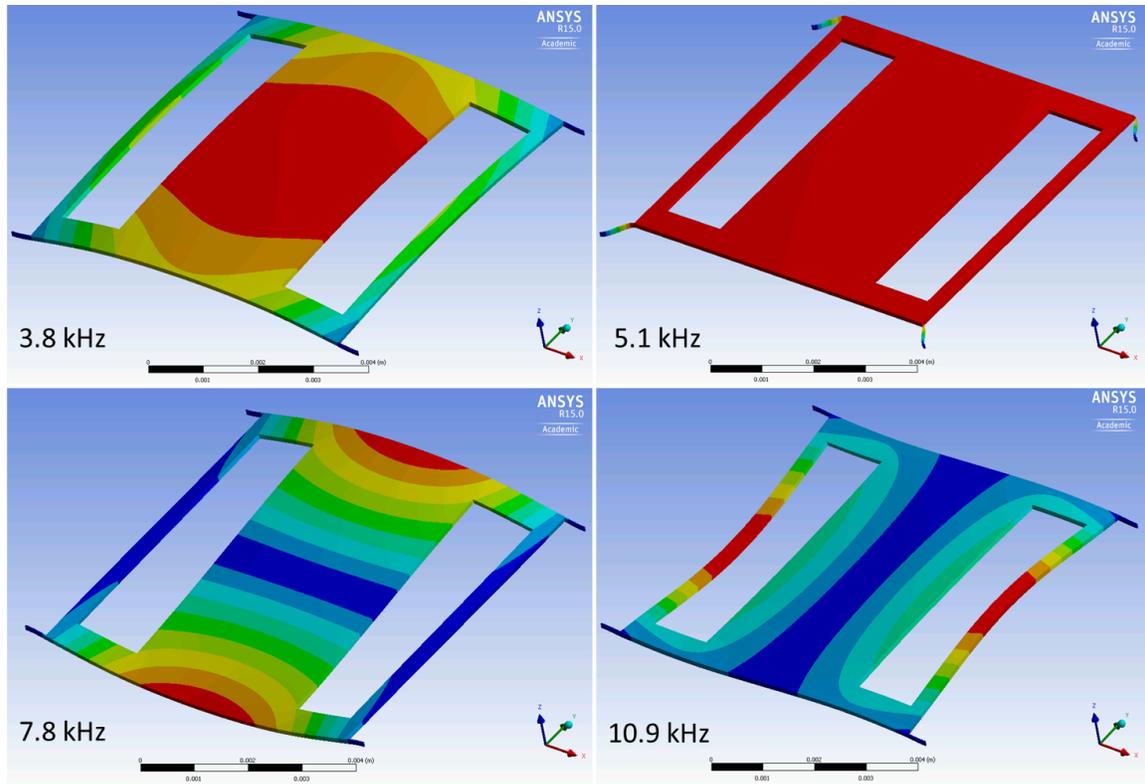


Figure 3.17 - The first four mode shapes for the second modified in-plane accelerometer for higher sensitivity

In order to address the issue regarding the unwanted modes, it was proposed to locate the elastic elements and anchor points inside the moving frame in a way to suppress the unwanted flexural modes, herein referred to as Mode Tuning Structural Platform (MTSP). MTSP include the modifications of substituting the proof mass with a moving frame, implementing sensing elements on the internal and external edges of the moving frame, and locating elastic elements and anchor points inside and outside of the moving frame [66], [67]. Employing this platform for designing an accelerometer could address both the sensitivity and the noise issues. MTSP can be thought of as a topology optimization problem. In this current thesis, the optimization process was performed by the designer through consecutive FEM simulations considering the existing constraint. In the future works, an optimization code could be developed to deliver an optimized structural shape in terms of bandwidth, noise, and sensitivity by considering the dimensional constraints. Figure 3.18 shows a schematic of an accelerometer in MTSP platform. As shown, the continuous solid body proof mass is replaced by a moving frame. The moving frame provides enough space to enclose the sensing elements and also internal anchors and suspension beams.

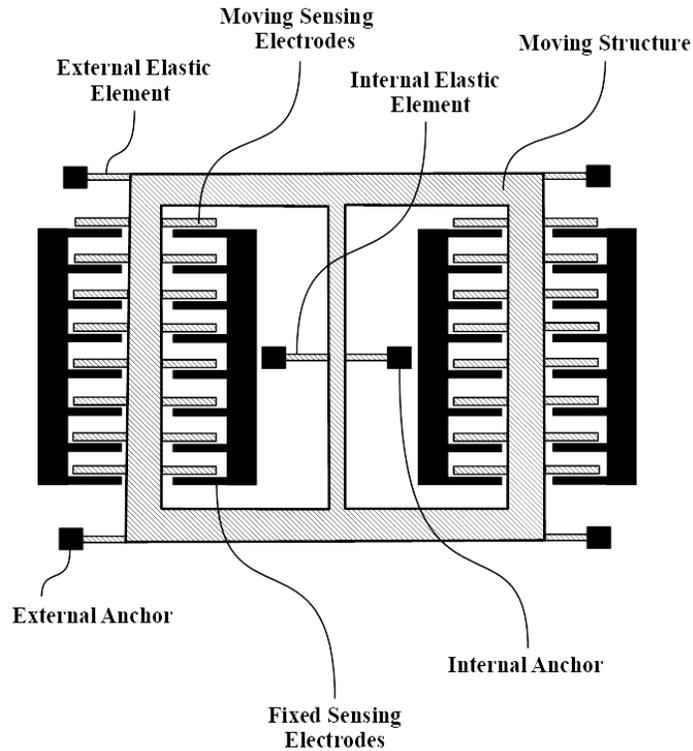
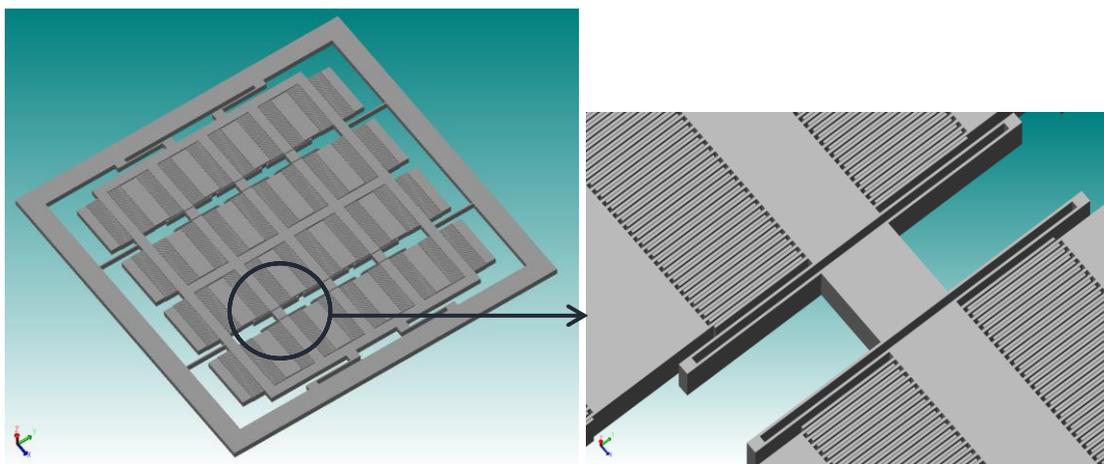
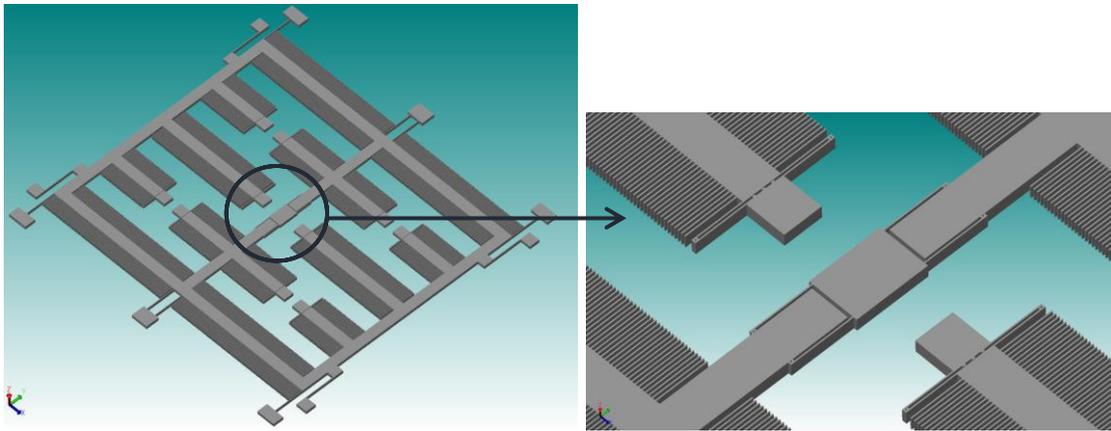


Figure 3.18 - A general Schematic of an accelerometer designed based on MTSP

In the first round of design, two accelerometers were designed based on MTSP. The accelerometer designs, i.e. Design A and Design B, are shown on the left side of Figure 3.19. The enlarged views of these accelerometers are shown in right side of the picture. In the enlarged view, the anchors, suspension beams, sensing elements, and moving structure are distinguishable.



(a)



(b)

Figure 3.19 - 3D view of the in plane capacitive accelerometers prototype II designed based on MTSP, a) Design A, b) Design B

Design A and B modal analysis simulation results in CoventorWare are shown in Figure 3.20 and Figure 3.21. As shown in these figures, the unwanted modes are properly pushed away from the operating bandwidth of the device. The second mode of operation of Design A and B has more than 5 kHz and 10 kHz separation from the first resonant mode, respectively. The mechanical and electrical properties of the designed accelerometers are summarized in Table 3.7.

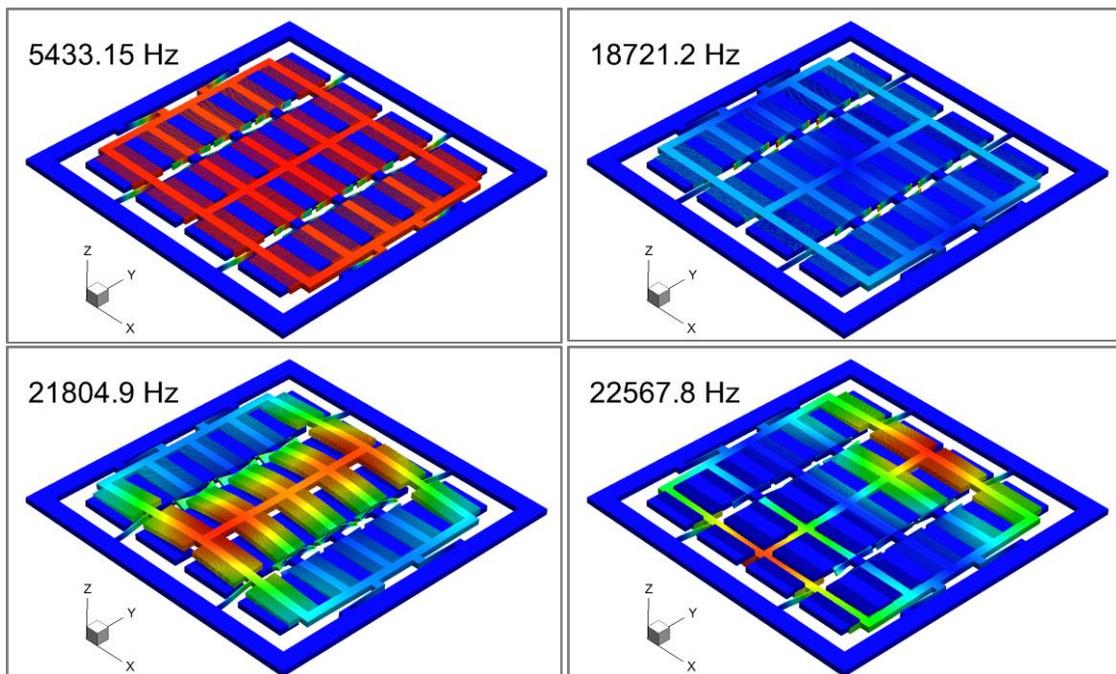


Figure 3.20 – Simulated modal analysis of prototype II, Design A

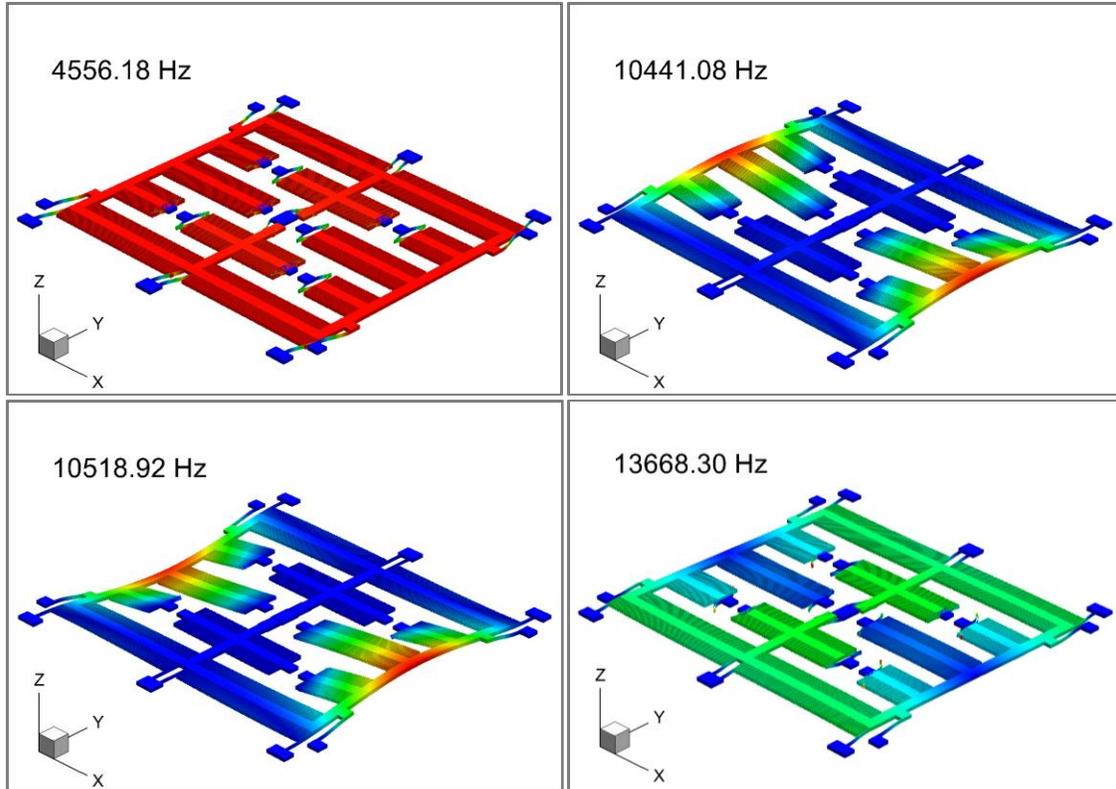


Figure 3.21 - Simulated modal analysis of prototype II, Design B

Table 3.7 - Properties of the in-plane accelerometers prototype II designed in MTSP

Mechanical Properties	Design A			Design B		
Mass (mg)	4.43			4.5		
Resonance Frequency (kHz)	5.4			4.6		
MNEA (ng/\sqrt{Hz})	330			317		
Electrical Properties	A1	A2	A3	B1	B2	B3
Bulk Capacitance (pF)	255	215	193	272	238	203
Total No. of Combs	1122	1080	1054	1196	1134	1106
Sensitivity (pF/g)	1.67	1.2	1	2	1.5	1.18

From the design point of view, these accelerometer designs not only meet the design requirements but also exceed them. However, in reality, many practical issues came up in the fabrication process as will be explained in detail in the next chapter. To put the fabrication problems in a nutshell, the main issue was the short circuit between the comb fingers due to the scattered particles in the cleanroom. For prototype II designs, this issue was even worse since the area of the sensing electrodes on a single

die was large and a single particle could ruin the functionality of the whole device. Therefore, it was proposed to decrease the number of the sensing electrodes down to a value that just meets the project requirements. These modifications resulted in the final product called Prototype III as explained in the next section.

Prototype III

Prototype III accelerometer 3D layout is shown in Figure 3.22 - a. Similar to prototype II, the accelerometer was designed based on MTSP. Figure 3.22 – b shows the enlarged views of the internal anchors and elastic elements. The accelerometer constitutes moving proof mass, suspension beams, anchor points and parallel electrodes which act as the sensing elements. The sensing axis of the accelerometer is along the x-direction. The accelerometer has six internal beams and six external beams as the suspension elements. The internal elastic elements are designed to suppress the flexural vibration modes. The mechanical and electrical properties of the designed accelerometers are summarized in Table 3.8.

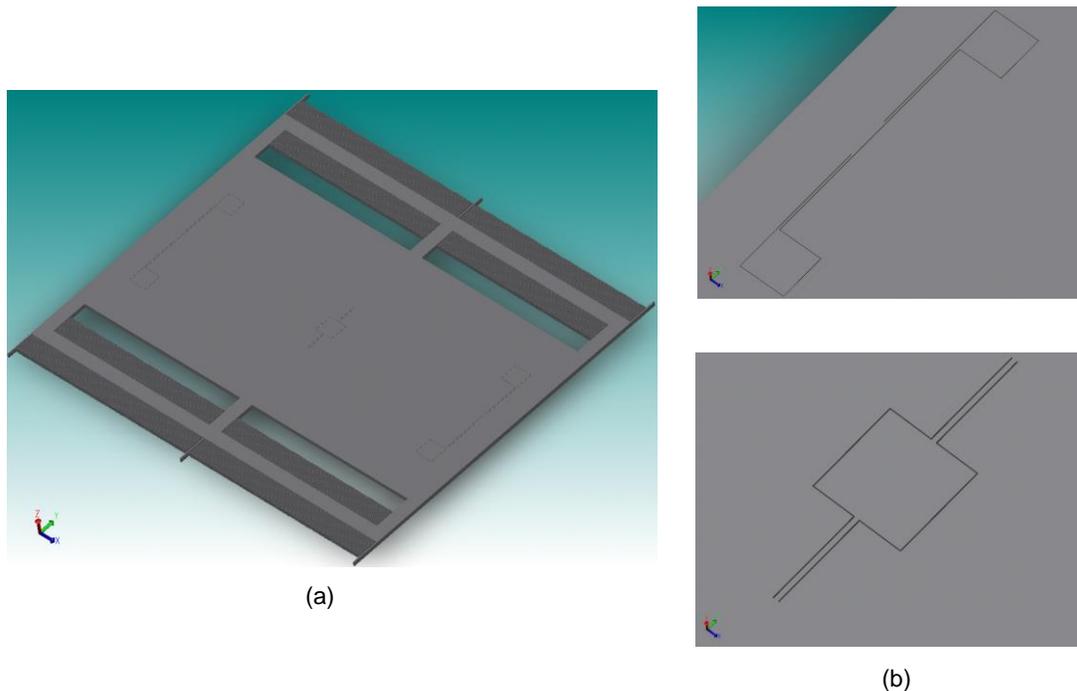


Figure 3.22 – a) 3D schematic of the in-plane accelerometer, prototype III, b) enlarged view of the internal anchors and elastic elements

Modal analysis of the accelerometer was performed in CoventorWare. Figure 3.23 shows the first four mode shapes of the accelerometer. The dynamic analysis of the

accelerometer shows that the first resonance frequency of the accelerometer corresponds to x- direction vibration with a frequency of 4.6 kHz. The second mode is apart from the first mode by more than 6 kHz. Therefore, the analysis confirms using MTSP could be a viable approach for widening the bandwidth of the accelerometer and achieving high-performance accelerometer designs.

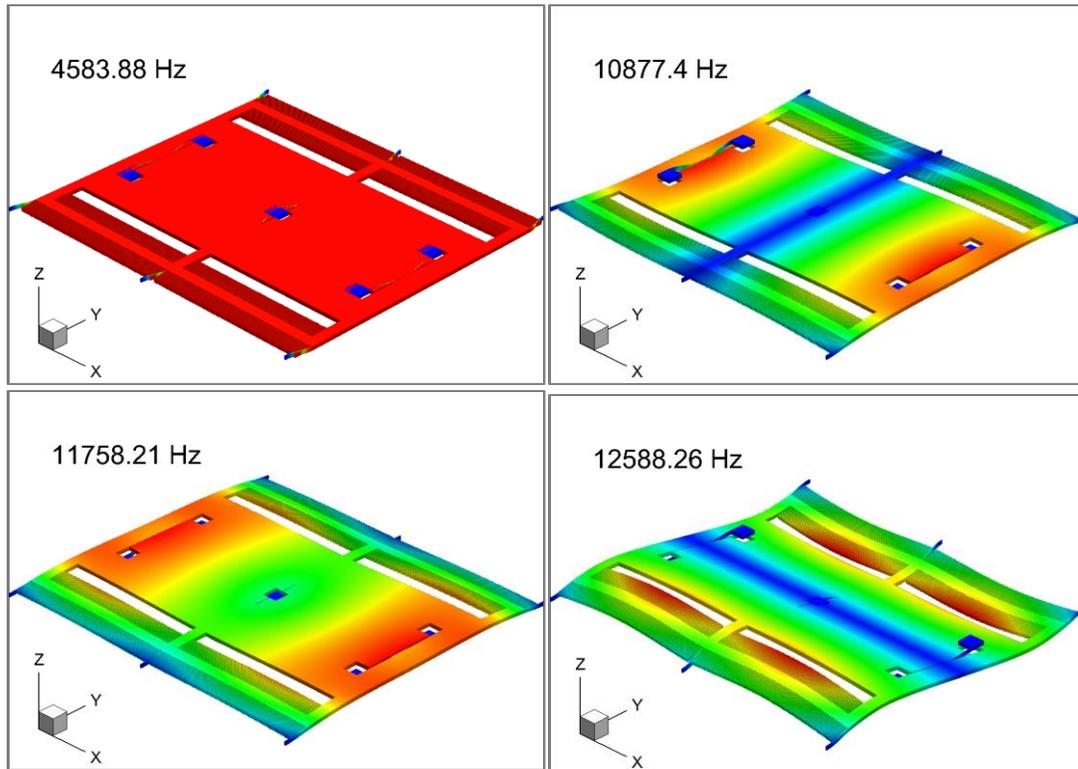


Figure 3.23 - Simulated modal analysis of prototype III

Table 3.8 - Properties of the in-plane accelerometers prototype III designed in MTSP

Mechanical Properties		
Mass (mg)	9	
Resonance Frequency (kHz)	4.6	
MNEA (ng/\sqrt{Hz})	Q=1	741
	Q=10	234
Electrical Properties		
Bulk Capacitance (pF)	72	
Sensitivity (pF/g)	0.65	

Chapter 4. Fabrication

In this section, the fabrication process developments for out-of-plane and in-plane accelerometers are explained. The developments of the fabrication processes were completed at the following cleanrooms:

- Institute of Micromachined and Microfabrication Research (IMMR) facility at School of Engineering Science, Simon Fraser University
- 4D LABs at Simon Fraser University
- Lurie Nanofabrication Facility (LNF) at the University of Michigan
- nanoFAB at the University of Alberta

Throughout the rest of this work, OA will be used as an abbreviation for Out-of-plane Accelerometer and IA will stand for In-plane Accelerometer. The detailed fabrication process steps for out-of-plane (OA) and in-plane accelerometers (IA) are attached in Appendix B.

4.1. Out-of-Plane Accelerometer Fabrication Process

The original idea for the fabrication of the out-of-plane MEMS accelerometer was to make the sensor out of two bonded wafers: a glass wafer on which the top fixed electrode is located and a Silicon-On-Insulator (SOI) wafer from which the proof mass, membrane, and contact holes were etched.

The fabrication process of the out-of-plane accelerometer was significantly changed through the evolving versions of the product. Considering the available micro-fabrication resources at Simon Fraser University, the initial fabrication processes for the out-of-plane accelerometers were developed based on wet etching of the proof mass and square membrane. However, due to the emerging technical challenges, the fabrication process was later on transformed to dry etching of the proof mass and circular membrane. Therefore, a few steps of the fabrication process were outsourced to nanoFAB at the University of Alberta. In this work, SPP stands for the square proof mass

process which is based on wet etching of the proof mass, and CPP stands for the circular proof mass process which is based on dry etching process.

In this section, both the processes for the square and circular proof mass devices along with the outcomes of each method are explained in detail.

4.1.1. Square Proof Mass Process (SPP)

Figure 4.1 shows a schematic of an out-of-plane accelerometer die based on the wet etching process. The accelerometer die is an anodically bonded glass and SOI wafer. The fabrication process includes processes on the glass wafer, processes on the SOI wafer, anodic bonding of glass and SOI wafer, and processes on the integrated wafer.

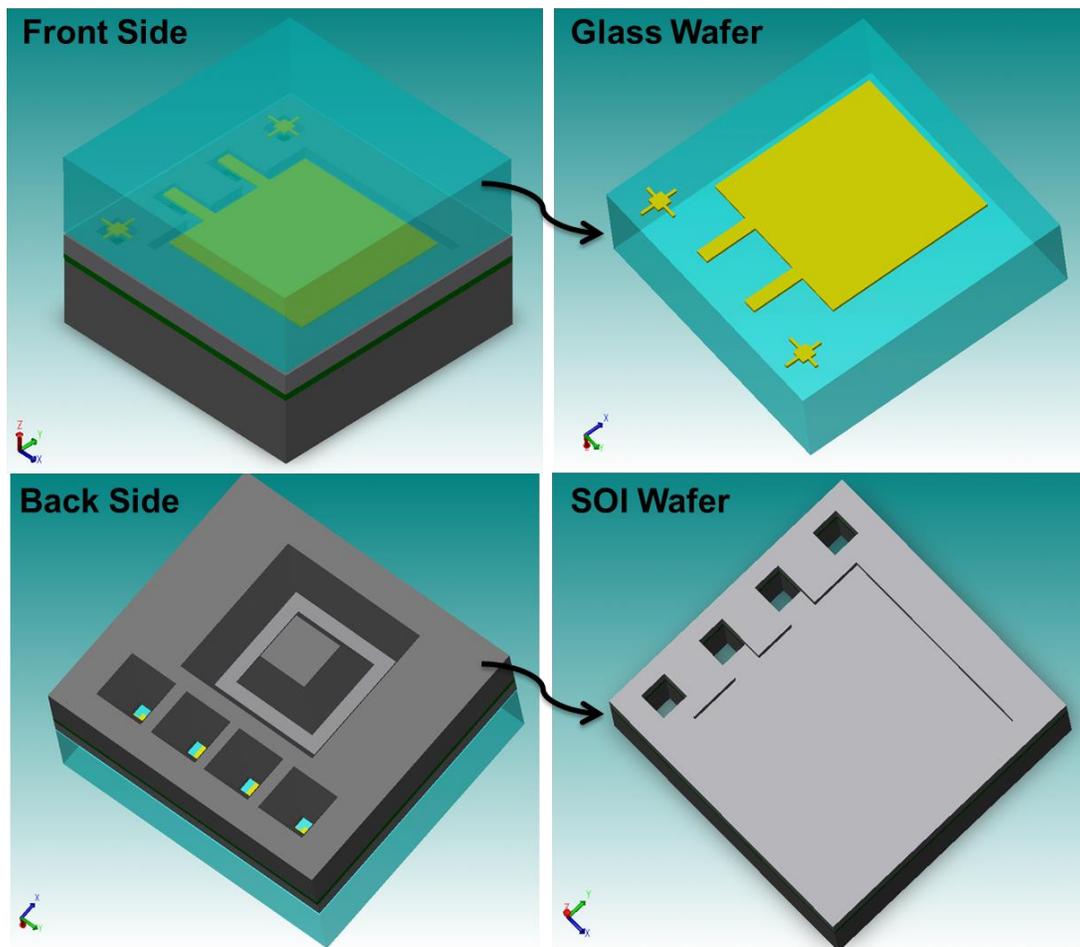


Figure 4.1 - Schematic of out-of-plane accelerometer die based on SPP

The wet etching process includes five masks. The mask layouts for a single die, including Dimples, Contacts, Cavity, Top Electrode, and Backside, are shown in Figure 4.2. The die size is 10 mm × 10 mm. The Top Electrode mask is used for top fixed electrode metal patterning on the glass wafer. The Dimples, Cavity, and Contacts masks were used for processes on the device layer of the SOI wafer. The Backside mask was used for carving the proof mass out-of-handle layer of the SOI wafer.

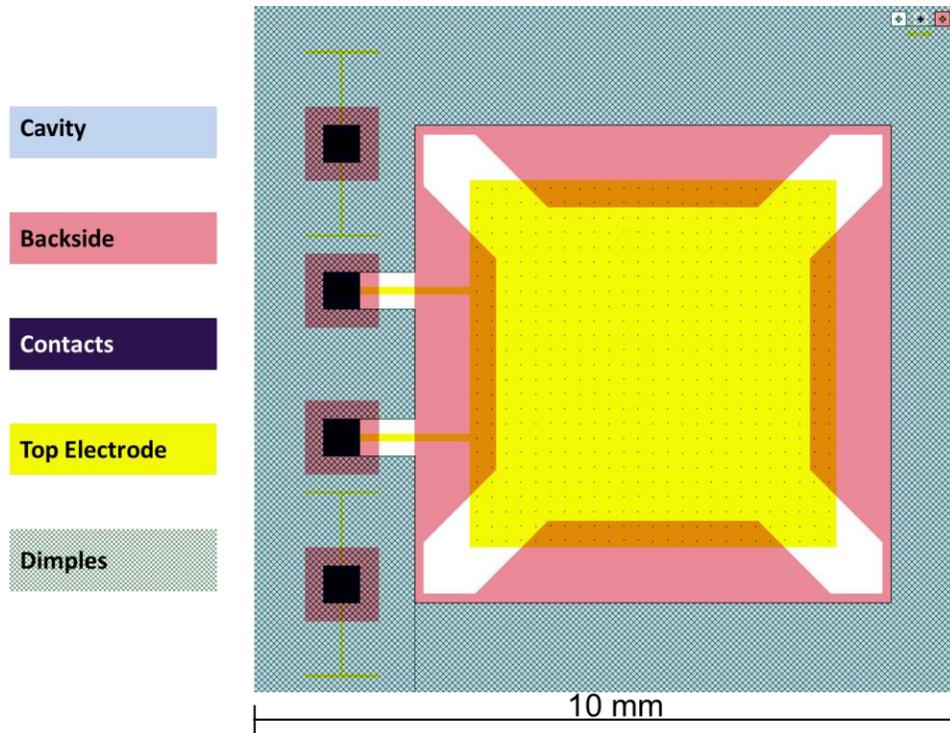


Figure 4.2 - Masks layout for a single die of the out-of-plane accelerometer based on SPP

The first processing step included depositing metal on glass wafer as the fixed top electrode. The starting material was a 4-inch Borofloat® 33 wafer with a thickness of 300µm. Table 4.1 summarizes the specifications of the used glass wafer:

Table 4.1- Specification of the Borosilicate wafer provided by the manufacturer company [68]

Diameter [mm]	Material	Thickness [µm]	Expansion coefficient (CTE)	Log electr. resistance	volume
100	Borofloat® 33	300	$3.25 \times 10^{-6} K^{-1}$ (adapted to Si)	(250°C): 8.0 Ωcm (350°C): 6.5 Ωcm	

As shown in Figure 4.3, by using the lift-off process [69], a 50 nm layer of Titanium, a 50 nm layer of Platinum and a 200 nm layer of gold were deposited on the desirable areas of the glass wafer. The combination and thicknesses of the deposited metals were based on [70]. The deposition was performed using the physical vapor deposition equipment at SFU's 4D Labs [71].

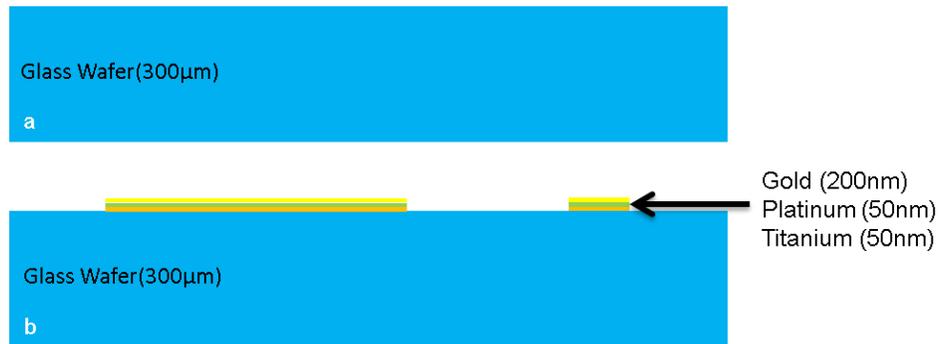


Figure 4.3 - Lift-off process on the glass wafer for depositing electrodes in SPP

Figure 4.4 - a shows the Top Electrode mask layout for metal deposition. The “Fixed Electrode”, as indexed in Figure 4.4 - a, is located on top of the cavity on the SOI wafer and forms the top electrode. After bonding the glass and SOI wafer, the area marked as “Contacts to Membrane” in Figure 4.4 - a, would get in contact with the device layer of the SOI wafer, which would form the bottom moving electrode. Figure 4.4.b shows the final glass wafer after metal deposition. At this stage, the glass wafer was ready for anodic bonding. Hence, the next step included the processing on the SOI wafer and its preparation for anodic bonding.

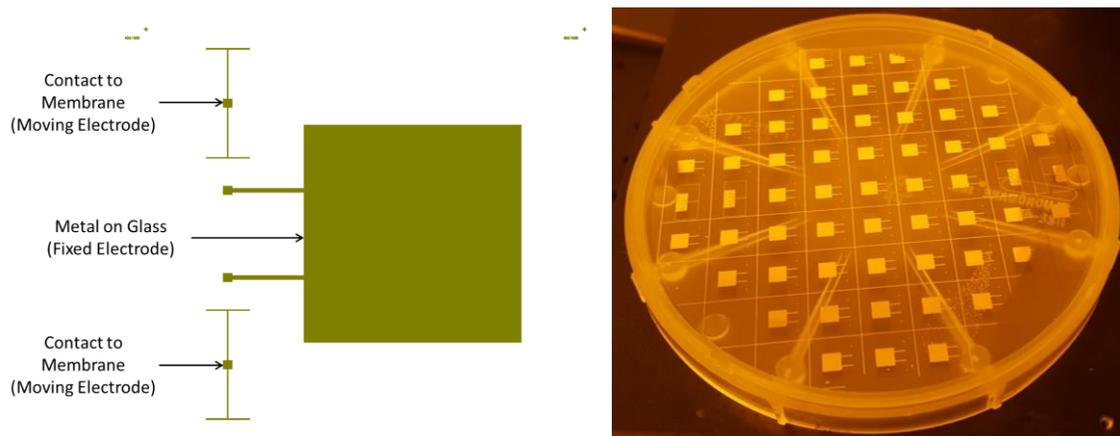


Figure 4.4 - a) A single die electrode mask for out-of-plane accelerometer in SPP, b) Glass wafer after metal deposition which acts as fixed electrode

The next fabrication step included the processes on the SOI wafer. The term SOI refers to a three-layer material stack which comprises a top layer of prime quality single crystal silicon (Device Layer) on an electrically insulating silicon dioxide layer (Buried Oxide, BOX), and a substrate bulk silicon wafer (Handle wafer).

The starting SOI wafer was a (100)-oriented 4" SOI wafer with an 8 μ m thick silicon layer, 1.5 μ m buried oxide (BOX), and 500 μ m thick silicon wafer. Table 4.2 summarizes the specifications of the used SOI wafer:

Table 4.2 - Specifications of the SOI wafer provided by the manufacturer for fabrication of out-of-plane accelerometer in SPP

Diameter [mm]	Type-orientation	Device thickness [μ m]	Device resistivity [Ω -cm]	Handles thickness [μ m]	Handle resistivity [Ω -cm]	Box thickness [μ m]
100	P/B-(100)	8 \pm 1	0.005-0.020	500 \pm 10	0.005-0.020	1.5 \pm 5%

At the beginning of the process, 400nm of SiO₂ and 120 nm of Si₃N₄ were deposited as the KOH (Potassium Hydroxide) etching masking layers on the backside of the SOI wafer, i.e., the handle wafer, using thermal oxidation and PECVD, respectively. Figure 4.5 illustrates the cross-sectional view of the processing steps on the SOI wafer before the anodic bonding process.

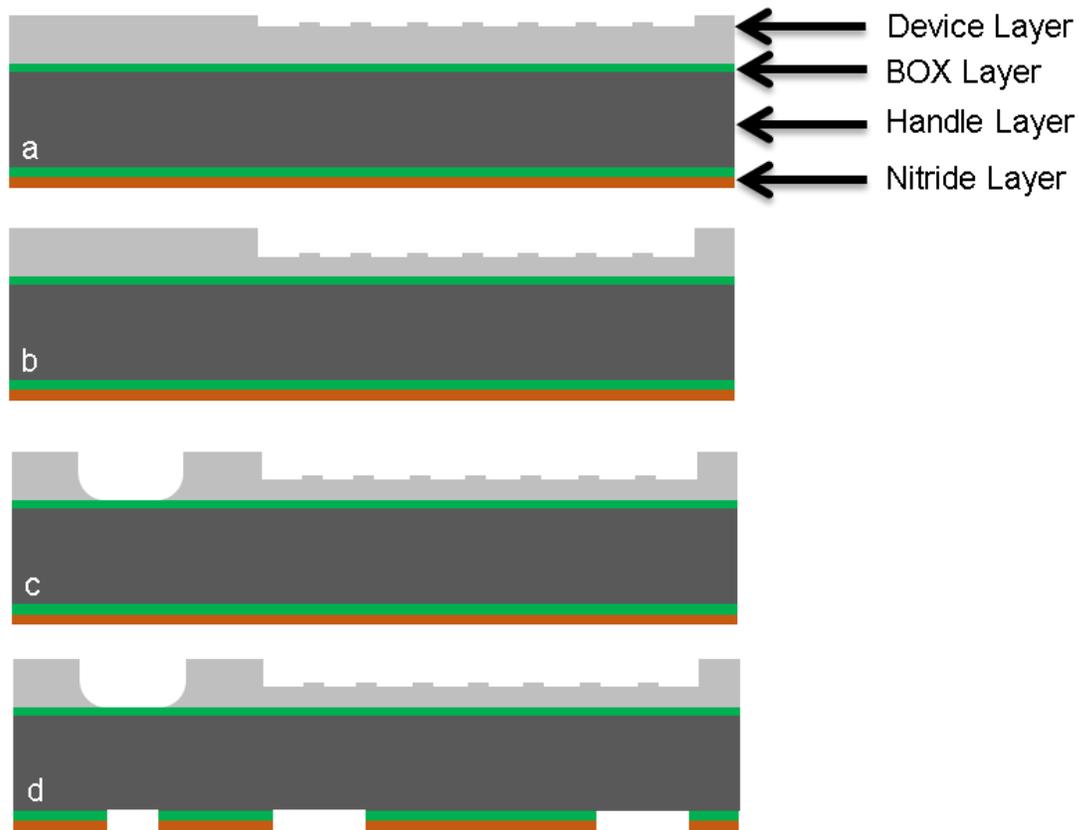


Figure 4.5 - SOI wafer process steps for out-of-plane accelerometer in SPP which includes a) etching the dimples on device layer, b) etching the cavity on device layer, c) etching contacts on device layer, and d) etching proof mass mask on the deposited nitride and oxide on handle wafer

According to Figure 4.5, an array of tiny squares ($5\ \mu\text{m} \times 5\ \mu\text{m}$) was initially dry-etched on the device layer of the SOI wafer using Reactive Ion Etching (RIE) [72]. These structures, also known as dimples, were etched to avoid stiction between the top electrode and the membrane. The height of the dimples, i.e. the depth of the etch, was 150nm. Figure 4.6 shows part of the device layer after the RIE etching of the dimples.

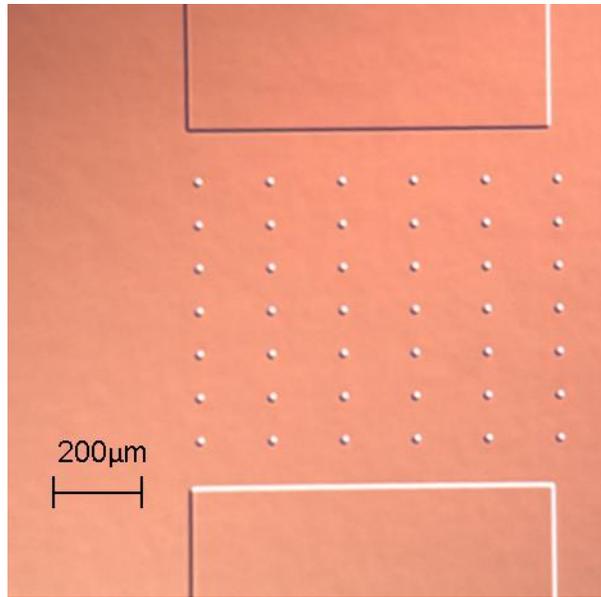


Figure 4.6 - Dimples etched on the device layer of the out-of-plane accelerometer in SSP

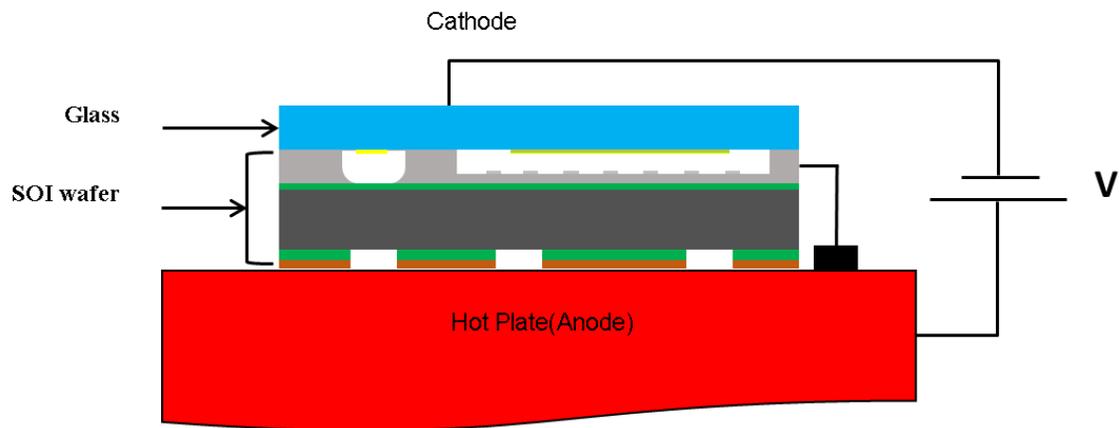
Following the dimples etching, the cavity was etched with a depth of 800nm on the device layer using a “Cavity” mask. The depth of this cavity formed the capacitive sensing gap between the top fixed electrode, which was on the glass, and the bottom moving electrode, which was the membrane.

The third processing step on the SOI wafer was etching the contacts on the device layer up to the BOX layer. The contacts were used for accessing the electrodes on the glass wafer. Later on, contacts would be etched on the handle wafer as well as the BOX layer, which consequently made a through hole in the SOI wafer. The contacts were etched using XeF_2 , which is a dry, isotropic and vapor-phase silicon etchant.

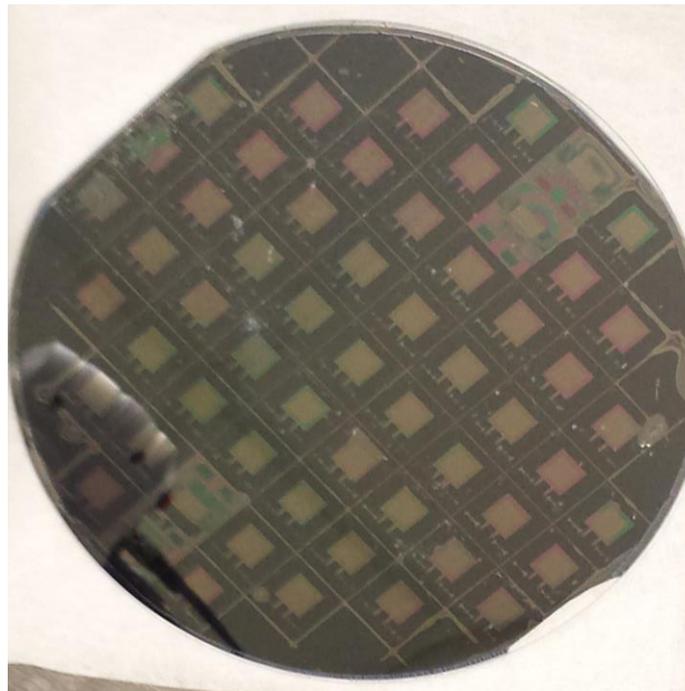
The final processing step on the SOI wafer was etching the handle wafer’s nitride and oxide layers using the Backside mask. These layers would be used later as KOH etching hard mask. The nitride and oxide layers were etched using RIE and HF etching, respectively. Upon finishing this step, the SOI wafer was ready for anodic bonding.

Anodic bonding is a wafer bonding technique used to create hermetic sealing within a silicon and glass wafer [73]. In our case, the standard cleaning process was initially performed to remove organics and particles from the surface of the glass and SOI wafer. The two wafers were subsequently aligned using the mask aligner. Then, using the developed setup at the ENSC clean room, the anodic bonding process was performed at 400°C with an applied voltage of about 700 volts. The schematic of the

anodic bonding setup and the anodically bonded wafers are shown in Figure 4.7.a and Figure 4.7.b.



(a)



(b)

Figure 4.7 – a) Schematic of the anodic bonding setup for bonding glass and SOI wafer, b) Anodically bonded glass and SOI wafer from glass side

After bonding the glass and silicon wafer, the final steps included the processes on the unified wafer. As shown in Figure 4.8, these sets of processes included KOH etching of the handle wafer for carving out the proof mass and contact holes, as well as etching the BOX layer to make the through holes and get access to electrodes on the glass wafer.

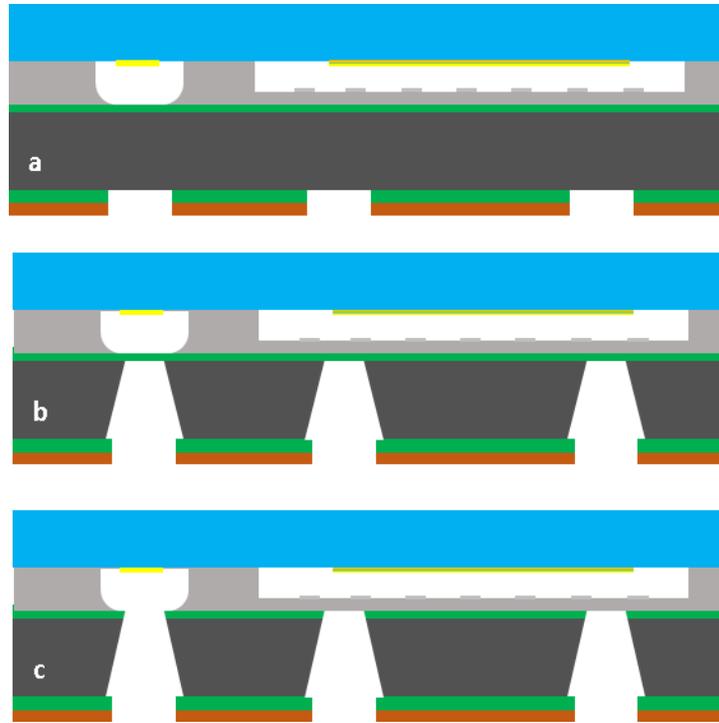


Figure 4.8 – The process flow on the anodically bonded wafer in SPP, a) anodically bonded glass and silicon wafers, b) KOH etching of the handle wafer, and c) HF etching of the BOX layer

After anodically bonding the silicon and glass wafers, the proof mass and the contact holes were etched from the handle wafer using KOH etching. KOH etching is a wet anisotropic etching process. The KOH etch rate of silicon depends on the crystallographic directions of the silicon wafer. Therefore, one of the issues encountered in carving the proof mass from the handle wafer was the convex corner undercutting. In the wet etching process of the out-of-plane accelerometer, since the handle wafer is thick, i.e. 500 μm , the convex corner undercutting causes a remarkable part of the proof mass to be etched. Subsequently, it would affect the MNEA. In order to address this issue, a corner compensation structure was added to the corners of the square proof mass layout as shown in Figure 4.2, Backside mask. Adding the corner compensation structures to the corners of the proof mass resulted in losing less mass during the proof mass etching. The procedure for designing the corner compensation was mainly performed based on the experimental results of [74]. To perform KOH etching, the unified wafer was fitted into a Teflon wafer chuck [75] for protecting the sides and backside of the wafer. It was then put into a 33% KOH solution at 80°C. The unified wafer inside the wafer chuck after 264 μm of etching is shown in Figure 4.9. Finally, the handle wafer was etched entirely, and etching was stopped at the BOX layer.



Figure 4.9 – Anodically bonded silicon and glass wafer inside the Teflon wafer chuck, the handle wafer was etched to the depth $264\mu\text{m}$

After etching the handle wafer, the final stage is etching the BOX layer using vapor HF etching (VHF) [76]. The main reason for removing the BOX layer was to make a through hole to get access to the top fixed electrode. Figure 4.10 shows contact holes from the backside of the unified wafer before and after the vapor HF etching. The wrinkled area in the picture is the BOX layer. One of the issues with this step of the process was the growing of cracks in the oxide layer. Cracks caused vapor HF to leak to the underneath cavity and attack the glass and gold layers.

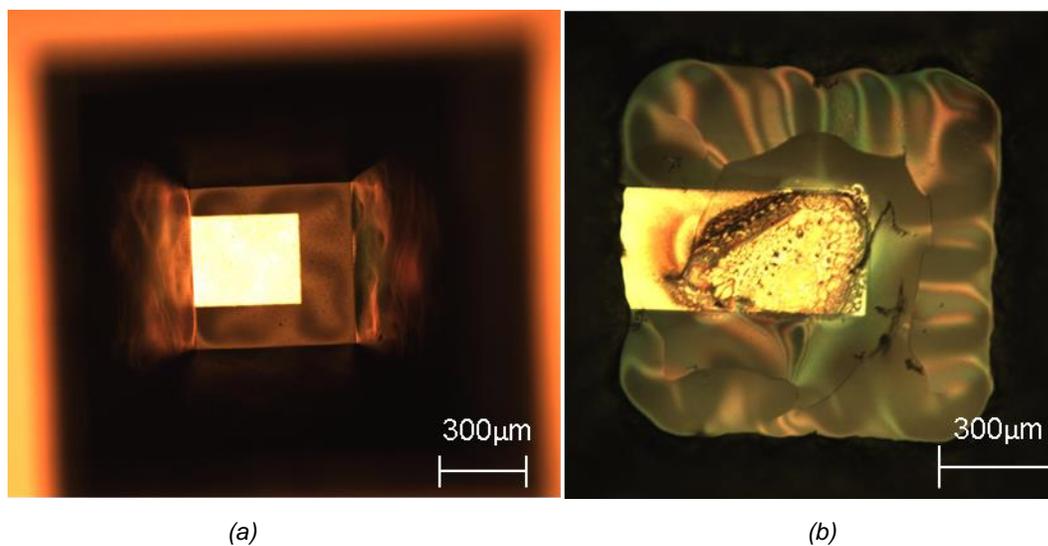


Figure 4.10 – Contacts to top fixed electrode imaged from backside of SOI wafer, the wrinkles are oxide layer a) before HF etching, and b) after HF etching, the gold was attacked by HF leakage from the cracks in the oxide layer

After removing the BOX layer, the chips were ready for on-wafer functionality test. Upon being approved by the initial functionality test, the working dies could have been diced, packaged and wire-bonded. However, the wet etching process for the fabrication of the out-of-plane accelerometers ran into various problems leading to non-functional devices. The primary issue with SPP was due to the KOH wet etching process. The wet etching process was highly dependent on various parameters such as the solution concentration and temperature, making it difficult to control the process. Moreover, as the membrane thinned out, even before the etch solution reached the BOX layer, the membranes broke. As a result, the KOH solution leaked to the device layer side of the wafer, and damaged the proof masses. Figure 4.11 - a demonstrates the whole wafer and Figure 4.11 - b shows one of the cracked corners of the membrane. The corner compensation structure is also visible in this picture.

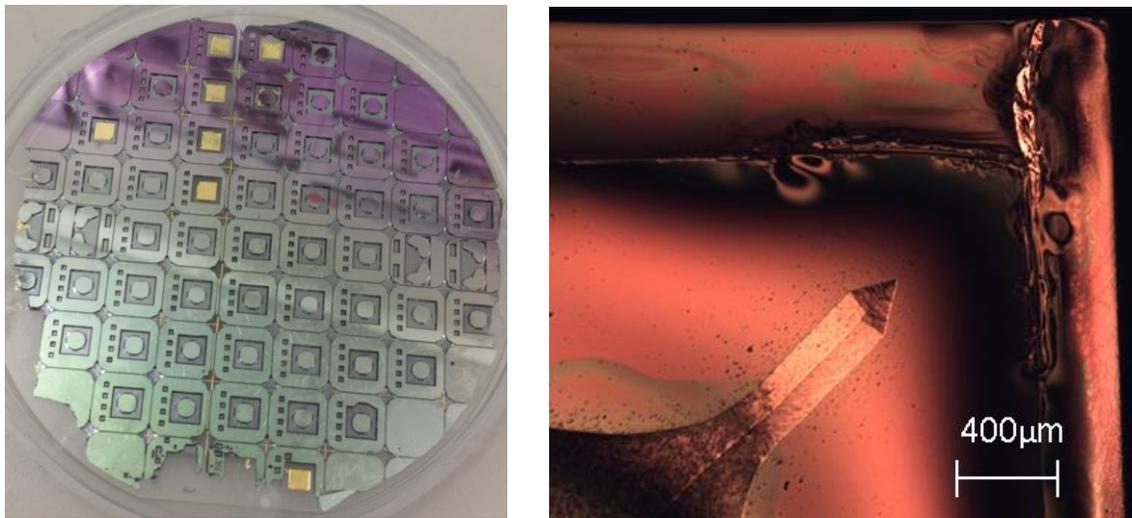


Figure 4.11 - a) The whole wafer after KOH etching. Some of the proof masses was went off, and the whole wafer was rendered useless, and b) part of a cracked die

It was also observed that part of the membrane got stuck to the top glass electrode on the broken membrane chips. This was almost visible in Figure 4.11 - b as well. Based on such observations as well as cracks in the membrane, it was concluded that performing anodic bonding at high temperatures (400 °C) and then bringing the wafer back to the standard temperature (20 °C) could have caused these issues. As the temperature decreased, the pressure of the closed cavity between the top electrode and the membrane became less than its surrounding pressure. Therefore, the membrane

broke as it thinned out due to the pressure difference. To solve this issue, it was proposed to connect the closed cavity to the atmosphere through some vent channels. Meanwhile, to reduce the number of processes on the SOI wafer, the cavity was moved to the glass wafer instead of the device layer. The etch depth was also increased. Finally, to achieve a less environment-dependent process for the proof mass etching, the wet etching of the proof mass was replaced with Deep Reactive Ion Etching (DRIE). By the transition to DRIE which reduced stress concentration across the membrane, the membrane changed to an annular shape. Applying all of the above modifications, a new process was developed based on the dry etching of the circular proof mass. This process is explained in more details in the next section.

4.1.2. Circular Proof Mass Process (CPP)

Similar to the wet etching process, the fabrication process of the out-of-plane accelerometer using dry etching comprised three major steps on the SOI wafer, glass wafer, and the anodically bonded SOI and glass wafer. Each step consists of a few sub-steps which are explained in detail in this section. Figure 4.12 shows a schematic of an out-of-plane accelerometer die based on dry the etching process. As observed in Figure 4.12, the cavity was etched on the glass wafer and a vent channel was implemented besides the cavity for pressure adjustment.

Similar to the SPP, CPP is a five-mask process which includes Dimples, Contacts, Cavity, Top Electrode, and Backside masks. The first major step for the fabrication of the out-of-plane accelerometer in CPP included the process performed on glass wafer. Figure 4.13 illustrates this process flow. This major step was developed by Bahareh Yaghootkar at ENSC cleanroom and 4D labs.

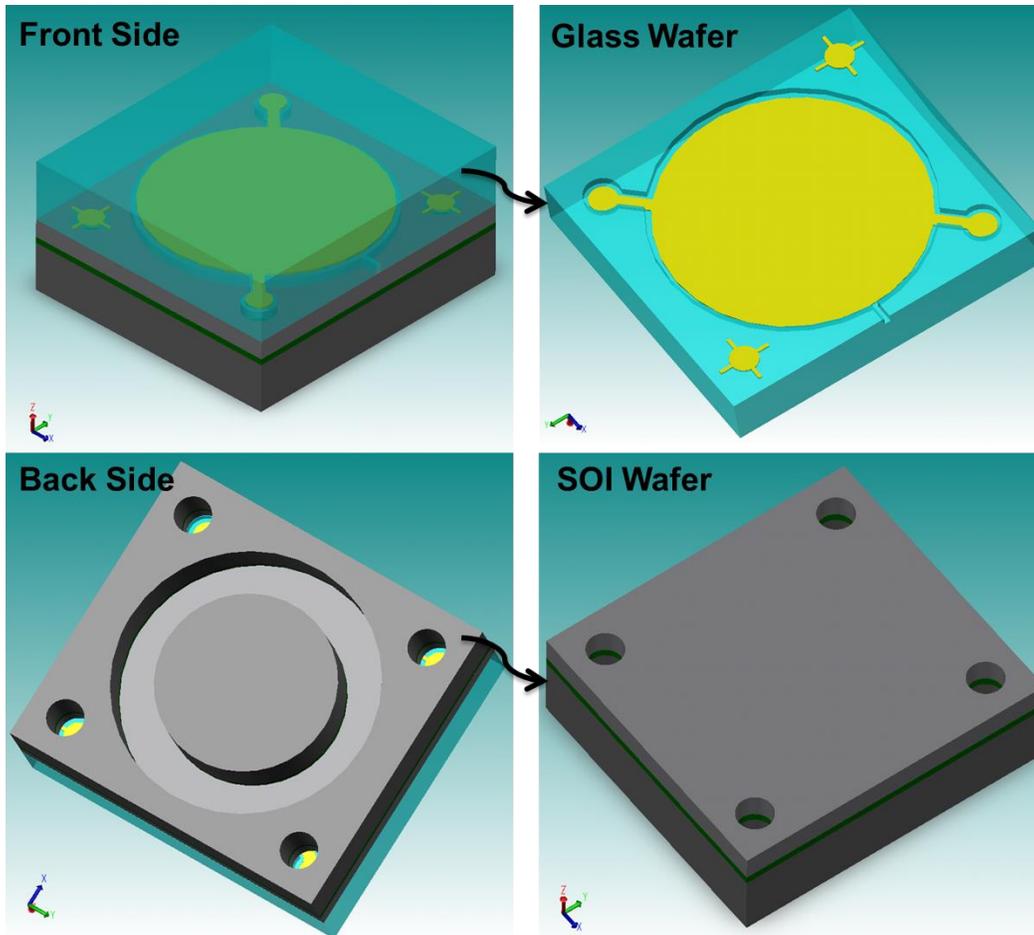


Figure 4.12 - Schematic of out-of-plane accelerometer die based on CPP

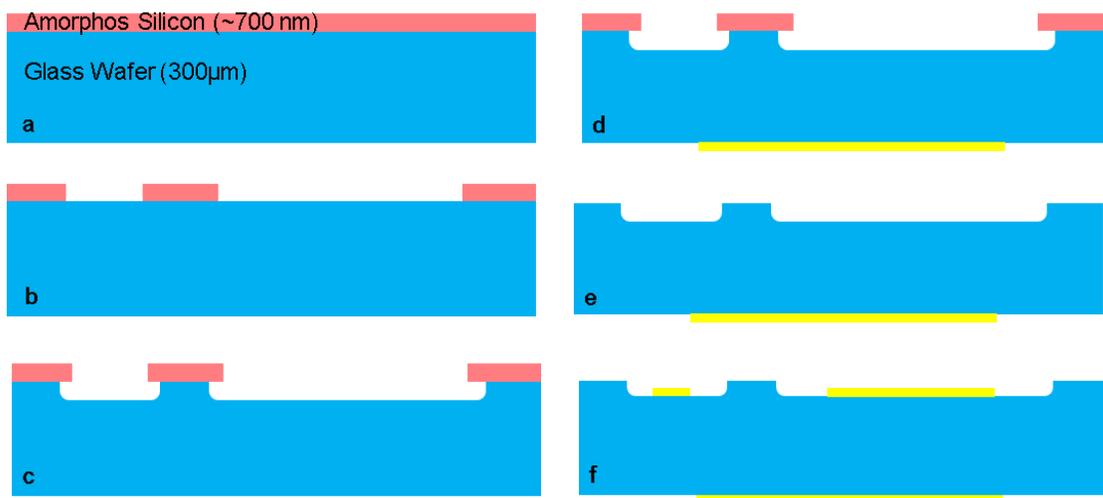


Figure 4.13 – Fabrication process on the glass wafer for out-of-plane accelerometer in CPP, a) deposition a layer of amorphous silicon as a hard mask, b) etching the hard mask using RIE, c) etching cavities on glass wafer, d) deposition of backside metal for die attachment, e) etching the a-Si layer, and f) top fixed electrode metal deposition on the cavity side of the glass wafer

The process started with a 4-inch Borofloat® 33 wafer with a thickness of 300µm with the properties summarized in Table 4-1. To etch the glass wafer in VHF, it was required to deposit a masking layer on the glass wafer which was resistant to HF. In the first step, a ~700 nm layer of amorphous Silicon (a-Si) was deposited as the masking layer on the glass wafer using the PECVD machine. Subsequently, the a-Si layer was patterned using the Cavity mask, as shown in Figure 4.14. The vent channels can be seen on the Cavity mask. The channels connect the cavity to the edges of the wafer which is at atmospheric pressure. After etching the hard mask using RIE, the glass wafer was put into the VHF chamber for vapor HF etching of the openings on the glass wafer to a depth of ~5µm.

The next step was the deposition of a stacked layer of Titanium (20nm), Platinum (20nm), and Gold (150nm) on the backside of the wafer using a lift-off process. The purpose of depositing the backside gold was for soldering the die to the carrier package later in the packaging process. The packaging and die attachment process is explained in more details in the last section of this chapter.

The last step in the glass wafer processing was depositing a metal layer inside the glass cavities. To that end, the a-Si hard mask was initially removed using KOH etching. Afterwards, a stacked layer of Titanium (20nm), Platinum (20nm), and Gold (150nm) was deposited on the glass wafer using physical vapor deposition. This layer, which would act as the top fixed electrode, was patterned using an “Electrode” mask shown in Figure 4.14.a. The reason for dividing the top electrode mask to an annular and a circular electrode instead of an integrated circular one was to enable the use of one of the electrodes for sensing and the other for feedback controlling.

Upon performing all of the above processes, the final glass wafer as shown in Figure 4.14-b, would be ready for anodic bonding to SOI wafer.

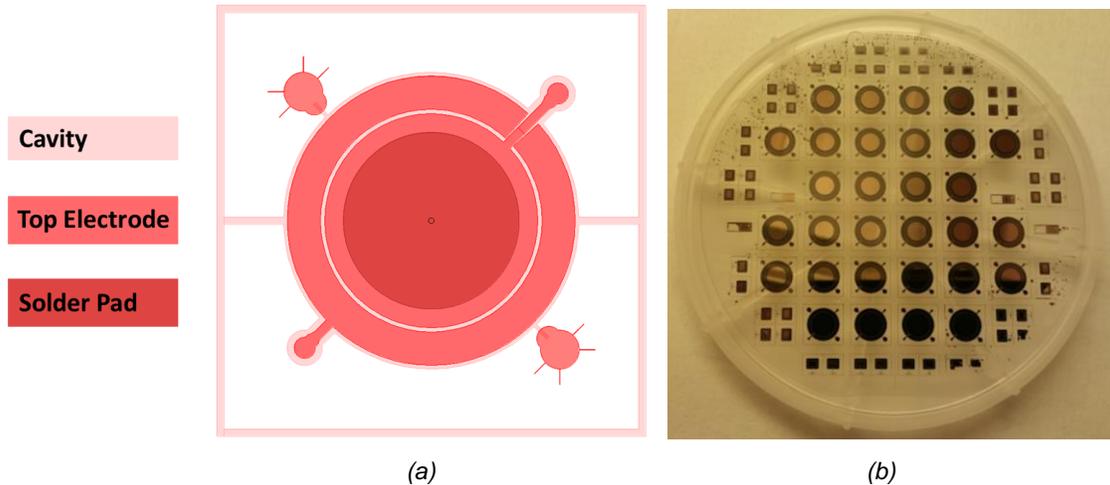


Figure 4.14 – a) Cavity, Top Electrode, and Solder Pad masks layout for a single die of the out-of-plane accelerometer in CPP, b) Glass wafer from backside after metal deposition which acts as the fixed electrode

After processing the glass wafer, the next major step included the processes on the SOI wafer. The specifications of the starting SOI wafer are summarized in Table 4-2.

Figure 4.15 illustrates the two-step process flow on the SOI wafer. In the first processing step on the SOI wafer, the array of dimples which constitute $5\mu\text{m} \times 5\mu\text{m}$ squares, were dry etched on the device layer for a depth of 100 nm. As mentioned in the previous section, the dimples were implemented on the device layer in order to avoid stiction between the top and bottom electrodes, i.e., the membrane. Figure 4.16 shows dimples etched on the membrane. After etching the dimples, the next step was etching the contact holes on the device layer. Later on, the contact holes would be etched from the handle wafer as well. Therefore, they make through-silicon holes to access the glass wafer electrodes. Etching of the contacts was performed using XeF_2 etching which is an isotropic silicon etchant. At this stage, the SOI wafer was ready for anodically bonding to the glass wafer.



Figure 4.15 – Fabrication process flow on SOI wafer for the out-of-plane accelerometer in CPP, a) etching the dimples on the device layer, b) etching contact holes on the device layer

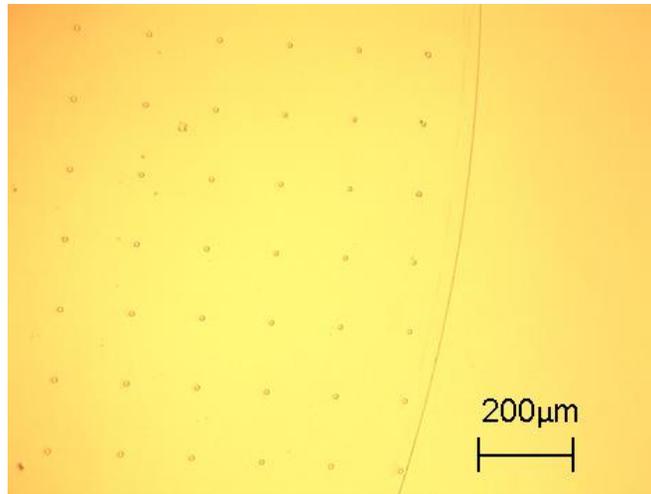


Figure 4.16 - Dimples etched on the device layer of out-of-plane accelerometer in CPP

The last major steps included the glass and the silicon wafer anodic bonding, carving out the proof mass from the handle wafer of the SOI wafer, and etching the BOX layer. The process flow for this major step is presented in Figure 4.17.

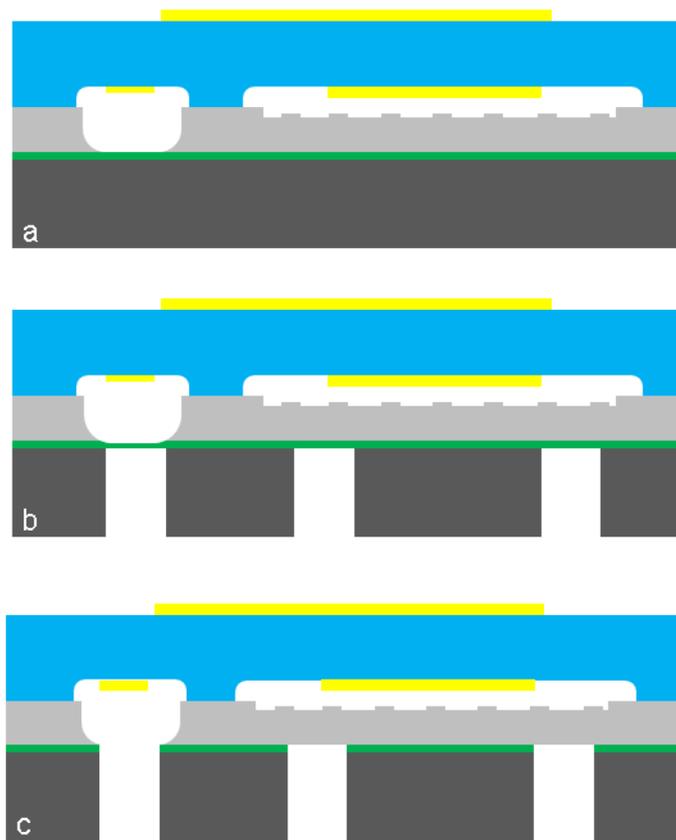


Figure 4.17- The process flow on the anodically bonded wafer for the dry etching process of the out-of-plane accelerometers, a) anodically bonding glass and silicon wafers, b) DRIE of the handle wafer, and c) HF etching of the BOX layer

As illustrated in Figure 4.17, after bonding the processed glass and SOI wafer, the handle wafer of the SOI wafer was etched using DRIE. Following this step, the BOX layer was etched using VHF etching. However, in most of the chips, the BOX layer broke, and the VHF etching was not required anymore. Figure 4.18.a shows the unified wafer after DRIE and Figure 4.18–b shows SEM image of one of the contact holes from the backside. In this figure, the edges of the BOX layer and the electrode on the glass wafer are distinguishable. At this stage, the wafer was ready for dicing and packaging. In the last section of this chapter, a summary of the packaging process is explained and the pictures of the final packaged devices are presented.

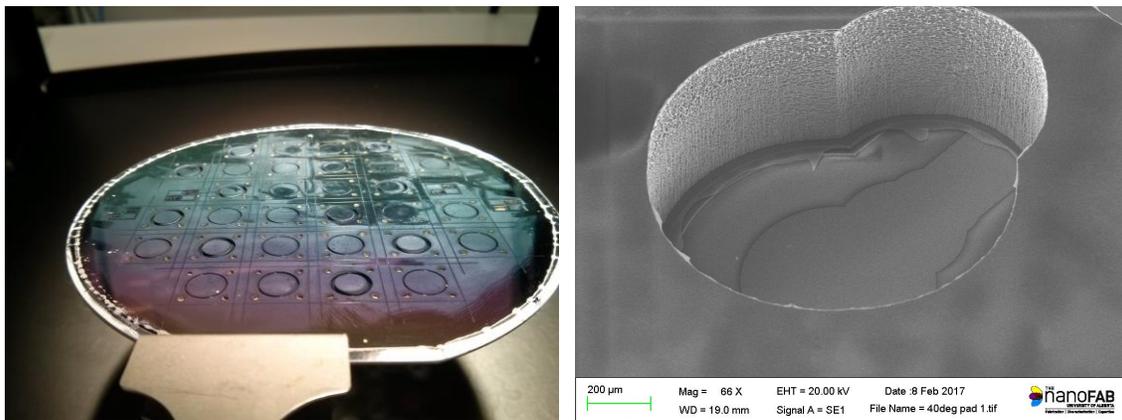


Figure 4.18 – a) out-of-plane accelerometer dry etching process unified wafer at the final step, and b) SEM image from one of the contact holes

4.2. In-Plane Accelerometer Fabrication Process

The proposed in-plane accelerometers were fabricated using bulk micromachining technology. A P-type (100) Silicon-On-Insulator (SOI) wafer was used as the starting material for fabrication. The SOI wafer included a 100 µm device wafer, a 5µm buried oxide layer (BOX layer), and a 500 µm handle wafer. Figure 4.19 shows the fabrication process flow of the accelerometer. The fabrication was a three-mask process which included two lithography steps and a shadow mask. In the first step, lithography was performed to define the metal contact pads. Following that, 20 nm of Chromium and 200 nm of Gold were deposited on the device layer of the SOI wafer using the physical vapor deposition technique. Subsequently, the metal contacts on the wafer were realized using a lift-off process. In the next step, 20 nm of Chromium and 200 nm of Gold were deposited on the handle layer of the SOI wafer using shadow mask and physical vapor

deposition. This layer would be used later for soldering the MEMS device dies to the carrier package. Later on, a 2.2 μm layer of SiO_2 was deposited on the device layer by chemical vapor deposition. This layer, along with a thick layer of photoresist, would be used as the hard mask for Deep Reactive Ion Etching (DRIE). Upon etching of the masking layer using HF, the device layer was etched by DRIE. The wafer was then diced using the Stealth Laser Dicing technology [77] followed by an examination of the individual dices. Finally, the structure was released by etching the buried oxide (BOX) layer using vapor HF etching. The released device was then individually packaged in the leadless chip carrier and wire bonded as explained in more detail in the last section of this chapter.

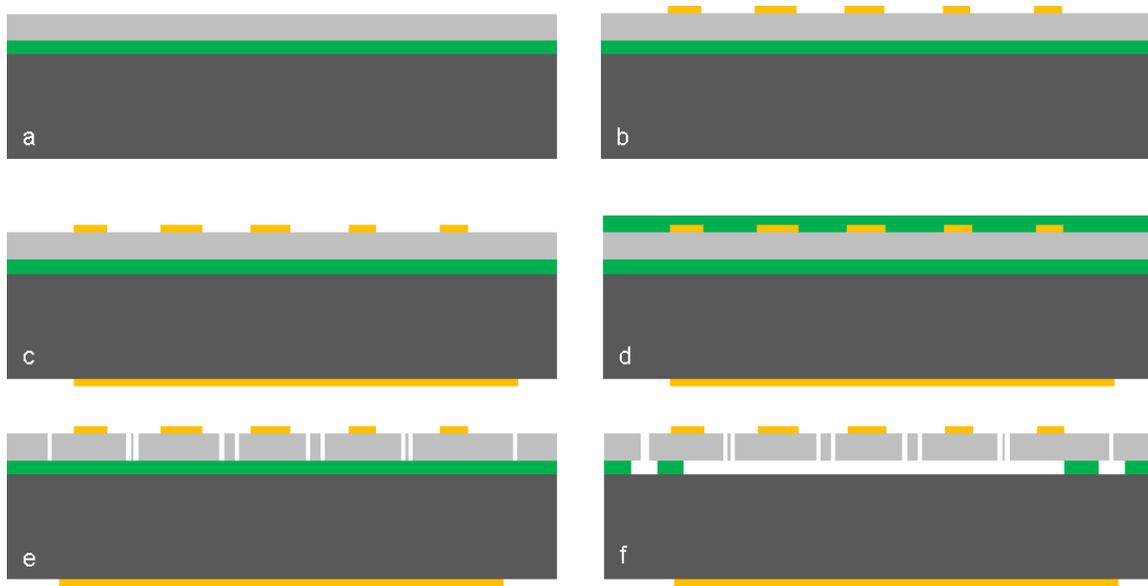


Figure 4.19 - Fabrication process flow of the in-plane accelerometer, a) starting material is an SOI wafer with 100 μm device layer, 5 μm BOX layer, and 500 μm handle wafer, b) metal deposition using lift-off process on device layer, c) metal deposition on handle wafer using shadow mask, d) PECVD of SiO_2 on device layer as the masking layer for RIE, e) HF etching of the oxide layer and DRIE of the device layer, and f) Release structures using vapor HF.

To fabricate the devices using the proposed fabrication process, several rounds of fabrication were performed. Due to the lack of Deep Reaction Ion Etching (DRIE) equipment at SFU facilities, the dry etching process was outsourced elsewhere. The first facility where the wafers were sent out for performing DRIE was Sherbrook University. Due to the lack of an optimized process at Sherbrook University, several issues were raised during the DRIE process which impeded the devices from working properly. Some examples of the problems during the first round of fabrication is summarized in Appendix

B. Upon unsuccessful process of the DRIE process at University of Sherbrook, the DRIE step was outsourced to Lurie Nanofabrication Facilities at the University of Michigan for the next round of fabrications. According to Chapter 3, the in-plane accelerometers prototype I needed a low aspect ratio etching and was designed for the verification of the fabrication capabilities. The etching aspect ratio of prototype I accelerometers was 20, i.e., etching a $5\mu\text{m}$ gap in the $100\mu\text{m}$ thickness of the silicon. A picture from the wafer after depositing the metal contacts and a picture from the die after DRIE are shown in Figure 4.20-a and b, respectively. Upon the successful etching of the wafer, the devices were diced, packaged and wire bonded. A short description of the packaging process is explained in the next section.

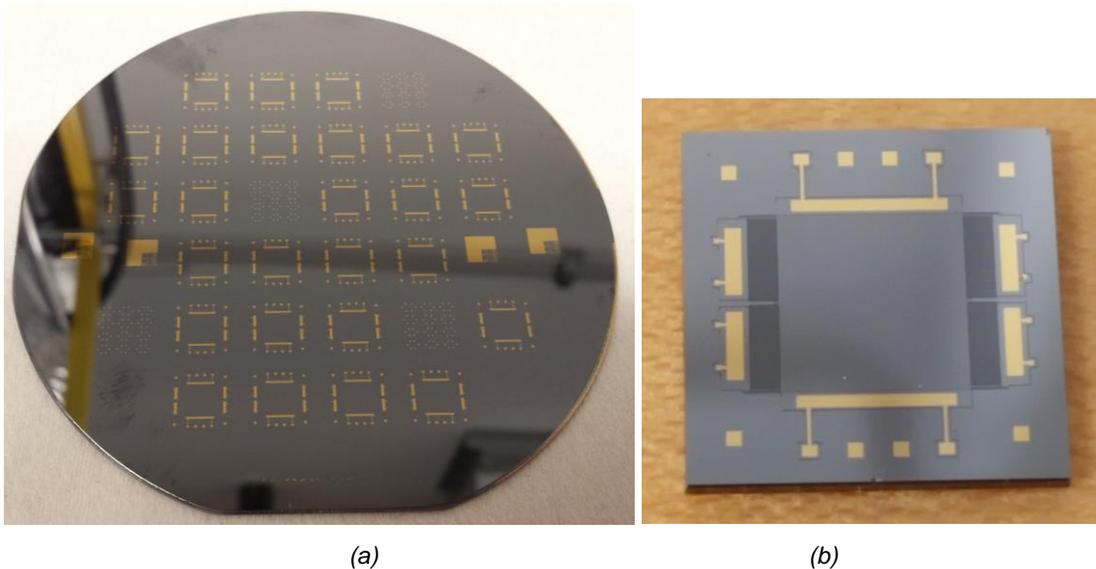


Figure 4.20 – a) SOI wafer after deposition of metal contacts for in-plane accelerometer prototype #1, b) one of the dies after DRIE, the die is 10 mm by 10 mm

The second prototype of the in-plane accelerometers was fabricated using the same general fabrication procedure. The difference between the first and second fabrication processes was in the aspect ratio of the etching. The aspect ratio in the in-plane accelerometer prototype II was 50, i.e., etching $2\mu\text{m}$ in $100\mu\text{m}$ thickness of the silicon. The recipe for the deep etching of the silicon was the advanced DRIE with ramped process parameters [78]. This process, which had been developed at the University of Michigan, improved the achievable aspect ratio and reduced Aspect Ratio Dependent Etching (ARDE) [79]. Figure 4.21 shows the final processed wafer before dicing.

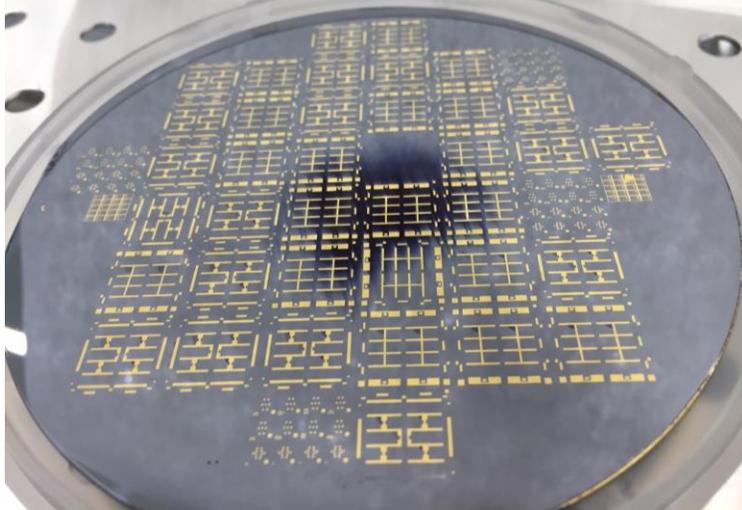
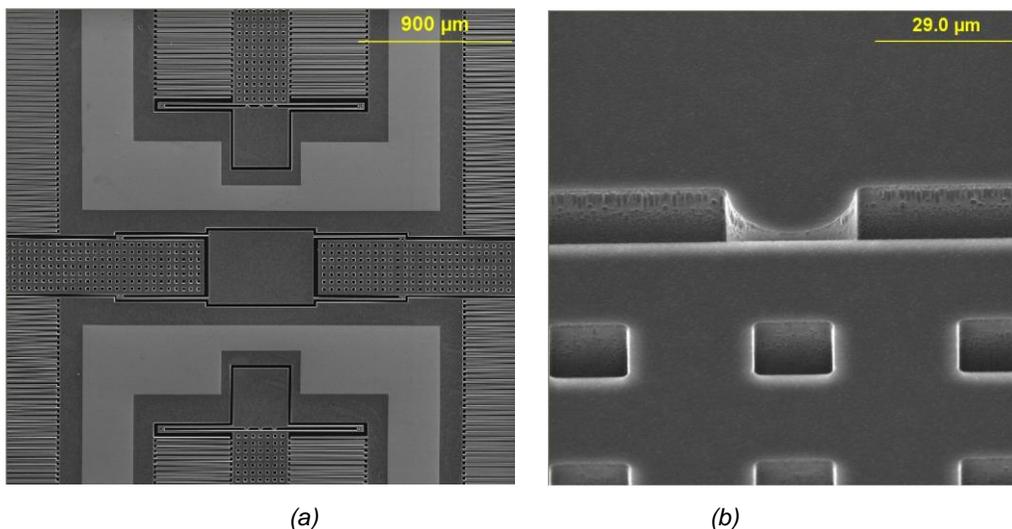


Figure 4.21- In-plane accelerometer prototype #2; the final processed wafer

The SEM pictures of one of the final dies are shown in Figure 4.22. Figure 4.22-a shows an SEM image from the central part of the prototype II, Design B. In this picture, part of the comb fingers, moving frame, internal anchors, and elastic elements can be seen. Figure 4.22-b is an SEM image of a shock stop. The etch holes are also visible in this picture. Figure 4.22-c is a top view of the comb fingers where part of the moving frame is also visible. Figure 4.22-d is the SEM image of the comb fingers where the comb width and the gap between fingers are shown. Figure 4.22-e shows the SEM image of the cross-section of the comb fingers. By comparing Figure 4.22-c and Figure 4.22-e, it can be seen that the aspect ratio of 50 was achieved. Finally, in Figure 4.22-f, which is the enlarged SEM image of the cross-section of the comb fingers, the device layer, BOX layer, and handle wafer are distinguishable.



(a)

(b)

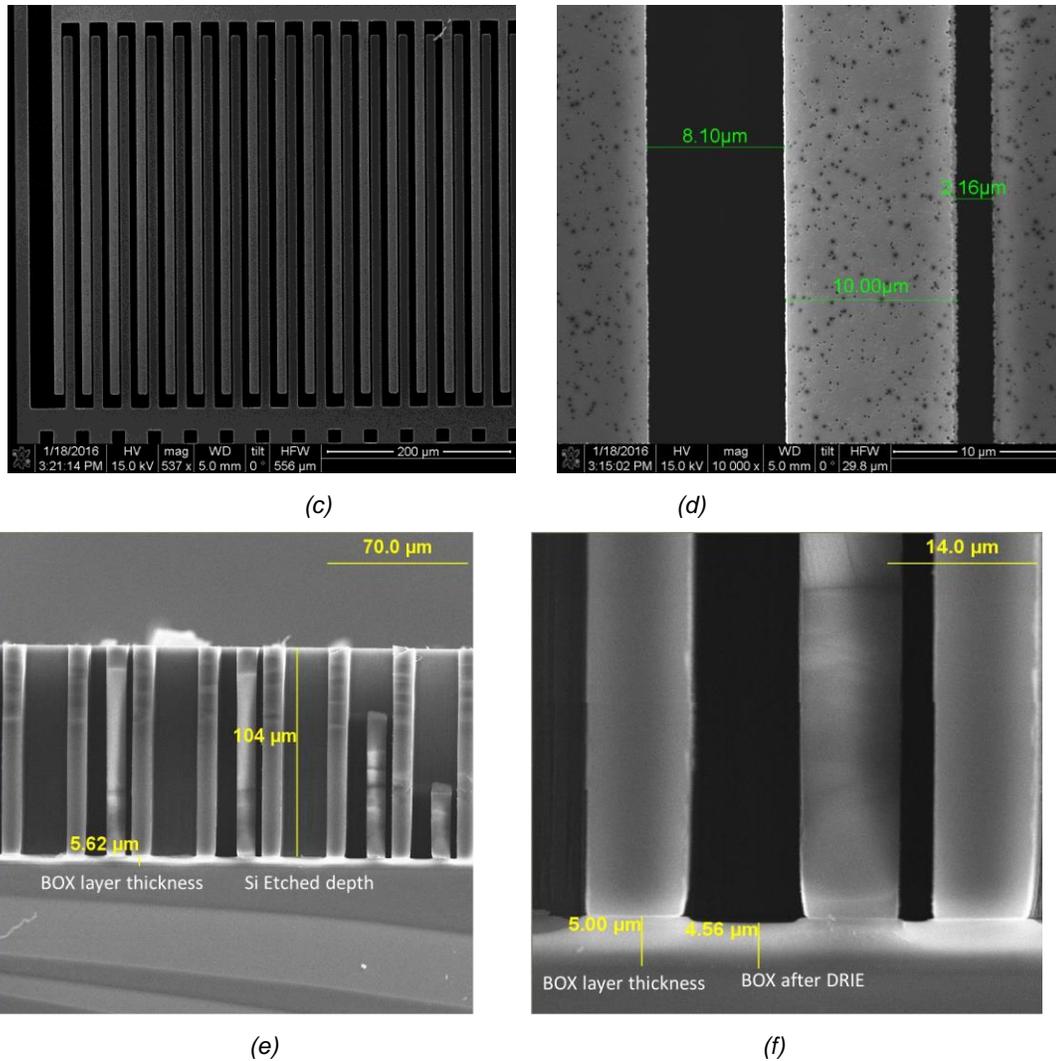


Figure 4.22 – High aspect ratio comb fingers using UDRIE (Ultra High Aspect-Ratio And Thick Deep Silicon Etching) process, a) SEM image of the comb fingers, moving frame, internal anchors and elastic elements, b) shock stop, c) comb fingers, top view, d) SEM image of comb fingers top view, e) SEM image of the cross-section of the comb fingers, f) enlarged SEM image of the cross-section of the comb fingers

Although the high aspect ratio DRIE process delivered proper results in terms of right-angled side walls, the yield of the fabrication process was drastically low. In the first fabrication run, various defects were identified which had destroyed the functionality of the devices. The identified defects had different sources including particles on the wafer at different steps such as lithography and etching, undeveloped areas, broken fingers due to shock application, and voids in SOI wafer. A summary of these incidents and their characterization are shown in Appendix B. Upon the investigations performed on the received processed wafers from LNF facilities and the feedbacks conveyed by them, the quantity of the defects were decreased in the next run. However, because the combs formed a considerable area of the wafer in prototype II, even one defect could affect the

functionality of the whole device. This fact affected the fabrication yield drastically. Therefore, the third in-plane prototype was designed and fabricated with the aim of decreasing the area of the comb fingers. The fabrication process was exactly similar to the process described for prototype II. Figure 4.23 shows the final wafer which contains about 50 prototype III accelerometers. After this step, the wafer was diced, packaged, and wire-bonded. Figure 4.24-a, shows the SEM image of one side of the accelerometer. In this figure, the beam, anchor, etch holes, and the electrodes can be clearly observed. Figure 4.24 – b shows the central part of the accelerometer. The internal anchor and the two elastic beams extended from the middle anchor and connected to the moving frame are visible in this picture.

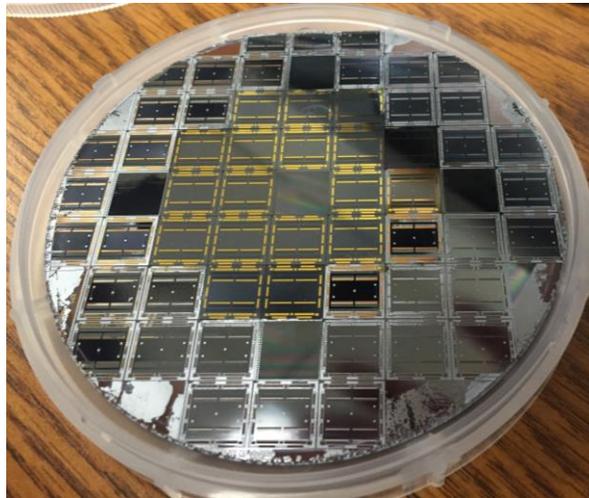


Figure 4.23 - In-plane accelerometer prototype III, the final processed wafer

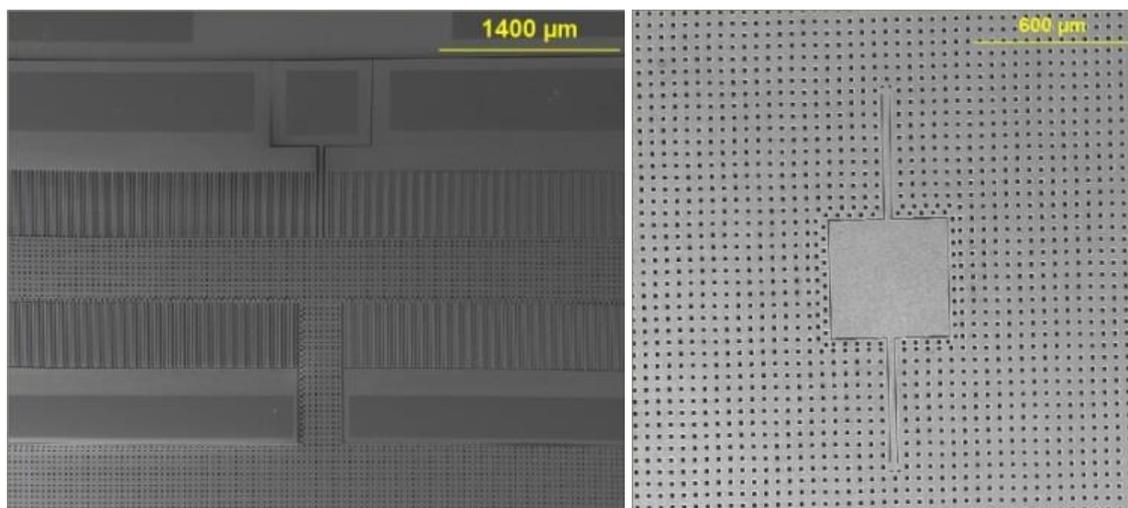


Figure 4.24 – a) SEM image of the electrodes and moving frame, and b) SEM image of one of the internal anchors and the two elastic elements in the middle of the moving frame

4.3. Packaging Process

The next step after dicing the finalized wafer into the dies is packaging and wire-bonding. MEMS packaging is an essential step in developing micro-sensors since it has a direct effect on performance, reliability, and cost of the final product [80]. Wafer Level Packaging (WLP) and Chip Level Packaging (CLP) are the two principal techniques in MEMS packaging technology. WLP, as its name implies, is the batch technology for packaging the dies while they are still part of the wafer. In the CLP technique, each die (device) is put into a package, and the packaging process is performed individually for each die. Although WLP provides a small-size and cost-effective packaging technique, the CLP technique was employed in this research to avoid extra complications to the process development and to simplify fault detection. CLP consists of 4 steps of die attachment, wire-bonding, sealing, and testing [81]. Die attachment includes attaching the device chips to the chip carrier to provide mechanical support. Wire-bonding creates electrical connection between the MEMS device and the chip carrier. In this case, the MEMS device could have access to the environment it needs to interact with. Sealing or encapsulation is performed in order to create a controlled operating environment for the MEMS device and also keep it safe from physical and chemical damages [80]. In the CLP technique, which is also called discrete packaging, metal, plastic or ceramic chip carriers are used for holding the MEMS device chips. In this research, 44-pin ceramic Leadless Chip Carriers (LCC) were used for packaging. The dimension of the package was $12.04(\pm 0.25)$ mm \times $12.04(\pm 0.25)$ mm \times $2.24(\pm 0.23)$ mm. The cavity of the package was coated with a layer of gold. The packaging process was performed using SRO-700 Vacuum Packaging System [82]. This system is a Solder Reflow Oven (SRO) which can be used for die attachment, sealing, and vacuum encapsulation.

To perform die attachment, the backside of the MEMS devices was coated with a layer of gold, and Au80/Sn20 alloy was used as die attachment material. After aligning the MEMS device on top of Au80/SN20 inside the package, the whole package was put inside the SRO-700 system. Following this step, the chamber was heated up to 300°C which is slightly higher than the eutectic melting point of Au80/Sn20, i.e., 280°C. After a few seconds the chamber was heated down and the rigid attachment between the MEMS die was formed.

The next step in the packaging process was wire-bonding. Wire-bonding creates the electrical connection between the MEMS device and the package. Consequently, the MEMS device can be interfaced with the electrical circuit. The equipment which was used for wire bonding was a wedge-ball K&S 4700 wire Bonder at Simon Fraser University's 4DLabs. Figure 4.25 shows the accelerometers inside the packages after die attachment and wire-bonding.

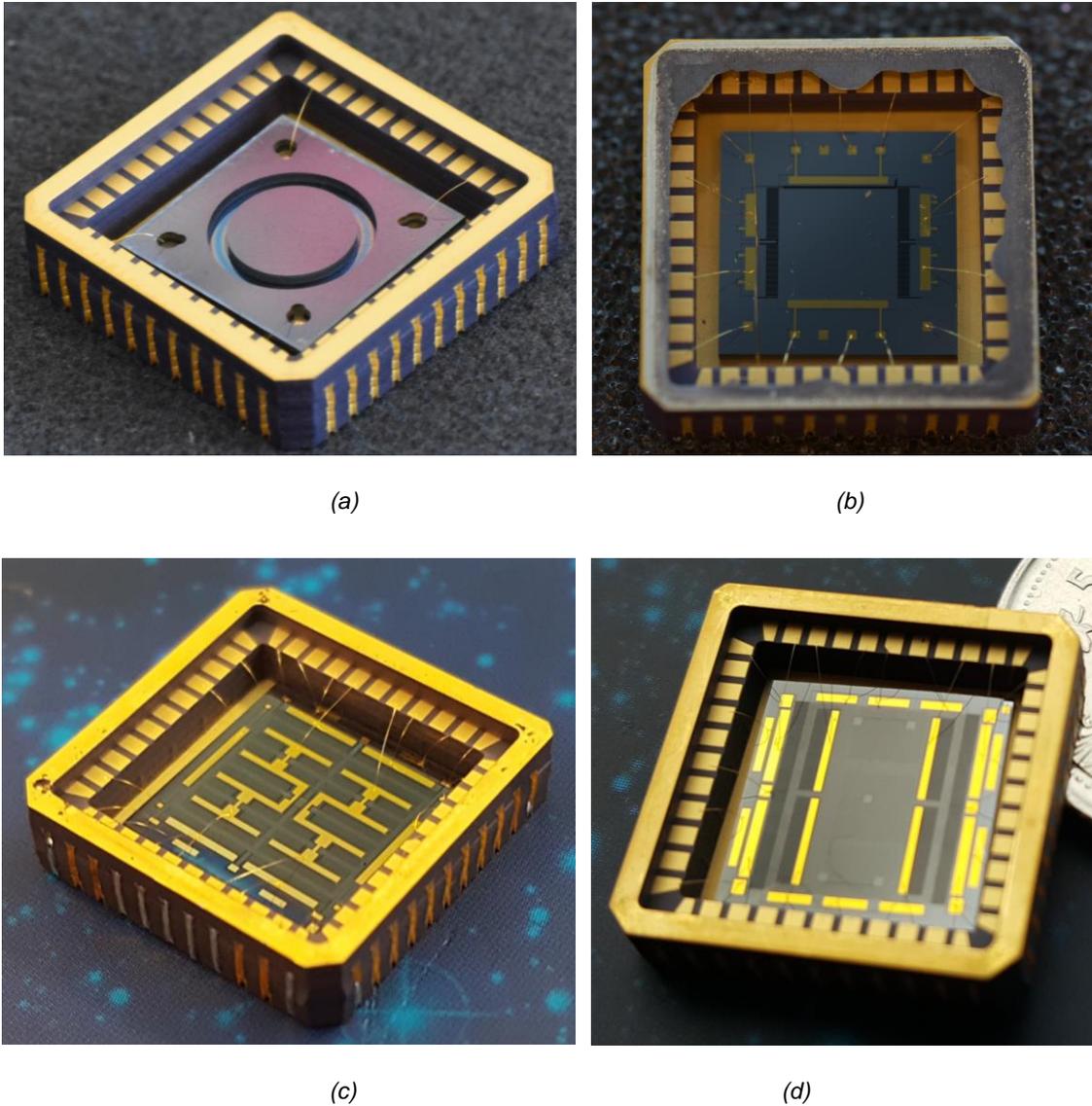


Figure 4.25 – Accelerometers after die attachment and wire bonding, the die sizes for all accelerometers are 10mm by 10mm, a) out-of-plane accelerometer, b) in-plane accelerometer, PTI, c) in-plane accelerometer, PTII, and d) in-plane accelerometer, PTIII

After the wire bonding step, the accelerometers were temporarily covered by lids using tapes for characterizations and experimental studies. Upon the confirmation of functionality of the devices, the accelerometers would be sealed and encapsulated using the process which was developed by Yuxi Zhang at Intelligent Sensors Laboratory [81]. Other than encapsulation process development, he also developed an in-package pressure monitoring system using bond wire Pirani sensor. For the purpose of this research, the accelerometers were tested using the temporary lids.

Chapter 5. Experimental Results

A range of electrical and mechanical tests including frequency response test, sensitivity experiment, and noise floor evaluation were performed to characterize the performance of the fabricated devices. In this chapter, the interface electronics, the experiment methodology, the experimental setup, and the characterization results of the fabricated micro accelerometers are elaborated. All the interface electronics presented here were designed by Soheil Azimi and were utilized for characterization of the accelerometers.

5.1. Interface Electronics

In order to evaluate the performance of the developed accelerometers, it was necessary to interface the MEMS devices with an electronic circuit. The capacitive changes of the accelerometer that are caused by an input acceleration need to be converted to an output voltage. Two different kinds of capacitance-to-voltage converter circuits were designed and implemented: low-power circuit, and low-noise circuit. In this section, the working principle of the two circuits are explained.

5.1.1. Low Power Circuit

For the low power circuit, an off-the-shelf general-purpose high-resolution capacitive readout chip called MS3110 was used [83]. This ultra-low noise capacitive CMOS IC requires only a single +5V DC supply and some decoupling components. MS3110 can provide an output voltage proportional to the changes in capacitance value with a resolution down to $4 \frac{\text{aF}}{\sqrt{\text{Hz}}}$, and it can work in either single-ended or differential mode. The MS3110 also includes an on-chip dummy capacitor for quasi-differential operation and initial adjustment. The power consumption of this circuit is 15mW.

As shown in Figure 5.1, the designed interface circuit includes the sensor and the readout PCB which are mounted on top of each other using the connectors. The layout of the circuits is presented in Appendix C.

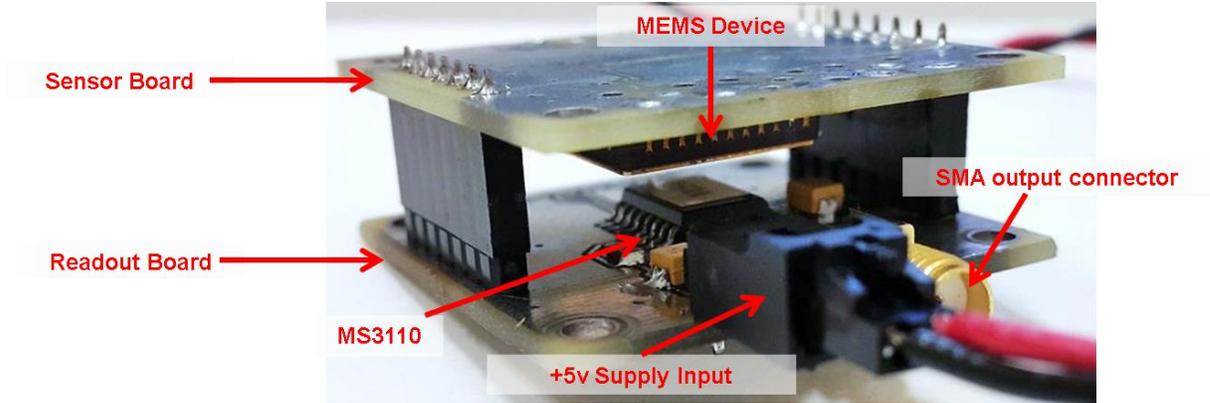


Figure 5.1 - Sensor test board (up) and MS3110 interface board (down) attached together

Considering the resolution of MS3110 reported on its datasheet as $4 \frac{aF}{\sqrt{Hz}}$ as well as the desired noise limit of the system which is $0.5 \frac{\mu g}{\sqrt{Hz}}$, the sensitivity of the MEMS devices should be:

$$MEMS \text{ devices Sensitivity} = \frac{4 \frac{aF}{\sqrt{Hz}}}{0.5 \frac{\mu g}{\sqrt{Hz}}} = 8 \frac{pF}{g} \quad (5.1)$$

The derived value for the sensitivity of the sensors is far more than the designed sensitivities for the accelerometers which are less than 2 pF/g. Therefore, although MS3110 is considered a low-noise readout chip in the market for MEMS sensors, it does not meet the requirements of this study. Accordingly, a lower-noise interface electronic was designed as explained in the next section.

5.1.2. Low-Noise Circuit

The low noise interface electronic was designed for capacitance differential sensing. It is a serial combination of a transimpedance amplifier (TIA) and a synchronous demodulator. The circuit converts the capacitance (C) changes of the accelerometer to voltage (V). Figure 5.2 shows the simplified block diagram of the C2V readout circuit.

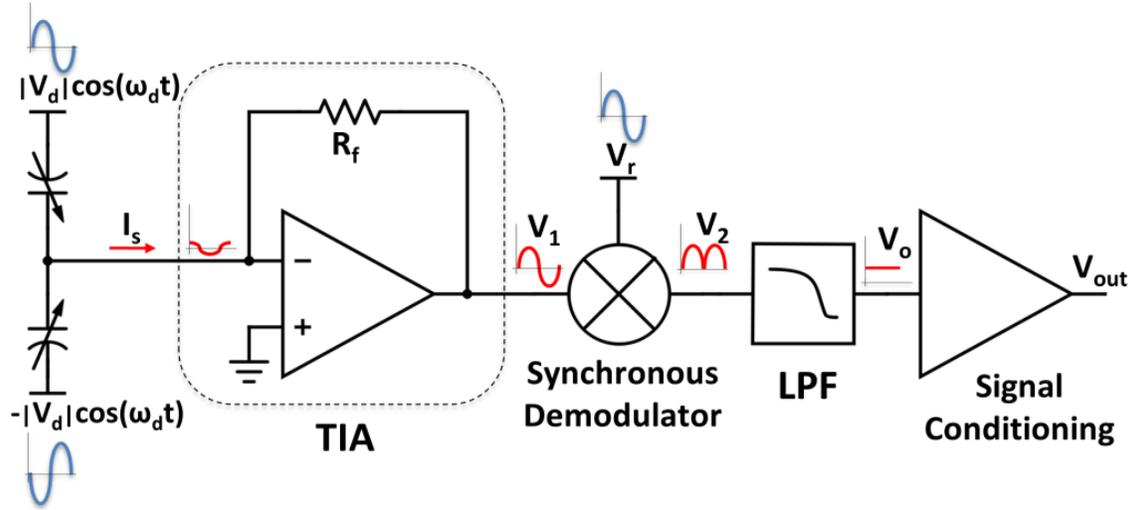


Figure 5.2 - Simplified block diagram of the readout circuit

The circuit works in the differential sensing mode. For single-ended readings, a constant capacitor is connected as one of the sense capacitors. The sense capacitors are driven by sinusoidal signals with 180° phase difference. The output signal is read through the proof-mass. The proof-mass is held at virtual ground by the TIA. The accelerometer's output current goes through the feedback resistor (R_f) and is amplified and converted to a voltage at the output of the TIA. The amplitude of this voltage is proportional to the capacitance changes of the accelerometer (ΔC) in the flat-band region of the amplifier:

$$V_1 = 4\pi f_d |V_d| R_f \Delta C \cos(2\pi f_d t + \varphi) \quad (5.1)$$

where f_d and $|V_d|$ are the frequency and amplitude of the drive signal, and φ is its phase difference with the drive signal due to the speed limitations of the TIA or parasitics. Following the voltage amplification, the TIA's output is multiplied by a reference voltage signal of the same frequency using a multiplier component. According to equation (5.2), upon multiplication, the output signal of the multiplier would have an AC as well as a DC component:

$$V_2 = \frac{1}{2} |V_1| |V_r| [\cos(4\pi f_d t + \varphi + \varphi') + \cos(\varphi - \varphi')] \quad (5.2)$$

where $|V_r|$ is the amplitude of the synchronous demodulator reference signal, $|V_1| = 4\pi f_d |V_d| R_f \Delta C$, and φ' is the reference signal phase difference with the drive signal. The high frequency AC component is eliminated using the low pass filter. According to equation (5.3) the remaining DC component has a linear relationship with the applied input acceleration:

$$|V_o| = 2\pi f_d |V_d| |V_r| R_f \Delta C \cos(\varphi - \varphi') \quad (5.3)$$

As seen in equation (5.3), minimizing the phase difference between the drive and reference signals leads to the output signal maximization.

In order to implement the circuit, the OPA656 FET-input operational amplifier from Texas Instruments was selected for the transimpedance amplifier with an R_f value of 100k Ω . AD835 analog multiplier from Analog Devices was selected for the demodulation. The drive voltage frequency was set to 1 MHz with maximum amplitude of 4.5V. The total sensitivity of the circuit is ~4.0V/ ρ F.

The Electrical Noise Equivalent Acceleration (ENEA) of the low-noise circuit is dominated by the TIA noise at the drive frequency and can be estimated by:

$$ENEA = \left[\frac{v_{ne}}{G_s} \right] \quad (5.4)$$

where v_{ne} (V/ $\sqrt{\text{Hz}}$) is the voltage noise floor of the readout circuit and G_s (V/g) is the system's total gain. Circuit simulation predicted an output noise floor of 1 μ V/ $\sqrt{\text{Hz}}$ in the flat-band region of the readout circuit. The experimental noise performance of the low-noise circuit along with the MEMS device are further discussed in the Noise Performance section. The low-noise circuit layout is presented in Appendix C.

5.2. Sensitivity

The very first test performed for evaluating the functionality of the fabricated accelerometers was the DC sensitivity test. The sensitivity (or scale factor) of an accelerometer is the output voltage change per unit of the input acceleration at the

nominal voltage and temperature measured in mV/g. In order to perform the sensitivity test, the accelerometers were connected to a Stanford Research RLC meter at 100 kHz. By rotating the accelerometer, i.e., applying $\pm g$, the change in the capacitance was measured. Table 5.1 shows the theoretical and experimental sensitivity of the designed and fabricated out-of-plane accelerometers.

Table 5.1– Out-of-Plane Accelerometer Sensitivity

Out-of-Plane Accelerometers			
	Design A1	Design A2	Design A3
Theoretical Sensitivity (pF/g)	0.11	0.72	6.56
Measured Sensitivity (pF/g)	0.13	0.88	4.08
Theoretical Bulk Capacitance (pF)	170		
Measured Bulk Capacitance (pF)	189		

The disagreements between the theoretical and measured sensitivities are mainly due to issues in the fabrication process. Imperfections in the fabrication steps cause over-etch, under-etch, non-straight side walls, etc. Each of these issues could cause changes in resonance frequency which ultimately affect the sensitivity, or could directly affect the sensing electrodes. Another discrepancy root cause between the experimental and theoretical data is the effects of parasitic. Parasitic capacitances are unwanted capacitances that exist between the different parts of electronic components due to their proximity to each other [84]. The parasitic capacitance causes the theoretical bulk capacitance value to have a considerable difference with the measured value. That is because the measured value includes the capacitance between the contact pads, bond wires, package lid, in addition to the sensing capacitance.

The sensitivity results of the in-plane accelerometers are shown in Table 5.2. This table has two main columns which are associated with prototype I (PT I) and prototype III (PT III) of the in-plane accelerometers.

Table 5. 2 – In-Plane Accelerometers Sensitivity Study

In-Plane Accelerometer					
		PT I		PT III	
Theoretical Sensitivity (pF/g)	LG*	SG*	0.65		
	0.14	0.28	LR*	HR*	
Measured Sensitivity (pF/g)	0.14	0.31		0.89–1.14	(Before Gold Deposition)
Theoretical Bulk Capacitance (pF)	12	17	72		
Measured Bulk Capacitance (pF)	42	46	195-219	68 - 71	158 - 164
Measured Resistivity (Ω)	250	400	10-20	2-20M	~100

*LG: Large Gap
*SG: Small Gap

LR*: Low Resistivity Wafer
HR*: High Resistivity Wafer

One of the raised issues in measuring the sensitivity of prototype III devices was the drastic drop of sensitivity between the devices from the two batches of fabrication rounds. Upon some investigations, it appeared that the resistivity of the SOI wafer was different between the two fabrication runs. In the first batch, the resistivity of the wafer was 0.01-0.02 Ω .cm, whereas in the second batch, it was 1-3 Ω .cm. That caused a resistance in range of 2-3 M Ω to exist in series between each sense comb and the proof mass in the high resistivity devices, as shown in Figure 5.3. As a result, the total sensitivity of the devices was affected. In order to resolve this issue, a layer of gold with a thickness of 200nm was deposited on the high resistivity devices. After metal deposition, the resistivity of the devices decreased to ~100 Ω , and the sensitivity was improved, as expected.

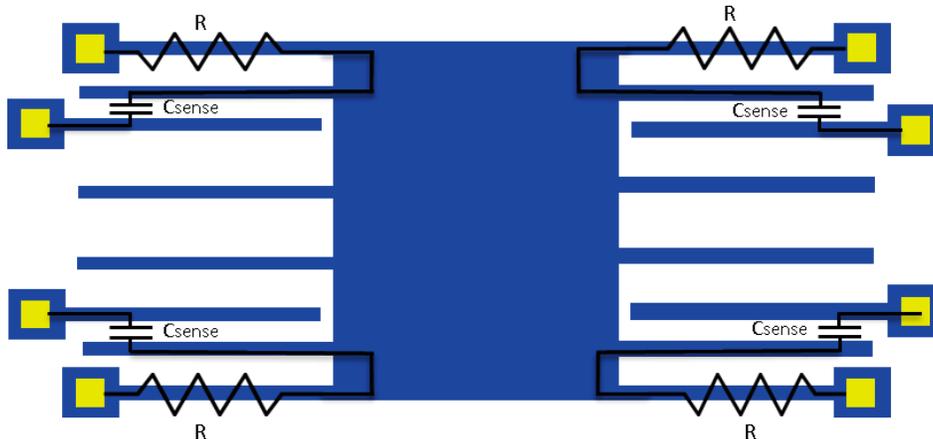


Figure 5.3 – The resistors in series with the sensing capacitors cause sensitivity drop

5.3. Frequency Response

To study the frequency response of the accelerometer system, different test setups could be designed. The core of the dynamic response characterization is actuating the device within the desired frequency band and measuring the output of the system. For the designed capacitive accelerometers, actuation can be done mechanically using a mechanical shaker, or electrostatically, by applying DC and AC voltages to the control electrodes of the accelerometer device. Similarly, the output of the system can be measured using direct methods such as measuring the proof mass motion by laser vibrometry or using the sensing capacitance variation in response to the proof mass actuation.

There are a few drawbacks associated with each method as explained below. In order to actuate a system using a mechanical actuation, the accelerometer along with the interface electronic is mounted on a fixture which is attached to the shaker. Due to the structural discontinuities, numerous resonance peaks are observed within the desired frequency sweep. Consequently, the dynamic response of the sole MEMS device becomes indistinguishable. Figure 5.4 shows an example of the frequency response associated with one of the accelerometers on the shaker. The blue graph shows the frequency response of the designed fixture, and the pink graph shows the frequency response of the in-plane prototype-III accelerometer. As observed in Figure 5.4, the dynamic response contains numerous peaks due to the mountings, interface electronics board, and connectors.

Due to the mentioned problems in using the shaker, it was decided to actuate the accelerometer system electrostatically. Therefore, the undesired resonance modes caused by the mechanical connections could be eliminated. Another issue in the dynamic response characterization pertains to the quality factor of the mode shapes. The designed accelerometers work in atmospheric pressures. However, some mode shapes have low quality factors. Therefore, they are not observable in the frequency response tests that are performed under atmospheric pressure. Accordingly, the dynamic response tests in this study were performed using electrostatic actuation and sensing inside a vacuum chamber. Nonetheless, some tests were performed on out-of-plane devices using the single-axis laser Doppler vibrometer at the ISL. These tests were performed in the atmosphere and did not show the first few resonance frequencies.

However, according to Figure 5.5, some high-frequency high-Q mode shapes were detectable in the tests using Laser vibrometry.

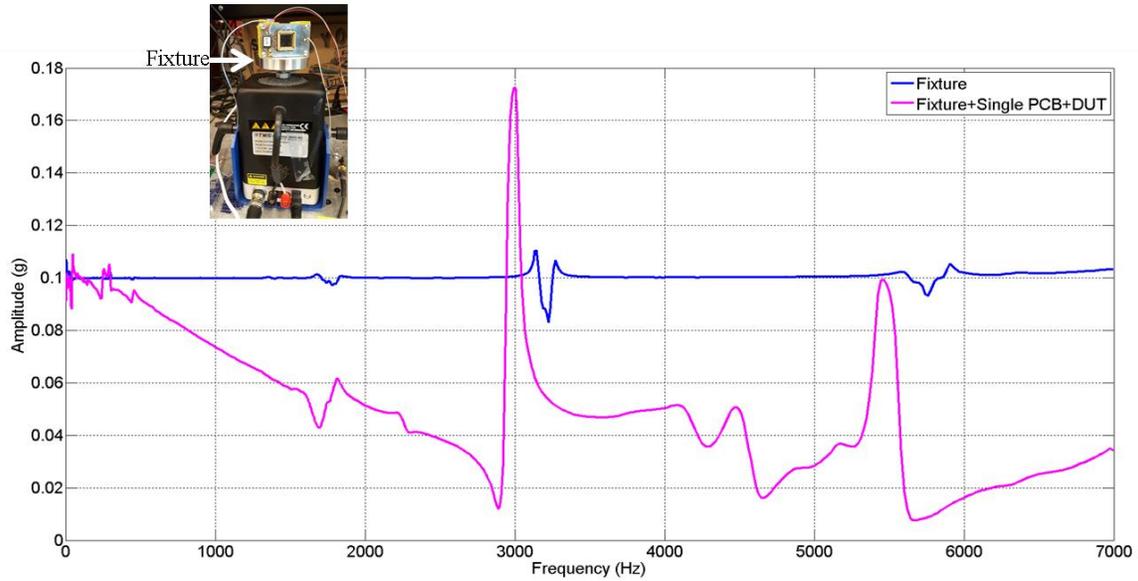


Figure 5.4 - Dynamic response of the in-plane PT II accelerometer on the shaker

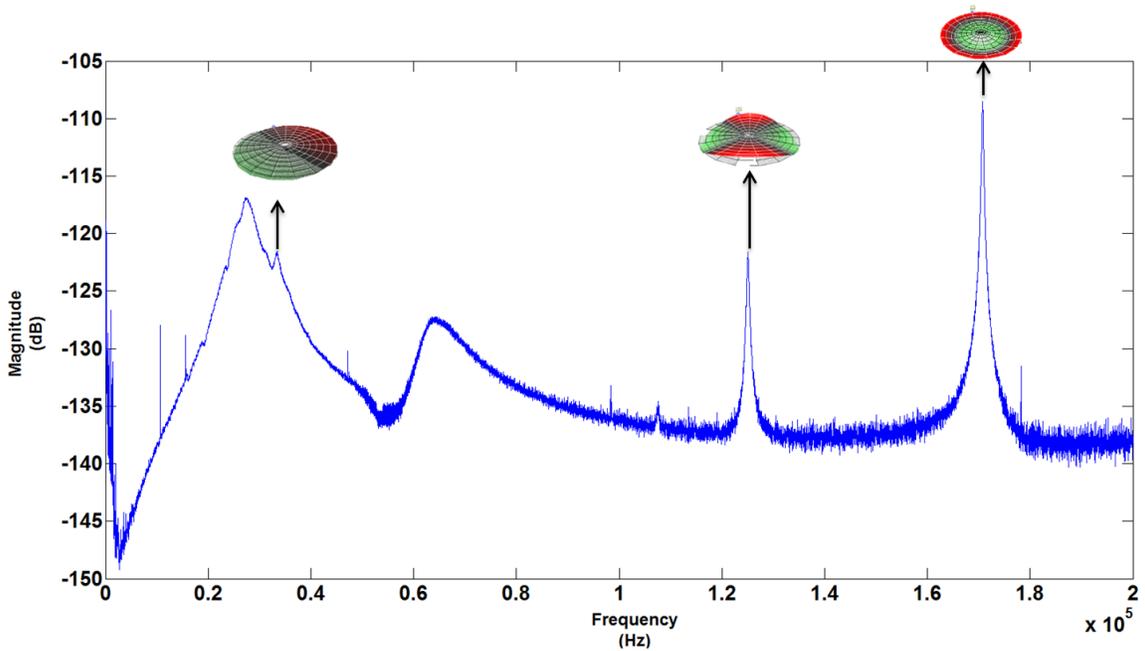


Figure 5.5 - Dynamic response test for out-of-plane accelerometers using laser doppler vibrometer

In the two following sub sections, the main test setup for measuring the dynamic response of the out-of-plane accelerometers as well as the test results are initially presented. Similarly, the main test setup for the in-plane accelerometers is explained and the results are shown.

5.3.1. Frequency Response – Out-of-Plane Accelerometer

The test setup for measuring the frequency response of the out-of-plane accelerometer is shown in Figure 5.6. As mentioned before, the accelerometer was tested in a vacuum chamber to eliminate squeeze film damping, increase the quality factor, and make the mode shapes visible. The test setup includes a HF2TA current amplifier, a Zurich Instruments HF2LI digital lock-in amplifier, and a DC voltage source [85]. During this test, the proof mass was biased with a DC and AC voltage. The AC voltage actuated the proof mass. The current output of the accelerometer was amplified using the current amplifier and was read through the lock-in amplifier.

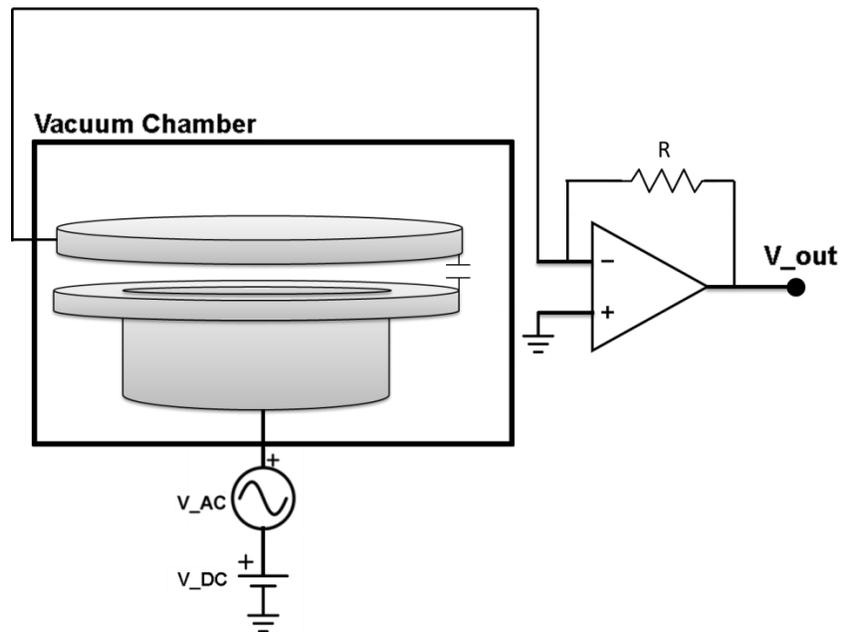


Figure 5.6 - Experimental setup for resonance frequency and quality factor measurement of the out-of-plane accelerometer

The dynamic response plot of the out-of-plane capacitive accelerometer, Design A2 with 350 μm membrane width, is shown in Figure 5.7. This experiment was performed at a pressure of 8 Pa. The applied DC and AC voltages were 2 V and 100 mV, respectively. The amplifier gain was set at 10 M Ω .

The experimental result shows that the first resonant mode of the accelerometer is at 5.2 kHz. According to the ANSYS numerical simulation, the mode shape corresponding to this frequency is the first out-of-plane mode also depicted in Figure 5.7.

Regarding the fact that the mechanical resonance frequency is considered to be the upper limit for the operating frequency of an accelerometer system, the plot of the dynamic response of the accelerometer asserts the fact that the working bandwidth of the device is more than 4 kHz. Although, some sensing techniques employ structures beyond their resonance frequencies as well [66].

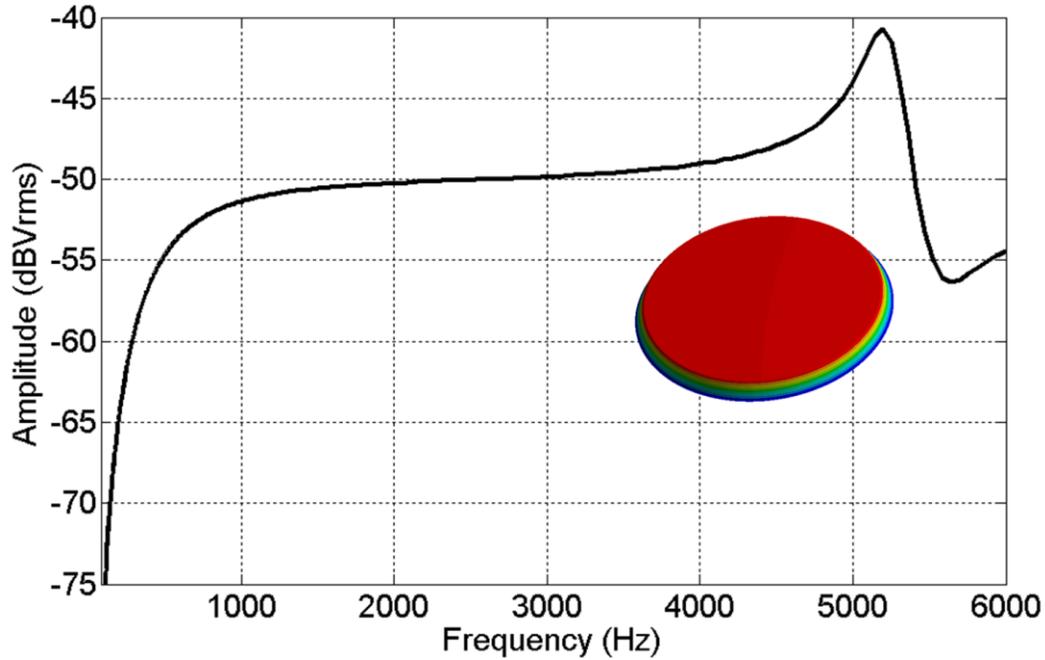


Figure 5.7 - Dynamic response characteristic plot of the 5 kHz out-of-plane accelerometer

The experimental first resonance frequencies of the three designs of out-of-plane accelerometers are summarized in Table 5.3. The discrepancies between the simulated and measured values of the resonance frequency are mainly due to the fabrication issues such as the quality of the anodic bonding of silicon and glass, sidewall angles in the DRIE process, stress in the oxide layer, etc.

Table 5.3 - Theoretical, simulated and measured resonance frequencies

	Design A_1	Design A_2	Design A_3
Theoretical Resonance Frequency	13.3 kHz	5.1 kHz	1.6 kHz
Simulated Resonance Frequency	14.8 kHz	5.7 kHz	2.2 kHz
Measured Resonance Frequency	13.5 kHz	5.2 kHz	2.8 kHz

As mentioned earlier, the quality factor is a measure of how damped a system is. Quality factor is inversely proportional to the noise floor of the accelerometer system.

The quality factor of the accelerometer is estimated using the frequency response of the device by [86]:

$$Q = \frac{f_{res}}{\Delta f_{-3dB}} \quad (5.5)$$

where f_{res} is the resonance frequency of the system, and Δf_{-3dB} is the 3 dB bandwidth of the device response around its resonance frequency. To find the quality factor of the accelerometers and its correlation with pressure, a test was performed using the same setup shown in Figure 5.6. The experimental procedure was changing the pressure of the vacuum chamber from 2 Pa to the atmospheric pressure while recording the quality factor of the device. However, beyond pressures of approximately 1 kPa, the resonance peak was indistinguishable. Figure 5.8 shows the result of this experiment. As observed in Figure 5.8, the quality factor of the system increases as the pressure decreases. The portion of the quality factor associated with the squeezed-film damping is correlated with pressure: decreasing pressure enhances the quality factor [87]. However, as the pressure drops down to a few Pascals, the growth rate of the quality factor slows down. At this point, the system's quality factor is restricted by other dissipation mechanisms such as anchor loss [88].

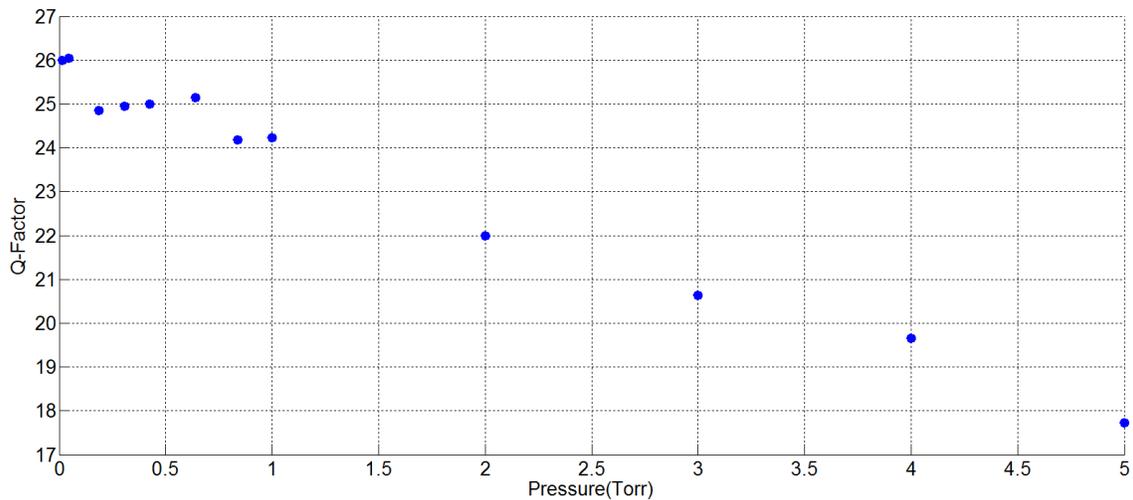


Figure 5.8 - Plot of the quality factor of the out-of-plane accelerometer vs. the vacuum chamber pressure

5.3.2. Frequency Response - In plane Accelerometer

The test setup for measuring the frequency response of the in-plane accelerometer is shown in Figure 5.9. The test is performed inside a vacuum chamber to decrease squeezed film damping and make the mode shapes visible. During this test, the proof mass was biased with a DC voltage. The electrodes which were implemented to apply the control voltage signals were biased with a differential AC voltage to actuate the proof mass. The differential current output of the accelerometer was measured at the sensing combs.

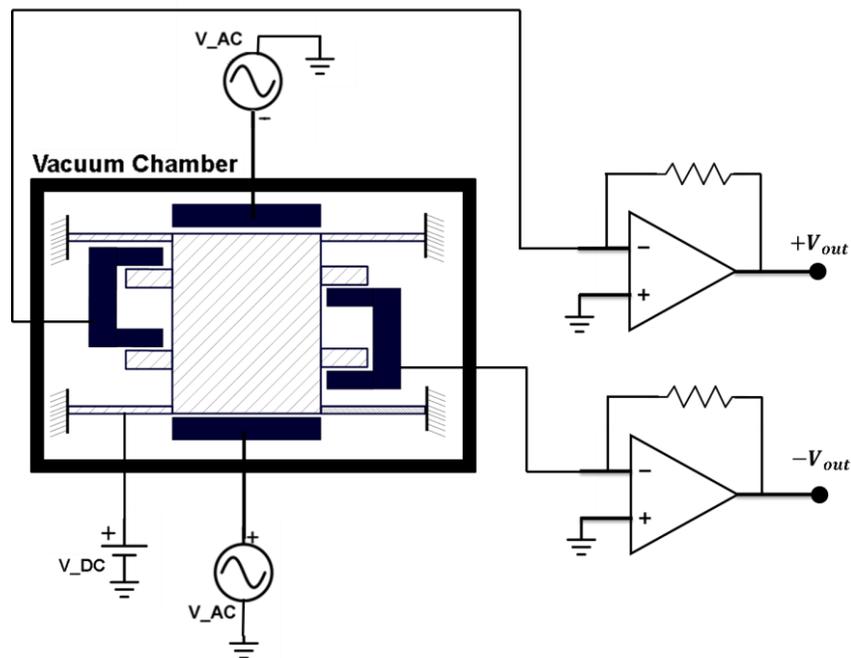


Figure 5.9 - Experimental setup for resonance frequency and quality factor measurement of the in-plane accelerometers

The frequency response of the prototype I is shown in Figure 5.10. The test was performed at the pressure of 25 Pa and the results show a resonance frequency of ~2.2 kHz. In this test, the proof mass was biased with 20V DC voltage and the structure was activated by 1V AC chirp signal.

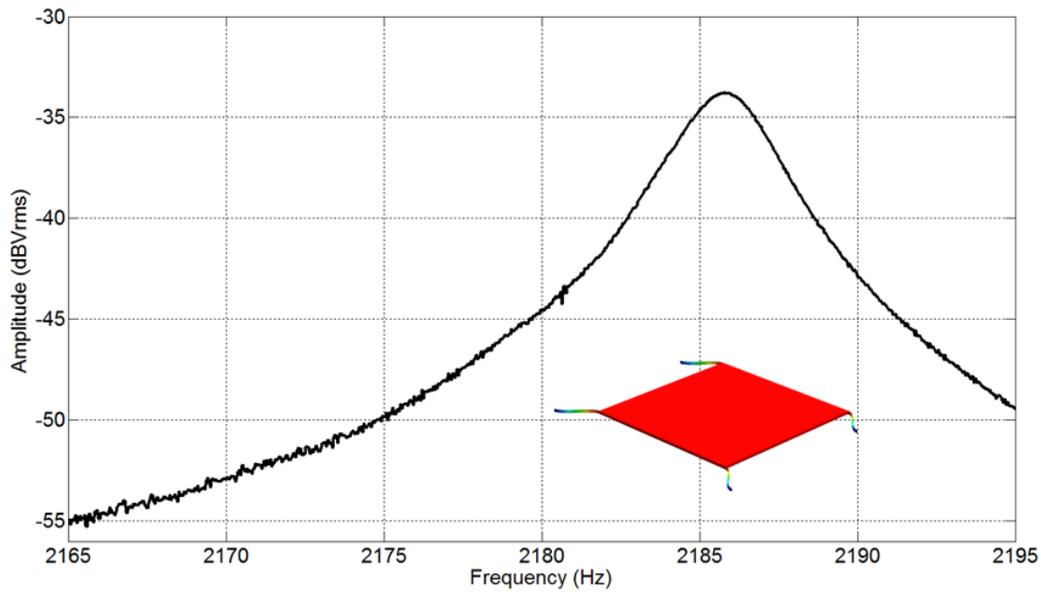


Figure 5.10 - Frequency response of in-plane accelerometer prototype I

Using the same setup, shown in Figure 5.9, other sets of experiments were performed in order to identify the correlation of the quality factor to the pressure. During this test, the pressure of the vacuum chamber was changed from 12 Pa to 700 Pa, and the quality factors of the device at each pressure were recorded. Figure 5.11 shows the effect of viscous damping on quality factor. As evident from the figure, by decreasing the pressure the quality factor is increased.

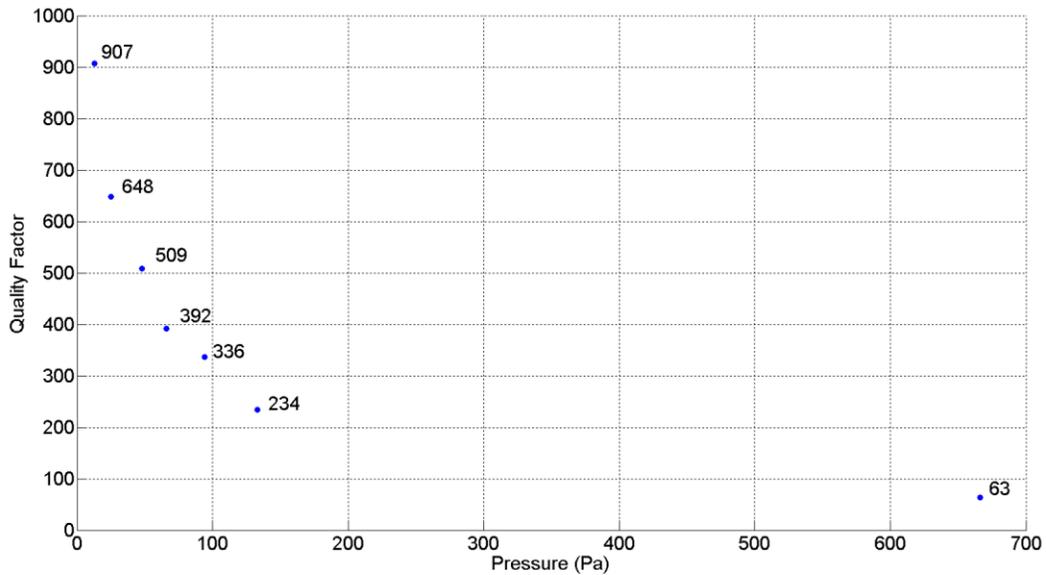


Figure 5.11 - Quality Factor vs. vacuum chamber pressure for in-plane accelerometer prototype I

The test results for the in-plane accelerometer prototype III are shown in Figure 5.12 by the red line. During this test, the proof mass was biased with 1V DC voltage and was actuated by 10mV AC voltage. The resonance frequency was recorded at 4.2 kHz with an in-plane mode shape. The result had less than 6% deviation from the ANSYS numerical simulation results.

The frequency response can be adversely affected by parasitic feedthrough components. When the parasitic capacitance becomes comparable with the measured bulk capacitance, part of the driving signal goes through the parasitic component[89], [90]. This issue becomes even worse at higher frequencies, since the parasitic impedance becomes so small compared to the mechanical resistance. As a result, the resonant signal becomes undistinguishable. In order to resolve this issue and remove the effect of the feedthrough current from the final results, the output of the system was initially recorded while the DC voltage was cut off. Consequently, the output of the system which contains the feedthrough current was recorded in the absence of resonance. Subsequently, the frequency response was again recorded by applying a 1V DC voltage. Finally, by subtracting the two signals, the parasitic capacitance feedthrough current was removed and the resonance peak was clearly identified.

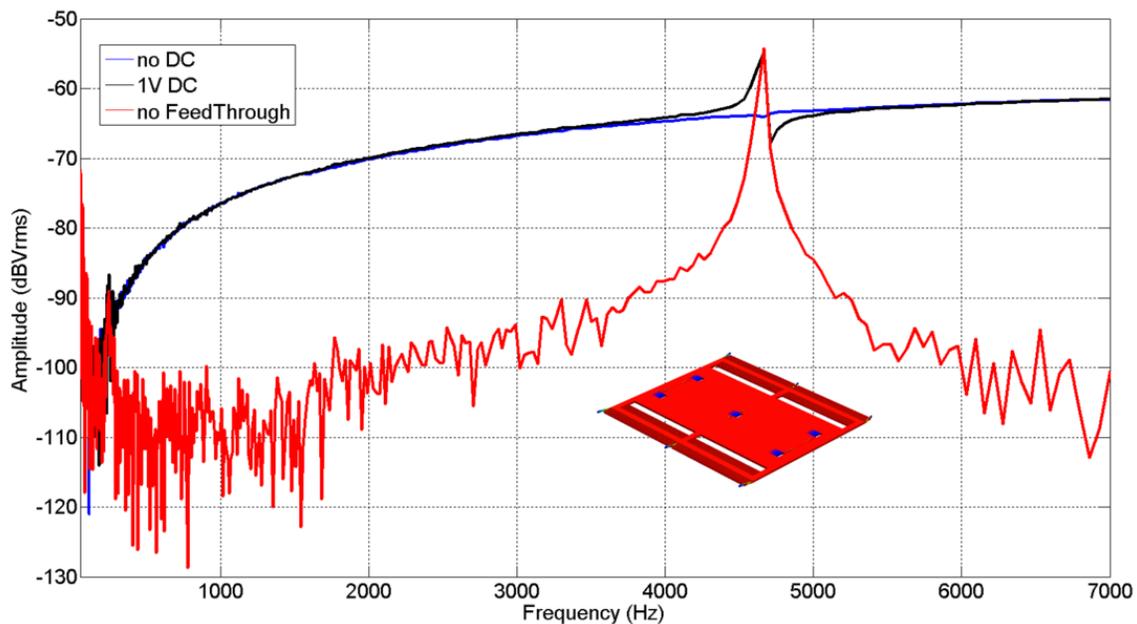


Figure 5.12 – The frequency response function of in-plane accelerometer prototype III

The quality factor versus the vacuum chamber pressure is shown in Figure 5.13. The minimum attained pressure was 1.5 Pa and the quality factor was increased significantly by decreasing the pressure.

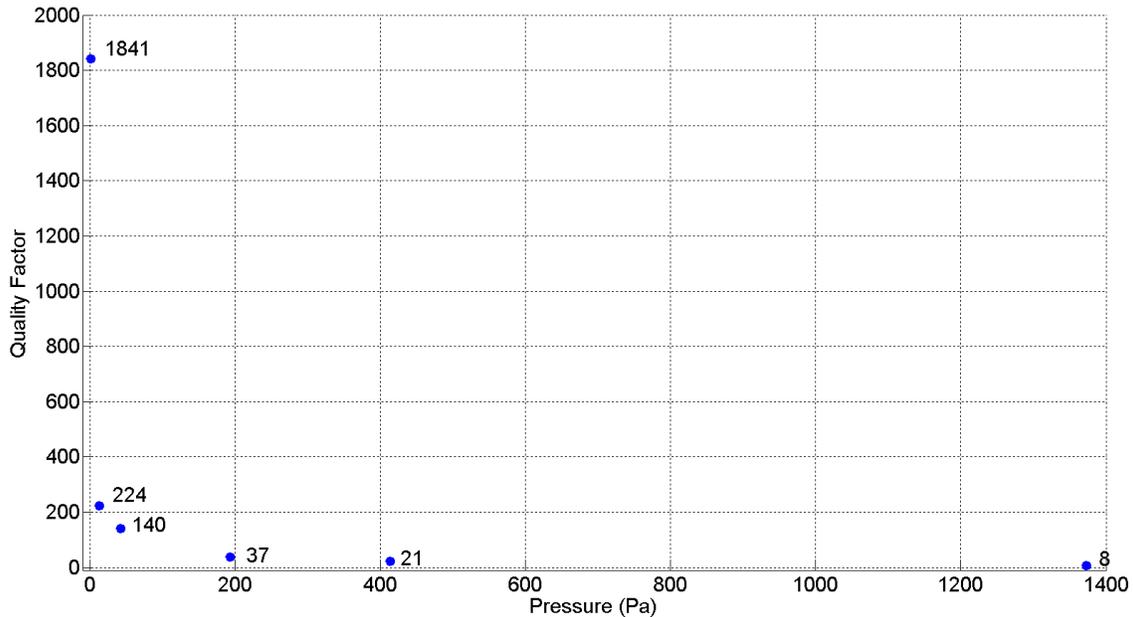


Figure 5.13 – The quality factor vs. vacuum chamber pressure for in-plane accelerometer prototype III

5.4. Linearity

For a sensor system, it is desirable that the output signal reproduce the input signal behavior. In order to achieve this, it is expected that the accelerometer have a linear response within some specified range. The lower limit of this range is the noise floor of the system, and the upper limit depends on limiting factors such as the pull-in phenomenon, the physical condition of the sensor material, the packaging, etc. To specify the working range of the accelerometer, its linearity should be characterized in order to correlate the sensor output to various applied acceleration signals. To evaluate the sensitivity and linearity of the designed MEMS devices, a dynamic test using the test setup shown in Figure 5.14 was carried out. The test setup includes a closed-loop system consisting of a high frequency shaker, its controller, and a reference accelerometer. To perform the sensitivity test, the sensor was paired with the low-power interface electronics. Then, the accelerometer placed on a proper fixture and was fixed to the shaker. A proper fixture is one that does not have any resonance frequency align

with shaker activation axis in the desired frequency band of the experiment. Appendix D has a short discussion on the fixture design process and the designed fixtures for in-plane accelerometers.

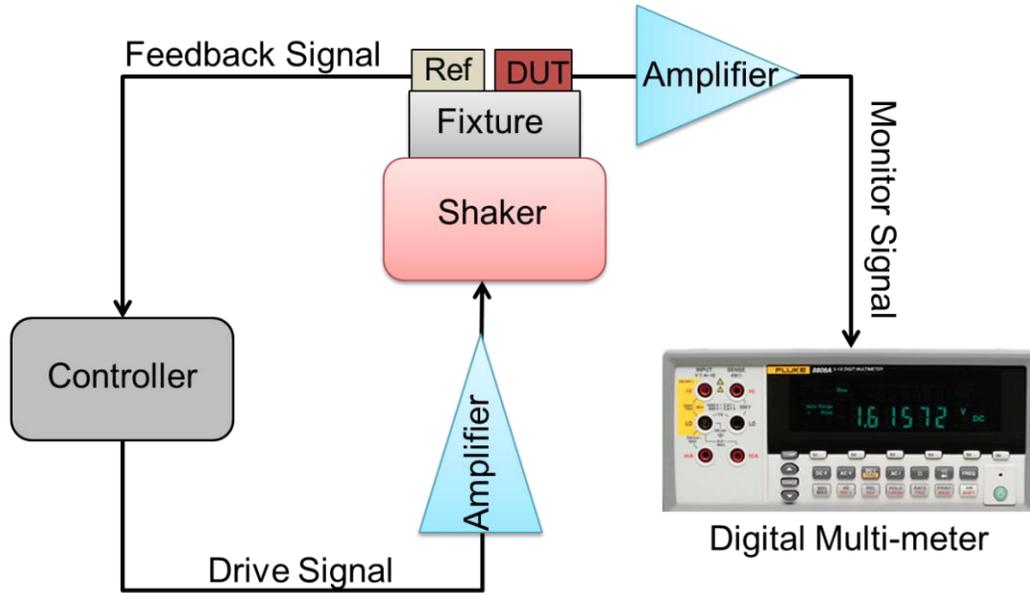


Figure 5.14 - Sensitivity Test Setup Schematic

To perform the sensitivity test, a sinusoidal input at specific excitation frequencies was applied to the shaker. The magnitude of the signal was in the range of 200mg to 3g. The minimum and maximum applied accelerations were limited by the shaker capabilities. The percentage of the non-linearity of the accelerometer was identified using equation (5.6) [91]. By the definition, non-linearity is the maximum deviation of the output voltage from a best fit straight line, which is divided by the sensitivity of the device and is expressed as a percentage of the full-scale output in g.

$$Non - Linearity = \frac{Maximum\ Deviation\ (g)}{Full\ Scale\ Output\ (g)} \times 100\% \quad (5.6)$$

Upon performing the test, it was concluded that the nonlinearity of the sensors within the range of the experiment was 0.5% and 0.1% for the out-of-plane and in-plane accelerometers, respectively. Figure 5.15 shows the linearity characteristic of one sample of out-of-plane, Design A1, and in-plane accelerometer, prototype III.

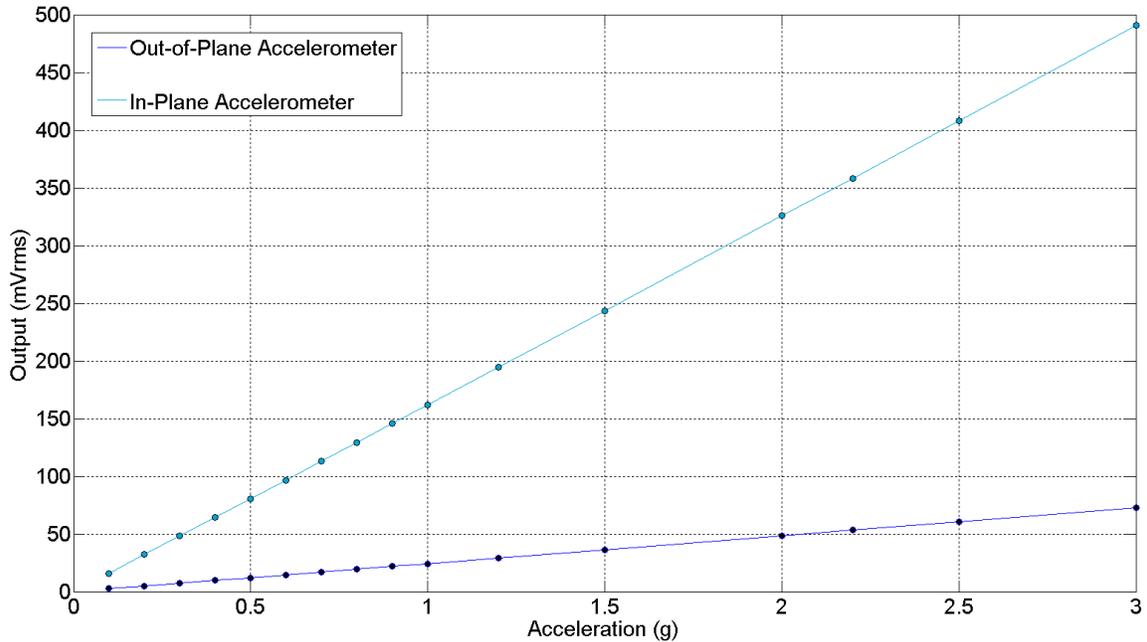


Figure 5.15 - Linearity Characteristic graph of out-of-plane and in-plane accelerometers

5.5. Noise Performance

To identify the noise performance of the system, the MEMS devices were paired with the low-noise circuit. In order to keep the environmental vibration variations at a minimum, during this test the accelerometer was put on an anti-vibration table. The output signal of the accelerometers was recorded using National Instruments PXI 4462 A/D, a 24-bit, 204.8 kS/s dynamic signal analyzer with zero-g acceleration input. All of the data was recorded using a 200 KS/s sampling rate within the time range of 1s. Considering the Nyquist theorem, since the sampling frequency is 200 kHz, the output noise frequency is 100 kHz. Figure 5.16 shows the experimental result for the total noise equivalent acceleration of the complete system in the frequency domain for in-plane and out-of-plane accelerometers. For all three accelerometers, out-of-plane, in-plane PT I and in-plane PT III, in the low-frequency portion of the spectrum, the $1/f$ noise of the output signal conditioning amplifiers is apparent, followed by the flat-band noise floor of the circuit. At around 5 kHz, the low-pass filter attenuates the output noise until it reaches the minimum noise floor of the measurement setup. It is claimed that the noise performance of the accelerometers are better than what was measured. The most important reason that supports this claim is that the developed accelerometers are reacting to the environmental sounds even when they are on the anti-vibration table.

Regarding the fact that all the tests were performed at Intelligent Sensors Laboratory which is not an anechoic chamber, it can be concluded that part of the noise floor is due to the environmental noise. In addition, the low-noise circuit was optimized for in-plane accelerometer PT III. Considering these issues, the results show a noise floor of less than $0.5 \mu\text{g}/\sqrt{\text{Hz}}$ in the flat-band region of the frequency.

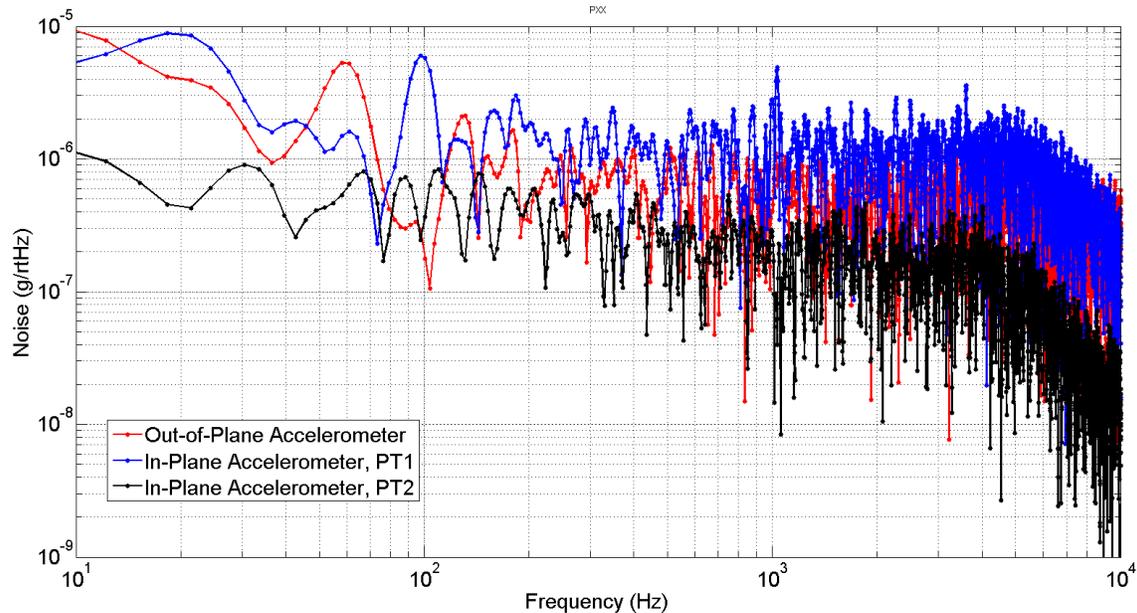


Figure 5.16 - Experimental result of the in-plane accelerometer TNEA in the frequency domain

5.6. Dynamic Range

Dynamic range is defined by the maximum measured signal to the minimum measured signal. The maximum measured signal was limited to shaker capabilities. However, the maximum applied acceleration was 3 g. On the other side of the spectrum, the noise level of the device can be interpreted as the minimum measurable signal from the accelerometer. Regarding the noise measurements, if the noise floor considered as $0.5 \mu\text{g}/\sqrt{\text{Hz}}$, the dynamic range of prototype III would be more than 135 dB.

5.7. Underwater Experiments

In the underwater set of experiments, the directional performance and frequency response of the accelerometer were evaluated in the underwater facilities. These tests were only performed on the in-plane prototype III accelerometers.

In order to analyze the cross-axis sensitivity of the device, the accelerometer and its interface circuit were sealed and placed inside a pressure vessel which was acoustically matched to water. The system was placed inside a vibration-isolated pool at Ultra Electronics testing facilities. The module was left powered and submerged in the tank overnight to ensure a stable operating temperature. The test setup is shown in Figure 5.17.

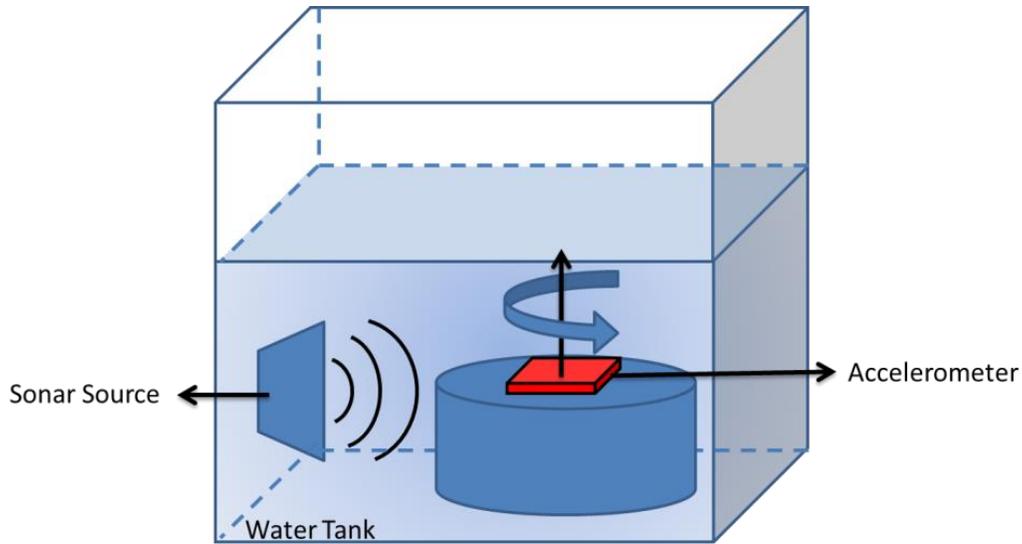


Figure 5.17 - Test setup for measuring the cross axis sensitivity of the accelerometer using sonar waves

The pulsed sonar source was emitting sound waves at 3 kHz. At the receiving end, the accelerometer assembly rotated at a constant angular rate. The output of the accelerometer was recorded. Figure 5.18 illustrates the magnitude of the sensor output versus the deviation angle from the sonar source on a polar plot. At 0 degree, the accelerometer sense axis is perpendicular to the acoustic source emission axis. At 90 degrees, the accelerometer sense axis and acoustic source are parallel. As can be seen in the figure, the cross-axis sensitivity of the accelerometer exhibits nulls of better than negative 30 dB along the directions normal to the desired axis of sensitivity.

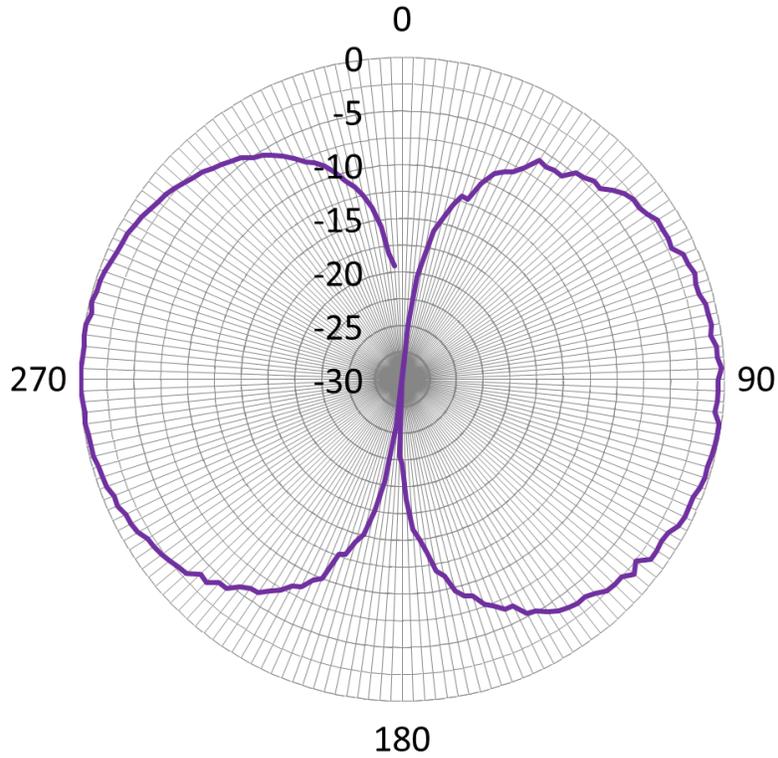


Figure 5.18 - Cross-axis sensitivity of the accelerometers measured using sonar waves

Using the setup shown in Figure 5.17 at a fixed angle, the dynamic response of the accelerometer was measured. In this test, the pulsed sonar source generated signals from 500 Hz to 11 kHz, and the output of the accelerometer was recorded. The result is shown in Figure 5.19.

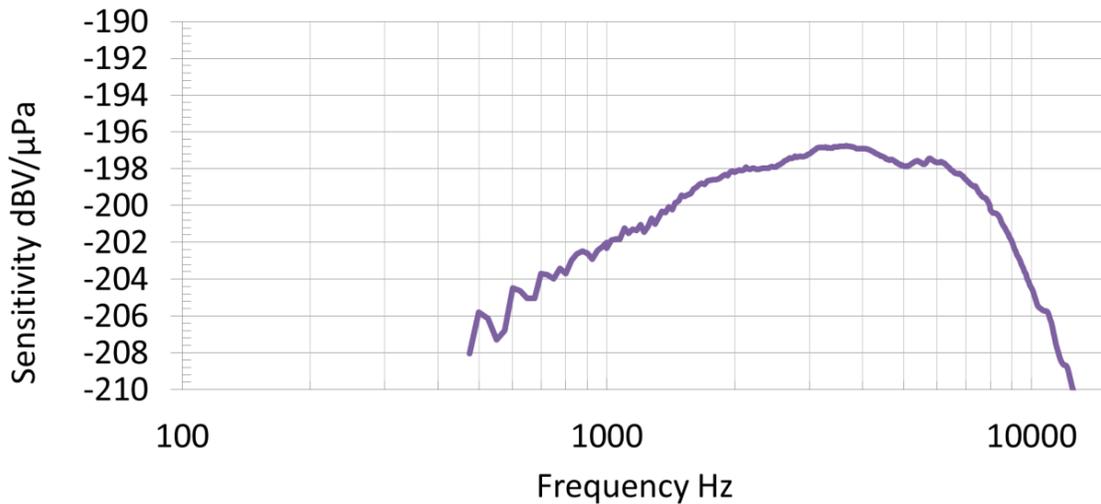


Figure 5.19 - Frequency response of the developed accelerometer in response to sonar waves

Chapter 6. Conclusions and Future Work

In this chapter, an overview of the achievements of this research project is presented. In the conclusions section, the contributions of this thesis to the literature are demonstrated. Following that, the resulting publications are listed. Finally, the future research ideas that were developed during the course of this thesis are discussed.

6.1. Conclusions

This dissertation was a study on developing capacitive high performance micro accelerometers for acoustic and sonar wave detection. The developed accelerometer is also applicable to structural health monitoring, condition monitoring, geophysical surveillance, and seismic imaging. In the context of this thesis, the term high-performance pointed at sub- μg noise level performances along with the bandwidth of a few kHz. After initial investigations, it was found that no viable accelerometer or design approach existed in the literature for the design and fabrication of the intended high-performance device.

Over the course of this project, two distinct high-performance accelerometers for the measurement of out-of-plane and in-plane inertial forces were developed. Experimental measurements on the fabricated prototypes demonstrated a combination of performance metrics unattained by prior MEMS accelerometers, to the best of the author's knowledge. The unprecedented performance metrics for the developed accelerometers were achieved through the novel designs and the novel fabrication process.

The out-of-plane accelerometer consisted of a circular proof mass attached to the substrate through an annular membrane. Within a few μm on top of the proof mass, a fixed plate was inserted, creating a varying capacitor to measure the applied acceleration. The out-of-plane accelerometer design was materialized using anodically-bonded SOI and glass wafers. The proof mass and the membrane were carved out of the SOI wafer, and the fixed electrode was implemented on the glass wafer. The developed fabrication process can be utilized as a platform for developing high performance accelerometers. The process provides the possibility of developing

continuous membrane-type suspension elements which could contribute in lowering cross-axis sensitivity and uniform displacement for the proof mass. Moreover, the process provided the full wafer thick proof mass which significantly improved the mechanical noise of the accelerometer system. The developed out-of-plane accelerometer was proven to have an operating bandwidth of 5 kHz, sensitivity of ~ 0.9 pF/g, and total mechanical noise equivalent acceleration of less than $450\text{ng}/\sqrt{\text{Hz}}$ in the flat band region. The open loop dynamic range of the accelerometer system was estimated to be higher than 130 dB while operating at atmospheric pressure.

For the in-plane devices, a design platform called the Mode Tuning Structural Platform was proposed to increase the operating bandwidth of the micromachined accelerometers, while maintaining high sensitivity and low-noise. This platform included alteration of the accelerometer's proof mass to a moving frame that provided a large area for sensing electrodes. The undesired vibration modes of such electrodes were suppressed by the placement of anchors and elastic elements within and around them. Using this platform, three various accelerometers were designed and fabricated. The experiments performed on the final devices showed that the accelerometers could achieve the total noise equivalent of less than $500\text{ng}/\sqrt{\text{Hz}}$ while maintaining a wide bandwidth of 4 kHz. In addition, the stiffness of the structure allowed for achieving a dynamic range of higher than 135 dB.

The research resulted in three conference papers, two journal papers and one patent application, as listed below:

1. **F. Edalatfar**, S. Hajhashemi, B. Yaghootkar, and B. Bahreyni, "Dual mode resonant capacitive MEMS accelerometer," in *2016 IEEE International Symposium on Inertial Sensors and Systems*, 2016, pp. 97–100.

2. **F. Edalatfar**, B. Yaghootkar, A. Q. A. Qureshi, S. Azimi, and B. Bahreyni, "Design, fabrication and characterization of a high performance MEMS accelerometer," in *2016 IEEE SENSORS*, 2016, pp. 1–3.

3. **F. Edalatfar**, S. Azimi, A. Q. A. Qureshi, B. Yaghootkar, and B. Bahreyni, "Wideband, low-noise accelerometer with open loop dynamic range of better than 135DB," in *2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, 2017, pp. 1187–1190.

4. **F. Edalatfar** *et al.*, "A Wideband, Low-noise Accelerometer for Sonar Wave Detection," *IEEE Sens. J.*, vol. PP, no. 99, pp. 1–1, 2017.

5. **F. Edalatfar** *et al.*, "High Performance MEMS Accelerometers based on a Novel Microfabrication Process," *Sensors Actuators A*, 2018, under review

6. US Prov. App. 62/425,020; ACCELEROMETER SENSOR

6.2. Future Work

This research work intended to develop a capacitive high performance accelerometer. Further research and studies can be undertaken both in regards to device performance improvements as well as the development of novel applications:

1. One of the areas that can be developed further to improve micro accelerometers performance while making it appropriate for commercialization is improving the packaging process. As mentioned in Chapter 4, the devices were packaged using chip level packaging. Chip level packaging has some drawbacks in a commercial electronic product. These drawbacks include the final cost of the packaging process due to the manufacturing cost of the packages, requirement of more time for packaging step in comparison to batch packaging, and increased overall size of the sensor. Therefore, it is proposed to modify the fabrication process to implement wafer-level packaging. Using WLP, the effective die size of the accelerometer could be increased leading to even lower noise. Moreover, in an established high-yield process, the WLP contributes to significantly lowering the final cost of the chips.

2. Another aspect of the research that can be further improved is the noise floor of the accelerometer. The total noise equivalent acceleration can be reduced by reducing the electrical noise equivalent acceleration and the mechanical noise equivalent acceleration. The following are recommended in that regards:

a) In order to reduce ENEA, and consequently reduce TNEA, it is recommended to design ultra-low-noise capacitive interface electronics.

b) In order to reduce MNEA, it is required to increase the mass and the quality factor. Increasing the mass is limited by the die size. However, it can be enhanced by

developing an accelerometer with small footprint but large thickness. This can be subject to further research. Meanwhile, MNEA can be reduced by increasing the quality factor of the MEMS device. Quality factor can be enhanced by vacuum packaging as well as modifying the design for reducing anchor losses. Modeling the dissipation mechanisms, finding out the dominant sources, proposing new mechanical designs for reducing energy dissipation in the developed accelerometers, are among other areas of future work.

3. Another development area is adding feedback controls to the MEMS accelerometers. By adding feedback controls, the bandwidth of the devices could be even further enhanced. Moreover, in a device with a high quality factor, a feedback controller is necessary to suppress the oscillations.

4. In chapter 3, Mode Tuning Structural Platform was introduced as an idea for developing high performance accelerometers. The initial method used by the author for achieving the high performance micromechanical design was based on trial and error rather than a specific algorithm. A great extension to this idea would be developing an algorithm for topology and support position optimization for maximizing the fundamental frequency of the structure with the desired mode shape. Various research work has been reported in the literature in the field of topology optimization of vibrating structures for achieving specific eigenfrequencies and eigenmode shapes [92]–[103]. However, there are no through analysis in the literature on the combination of topology and boundary condition optimizations on structures with frequency and mode shape constraints [104], [104]–[108]. Therefore, commencing a research work in this field would be beneficial in the design of high performance mechanical structures.

References

- [1] American Standards Association, *American standard acoustical terminology*. [New York], 1951.
- [2] K. Kaouri, "Left-right ambiguity resolution of a towed array sonar," masters, University of Oxford, 2000.
- [3] "HydrophoneHandbook_eReader_Ed2_20151208." [Online]. Available: <http://ondacorp.com/Handbook/#p=112>. [Accessed: 13-Dec-2017].
- [4] G. C. Carter, *Coherence and time delay estimation: an applied tutorial for research, development, test, and evaluation engineers*. IEEE Press, 1993.
- [5] T. B. Gabrielson, D. L. Gardner, and S. L. Garrett, "A simple neutrally buoyant sensor for direct measurement of particle velocity and intensity in water," *J. Acoust. Soc. Am.*, vol. 97, no. 4, pp. 2227–2237, Apr. 1995.
- [6] A. Barbagelata, P. Guerrini, and L. Troiano, "Thirty Years of Towed Arrays at NURC," *Oceanography*, vol. 21, no. 2, pp. 24–33, Jun. 2008.
- [7] "Ultra Maritime Systems." [Online]. Available: <http://www.ultra-ms.com/>. [Accessed: 12-Jan-2018].
- [8] C. B. Leslie, J. M. Kendall, and J. L. Jones, "Hydrophone for Measuring Particle Velocity: The Journal of the Acoustical Society of America: Vol 28, No 4," *J. Acoust. Soc. Am.*, vol. 28, 1956.
- [9] G. M. Wenz, "Acoustic Ambient Noise in the Ocean: Spectra and Sources," *J. Acoust. Soc. Am.*, vol. 34, no. 12, pp. 1936–1956, Dec. 1962.
- [10] H. K. Rockstad, T. W. Kenny, P. J. Kelly, T. B. Gabrielson, M. J. Berliner, and J. F. Lindberg, "A microfabricated electron-tunneling accelerometer as a directional underwater acoustic sensor," *AIP Conf. Proc.*, vol. 368, no. 1, pp. 57–68, Apr. 1996.
- [11] R. Abdolvand, B. V. Amini, and F. Ayazi, "Sub-Micro-Gravity In-Plane Accelerometers With Reduced Capacitive Gaps and Extra Seismic Mass," *J. Microelectromechanical Syst.*, vol. 16, no. 5, pp. 1036–1043, Oct. 2007.
- [12] R. Gholamzadeh, K. Jafari, and M. Gharooni, "Design, simulation and fabrication of a MEMS accelerometer by using sequential and pulsed-mode DRIE processes," *J. Micromechanics Microengineering*, vol. 27, no. 1, p. 015022, 2017.
- [13] L. M. Roylance and J. B. Angell, "A batch-fabricated silicon accelerometer," *IEEE Trans. Electron Devices*, vol. 26, no. 12, pp. 1911–1917, Dec. 1979.
- [14] "MEMS Market Tracker-Q3 2015." .
- [15] "High-End Gyroscopes, Accelerometers and IMUs for Defense, Aerospace & Industrial." Yole Developpement, 2015.
- [16] D. J. Inman, *Engineering Vibration*. Prentice Hall, 2001.
- [17] S. D. Senturia, *Microsystem Design*. Springer Science & Business Media, 2007.
- [18] T. B. Gabrielson, "Mechanical-thermal noise in micromachined acoustic and vibration sensors," *IEEE Trans. Electron Devices*, vol. 40, no. 5, pp. 903–909, May 1993.
- [19] F. Mohd-Yasin, D. J. Nagel, and C. E. Korman, "Noise in MEMS," *Meas. Sci. Technol.*, vol. 21, no. 1, p. 012001, 2010.
- [20] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "Noise analysis and characterization of a sigma-delta capacitive microaccelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 352–361, Feb. 2006.
- [21] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proc. IEEE*, vol. 86, no. 8, pp. 1640–1659, Aug. 1998.

- [22] A. L. Roy and T. K. Bhattacharyya, "Design, fabrication and characterization of high performance SOI MEMS piezoresistive accelerometers," *Microsyst. Technol.*, vol. 21, no. 1, pp. 55–63, Jan. 2015.
- [23] S. Huang *et al.*, "A high-performance micromachined piezoresistive accelerometer with axially stressed tiny beams," *J. Micromechanics Microengineering*, vol. 15, no. 5, p. 993, 2005.
- [24] Y. Li, Q. Zheng, Y. Hu, and Y. Xu, "Micromachined Piezoresistive Accelerometers Based on an Asymmetrically Gapped Cantilever," *J. Microelectromechanical Syst.*, vol. 20, no. 1, pp. 83–94, Feb. 2011.
- [25] S. Beeby, *MEMS Mechanical Sensors*. Artech House, 2004.
- [26] C. Tse *et al.*, *Design of a Power Scalable Capacitive MEMS Accelerometer Front End*. .
- [27] R. F. Yazıcıoğlu and T. Supervisor: Akin, *Surface micromachined capacitive accelerometers using memstechnology*. Ankara: METU, 2003.
- [28] G. Krishnan, C. U. Kshirsagar, G. K. Ananthasuresh, and N. Bhat, "Micromachined High-Resolution Accelerometers," *J. Indian Inst. Sci.*, vol. 87, no. 3, p. 333, Dec. 2012.
- [29] V. Kempe, *Inertial MEMS: Principles and Practice*. Cambridge University Press, 2011.
- [30] A. Corigliano, R. Ardito, C. Comi, A. Frangi, A. Ghisi, and S. Mariani, "Microsystems and Mechanics," *Procedia IUTAM*, vol. 10, pp. 138–160, Jan. 2014.
- [31] F. Edalatfar, S. Hajhashemi, B. Yaghootkar, and B. Bahreyni, "Dual mode resonant capacitive MEMS accelerometer," in *2016 IEEE International Symposium on Inertial Sensors and Systems*, 2016, pp. 97–100.
- [32] A. A. Seshia *et al.*, "A vacuum packaged surface micromachined resonant accelerometer," *J. Microelectromechanical Syst.*, vol. 11, no. 6, pp. 784–793, Dec. 2002.
- [33] R. Hiratsuka, D. C. van Duyn, T. Otaredian, and P. de Vries, "A novel accelerometer based on a silicon thermopile," in *1991 International Conference on Solid-State Sensors and Actuators, 1991. Digest of Technical Papers, TRANSDUCERS '91*, 1991, pp. 420–423.
- [34] U. A. Dauderstädt, P. J. French, and P. M. Sarro, "Temperature Dependence of a Thermal Accelerometer," in *Sensor Technology in the Netherlands: State of the Art*, Springer, Dordrecht, 1998, pp. 55–60.
- [35] V. Milanovi *et al.*, *Convection-based Accelerometer and Tilt Sensor Implemented in Standard CMOS*. .
- [36] J. Bahari, J. D. Jones, and A. M. Leung, "Sensitivity Improvement of Micromachined Convective Accelerometers," *J. Microelectromechanical Syst.*, vol. 21, no. 3, pp. 646–655, Jun. 2012.
- [37] R. Mukherjee, J. Basu, P. Mandal, and P. K. Guha, "A review of micromachined thermal accelerometers," *J. Micromechanics Microengineering*, vol. 27, no. 12, p. 123002, 2017.
- [38] F. A. Levinzon, "Ultra-Low-Noise Seismic Piezoelectric Accelerometer With Integral FET Amplifier," *IEEE Sens. J.*, vol. 12, no. 6, pp. 2262–2268, Jun. 2012.
- [39] "PCB Model 333B30," *PCB PIEZOTRONICS*, 16-Dec-2017. [Online]. Available: <https://www.pcb.com/products.aspx?m=333B30>. [Accessed: 16-Dec-2017].
- [40] T. Vohra, B. Danver, A. Tveten, and A. Dandridge, "High performance fibre optic accelerometers," *Electron. Lett.*, vol. 33, no. 2, pp. 155–157, Jan. 1997.
- [41] A. G. Krause, M. Winger, T. D. Blasius, Q. Lin, and O. Painter, "A microchip optomechanical accelerometer," *Nat. Photonics*, vol. 6, no. 11, pp. 768–772, Oct. 2012.

- [42] K. Zandi, J. Zou, B. Wong, R. V. Kruzelecky, and Y. A. Peter, "VOA-based optical MEMS accelerometer," in *16th International Conference on Optical MEMS and Nanophotonics*, 2011, pp. 15–16.
- [43] F. Guzmán Cervantes, L. Kumanchik, J. Pratt, and J. M. Taylor, "High sensitivity optomechanical reference accelerometer over 10 kHz," *Appl. Phys. Lett.*, vol. 104, no. 22, p. 221111, Jun. 2014.
- [44] H. K. Rockstad, T. W. Kenny, J. K. Reynolds, W. J. Kaiser, and T. B. Gabrielson, "A miniature high-sensitivity broad-band accelerometer based on electron tunneling transducers," *Sens. Actuators Phys.*, vol. 43, no. 1, pp. 107–114, May 1994.
- [45] C.-H. Liu *et al.*, "Characterization of a high-sensitivity micromachined tunneling accelerometer with micro-g resolution," *J. Microelectromechanical Syst.*, vol. 7, no. 2, pp. 235–244, Jun. 1998.
- [46] C.-H. Liu and T. W. Kenny, "A high-precision, wide-bandwidth micromachined tunneling accelerometer," *J. Microelectromechanical Syst.*, vol. 10, no. 3, pp. 425–433, Sep. 2001.
- [47] X. Zou and A. A. Seshia, "A high-resolution resonant MEMS accelerometer," in *2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, 2015, pp. 1247–1250.
- [48] X. Zou, P. Thiruvengathan, and A. A. Seshia, "A Seismic-Grade Resonant MEMS Accelerometer," *J. Microelectromechanical Syst.*, vol. 23, no. 4, pp. 768–770, Aug. 2014.
- [49] J. Gannon, H. Pham, and K. Speller, *A Robust Low Noise MEMS Servo Accelerometer*. .
- [50] "Colibrys - MEMS Accelerometers," *Colibrys – MEMS Accelerometers*. [Online]. Available: <http://www.colibrys.com/>. [Accessed: 28-Apr-2017].
- [51] R. G. Walmsley, L. K. Kiyama, D. M. Milligan, R. L. Alley, D. L. Erickson, and P. G. Hartwell, "Micro-G silicon accelerometer using surface electrodes," in *2009 IEEE Sensors*, 2009, pp. 971–974.
- [52] D. J. Milligan, B. D. Homeijer, and R. G. Walmsley, "An ultra-low noise MEMS accelerometer for seismic imaging," in *2011 IEEE SENSORS Proceedings*, 2011, pp. 1281–1284.
- [53] "Three-phase capacitive position sensing - IEEE Conference Publication." [Online]. Available: <http://ieeexplore.ieee.org/document/5690265/>. [Accessed: 18-Dec-2017].
- [54] J. Laine and D. Mougnot, "A high-sensitivity MEMS-based accelerometer," *Lead. Edge*, vol. 33, no. 11, pp. 1234–1242, Nov. 2014.
- [55] "Sercel - Seismic acquisition systems," 2017. [Online]. Available: <http://www.sercel.com/Pages/default.aspx>. [Accessed: 28-Apr-2017].
- [56] J. Gannon, H. Pham, and K. Speller, "A Robust Low Noise MEMS Servo Accelerometer." Technical Paper of the Applied MEMS Inc., 2001.
- [57] L. Aaltonen and K. Halonen, "Continuous-time interface for a micromachined capacitive accelerometer with NEA of 4 g and bandwidth of 300 Hz," *Sens. Actuators Phys.*, vol. 154, no. 1, pp. 46–56, Aug. 2009.
- [58] J. Bernstein, R. Miller, W. Kelley, and P. Ward, "Low-noise MEMS vibration sensor for geophysical applications," *J. Microelectromechanical Syst.*, vol. 8, no. 4, pp. 433–438, Dec. 1999.
- [59] M. Yucetas, M. Pulkkinen, A. Kalanti, J. Salomaa, L. Aaltonen, and K. Halonen, "A High-Resolution Accelerometer With Electrostatic Damping and Improved Supply Sensitivity," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1721–1730, Jul. 2012.
- [60] Q. Hu, C. Gao, Y. Hao, Y. Zhang, and G. Yang, "Low cross-axis sensitivity micro-gravity microelectromechanical system sandwich capacitance accelerometer," *IET Micro Nano Lett.*, vol. 6, no. 7, pp. 510–514, Jul. 2011.

- [61] J. Xie, M. Song, and W. Yuan, "A high sensitivity micromachined accelerometer with an enhanced inertial mass SOI MEMS process," in *The 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems*, 2013, pp. 336–339.
- [62] N. R. Council, *Ocean Noise and Marine Mammals*. 2003.
- [63] M. A. Rasouli, "Employing piezjunction effect for resonant micro-device applications," Thesis, Applied Sciences: School of Mechatronic Systems Engineering, 2016.
- [64] R. Budynas, W. Young, and A. Sadegh, *Roark's Formulas for Stress and Strain, 8th Edition*. McGraw-Hill Education, 2011.
- [65] F. Edalatfar, B. Yaghootkar, A. Q. A. Qureshi, S. Azimi, and B. Bahreyni, "Design, fabrication and characterization of a high performance MEMS accelerometer," in *2016 IEEE SENSORS*, 2016, pp. 1–3.
- [66] F. Edalatfar *et al.*, "A Wideband, Low-noise Accelerometer for Sonar Wave Detection," *IEEE Sens. J.*, vol. PP, no. 99, pp. 1–1, 2017.
- [67] F. Edalatfar, S. Azimi, A. Q. A. Qureshi, B. Yaghootkar, and B. Bahreyni, "Wideband, low-noise accelerometer with open loop dynamic range of better than 135DB," in *2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, 2017, pp. 1187–1190.
- [68] "Glass Wafers, Fused Silica Wafers and substrates from Plan Optik AG." [Online]. Available: http://www.planoptik.com/en/products/borosilicate_standard.html. [Accessed: 03-Dec-2017].
- [69] *MEMS Materials and Processes Handbook | Reza Ghodssi | Springer*. .
- [70] "MicraGEM-Si™ – SOI MEMS Process," *Micralyne*. [Online]. Available: <https://www.micralyne.com/technology-platforms/micragem-si/>. [Accessed: 03-Dec-2017].
- [71] "PVD 3 - 4D LABS Nanofabrication." [Online]. Available: <https://users.4dlabs.ca/tools/pvd3.html>. [Accessed: 03-Dec-2017].
- [72] "RIE 2 - 4D LABS Nanofabrication." [Online]. Available: <https://users.4dlabs.ca/tools/rie2.html>. [Accessed: 03-Dec-2017].
- [73] Z. Cui, "Anodic Bonding," in *Encyclopedia of Microfluidics and Nanofluidics*, D. L. Prof, Ed. Springer US, 2008, pp. 50–54.
- [74] M. Shayan, B. Arezoo, A. S. Vanini, and A. A. Kotamjani, "Silicon (100) undercutting modelling and corner compensation structures design in wet anisotropic etching process," *Proc. Inst. Mech. Eng. Part B J. Eng. Manuf.*, vol. 225, no. 7, pp. 1041–1049, Jul. 2011.
- [75] "KOH Etching Chucks / Wet Etching – AMMT." [Online]. Available: <http://www.ammt.com/products/wet-etching/>. [Accessed: 03-Dec-2017].
- [76] "HF Vapor Phase Etcher." [Online]. Available: <https://www.idonus.com/activities/products/mems-products/hf-vapor-phase-etcher.html>. [Accessed: 03-Dec-2017].
- [77] F. Fukuyo, K. Fukumitsu, and N. Uchiyama, "Stealth Dicing Technology and Applications," presented at the 6th Int. Symp. Laser Precision Microfabrication, 2005.
- [78] Y. Tang, A. Sandoughsaz, and K. Najafi, "Ultra high aspect-ratio and thick deep silicon etching (UDRIE)," in *2017 IEEE 30th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2017, pp. 700–703.
- [79] M. Darnon, "2 - Plasma Etching in Microelectronics," in *Plasma Etching Processes for CMOS Devices Realization*, N. Posseme, Ed. Elsevier, 2017, pp. 23–58.

- [80] K. Najafi, "Micropackaging Technologies for Integrated Microsystems: Applications to MEMS and MOEMS," presented at the Micromachining and Microfabrication Process Technology VIII, 2003, vol. 4979, pp. 1–20.
- [81] Y. Zhang, "MEMS Hermetic Packaging for Extremely Sensitive Accelerometers with In-Package Pressure Sensing Solution," Thesis, Applied Sciences: School of Mechatronic Systems Engineering, 2016.
- [82] "SRO-700 TABLE TOP – IR VACUUM REFLOW SYSTEM," *ATV Technologie GmbH*. [Online]. Available: <https://www.atv-tech.com/sro-700>. [Accessed: 01-Dec-2017].
- [83] "Irvine Sensors ASIC." [Online]. Available: http://www.irvine-sensors.com/sensor_asic. [Accessed: 25-May-2017].
- [84] P. Rantakari, J. Kiihamäki, M. Koskenvuori, T. Lamminmäki, and I. Tittonen, "Reducing the Effect of Parasitic Capacitance on MEMS Measurements," in *Transducers '01 Eurosensors XV*, Springer, Berlin, Heidelberg, 2001, pp. 1528–1531.
- [85] "HF2LI Lock-in Amplifier," *Zurich Instruments*, 10-Mar-2015. [Online]. Available: <https://www.zhinst.com/products/hf2li>. [Accessed: 19-Dec-2017].
- [86] B. Bahreyni, "Chapter 6 - Damping Mechanisms," in *Fabrication and Design of Resonant Microdevices*, Norwich, NY: William Andrew Publishing, 2009, pp. 113–128.
- [87] M. Bao and H. Yang, "Squeeze film air damping in MEMS," *Sens. Actuators Phys.*, vol. 136, no. 1, pp. 3–27, May 2007.
- [88] Z. Hao, "Anchor Loss in MEMS/NEMS," in *Encyclopedia of Nanotechnology*, Springer, Dordrecht, 2016, pp. 123–130.
- [89] W.-T. Chang, "Static and Motional Feedthrough Capacitance of Flexural Microresonator," *Active and Passive Electronic Components*, 2011. [Online]. Available: <https://www.hindawi.com/journals/apec/2011/546986/>. [Accessed: 12-Jan-2018].
- [90] J. E.-Y. Lee, *Silicon Micromechanical Resonators for Measurements of Mass and Charge*. University of Cambridge, 2009.
- [91] "Accelerometer Terminology Guide." Freescale Semiconductor Inc., May-2007.
- [92] C. Angulo, E. G. Vadillo, and J. Canales, "Optimization of structures with frequency and mode shape constraints," *Eng. Comput.*, vol. 11, no. 1, pp. 81–91, Jan. 1994.
- [93] "A modal-based approach for optimal active modifications of resonance modes - ScienceDirect." [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0022460X14007196>. [Accessed: 22-Dec-2017].
- [94] Z.-D. Ma, N. Kikuchi, and I. Hagiwara, "Structural topology and shape optimization for a frequency response problem," *Comput. Mech.*, vol. 13, no. 3, pp. 157–174, Dec. 1993.
- [95] J. D. Deaton and R. V. Grandhi, "A survey of structural and multidisciplinary continuum topology optimization: post 2000," *Struct. Multidiscip. Optim.*, vol. 49, no. 1, pp. 1–38, Jan. 2014.
- [96] S. Zargham, T. A. Ward, R. Ramli, and I. A. Badruddin, "Topology optimization: a review for structural designs under vibration problems," *Struct. Multidiscip. Optim.*, vol. 53, no. 6, pp. 1157–1177, Jun. 2016.
- [97] "Efficient topology optimization in MATLAB using 88 lines of code | www.TopOpt.dtu.dk." [Online]. Available: <http://www.topopt.dtu.dk/?q=node/751>. [Accessed: 22-Dec-2017].

- [98] "Topology Optimization of Stressed Capacitive RF MEMS Switches - IEEE Journals & Magazine." [Online]. Available: <http://ieeexplore.ieee.org/document/6353106/>. [Accessed: 22-Dec-2017].
- [99] Y. M. Xie and G. P. Steven, "Evolutionary structural optimization for dynamic problems," *Comput. Struct.*, vol. 58, no. 6, pp. 1067–1073, Mar. 1996.
- [100] Y. Maeda, S. Nishiwaki, K. Izui, M. Yoshimura, K. Matsui, and K. Terada, "Structural topology optimization of vibrating structures with specified eigenfrequencies and eigenmode shapes," *Int. J. Numer. Methods Eng.*, vol. 67, no. 5, pp. 597–628, Jul. 2006.
- [101] N. L. Pedersen, "Maximization of eigenvalues using topology optimization," *Struct. Multidiscip. Optim.*, vol. 20, no. 1, pp. 2–11, Aug. 2000.
- [102] R. Meske, B. Lauber, and E. Schnack, "A new optimality criteria method for shape optimization of natural frequency problems," *Struct. Multidiscip. Optim.*, vol. 31, no. 4, pp. 295–310, Apr. 2006.
- [103] "Structural design for desired eigenfrequencies and mode shapes using topology optimization | SpringerLink." [Online]. Available: <https://link.springer.com/article/10.1007/s00158-012-0840-2>. [Accessed: 22-Dec-2017].
- [104] "A level set method for shape and topology optimization of both structure and support of continuum structures - ScienceDirect." [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0045782514000279>. [Accessed: 22-Dec-2017].
- [105] "Optimization of support positions to maximize the fundamental frequency of structures - Wang - 2004 - International Journal for Numerical Methods in Engineering - Wiley Online Library." [Online]. Available: <http://onlinelibrary.wiley.com/doi/10.1002/nme.1124/full>. [Accessed: 22-Dec-2017].
- [106] J.-L. Marcelin, "Optimization of the boundary conditions by genetic algorithms," *Int. Rev. Mech. Eng.*, vol. 6, no. 1, pp. 50–54, Feb. 2012.
- [107] J. H. Son and B. M. Kwak, "Optimization of boundary conditions for maximum fundamental frequency of vibrating structures," *AIAA J.*, vol. 31, no. 12, pp. 2351–2357, 1993.
- [108] A. R. Inzarulfaisham and H. Azegami, "Solution to boundary shape optimization problem of linear elastic continua with prescribed natural vibration mode shapes," *Struct. Multidiscip. Optim.*, vol. 27, no. 3, pp. 210–217, May 2004.

Appendix A. Fabrication Process

Out-of-Plane Accelerometers, Square Membrane Prototypes

a) SOI wafer Process

#	Process Step	Process Detail
1	Oxidation	
1.1	RCA Clean	Putting Glass and Silicon Wafer in 85°C Solution of DI Water, Amonium Hydroxide, and Hydrogen Peroxide with relative proportion of 5:1:1 for 15 minute
1.2	Oxidation	400nm of thermal oxide
2	Nitride Deposition	120nm of PECVD oxide
3	Wafer Preparing	
3.1	RCA cleaning	Putting Glass and Silicon Wafer in 85°C Solution of DI Water, Amonium Hydroxide, and Hydrogen Peroxide with relative proportion of 5:1:1 for 15 minute
3.2	Front side Nitride Removal by RIE	4D lab, RIE2 machine, Reciepe R1, etching nitride for 5 minute
3.3	Front side oxide removal	HF 49% >> etch rate of oxide: 70 nm/min ; etch for 10 min
4	Lithography (Mask 1: Cavity)	Front Side
4.1	Spin photoresist on back side	3500 rpm for 30 second, Shipley Resist 1813
4.2	Soft Bake	90 seconds on hot plate @115 °C
4.3	Spin photoresist on Top side	3500 rpm for 30 second, Shipley Resist 1813
4.4	Soft Bake	90 seconds on hot plate @115 °C
4.5	Lithography	8 seconds exposure
4.6	Development	MF-319, end time is specified visually
4.7	Inspection	Measure thickness of the resist using optical profilometer and see the structures under the microscope
4.8	Hard Bake	90 seconds on hot plate @115 °C
4.9	RIE etching	4D lab, RIE2 machine, Reciepe R1, etching silicon for for 9 minute(700 nm)
4.10	Photoresist stripping	Using Acetone
4.11	Inspection	Measure depth of the etched profile using optical profilometer and inspect features under the microscope
5	Lithography (Mask 2: Dimples)	Front Side
5.1	Spin photoresist on back side	3500 rpm for 30 second, Shipley Resist 1813

#	Process Step	Process Detail
5.2	Soft Bake	90 seconds on hot plate @115 °C
5.3	Spin photoresist on Top side	3500 rpm for 30 second, Shipley Resist 1813
5.4	Soft Bake	90 seconds on hot plate @115 °C
5.5	Lithography	8 seconds exposure
5.6	Development	MF-319, end time is specified visually
5.7	Inspection	Measure thickness of the resist using optical profilometer and see the structures under the microscope
5.8	Hard Bake	90 seconds on hot plate @115 °C
5.9	RIE etching	4D lab, RIE2 machine, Reciepe R1, etching silicon for for 2 minute(150 nm)
5.10	Photoresist stripping	Using Acetone
5.11	Inspection	Measure depth of the etched profile using optical profilometer and inspect features under the microscope
6	Lithography (Mask 3: Contact Cuts)	Front Side
6.1	Spin photoresist on back side	3500 rpm for 30 second, Shipley Resist 1813
6.2	Soft Bake	90 seconds on hot plate @115 °C
6.3	Spin photoresist on Top side	3500 rpm for 30 second, Shipley Resist 1813
6.4	Soft Bake	90 seconds on hot plate @115 °C
6.5	Lithography	8 seconds exposure
6.6	Development	MF-319, end time is specified visually
6.7	Inspection	Measure thickness of the resist using optical profilometer and see the structures under the microscope
6.8	Hard Bake	90 seconds on hot plate @115 °C
6.9	RIE etching	4D lab, etching silicon by Xe2F, do it for 45 cycle(etch rate is around 2micron/10 cycle and we want to etch 8 micron, all the device layer)
6.10	Photoresist stripping	Using Acetone
6.11	Inspection	Measure depth of the etched profile using optical profilometer and inspect features under the microscope
7	Lithography (Mask 4: Proof Mass)	Back Side
7.1	Spin photoresist on Top side	3500 rpm for 30 second, Shipley Resist 1813
7.2	Soft Bake	90 seconds on hot plate @115 °C
7.3	Spin photoresist on back side	3500 rpm for 30 second, Shipley Resist 1813
7.4	Soft Bake	90 seconds on hot plate @115 °C
7.5	Lithography	8 seconds exposure – Back to front alignment
7.6	Development	MF-319, end time is specified visually

#	Process Step	Process Detail
7.7	Inspection	Measure thickness of the resist using optical profilometer and see the structures under the microscope
7.8	Hard Bake	90 seconds on hot plate @115 °C
7.9	RIE etching	4D lab, RIE2 machine, Reciepe R1, etching nitride for 5 minute
7.10	Photoresist stripping	Using Acetone
7.11	Inspection	Measure depth of the etched profile using optical profilometer and inspect features under the microscope
7.12	HF etching	HF 49% >> etch rate of oxide: 70 nm/min ; etch for 10 min
7.13	RCA cleaning	Putting Glass and Silicon Wafer in 85°C Solution of DI Water, Amonium Hydroxide, and Hydrogen Peroxide with relative proportion of 5:1:1 for 15 minute
7.14	Aligning glass wafer and Silicon Wafer	Using Mask aligner
7.15	Anodic Bonding	at 400°C and 600 volt
7.16	KOH etching	Putting wafer in 30% KOH solution @80°C for around 6 hours
7.17	Inspection	Measure depth of the etched profile using optical profilometer
7.18	Dicing	Using laser cutting machine

b) Glass Wafer Process

#	Process Step	Process Details
1	1. Lithography (Mask 5: Electrodes)	Front Side
1.1	RCA clean	Putting Glass and Silicon Wafer in 85°C Solution of DI Water, Amonium Hydroxide, and Hydrogen Peroxide with relative proportion of 5:1:1 for 15 minute
1.2	Spin photoresist	3500 rpm for 90 second, LOR resist
1.3	Soft Bake 1	4 min on hot plate @180 °C
1.4	Spin Photoresist	3500 rpm for 30 second, Shipley 1813 resist
1.5	Soft Bake 2	90 sec on hot plate @115 °C
1.6	Development	MF-319, end time is specified visually until the top photoresist has been removed
1.7	Hard Bake 1	
1.8	Development	MF-319, for about 2 min

#	Process Step	Process Details
1.9	Hard Bake 2	
1.10	Inspection	Measure thickness of the resist using optical profilometer
1.11	Metal Deposition	4D lab,PVD 3 machine, subsequently 50 nm Ti, 50 nm Pt, 200 nm Au
1.12	Photoresist stripping	30 minute in remover-PG @75°C along with sonicating

Out-of-Plane Accelerometers, Circular Membrane Prototypes

a) Glass Wafer Process

#	Process Step	Process Details
1.	Cleaning	These steps are better to be repeated twice. Surface cleanness is critical for having a good film deposition
1.1	Acetone bath	Soak in Acetone Ultrasonic bath at room temperature for 10 min
1.2	IPA bath	Soak in IPA Ultrasonic bath at room temperature for 10 min
2.	Hard mask deposition (Amorphous Silicon)	Deposit a layer of a-Si with the thickness of 600-700nm using PECVD Note: In order to have a film with no pinholes, it's better to do the film deposition in two steps of 1000 Sec.
3.	First Lithography for Cavity	
3.1	Dehydration of the glass wafer	@180°C for 15 min
3.2	HDMS coating	For 5 min
3.3	Spin coating PR	
3.4	Exposure	for 2.3 Sec
3.5	Development	for 80-90 Sec
3.6	Opening windows for etching cavities	
3.7	RIE	O2:4mTorr, CF4: 40mTorr, Pressure: 100mTorr, Power:100W for 4-5 min
3.8	Vapor HF etching	Dehydration of the glass wafer@150°C for 15 min. VHF etching @45°C for 1 minutes and

#	Process Step	Process Details
		40 seconds for 2.9 um depth. Note: Dehydration is important for having a smooth surface. It also effects the etching time.
3.9	Photoresist layer stripping	Soak in Acetone Ultrasonic bath at room temperature for 10 min & Soak in IPA Ultrasonic bath at room temperature for 10 min
3.10	Inspection	Inspect the quality of the a-Si after VHF optically. Sometimes the a-Si would be affected by VHF. NOTE: If the quality of a-Si layer is perfect leave it as a protection layer for the back-side lithography. Strip it using KOH in case you have any doubts before proceeding to the next step
4.	Second Lithography: Back-side metallization	
4.1	RCA cleaning	
4.2	Dehydration	@180°C for 15min
4.3	HDMS coating	
4.4	Coating with LOR2A	Use GLOR recipe at 4D labs
4.5	Soft Bake	@180°C for 4 min
4.6	Cool down	For 3 min
4.7	Photoresist Spin Coating	Use MB4 recipe at 4D labs
4.8	Soft Bake	@110°C for 1 min
4.9	Cool down	For 2 min
4.10	Exposure	For 2.3 Sec
4.11	Hard bake	@110°C for 2 min
4.12	Development	MF-319 for 80-90 seconds
5.	Metallization	PVD 3 E-Beam metallization 1) Ti: 20 nm (deposition rate: 0.5 Å/s) 2) Pt: 20 nm (deposition rate: 0.2 Å/s) 3) Au: 150 nm (deposition rate: 1.1-1.5 Å/s) Note: Do not exceed these deposition rates.
6.	Lift Off Process	Leave the sample in 1160 stripper @60°C for 45min to 1 hour.

#	Process Step	Process Details
7.	a-Si removal	Leave in 33% KOH solution @80°C for 30Sec
8.	Third Lithography: Electrode metallization	
8.1	RCA cleaning	
8.2	Dehydration	@180°C for 15min
8.3	HDMS coating	
8.4	Coating with LOR2A	Use GLOR recipe at 4D labs
8.5	Soft Bake	@180°C for 4 min
8.6	Cool down	For 3 min
8.9	Photoresist Spin Coating	Use MB4 recipe at 4D labs
8.10	Soft Bake	@110°C for 1 min
8.11	Cool down	For 2 min
8.12	Exposure	For 2.3 Sec
8.13	Hard bake	@110°C for 2 min
8.14	Development	MF-319 for 80-90 seconds
9.	Metallization	PVD 3 E-Beam metallization 1) Ti: 20 nm (deposition rate: 0.5 A ⁰ /s) 2) Pt: 20 nm (deposition rate: 0.2 A ⁰ /s) 3) Au: 150 nm (deposition rate: 1.1-1.5 A ⁰ /s) Note: Do not exceed these deposition rates.
10.	Lift Off Process	Leave the sample in 1160 stripper @60°C for 45min to 1 hour.

b) SOI wafer Process

#	Process Step	Process Details
1	RCA cleaning	Putting Silicon Wafer in 85°C Solution of DI Water, Amonium Hydroxide, and Hydrogen Peroxide with relative proportion of 5:1:1 for 15 minute
2	Lithography (Mask 1: Dimples)	Front Side
2.1	Spin photoresist on back side	3500 rpm for 30 second, Shipley Resist 1813
2.2	Soft Bake	90 seconds on hot plate @115 °C
2.3	Spin photoresist on Top side	3500 rpm for 30 second, Shipley Resist 1813
2.4	Soft Bake	90 seconds on hot plate @115 °C
2.5	Lithography	8 seconds exposure
2.6	Development	MF-319, end time is specified visually
2.7	Inspection	Measure thickness of the resist using optical profilometer and see the structures under the microscope
2.8	Hard Bake	90 seconds on hot plate @115 °C
2.9	RIE etching	4D lab, RIE2 machine, Recipe R1, etching silicon for 2 minute(150 nm)
2.10	Photoresist stripping	Using Acetone
2.11	Inspection	Measure depth of the etched profile using optical profilometer and inspect features under the microscope
3.	Lithography (Mask 3: Contact Cuts)	Front Side
3.1	Spin photoresist on back side	3500 rpm for 30 second, Shipley Resist 1813
3.2	Soft Bake	90 seconds on hot plate @115 °C
3.3	Spin photoresist on Top side	3500 rpm for 30 second, Shipley Resist 1813
3.4	Soft Bake	90 seconds on hot plate @115 °C
3.5	Lithography	8 seconds exposure
3.6	Development	MF-319, end time is specified visually
3.7	Inspection	Measure thickness of the resist using optical profilometer and see the structures under the microscope
3.8	Hard Bake	90 seconds on hot plate @115 °C
3.9	RIE etching	4D lab, etching silicon by Xe2F, do it for 45 cycle(etch rate is around 2micron/10 cycle and we want to etch 8 micron, all the device layer)
3.10	Photoresist stripping	Using Acetone
3.11	Inspection	Measure depth of the etched profile using optical profilometer and inspect features under the microscope

c) Integrated Wafer Process

#	Process Step	Process Details
1	RCA cleaning	Putting Glass and Silicon Wafer in 85°C Solution of DI Water, Amonium Hydroxide, and Hydrogen Peroxide with relative proportion of 5:1:1 for 15 minute
2	Aligning glass wafer and Silicon Wafer	Using Mask aligner
3	Anodic Bonding	at 400°C and 600 volt (the voltage depends on the applied area)
4	Inspection	Measure depth of the etched profile using optical profilometer
5	Lithography (Mask 4: Backside)	Backside
5.1	Spin Thick Photoresist on the backside	
5.2	DRIE	
5.3	Inspection	Measure depth of the etched profiles
6	Dicing	Using laser cutting machine

Appendix B. Fabrication Issues

Prototype I

An example of fabrication issues in in-plane accelerometers prototype I is shown in Figure 1 – a and b. These pictures shows the comb fingers of the device are broken due to notching at Si/Oxide interface. Notching is a localized undercutting of silicon at the silicon/insulator interface. Due to the fact that for a set of comb finger, narrow and wide gaps are located beside each other, the notching effect was also aggravated by the aspect ratio dependent etching (ARDE) effects. In ARDE, wider features are etched faster and reached the insulating layer faster than the narrower features [79]. A sample of ARDE phenomenon is shown in Figure 2.

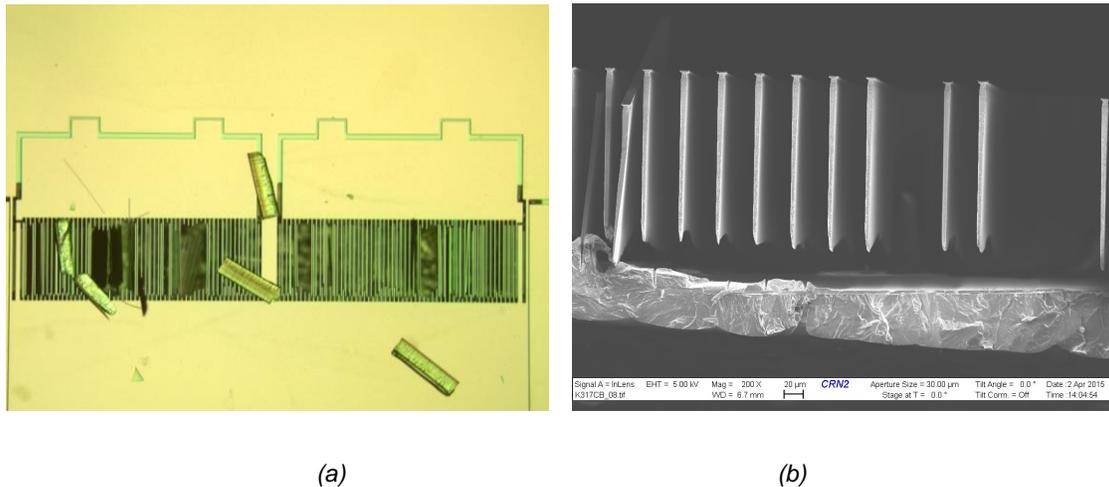


Figure B - 1- a) Broken fingers in in-plane accelerometer, b) SEM image from the combs cross section of the not working in-plane accelerometers

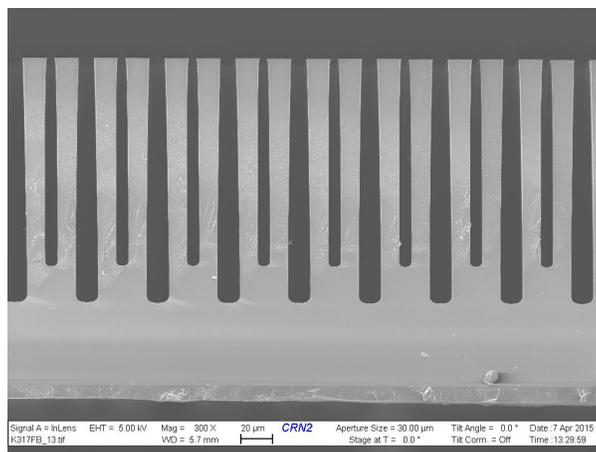


Figure B - 2 - A sample of ARDE phenomenon in Si etching

Prototype III

In the first round of prototype III fabrication, various issues were come up which were leaded to different types of defects. The identified defects can be divided into five categories. The first category is the star shape defects. Figure 3 shows the star shape defects under the microscope and SEM machine. It seemed that star shape defects were the result of wafer bombardment before DRIE by particles. The bombardment caused the photo resist to scattered around the bombarded point and consequently after DRIE etching, it caused deep trenches to form.

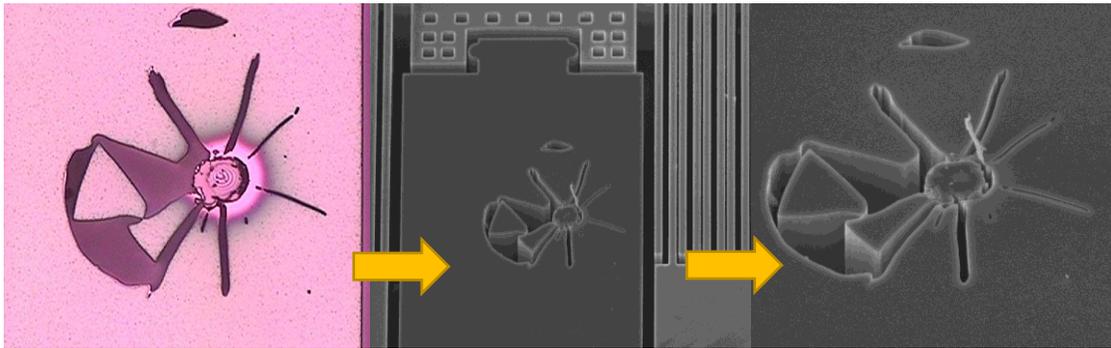


Figure B - 3– Star shape defects in prototype III fabrication

In order to have better understanding of the source of defect, an elemental analysis using SEM was performed. According to the result of the analysis, shown in Figure 4, Silicon, Oxygen and Carbon were the 3 top abundant materials in the defect area. Carbon is the sign of existence of photoresist.

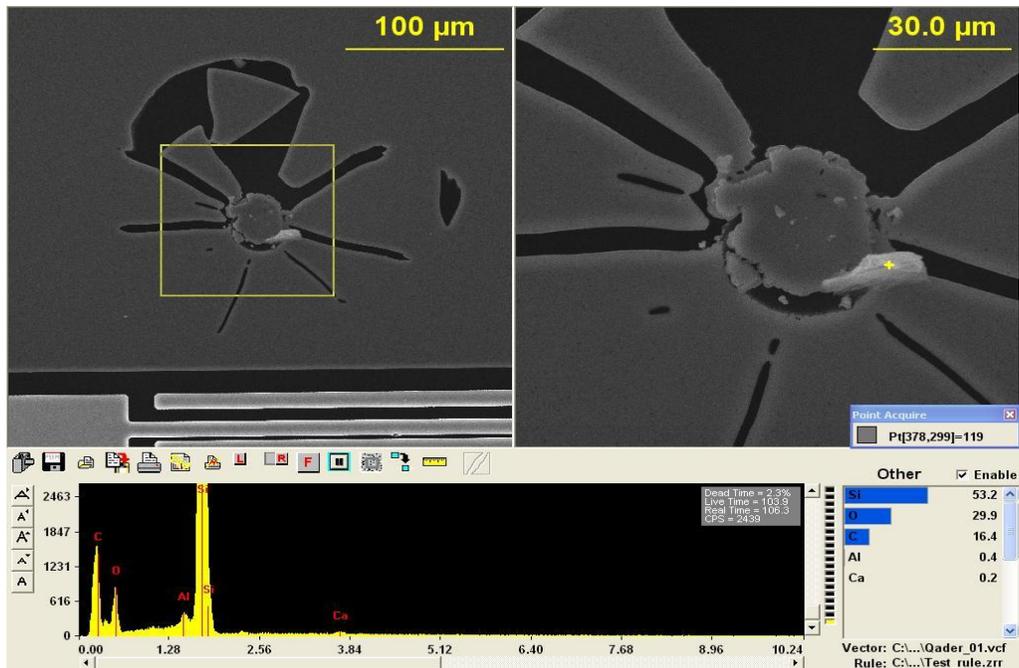


Figure B - 4 – Star Shaped defects

The second category of the defects was unetched holes covered by the clogs shown in Figure 5. In order to identify the nature of the deposited clog on the wafer, an element analysis using SEM machine was performed. Based on the analysis, as shown in Figure 6, the deposited clog on the wafer was Al_2O_3 . In the first fabrication round, Al_2O_3 , was used as the masking material for DRIE. These defects showed that the Aluminum deposition chamber was polluted with Al_2O_3 particles.

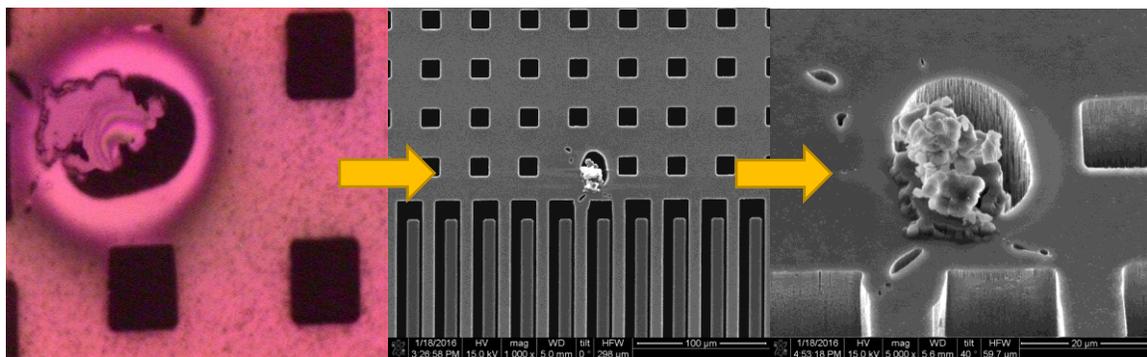


Figure B - 5 - Unetched holes covered by Al_2O_3

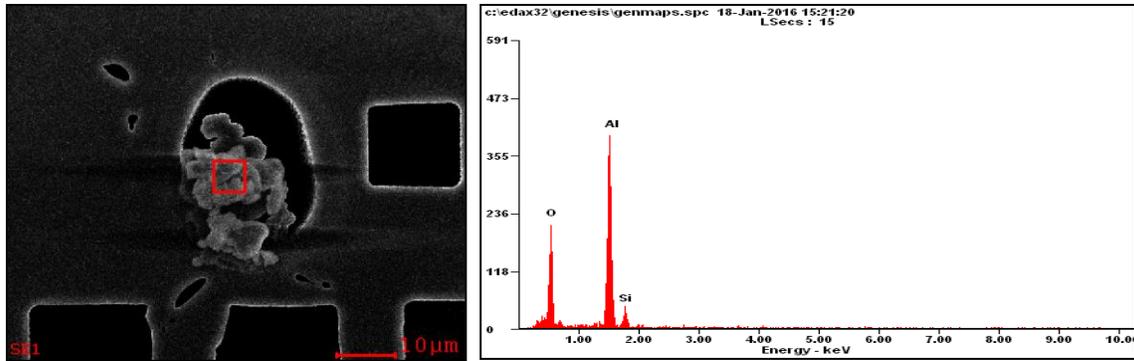


Figure B - 6 - Un-etched holes element analysis

The third category of the defects was the big holes on the wafer. Figure 7 shows the SEM image of these defects. As it is evident from the SEM results, at the bottom of the holes, the traces of the etch holes are distinguishable. Based on these pictures, this incident was happened after DRIE step.

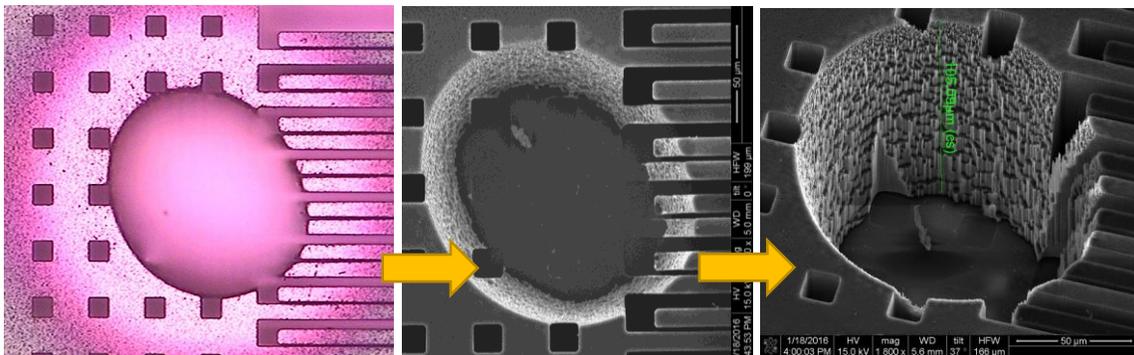


Figure B - 7 - Big hole defects

The element analysis of the wall of the big holes only showed silicon. The results are shown in Figure 8. After investigations, it was concluded that this incident was due to the voids in the SOI wafer which caused the localized heating during DRIE. Upon communications with quality control of the wafer provider company, it was turned out that one of their SOI wafer batches, which we had used, had the void problems.

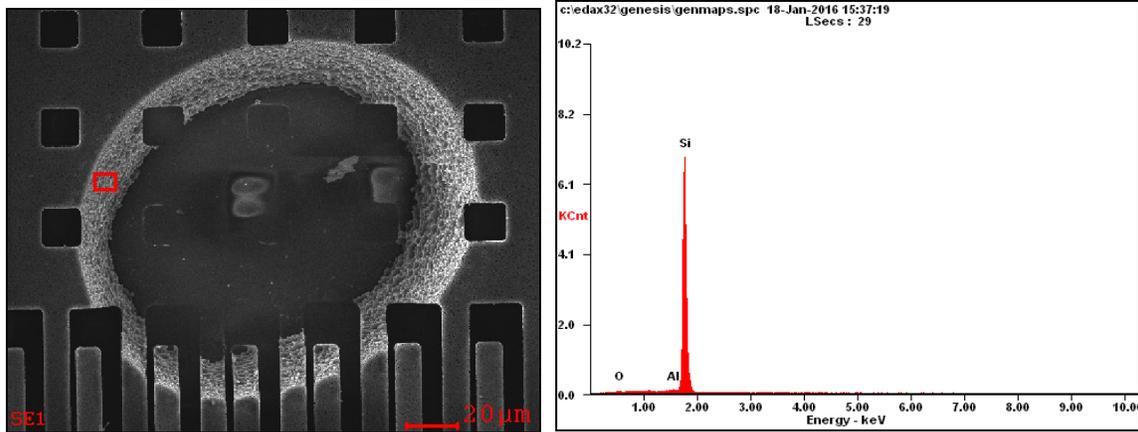


Figure B - 8 – Element analysis of the big holes defects

The fourth category of the defects included the areas that has not been developed and etched. Figure 9 shows a few samples of these incidents. It is concluded that development time and also the agitation during the development was not enough and it needed to be increased.

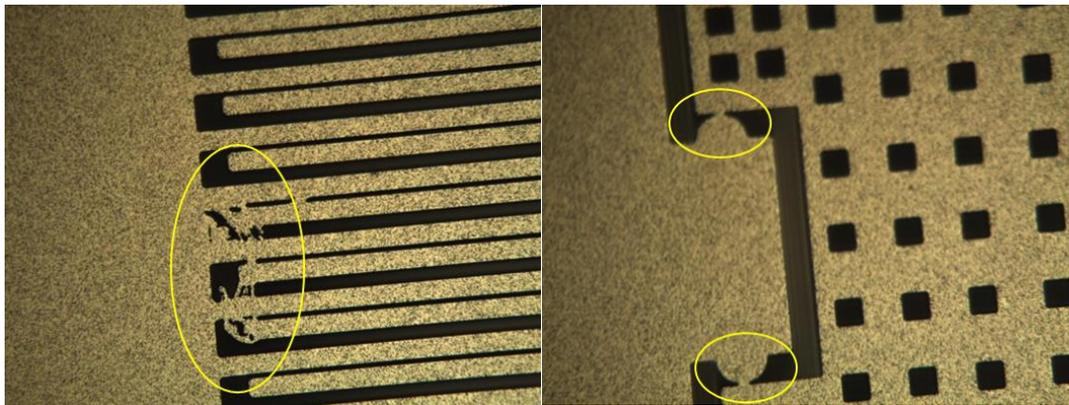


Figure B - 9 - Undeveloped and un-etched areas

The last category of the defects was included the broken fingers, the broken suspension elements and scattering of the debris all around the wafer. Figure 10 shows a few samples of these kinds of defects. It was identified that this incident was due to use dicing saw for dicing the wafer. As a result, for next round of fabrications, it was decided to use the laser machining for dicing the wafers.

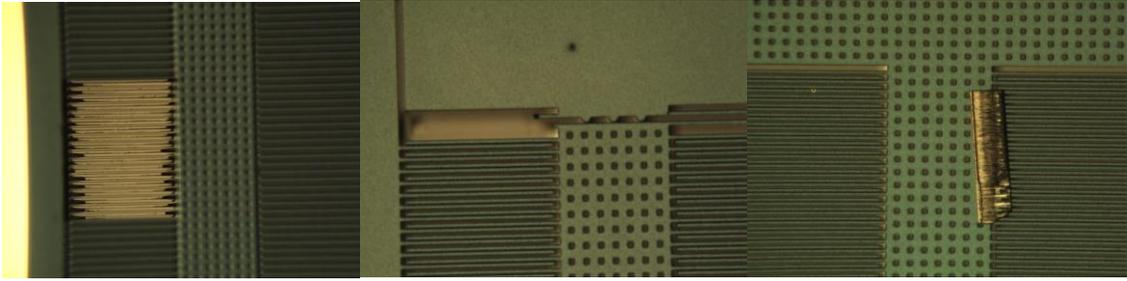
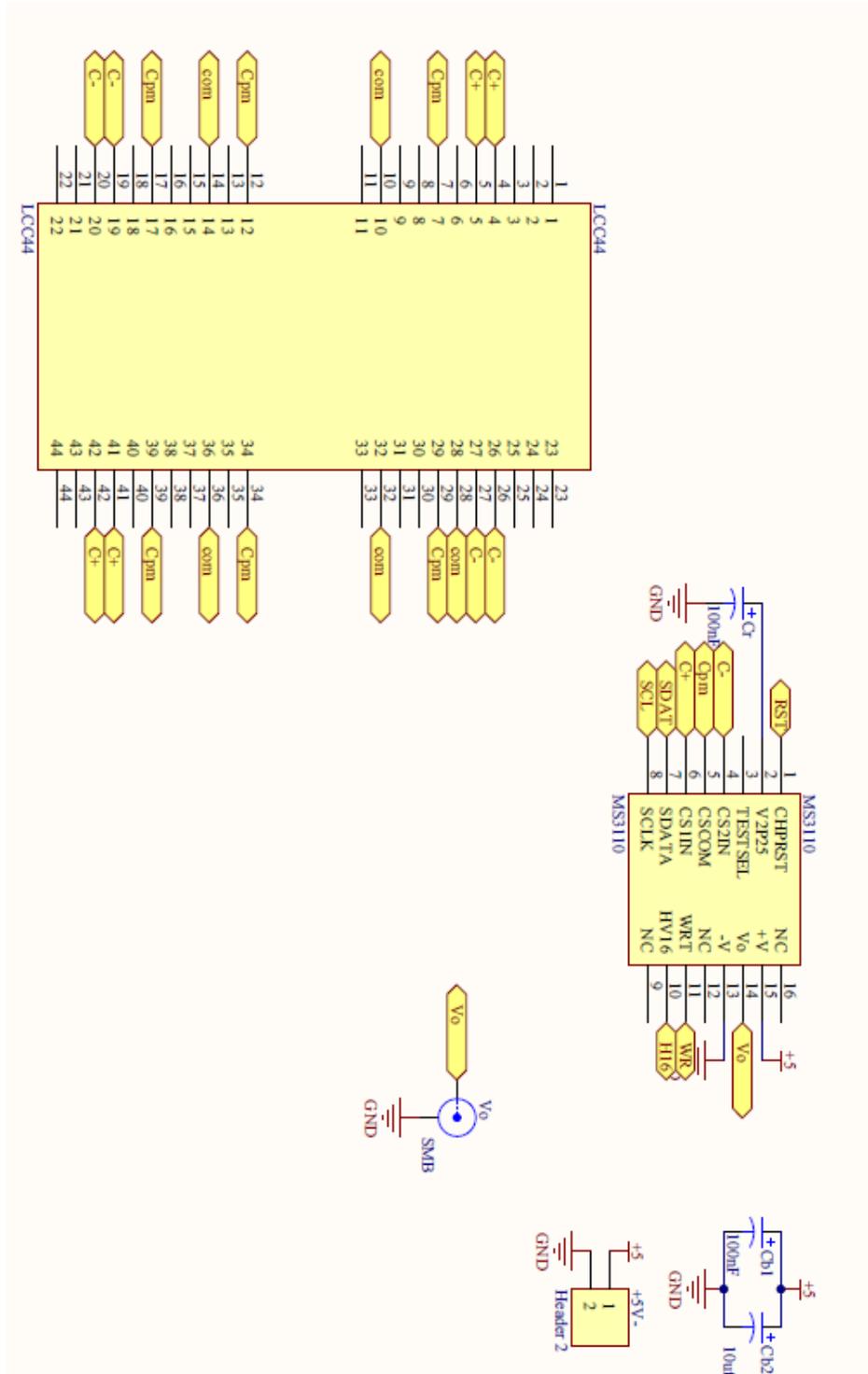


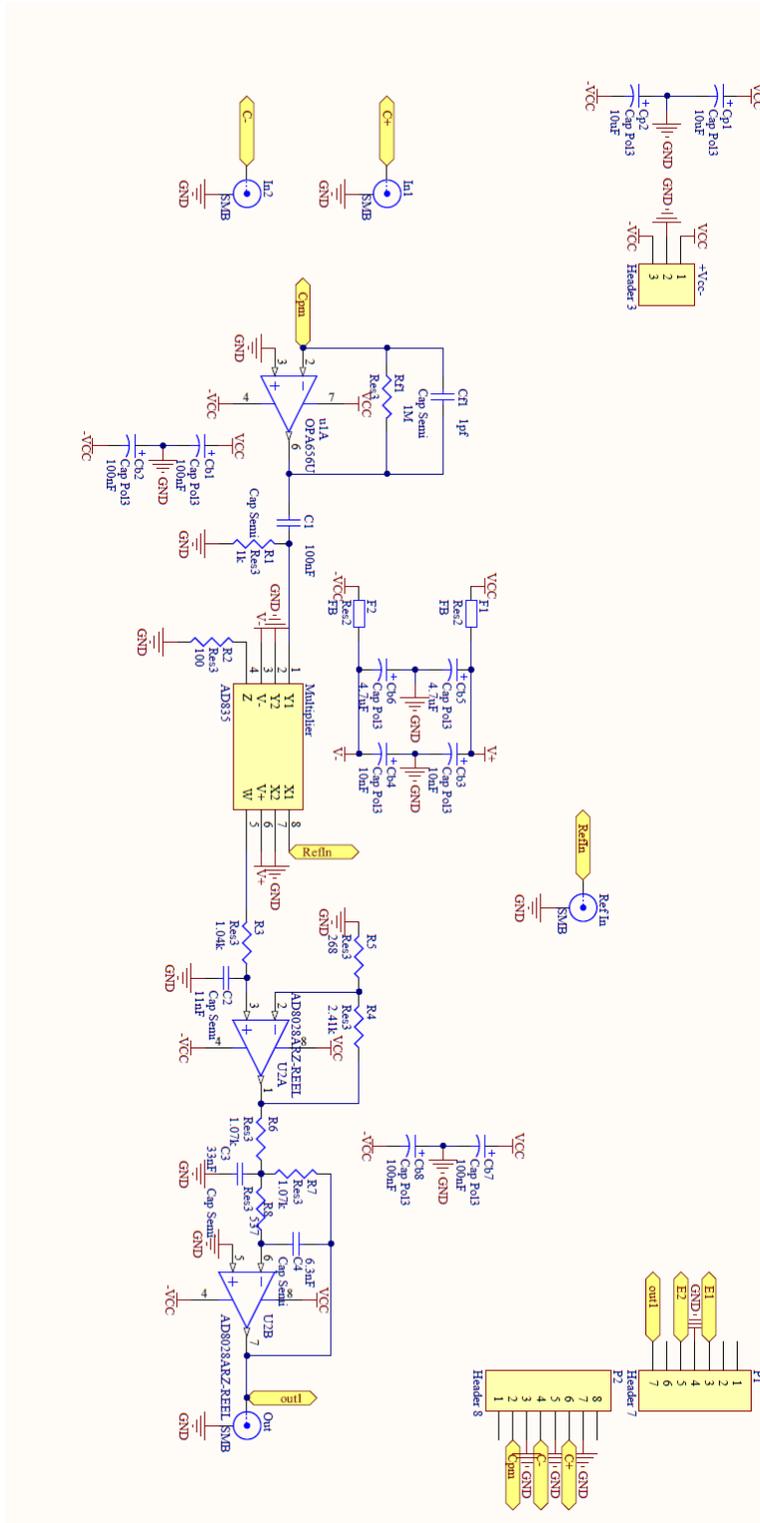
Figure B - 10 – Wafer defects due to the use of saw for dicing

Appendix C. Interface Electronic

Low-power circuit



Low-Noise Circuit



Appendix D. Shaker Fixture

In order to perform the vibration tests, it was required to design and build a test fixture to make an interface between the MEMS sensor and the vibration shaker. The purpose of this fixture was to couple mechanical energy from the shaker into the device under test (DUT). The necessity of designing a proper fixture is minimizing the effects caused by the fixture, such as resonant frequencies of the fixture, during vibration tests. A few constraints are needed to be considered in order to design a proper fixture.

- The attachment details of the fixture to the shaker including bolt size and thread size
- Size and configuration of the PCBs containing the MEMS device.
- Test axis for which the fixture is designed, which in our case it was designed in x and y directions for in-plane and out-of-plane accelerometer tests, respectively.
- Maximum mass that can be attached to the shaker which was less than 0.6 lbs for applying up to 10g's peak acceleration based on the shaker manual.

Considering the above constraints, using manual trial and error for topology optimization, the designed fixture for the in-plane accelerometers were designed as shown in Figure D-1:

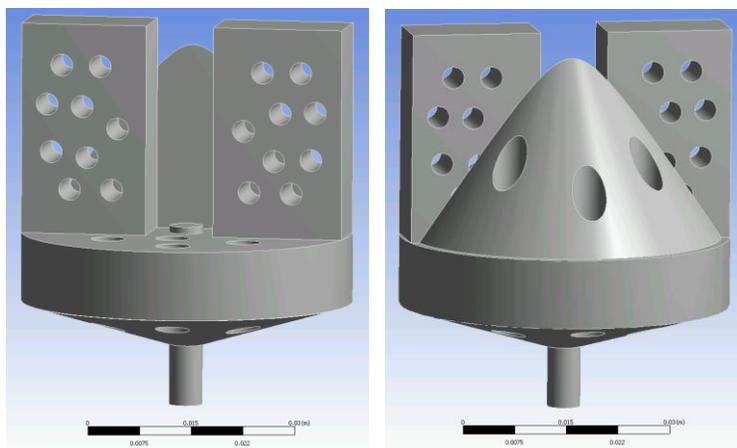


Figure D-1- Designed fixture for in-plane accelerometer testing

The simulated resonance frequencies of the fixtures are shown in Figure D-2, and the experimental frequency response of the sole fixture on shaker is shown in Figure D-3.

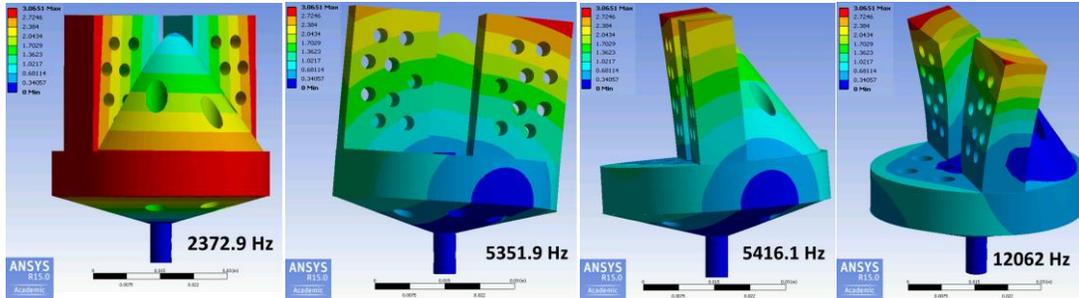


Figure D-2 - Modal analysis results of the designed fixture in ANSYS

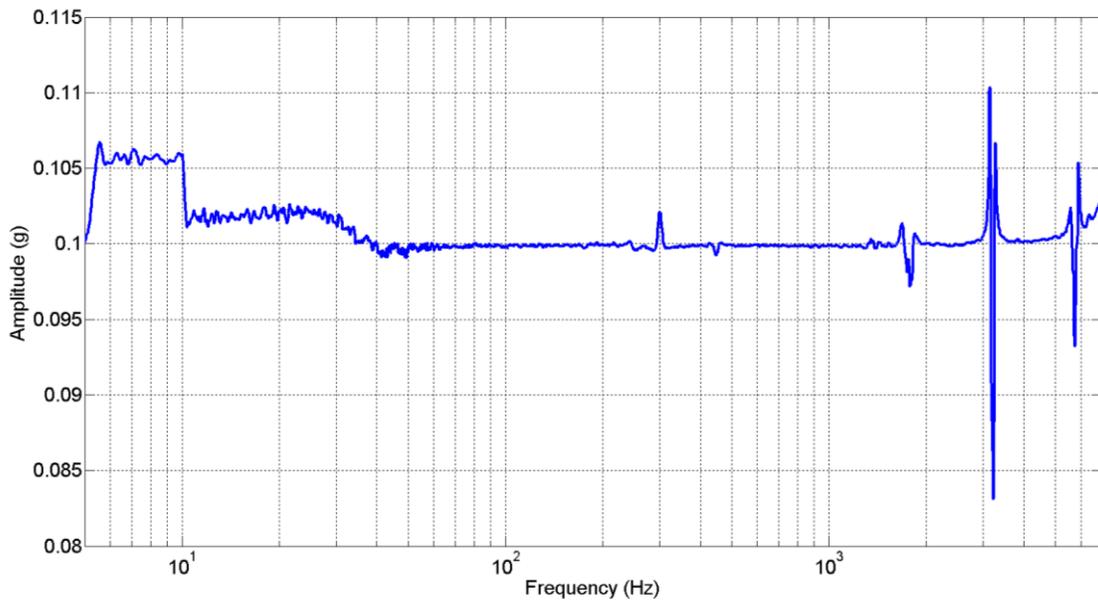


Figure D-3 – Frequency response of the fixture tested on the shaker