A new, low-cost, PDMS metallization process for highly conductive flexible and stretchable electronics

by

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Abstract

This thesis describes a novel microfabrication process to produce thick-film copper microstructures that are embedded in polydimethylsiloxane (PDMS). This process has reduced fabrication complexity and cost compared to existing techniques, and enables rapid prototyping of designs using minimal microfabrication equipment. This technology differs from others in its use of a conductive copper paint seed layer and a unique infrared-assisted transfer process. The resulting microstructures are embedded flush with the PDMS surface, rather than on top, and adhere to PDMS without the need of surface modifications. The 70-micrometers-thick copper layer has a surface roughness of approximately 5 micrometers, a low film resistivity of 2.5-3 micro-Ohm-cm, and can be patterned with feature sizes of 100 micrometers. The low-cost, thick metal films demonstrate a comparative advantage in high-current, low-power applications, with feature sizes and metal layer properties that are otherwise comparable to similar processes.

Several applications are fabricated, including stretchable interconnects integrated with fabrics for wearable devices and a multi-layer electromagnetic microactuator with a soft magnetic nanocomposite polymer core for large magnetic field generation. The interconnects can accommodate strains of 57 percent before conductive failure, which is similar to existing technology, and demonstrate a significantly lower resistance of less than 0.5 Ohm per device. The actuator produces an average magnetic field of 2.5 milli-Tesla per volt applied within a cylindrical volume of 34 cubic millimeters. Simulations indicate that fields of up to 1 Tesla are possible for 200 micro-second input pulses, and that significantly larger fields are achievable through simple design modifications. These results are comparable to existing devices, while our device has the advantage of being fully flexible, low-cost, and is easily integrated with various substrates and polymer microfabrication processes.

Keywords: Microfabrication; electrodeposition; stretchable electronics; wearable electronics; micropattern transfer; MEMS

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List of Acronyms

2D	Two-dimensional
3D	Three-dimensional
ACF	Anisotropic Conductive Films
BSED	Backscatter Electron Detector
CNT	Carbon Nanotube
DC	Direct Current
DI	Deionized
DMM	Digital Multimeter
DOF	Degrees of Freedom
ELD	Electroless Deposition
EMF	Electromotive Force
FPCB	Flexible Printed Circuit Board
IC	Integrated Circuit
IR	Infrared
LE	Linear Estimator
LEPD	Linear Estimator Percent Difference
LIGA	Lithography, Electrodeposition and Moulding (German acronym for “Lithographie, Galvanoformung, Abformung”)
LOC	Lab-on-a-Chip
LPF	Low Pass Filter
MAGMAS	Magnetic Microactuators and Systems
MEMS	Microelectromechanical Systems
MOKE	Magneto-Optical Kerr Effect
NCP	Nanocomposite Polymer
PCB	Printed Circuit Board
PDMS	Polydimethylsiloxane
PET	Poly(ethylene terephthalate)
PI	Polyimide
PMMA	Poly(methyl methacrylate)
PP	Polypropylene
PU	Polyurethane

RC	Resistor-Capacitor
RCL	Reconfigurable Computing Laboratory
RIE	Reactive Ion Etching
RLC	Resistor-Inductor-Capacitor
RMS	Root Mean Square
ROI	Regions of Interest
SAM	Self-Assembled Monolayer
SCR	Silicon Controlled Rectifier
SE	Standard Error (of the mean)
SEM	Scanning Electron Microscope
SFU	Simon Fraser University
UIL	Microinstrumentation Laboratory
WOS	Work of Separation

Chapter 1.

Introduction

Over the last century, there has been perhaps no greater influence on the relationship between technology and society than the proliferation of miniaturized electronics. From the invention of the first solid state transistor in 1947 [1], transistor sizes have shrunk to the scale of tens of nanometers in modern devices [2]. Now, nearly half of the global population has access to a modern cellphone [3] that contains over a thousand times more computing power, at a fraction of the mass, than the computers that once powered NASA's space shuttle [4] [5]. These rapid changes in computing have resulted, in part, from improvements to the size, cost, and performance of commercial electronics. However, such innovations are not unique to computation. More recently, novel fabrication processes and designs have been applied to other functions such as sensing, actuation, and communication [6] [7], all of which have the potential to impact society on a similar scale. Like the miniaturization of computation, the miniaturization of these functions has a great potential to shape both technology and society in the years to come. At the same time, new technologies that reduce fabrication complexity and cost while enhancing device mobility and functionality must continue to develop to promote the integration of electronic devices in our daily lives.

One of the earliest variations of standard silicon-based microelectronics processing was the development of silicon micromachining for the production of piezoresistive sensors [8]. At the time, this was one of the first innovations demonstrating that miniaturization could benefit not only computation, but also the measurement and manipulation of properties in the physical world. The silicon micromachining process has since grown to become a fundamental component of modern microelectromechanical systems (MEMS) device fabrication. However, the seamless integration of electronics with everyday activities requires a progression

beyond the use of stationary and rigid electronics, such as silicon-based computers and printed circuit boards (PCBs), that incorporates traditional electronic functions into alternative materials and substrates. One of the most familiar demonstrations of this progression is the use of portable electronics in biomedical applications. To achieve portability and integration with the human body, silicon and metal conductor materials are commonly replaced with flexible and stretchable alternatives such a polymer-based conductors [9]. At the same time, these conductors and other electronic components are integrated with alternative substrates such as clothing [10] or biocompatible polymers [11], rather traditional substrates such as the PCB. These developments have led to the transformation of isolated, fixed machines to multifunctional, mobile devices integrated with dynamic surfaces, such as the human body [12] [13].

The effort to integrate electronics with alternative materials and substrates is part of an emerging field of research known as flexible and stretchable electronics. Generally, flexible and stretchable devices have several advantages over their rigid counterparts, including the ability to conform to a curved surface (for example, the human body), to be folded within a constrained volume, and to otherwise be physically stretched and flexed without failing. Aside from the biomedical applications referenced previously, example applications in this area include waterproof optoelectronics and stretchable displays [14] [15], stretchable organic solar cells [16], stretchable and foldable integrated circuits [17] [18], and a wide variety of bio-integrated devices [19]. To meet the needs of these modern applications, the development of cost-effective micro and nanofabrication processes that produce highly conductive, flexible materials will remain an active area of research for the foreseeable future.

1.1. Motivation

Despite the impressive performance of modern flexible and stretchable devices, challenges relating to fabrication complexity and cost continue to persist. To increase the utilization of stretchable devices and promote their commercial success, fabrication process improvements must be made that address these challenges. This is illustrated using an example of a modern metallization process that enables highly-conductive, high-resolution metal patterns to be stamped directly onto human skin [20]. Although the

final product is an impressive achievement, the fabrication process involves the use of electron beam evaporation equipment for deposition, and several intermediate chemical processing steps that include the use of hazardous hydrofluoric acid. This combination of costly deposition equipment and multiple chemical processing steps is common to many modern processes, and is one example that has inspired this work to develop a simple, low-cost process alternative for flexible and stretchable electronics fabrication.

Aside from the challenges of complexity and cost, stretchable electronic devices must effectively maximize both conductivity and stretchability. Typically, conductivity in stretchable devices is achieved with thin metal films or polymer-based conductors. Fabrication methods for these conductors can include the direct deposition of metal on polymers [21], nanocomposite polymer (NCP) fabrication [22], fabrication using conductive polymers [23], and inkjet printing of conductive inks [24]. While many of these methods can produce highly flexible and stretchable features, the conductivity of non-metal structures is generally poorer than deposited metals. Therefore, the metallization of polymers is an important area of research in the fabrication of flexible electronics. The issue of conductivity can be further addressed through the development of thick metal films, rather than thin films, due to their increased ability to conduct electricity and function in low-power, high-current devices. For example, although the aforementioned example of stamping electronics directly onto the skin [20] uses metals, film thicknesses on the order of hundreds of nanometers may perform poorly in applications with high current requirements, such as electromagnetic actuators. At the same time, higher conductivities reduce the amount of stored energy required to power mobile devices, which improves portability. However, despite the high conductivity of thick metal films, their inherent rigidity compared to non-metallic conductors (such as NCPs) can reduce their suitability for use in flexible and stretchable electronics. Therefore, the development of a polymer metallization process should be paired with efforts to maximise the stretchability of the deposited features. In this thesis, we seek to maximise both conductivity and stretchability by investigating a new method of depositing thick metal films directly onto polymer with micropatterned conductor geometries that are optimized to achieve the maximum strain before conductive failure.

The consistent and reliable deposition of metals directly onto polymers and elastomers such as PDMS is difficult, and can lead to multiple forms of failure [25]. These failures are often due to the poor adhesion that results from depositing metal layers directly onto a flat, cured, polymer surface. In such cases, the metal sides and metal-polymer interface are exposed and prone to delamination. In some PDMS-based processes, an oxygen plasma or self- assembled monolayer (SAM) surface treatment is performed to promote adhesion to the metal layer [26]. However, this type of surface treatment is one example of process complexity that we wish to eliminate. Therefore, along with maximizing conductivity and stretchability, we seek to develop an effective mechanism for metal-polymer adhesion without the use of surface treatments.

1.2. Objectives and Contributions

The main purpose of this thesis is to develop an effective process alternative for flexible and stretchable electronics fabrication that demonstrates improvements over existing processes in terms complexity, cost, and conductivity while maximising the stretchability of patterned features. This process should be, at least theoretically, well suited to wide variety of metal conductors and substrates, and scalable in terms of conductor area and production volume. In this thesis, the conductor and substrate materials are limited to PDMS and copper, respectively. We select these materials due to their extensive use in existing studies, ease of fabrication, and desirable electrical and mechanical properties. Material selection and process scalability are discussed in detail in Chapter 2. The process must also be capable of producing feature sizes as small as 100 μm to function in micro-scale applications, and demonstrate an effective adhesion mechanism at the metal-substrate layer. We also seek to develop applications that demonstrate the use of this process in stretchable electronics, wearable electronics, and MEMS applications.

To address the common concerns of adhesion and conductivity while reducing the complexity and cost of fabrication found in modern processes, we propose the development of a new low-cost, thick-film metallization process. This process uses simple fabrication steps and minimal lab equipment, resulting in flexible, highly conductive microstructures embedded in PDMS. The proposed method includes the

electrodeposition of thick metal films to increase conductivity and a unique infrared (IR)-assisted process to transfer the deposited layer from a sacrificial conductive paint seed layer onto an uncured PDMS substrate. This transfer process addresses the concerns of adhesion by encapsulating the metal layer sidewalls in PDMS as it cures. The addition of a final encapsulating layer of PDMS is optional in situations where exposure of the top-facing copper is undesired. However, access to an exposed copper face may be required in certain applications, such as electrochemical sensing [27]. This novel patterning and transfer process uses minimal fabrication equipment, low cost materials, and relatively few processing steps to address the issues of complexity and cost that are characteristic of other metallization processes. In addition, the unique IR-assisted transfer from a sacrificial seed makes the process adaptable to a variety of substrates and applications, such as fabrics and aligned multi-layer devices. Further analysis and discussion of the process's versatility suggest that the process is highly adaptable in terms of conductor material, target/substrate material, and scalability. Stretchable patterns with various curvilinear geometries are fabricated and characterized to maximize the stretchability of the patterned metal layers. The response of these patterns to cyclic failure and recovery is also characterized. A single stretchable pattern is used to demonstrate the use of this process in wearable applications. Finally, a low-power, high-current, electromagnetic actuator demonstrates several process capabilities, including the incorporation of aligned metal layers and the integration of NCPs that are patterned via soft lithography. The actuator design is optimized for maximum magnetic field generation, and is characterized using both simulation data and experimental data from a fabricated device.

The objectives of this thesis are summarized as follows:

- To develop a new polymer metallization process for flexible and stretchable electronics using PDMS as a substrate. The process must:
    - Produce thick metal films for highly conductive features enabling low-power, high-current devices
    - Enable rapid prototyping of designs and use minimal laboratory equipment

- To fully characterize the metal layer produced by the proposed process, and demonstrate highly conductive structures with feature sizes as small as 100 μm. The characterization of the metal layer is performed in terms of:
    - Resistivity
    - Thickness and surface roughness versus time
    - Defects (reliability)
    - Adhesion
    - Feature size and resolution limits. Test structures include:
        i. Linear features testing trace width
        ii. Linear features testing nearest spacing
        iii. Circular features testing trace width
        iv. Circular features testing nearest spacing
        v. Pegs
        vi. Holes
- To fabricate highly stretchable electrical interconnects exhibiting low resistance compared to similar devices fabricated using existing technology. This includes:
    - The maximization of interconnect stretchability through the optimization of design parameters
    - A demonstration of cyclic failure and recovery of the devices fabricated using this process.
- To demonstrate a process alternative enabling highly conductive, low-cost, wearable electronics, including:
    - A modified process where an electrical interconnect is directly integrated, or ‘stamped’, onto stretchable fabric
    - A characterization of the stretchability of the wearable interconnects

- To demonstrate a multi-layer, high-current application enabled by the newly developed process. This is shown through the fabrication and characterization of an electromagnetic actuator, including:
    - A design optimized for high-current pulses and large electromagnetic field generation, ideal for MEMS switches and bi-stable latches or valves
    - A modified process for aligned, multi-layer, metal-on-PDMS devices
    - A modified process for the integration of NCPs patterned via soft lithography

Through the completion of these objectives, we demonstrate the following contributions to the field:

- The first investigation of a new PDMS metallization technique involving the IR-assisted transfer of electrodeposited copper microstructures from a sacrificial conductive paint to PDMS. This simple, low-cost fabrication alternative has the potential to benefit new research, rapid prototyping, and large-scale fabrication in the field of flexible and stretchable electronics.

- A solution to help alleviate the problem of metal-PDMS delamination commonly observed in existing deposition processes. This is achieved by transferring the metal patterns to PDMS before curing through an IR-assisted process. The metal patterns are embedded flush with the PDMS surface, mechanically locking them in place.

- Empirical evidence and analysis supporting the optimization of serpentine patterns for stretchability in electrical interconnects. This expands on previous efforts to identify the combination of geometric parameters that maximizes the stretchability of these patterns.

- A versatile new alternative for ‘stamping’ metal layers onto unconventional substrates, such as stretchable fabrics for wearable electronics

- A demonstration of increased magnetic field generation in planar electromagnetic actuators through an enhanced process utilizing stacked, aligned coils and an integrated Fe-PDMS core

1.3. Organization

Chapter 2 contains the background and prior art relating to this thesis, including a discussion of the materials, mechanics, fabrication processes, and challenges in the field of flexible and stretchable electronics. Chapter 3 gives a detailed description of the

proposed fabrication process, and discusses the fabrication challenges that are addressed. Chapter 4 provides a characterization and analysis of the fabricated metal layer. Chapter 5 presents an application of this process in stretchable and wearable electronics. Chapter 6 presents a low-power, high-current, MEMS application via an electromagnetic actuator design. Future work and concluding remarks are given in Chapter 7 and Chapter 8, respectively.

Several chapters contain significant portions of material that is adapted from existing studies published by our group. Background material in Chapter 2 is adapted from references [28], [29], and [30]. Material presented in Chapter 3 and Chapter 4, relating to the fabrication and characterization of the proposed process, is adapted from references [28] and [30]. Material related to stretchable and wearable electronics in Chapter 5 is adapted from [29] and [31] Finally, Chapter 6 is adapted from material in [31] and [32], though much of the characterization data in Chapter 6 is, to-date, unpublished.

Chapter 2.

Background and Prior Art

Flexible electronics is an emerging technology, enabling new applications that cannot be fabricated using traditionally rigid substrates. In the context of electronics, the term “flexible” describes material properties ranging from slightly bendable to highly elastic or conformal. Solar arrays fabricated in the 1960s are among the first examples of such flexible devices, gaining their flexibility as a by-product of being fabricated on thin silicon substrates [33]. This practice results in an increased cell power-to-weight ratio, which is a common requirement in space applications. Over time, flexibility has become a desirable quality in many electronic devices. Industrial applications have grown from silicon solar cells to flexible displays and X-RAY sensor arrays, while academic research is directed more towards conformal displays, sensors, and wearable devices [34]. Other modern applications include wearable monitoring devices [35], implantable neural or muscular stimulators [36], implantable drug delivery and fluid control systems [37], flexible sensors and actuators [26] [32] [38], and flexible integrated circuit technology [39].

Despite growth in the flexible electronics industry, there is a common misconception that commercial devices, such as cellular phones and digital cameras, which incorporate many flexible components, are purely rigid. This misconception is understandable, as the relatively few flexible components are often contained and hidden within a rigid body. However, flexible components are critical to enabling the high densities of electronics found in these devices. Among the most familiar of these components is the flexible printed circuit board (FPCB). Despite being packaged and hidden from the consumer, FPCBs are commonplace and found, for example, connecting the motherboard to peripheral components in mobile devices. Although FPCBs represent an established and growing industry, they are limited in many ways.

For example, FPCBs cannot bend effectively in multiple directions simultaneously, or conform to arbitrary surfaces. It is also difficult to fabricate multilayered or integrated devices on a single substrate, especially unconventional substrates such as fabrics, using commercially available FPCBs.

The challenges faced by FPCBs and other flexible components are addressed in the field of stretchable electronics. The use of stretchable conductors enables devices that can conform to arbitrary surfaces by simultaneously bending and stretching in multiple dimensions. Wearable electronics, a subset of stretchable electronics, demonstrate a further progression by integrating sensing, actuating, communication, and computing components with the human body via clothing or other low-profile wearables [40]. These components have many practical uses. For example, fiber-based devices are used in wearable generators that power personal electronics and in wearable body temperature sensors [41]. Devices that are more specialized include cardiovascular monitors for portable healthcare [42], and wearable computers to aid astronauts during extravehicular activities (space walks) [43]. One of the main challenges in integrating conventional electronics with fabrics is the fact that fabrics are typically not suitable as substrates in traditional fabrication processes. Some approaches to overcome this challenge include the use of conductive fibers, and screen printing conductive ink patterns onto fabric [44]. Unfortunately, conductive fibers and screen printable inks often exhibit a resistivity over 100 times larger than the traditional metal conductors used in electronics (see Section 4.2.1). In low-power and highly portable applications, the minimization of resistance is critical. In these applications, ink-based or fiber-based conductors may not be suitable solutions.

The relatively high resistivity of fibers and screen printed inks illustrates one of the main challenges with flexible and stretchable electronics, which is the attempt to combine mechanical flexibility with electrical performance. This challenge is typically approached from several directions, including the selection of suitable materials and substrates, the optimization of conductor geometries, and the selection of an appropriate fabrication process. The selection of a fabrication process is critical, as it constrains the set of appropriate materials and conductor topologies, and ultimately determines the mechanical and electrical properties of a fabricated device. The choice of fabrication

process also affects common manufacturing challenges such as cost, complexity, and production volume. Other considerations may be application dependant, including the ability to fabricate multi-layer devices, the ability to integrate additional materials and processes, and the quality of conductor-substrate adhesion. The development of novel fabrication processes represents an ongoing effort to address these challenges, and to enable new applications that may not be fabricated using existing technologies.

The fabrication of flexible and stretchable electronics is generally subdivided into two categories. The first category involves the use of traditional conductors such as silicon or metals. These conductors offer superior electrical performance, but suffer in terms of mechanical performance relating to flexibility. To compensate for their mechanical properties, these conductors are often patterned to enable stretching, or are used in conjunction with other elastic materials. An example strategy that integrates rigid conductors with elastic materials is to fabricate rigid, conductive, 'islands' in an elastic mesh [45]. With this strategy, the overall device is macroscopically stretchable and conductive, as long as the rigid regions are kept small compared to the surrounding elastic regions. In the second category, stretchable electronic devices use intrinsically stretchable materials that have superior mechanical performance compared to metals or silicon. One common approach in this category is to dope a polymer, selected for its mechanical properties, with conductive particles resulting in a conductive polymer-based composite. While these materials exhibit impressive mechanical properties, the conductivity of polymer-based conductors is generally poorer than pure metals. For stretchable electronics applications with strict electrical performance requirements, the deposition and patterning of metals on elastic substrates remains an important strategy.

The research presented in this thesis is heavily motivated by a desire to produce highly conductive devices with an emphasis on electrical performance. Therefore, the background presented in this chapter focuses mainly on highly conductive materials, such as metals, and the related processes used in the fabrication of stretchable electronics. However, a set of alternative materials and processes is also presented to provide context and the opportunity for comparison. A presentation of the theory relevant to mechanical stretching and conductivity is presented in Section 2.1 and Section 2.2, respectively. This is followed by a discussion of the elastic materials commonly found in

flexible and stretchable devices in Section 2.3. The fabrication processes used in flexible and stretchable electronics are discussed in Section 2.4, with an emphasis on electrodeposition in Section 2.5. An overview of the stretchable geometries applied to metal conductors is given in Section 2.6. Several experiments in this thesis use multiple devices to provide a statistical assessment of the measured values; the relevant statistical theory is given in Section 2.7.

2.1. Mechanics

The conductors presented in this thesis are evaluated based on their ability to both stretch and conduct electricity. Therefore, it is prudent to provide a brief background on the relevant mechanics and electrical properties required to understand a relationship between conductor strain and resistivity [46].

Flexing and stretching are examples of material deformations that can occur when a material is exposed to mechanical stress. This stress is calculated using Equation 1:

$$\sigma = \frac{F}{A} \tag{1}$$

where F is an applied force, A is the cross-sectional area over which the force is applied, and σ is the resulting mechanical stress. The deformations that result from an applied stress are mechanical strains. Mechanical strain is expressed as the deformation length per unit length, as shown in Equation 2:

$$\varepsilon = \frac{\Delta L}{L_o} \tag{2}$$

where L_o is the original length of the material, ΔL is the total change of length due to an applied stress, and ε is the mechanical strain. The variables in these stress and strain equations correspond to a single axis, and several equations are often used to describe the stress and strain along independent axes.

Strain is also referred to as percent elongation, as it captures the amount that a material expands or contracts compared to its original length, L_o. If a strain is reversible, then the deformation is called elastic. Young's Modulus, E, quantifies the relationship between stress and strain in the linear region of a material experiencing elastic deformation (where Hooke's Law holds). This relationship is given by Equation 3:

$$\sigma = E\varepsilon \tag{3}$$

where σ and ε are the stress and strain, respectively. In this case, Young's Modulus is often referred to as the modulus of elasticity.

Equations 1 to 3 do not contain directional information. In simple cases (for example, a rod undergoing elongation), the direction of stress and strain are obvious and the axis may not need to be specified. In more complicated cases, where stress and strain appear in more than one dimension, the subscripts $x, y,$ and z specify the axis in a given equation. Multiple three-dimensional (3D) stress and strain equations may be collectively described in matrix form. Specifying direction is especially important in elastic materials, where a uniaxial tensile stress applied in one direction will result in compression in perpendicular directions. This effect is observed in the familiar scenario of an elastic band becoming thinner as it is stretched. The relative amount of compression experienced in the perpendicular directions is quantified by a parameter called Poisson's ratio. If a material experiences a tensile strain in an arbitrary direction, z, and the corresponding compressive strains are equal in the perpendicular directions x and y, then material is said to be isotropic. In this case, Poisson's ratio is given by Equation 4:

$$\nu = -\frac{\varepsilon_x}{\varepsilon_z} = -\frac{\varepsilon_y}{\varepsilon_z} \tag{4}$$

where ν is Poisson's ratio and ε_n is the strain in direction n. The negative sign is included so that Poisson's ratio is positive, as the reactive strains will always have the opposite sign of the applied strain.

When materials experience strains large enough that they are no longer reversible, then the deformations are called plastic rather than elastic. The point at which the material begins to experience plastic deformations is called the yield point, and it appears at a stress that corresponds to the yield strength. The elastic-plastic transition is often gradual, and the yield strength is not easily determined. One common convention is to define the yield strength to be the amount of stress required to cause 0.2% permanent strain. Other behaviours can be observed at the elastic-plastic transition, but their description is beyond the scope of this thesis. After yielding, a material experiences plastic deformation under increasing stress. The amount of plastic deformation that a material is able to withstand before fracture is known as the material's ductility. The stress required to increase plastic deformation will continue to a maximum point. The value of the stress experienced at this point is called the material's tensile strength. After this point, an applied stress will decrease until the material experiences total failure, or fracture. The reason for the stress decreasing after surpassing the material's tensile strength is that the material begins to soften due to accumulated damage. Deformations after this point become localized rather than uniformly dispersed. This localized deformation before the point of failure result in a consequence known as necking.

2.1.1. Mechanics of Thin Films

The mechanics and failure mechanisms associated with thin films deposited onto flexible substrates are of particular importance in flexible electronics [47] [48] [49] [50]. In general, the deposition of thin films onto substrates (flexible or not) results in residual stresses within the deposited layer [51]. While film stresses can adversely affect device functionality, they can also potentially be used as an advantage [51]. Therefore, it is important that the film stresses resulting from a particular deposition process are well understood.

Residual film stresses are classified as either intrinsic or extrinsic. Intrinsic stresses result from the film deposition process and are often referred to as growth stresses. Intrinsic stresses may have different causes depending on the deposition process and can be either compressive or tensile [51]. The stress within a 2D thin film is often modelled by the biaxial stress equation, where only normal stresses (in the x- and

y-direction) are considered and are assumed to equal [51]. This biaxial stress is described in Equation 5:

$$\sigma = \sigma_x = \sigma_y = \frac{E}{1-\nu} \cdot \varepsilon \tag{5}$$

where ν is the Poisson's ratio of the film material, E is the Young's Modulus, and σ_x and σ_y are the normal stress components in the x- and y-direction, respectively. According to convention, tensile stress is positive while compressive stress is negative.

As an example of intrinsic stress, the electrodeposition of copper onto silicon substrates has been shown to result in tensile stress in the deposited layer [52]. In contrast, extrinsic stresses are imposed by external factors. One of the most common extrinsic stresses is thermal mismatch stress, which is caused by a mismatch between the coefficients of thermal expansion in the deposited film and the substrate. For a stress-free film transferred to a substrate at a uniform deposition temperature, T_d, the resulting thermal mismatch strain after cooling to room temperature, T_r, is given by Equation 6:

$$\varepsilon_{mismatch} = (\alpha_f - \alpha_s)(T_d - T_r) \tag{6}$$

where $\varepsilon_{mismatch}$ is the thermal mismatch strain, and α_f and α_s are the coefficients of thermal expansion for the deposited film and the substrate, respectively. The associated stress due to thermal mismatch is given Equation 7:

$$\sigma_{mismatch} = \frac{E}{1-\nu}(\alpha_f - \alpha_s)(T_d - T_r) \tag{7}$$

In addition to residual stresses, devices in flexible electronics applications are also subject to external stresses. For example, when a user bends a part of his or her body with an attached wearable device, the outer surface of the device may experience a tensile (or compressive) stress while the inner surface experiences a compressive (or tensile) stress. If the stresses on the deposited material become too high, the resulting

strains can lead to device failure. For relatively brittle films on flexible substrates, film cracking and delamination are the most common forms of failure [53], while the likelihood of a given failure depends on both film adhesion and layer geometry [47]. Therefore, the careful selection and arrangement of materials in multi-layer devices is critical to achieving device reliability.

2.2. Electrical Properties

Aside from the ability to stretch, the other crucial property of a stretchable electronic device is the ability to conduct electricity. The most familiar electrical conduction law, Ohm's Law, relates electrical current, I, which is the time rate of change of passing charge, to an applied voltage, V, according to Equation 8:

$$V = IR \tag{8}$$

where R is the resistance of the material transmitting the electrical current. The resistance is dependent on the geometry of a device. For devices with length, L, and uniform cross-sectional area, A, the resistance is calculated according to Equation 9:

$$R = \frac{L\rho}{A} \tag{9}$$

where ρ is the resistivity of the device material. Resistivity is a material property that is independent of geometry.

2.2.1. Resistivity of Thin Films

Although the resistivity of conductive materials is independent of geometry, there are additional details relevant to measuring and representing the electrical properties of thin films as opposed to bulk materials. For thin films, the cross-sectional area, A, in Equation 9 is alternatively written as $t \cdot W$ (thickness multiplied by width), as shown in Equation 10:

$$R = \frac{\rho L}{tW} \tag{10}$$

The resistivity of a thin film divided by the thickness is known as the film's sheet resistance, R_S. Therefore, for square films with L equal to W, the resistance of a thin film is given by the sheet resistance. Although the units of resistance and sheet resistance are equivalent, sheet resistance is often expressed as Ohms-per-square to differentiate between bulk material resistance measurements. To measure sheet resistance, a four-point probe configuration may be used, as shown in Figure 1 [54].

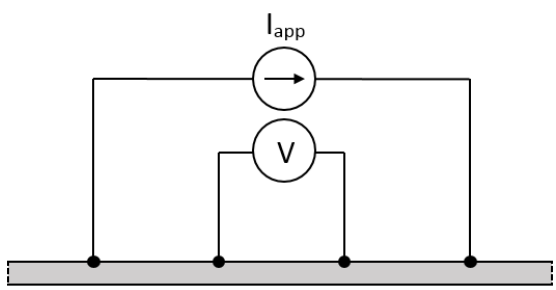


Figure 1. Four-point probe configuration used to measure sheet resistance.

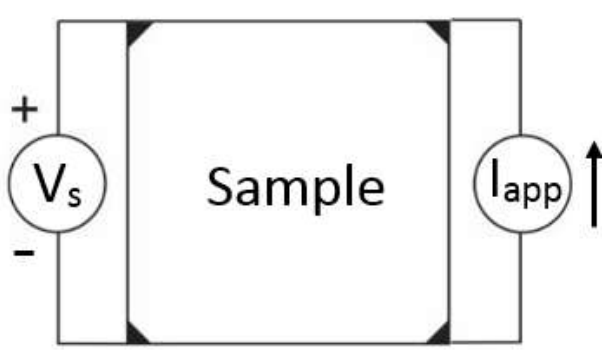


Figure 2. Illustration of the Van der Pauw method used to determine resistivity. A current is applied (I_{app}) along one edge of a square sample, while voltage is sensed (V_s) across the opposite edge [30].

In the four-point probe configuration shown in Figure 1, four equidistant probes are aligned and placed in contact with the film surface. A current is passed between the

outer contacts, and the voltage is measured between the inner contacts. For a film of infinite extent, the sheet resistance is given by Equation 11:

$$R_s = \frac{\pi V}{I \ln 2} \tag{11}$$

where I is the applied current and V is the measured voltage. In practice, Equation 11 may be used for finite films assuming the distance between probes is much smaller than the dimensions of the film.

For sheets of finite size, an alternative method of measuring sheet resistance may be used. According to the Van der Pauw method [55], the sheet resistance of arbitrary film geometries may be measured by contacting four probes along the perimeter of the film and applying current to two neighbouring probes while measuring the voltage drop across opposite probes [54]. For arbitrary shapes, the resulting calculation of sheet resistance requires a numerical approximation of the transcendental equation proposed by Van der Pauw [54]. Fortunately, the situation is simplified by using symmetric geometries, such as the square shown in Figure 2, rather than arbitrary shapes. In such cases, the Van der Pauw calculation reduces to Equation 11, assuming that the ratio of applied current to measured voltage is independent of probe orientation [56].

2.3. Substrate Materials

Flexible electronic devices typically consist of a flexible substrate chosen for its mechanical properties coupled with a conductive material chosen for its electrical properties. To provide a flexible or stretchable platform, highly elastic polymers or elastomers are often chosen due to their ability to undergo large elastic deformations. Elastomers consist of long-chain molecules linked together in a network of chains. Each chain acts as mechanical spring, which results in the elastic behaviour of the network. Different chemical structures within a given polymer lead to different material properties. For example, the strong silicon-oxygen chain found in silicone-based elastomers makes these molecules useful over a wide range of temperatures compared to carbon-carbon

chain molecules, such as those found in thermoplastic polymers. One of the most common polymers used in the development of flexible and stretchable electronics is PDMS. PDMS is a highly flexible silicone-based elastomer that is used in many microfluidic and MEMS applications due to its desirable mechanical properties, such as elasticity, and the ease with which it can be micropatterned into complex structures [57] [58]. In addition, the composition of PDMS may be adjusted to modify its mechanical properties, such as elasticity [59]. Other benefits of PDMS include transparency, chemical inertness, biocompatibility, and a wide operating temperature range with consistent mechanical properties between -100 ˚C to 100 ˚C [60]. Other polymers are also useful as substrates in flexible electronics, such as poly(methyl methacrylate) (PMMA) [61], poly(ethylene terephthalate) (PET), and polyimide (PI) [62]. However, PDMS is used exclusively in this thesis due to its extensive use in existing studies and desirable mechanical properties. For example, as shown Table 1, the Young's Modulus of PDMS is roughly 1000 times smaller than PET, PMMA, and PI, which enables relatively large strains given an applied tensile stress.

Table 1. Thermal and mechanical properties of common polymers.

	Density (g/cm^3)	Thermal Conductivity (W/mK)	Coefficient of Thermal Expansion (ppm/°C)	Young's Modulus (GPa)	Ref.
PDMS	1.23	0.17-0.3	310	0.0018	[63], [64]
PET	1.35	0.15	117	2.8-4.1	[46], [65]
PI	1.39	0.2	16	4-5	[63], [66]
PMMA	1.16	0.186	90-162	2.24-3.24	[46], [63], [65]

The thermal properties of a material, such as those shown in Table 1, also play an important role in material selection. For example, thermal conductivity, which describes the relationship between heat flow and temperature gradients within a material, is important when temperature gradients are expected and heat transfer must be controlled. Similarly, the coefficient of thermal expansion, which describes the fractional change in length versus the change in temperature, can be crucial in applications where large operating temperatures are expected. The mechanical properties of a material are also often temperature dependent. For example, the Young's

Modulus of PDMS is dependent on both curing temperature [67] and operating temperature [68]. During product design, the various physical properties of many materials must be considered in the context of a given application. Therefore, in the context of this thesis, alternative polymers must be explored in future applications of this process.

Aside from selecting a flexible substrate, the selection of a suitable conductor material is also important. Various conductor materials commonly used in flexible and stretchable electronics are discussed in Section 2.4.

2.4. Fabrication Processes

Despite the appealing material properties of PDMS discussed in Section 2.3, integrating polymers with traditional fabrication processes can be challenging. This difficulty is due to differences in the physical properties of polymers compared to traditional conductive materials, such as metals and silicon. Some metals commonly used in microelectronics, such as platinum [69] and gold [25] [70], can be directly deposited onto PDMS for electrical interconnects and integrated electronics. However, these metals are difficult to pattern on flexible polymer substrates and often experience cracking or deformation during the manufacturing process [25] [70]. One of the main factors responsible for these difficulties, besides adhesion, is the difference in mechanical properties between metals and polymers. To improve the flexibility and resistance to cracking of metal-PDMS devices, alternatives to direct metallization are often explored. As mentioned in Chapter 1, these alternatives include flexible NCPs [22], conductive polymers [23], and inkjet printing of conductive inks [24]. These methods are discussed in further detail here.

NCPs have a variety of uses depending on the selection of both the materials and the fabrication method. NCPs are often patterned using micromolding techniques (also known as soft lithography) [22] to form stretchable conductors in microfluidics and lab-on-a-chip (LOC) applications [71] [72]. NCPs are also screen printed onto numerous substrates such as fabrics for wearable devices [73]. A variety of dopants (typically nano- or micro- particles) are used depending on the application, including carbon

nanotubes (CNTs) for conductors [74], magnetic particles for actuation and sensing [71], silver/silver-chloride for bio-integration [72], and even ferrofluids for biocompatible electrodes with magnetically inducible microstructures [75].

Unlike NCPs, conductive polymers are inherently conductive without the use of particles such as CNTs. Implantable devices using inherently conductive polymers, such as conductive hydrogels, have been shown to improve cardiac cell signalling after myocardial infarction (heart attack) in some cases [76], while other conductive polymers have been used to improve lithium-ion battery anodes [77] and as active layers in organic solar cells [78]. Conductive polymers often use the same fabrication processes as NCPs, such as micromolding, as well as other processes that may not be suitable when using high concentrations of conductive dopants, such as electrospinning [79].

Finally, inkjet printing is used to create 3D interconnects [80], organic semiconductors [81], electrical contacts [82] [83], and other metallic structures [84]. These applications typically rely on an ink medium doped with a metallic conductor, and often require further processing steps to enhance conductivity. One of the drawbacks of inkjet printing in particular is that it is a serial rather than parallel process, making it difficult to achieve rapid, large-scale fabrication. Another drawback of inkjet printing is that conductive inks are often more resistive than pure metals. In general, strategies that use alternative materials, such as inkjet printing, produce conductors with more resistance than those that deposit pure metals. Therefore, to maintain highly conductive flexible electronics, a reliable process for the metallization of polymers, including PDMS, remains an important area of research.

Current polymer metallization techniques include metal lift-off [85] [86], shadow masking [87] [88], microcontact printing (μCP) [89] [90] [91], nanoparticle film deposition [92] [93], and electroless deposition (ELD) [94]. Although these methods apply to polymers in general, particular attention is given to PDMS in this thesis. Lift-off techniques first involve photoresist deposition and patterning followed by metal deposition via evaporation or sputtering. The final step is the removal of the photoresist and the overlying metal. One difficulty with the lift-off method is that the photoresist layer can form microcracks during the sputtering step that lead to electric shorting and device

failure in the metallized layer [25]. In addition, the photoresist removal process often involves the use of solvents, which can swell polymers such as PDMS and cause further deformations in the metal layer. The replacement of typical photoresists with SU-8, a negative-working photo-epoxy, is used as an alternative to photoresists that require solvents for removal. However, SU-8 still suffers from issues of adhesion and microdeformations [25].

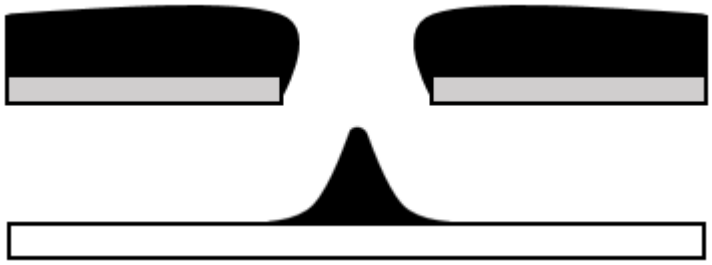


Figure 3. Exaggerated limitations of shadow masking. The mask (grey) becomes loaded with the deposited material (black) over time. The resolution of the deposited material is limited due to the mask-to-substrate (white) separation distance.

Shadow masking, which uses a micromachined template separated from the substrate rather than a photoresist, has limitations on feature size since the template is not directly adhered to the substrate [28]. Other limitations of shadow masking are that it cannot be used to form isolated or enclosed features such as circular traces and pegs, and that the template eventually becomes unusable due to loading of the masked material [28]. Limitations due to mask loading and substrate separation are illustrated in Figure 3.

The use of μCP involves pre-forming a metal pattern on a specialized stamp that is then transferred to the PDMS substrate through physical contact. The pre-forming of the metal and the transfer require additional fabrication steps, often including several surface modifications to the polymer substrate, which can be relatively complex [94] [95].

Nanoparticle film deposition is a promising technology that also requires the extra fabrication step in producing a polymer stamp, but it has not yet been shown to be capable of producing thick film metallization on PDMS. Finally, ELD is a chemical process that first requires the polymer surface to be selectively activated or modified,

typically using either μCP or the inkjet printing of catalysts [28]. Even after surface modifications, the consistent and reliable deposition of thick metal films directly onto PDMS has proven difficult [95].

2.5. Electrodeposition

Electrodeposition is one of the most established methods of depositing metal layers onto conductors. It is an effective metal deposition process that, unfortunately, requires a conductive seed layer and cannot be used to deposit metal layers onto polymers directly. The terms “electroplating” and “electrodeposition” are commonly used interchangeably. However, electrodeposition is a general term for the electrolytic deposition of metal onto an electrically reducing cathode. In contrast, electroplating occurs by the process of electrodeposition, and often involves the coating of an object’s surface with a thin metal layer to exploit the different material properties of the coating layer. Copper is most often used in electrodeposition processes in the electronics industry due to its electrical properties, simple bath chemistry, and relatively forgiving processing steps. However, other metals such as gold, platinum, and nickel are also routinely deposited [96] [97] [98]. This versatility in conductor material selection is one of the great benefits of electrodeposition. In many cases, any of these common metals may be selected, depending on the application requirements.

Copper electroplating has been reported as early as 1810 [99], and in 1831 was demonstrated by the English inventor Henry Bessemer as an effective method of producing steel castings of insects, plants, and small amphibians [100]. In the 1960s, the early years of the electronics industry, copper electrodeposition through photolithographic masks was developed as a way to pack narrow conductors within small regions for high-density electronics [101]. By the 1970s, electron beam and X-RAY lithography were used in conjunction with copper electrodeposition to produce high aspect ratio electronics with vertical sidewalls [101].

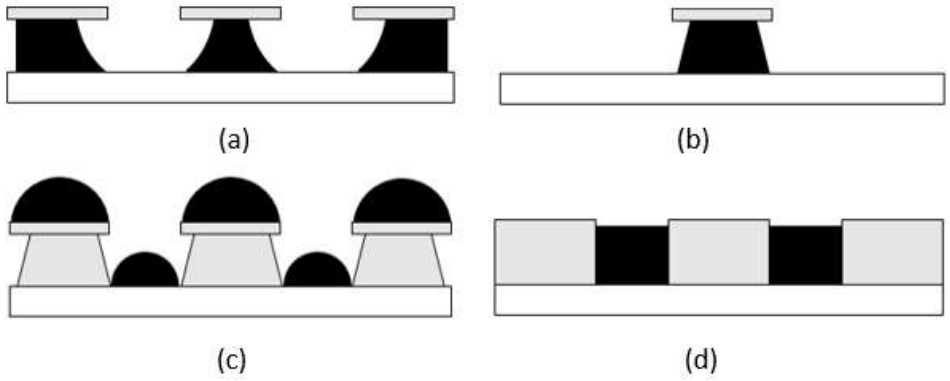


Figure 4. Various methods of metal deposition for high aspect ratio features. The deposited metal is coloured black, while masking and photoresist features are coloured grey. (a) Chemical etching results in undercut, (b) sputter etching, ion milling, and/or RIE result in a 'shrinking umbrella' effect, (c) lift-off results in spherical conductors and an 'expanding umbrella' effect, while (d) electrodeposition with X-RAY lithography results in straight and vertical sidewalls.

The vertical sidewalls of metals produced by electrodeposition and X-RAY lithography compared to conductors produced by other deposition techniques are shown in Figure 4. Here we see the conductor profiles (coloured in black) that result from various fabrication techniques including (a) chemical etching, (b) ion milling or reactive ion etching (RIE), (c) lift-off, and (d) electrodeposition. Although the conductor features are exaggerated, electrodeposition is able to produce the highest density and resolution of conductors in high aspect ratio electronics due to superior vertical sidewalls [101]. The relative advantage of electrodeposition and X-RAY lithography in terms of resolution and aspect ratio also applies to inkjet printing and shadow masking. For example, the resolution limit of inkjet printing is generally greater than one micrometer [81], while it is difficult to achieve high aspect ratio patterns with shadow masking due to the resolution and loading limitations shown in Figure 3.

In addition to a producing a desirable conductor profile, electrodeposition has the added benefit of being both inexpensive and versatile in terms of target substrates and deposited materials. The largest capital expense of most fabrication processes is the specialized equipment required for deposition and lithography. For electrodeposition through photolithographic masks, the equipment required for photolithography cannot be avoided. However, no other specialized equipment is required for deposition other than a

source of electric potential, a bulk source of metal ions, and an electrodeposition bath. Compared to other deposition equipment, such as the equipment required for electron-beam evaporation or ion-beam sputtering, the equipment required for electrodeposition comes with greatly reduced complexity and cost.

Concerning versatility, a distinct advantage of electrodeposition is shown by the early work of Bessemer mentioned previously in this section, where irregular 3D shapes are electroplated from all directions, rather than perpendicular to one planar surface alone [100]. Electrodeposition is also a highly adaptable process, with considerable flexibility in the selection of deposition parameters. This enables the control of various physical properties of the deposited material, such resistivity, internal stress, adhesion strength [102], and ductility [103]. This optimization of parameters can be of great benefit to many applications. For example, optimizing the ductility of deposited metals makes them more attractive for use in stretchable electronics applications. More advanced electrodeposition methods enable the deposition of metal composites [104] [105], and even metal-in-non-metal matrix materials for photoactive and energy storage applications [106] [107]. As mentioned previously, a variety of metals such as nickel, gold, copper, and platinum are routinely deposited. This flexibility in material selection allows for a wide range of mechanical and electrical requirements to be met. In addition, electrodeposition is easily scaled and can be performed on arbitrarily large substrates, assuming that a suitable bath can be constructed. In contrast, standard metal deposition equipment often limits the substrate size to typical silicon wafer dimensions (currently 4 to 12 inches in diameter).

In the 1980s, the use of electrodeposition expanded beyond the electronics industry and into MEMS through a process known as LIGA (Lithographie, Galvanoformung, Abformung) [108]. Although LIGA is only one among many fabrication processes developed during this period and through the 1990s for the fabrication of MEMS, LIGA became recognized as the most promising method for the mass fabrication of 3D microstructure components [109]. In the LIGA process, 3D metal structures are fabricated via electrodeposition through high aspect ratio poly(methyl methacrylate) (PMMA) photoresist using synchrotron (X-RAY) radiation. These metal structures are

then used as molds in an injection molding process, producing low-cost copies of plastic components with micro- and nano-scale features.

A great innovation of LIGA over previous uses of electrodeposition is that it is used to fabricate MEMS devices, rather than coatings or simple conductors, having micro- and nano-scale precision while remaining compatible with relatively large-scale physical processes. However, complications arising from the use of synchrotron lithography and chemical processing during mold release make this process relatively expensive and complex. Synchrotron lithography involves the use of X-RAYs as an exposure source, and requires a synchrotron radiation source that can cost between $20 million and $100 million [110]. The use of X-RAYs also comes with many fabrication challenges compared to optical lithography, but does allow for high aspect ratio patterning of thick-film resists that are sensitive to X-RAY radiation [110]. For nickel deposited on silicon, a typical example of the LIGA process, a complete chemical etch of the silicon substrate is also required to release the nickel mold [111].

Complications aside, the use of a sacrificial substrate for electroforming and patterning thick metal layers is an appealing concept. We propose that this method could be applied to overcome some of the challenges associated with the fabrication methods discussed in Section 2.4. For example, the problems of poor adhesion and film reliability that result from the deposition and patterning of metal layers on PDMS directly could be overcome by electrodeposition and patterning on a sacrificial substrate before transferring to PDMS. In addition, if the transfer proceeds without use of hazardous chemicals, then the direct transfer to a wide variety of substrates (perhaps even biological substrates) may be possible. Finally, although LIGA is traditionally used to fabricate 3D microstructures or MEMS devices, the electrodeposition process can also produce micropatterned, thick-film, metal conductors in general. Such films are attractive for applications requiring highly-conductive, low power electronics. For these reasons, we propose the development of a new metallization process using simple fabrication steps and minimal lab equipment, where thick-film electrodeposited micropatterns are transferred from a sacrificial layer to uncured PDMS. The proposed process uses standard lithography and an IR-assisted transfer process, resulting in highly conductive microstructures embedded in a flexible substrate.

2.6. Stretchable Geometries

Using a given fabrication process, stretchable metal patterns on polymers are generally achieved in two ways. The first method employs out-of-plane surface waves formed by pre-stressed thin metal films [112] [113], while the second method uses in-plane metal geometries that are able to stretch via the bending of curves in a serpentine pattern [114] [115] [116] [117] [118]. As mentioned previously in this chapter, this thesis focuses on thick-film metal conductors due to their enhanced conductance compared to thin-film conductors. In this case, the method of compressed surface waves is generally not applicable, since thick films do not buckle at the same scale as nano-scale films under compressive strains. Therefore, we focus on in-plane patterns.

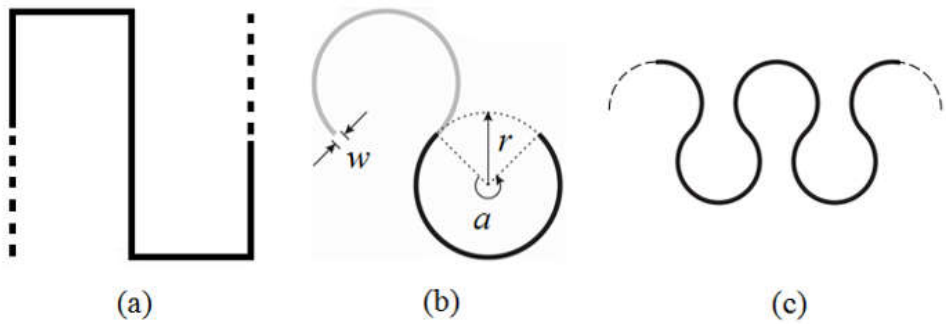


Figure 5. (a) A traditional unit Peano curve and (b) modified unit Peano curve, defined by trace width w, radius r, and arc angle a. (c) A first-order Peano curve is a repeated unit horseshoe pattern [29].

In the work of Rogers et al. [115], an in-plane, fractal-inspired, space-filling curve (or Peano curve [119]) is investigated to support biaxial and radial strains while allowing for a range of conductor topologies that can be tailored to a given application. The traditional unit Peano curve is shown in Figure 5(a) [119], along with the modified unit Peano curve having rounded corners in Figure 5(b) [115]. A horseshoe pattern repeated in one direction describes a first-order Peano curve, as shown in Figure 5(c).

Bendable serpentine patterns are formed by periodically repeating the horseshoe pattern shown in Figure 5(b), defined by the trace width, *w*, arc angle, *a*, and radius, *r*. A scale factor equal to r/w is also defined to describe this pattern, which is independent of arc angle [118]. Uniaxial strains can be applied to the pattern in Figure 5(c) while conductivity is maintained. Higher-order Peano curves are formed by repeating the unit

horseshoe geometry in fractal-based patterns, and can support biaxial and radial strains [115]. Although several groups have simulated and characterized sets of first-order curves, the systematic characterization of fabricated curves through parameter variation has yet to be accomplished. The first characterization that has not been fully explored investigates the relationship between the strain measured at conductive failure and the scale factor, r/w. One set of simulations using first-order curves has shown that increasing the scale factor leads to a decrease in strain within the conductor during stretching [118], which can be interpreted as an increase in stretchability. Another set of simulations using second-order curves has shown that, at a certain point, increasing the scale factor can decrease the strain measured at the onset of plastic deformation within the conductor, which can be interpreted as a decrease in stretchability [115]. The scale factor that results in the largest strain before the onset of plastic deformation can be defined as the optimal scale factor. In Chapter 5, we test geometries with targeted scale factors to reconcile these results.

The second unverified result relates a curve's stretchability to its arc angle. Previous simulations have shown that the strain measured at the onset of plastic deformation within the conductor increases proportionally to the arc angle, from 180˚ to 270˚ [115]. However, we have found no studies that verify these simulations by testing fabricated patterns with arc angles increasing from 180˚ to 270˚, nor have we found studies that show that arc angles greater than 270˚ have been either simulated or fabricated.

Finally, the ability of serpentine metal patterns to recover after being stretched beyond conductive failure and relaxed should also be explored. Previous studies have performed cyclic testing of such patterns at relatively lower strains to measure the response to fatigue [120], but we have been unable to find results that demonstrate cyclic failure beyond conductive failure and recovery.

2.7. Statistical Assessment

In this thesis, multiple samples and measurements are made to provide a statistical assessment of the measured values. For example, to determine the minimum

feature size of the new process, ten samples each of several test structure geometries are fabricated and assessed for reliability. This is not statistically rigorous, but if all ten samples of a feature are successful at a given resolution, then it is reasonable to expect that this feature is within the resolution limits of the process. We also expect variability during the measurement of thickness, resistivity, and surface roughness.

To provide a statistical assessment of the mean and standard error of the mean of the measured properties, five samples are fabricated and characterized for each metric/deposition time combination. The five samples used to measure each metric can be thought of as a population, as there are no additional samples fabricated in this thesis. However, to draw general conclusions about the process as it applies to any number of samples, we treat these measurements as a population sample, rather than an entire population. Reflecting this, the equations for statistical mean and standard error of the mean are shown in Equations 12 and 13 [121]:

$$\bar{x} = \frac{1}{n}\sum_{i=1}^{n} x_i \tag{12}$$

$$SE = \frac{s}{\sqrt{n}} \tag{13}$$

where $\bar{x}$ is the sample mean, n is the number of samples, x_i is the ith measurement value, *SE* is the standard error of the mean, and *s* is the standard deviation of the population sample, calculated using Equation 14:

$$s = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \bar{x})^2}{n-1}} \tag{14}$$

Confidence intervals are used to further describe how likely the observed sample data is to match the actual population data. A confidence interval (CI) is an estimated range of values that is likely to contain the actual, but unknown, population parameter. The probability that a given confidence interval contains the true value of the parameter

is called the level of confidence, C. Since the true mean and standard deviation of the population are not known, the sample mean follows a non-Gaussian distribution known as the t distribution. This distribution approaches the Gaussian distribution as the number of samples in a normally distributed population increases. The t distribution is also described by the corresponding degrees of freedom (DOF), which is simply $n-1$. To find the confidence level C of a given CI, Equation 15 is used [121]:

$$CI = \bar{x} \pm t^{*}SE \tag{15}$$

where t^{*} is the upper *(1-C)/2* critical value for the t distribution with *n-1* DOF. The value for t^{*} is commonly referenced in tabulated t –tables.

Chapter 3.

A New Approach to PDMS Metallization

The main focus of this chapter is to describe a new process for the fabrication of flexible and stretchable electronics that overcomes many of the challenges described in Section 2.4. We begin in Section 3.1 by expanding on the challenges outlined in Section 2.4, particularly as they relate to the deposition and patterning of metal on PDMS. These challenges include metal patterning and PDMS adhesion, process integration and adaptability, and the fabrication of aligned multi-layer devices. In Section 3.2, we present a detailed description of a new fabrication process designed to overcome these challenges.

Through the development of this process, our research has produced a unique approach to transferring metal micropatterns to polymer substrates. In Section 3.3, we highlight several key components of the new approach that enable us to overcome the challenges described in Section 3.1. In Section 3.4, we discuss how process integration, adaptability, scalability, and cost are addressed. The remaining challenges relating to conductivity (electrical properties), stretchability (mechanical properties), and adhesion are addressed with significant characterization data in future chapters and referenced appropriately in Section 3.5.

3.1. Open Fabrication Challenges

In this section, we expand on the challenges associated with the fabrication of flexible and stretchable electronics introduced in Section 2.4. These challenges include adhesion at the conductor-polymer interface; the ability to integrate additional materials, processes, and standalone components; and, the development of aligned, multi-layer

devices. These challenges, particularly as they relate to the metallization of PDMS, are discussed here in detail.

3.1.1. Patterning and Adhesion

One of the main challenges of depositing and patterning metal layers onto cured PDMS is that PDMS surface properties ultimately cause poor metal-PDMS adhesion. These properties include the abundance of unreacted oligomers and low surface energies, which require surface treatments for reliable adhesion [122] [123] [124]. Another aspect preventing adhesion is that the metal layer is normally deposited on top of a flat, cured PDMS surface, resulting in a top surface with the metal sides and metal-to-PDMS interface exposed and prone to delamination. The deposition and patterning of a metal layer directly onto cured PDMS is a common trait among the existing fabrication processes discussed in Section 2.4. In contrast, the proposed method of transferring an electrodeposited, pre-patterned metal layer into uncured PDMS is meant to improve adhesion of the metal layer by mechanically locking the patterned sidewalls within the PDMS substrate as it cures.

In addition to encapsulating the metal layer sidewalls in PDMS, controlling surface roughness may also be used to improve adhesion. For typical electronic applications, such as electrical interconnects, roughness should generally be minimized. However, surface roughness can have a positive impact on polymer-metal adhesion [125], with one study being entirely dedicated to producing extremely rough plated copper surfaces [126]. Increased surface roughness also results in increased surface area, which may be beneficial in applications such as electrochemical sensing [127]. In contrast, most studies attempt to minimize the roughness of electroplated layers for improved uniformity and conductivity. For example, a root-mean-square (RMS) surface roughness of 10 nm is reported for electroplated copper [128], while super-conformal copper electroplating with 500 nm features is also reported [129]. Methods of controlling roughness, whether to improve conductivity or adhesion, are dependent on the conductive seed layer morphology and deposition parameters. As the studies relating to surface roughness have shown [128] [129], electrodeposition allows for the regulation of a wide range of surface profile characteristics. As a result, this

enables a customized balance of adhesion and uniformity in the deposited metal layer. It is therefore important to analyze the surface profile of the conductors deposited using our proposed process, and any ability to control these parameters presents a significant opportunity.

3.1.2. Integration and Adaptability

The deposition and patterning of a single conductive layer is one among several steps required to fabricate a functional device. Additional materials, processes, and fabrication techniques may need to be integrated, such as NCPs for sensing and actuation [72] [130], or micromolded polymers for MEMs applications [71]. Along with sensors and actuators, microprocessors and other components may require integration, and it is important that establishing electrical contact with these components is possible. Therefore, the ability to solder external components to deposited films is a requirement of the newly developed process.

In addition to system-level fabrication, where the integration of sensors and/or other materials for functional purposes is the main concern, one of the principal motivators for this work is to allow the integration of these systems with unconventional substrates. Therefore, developing a process that allows for a simple transfer of a flexible, conductive layer to a variety of substrates remains an important challenge. One approach that addresses this challenge is to develop a patterned metal layer stamp on a sacrificial substrate that can be transferred to a variety of surfaces using an intermediate adhesive layer. Stamping pre-patterned metal layers directly onto the skin [20] is an example of this approach that has inspired our work to develop a similar stamping process. In contrast to this existing approach [20], we wish to develop a low-cost alternative while eliminating the use of specialized deposition equipment and strong acids during the transfer process. As another example of stamping onto unconventional substrates, we also wish to transfer conductive metal layers directly onto micromolded polymers. As demonstrated in Section 3.4.1, this allows for 3D NCP polymer structures to be integrated with the conductive layer in 3D devices.

One challenge of the stamping technique is that integrating alignment features may be required to align the stamp pattern with the target substrate. However, this requirement also presents an opportunity to integrate functional materials with the alignment features and to fabricate aligned multi-layer devices. The integration of functional materials with alignment features and the demonstration of an aligned multi-layer device are both presented in Chapter 6.

3.1.3. Multilayer Devices

The fabrication methods discussed Section 2.4 often result in the deposition of a single conductive layer. However, multi-layer devices offer many advantages compared to their single layer counterparts. In particular, multi-layer conductors can accommodate more current, which is important for high-current applications such as electromagnetic actuators; they enable increased functionality, as some devices inherently require multiple layers, such as semiconducting devices; and, they increase overall device density by extending a fixed two-dimensional (2D) area vertically. 3D polymer microstructures are found, for example, in multilayer SU-8 tissue scaffolds [131] and in 3D PDMS channels in microfluidic devices [132]. While these applications stack and align polymer layers, they do not include integrated conductive layers. One method of stacking conductors onto PDMS is through a micropattern transfer process, where patterned CNT-based conductive inks are transferred onto PDMS layers successively [133]. However, the lack of alignment features makes it difficult to achieve alignment between layers. Rather than using highly resistive inks, an alternative approach incorporates the injection of liquid solder into aligned, 3D PDMS microfluidic channels [134]. These liquid solder channels cool and solidify to form aligned 3D conductive layers. Although this is a creative solution, the injection of liquid metal into microfluidic channels requires high temperatures and fluid pressures during processing, which can be especially difficult over large areas. An approach quite similar to what we desire is seen in the fabrication of multi-layer electrode arrays in PDMS for neural stimulation [135], where metal foils are deposited onto PDMS and selectively patterned using a serial laser etching process. The process is repeated to achieve multi-layer devices. Again, without alignment features, multi-layer alignment remains difficult. More importantly, the laser-etching step is a serial process that is difficult to scale to large

volume production. Our proposed solution is to incorporate alignment features with the stamping process mentioned in Section 3.1.2, so that multiple conductive layers can be stamped and aligned with the target substrate.

3.1.4. Additional Challenges

Scalability and cost are important factors in any fabrication process, and can be particularly challenging when adapting a new process to large-scale production. Therefore, the scalability and cost of the newly developed process are discussed in detail in Section 3.4.2. The remaining challenges relating to conductivity (electrical properties), stretchability (mechanical properties), and adhesion are addressed with significant characterization data in future chapters and referenced appropriately in Section 3.5.

3.2. Detailed Design and Fabrication

In this section, we present the detailed description of a new fabrication process designed to overcome the challenges addressed in Section 3.1. We begin with an overview of the process flow, as illustrated in Figure 6. In Figure 6(a), the sacrificial layer begins with a multipurpose transparency film. (b) A conductive paint seed layer is deposited onto the transparency film via airbrushing, and is air-dried for 24 hours. After drying, the seed layer is mechanically polished to reduce the initial roughness of the surface. The polished seed layer is then optionally processed in a tinning solution to increase surface conductivity. In this thesis, half of the samples are tinned to assess the effectiveness of the tinning processing step. (c) A dry-film photoresist is laminated onto the seed layer, and (d) processed using standard photolithography. (e) The copper metallization layer is grown via electrodeposition through the masking pattern defined by the photoresist, followed by (f) a photoresist strip to expose the copper layer. (g) The assembly is then placed face down over uncured PDMS on a glass substrate, degassed, and pre-baked. Once the PDMS cures in the pre-bake to the point that peaks no longer form when contacted with a glass rod, the assembly is treated with IR heat from above. (h) During the IR heating stage, the metallization layer is detached from the sacrificial seed and embedded in the PDMS without exposing the outside walls or bottom metal-to-

PDMS interface to the environment. This eliminates the need for PDMS surface modifications to promote adhesion, and is one of the defining features of our process. Additional details are provided in Section 3.2.5. (i) The metallized PDMS is then optionally covered with an encapsulating layer of PDMS before (j) being removed from the glass substrate. The encapsulation layer can be added after removing the bottom PDMS layer from the glass substrate, if desired. However, the integration of other components (Section 3.4.1) is often more reliable when the assembly remains on the glass substrate. Encapsulating the metal layer as soon as possible reduces prolonged exposure of the metal layers.

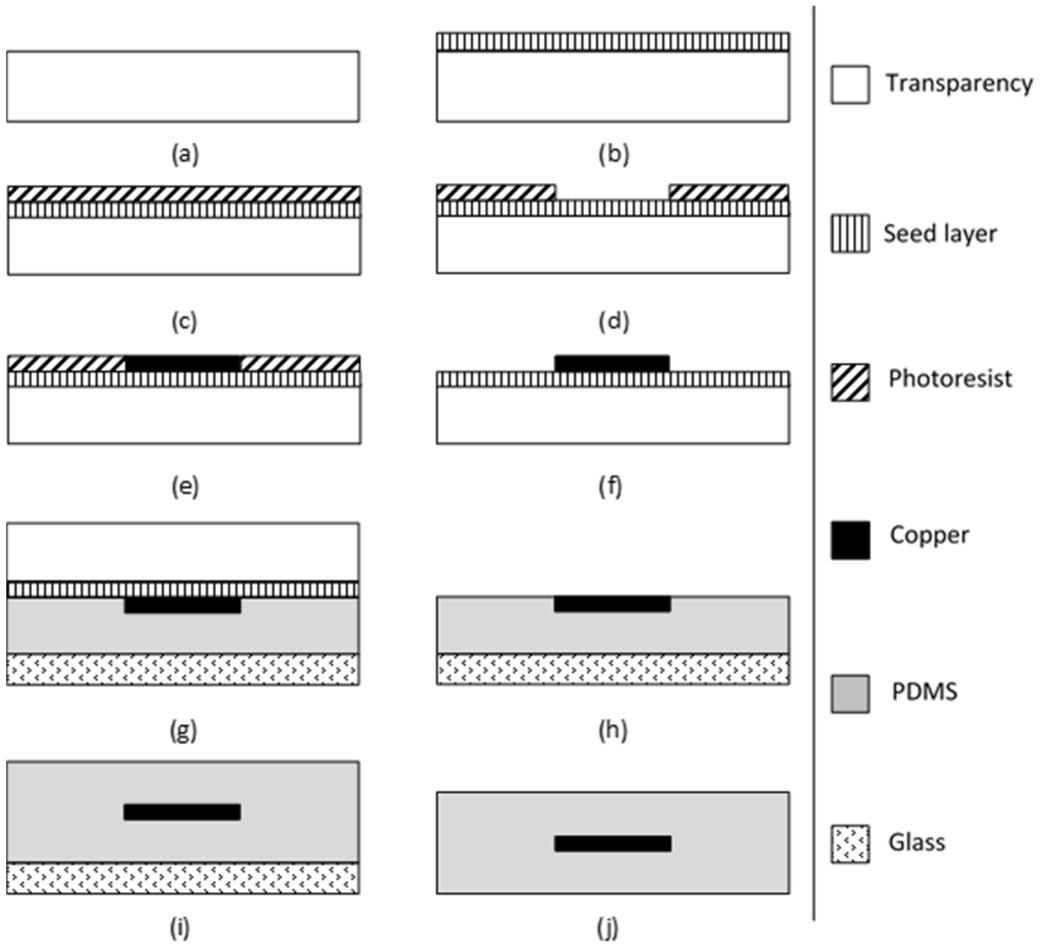


Figure 6. Process diagram for PDMS metallization, illustrating the (a) transparency substrate, (b) airbrushed seed layer, (c) laminated and (d) patterned dry film photoresist, (e) electrodeposited copper, (f) photoresist stripping, (g,h) IR-assisted transfer to PDMS, (i) encapsulation, and (j) removal of the metal-in-PDMS assembly.

3.2.1. Equipment and Materials

Multipurpose transparency sheets measuring 8.5 inches by 11 inches (3M™ model PP2950) are used as substrates for the conductive seed layer. The chemical composition of the transparency sheets is not known, as this information is not provided by the manufacturer. Copper conductive paint (Caswell Canada) is airbrushed onto the substrate using an Iwata Neo CN airbrush with a Mastercraft 3 gallon air compressor. Mechanical polishing is performed using several grades of abrasive sheets (Norton Abrasives and Klingspor Abrasives). The seed layer is processed in a tinning solution (Caswell Canada) to improve conductivity. The copper electrodeposition solution (Caswell Canada) includes two proprietary copper brighteners. Dry film photoresist (DuPont Riston MM540) is used to define the electrodeposition patterns, and is laminated onto the seed using a hot roll laminator (Apache AL13P). The photoresist is patterned using an ABM mask alignment and exposure system. Photoresist development and stripping are performed using an Na_2CO_3 solution and methanol, respectively. The PDMS base elastomer and curing agent (Sylgard® 184, Dow Corning Inc. USA) are mixed and degassed before the metal transfer stage. IR radiation (General Electric, 250W) promotes delamination of the metal layer from the seed. Note that a characterization of the IR source in terms of radiation intensity versus wavelength is not provided. All equipment is used as-is from the manufacturers, and materials are processed according to the manufacturers' recommendations.

3.2.2. Sacrificial Seed Layer

This subsection describes the deposition, mechanical polishing, and tinning of the sacrificial conductive paint seed layer. Transparency films (3M™) form the base layer for the sacrificial substrate, and are optionally pre-cleaned with deionized (DI) water. Chemical solvents are not used during cleaning. This maintains the hydrophilic coating as supplied by the manufacturer and promotes adhesion of the paint to the film. The seed layer is deposited using an Iwata Neo™ airbrush, operated at an air pressure of 40 PSI using a three gallon air compressor. The conductive paint is mixed at a 6:1 ratio with deionized (DI) water to achieve the optimal consistency for airbrushing (found empirically).

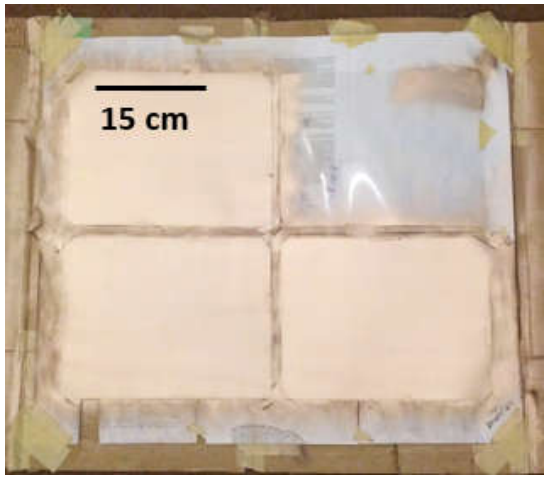


Figure 7. Four transparency films used as airbrushing targets. Three films have a deposited paint layer, while one remains bare.

Airbrushing proceeds in a standard laboratory fume hood for ventilation and safety purposes. Multiple transparency substrates are taped to a cardboard backing and each is sprayed with 18mL of the 6:1 paint mixture. The amount of DI water in this mixture is found empirically to be both necessary and sufficient for producing a well-formed seed layer. The airbrush target setup is shown in Figure 7, where three of four transparency films have undergone the paint deposition process.

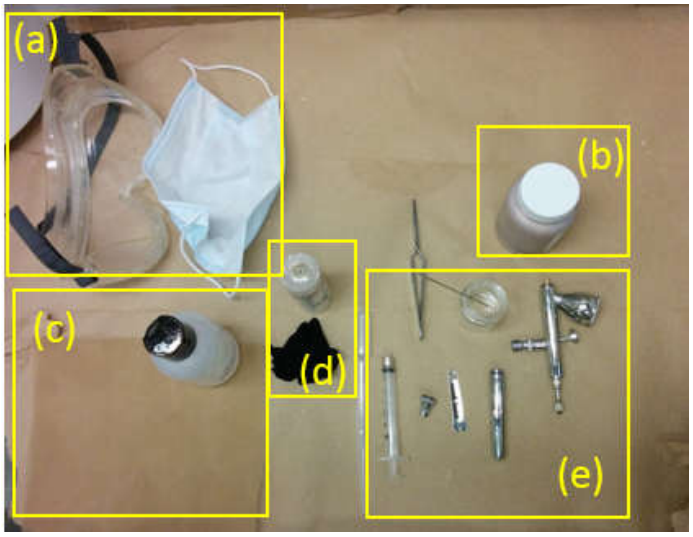


Figure 8. Airbrushing materials, including (a) safety equipment, (b) conducive paint, (c) primary aliquot container with coarse mesh filter, (d) secondary aliquot container with fine mesh filter, and (e) the deconstructed airbrush with miscellaneous cleaning tools.

Figure 8 shows a subset of the necessary equipment and materials used during airbrushing, including safety materials, paint filters, and the airbrush. Two stages of filters are used. A coarse filter is used in the first stage as the paint is transferred to a primary aliquot. A fine filter is used in the second stage as the paint is transferred to a secondary aliquot. This filtering removes large particles that can clog the airbrush nozzle.

Airbrushing does not require technical training, and is relatively simple compared to alternative deposition methods that use sophisticated laboratory equipment. However, effective airbrushing is a craft. Paint composition, airbrush selection, substrate properties, deposition parameters, and the deposition environment all play important roles in the quality of the deposited layer. Deposition parameters include considerations such as distance to target, source air pressure, and airbrush nozzle diameter. Similarly, environmental parameters include considerations such as temperature and humidity. The purpose of this thesis is not to explore the intricacies of airbrushing, and a detailed discussion of the possible effects due to variations in airbrush processing parameters is not included. Fortunately, the technique used in this thesis is simplified by the deposition of uniform paint layers on a flat, featureless target.

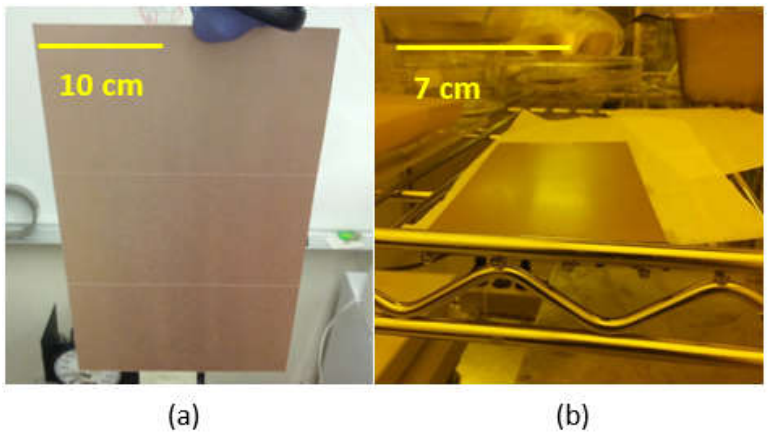
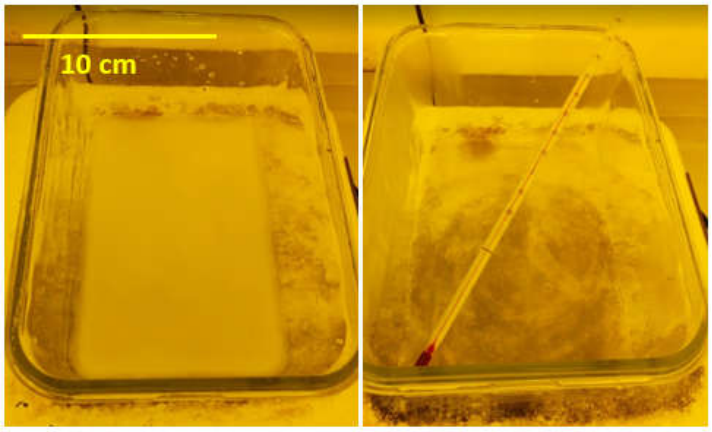


Figure 9. Paint surface after deposition and drying, (a) before and (b) after polishing.

After deposition, the painted assembly is left to dry overnight. When dry, the assembly is removed from the enclosure, and the seed layers are mechanically polished by hand using abrasive sheets to produce a smooth, uniform surface. The seed layer

exhibits a rough surface before polishing, as shown in Figure 9(a), while a mirror-like finish can be seen after polishing in (b). This surface roughness is characterized in detail in Section 4.2.2. To achieve a smooth final surface, four abrasive sheets are employed with grit ratings increasing from 400 to 1200. After polishing, a single sheet measuring 8.5 inches by 11 inches is cut into six segments of equal size according to the electrodeposition bath dimensions, with each segment measuring approximately 7 cm by 14 cm.



(a) (b)

Figure 10. Tinning solution bath setup, showing (a) an opaque solution at room temperature and (b) a transparent solution at 50°C.

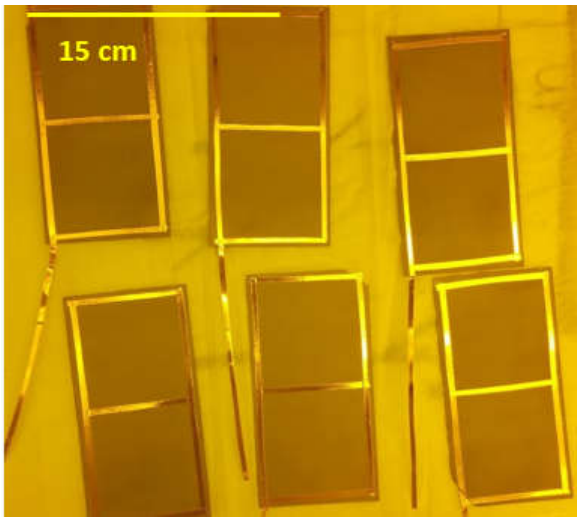


Figure 11. Six seed layer samples originating from a single transparency film after mechanical polishing, tinning, and the application of conductive tape.

Polished seed layers are immersed in a tinning solution at 50°C for 5 minutes to increase surface conductivity, as recommended by the manufacturer. The tinning solution is initially opaque at room temperature and transparent when heated to 50°C, as shown in Figure 10(a) and (b), respectively. After tinning, copper tape with a conductive adhesive backing is applied around the perimeter of the substrate, with a trailing portion approximately 15 cm in length used to establish an electrical connection to the external power source during electrodeposition. Constraining the seed layer area enclosed within the copper tape to less than 20 square inches ensures a uniform deposition layer within the enclosed area. Six seed layer samples from a single transparency film are shown in Figure 11.

3.2.3. Dry Film Photoresist

Dry film photoresist defines the metal patterns during electrodeposition. DuPont Riston MM540 photoresist sheets, measuring 30 cm wide with a thickness of 36 μm, are laminated onto the seed layer using a hot roll laminator. Early experiments show that liquid photoresists are difficult to develop and strip from the conductive paint, while dry films are relatively simple to process. It is suspected that this is due to liquid photoresist percolating into the granular paint seed, as opposed to dry films that remain intact above the surface.

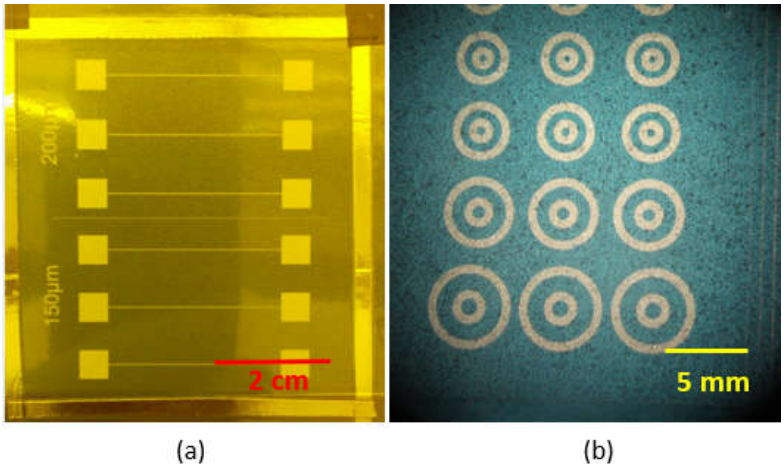
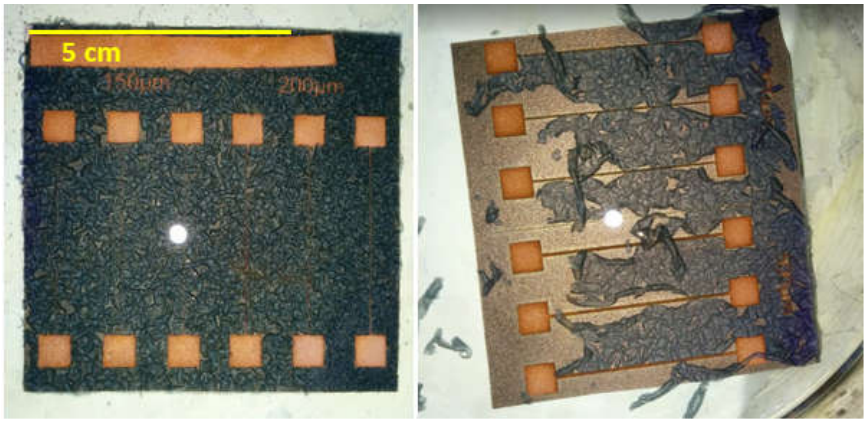


Figure 12. (a) Wide-field and (b) magnified views of photoresist features after exposure and development

During lamination, the photoresist is laid manually onto the seed and hot-rolled at a temperature and speed of 115°C and 70 cm/minute, respectively. The seed layer surface is pre-wetted with DI water immediately before the photoresist is applied, which enables unwanted air bubbles between the seed and photoresist to be pressed out manually before lamination. The thin DI water layer also promotes consistent photoresist patterning and development, and encourages delamination during the stripping process. After lamination, the photoresist is patterned with a 25 mJ/cm^2 exposure over a period of one second provided by an ABM mask alignment and exposure system. Mylar film photomasks are used to provide the pattern template. After exposure, development takes place in a Na_2CO_3 bath with a concentration of 1% by weight for 3 minutes.



(a) (b)

Figure 13. Photoresist stripping process via methanol immersion. (a) The photoresist begins to wrinkle before (b) delaminating, rather than dissolving.

Figure 12 shows a wide-field view (a) and a magnified view (b) of the photoresist layer after exposure and development. These patterns are discussed further in Section 4.1.4. After development, the assembly proceeds to the electrodeposition stage (Section 3.2.4), and is followed by photoresist stripping. Photoresist stripping is performed via three minutes of agitated immersion in methanol at room temperature. In contrast to liquid resists, the photoresist in this process is delaminated rather than dissolved during stripping. This behaviour is shown in Figure 13.

3.2.4. Copper Electrodeposition

Copper electrodeposition is performed in a sulfuric acid (H_2SO_4) bath composed of DI water, copper crystals (copper sulfate pentahydrate), sulfuric acid, and two proprietary copper brightener components (Brightener A and Brightener B).

Table 2. Electrodeposition bath composition for one litre of solution [30].

Total (L)	Water (L)	Copper Crystals (g)	H2SO4 (mL)	Brightener A (mL)	Brightener B (mL)
1	0.92	200	83.4	7.8	1.6

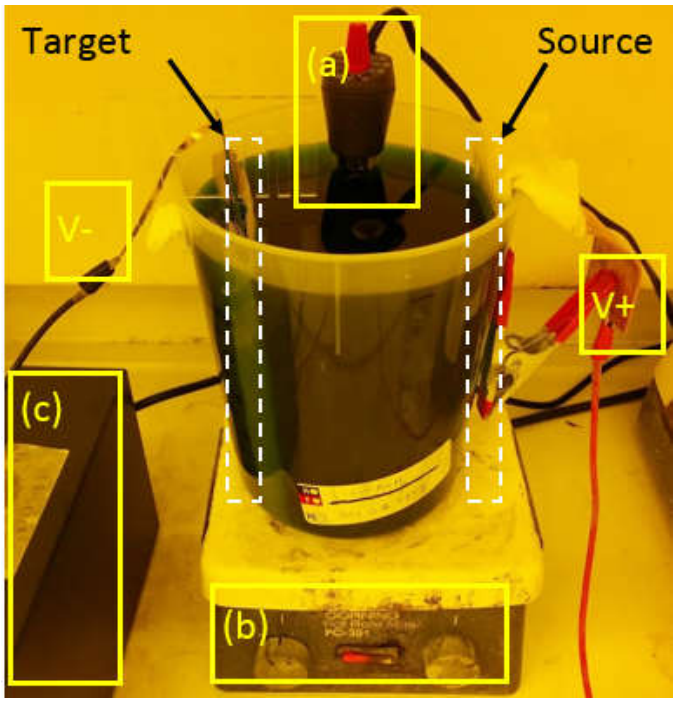
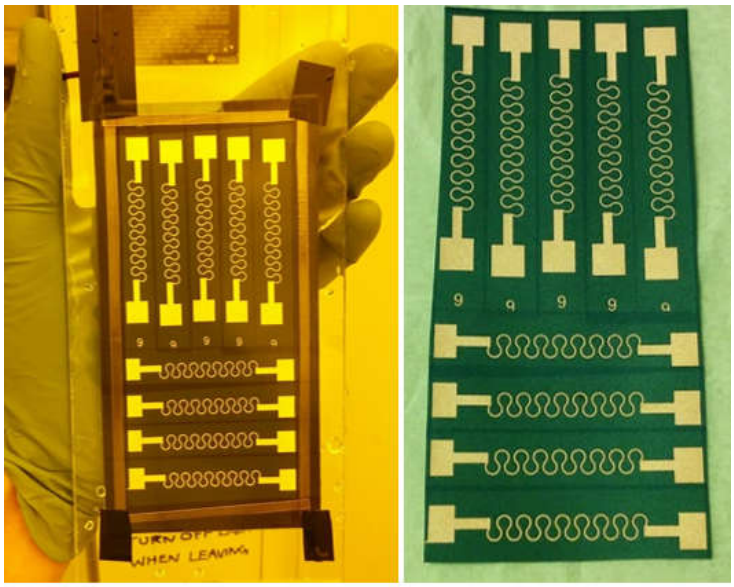


Figure 14. Electrodeposition setup. A two litre PP container holds the sulfuric acid bath. (a) The heater, (b) magnetic stirring plate, and (c) a portion of the power supply are visible, along with connections to the source (V+) and target (V-).

For a one litre bath, the quantities of each component are given in Table 2. Electrodeposition is performed with a constant direct current density between the source and target of 10 mA/cm^2 at 30 °C under agitation provided via magnetic stirring. Voltage levels are not monitored during deposition. The bath is contained in a two litre Nalgene

polypropylene (PP) beaker, shown in Figure 14. Before deposition begins, test strips (BDH® 35309.606) are used to provide an approximate measure of the pH level from 0 to 14. These measurements indicate that the bath pH always remains below a level of 3. The pH level of the bath is recommended to be within 1.2 to 2.7 by the manufacturer. However, in the current iteration of the process, the pH level is neither precisely monitored nor controlled. After deposition, DI water is added to compensate for water loss due to evaporation and restore the bath to its original level before deposition.

Additional bath components shown in Figure 14 include (a) the aquarium heater, (b) the magnetic actuation plate, and (c) the direct current (DC) power supply. The magnetic actuation plate provides a rotating magnetic field to a one inch stir bar at the bottom of the bath. The seed layer (target) is mounted on a PMMA dipping plate and surrounded by a nylon mesh within the bath. The bulk copper anode (source) is enclosed within a white anode bag, visible on the right side of the bath in Figure 14. This anode bag prevents impurities released from the copper anode during plating from mixing into and contaminating the bath. Electrical connections from the target (V-) and the source (V+) to the power supply are located outside bath.



(a) (b)

Figure 15. (a) Assembly mounted on the PMMA dipping plate immediately after electrodeposition, and (b) after removal of the dipping plate and copper tape perimeter.

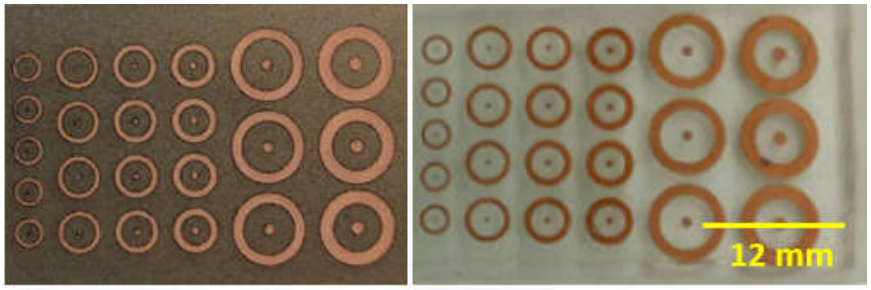
Figure 15 shows a patterned assembly mounted on a PMMA dipping plate (a) immediately after electrodeposition and (b) before photoresist stripping. The serpentine patterns seen in Figure 15 are discussed in detail in Chapter 5. A quantitative analysis of the deposited layer is provided in Section 4.2.2. However, we note here that, qualitatively, the deposited layers exhibit a degree of internal compressive stress. A single structure cut from the assembly in Figure 15 (measuring 15 mm by 65 mm) will consistently demonstrate raised edges, to a height of approximately one millimeter at each end, when placed face-down on a flat surface. This behaviour is consistent with existing copper electrodeposition studies, though tensile stresses are also possible [136] [137]. A detailed characterization of the residual stress in deposited films is to be completed in future work.

3.2.5. Transfer to PDMS

After photoresist stripping, the patterned metal layer is transferred to PDMS through an IR-assisted transfer process. This process begins by mixing the base elastomer and curing agent by hand in a 10:1 ratio by weight as recommended by the manufacturer. After mixing, the PDMS is placed in a vacuum chamber for 30 minutes for degassing. The degassed PDMS is poured over a glass substrate. After self-levelling of the PDMS, the copper assembly is placed face down on top, allowing the PDMS to flow over and surround the metal patterns. The transfer process begins by pre-baking the assembly on a hot plate for 5 minutes at 110°C, until peaks no longer form when the PDMS is contacted with a glass rod. After initial curing, the assembly is treated from above with a 250W IR heat lamp at a distance of approximately 3 inches for 30 seconds. A determination of the required IR intensity for this process is not provided in this thesis, and is left to future work.

During the IR treatment stage, the metallization layer becomes detached from the seed layer, while the seed layer remains adhered to the transparency film. The sacrificial seed-on-film assembly is then peeled away, revealing a metallization layer that is permanently embedded in PDMS without suffering from cracking, bending, or other deformations. Methanol is optionally used to rinse away seed layer residue that has

inadvertently transferred to the PDMS. This additional rinse is achieved through agitated immersion in methanol at room temperature for an additional thirty seconds, as required.



(a) (b)

Figure 16. An example metal pattern imaged (a) before and (b) after the transfer to PDMS.

An example metal pattern before and after PDMS transfer is shown in Figure 16(a) and (b), respectively. The metal pattern shown in Figure 16 is one of several structures used to characterize the minimum feature size associated with this process in Section 4.2.3.

3.3. Advantages of the New Approach

The two main innovations of this process are closely related and are directly responsible for the advantages leveraged in this section. The first innovation is the use of a sacrificial conductive paint seed layer as a substrate for electrodeposition (Section 3.3.1), and the second is the chemical-free transfer of the metal patterns to uncured PDMS using IR radiation (Section 3.3.2). In addition, although the use of electrodeposition alone is not novel, it does provide several advantages in the context of this process (Section 3.3.3).

3.3.1. Conductive Composite Paint

The use of a sacrificial conductive paint seed layer yields several unique benefits. Most importantly for our process, the sacrificial layer enables the controlled delamination of electrodeposited copper from a conductive composite seed to polymer

targets through IR radiation alone. This unique process is not demonstrated in literature. In addition, the dependence of metal-seed adhesion on seed layer properties is well-known [138], and could be explored further to promote delamination during the transfer stage. The paint used in this process is not formulated for the explicit purpose of an IR-assisted transfer. Therefore, it is reasonable to expect that the delamination process could be improved through modifications to the paint formulation. Additional adaptations of the conductive paint seed layer are discussed in the remainder of this section. Although these adaptations are not yet applied to the current version of the process, their discussion inspires several potential avenues for future work.

First, it is possible to deposit conductive paint via airbrush onto a variety of substrate materials and profiles. This allows for the deposition of metals onto irregular (non-flat) surfaces in general. As previously mentioned, this has been demonstrated through the metal casting of insects and other lifeforms [100]. In contrast, traditional seed layers, such as prefabricated metal films or rigid conductive substrates, result in flat deposited layers. The ability to deposit metal layers onto non-flat surfaces is advantageous in applications that require a deposited profile to match a non-flat target substrate. For example, flat strain gauges placed onto cylindrical targets will produce a response if the gauge is bent from its initial state to fit the target. However, if the gauge is fabricated on a matching cylindrical substrate before transferring to the target, the undesired response during fitting can be avoided. Although we only explore flat seed layer substrates in this thesis, the ability to deposit on alternative substrates presents a distinct advantage that can be explored in future work.

The use of a composite paint also allows for the modification of the chemical and physical properties of the seed layer. The ability to customize and enhance material properties while maintaining a set of requirements is a general feature of composite materials [139]. In this case, the composite material is a conductive paint and the two main requirements are (1) that the paint must adequately conduct electricity for effective electrodeposition, and (2), that the seed layer must delaminate from the deposited layer during the IR-assisted transfer process. Additional consideration is given to secondary effects, such as surface roughening in the deposited layer. Again, we do not explore alternative paint compositions in this thesis. However, we expect that alternative seed

layers in future iterations of this process will lead to conductor layers with significantly improved physical properties.

We also assume that modifications to the conductive paint seed layer can be made to improve the electrical and mechanical properties of the deposited layer. For example, research in the field of template electrodeposition shows that the physical properties of deposited layers are highly dependent on seed layer profile and composition [140] [141]. In the context of this process, the relationship between physical properties of the deposited layer, such as surface roughness, and seed layer composition remains a topic of interest. This relationship may be studied by modifying the size, shape, and density of the conductive particles while keeping the composition of the paint medium otherwise constant. In contrast, traditional conductive substrates such as metal foils and silicon wafers come “as-is,” with limited chemical flexibility and smooth, uniform surfaces. While uniformity and smoothness are often desired, some applications benefit from alternative surface profiles and patterns. For example, the performance of electrochemical sensors is often proportional to electrode surface area, which is in turn proportional to surface roughness [127]. In this case, using a paint seed layer with a similar surface profile is favourable to producing rough metal layer surfaces. In addition to roughness, the conductivity of composites is highly dependent on the composition and density of the embedded conductive particles [142] [143] [144]. Therefore, we expect that modifications to the conductive paint composition could increase seed layer conductivity and, as a result, improve the physical properties of the metal layer. These modifications may be explored in future work.

3.3.2. IR-assisted Transfer

Similar to the use of a conductive paint seed layer, the IR-assisted transfer process leads to several unique benefits. First, this process avoids the challenges associated with patterning metal layers on PDMS by first depositing and patterning metal layers on a sacrificial substrate. However, this concept is not entirely novel. The most similar process to ours involves the use of a conductive metal foil as a sacrificial substrate, onto which 10 μm-thick gold films are deposited via electrodeposition [117]. The subsequent transfer to PDMS is achieved by pouring liquid PDMS over the

deposited patterns, curing the PDMS, and finally chemically etching the metal foil substrate. However, like LIGA, the use of hazardous chemical etchants in this process is unattractive in comparison to our mild IR-assisted transfer process. The IR-assisted process is made possible by the use of a conductive paint seed layer, which delaminates from deposited metal layers during IR treatment. This IR-assisted delamination is not seen with traditional seed layer materials, and allows the deposited patterns to be stamped directly onto a variety of target substrates. This is demonstrated in Section 3.4.1 and Chapter 5, with PDMS acting as an adhesive layer to facilitate the transfer to wearable fabrics. In addition, the IR-assisted stamping process can be integrated with other fabrication processes, such as polymer micromolding and screen-printing of conductive composites (Section 3.4.1), and multilayer device fabrication (Chapter 6).

3.3.3. Electrodeposition

Electrodeposition, as a metal deposition method, is desirable for several reasons. First, the equipment required for electrodeposition is generally low in cost compared to alternative equipment such as sputtering or electron beam evaporation [145]. In addition, electrodeposition allows for arbitrarily large substrates, assuming the construction of an appropriately sized bath is feasible. This is in contrast to fixed, wafer-sized deposition chambers found in conventional deposition equipment.

More importantly for our purposes, thick films are easily deposited using electrodeposition. In contrast, stretchable electronics applications with metal conductors often rely on physical vapour deposition methods that produce thin, sub-micron films [112] [113]. Thick films are relatively durable compared to thin films, and can even withstand surface-mount and through-hole soldering processes (see Section 3.4.1). This allows for the integration of traditional electronic components and processes. Thick metal films are also highly conductive, which enables applications requiring large currents such as electromagnetic actuators (Chapter 6). Finally, in our process, thick-film deposition also provides a mechanism to promote metal-PDMS adhesion (Section 4.2.4).

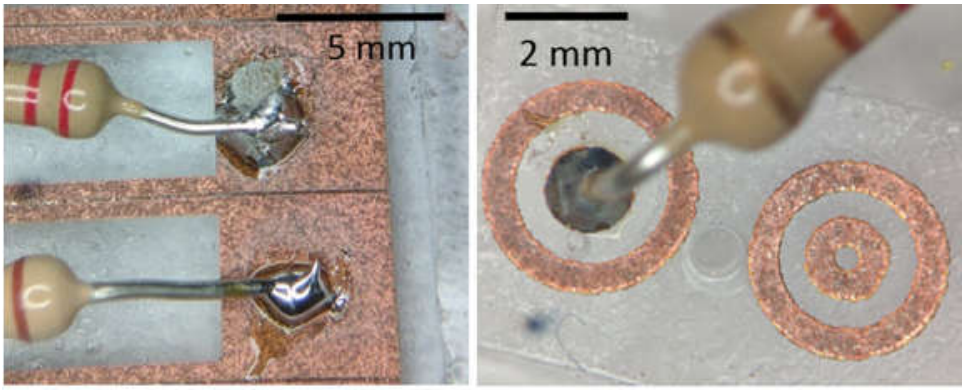
Along with the benefits mentioned in this section, there are also some general advantageous to the process as a whole. The process is simple, and none of the processing steps requires particular technical expertise. In addition, the use of a conductive paint, electrodeposition, and transfer via IR exposure are low cost processing steps and are theoretically scalable to a roll-to-roll fabrication process (Section 3.4.2).

3.4. Discussion

The discussion in this section provides a qualitative assessment of the integration, adaptability, scalability, and cost of the proposed process. Examples in Section 3.4.1 demonstrate the integration of alternative processes, materials, and components, along with adaptations of the base process to alternative substrates. The adaptations required for wearable applications and multi-layer devices are presented in more detail in Section 5.2.1 and Section 6.4.2, respectively. The cost of the proposed process in its current form is discussed in Section 3.4.2, along with the potential for large-scale adaptations. This includes an analysis of the equipment and materials required for each process step in Section 3.2. Quantitative analyses related to the adhesion mechanism, metal layer properties, and patterned feature sizes require significant characterization data and are presented separately in Chapter 4.

3.4.1. Integration and Adaptability

Section 3.1.2 highlights the importance of integrating alternative materials, processes, and fabrication techniques with emerging flexible and stretchable electronics fabrication processes. This includes the integration of NCPs for sensors and actuators, micromolded polymers for MEMS and microfluidic applications, and the ability to provide electrical connections to external or discrete components. In addition, the ability to integrate flexible, conductive layers with a variety of substrates through a simple transfer process remains an ongoing challenge.



(a) (b)

Figure 17. (a) Surface and (b) through-hole solder bonds applied directly to the deposited films.

In conventional electronics, discrete components are mounted on PCB substrates with electrical contact provided by Sn-Pb solder joints (some solders are Pb-free). However, in flexible electronics, thin metal films and conductive composites are almost entirely incompatible with traditional soldering. As a result, strategies such as anisotropic conductive films (ACF) [146] [147] and conductive composite interconnects [148] [149] are routinely used to provide electrical contact between flexible films, or between flexible films and discrete components. However, conductive composites generally cannot match the performance of metal solder joints (see Section 4.2.1 for a discussion on conductive composites). If composites are not used, discrete components require intermediate connection schemes, such as FPCBs or thinned silicon, for bonding to polymer-based devices [150] [151] [152]. Considering these difficulties, the ability to solder flexible films directly is a distinct advantage with respect to integrating with traditional electronic components. Fortunately, the thick films deposited using the newly developed process allow for direct soldering. Examples demonstrating this ability are shown using surface and through-hole connections in Figure 17(a) and (b), respectively.

While Figure 17 demonstrates the ability to solder discrete components after the films are transferred to PDMS, we speculate that a more effective strategy may be to integrate discrete components before the transfer to PDMS. This is due to the observation that, although the copper films adhere relatively well to the PDMS substrate after transfer, they are even more stable while still attached to the seed layer at room

temperature. If discrete components are added at this earlier stage, a consequence is that the components will be embedded in the liquid PDMS as it cures, similar to the copper film as it is placed face down on uncured PDMS. Additional components can then be added to the exposed metal film after transfer, allowing for the integration of discrete components on both sides of the copper films. This strategy also applies to the use of conductive inks or NCPs instead of solder.

It is important to note that the integration of discrete components is currently limited by manual placement. As a consequence, components with strict alignment requirements may not be suitable for integration with this process. For example, in complex optical systems with many individual components, precise mechanical alignment is likely to be a difficult problem using the proposed process. This is especially problematic for multi-layer devices, where inter-layer alignment poses an additional challenge to intra-layer alignment. We discuss multi-layer device fabrication and the alignment strategy used in this process in greater detail in Section 6.4.2. However, we note here that the alignment error between layers is on the order of 100 μm (see Figure 79), which is unacceptable in precision applications. Rather, the current process is more suitable for integration with components that are typically placed on PCBs, such as packaged integrated circuits, communications transceivers, and passive electrical components. In future work, we hope to develop strategies to improve both the inter-layer and intra-layer alignment of integrated components.

In the context of this thesis, adaptability and integration also refer to the ability to transfer metal layers directly to a variety of substrates though modifications to the base process shown in Figure 6. To transfer metal layers onto unconventional surfaces, the role of PDMS is converted from that of a substrate to an adhesive layer. In this manner, copper patterns can be ‘stamped’ onto a target substrate with PDMS acting to facilitate delamination from the seed and deposition onto the substrate. This modified process is shown in greater detail in Section 5.2.1, where stretchable metal patterns are transferred to fabrics for wearable electronics.

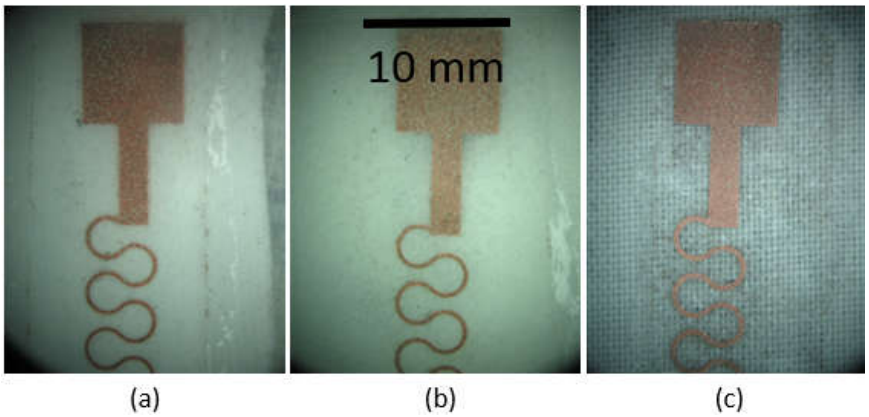


Figure 18. Metal patterns applied directly to a various fabrics through a modified stamping process. This includes (a) a stretchable crepe fabric (95% polyester, 5% spandex), (b) a stretchable constellation knit (100% mixed fibers), and (c) a non-stretchable drapery lining (100% cotton).

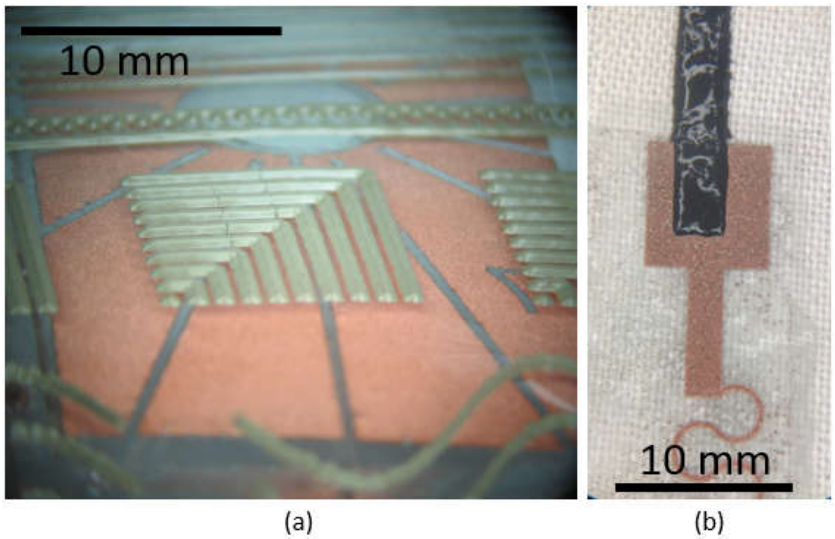


Figure 19. Modifications of the base process showing (a) the incorporation of micromolded polymers and (b) the incorporation of NCP polymer deposition.

Figure 18 provides a brief demonstration of the ability to use various fabrics as substrates using a modified stamping process. Here, stretchable metal patterns (these patterns are also discussed Chapter 5) are applied directly to (a) a stretchable crepe fabric (95% polyester, 5% spandex), (b) a stretchable constellation knit (100% mixed fibers), and (c) a non-stretchable drapery lining (100% cotton). The stretchability of these patterns on wearable fabric is studied in Section 5.2.2.

The base process is also easily modified to incorporate NCPs and micromolded polymer fabrication processes. Figure 19(a) shows the incorporation of a deposited metal layer with a micromolded NCP layer, while (b) shows the incorporation of a screen-printable conductive NCP on fabric. The incorporation of conductive NCPs enables the integration of discrete components through an alternative strategy to soldering. However, the integration of external components is currently limited to solder-based and NCP-based processes. Additional integration strategies, such as the use of ACFs, are not explored in this thesis. The modified process used to integrate polymer micromolding is described in detail in Section 6.4.2. Section 6.4.2 also demonstrates the use of the metal pattern in Figure 19(a) as an electromagnetic actuator. When combined with micromolded magneticNCPs, this process could allow for electromagnetic valves and actuators in PDMS-based microfluidic devices to be integrated on a single substrate [130]. Screen printable NCPs, as shown in Figure 19(b), have applications in wearable electronics [153], and could be used to increase the stretchability of the wearable devices described in Chapter 5.

3.4.2. Scalability and Cost

The total cost for all equipment and materials, aside from the mask aligner and not including common laboratory supplies, is less than 1000 CAD. This assumes that less than 10 ft^2 (less than one square meter) of material is required to reproduce the experiments contained in this thesis. Table 3 shows the one-time (capital) equipment and material costs required to construct a two litre prototype bath, while Table 4 shows the ongoing costs per square foot of finished product.

Table 3. One-time equipment and material costs for two litre bath.

Material/ Equipment	Bath Container	Bath Solution	Fabric Mesh	Power Supply	Stir Bar	Mylar mask	Air-brush	Air Com-pressor
Cost (CAD)	$25.00	$45.36	$3.53	$200.00	$8.15	$40.00	$75.00	$150.00
Total (CAD)	**$547.04**	-	-	-	-	-	-	-

Table 4. Ongoing fabrication cost per square foot (~0.1 m^2). Assumes 1:10 ratio of deposited copper area to substrate area.

Material/ Equipment	Tinning Solution	Conductive paint	Mechanical Polisher	Photo-resist	3M™ Sheets	PDMS	Copper Source
Cost (CAD)	$10.97	$7.70	$0.32	$4.65	$0.31	$13.01	$1.50
Total (CAD)	**$38.46**	-	-	-	-	-	-

The assumptions in Table 4 are that the PDMS transfer layer is one millimeter thick, and the deposited copper area to substrate area ratio is 1:10. In addition to a low overall cost, the fabrication of conductor layers can be achieved in approximately one day, which is highly desirable for rapid prototyping of new designs. In addition, each of the steps outlined in Section 3.2 are, in principle, easily adapted to large-scale fabrication processes.

Large-scale processes used in the fabrication of flexible devices are often roll-to-roll processes [154] [155] [156]. As such, it is highly desirable for emerging processes to be scalable to roll-to-roll systems. The following is a description of a possible roll-to-roll adaptation of the current process. First, the transparent substrates in Section 3.2.2 are scaled to rolls from individual letter sized sheets. Comparable polymer materials, such as PET [157], are routinely incorporated into roll-to-roll processes. Conductive paint deposition also requires scaling to match the throughput of the transparent substrate. This is achieved using a roll-to-roll spray deposition method [158]. A roll-to-roll dry film photoresist deposition and exposure stage similar to [159] is employed to deposit and pattern the photoresist. Roll-to-roll electrodeposition [160] follows. After applying a methanol spray (similar to the airbrush configuration) to strip the remaining photoresist, liquid PDMS is applied in a fashion similar to other roll-to-roll processes using liquid polymers [161]. Finally, a scaled lamp provides the IR radiation for transfer [162], while a separation tool removes the metal-PDMS layer from the substrate. A complete roll-to-roll adaptation of the newly developed process is not explored further in this thesis. However, each of the components in the current process are designed such that similar roll-to-roll adaptations have been previously demonstrated.

3.5. Remaining Challenges

The remaining challenges described in Section 3.1 that have yet to be addressed include metal-PDMS adhesion, electrical and mechanical performance optimization, and multilayer device fabrication. These challenges, unlike those discussed in this chapter, require a significant amount of characterization data. As such, these challenges are treated with an appropriate level of detail in further chapters. Chapter 4 demonstrates the exceptional adhesion and electrical performance of the deposited metal layers; Chapter 5 explores metal geometries that are optimized for stretchability (mechanical performance); and, Chapter 6 provides a detailed description and demonstration of an aligned, multi-layer device via a high-current electromagnetic actuator. It is also important to note that the frequency response of the metal layer is not explored in this thesis. However, we briefly discuss the frequency response of Peano-based designs in the introduction of Chapter 5 (before Section 5.1), and propose that a wearable device with integrated wireless components be fabricated in future work in Chapter 7.

Chapter 4.

Process Characterization

To complement the analysis in Chapter 3, this chapter provides a detailed characterization of the physical properties of the deposited layer. These physical properties are metal layer thickness, resistivity, and surface roughness. In addition to physical properties, the minimum feature size and metal-PDMS adhesion strength are also studied, and an analysis of film reliability and other surface features is provided through scanning electron microscope (SEM) imaging. Reliability in this case is measured by the presence of defects or holes in the metallization layer. This chapter is dedicated solely to experimental results and analysis. Further discussion, conclusions, and future work relating to the data collected in this chapter is presented in Chapter 7 and Chapter 8.

This chapter begins with a description the experimental procedures in Section 4.1, while Section 4.2 contains the results and analysis of the experimental data. The samples used to characterize the physical properties of the metal layer are fabricated and tested after several periods of electrodeposition. An analysis of the metal layer properties versus deposition time is presented in Section 4.2.2. Five individual samples are fabricated and tested for each measurement to provide a statistical assessment of the measured values. Each set of experiments is performed once on a tinned seed layer, and once on an untinned seed layer. A comparison of these two sets of data provides insight into the effectiveness of using a tinning layer on the quality of the metal layer.

Characterization of additional mechanical properties relevant to applications in stretchable electronics, such as stretchability, are presented in Chapter 5. Chapter 5 also demonstrates the application of this process to wearable fabrics. A multi-layer

device demonstrating exceptional conductance of the metal layers is also presented separately in Chapter 6.

4.1. Experimental Procedure

Square films measuring 1.5 cm by 1.5 cm are fabricated to characterize thickness, surface roughness, resistivity and reliability of the copper and seed layers. The experiments measuring thickness and surface roughness are described in Section 4.1.1, while the experiments measuring resistivity and reliability are described in Section 4.1.2 and Section 4.1.3, respectively. A set of five film samples is fabricated and tested for each measurement, and the statistical mean and standard error of the mean are calculated and discussed. This characterization is repeated for independent sets of samples after electrodeposition periods of one hour, two hours, three hours, and four hours. In addition, an initial set of seed layer experiments is performed to determine the effect of mechanical polishing. In the initial seed layer experiments, three square samples are fabricated and measured for thickness, surface roughness, and resistivity before and after polishing.

Experiments relating to the characterization of the minimum feature size and adhesion strength of the copper-PDMS interface are presented in Section 4.1.4 and Section 4.1.5, respectively. The minimum feature size is characterized by fabricating ten samples of various test structures and identifying the minimum size that can be reliably fabricated before failure. The adhesion strength is measured by peeling an embedded test structure from the PDMS substrate while connected to a linear stage and load sensor test apparatus. The linear stage and load sensor test apparatus is described in greater detail in Section 5.1.2.

4.1.1. Thickness and Surface Profile

Thickness and surface profile measurements are acquired using a KLA-Tencor series benchtop stylus profilometer and its accompanying software package. The profilometer/software package provides measurement data for thickness (step height), T, the arithmetic mean of surface roughness amplitudes, R_a, and the arithmetic mean of

surface waviness amplitudes, W_a. These values are all dependent on the Gaussian filter cut-off length and scan length, which in this case are 80 µm and 3000 µm, respectively. An in-depth discussion of the meaning of these measurements, and surface metrology in general, can be found in existing studies [163] [164]. Briefly, the filter cut-off value is similar to a high pass filter of the original surface measurement profile. Applying the filter produces a high frequency roughness profile and low frequency waviness profile of the surface.

4.1.2. Resistivity

Resistivity values are calculated by applying a constant current across one length of a square test sample and measuring the voltage drop across the opposite edge. This method (the Van der Pauw method) is described in greater detail Section 2.2.1.

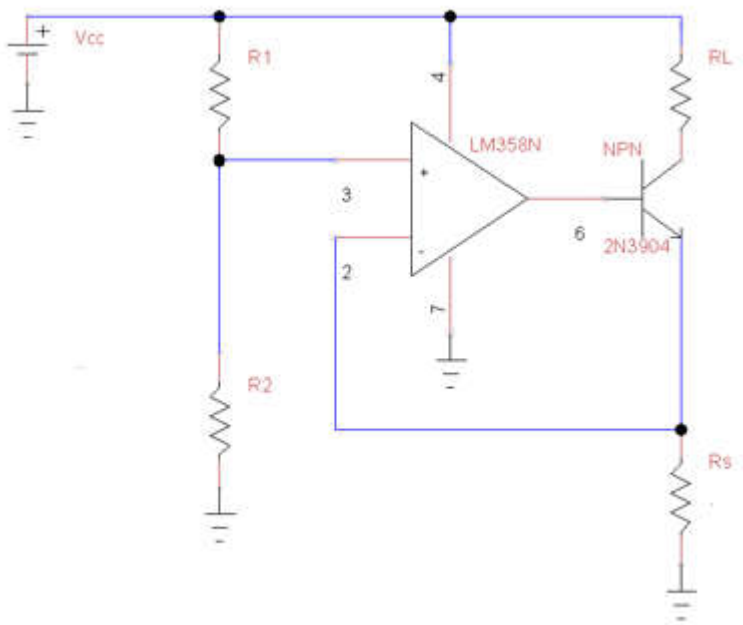


Figure 20. Constant current source (across RL) used in the resistivity experiments discussed in this chapter.

The constant current source required by the Van der Pauw method is provided by the test circuit shown in Figure 20. This common current source circuit uses a voltage divider and a LM358N operational amplifier to provide a constant voltage across the resistor *RS*. This constant voltage results in a constant current across *RS,* which is

provided by the 2N3904 npn transistor. Ignoring the relatively small transistor base current, the current across *RS* is matched across the load, *RL*. The benefit of this configuration is that the load current (transistor collector current) is constant across a relatively wide range of load resistances, *RL*. The npn transistor is required to produce a 100 mA collector current, as the LM358N maximum output current rating is limited to 40 mA. A 100 mA collector current allows for sufficiently large voltages to be measured, while remaining safely below the 200 mA maximum current rating of the npn transistor. In this experiment, a single constant current value is used. However, experiments may be repeated with various current values to achieve a more robust measurement.

The nominal values of the resistors used in these experiments are 12 kΩ for *R1*, 1.5 kΩ for *R2*, and 12 Ω for *RS*. The value for the current across the load, *RL,* is calculated using Equation 16:

$$I_{RL} = \frac{V_2}{RS} = V_{cc}\frac{R_2}{R_2 + R_1}\frac{1}{RS} \tag{16}$$

The calculated nominal current with an applied voltage (V_{CC}) of 10 V is approximately 93 mA, while the actual current is measured to be 89 mA using a handheld digital multimeter (DMM).

Note that the resistivity measurement method in Section 2.2.1 describes a single measurement. In this experiment, the measurement is repeated after rotating the sample and reversing electrode polarities to minimize systemic error, for a total of four measurements per sample. From these values, the resistivity of the sample is calculated according to Equation 17:

$$\rho = \frac{\pi T}{\ln 2}\left(\frac{V_{s\_1}/I_{app\_1} + \ldots + V_{s\_n}/I_{app\_n}}{n}\right) \tag{17}$$

where I_{app} is the applied current, V_s is the measured voltage, T is the measured film thickness, n is the number of samples, and ρ is the resistivity. Equation 17 follows

directly from Equation 11 (Section 2.2.1) and is used to calculate the mean of *n* measurements rather than a single measurement.

4.1.3. Surface Quality and Reliability

The surfaces of various samples are imaged to quantify defects and identify other notable surface qualities. These images are collected at several resolutions using an Explorer model SEM manufactured by FEI/Aspex. The ImageJ software package (National Institutes of Health, public domain) is used to quantify and analyze surface defects/holes of various sizes for each sample. Other qualities, such as grain size and distribution, are also discussed.

4.1.4. Minimum Feature Size

Various test structures are used characterize the minimum feature size of this process. A total of ten samples per structure are fabricated and assessed for reliability. This is not statistically rigorous, but if all ten samples of a feature are successful at a given resolution, then it is reasonable to expect that this feature is within the resolution limits of the process.

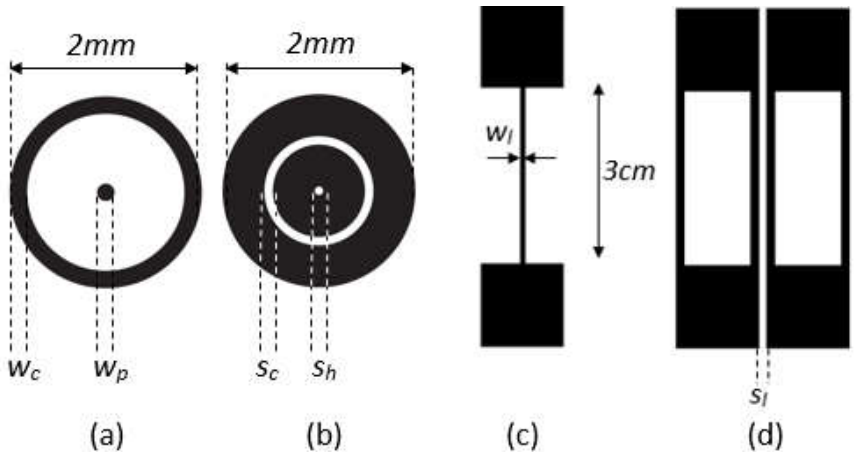


Figure 21. Patterns used to determine the minimum feature size of the fabrication process. These patterns test (a) minimum trace width for circular features (including pegs), (b) minimum trace spacing for circular features (including holes), (c) minimum trace width for linear features, and (d) minimum trace spacing for linear features [28].

The test structures in Figure 21 are used to characterize the resolution limits of the process. The types of features shown in Figure 21 are (a) w_c, the minimum trace width for circular features; (b) w_p, the minimum diameter of pegs; (c) w_l, the minimum trace width for linear features; (d) s_c, the minimum trace spacing for circular features; (e) s_h, the minimum diameter of holes; and (f), s_l, the minimum trace spacing pattern for linear features. The linear features are 3 cm long (not including contact pads) and the circular features are a total of 2 mm in diameter. All features are fabricated and tested a total of ten times for resolutions of 25 µm, 50 µm, 75 µm, 100 µm, 150 µm, and 200 µm. The number of successful features at a given resolution is used to quantify the resolution limits of the process. A 'successful' feature is identified if it is able to conduct electricity (i.e. it is not an open circuit from end to end) for linear features testing trace width. For linear features testing trace spacing, the additional constraint is that the trace remains in open circuit contact with its neighboring trace. Conductivity tests for linear features are performed using a handheld DMM, with conductive copper tape providing electrical contact to the contact pads. Open and closed circuit tests cannot easily be applied to the circular features, pegs, or holes in Figure 21(a) and (b) because of their relative scale and lack of contact pads. Therefore, these are analyzed visually under a microscope and deemed to be successful if there are apparently no unintended open circuits, shorts, missing pegs, or closed holes.

4.1.5. Adhesion

Precise and accurate measurements of adhesion strength can be difficult, and there is no widely accepted method to measure the interfacial atomic bond strength between PDMS and deposited metal films. However, a simple tape test (Scotch™) is generally used to qualitatively assess the adhesion of a deposited film [165].

To perform the test, tape is pressed firmly on the deposited layer, and pulled back slowly at an angle of approximately 180°. After the test, the film is either fully lifted, partially lifted, or remains fully adhered to the PDMS [165]. Tape tests performed for the proposed process show that the deposited layers consistently remain fully adhered to the PDMS. Although this test confirms that the copper films meet a qualitative benchmark, the results lack quantitative data.

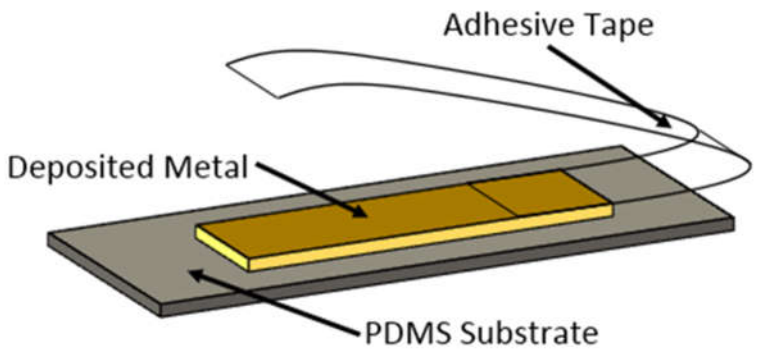


Figure 22. Schematic illustration of the Scotch™ tape adhesion test.

A schematic of the test is illustrated in Figure 22. The tape test is ineffective in this case for two reasons. First, thick films have a relatively large degree of structural integrity compared to thin films, and can sustain large tensile and/or shear forces before failure. Therefore, in the case of thick films, partial delamination is less likely to occur. Second, the metal films in this process are embedded flush with the PDMS surface. This results in undesired adhesion between the tape and the PDMS layer, and it is difficult to arrange a test such that only the metal layer is in contact with the tape.

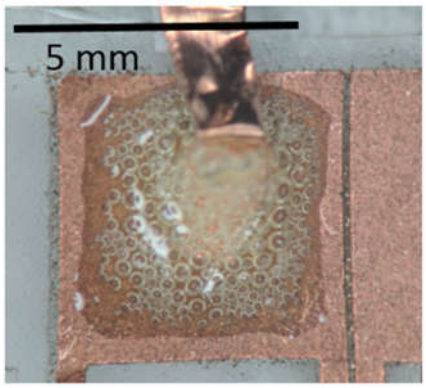


Figure 23. High-strength Gorilla Glue applied to 5 mm by 5 mm copper pads for adhesion tests.

To obtain quantitative adhesion strength data, a modified tape test is performed that utilizes a stronger adhesive force than a metal-tape interface. In this experiment, a linear stage (Zaber Technologies T-LS28-SMV) provides the tensile force, while a load sensor (FUTEK LRF400, 5lb) measures the pulling force applied by the linear stage. Copper tape (3M™) approximately 1 mm wide is affixed to deposited copper pads

(squares measuring 5 mm by 5 mm) using a layer of high-strength adhesive (Gorilla Glue™). The adhesive is applied to the pad such that coverage of the copper surface is maximized while contact between the adhesive and PDMS is prevented, as shown in Figure 23.

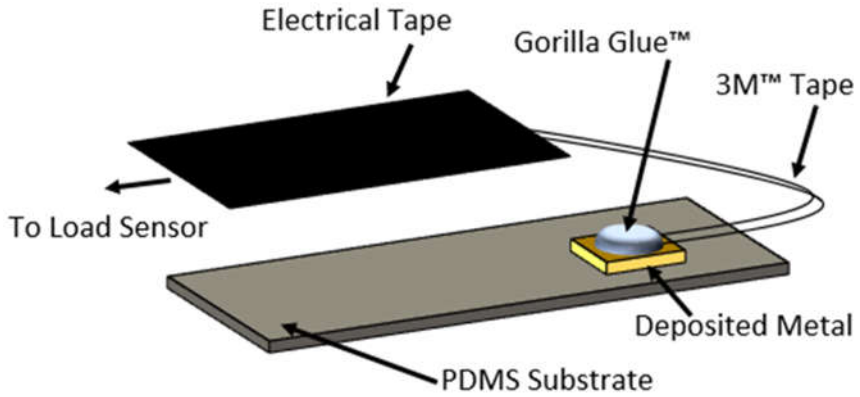


Figure 24. Modified tape test using gorilla glue and square contact pads.

The copper tape is attached to the load cell assembly using ordinary electrical tape. The electrical tape has an elastic quality that allows tensile forces to increase slowly before complete delamination of the contact pad from the PDMS. The linear stage operates a speed of one millimetre per second, and the test is performed for three different samples. A schematic illustration of the test setup is shown in Figure 24.

The adhesion test is performed twice, using two sets of samples with three samples in each set. Both sets of samples are tested with a linear stage speed of one millimeter per second. However, the first set of samples are tested using a 10 cm long strip of electrical tape, while the second set of samples are testing using a 5 cm long strip of electrical tape. The elasticity of the tape, extended over a shorter length in the second set of tests, is expected to increase the rate of tension increase at the bond site. This is expected to allow a comparison of the adhesion strength between the two tests under varying rates of applied stress.

4.2. Results and Analysis

This section presents the results corresponding to the experimental procedure outlined in Section 4.1. Each subsection also contains an analysis and discussion of these results. This section begins with a characterization of the physical properties of the conductive paint seed layer and the deposited copper layer. This is followed with a characterization and analysis of the metal layer defect distribution, minimum feature size, and adhesion strength. Note that in all SEM images, the scale among sub-images within a single figure is consistent unless otherwise stated.

4.2.1. Sacrificial Seed Layer

As discussed in Section 3.3.1, the seed layer has a strong influence on the growth and quality of the metallization layer. Therefore, a characterization of thickness, resistivity, surface roughness, reliability, and surface quality of the seed layer is provided in this section. A minimum feature size characterization is not provided for the seed layer, as the seed layer is deposited as a uniform layer and is never patterned.

Table 5. A comparison of three seed layer samples measured before and after mechanical polishing.

Copper Seed	Thickness (μm)	Surface Roughness (μm)	Resistivity (μΩ-cm)
Polished	50-70	5-10	326 ± 28
Unpolished	80-100	20-25	282 ± 18

Table 6. Measured physical properties of conductive copper paint seed layer. These measurements correspond to five polished seed layer samples [28].

	Mean	Standard Deviation	Standard Error
Thickness (T) (μm)	63.2	7.80	3.49
Resistivity (ρ) (μΩ-cm)	376	66.8	29.9
Roughness (R_a) (μm)	0.293	0.0460	0.0206
Waviness (W_a) (μm)	0.794	0.190	0.0850

The results of the initial seed layer experiments used to compare polished to unpolished seed layers are shown in Table 5. The standard error of the mean is shown for the resistivity measurements only. These measurements show that mechanical polishing effectively reduces the surface roughness of the seed layer without significantly increasing the resistivity. In an effort to achieve a consistent surface profile, polished seeds are used in all further experiments in this thesis.

After the initial measurements of the seed layer, the full seed layer characterization is performed using five polished seed layer samples. The measured values for the seed layer thickness, resistivity, and surface profile metrics (R_a and W_a) are given in Table 6. A full discussion of the results in Table 6 is more relevant in the context of a comparison to the metallization layer, and is provided in Section 4.2.2. However, it is interesting to note that the resistivity of this composite paint is quite low compared to other reported conductive composites. For example, other studies have reported a resistance of 1000 μΩ-cm for silver 50% loaded by weight in epoxy resin; 2000×10^3 μΩ-cm for carbon black 30% loaded by weight in polyethylene; 1000×10^6 μΩ-cm for iron 50% loaded by weight in styrene/acrylonitrile [142]; 2000 μΩ-cm for a graphite-carbon black mixture in a modified poly sulfide epoxy resin [143]; and, 175 μΩ-cm for a highly conductive carbon-nanotube/silver-flake hybrid composite in polyvinylidenefluoride copolymer [144].

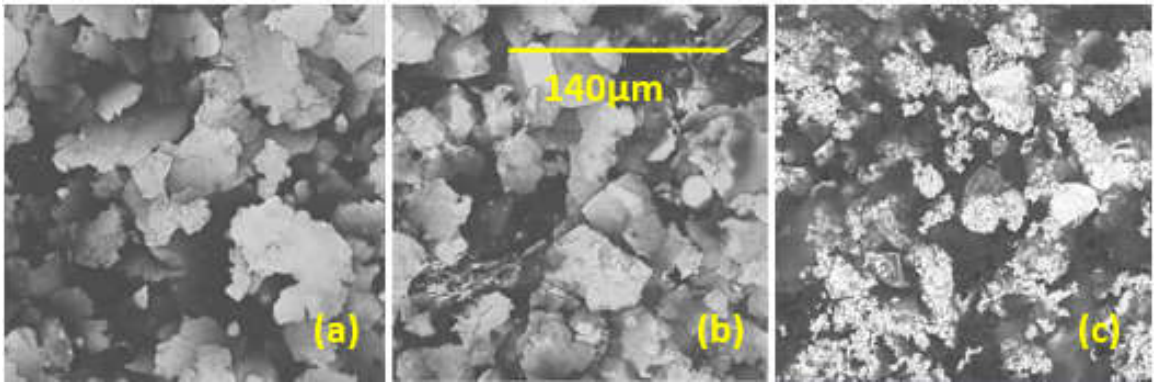


Figure 25. SEM images of the conductive copper paint (a) before polishing, (b) after polishing, and (c) after tinning [28].

SEM images of the seed layer before polishing, after polishing, and after tinning are shown in in Figure 25(a), (b) and (c), respectively. In Figure 25(a), it appears as

though the largest copper flakes are 50-75 μm in diameter. A visual comparison of the remaining images appears to show a slight decrease in flake size after polishing in Figure 25(b), and distinct tin crystal formation on the copper flakes after tinning in Figure 25(c). Elemental analysis with the SEM explorer confirms the observation of tin crystals, showing an elemental composition of 80% Cu and 10.2% Ag (plus trace elements) when centered over a copper flake before tinning, compared to 49.5% Sn, 35.5% Cu, and 9.9% Ag (plus trace elements) when centered over a tin crystallized copper flake after tinning. A detailed characterization of grain size and distribution in the seed layer before polishing, after polishing, and after tinning is intended for future work. However, a rough visual estimate is provided.

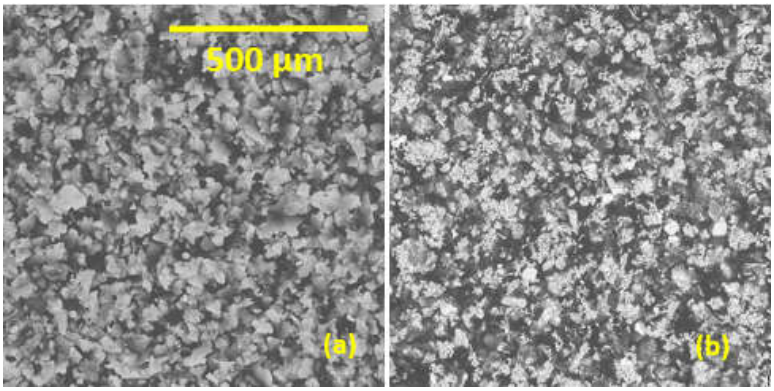


Figure 26. Medium-field SEM images of an (a) untinned and (b) tinned seed layer. These images are used to qualitatively assess the size and distribution of the copper flakes.

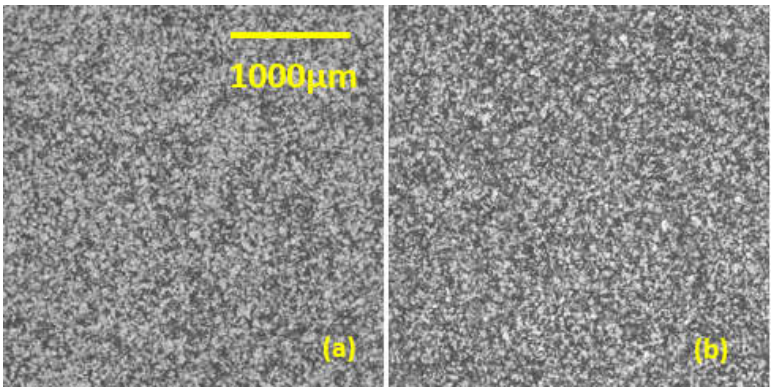


Figure 27. Large-field SEM images of an (a) untinned and (b) tinned seed layer, used to qualitatively assess the size and distribution of the copper flakes.

Additional SEM images are used to qualitatively assess the copper flake diameter and distribution. These observations are made using medium-field and wide-field SEM images comparing unpolished, untinned seed layers to polished, tinned seed layers. These images are shown in Figure 26 and Figure 27, respectively. Again, it appears as though the larger copper flakes are in the range of 50-75 μm in diameter before polishing, with a smaller number of flakes appearing in range of 20-30 μm in diameter. As mentioned previously, it appears as though the copper flakes have a slightly smaller diameter after polishing, though flake size is difficult to assess qualitatively at these scales. It also appears as though roughly half of the surface is comprised of exposed copper flakes while the other half is comprised of the non-conductive paint medium. It is assumed that both the size and distribution of the copper flakes will heavily influence the quality of metallization layer and minimum resolution of deposited features.

4.2.2. Metal Deposition Layer

The metal layer is deposited via electrodeposition in an acid copper bath as described in Section 3.2.4. The 1.5 cm by 1.5 cm square samples are deposited without masking at 10 mA/cm^2 for one to four hours at increments of one hour. As mentioned in Section 4.1, five samples at each deposition time are measured for statistical purposes, for both tinned and untinned seed layers. These samples are characterized in terms of thickness, surface roughness, surface waviness, and resistivity versus deposition time in a similar fashion to the seed layer. Unlike the seed layer, film reliability, surface quality, and the minimum feature size of the deposited metal layer are also analyzed.

Table 7. Mean thickness and standard error versus deposition time for metal layers on tinned and untinned seeds [28].

Deposition time (h)	Untinned Seed		Tinned Seed	
	Thickness (μm)	Standard Error (μm)	Thickness (μm)	Standard Error (μm)
1	19.6	0.5	20.7	1.3
2	35.5	2.2	36.4	2.4
3	53.7	3.8	49.9	2.7
4	69.9	3.9	62.6	5.0

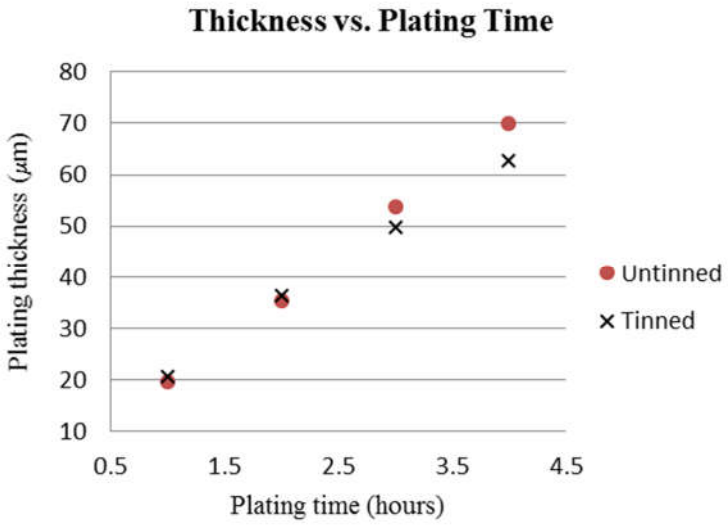


Figure 28. Copper thickness as a function of deposition time for tinned and untinned seed layers [28].

The results for copper thickness versus deposition time are shown in Figure 28. Standard error bars are not shown for the sake of clarity within the chart area. The mean thickness and standard error of the mean for these measurements are given in Table 7. The untinned layer is deposited at a rate of approximately 17.5 μm per hour, while the tinned layer deposits slower, closer to 15 μm per hour. The mean and standard error are calculated based on the measurements of five different samples for each deposition time. Since both layers are deposited using the same current density, it may be that the tinned layer results in a denser copper metallization layer. This discrepancy in thickness is not fully understood, but may be due to an increased variance in film surface conductivity after tinning. However, these measurements are subject to a degree of error. Estimating the thickness of a rough surface is inherently prone to error, and step height measurements may be unintentionally collected at localized peaks or valleys on the sample surface. The relationship between film thickness and time is investigated further using the data collected for resistivity of the metallization layer.

Table 8. Mean resistivity and standard error versus deposition time for metal layers on tinned and untinned seeds [28].

Deposition Time (h)	Untinned Seed		Tinned Seed	
	Resistivity (μΩ-cm)	Standard Error (μΩ-cm)	Resistivity (μΩ-cm)	Standard Error (μΩ-cm)
1	9.96	1.11	8.47	1.77
2	3.11	0.24	3.29	0.38
3	3.22	0.19	3.09	0.18
4	2.76	0.09	2.53	0.11

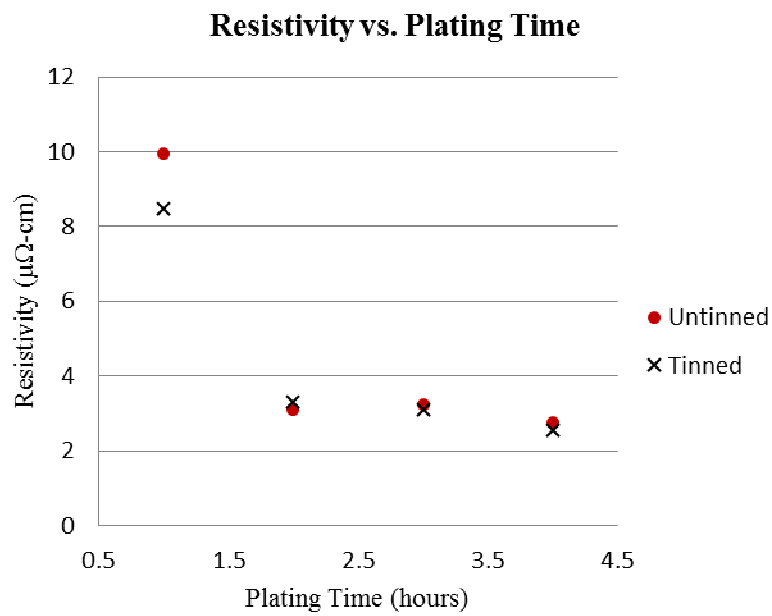


Figure 29. Deposited copper resistivity as a function of deposition time for tinned and untinned seed layers [28].

The resistivity of the metallization layer as a function of deposition time is shown in Figure 29. Once again, the standard error bars are not shown for the purpose of clarity, and are instead given in Table 8. The standard error appears relatively consistent between the tinned and untinned layers. Both sets of data show that the electrical resistivity is relatively high after one hour, before sharply decreasing at two hours and remaining relatively steady thereafter. From these measurements, it appears that for short deposition times, the copper layer is not yet uniformly deposited and likely suffers

from large discontinuities. It is also possible that the surface morphology of the deposited layer changes with time and influences film resistivity. Although the surface morphology is characterized in terms of surface roughness and surface waviness, the relationship to resistivity is not explored further.

The speculation that the tinned seed layer produces a denser, more conductive deposited copper layer is once again suggested by Figure 29, but cannot be confirmed with confidence due to uncertainty in the measurements. After four hours of deposition, the tinned and untinned samples have a resistivity of 2.53 μΩ–cm and 2.76 μΩ–cm, respectively. These values are approximately 10% larger than other reported values for electroplated copper [128] [166], and significantly larger than the resistivity of bulk copper, which is 1.68 μΩ–cm [167]. However, compared to the resistivity values mentioned in Section 4.2.1, the deposited layer is approximately 100 times more conductive than even the most conductive composites.

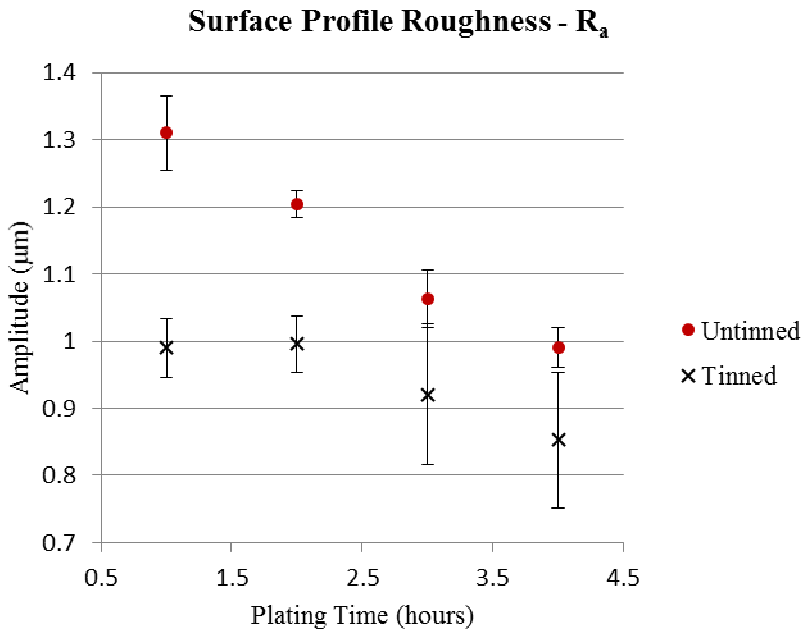


Figure 30. Deposited copper surface roughness as a function of deposition time [28].

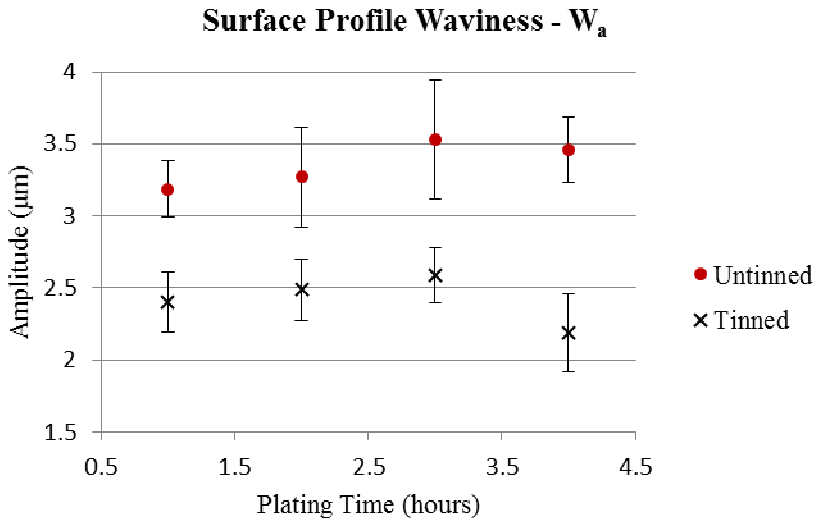


Figure 31. Deposited copper surface waviness as a function of deposition time [28].

The surface roughness and waviness amplitudes of the metallization layer are shown in Figure 30 and Figure 31, respectively. The first observation is that tinned seed layers produce reduced roughness and waviness in the deposited copper layers compared untinned seed layers. The surface roughness decreases over time for both sets of data, while the surface waviness remains relatively more stable. Added together, the roughness and waviness profiles show that surface features have approximately 5 µm amplitudes, or are 10 µm from top to bottom. This approximation is confirmed by analyzing the raw profilometer output from the sample measurements. In other studies, a RMS surface roughness of 10 nm has been reported [128] compared to our RMS roughness measurements of approximately 1 µm after four hours. Others have reported super-conformal electrodeposition with 500 nm features [129]. Therefore, the deposited copper in this thesis appears to be 10-100 times rougher than the results in existing studies. For typical electronic applications, such as electrical interconnects, roughness is generally minimized. However, surface roughness can have a positive impact on polymer-metal adhesion [125], and one study is entirely dedicated to producing extremely rough copper surfaces [126]. Increased surface roughness may also be desired in applications such as electrochemical sensing [127]. Methods of controlling roughness, which is likely to be heavily dependent on the conductive seed layer morphology, is a potential avenue for future research.

Table 9. SEM images of the copper layer after one to four hours of deposition on an untinned seed. Table rows correspond to deposition time, while table columns correspond to image scale.

Scale: :

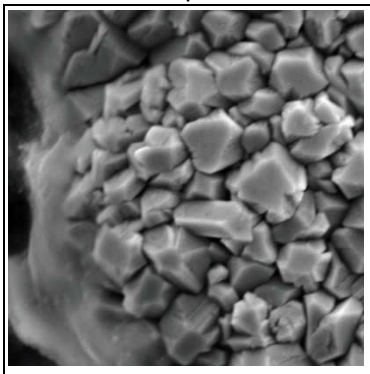
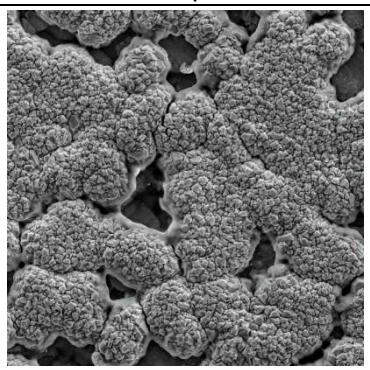
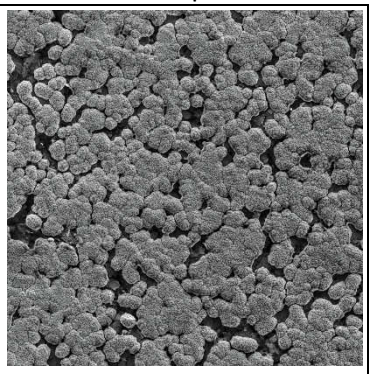
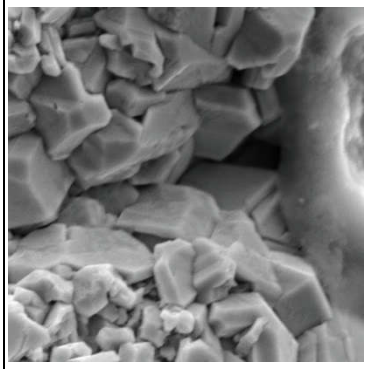
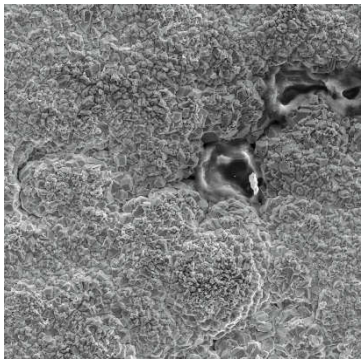
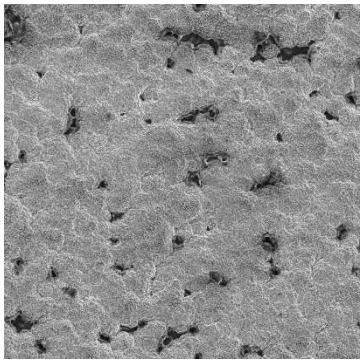
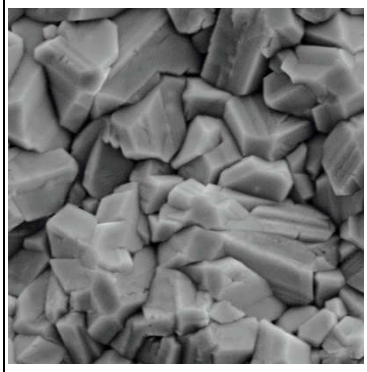
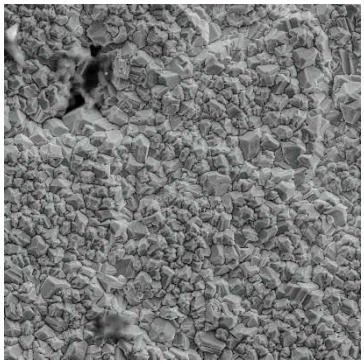
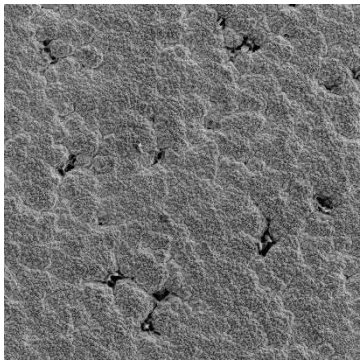
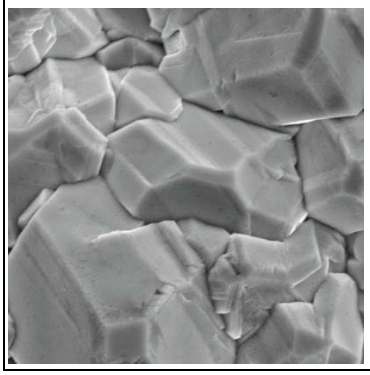
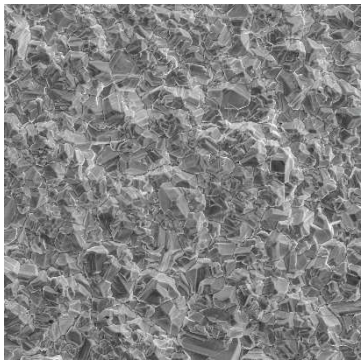
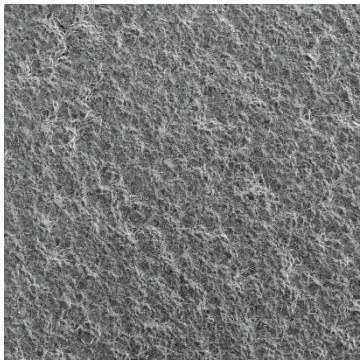
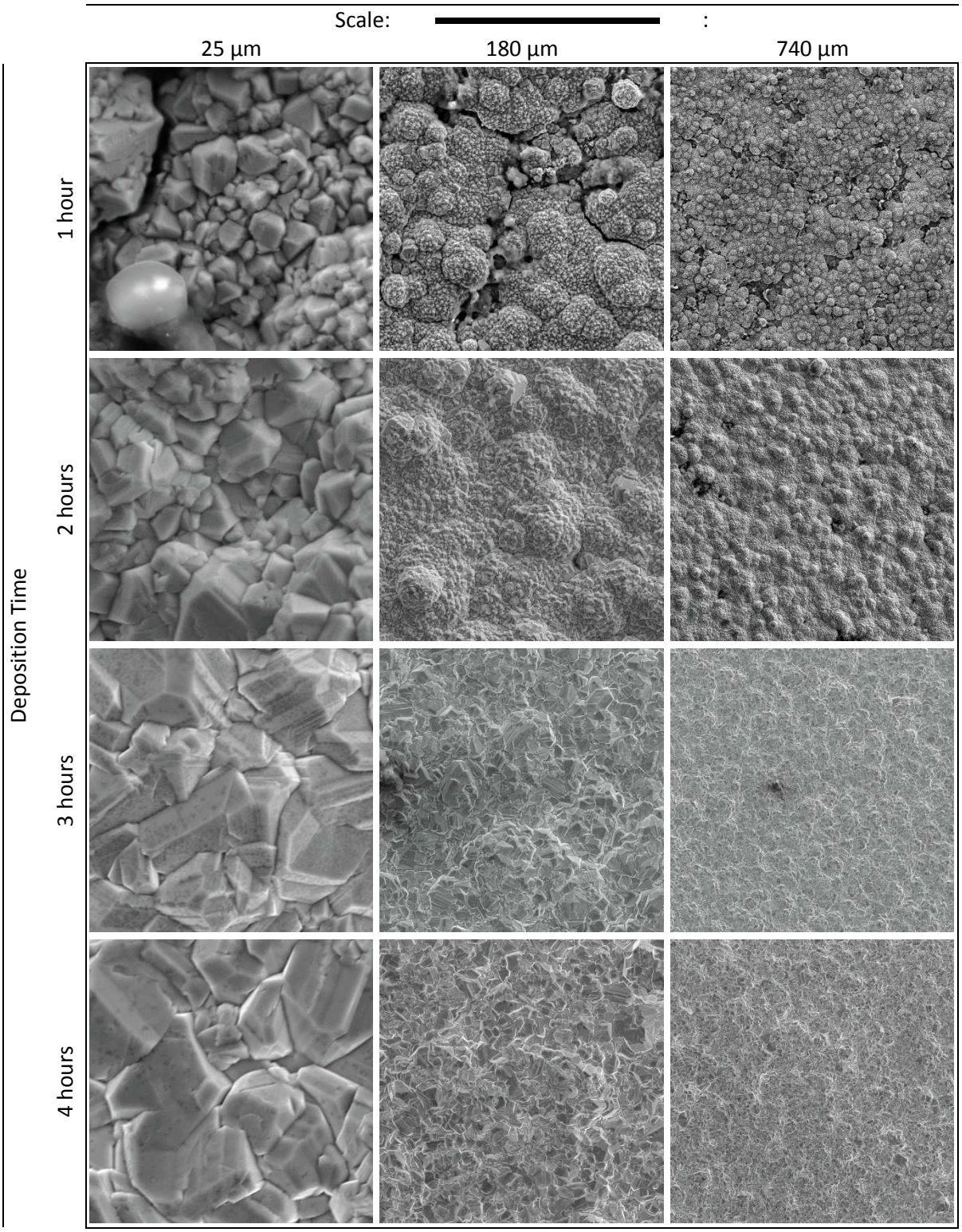
Deposition Time	25 µm	180 µm	740 µm
1 hour			
2 hours			
3 hours			
4 hours			

Table 10. SEM images of the copper layer after one to four hours of deposition on a tinned seed. Table rows correspond to deposition time, while table columns correspond to image scale.



SEM images of the metallization layer after one to four hours of deposition for both the untinned and tinned seed layers are shown in Table 9 and Table 10, respectively. Each row corresponds to a deposition time, from one hour of deposition shown in the top row of images up to four hours of deposition in the bottom row of images. Each column has an associated image resolution, with resolutions decreasing from left to right. After one hour of deposition, large discontinuities remain in the deposited layer on both seeds. This is predicted by the analysis of the resistivity trends in Figure 29. The discontinuities, or voids, slowly fill during deposition, until only sparse, discreet holes remain after four hours. The images after four hours of deposition appear very similar in both tables. Another common feature in both sets of images is that the deposited copper grain size increases from approximately 1 to 3 μm after one hour to 10 μm after four hours.

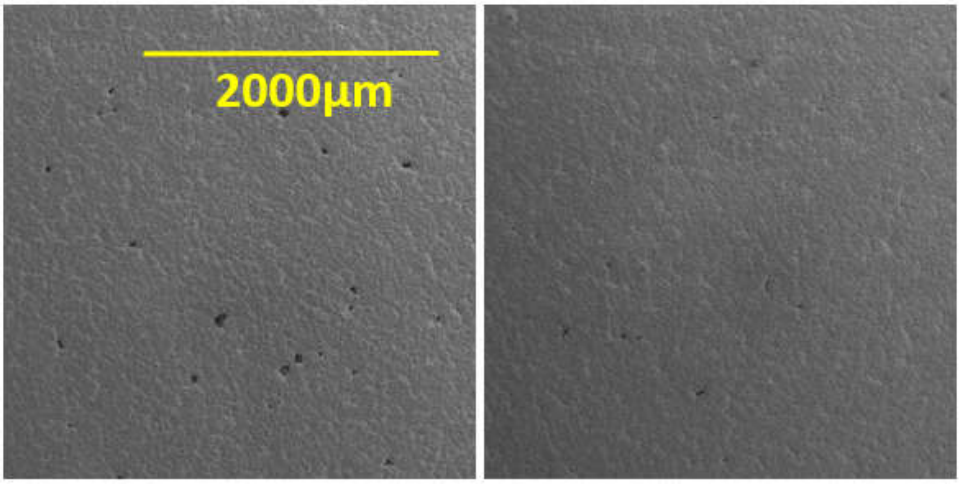


Figure 32. Low-resolution SEM images of deposited layers after four hours of deposition on an untinned seed (left) and a tinned seed (right) [28].

In comparing Table 9 to Table 10, it is apparent from the low-resolution images corresponding to the first three hours of deposition that the deposited layers on a tinned seed have relatively fewer voids. This is especially apparent after three hours of deposition, where the untinned seed appears less filled than the tinned seed. The tinned layers also exhibit surface nodules or localized peaks, particularly in the first two hours of deposition. Paired with the roughness and waviness data in Figure 30 and Figure 31, which indicates that the overall roughness and waviness both decrease on tinned seeds, it appears that localized nodules may have less of an effect on surface roughness than

voids. Given the scale and resolution of the images, the surface quality is moderately dependent on the image position on the sample and distribution of defects in the imaged area. However, by viewing a larger area at a lower resolution after four hours of deposition, the deposited layer appears more uniformly filled on the tinned seed layer, as shown in Figure 32.

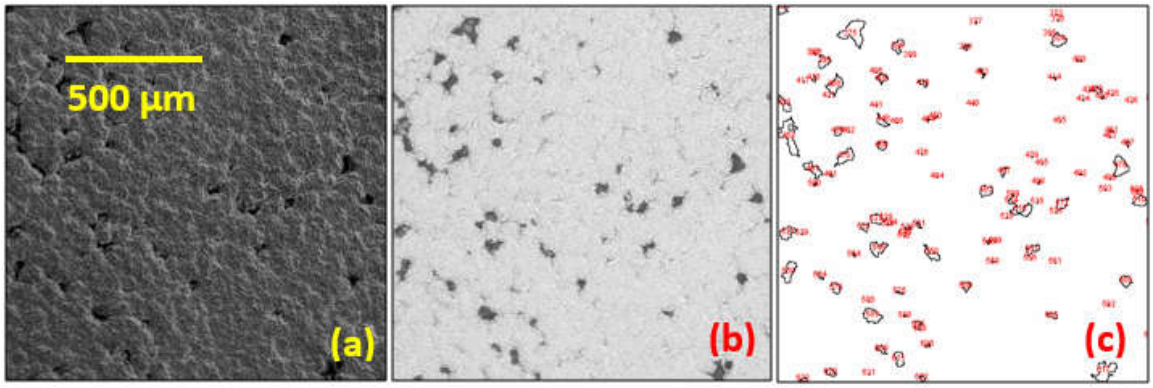


Figure 33. (a) SEM image after three hours of deposition on an untinned seed, (b) the corresponding BSED image, and (c) the defect-filtered image from ImageJ.

To analyze defects in the deposited layers, SEM images of the copper surface are collected with a field of view equal to 3.2 mm by 3.2 mm. For the analysis of these regions of interest (ROI), the SEM is operated in Backscatter Electron Detector (BSED) mode for maximum contrast between the deposited copper and the defects. ImageJ image analysis software is used with built-in particle analysis tools to quantify the defect size and distribution. Note that in contrast to the characterization of surface roughness and conductivity, the ROI data is collected from a single sample for each deposition time, rather than all five samples. This follows from the assumption that by imaging and analyzing a reasonably large area (in this case over 10 mm^2), a reliable estimate of defect distribution is obtained. As an example, an image of an untinned seed layer is shown after three hours of deposition in Figure 33(a), while the corresponding BSED image and ImageJ defect-filtered image are shown in (b) and (c), respectively.

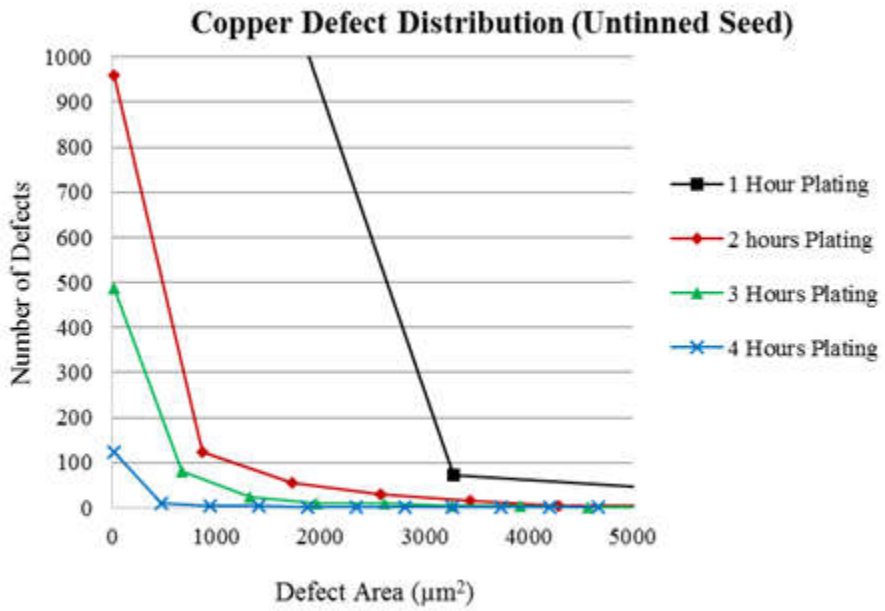


Figure 34. Defect distribution for deposited copper layers at various deposition times on an untinned seed [28].

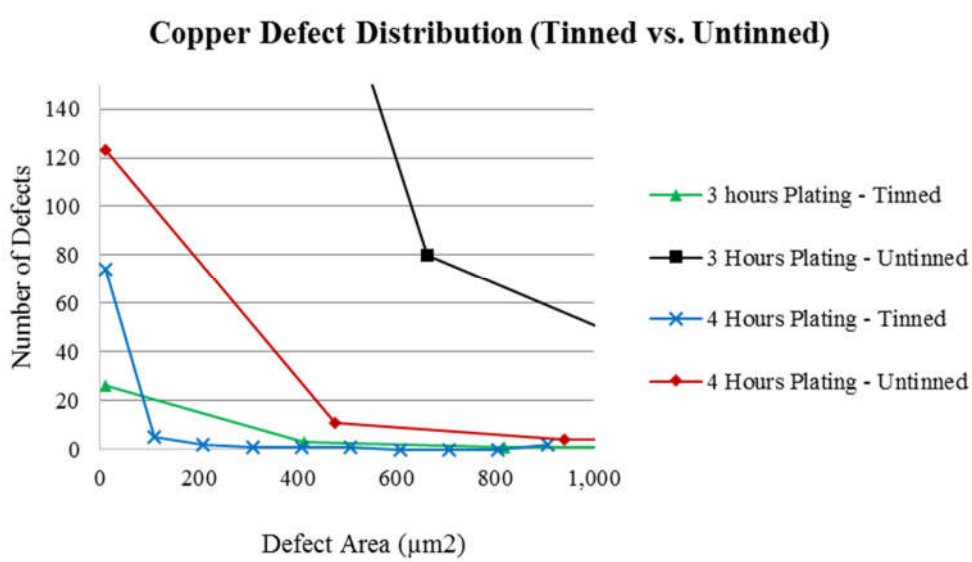


Figure 35. A comparison of the defect distribution for deposited copper layers at various deposition times, deposited on both tinned and untinned seed layers [28].

Figure 34 and Figure 35 show a subset of the data collected for the analysis of defect distribution in the deposited layer. Note that these figures focus on regions of

interest in the defect distribution data, and some of the collected data points are not shown. However, the general trend of each data series in Figure 34 and Figure 35 continues for the points that are (not shown) beyond the chart area. Each series corresponds to a deposition period from one to four hours. Figure 34 shows four data series corresponding to metal layers that are deposited on an untinned seed, while Figure 35 highlights a reduction of defects for layers deposited on a tinned seed versus an untinned seed. From Figure 34, the decrease in the number of defects can be seen both as the area of the defects increases and as the deposition time increases. Though not seen easily in the plot, there are over 100 defects less than 10 μm^2 and 11 defects less than 475 μm^2 after four hours of deposition. Though we do not identify a specific benchmark that we must satisfy in terms of reliability, we note that after four hours of deposition, there appears to be relatively few voids and discontinuities in the deposited layer (see images in Table 9 and Table 10). We also wish to avoid any loss of flexibility that may result from additional deposition beyond four hours. Therefore, we conclude that a deposition period of four hours is necessary and sufficient in the context of reliability and flexibility.

In Figure 35, the general trend that the number of defects decreases with both deposition time and defect area is maintained. It is interesting to note that for this subset of data, the number of defects corresponding to three hours of deposition on a tinned layer is less than the number defects corresponding to four hours of deposition on an untinned layer. Comparing the corresponding images in Table 9 and Table 10, this result is neither obvious nor surprising. The result illustrates the importance of the tinning layer in promoting the uniformity of the deposited layer. It is curious that the number of 10 μm^2 defects is actually higher in the tinned data comparing 4 hours of deposition to 3 hours of deposition. For defects of this scale, it is possible that inconsistencies in the image capture and filtering process could result in large variations in the number of defects detected, which could account for this discrepancy.

In general, the conclusion that tinning the seed layer produces a more reliable metal layer appears clear. Therefore, tinned seed layers are used exclusively to characterize the resolution limits and adhesion strength in Section 4.2.3 and Section 4.2.4, respectively. Also note that 4 hours of plating is performed (exclusively) in

these sections. The same conditions of four hours of plating on a tinned seed layer also apply to the remaining applications discussed in Chapter 5 and Chapter 6. It is assumed that plating for longer periods will reduce the number and size of surface defects in the plated layer.

4.2.3. Feature Size

Recall that the test structures in Figure 21 are used to characterize the resolution limits of the process. All features are fabricated and tested a total of ten times for resolutions of 25 µm, 50 µm, 75 µm, 100 µm, 150 µm, and 200 µm.

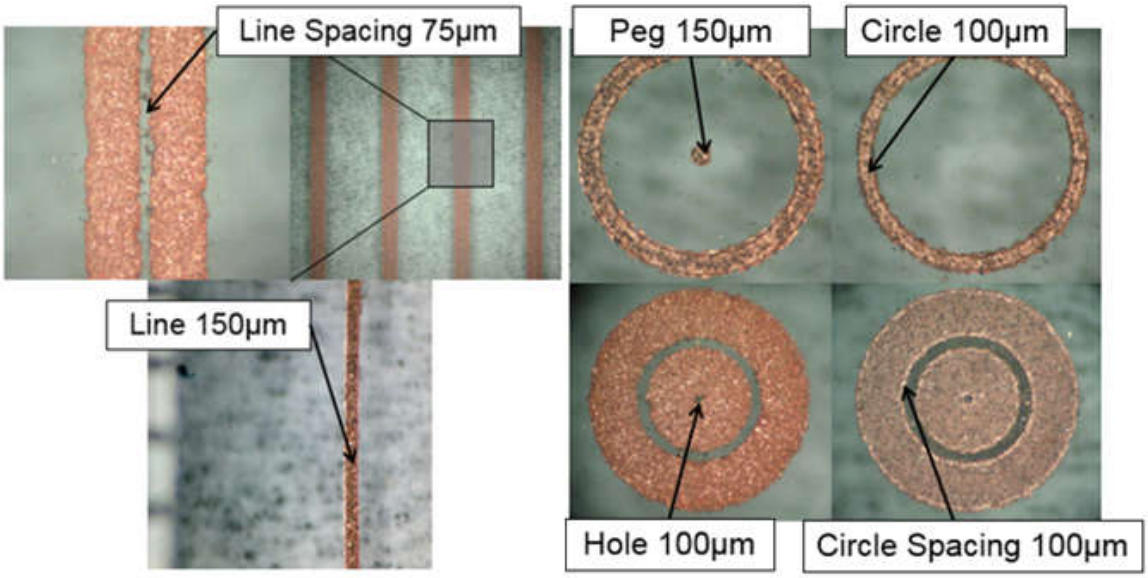


Figure 36. Various structures fabricated to test feature size limits, including 75 µm linear spacing features, a 150 µm linear resolution feature, a 150 µm peg feature, a 100 µm hole feature, a 100 µm circular spacing feature, and a 100 µm circular spacing feature [28].

Figure 36 shows the deposited copper geometries testing feature size fully fabricated and embedded in PDMS. Linear features and circular features testing both trace width and trace separation are shown together in Figure 36. Small, isolated features, such as pegs and holes tend to fail at a higher rate compared to larger features such as lines and circles. The deposited copper layer does not transfer completely free from the seed layer without a trace amount of seed layer residue. This is demonstrated

by the small reflective flakes distributed sparsely throughout the PDMS near the linear spacing and circular resolution features in Figure 36. For linear features, a failure due to short circuit contact between the spaced traces due to residual seed layer has not been recorded while collecting the data presented in this section, even with spacing as small as 50 µm. However, circular spacing features are not as successful, and short circuit contacts are observed for spaces as large as 75 µm.

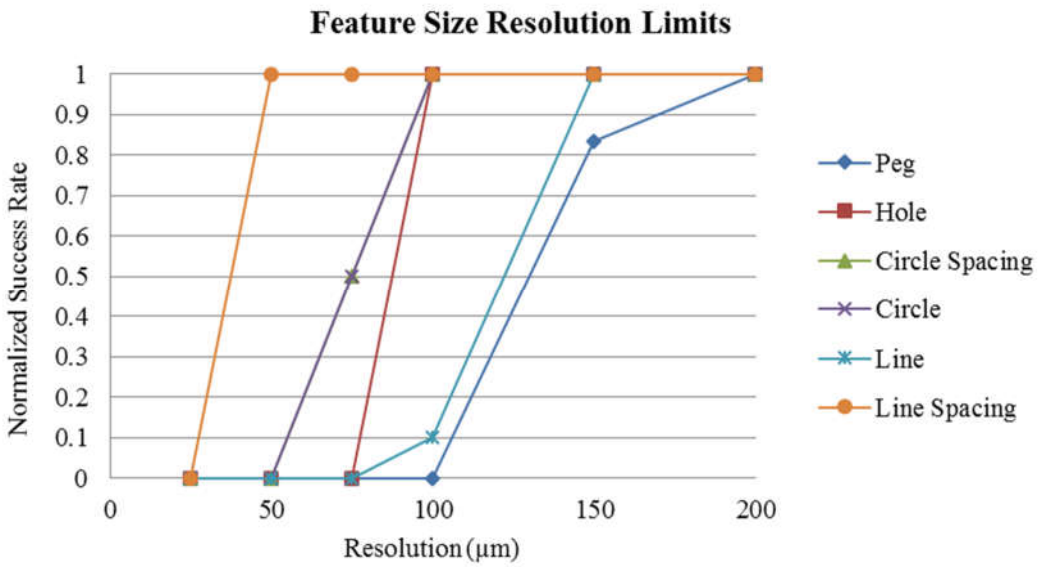


Figure 37. Summary of feature size resolution limits. The success rate based on ten fabricated samples of each test structure are shown [28].

The dimensions of the test structures must be noted, as they affect the overall result of the feature size resolution limit summary shown in Figure 37. For instance, the circular traces are shown to be 50% successful at 75 µm, while the linear traces are only marginally successful at 100 µm. Although the success rate is affected by feature geometry, it is more likely in this case that the discrepancy is due to the linear traces having a longer path length, and therefore are more likely to fail due to the distribution of metal layer defects discussed previously in this section. Overall, it the resolution limit for this process is approximately 100 µm. However, in the context of large-scale fabrication, it is reasonable to limit the minimum feature size to 150 µm or 200 µm. The relationship between a feature's resolution limit and its position on the substrate is to be explored in future work.

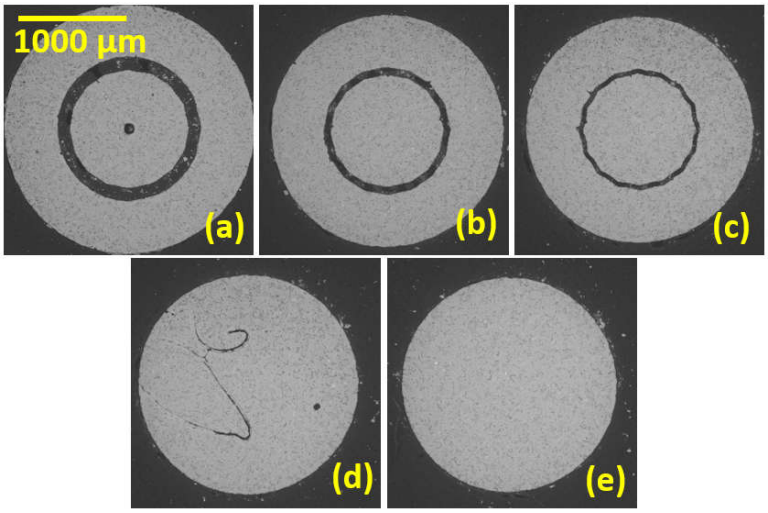


Figure 38. SEM images of the characterization structure testing circular spacing and holes. Image (a) corresponds to a feature size of 150 µm, (b) to 100 µm, (c) to 75 µm, (d) to 50 µm, and (e) to 25 µm.

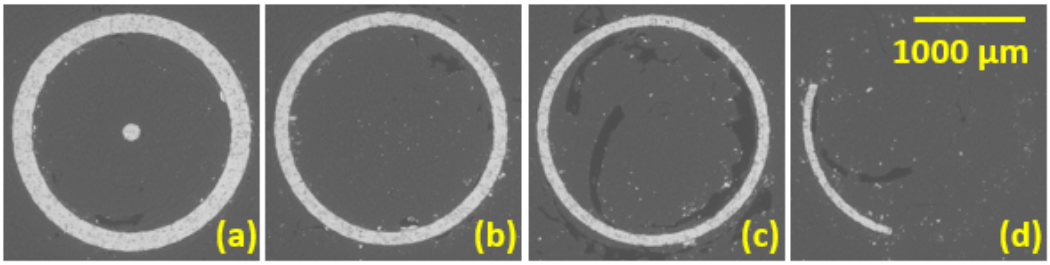


Figure 39. SEM images of the characterization structure testing circular trace width and pegs. Image (a) corresponds to a feature size of 200 µm, (b) to 150 µm, (c) to 100 µm, and (d) to 75 µm.

SEM images of the characterization structures testing circular photoresist spaces and circular copper traces are shown in Figure 38 and Figure 39, respectively. The 25 µm photoresist spaces in Figure 38(e) are not present at all. In Figure 38(d), the 50 µm space appears as a defect, as the photoresist is present but partially delaminated. Circular spaces 75 µm wide in Figure 38(c) are reliable, though not entirely smooth. At 100 µm, the circular spaces are quite smooth, and at 150 µm, holes are present as shown in Figure 38(b) and Figure 38(a), respectively. In Figure 39(d), copper traces are visible but unreliable at 75 µm. Traces are reliable at 100 µm and 150 µm in Figure 39(c) and Figure 39(b), respectively, while pegs become reliable at 200 µm in Figure 39(a). Some peg features are observed at 150 µm (see summary in Figure 37), but are not present for the structure imaged in Figure 39.

4.2.4. Adhesion

Two modified tape tests are performed to obtain quantitative adhesion strength data. The first test is conducted with a reduced strain rate relative to the second test so the relationship between adhesion strength and strain rate may be assessed.

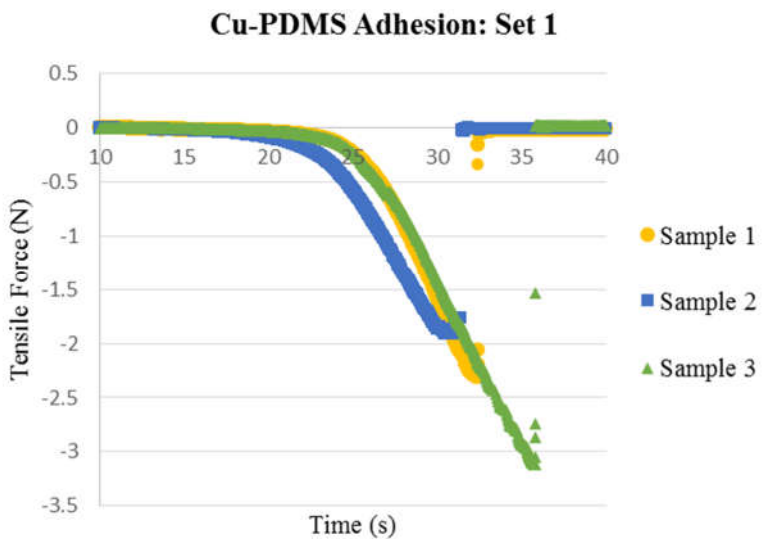


Figure 40. Modified tape test results for the first set of three samples.

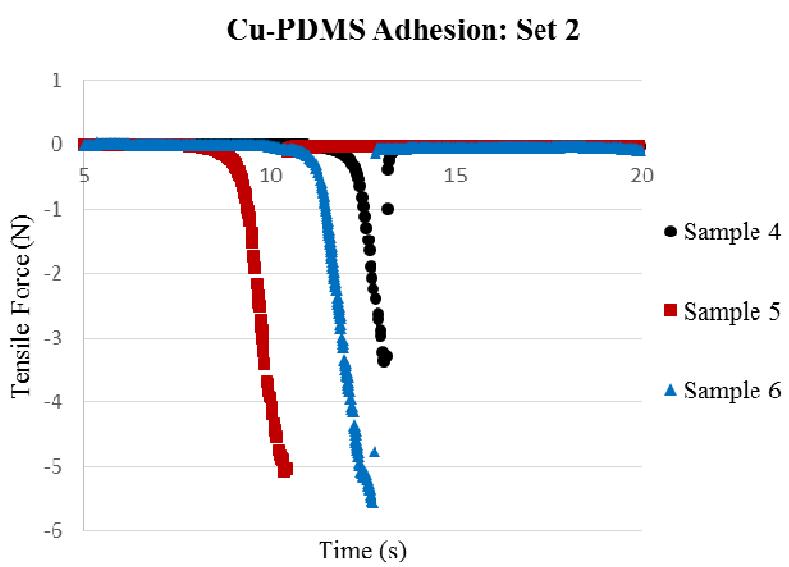


Figure 41. Modified tape test results for the second set of three samples.

The results for the first and second adhesion tests are shown in Figure 40 and Figure 41, respectively. For reference, these tests are described in greater detail Section 4.1.5. Note the time scale difference between the figures. The sharpness of the data peaks in Figure 41 is even more pronounced considering the mismatched scale. Two differences between the two sets of results are immediately apparent. First, in the first set of experiments, the tensile force before failure ranges from approximately 2 N to 3 N, while in the second set of experiments the force ranges from approximately 3 N to 5.5 N. Second, the tensile stress increases over a period of approximately 15 seconds in the first set of data, while the same increase occurs over a shorter period of approximately 2.5 seconds in the second set. This suggests that the absolute stress measured at failure is dependent on the rate of increase of the applied tensile force. A discrete integral of the applied force over the time of tensile stress increase shows a total impulse of approximately 4 N·s for Sample 4 in Figure 40 and 9 N·s for Sample 1 in Figure 41. Although Sample 1 experiences failure at a lower tensile stress, it also sustains almost double the total impulse. A characterization of the relationship between the applied stress versus impulse at failure requires further study, and is not presented in this thesis. It is however apparent that the adhesion force ranges between 2 N to 6 N for a 25 mm^2 bond pad under the conditions of these tests.

Existing studies that present similar measurements of adhesion are difficult to find, especially relating to impulse versus absolute tensile stress at failure. This is due to the fact that our experiments characterize the force required to remove a rigid, thick-film bonded pad. In contrast, adhesion tests typically involve the continuous peeling of a thin, deposited film [168] [169]. Therefore, the state of the bond in this is case is comparatively binary; the pad is initially fully adhered to the PDMS substrate until failure, at which point the pad delaminates almost immediately. With this caveat in mind, we compare our results to an existing study investigating the adhesion between PDMS and deposited copper films performed by Hoefnagels et al. [170]. In the study by Hoefnagels et al., a similar experiment is presented where an increasing force is applied before a maximum steady-state force is reached, leading to delamination [170]. The difference in our experiment is that a steady delaminating state is not achieved. Adhesion strength is quantified by the work of separation (WOS), which is equal to the force applied, F, divided by the width of the film trace, b [170]. Using the maximum force measured during

our experiments, 5.55 N for Sample 6, and a width of 5 mm, the calculated WOS in our experiments is 1.1 kN/m. This is quite close to the value of 1.3 kN/m calculated by Hoefnagels et al. [170].

The fact that the calculated WOS is slightly smaller in this thesis compared to the value reported in an existing study can potentially be justified though further analysis of the adhesion model proposed in the same existing study [170]. In the study by Hoefnagels et al., the main proposed source of adhesion between deposited copper and PDMS is the formation, elongation, and rupture of PDMS fibrils at the copper interface. During steady-state delamination, the rupture rate of fibrils at the delamination front is constant, and fibrils away from the delamination front remain intact. However, in our experiments, the increasing tensile forces leading up to complete delamination could lead to a portion of fibrils rupturing throughout the pad area before the point of failure. In this model, it is conceivable that a slower rate of tension increase (decreased strain rate) corresponding to a longer time period could result in more fibrils rupturing during the ramp to a given tensile force compared to faster rates of tension increase. This suggestion is supported by a comparison of Figure 40 and Figure 41, where the samples with a decreased strain rate experience a smaller force during delamination. This speculation cannot be further supported with the exiting data, though it is important to note that strain rate is known to affect mechanical properties of PDMS, such as Young's Modulus [171]. Future work is required for further analysis.

For copper films fabricated using our process, we hypothesize several factors that contribute to adhesion. First, we assume that the strength of adhesion is proportional to surface roughness, which is supported by existing studies [170]. The justification of this assumption is that increased surface roughness leads to increased surface area and increased fibril formation. In addition to increased surface roughness, embedded sidewalls also provide increased surface area, and are assumed to increase adhesion accordingly. Finally, we hypothesize that over-plating during electrodeposition could act as an anchor for the metal layer when deposited up-side-down in PDMS. The surface roughness of the metal layer is characterized earlier in this chapter, while the over-plating during electrodeposition and embedded sidewalls are explored in the following subsections.

Embedded Sidewalls

A linear spacing test structure (see Figure 21 for reference) is used to measure the portion of the deposited layer sidewalls that remains embedded after the transfer to PDMS. After one of the linear structures in a pair is removed, a profilometer measurement is acquired across a path that traverses both the remaining and the removed structures.

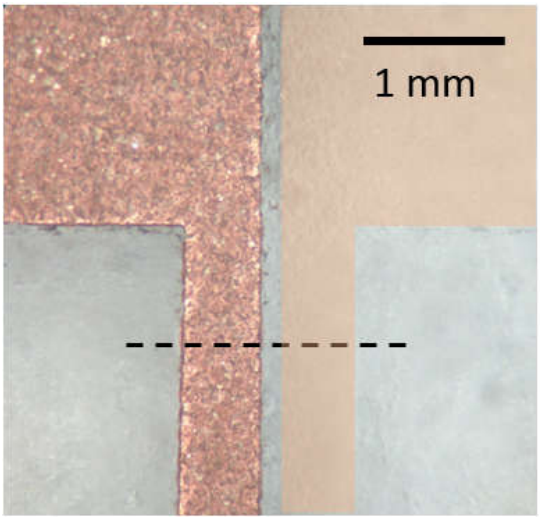


Figure 42. Structure used to measure embedded sidewalls with a profilometer. The dashed line defines the profilometer path.

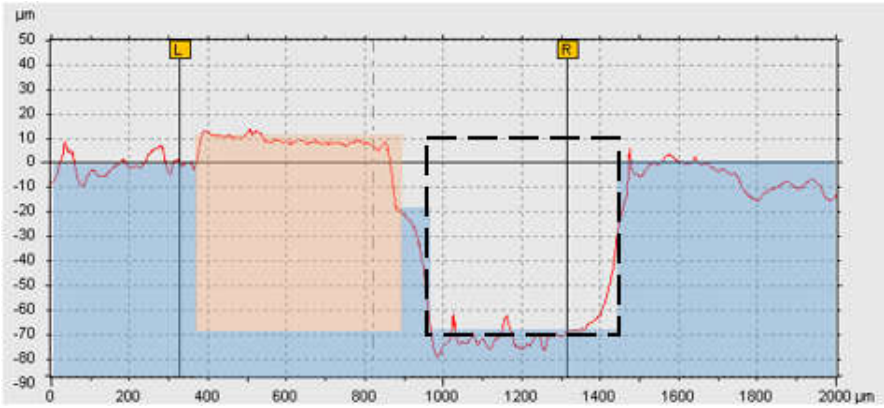


Figure 43. Profilometer output from the embedded sidewalls measurement. Blue and red shapes have been superimposed to illustrate PDMS and deposited copper, while the dashed square outlines the void from the removed copper trace.

The path of the profilometer is shown in Figure 42 as a dashed line, and the resulting profilometer output is shown in Figure 43. In Figure 43, a level of zero represents the PDMS surface. After approximately 400 μm of horizontal travel, the profilometer head rises 10 μm when it encounters the 500 μm wide copper trace. The profilometer then shows a 30 μm step down to the PDMS area between the two copper traces, before dropping an additional 50 μm to the bottom of the void where the second copper trace was removed. After 500 μm of horizontal travel corresponding to the removed trace, the profilometer rises 70 μm to its original level. Blue and red shapes have been superimposed on the figure to illustrate the PDMS and deposited copper, while the dashed square outlines the void from the removed copper trace. It can be seen that approximately 70 μm of the 80 μm copper outer sidewall is embedded in PDMS, while 50 μm of the inner sidewalls are embedded. It is possible that air bubbles between the traces, which may remain due to insufficient degassing, account for the reduced PDMS height compared to the outer walls. Ignoring this reduction, approximately 140 μm of additional copper-PDMS interface exists in the copper trace cross-section due embedded sidewalls. If the adhesion strength is indeed proportional to copper-PDMS interface area, then a significant portion of the adhesion force in thin traces will be due to the sidewalls. This is because the ratio of PDMS-copper interface length to width, *b* (from the WOS calculation), is inversely proportional to the width, *b.* In addition, no matter what the trace width is, at least 140 μm of embedded sidewalls will provide a significant minimum adhesion force to all traces.

Over-Plated Anchor

An over-plated anchoring mechanism is postulated to increase the adhesion of the deposited copper features to the PDMS substrate. This mechanism results from over-plating during the electrodeposition process, which is suspected to produce umbrella-like structures on top of the deposited features. When embedded upside down in PDMS, these structures may act to mechanically anchor the deposited features in place within the PDMS.

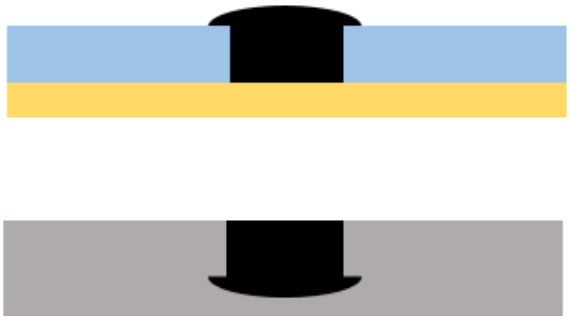


Figure 44. Postulated over-plated anchoring mechanism. An over-plated deposited layer (top) acts as an anchor when transferred to PDMS (bottom).

A diagram illustrating the postulated over-plated anchoring mechanism is shown in Figure 44. The top diagram in Figure 44 shows a copper deposition layer (black) over-plated through the photoresist pattern (blue). When transferred to PDMS, the over-plated portion acts as an anchor in the PDMS as shown in the bottom diagram in Figure 44.

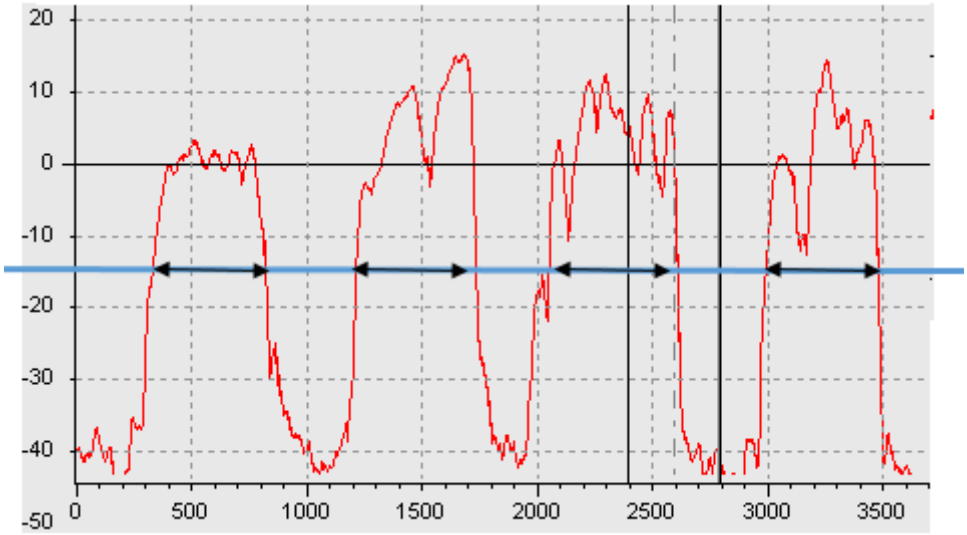


Figure 45. Profilometer measurement corresponding to the top of the copper test structure before transfer to PDMS. Width measurements are collected at the superimposed horizontal blue line.

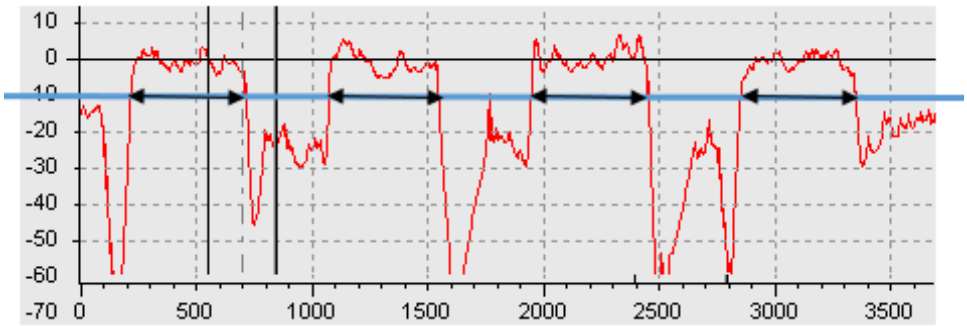


Figure 46. Profilometer measurement corresponding to the bottom of the copper test structure after transfer to PDMS. Width measurements are collected at the superimposed horizontal blue line.

To confirm this speculation, profilometer measurements are taken across the surface of a structure used to test circular spacing (for reference, see Figure 21) before and after transferring to PDMS. If the over-plating hypothesis is true, then the copper width measured at the top of the deposited layer will be larger than the measured copper width at the bottom of the deposited layer after transfer to PDMS. The profilometer measurements corresponding to the top of the trace before transfer and the bottom of the trace after transfer are shown in Figure 45 and Figure 46, respectively. The width of the traces in both figures is measured at the location of the superimposed horizontal blue line, and the arrows indicating width have consistent lengths in both figures.

Table 11. A comparison of the widths at the top and at the base of deposited features (shown in Figure 45 and Figure 46).

	Width 1 (μm)	Width 2 (μm)	Width 3 (μm)	Width 4 (μm)	$\bar{x}$ (μm)	σ (μm)
Before Transfer (Cu top)	482.6	509.0	558.6	492.3	510.6	33.8
After Transfer (Cu bottom)	504.2	475.6	504.2	501.5	496.3	13.9

The width measurements from Figure 45 and Figure 46, including the calculated mean and standard deviation of the widths, are summarized in Table 11. From Table 11, the copper trace width is approximately 500 μm in both sets of data, as expected. The mean width after transfer is approximately 15 μm smaller than the mean width before transfer, indicating that a small over-plating effect may be present. However, considering

the relatively large standard deviation of the measurements compared to the difference in the mean, the over-plating effect may, in fact, be negligible. To properly analyze the over-plated features and any relationship to the copper-PDMS adhesion strength remains a goal for future work.

Chapter 5.

Applications in Stretchable and Wearable Electronics

In Chapter 2, we review a growing number of applications in the field of stretchable electronics. These applications incorporate conformal electronic devices with dynamic surfaces that are unconventional in the context of traditional microelectronics. There are two primary areas of research in this field; the first area is in the development of novel materials and fabrication processes for stretchable conductive layers, and the second is in investigating innovative conductive patterns to enhance stretchability. In this chapter, we present an application of the novel fabrication process introduced in Chapter 3 to the field of stretchable electronics. This demonstration includes the design, fabrication, and characterization of first-order curved Peano structures fabricated using the newly developed thick-film copper metallization process. We also study the effects of modifying Peano-curve geometries to maximize the stretchability these structures. This includes a characterization of the relationship between relative resistance and tensile strain in fabricated devices while systematically varying the geometric parameters of various curve designs. We also characterize the response of the fabricated structures to cyclic failure and recovery. These results demonstrate the successful application of the newly developed process to stretchable electronics, enabling highly conductive, low-cost stretchable devices. These results also provide insight into the geometric optimization of Peano curves for stretchable interconnects.

Wearable electronics, a more recent development of stretchable electronics, represents an attempt to integrate sensing, actuating, communicating and computing components with the human body via clothing [40]. Wearable substrates such as fabrics are typically not suitable as substrates in traditional fabrication processes. Therefore, integrating electronics with wearable substrates remains an ongoing challenge. Some approaches to this challenge include developing conductive fibers and conductive patterns screen-printed on fabric [44]. However, while such fibers and screen printable

inks are conductive, their conductivity has not been shown to match that of metals. This is important as low power and high portability are common constraints in wearable applications. To overcome this problem, we present a modified version of the fabrication process in Chapter 3 that enables the integration of highly conductive stretchable metal patterns directly with stretchable fabric. This process modification is characterized by a simple new stamping technique that is easily adapted to a wide range of target substrates. Using the optimized Peano-curve patterns developed previously in this chapter, we also characterize the stretchability of the conductive patterns deposited onto a stretchable fabric for wearable electronics. Thus, we provide a novel process for wearable electronics fabrication by integrating highly-conductive, low-cost stretchable metal patterns directly with wearable fabrics

Much of the background material relevant to stretchable electronics, stretchable geometries, and wearable electronics is presented in Chapter 2, particularly in the introductory paragraphs and in Section 2.6. This includes an in-depth discussion of stretchable and wearable electronics applications, and a summary of the current challenges faced by modern fabrication processes. Peano curves and stretchable geometries are also introduced. We review a selected portion of the background material relating to Peano curves here, as this material is referenced frequently in this chapter.

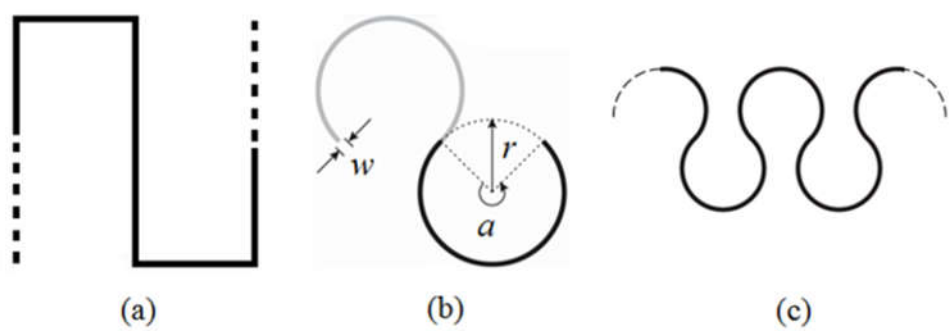


Figure 47. (a) A traditional unit Peano curve and (b) a modified unit Peano curve defined by trace width w, radius r, and arc angle a. (c) A first-order Peano curve is a repeated unit horseshoe pattern [29].

Stretchable metal patterns can generally be achieved on polymers using pre-stressed, thin-film, metal conductors that form stretchable metallic surface waves [112] [113], or in-plane metal conductors that are able to stretch via the bending

of curves in a serpentine pattern [114] [115] [116] [117] [119]. In the work of Rogers et al. [115], a fractal-inspired space-filling curve, or Peano curve [119], supports biaxial and radial strains while allowing for a range of conductor topologies. The traditional unit Peano curve is shown in Figure 47(a) [119], along with the modified unit Peano curve having rounded corners in Figure 47(b) [115]. A thorough explanation of the geometric parameters describing the curve in Figure 47(b) is given in Section 5.1.1.

It is also interesting to note that, besides enabling stretchable devices in general, fractal-inspired Peano patterns are adapted by Rogers et al. in a mechanically-tunable radio frequency device [115]. The device has a fundamental mode at 1.7 GHz and an impedance of 42 Ω at resonance. Such a demonstration is relevant to the application of our proposed process in wearable electronics, as the frequency response of integrated devices can often be a critical component in the design of a wearable device. In future work, we hope to characterize the frequency response of similar devices fabricated using the proposed process, and explore the possibility of integrating wireless communications and charging components with wearable fabrics.

In this thesis, we expand on the investigation of Peano curves and similar patterns for use in stretchable electronics by fabricating a large set of repeated first-order Peano curve structures and systematically testing the effect of geometric parameter variation on stretchability. Stretchability is defined here as the ability to maintain conductivity under an applied strain. Such geometric parameter variation has thus far only been simulated in existing studies, or physically tested to a lesser extent. In addition to thoroughly examining the effect of geometric parameter variation on stretchability, we characterize the evolving strain measured at device failure during cyclic stretching and relaxation conditions, which is not demonstrated in existing studies. Failure is defined in this thesis as the point at which a device exhibits zero conductivity due to an increasing applied strain.

5.1. Stretchable Interconnects

The process modifications in this thesis are based off the newly-developed process presented in Chapter 3. Similar to other in-plane metallization

methods [114] [117], the deposition of metal is achieved via electrodeposition due to its relatively low cost and process complexity. The distinguishing feature of this process is the metal transfer step, which includes an IR-assisted heating method to facilitate the transfer of copper structures to PDMS. This eliminates the need for chemical processing and enables the direct transfer of metal patterns to a wide range of substrates, including stretchable fabrics.

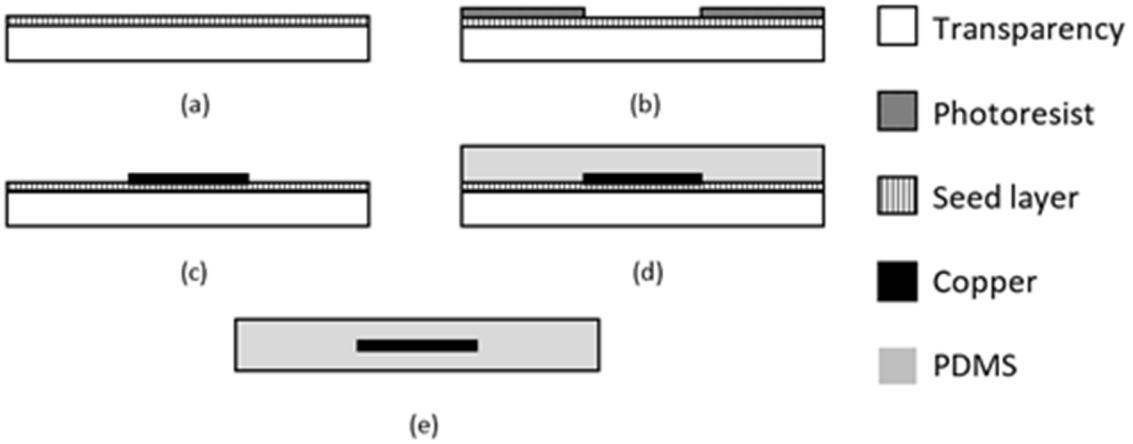


Figure 48. Base fabrication process. (a) A transparency film is airbrushed with a conductive copper paint layer before (b) photoresist is deposited and patterned. (c) Copper is deposited through the photoresist, which is then stripped before (d) liquid PDMS is poured over the assembly. (e) A baking procedure transfers the copper to PDMS and a PDMS encapsulation layer is added [31].

A simplified description of the base process is shown in Figure 48, which is used for reference when comparing to the modified process described in Section 5.2.1. A clear transparency film designed for high temperature applications is the substrate for an electrically conductive copper paint seed layer, as shown Figure 48(a). The seed layer is deposited using an airbrush. Dry film photoresist is laminated on top of the seed and patterned using standard photolithography, as shown Figure 48(b). In Figure 48(c), a 70 μm copper film is deposited through the photoresist mask via electrodeposition and the remaining photoresist is stripped. The metal transfer step is distinguished by an IR-assisted transfer process, with the copper structures initially embedded in uncured PDMS, as shown Figure 48(d). During heating, the PDMS cures and the copper structures are delaminated from the seed, remaining embedded in the PDMS. The

deposited layer is optionally encapsulated with an additional PDMS layer, as shown in Figure 48(d). This method does not require chemical processing, though any remaining seed layer residue that is transferred with the copper can be rinsed away with methanol, if desired. This process is modified in Section 5.2.1 as a stamping process for the direct transfer of metal layers to fabrics.

5.1.1. Stretchable Geometry

Serpentine patterns are commonly used when fabricating stretchable structures in planar metallization processes [114] [115] [116] [117] [118]. These structures are formed by periodically repeating a horseshoe pattern defined by the trace width *w*, arc angle *a*, and radius *r*, as shown in Figure 47(b). A scale factor equal to r/w is also defined, which is independent of arc angle [118]. This horseshoe pattern is a modified version of the traditional unit Peano curve shown in Figure 47(a). In this thesis, a horseshoe pattern repeated in one direction (c) describes a first-order Peano curve, to which uniaxial strains can be applied while resistance is measured. Higher-order Peano curves are formed by repeating the unit horseshoe geometry in fractal-based patterns, and support biaxial and radial strains [115]. However, such higher order curves are not explored in this thesis. Although several groups have simulated and characterized a small set of first-order curves, the systematic characterization of fabricated curves through parameter variation has not been demonstrated.

The first characterization that we perform with fabricated devices investigates the relationship between the strain measured at conductive failure and the scale factor, r/w. One simulation-based study using first-order curves has shown that increasing the scale factor leads to a decrease in strain within the conductor during stretching [118], which is interpreted as an increase in stretchability. Another set of simulations using second-order curves has shown that, at a certain point, increasing the scale factor can decrease the strain measured at the onset of plastic deformation within the conductor, which is interpreted as a decrease in stretchability [115]. The scale factor that results in the largest strain before the onset of plastic deformation can be identified as the optimal scale factor. To reconcile the results between the two studies, we test geometries using the optimal scale factor found in simulation [115], defined here as α and approximately

equal to 4.57, and the beyond-optimal scale factor used in fabrication [115], defined here as β and approximately equal to 8.85.

The second result that we propose to verify with physical models is that stretchability is proportional to a curve's arc angle. Previous simulations have shown that the strain measured at the onset of plastic deformation within the conductor increases proportionally to the arc angle, from 180˚ to 270˚ [115]. To verify these simulations and expand the current understanding beyond the 270˚ limit, we perform characterization experiments on geometries with 180˚, 270˚, and 285˚ arc angles. Arc angles greater than 285˚ are not tested as the resulting curves exhibit small separation distances or overruns between neighbouring traces.

Finally, we characterize the ability of these structures to recover after being stretched beyond conductive failure and relaxed. Previous studies have performed cyclic testing of similar structures at relatively lower strains to measure the response to fatigue [120], but we have been unable to find results that demonstrate cyclic testing beyond conductive failure and recovery.

Table 12. Geometric parameters for the twelve different structures tested in this thesis. The dimensionless scale factors (equal to r/w), α and β, are 4.57 and 8.85, respectively [29].

Structure Number	Arc Angle (˚)	Copper Width (μm)	Scale Factor
1	180	100	β
2	180	200	β
3	180	300	β
4	270	100	β
5	270	100	α
6	270	200	β
7	270	200	α
8	270	300	β
9	270	300	α
10	285	100	β
11	285	200	β
12	285	300	β

The strain measured at the point of conductive failure determines the stretchability of a given structure. A comparison of the stretchability between all structures reveals the effects of geometric parameter variation on stretchability. In the cyclic failure tests, the strain is measured both at the point of failure during stretching and at the point of conductive recovery during relaxation. This allows us to quantify the ability of these structures to recover after iterative failures. Twelve unique structures are evaluated in this thesis with geometric parameters given in Table 12. The structure numbers associated with each geometry allow for convenient referencing in the following sections. To provide a statistical assessment of the results, three samples of each structure are fabricated and tested, resulting in thirty-six individually tested samples.

5.1.2. Results and Discussion

In this section, we present the results and analysis of the characterization experiments described in Section 5.1.1. This analysis provides a contribution to the understanding of geometric optimization for stretchability using measurement data and a comparison to existing studies. In addition, we provide a demonstration and characterization of the cyclic failure and recovery of devices fabricated using the newly developed process.

Test apparatus

Samples are tested individually with one end fixed in position and the other end connected to a movable load cell (FUTEK LRF400, 5lb). The load cell is positioned with a linear stage (Zaber Technologies T-LS28-SMV). The positioning of the linear stage is controlled with using LabVIEW (National Instruments). Tests are performed by commanding the linear stage to move the load cell, which pulls one end of the sample in tension while force and position measurements are recorded by the load cell and linear stage, respectively. Only uniaxial tensile forces are applied.

Resistance is calculated using voltage measurements recorded during stretching using a 12-bit National Instruments PCI data acquisition card (NI PCI-6071E). Resistance and position values are both sampled at 20 Hz, while the stage position is moved at 10 μm/s. Note that we perform these tests using a single strain rate. In the

future, we intend to explore the relationship between strain rate and stretchability. Copper tape (3M™) is attached to each end of a sample to provide external electrical connections. A silver-based ink is added at the connection sites to ensure stable connectivity to the testing apparatus.

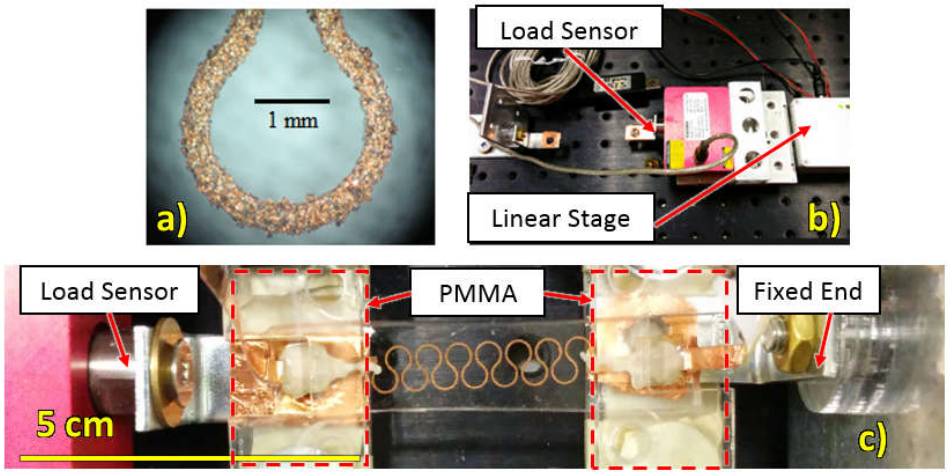


Figure 49. (a) Magnified view of an individual arc in a sample structure. (b) Testing apparatus. (c) Full view of a sample structure before testing [29].

Figure 49(a) shows a single arc of an individual sample under magnification, (b) shows the sample testing platform, and (c) shows a sample without magnification prior to testing. The brackets connecting the sample to the testing platform are visible in Figure 49(b) and (c). Each end of the sample rests above one of these brackets, while two pieces of laser-cut PMMA sit below the bracket and above the sample on each end. The PMMA pieces are then forced together using a screw tensioning system (not visible) until each end of the sample is firmly affixed to its corresponding bracket. As the linear stage is commanded to move, the attached bracket pulls one end of the sample while the other remains fixed, which results in the sample experiencing a uniaxial strain. Though the sample is free to rotate where it is not attached to either bracket, sample rotation is inhibited by a relatively large contact area between the sample and the brackets.

Uniaxial stretching until failure

The first set of experiments characterize the relationship between strain and relative resistance as the samples are stretched uniaxially from a resting position to the

point of failure. Before stretching, initial values of resistance and stage position are recorded. Strain, also known as percent elongation and written $\Delta L/L_o$, and relative resistance values ($\Delta R/R_o$) are calculated from these measurements.

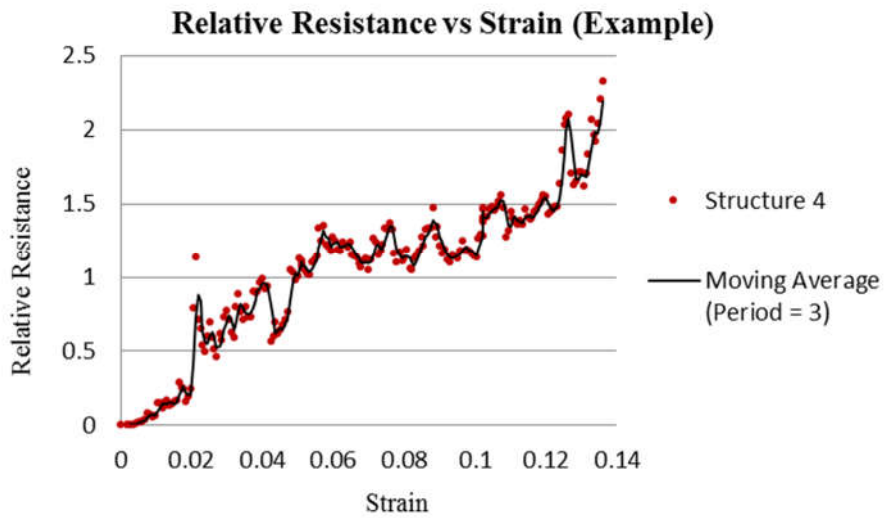


Figure 50. Relative resistance versus strain from an example uniaxial strain test. This test corresponds to one the Structure 4 samples.

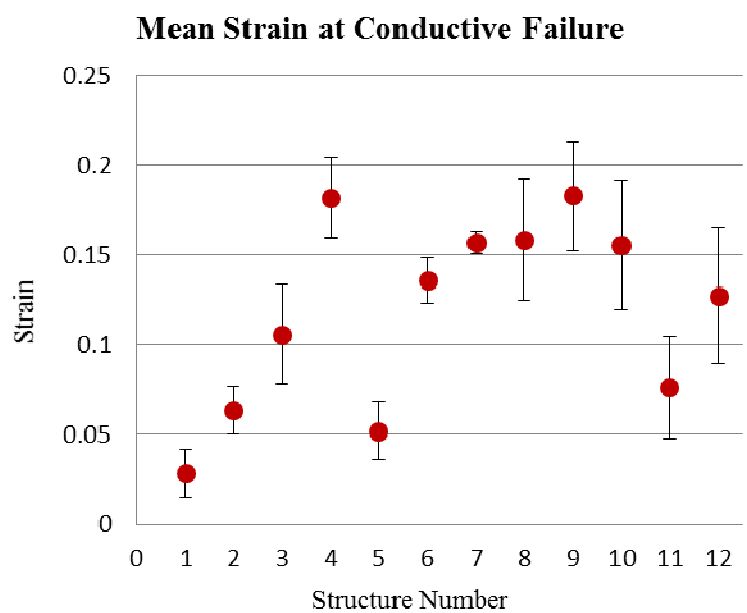


Figure 51. Aggregated results showing the average strain measured at conductive failure for all structures [29].

Figure 50 shows an example graph of relative resistance versus strain generated from the data collected during a single experiment. A moving average trend line (black) with a period of three is also shown. This data corresponds to the third test of Structure 4, with a final strain at failure of 0.14. In this graph, the regions of elastic and plastic deformation (described in Section 2.1) are visible. However, many of the tests result in an abrupt jump in relative resistance at the point of failure. Therefore, in the current iteration of the process, the interconnects are not suitable for applications where a smooth evolution of resistance versus strain is required, such as strain gauges. Methods to improve consistency during stretching may be explored in future work.

As mentioned, three tests are performed for each of the twelve geometries resulting in a total of thirty-six measurements. After testing three samples of each structure, the mean and standard error of the mean for the strain measured at failure are calculated and shown together in Figure 51.

To determine the effect of arc angle, we compare structures with a constant scale factor while varying the arc angle. These tests are performed for three groups in total, all of which have equal scale factors. Each group contains samples with arc angles of 180˚, 270˚, and 285˚. However, the magnitudes of the parameters used in the scale factor calculation (*r* and *w*) differ among the groups.

Table 13. The three groups of structures from Table 12 used to test the effects of arc angle. All structures have a constant scale factor (β), and each group has a constant trace width.

Group Number	Structure Number	Arc Angle (˚)	Copper Width (μm)	Scale Factor
1	1	180	100	β
	4	270	100	β
	10	285	100	β
2	2	180	200	β
	6	270	200	β
	11	285	200	β
3	3	180	300	β
	8	270	300	β
	12	285	300	β

The groups of structures used to test the effects of arc angle variation are defined in Table 13. Samples in the first, second, and third group have copper trace widths of 100 μm, 200 μm, and 300 μm, respectively. In each group, the average strain at failure is found to be greatest in the 270˚ structures (all other parameters being equal), followed by the 285˚ structures, and lastly the 180˚ structures. The increased strain at failure in samples with a 270˚ arc angle compared to 180˚ confirms the simulation results in existing studies [115]. The decrease in strain at failure for arc angles of 285˚ compared to 270˚ is consistent among the sample groups and is intriguing. The decrease in strain at failure breaks the trend of increasing strain with increasing arc angle. However, we are not aware of any existing studies that confirm the consistency of these results. This warrants further investigation of arc angles beyond 270˚. One possible explanation for this behaviour is that larger arc angles result in areas of increased strain within the conductor, particularly where the angle of the conductor path is opposed to the direction of tension.

To determine the effect of scale factor, we again use three groups of structures. we compare structures with a constant arc angle while varying the scale factor. Here, all structures have a constant arc angle of 270˚, while each group contains two structures with similar trace width and one structure per scale factor.

Table 14. The three groups of structures from Table 12 used to test the effects of scale factor. All structures have a constant scale factor (β), and each group has a constant trace width.

Group Number	Structure Number	Arc Angle (˚)	Copper Width (μm)	Scale Factor
1	1	270	100	β
	10	270	100	α
2	2	270	200	β
	11	270	200	α
3	3	270	300	β
	12	270	300	α

The groups used to test the effects of scale factor are defined in Table 14. Simulations in an existing study presented by Fan et al. suggest that structures with a beyond-optimal (larger) scale factor will result in a lower value for the strain measured at

failure compared to the structures with the simulated optimal scale factor [115]. However, this is contrary to the observations in another study presented by Gonzalez et al., which indicate that increasing the scale factor increases the strain measured at failure [118]. For structures having 300 μm and 200 μm trace widths, we observe an increase in the average strain at failure for the optimal scale factor compared to the larger scale factor determined in the study presented by Fan et al. [115]. However, for structures having 100 μm trace widths, this relationship is reversed. Therefore, a conclusive statement regarding the relationship between scale factor and strain at failure cannot be made for the geometries tested here. This result provides support for the inconsistency between the studies presented by Fan et al. and Gonzalez et al. [115] [118], and indicates that maximizing the scale factor may yield inconsistent results.

A more detailed analysis of the simulations in Gonzalez et al. shows that while increasing the scale factor consistently improves stretchability according to a predictable relationship, this relationship becomes less predictable at scale factors lower than approximately 7.5. Therefore, while a scale factor of approximately 4.57 is predicted to be optimal in the study presented by Fan et al. [115], this falls in the region of decreased predictability shown by Gonzalez et al. [118]. This provides some justification for the discrepancy between these two studies. This is of particular importance considering that smaller scale factors correspond to more compact designs. That is, for a given trace width, a smaller radius reduces both the device footprint and the scale factor. The drive to design for smaller footprints must then be balanced with the understanding that miniaturization may have an unpredictable impact on stretchability. Detailed simulations are warranted for new designs to ensure the desired balance between decreasing the device footprint and the resulting unpredictability of a decreased scale factor.

Cyclic tension testing

A subset of the structures tested for uniaxial stretching is selected to conduct cyclic failure and recovery experiments. Six samples, comprising one sample each of Structure 2, 5, 6, 7, 9, and 12 are chosen for these tests, as these structures represent the population of geometric parameters used in this thesis.

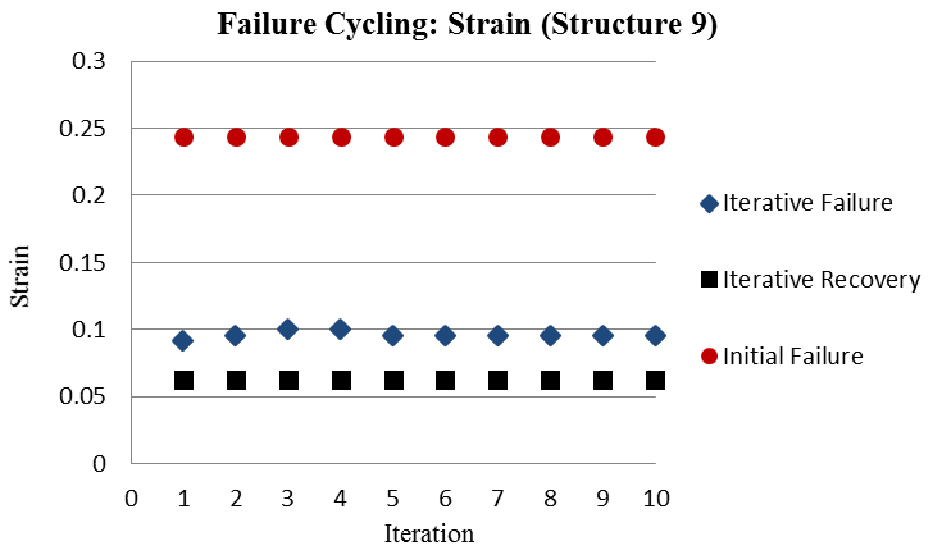


Figure 52. Strain measurements for one sample (Structure 9) collected during conductive failure and recovery cycling [29].

The cyclic failure experiment begins by stretching the sample while recording the strain and relative resistance at failure. The sample is then relaxed, and the strain and relative resistance are recorded at the point of conductive recovery. The relative resistance is also collected at the point of zero strain after recovery. The cycle of failure and recovery is carried out for ten iterations. The selected number of iterations is not expected to constitute a long-term measurement of the structures' response to failure and recovery. However, we speculate that ten iterations are sufficient to identify any clear trends in the short-term cyclic failure and recovery data.

Figure 52 shows a single representative sample (Structure 9) of the strain measured during ten cycles of failure and recovery. The strain at the initial failure (before any previous failures) is shown as a constant for reference against the strain value for iterative failure and recovery in each cycle. The strains at iterative failure and recovery also appear relatively stable. In addition, the strains at failure and recovery are both lower at each iteration than the strain at the initial failure, which is reasonable since the structure does not initially contain any of the breaks, cracks, or other discontinuities that presumably occur after the first failure. The strain at failure is larger than the strain at recovery, which indicates that the structures are more effective at retaining conductivity while being stretched than they are at recovering conductivity after being relaxed.

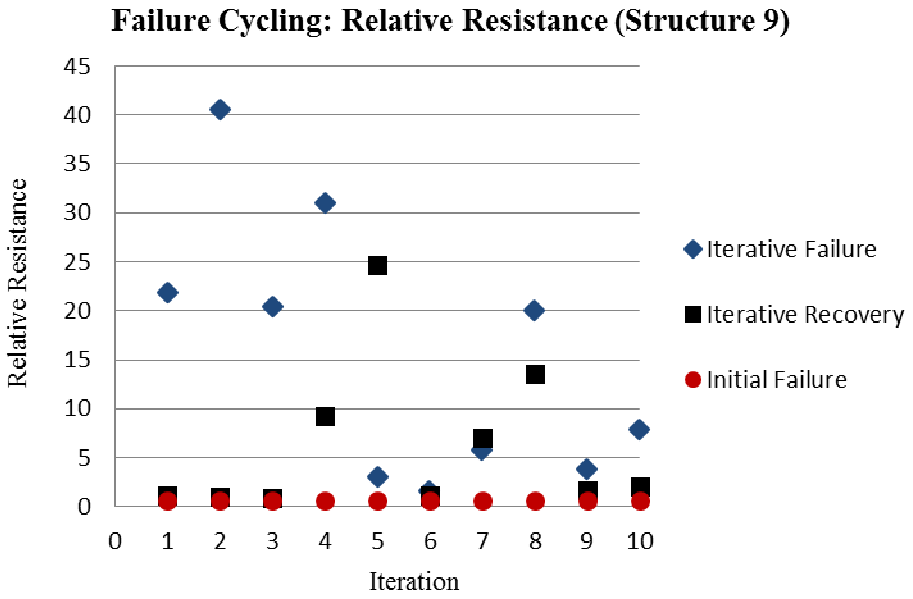


Figure 53. Relative resistance measurements for one sample (Structure 9) collected at conductive failure and recovery during strain cycling tests.

Although the failure and recovery occur at a consistent strains, the relative resistance values measured at this point are less consistent, as shown in Figure 53. We speculate that this is due to the unpredictable nature of the discontinuities in the conductor at the point of failure. If the conductor separates at the point of failure abruptly, then the relative resistance measured just before the point of failure may be small. However, if a discontinuity (break in the conductor) grows slowly over time, the measured relative resistance may increase significantly before the conductor separates entirely. Similarly, during recovery, the contact area at the point of reconnection may be unpredictable. Thus, a large degree of variation in relative resistance may be expected. At successive iterations, the relative resistance at recovery tends to follow the relative resistance at failure, and is often less than the relative resistance at failure. This trend is consistent in all structures undergoing this test. Considering that recovery happens at lower strains compared to failure, it is not surprising that the relative resistance should also be lower, as relative resistance tends to be proportional to strain.

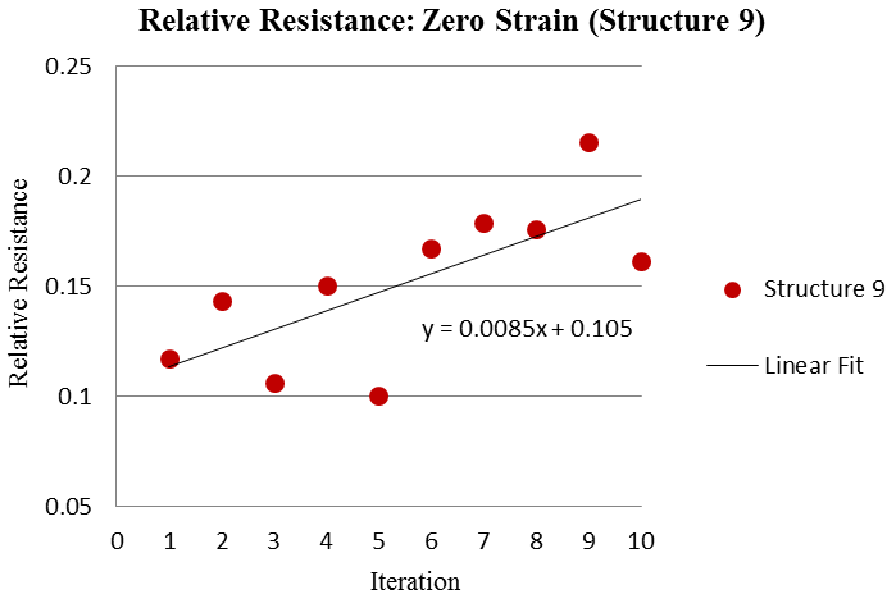


Figure 54. Relative resistance measurements for one sample (Structure 9) collected at zero strain during strain cycling tests.

The relative resistance values measured at zero strain (after recovery) for Structure 9 are shown in Figure 54. This plot shows that the resistance at zero strain after successive failures is approximately 15% higher than the original resistance before failure. A linear fit of the data indicates that the relative resistance may be increasing proportionally to the number of iterations. This suggests a decrease in performance at zero strain as the device experiences additional failures.

Table 15. Relative resistance values measured at zero strain (after failure) for six representative structures.

Structure	2	5	6	7	9	12
Mean	0.29	0.27	0.12	0.0087	0.14	0.12
Standard Error	0.099	0.038	0.013	0.013	0.017	0.015
Slope of Linear Fit	-0.051	0.015	-0.0032	0.0095	-0.00070	0.0094

A summary of the same data collected for all six representative structures is shown in Table 15. For all structures, the mean relative resistance at zero strain after all ten recoveries is shown, and is consistently greater than the original resistance. However, the magnitude of the mean relative resistance and the slope of the linear fit among all iterations are both inconsistent. In half of the cases, the slope of the linear fit

is negative, suggesting a trend of increased performance in terms of relative resistance at zero strain after successive iterations. However, we caution that the amount of data is limited and do not assume that this behaviour represents a general, long-term trend. It is clear, however, that a performance degradation at zero strain results after successive failures.

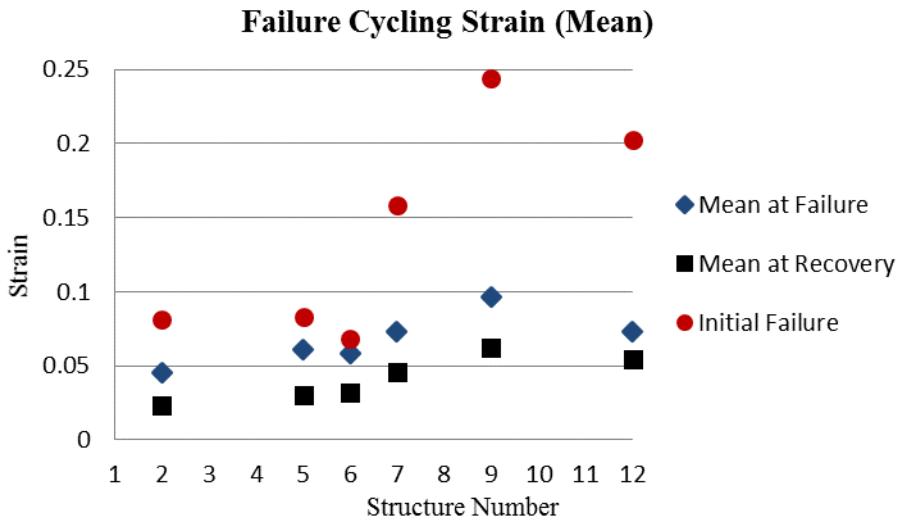


Figure 55. Aggregated results for six representative geometries measuring mean strain at conductive failure over ten cycles of failure and recovery [29].

Having collected cyclic failure and recovery data for six different samples, the mean strain at failure and recovery across all iterations for each structure are calculated and plotted together in Figure 55. Figure 55 shows once again that the strain at the initial failure is the largest for all structures, followed by the average strain at failure and the average strain at recovery. As expected, samples with a larger strain at the initial failure generally have a larger average strain at failure and recovery across all iterations.

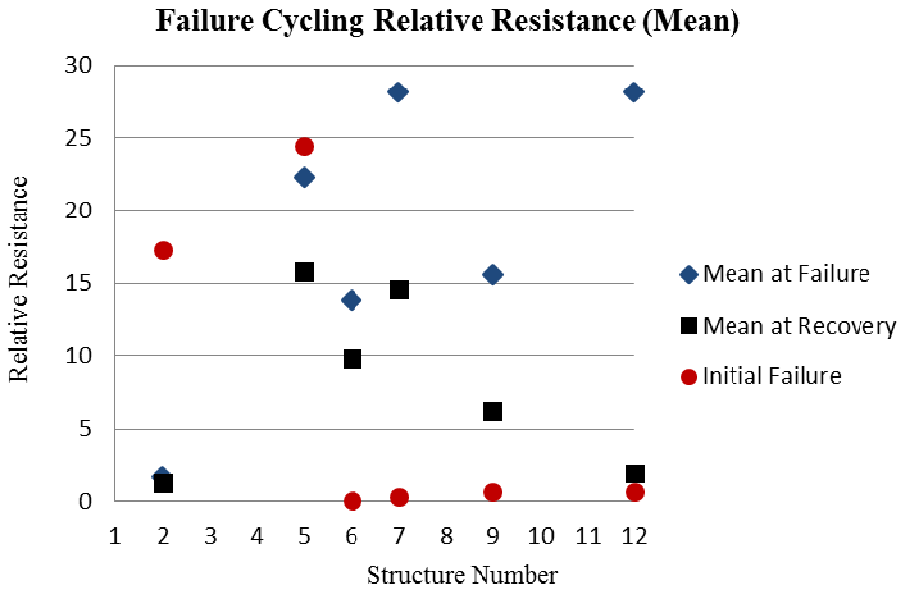


Figure 56. Aggregated results for six representative geometries measuring mean relative resistance over ten cycles of conductive failure and recovery.

The relative resistance values measured during failure and recovery are found to be generally less consistent compared to the strain, as shown in Figure 56. One consistent feature is that, for all samples, the average relative resistance at failure is higher than the average resistance at recovery. It is interesting to note that the relationship between the relative resistance at the first failure and the mean of the relative resistance across all ten cycles is unpredictable. Similar to the analysis of Figure 53, this degree of scatter in the data may be attributable to the fact that failure and recovery occur at a location in the conductor that has an unstable connection. Thus, a large degree of variation in relative resistance may be expected.

5.2. Wearable Interconnects

In this section, we characterize a wearable device fabricated using a modified process with patterns transferred directly onto stretchable fabric. The device consists of a stretchable interconnect design as defined by Structure 9 in Table 12, which is shown in Section 5.1.2 to be capable of enduring the largest strain before conductive failure

relative to other tested designs. We modify the base transfer process described in Section 5.1 to enable the transfer of deposited copper patterns directly to stretchable fabric. The same testing procedure and apparatus from Section 5.1.2 are employed to characterize the relationship between relative resistance and strain in fabricated devices. We also characterize the mechanical constraints imposed by interconnects on the fabric substrate by measuring the force required to stretch the devices compared to an unmodified fabric sample. Through an analysis of the characterization results, including a comparison to the results in Section 5.1.2, we conclude that the newly developed process is well suited to low-cost wearable electronics applications with strict electrical and moderate mechanical requirements.

5.2.1. Modified Transfer Process to Fabrics

In the modified process, the role of PDMS is converted from that of a substrate to an adhesive layer that enables metal layers to be transferred directly onto fabrics. In this manner, copper patterns can be 'stamped' directly onto the target substrate. The modified process is illustrated in Figure 57. Figure 57(a) shows the patterned copper layer on the sacrificial seed layer, which is identical to the corresponding stage of the base process shown in Figure 48(c). The modified process differs from the base process in Figure 57(b), where a thin layer of PDMS is deposited onto the stamp. Figure 57(c) demonstrates the copper stamp placed on top of the target substrate, and the IR-assisted transfer proceeds as before. The result shown in Figure 57(d) is a copper pattern deposited directly onto the fabric. During the transfer, liquid PDMS is embedded within the voids of the fabric creating a fully integrated PDMS-fabric hybrid layer with exceptional adhesion.

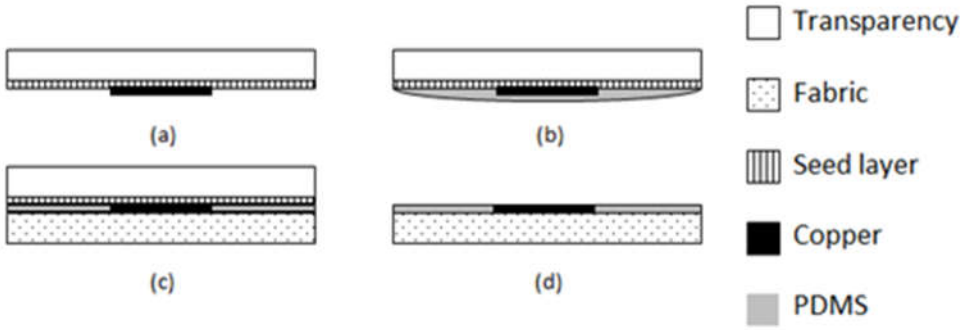


Figure 57. A modified process for stamping conductive layers onto wearable fabrics. (a, b) A thin layer of PDMS is deposited onto a metal pattern stamp before (c) being placed on top of the target fabric. (d) An IR-assisted baking procedure releases the metal into the PDMS, and cures the PDMS as it integrates with the fabric [31].

In step (b) from Figure 57, 1 mL of PDMS is deposited onto the metal pattern before transfer. This results in a final PDMS thickness of approximately 100 μm. However, the PDMS thickness is inconsistent across the fabric substrate and is difficult to measure accurately. A detailed study of the PDMS adhesive layer is left to future work.

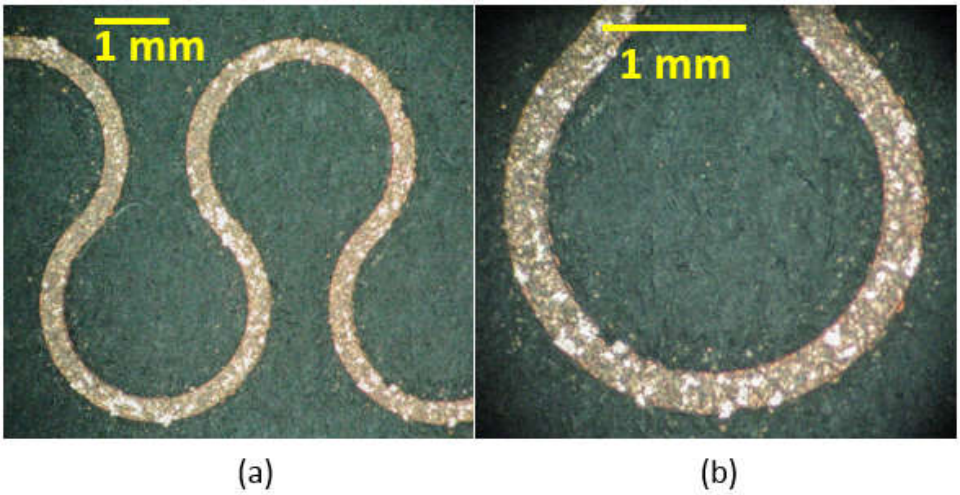


Figure 58. Magnified views of the metal-on-fabric assembly before PDMS encapsulation.

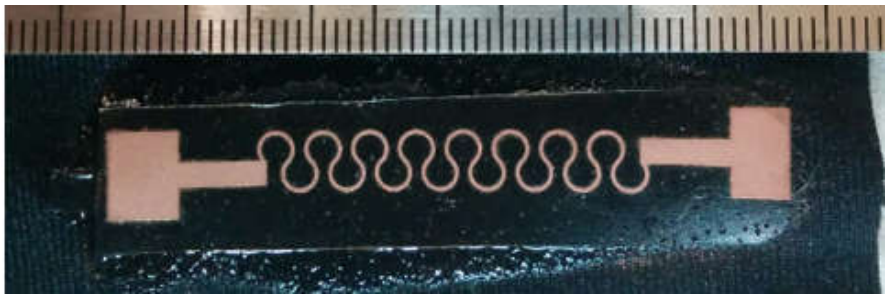


Figure 59. A stretchable interconnect for wearable electronics. The metal deposition layer is transferred directly to the fabric substrate through a modified stamping process [31].

In this thesis, the target substrate is the stretchable fabric Luon™ from Lululemon Athletica. We select this particular fabric due to its popularity and well-known stretchable qualities. The curvilinear pattern shown in Figure 59 has the same design as Structure 9 from Section 5.1.2, and accommodates the most strain among all tested structures. Each segment in the curve has a 300 μm trace width, an arc angle of 270º, and a radius of curvature of 1.37 mm. Magnified views of the assembly are shown in Figure 58.

5.2.2. Characterization

In this section, we characterize the wearable interconnects described in Section 5.2.1. We demonstrate that the devices exhibit a high degree of stretchability and conductance, and that the modified process is well suited to wearable electronics applications. The characterization is less comprehensive compared to Section 5.1.2, and focuses only on the stretchability of a single geometry (Structure 9 from Table 12). Three identical samples are fabricated on stretchable fabric, and each device is subjected to a uniaxial strain test. The strain measured at conductive failure determines the stretchability of the wearable interconnects, while the force versus strain curve quantifies the mechanical constraints imposed on the fabric.

Table 16. Strain measured at conductive failure, initial resistance, and force versus strain for each stretch test. The wearable interconnects can accommodate approximately 57% elongation before failure, and require 40 N of tensile force per unit of strain (100% elongation).

	Sample	Strain	R_o (Ω)	Force/Strain (N)
	1	0.601	0.12	36.3
	2	0.520	0.10	34.9
	3	0.600	0.40	38.6
Mean	-	0.574	0.21	36.6
Std. Err.	-	0.027	0.10	1.08

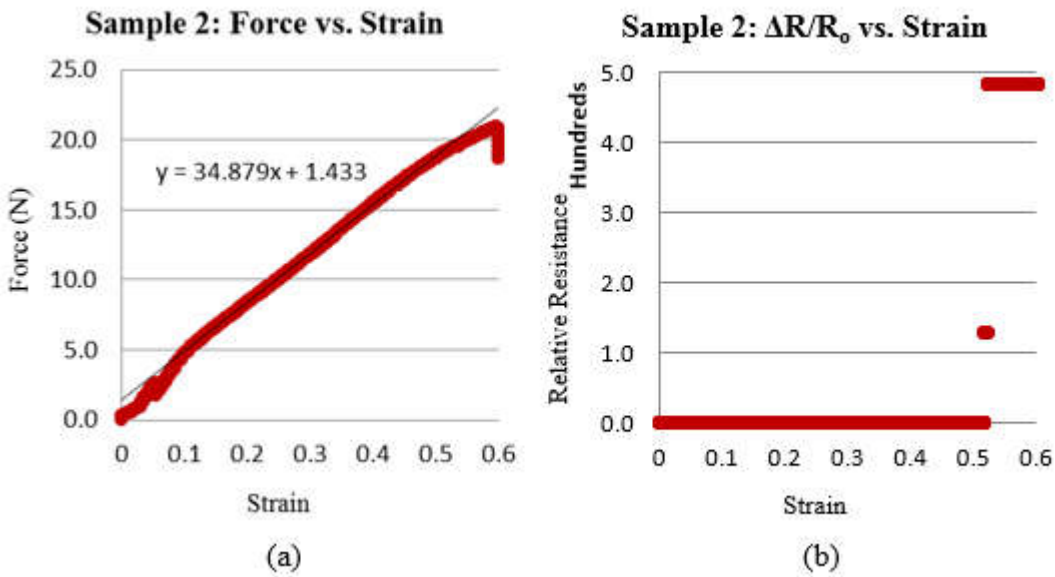


Figure 60. (a) Force versus strain and (b) relative resistance versus strain for the second test sample.

The results of a single test sample are shown in Figure 60. This example shows that approximately 37 N of tensile force is required per unit of strain (100% elongation), and that the device is able to stretch by 52% before experiencing conductive failure. The results for each sample are qualitatively similar to those shown in Figure 60, including the abrupt increase in relative resistance at the point of failure. The results for all tests, including initial resistance, are summarized in Table 16.

5.2.3. Discussion

In Section 5.1, the mean strain at conductive failure for Structure 9 is shown to be approximately 0.18. In comparison, the mean strain of approximately 0.57 given in Table 16 is significantly larger for the same geometry. This may indicate that the modified process for transferring patterns directly to fabrics results in increased stretchability. However, it is important to note that the fabrication of the devices in Section 5.1 corresponds to an earlier iteration of the base fabrication process [30]. In contrast, the wearable devices in Section 5.2 correspond to a more recent and improved version of the base fabrication process [28]. Although the general processing steps are the same between the two process iterations, the experience gained between the two studies has resulted in an improved deposition layer in many respects, with the most notable improvement being an increase in conductivity by a factor of two. It is conceivable that the increase in stretchability observed between Section 5.2 and Section 5.1 is mainly due to improvements in metal layer deposition, rather than process modifications made when transferring to fabrics. To resolve this inconsistency, the experiments in Section 5.1 and Section 5.2 must be repeated using the same iteration of the base process.

The overall performance of the wearable interconnects, including an approximate elongation of 57% at failure and initial resistance of 0.2 Ω, is comparable to existing technology and, in some ways, superior. Similar Peano-based, metal conductors are able to withstand 52% to 72% elongations before failure with initial resistances of approximately 10 Ω [114] [117]. Therefore, the thick-film curves developed in this thesis are comparable to similar Peano-based strategies in terms of their ability to stretch before failure. At the same time, the initial resistance in our devices is between 10 to 100 times smaller [114] [117], which is due to the deposition of thick metal films enabled by the new fabrication process. It is important to note that the strain values reported here are within the strain limits imposed by human skin, which exhibits an elastic response to strains less than 15% and is permanently damaged by strains over 30% [172]. Therefore, from a mechanical reliability perspective, these devices are wearable.

In comparison, conductive textiles employing metal wires integrated with woven fabrics are typically only able to stretch by 20% to 30% due to the basic structure of

woven and non-woven textiles [40]. In contrast, NCP-based devices are able to withstand elongations beyond 300% and exhibit excellent responses of relative resistance to strain [173]. However, the superior mechanical performance of NCP-based devices is paired with large initial resistances, up to several mega-Ω, which can be prohibitive in applications with low power requirements [173]. For applications requiring low resistance and moderate stretchability, we provide an excellent process alternative to existing technology. This process also has the added benefits of low fabrication costs and the ability to transfer directly to a variety of substrates.

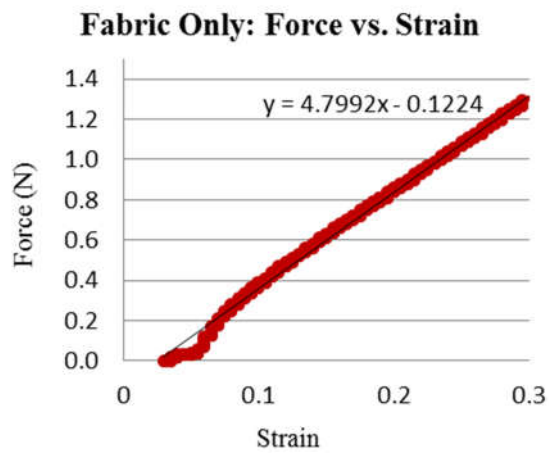


Figure 61. Force versus strain for an unmodified sample of Luon™ fabric.

One drawback of the current process as it applies to wearable electronics is the relative increase in force required per unit of strain compared to unmodified fabric. From Table 16 (presented earlier in this discussion), an average force of 37 N is required to stretch our devices by 100%, while the characterization of unmodified Luon™ in Figure 61 indicates that approximately 4.8 N is required for the same strain. Therefore, although we have demonstrated excellent electrical and mechanical properties from a reliability perspective, wearable applications for commercial use will likely require a reduction in mechanical constraint imposed upon the target substrate.

It is also important to note that, although we characterize the force-strain relationship in the forward (tensile) direction, we do not investigate the presence of hysteresis upon unloading. Many cycles of loading and unloading are expected in wearable applications. Therefore, it is important to study this behaviour in future work, as

well as the relationship between uniaxial force and strain under cyclic testing conditions. Wearable fabrics are also expected to experience additional forms of stress, such as bending and twisting. Therefore, future experiments must also evaluate these additional forms of stress through modified testing platforms. It is useful to model such platforms on the human body [174], though a more complete description of future testing platforms is beyond the scope of this thesis.

Chapter 6.

A Multi-layer, Fully-flexible, Electromagnetic MEMS Actuator for Large Magnetic Field Generation

The main goal of this chapter is to supplement the characterization data in previous chapters by highlighting the high conductivity and current-carrying capacity of the deposited layer. This is most appropriately demonstrated through the design, fabrication, and characterization of a low-power, high-current device. The chosen device is demonstrated via a multi-layer, thick-film, flexible electromagnetic MEMS microactuator that is not easily fabricated using existing methods. For reference, the advantages of multi-layer devices in general are discussed in Section 3.1.3, along with an examination of existing techniques for multi-layer device fabrication. The advantage of multi-layer fabrication for the device presented in this chapter is the potential for increased magnetic field generation. In fabricating the actuator, we also introduce a novel process variation enabling aligned, multi-layer devices with integrated ferromagnetic NCP components.

The multi-layer electromagnetic actuator presented in this chapter produces large magnetic fields over short periods and can be readily integrated into microfluidic, MEMS and LOC devices. While previous studies have shown that magnetic microactuators are well suited for use in various MEMS applications, low output forces and actuator deflections have resulted in relatively few commercially successful devices. In an effort to increase actuator deflections, several studies have shown that high current pulses over shorter periods can produce relatively large magnetic fields in both non-planar [175] [176] and planar [177] coil designs. Such large magnitude fields enable applications where high magnetic fields are required, such as the magnetization of thin-films [178]. Studies have also shown that the addition of heat sink structures to the actuator coils can enable increased currents due to superior heat dissipation and

reduction of the mechanical stresses produced by magnetic pressure [179]. In this thesis, heat sink structures and short current pulses, similar to those demonstrated in previous studies, are combined to maximize the magnetic field generated within a planar coil actuator design fabricated using the newly developed process.

A significant portion of this chapter is dedicated to the simulation and characterization of the proposed actuator from a performance perspective. However, it is important to understand that the primary benefit of our device compared to existing technology relates to the fabrication process. In contrast to the actuators presented in existing studies [155] [158], our process allows for fully-flexible, multi-layer device fabrication. Along with the possibility of integrating NCP processes and fabricating on wearable substrates, this enables an entirely new application space for integrated electromagnetic actuators in flexible and wearable electronics. This process could also be adapted to multi-layer, polymer-based (flexible) LOC and microfluidics applications. We are unaware of existing process technologies that enable similar levels of integration combined with electromagnetic actuation.

Section 6.1 provides a background of electromagnetic MEMS microactuators and a motivation for the design presented in this thesis. Section 6.2 specifies the design of a single planar coil used in this thesis, both with and without heat sinking fins. Section 6.2 also provides a brief motivation for the simulation and empirical studies presented in Section 6.3 and Section 6.4, respectively. The simulation calculations (Section 6.3) show that heat-sinking structures (also called fins) effectively dissipate heat from the coil, preventing thermal damage in the coil and enabling larger coil currents. Cooling due to the presence of heat sinking features is particularly evident for long duration current pulses and at steady-state. Geometric variation in terms of coil width and radius of curvature is also performed to study the effect of coil geometry in this application. The maximum current that can be applied in short duration pulses and at steady-state is simulated and used to compare each of the studied geometries. Overall, the coils with fins are found to produce a magnetic field that is three to six times the field produced by coils without fins at steady-state. This relative advantage is found to decrease as the input voltage period is decreased. All simulations are carried out using COMSOL Multiphysics finite element analysis software. Section 6.4 describes the physical actuator

fabrication, driver circuit design, and magnetic field sensor calibration. The characterization and analysis of the magnetic field produced by the fabricated actuator is presented in Section 6.5. A discussion of these results and a comparison to the simulation study is presented in Section 6.6.

6.1. Electromagnetic MEMS Actuators

MEMS are applied to a wide variety of scientific and engineering problems. MEMS-based applications such as chemical sensors [180], sequencing the human genome [181], the manipulation of biological cells [182], polymerase chain reaction [183], and capillary electrophoresis [184] demonstrate not only the academic importance of these systems, but also their commercial potential. Unfortunately, although many microactuators are studied in academia, relatively few have found commercial success. To increase commercial success, improvements must be made to low actuation forces and displacements, and to the cost and complexity of fabrication. Within the Microinstrumentation Laboratory (UIL) and Reconfigurable Computing Laboratory (RCL) at Simon Fraser University (SFU), we study magnetic actuation schemes that produce relatively large deflections and that can be easily integrated into a variety of low-cost, large-scale fabrication schemes, particularly for use in microfluidic devices [7] [32] [130] [185] [186] [187]. Unfortunately, the common drawback in each of these studies is the lack of a miniaturized magnetic microactuator capable of producing large magnetic fields in the range of 100 mT.

Similar to the devices fabricated in the UIL and RCL, magnetic microactuators and systems (MAGMAS) in general have been used for a variety of applications and all share the same common requirement of an applied magnetic field for actuation [188] [189] [190]. This field can be generated either via an existing permanent magnetic or a current conducting coil, which can be planar or 3D. General-purpose actuators using external permanent magnets are integrated into a variety of applications [191] [192], while others are used for specific applications such as pumps [193] [194], particle sorters [195], and valves [196]. The incorporation of 3D electromagnetic coils is leading the effort to progress beyond the use of external

permanent magnets that can be large, expensive, and offer low control over magnetic field strength [197].

While the previously mentioned MAGMAS have shown that magnetic microactuators are useful in a variety of interesting applications, many suffer from a dependence on permanent magnets and large 3D coils that are not easily integrated into common microfabrication schemes. Most fabrication processes, particularly those that are suitable for large-scale, low-cost applications, are more suited to planar processes. In addition to providing a simpler fabrication process, planar coils are applicable to a wide variety of applications where there are constraints on device volume. Such constraints can be found, for example, in implantable nuclear magnetic resonance devices [198] [199]. In addition, planar coils are useful for measuring the deflections of membranes [200], as magnetic field sensors [201], and in magnetic bead transportation systems [202]. Although these devices show that magnetic microactuators based on planar coils are effective, they generally produce magnetic fields that are much weaker in comparison to alternative actuators using large external coils or permanent magnets. Generating large magnetic fields from a single planar coil remains an ongoing challenge in the field. One solution to this problem involves the use of pulsed, large magnitude currents in planar coils for short duration, large magnitude electromagnetic field generation [175] [176] [179].

A limitation in generating large magnetic fields is that large thermal stresses due to resistive heat loss in the conductor can lead to device failure. Electric current pulsing helps to overcome this problem, as the energy lost to resistive heating is proportional to the duration of the pulse. Another limitation is the energy required to formulate large magnetic fields. Although larger coils can withstand higher heating loads and mechanical stresses, they also require relatively large input energies. Since the magentostatic energy stored in a coil is proportional to its volume, the required input energy in a tens-of-microns scale device compared to a centimeter scale device can be reduced by a factor of over 100 [179].

In the case of a single planar coil with radius *r*, the magnetic flux density along the coil's central *z*-axis is expressed using the well-known Biot-Savart Law applied to planar coils:

$$B(z) = \frac{\mu_o}{4\pi} I \frac{2\pi r^2}{(r^2 + z^2)^{3/2}} \tag{18}$$

where *B* is the magnetic flux density, *I* is the input current, μ_o is the magnetic permeability constant, and *z* is the distance above the coil at its center. However, to account for coil thickness, inner radius, and outer radius, the magnetic field at the center of such a coil carrying a uniform current distribution is expressed as

$$B = \frac{\mu_o}{r_i} I \frac{F(\alpha, \beta)}{2(\alpha - 1)\beta} \tag{19}$$

where:

$$F(\alpha, \beta) = \beta \ln \frac{\alpha^2 + \sqrt{\alpha^2 + \beta^2}}{1 + \sqrt{1 + \beta^2}} \tag{20}$$

is a geometrical component of the coil dimensions, with $\alpha = r_o/r_i$ and $\beta = t/2r_i$. Here, r_o and r_i are the outer and inner radius of the coil respectively, and t is the coil thickness [179]. An additional equation approximates the maximum pulse duration of an applied current that will achieve a specified magnetic field intensity while ensuring that the device temperature does not increase beyond a given limit due to the resistive heating of the coil [179]. If the actuator is well defined, meaning that the component has been fully designed and the mechanical response to magnetic fields is known, this equation can be used to generate a set of magnetic-field-pulse-duration pairs that may be input into the mechanical model to determine device actuation. For a given mechanical system, an optimal field-duration pair will lead to the largest actuator

deflection. However, this type of analysis is beyond the scope of this thesis, as discussed in Section 6.3.3.

6.2. Coil Design

In this section, we focus on the design of planer coils with heat sinking fins. These fins allow for increased input currents and generated magnetic fields, similar to the actuator designs found in other pulsed magnetic field approaches [175] [176] [179]. Although the heat-sinking fin design concept is previously demonstrated, the effects of the incorporating fins have not been characterized through experiment or through simulation.

In this thesis we hope to analyze the effects of fins in two ways. First, we aim to determine the degree to which the magnetic field can be increased in finned versus clean designs before device failure. This is done for both steady-state and pulsed currents. Second, we wish to gain insight into how actuators of various dimensions compare to each other across the two designs. Specifically, we wish to compare the maximum magnetic fields produced by finned and clean designs with varying trace widths, *w,* and radius, *r*. Wider conductors can accommodate more current, but the additional current that flows farther from the coil center contributes less to the magnetic field, and it may be possible to determine an optimal trace width. To compare the maximum magnetic field produced by fin designs versus clean designs, several coil geometries of varying dimensions are simulated. The selection of widths and radii is somewhat arbitrary. However, the widths and radii are consistent with the feature sizes presented in previous chapters this thesis.

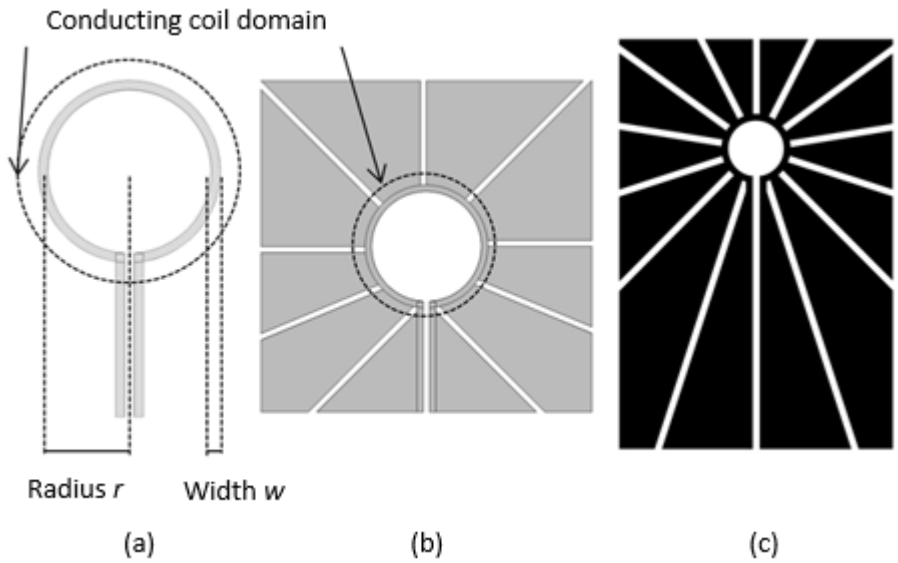


Figure 62. (a) Clean and (b) finned coil designs used in simulation. The coil geometries are described by the parameters *r* and *w*, representing the radius and width respectively. (c) Mask pattern used to fabricate the finned coil used in characterization experiments [31].

The general design of the planar coils used in this chapter is shown in Figure 62. Note that the geometry in Figure 62(a) has no heat-sinking features, and is referred to as the 'clean' design. Figure 62(b) has heat-sinking features, and is referred to as the 'finned' design. The parameters defining these geometries are the conductor width, *w*, and the radius of the conducting coil domain, *r*, which are both shown in Figure 62(a). The values for *r* and *w* vary across simulations, and are specified in the relevant subsections in Section 6.3. The widths used during simulation in this chapter form a subset of the set of widths tested during the characterization of feature size in Chapter 3. Similarly, all radii used during simulation correspond to values used during strain tests in Chapter 5.

In contrast to the many geometries tested in simulation, only a single geometry is fabricated (Section 6.4.2) and characterized (Section 6.5) using the masking pattern shown in Figure 62(c). The geometric parameters, *r* and *w,* selected for device fabrication are discussed in Section 6.4. The thickness of the coils in both simulation and fabrication corresponds the deposition thickness found in Section 4.2.2, which is 70 μm.

6.3. Simulation

The simulations presented in this section explore various combinations of the parameters *r* and *w* for both clean and finned designs to analyse the relationship between coil geometry and the maximum generated magnetic field. The maximum magnetic field is found by first identifying the maximum voltage that can be applied to a given geometry. The maximum voltage is determined by applying a steadily increasing input voltage until the point of failure is reached when the coil temperature exceeds a specific limit. In this thesis, the temperature limit corresponding to the point of failure is defined as the melting point of copper, T_C, which is 1358 K [203].

The first set of simulations characterize the relationship between coil width and the maximum steady-state magnetic field by keeping the coil radius constant while varying the width. The relationship between coil radius and maximum steady-state magnetic field is studied in a similar fashion in the second set of simulations. After the steady-state simulations, input pulses are examined. In the third set of simulations, 100 μs voltage pulses are applied to coils with varying widths to understand the effect of coil width on pulsed magnetic field magnitude. In the fourth set of simulations, input voltages with pulse periods ranging from 1 μs to 100 ms are applied to a single coil geometry to characterize the effect of pulse period on the magnitude of the generated magnetic field.

All voltage pulses are applied as constant (step) inputs. Current pulses with a realistic profile and time constant will be applied in future work to better represent a physical system. It is envisioned that this will involve the use of a transient circuit model to evaluate time dependent currents, with the coils attached to the circuit. This is in contrast to the current model, which simply utilizes boundary conditions at the coil terminals to apply input voltage (shown later in Section 6.3.4, Figure 66). It is also appropriate to study the frequency response of the coils in future work, as the coils' self-inductance and resistance may set an upper frequency limit to the minimum pulse duration that can be applied.

6.3.1. Simulation Model

All simulations are performed using COMSOL version 5.2. Two different COMSOL models are required for our simulations. The first model uses the Joule Heating Multiphysics interface, which includes the Electric Currents and Heat Transfer in Solids interfaces. This model is used to determine the maximum input voltage that can be applied across the actuator before the device experiences failure due to overheating. To find the point of failure, a linear interpolation is performed using multiple simulation results and the maximum applied voltage input is calculated. The interpolation method is discussed further in Section 6.3.6. The maximum input voltages determined in the first model are then applied as inputs to a second model to determine the resulting maximum generated magnetic field.

Joule Heating Model

The first model utilizes the Joule Heating Multiphysics interface, which includes the Electric Currents and Heat Transfer in Solids interfaces. This model is used to determine the maximum input voltage that can be applied across the electromagnetic actuator before the device experiences failure due to overheating. The following Multiphysics Interfaces are used to couple the Electric Currents Interface to the Heat Transfer in Solids Interface: the Electromagnetic Heat Source Interface (applied to all domains), the Boundary Electromagnetic Heat Source Interface (applied to all boundaries), and the Temperature Coupling Interface (not applicable to domains or boundaries).

Table 17. Material properties of copper used in the COMSOL Joule Heating model. All properties are independent of temperature and time.

Material Property	Value	Units
Electrical Conductivity	5.998×10^7	S/m
Heat Capacity	385	$J/(K \cdot kg)$
Relative Permittivity	1	$1(Unitless)$
Density	8700	kg/m^3
Thermal Conductivity	400	$W/(m \cdot K)$

Table 17 lists the material properties of copper used in the Joule Heating model. These material properties are applied by default in COMSOL. Copper is the only material used in this model, and is applied to every domain of the geometry. These properties are independent of both temperature and time. In future studies, the copper material properties should be modeled assuming a linearized resistivity to improve the accuracy of the simulation.

In the Electric Currents Interface, currents are conserved in all domains according to the current conservation equations given in Equations 21 to 23, which apply to stationary studies:

$$\nabla \cdot \boldsymbol{J} = Q_j \tag{21}$$

$$\boldsymbol{J} = \sigma \boldsymbol{E} + \boldsymbol{J_e} \tag{22}$$

$$\boldsymbol{E} = -\nabla V \tag{23}$$

where $\boldsymbol{J}$ is the electric current density, Q_j is a distributed current source, $\boldsymbol{E}$ is the electric field, $\boldsymbol{J_e}$ is the externally generated current, and V is the electric potential. Equation 22 is modified for time-dependent studies, as shown in Equation 24:

$$\boldsymbol{J} = (\sigma + \varepsilon_0 \varepsilon_r \frac{\partial}{\partial t})\boldsymbol{E} + \boldsymbol{J_e} \tag{24}$$

where ε_0 is the permittivity of free space and ε_r is the relative permittivity of copper. All surface boundaries are electrically insulated (the normal current density is zero) except for the terminals shown in Figure 66, which are the input voltage terminals. The initial value of the electric potential is zero in all domains. Further details regarding the Electric Currents Interface are found in the accompanying COMSOL software user's guide for this module [204].

In the Heat Transfer in Solids Interface, heat transfer is defined in all domains according to the heat transfer equations given in Equation 25 and Equation 26, which apply to stationary studies:

$$\rho C_p \boldsymbol{u} \cdot \nabla T + \nabla \cdot \boldsymbol{q} = Q + Q_{ted} \tag{25}$$

$$\boldsymbol{q} = -k \nabla T \tag{26}$$

where ρ is the material density, C_p is the heat capacity at constant pressure, $\boldsymbol{u}$ is the velocity vector, T is the absolute temperature, $\boldsymbol{q}$ is the heat flux by conduction, Q is the heat source due to resistive heating, Q_{ted} is the heat source due to thermoelastic damping, and k is the thermal conductivity of the material. Equation 25 is modified for time-dependent studies, as shown in Equation 27:

$$\rho C_p \frac{\partial T}{\partial t} + \rho C_p \boldsymbol{u} \cdot \nabla T + \nabla \cdot \boldsymbol{q} = Q + Q_{ted} \tag{27}$$

The initial temperature value in all domains is 293.15 K. Heat flux at all boundaries is purely convective, though future studies should include radiative heat transfer to improve the accuracy of simulation results. This study uses a heat transfer coefficient of 5 W/(m^2·K), which is the heat transfer coefficient for air used in the Heating Circuit demonstration application included with this version of COMSOL (5.2a). A constant pressure of one atmosphere is maintained in both interfaces. Further details regarding the Heat Transfer in Solids Interface are found in the accompanying COMSOL software user's guide for this module [205].

Magnetic and Electric Fields Model

The second model uses the Magnetic and Electric Fields interface to simulate the magnetic field produced by the coils using the maximum voltages found using the Joule Heating model. Both models use the built-in copper material definition given in Table 17,

while the second model also uses the built-in material definition for air shown in Table 18. All material properties are independent of both temperature and time.

Table 18. Material properties of air used in the COMSOL Magnetic and Electric Fields model. All properties are independent of temperature and time.

Material Property	Value	Units
Electrical Conductivity	10	S/m
Relative Permeability	1	$1\ (Unitless)$
Relative Permittivity	1	$1\ (Unitless)$

In the Electric and Magnetic Fields Interface, Ampère's law and the equation of continuity for the electric current are provided by Equations 28 to 32, which apply to both stationary and time-dependent studies:

$$\nabla \times \mathbf{H} = \boldsymbol{J} \tag{28}$$

$$\boldsymbol{B} = \boldsymbol{\nabla} \times \boldsymbol{A} \tag{29}$$

$$\boldsymbol{J} = \sigma \boldsymbol{E} \tag{30}$$

$$\nabla \cdot \boldsymbol{J} = 0 \tag{31}$$

$$\boldsymbol{E} = -\nabla V \tag{32}$$

where $\mathbf{H}$ is the magnetic field, $\boldsymbol{B}$ is the magnetic flux density, $\boldsymbol{A}$ is the magnetic potential, and all remaining quantities are as previously defined. A constant temperature of 293.15 K is maintained for all simulations using this model. A constant pressure of one atmosphere is also maintained. The outer surface boundaries defined by the bounding box of air (see Figure 64) are magnetically insulated such that the tangential components of the magnetic field potential are zero. The outer surface boundaries are

also electrically insulated such that the normal current density is zero, except for the terminals used to apply voltage. The initial electric and magnetic field potentials are zero in all domains.

Mesh Generation

Meshes in both the stationary and time-dependent studies are generated with the Predefined Normal size and the Free Tetrahedral shape provided in COMSOL. The maximum and minimum element sizes of the generated meshes vary among the actuator geometries defined in Section 6.3.2. The maximum and minimum element sizes of the mesh generated for models having a 500 μm trace width are 2.48 mm and 464 μm, respectively. For models having a 200 μm trace width, the maximum and minimum element sizes are 2.45 mm and 441 μm, respectively. In the magnetic and electric fields model, a bounding box of air is defined, which contains the magnetic fields generated by the actuator. The maximum element size contained in the bounding box is 3.00 mm. Convergence of the various solutions calculated by COMSOL has not been evaluated using different mesh sizes. However, a Predefined Normal mesh size is chosen for the initial simulations presented in this thesis based on the speculation that this mesh size generally results in acceptable model accuracy and moderate simulation run times. Confirmation that the results are independent of the mesh size must be provided in future studies to validate the results presented in this chapter.

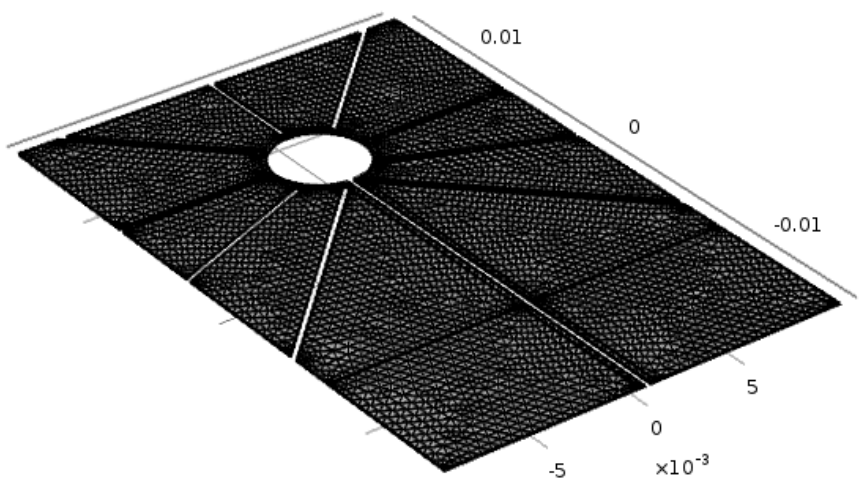


Figure 63. Mesh applied to a coil in the COMSOL Joule Heating interface, used to find the maximum applied voltage.

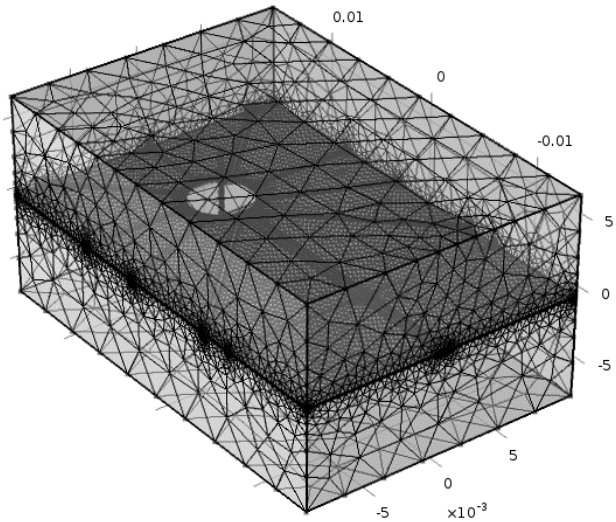


Figure 64. Mesh applied to a coil in the COMSOL Electric and Magnetic Fields interface, used to find the maximum generated magnetic field.

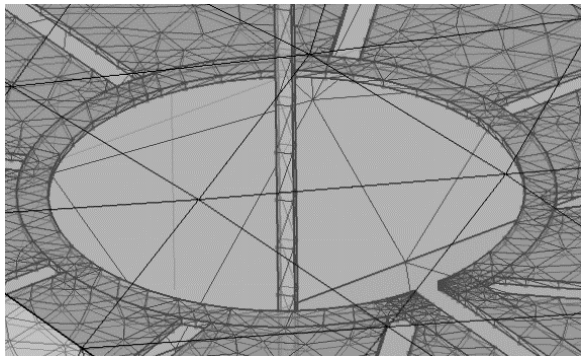


Figure 65. Detailed view of the coil center from Figure 64, revealing the cylinder defined to acquire precise measurements of the magnetic field at the coil center.

Figure 63 and Figure 64 show generated meshes for geometries having a 200 μm trace width in both models. Note that the second model (Figure 64) used to simulate magnetic fields requires a bounding box of air as a medium to contain the generated magnetic fields. Within the bounding box shown in Figure 64, an inner cylinder is defined at the coil center to provide a finer mesh for precise measurements at the probe locations. This is shown more clearly in Figure 65.

Details regarding the selection of the geometric parameters (*r* and *w*) used in simulation are given in the next section (Section 6.3.2), while the selection of input pulse duration is discussed in Section 6.3.3. Section 6.3.4 and Section 6.3.5 outline the procedure for measuring the maximum applied voltage and the resulting generated magnetic field, respectively. Section 6.3.6 presents the results of the simulations and an accompanying analysis.

6.3.2. Actuator Geometry

The selection of geometries reflects a desire to maintain consistency between the structures fabricated in Section 4.1.4 and Section 5.1.1 in terms of radius of curvature and trace width. In addition, the geometries are selected to allow for an analysis of the generated magnetic field verses trace width, radius, and duration of voltage input. In Section 4.2.3, we show that reliable fabrication cannot be guaranteed for trace widths equal to or below 100 μm using our proposed process. In addition, the simulations performed in this section represent relatively stressful conditions that would likely result in high failure rates for 100 μm coils. Therefore, coil widths of 100 μm are assumed to be insufficiently reliable, and widths of 200 μm, 300 μm, and 500 μm are simulated.

Table 19. Actuator geometry labels for each combination of parameters used in simulation.

Geometry	Radius (mm)	Width (μm)	Conductance (S)	
			Finned	Clean
1	2.283	200	93.0	21.1
2	2.283	300	107	31.5
3	2.283	500	133	52.4
4	0.915	200	123	24.7
5	1.371	200	108	23.3
6	1.827	200	98.8	22.1
7	2.657	200	89.4	20.2

Simulations that isolate the relationship between magnetic field and a variable trace width require a constant radius of curvature. Although there are no hard constraints on the selection of a coil radius, the radius is selected based on a scale factor

determined in Section 5.1.1 ($w/r = 0.219$). Assuming a trace width of 500 μm and a scale factor of 0.219, a radius of 2.283 mm is used. Simulations that isolate the relationship between magnetic field and a radius of curvature require a constant trace width. This characterization is performed using a trace width of 200 μm while the radius varies from 0.913 mm (applying the scale factor to 200 μm trace widths) to 2.657 mm.

Each simulated geometry is given a label for convenient referencing. These geometry labels are collectively shown in Table 19 along with the values of *w* and *r*. For reference, the conductance of each geometry is also shown for finned and clean designs. The conductance is given directly in COMSOL as a global evaluation for each geometry. All simulations use an actuator thickness of 70 μm, which is the resulting copper thickness after 4 hours of electrodeposition found in Section 4.2.2.

Due to the repetitive nature of the simulations, parametric sweeps are performed within COMSOL for the width, radius, and applied voltage parameters at each stage. This requires that the geometry is defined in the COMSOL model builder as a function of the parameters *w* and *r*. In this manner, all structures can be simulated with an arbitrary set of dimensions and input voltages in a single simulation run.

6.3.3. Outline of Simulations

The performance of the actuators is analyzed under both steady-state and pulsed input conditions. The first set of simulations use steady-state inputs, while the second set of simulations use high-magnitude, short-duration voltage pulses to increase the maximum magnetic field within the actuator. In both cases, device failure eventually occurs due to Joule heating within the coil, which is proportional to the magnitude and duration of the applied current. Therefore, higher magnitude current pulses require shorter durations.

Table 20. Description of simulation sets, with the corresponding parameters used in each simulation. All simulations are performed for finned and clean designs, with an actuator thickness of 70 μm.

Simulation Set		Duration (μs)	Radius (mm)	Width (μm)
1. Magnetic field versus trace width: steady-state	1.1	N/A	2.283	200
	1.2	N/A	2.283	300
	1.3	N/A	2.283	500
2. Magnetic field versus radius: steady-state	2.1	N/A	0.915	200
	2.2	N/A	1.371	200
	2.3	N/A	1.827	200
	2.4	N/A	2.283	200
	2.5	N/A	2.657	200
3. Magnetic field versus trace width: pulsed input	3.1	100	2.283	200
	3.2	100	2.283	300
	3.3	100	2.283	500
4. Magnetic field versus pulse duration	4.1	1	2.283	500
	4.2	10	2.283	500
	4.3	10^2	2.283	500
	4.4	10^3	2.283	500
	4.5	10^4	2.283	500
	4.6	10^5	2.283	500

The deflection of a typical device, such as a cantilever-based electromagnetic valve, is dependent on both the magnitude and duration of an applied pulse. However, determining an optimized magnitude-duration pair is non-trivial, and requires a detailed design of all actuator components, along with an analysis of the mechanical response of the deflecting component to an applied magnetic field. In this thesis, we do not study a deflecting component, and have therefore made the choice to study a voltage pulse durations of 100 μs. Although somewhat arbitrary, a 100 μs duration pulse lies between one second and tens of nanoseconds, which are assumed to bound the mechanical time constant of any physical actuator we might potentially fabricate.

In addition to exploring 100 μs duration pulses, we also wish to characterize the effect of varying the pulse duration versus the generated magnetic field magnitude. Therefore, a single geometry is simulated with input pulse durations ranging from 1 μs to

0.1 s, with pulse durations incrementing by a factor of 10 in each set of simulations. Given the motivations outlined thus far in Section 6.3, a summary of the simulations performed in this section are given in Table 20.

6.3.4. Maximum Input Voltage

In the first COMSOL model, voltages are applied to each structure and the corresponding temperature is calculated. Voltage is applied across the terminals of each structure through constant voltage boundary conditions in the COMSOL model. The temperature is recorded using a COMSOL probe measuring the maximum temperature within the conducting coil domain. Temperature in all other domains is not recorded. Increasing the applied voltage eventually leads to device failure due to unsustainable temperatures within the conductor, similar to the failure of a fuse. This critical temperature is defined as the melting point of copper, T_C, which is equal to 1358 K [203].

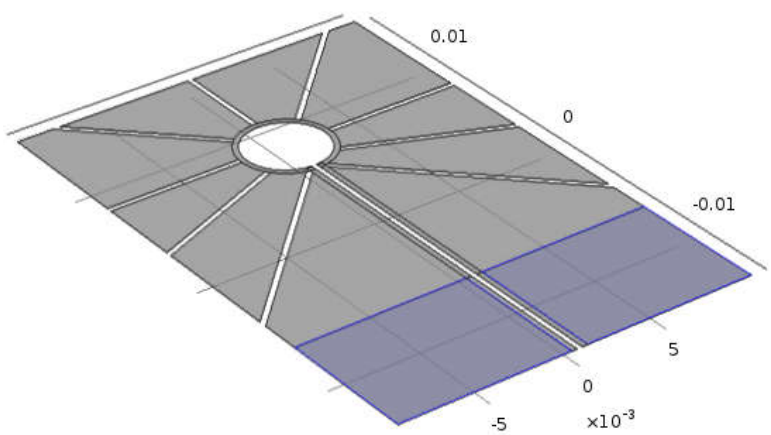


Figure 66. Input voltages are applied across the highlighted boundaries in the COMSOL models, as shown in this finned geometry.

The voltage terminals (applied as boundary conditions in COMSOL) are shown for an example geometry in Figure 66 as highlighted surfaces. This terminal area is meant to approximate the contact area of the terminals where input voltage is applied in the fabricated device.

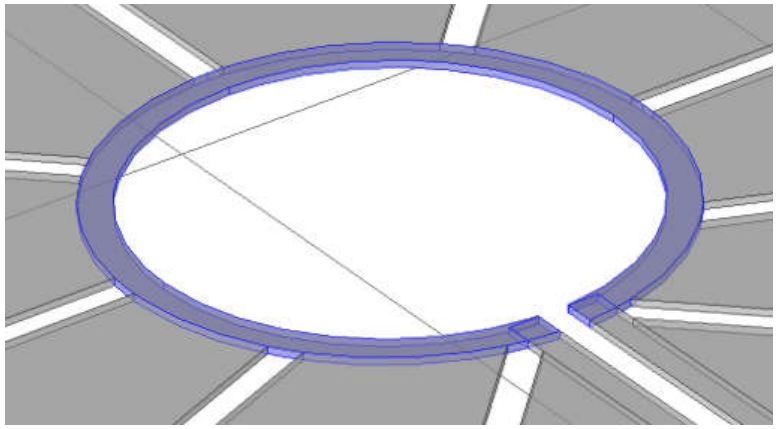


Figure 67. The highlighted coil domain in the COMSOL model is probed for maximum temperature during simulations.

Figure 67 shows the highlighted area corresponding to the coil domain where the maximum temperature is recorded with a COMSOL probe. The critical voltage is approximated by a linear fit of multiple simulated voltages that result in maximum coil temperatures near T_C. We call this critical voltage approximation the linear estimator (LE). As a condition to ensure accuracy, we suggest that the percent difference of the linear estimator (LEPD) be kept to less than 5%. We define the LEPD as the average percent difference of the nearest simulated temperature above (T^+) and below (T^-) the critical temperature compared to the critical temperature itself, as stated in Equation 33:

$$LEPD \equiv \frac{T^+ + T^-}{2T_C} \leq 0.05. \tag{33}$$

In addition to applied voltage, the average current density within the coil is also recorded using an additional probe in the conducting coil domain. In contrast to the maximum temperature probe, the average current density probe only measures current vectors normal to the coil path. The current density results are discussed qualitatively in Section 6.3.6, during an analysis of the overall simulation results.

6.3.5. Maximum Magnetic Field

The critical voltages found using the methods described in Section 6.3.4 are applied to the coils in a second COMSOL model to determine the resulting magnetic field. The simulated magnetic field is measured at several positions above the center of the coil using a single-point COMSOL measurement probe. The coil is oriented such that the top and bottom face of the planar coil are parallel to the x-y plane, and the central plane of the coil (between the top and bottom face) rests at a height of z = 0.

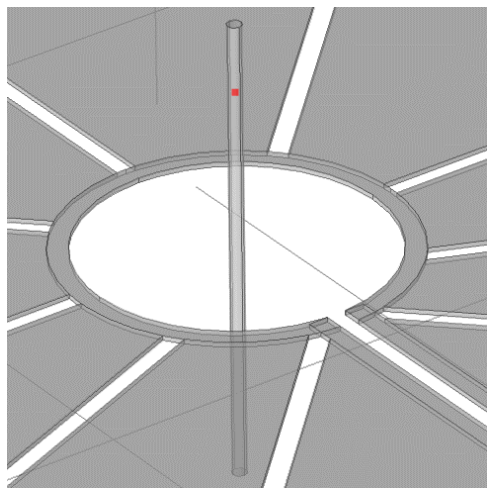


Figure 68. An example point probe (red dot) used to measure the magnetic field above the coil center during simulation.

Measurement probes are placed directly above and in-line with the coil center. The locations of the measurement probes along the z-axis are 0 µm, +/- 35 µm (in line with the top and bottom face of the 70 µm thick actuator), and N*5*70 µm, where N = 1, 2, 3,…, 10. An example probe is shown in Figure 68 as a red dot above the coil center.

6.3.6. Results and Analysis

This section contains an analysis of the results obtained from the simulations defined in Table 20. This includes a summary of the high-level results for these simulations, as well as a detailed analysis of the relationship between the maximum generated magnetic field and the actuator coil geometry. The relationship between the maximum generated magnetic field and input pulse duration for a single coil geometry is

also studied. However, the main contribution is an analysis of the maximum magnetic field that can be generated using the actuator designs presented in Figure 62.

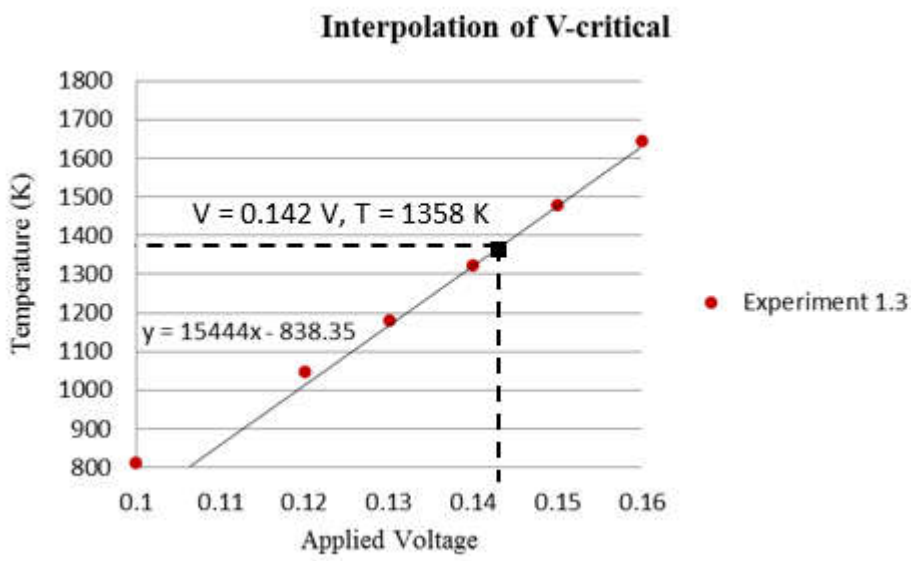


Figure 69. Maximum steady-state voltage interpolated from several simulations of temperature versus voltage (from Simulation 1.3, finned).

Figure 69 shows an example of the linear interpolation method used to determine the maximum applied voltage that can be applied to a given geometry under the specified input voltage conditions. This particular example corresponds to Simulation 1.3 in Table 20, which describes a steady-state voltage applied to Geometry 3. A linear of fit of the two data points corresponding to 0.14 V and 0.15 V applied is also shown, and is used to calculate a maximum applied voltage of 0.142 V corresponding to a temperature of 1358 K. This example is represents the only simulation that results in an LEPD greater than 5%. Despite the LEPD being greater than 5%, the data in Figure 69 shows a region of interpolation that is satisfactorily linear. The error is therefore assumed to be acceptable.

Table 21. Results for the simulations defined in Table 20. The maximum magnetic field measured at the coil center is shown, along with the LEPD for each interpolation used to calculate the applied voltage.

Simulation Set		V_{max}		B (mT) (z = 0)		LEPD (%)	
		Finned	*Clean*	*Finned*	*Clean*	*Finned*	*Clean*
1. *B* versus *w* (steady-state)	1.1	0.244	0.182	4.73	0.986	1.3	0.9
	1.2	0.228	0.165	5.06	1.25	1.4	1.0
	1.3	0.205	0.142	5.50	1.70	4.0	5.5
2. *B* versus *r* (steady-state)	2.1	0.220	0.175	13.8	2.49	0.4	0.5
	2.2	0.233	0.179	8.67	1.66	3.6	0.5
	2.3	0.241	0.182	6.10	1.27	0.3	0.4
	2.4	0.244	0.182	4.73	0.986	1.3	0.9
	2.5	0.250	0.189	4.03	0.829	3.3	2.2
3. *B* versus *w* (pulsed)	3.1	6.82	29.8	132	162	2.4	0.5
	3.2	7.91	27.2	176	206	2.0	0.6
	3.3	9.80	25.6	263	301	0.9	3.4
4. *B* versus Δt_{pulse}	4.1	62.1	153	1666	1790	1.40	1.13
	4.2	23.1	59.7	620	701	3.65	2.93
	4.3	9.80	25.6	263	301	0.88	3.39
	4.4	4.34	10.5	117	124	1.99	4.16
	4.5	1.91	3.40	51.4	39.9	4.58	4.92
	4.6	1.07	1.03	28.7	12.1	1.54	1.61

Table 21 shows the high level results describing the maximum magnetic field that can be generated. These results are calculated in COMSOL according the simulation conditions described in Table 20. The maximum input voltage is calculated through the process described in Section 6.3.4, while the resulting magnetic field is calculated according the process described in Section 6.3.5. The LEPD corresponding to the interpolation of applied voltages calculated in each simulation is also shown. Although the applied voltage is less meaningful than the magnetic field results (voltage is highly dependent on conductance), the voltages applied in all simulations are also included in Table 21 for reference.

Simulation Set 1 and 2: Steady-state magnetic field

Several observations are immediately apparent from an analysis of the results in Table 21. The first observation is that, at steady-state, the finned designs are capable of producing magnetic fields roughly five times larger than those produced by clean designs. However, for pulsed magnetic fields, the clean designs appear to produce larger fields for short duration pulses. For longer pulses (greater than 100 μs), the finned designs produce larger fields. This interesting result, which is not found in existing studies, is discussed further in Section 6.3.6.

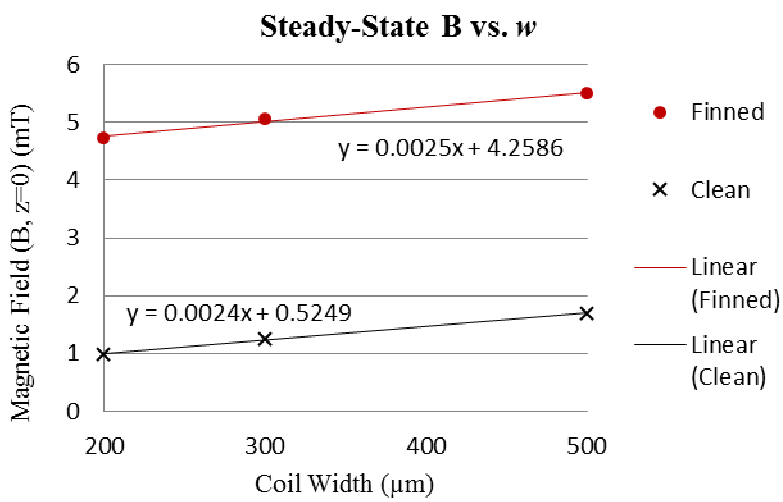


Figure 70. Steady-state magnetic field versus coil width for finned and clean designs.

The second observation is that the magnetic field increases proportionally to trace width at steady-state. This relationship is illustrated in Figure 70, which shows the results for both finned and clean designs. A linear fit of the data for both designs is also shown, though it is not certain whether the relationship is truly linear given the limited set of data. Additional simulations could be performed in future work to assess the linearity of the relationship.

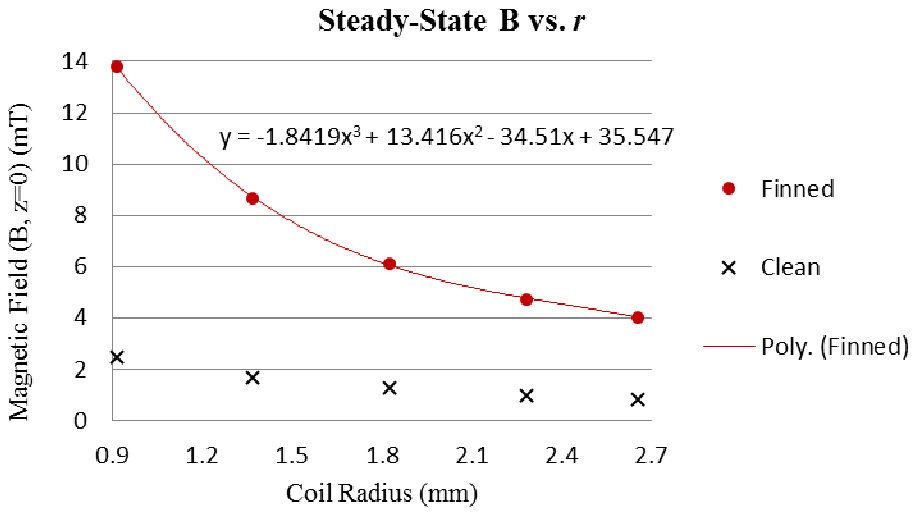


Figure 71. Steady-state magnetic field versus coil radius for finned and clean designs.

The third observation is that, given a constant trace width, the coil radius is inversely proportional to the generated magnetic field. This relationship is illustrated for both finned and clean designs in Figure 71, and is especially visible for finned geometries. Qualitatively, this relationship is not surprising as Equation 20 dictates that the magnetic field is proportional to the inverse of the radius. In addition, the *ratio* of the generated magnetic fields between finned and clean designs also appears inversely proportional to the radius. This observation follows from the fact that the increase in magnetic field as the radius decreases in clean geometries is relatively flat compared to finned geometries. This result is not immediately obvious from the equations presented thus far. We speculate that one contributing factor to this effect is that the ratio of cooling fin area to empty space within the design increases as the coil radius decreases. For large radii, the cooling fins become less dominant and the simulations for finned designs approach the corresponding clean design simulations. Still, it may be that small radii result in large magnetic fields for finned designs regardless of fin extension. Further analysis of this effect is left to future work. Note that a third-order polynomial trend line is also generated for the finned data in Figure 71, which is used during the discussion in Section 6.6.

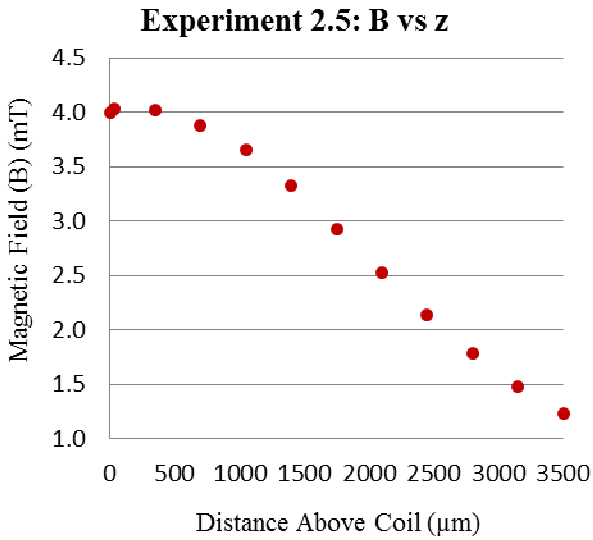


Figure 72. Simulation results for the magnetic field measured at various distances above the coil center in Simulation 2.5.

For reference, a single simulation of magnetic field versus distance above the coil is shown in Figure 72. This data corresponds to the finned design in Simulation 2.5. The general shape of the magnetic field is similar in all simulations, and aligns well with the commonly understood shape of magnetic fields that follow Equation 30.

Simulation Set 3 and 4: Pulsed magnetic field

Simulation Sets 3 and 4 correspond to pulsed input voltages as opposed to steady-state. In Simulation Set 3, it is interesting to note that, in contrast to the steady-state results, the clean structures are found to generate stronger magnetic fields compared to the finned structures for 100 μs pulse durations. This result is explored further in Simulation Set 4 through the variation of input pulse duration.

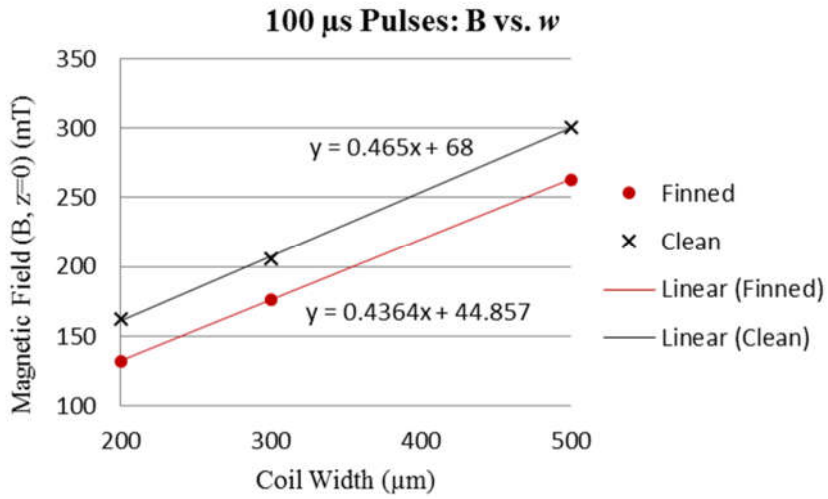


Figure 73. Magnetic field versus coil width for 100 µs voltage pulses.

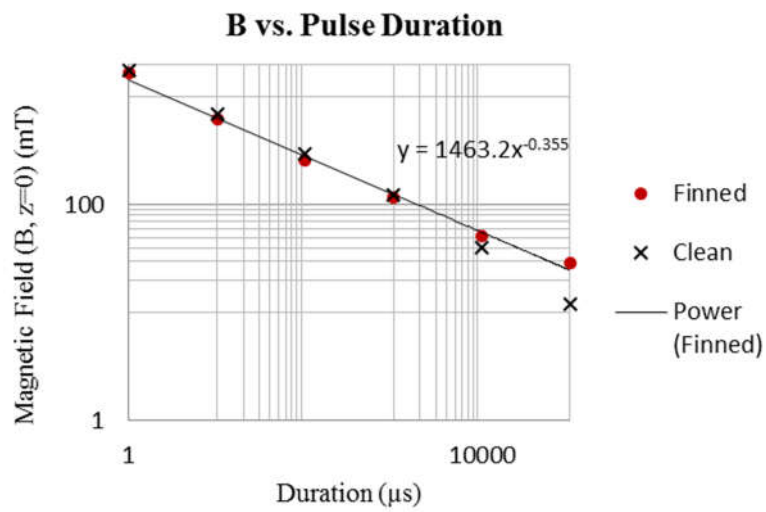


Figure 74. Magnetic field versus pulse duration for voltage pulses ranging from 1 µs to 100 ms.

The magnetic field versus coil width for 100 µs pulses is shown in Figure 73, while the magnetic field strength versus pulse duration for a single coil geometry (Geometry 3) is shown in Figure 74. A linear trend is added to both sets of data in Figure 73, though once again it is uncertain whether this relationship is truly linear given the limited set of data. Note the logarithmic scale on both the x- and y-axis in Figure 74. A trend line is also generated for the finned data in Figure 74, which is used during the

discussion in Section 6.6. We observe that for both finned and clean designs, the magnetic field is inversely proportional to pulse duration. For relatively short durations (less than 1 ms), the clean design outperforms the finned design once again, though the performances are relatively close. However, as the pulse duration increases, the finned design approaches and surpasses the performance of the clean design. This change in relative performance as the pulse lengths increase is expected, as the magnetic fields produced by the finned design at steady-state are several times those produced by the clean design.

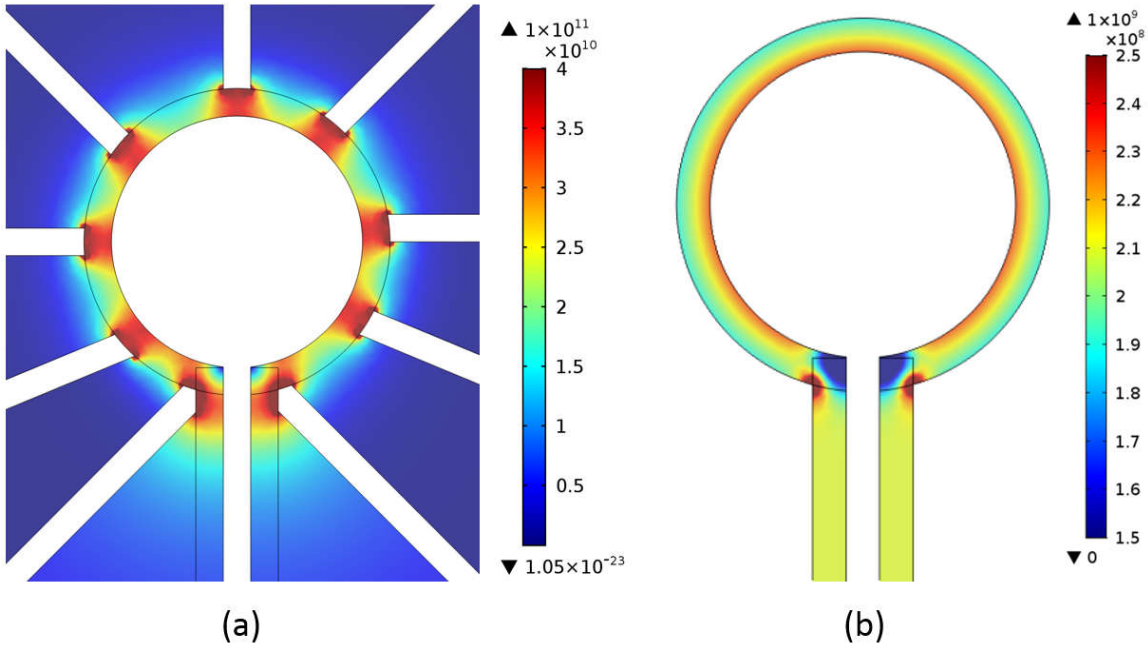


Figure 75. Current density distribution for finned and clean Geometry 3 designs given (a) a 10.2 V pulse after 100 μs and (b) a steady-state input of 0.147 V. Current density scales are in A/m^2.

The surprising result that clean designs outperform finned designs for short duration pulses is not fully understood, and is not explored with further simulation in this thesis. However, we suspect that this effect is related to heat dissipation within the actuator. Figure 75 shows a typical current density distribution in (a) finned, pulsed designs and (b) clean, steady-state designs. These current density distributions are qualitatively the same for steady-state and pulsed voltages in general. Regardless of input voltage profile, the current density displays some interesting gradients at the junction of each fin to the conducting coil domain in Figure 75(a). A similar gradient is

seen in the clean design (b) where the coil domain meets the electrical contact lines. These junction areas represent current pinching points, indicated by a red colour shift, while the outer fin areas represent current spreading points, indicated by a blue colour shift. It is at these junction areas that device failure eventually occurs due to excessive temperatures within the coil.

It is important to note that this study does not include an investigation into the effects of electromigration, which could lead to decreased performance and an increased failure rate in the long-term. The median time to failure of an electronic device due to electromigration is inversely proportional to the square of the current density within a conductor (approximately) [206]. The maximum current densities calculated in steady-state and pulsed simulations are 1.36×10^{9} A/m^2 and 1.67×10^{11} A/m^2, respectively. These represent relatively large current densities, and it is prudent, therefore, to study the long term effects of electromigration in future work.

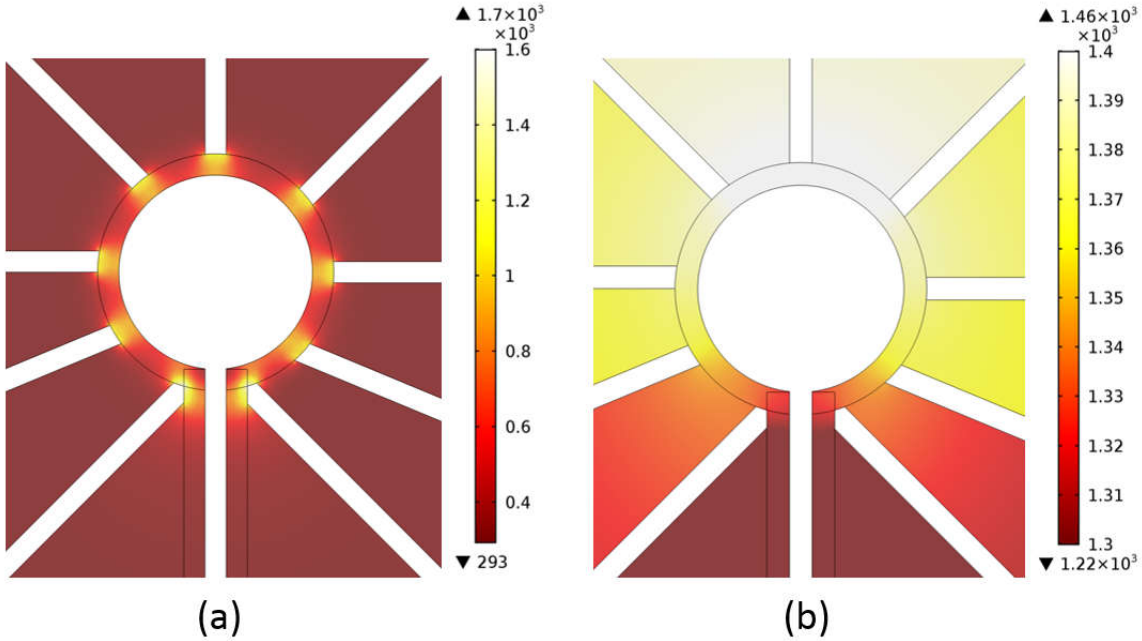


Figure 76. Temperature distribution (degrees K) for Geometry 3 (finned) given (a) a 10.2 V pulse after 100 μs and (b) a steady-state input of 2.1 V.

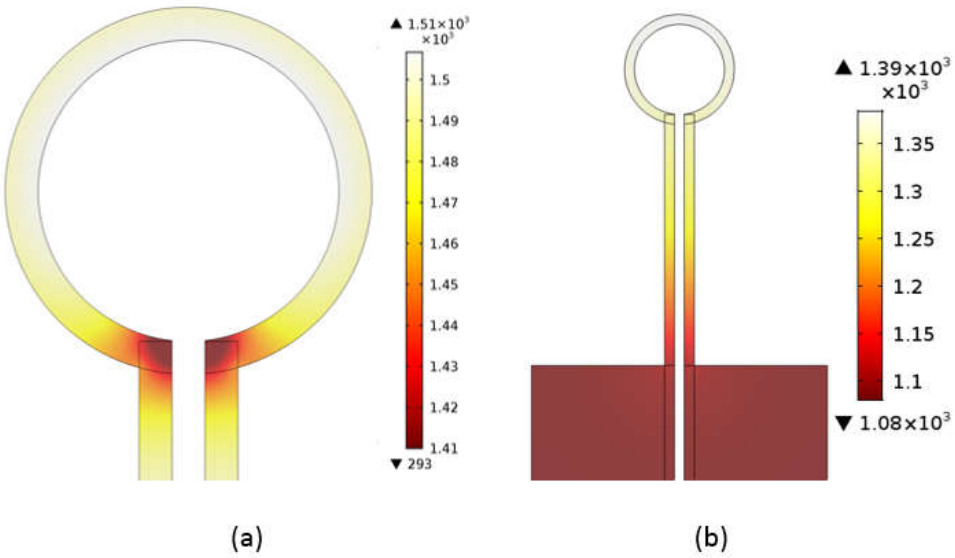


Figure 77. Temperature distribution (degrees K) for Geometry 3 (clean) given (a) a 3.46 V pulse after 10 ms and (b) a steady-state input of 0.147 V.

The typical temperature distribution for finned designs is shown in Figure 76, under both (a) pulsed and (b) steady-state conditions. The distribution for clean designs is similarly shown in Figure 77. For short duration pulses, the resulting temperature distribution resembles the current density distribution, and higher temperatures are concentrated at the junction areas as seen in Figure 76(a) and Figure 77(a). For steady-state voltages, the temperature has additional time to spread evenly across the conductor area, as seen in Figure 76(b) and Figure 77(b). This temperature spreading acts to remove the stress due to high temperatures at the junction areas.

In contrast to the finned geometry, the clean geometry has only two junction areas where the coil domain meets the contact lines, and there are no other current pinching points. In addition, the junction area on the finned design where the coil domain meets the contact lines has additional junctions nearby due to fins contacting the coil domain. We suspect that the additional junction areas lead to increased temperatures for finned designs relative to clean designs, and may be responsible for the decreased performance of finned designs under short-duration input pulse conditions. We also suspect that the definition of the geometry within COMSOL, which has resulted in prominent areas of current pinching, may play a significant role in the observed decrease in performance of finned designs for short pulse periods. Regardless of this

interesting result, there are several important conclusions regarding strategies to maximize the generated magnetic field. The most effective methods to maximize the generated magnetic field are to minimize both the coil radius and pulse duration. Increasing coil width also results in stronger magnetic fields, but to a lesser extent, and it is unclear whether this trend continues for trace widths beyond the scales measured here.

6.4. Experiment

The main objective of this section is to describe the fabrication and experimental procedure used to characterize an aligned, multi-layer electromagnetic actuator. The actuator is fabricated using a modified version of the process presented in Section 3.2. A characterization and analysis of the magnetic field produced by the actuator is presented in Section 6.5, while this section describes the actuator fabrication (Section 6.4.2), current pulse driver circuit (Section 6.4.3), and magnetic field sensor calibration (Section 6.4.4). A discussion of the results and a comparison to the simulation study is presented in Section 6.6. Note that the physical characterization study and the simulation study are independent, as the actuator design is not selected based on simulation results. However, the simulation results do allow for a comparison with the actuator characterization, and an analysis of the actuator performance in Section 6.6.

6.4.1. Equipment and Materials

The equipment and materials used to fabricate the actuator are the same as those discussed in Section 3.2. In addition, the experiments involve a voltage-pulse driver circuit and a magnetic field sensing coil, which is also called a search coil. The driver circuit components include four 0.2 Ω resistors (PF2203-0R2F1, Riedon), two 120 μF, 450 V aluminum electrolytic capacitors (FUCP2W121MHD, Nichicon), four silicon controlled rectifiers (SCR) (SK055R, Littelfuse, Inc.), and four 3 A, 1000 V avalanche diodes (SF5408-TR, Vishay Semiconductor). The magnetic field sensor and calibration assembly includes a NanoAct magnetic actuator coil and two MiniAct magnetic actuator coils, all manufactured by Plantraco, Ltd. During the magnetic field sensor characterization, voltage measurements are acquired using a National

Instruments PCI data acquisition card (NI PCI-6071E), and magnetic fields are measured with a F.W. Bell Hall Effect 5100 Series Tesla Meter from Pacific Scientific OECO. The driver circuit is charged using a Stanford Research Systems Model PS310 1250V DC power supply, and the magnetic field sensing coil output voltage is measured, recorded, and exported using a Rohde & Schwarz model HMO1002 oscilloscope.

6.4.2. Fabrication

One of the most significant advantages of the newly-developed fabrication process is that multi-layer devices are easily fabricated using a modified version of the base process. The modified process includes the utilization of pattern transfer 'stamps' and inter-layer alignment features to achieve an aligned, multi-layer device. The modified process also allows functional materials to be incorporated into the device design via the alignment features.

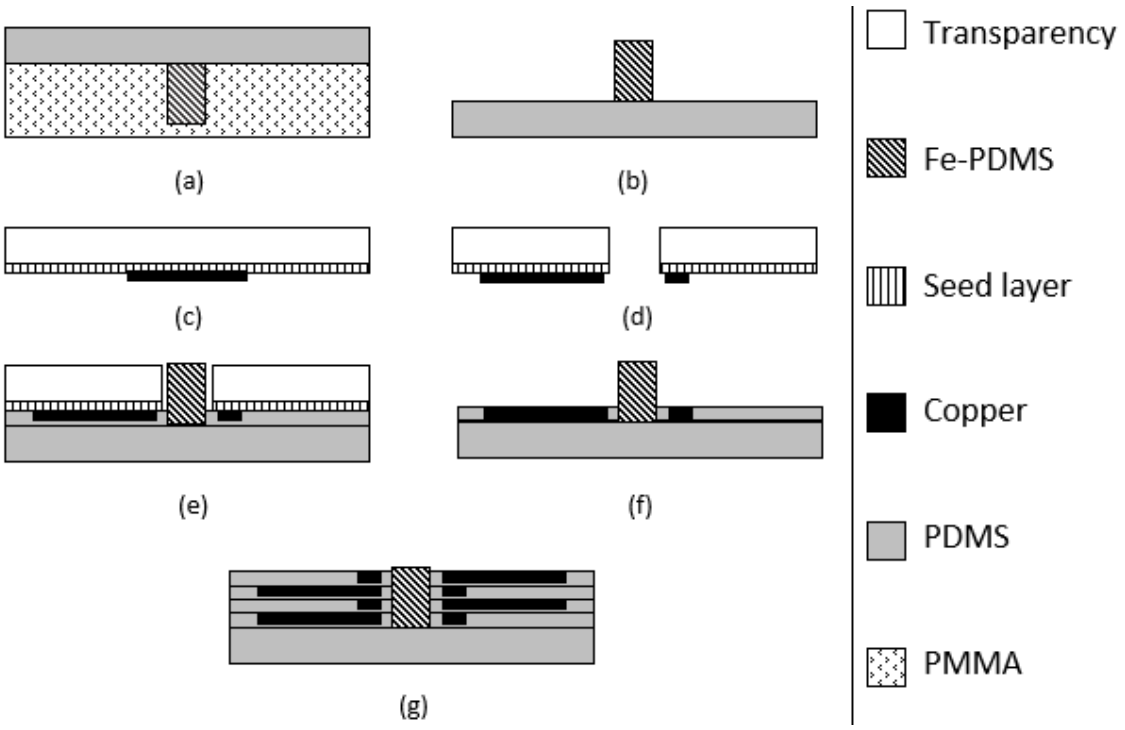


Figure 78. Modified process for an aligned multi-layer device with integrated NCP. (a, b) The Fe-PDMS alignment post is fabricated via micromolding, and (c, d) the stamp is fabricated with a matching alignment hole. (e, f) A single layer is transferred and aligned via stamping. (g) Successive stamping produces a multi-layer device [31].

The process modifications in this section are based off the low-cost, large-scale, micropattern transfer process outlined in Section 3.2. Similar to the modified process for wearable fabrics (shown in Section 5.2.1), copper patterns are once again 'stamped' onto a target substrate, with PDMS acting to facilitate delamination from the seed and adhesion to the target. In the case of a multi-layer device, PDMS additionally provides electrical insulation between conductive layers. The process is further modified to produce aligned metallization layers and to incorporate NCPs. The stacking and alignment process is shown in Figure 78. In (a) and (b), an Fe-PDMS NCP post is fabricated on a PDMS substrate using an NCP micromolding process that is demonstrated in existing studies [71]. In (c) and (d), the deposited copper stamp is modified with a laser-cut alignment hole to facilitate alignment between layers using the corresponding Fe-PDMS alignment post. The alignment hole is cut before electrodeposition using a CO_2 laser apparatus [71]. The stamping of a single layer through the alignment post is illustrated in (e) and (f), while (g) shows the result of stacking four aligned metal layers. Note that the rotation of layers is not constrained by the alignment post in this process. To further align and constrain rotation between layers, multiple alignment features are required.

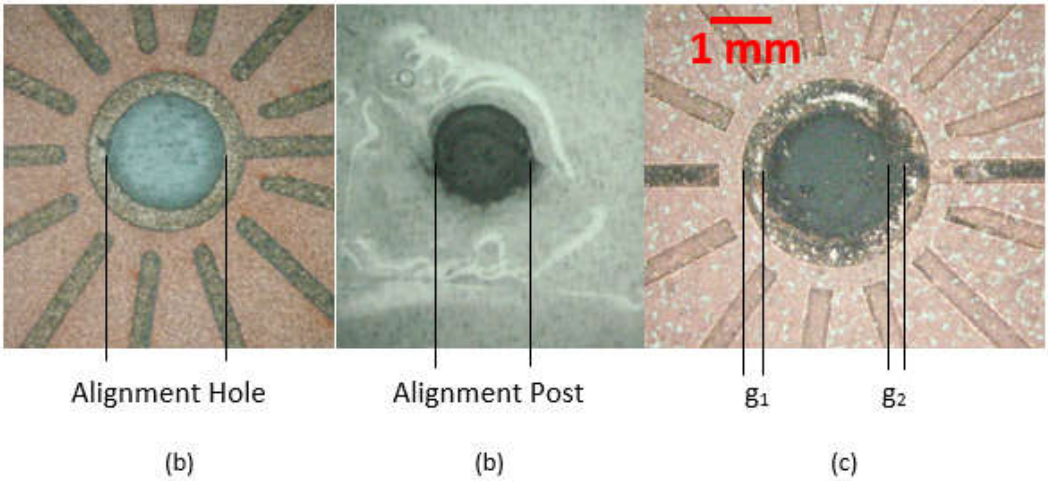


Figure 79. (a) A single-layer stamp with alignment hole and (b) an Fe-PDMS alignment post. (c) The single-layer stamps are transferred successively to create a well-aligned multi-layer device. The gap between the top metallization layer and the alignment hole, g_1, and the gap between the Fe-PDMS alignment post and the stamp alignment hole, g_2, are also visible [31].

In the electromagnetic actuator presented in this thesis, the inter-layer alignment features are composed of a ferromagnetic PDMS (Fe-PDMS) NCP, potentially allowing for increased magnetic field generation in the multi-layer coils. Although the effect of the Fe-PDMS NCP on the generated magnetic field is not characterized in this thesis, it is well known that an iron core component significantly increases the magnitude of magnetic field generation within a conductive coil. However, it is not certain whether the Fe-PDMS NCP, as opposed to bulk iron, will result in increased magnetic field generation. A single layer of the actuator fabricated in this thesis has a finned coil design (as shown in Section 6.2, Figure 62).

Figure 79 shows (a) a single-layer stamp and laser-cut alignment hole, (b) the Fe-PDMS alignment post, and (c) the stamped layer after deposition onto the substrate. The gap, g_1, between the top metallization layer and the alignment hole in the assembled device is identifiable by the residual traces of seed layer (c) that have been transferred to the PDMS during the curing process. This residual seed layer is undesired. However, as demonstrated in Section 4.2.3, the residual seed is found to be effectively non-conducive and does not result in electrical shorts across conducting patterns, even between traces spaced as near as 50-75 μm. The gap between the Fe-PDMS alignment post and the stamp alignment hole, g_2, is also easily visible in Figure 79(c). Both gaps appear even around the alignment feature, indicating that the alignment process is qualitatively effective. In addition, each layer is electrically isolated, with an open circuit load detected when measuring across all combinations of layers using a handheld DMM. Within a single layer, for all layers, a resistance of 0.0 Ω is measured end to end using the DMM. The metallization layers are, therefore, well-isolated and highly conductive, though the resistance cannot be measured effectively with the DMM.

The laser-cut alignment hole in the transparency substrate is required to have a slightly smaller radius than the deposited coil (g_1 in Figure 79). Therefore, the laser-cut radius is 80% smaller than the coil radius to allow a degree of tolerance. Similarly, the corresponding Fe-PDMS post must have a smaller radius than the alignment hole (g_2 in Figure 79), and is designed to be 80% smaller than the alignment hole. Note that the geometry fabricated here has the same definition as Geometry 3 defined in Table 19.

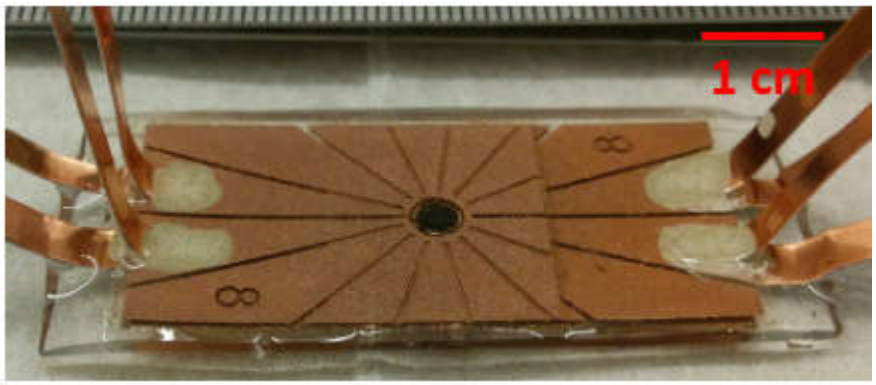


Figure 80. A four-layer electromagnetic actuator incorporating an Fe-PDMS NCP post for increased magnetic field generation and to facilitate alignment between layers [31].

A completed electromagnetic actuator component has four metallization layers as shown in Figure 80. Successive layers are rotated 180˚ to minimize asymmetries in the generated magnetic field [177]. A 130g mass is placed on top of the stamp during the transfer step, which results in an unknown PDMS thickness between metallization layers. To determine this thickness, the height of the Fe-PDMS substrate is measured before transferring any metallization layers and after all four layers have been transferred. The resulting average PDMS thickness between layers is found to be 246 µm. In future work, this thickness may be optimized to keep the conductive layers as close as possible while maintaining electrical isolation. We speculate that this optimization will result in stronger magnetic field generation within the actuator, as the intensity of the magnetic field decreases as the distance to each coil layer increases. Electrical connectivity to each layer is established using copper tape (3M™) and a silver-based conductive paint. In total, two four-layer actuator components are fabricated, assembled, and characterized. The characterization is performed in Section 6.5.2.

It is important to note that qualitative observations of the multi-layer device show that it is noticeably less flexible than a single deposition layer. In future work, the impact of multiple layers on the mechanics of the deposited films must be explored. As mentioned in Section 2.1.1, a given failure in the deposited films depends on both film adhesion and layer geometry [47]. Therefore, the careful selection and arrangement of materials in multi-layer devices is critical to achieving device reliability, and must be explored in future work.

6.4.3. Pulsed Driver Circuit

A resistor-inductor-capacitor (RLC) circuit, commonly used in pulsed field generation experiments [175] [176] [178] [179], drives the actuator shown in Figure 80.

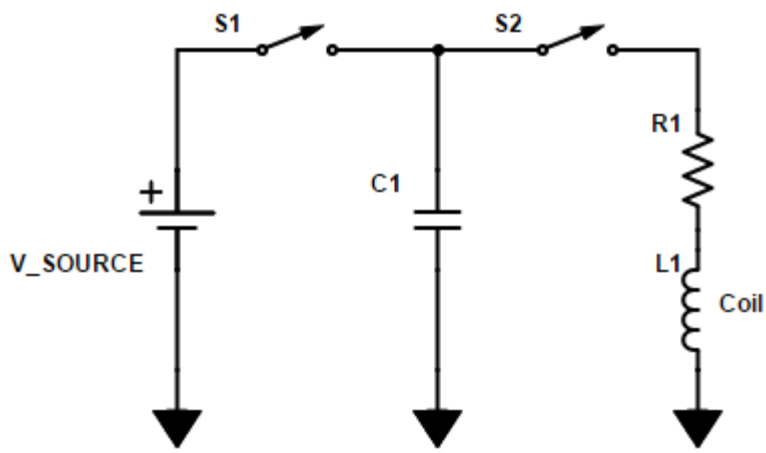


Figure 81. Simple example of an RLC current pulse generator circuit.

An example of a simple current pulse driver circuit is shown in Figure 81. During the charging phase, the input switch (S1) is closed, allowing a DC voltage source (V_SOURCE) to charge the input capacitor (C1). When the capacitor is fully charged, S1 is opened and C1 remains charged to the voltage delivered by V_SOURCE. To discharge the circuit, a second switch (S2) is closed, allowing the charge stored in C1 to flow through the load resistor (R1) and inductive coil (L1). The resonant frequency and current pulse period produced by this circuit, ω_o and T_o, respectively, are given by Equation 34:

$$\omega_o = {}^{1}/_{\sqrt{LC}}, \qquad T_o = \pi\sqrt{LC} \tag{34}$$

where L and C represent the circuit inductance and capacitance, respectively. RLC circuits are known to oscillate, with the value of resistor R1 being proportional to the circuit oscillation dampening.

Several modifications to the basic circuit in Figure 81 are commonly applied to enhance device performance and provide circuit protection. These enhancements typically relate to the switching mechanism that initiates the current pulse discharge, and to protection elements that are placed in parallel to the inductive actuator coil. Assuming high-voltage, short-period input pulses are required, a manual triggering switch (S2 in Figure 81) is insufficient. Applications typically use a silicon switch, or silicon controlled rectifier (SCR) [176] [178].

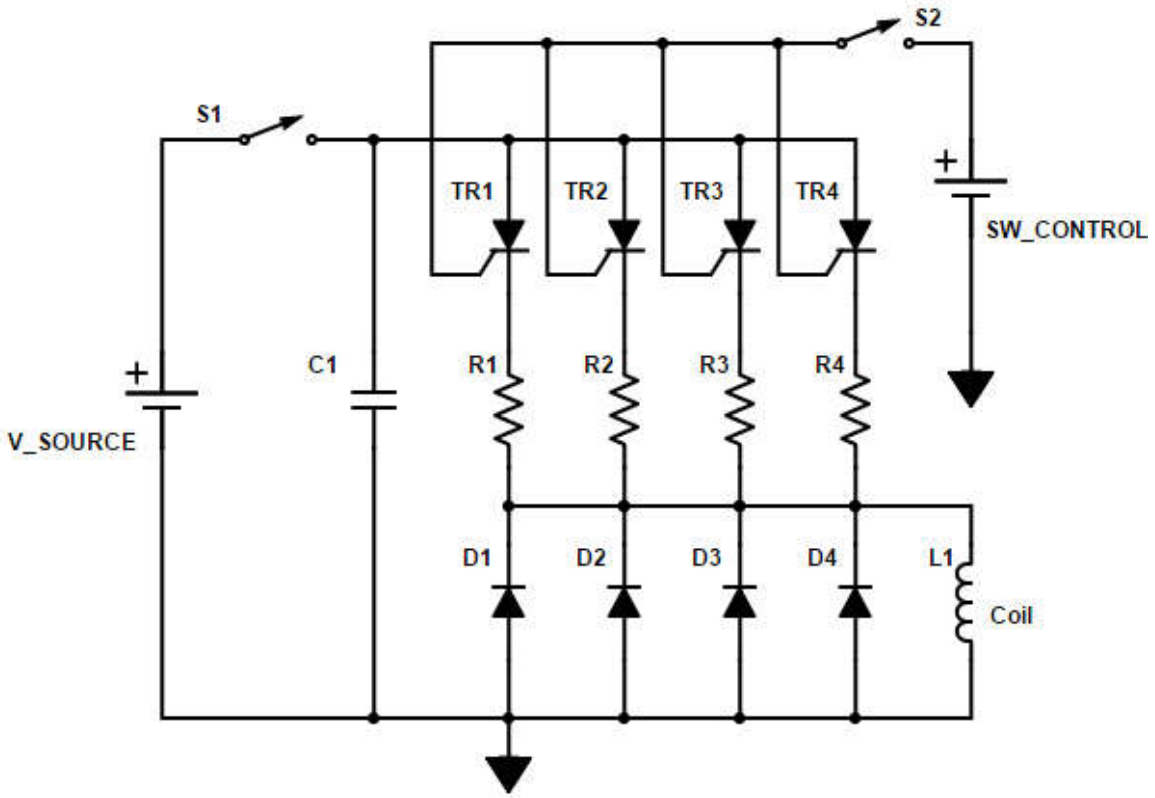


Figure 82. Schematic of the circuit used in this experiment.

SCRs are available in high-voltage and high-current varieties, and are easily triggered (allowing current to flow) using a relatively low voltage control pulse applied to a third terminal. An advantage of the SCR is that it can be activated at any time using the control terminal, allowing for configurations with intelligent computer control. Alternative switching solutions, such as spark gaps [175] [179], are more robust but can only by triggered by breaching the spark-gap input voltage threshold. In comparison, SCRs can be triggered with a wide range of input voltages. In circuits where large

currents are discharged, SCRs are often placed in parallel.The parallel SCRs used in this circuit are labelled TR1 to TR4 in Figure 82.

Figure 82 shows the modified circuit used in this experiment to deliver the voltage pulse. A manual switch, S1, is initially closed and a power supply, V_SOURCE, is used to charge the capacitor, C1. After the capacitor is charged, S1 is opened to disconnect the power supply, and the SCRs are triggered to deliver the pulse. The SCRs are triggered by a simple 1 V voltage step provided by SW_CONTROL (a current limited power supply), which is connected to the SCR gate terminal by pressing a push-button switch, S2. After the SCR is triggered and the input voltage pulse is delivered, a large negative potential is generated by the inductive coil that tends to resist the loss of current. As a result, large negative potentials can form across the SCRs, which tend to damage them immediately or over time. To protect against this situation, protection diodes, also called flyback diodes, are placed antiparallel to the coil [176] [178]. These are labelled D1 to D4 in Figure 82. This protects both the capacitor and SCR bank from the large induced reverse voltage by providing a path for the current to flow and snubbing the reverse voltage down to the diode voltage drop (less than 1 V).

Additional resistance is optionally added to the circuit to achieve the desirable input pulse shape and to protect the SCRs from large currents due to unsynchronized triggering. The additional resistances are labelled R1 to R4 in Figure 82. In the fabricated circuit, each of the parallel resistors has a value of 0.2 Ω. For pulsed electromagnetic actuators, a critically damped, or slightly overdamped, RLC circuit provides the ideal input pulse shape [176]. To achieve a critically damped circuit, the resistance, *R*, must satisfy Equation 35:

$$R = 2\sqrt{L/C} \tag{35}$$

To calculate the desired circuit resistance using Equation 35, the circuit capacitance and inductance must first be determined. The total inductance of the fabricated coil (shown in Figure 80 and labelled “L1” and “Coil” in Figure 82) is measured to be 85 μH using an LRC Bridge 2400 (Electro Scientific Industries, Inc.). This value is

verified experimentally by assembling a test RLC circuit using a known capacitor value and the fabricated coil. Using the RLC test circuit, the input frequency is adjusted until resonance is observed, and Equation 34 is used to calculate the inductance of the coil. With a known coil inductance, Equation 35 is used to calculate the required capacitance to achieve a target input pulse period. Note that the input pulse period corresponds to $T_o/2$, since the input voltage magnitude decreases significantly after the first half-wave period in an overdamped circuit. Rather than targeting a particular pulse period, two available 120 μF, 450 V aluminum capacitors are placed in series in the fabricated circuit. This results in a 60 μF, 900V equivalent capacitance, and allows for high voltage inputs. These are labelled together as C1 in Figure 82. The corresponding half wave input pulse period is calculated to be approximately 200 μs. Finally, a target resistance of 2.4 Ω is calculated using Equation 35 with the actual values for inductance (L1) and capacitance (C1).

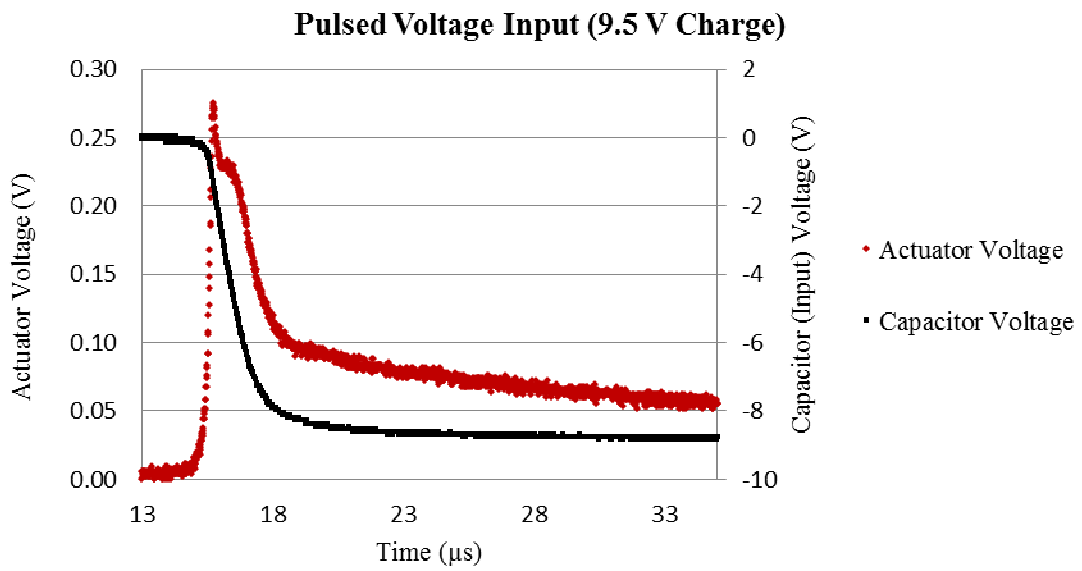


Figure 83. Voltage measured across the capacitor input and actuator coils during a discharge. The initial capacitor charge is 9.5V.

To determine the actual circuit resistance, the resistance of the actuator is first measured by applying a constant 2.83 mV input across the coil. A coil current of 188 mA is measured, resulting in a calculated resistance of approximately 15 mΩ, while the LRC bridge provides a measurement of 20 mΩ. The resistance of the entire circuit (also provided by the LRC Bridge) is 80 mΩ, and is measured by shorting the SCR anodes to

cathodes and opening the circuit between the input capacitors. Although the resistances of both the coil and the full circuit are measured, this does not necessarily reveal the peak coil voltage to capacitor charge ratio. To determine this ratio, we record both the coil and capacitor voltage during a capacitor discharge, as shown in Figure 83. From Figure 83, it can be observed that a peak voltage of 276 mV is measured across the coil during an 8.9 V capacitor discharge. This means that for every volt stored in the capacitors, 30.9 mV is delivered to the actuator. At this point we may add resistance to the circuit to meet the target resistance of 2.4 Ω for a critically damped circuit. However, due to the relatively low peak voltages delivered to the coil and an input pulse profile that is already satisfactory, no additional resistance is added. This also ensures that sufficiently large voltages are provided to the actuator.

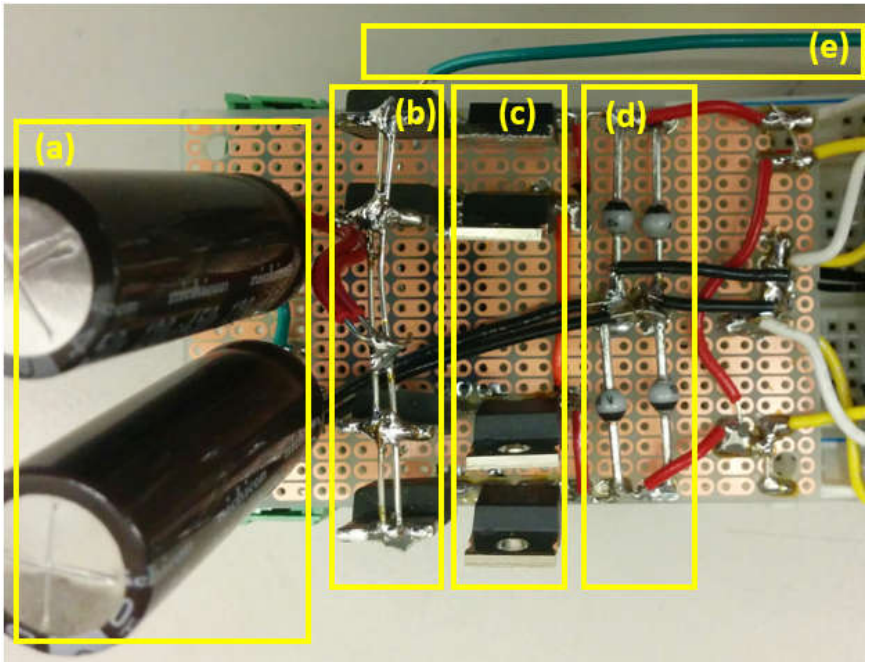


Figure 84. Voltage pulse driver circuit. (a) Current flows from the capacitor bank, (b) through the SCRs and (c) resistors before reaching the actuator. (d) Flyback diodes provide protection, and (e) the SCRs are triggered by an external voltage source.

The completed driver circuit is shown in Figure 84. The visible components include (a) the capacitor bank, (b) SCR array, (c) SCR-series resistors, (d) flyback diodes, and (e) an external connection for triggering the SCRs. The actuator is positioned to the right of the circuit (outside the image). With the completion of the

pulsed driver circuit, a magnetic field sensor (used to measure the generated magnetic field) must be constructed and characterized.

6.4.4. Magnetic Field Sensor

Pulsed magnetic fields are often measured using a calibrated secondary sensing coil, also known as a search coil [179] [176]. In this experiment, the search coil method is used for convenience. While the search coil method is convenient, more sophisticated methods, such as the magneto-optic Kerr effect (MOKE) method [175], are able to provide improved accuracy. The magnitude of a magnetic field, *B,* is calculated by dividing the integral of the induced voltage in the search coil, ε, by the coil area, *A*, according to Equation 36 (Faraday's law of induction) [176]:

$$\varepsilon = -\frac{d\Phi_B}{dt} = -\frac{d(BA)}{dt} \tag{36}$$

Equation 36 can alternatively be expressed as Equation 37 for a changing magnetic field, *B*, and static coil area, *A*.

$$B(t_f) - B(t_i) = \frac{-\int_{t_i}^{t_f} \varepsilon dt}{A} \tag{37}$$

Equation 37 allows us to calculate the magnetic field produced by our fabricated actuator by integrating the induced voltage in the search coil over the pulsed magnetic field period. However, the use of this equation requires that the area of the search coil, *A*, be determined. While it is possible to calculate the area of a simple coil using known geometric parameters, the area of the search coil used in this thesis is determined empirically since the coil contains an unknown number of turns. Even in cases where there is a single turn in the coil, it is common practice to perform an empirical characterization of the effective coil area. To determine the effective area of the search coil, a series of known magnetic fields are established and the resulting voltage

response of the search coil is measured. The area of the coil is calculated using Equation 38, which follows from a simple rearrangement of Equation 37:

$$A = \frac{-\int_{t_i}^{t_f} \varepsilon dt}{B(t_f) - B(t_i)} \tag{38}$$

To characterize the search coil using Equation 38 requires that the coil be placed in known (uniform) initial and final magnetic fields. A Helmholtz coil pair, which produces a relatively large, uniform magnetic field between the two coils in the pair [177], is used to generate these known reference fields.

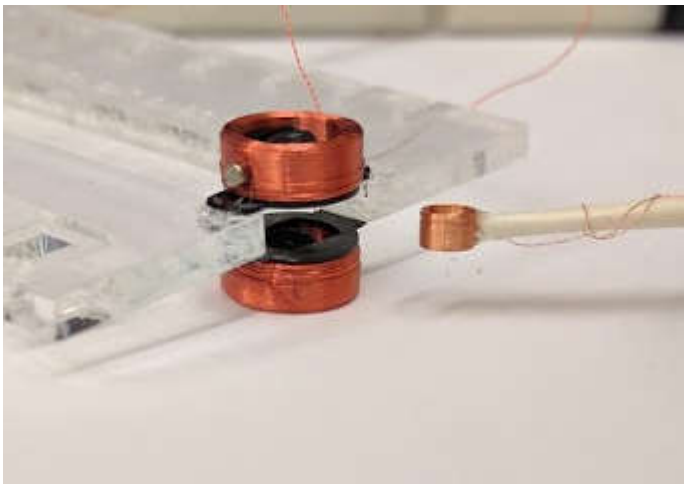


Figure 85. Helmholtz pair (left) and search coil (right) used to determine the search coil area, *A*.

The experimental configuration of the Helmholtz pair and search coil, both purchased from Plantraco, Ltd., is shown in Figure 85. Before using the Helmholtz coil pair to characterize the search coil, the pair is characterized to determine the generated magnetic field versus applied current. Currents between 50 mA to 200 mA are applied to the Helmholtz pair, and the resulting magnetic field is measured using a F.W. Bell Hall Effect 5100 Series Tesla Meter (Pacific Scientific OECO). This Tesla Meter is placed in the center of the coils and adjusted until a stable maximum value is recorded. This measurement is simplified by the fact that the field within the Helmholtz pair is relatively homogeneous [177].

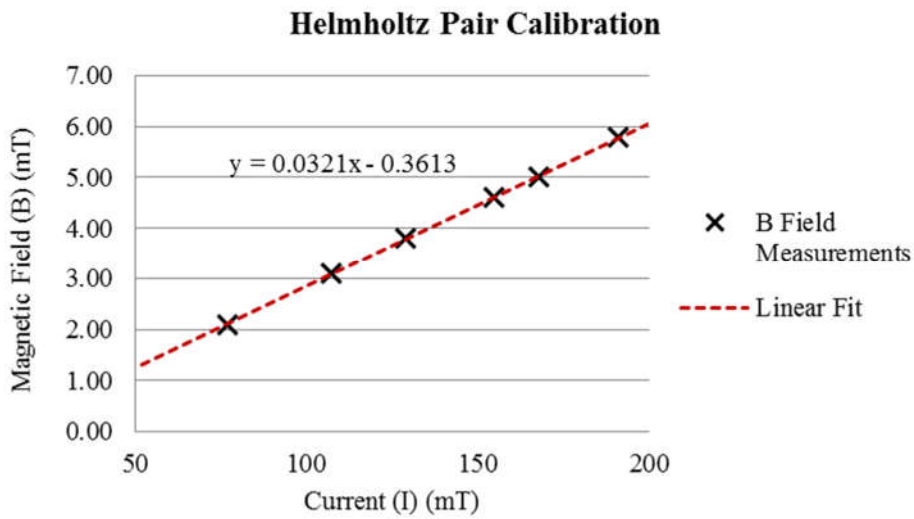


Figure 86. Characterization of generated magnetic field versus applied current in the Helmholtz pair.

Figure 86 shows the magnetic field measured with respect to the voltage applied to the Helmholtz pair. According to a linear fit of the experimental results shown in Figure 86, the coils produce approximately 32 mT per Amp applied. After the characterization of the magnetic field generated by the Helmholtz pair, the tesla meter is replaced with the search coil so that the effective area of the search coil can be determined experimentally.

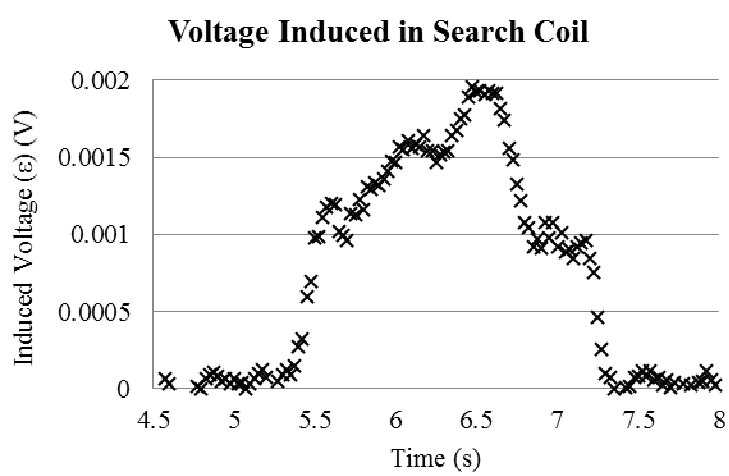


Figure 87. Single measurement of the induced voltage in the sensing coil while increasing the current in the Helmholtz pair from 2.6 mA to 65 mA.

A known current step is applied to the Helmholtz pair while the induced voltage in the search coil is recorded. An example measurement of the induced voltage is shown in Figure 87, where the applied current to the Helmholtz pair is increased from 2.6 mA to 65 mA over a period of two to three seconds. A simple inverting operational amplifier circuit with a gain of 254 is used during the acquisition of the data in Figure 87. The amplifier circuit is used to both amplify relatively small induced voltages, as well as to filter out high frequency noise in the search coil output. The voltage is integrated numerically using the well-known trapezoidal integral approximation shown in Equation 39.

$$\int_a^b F(x)dx \cong (b-a)\left[\frac{F(a)+F(b)}{2}\right] \tag{39}$$

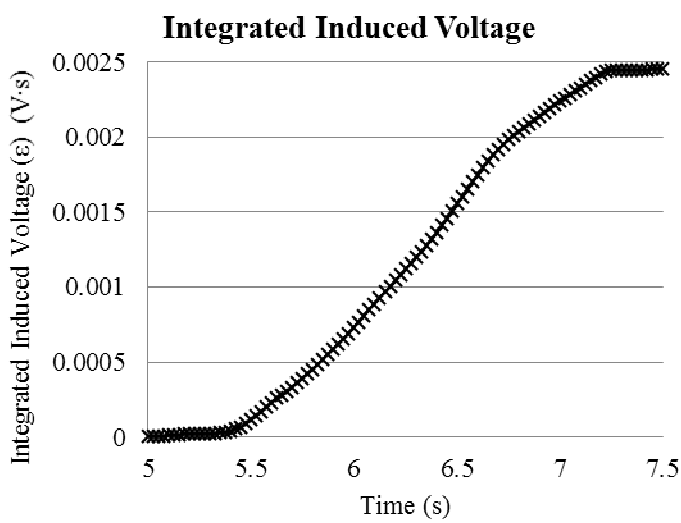


Figure 88. Integration by trapezoidal approximation of the measured induced voltage from Figure 87.

The integrated voltage corresponding to the applied current Figure 87 in is shown in Figure 88. Again, this data corresponds to an amplified signal with a gain of 254. Equation 38 is now used to determine the effective area of the search coil. The final integrated value in Figure 88 (approximately 0.00245 V·s) is divided by 254 (the voltage gain in the measurement circuit) and 1.64 mT (the difference of the magnetic fields measured at applied currents of 2.6 mA and 65 mA), resulting in an area of 58.7 cm^2.

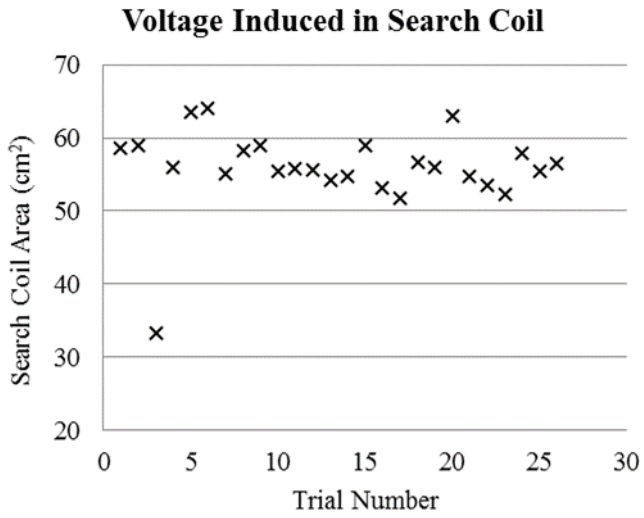


Figure 89. Effective search coil area measurement results.

This search coil area calculated from Figure 88 is shown as the first data point in Figure 89, while the remaining 25 data points correspond to repeated experiments with each current step ranging between 50 mA – 100 mA. The mean and standard error of the search coil area is calculated to be 55.8 +/- 1.1 cm^2. A single data point lies below 40 cm^2 and is included in the calculation of the sample mean, though it may be considered an outlier. Having a known value for the effective area of the search coil allows us to characterize the generated magnetic field of the fabricated actuator using Equation 37.

6.5. Experimental Results and Analysis

The first actuator measurements are acquired by applying constant (steady-state) currents to a single-layer device while measuring the voltage drift over time. The purpose of this measurement is to compare the relative ability of finned structures versus clean structures to dissipate heat at steady-state. The experiment does not involve the use of pulsed currents, or actuator design variation. In the second set of experiments, a multilayer, finned design is fabricated and subjected to voltage pulses of various magnitudes, which are delivered by the driver circuit described in Section 6.4.3. The resulting magnetic field is measured using the secondary sensing coil described in

Section 6.4.4. Finally, the magnetic field produced by the fabricated device versus applied voltage is analysed and compared to the simulated results.

6.5.1. Steady-State Voltage

The single-layer devices used to compare the relative ability of finned versus clean designs to dissipate heat at steady-state are shown in Figure 90. Figure 90(a) shows the finned design, (b) shows the clean design, and (c) shows a reference/control device used to isolate the voltage of the actuator coils from external sources of resistance.

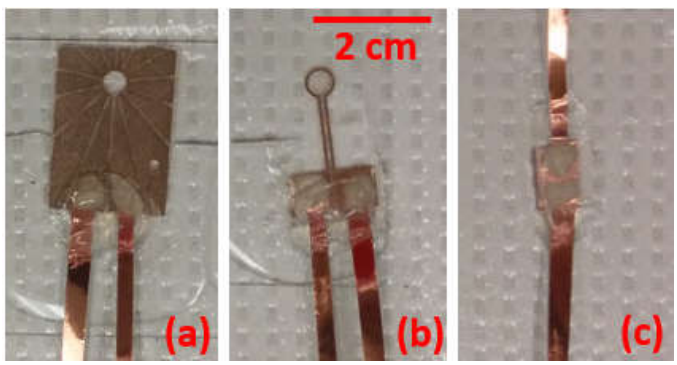


Figure 90. Fabricated devices used to compare the relative ability of (a) finned versus (b) clean designs to dissipate heat at steady-state. (c) A control structure is used to isolate the coil measurements.

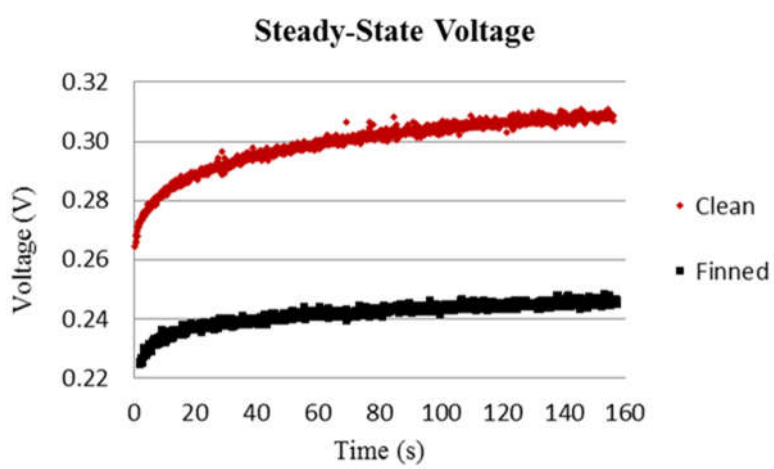


Figure 91. Steady-state voltage measured across finned and clean designs under a constant input current of 5 A.

A constant current of 5 A is applied to each device in Figure 90 and the voltage is recorded over a period of nearly 3 minutes. The resulting voltage measurements are shown in Figure 91. The voltage across the calibration device maintains a relatively steady value of 0.125 V during the experiment and is not shown in Figure 91. In contrast, the voltage across both the finned and clean designs continually increases with time. We suggest that the increase in voltage over time is attributable to an increased temperature over time and the temperature-dependent resistivity of copper [167]. At the end of the experiment, the voltage across the finned design appears to have levelled off compared to the clean design, which continues to increase at a faster rate. An increase in voltage of approximately 0.02 V from a starting voltage of 0.225 V indicates a percent increase of approximately 9% for finned designs, while the clean design voltage increases by approximately 15%. Therefore, we conclude that the finned design has a lower initial resistance and maintains that resistance more effectively at steady-state compared to the clean design. This agrees with the conclusions derived from the simulation results in Section 6.3. Note that during the experiment, the input current decreased slightly for all samples from approximately 5.10 A to 5.07 A. This is less than 1% difference in the applied current, and does not significantly affect our observations or conclusion.

6.5.2. Pulsed Voltage

The complete apparatus for measuring the generated magnetic field is shown in Figure 92. This includes (a) the voltage-pulse driver circuit, (b) actuator coil assembly, (c) magnetic field sensing coil, and (d, e) support circuits.

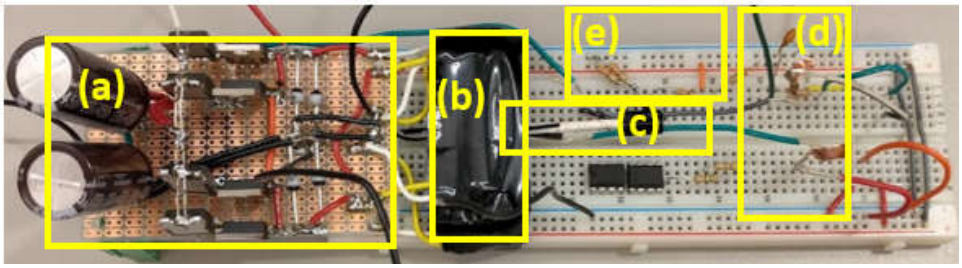


Figure 92. Pulsed magnetic field measurement apparatus including (a) voltage-pulse driver, (b) actuator coil, (c) search coil, (d) LPF, and (e) SCR trigger.

The actuator coil assembly consists of two multi-layer actuator components (a single component is shown in Figure 80), with the top face of each component facing the other. The centers of the coils are aligned with, and are separated by, the search coil. The assembly is enclosed with black tape for support. In contrast to the search coil calibration experiment (Section 6.4.4), an amplifier circuit for the search coil output is not required, as the output voltages in this experiment are relatively large. However, the search coil output still requires the high frequency noise cancellation that is initially provided by the amplifier circuit. Therefore, a resistor-capacitor (RC) low pass filter (LPF) circuit, consisting of a 1.178 kΩ resistor in series with an 811 pF capacitor, is used to filter high-frequency noise from the search coil, as shown in Figure 92(d). In Figure 92(e), a simple voltage divider with a push button switch triggers the SCR array with approximately 0.8 V at 80 mA. The two discrete integrated circuit (IC) components visible in Figure 92 are unused and disconnected.

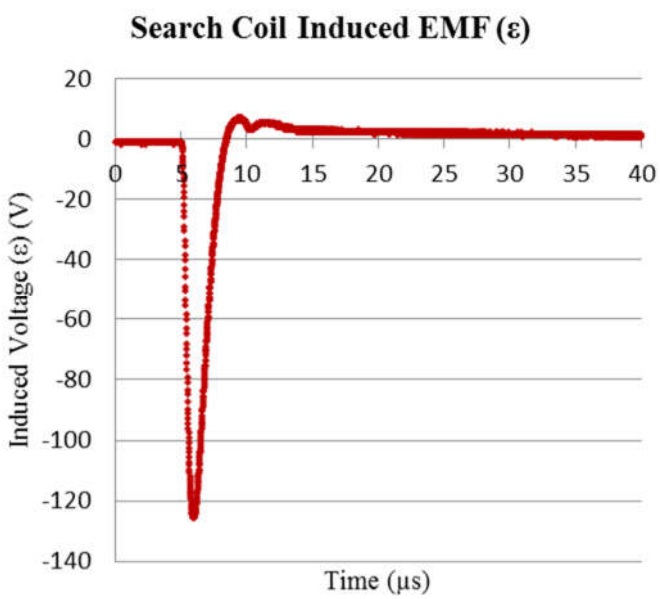


Figure 93. Search coil induced EMF after 480 V capacitor discharge.

An example measurement of the induced voltage in the search coil, ε, also called the induced electromotive force (EMF), is shown in Figure 93. For this example, the capacitors are charged to 480 V initially before being discharged by the SCR trigger. According to the analysis of the actual voltage delivered to the actuator by the capacitors

(Figure 83 in Section 6.4.3), this corresponds to a 14.8 V discharge across the actuator. In response to the actuator discharge, a maximum voltage of 125 V is measured across the search coil. The peak (negative) voltage across the search coil is reached in less than 1 μs, at which point the induced voltage begins to decrease in magnitude. At 8.5 μs the induced voltage reverses polarity and reaches a maximum (positive) value of 6.4 V at 9.5 μs, before slowly decreasing to 0 V over a period of 200 μs to 300 μs.

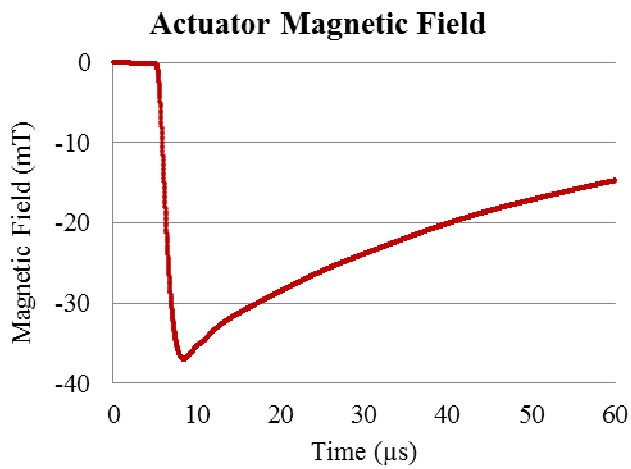


Figure 94. Magnetic field generated by the actuator given a 14.8 V peak voltage across the coil.

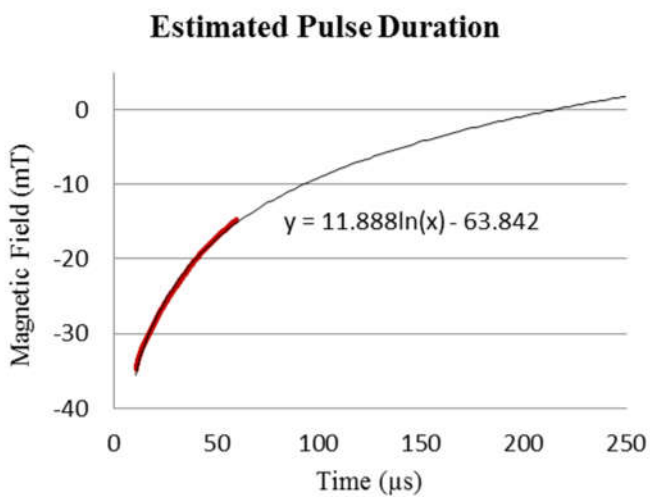


Figure 95. Estimated duration of the magnetic field pulse (215 μs) based on the extrapolation of a logarithmic trend.

According to Equation 37, the magnetic field generated by the actuator is equal to the integral of the induced EMF divided by the search coil area. For this example, the calculated magnetic field generated by the actuator is shown in Figure 94. The field reaches a maximum value of 37.1 mT at approximately 8.5 μs before decreasing logarithmically down to zero. The estimated duration of the pulse is 215 μs according to an extrapolation of the logarithmic trend line shown in Figure 95. This is close to the predicted pulse period of 200 μs, which is calculated using circuit component values in Section 6.4.3. A full decay of the pulse from its peak value to zero mT (without extrapolation) is not shown, as the oscilloscope measurement periods are limited to 60 μs.

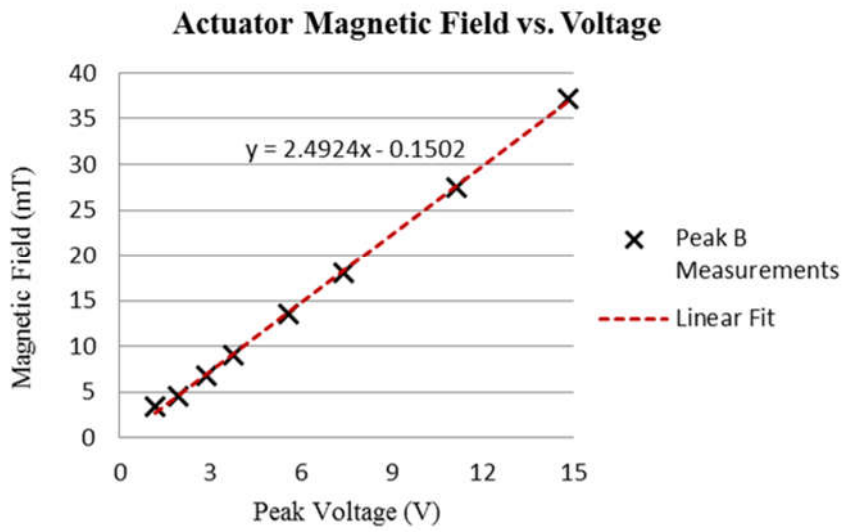


Figure 96. Peak magnetic field within the actuator versus peak applied voltage. A linear fit suggests 2.49 mT/V.

This experiment is repeated several times for various capacitor voltages from 40 V to 480 V, and the results are collectively shown in Figure 96. The peak voltage refers to the peak voltage across the actuator coil, which is calculated from the capacitor charge by multiplying the capacitor voltage by 0.0309, according to the analysis of Figure 83 in Section 6.4.3. A linear fit of the data indicates that a peak magnetic field of approximately 2.5 mT is generated per volt (peak) delivered to the actuator coil given the pulse shape observed in Figure 93.

6.6. Discussion

As mentioned in the introductory remarks of this chapter, a significant amount of characterization data is collected and analysed to assess the performance of the actuator in terms of the generated magnetic field. Performance aside, the key benefit of the actuator presented in this thesis compared to existing studies relates to the fabrication process. In contrast to the actuators presented in [176] and [179], our process allows for fully-flexible, multi-layer device fabrication. Along with the possibility of integrating NCP processes and fabricating on wearable substrates, this enables an entirely new application space for large magnitude electromagnetic actuators in flexible and wearable electronics. We are unaware of existing process technologies that enable similar levels of integration combined with the ability to generate 37 mT fields.

Given the high-level benefits associated with the fabrication process alone, we also wish to provide a detailed assessment of the performance of the actuator in terms of the generated magnetic field. Although 37 mT fields are demonstrated in this chapter, this is not necessarily the maximum magnetic field that can be generated using the proposed design. Simulation data in Section 6.3 suggest that relatively simple design modifications and decreasing the input pulse duration could lead to significantly larger fields. We therefore propose to investigate the potential for increased magnetic field actuation in detail, and to compare the estimated maximum values to those found in existing studies.

The two main goals of this discussion are (1) to estimate the maximum magnetic field that can be generated using the fabrication scheme presented here, and (2) to assess the level of agreement between the physical characterization data and the simulation data. We also compare the estimated maximum performance of the fabricated actuator to existing studies. In an attempt to estimate the maximum magnetic field that can potentially be generated using the fabrication scheme presented here, we must first validate the simulation model. If the simulation model is a reasonably accurate representation of the physical system, we may use the simulation results from Section 6.3.6 to estimate the performance of a modified actuator design that more closely resembles the configurations found in existing studies.

To compare the fabricated device to simulation, there are a number of discrepancies that must be considered:

- Input pulse shape: the pulse applied in simulation is constant (step), which differs from the circuit-generated pulse shape shown in Figure 83.

- Pulse duration: a 200 μs pulse is applied to the fabricated actuator, while the nearest simulated pulse duration in Section 6.3 is 100 μs.

- Probe setup: the magnetic field calculation in COMSOL is performed using point probes positioned directly above the coil center, as shown in Figure 68. In contrast, the search coil is positioned according the description in Section 6.5.2, and measures the magnetic field within the entire volume of the coil between the top and bottom actuator components.

- Conductance: the conductance of the simulated actuators provided by COMSOL is significantly larger than the measured conductance of the fabricated actuator.

Given these considerations, a number of assumptions are made. First, we conservatively ignore pulse shape. Since the maximum voltage is found in simulation using a constant (step) pulse profile, it is expected that an applied voltage with a Gaussian profile, or profile similar to Figure 83, will allow for significantly larger peak input voltages and generated magnetic fields. By ignoring this difference in input profiles, we get a conservative estimate for the maximum field that can be generated by the fabricated device. Next, we use simulation data to estimate the maximum magnetic field profile for 200 μs pulse periods applied to Geometry 3. These conditions reflect those in the physical characterization experiments. The maximum magnetic field for a 100 μs pulse is found via simulation to be 263 mT in Simulation 4.3. Using the trend line generated from the set of all results from Simulation Set 4 (Figure 74), the maximum magnetic field for a 200 μs pulse using Geometry 3 is found to be approximately 229 mT. As expected, this is less than the field corresponding to a 100 μs pulse, as Joule heating within the coil is proportional to pulse duration. The ratio of the magnetic field magnitude found in the 100 μs simulation compared to the estimated value for a 200 μs pulse is 263 mT to 229 mT. We suggest that this ratio may be applied as a scaling factor to the magnetic field profile along the z-axis for 100 μs pulses simulated in Simulation 4.3 to estimate the magnetic field profile for Geometry 3 given a 200 μs input pulse. This estimated profile is shown in Figure 97. We calculate the corresponding input

voltage by scaling the applied voltage from Simulation 4.3 with the same ratio, resulting in 8.53 V applied.

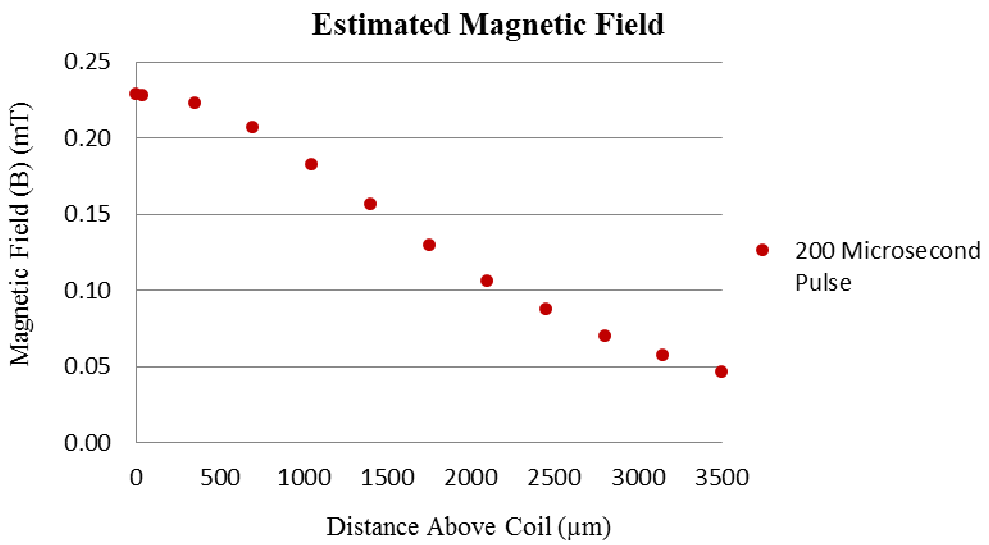


Figure 97. Estimated magnetic field generated by Geometry 3 given a 200 µs input pulse.

We also compensate for the experimental setup. In the COMSOL studies, only a single actuator plane is simulated. In contrast, the fabricated actuator consists of two components that contain four actuator layers each. It is shown in Section 6.4.2 that the average PDMS thickness between the metal layers of the fabricated actuator is approximately 246 µm. In addition, the top and bottom actuator components are separated by a height of 2.55 mm due to the height of the search coil. Therefore, for both the top and bottom actuator components, the center of the search coil is 1.521 mm from the top actuator layer, 1.767 mm from the second layer, 2.103 mm from the third, and 2.259 mm from the fourth. Applying a linear interpolation to the data from Figure 97 for the field contribution from each layer, and summing the values for all layers, results in a final value of 1.02 T. To summarize, the initial estimate of 229 mT for a single coil found in simulation is increased to 1.02 T after compensating for the experimental setup, which contains a total of eight coils at various positions along the z-axis. The value of 1.02 T represents an estimate the maximum magnetic field that can be achieved at the center of the search coil before device failure. It is calculated based on an interpolation of simulation results to match the pulse duration and actuator configuration used in the

physical characterization experiments. We note that the scaling factor that accounts for the difference between a single actuator and the configuration used in our experiment is approximately equal to 4.45 (unitless).

Now, we compare the simulation-based estimate to an estimate using physical characterization data. To estimate the magnetic field generated by the fabricated device given the input voltage applied in simulation, we use the characterization data summarized in Figure 96. As shown in Figure 96, the magnetic field measured by the search coil in the fabricated actuator follows a linear trend of 2.49 mT/V. Given the maximum estimated input voltage found in simulation for this configuration (8.53 V), this trend yields a magnetic field generated by the fabricated device of approximately 21.2 mT. This differs significantly from the simulation-based estimate of 1.02 T. In fact, it is even lower than the measured magnetic field result of 37 mT. However, there is another important correction that must be made due to the discrepancy between the measured resistance of the fabricated actuator and the conductance of the actuator model given in COMSOL. This inconsistency results in significantly less current in the fabricated actuator compared to the COMSOL model given the same input voltage. Since the generated magnetic field is proportional to current rather than voltage (Equations 30 and 31), we must scale the input voltage applied in the fabricated actuator estimate so that the current matches the simulation-based estimate. We use the conductance of Geometry 3 given in COMSOL (133 Siemens, Table 19) and the measured resistance of 0.16 Ω per actuator layer (20 mΩ is measured for all eight layers in parallel in Section 6.4.3) to calculate a voltage scaling factor of 21.28. This calculation follows directly from Ohm's Law, given by Equation 8 in Section 2.2. We apply the scaling factor to the voltage applied in simulation (8.53 V) and, using the 2.49 mT/V trend from Figure 96, calculate a predicted magnetic field output of 0.45 T for the fabricated device. This value represents the maximum magnetic field that can be generated by the fabricated actuator before failure given a 200 μs input pulse, as measured by the search coil.

The estimate of the maximum magnetic field using physical characterization data is approximately half of the estimate corresponding to simulation data alone. In an attempt to justify this discrepancy, we note that the simulation-only estimate corresponds to the field measured at a single point within the center of the search coil, while the

measurement of the fabricated actuator is effectively averaged over the entire volume of the search coil. We suggest, therefore, that the search coil measurement provides an underestimate of the magnetic field strength at the search coil center. This is supported by the assumption that the magnetic field strength in a Helmholtz configuration is largest at the center of the configuration and decreases in proportion to the distance from the center [177]. We also suspect that non-idealities in the fabricated device and measurement apparatus may contribute to this inconsistency. For example, misalignment between the search coil and the actuator will lower the effective area of the search coil, and the measured response of the search coil to magnetic fields will decrease accordingly. While these inaccuracies may contribute to the differences between the simulation and experimental results, further analysis is required to quantify this contribution.

Despite the assumptions made in this analysis, the simulation results provide valuable insight into the relationship between actuator design parameters and the generated magnetic field. In addition, we conclude that simulation results may be used to provide a moderately reliable estimate of the magnetic field generated by fabricated devices, as long as input current conditions are consistent. Given this conclusion, we propose to use the relationships between maximum magnetic field strength, pulse duration, and coil radius found in simulation to estimate the performance of a modified actuator design.

Given the substantial increase in magnetic field associated with decreasing both coil radius (Figure 71) and pulse duration (Figure 74), we expect that the fabricated actuator demonstrated in this thesis can be modified to produce significantly larger fields. A 30 ns input pulse duration, which is demonstrated in a similar investigation into pulsed magnetic field generation [179], applied as an input to the trend line equation in Figure 74 results in an estimated maximum magnetic field of 4.99 T for a single coil. Recall that the scaling factor that accounts for the difference between a single actuator and the configuration used in our experiment is approximately equal to 4.45. Applying this scaling factor, we estimate that maximum magnetic field that can be produced by our actuator given a 30 ns input pulse is 22.2 T. In addition to compensating for pulse duration, we also wish to estimate the maximum magnetic field that can be produced

given a reduction in coil radius. For this estimate, we assume a minimum inner coil diameter of 50 μm. This assumption is slightly aggressive given the minimum feature size analysis in Section 4.2.3, but has been demonstrated in a similar existing study [177]. Applying a 25 μm radius versus a 2.283 mm radius to the trend line equation in Figure 71 results in an additional increase of the magnetic field by a factor of 7.27. This results in a total estimated generated magnetic field of approximately 160 T. Recall that the original estimate of the maximum magnetic field generated by the fabricated device using physical characterization data is 0.45 T. This is approximately half of the 1.02 T estimate generated using simulation data alone. If we assume that the field generated by the modified fabricated device under a 30 ns pulse is also measured to be half of the simulated maximum (160 T), the result is an 80 T field measured within the volume of the search coil.

We note that the scaling used compensate for a reduction in radius using the trend line in Figure 71 cannot be applied to our fabricated design with confidence. This is because the results in Figure 71 apply to a coil width of 200 μm under steady-state input conditions, while we are estimating the maximum magnetic field of a 500 μm radius coil under pulsed inputs; we speculate that the relationship between the generated magnetic field and coil radius is dependent on both coil width and pulse duration. While further characterization is certainly required, we conclude that the simulation data and physical characterization data support the speculation that magnetic fields larger than 50 T may be possible using the modified actuator design presented in this section. Therefore, in addition to the high-level benefits related to device integration and flexibility, the performance of electromagnetic actuators fabricated using our multi-layer, thick-film fabrication scheme may even be able to meet or exceed the performance of existing, rigid configurations [176] [179].

Chapter 7.

Future Work

Future work for this new process includes a demonstration of its adaptability to large scale fabrication by patterning a full 8.5 × 11 inch transparency sheet in a large electrodeposition bath before transferring to PDMS. If accomplished, this will suggest that our process can be adapted to large scale fabrication, which is desired for a commercially viable process. Although the construction of a custom exposure unit for large substrates would be required, it would eliminate the need for a photolithographic aligner, which is the only conventional microfabrication equipment currently used in this process. Other areas of investigation include improvements to the metallization layer in terms of conductivity, uniformity, resolution limits, and surface roughness. These improvements will most likely come from formulating an alternative to the sacrificial copper seed and modifying the electrodeposition bath chemistry and deposition parameters. A more conductive paint, with finer grain size and fewer areas of reduced conductivity, could produce a more uniform and conductive metal layer. Alternative paint formulations should also be investigated for the purpose of improving the IR-assisted delamination and transfer process. An encapsulation layer may also be investigated, but is not studied in detail in this thesis. In future experiments, the thickness of the PDMS encapsulation layer should be both controlled and measured. The minimum encapsulation thickness should also be evaluated, and alternative encapsulation strategies and materials should be explored. Although the encapsulation layer acts to protect the circuit, it can also influence the mechanical properties of a fabricated device and can affect device functionality in general. Throughout the investigation of these process refinements, improving the minimum feature size of the deposition layer should remain a primary goal. More significant process variations, such as the development of a hybrid process variant with nanocomposite polymers to promote flexing and stretching in

high stress areas, should also be developed. A proof of concept for this hybrid process is demonstrated in Section 3.4.1.

Aside from metal layer enhancements, we are enthusiastic about the potential applications for this process in the field of wearable electronics. In the future, we hope to produce a mobile, wearable system including sensing, actuating, charging, and communicating components integrated on a platform fabricated using this process. This will include the integration of external components and alternative NCP-based polymer processes, both demonstrated briefly in Section 3.4.1. As mentioned in Chapter 5, this work will also involve a characterization of the frequency response of fabricated devices. Before fabricating more advanced devices, additional characterization data relating to the stretchable interconnects is required. For example, the reliability of Peano-based interconnects after being washed and dried requires further study, as does the relationship between force and strain for the interconnects deposited onto a representative set of fabrics.

The study of the multi-layer electromagnetic actuator has led to a number of valuable results, but it has also raised several concerns warranting further investigation. Regarding the simulations, in Section 6.3.1 we propose several modifications to improve the fidelity of the simulation model. In addition, in Section 6.3.6 we propose several design improvements to minimize the observed temperature gradients shown in Figure 76 and Figure 77 under pulsed input conditions. The modifications could be as simple as rounding the sharp corners found in junction areas to decrease the observed current density gradients, but other features may also be explored. An investigation into the improved performance of clean versus finned structures for relatively small input pulse durations warrants further investigation, and the mechanism is not yet fully understood. Regarding the physical device, we propose several improvements to increase the peak magnetic field generated by the actuator. First, the increase in magnetic field associated with decreasing coil radius and pulse duration suggests that in future iterations, the coil radius and input pulse duration should be minimized. In addition, the driver circuit may be improved to increase the ratio of voltage delivered to the actuator compared to the initial capacitor voltage, which will remove the requirement for large input voltage

sources. Eventually, we would like to develop an improved device as part of a pump or valve solution in a microfluidic/LOC application.

Chapter 8.

Conclusion

This study has provided the detailed characterization of a newly developed method of PDMS metallization through a simple, low-cost micropattern transfer process. This process includes the electrodeposition of thick metal films to provide patterned layers with extremely low resistance, and addresses the common problem of metal-polymer adhesion by encapsulating the metal layer in PDMS as it cures. This patterning and transfer process uses minimal fabrication equipment, low-cost materials, and relatively few processing steps to address issues of complexity and cost that are characteristic of other metallization processes. We also demonstrate the solderability of the deposited layer, the integration of screen-printed conductive NCP layers, and two application-specific process modifications. The first modification is used to demonstrate a versatile new method for 'stamping' metal layers onto unconventional substrates such as stretchable fabrics for wearable electronics. The second modification is used to demonstrate a multi-layer electromagnetic actuator utilizing stacked, aligned planar coils and an integrated Fe-PDMS core. The new fabrication process has been thoroughly characterized in terms of resistivity, surface roughness, thickness, feature size, reliability, and other surface features.

The deposited structures have a mean thickness of 70 μm, a minimum feature size of roughly 100 μm, a surface roughness profile containing an average of roughly 5 μm features, and a film resistivity of approximately 2.5 μΩ-cm to 3 μΩ-cm. Although the copper resistivity is roughly 10% larger than other copper electrodeposition processes, the overall film thickness combined with high film conductivity make this process ideal for high-current, low-power applications. The 100 μm minimum feature sizes allow the use of this process in a wide variety of microsystems applications. Although other deposition techniques can surpass the feature size demonstrated here,

we suggest several potential approaches to improving the minimum feature size. The 5 μm roughness features are 10 to 100 times larger than electrodeposited layers shown in other studies, which is likely due to the use of our particular conductive paint seed layer rather than a bulk metal or semiconductor material. This roughness profile may improve PDMS adhesion, and could be useful in some applications such as electrochemical sensing. The data relating to defect distribution in the metal layers shows that after four hours of deposition, approximately five defects with an area of 100 μm^2 exist within a 10 mm^2 enclosing area. It is difficult to compare this data to existing studies. However, we assume that the number of defects is heavily dependent on the seed layer composition and morphology, and that a reduction on defects can be achieved by investigating new seed layer formulations and deposition techniques. To further explore the potential of this process, there are a number of process variations that may be investigated in future work, particularly relating to seed layer formulation and deposition, to ensure the finest resolution and reliability in the finished product.

We have performed the characterization and parametric analysis of first-order Peano structures fabricated using the newly developed process. We have also demonstrated the application of this process to wearable electronics through the characterization of wearable, stretchable interconnects. The Peano-based interconnect design corresponding to the maximum strain at conductive failure is able to stretch by approximately 57% on wearable fabrics before failure. On PDMS alone, the interconnects are able to stretch by less than 20% before failure. However, this decrease in stretchability is attributed mainly to the fact that the PDMS-only characterization corresponds to an earlier iteration of the deposition process. The relationship between relative resistance and tensile strain of Peano-curves is thoroughly investigated, and the geometries resulting in maximum strain before failure are found to match simulated predictions in existing studies with two caveats. First, maximum strains are found to be lower in 285˚ geometries compared to 270˚ geometries, demonstrating that the gains typically associated with increasing arc length are limited. Second, the gains typically associated with maximizing the ratio of radius of curvature to wire width are shown to be limited in the context of miniaturized devices. In addition, cyclic failure and recovery tests show that these devices consistently fail and recover conductivity at strains that are relatively consistent over ten iterations. We speculate that failure at each iteration is due

to the development of a discontinuity in the conductor at the fracture site of the original failure. The strain at failure for each iteration after the initial failure is consistent, and always less than the strain at the initial failure. Similarly, the strain at recovery is consistent and is less than the strain at failure. We speculate that recovery occurs when two sides of the disjointed conductor regain contact at the site of failure, leading to the rapid recovery of conductivity. In contrast to the strain at failure and recovery, the relative resistances during cyclic testing are less consistent.

We also demonstrate a high current, low-power electromagnetic actuator using the newly developed process. The maximum measured magnetic field for the fabricated actuator is 37 mT. Given the conservative input voltages applied to the fabricated device and a significantly larger estimated maximum input voltage, a magnetic field of 1.04 T may be possible for 200 μs input pulses. Simulation data also suggests that the peak magnetic field may be significantly increased by reducing the coil radius, minimizing the input pulse duration, and modifying the driver circuit to deliver maximum voltage to the coil relative to the input capacitor charge. This application demonstrates several key advantages of our process, including thick metal film deposition and the ability to fabricate aligned, multi-layer devices. The overall fabrication scheme also allows for integrated, full-flexible devices in wearable electronics. This work is applicable to many applications requiring short duration magnetic field pulses, such as bi-stable magnetic MEMS latches and valves in microfluidics applications.

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