

Totem-Pole Power Factor Correction Rectifier with Gallium-Nitride Devices for Telecom Power Supply

by

Rifat Alam Siddique

B.Sc.Engg., Bangladesh University of Engineering and Technology, 2012

Thesis Submitted in Partial Fulfillment of the
Requirements for the Degree of
Master of Applied Science

in the

School of Mechatronic Systems Engineering
Faculty of Applied Sciences

© Rifat Alam Siddique 2016

SIMON FRASER UNIVERSITY

Fall 2016

All rights reserved.

However, in accordance with the *Copyright Act of Canada*, this work may be reproduced without authorization under the conditions for "Fair Dealing." Therefore, limited reproduction of this work for the purposes of private study, research, criticism, review and news reporting is likely to be in accordance with the law, particularly if cited appropriately.

Approval

Name: Rifat Alam Siddique

Degree: Master of Applied Science

Title: Totem-Pole Power Factor Correction Rectifier
with Gallium-Nitride Devices for Telecom Power
Supply

Examining Committee: **Chair:** Dr. Krishna Vijayaraghavan
Assistant Professor

Dr. Jiacheng (Jason) Wang
Senior Supervisor
Assistant Professor

Dr. Behraad Bahreyni
Supervisor
Associate Professor

Dr. Rahul Khandekar
Supervisor
Team Lead - Power Electronics Control
Alpha Technologies Ltd.

Dr. Mehrdad Moallem
Internal Examiner
Professor

Date Defended/Approved: December 14th, 2016

Abstract

Wide-bandgap (WBG) semiconductor technology will largely replace silicon switching devices in the active power factor correction (PFC) circuit of a telecom power supply in the near future. Superior electrical characteristics of commercially available Gallium Nitride (GaN) devices make totem-pole PFC a clear winner over competing topologies in terms of efficiency. This thesis focuses on the development of a totem-pole PFC using state-of-the-art GaN devices for next-generation telecom power supplies. A detailed investigation of ac zero-crossings of this topology has successfully identified the rapid fluctuation in voltage across low-frequency MOSFET as the source of common-mode noise. An equivalent circuit accompanied by a set of equations correlate different circuit parameters with the noise generation. Challenges associated with current reversal near zero-crossings of a synchronous totem-pole PFC are studied and a formerly unreported source of common-mode noise generation around ac zero-crossings has been investigated in detail.

Keywords: Totem-pole; Power factor correction; Gallium Nitride; Wide-bandgap; Common-mode noise

Acknowledgements

I would like to thank my senior supervisor Dr. Jason Wang for his perpetual support, encouragement and kind suggestions throughout the course of my work. His valuable advice on research issues, experimental verification, and writing manuscripts has always been a great help to me. It was a pleasure having the opportunity to work in his lab.

I would like to extend my sincere gratitude to Dr. Behraad Bahreyni for taking the time to serve as my supervisor and providing me with valuable comments to improve this work.

I am sincerely thankful to Dr. Rahul Khandekar, who with his exceptional skill, vast knowledge, and professional expertise has guided me throughout the course of this work. He has been a wonderful mentor to me and I remain grateful to him for his support and kindness.

Many thanks to Peter Ksiazek from Alpha Technologies Ltd. for his ongoing guidance, generous support and for all the technical discussions we had together. It was my privilege to learn from a brilliant engineer and wonderful person like him.

I would like to take this opportunity to thank Alpha Technologies Ltd. for providing constant support and laboratory facility for this work. My special thanks to all the engineers and technicians in Alpha for their supports and kind guidance throughout the duration of this work.

I would like to acknowledge that this work was funded partly by The Natural Sciences and Engineering Research Council of Canada (NSERC) and Mathematics of Information Technology and Complex Systems (MITACS).

Last but not least, I would like to thank my family in Bangladesh, for being an everlasting source of encouragement, love, and sacrifice that kept me going.

Table of Contents

Approval.....	ii
Abstract.....	iii
Acknowledgements.....	iv
Table of Contents.....	v
List of Tables.....	vii
List of Figures.....	viii
Chapter 1. Introduction.....	1
1.1 Background.....	1
1.2 Research Scope.....	5
1.3 Thesis Outline.....	6
Chapter 2. Wide-Bandgap Semiconductors in Power Factor Correction Devices.....	7
2.1 Wide-bandgap Semiconductor.....	7
2.1.1 Gallium Nitride (GaN) Semiconductor Device.....	10
Construction.....	10
Normally-off GaN.....	11
Reverse Conduction in Lateral GaN.....	12
Current Collapse.....	13
2.2 Power Factor Correction (PFC).....	14
2.2.1 ac-dc Power Conversion Architecture: Single and Two-Stage.....	14
2.2.2 Passive PFC Topologies.....	17
2.2.3 Active PFC Topologies.....	18
Bridge PFC.....	18
Bridgeless PFC.....	20
2.3 PFC Topologies Using WBG Semiconductors.....	30
2.3.1 Suitable PFC Topologies for WBG Application.....	30
2.3.2 Comparison.....	31
Chapter 3. Totem-pole PFC.....	35
3.1 Operation.....	35
3.1.1 Positive Half Cycle Operation.....	36
3.1.2 Negative Half Cycle Operation.....	37
3.2 Simulation-Based Study.....	38
3.3 Common-Mode Noise.....	40
3.4 Zero-Crossing Spike Current.....	44
3.4.1 Origin of Zero-crossing Spike Current.....	45
What's in Literature?.....	45
Analysis of Zero-crossing Spike Issue.....	46
3.4.2 Effect of Zero-crossing Spike Current on EMI.....	52
3.4.3 Switching Techniques to Mitigate CM Noise.....	56

Chapter 4. Synchronous Totem-pole PFC	60
4.1 Reverse Conduction Mode	60
4.1.1 Switching Technique to Avoid Reverse Current Flow.....	62
4.2 CM Noise during Reverse Conduction Mode	63
Chapter 5. Design Implementation of Totem-pole PFC	68
5.1 Design Equations	68
5.2 GaN Half-Bridge Design	70
5.2.1 Evaluation Board Overview.....	70
5.2.2 Gate Drive Design	70
5.3 Low-Frequency Half-Bridge Leg Design	73
5.4 Inductor Design	74
5.5 Current Sensing and Zero-crossing Detection	75
5.6 Experimental Setup and Result	76
Chapter 6. Conclusions	79
6.1 Summary.....	79
6.2 Future Work.....	80
References.....	82
Appendix A. Analysis of Equivalent Circuit.....	88
Appendix B. Derivation of Design Equations	95

List of Tables

Table 2-1:	Physical characteristics of Si and major WBG materials [16][17].....	8
Table 2-2:	Key datasheet parameters for selected switching devices.....	33
Table 3-1:	Parasitic capacitances for CM noise simulation.....	43
Table 5-1:	Verification of design equations from simulation.....	69

List of Figures

Figure 1.1:	Different fields of application for ac-dc converters	1
Figure 1.2:	Diode bridge rectifier. Current and voltage waveforms	2
Figure 1.3:	Two-stage ac-dc conversion.....	3
Figure 1.4:	Traditional full-bridge PFC.....	3
Figure 2.1:	Bandgap of different materials.....	7
Figure 2.2:	Baliga's Figure of Merit for Si and some WBG semiconductors.....	9
Figure 2.3:	Lateral GaN structure	11
Figure 2.4:	Cascode GaN	11
Figure 2.5:	Schematic cross section of GaN-GIT	12
Figure 2.6:	Reverse conduction characteristics of an e-mode GaN HEMT [22]	13
Figure 2.7:	Conceptual representation of single-stage power architecture	15
Figure 2.8:	Conceptual representation of two-stage power architecture	15
Figure 2.9:	Two-stage passive PFC	17
Figure 2.10:	Bridge PFC	19
Figure 2.11:	Positive half-cycle operation of the bridge PFC	19
Figure 2.12:	Basic bridgeless PFC	20
Figure 2.13:	Positive and negative half cycle operation of basic bridgeless PFC.....	21
Figure 2.14:	Basic bridgeless PFC with parasitic capacitors responsible for EMI	22
Figure 2.15:	Basic bridgeless PFC with capacitor bypass	23
Figure 2.16:	Semi-bridgeless PFC	23
Figure 2.17:	Dual boost bridgeless PFC with reduced EMI	24
Figure 2.18:	Dual boost bridgeless PFC with bidirectional switch.....	24
Figure 2.19:	Positive half cycle operation of dual boost PFC with bidirectional switch	25
Figure 2.20:	Pseudo totem-pole bridgeless PFC	25
Figure 2.21:	Three-level boost bridgeless PFC rectifier	26
Figure 2.22:	Three-level PFC with nature voltage clamp	27
Figure 2.23:	Positive half cycle operation of three-level nature voltage clamp PFC....	27
Figure 2.24:	Voltage doubler PFC.....	28
Figure 2.25:	Positive half cycle operation of voltage doubler PFC circuit.....	29
Figure 2.26:	Totem-pole PFC.....	30
Figure 2.27:	PFC topologies for efficiency comparison.....	32
Figure 2.28:	Simulation-based efficiency comparison between different PFC topologies using WBG devices	33
Figure 3.1:	Totem-pole PFC.....	35
Figure 3.2:	Positive half cycle operation of totem-pole PFC	36
Figure 3.3:	Reverse recovery current flow for Si-MOSFET.....	37
Figure 3.4:	Negative half cycle operation of totem-pole PFC.....	38

Figure 3.5:	Totem-pole PFC simulation circuit.....	38
Figure 3.6:	Totem-pole PFC simulation waveforms.....	39
Figure 3.7:	Simulation-based efficiency comparison	39
Figure 3.8:	Split-phase power supply	40
Figure 3.9:	Totem-pole PFC with Y-capacitor and C_{fg}	41
Figure 3.10:	Equivalent circuit around zero-crossing for CM noise analysis	42
Figure 3.11:	Simulation circuit for analyzing CM noise in totem-pole PFC.....	43
Figure 3.12:	LISN.....	44
Figure 3.13:	LISN waveforms.....	44
Figure 3.14:	Totem-pole PFC near zero-crossing.....	46
Figure 3.15:	Zero-crossing spike current.....	47
Figure 3.16:	Negative to positive zero-crossing waveforms.....	48
Figure 3.17:	Transitional stages during negative to positive zero-crossing.....	49
Figure 3.18:	Negative to positive zero-crossing equivalent circuit	51
Figure 3.19:	Negative to positive zero-crossing equivalent circuit simulation.....	52
Figure 3.20:	Graphical representation of equation (3-8)	54
Figure 3.21:	Dependance of $N(t)_{max}$ on different circuit parameters	54
Figure 3.22:	Graphical representation of equation (3-10)	55
Figure 3.23:	Zero-crossing transition with soft start	57
Figure 3.24:	Zero-crossing CM noise reduction as shown in [56]	58
Figure 3.25:	Reduction of CM noise by applying constant duty after ZC	59
Figure 4.1:	Dc-dc Boost Converter	60
Figure 4.2:	Reverse conduction mode during positive half cycle	61
Figure 4.3:	Switching techniques to avoid RCM	62
Figure 4.4:	MOSFET drain to source voltage fluctuation during RCM	63
Figure 4.5:	Generation of CM noise during RCM.....	65
Figure 4.6:	CM noise generation during RCM	66
Figure 4.7:	Mitigation of CM noise during RCM.....	67
Figure 5.1:	High-frequency GaN leg of the totem-pole PFC	70
Figure 5.2:	Gate drive circuitry from GaN EVB user manual [64].....	72
Figure 5.3:	Low-frequency leg gate drive connection	73
Figure 5.4:	Low-frequency MOSFET leg of the prototype.....	73
Figure 5.5:	Inductor designed for the prototype	74
Figure 5.6:	Hall effect sensor connections.....	75
Figure 5.7:	Zero-crossing detection circuit for totem-pole PFC.....	76
Figure 5.8:	Totem-pole PFC prototype	77
Figure 5.9:	Input voltage and current of the totem-pole PFC prototype	78

Chapter 1. Introduction

1.1 Background

The electricity distribution network of modern days is largely based on ac systems. But in the user end, this energy is consumed very often in the form of dc since modern electric loads are in large measure dc loads. Therefore, an intermediate stage is required to convert the ac current to dc. Conventionally, ac–dc converters, which are also called rectifiers, are developed using diodes and thyristors to provide controlled and uncontrolled dc power with unidirectional and bidirectional power flow [1]. The ac-dc conversion of electric power is widely used in many applications such as battery energy storage systems, telecom/datacenter power supplies, uninterruptible power supply (UPS), and renewable energy harvesting systems.

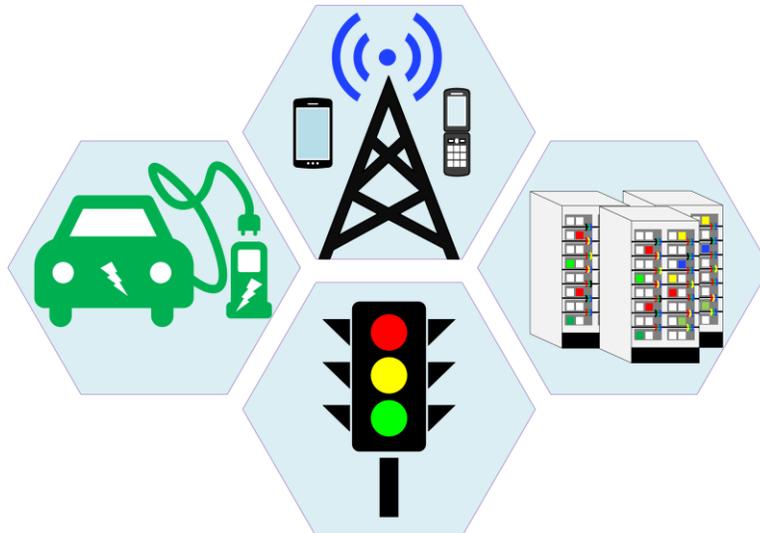


Figure 1.1: Different fields of application for ac-dc converters

Traditional diode based rectifier consists of a front-end diode bridge followed by a bulky capacitor to smoothen the output dc voltage [2]. Such ac-dc converter inevitably introduces highly distorted input current into the line and results in serious current harmonics and low power factor [3], [4].

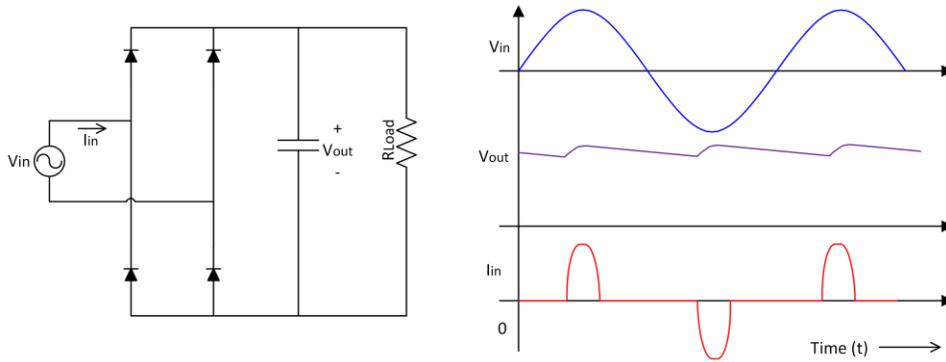


Figure 1.2: Diode bridge rectifier. Current and voltage waveforms

Since the harmonics generated by the diode rectifiers are reflected back to the ac line, they introduce losses in the system and interfere with other communication devices connected to the line. Such unwanted harmonics in power lines became problematic and as a preventive measure, strict regulations such as IEC 61000-3-2, IEEE Standard 519-1992 are followed by the regulatory committees like FCC and CSA [5][6]. To comply with these standards in power supply design, the traditional diode based rectifiers are often linked with a boost converter to shape the input current. This arrangement is commonly known as a Power Factor Correction device or PFC. Power factor is a measure of power quality and it is calculated by equation (1-1). Power factor is a dimensionless number between 0 and 1. Unity power factor means that maximum real power being transferred to load and it's a desirable condition.

$$Power\ Factor\ (PF) = \frac{Real\ Power\ (W)}{Apparent\ Power\ (VA)} \quad (1-1)$$

A Power Factor Correction circuit controls the input current drawn from the ac mains to maximize the available real power. Ideally, the electrical appliance should appear to the ac grid as a pure resistor, in which case the reactive power drawn by the device will be zero [7]. Power factor correction circuit can be of two major types – Passive and Active. In passive PFC design, an LC filter is inserted between the ac line and diode bridge. Though this approach is rugged and very simple, the PFC is remarkably bulky and generally the power factor is poor [8]. Passive PFC hence is an unpopular choice for most applications.

The introduction of active PFC led to a two-stage approach in the power supply design where the PFC stage is followed by a dc-dc converter. The result is an overall improvement in efficiency while maintaining a unity power factor [9].

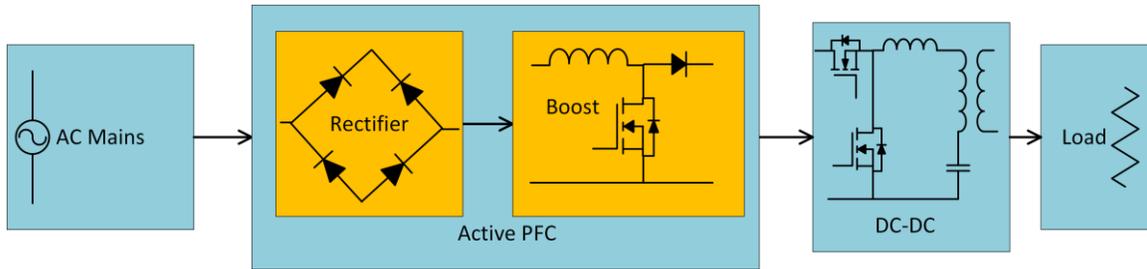


Figure 1.3: Two-stage ac-dc conversion

There are different topologies for implementing active PFC techniques [10], among which the boost converter is the representing topology because it exhibits many advantages such as small input current ripple due to the series connection of the inductor at the input side, high power factor over the whole input voltage range, small size of the output capacitor due to its high voltage, and simple circuit [8].

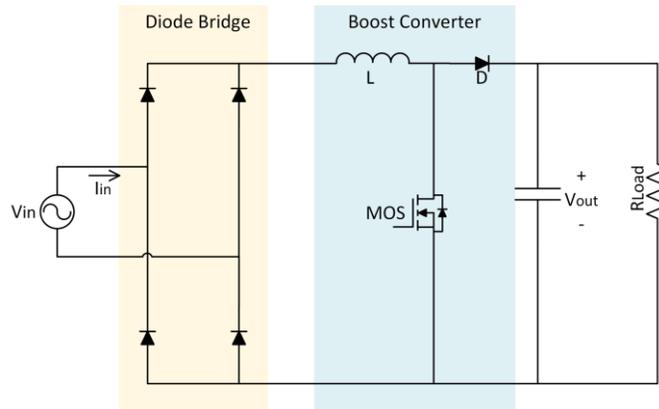


Figure 1.4: Traditional full-bridge PFC

The boost converter based PFC can be operated either in discontinuous or continuous current conduction mode depending on the characteristic of the inductor current. Since the continuous nature of the boost converter's input current results in low conducted electromagnetic interference (EMI) compared to discontinuous conduction, it is by far the popular choice for 400W to several kilowatt power level [11].

The inclusion of several passive and active solid-state devices like diode and MOSFET increases the overall cost of the active PFC based power supply. So cost reduction remained a key challenge for design engineers and industries for past decades have largely been dominated by Silicon (Si) based semiconductor devices because of their low cost and commercial availability.

PFC is an integral part of power supplies in various industries. Over the last few decades, driven by the continuous increase of the integration density of microelectronic circuits, the development of power supplies in data centers and telecom installations has been characterized by a constant demand for an increase in power density and efficiency [12]. Though Si-based power switching devices are mature and well established, they suffer from some important limitations regarding blocking voltage capability, operation temperature, and switching frequency [13]. Using traditional Si-based devices therefore offer very little room for improvement in telecom and data centre power supplies.

With the continuing trend toward higher power rating, higher efficiency, lower weight, and smaller size power electronic converters in various applications, the need for better performance power switching devices has been warranted [14]. As a result, the wide-bandgap (WBG) semiconductor devices were introduced in power converters. These WBG power semiconductor devices can achieve high efficiency while switching at high-frequency resulting in a dramatic improvement in power density. Among the possible WBG semiconductor candidates, Silicon Carbide (SiC) and Gallium Nitride (GaN) show the best trade-off between theoretical characteristics (high blocking voltage capability, high-temperature operation, and high switching frequencies), commercial availability of the starting material (wafers and epitaxial layers), and maturity of their technological processes [13].

Currently SiC and GaN-based power semiconductors are aiming primarily at different markets. GaN-based devices are well suited for 200-900V applications whereas SiC-based power devices are being tailored for power electronics from 900 to 15,000V and higher. It is expected that by 2020, WBG devices will replace most Si semiconductor devices in the 600-1700V range. As per the projection of market research and strategy consulting company *Yole Développement*, the first sector to embrace GaN-based semiconductor devices is the Power Factor Correction (PFC) circuits in power supply units. According to their estimate, the power supply/PFC sector is expected to dominate the GaN market from 2015 to 2018 before the automotive sector eventually emerges as another major one [15].

The fast switching speed and low on-resistance of the WBG devices allow high-frequency operation, which consequently reduces the cost and volume of power supply units. Due to their small gate capacitance, the newly emerging GaN high electron mobility

transistors (HEMT) present a good choice for high-efficiency power supply design. Another important property that distinguishes the WBG devices including GaN HEMTs from traditional Si-based devices is their superior reverse recovery characteristics. Especially GaN switching devices have almost zero reverse recovery, which allows the use of GaN HEMTs in some new topologies. In this work, GaN HEMTs were employed to build a totem-pole PFC in order to explore the use of WBG devices in the front-end of power supply units.

1.2 Research Scope

Wide-bandgap power switching devices especially GaN HEMTs are recently finding ground in PFC applications as expected. Since early 2015, 600V rated GaN devices are available commercially and various power supply designing companies are focusing on building GaN-based solutions in the near future. GaN devices are still far from their price parity with Si-based devices but the scenario will change in future and GaN-based designs will be in production.

This research investigates the use of GaN devices in bridgeless PFC topology and addresses different challenges in designing the final product. The direction of this research is primarily oriented towards practical design considerations. In a broader sense, the scope includes a review of PFC topologies, detail simulation-based efficiency analysis for selecting the most promising topologies of bridgeless PFCs, defining design equations, exploring noise issues associated with the selected topology, building a prototype, gather in-depth knowledge of different practical issues and possible solutions for the next stage of product development. Though GaN is intended for much high-frequency operation, in this research, switching frequency was kept relatively low (100 kHz) to facilitate the understanding of the performance of GaN switching devices in a bridgeless topology and to keep the gate driver design relatively simple.

This research does not cover the full analysis of EMI issues associated with high-frequency switching since it is considered the subject of further and separate research. The control scheme implemented in this work is standard for any semi-bridgeless topology. Power stage simulations were performed in *PSIM version 10*. Due to the unavailability of GaN model in selected simulation platform, a three-state MOSFET model was attributed the GaN datasheet values to produce a fairly reliable model of GaN HEMT.

1.3 Thesis Outline

Chapter 2 compares different physical characteristics of wide-bandgap materials with silicon. Challenges associated with WBG device fabrication and present trend in overcoming those challenges for GaN device manufacturing have also been covered in this chapter. A review of popular approaches for constructing normally-off GaN devices accompanied by a discussion of the reverse conduction technique in a lateral GaN is presented too. Then the chapter explores the pros and cons of single and two-stage PFC design approaches. A review of popular passive and active PFC topologies has been presented with brief details about their operating principle. Finally, a selected set of topologies have been simulated to compare their efficiency in order to find the suitable WBG device and PFC topology for telecom power supply.

Chapter 3 presents a detailed explanation of the operation of totem-pole PFC along with an efficiency comparison between synchronous and non-synchronous switching techniques. A modified common-mode (CM) noise model for totem-pole PFC at zero-crossing has been presented too. The well-reported issue of zero-crossing spike current is revisited in great detail and new observations have been made. Origin of zero-crossing spike current has been covered with the help of practical waveforms and several solutions have been assessed to mitigate the CM noise at zero-crossing.

Chapter 4 explains the challenges associated with synchronous switching in a totem-pole PFC. Several switching techniques to avoid the reverse current flow around zero-crossing have been covered in this chapter too. A previously unreported issue of CM noise generation around zero-crossing has been explained and a solution has been proposed to mitigate the noise.

Chapter 5 presents a set of design equations to accurately calculate the current and voltage for different parts of the totem-pole PFC circuit. Finally, the design steps for a working prototype of totem-pole PFC are presented with relevant waveforms.

Chapter 6 draws the conclusion and discusses future works.

Chapter 2. Wide-Bandgap Semiconductors in Power Factor Correction Devices

2.1 Wide-bandgap Semiconductor

The bandgap for a material is defined as the energy difference between the top of its valance band and the bottom of its conduction band. The bandgap is particularly important for determining the electrical characteristics of the material. For an insulator, this gap is much larger so the electrons cannot easily jump from the valance band to conduction band and carry electricity. For a conductor, there is no bandgap and these two bands overlap. Semiconductor materials have a moderate band gap, larger than a conductor but smaller than an insulator. Depending on the extent of this gap, a semiconductor can show different characteristics. Typically, the wider the bandgap is, the higher the temperature it can sustain.

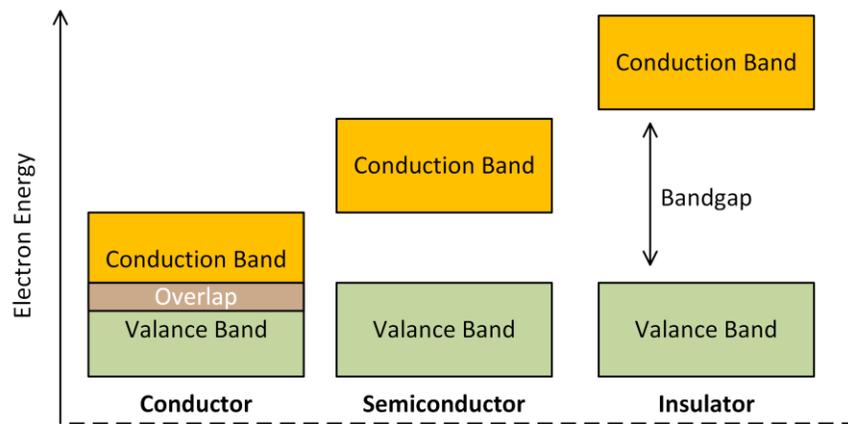


Figure 2.1: Bandgap of different materials

Silicon has a bandgap of 1.2 eV and it is not considered a wide-bandgap (WBG) material. The bandgap of popular WBG materials is approximately three times that of silicon. Common WBG materials are SiC, GaN, and Diamond. As it is shown in Table 2-1, SiC and GaN have similar bandgap and electric breakdown field, however, these values are significantly higher than silicon. Because of the superior thermal conductivity, SiC devices can transfer more heat out of the device for more efficient cooling. This is why SiC is considered particularly suitable for high-temperature environment operations. GaN has similar thermal conductivity as silicon. Diamond is the ultimate semiconductor according to its physical properties.

Table 2-1: Physical characteristics of Si and major WBG materials [16][17]

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant ϵ_r	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field E_c (kV/cm)	300	400	2500	2200	2000	10000
Electron Mobility μ_n (cm ² /Vs)	1350	8500	420 ^a 84 ^c	950 ^a 1190 ^c	1000 ^a 2000 ²	2200
Hole mobility μ_p (cm ² /Vs)	600	400	101	115	850	850
Thermal conductivity λ (W/cm-K)	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity v_{sat} ($\times 10^7$ cm/s)	1	1.2	2.0	2.0	2.5	2.7
Baliga's Figure of Merit (BFOM) ($\epsilon_r \mu_n E_c^2$) (kV/s)*	1	123	175	402	497	836.87

Note: ^a Mobility along a-axis ^c Mobility along c-axis ² 2-DEG * Normalized to Si properties

Wide-bandgap materials have larger breakdown field (E_c) compared to silicon. Therefore, power device with higher breakdown voltage can be built with WBG materials. In other words, for the same breakdown voltage level, WBG devices will be thinner in size. A smaller device has relatively shorter drift region which contributes to the reduction of device on-resistance. The drift region width under breakdown conditions is given by equation (2-1) as per [18].

$$W_d(V_B) = \frac{2V_B}{E_c} \quad (2-1)$$

where V_B is the breakdown voltage. The on-resistance of the unipolar device is given by equation (2-2).

$$R_{on} = \frac{4V_B^2}{\epsilon_s \mu_n E_c^3} \quad (2-2)$$

where, ϵ_s is the dielectric constant and μ_n is the electron mobility.

Smaller WBG devices store less reverse recovery charge (Q_{rr}) and hence their switching performance is much improved. The lateral GaN device does not have a traditional body diode p-n junction so it holds almost zero reverse recovery charge. With less reverse recovery charge, the overall switching loss is minimized even under hard switching operations. This simplifies the control and reduces additional costs of a soft-switching topology.

WBG semiconductors have high saturated drift velocity compared to silicon. This allows WBG devices to be switched at very high frequencies. High-frequency switching is

particularly desirable in power electronic equipment since it essentially reduces the size of the bulky passive components in the circuit. High drift velocity also means the charge in a depletion region of the WBG diode can be removed at a faster speed. This further reduces the reverse recovery loss.

SiC shows better performance at higher temperatures compared to GaN. This is because the thermal conductivity of GaN is approximately one-fourth of SiC. This restricts the possibility of using GaN in very high temperature. Growing GaN on top of a SiC substrate is one way to increase the thermal conductivity of GaN but this does not quite achieve the same level of performance. Another limitation with GaN devices is that pure GaN substrates are commercially unavailable. As a result GaN devices are grown on foreign substrates like SiC, Si or Sapphire. SiC wafer is expensive so Si is preferred for the mass production of GaN [13].

SiC is a more mature WBG power semiconductor than GaN. Though GaN faces some fabrication challenges now, the superior breakdown field and electron mobility provide GaN the theoretical potential to outperform SiC up to a certain thermal level in terms of on-resistance and switching frequency. GaN's higher breakdown voltage also ensures small device with fewer layers which in turn leads to less reverse recovery charge as compared to SiC. This is why GaN is exceptionally suitable for high-efficiency applications.

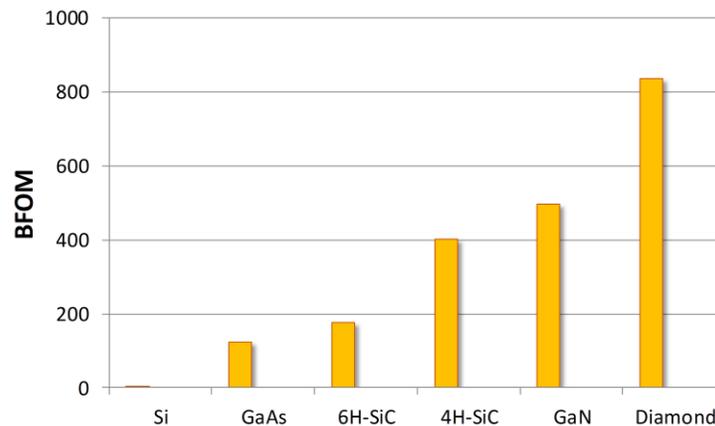


Figure 2.2: Baliga's Figure of Merit for Si and some WBG semiconductors

Note: BFOM values are normalized to Si

Baliga's figure of merit (BFOM) includes electron mobility and critical field into consideration and therefore regarded as a better tool for comparing high-speed high-efficiency devices. A greater figure of merit for a power semiconductor means that the devices can switch at a higher frequency while operating under a higher voltage. As it is evident from Figure 2.2, GaN outperforms SiC in terms of switching frequency and efficiency.

2.1.1 Gallium Nitride (GaN) Semiconductor Device

Construction

Silicon and SiC power devices utilize a vertical structure to maximize the current conduction capacity while keeping the on-resistance within the limit. Vertical device fabrication requires a matched substrate to grow the device on. Since a stable low-cost GaN substrate is unavailable, vertical GaN devices are still mostly under research and commercially unavailable. Some manufacturers like Avogy, Inc. has extensive patents on GaN-on-GaN devices and plan to commercialize their power switches soon. There have been some works to grow vertical GaN devices on Si substrate too [19].

Due to the unavailability of inexpensive GaN substrate for commercial vertical devices, much development has been done on lateral GaN devices. A number of manufacturers now offer GaN power switches rated up to 650V with relatively high current capacity. Structurally, lateral GaN devices are heterojunction field-effect transistors (HFET) which are also known as High Electron Mobility Transistor (HEMT).

Lateral GaN devices form a high electron mobility two-dimensional electron gas (2DEG) at the interface of the heterojunction due to the lattice mismatch between two semiconductors. GaN/AlGaN is a common heterojunction structure among GaN manufacturers. In a GaN/AlGaN heterojunction, the 2DEG is formed beneath the AlGaN layer as a result of crystal polarity. As shown in Figure 2.3, the accumulated electrons in 2DEG create a channel between the source and the drain to conduct electricity. The natural presence of 2DEG makes the lateral GaN a normally-on device. Such devices have little application in voltage source based power electronics topologies if they are normally-on. Therefore, some design adjustments were necessary to make them normally-off.

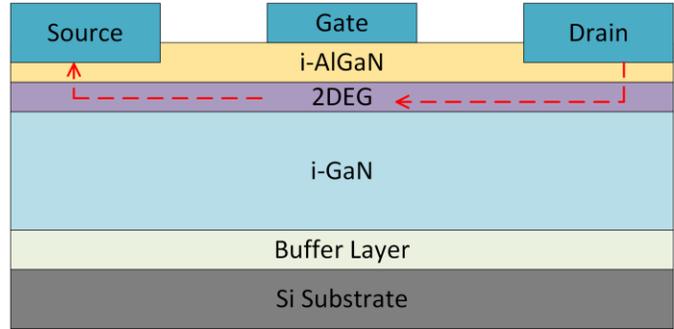


Figure 2.3: Lateral GaN structure

Normally-off GaN

One design approach for constructing normally-off enhancement mode (e-mode) GaN is by adding a low voltage Si-MOSFET in series with the depletion mode (d-mode) GaN. This device structure as shown in Figure 2.4 is known as the cascode-GaN and manufactured commercially by *Transphorm* [20]. In a cascode structure, the arrangement is such that the voltage across the MOSFET is applied as the gate-source voltage of the GaN. When the MOSFET is ON, gate-source voltage of the GaN drops to zero and it starts conducting. The current flows through the GaN and the MOSFET channel simultaneously. There are some major design concerns for cascode GaN devices. Since the MOSFET is placed in the gate loop of the GaN, the parasitic capacitances of these two devices are very critical. To ensure proper voltage sharing, the capacitances need to be matched properly. Despite these challenges in construction, cascode GaNs are available for up to 650V now. These devices however exhibit some reverse recovery charge primarily due to the presence of the Si-MOSFET body diode in the cascode structure. Some commercially available normally-off GaN devices employ additional circuitry between the gate and source to eliminate the Si-MOSFET body diode from the current path.

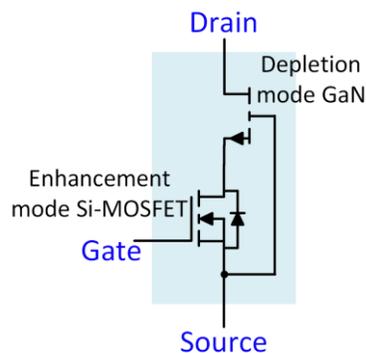


Figure 2.4: Cascode GaN

To deplete the normally-on channel of a lateral GaN device, another popular technique among the manufacturers is to insert a p-doped layer under the gate in order to increase the gate threshold voltage. A number of manufacturers including Panasonic and EPC use this technique. Panasonic used to place a p-AlGaN under the gate but recently have introduced p-GaN instead of that. This type of enhancement mode GaN devices are known as Gate Injection Transistor (GIT) [21]. The Panasonic GaN-GIT requires a steady current of few mA to be supplied to the gate during the ON period. GaN-GITs often need a complicated gate drive design because of that.

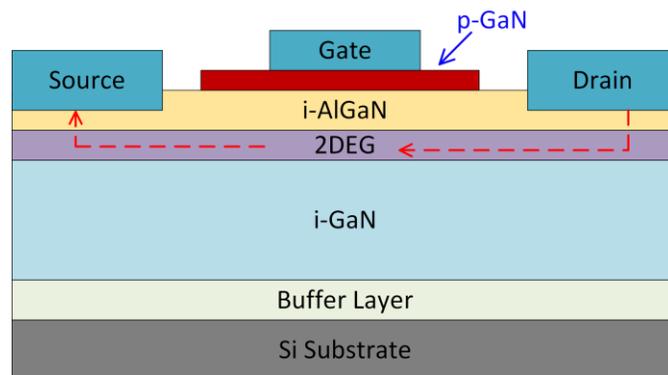


Figure 2.5: Schematic cross section of GaN-GIT

There are a few other techniques to construct normally-off GaN devices. One popular technique is to use a recessed gate where the AlGaN layer under the gate is etched out to break the normally-on 2DEG channel. Some manufacturers also use an insulation layer under the gate while others have developed alternative techniques to avoid the insulation layer. *Exagan*, *NEC*, and *HRL* use variants of recessed gate technique in their products. *GaN Systems* has not published the structure of their gate design yet [19].

Reverse Conduction in Lateral GaN

Silicon power MOSFETs conduct reverse current through their intrinsic body diode. But lateral GaN devices do not have a body diode for natural reverse conduction. There are three major techniques for conducting reverse current in e-mode GaN HEMTs. For a cascode structure, the body diode of the series MOSFET conducts the reverse current. Since the forward voltage drop of the diode is almost zero for the low voltage MOSFET, this voltage appears across the GaN gate and the d-mode GaN channel starts to conduct. This way a cascode GaN mimics the operation of a body diode.

An alternative approach is to add an antiparallel Schottky diode across the e-mode GaN for allowing reverse conduction of current. This approach may require a larger die but it can be a cheap solution for some applications.

The majority of e-mode GaN devices utilize an inherent property of the GaN called self-commutated reverse conduction (SCRC) [22]. Due to the symmetry of the device, the GaN channel conducts electricity when the gate to drain voltage (V_{gd}) exceeds a threshold ($V_{gd,th}$) under reverse biased condition. V_{gd} can be calculated by equation (2-3).

$$V_{gd} = V_{gs} - V_{ds} \quad (2-3)$$

The reverse conduction characteristics of an e-mode GaN is shown in Figure 2.6. It is apparent from the figure that an increased negative gate drive voltage will result in an additional voltage drop in the device during reverse conduction.

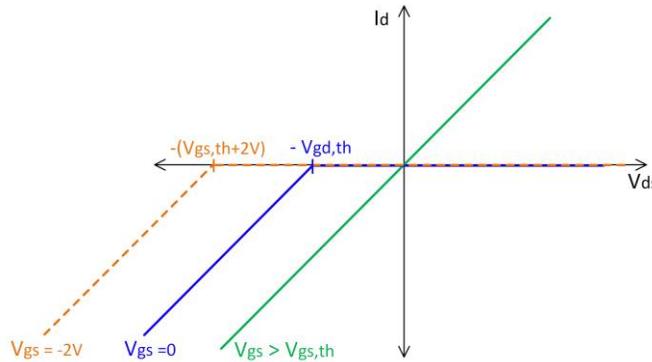


Figure 2.6: Reverse conduction characteristics of an e-mode GaN HEMT [22]

Compared to a traditional MOSFET, the reverse voltage drop of a GaN device is higher and accounts for additional loss into the device. It is possible that the device may end up over heating and eventually damaging the die if operated in reverse conduction mode for an extended period of time. Apart from the reliability issue, reverse conduction in GaN results in a rather poor efficiency. Therefore, it is often desirable to adopt the synchronous operation of GaN during reverse conduction. In synchronous operation, a gate voltage ($V_{gs} > V_{gs,th}$) is applied once the reverse current has transitioned properly.

Current Collapse

Current collapse due to dynamic $R_{ds(on)}$ is a well-known issue for Lateral GaN devices. Because of various construction limitations, the on-resistance of the device

increases over time and results in increased conduction loss. This phenomenon can potentially fail the device under normal operation due to thermal runaway. In [23] three major reasons have been mentioned that is responsible for the current collapse.

1. Trapping of electrons in the gate-drain surface that works as a virtual gate to weaken the 2DEG. A shrinking 2DEG channel increases the on-resistance of the GaN device. Since the electric field is strong near the drain region in a lateral device, some electrons remain trapped near the drain due to material impurities in the GaN structure and further contribute to the on-resistance rise.
2. Trapping of hot electrons in the carbon doped buffer region of the device.
3. Trapping of electrons in the gate insulator of Metal Insulator Semiconductor (MIS) HEMTs.

To mitigate the effect of trapped electrons, majority of the manufacturers use field plates to redistributing the electrons properly. Panasonic however has their unique approach of using a second p-doped drain that expels trapped electrons from that region.

2.2 Power Factor Correction (PFC)

2.2.1 ac-dc Power Conversion Architecture: Single and Two-Stage

An ac-dc power conversion architecture can either be single-stage or two-stage. In general, a power supply must draw a sinusoidal current in the input and guarantee a tightly regulated dc bus on the output while providing isolation between the source and load. In a two-stage approach, the front end of the power supply is a PFC that ensures sinusoidal input current. PFC stage is followed by a dc-dc converter that provides transformer isolation and maintains a tightly regulated output dc bus. Necessary modification of the output voltage level is performed in the dc-dc stage.

Figure 2.7 shows a conceptual structure of single-stage PFC. Electromagnetic compatibility (EMC) regulations like *IEC 61000-3-2* do not require the input current to be precisely sinusoidal, rather if the total harmonic distortion (THD) is within the limit, the

power supply meets the requirement. Therefore, a popular power conversion approach, especially at low power level, is a single-stage architecture. Here a passive LC filter is usually employed to shape the input current and reduce harmonics. After filtering, the voltage across energy storage capacitor C_b serves as the input stage for the following dc-dc stage. These two sub-stages are shown in Figure 2.7. There is only one control loop in this design that tightly regulates the output dc bus. So the intermediate energy storage capacitor voltage (V_b) is mostly unregulated in this architecture.

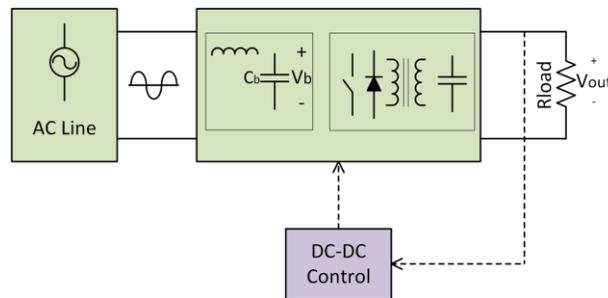


Figure 2.7: Conceptual representation of single-stage power architecture

A two-stage power supply architecture is shown in Figure 2.8. Here the power is processed through two consecutive stages of PFC and dc-dc converter. These stages are linked through a common dc bus which is loosely regulated by a PFC controller. Because there are two stages and two controllers in place, this architecture can be expensive compared to the single-stage approach. However, two-stage approach generally yields better efficiency. As the PFC and dc-dc stages operate separately, both of these can be highly optimized and efficient [24]. The input PFC stage can achieve unity power factor and the intermediate dc bus voltage being somewhat regulated keeps the dc-dc input voltage within a narrow range in the two-stage architecture.

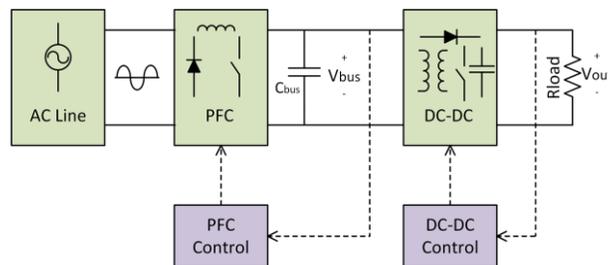


Figure 2.8: Conceptual representation of two-stage power architecture

The single-stage approach requires fewer active switches so it can be a cost effective solution. However, in a single-stage solution, unlike a two-stage approach, the energy storage capacitor voltage (V_b) is not loosely regulated but varies with the input

voltage. For a universal line input (90Vac-265Vac) the capacitor voltage can fluctuate between 130Vdc to 400Vdc. This wide voltage range requires a large and bulky capacitor for the single-stage approach. Majority of the modern day loads, including telecom and datacenter loads, require the power supply to maintain its output voltage within an operable range for a certain period of time after the dropout of the input ac line. This time interval is called hold-up time. A reasonable duration of hold-up time is necessary to ensure orderly termination of the electronic load or to transfer the power to a UPS. The duration of hold-up time directly influences the capacitor selection. The size of the intermediate bus capacitor in a two-stage architecture or the energy storage capacitor of a single-stage architecture can be calculated by equation (2-4) [24].

$$C = \frac{2 P_{out} t_{hold}}{V_{out(nom)}^2 - V_{out(min)}^2} \quad (2-4)$$

The hold-up time can be defined in different ways based on the application. A 10 ms hold-up time for nominal input voltage or 20 ms for minimum input voltage is commonly practiced values in many applications. For a minimum input of 90Vac, the two-stage power supply ensures a nominal output voltage of 400Vdc. The minimum output voltage in that case is usually kept around 300Vdc. For a single-stage approach, at 90Vac input, the input stage bus voltage is approximately 130Vdc. If the minimum bus voltage in this case is restricted at 90Vdc, it can be calculated from equation (2-4) that the approximate size of the energy storage capacitor is almost 8 times larger for a single-stage architecture than it is in a two-stage design.

In the single-stage approach, one set of switches performs the task of PFC and dc-dc conversion. At low input voltage, the energy storage capacitor voltage remains low, and the switches carry more current to maintain the same power level. This requires the power semiconductor switches to be rated for high current in a single-stage approach. High current rated switches increase the overall cost of the converter and cause additional conduction loss. In [25] it was also shown that the single-stage converter has a higher peak inductor current than the two-stage PFC converter. A high peak current warrants for a larger inductor which further reduces the efficiency and power density of the converter.

Though the single-stage power supply reduces the number of the semiconductor devices by eliminating the PFC power and control stage, it requires higher rated semiconductor devices and bulky passive components. Therefore, the single-stage

approach is only attractive for lower power levels (<100W). Two-stage architecture is the preferred architecture for high efficiency and power level.

2.2.2 Passive PFC Topologies

As the name implies, passive PFCs use passive elements to regulate the power factor to be typically between 0.7-0.85. To meet the terms of the IEC 61000-3-2 regulations, it is not necessary to have a unity power factor waveform. The requirements are in terms of harmonic content and as long as they are within the admissible limit, the product complies with the regulation [24]. Hence, the shape of the input current waveform can be very different from a sinusoid. In IEC 31000-3-2, the equipment is classified into four classes: A, B, C, and D. Class B is for portable equipment, Class C is for lighting equipment, Class D is only for TV sets, monitors, and computers. Finally, rest of all the equipment fit in Class A. Each Class has different requirements for allowable harmonics ranging from the 2nd to the 39th.

EMC compatibility requirements for Class B equipment are particularly stringent since they are intended to be used in the domestic environment. Most of the industry equipment fit into Class A and the requirements are less strict for them. This leaves the designers with the option to use passive PFCs to meet the IEC 61000-3-2 harmonic limits. For Class A equipment at low power level, passive PFC can be a viable solution. However, when the power level is high, a sinusoidal input current is almost always needed to meet the regulations [26] [27].

Passive PFCs are simple, reliable, sturdy, and generate less EMI than active PFCs. LC filters are a popular choice for passive PFC construction.

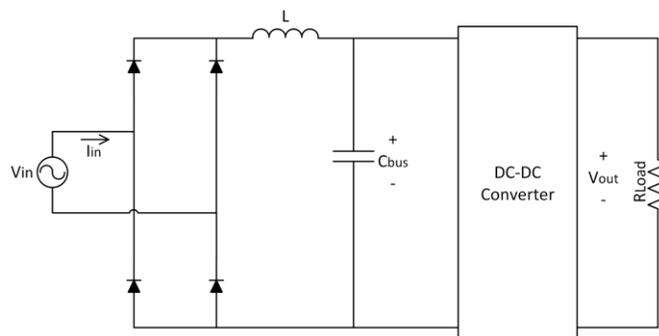


Figure 2.9: Two-stage passive PFC

In Passive PFC solution, the storage capacitor is selected based on a hold-up time which is usually 10-20 msec. For high power applications, the size of the bulk capacitor will be considerably big and expensive. Also when the input voltage range is wide, the design requires larger capacitors. Due to input voltage fluctuation, the output rail is often not regulated properly and requires a dc-dc stage for voltage regulation.

Though the passive PFC is inherently simple, it has some disadvantages. First, the bulkiness of added inductor restricts its inclusion into many applications. Second, a wide range of input voltage requirement limits the application of passive PFC circuits in many appliances. And finally, the loosely regulated dc rail in passive PFC output leads to a cost and efficiency penalty on the dc-dc converter that follows the PFC stage [7].

2.2.3 Active PFC Topologies

Active PFC utilizes active switching devices (Transistor, MOSFET etc.) in its design to regulate a sinusoidal input current and to keep the harmonics within the acceptable limit. This is why at high power levels active PFC is a popular choice. In recent years, the market trend of rising price of wire and magnetic materials and declining price of semiconductor materials have favored the application of active PFC in majority of the power supply solutions.

Popular active PFC topologies are some derivatives of traditional boost converter but the construction varies widely. The boost converter based design is favoured because in the boost converter, the filter inductor is on the input side, which provides a smooth continuous input current waveform as opposed to the discontinuous input current of the buck or buck-boost topology [28]. There are various competing boost converter based topologies available in this domain and the choice of the best topology depends largely on the application and design priorities. There often is a need to compromise between efficiency, power density, robustness, cost, and complexity in the course of designing a power supply and this often guides the selection of appropriate PFC topology [29].

Bridge PFC

In a traditional boost PFC topology, the input ac current is rectified by a diode bridge. As shown in Figure 2.10, the rectifier stage is followed by a boost converter to

shape the input current. The bridge PFC can operate in different modes such as continuous conduction, discontinuous conduction, and critical conduction mode.

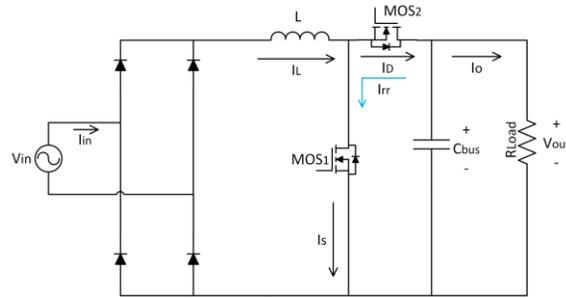


Figure 2.10: Bridge PFC

During the positive half cycle of the ac input voltage, MOS_1 is turned ON during the charging period and the inductor current rises to a certain value. The current path is shown in Figure 2.11 (a). As soon as MOS_1 is turned off, the inductor current commutates through the body diode of MOS_2 and charges the bus capacitor. To reduce the conduction loss, MOS_2 can be turned ON at this instant. Depending on the operation mode, the current in the discharging stage can be kept continuous or discontinuous. In the next switching cycle, MOS_1 is again turned ON and the body diode of MOS_2 blocks the total bus voltage after going through a reverse recovery.

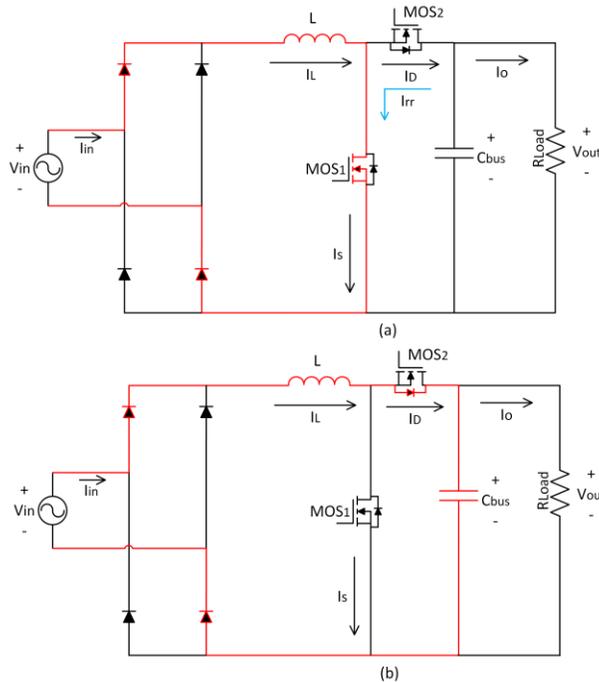


Figure 2.11: Positive half-cycle operation of the bridge PFC

Some major disadvantages with this topology are that the active MOSFET (MOS_1) is hard switched and the synchronous MOSFET (MOS_2) body diode has reverse recovery loss. The reverse recovery poses a great problem when the converter is operated at high frequencies. Beside efficiency loss, the adverse effect of the reverse recovery of the diode is responsible for poor EMC performance and additional thermal management. Numerous solutions have been proposed over the years to address this issue. Most of them suggest the inclusion of some form of active snubber to reduce the reverse recovery related losses and improve the EMC performance [30]–[32]. Another major drawback of this topology is, due to the presence of the diode bridge, the current path essentially includes as many as three semiconductor devices in both charging and discharging stage. Therefore, the converter efficiency is compromised due to excessive conduction loss, especially at low input voltage [11].

The introduction of wide band gap materials in power converters can reduce the reverse recovery loss associated with this topology and effectively eliminate the need for snubber circuits. On the other hand, the conduction loss issue has also led researchers to propose bridgeless boost-based rectifier topologies.

Bridgeless PFC

The dominant loss in active boost PFC converters is the conduction loss, specifically the conduction loss in the diode bridge rectifier. To further improve the PFC efficiency, the focus of many recent R&D efforts has been put on developing techniques that minimize this conduction loss in the converter. One very popular approach is the use of a bridgeless PFC boost converter. By eliminating the diode bridge rectifier from the input, the bridgeless PFC essentially increases the overall efficiency of the converter by reducing the number of semiconductor devices in the current path [33].

Basic Bridgeless PFC

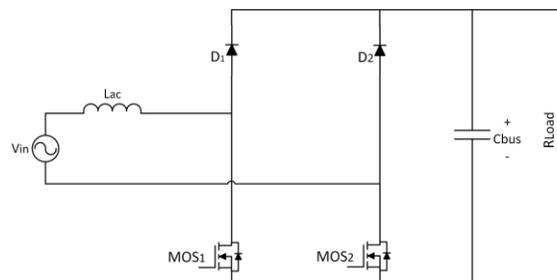


Figure 2.12: Basic bridgeless PFC

The basic bridgeless topology, as shown in Figure 2.12, was reported by the Texas A&M University's power electronics group back in 1993 [34]. This particular topology achieves significant efficiency gain by eliminating the diode bridge from the input stage. Since the inductor is placed on the ac side, this helps to shape the input current and contributes to the reduction of EMI. Both active switches being referred to the same ground makes the gate drive design relatively easier in this topology.

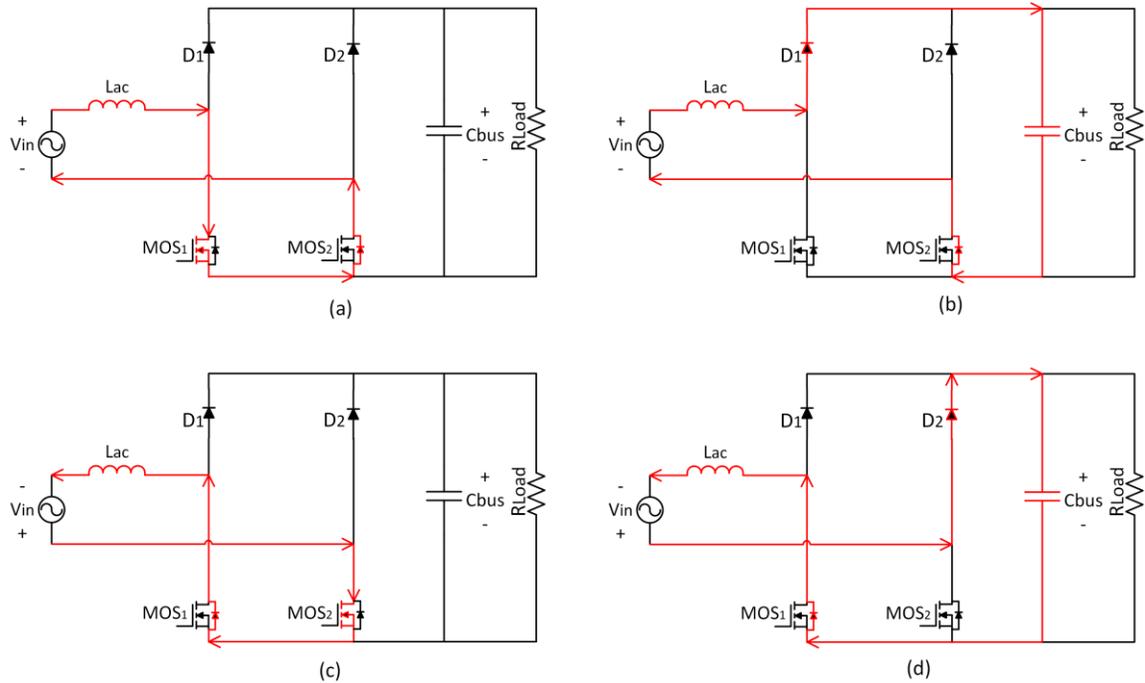


Figure 2.13: Positive and negative half cycle operation of basic bridgeless PFC

In each half cycle, one MOSFET works as the active switch of a boost converter. During the charging stage, the active MOSFET channel and the body diode of the other MOSFET conducts the electricity as shown in Figure 2.13 (a), (c). The active switch is turned OFF to freewheel the current through the diode during the discharging stage as shown in Figure 2.13 (b), (d). In the next switching cycle, as the active MOSFET turns ON again, the freewheeling diode goes through a reverse recovery.

A poor reverse recovery performance of the diodes can cause a significant increase in the switching power losses in this topology. It also causes a large amount of EMI noises, making the continuous conduction mode (CCM) operation of this topology impractical [35]. A fast recovery diode thus is preferred for this topology. All four semiconductor devices used in the basic bridgeless PFC must be fast switching

semiconductor devices in order to keep the magnetics size within a reasonable limit. This requirement introduces a downside as fast switching semiconductors typically exhibit higher $R_{ds(on)}$ leading to a trade-off between operating frequency and magnetics sizing. The implementation of basic bridgeless topology often requires isolated current and voltage sensing which introduces additional complexity and cost to the design [36]. Input current and voltage sensing is essential for implementing average current mode control or peak current mode control. The average current mode control is by far the most popular control method in basic bridgeless PFC because of its high performance and less complexity. In average current mode control, the controller multiplies the input voltage sine wave with the voltage loop output to generate the current reference while the current loop regulates the inductor average current to follow the reference. To avoid the design complexity of sensing circuits, *one cycle control* has been proposed in the literature [37].

The most significant difficulty with the basic bridgeless topology arises from its poor EMI characteristics. Larger CM chokes are usually required to meet the EMC standards in this topology which increases the cost and limits the power density of the converter. A detailed CM noise modeling of this topology, as shown in Figure 2.14, was described in [38]. In the bridgeless PFC topology, the output dc bus is always floating with respect to the input ac line. Thus, not only the parasitic capacitances between the MOSFET and the earth C_{d1} and C_{d2} , but also the parasitic capacitances between the output terminals to the earth C_n and C_p contribute to the CM noise [37].

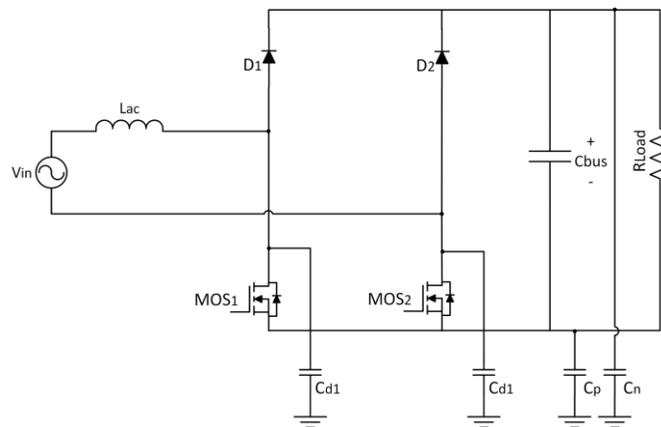


Figure 2.14: Basic bridgeless PFC with parasitic capacitors responsible for EMI

To overcome this problem, some have suggested using two capacitors in the input circuit, as shown in Figure 2.15, to create a high-frequency bypass path between the ac line and the ground. But this solution can only be implemented when the topology is using

split inductors or coupled inductor. If there is only a single inductor in the design, one of the bypass capacitors will appear across the MOSFET to essentially make its switching speed too slow. Further improvement of this topology in terms of CM noise was proposed in [39].

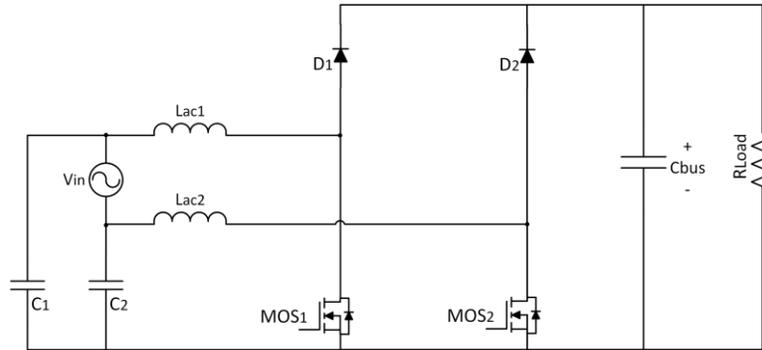


Figure 2.15: Basic bridgeless PFC with capacitor bypass

Semi-Bridgeless PFC

To reduce the problem of high CM noise in traditional bridgeless PFC structure, a new topology was developed and used in industry. The semi-bridgeless topology uses two diodes to essentially clamp the ac input lines to the output dc-bus during the positive and negative half cycles respectively.

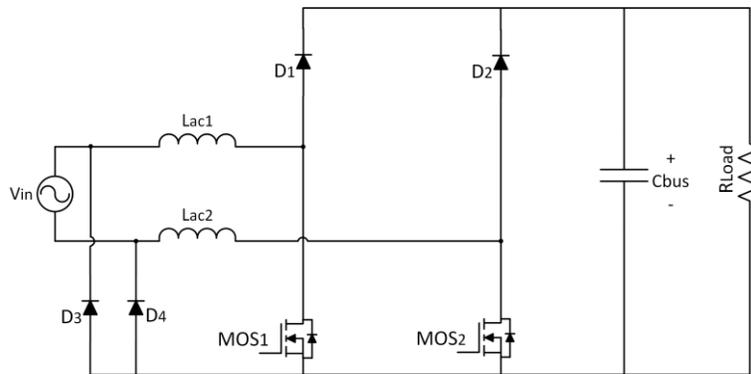


Figure 2.16: Semi-bridgeless PFC

The semi-bridgeless topology, as shown in Figure 2.16, needs two inductors, which are sometimes realized as coupled inductors, in its input line. During the positive half cycle operation of the converter, slow diode D_4 clamps the high-frequency ac line to the ground node. During the negative half cycle, slow diode D_3 performs the same task.

The semi-bridgeless topology can achieve very high performance but it needs more components and the problem of diode reverse recovery is inherited from the basic bridgeless topology. This topology incorporates four fast devices (D_1 , D_2 , MOS_1 , MOS_2) which limits the peak efficiency. Two inductors are needed in the design as compared to one in the basic bridgeless topology. The extra inductor helps with better heat dissipation but it adds to the overall cost and weight of the power supply. Another major drawback of this topology is the low utilization of switches and magnetic components [40]. In order to improve utilization of magnetic material, the common-core inductor is proposed in [41].

Dual Boost Bridgeless PFC with Bidirectional Switch

To address the high CM noise problem, a bridgeless PFC was developed with a single inductor and two diodes added to clamp the bus [42].

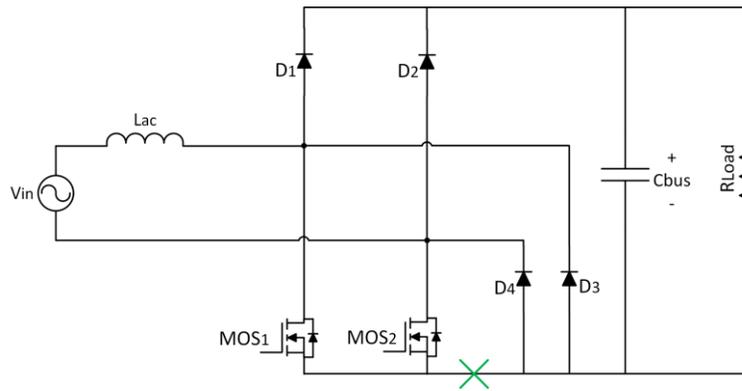


Figure 2.17: Dual boost bridgeless PFC with reduced EMI

The common diode node in the topology shown in Figure 2.17 can be disconnected from switches MOS_1 and MOS_2 . Based on this idea, a new PFC topology was proposed in [43].

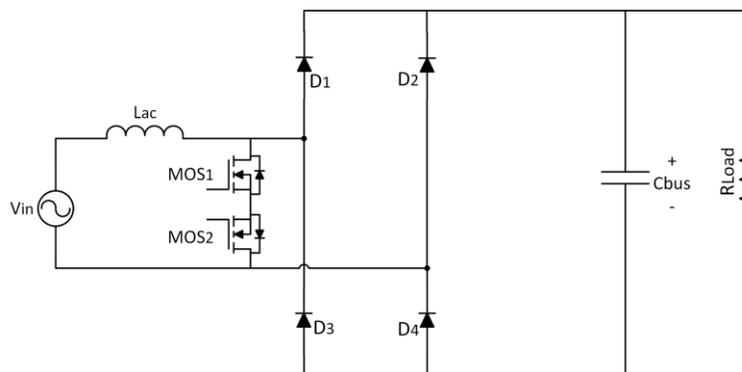


Figure 2.18: Dual boost bridgeless PFC with bidirectional switch

In the dual boost bridgeless PFC with bidirectional switch topology, as shown in Figure 2.18, D_1 and D_3 are fast recovery diodes, whereas D_2 and D_4 are slow diodes. During the positive half cycle, MOS_1 turns ON during the charging stage. As shown in Figure 2.19 (b), when MOS_1 is turned OFF, the current flows through the diodes D_1 - D_4 to charge the bus capacitor. During the negative half cycle, MOS_2 is operated in the similar PWM manner to perform the PFC operation.

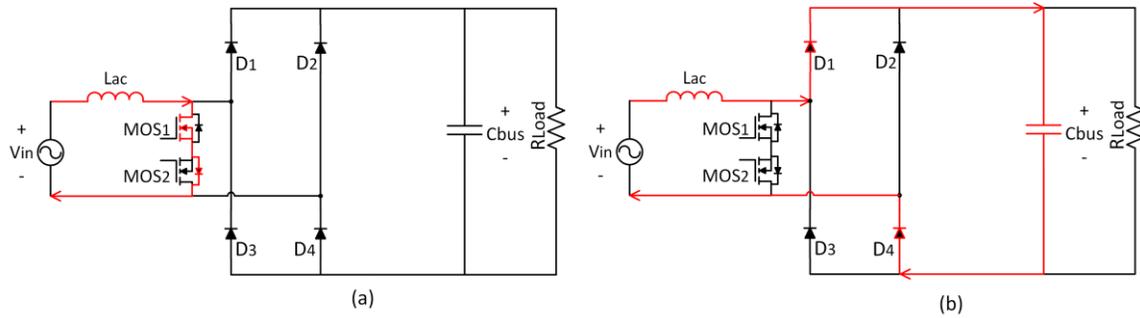


Figure 2.19: Positive half cycle operation of dual boost PFC with bidirectional switch

Neither of MOS_1 or MOS_2 is referenced to the dc ground in this design. As a result two isolated gate supplies are required to operate the MOSFET gate drivers. This is a drawback of this topology because of the additional cost of the isolated supply. Moreover, this topology uses two extra diodes and four high-frequency semiconductor devices as compared with the other solutions. This combination of additional high frequency power devices limits the peak efficiency.

Pseudo Totem-Pole Bridgeless PFC

Another variation of the bridgeless PFC topology, as shown in Figure 2.20, was proposed in [44], [45]. Because of the specific arrangement order of MOS_1 and MOS_2 in Figure 2.20, this topology is called a pseudo totem-pole PFC.

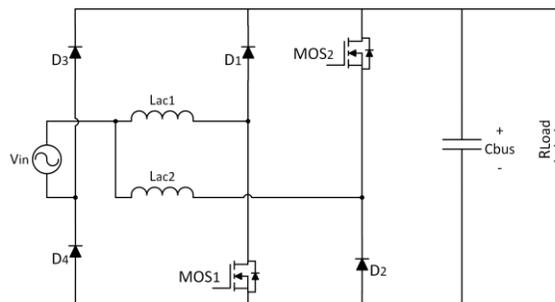


Figure 2.20: Pseudo totem-pole bridgeless PFC

During the positive half cycle of the input ac voltage, the current flows through MOS_1 and D_4 during the charging state. The current is discharged through D_1 - D_4 in the subsequent switching instance. During the negative half cycle, MOS_2 is turned ON and OFF to charge and discharge the inductor. In this topology, MOS_1 and MOS_2 cannot be operated with the same PWM signal. Since MOS_2 is a high-side switching device, it needs an isolated gate drive or bootstrap supply to operate. This may limit the practical implementation of this circuit.

Three Level PFC with Nature Voltage Clamp

The single phase three-level PFC was never a very popular topology for practical implementations partly because of the unavailability of high voltage rated devices. With the advent of WBG devices, this scenario is set to change in the near future. Nonetheless, there already are some promising three-level topologies in existence that were proposed in the literature over the years. In [46], such a three-level PFC topology with two inductors was presented that can achieve zero voltage turn-on.

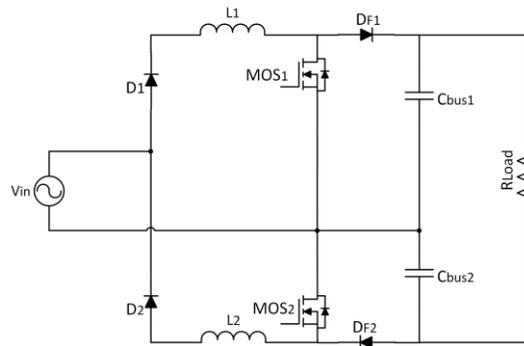


Figure 2.21: Three-level boost bridgeless PFC rectifier

By placing the inductor in line with the ac input, a variation of this topology was presented in [47]. Utilizing a principle called *nature voltage clamping*, this topology, as shown in Figure 2.22, can ensure half of the output bus voltage stress across all devices including diode D_{f1} and D_{f2} .

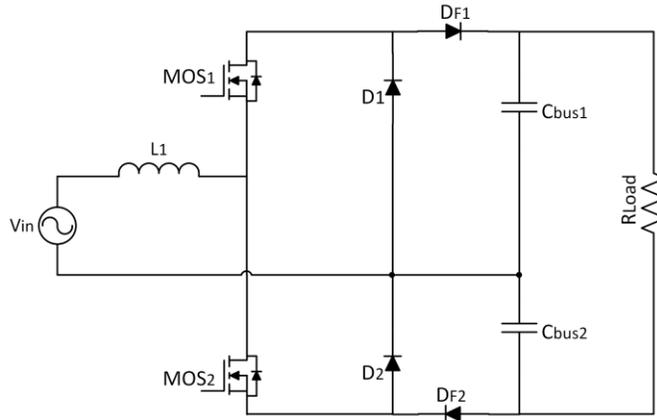


Figure 2.22: Three-level PFC with nature voltage clamp

The topology needs two fast diodes D_{f1} and D_{f2} . During the positive half cycle, when MOS_2 turns ON, the inductor current is charged. During the transition period between switching, both D_{f1} and MOS_1 body diode starts to go reverse biased. Since D_{f1} is faster, it goes through reverse recovery quicker than MOS_1 body diode and blocks the whole V_{o1} voltage as shown in Figure 2.23 (a). Due to the natural clamping of MOS_1 body diode, D_{f1} only blocks V_{o1} , not the whole dc bus voltage. During the discharge stage, slow diode D_2 is nature clamped to ensure that MOS_2 blocks only half the total bus voltage.

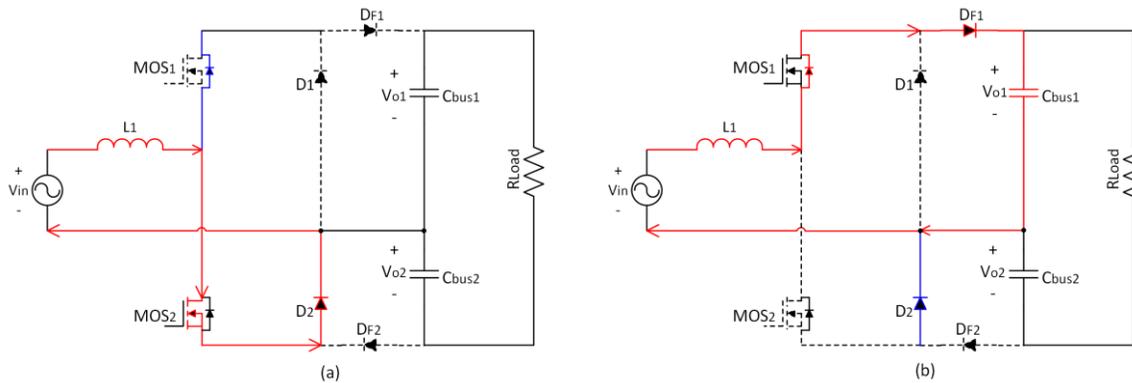


Figure 2.23: Positive half cycle operation of three-level nature voltage clamp PFC

The three-level nature voltage clamp PFC topology has an output bus voltage twice that of the traditional bridgeless PFC. This means the output bus current is lower than in the other topologies and conduction losses are reduced in the following dc-dc converter. But the higher bus voltage can be a limiting factor too. Since in the two-stage architecture, the PFC stage is followed by a dc-dc stage, and the higher dc bus voltage means the dc-dc stage will require higher rated, more expensive and less efficient devices. Since one of the switching devices is on the high-side in this topology, the gate drive circuit

needs an isolated supply. The device count is also higher than other topologies. Due to the presence of two bus capacitors at the output, the voltage balancing is an inherent difficulty with this topology. Finally, D_{f1} and D_{f2} have to be diodes with less reverse recovery charge to ensure better efficiency. Traditional silicon diodes are not suitable for this topology but it can potentially be an appropriate choice for introducing WBG devices, especially for high power applications.

Single phase Voltage Doubler PFC

A single-phase three-level voltage doubler converter was proposed in [48] which can maintain high bus voltage whilst controlling the rectifier input current wave shape to achieve unity power factor.

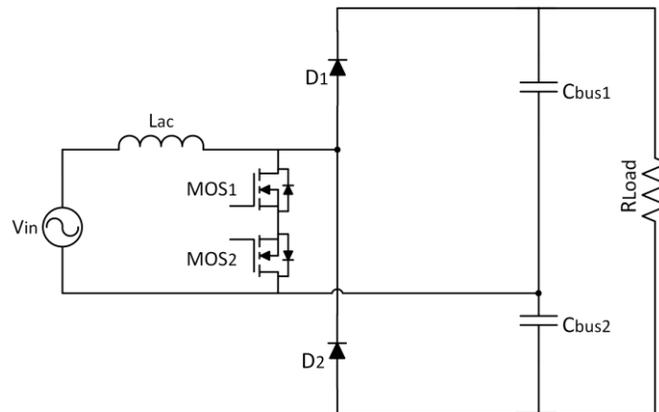


Figure 2.24: Voltage doubler PFC

During the positive half cycle operation, MOS_1 is turned ON and the current flows through MOS_1 channel and MOS_2 body diode to charge the inductor. During the discharge period, the inductor current freewheels through the diode D_1 to charge the bus capacitor C_{bus1} . Only this one capacitor is charged over one positive half cycle. Similarly, during the negative half cycle, C_{bus2} is charged. Total bus voltage is two times the capacitor voltage value. Though the output bus voltage is high in this topology, the device stress on each MOSFET is half the bus voltage. The diodes however have to withstand the whole dc bus voltage. The operation of the three level voltage doubler topology during the positive half cycle is shown in Figure 2.25.

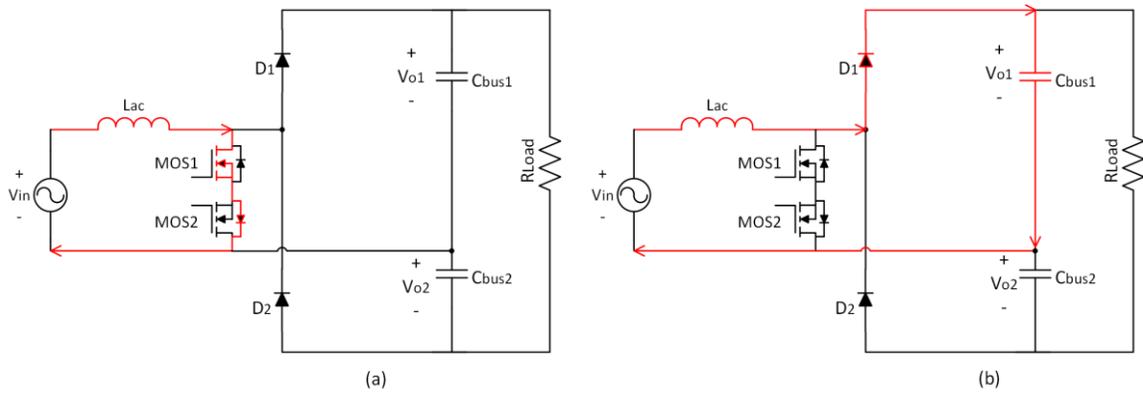


Figure 2.25: Positive half cycle operation of voltage doubler PFC circuit

Since the discharge current flows through only one device, three-level voltage doubler PFC topology accounts for significantly low conduction loss. Due to the high bus voltage, the current is small on the output side, which can further improve the efficiency of the following dc-dc converter stage. One major challenge in this topology is the selection of appropriate diodes. First of all, the freewheeling diodes have to be rated for twice the usual voltage. High voltage Si-diodes suffer from additional forward voltage drop and generally exhibit poor reverse recovery performance. Hence it is almost impractical to implement this topology using Si-diodes. Some literature have proposed solutions to reduce the reverse recovery current in this topology by adding passive snubbers [49], [50]. But these solutions account for additional cost and reduce the power density of the system. With the advent of 1200V rated SiC devices, three-level voltage doubler PFC topology can be an interesting choice to explore especially for high power applications.

Totem-pole PFC

Totem-pole PFC is a modification of the basic bridgeless PFC topology. The structure is very simple with two active switching devices placed in a half-bridge to form a high-frequency switching leg. The other half-bridge leg transitions at line frequency and can be implemented by two diodes. Totem-pole PFC requires only two high-frequency semiconductor devices as opposed to four for other bridgeless topologies. This enables the totem-pole topology to potentially achieve very high power density with a lower cost of materials.

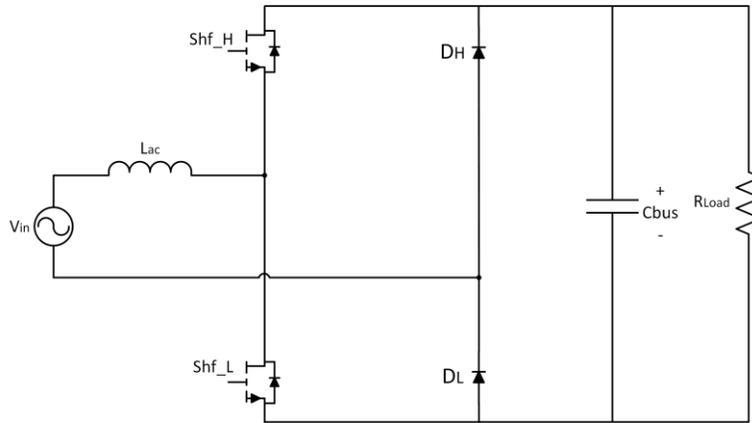


Figure 2.26: Totem-pole PFC

Though this topology can yield theoretically superior efficiency and power density, it is very challenging to achieve that by using traditional Si-MOSFETs. This is because, in CCM operation, the high-frequency devices switch under hard-switching conditions and suffer from severe reverse recovery problem of the MOSFET body diode [51]. This is why totem-pole PFC has traditionally been operated under critical conduction mode [52][53]. But critical current mode operation does not harness the full potential of this topology and introduces additional noise to the system. Newly emerging WBG semiconductor devices can be a perfect match for this topology since they have almost zero reverse recovery. Relatively smaller switching loss in WBG devices makes them particularly suitable for CCM operation in totem-pole PFC.

2.3 PFC Topologies Using WBG Semiconductors

2.3.1 Suitable PFC Topologies for WBG Application

The objective of this section is to identify the appropriate PFC topology for the next generation telecom power supplies incorporating wide-bandgap devices. The telecom sector requires very efficient power supplies with high power density. The power architecture is predominantly two-stage in telecom power supplies for high efficiency. So, while selecting the PFC topology, the implications of the selected topology on subsequent dc-dc stage were considered too. Since the bridgeless PFC topologies ensure very high efficiency, the initial selection of competing designs were some variants of bridgeless topology but the focus was to introduce WBG devices in the design for harnessing maximum efficiency.

Semi-bridgeless PFC topology is currently the popular topology for telecom power supplies because of its high efficiency and less expensive material cost. The advent of WBG devices however enables other bridgeless topologies to be designed with considerably high efficiency. In the remainder of this section, a comparison between such three topologies is presented.

Totem-pole PFC has been discussed in the literature for its potential to be a high-efficiency topology. Unlike most designs, this topology requires only two high-frequency semiconductor switches. This certainly is a less expensive solution with the potential to increase the switching frequency. Before the availability of WBG devices, it was impossible to design a high-efficiency totem-pole PFC with Si-MOSFETs because of the significant reverse recovery loss in the body-diode. Since GaN devices with very small reverse recovery charge are commercially available now, it makes totem-pole PFC a prospective choice for high-efficiency power supply design.

Similarly, three-level topologies are good choices for high-efficiency, high-power PFC solutions. The three-level nature voltage clamp (NVC) topology presented in section 2.2.3 is selected for comparison with totem-pole PFC here. This topology does not yield high efficiency with silicon devices. However, with the advent of 600V SiC diodes, three-level NVC topology certainly presents a new option.

Three-level voltage doubler topology presented under section 2.2.3 is a suitable topology for introducing WBG devices. This design has been abandoned by the researchers because of its poor efficiency with silicon technology. With WBG devices, this topology has the potential to reach its full efficiency. Three-level voltage doubler topology requires 1200V rated SiC diodes. Since SiC is a fairly matured technology at this voltage level, it was considered worth comparing the efficiency of the three-level voltage doubler topology against other competing designs.

2.3.2 Comparison

This section compares the performance of three selected topologies – Totem-pole PFC, three-level NVC, and three-level voltage doubler based on simulation. For further increasing the efficiency, few modifications have been made in device selection and switching technique. Circuit diagrams of these topologies are presented in Figure 2.27.

The totem pole PFC is evaluated with both GaN and SiC FETs. For better efficiency, the diode leg of three-level NVC is replaced with MOSFET. In both three-level topologies, synchronous switching is enabled to minimize the MOSFET body diode conduction loss.

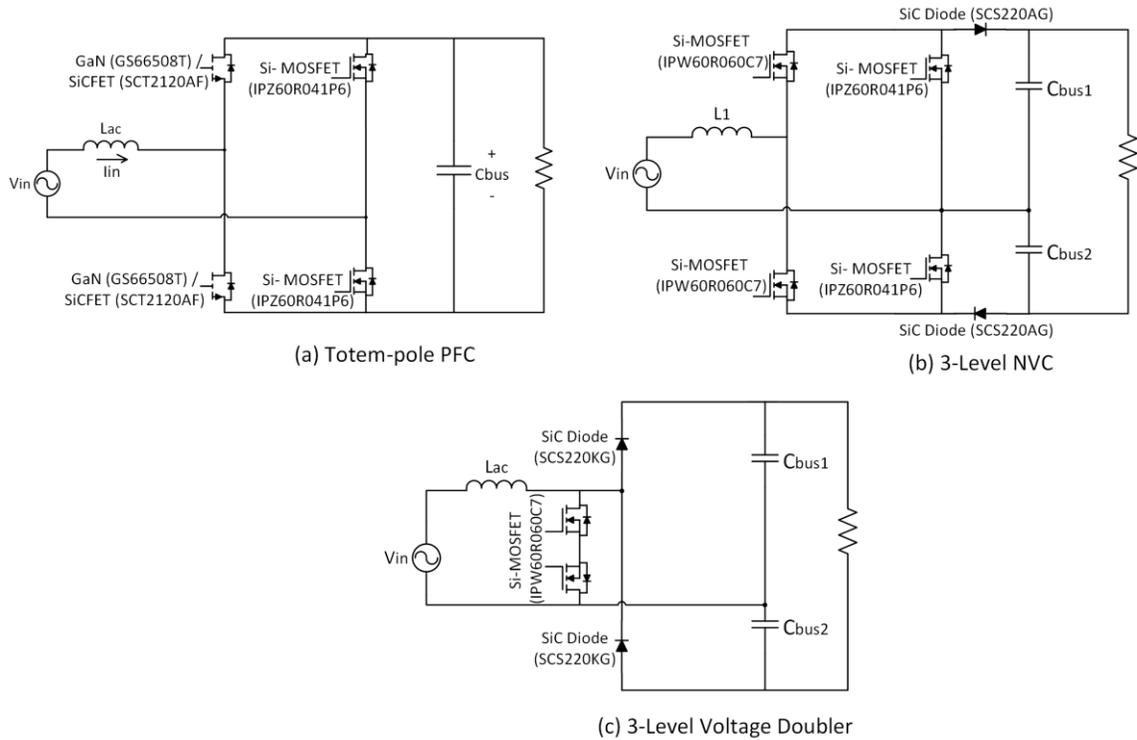


Figure 2.27: PFC topologies for efficiency comparison

Each of the selected topologies incorporates a pair of high-frequency switches. For totem-pole PFC, the high-frequency switches must be wide-bandgap devices to minimize the reverse recovery current. GaN HEMT (GS66508T) manufactured by GaN Systems and SiC FET (SCT2120AF) manufactured by ROHM have been used for this purpose. Both three-level topologies require high-frequency SiC diodes but the voltage ratings for the diodes are different. The high-frequency switch in both three-level topologies is implemented by *Infineon* C7 MOSFETs. Key parameters for the switching devices are presented in Table 2-2. It is evident from the parameters that wide-bandgap semiconductors such as GaN and SiC have superior reverse recovery characteristics. Due to the low parasitic capacitance, the GaN device can switch significantly faster than others.

Table 2-2: Key datasheet parameters for selected switching devices

Description	GaN GS66508T	SiCFET SCT2120AF	MOSFET IPW60R060C7	MOSFET IPZ60R041P6
Breakdown voltage (V)	650	650	600	600
On-resistance, $R_{ds(on)}$ (m Ω)	75	130	75	55
Diode on-resistance (m Ω)	125/80**	125	23.3	110
Diode threshold voltage (V)	1.9	1.5	0.55	0.55
Input capacitance, C_{iss} (pf)	260	1200	2850	8180
Output capacitance, C_{oss} (pf)	65	90	54	150
Reverse transfer capacitance, C_{riss} (pf)	2	13	11	20
Reverse recovery charge, Q_{rr} (nC)*	~ 0	~ 53	~ 3500	~ 4300

Note: *Normalized for 10A forward current. **Reverse conduction of channel. All parameters are calculated for 75°C

The inductor is calculated for 1.5 kW output power and the same inductor model is used for all simulations. The value of the inductor is 237.5 μ H with an equivalent series resistance (ESR) of 55 m Ω . Nominal dc bus voltage is 385 V for totem-pole PFC and 770 V for three-level topologies where each bus capacitor is assumed to be 600 μ F. The switching frequency is kept at 100 kHz for all applications. A comparison of simulated efficiency over a wide range of power is shown in Figure 2.28.

It is apparent that the totem-pole PFC using GaN devices shows better efficiency even at 100 kHz switching frequency. Totem-pole PFC using SiC is slightly less efficient at full load, primarily because the SiC FET body diode suffers from a small reverse recovery loss. In many applications, a SiC Schottky barrier diode (SBD) is placed in parallel with the FET to eliminate that small reverse recovery [54]. Some manufacturers commercialize SiC FETs with a parallel SiC SBD within the same package (e.g. *SCH2080KE* from *ROHM*).

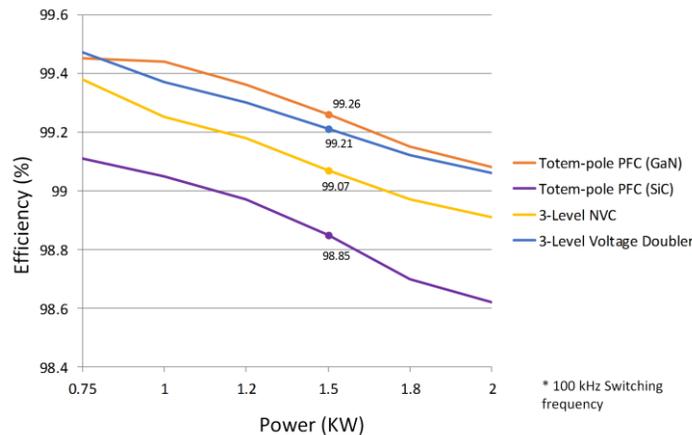


Figure 2.28: Simulation-based efficiency comparison between different PFC topologies using WBG devices

Both three-level topologies show good performance primarily due to very small reverse recovery loss on the SiC diodes. The three-level voltage doubler circuit is particularly efficient because, unlike other topologies, its current freewheeling path consists only one device. The three-level NVC circuit requires two extra devices, so the overall circuit has less power density. Both three-level topologies require additional capacitors to keep the dc bus voltage constant. This eventually decreases the power density of the system. In practice, the three-level topologies can potentially encounter an imbalanced dc bus mid-point voltage which may result in erroneous operation of the PFC. Controlling the dc bus mid-point voltage therefore poses additional challenge for the three-level topologies while the totem-pole PFC control is very simple. For an 800V output dc bus of a three-level PFC, the subsequent dc-dc converter devices have to be rated for high voltage.

A totem-pole PFC using GaN is thus preferable for high efficiency and high power density applications. Three-level topologies, especially three-level voltage doubler PFC may find ground in high power applications where an 800V bus is advantageous. For next generation telecom power supply (< 5 kW), a totem-pole PFC using GaN HEMT is therefore considered the appropriate topology in this work.

Chapter 3. Totem-pole PFC

This chapter discusses the operation of totem-pole PFC and various design constraints and challenges associated with this topology.

3.1 Operation

The totem-pole PFC is a boost converter derived topology. It essentially utilizes two boost converters during each ac line voltage half cycle. The totem-pole topology includes two half-bridge legs. One half-bridge switches at high switching frequency and is denoted as the high-frequency (HF) leg. The other half-bridge switches at the line frequency and is denoted as the low-frequency (LF) leg. A totem-pole PFC is shown in Figure 3.1.

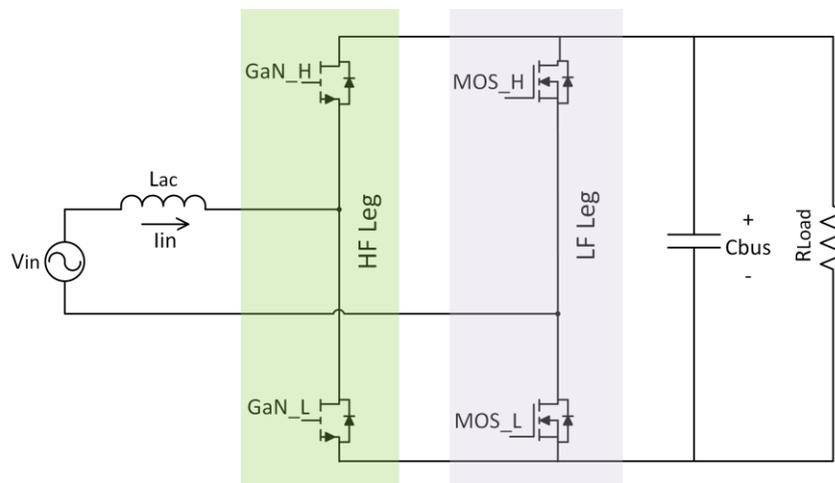


Figure 3.1: Totem-pole PFC

The high-frequency switching devices are hard switched in this topology when the PFC works in continuous conduction mode. Wide-bandgap semiconductor devices are particularly suitable for the HF leg construction since they have almost zero reverse recovery charge (Q_{rr}). Two GaN HEMT devices are used to implement the HF leg in this work. This particular arrangement of the high-frequency switching devices in one half-bridge leg is reflected in the name 'Totem-pole'. The devices are marked either high-side (GaN_H) or low-side (GaN_L) based on their relative position from the negative dc bus.

The low-frequency leg of the totem-pole PFC topology can be implemented with two regular silicon diodes. The diode has a high forward drop during normal operation and results in poor efficiency. Since MOSFETs suffer from smaller conduction loss compared to regular diodes, to improve the overall efficiency, a Si-MOSFET half-bridge is preferred for constructing the LF leg. As the switching frequency of the LF leg is only 60Hz (or 50Hz based on the power grid), a slow MOSFET with significantly lower $R_{ds(on)}$ can be used to further improve the efficiency.

3.1.1 Positive Half Cycle Operation

During the positive half cycle of the ac line voltage, the low-side switch GaN_L operates at high frequency and acts as the active switch of a boost converter. When GaN_L is turned ON with a calculated duty, the total input voltage V_{in} is applied to the inductor and positive inductor current builds-up. This operation is shown in Figure 3.2 (a). Low-side switch MOS_L is kept ON during this period to minimize the conduction loss.

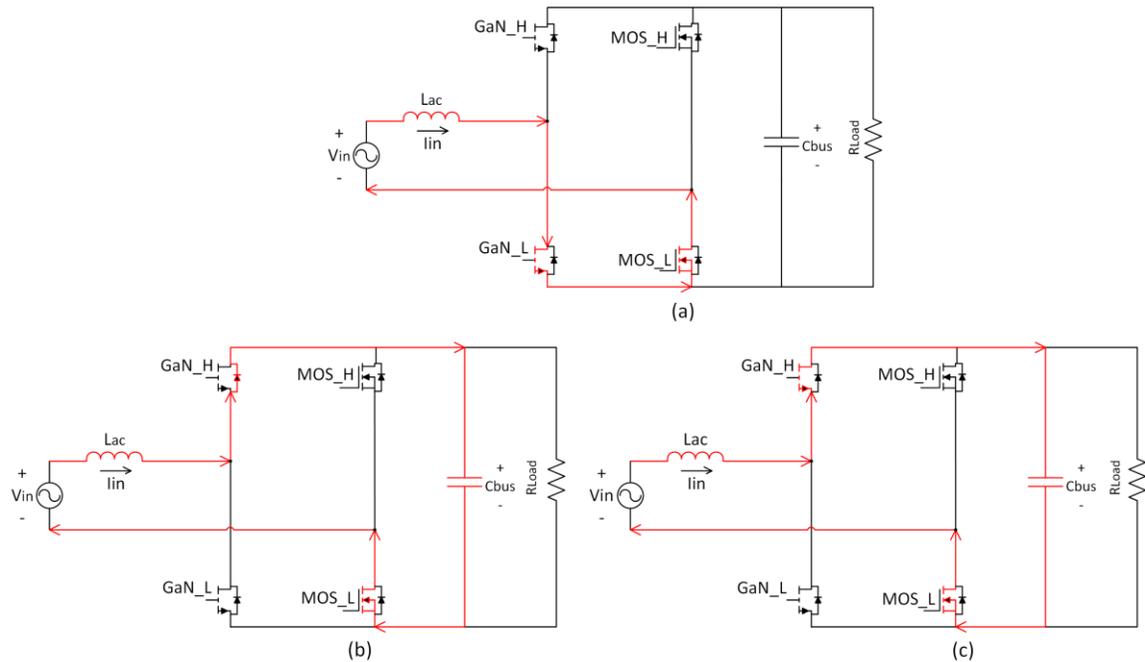


Figure 3.2: Positive half cycle operation of totem-pole PFC

After the calculated duty period, GaN_L is turned OFF and the inductor current freewheels through the high-side GaN_H diode. Throughout the freewheeling period, inductor delivers its stored power to the output dc bus as shown in Figure 3.2 (b). For synchronous switching, GaN_H is turned ON during this period and the freewheeling

current transfers to the GaN_H channel in zero-voltage switching (ZVS) manner to minimize the conduction loss. This instance is shown in Figure 3.2 (c). During synchronous operation of the high-frequency leg, GaN switches operate in a complimentary fashion. A deadtime is provided between the switching to avoid shorting of the dc bus

When the low-side GaN_L is turned ON again after the freewheeling period, inductor current commutates from the GaN_H diode to the GaN_L channel. If silicon MOSFETs are used in place of GaN HEMTs in the HF leg, a reverse recovery current will flow during this transition period and result in reduced efficiency. This problem essentially curtails the possibility of using a Si-MOSFET for the HF leg, making wide-bandgap semiconductor devices the only suitable candidate.

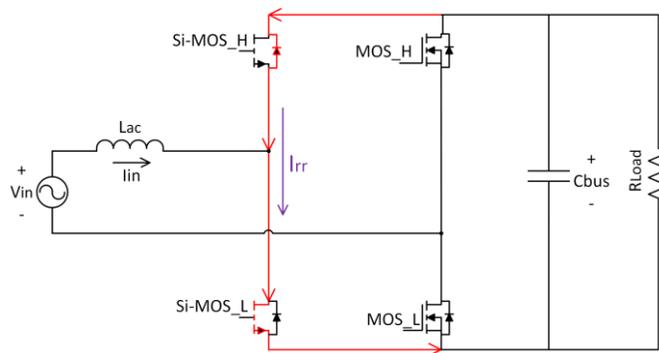


Figure 3.3: Reverse recovery current flow for Si-MOSFET

Switching frequency of Si-MOSFET depends on the amount of gate charge Q_g . A smaller gate charge means the device can be switched at a higher frequency. However, the higher the gate charge, the lower the on-resistance $R_{ds(on)}$ will be [55]. Since the LF leg operates only at the line frequency, slow MOSFETs with smaller $R_{ds(on)}$ can be selected for the LF leg to improve the efficiency of the PFC. Since only two devices conduct at a given interval during the operation of this PFC topology, it yields better efficiency compared to traditional full bridge based PFC.

3.1.2 Negative Half Cycle Operation

During the negative half cycle, GaN_H operates as the active switch. When GaN_H is turned ON with the calculated duty period, the negative inductor current rises linearly as shown in Figure 3.4 (a). For the entire duration of negative half cycle, high-side MOS_H is kept ON. As soon as GaN_H is turned OFF after the charging duty period, the inductor current freewheels through MOS_H to the dc bus and returns through the GaN_L

diode. For synchronous operation, GaN_L can be turned ON at this instance. If the low-side switch of the HF leg has a reverse recovery, there will be a reverse current flowing through the HF leg in the next switching cycle.

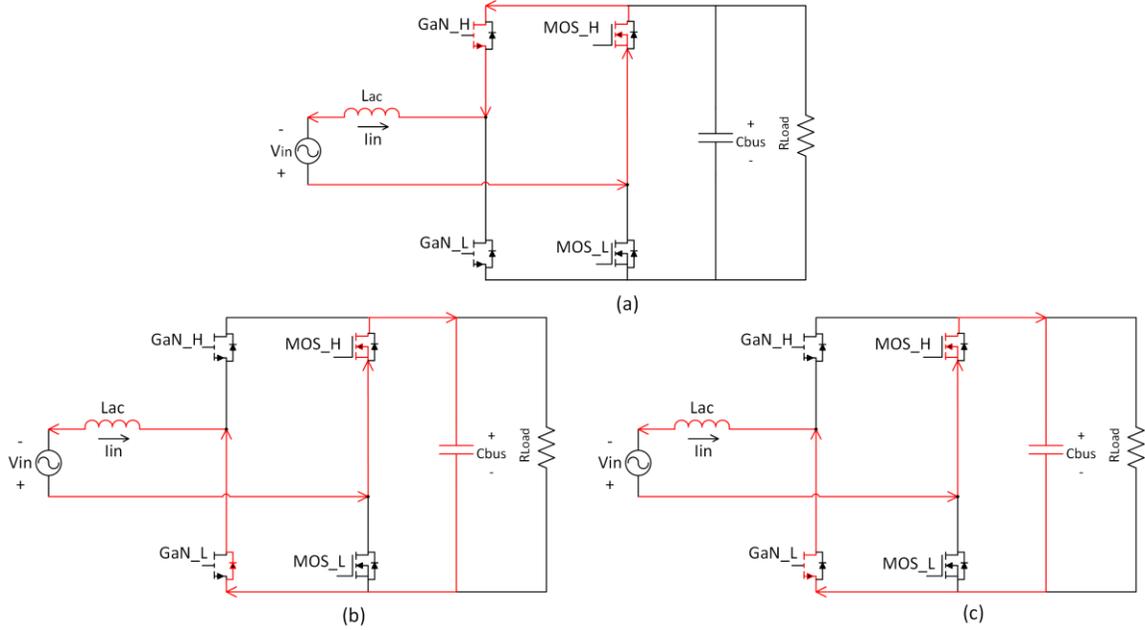


Figure 3.4: Negative half cycle operation of totem-pole PFC

3.2 Simulation-Based Study

A simulation of totem-pole PFC was performed in PSIM simulation software. The schematic of the simulation circuit is provided in Figure 3.5.

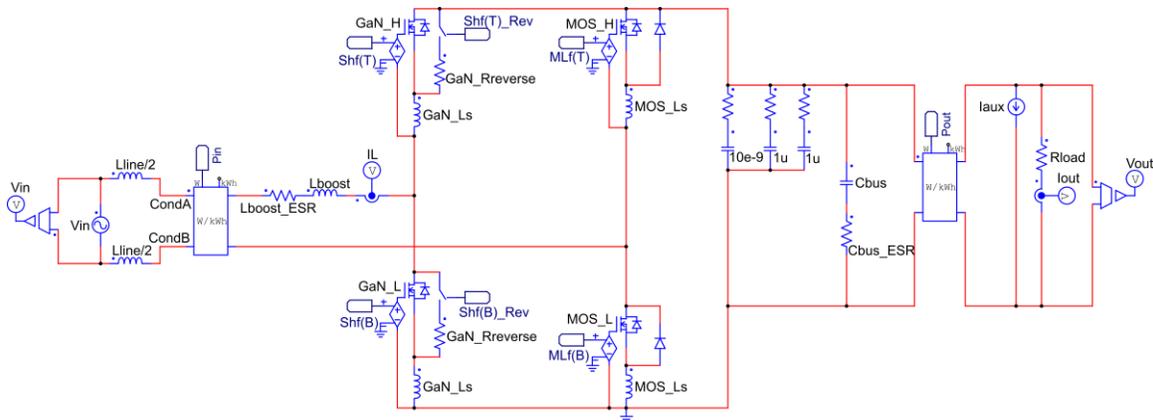


Figure 3.5: Totem-pole PFC simulation circuit

Since GaN HEMT devices are not available in PSIM, a 3-state MOSFET with GaN HEMT parameters as shown in Table 2-2 was used to replicate the GaN characteristics.

Simulation results are shown in Figure 3.6. From the waveforms, it is evident that the inductor current is in phase with the input voltage. So the PFC works with almost unity power factor while maintaining a stable output dc bus.

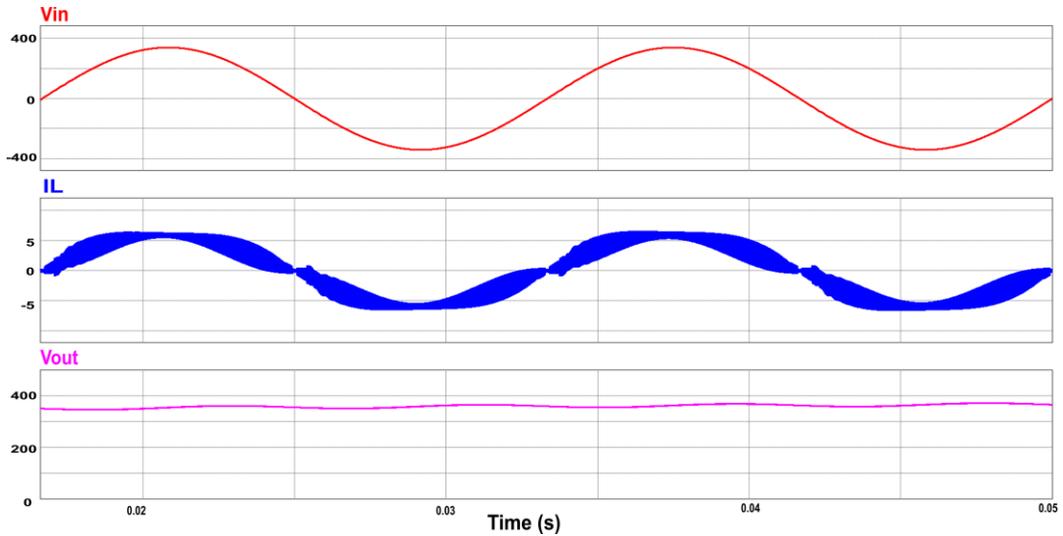


Figure 3.6: Totem-pole PFC simulation waveforms

The simulation model was operated under both non-synchronous and synchronous switching and the efficiency was tabulated. A comparison of the efficiency curve as shown in Figure 3.7 confirms that the synchronous operation yields better efficiency.

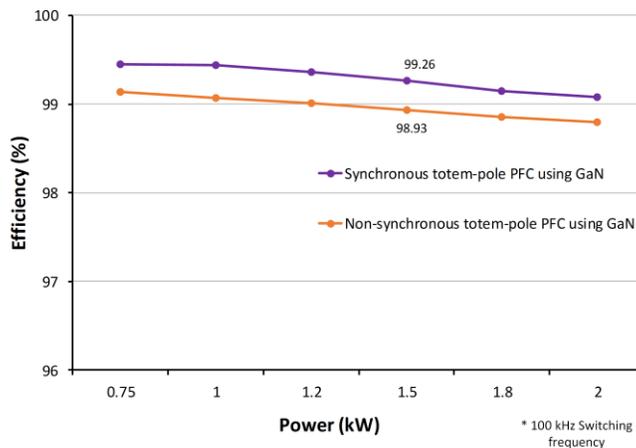


Figure 3.7: Simulation-based efficiency comparison

3.3 Common-Mode Noise

Switching power supplies are a major source of noise. Bridgeless PFCs are particularly prone to generate CM noise. Totem-pole PFC is considerably noisier than a traditional bridge type PFC. Especially around the zero-crossing of the converter, significant amount of CM noise is observed.

To facilitate the analysis of CM noise in totem-pole PFC, a CM noise model is developed in [56] by TDK-Japan. For most of the North American power distribution network, this model requires some minor modification. A *split-phase* system, also known as *single phase three wire* system is generally used in North American power distribution. In this system, the secondary winding of the transformer is center-tapped and the neutral is physically grounded as shown in Figure 3.8. Small household loads are typically connected between line to neutral (120V) and heavy loads are connected between line to line (240V).

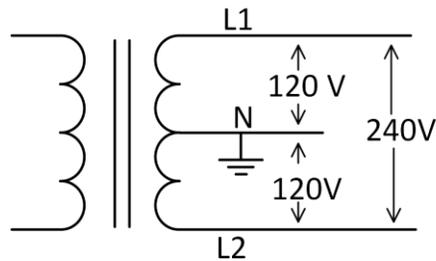


Figure 3.8: Split-phase power supply

The connection of the input stage PFC of a power supply module is shown in Figure 3.9 (a). As emphasised, the neutral of the supply line is physically grounded in this adapted model. A simplified version of this circuit is shown in Figure 3.9 (b). Here, C_{fg} is the frame to ground capacitance of the power supply unit. Any change in voltage (V_{fg}) across this capacitor will inject CM noise current into the ground (I_{fg}) and this will increase the overall conducted noise.

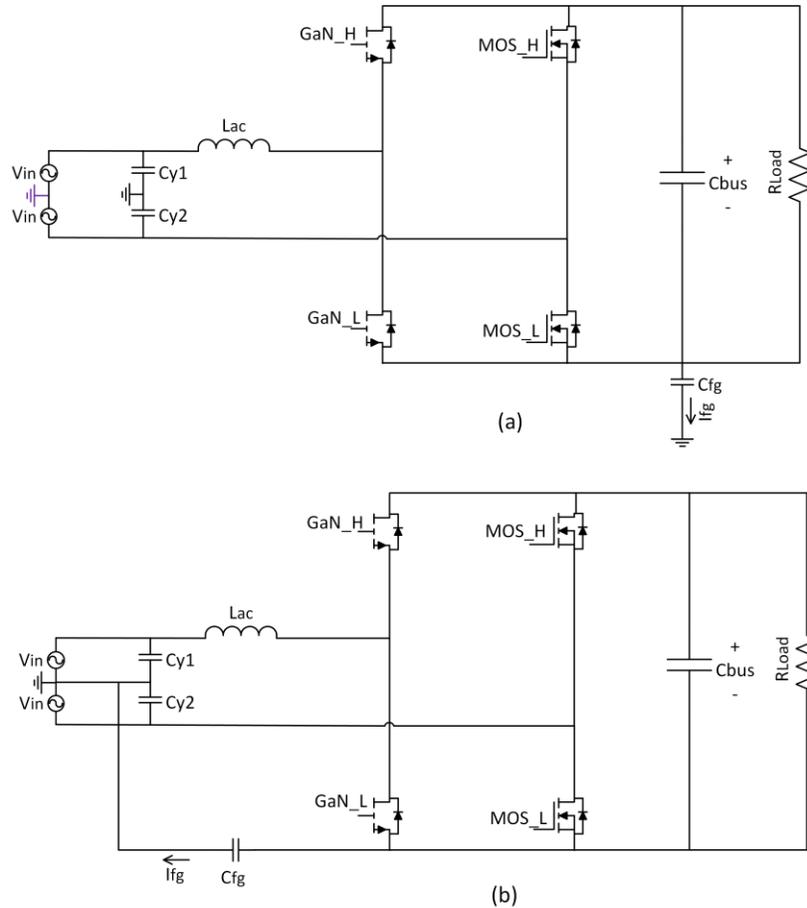


Figure 3.9: Totem-pole PFC with Y-capacitor and C_{fg}

Since the CM noise is particularly significant around line voltage zero-crossing in the totem-pole PFC, the CM noise model is adjusted for this interval in Figure 3.10. Around zero-crossing the input voltage V_{in} is almost zero, so the source has been replaced with a shorted line in Figure 3.10 (a). Since the mid-point of the input source is connected to the earth, the Y-capacitors can then be eliminated from the model and the circuit can be redrawn as shown in Figure 3.10 (b). Unlike the model presented in [56] where the Y-capacitors were summed with C_{fg} to calculate the effective CM capacitance, this adjusted model for split-phase system confirms that the Y-capacitors should be excluded from analysis. The final equivalent circuit can be redrawn as Figure 3.10 (c) with C_{fg} across the low-side MOSFET.

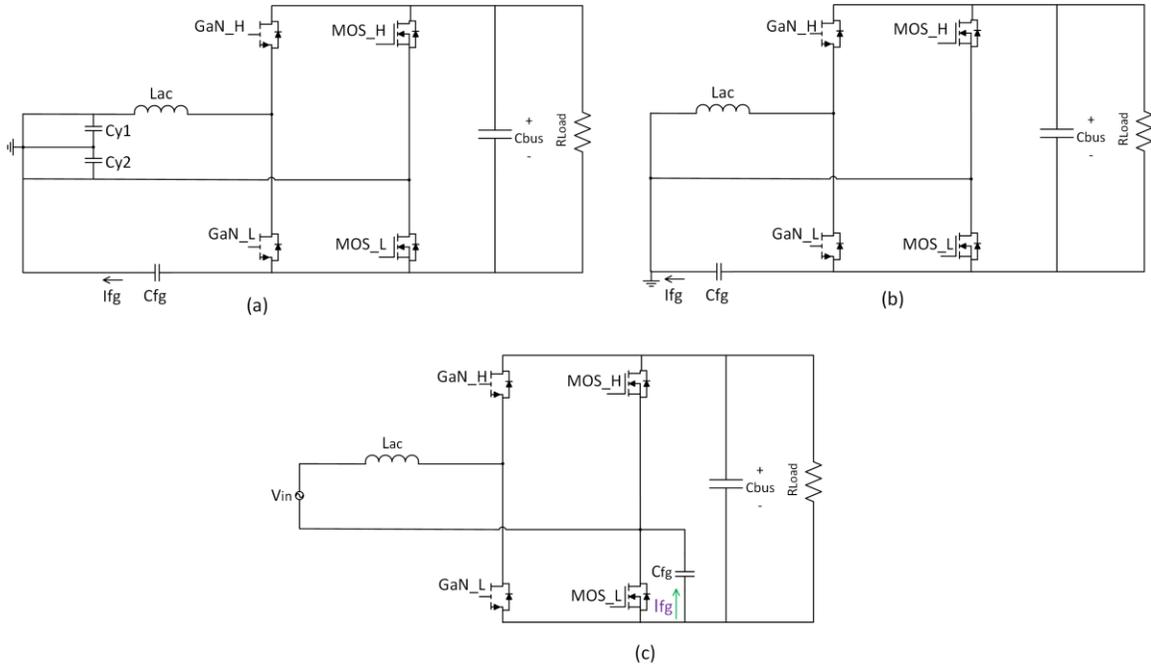


Figure 3.10: Equivalent circuit around zero-crossing for CM noise analysis

From Figure 3.10 (c) it is apparent that the CM noise around zero-crossing is determined by the rate of change of voltage across *MOS_L*. Equation (3-1) represents the relationship between CM noise current and drain-source voltage of *MOS_L*.

$$I_{fg} = -C_{fg} \frac{d}{dt} (V_{ds(MOS_L)}) \quad (3-1)$$

The negative sign in the equation is placed to match the direction of current in Figure 3.10. From equation (3-1) it is evident that any rapid change in drain-source voltage of *MOS_L* will result in increased CM noise. As described in section 3.1, *MOS_L* is kept ON for the full duration of the positive half cycle and *MOS_H* is kept ON for the negative half cycle. During the zero-crossing of ac line voltage, the LF leg MOSFETs change their switching states to either block the dc bus voltage or conduct current. Hence at zero-crossing, the voltage across *MOS_L* goes through a sharp change and this leads to a significant injection of CM noise into the system. A detailed analysis of zero-crossing noise issue is presented in section 3.4.

Any rapid change of voltage across the LF leg MOSFETs will result in an increased CM noise. Depending on the load, the PFC may operate in reverse conduction mode (RCM) near zero-crossings and give rise to further CM noise. This event is explained in section 4.1.

A simulation-based study of the totem-pole PFC shows increased CM current near zero-crossings. The simulation circuit is shown in Figure 3.11.

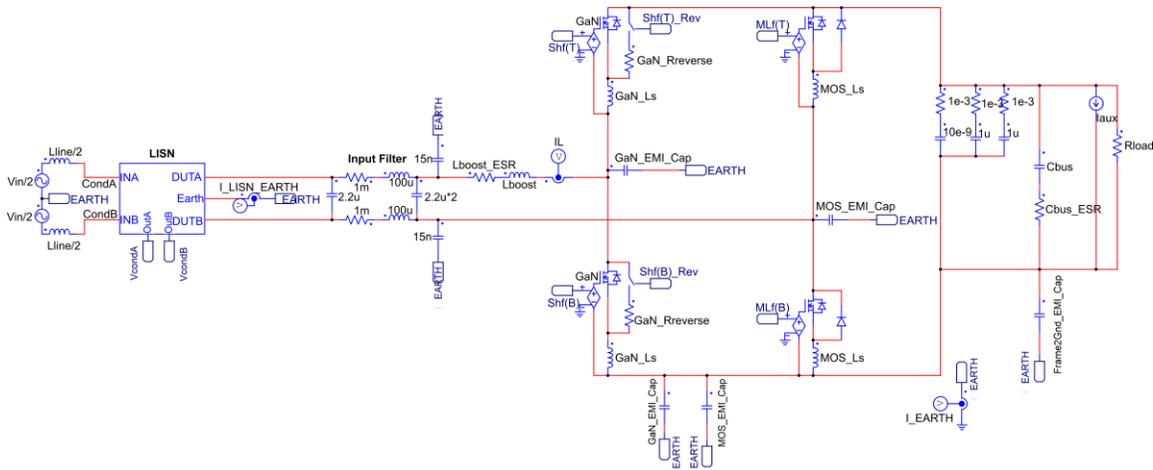


Figure 3.11: Simulation circuit for analyzing CM noise in totem-pole PFC

In a practical power supply, the parasitic capacitance between the switching device and its adjacent heatsink contributes to the CM noise too. In addition to the frame-to-ground capacitance, these parasitic capacitances were also taken into account in the simulation model. The values of these stray capacitors were calculated based on the device package size and adjacent thermal pad size. The frame-to-ground capacitance is considered a typical value of 100pF. The parasitics associated with CM noise simulation circuit is shown in Table 3-1.

Table 3-1: Parasitic capacitances for CM noise simulation

Description	Value (pF)
GaN_EMI_Cap	16
MOS_EMI_Cap	26
Frame2Gnd_EMI_Cap	100

A Line Impedance Stabilization Network (LISN) is placed after the input voltage source to observe the conducted noise in the system. The LISN provides a known impedance to the equipment under test (EUT) for repetitive measurement. For all simulations in this work, the same LISN model as shown in Figure 3.12 is used for comparison of different operating conditions. This LISN structure is commonly used for FCC compliance as well as CISPR testing in the range of 150 kHz to 30 MHz.

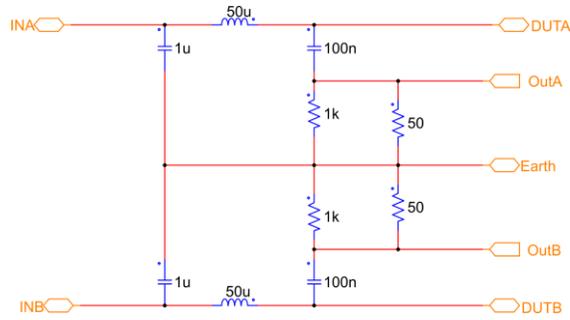


Figure 3.12: LISN

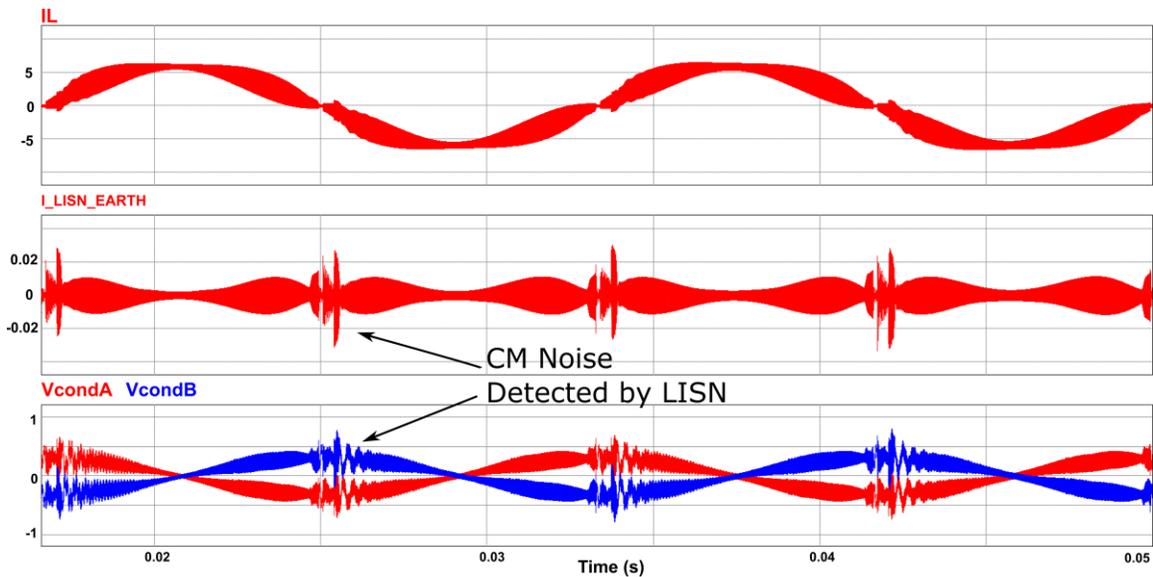


Figure 3.13: LISN waveforms

The simulation results are shown in Figure 3.13. I_{LISN_EARTH} is the current flowing into the earth. V_{condA} and V_{condB} are the noise detected by the LISN from two input conductors. It is evident from the simulation that a significant amount of noise is present around zero-crossings as presumed.

3.4 Zero-Crossing Spike Current

A well-reported issue with totem-pole PFC is the large spike in input current at ac zero-crossing. This is an inherent issue with this topology that has been associated with the CM noise. Though this problem is frequently stated in the literature, the origin of the spike current is often not understood properly and its impact on the noise performance of the totem-pole PFC requires further clarification. This section will present the knowledge

from already published literature at first. Then an in-depth analysis based on both simulation and experimental data will shed more light onto this issue. Finally, several solutions to avoid the CM noise generated during zero-crossing will be discussed.

3.4.1 Origin of Zero-crossing Spike Current

What's in Literature?

Some publications have highlighted the zero-crossing spike current issue and identified two major reasons behind the spike issue.

Most of the works attribute the current spike issue with LF leg MOSFET body diode's reverse recovery and the slow transition of the LF leg. In [52], the authors have mentioned that the reverse recovery of the LF leg MOSFET body diode contributes to the spike current during zero-crossing. The idea was expanded in [57] and it has been observed that the current spike issue is more associated with the slow transition of the LF leg after zero-crossing. Since the LF leg Si-MOSFETs are slow switching devices compared to GaN devices, after zero-crossing, the LF leg MOSFETs transition well after the GaN is switched. This gives rise of the spike current through the inductor.

In the literature, the LF leg MOSFET's slow switching speed has been identified as one of the responsible factors that causes the zero-crossing spike current. If a fast switching MOSFET is used and the LF leg is forced to transition instantly after zero-crossing, before the HF leg GaN even switches, it will certainly eliminate the inductor spike current. But as it is discussed in section 3.4.2, switching the LF leg immediately after zero-crossing is not the solution and doing this will only worsen the noise problem. Since the existing publications have often failed to link the origin of CM noise with zero-crossing spike current, they have misidentified the bottleneck in this case. Zero-crossing spike current is an inherent problem with this topology. It is not the root cause of CM noise, rather an effect of the voltage transition of the LF leg MOSFET C_{oss} at zero-crossing. Eliminating the spike current does not necessarily reduce the CM noise.

In [56] it was shown that it is possible to increase the inductor current spike intentionally to achieve less CM noise. Though this approach will increase the differential mode noise, the analysis provides further insight into the spike issue.

Although the zero-crossing current is often described as a ‘spike’ current in literature, it is not a spike in the regular sense. Since the current flows through an inductor, it cannot rise abruptly. Rather the current rises to a peak value immediately after zero-crossing and it actually remains at this level for the whole duty cycle. The body diode of MOSFET in the LF leg assists the current to sustain during this instance. A detailed analysis of the origin of the zero-crossing current spike is presented in the following section.

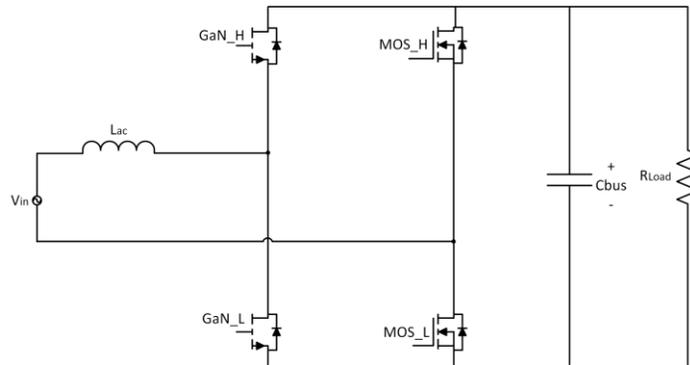


Figure 3.14: Totem-pole PFC near zero-crossing

To eliminate the CM noise problem of the totem-pole PFC, the majority of the research works have exclusively focused on solving the zero-crossing spike current issue. But the CM noise generated before and after the zero-crossing instance, as shown in Figure 3.13, has largely been overlooked. When the totem-pole PFC is operating around the zero-crossing, the inductor current drops to zero during a switching cycle and then reverses. This operating instance can give rise to CM noise as discussed in 4.1. In [58] the authors have briefly stated the possibility of reverse current conduction around zero-crossing. But the work does not mention the consequences of the reverse conduction mode (RCM) on CM noise around zero-crossing.

Analysis of Zero-crossing Spike Issue

The following analysis studies the negative to positive half cycle zero-crossing current spike issue in detail. Since the operation of totem-pole PFC is symmetric, positive to negative zero-crossing will follow the same analysis.

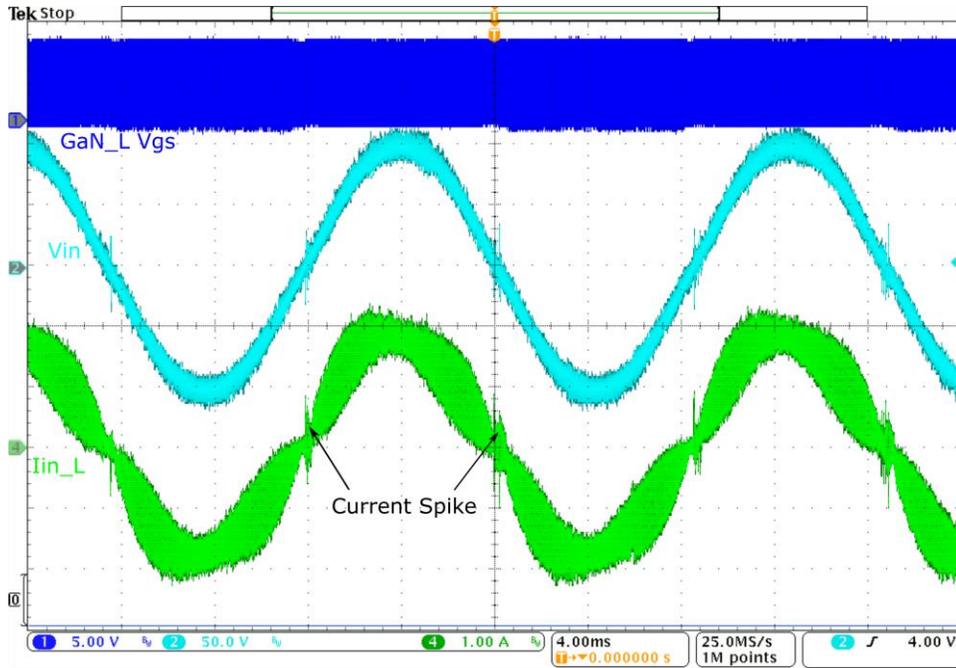


Figure 3.15: Zero-crossing spike current

During negative half cycle operation of the PFC, high-side MOS_H conducts current for the total duration of the half cycle. So the voltage across MOS_H remains zero and the low-side MOS_L blocks the full dc bus voltage. Voltage distribution across the LF leg during the negative half cycle is shown in Figure 3.17 (a). For the purpose of explanation, the bus voltage is assumed to be 400V. Just before the zero-crossing, GaN_H switches with maximum duty ($\sim 100\%$) and the low-side GaN_L remains open to block the full bus voltage of 400V. Just after zero-crossing into the positive half cycle, GaN_L turns ON with maximum duty period. The C_{oss} of GaN_L quickly dissipates through the channel and drops to zero voltage. Consequently, drain-source voltage of GaN_H rises quickly to block the total dc bus voltage as shown in Figure 3.17 (b). Since the input voltage after the zero-crossing is very small, the calculated duty of GaN_L is almost 100%. So the low-side GaN_L stays closed for a long duration of time. This provides a path for the MOS_H reverse recovery current to flow.

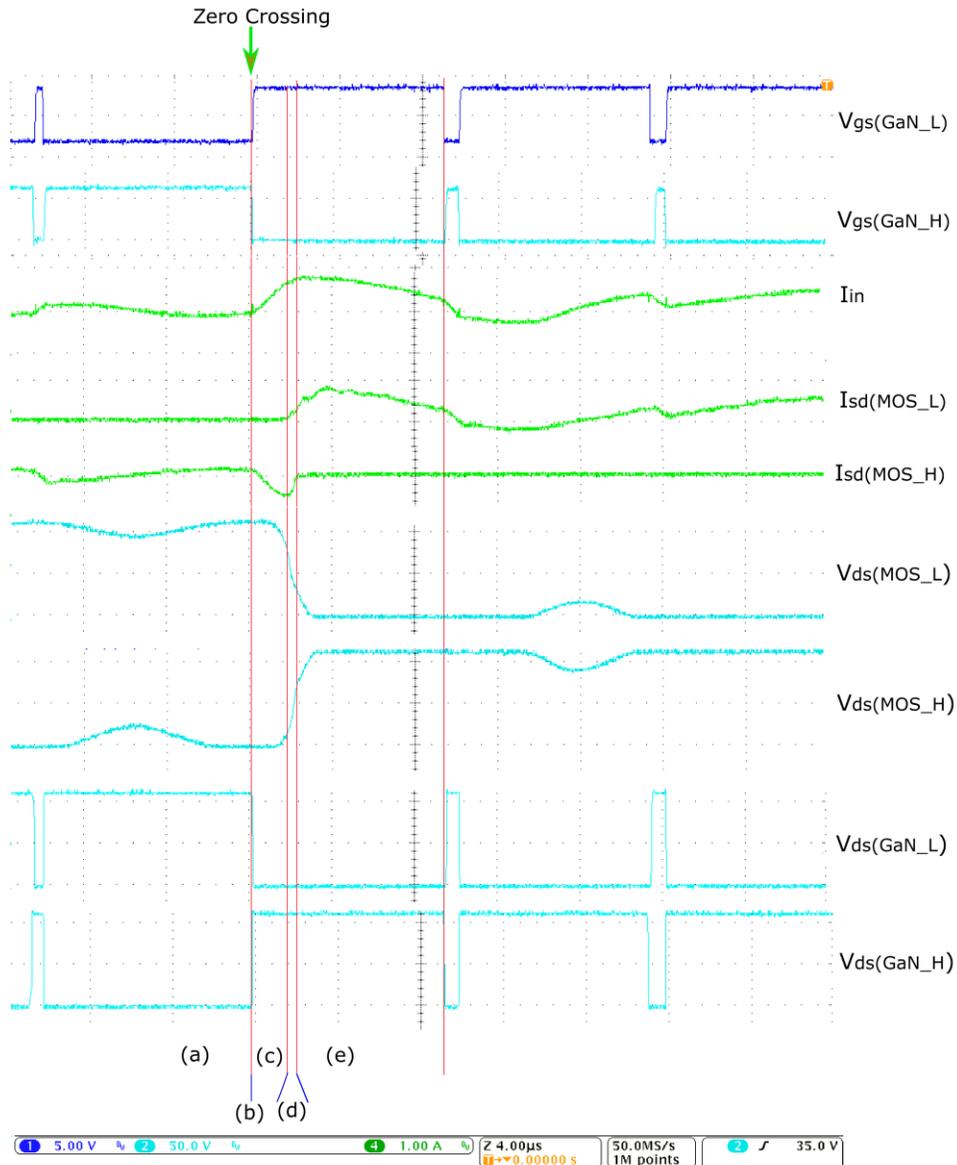


Figure 3.16: Negative to positive zero-crossing waveforms

Note: Multiple oscilloscope waveforms aligned to the same switching instance.

The quantity of reverse recovery charge left in the high-side MOSFET is very small at any zero-crossing. This is because the current through the *MOS_H* body diode was very little before the zero-crossing and there remained only a few reverse recovery charge trapped in the *p-n* junction of the body diode. When *GaN_L* is turned ON after the zero-crossing, the whole dc bus voltage starts to drive the *MOS_H* body diode into reverse bias and the small amount of reverse recovery charge flows through the inductor as I_{rr} . This instance is shown in Figure 3.17 (c). For the duration of which reverse recovery current

flows, the voltage across MOS_H remains zero and MOS_L blocks 400V without dissipating any charge from its C_{oss} .

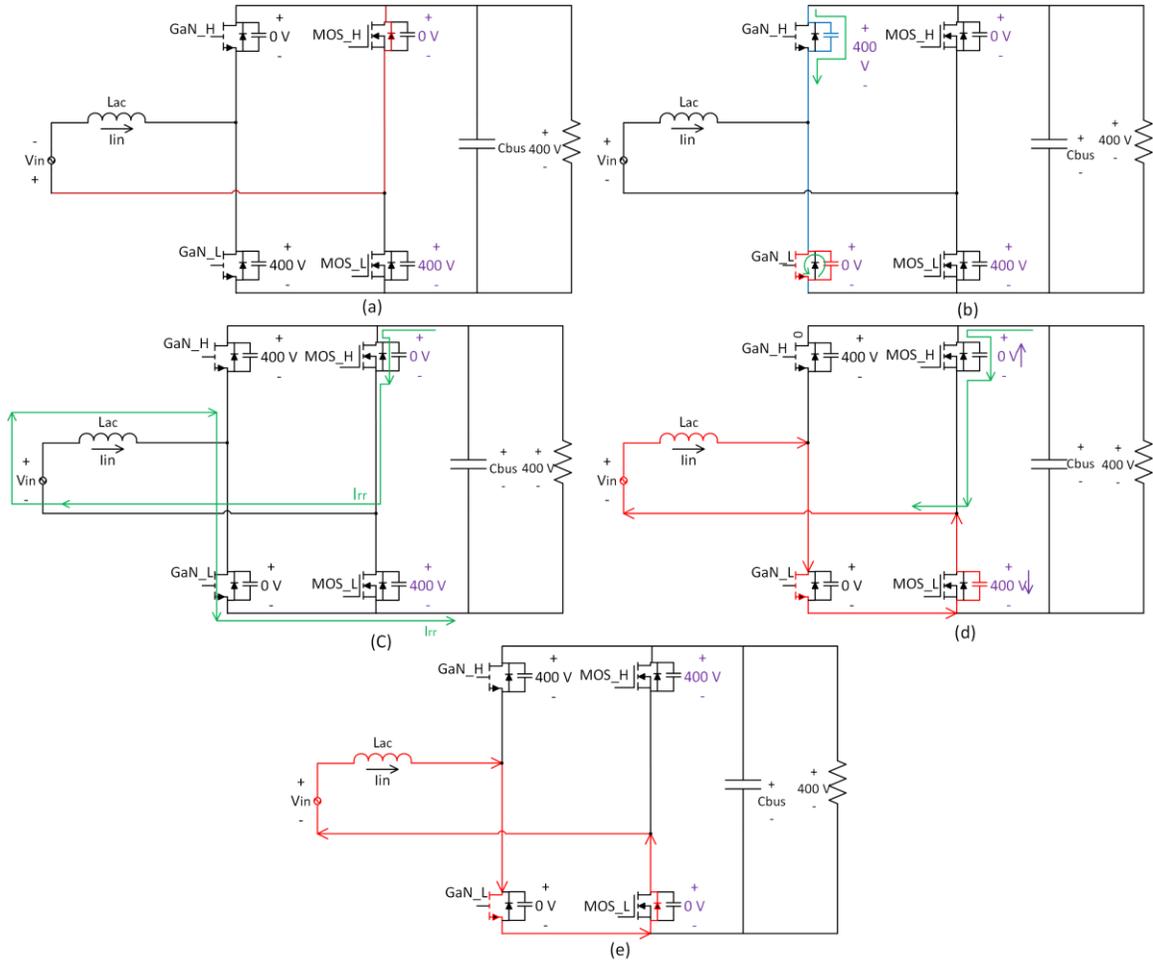


Figure 3.17: Transitional stages during negative to positive zero-crossing

Note: Stages (a)-(e) are representative of the same time interval shown in Figure 3.16

The reverse recovery current drops to zero quickly. But the inductor current remains continuous and drives the C_{oss} of MOS_L to start discharging. This is when the voltage across the LF MOSFET leg starts to change. As V_{in} is very small at this instance, the total 400V of MOS_L C_{oss} is applied across the inductor and the positive inductor current rises quickly. During this instance, the inductor current reaches its peak and appears as a spike current in the waveform. The operation is shown in Figure 3.17 (d). Throughout this stage, MOS_H drain-source voltage builds up while MOS_L C_{oss} voltage keeps dropping. Since the output capacitance of MOSFETs is in the order of few hundred pF (typically ~ 200 pF) the voltage changes quickly as it can be seen from the time interval

(d) in practical waveforms of Figure 3.16. Current and voltage change during this stage is shown in Figure 3.17 (d).

An equivalent circuit for the negative to positive zero-crossing operation is shown in Figure 3.18 (a). Since the output bus voltage remains fairly constant for a small period of time, it is modeled as a dc source with a voltage of V_{bus} . The resistance in series with the inductor is made up mostly of the ESR of the inductor and ranges up to few $m\Omega$. Since the input voltage is very small, it has been ignored from analysis and replaced with a shorted line. V_c is the drain to source voltage of MOS_L . From the analysis of section 3.2, any rapid change in voltage V_c is responsible for the CM noise.

The moment GaN_L turns ON, both output capacitors of GaN HEMTs transition quickly. In the next step, the reverse recovery current of MOS_H flows through the inductor. At the peak of reverse recovery current, the LF leg C_{oss} comes into conduction. It is vastly complicated to model the reverse recovery current in an equivalent circuit. For simplicity, it is assumed that the inductor is carrying maximum reverse current (I_{rrm}) when the LF MOSFET output capacitors start conducting. Since the purpose of the analysis is to understand the transition speed of MOS_L drain-source voltage, this assumption remains fairly accurate. MOS_L C_{oss} blocks the total bus voltage prior to switching and voltage across MOS_H C_{oss} remains zero. The resulting circuit falls into a simple RLC circuit as shown in Figure 3.18 (b).

A mathematical analysis of the equivalent circuit in Figure 3.18 (b) is performed in Appendix A. The voltage across MOS_L C_{oss} can be calculated by equation (3-2)

$$V_c(t) = e^{-\alpha t} (V_{bus} \cos \omega_d t - \frac{I_{rrm}}{C \omega_d} \sin \omega_d t + \frac{V_{bus} \alpha}{\omega_d} \sin \omega_d t) \quad (3-2)$$

Here, α is a constant and ω_d is the damped natural frequency of the circuit.

$$\alpha = \frac{R}{2L_{ac}} \quad (3-3)$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \quad (3-4)$$

The undamped natural frequency ω_0 can be calculated by equation (3-5).

$$\omega_0 = \frac{1}{\sqrt{L_{ac} C}} \quad (3-5)$$

Here it was assumed that $C = 2 C_{oss}(MOS)$. As mentioned before, V_c is the drain source voltage of MOS_L . The resistance R in the equivalent circuit is very small and it works as a damping element in the circuit. For the analysis of transient change of V_c , the effect of R can be ignored.

Setting $R=0$ we get

$$\alpha = \frac{R}{2L_{ac}} = 0$$

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} = \omega_0$$

And

$$V_c(t) = V_{ds}(MOS_L) = V_{bus} \cos \omega_0 t - \frac{I_{rrm}}{C \omega_0} \sin \omega_0 t \quad (3-6)$$

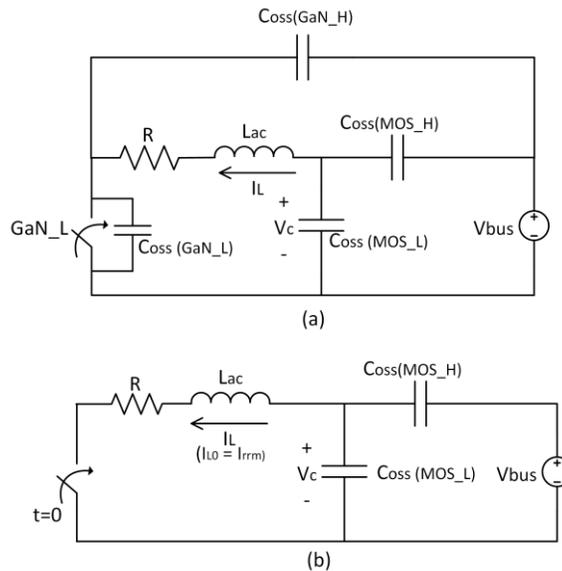
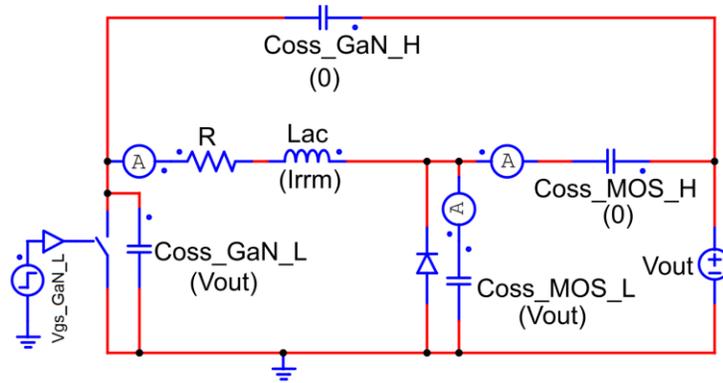
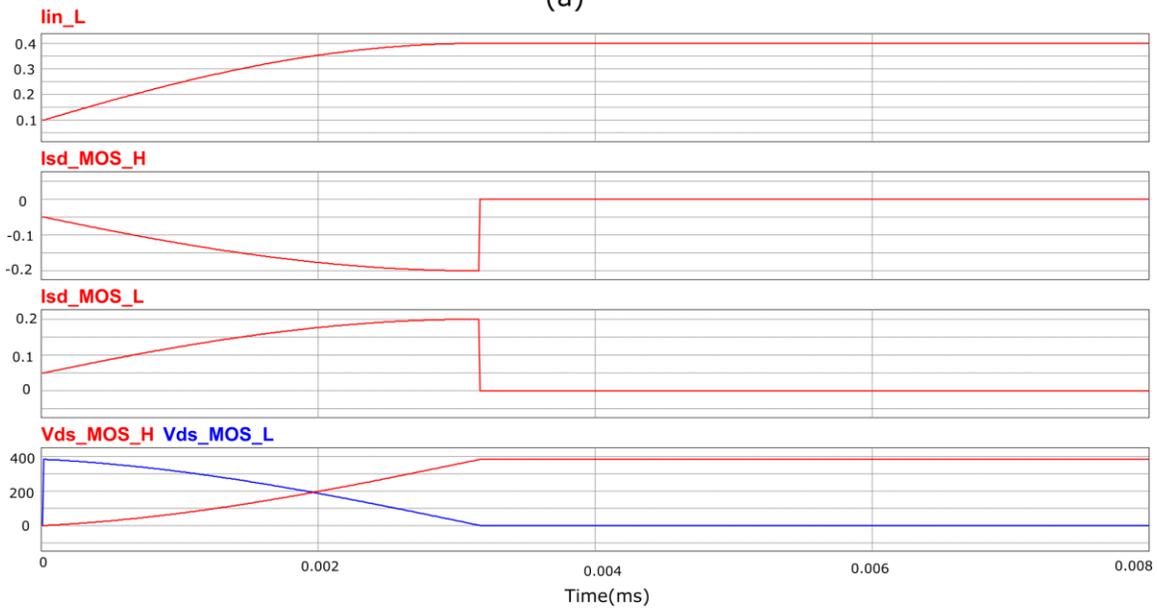


Figure 3.18: Negative to positive zero-crossing equivalent circuit

A simulation of the equivalent circuit is performed in PSIM software. The waveforms in Figure 3.19 show that the current as well as the voltage across the LF leg MOSFET transitions in a sinusoidal manner.



(a)



(b)

Figure 3.19: Negative to positive zero-crossing equivalent circuit simulation

After *MOS_L* output capacitor charge is dissipated, the drain-source voltage of *MOS_L* drops to zero. The inductor current being continuous, forces the body diode of *MOS_L* to turn ON. The inductor current then flows through the *MOS_L* body diode and remains fairly stable for the remainder of the duty cycle. The current path is highlighted in Figure 3.17 (e).

3.4.2 Effect of Zero-crossing Spike Current on EMI

From the discussion presented in section 3.2, it is evident that near zero-crossing point, CM noise depends on the voltage across the LF MOSFET leg. Equation (3-1) shows that the noise current is proportional to the rate of change of voltage across *MOS_L*.

$$I_{fg} = -C_{fg} \frac{d}{dt}(V_{ds(MOS_L)}) \quad (3-1)$$

For assisting the analysis, a function $N(t)$ is defined such that

$$I_{fg} = C_{fg} N(t)$$

Where,

$$N(t) = -\frac{d}{dt}(V_{ds(MOS_L)}) = V_{bus} \omega_0 \sin \omega_0 t + \frac{i_{rrm}}{c} \cos \omega_0 t \quad (3-7)$$

In this analysis $N(t)$ serves as a noise function. CM current at zero-crossing is proportional to $N(t)$. During the switching transition, the noise current reaches its peak value when $N(t)$ is maximum. As shown in the detailed derivation in Appendix A, the maximum value of $N(t)$ can be calculated by equation (3-8).

$$N(t)_{max} = \sqrt{(V_{bus} \omega_0)^2 + \left(\frac{i_{rrm}}{c}\right)^2}$$

$$N(t)_{max} = \sqrt{\left(\frac{V_{bus}}{\sqrt{2} L_{ac} C_{oss}}\right)^2 + \left(\frac{i_{rrm}}{2 C_{oss}}\right)^2} \quad (3-8)$$

Figure 3.20 is a simplified representation of equation (3-8). A number of important observations can be made from equation (3-8).

- Dc bus voltage is directly proportional to the amount of noise generated. CM noise will increase for larger bus voltage.
- Increasing the size of either the inductor or capacitor can reduce the amount of noise generated at zero-crossing. Since the cost and power density of the system is largely affected by larger magnetics, increasing the inductor size is often not a suitable solution. Adding extra capacitor across MOSFET C_{oss} can also decrease the amount of CM noise. Capacitors are relatively cheaper and light weight compared to inductors. However, additional capacitors can introduce some other issues.
- LF leg MOSFET's reverse recovery current also contributes to the noise. Large reverse recovery current will increase the CM noise at zero-crossing.

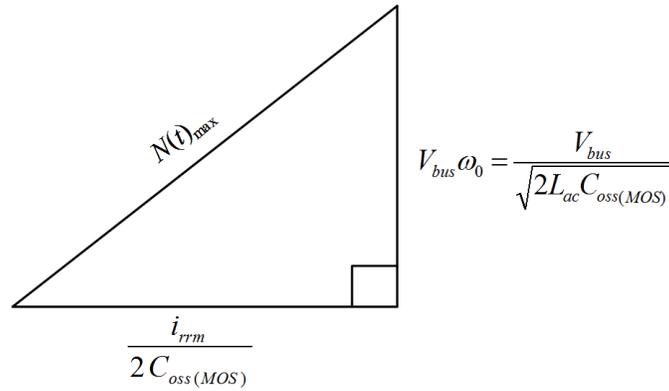


Figure 3.20: Graphical representation of equation (3-8)

Not every circuit parameter affects the noise current equally. For most of the applications, V_{bus} is predefined and not a variable. To simplify the analysis, if the V_{bus} is considered constant, equation (3-8) reduces to a three variable function. An isosurface plot of this function is shown in Figure 3.21. It is evident that the amount of generated noise changes slowly with varying I_{rrm} . Similarly, the inductor size individually has little impact on the noise generation. However, any change in the MOSFET C_{oss} immediately impacts the value of noise function. A large C_{oss} reduces the noise significantly.

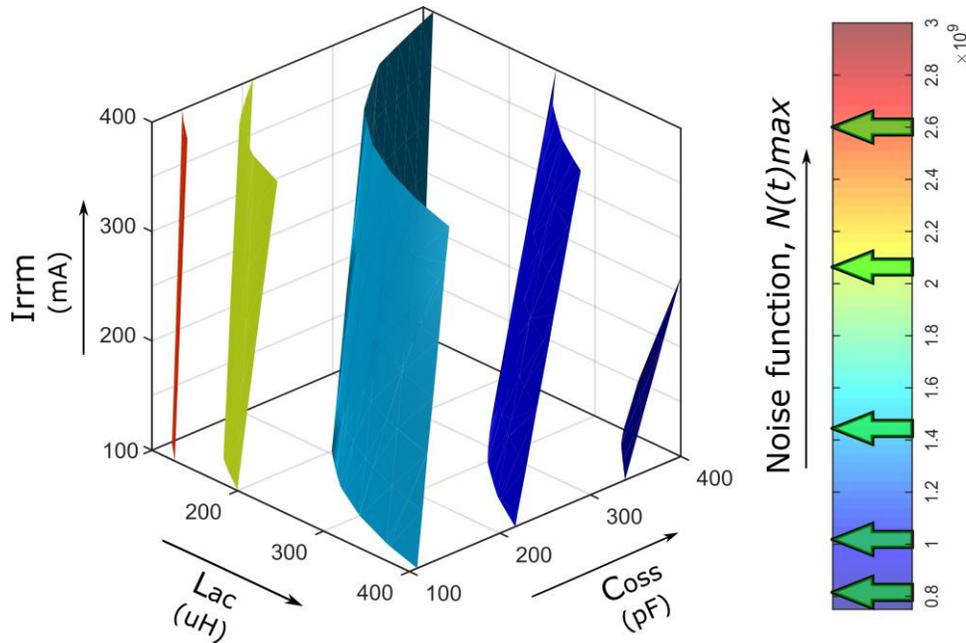


Figure 3.21: Dependence of $N(t)_{max}$ on different circuit parameters

Note: V_{bus} is assumed to be 400V. Color coded isosurfaces are plotted in MATLAB.

Inductor current of the equivalent circuit of Figure 3.18 (b) is calculated in Appendix A as

$$I_L(t) = V_{bus} \sqrt{\frac{2C_{oss}}{L_{ac}}} \sin \omega_0 t + I_{rrm} \cos \omega_0 t \quad (3-9)$$

Peak inductor current during zero-crossing can be calculated from here as

$$I_L(t)_{peak} = \sqrt{\left(V_{bus} \sqrt{\frac{2C_{oss}}{L_{ac}}} \right)^2 + (I_{rrm})^2} \quad (3-10)$$

Figure 3.22 shows an illustrative representation of equation (3-10) for better visualization. It is evident that adding more capacitors across MOSFET C_{oss} will increase the inductor peak current. In other words, added capacitor increases the current spike during zero-crossing. In [56] a similar methodology is employed to mitigate the CM noise. This approach is covered in greater detail under section 3.4.3. The reverse recovery current of the LF MOSFET also increases the current spike at zero-crossing. However a bigger inductor will decrease the spike current peak.

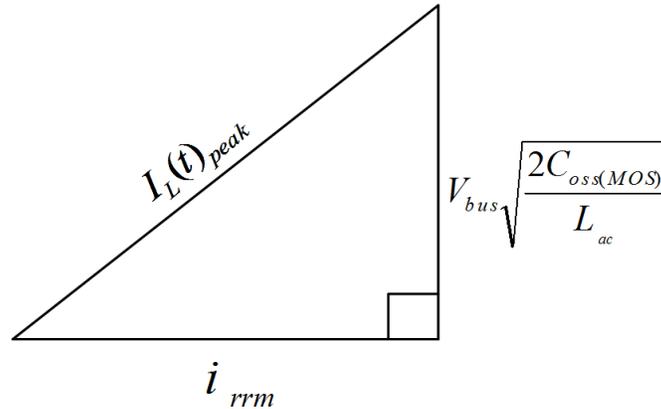


Figure 3.22: Graphical representation of equation (3-10)

A sudden drop of voltage across MOS_L during negative to positive zero-crossing contributes to the CM noise. During positive to negative zero-crossing, MOS_L voltage escalates quickly and results in CM noise current in a similar fashion. This rapid fluctuation of the drain-source voltage across the LF leg MOSFETs is the prime source of noise in totem-pole PFC at zero-crossing.

3.4.3 Switching Techniques to Mitigate CM Noise

Much effort has been invested in the literature to solve the zero-crossing spike current issue. The majority of these works have identified zero-crossing spike current as the primary source of CM noise and tried to minimize the current spike around zero-crossing. But it is evident from the discussion in section 3.4.2 that decelerating the rate of change of MOS_L drain to source voltage around a zero-crossing is crucial to mitigate the noise. The switching techniques adopted by some literature to mitigate the spike current eventually achieves a decelerated voltage transition across the LF leg MOSFETs and reduces the CM noise accordingly. But understanding the root cause of noise generation at zero-crossings offers further possibility of developing alternative techniques for dealing with this issue.

A popular approach that has been suggested in the literature for minimizing the current spike is the soft-start switching technique of HF leg just after zero-crossing. This particular switching scheme has been patented for totem-pole PFC by TDK-Japan [59]. Several other works have adopted this method to achieve better noise rejection in their design [57], [58], [60]. According to this approach, the high-frequency active switch starts with a very small duty after a zero-crossing and gradually increases the duty in every switching cycle from there. The calculated duty by the control loop is ignored for the duration of this soft-start scheme. The soft-start duty of the active switch during negative to positive zero-crossing is shown in Figure 3.23.

Providing a small duty allows only a small amount of current to flow through the inductor at first. This ensures that the LF leg MOSFET drain-source voltage changes only slightly. As soon as the active switch turns OFF after this small duty, the inductor discharges the energy into the dc bus through the boost diode. In the next switching instance, a slightly larger duty is applied and MOSFET C_{oss} voltage changes accordingly. Repeating this pattern for next few cycles ensures that the drain-source voltage of the MOSFET changes in small steps. This switching technique can reduce the rate of change of MOSFET drain-source voltage at zero-crossings and decrease the conducted EMI as a result.

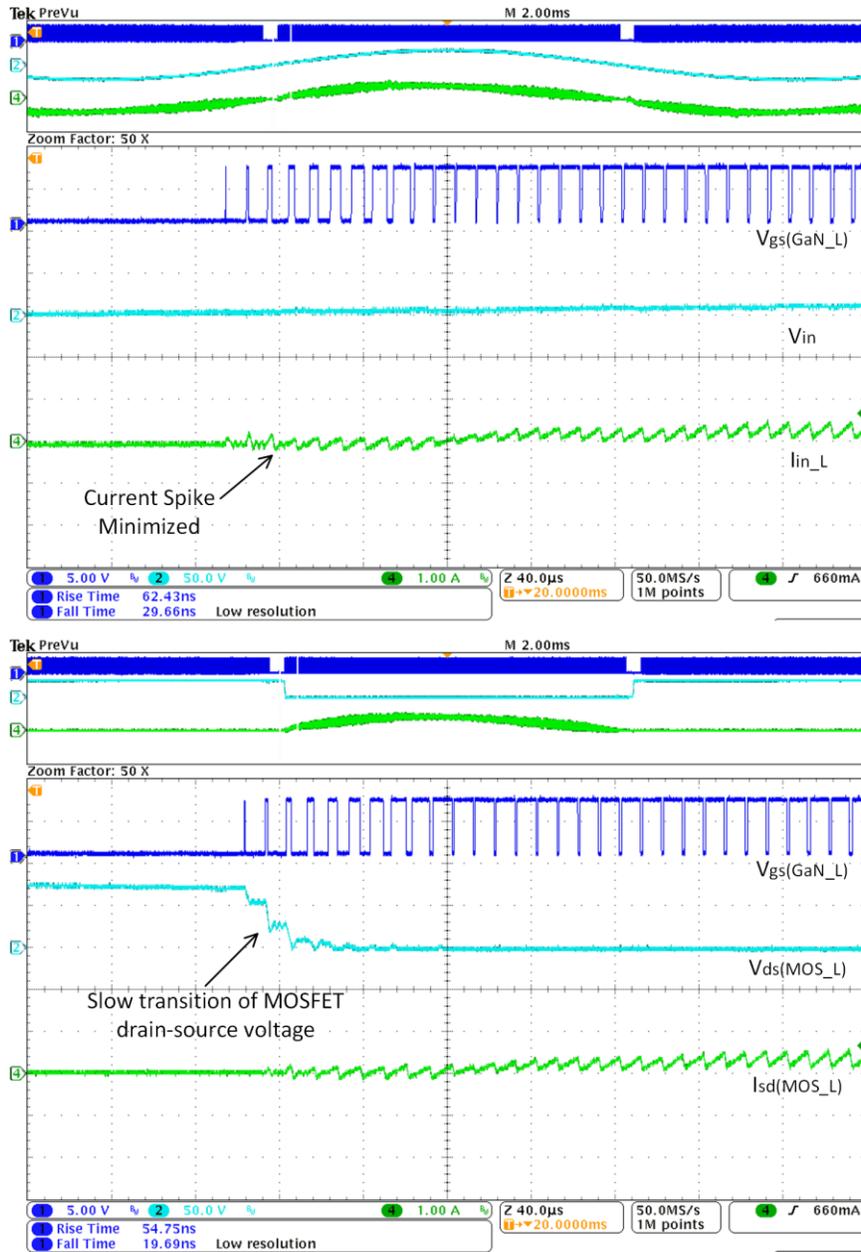


Figure 3.23: Zero-crossing transition with soft start

The second method to deal with the zero-crossing CM noise issue is presented in [56], [61]. This method achieves a slow transition of the MOSFET drain-source voltage by adding extra capacitors across the LF leg MOSFETs. Adding C_1 and C_2 as shown in Figure 3.24 will decrease the rate of change of MOS_L drain to source voltage around zero-crossing. This guarantees that the CM current calculated by equation (3-1) is reduced. The problem with this approach is that during zero-crossing, due to the presence of added capacitors across the MOSFETs, the inductor current spike becomes larger as it is evident from equation (3-10). This may introduce other issues including increased differential

mode noise as predicted in [56]. An abnormally big spike may require large magnetics design and produce additional radiated EMI.

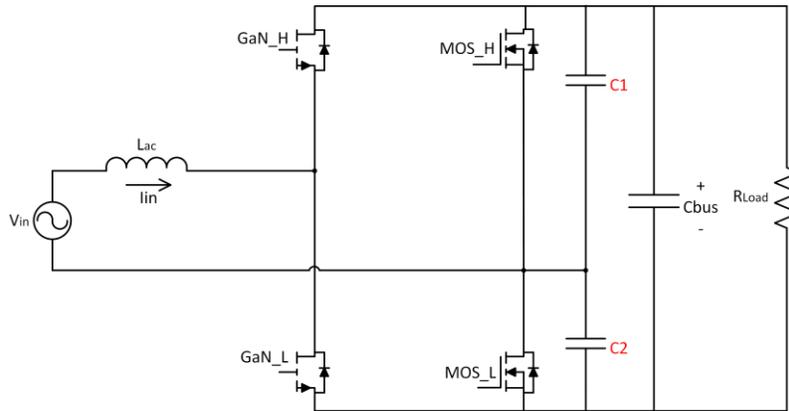


Figure 3.24: Zero-crossing CM noise reduction as shown in [56]

The issue of zero-crossing CM noise can be reduced by just decelerating the change of *MOS_L* drain to source voltage. To keep the differential mode noise including other issues within the limit, it is desirable to keep the spike current small. Increasing the inductor spike current deliberately to reduce the CM noise thus is not the preferred technique for most applications. Zero-crossing soft start scheme is the superior solution since it can ensure the slow transition of MOSFET drain-source voltage while ensuring reduced input current spike. Executing soft-start scheme requires additional microcontroller resource and adds complexity to the control.

As an alternative approach, it is possible to apply a constant small duty for a few switching cycles after a zero-crossing until the MOSFET drain-source voltage is transitioned completely and then resume normal operation. This can be achieved rather easily without consuming much of the microcontroller resources. The waveforms for this approach are shown in Figure 3.25. Using this switching technique MOSFET voltage can be controlled to transition slowly after the zero-crossing. Although the current start to rise when normal switching resumes, this is not a spike current. This sudden rise in current, though affect the current shape, does not contribute to the CM noise. This overshoot appears because the controller attempts to compensate for the error accumulated over the period for which a constant duty was applied. This can be avoided in most cases by resetting the controller after the constant duty switching period or by applying feed-forward duty.

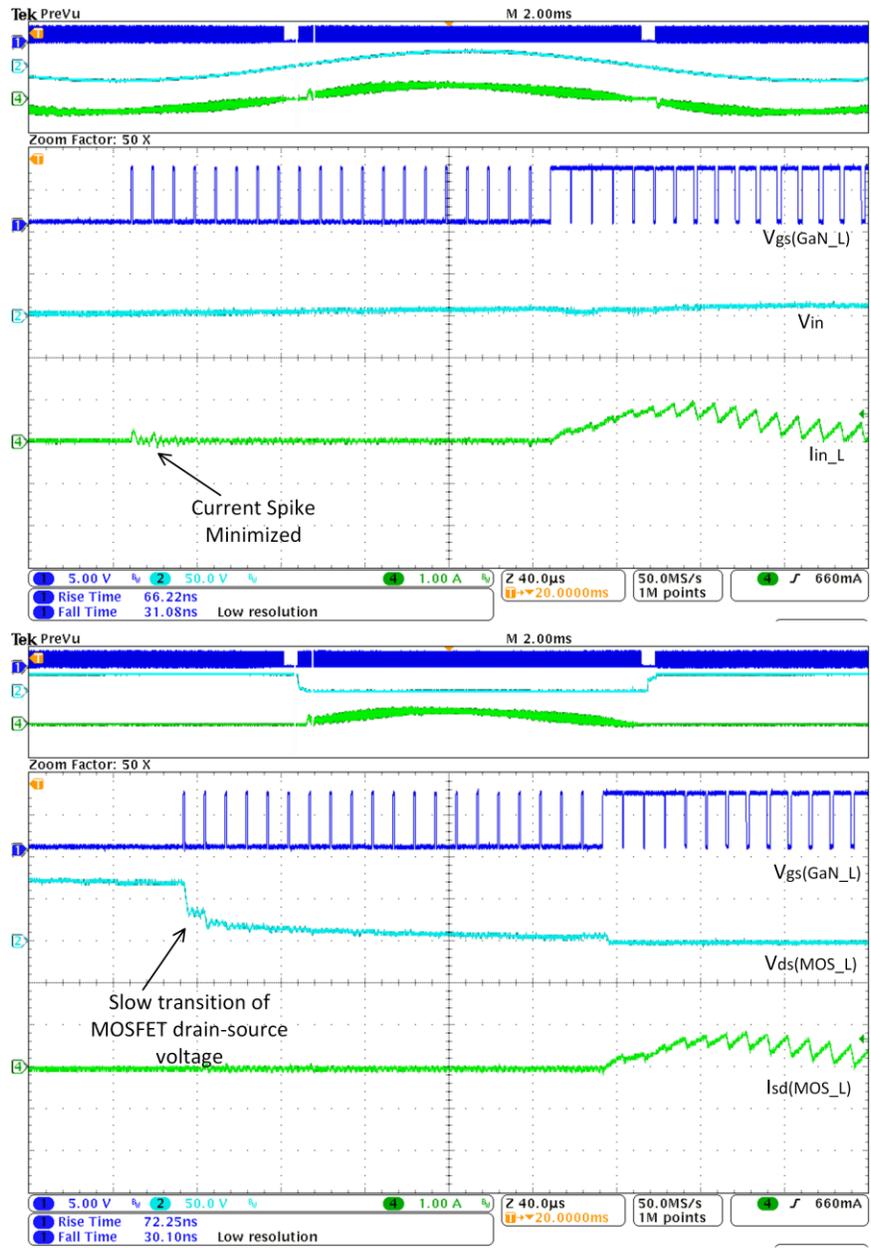


Figure 3.25: Reduction of CM noise by applying constant duty after ZC

Chapter 4. Synchronous Totem-pole PFC

In a totem-pole PFC, synchronous switching is achieved by turning the high-frequency switching device ON during the current freewheeling period. Synchronous switching ensures a reduced conduction loss. Due to the presence of the parallel diode, synchronous switching occurs in ZVS manner which accounts for very small switching loss. If the low-frequency leg of the totem-pole PFC is made of two MOSFETs, there are some challenges when the PFC operates near ac zero-crossings.

4.1 Reverse Conduction Mode

In traditional boost converter operating in discontinuous conduction mode (DCM), the current through the inductor becomes zero during a switching cycle. The inductor current can even become zero in a continuous conduction mode (CCM) converter if operated at very light load. This happens because the input side inductor design usually leaves some room for ripple current. Smaller ripple current requires larger inductors. So to keep the inductor size within an acceptable limit, some tolerable ripple current is permitted for which the converter works in CCM at full load. For light load operation the inductor current becomes very low and during the freewheeling period through the diode, current reaches zero before the active switch is turned ON again. Since the diode remains in series with the load during the discharge stage, it blocks the reverse current flow from the output dc bus to the source.

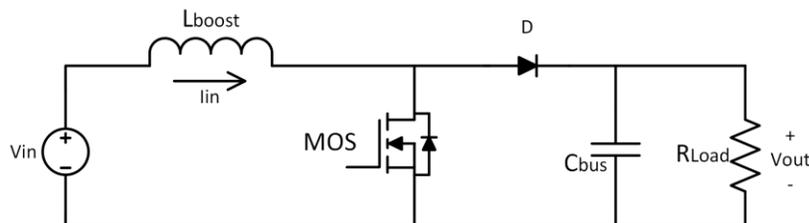


Figure 4.1: Dc-dc Boost Converter

If the diode (D in Figure 4.1) is replaced with a MOSFET and operated in synchronous switching during light load condition, the current will flow backward during DCM instance to charge the dc source. The reverse current increase rather slowly here due to the presence of a constant voltage input dc source.

Since the inductor current in a totem-pole PFC is very small before and after an ac zero-crossing, it can drop to zero during a switching period and then flow in the reverse direction. The input voltage of the PFC being almost zero during this period means the reverse current can rise rapidly and disrupt the operation of the PFC. At what switching instant the inductor current will drop to zero depends on the size of the inductor and load. A smaller inductor means the peak to peak ripple current is large and the current will drop to zero well before actual ac zero-crossing. A lighter load will draw low current from the source allowing the ripple current to start reaching zero early. Around ac zero-crossing the input voltage (V_{in}) is almost zero. If synchronous switching is enabled during this period, the output dc bus will end up reversing the current through the inductor. This operation of totem-pole PFC is called ‘Reverse Conduction Mode (RCM)’ in this thesis.

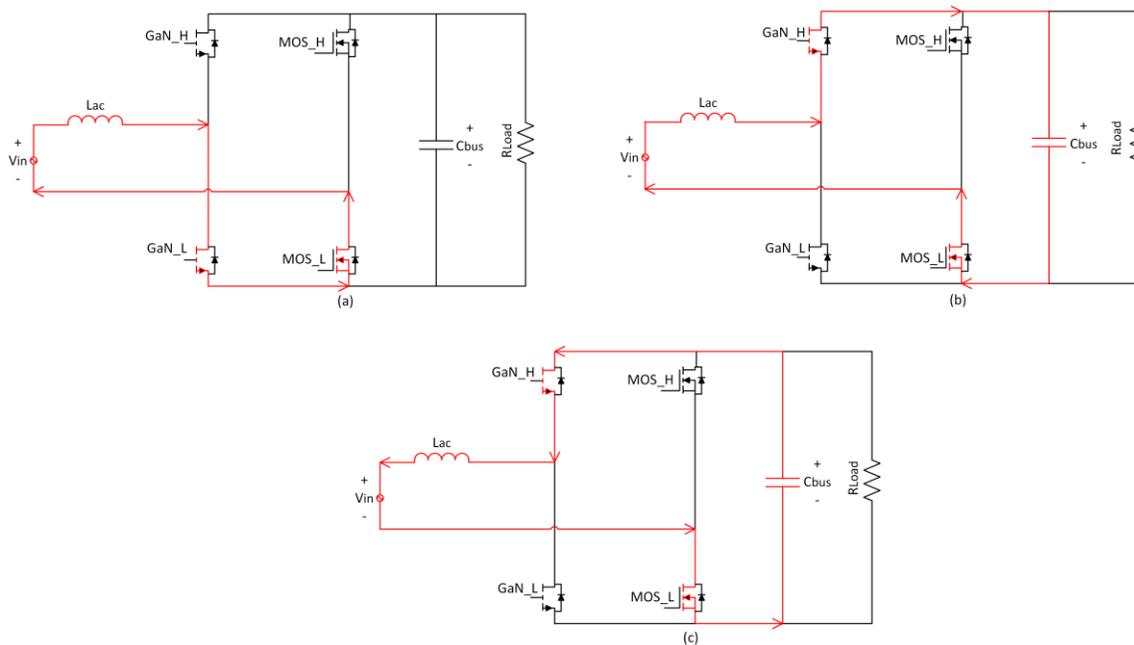


Figure 4.2: Reverse conduction mode during positive half cycle

Figure 4.2 (a) shows the instance when the PFC is operating just before positive to negative zero-crossing. GaN_L is the active switch and it operates with maximum duty during this time. MOS_L conducts the charging current for the interval when GaN_L remains closed. For a brief period, GaN_L turns OFF to discharge the current to the dc bus. If the synchronous operation of the PFC is implemented, this freewheeling current then flows through the high-side GaN_H as shown in Figure 4.2 (b). Since the inductor current is very small, it will discharge and drop to zero quickly. The input voltage V_{in} being almost zero means the entire dc bus voltage ($\sim 385V$) appears across the inductor when

the inductor current drops to zero. This will drive reverse current to flow through the inductor for the remainder of the period. If allowed to flow, this current can rise quickly through the inductor as shown in Figure 4.2 (c). Depending on the size of the inductor and switching frequency, this current can increase over subsequent switching cycles and completely disrupt the control loop operation. It also accounts for additional loss.

4.1.1 Switching Technique to Avoid Reverse Current Flow

The reverse current conducts through the synchronous GaN switch and the low-frequency MOSFET switch. These two devices being simultaneously ON when the inductor current falls to zero creates a path for reverse current to flow. Reverse current conduction can happen in traditional boost converter if it is operating in synchronous rectification (SR) mode. To avoid the reverse current flow, the synchronous switch is turned OFF after detecting the reverse current [62]. This approach senses the current more frequently and requires considerably more microcontroller resources. For totem-pole PFC, a preferred solution is to keep either or both switches OFF during RCM operation.

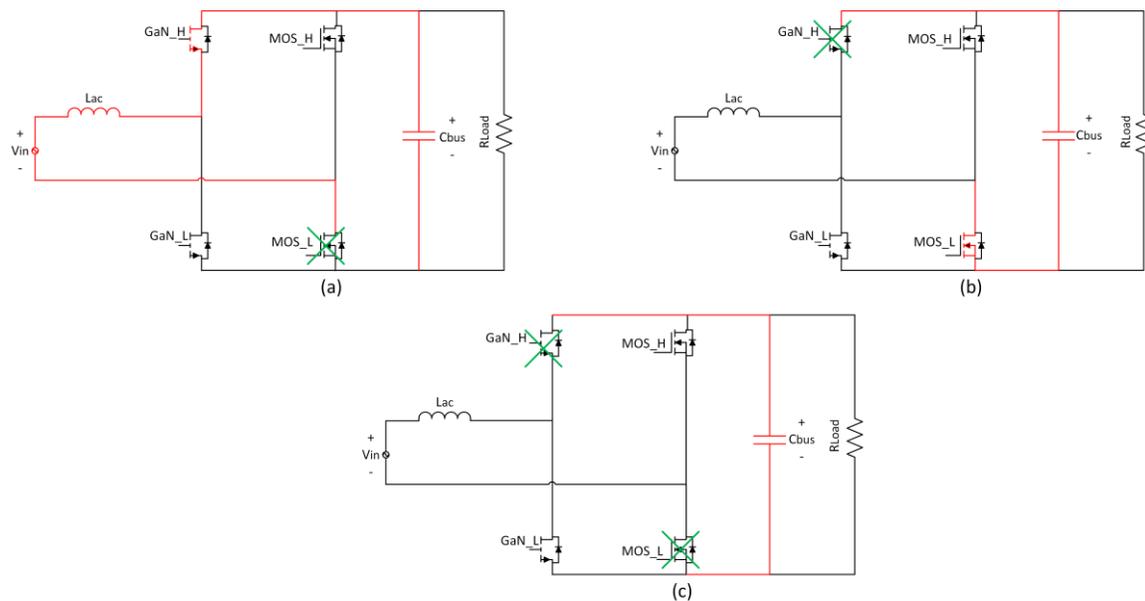


Figure 4.3: Switching techniques to avoid RCM

Figure 4.3 shows possible solutions to avoid the reverse current flow during positive half cycle operation. Keeping *MOS_L* forced turned OFF during the RCM period can avoid reverse current flow as shown in Figure 4.3 (a). Forcing *GaN_H* OFF during this period achieves the same effect as shown in Figure 4.3 (b). Alternatively, both switches

can be forced OFF to block the reverse flow path as it is evident from Figure 4.3 (c). Turning OFF the HF leg GaN alternative switching means the system loses synchronous operation. Achieving this can be challenging while designing the control in microcontroller. Since the LF leg is controlled separately, it's simple to manipulate. Therefore, the solution provided in Figure 4.3 (a) is easily attainable and preferred in most applications. In [63], this switching mechanism was implemented during RCM operation.

4.2 CM Noise during Reverse Conduction Mode

From section 3.2 it is apparent that conducted noise greatly increases if the voltage across the *MOS_L* changes rapidly with high dv/dt . While analysing RCM switching interval in the preceding section, the effect of parasitic components was largely ignored. If the reverse recovery of the LF leg MOSFET body diode along with the output capacitance of the semiconductor devices are taken into account, their obvious consequence on the noise performance of the totem-pole PFC becomes evident.

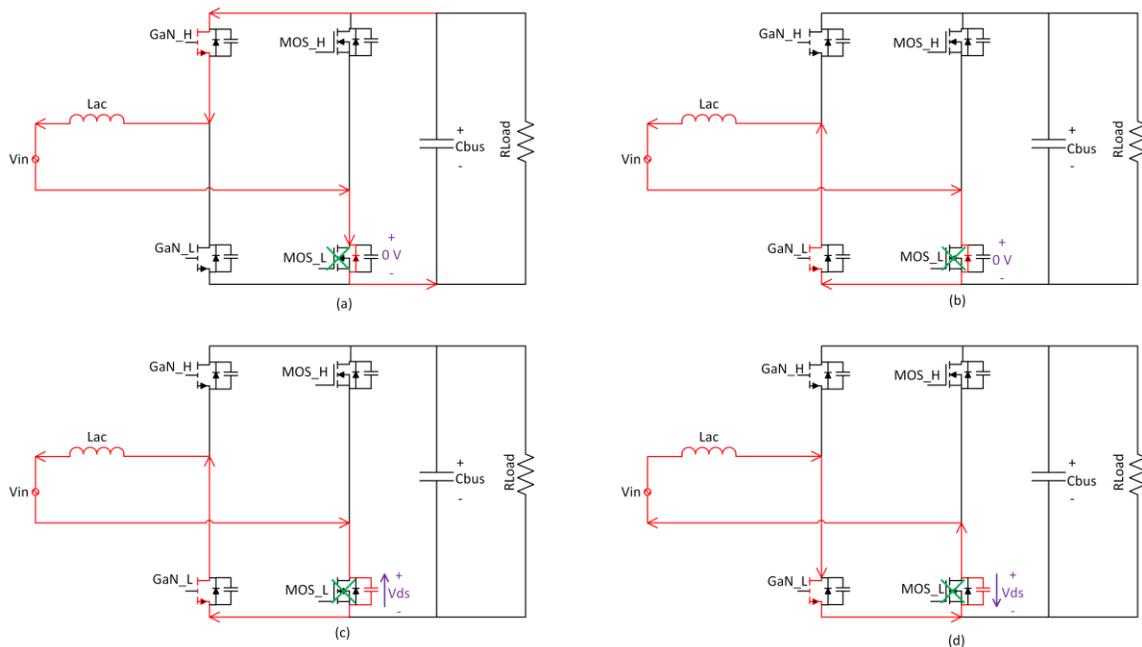


Figure 4.4: MOSFET drain to source voltage fluctuation during RCM

Note: Intervals (a)-(d) are titled in coherence with the stages shown in Figure 4.5.

The solution presented in Figure 4.3 (a) to block the reverse current is preferred for its simple application. According to this approach, the LF leg MOSFET is forced switched OFF during the RCM instance to effectively eliminate reverse current conduction.

If reverse recovery of the MOSFET is considered in the analysis, there still remains a possibility of small reverse conduction through the LF MOSFET body diode. Due to the presence of input inductor in the conduction path, this small current eventually transfers to the MOSFET C_{oss} to change the voltage distribution across the LF leg MOSFETs.

When the inductor current drops to zero during positive half cycle RCM interval, even if MOS_L is kept off, some reverse recovery current still flows through the MOS_L body diode as shown in Figure 4.4 (a). A practical waveform of the same instance is presented in sub-interval (a) of Figure 4.5. The reverse inductor current can rise quickly during this time. The voltage across MOS_L remains zero since the diode is conducting. In the next switching cycle, when the active switch GaN_L turns on, the inductor current keeps on flowing in the same direction due to its continuous nature. The MOS_L body diode conducts the reverse current until all of its reverse recovery charge is depleted. MOS_L drain-source voltage remains zero throughout this interval as shown in Figure 4.5 (b). Once the body diode's junction is devoid of all charges, it stops conducting reverse current. The inductor current then finds a path to flow through the MOS_L C_{oss} . A typical value of C_{oss} being in the range of a few hundred pico-farads results in a quick rise of MOS_L drain-source voltage. The inductor current drops throughout the time and reaches zero eventually. This is when the voltage across MOS_L rises to its maximum value. This operation is denoted by sub-interval (c) in both Figure 4.4 and Figure 4.5. In the following interval, C_{oss} of MOS_L dissipates quickly through the inductor. Drain-source voltage of MOS_L drops to zero again as the body diode of MOS_L starts to conduct the forward current. This discharging interval is shown in Figure 4.4 (d). As long as the PFC operates in RCM, MOS_L C_{oss} keeps charging and discharging in consecutive switching cycles and results in a rapid fluctuation of the voltage across MOS_L . Following the discussion in section 3.2, this high dv/dt of MOSFET drain-source voltage increases the CM noise of PFC significantly.

The fluctuation of the LF leg MOSFET drain-source voltage during RCM can be observed in the totem-pole PFC prototype as shown in Figure 4.5.

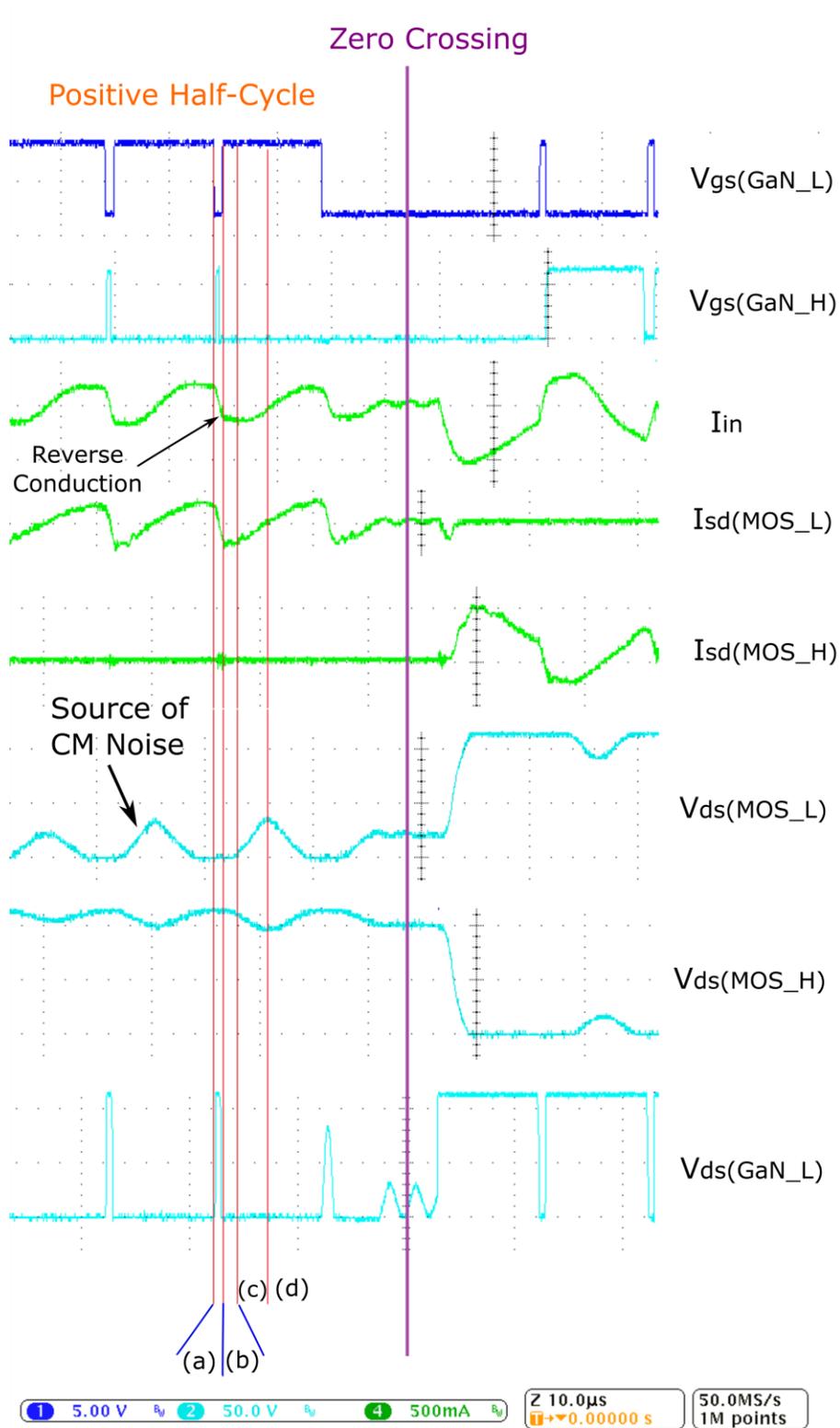


Figure 4.5: Generation of CM noise during RCM

Note: Combined image of multiple waveforms aligned at same switching instance

Simulation of a totem-pole PFC shows the fluctuation of MOS_L drain-source voltage during RCM interval and its effect on generated noise. The waveforms are presented in Figure 4.6.

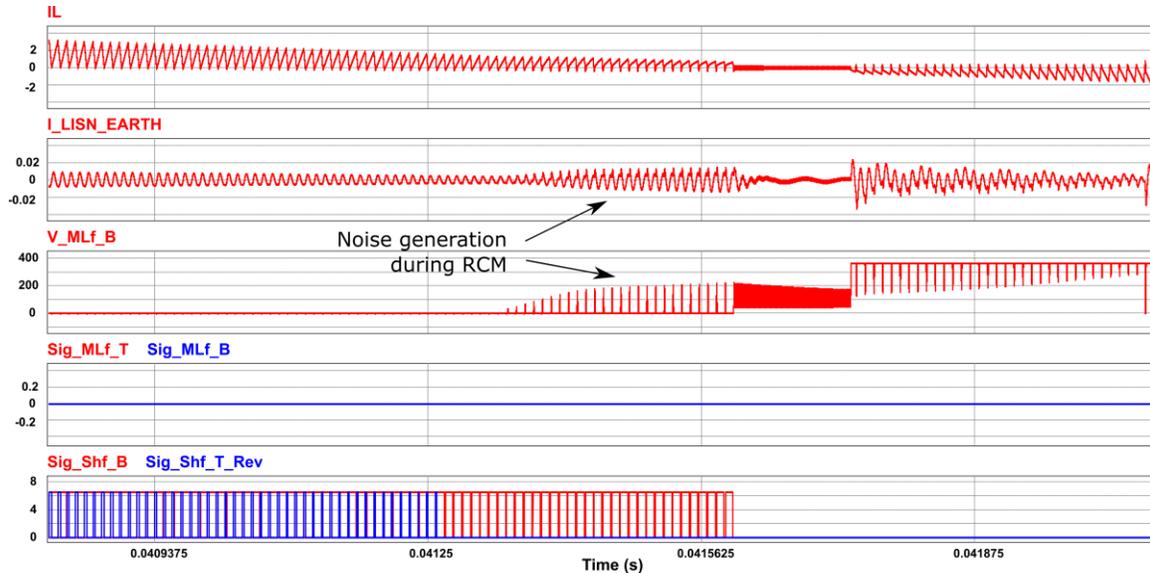


Figure 4.6: CM noise generation during RCM

Fluctuation in the MOS_L drain-source voltage can occur even when both responsible switches are forced OFF during RCM. In this case, MOS_L body diode conducts the reverse recovery current and GaN_H output capacitor charges up consequently. Depending on the output capacitor size of the GaN switch, this reverse current may reach a high enough value to change the $MOS_L C_{oss}$ voltage in the next switching cycle.

One possible way to deal with this issue is by implementing the switching pattern presented in Figure 4.3 (b). In this approach, synchronous GaN switch is forced OFF but the LF leg MOSFET is kept ON during the RCM operation. Since the MOSFET channel is conducting during the whole time, its voltage remains constantly zero throughout. $GaN_H C_{oss}$ together with $GaN_L C_{oss}$ acts as a voltage divider to block the dc bus voltage. A simulation of the totem-pole PFC shows significant improvement applying this approach as shown in Figure 4.7.

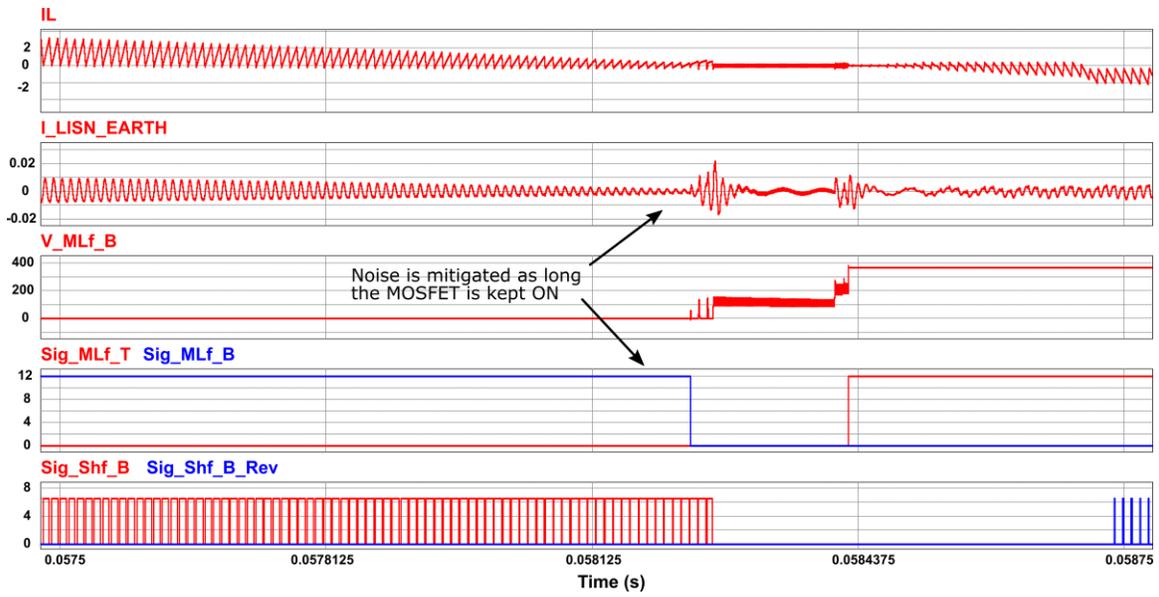


Figure 4.7: Mitigation of CM noise during RCM

Chapter 5. Design Implementation of Totem-pole PFC

5.1 Design Equations

The equations to calculate the power stage of a totem-pole PFC are established in this work. Design equations are necessary for developing the product from scratch and vital for the selection of components. Some key design equations are presented here. A detailed explanation of derivation process can be found in Appendix B.

The duty cycle of the PFC switch changes with varying input ac voltage. An average duty can be measured by equation (5-1) where η is the efficiency and PF is the power factor.

$$D = \frac{(V_{out} - V_{in(rms)}) PF \eta}{V_{out}} \quad (5-1)$$

If the input inductor of the PFC is L and switching frequency is denoted f_{sw} , then the peak-to-peak current ripple in the inductor will be

$$\Delta I_L = \frac{V_{in(rms)} D}{L f_{sw}} \quad (5-2)$$

Assuming average current control mode, the average of the actual inductor current will be the average of the calculated reference current. Average inductor current can be calculated by equation (5-3).

$$I_{L(Avg)} = \frac{2\sqrt{2}}{\pi} \frac{P_{out}}{V_{in(rms)} PF \eta} \quad (5-3)$$

RMS inductor current is another important parameter, especially when designing the inductor. This can be calculated by equation (5-4).

$$I_{L(RMS)} = \frac{P_{out}}{V_{in(rms)} PF \eta} \sqrt{1 + \frac{\Delta I_L^2}{12 I_{L(Avg)}^2}} \quad (5-4)$$

For designing the inductor, peak current of the inductor must be known precisely. The inductor current reaches the peak during the peak of the ac half cycle. At this moment, the duty and inductor current ripple can be calculated by the equations below.

$$D_{pk} = \frac{V_{out} - \sqrt{2} V_{in(rms)} PF\eta}{V_{out}} \quad (5-5)$$

$$\Delta I_{L(pk)} = \frac{\sqrt{2} V_{in(rms)} PF\eta D_{pk}}{L f_{sw}} \quad (5-6)$$

From this, the peak inductor current can be precisely calculated by equation (5-7).

$$I_{L(max)} = \sqrt{2} \frac{P_{out}}{V_{in(rms)} PF\eta} + \frac{\Delta I_{L(pk)}}{2} \quad (5-7)$$

RMS current through the high-frequency GaN HEMT can be calculated as shown in equation (5-8).

$$I_{HF(RMS)} = \frac{P_{out}}{PF\eta V_{in(rms)}} \sqrt{1 + \frac{\Delta I_L^2}{12 I_{L(Avg)}^2}} \sqrt{0.5 - 0.6 \frac{PF\eta V_{in(rms)}}{V_{out}}} \quad (5-8)$$

Similarly, the RMS current through the low-frequency leg MOSFET can be calculated by equation (5-9).

$$I_{LF(RMS)} = \frac{P_{out}}{\sqrt{2} V_{in(rms)} PF\eta} \sqrt{1 + \frac{\Delta I_L^2}{12 I_{L(Avg)}^2}} = \frac{I_{L(RMS)}}{\sqrt{2}} \quad (5-9)$$

The RMS current of the boost diode, or in the case of synchronous operation, the current through the synchronous switch is calculated by equation (5-10).

$$I_{D(RMS)} = P_{out} \sqrt{1 + \frac{\Delta I_L^2}{12 I_{L(Avg)}^2}} \sqrt{\frac{4\sqrt{2}}{3\pi PF\eta V_{out} V_{in(rms)}}} \quad (5-10)$$

The equations were verified with careful simulation. The results are presented in Table 5-1. The equations precisely calculate the currents and hence very convenient for designing the totem-pole PFC.

Table 5-1: Verification of design equations from simulation

Description	Symbol	Unit	Equation	Simulation	Error (%)
Inductor Current RMS	$I_{L(RMS)}$	A_{RMS}	6.517	6.458	0.90
Maximum Inductor Current	$I_{L(max)}$	A_{pk}	9.982	9.933	0.49
HF FET RMS Current	$I_{HF(RMS)}$	A_{RMS}	2.394	2.362	1.36
LF FET RMS Current	$I_{LF(RMS)}$	A_{RMS}	4.608	4.567	0.90
Boost Diode RMS Current	$I_{D(RMS)}$	A_{RMS}	1.948	1.960	0.62

Input RMS voltage is 240 Vac. PFC output power is 1.5 kW

5.2 GaN Half-Bridge Design

5.2.1 Evaluation Board Overview

For building the totem-pole PFC prototype, Gallium-nitride devices manufactured by *GaN Systems Inc.* is used. A half-bridge evaluation board (EVB) from *GaN Systems* using 650V devices GS66508T formed the high-frequency leg of the PFC. A simplified diagram of the HF GaN leg is shown in Figure 5.1. The top side cooled 650V GaN HEMT devices are mounted at the bottom of the EVB with an accompanying heat sink [64]. To drive the GaN HEMTs, the EVB requires a 9-12V dc input.

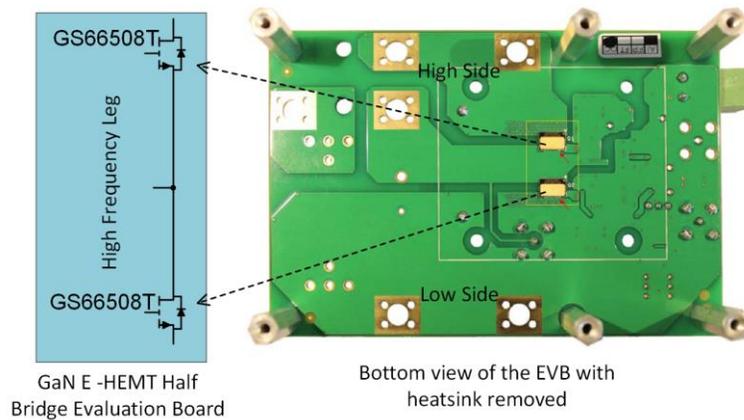


Figure 5.1: High-frequency GaN leg of the totem-pole PFC

5.2.2 Gate Drive Design

The GaN half-bridge has two devices in series. One device is adjacent to the negative dc bus and usually referred to as the low-side device. The other GaN is connected to the positive dc bus and called the high-side GaN. The GaN half-bridge EVB utilizes two isolated gate drive ICs SI8261BIC from *Silicon Labs*. Since the gate signals generated by the control circuit are referenced to the negative dc bus, it is necessary to use an isolated gate drive IC for the high-side GaN. To keep the symmetry between both gate-drives, the low-side gate drive is also implemented using the same isolated IC. Symmetric gate circuit is important to ensure similar propagation delay in both drivers. Powering the high-side gate drive is also a challenge. The voltage of the high-frequency leg mid-point fluctuates depending on which GaN is ON or OFF at a particular moment. If the high-side device is ON, the midpoint voltage is essentially the output bus voltage. If

the low-side GaN is ON, the midpoint voltage is zero with respect to the negative dc bus. This fluctuating midpoint voltage makes it a challenging task to drive the high-side GaN.

To turn the high-side GaN ON, a voltage equal to the driving voltage (~6V) must be applied between the gate and source of this device. Since the source is connected to the high-frequency leg mid-point, the source voltage keeps fluctuating. This makes it impossible to employ a power supply referenced to the negative dc bus to drive the high-side GaN. There are two popular approaches for solving this issue. First and a slightly expensive solution is to use an isolated supply for the gate drive IC. The design involves a small transformer to isolate the gate drive power circuit from the rest of the system. A small flyback or push-pull converter can perform the task of isolation. Additional control circuitry then is required to maintain the accurate power flow. Though expensive, this approach is usually preferred for high-speed drive.

Another approach for designing a high-side gate drive is bootstrap supply. Here a bootstrap diode followed by an energy storage capacitor is employed to drive the gate IC. Since no extra transformer or control circuitry is required, this is a cheaper alternative for driving the high-side gate. But for this design to work properly, the low-side device must turn ON periodically in order to charge the energy storage capacitor. In a totem-pole PFC high-frequency leg, the top and bottom devices always switch alternatively, so charging the bootstrap capacitor is not an issue for this topology. However, the capacitor has to be sized for appropriate switching frequency to ensure that the gate drive voltage does not fall below the threshold voltage of the GaN. The drawback of this approach is that the switching frequency is limited by the bootstrap diode. The diode goes through a repetitive reverse biased condition in each switching cycle and most diodes can response fast only up to a certain high frequency. Since the totem-pole PFC in this work is driven only at 100 kHz, it is convenient to use a bootstrap supply for this prototype. The EVB is equipped with a built-in bootstrap supply which is shown in Figure 5.2.

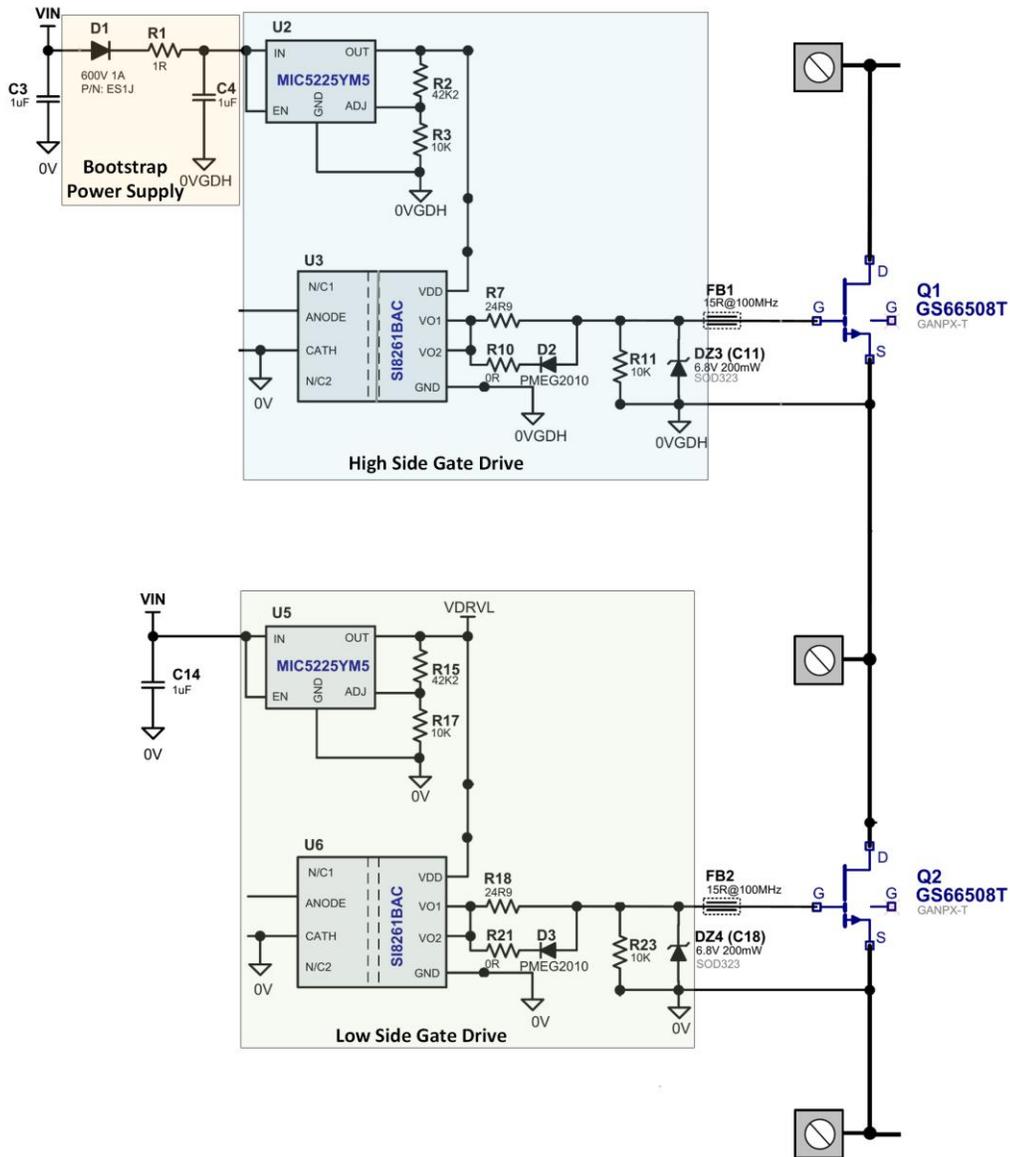


Figure 5.2: Gate drive circuitry from GaN EVB user manual [64]

Though the GaN can switch at a very high frequency, the gate ICs available commercially do not allow very high CMTI (common-mode transient immunity). The SI8261BIC gate drive IC has a minimum CMTI of 35 KV/ μ S. To preserve the purity of the gate signal from transient noise, a gate resistance of 24.9 Ω is used for the charging path. This additional gate resistance ensures a rise time of approximately 50ns for the GaN HEMTs and limits the CMTI within 20 KV/ μ S for a 400V bus. The return path consists of a diode and a 0 Ω resistor for fast turn off.

5.3 Low-Frequency Half-Bridge Leg Design

The low-frequency leg of the totem-pole PFC is constructed using two IPZ60R041P6 MOSFETs from *Infineon*. This is a four pin MOSFET with a kelvin source connection for reducing the gate loop inductance.

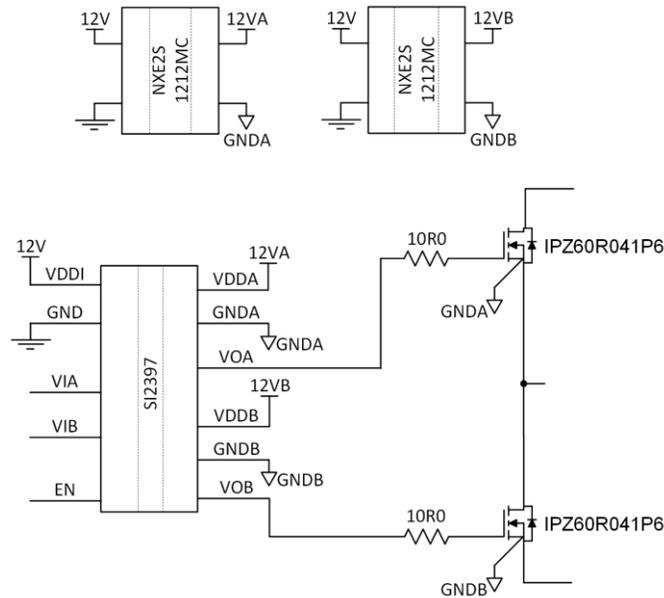


Figure 5.3: Low-frequency leg gate drive connection

The high-side MOSFET requires an isolated gate drive for proper operation. The driving voltage of a MOSFET is approximately 12V. So a 12V isolated half-bridge driver SI2397 from *Silicon Labs* is used to construct the drive circuit of the low-frequency leg. The gate drive IC is powered by a 12V supply referenced to the negative dc bus. Two input signals VIA and VIB are isolated from the output side of the IC.

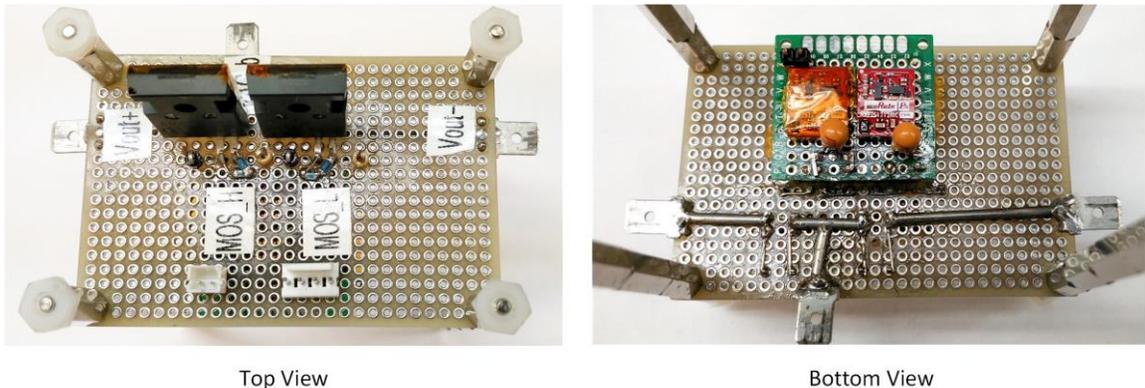


Figure 5.4: Low-frequency MOSFET leg of the prototype

To power the drive circuit on the output side, a bootstrap circuit may be employed as before. But the low-frequency leg of the PFC operates only at line frequency (60Hz), so the energy storage capacitor in the bootstrap circuit will be substantially large for powering the gate drive throughout the total ac half cycle. Instead of using a bulky capacitor for the bootstrap circuit, an isolated power supply approach is considered preferable for driving the low-frequency leg. Two 12V-12V isolated power supplies NXE2S1212MC from *Murata* are used to build this prototype. The low-frequency MOSFETs' rise and fall time are controlled by a 10Ω gate resistance.

5.4 Inductor Design

The input side inductor is a very important component in the design of totem-pole PFC. It is preferable that the inductor size remains reasonably small to reduce the total manufacturing cost and to ensure high power density. The inductor for the prototype was calculated for 1.5 kW output power.

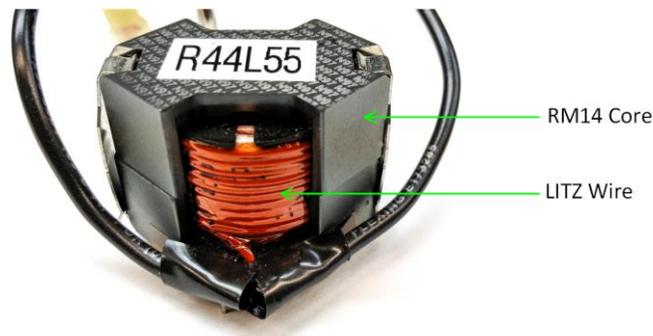


Figure 5.5: Inductor designed for the prototype

The calculated inductor current is 8.3A with a peak-peak ripple of 3.5A for 1.5 kW output power. Minimum input voltage was assumed to be 187V for which the PFC output will be regulated to 385V. The required inductance was calculated to be 237.5μH from equation (5-11).

$$L = \frac{\sqrt{2}V_{in(min)}D_{max}}{\Delta I_{L(max)}f_{sw}} \quad (5-11)$$

For designing the inductor, *N97* core material was selected because of its better efficiency at high frequency. With a core gap of 2.45 mm, an RM14 core can achieve the desired inductance with 40 turns of wire. Since the inductor carries high-frequency current

in totem-pole PFC, it is important to minimize the skin effect in the inductor wire. Litz wire is specially designed to reduce the skin effect and proximity effect losses, and therefore is preferred over solid wire for constructing the inductor. The finished inductor has an equivalent series resistance of 55 m Ω .

5.5 Current Sensing and Zero-crossing Detection

The inductor current is sensed using a Hall Effect sensor (ACS716) from *Allegro Microsystems*. The current flows through the copper conduction path of the Hall sensor and the sensor detects the generated magnetic field to produce a proportional voltage at the output. The current conduction path is electrically isolated from the sensor signals, so an additional opto-coupler is not necessary. The current sensor output voltage has two components- zero current offset voltage and a voltage proportional to the input current.

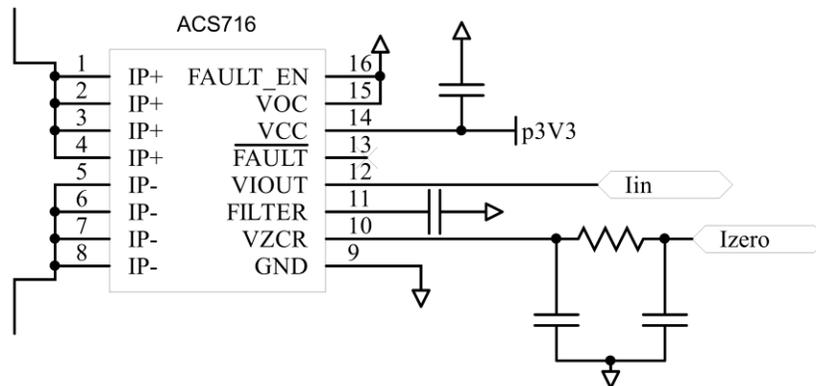


Figure 5.6: Hall effect sensor connections

Accurate detection of the ac zero-crossing is particularly important for a power factor correction circuit. In a totem-pole PFC, both input lines transition to a different voltage level at zero-crossing. So a simple way to detect the zero-crossing is by comparing the individual line voltages with respect to the negative dc bus. A zero-crossing detection circuit is shown in Figure 5.7. For many applications, it is common practice to isolate the signals from the sensing circuit and then compare to get a stable reference. But in this topology, it is possible to achieve zero-crossing detection without isolating the signals. This is an inexpensive solution for product development.

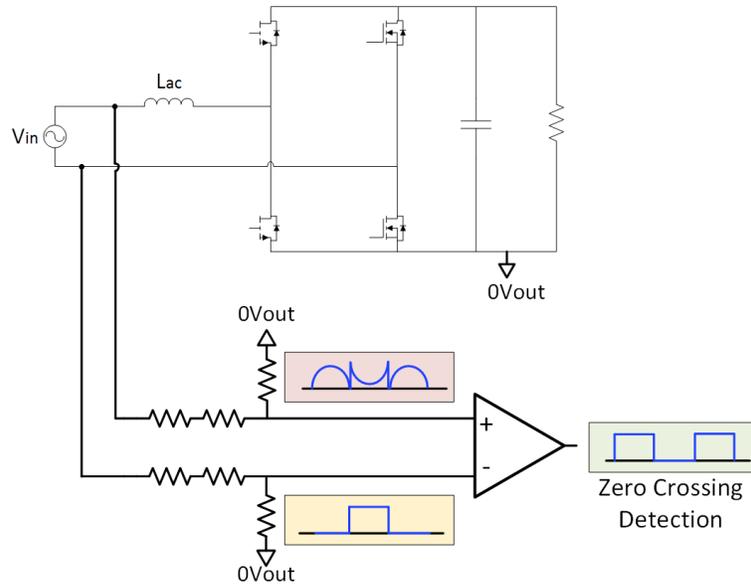


Figure 5.7: Zero-crossing detection circuit for totem-pole PFC

Quick detection of the zero-crossing is important for ensuring unity power factor. Since the input voltage rises slowly after the zero-crossing, it is preferable not to restrict the sensed voltages in Figure 5.7 within the logic level (3.3V-5V) but to let it rise to a value two or three times the logic level. The voltages detected by the voltage divider are not sinusoidal for a totem-pole PFC. During the negative half cycle, both sensed voltages are offsetted to the dc bus voltage. In the prototype design, the voltage dividers from V_{in} are set in such a way that the sensed voltage peak is around 12V-15V for 385V output bus. This voltage is carefully selected based on the acceptable input limit of the comparator IC.

5.6 Experimental Setup and Result

The final prototype consists of four major sections- the high-frequency leg, input inductor, the low-frequency leg and a control board. The switching frequency of the GaN HEMT is 100 kHz. The prototype has an Inrush current protection circuit at the input side that consists of few PTC thermistors and a relay switch. The relay is operated by the controller. The inrush protection circuit is followed by the hall sensor. A diode bridge can also be added before the PFC to bypass any surge current.

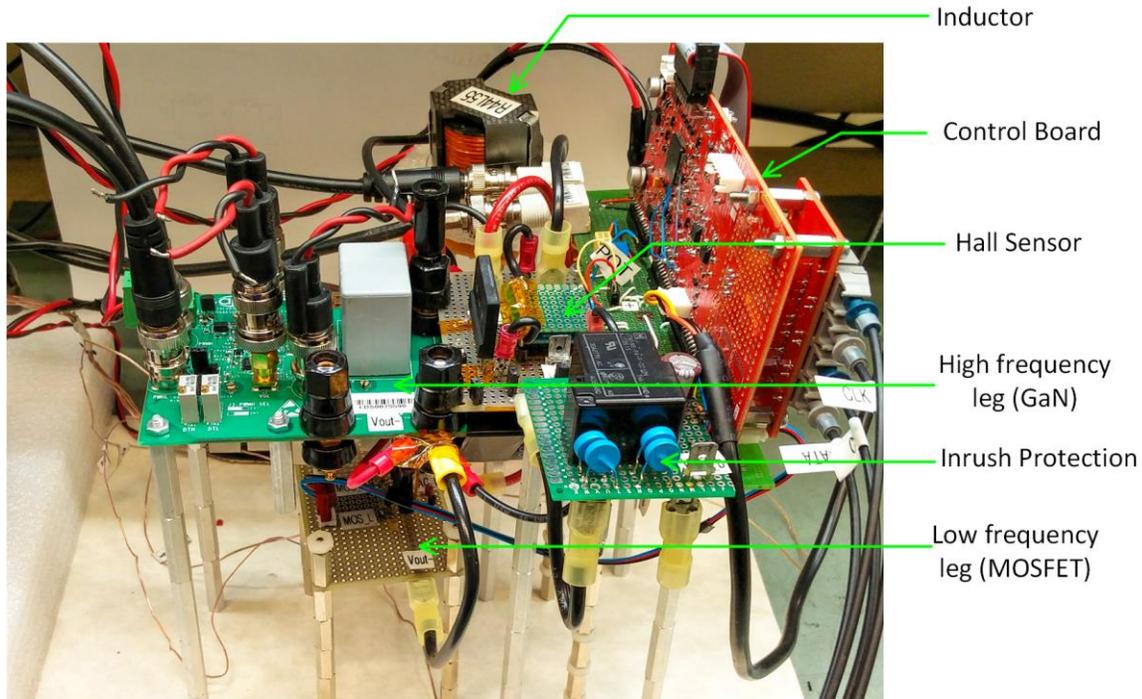


Figure 5.8: Totem-pole PFC prototype

A microcontroller (TMS320F28035) from *Texas Instruments* performs the control loop calculations and executes the protection measures. A voltage divider from the output bus serves as a feedback signal for the voltage control loop while simultaneously works as the input for over-voltage protection (OVP) mechanism. Feedback from the Hall sensor is read through a set of ADCs by the microcontroller in each switching cycle to perform the current control loop calculation. The hall sensor output also serves as the input for over-current protection (OCP) mechanism.

The GaN HEMTs show superior performance even at low voltage, light load condition. Unlike silicon MOSFET, the GaN parasitic capacitors remain small under low voltage condition. Figure 5.9 shows the input voltage and current waveforms when the PFC is working under 30% of full bus voltage (~115V). The relative stability of dynamic capacitance values enables GaN totem-pole PFCs to be operated efficiently under a wide range of voltage and power. Even at a very light load, the PFC ensures a power factor of 0.99.

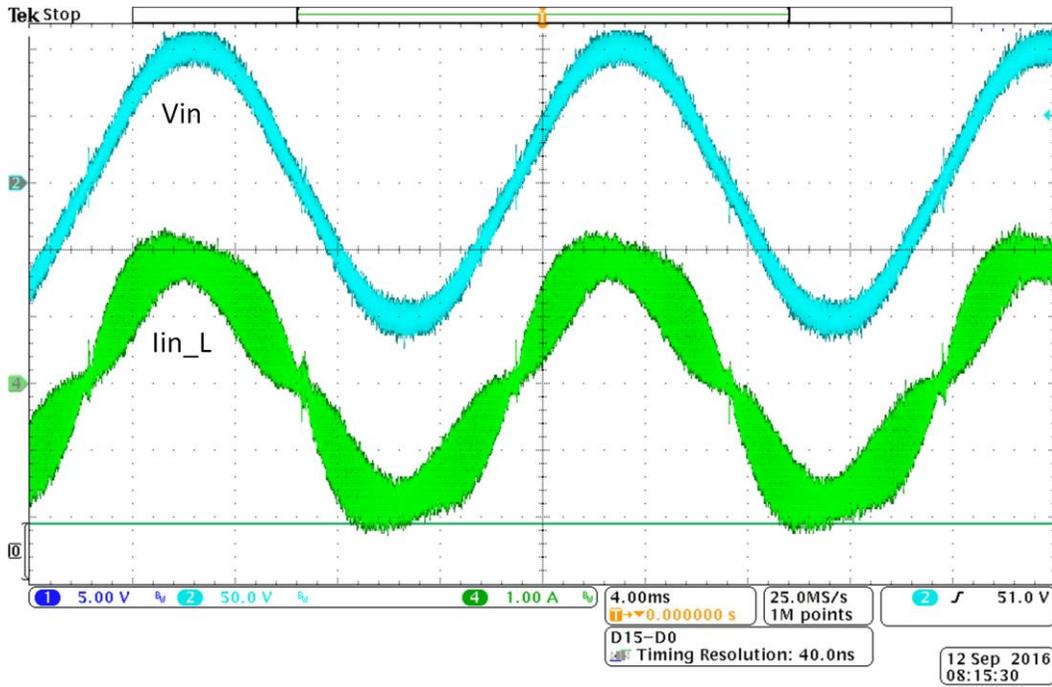


Figure 5.9: Input voltage and current of the totem-pole PFC prototype

Note: Prototype working at 100W. Switching frequency is 100 kHz.

Chapter 6. Conclusions

6.1 Summary

In this thesis, a totem-pole PFC is developed using Gallium Nitride (GaN) HEMTs. After careful comparison between potential topologies, totem-pole PFC was selected as the suitable topology for designing high-efficiency telecom power supplies. CM noise generated in bridgeless PFC topologies has always been the limiting factor and totem-pole PFC, though very efficient, shows severe CM noise at ac zero-crossings. Part of this thesis is devoted to exploring this issue and new observations through mathematical modeling have been made. A previously unreported issue of noise generation around the zero-crossing point has been reported and explained too. The key findings and novel contributions of this thesis is listed below.

- The efficiency of competing bridgeless topologies are compared through simulation using different WBG devices and switching approach. It is found that synchronously operated totem-pole PFC using GaN HEMT is efficient for a wide range of power over competing topologies.
- A modified CM noise model at zero-crossings of totem-pole PFC is developed to facilitate the analysis of spike current issue.
- The rapid change in low-frequency leg MOSFET drain-source voltage is identified as the principal source of CM noise at zero-crossings. The spike current at zero-crossing is shown as a consequence of this rapid change of voltage, not the root cause of the noise as assumed by several earlier publications. A simulation model using LISN is presented to capture and identify the noise at zero-crossing.
- An equivalent circuit at ac zero-crossing is developed to outline the effect of various circuit parameters on CM noise generation.
- The effect of PFC bus voltage, inductor size, low-frequency leg MOSFET output capacitor and reverse recovery current on CM noise generation is established through a set of equations. This analysis can potentially serve as additional design considerations for selecting appropriate inductor size and MOSFET parameters, especially in tightly regulated EMI applications.
- An alternative switching approach to mitigate the zero-crossing CM noise is proposed and implemented. Already suggested approaches from published literatures have also been revisited and experimentally evaluated.

- The challenges associated with synchronous switching in totem-pole PFC are outlined in detail. It is shown that, around the zero-crossing point, the inductor current may flow in the reverse direction depending on the switching conditions. This instance is identified as reverse conduction mode (RCM). A set of switching techniques has been proposed to avoid the reverse current flow.
- A newfound source of CM noise generated in reverse conduction mode is reported. Reverse recovery charge of the low-frequency leg MOSFET has been identified as the origin of this noise. An appropriate switching technique to avoid this issue is proposed and verified by simulation.
- A set of design equations for totem-pole PFC is established and later verified through simulation.
- Appropriate design solutions for the gate drive and zero-crossing detection circuit are proposed. It was implemented that a bootstrap power supply for high-side GaN can operate reliably at 100 kHz switching frequency. The high-side gate drive of low-frequency leg requires a big capacitor for the bootstrap circuit, so an isolated supply is preferred. Finally, an inexpensive zero-crossing detection circuit is also presented.

6.2 Future Work

Based on the knowledge accumulated and experience gained throughout the course of this thesis, following directions may be considered for future research.

- Operating the prototype at full power and taking efficiency measurement.
- Increasing the frequency of operation. For high-frequency switching, the gate drive for GaN HEMTs may require an isolated supply. CMTI of gate drive IC is another limiting factor for increasing the switching frequency.
- An interleaved continuous conduction mode totem-pole PFC can be developed especially for high power applications.
- Electro Magnetic Interference (EMI) issues at the zero-crossings have been discussed in this work. The overall EMI analysis and mitigation techniques of totem-pole PFC are considered the tail-end activity for the prototype development and therefore it's a topic for future research.
- Finally, a PCB board can be designed to test the competing GaN devices offered by other manufacturers. Since GaN technology is still very much under development, it is important to test competing devices from different

manufacturers. The structure of GaN HEMT and their driving technique varies widely over different manufacturers, therefore, it is preferable to design the PCB board using a 'daughter card' approach. The main board will accommodate everything except the high-frequency leg GaNs with a slot for mounting the daughter card. Individual daughter card can then be designed for different GaN devices. This approach will guarantee optimized gate driving circuit while ensuring rapid prototyping.

References

- [1] B. N. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.
- [2] H.-L. Cheng, Y.-C. Hsieh, and C.-S. Lin, "A Novel Single-Stage High-Power-Factor AC/DC Converter Featuring High Circuit Efficiency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 524–532, Feb. 2011.
- [3] Hung-Liang Cheng, Chun-An Cheng, and Chu-Shen Chang, "A novel single-stage HPF AC/DC converter with integrated buck-boost and flyback converters," in *2013 International Symposium on Next-Generation Electronics*, 2013, pp. 146–149.
- [4] L. Petersen and M. Andersen, "Two-stage power factor corrected power supplies: the low component-stress approach," *APEC. Seventeenth Annu. IEEE Appl. Power Electron. Conf. Expo. (Cat. No.02CH37335)*, vol. 2, no. c, pp. 1195–1201, 2002.
- [5] IEC, "IEC 61000-3-2 Electromagnetic compatibility (EMC) - Part 3-2: Limits for harmonic current emissions (equipment input current ≤ 16 A per phase)," 2005.
- [6] IEEE, *Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems IEEE Recommended Practices and*, vol. 1992, no. June. 1992.
- [7] ON Semiconductor, "Power factor correction (PFC) handbook," p. 130, 2011.
- [8] Zaohong Yang and P. Sen, "Recent developments in high power factor switch-mode converters," in *Conference Proceedings. IEEE Canadian Conference on Electrical and Computer Engineering (Cat. No.98TH8341)*, 1998, vol. 2, pp. 477–480.
- [9] V. C. Percy and R. Ramaprabha, "Design and implementation of multilevel type full-bridge converter for telecom power supplies," in *2014 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2014]*, 2014, pp. 239–244.
- [10] K. I. Hwu and Y. T. Yau, "An Interleaved AC-DC Converter Based on Current Tracking," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1456–1463, May 2009.
- [11] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase PFC topologies based on the boost converter," in *2010 9th IEEE/IAS International Conference on Industry Applications - INDUSCON 2010*, 2010, pp. 1–6.
- [12] M. M. Jovanovic, "Power Supply Technology – Past , Present , and Future."

- [13] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.
- [14] D. Han and B. Sarlioglu, "Performance Evaluation of GaN-Based Synchronous Boost Converter under Various Output Voltage, Load Current, and Switching Frequency Operations," *J. Power Electron.*, vol. 15, no. 6, pp. 1489–1498, Nov. 2015.
- [15] A. Bindra, "Wide-Bandgap-Based Power Devices: Reshaping the power electronics landscape," *IEEE Power Electron. Mag.*, vol. 2, no. 1, pp. 42–47, Mar. 2015.
- [16] T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 402–405.
- [17] K. Patel, "GaN is Great, True GaN™ is Better!," *Avogy Technical paper*, 2016. [Online]. Available: <http://avogy.com/wp-content/uploads/2016/06/GaN-is-Great-v4.pdf>. [Accessed: 06-Nov-2016].
- [18] B. J. Baliga, "SiC power devices: From conception to social impact," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, 2016, vol. 423, no. 1, pp. 192–197.
- [19] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.
- [20] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and Application of 600 V GaN HEMT in Cascode Structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.
- [21] H. Li, C. Yao, C. Han, J. A. Brothers, X. Zhang, and J. Wang, "Evaluation of 600 V GaN based gate injection transistors for high temperature and high efficiency applications," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 85–91.
- [22] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.
- [23] G. Meneghesso, M. Meneghini, E. Zanoni, P. Vanmeerbeek, and P. Moens, "Trapping induced parasitic effects in GaN-HEMT for power switching applications," *2015 Int. Conf. IC Des. Technol. ICICDT 2015*, no. iv, 2015.
- [24] A. Fernandez, J. Sebastian, M. M. Hernando, P. Villegas, and J. Garcia, "Helpful Hints to Select a Power-Factor-Correction Solution for Low- and Medium-Power Single-Phase Power Supplies," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 46–

55, Feb. 2005.

- [25] Jindong Zhang, M. Jovanovic, and F. Lee, "Comparison between CCM single-stage and two-stage boost PFC converters," in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, 1999, vol. 1, pp. 335–341 vol.1.
- [26] W. M. Lin, M. M. Hernando, A. Fernandez, J. Sebastian, and P. J. Villegas, "A New Topology for Passive PFC Circuit Design to Allow AC-to-DC Converters to Comply with the New Version of IEC1000-3-2 Regulations," 1995, pp. 3–8.
- [27] A. Fernandez, A. Ferreres, P. Villegas, J. Sebastian, and L. Alvarez, "Size comparison between a half bridge converter with an AICS and a two-stage boost converter operating in a narrow input voltage range," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, 2001, vol. 4, pp. 1793–1798.
- [28] S. Abdel-rahman, F. Sückler, and K. Siu, "PFC boost converter design guide," 2016.
- [29] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," *Integr. Power Electron. Syst. (CIPS), 2012 7th Int. Conf.*, pp. 1–22, 2012.
- [30] C. Da Cunha Duarte and I. Barbi, "A new family of ZVS-PWM active-clamping DC-to-DC boost converters: analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 12, no. 5, pp. 824–831, 1997.
- [31] M. M. Jovanovic and Yungtaek Jang, "A new, soft-switched boost converter with isolated active snubber," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 496–502, 1999.
- [32] Il-Oun Lee, D. Y. Lee, and B. H. Cho, "High performance boost PFC pre-regulator with improved zero-voltage-transition (ZVT) converter," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, 2002, pp. 1387–1391.
- [33] M. M. Jovanovic and Y. Jang, "State-of-the-Art, Single-Phase, Active Power-Factor-Correction Techniques for High-Power Applications—An Overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.
- [34] P. N. Enjeti and R. Martinez, "A high performance single phase AC to DC rectifier with input power factor correction," in *Proceedings Eighth Annual Applied Power Electronics Conference and Exposition*, 1993, vol. 11, no. 2, pp. 190–195.
- [35] W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, "Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction," *IET Power Electron.*, vol. 1, no. 2, p. 194, 2008.

- [36] A. F. de Souza and I. Barbi, "High power factor rectifier with reduced conduction and commutation losses," in *21st International Telecommunications Energy Conference. INTELEC '99 (Cat. No.99CH37007)*, 1999, p. 158.
- [37] B. Lu, R. Brown, and M. Soldano, "Bridgeless PFC implementation using one cycle control technique," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2005, vol. 2, pp. 812–817.
- [38] Haoyi Ye, Zhihui Yang, Jingya Dai, Chao Yan, Xiaoni Xin, and Jianping Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in *2004 10th International Workshop on Computational Electronics (IEEE Cat. No.04EX915)*, 2004, pp. 575–582.
- [39] P. Kong, S. Wang, and F. C. Lee, "Common Mode EMI Noise Suppression for Bridgeless PFC Converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291–297, Jan. 2008.
- [40] Liu Guihua, Wang Wei, Liu Jing, and Xu Dianguo, "Research on conventional PFC and bridgeless PFC in air conditioner," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, vol. 3, pp. 666–669.
- [41] Y. Jang and M. M. Jovanovic, "A Bridgeless PFC Boost Rectifier With Optimized Magnetic Utilization," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.
- [42] L. Huber, Yungtaek Jang, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
- [43] X. Xin, T. Liu, J. Zeng, H. Wu, and J. Ying, "Asymmetrical H-PFC for Low Line Applications," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 1077–1081.
- [44] P. Wong and F. C. Lee, "A Novel Concept in Integrating PFC and DC / DC Converters."
- [45] Jinjun Liu, Weiyun Chen, Jindong Zhang, Dehong Xu, and F. C. Lee, "Evaluation of power losses in different CCM mode single-phase boost PFC converters via a simulation tool," in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*, vol. 4, pp. 2455–2459.
- [46] Gang Yao, Haiyang He, Yan Deng, and Xiangning He, "A ZVT PWM Three Level Boost Converter for Power Factor Preregulator," in *37th IEEE Power Electronics Specialists Conference*, pp. 1–5.
- [47] J. Zhang, Z. Lu, and B. Su, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electron.*, vol. 5, no. 3, pp. 358–365, Mar. 2012.

- [48] J. C. Salmon, "Circuit topologies for single-phase voltage-doubler boost rectifiers," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 521–529, 1993.
- [49] Weiming Lin, Junlai Huang, Jinhui Wang, and Jianhua Zou, "A novel high efficiency soft-switched PWM boost rectifiers with low conduction losses," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, 2008, vol. 1, pp. 1340–1346.
- [50] W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, "An improved bridgeless PFC boost-doubler rectifier with high-efficiency," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 1309–1313.
- [51] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.
- [52] B. Su, J. Zhang, and Z. Lu, "Totem-Pole Boost Bridgeless PFC Rectifier With Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.
- [53] Bin Su and Zhengyu Lu, "An Interleaved Totem-Pole Boost Bridgeless Rectifier With Reduced Reverse-Recovery Problems For Power Factor Correction," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1406–1415, Jun. 2010.
- [54] S. Bontemps, A. Basler, and P. L. Doumergue, "Evaluation of the need for SiC SBD in parallel with SiC MOSFETs in a module phase leg configuration," *PCIM Eur. 2015; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag. Proc.*, no. May, pp. 19–21, 2015.
- [55] J. Brown and G. Moxey, "Power MOSFET basics: Understanding gate charge and using it to assess switching performance," *Vishay Siliconix Appl. Note 605*, 2003.
- [56] B. Zhang, K. Shi, Q. Lin, G. M. Dousoky, M. Shoyama, and S. Tomioka, "Conducted noise reduction of totem-pole bridgeless PFC converter using GaN HEMTs," in *2015 IEEE International Telecommunications Energy Conference (INTELEC)*, 2015, pp. 1–5.
- [57] L. Xue, Z. Shen, D. Boroyevich, and P. Mattavelli, "GaN-based high frequency totem-pole bridgeless PFC design with digital implementation," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 759–766.
- [58] B. Sun, "How to reduce current spikes at AC zero-crossing for totem-pole PFC," *Analog Appl. Journal, Texas Instruments*, 2015.
- [59] Satoshi Tomioka, "Bridgeless power factor correction converter," U.S. Patent 20120069615 A1, 2011.

- [60] Y. Tang, W. Ding, and A. Khaligh, "A bridgeless totem-pole interleaved PFC converter for plug-in electric vehicles," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, vol. 2016–May, pp. 440–445.
- [61] B. Zhang, Q. Lin, Y. Shimada, J. Imaoka, M. Shoyama, and S. Tomioka, "Analysis and reduction method of conducted noise in GaN HEMTs based totem-pole bridgeless PFC converter," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 274–278.
- [62] Junfei Wang, Feng Zheng, Yu Zhang, Peikang Wang, Xiaoyu Yang, and Depeng Bai, "A new control method for boost converter in discontinuous conduction mode with synchronous rectification and zero voltage switching," in *2013 IEEE ECCE Asia Downunder*, 2013, pp. 650–654.
- [63] L. Zhou, Y. Wu, J. Honea, and Z. Wang, "High-efficiency True Bridgeless Totem Pole PFC based on GaN HEMT: Design Challenges and Cost-effective Solution," *PCIM Eur. 2015; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag. Proc.*, no. May, pp. 1–8, 2015.
- [64] GaN Systems Inc., "GS66508T -EVBHB 650V GaN E -HEMT Half Bridge Evaluation Board User's Guide." [Online]. Available: http://gansystems.com/evaluationboards/GS66508TEVBHB_UserGuide_rev2151020.pdf. [Accessed: 13-Nov-2016].

Appendix A.

Analysis of Equivalent Circuit

This section provided detail analysis of the equivalent circuit presented in page.51.

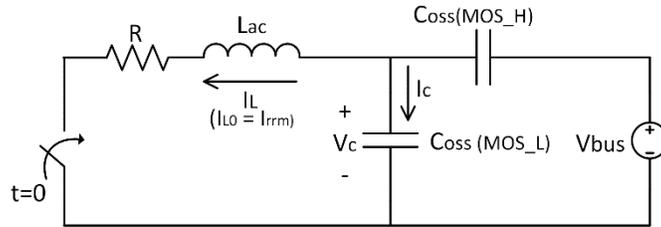


Figure A.1: Negative to positive zero-crossing equivalent circuit

For $t < 0$, we assume that the inductor current is equal to the maximum reverse recovery current and both MOS_H and MOS_L shares that current equally. The initial conditions are

$$I_L(0^-) = I_L(0^+) = I_{rrm} \quad (A-1)$$

$$V_c(0^-) = V_c(0^+) = V_{bus} \quad (A-2)$$

$$I_c(0^-) = I_c(0^+) = -\frac{I_{rrm}}{2} \quad (A-3)$$

Now,

$$I_c = C_{oss} \frac{dV_c}{dt}$$

$$\text{or, } \frac{dV_c(0^+)}{dt} = \frac{I_c(0^+)}{C_{oss}} = -\frac{I_{rrm}}{2C_{oss}} \quad (A-4)$$

For $t = \infty$, if this circuit is allowed to run for infinite time, MOS_H C_{oss} will block the full DC voltage and the final values the circuit parameters will be

$$V_c(\infty) = 0 \quad (A-5)$$

$$I_L(\infty) = 0 \quad (A-6)$$

To obtain the natural response of the circuit, the DC source has been turned OFF and the circuit is redrawn as below:

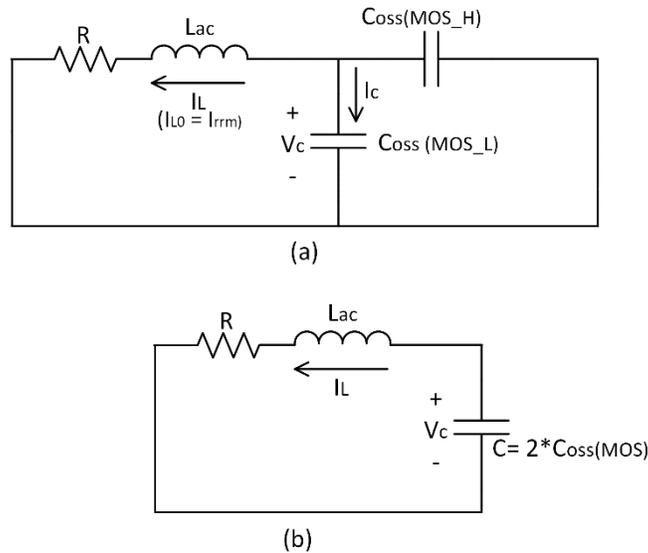


Figure A.2: Circuit for obtaining natural response

By combining both MOSFET C_{oss} into one, we can obtain a simple RLC circuit as shown in Figure A.2 (b). Here, $C = 2 * C_{oss}(MOS)$

Using KVL in the loop

$$-V_c + L_{ac} \frac{dI_L}{dt} + RI_L = 0 \quad (A-7)$$

And capacitor current

$$I_L = C \frac{dV_c}{dt} \quad (A-8)$$

Combining both equations we can get

$$\frac{d^2V_c}{dt^2} + \frac{R}{L_{ac}} \frac{dV_c}{dt} + \frac{V_c}{L_{ac}C} = 0 \quad (A-9)$$

The characteristics equation of this differential equation is

$$s^2 + \frac{R}{L_{ac}}s + \frac{1}{L_{ac}C} \quad (A-10)$$

The roots of this equation are

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \quad (A-11)$$

Here ω_0 is the undamped natural frequency.

$$\alpha = \frac{R}{2L_{ac}} \quad (A-12)$$

$$\omega_0 = \frac{1}{\sqrt{L_{ac}C}} \quad (A-13)$$

In the equivalent circuit, the resistance R is made of inductor ESR and in the range of few m Ω . Whereas the capacitor C_{oss} is in the range of few hundred Pico-farads. So for a practical case $\alpha \ll \omega_0$ and the response is always underdamped. This makes the roots imaginary

$$s_{1,2} = -\alpha \pm j \omega_d \quad (A-14)$$

Where the damped natural frequency is calculated as,

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \quad (A-15)$$

So the natural response of the system is

$$V_{cn}(t) = e^{-\alpha t} (A_1 \cos \omega_d t + A_2 \sin \omega_d t) \quad (A-16)$$

And the forced response is

$$V_{cf}(t) = V_c(\infty) = 0 \quad (A-17)$$

So the complete response is

$$V_c(t) = V_{cf}(t) + V_{cn}(t)$$

$$V_c(t) = e^{-\alpha t} (A_1 \cos \omega_d t + A_2 \sin \omega_d t) \quad (A-18)$$

Applying the initial condition from equation (A-2), we can find

$$A_1 = V_{bus} \quad (A-19)$$

Differentiating equation (A-18) and then using the initial condition from equation (A-4) we can derive

$$\frac{dV_c(0^+)}{dt} = -\alpha A_1 + A_2 \omega_d$$

$$A_2 = -\frac{I_{rrm}}{C \omega_d} + \frac{\alpha}{\omega_d} A_1 = -\frac{I_{rrm}}{C \omega_d} + \frac{V_{bus} \alpha}{\omega_d} \quad (A-20)$$

Substituting the value of A_1 and A_2 into equation (A-18) we get the final response of V_c .

$$V_c(t) = e^{-\alpha t} (V_{bus} \cos \omega_d t - \frac{I_{rrm}}{C \omega_d} \sin \omega_d t + \frac{V_{bus} \alpha}{\omega_d} \sin \omega_d t) \quad (A-21)$$

If we assume the resistance R negligible, then

$$\alpha = \frac{R}{2L_{ac}} = 0$$

$$\omega_d = \omega_0$$

And equation (A-21) becomes

$$V_c(t) = V_{bus} \cos \omega_0 t - \frac{I_{rrm}}{C \omega_0} \sin \omega_0 t \quad (A-22)$$

For simplifying the following calculations, we assume that

$$a = V_{bus} \quad (A-23)$$

$$b = \frac{I_{rrm}}{C \omega_0} \quad (A-24)$$

So equation (A-22) becomes

$$V_c(t) = a \cos \omega_0 t - b \sin \omega_0 t \quad (A-25)$$

From equation (3-1) in section 3.3 we know that the CM noise current at zero-crossing is defined by

$$I_{fg} = -C_{fg} \frac{d}{dt} (V_{ds(MOS_L)})$$

It logical to analyze the derivative of $V_c(t)$ of equation (A-25) since this is the actually the drain-source voltage of MOS_L in the noise equation.

Let's assume $N(t)$ is a noise function. Then

$$I_{fg} = -C_{fg} \frac{d}{dt}(V_{ds(MOSL)}) = -C_{fg} \frac{d}{dt}(V_C) = C_{fg} N(t) \quad (A-26)$$

Where,

$$N(t) = -\frac{d}{dt}(V_C) = a \omega_0 \sin \omega_0 t + b \omega_0 \cos \omega_0 t \quad (A-27)$$

$N(t)$ serves as a noise function in this analysis. The higher the value of $N(t)$, the higher the CM noise at zero-crossing. To find the maxima of $N(t)$, we first take the derivative of $N(t)$ and equate it to zero.

$$\frac{dN(t)}{dt} = a\omega_0^2 \cos \omega_0 t - b\omega_0^2 \sin \omega_0 t$$

$$\text{Or, } \tan \omega_0 t = \frac{a}{b} \quad (A-28)$$

From equation (A-28) we can find the exact time when the noise current will be maximum during transition period. But we are more interested to know the effect of circuit parameters on noise generation, so to find the maximum noise $N(t)_{max}$ we can replace the value of $\omega_0 t$ in equation (A-27) using inverse trigonometry and derive equation

$$N(t)_{max} = a \omega_0 \frac{a}{\sqrt{a^2+b^2}} + b \omega_0 \frac{b}{\sqrt{a^2+b^2}}$$

$$N(t)_{max} = \omega_0 \sqrt{a^2 + b^2} \quad (A-29)$$

Replacing the value of a, b from equation **Error! Reference source not found.**, REF eqA24 \h (A-24) into (A-29), we get

$$N(t)_{max} = \sqrt{(V_{bus} \omega_0)^2 + \left(\frac{i_{rrm}}{C}\right)^2} \quad (A-30)$$

Where

$$C = 2 C_{oss}(MOS)$$

$$\omega_0 = \frac{1}{\sqrt{L_{ac}C}}$$

Ignoring R means the total capacitor voltage V_c appears across the inductor in Figure A.2 (a). From there it can be calculated that

$$L_{ac} \frac{dI_L(t)}{dt} = V_c(t)$$

$$\text{or, } \frac{dI_L(t)}{dt} = \frac{V_c(t)}{L_{ac}}$$

$$\text{or, } I_L(t) = \frac{1}{L_{ac}} \int (V_{bus} \cos \omega_0 t - \frac{I_{rrm}}{C \omega_0} \sin \omega_0 t) dt$$

$$\text{or, } I_L(t) = \frac{V_{bus}}{L_{ac} \omega_0} \sin \omega_0 t + \frac{I_{rrm}}{L_{ac} C \omega_0^2} \cos \omega_0 t + U$$

$$\text{or, } I_L(t) = V_{bus} \sqrt{\frac{2 C_{oss}}{L_{ac}}} \sin \omega_0 t + I_{rrm} \cos \omega_0 t + U \quad (\text{A-31})$$

$$\text{At } t = 0, I_L(0) = I_{rrm}$$

Replacing this into equation (A-31)

$$U = 0$$

So

$$I_L(t) = V_{bus} \sqrt{\frac{2 C_{oss}}{L_{ac}}} \sin \omega_0 t + I_{rrm} \cos \omega_0 t \quad (\text{A-32})$$

Let's assume

$$I_L(t) = x \sin \omega_0 t + y \cos \omega_0 t \quad (\text{A-33})$$

Where,

$$x = V_{bus} \sqrt{\frac{2 C_{oss}}{L_{ac}}}$$

$$y = I_{rrm}$$

Differentiating equation (A-33) and setting the derivative of $I_L(t)$ to zero, we can write

$$\tan \omega_0 t = \frac{x}{y} \quad (A-34)$$

Replacing the angle $\omega_0 t$ from equation (A-34) into equation (A-33) we can get

$$I_L(t)_{peak} = \sqrt{x^2 + y^2}$$

$$\text{or, } I_L(t)_{peak} = \sqrt{\left(V_{bus} \sqrt{\frac{2 C_{oss}}{L_{ac}}}\right)^2 + (I_{rrm})^2}$$

Appendix B.

Derivation of Design Equations

The totem-pole PFC appears as a resistance to the input line. The ratio of the input current and voltage is therefore independent of time and it can be called the 'emulated resistance' R_E .

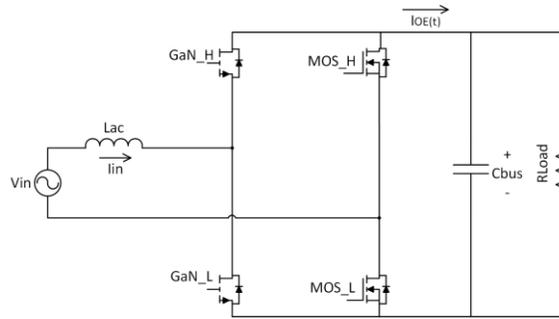


Figure B.1: Totem-pole PFC

So, R_E can be written in terms of time varying quantities

$$R_E = \frac{V_{in}(t)}{I_{in}(t)} \quad (B-1)$$

$$\text{or, } I_{in}(t) = \frac{V_{in}(t)}{R_E} \quad (B-2)$$

Setting a time varying instantaneous output current $I_{OE}(t)$, we get

$$PF \eta V_{in}(t) I_{in}(t) = V_{out} I_{OE}(t) \quad (B-3)$$

$$\text{or, } PF \eta V_{in}(t) \frac{V_{in}(t)}{R_E} = V_{out} I_{OE}(t)$$

$$\text{or, } I_{OE}(t) = \frac{PF \eta V_{in}^2(t)}{R_E V_{out}} \quad (B-4)$$

The relationship between the input and the output power is

$$P_{in} = \frac{V_{in,rms}^2}{R_E} = \frac{P_{out}}{PF \eta} \quad (B-5)$$

$$\text{or, } R_E = \frac{PF \eta V_{in,rms}^2}{P_{out}} \quad (B-6)$$

Replacing the value of R_E into equation (B-4),

$$I_{OE}(t) = \frac{P_{out} V_{in}^2(t)}{V_{out} V_{in,rms}^2} \quad (B-7)$$

Average current through the active switch of a boost dc-dc converter is

$$I_{SW_DCDC} = \frac{I_{out}}{1-D} \sqrt{D \left(1 + \frac{r^2}{12}\right)} \quad (B-8)$$

Since in the boost PFC, the input and output are function of time, we can write

$$I_{SW_Boost_PFC} = \frac{I_{OE}(t)}{1-D(t)} \sqrt{D(t) \left(1 + \frac{r^2}{12}\right)} \quad (B-9)$$

$$\text{Here, } r = \frac{\Delta I_L}{I_{L,avg}} \quad (B-10)$$

The duty period is a function of time for a PFC.

$$D(t) = \frac{V_{out} - PF \eta V_{in}(t)}{V_{out}} \quad (B-11)$$

And replacing the value of $D(t)$ and $I_{OE}(t)$ in equation (B-9), we get

$$I_{SW_Boost_PFC} = \frac{P_{out} V_{in}(t)}{PF \eta V_{in,rms}^2} \sqrt{\left(1 + \frac{r^2}{12}\right)} \sqrt{\frac{V_{out} - PF \eta V_{in}(t)}{V_{out}}} \quad (B-12)$$

Now, for totem-pole PFC, the switch only carries for half the line cycle. So the RMS of the switch current of totem-pole PFC can be measured from-

$$I_{SW_TPPFC_RMS} = \left[\frac{1}{\left(\frac{1}{f_{line}}\right)} \int_0^{1/2 f_{line}} \left(\frac{P_{out} V_{in}(t)}{PF \eta V_{in,rms}^2} \sqrt{\left(1 + \frac{r^2}{12}\right)} \sqrt{\frac{V_{out} - PF \eta V_{in}(t)}{V_{out}}} \right)^2 dt \right]^{1/2}$$

After carrying out the integration, we can find that

$$I_{SW_TPPFC_RMS} = \frac{P_{out}}{PF \eta V_{in,rms}} \sqrt{\left(1 + \frac{r^2}{12}\right)} \sqrt{0.5 - 0.6 \frac{PF \eta V_{in,rms}}{V_{out}}} \quad (B-13)$$

The RMS inductor current of the totem-pole PFC can be calculated the same way as a boost converter.

$$I_L = I_{L,avg} \sqrt{\left(1 + \frac{r^2}{12}\right)}$$

$$\text{or, } I_L = \frac{I_{OE}(t)}{1-D(t)} \sqrt{\left(1 + \frac{r^2}{12}\right)}$$

$$I_L = \frac{P_{out} V_{in}(t)}{PF \eta V_{in,rms}^2} \sqrt{\left(1 + \frac{r^2}{12}\right)} \quad (B-14)$$

So, the RMS current is

$$I_{L_TPPFC_RMS} = \left[\frac{1}{(1/2f_{line})} \int_0^{1/2f_{line}} \left(\frac{P_{out} V_{in}(t)}{PF \eta V_{in,rms}^2} \sqrt{\left(1 + \frac{r^2}{12}\right)} \right)^2 dt \right]^{1/2}$$

After carrying out the integration, we can find

$$I_{L_TPPFC_RMS} = \frac{P_{out}}{PF \eta V_{in,rms}} \sqrt{\left(1 + \frac{r^2}{12}\right)} \quad (B-15)$$

Other circuit parameters can be calculated from equations (B-13) and (B-15).