Micromachined Devices for Impedance Matching in Automotive Power Line Communications

by

Xiao Luo

B.Sc., Huazhong University of Science and Technology, 2008

Thesis Submitted in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

in the
School of Mechatronic Systems Engineering
Faculty of Applied Sciences

© Xiao Luo 2016

SIMON FRASER UNIVERSITY

Spring 2016

All rights reserved.
However, in accordance with the *Copyright Act of Canada*, this work may be reproduced, without authorization, under the conditions for "Fair Dealing." Therefore, limited reproduction of this work for the purposes of private study, research, criticism, review and news reporting is likely to be in accordance with the law, particularly if cited appropriately.

Approval

Name:	**Xiao Luo**
Degree:	**Master of Applied Sciences**
Title:	***Micromachined Devices for Impedance Matching in Automotive Power Line Communications***

Examining Committee: **Chair:** Dr. Majid Bahrami
Professor

Dr. Behraad Bahreyni
Senior Supervisor
Associate Professor

Dr. Woo Soo Kim
Supervisor
Assistant Professor

Dr. Ash Parameswaran
Internal Examiner
Professor
School of Engineering Science

Date Defended/Approved: April 13, 2016

Abstract

In power line communication (PLC), the signals are carried and distributed by the wiring system. It is a promising technology which uses the existing system and has wide coverage; however, the impedances at the interface of the power line and the loads are not well defined. The mismatch in the impedances causes potentially high attenuation. This problem can be addressed by developing impedance matching circuit using tunable components based on micro-electromechanical systems (MEMS). In this thesis, the MEMS-based approach was investigated. The tunable inductors and capacitors were designed, fabricated and characterized. A microfabrication process was designed to realize thin membranes attach to the structural layer. The deflection was characterized for a range of actuating voltages. The tunable capacitors were employed in the matching network and tested. The test results were compared with the theoretical results and discussed. This thesis demonstrates the electrostatically actuated MEMS devices and matching network that can work in the PLC system. Furthermore, this thesis should serve as the groundwork for students who wish to design the impedance matching networks or who wish to fabricate electrostatically actuated MEMS devices with thin membranes of their own.

Keywords: PLC; MEMS; Impedance matching circuit; Tunable capacitor

Dedication

I would like to dedicate my thesis to my beloved parents. I hope that I can complete the dream that you had for me all these years.

Acknowledgements

I would like to thank my senior supervisor Dr. Behraad Bahreyni. I am grateful to pursue my master study under his supervision. His sage advice, insightful criticisms, and patience aided my study as well as project research. During these years, his encouragement and help me overcome sorts of difficulties. Without his patience and valuable help, this thesis would not have been possible.

I am grateful to Dr. Woo Soo Kim and Dr. Ash Parameswaran for being on my committee and reviewing my thesis. I also feel very grateful to Dr. Lutz Lampe for providing the opportunity to take part in this project.

I would like to thank all my labmates in IMuTS lab especially Sadegh, Amin, and Ibrahim.

Last but not least, I would like to take this opportunity to thank my parents, Huiming Luo and Xianping Ma, for their constant support and love.

Table of Contents

Approval ii
Abstract iii
Dedication iv
Acknowledgements v
Table of Contents vi
List of Tables viii
List of Figures ix
List of Acronyms xiii

Chapter 1. Introduction 1
1.1. Motivation and Background 1
1.2. Outline of the thesis 4

Chapter 2. Literature Review 6
2.1. Impedance Matching 6
2.1.1. Maximum Power Transfer Theorem 7
2.1.2. Reflection Coefficient 7
2.1.3. Types of Impedance Matching Networks 8
2.2. Tunable Impedance Matching Networks 13
2.2.1. Tunable Micromachined Inductors 17
2.2.2. Tunable Micromachined Capacitors 20

Chapter 3. Fabrication 29
3.1. Device Plan View and Cross Section 29
3.2. Proposed Fabrication Process 32
3.2.1. RCA Clean 32
3.2.2. Sputtering 33
3.2.3. Photolithography 35
3.2.4. Fabrication of Conductive Membranes 38
3.3. Fabrication Process 42
3.3.1. Fabrication Process for Capacitors 42
3.3.2. Fabrication Process for Inductors 43

Chapter 4. Tunable Inductors 45
4.1. Simulations 45
4.1.1. Simplified Solenoid Inductors 45
4.1.2. Planar Inductors 46
4.2. Experiment 47
4.3. Test Results of Tunable Inductors 50

Chapter 5. Tunable Capacitors **56**
5.1. Theory and Design 56
5.1.1. Maximum Displacement 56
5.1.2. Breakdown Voltage 59
5.1.3. Capacitance of the Tunable Capacitor 60
5.2. Test Results of Tunable Capacitors 62

Chapter 6. Tunable Impedance Matching Network **71**
6.1. Access Impedance Range 71
6.2. Impedance Matching Simulation in ADS 73
6.3. Test Result of the Matching Network 80

Chapter 7. Conclusion and Future work **86**

References **88**

Appendix A. Matlab Code to Calculate Inductance Values **93**

Appendix B. Test Results for a Tunable Capacitor **97**

List of Tables

Table 3-1: The RCA cleaning process ... 33

Table 4-1: The simulation results of planar inductors ... 47

Table 4-2: The different parameters of ten planar inductors ... 48

Table 4-3: Test results of inductor L1 ... 51

Table 5-1: Calculated capacitances of capacitors with three different radii for different amounts of deflection at the centre of the membrane ... 61

Table 5-2: The matched impedances with tunable capacitor ... 65

Table 5-3: The matched impedances of the improved T-type matching network ... 66

Table 5-4: The matched impedances of the improved T-type matching network with a different C2 ... 67

Table 6-1: Theoretical and measured results ... 80

Table 6-2: Test results of the matching network with a tunable capacitor ... 84

List of Figures

Figure 1-1: A diagram of impedance matching network 3

Figure 1-2: Schematic of T-type matching network 4

Figure 2-1: The reflection coefficient 8

Figure 2-2: Schematic of the frequency-variable tuner. [9] ©2001 IEEE. 9

Figure 2-3: Schematic of the reconfigurable matching network with 8 switched MEMS capacitors. [10] ©2004 IEEE. 9

Figure 2-4: L-type matching networks. (a)Network for Z_L inside the 1+jx circle. (b)Network for $Z_L$outside the 1+jx circle 10

Figure 2-5: Two element LC impedance matchings 11

Figure 2-6: Forbidden regions of two element LC impedance matching 11

Figure 2-7: (a) Capacitor bridged double Pi-type network. (b) Its Pi network equivalence. [11] ©2013 IEEE 12

Figure 2-8: SEM picture of the fabricated MIM capacitor. [12] ©2010 IEEE. 13

Figure 2-9: The diagram of active inductor 14

Figure 2-10: Equivalent circuit of active inductor 14

Figure 2-11: PN junction under (a) forward bias and (b) reverse bias 16

Figure 2-12: Varactor diode circuit symbol 17

Figure 2-13: Energy dissipation phenomena of inductive devices on a lossy substrate 18

Figure 2-14: Top view of the 3D model structure of the proposed variable inductor. [16] ©2010 IEEE. 19

Figure 2-15: Copper electroplated solenoid variable inductor with silicon stepper. [19] ©2005 IEEE. 20

Figure 2-16: Tuning schemes based on different configuration of the magnetic core. (a) C-shape; (b) Q-shape; (c) a-shape. [20] ©2004 IEEE. 20

Figure 2-17: Schematic of a parallel capacitor 21

Figure 2-18: Schematic of mechanical and electrical force on the movable electrode 22

Figure 2-19: Schematic view of a dual-gap relay-type tunable capacitor. [27] ©2004 IEEE. 23

Figure 2-20: Two gap tunable capacitor structure. [28] ©2008 IEEE. 23

Figure 2-21: Layout and cross-sectional view of the parallel-plate MEMS tuning elements. [29] ©2007 IEEE. 24

Figure 2-22: A tunable capacitor with tri-state structure. [30] ©2008 IEEE. 24

Figure 2-23: (a) Air-bridge shunt ohmic switch top view; (b)Tunable capacitor with a tri-state structure based on a toggle push-pull mechanism. [31] ©2009 IEEE. 25
Figure 2-24: Schematic of the piezoelectric bimorph actuator. [32] ©2010 IEEE. 26
Figure 2-25: Schematic of the electro-thermal microactuator. [33] ©2014 IEEE. 27
Figure 2-26: Schematic of the magnetostatic actuator. [34] ©2005 IEEE........ 28
Figure 3-1: The proposed tunable capacitor: (a) plan view and (b) cross-section. 30
Figure 3-2: The proposed tunable inductor: (a) plan view and (b) cross-section. 31
Figure 3-3: Corona Vacuum Coaters for sputtering 34
Figure 3-4: The holder inside Corona Vacuum Coaters 35
Figure 3-5: Spin speed vs. Thickness for SU-8 3000 resists [40] 37
Figure 3-6: The illumination controller and the parameters shown in the meters 38
Figure 3-7: Three conditions of the wafers: (a) image of the wafers and (b) schematic of the membranes 40
Figure 3-8: The unevenness of the film after Corona treatment 41
Figure 3-9: The photograph of Ultrasonic Homogenizer and spraying gun 42
Figure 3-10: Fabrication steps and cross sectional view of the proposed tunable capacitor. (a) Wafer cleaning; (b) Metal deposition; (c) Metal etching; (d) SU-8 spinning; (e) SU-8 patterning; (f) Membrane bonding. 43
Figure 3-11: Fabrication steps and cross sectional view of the proposed tunable inductor. (a) Wafer cleaning; (b) Deposition of Metal 1; (c) Metal 1 etching; (d) Silicon dioxide deposition; (e) Silicon dioxide etching; (f) Deposition of Metal 2; (g) Metal 2 etching; (h) SU-8 spinning; (i) SU-8 patterning; (j) Membrane bonding. 44
Figure 4-1: Schematics of three simulated inductors with different gap between the coil plate and the core 46
Figure 4-2: Schematic of two simulated planar inductors with different gap between the inductor and the film 47
Figure 4-3: Schematic of ten planar inductors with different configurations 49
Figure 4-4: Top view of one planar inductor with cable 50
Figure 4-5: Fitting circuit of the PCB inductor 51
Figure 4-6: Test result of inductor L1 52
Figure 4-7: Test result of inductor L10 with aluminum film, floating (left) and grounded (right) respectively 53
Figure 4-8: Test result of inductor L10 with copper film, floating (left) and grounded (right) respectively 53

Figure 4-9: Test result of inductor L10 with carbon nanoparticles film, floating (left) and grounded (right) respectively 54

Figure 4-10: Test result of inductor L10 with magnetic film, floating (left) and grounded (right) respectively 54

Figure 4-11: Test result of inductor L10 with different films 55

Figure 5-1: Schematic of electric field between two parallel plates 57

Figure 5-2: Schematic of the circular diaphragm membrane. (a) Side view; (b) Top view 59

Figure 5-3: Changes in deflections with the voltages 61

Figure 5-4: Changes in capacitances with the voltages 62

Figure 5-5: Schematic of bias tee 63

Figure 5-6: Test results for a tunable capacitor 64

Figure 5-7: Schematic of T matching network with tunable capacitor 64

Figure 5-8: Range of matched impedances shown in the Smith Chart 65

Figure 5-9: Schematic of improved T matching network with a fixed capacitor in parallel with the tunable capacitor 66

Figure 5-10: Schematic of matched impedances of the improved T-type matching network shown in the Smith Chart 67

Figure 5-11: Schematic of matched impedances of the improved T matching network and different C2 shown in the Smith Chart 68

Figure 5-12: Summary of matched impedances of the T matching network with different C2 69

Figure 5-13: Schematic of matched impedances with tunable C1 70

Figure 6-1: The measured access impedances, (a) Magnitude; (b) Phase. [48] ©2008 IEEE. 72

Figure 6-2: Access impedance range for VPLC applications using frequencies between 1-100 MHz. The values on the chart are normalized to 50 Ω. [49] ©2014 IEEE. 73

Figure 6-3: Schematic of the impedance matching simulation 74

Figure 6-4: Four different configurations of the L-type matching networks 75

Figure 6-5: Paths in the Smith Chart of the matching networks 76

Figure 6-6: T-type matching network. (a) Paths in the Smith Chart; (b) Schematic of ADS circuit. 77

Figure 6-7: Pi-type matching network. (a) Paths in the Smith Chart; (b) Schematic of ADS circuit. 79

Figure 6-8: Circuit of matching network with a tunable capacitor 80

Figure 6-9: Comparison of the real part of the impedances with tunable capacitor changing from 10 pF to 20 pF 81

Figure 6-10: Comparison of the imaginary part of the impedances with tunable capacitor changing from 10 pF to 20 pF 82
Figure 6-11: Set up of testing the matching network with a tunable capacitor 83
Figure 6-12: Change of the real part of the impedances 85

List of Acronyms

AC	Alternating Current
ADS	Advanced Design System
CMOS	Complementary Metal–oxide–semiconductor
DC	Direct Current
EMC	Electromagnetic Compatibility
IPA	Isopropyl Alcohol
MEMS	Micro-electromechanical Systems
MIM	Metal-insulator-metal
MMIC	Monolithic Microwave Integrated Circuit
PEB	Post Exposure Bake
PLC	Power Line Communication
SEM	Scanning Electron Microscope

Chapter 1. Introduction

1.1. Motivation and Background

Originally power lines were designed to transmit electric power from a limited number of sources to a large number of sinks. The power line communication (PLC) technology involves transmitting data signals over a power line, making the power line not only a power carrier but also a signal carrier. The widespread availability of power line makes PLC a promising solution. PLC Technology allows the use of the existing and widespread power distribution infrastructure to provide high-speed networking capabilities along with other benefits [1]. No-additional-wiring makes PLC economically attractive. Compared to other communications, PLC also has the advantages of low cost, good connectivity and reliability.

The applications of PLC involve home automation, home networking, radio broadcasting, and automobile. PLC uses the household electrical power wiring as a transmission medium, enabling remote control of lighting and sensors for alarm systems without installation of additional control wiring [2]. The application areas of home automation range from basic comfort to security and energy conservation. In home automation and intelligent buildings, the power line provides a natural communications link for various devices, such as the sensors of an alarm system [3].

For home networking, the devices only need to be plugged into any outlet in an equipped building to enable communications without expensive rewiring. The company Inari provides home networking and residential access solutions using high data rate PLC communication for the internet, PC, and printer sharing for home and home office [4]. The radio programs can also be fed by special transformers put onto the lines.

Although the electromagnetic environment and the communication network topology in automobiles are very different from the home networking applications, both systems have similarities. As long as taking the characteristics of a power line communication system into account, the automotive applications have a good prospect [5]. One of the main advantages of PLC is an independent communication network, where the existing infrastructure can be reused. The power line has a large area of coverage, and also the access to the power line is relatively simple. Automotive PLC reduces the total amount of communication cables, which also reduces the introduction of electromagnetic compatibility (EMC) by additional electronic elements. It can both support the information transmitted between different nodes and the necessary energy.

Automotive PLC applications include Mechatronics, Telematics and Multimedia. Data, audio and video signals can be transmitted by digital means over power-line in vehicles. Because the power line is not originally designed for communication, PLC faces challenges like varying impedance, considerable noise and high levels of frequency-dependent attenuation when used as a signal communication channel. When the data signals are transferred over the power line, a major challenge is the varying impedance caused by plugging devices into or unplugging from the power line, which leads to high signal attenuation. The receiver cannot receive maximum power from the power line. The communication also has a high dependence of transmitter and receiver location. The locations of the transmitter and receiver have an effect on transmission error rates. PLC is also a complex communication environment. Noise in power lines is a significant problem for data transmission. Typical sources of noise include motors, lamps, switching power supplies and dimmer switches. Both the device's connecting into and disconnecting off the power line will result in high noise peaks. When connecting electronic circuit to the power lines, electromagnetic compatibility problems will arise in the interface. The channel parameters including impedance, attenuation as well as noise levels, fluctuate with time and load, which are very difficult to predict.

When the load impedance changes with the operations, it cannot receive maximum power from the power line (Figure 1-1). In this case, impedance matching network can be used between the power line and the load [6]. Maximum power is delivered when the load is matched to the line and power loss in the power line is

minimized. Impedance matching in a power distribution network may also reduce amplitude and phase errors.

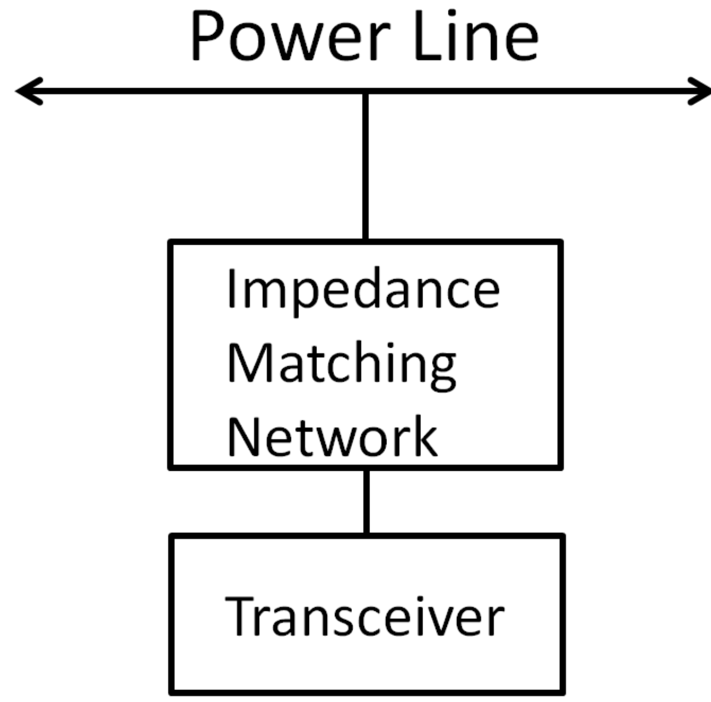


Figure 1-1: A diagram of impedance matching network

In impedance matching network, according to a wide range of topologies, tunable devices are needed. It can be composed of tunable capacitors and fixed inductors, tunable inductors and fixed capacitors, or tunable inductors and capacitors. To realize the tunable devices, two methods can be used to develop the adaptive impedance matching network. On one hand, the integrated circuits can perform the impedance matching electronically with the help of active inductors as well as varactors. [7] shows an matching network with an active capacitor. On the other hand, micro-electromechanical systems (MEMS) are well suited to accomplish small and low-cost adaptive impedance matching. In this thesis, MEMS devices are discussed.

1.2. Outline of the thesis

This thesis presents my work on the development of a tunable impedance matching network based on variable passive components made in MEMS technology. The proposed structure is shown in Figure 1-2. The components can be inductors or capacitors. Both tunable inductors and capacitors are investigated in this work.

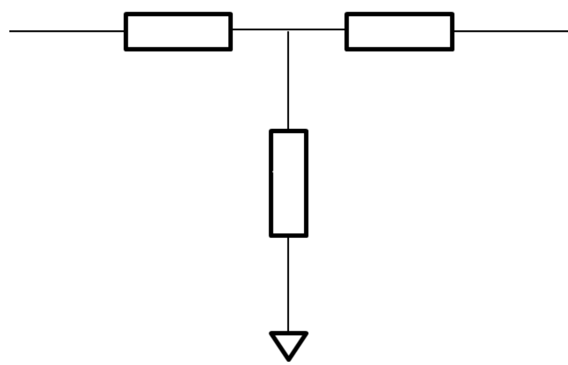


Figure 1-2: Schematic of T-type matching network

This thesis is organized as follows:

Chapter 1 provides motivation and background followed by the outline of the thesis. The power line is not originally designed to transfer signals; therefore, impedance mismatch will lead to high noise and low transfer efficiency. In this case, impedance matching network can be added between the power line and load to mitigate this problem.

Chapter 2 presents the literature review of impedance matching and tunable impedance matching networks. Different types of impedance matching networks are compared. Because of the impedance mismatch, tunable inductors and capacitors are needed.

Chapter 3 describes the fabrication process of the tunable devices. The device cross section is provided and the main steps are elaborated.

Chapter 4 presents the simulation of tunable inductors. Test inductors on PCB were fabricated and tested. The test results were explained.

Chapter 5 elaborates the design steps of tunable capacitors. After careful calculation, the parameters of capacitors were determined. They were fabricated on glass wafers and tested.

Chapter 6 discusses the theory and topology of tunable impedance matching networks. Tunable capacitors were inserted into the network to prove the liability of the design.

Chapter 7 concludes the thesis and discusses the future work.

Chapter 2. Literature Review

2.1. Impedance Matching

Impedance, denoted Z, is an expression of the opposition that an electronic component, circuit, or system offers to alternate electric current. It is the complex (vector) sum of ("real") resistance and ("imaginary") reactance. Reactance corresponds to capacitance and inductance. In a direct current (DC) circuit, resistance is the measure of the degree to which a conductor opposes an electric current through that conductor. All of the materials exhibit resistances at different levels. Low resistance materials are called good conductors while high resistance materials are called insulators. Superconductors have resistances with value close to zero. In alternating current (AC) circuit, capacitance and inductance also impede the flow of current, which is called reactance. The unit of measure is also ohm, but the value is a function of the frequency of the alternating current. The higher the frequency, the smaller the capacitive reactance and the greater inductive reactance.

Impedance matching means the operating state in that the load impedance and the internal impedance of the excitation source matches to each other, leading to a maximum power output. For circuits with different characteristics, matching conditions are not the same. In a purely resistive circuit, when the load resistance is equal to the source resistance, the state is called matching. When the internal excitation source and load impedances contain reactance components, in order to get the maximum power transfer, the load impedance should have the same magnitude but opposite sign to the source [8]. In other words, they should be complex conjugates. This matching condition is called conjugate matching.

2.1.1. Maximum Power Transfer Theorem

For any power source, the maximum power transferred from the power source to the load is when the impedance of the load is equal to the input impedance of the source as viewed from its output terminals. If the source and load are not totally resistive, the reactive components of source and load should be of equal magnitude but opposite phase. For a fixed reactive source, the maximum power theorem maximizes the real power delivered to the load by complex conjugate matching the load to the source. According to the Maximum power transfer theorem, impedance matching network can be inserted between the source impedance Z_S and load impedance Z_L to make an apparent Z_L which is the complex conjugate of Z_S (1-1).

$$Z_S = Z_L^* \tag{1-1}$$

2.1.2. Reflection Coefficient

When a transmission line is connected to a load, a reflection may occur if the impedances of a transmission line and load are not matched. It implies that part of the transmitting energy is reflected back to the source instead of reaching the load. The amplitude of the reflection is called the reflection coefficient, which describes the amplitude of a reflected wave relative to that of the incident wave (Figure 2-1). It can be given by equation (1-2) below, where Z_S is the impedance toward the source, Z_L is the impedance toward the load:

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{1-2}$$

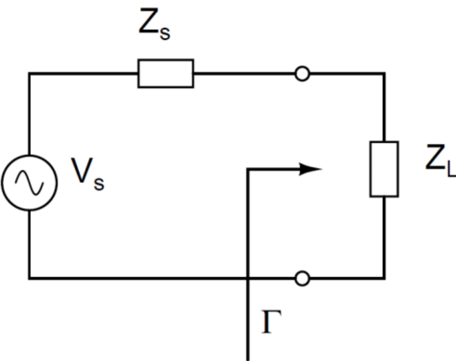


Figure 2-1: The reflection coefficient

The value of reflection coefficient is between -1 and 1. When the load is shorted (Z_S=0), the reflection coefficient is -1, while it is 1 when the load is open ($Z_L = \infty$). The impedance matching happens when the reflection coefficient is 0, which means the power is transferred to load with no reflection. In the case of a complex source impedance Z_S and load impedance Z_L, maximum power transfer is obtained when the source impedance equals the complex conjugate of the load impedance. So the primary goal of a matching network is to achieve impedance matching between the source impedance and the load impedance.

2.1.3. Types of Impedance Matching Networks

In high frequency applications, impedance matching networks/tuners are based on the double-stub or triple-stub topologies. In [9], an artificial tunable inductor is formed by J-inverter and tunable capacitor. The impedance matching network is realized by using Monolithic Microwave Integrated Circuit (MMIC) technology. The schematic can be found in Figure 2-2. However, these topologies occupy a large chip area and are, therefore, not suitable for low frequencies.

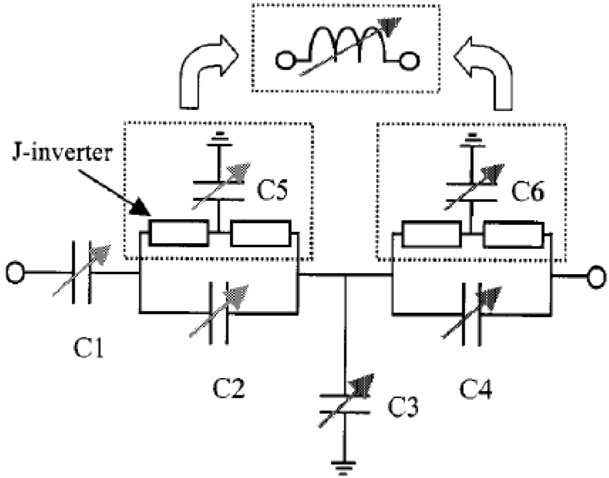


Figure 2-2: Schematic of the frequency-variable tuner. [9] ©2001 IEEE.

Impedance matching network can also be based on a transmission line. With 8 switched MEMS capacitors, the work in [10] provided a total amount of 256 impedance configurations.

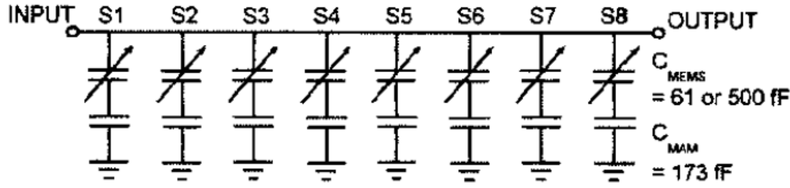


Figure 2-3: Schematic of the reconfigurable matching network with 8 switched MEMS capacitors. [10] ©2004 IEEE.

At low frequencies, the wavelength of the applied voltages and currents is long. In this case wave propagation effects may be neglected. The elements can be considered as lumped and modelled as resistors, inductors and capacitors. The impedance matching networks include L-type, pi-type and T-type. In the network, different values of capacitors and inductors are needed. If the impedance of the load fluctuates, the values of capacitors and inductors should be changed to meet the maximum power transfer requirement.

The simplest type of matching network is the L-section, which uses two reactive elements to match an arbitrary load impedance to a transmission line. Figure 2-4 shows two L-type matching networks. In both configurations, the reactive elements may be either inductors or capacitors, depending on the load impedance. The source is to the left of the LC circuit while the load is the impedance to the right. It is customary to normalize the impedances of L and C to the source impedance of Z_0.

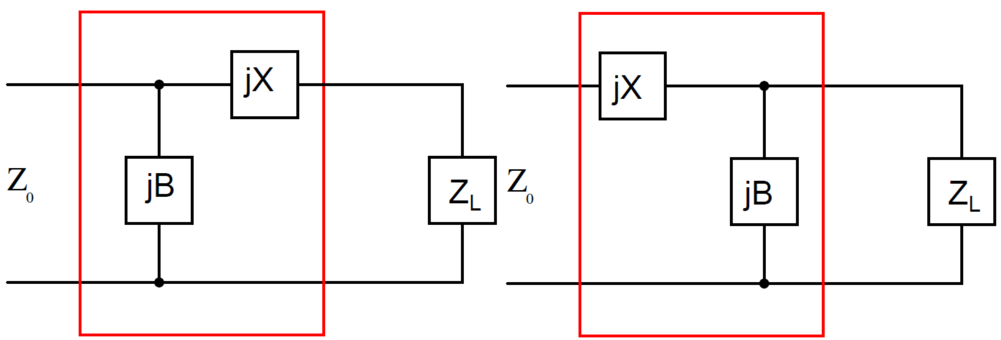


Figure 2-4: L-type matching networks. (a)Network for Z_L inside the 1+jx circle. (b)Network for $Z_L$outside the 1+jx circle

L-type matching network consist of two passive elements. Unfortunately, it can only work properly at low frequencies. Furthermore, it cannot be used for all possible load impedances. As shown on the Smith chart, the impedances cannot be matched to the source impedance in all cases. The region that cannot be matched is called as forbidden region for the matching network. Figure 2-5 shows four different configurations of two element LC impedance matching networks. Figure 2-6 shows the forbidden regions of these two element LC impedance matching networks.

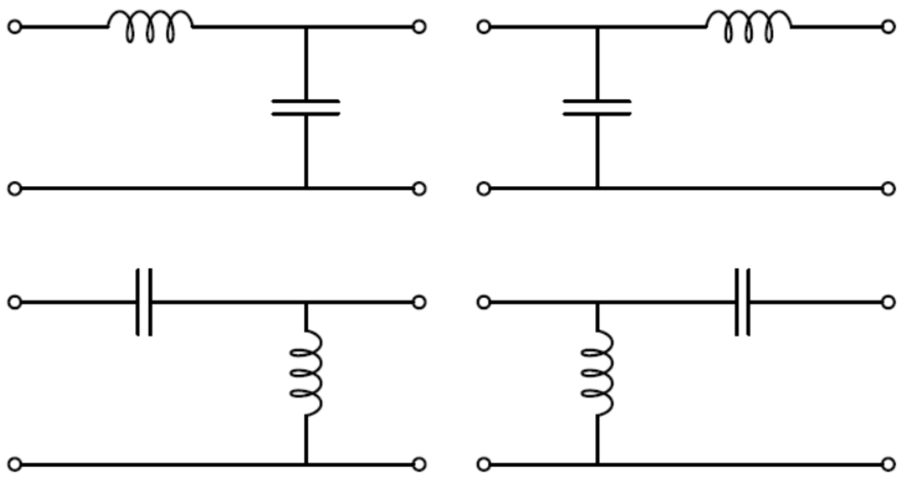


Figure 2-5: Two element LC impedance matchings

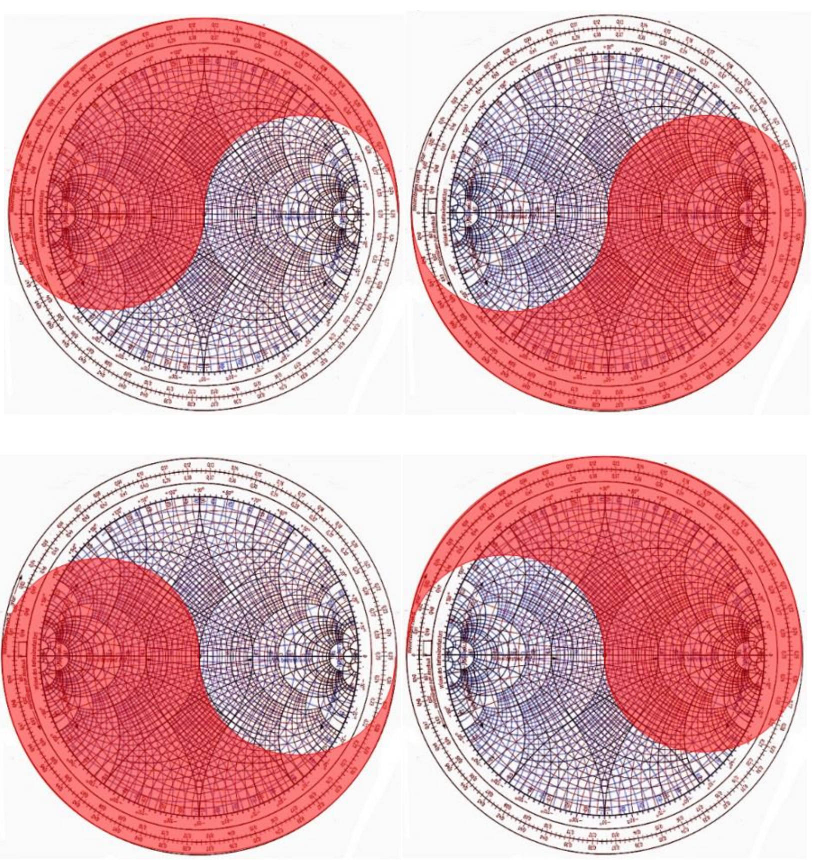


Figure 2-6: Forbidden regions of two element LC impedance matching

Pi-type and T-type matching network are adding one more lumped element to the L-type matching network, providing more flexibility and larger coverage on Smith chart.

To increase the tuning frequency range and to maximize the matched area across the Smith chart, the tunable matching network is chosen as a Pi-type network or modified Pi configuration [11] as shown in Figure 2-7.

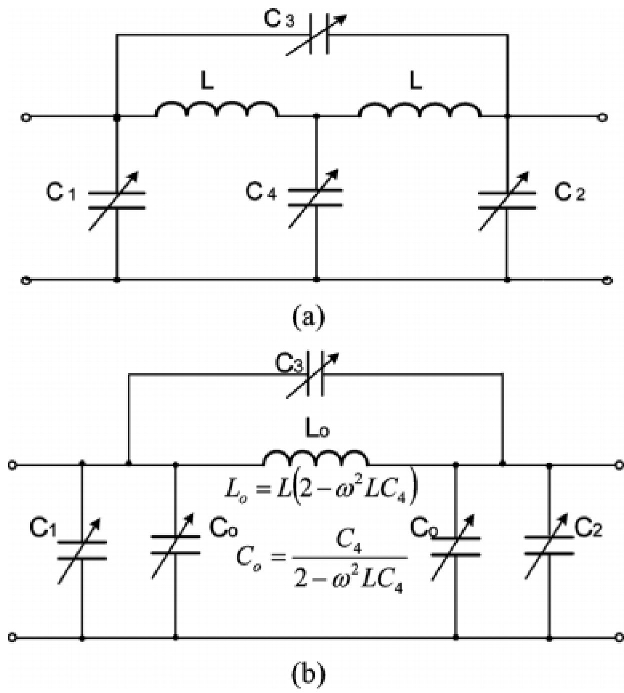


Figure 2-7: (a) Capacitor bridged double Pi-type network. (b) Its Pi network equivalence. [11] ©2013 IEEE.

To further expand the coverage, 8 tri-state RF-MEMS switches can be employed. Domingue., et al. proposed the design of impedance matching network consists of 8 tri-state RF-MEMS switches producing 6561 impedance states [12]. The tri-state MEMS switches present three different capacitance values. With one beam actuated, it has the first state and with two beams actuated, it has the second state. The third state corresponds the situation when no beam is actuated (Figure 2-8). Three different values are available for a larger band of the frequency range of operation. The measured results demonstrate wide coverage of the Smith chart between 5 GHz to 20 GHz,

realizing improved impedance coverage over a wide frequency range. However, it also has difficulty to work at low frequencies.

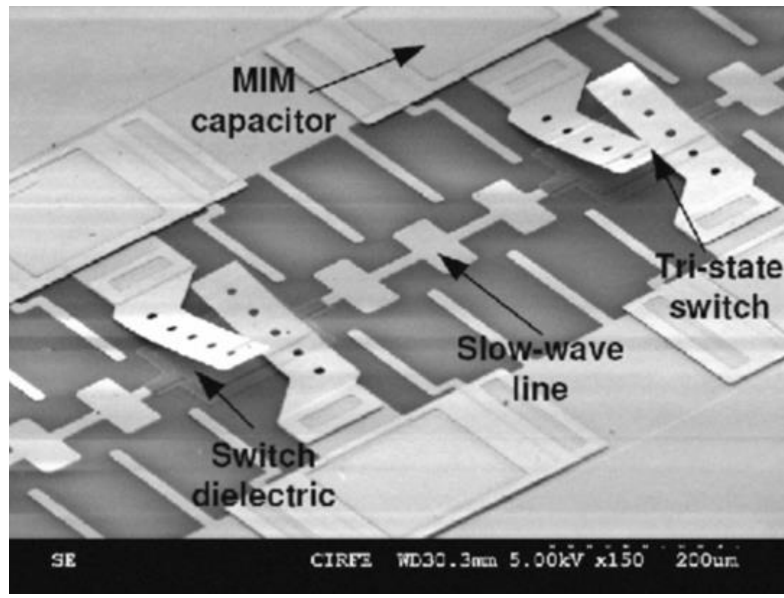


Figure 2-8: SEM picture of the fabricated MIM capacitor. [12] ©2010 IEEE.

2.2. Tunable Impedance Matching Networks

Building tunable inductors is a challenge, especially for integrated systems. The inductive behavior can be simulated using an active circuit. The basic principle is designing an active gyrator based on transistors. The current at one port is converted to a voltage at the other port, or vice versa. This converts the transistor's intrinsic capacitance C_{gs} into inductance.

A gyrator-C active inductor consists of two back-to-back connected transconductors [13]. As seen in Figure 2-9, M2 converts the input voltage into current to charge M1's gate-source capacitance C_{gs1}, while M1 converts the voltage of C_{gs1} into the input current. The equivalent circuit is shown in Figure 2-10. L is the equivalent inductance, r_L is the series resistance, R is the parallel resistance and C is the shunt capacitance.

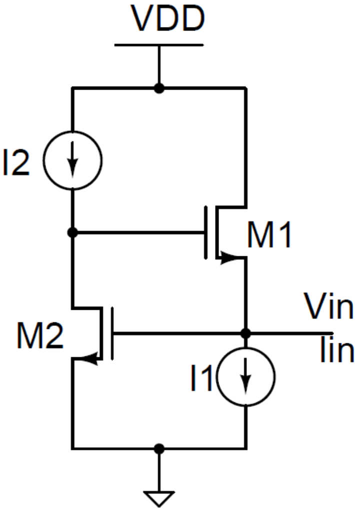


Figure 2-9: The diagram of active inductor

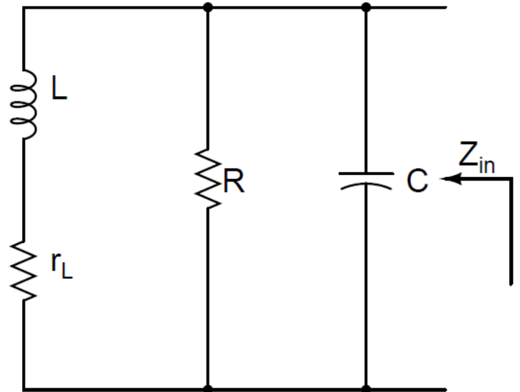


Figure 2-10: Equivalent circuit of active inductor

However, higher noise, nonlinearity, and power consumption are the major disadvantages of active inductors due to the fact that these circuits are realized using active devices which have higher noise [14].

Varactors are also used in tuning circuits. They are diodes that exhibit the characteristics of variable capacitors. A depletion region forms instantaneously across a PN junction, which is called dynamic equilibrium. However, this depletion region can be expanded and contracted by the voltage applied to the varactor.

The depletion region in the situation of reverse-biasing can form a parallel capacitor consisting of a layer of dielectric and two plates. The gap between the plates can be controlled by varying the reverse-bias voltage applied to the varactor. If the reverse-bias voltage increases, the width of the gap increases and the capacitance of the PN junction decreases. Both the forward biasing and reverse biasing are shown in Figure 2-11. The capacitance of the varactor is inversely proportional to the applied reverse bias. Figure 2-12 shows the circuit symbol of the varactor diode. However, the varactors have low electron emission efficiency in the PN junction. Normally they have large device areas and large connection resistances.

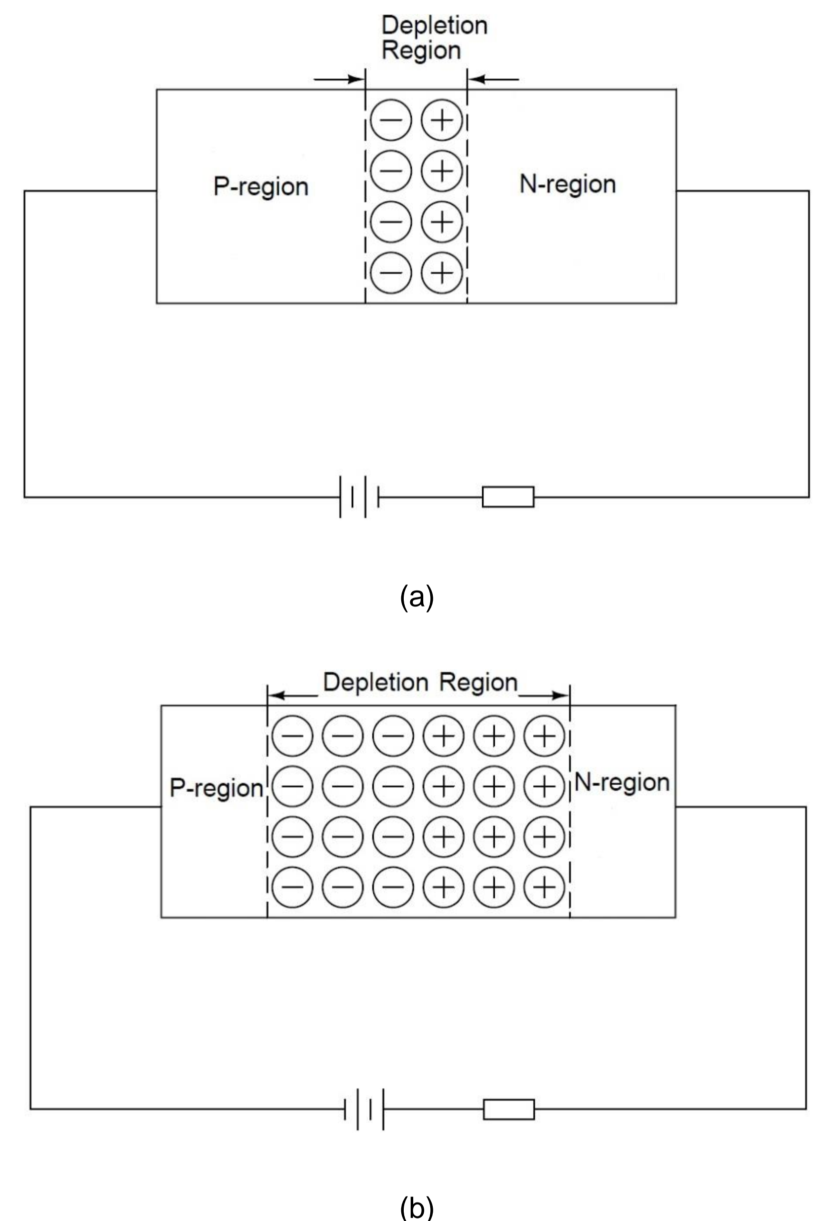


Figure 2-11: PN junction under (a) forward bias and (b) reverse bias

Figure 2-12: Varactor diode circuit symbol

MEMS devices have the advantages of small size, light weight, low power consumption, good durability, low cost and stable performance.

2.2.1. Tunable Micromachined Inductors

Inductance is a property of conductors. According to Lenz's law, the direction of induced current due to changes in magnetic flux generated in a magnetic flux is always such that it will oppose the change which produced it. When current in a closed loop changes, an electromotive force is induced to resist the change. If this happens in a self-loop, this inductance is called self-inductance, which is one of the properties of the closed loop. If this inductance creates an electromotive force in another inductor, this inductance is called mutual inductance. The relation between electromotive force and inductance can be expressed as equation (1-3).

$$\varepsilon mf = -L\frac{di}{dt} \tag{1-3}$$

where εmf is the electromotive force in volts, L is the inductance expressed in Henries and abbreviated as H, i is current in Ampere and t is time in seconds.

An inductor is a circuit element which is devoted to achieving a particular inductance in the circuit. The inductance of an inductor defines the ability of an inductor to store the energy for a given amount of current flow. The inductance can be calculated from equation (1-4).

$$V = L\frac{di}{dt} \tag{1-4}$$

where V is the induced voltage across the inductor in volts, i is the current flowing through the inductor and L is the inductance value of the inductor.

The properties of inductors depend upon a magnetic flux that exists mainly within the flux-guiding material [15]. In order to get tunable inductor, moving conductive membrane can be used above fixed inductor. When AC signal is applied to an inductor, it will induce an eddy current in the conductive membrane. According to Lenz's Law, the induced current produces magnetic fields which tend to oppose the change in magnetic field which produced it. The induced field thus decreases the intensity of the whole magnetic field and, therefore, decreases the inductance.

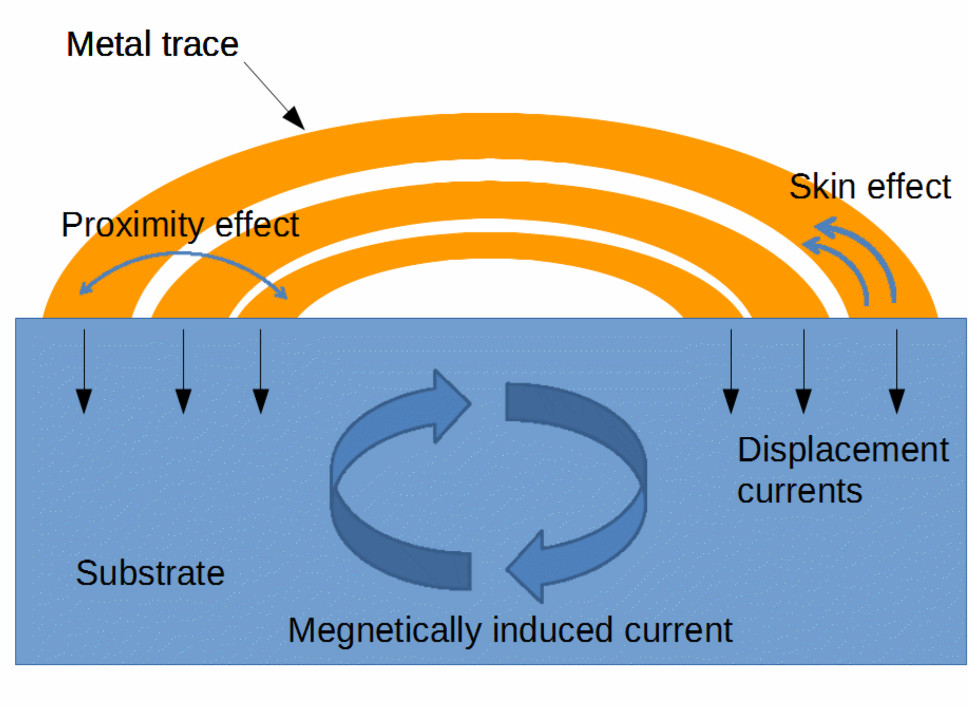


Figure 2-13: Energy dissipation phenomena of inductive devices on a lossy substrate

Based on this concept, tunable inductors can be realized by placing a conductive membrane above the inductors. By changing the gap between the membrane and the inductors, the inductances will also be altered.

Other techniques to modify the inductance have been proposed. For example, [16] and [17] used the conductive liquid shorten the metal coil, leading variation of inductance value. Although the variation ratio of the inductance and quality factor are high, the fabrication process was complex (Figure 2-14). The leaking problem of the fluid was also a major issue.

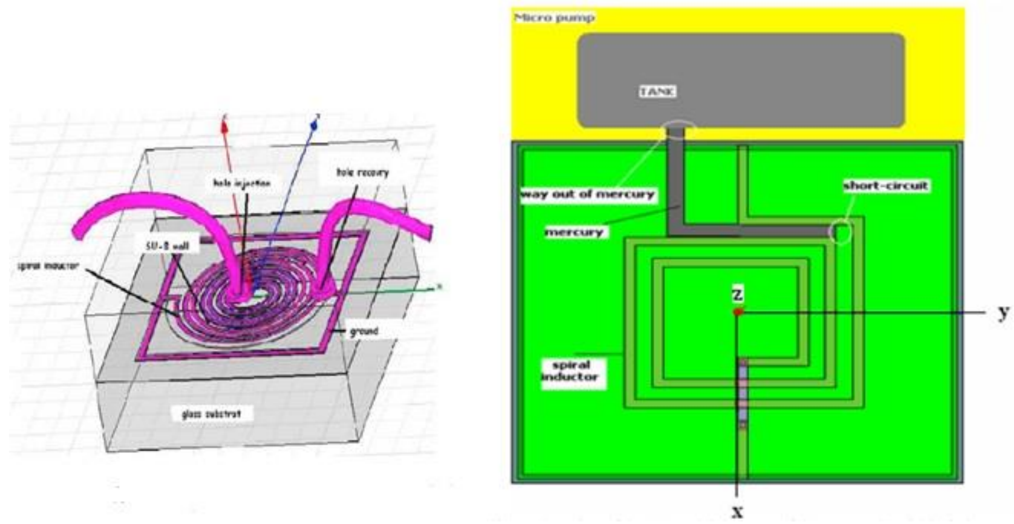


Figure 2-14: Top view of the 3D model structure of the proposed variable inductor. [16] ©2010 IEEE.

If the inductor consists of coils and a core, the inductance can be altered by changing the permeability of the core [18]. It shows the principle of piezomagnetic actuated tunable inductor. The permeability of the core can be changed with the voltage based on magnetoelastic interactions. The model was presented; however, the device was not fabricated due to the complex MEMS technology.

The inductance can also be changed by moving the core in or out of the coil. In [19], the solenoid inductor was electroplated copper. A nanomagnetic composite material was used as the core. The system was assembled by a 5 degree-of-freedom automated motion control platform using hybrid MEMS assembly technology and a

design library of silicon microgrippers, sockets, and handles. As seen in Figure 2-15, the whole process was complicated.

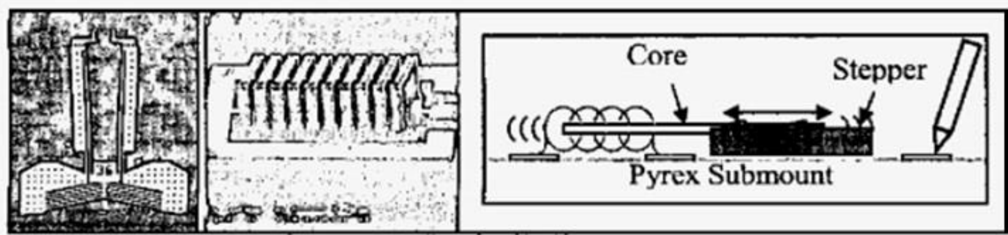


Figure 2-15: Copper electroplated solenoid variable inductor with silicon stepper. [19] ©2005 IEEE.

By controlling the magnet flux at the air gap, the inductance can be altered [20]. Figure 2-16 present three different configurations of the magnetic core.

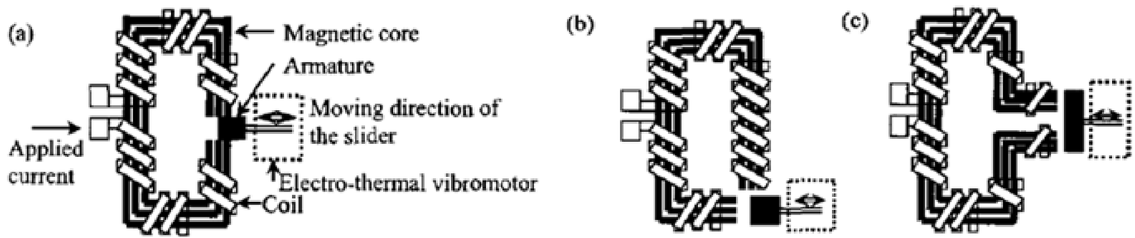


Figure 2-16: Tuning schemes based on different configuration of the magnetic core. (a) C-shape; (b) Q-shape; (c) a-shape. [20] ©2004 IEEE.

The inductance can also be altered by changing the gap of the two circuit in order control the magnetic coupling coefficient [21] [22] and by moving the magnet to shield the magnetic flux [23] [24].

2.2.2. Tunable Micromachined Capacitors

The basic function of a capacitor is as a storage element for electric energy. The terminal behavior of an ideal capacitor is given by

$$I = C\frac{dv}{dt} \tag{1-5}$$

where I is the current flowing into the capacitor in the direction of the voltage drop across the capacitor, t is the time and C is the capacitance value of the capacitor expressed in Farads and abbreviated as F [25].

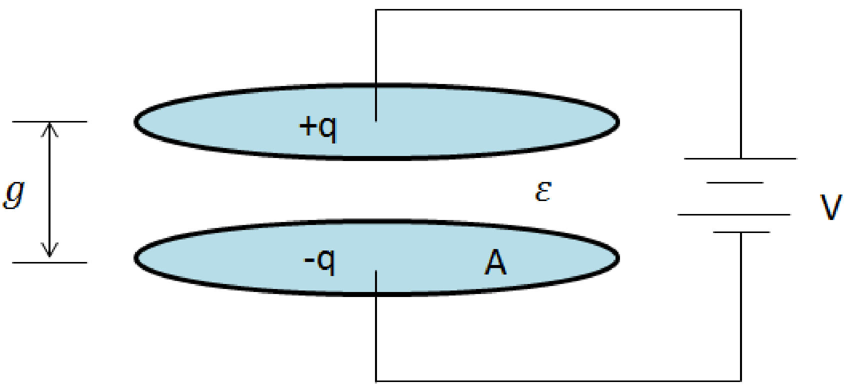


Figure 2-17: Schematic of a parallel capacitor

Figure 2-17 shows the geometry of a parallel-capacitor. It consists of two conductive plates separating by a dielectric which is characterized by permittivity ε. The capacitance can be express as:

$$C = \varepsilon\varepsilon_0 \frac{A}{d} \tag{1-6}$$

where C is the capacitance, ε is the relative permittivity of the material between the two plates, ε_0 is the permittivity of free space, A is the overlapping area of the two plates and d is the distance between two plates. The capacitance can change when the distance changes. Thus tunable capacitor can be realized by changing the distance between two plates. If the distance is reduced, the capacitance will increase.

When a voltage is applied to the movable electrode and fixed electrode, the movable plate will move towards to the fixed electrode with the increase of the voltage. The system will be in a critical balance status, where the mechanical force is equal to the electrical force (Figure 2-18).

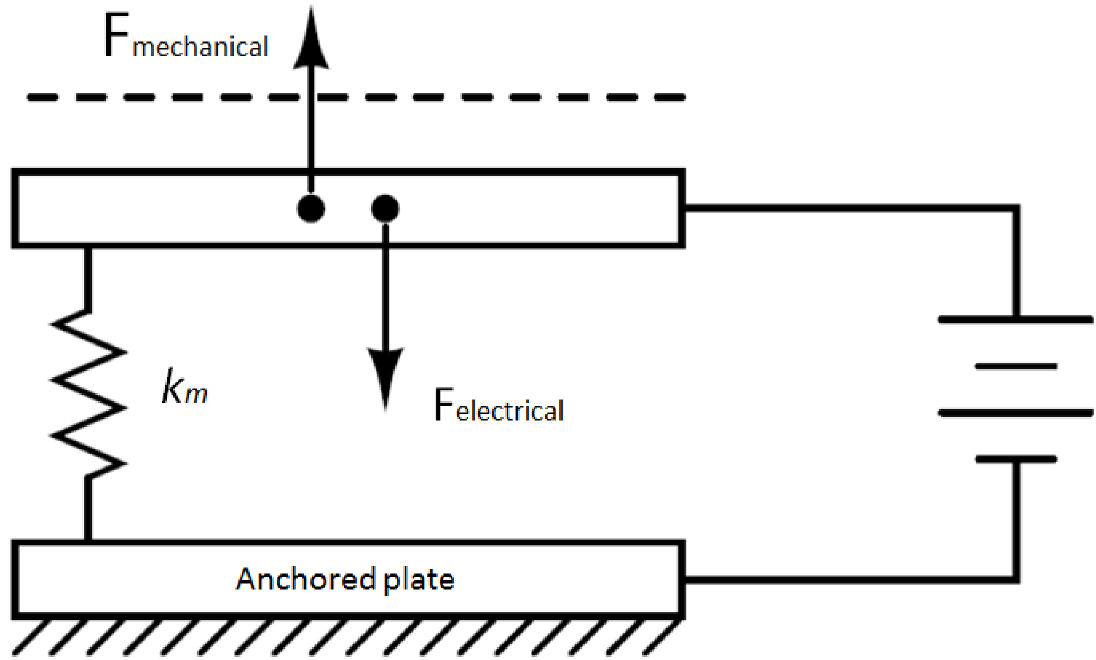


Figure 2-18: Schematic of mechanical and electrical force on the movable electrode

If the voltage continues to increase, due to the system's nonlinear status, the plates snap together once the gap decreases by about one third. This phenomenon is called "pull-in" which can be employed to design capacitive switches. They are switch devices that can open and/or close an electrical circuit at a rapid speed. In some situations, "pull-in" may damage the mechanism or cause burn-out due to contact under high applied voltage and should be avoided.

The equilibrium position is called "pull-in position", which is at one-third of the gap [26]. The applied voltage at equilibrium position is called "pull-in voltage". The electrostatic devices should be designed or operated at the voltage below the "pull-in" voltage.

Compared to digitally controlled MEMS capacitive switches, MEMS varactors have the advantage of continuous capacitance tuning. [27] demonstrated continuously tunable capacitor with a tuning ratio up to 17 using a dual-gap relay-type design. This

design overcomes the limitation of pull-in effect. It can be seen in Figure 2-19 that at the edges of the structure special humps are designed to avoid pull-in.

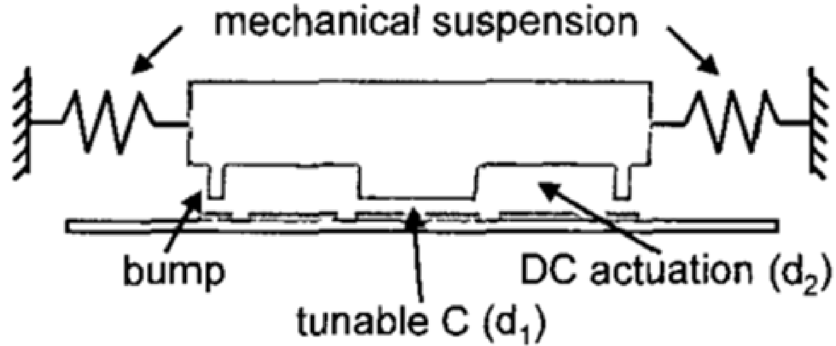


Figure 2-19: Schematic view of a dual-gap relay-type tunable capacitor. [27] ©2004 IEEE.

Another varactor with two gaps was shown in [28] and the structure was shown in Figure 2-20.

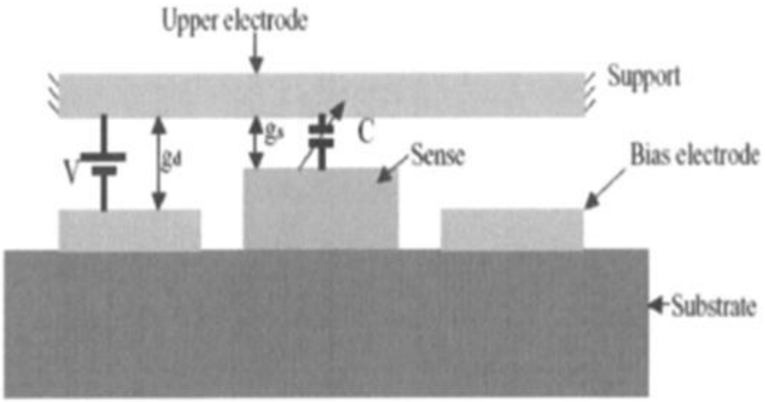


Figure 2-20: Two gap tunable capacitor structure. [28] ©2008 IEEE.

In [29] the integrated variable MEMS capacitors have a tuning range of 17% with a quality factor exceeding 20. The fabrication process can be compatible with CMOS (Complementary metal–oxide–semiconductor) process. However, the control of the MEMS capacitance is often not fully predictable due to its high susceptibility to the stresses of beam materials.

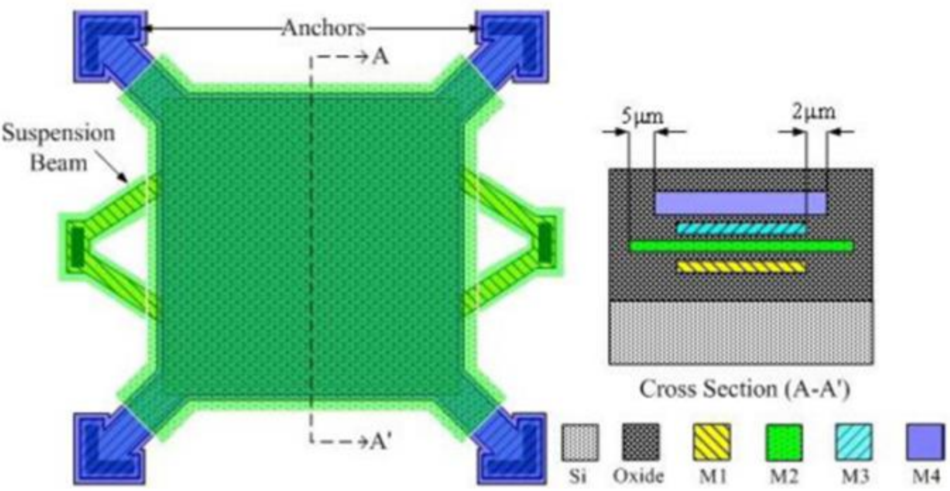


Figure 2-21: Layout and cross-sectional view of the parallel-plate MEMS tuning elements. [29] ©2007 IEEE.

In [30], a tunable capacitor with tri-state structure was introduced. The tuning range is 460% at 1 GHz. However, the fabrication process is relatively complex and expensive compared to the conventional digital capacitors.

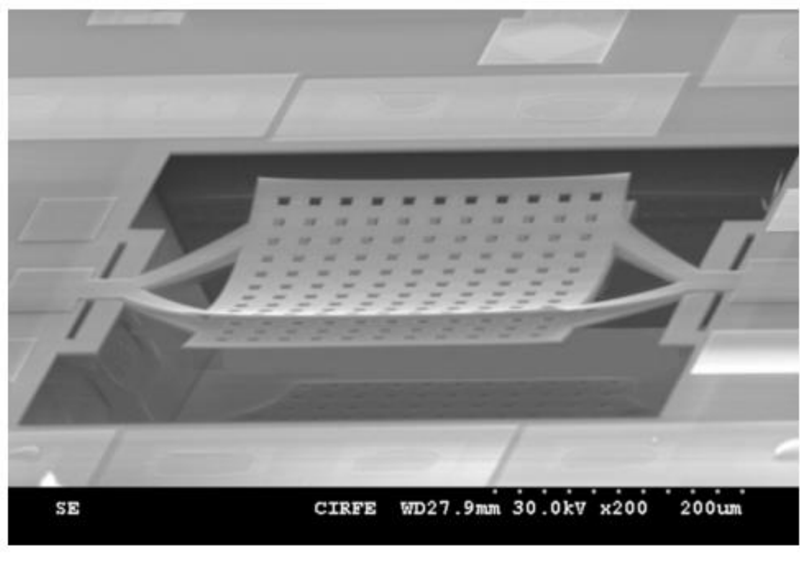


Figure 2-22: A tunable capacitor with tri-state structure. [30] ©2008 IEEE.

Another tri-state structure was realized based on a toggle push-pull mechanism [31]. When biasing the pull-out electrodes, the central part of the bridge raises up and the up-state capacitance is reduced. The capacitance is the smallest at ON-State. When a voltage is applied to pull-in area, the central part of the beam is pulled down thus increasing the bridge capacitance (Figure 2-23). A tuning ratio of 2.5 has been obtained.

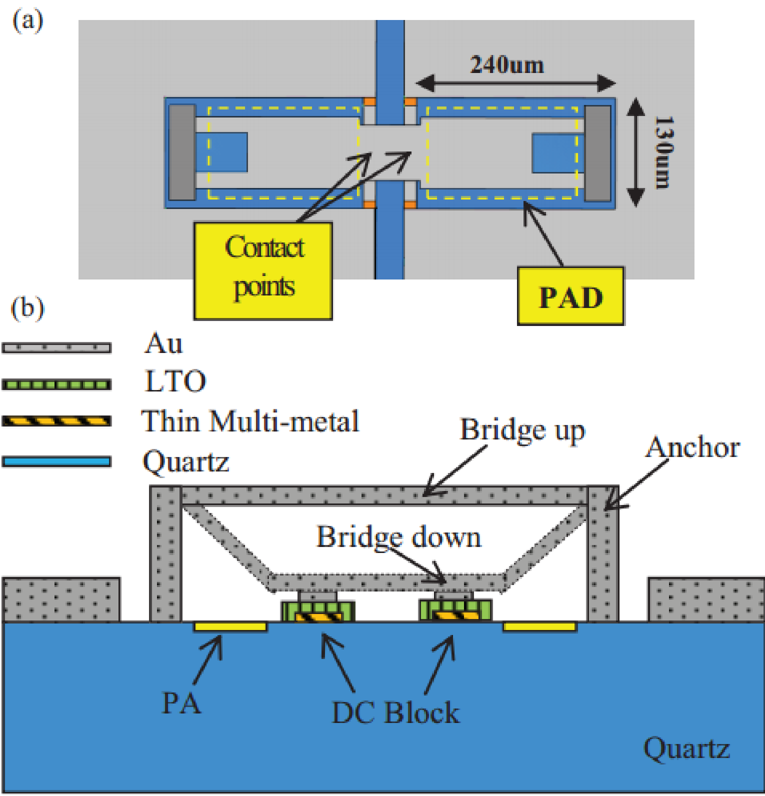


Figure 2-23: (a) Air-bridge shunt ohmic switch top view; (b)Tunable capacitor with a tri-state structure based on a toggle push-pull mechanism. [31] ©2009 IEEE.

In order to convert energy into the power output, the mechanism should realize mechanical moving like rotation, deflection and so on. These operations are performed by driving the actuator. In MEMS, piezoelectric actuator, magnetostatic actuator, thermal Actuator and electrostatic actuator are widely used.

Piezoelectric ceramic is a type of material that will produce mechanical deflection when applied voltage [32]. On the other hand, when vibrating the piezoelectric ceramic,

it will produce electric charges. Using this principle, piezoelectric bimorph can be formed as a cantilever that consists of two active layers: two piezoelectric ceramics or a piezoelectric ceramic and a metal sheet. The electric field causes one layer to extend and the other layer to contract, producing a displacement (Figure 2-24). The advantages of piezoelectric bimorph include large displacement and high efficiency. However, it has high power consumption and is hard to integrate in MEMS.

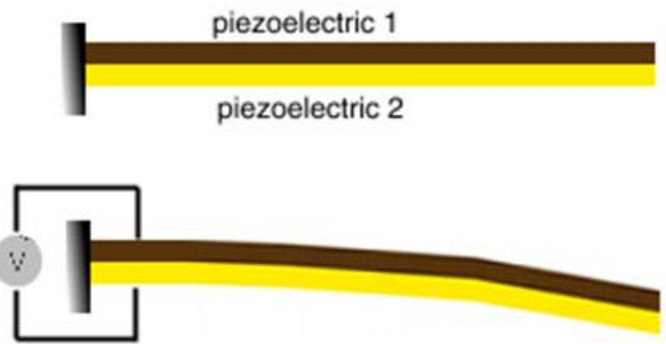


Figure 2-24: Schematic of the piezoelectric bimorph actuator. [32] ©2010 IEEE.

Thermal actuators generate displacement by amplifying thermal expansion. It also has two layers. One layer is heated more than the other and expands more, or the two layers have different thermal expansion coefficients, which mean they have a different change in volume in response to the same change in temperature. This imbalance creates motion [33]. A small amount of thermal expansion of one part of the device translates to a large amount of deflection of the overall device (Figure 2-25). The operating voltage of thermal actuator is low, so it is convenient to be used in the Standard integrated circuit voltage working environment. However, thermal actuator has low efficiency and slow response. Its operating frequency is low and is hard to be precisely controlled.

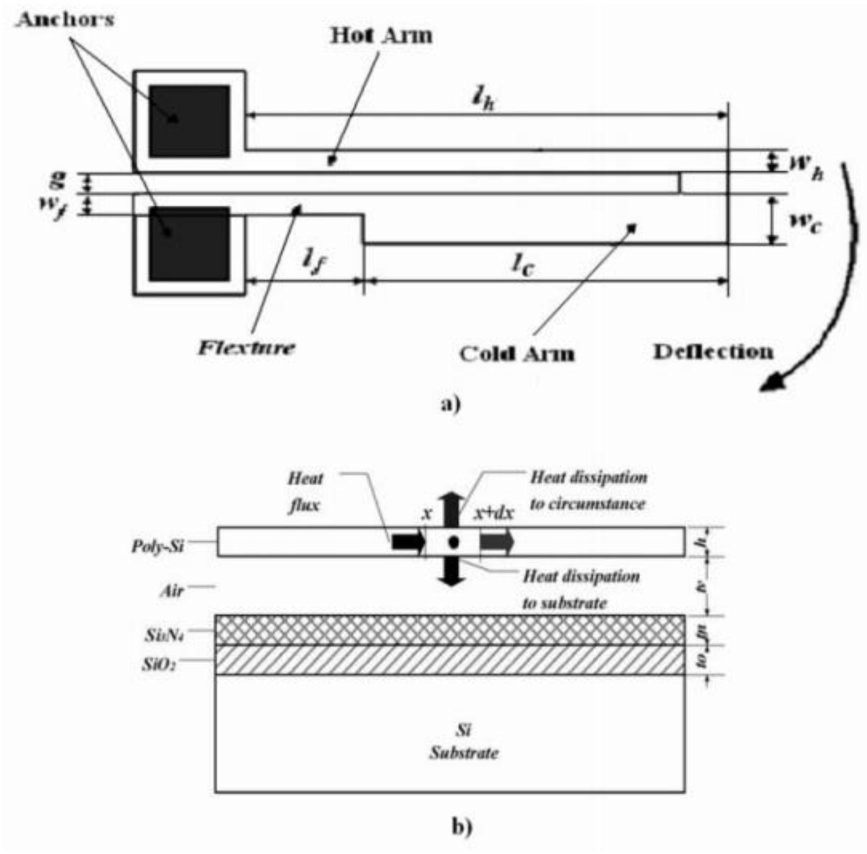


Figure 2-25: Schematic of the electro-thermal microactuator. [33] ©2014 IEEE.

A magnetostatic actuator is a device that applies force or torque onto the operator by a magnetic field. One method of the magnetostatic actuator is applying current through the coils. The current produce a magnetic field to move the magnet. Another method is applying a magnetic field to move the movable magnet with high permeability [34][33]. The magnetostatic actuator can be divided into two types: the movement of the active plate is perpendicular to the stationary plate or parallel to the stationary plate (Figure 2-26). For good performance, the core and movable part should have high magnetic permeability and good mechanical properties. In most of the situation, the structure should be used as part of the structure of the magnetic path. The integration and fabrication are relatively hard.

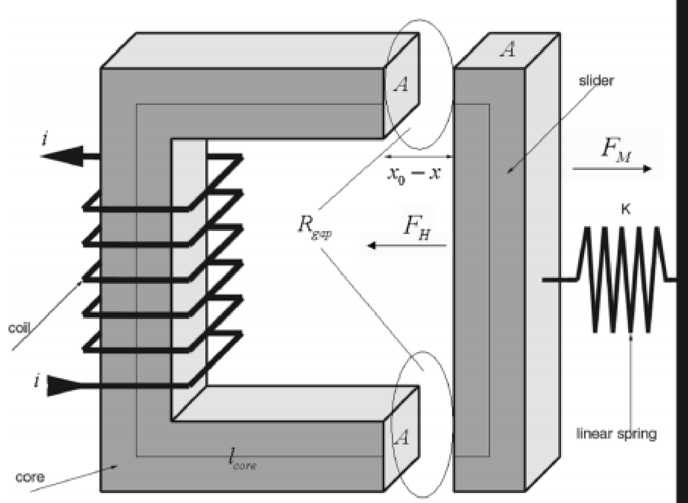


Figure 2-26: Schematic of the magnetostatic actuator. [34] ©2005 IEEE.

Electrostatic actuators use the force of electrostatic energy to move objects. In two mechanical elements, one that is stationary and the other one is movable. When two different voltages applied to them, which creates an electric field, the induced electrostatic force moves the movable part. Electrostatic actuators have the advantages of simple implementation, high operating frequency, and low power consumption.

Chapter 3. Fabrication

This thesis provides a method to fabricate the passive device based on polymer SU-8 as the structural layer. In order to obtain the tunable capacitor, the gap between two electrodes should be tunable. The proposed idea is that building the structural layer by SU-8 to create the gap. One electrode of the capacitor was made of metal deposited on the glass wafer. The metal was then patterned according to the design parameters. Polymer SU-8 was spun and patterned to ensure the gap between two electrodes. The thickness of SU-8 equals the gap between the electrodes. Finally, a polyimide membrane was bonded on SU-8. Several methods were provided and discussed.

This section of the thesis will present the following fabrication steps: wafer cleaning, sputtering, photolithography, and cross-linking the SU-8.

3.1. Device Plan View and Cross Section

The device fabrication begins with depositing a layer of metal on the wafer to form the fixed electrode. The metal layer is patterned to desired shapes. Then one layer of SU-8 is spun and patterned as the structural layer, which ensures the gap between two electrodes. The membrane is placed on top of the SU-8. It is flexible and conductive and employed as the movable electrode. Figure 3-1 shows the plan view and cross-sectional view of the proposed tunable capacitor.

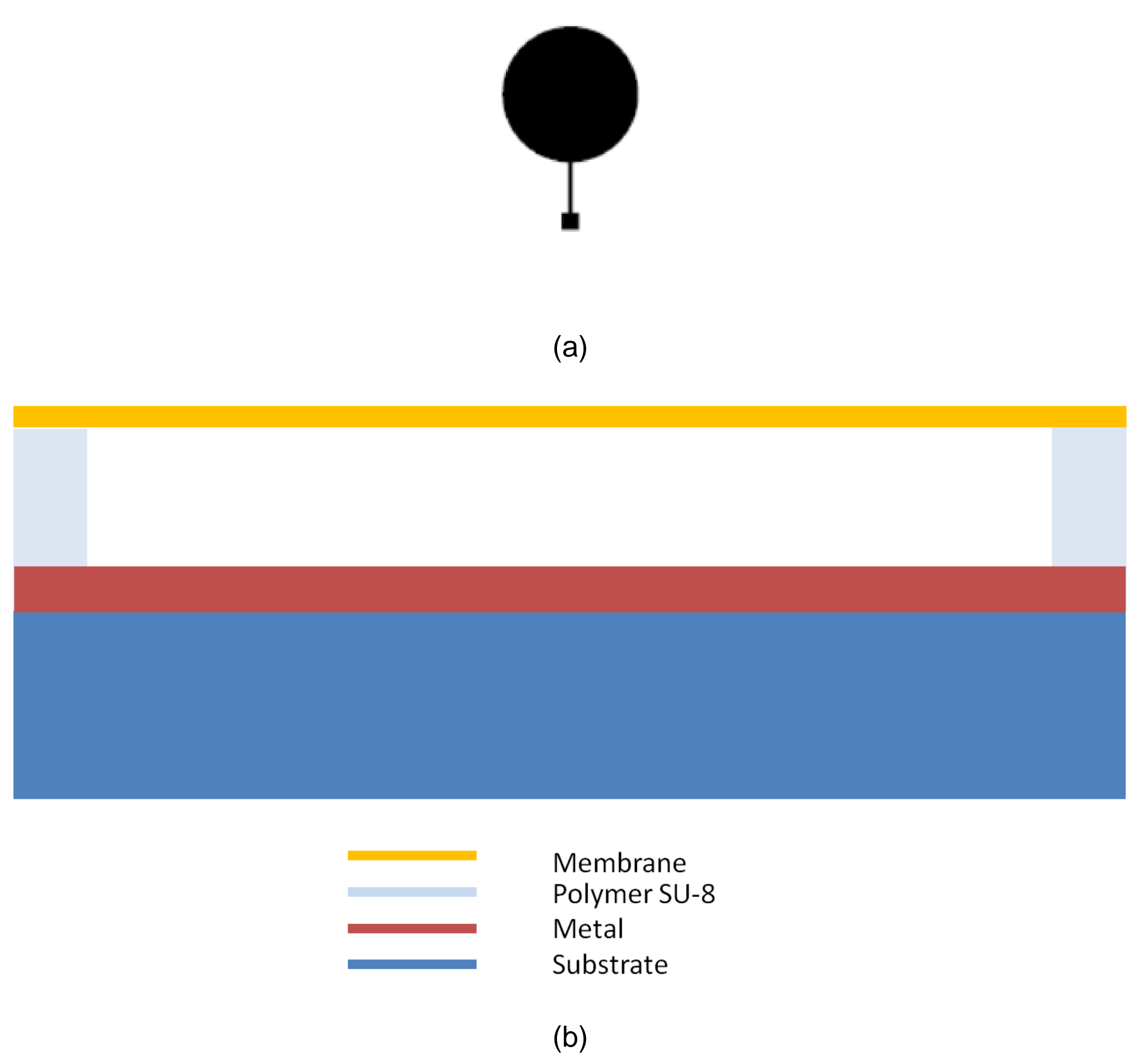
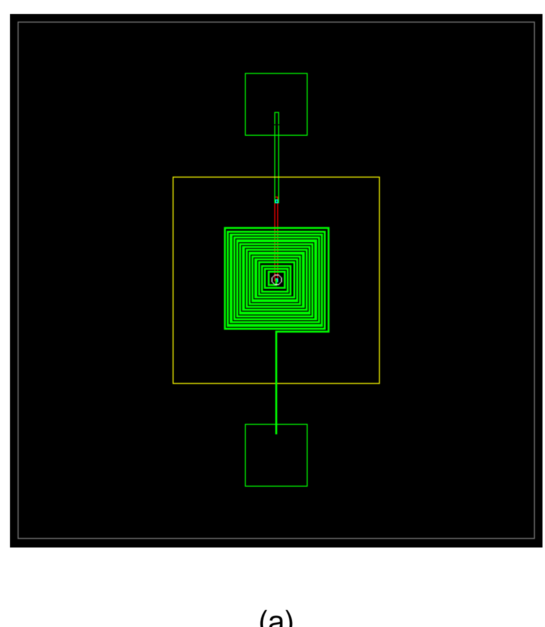


Figure 3-1: The proposed tunable capacitor: (a) plan view and (b) cross-section.

In order to pattern a spiral inductor on the wafer, a second metal layer should be deposited. Based on the process of fabricating tunable capacitors, a layer of insulator was deposited to separate the two metal layers. Vias were etched from the insulating layer, ensuring the connection between the metal layers. Then the second metal layer was deposited and patterned. Figure 3-2 shows the plan view and cross-sectional view of the proposed tunable inductor.



(a)

(b)

Figure 3-2: The proposed tunable inductor: (a) plan view and (b) cross-section.

3.2. Proposed Fabrication Process

3.2.1. RCA Clean

In the manufacturing process of micro-devices, the cleaning technology of wafers has an impact on the wafer process yield, component quality and reliability. With the increasingly complicated process technology and high level of integration, clean wafer surfaces are needed to make such sophisticated products. Therefore, cleaning technology is an important step in the manufacturing process. The standard cleaning process is known as RCA clean [35]. The main purpose of the RCA clean is to ensure that organic, ionic, and metallic contaminants are removed from the wafers. Typically it has three steps. Each step is designated to remove a particular class of contaminants. RCA1 aims to get rid of organic contaminants and metal. The HF Dip removes oxide formed during RCA1. Finally, RCA2 removes ionic contamination. Because glass slides are made of silicon dioxide, the step of removal of oxide layer was not chosen.

All these aqueous processing, including rinses, is performed with deionized water (DI waster). RCA1 was performed with a solution of 5 parts of DI water, 1 part (500ml) of aqueous ammonium hydroxide and 1 part of aqueous hydrogen peroxide for 10 minutes at the temperature of 75~85°C. RCA2 was performed with a solution of 5 parts of deionized water, 1 part of aqueous hydrochloric acid and 1 part of aqueous hydrogen peroxide. After dipping for enough time, the slides were rinsed in DI water for at least 3 minutes and then blown dry [36].

Table 3-1: The RCA cleaning process

Process step	Purpose	Details
RCA-1	Removed organics and metals	500ml NH_4OH (29%) 500ml H_2O_2 (30%) 2.7 l DI water 15 min at 70°C
HF Dip	Removes oxide formed during RCA-1	5 l DI water 100 ml HF (49%) 30 s
RCA-2	Removes alkali ions and cations	500ml HCl (29%) 500ml H_2O_2 (30%) 2.7 l DI water 15 min at 70°C

3.2.2. Sputtering

Metallization can be realized by Physical Vapor Deposition (PVD), which is a collective set of processes used to deposit thin layers of material, typically in the range of few nanometers to several micrometers. PVD include evaporation and sputtering. In the evaporation process, the target materials are contained in a crucible. A beam of electrons is generated, accelerated and directed towards the crucible. Part of the target material melts and the material evaporates [37]. Joule heating can also be used for this purpose.

Meanwhile, sputtering is a process whereby atoms are ejected from a solid target material due to bombardment of the target by energetic particles [38]. These particles “knock” metal atoms out of a “target”. The energetic atoms deposit on a wafer located near the target. It only happens when the kinetic energy of the incoming particles is much higher than conventional thermal energies. Due to better step coverage and less radiation damage, sputtering is chosen in many applications over evaporation. In this step, sputtering machine from Corona Vacuum Coaters (Figure 3-3) was used to sputter chrome and gold on the slides.

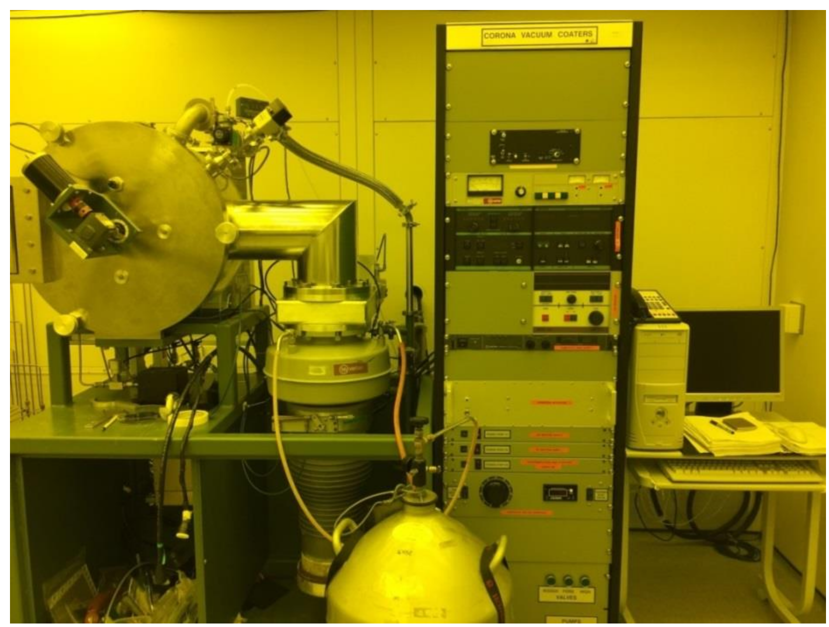


Figure 3-3: Corona Vacuum Coaters for sputtering

The slides were prepared by RCA1 and RCA2 cleaning and blown dry. Corona Vacuum Coaters was used to sputter the metals. Firstly the slides were loaded on the substrate holders (Figure 3-4). Secondly, the pressure was decreased to 1e-5 mTorr. Thirdly, the DC substrate bias and sputter current was set according to the metal material. For chrome, the DC substrate bias was 70 V and the sputter current was 250 mA. For gold, the DC substrate bias was 70 V and the sputter current was 190 mA. Fourthly, the required time was calculated, using the desired thickness divided by the sputter rate. After sputtering for such time, the metal layer can be formed on the slides. Then the setup can be changed and DC voltage can be applied to the next target. The second layer of metal can be sputtered. In this experiment, the thickness of chrome was 50 nm to make sure of the adhesion between glass and the gold. The thickness of gold was 200 nm to form the electrode.

Figure 3-4: The holder inside Corona Vacuum Coaters

One key point here is the pressure. Since the pressure should be as low as 1e-5 mTorr, it is lowered to 50 mTorr by rough valve. Then it is lowered to 1e-5 mTorr by high valve. The pressure was so low that materials which cannot meet the low outgassing criteria should not be put in the chamber.

3.2.3. Photolithography

Photolithographic technology is the foundation of fabricating semiconductor MOS tube and circuits on a silicon wafer. It is a technique which uses of ultraviolet light to transfer the geometric pattern to form a photomask to a light-sensitive chemical "photoresist" and finally to a thin film or the bulk of a substrate.

Photolithographic technology has two main steps including photocopying and etching process. The wafer is initially heated to drive off the moisture on the wafer surface. It then placed in the vacuum spinning system. A layer of liquid “adhesion promoter” is applied onto the wafer to promote the adhesion of the photoresist to the wafer. Photoresist is a kind of polymer which is sensitive to light typically with a wavelength of 2000 to 4500 angstroms.

Photoresists are divided into two categories. Positive photoresist is partially degraded by light and can be dissolved by the reaction of the developer. The non-exposed portion is consistent to the pattern of the mask. Positive photoresist has a high

resolution, large exposure margin, low pinhole density and non-toxic, etc., which make it suitable for the production of highly integrated devices. On the other hand, negative photoresist produces insoluble material after exposure to light by crosslinking reaction. The unexposed portion is dissolved by the developing solution. The obtained pattern is complementary to the pattern of the mask. Negative photoresist has high adhesion, high sensitivity and is suitable for production of low-integration devices.

The photo mask is produced in the form of an array of images using a step-and-repeat camera. It can be emulsion of chrome on glass for semiconductor circuits, or emulsion on transparent plastic for thin-film applications [39].

After exposure, the wafer will go through the etching process. By the use of chemical or physical methods, part of resist is removed from the surface of the wafer or dielectric layer, so as to obtain the desired pattern with a thin layer of a resist pattern on the wafer surface or the dielectric layer. Next the metal can be etched to the desired shape. After etching, the resist can be cleaned.

In the process, the slides were prebake in the oven at the temperate of 100°C for 20 minutes in order to get rid of the humidity. After they cooled down to room temperature, they were placed in the vacuum of spinning machine. 2~3 drops of S1838 from Shipley Microposit were applied onto the slides. The spinning speed was 4000 RPM and the duration time was 30 seconds. Then the slides were put on the hot plates for the soft bake. Softbake was importance to the process. After coating, the resist film contains a remaining solvent concentration. The softbake reduces the remaining solvent content in order to avoid mask contamination and as well as improve resist adhesion to the substrate. The slides can be softbaked at 100°C for 5 minutes or at 110°C for 1 minute.

After softbake, the slides were exposed to UV light for 7 seconds and developed in the MF319 developer from Microposit for 45 seconds. After rinsing in DI water over 3 minutes, the slides were hardbaked, harden the photoresist at 120°C for 20 minutes. At this point, the slides were ready to be etched. Gold etchant from Transene company was used to etch the top layer of gold. The time can be calculated according to the thickness of the gold layer. The etch rate was 28 Angstroms per second at 25°C. So the time was

around 70 seconds. Chromium etchant from Transene company was used to etch the chromium. The etch rate was 32 Angstroms per second at 40°C. So it's better to warm up the chromium etchant on the hotplate while etching. The time was around 15 seconds. Finally, the remaining photoresist can be striped by acetone.

In order to make the structural layer, SU-8 was used to form the gap. Different thicknesses can be obtained by spinning sorts of SU-8 at different speeds. For the thickness of 50 μm, both SU-8 3035 and SU-8 3050 can be chosen [40]. SU-8 3050 is thicker than SU-8 3035, therefore, it needs a higher spinning speed. The unevenness and imperfections increase with increasing spinning speed. Also, it is harder to etch the SU-8 3050. In this experiment, SU-8 3035 was used.

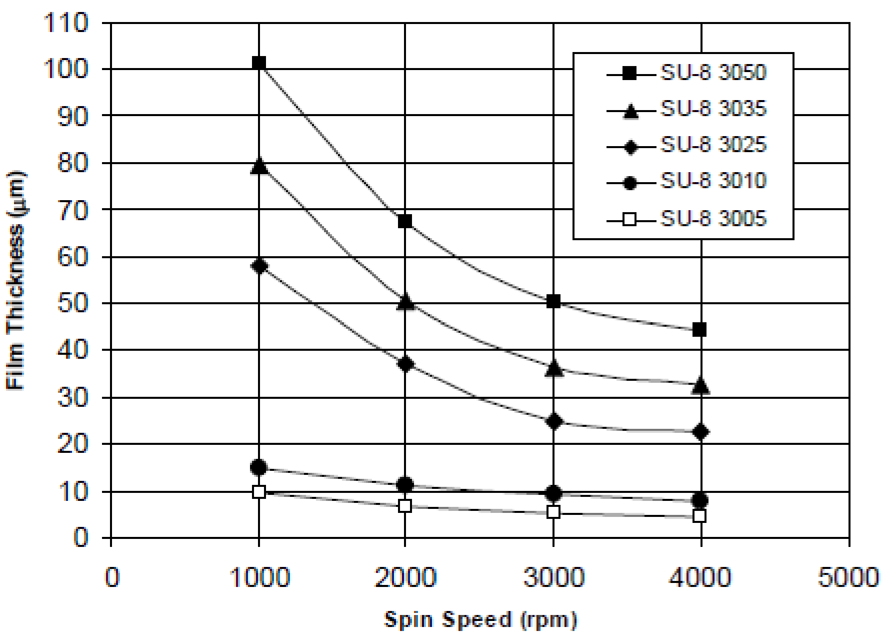


Figure 3-5: Spin speed vs. Thickness for SU-8 3000 resists [40]

The slides were spun with SU-8 3035 for 30 seconds. Because the viscosity of SU-8 3035 was up to 7400 cSt, the spin speed was from 0 to 2000 rpm gradually. Then the slides were placed on hot plates for 20 minutes. The temperature was controlled to increase from 25°C to 95°C at the speed of 450°C /hour. For the thickness of 50 μm, the exposure energy should be 150-250 mJ/cm^2 according to the data sheet. After setting up the illumination controller, we knew that the power was around 12 mJ*s/cm^2. The time can be calculated and 25 seconds was chosen.

Figure 3-6: The illumination controller and the parameters shown in the meters

Directly after exposure, the slides should be put onto the hot plate for post-exposure bake (PEB) for 4 minutes. The temperature of PEB was also 95°C. This step reduces mechanical stress formed during the soft bake and, therefore, improves resist adhesion and reduces underetching in subsequent wet chemical etching. For SU-8 3035, the thickness was relatively large, so the PEB was necessary. After PEB, the patterns can be shown in SU-8. No pattern means problems in the previous steps. The slides will be processed with MicroChem's SU-8 developer. During the developing, the fresh developer should be sprayed followed by a second spray of Isopropyl Alcohol (IPA) until the SU-8 was developed completely. Hard bake was performed to further cross-link the material.

The thickness of SU-8 was measured by Surftest SJ-400. The edge bead of SU-8 was in the range of 53.9~54.9 μm, and the inner thickness was in the range of 52.7~53.2 μm.

3.2.4. Fabrication of Conductive Membranes

In this section, methods of preparing the membrane were present. To start, three tried methods are listed and their associated challenges are explained. At last, the method used in the fabrication is provided.

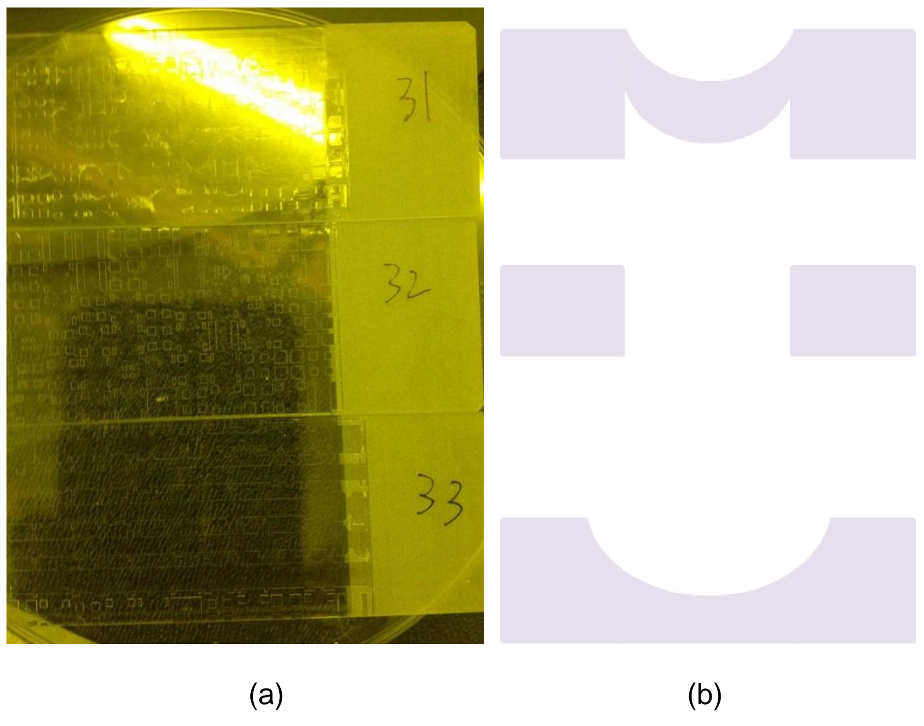
Double Exposure

Since the SU-8 is a negative photoresist. The light absorption of SU-8 at near UV (365nm - 400nm) is low. Also, the exposure amount obtained throughout the photoresist layer is relatively uniform, which assures structures with vertical side walls and a high aspect ratio. SU-8 also has good mechanical properties, chemical resistance, and thermal stability. It is not conductive and can be used as an insulator.

Two methods were tried. Some area of SU-8 can be first exposed to form the solid structure. Next step, the whole area of SU-8 is exposed at a shorter time, to form a thinner membrane at the top. The wafer was put on the hot plate for PEB. Finally, the unexposed SU-8 underneath the membrane can be dissolved and washed away. In the second method, the PEB was made after each exposure. The whole SU-8 was first exposed with a mask to form the solid structure. Next, the wafer was post exposure baked. Then it was second exposed for a shorter time and second post exposure baked. Finally, it was developed and rinsed.

Two masks were designed and fabricated. The first one is used to uncover the structural area. The second one is used to uncover the area of the membrane. The rest covered area was meant to be developed and form the channel of the developer to dissolve the unexposed SU-8 under the membrane.

However, SU-8 is gradually crosslinked by UV radiation. It is hard to tell the interface between the unexposed SU-8 and exposed SU-8. Besides, when developing the unexposed SU-8, the thin film is too thin to resist the rinsing water. When drying, it has a tendency to attach to the wafer because of the surface tension. Figure 3-7 shows three failure conditions of the wafers. The wafer with number 31 had the membrane easily damaged in the process of developing. If the time of second exposure is too short, a solid membrane is hardly formed. The top layer of SU-8 was developed. On the contrary, if the time of second exposure is too long, the unexposed SU-8 is hard to remove. They can be clearly seen in the wafer 32 and 33.



(a) (b)

Figure 3-7: Three conditions of the wafers: (a) image of the wafers and (b) schematic of the membranes

Corona Treating of Polyimide Films

Corona treatment uses high-frequency high voltage to discharge on the surface and produces low-temperature plasma. These ions penetrate into the surface by the shock and the destruction of the surface, thus oxidizing and polarizing the surface molecules, so as to increase surface adhesion.

In order to get good adhesion between the polyimide and SU-8, Corona treater was used to processing the surface of polyimide. However, the flatness of the surface was sacrificed in the process by the high voltage. Figure 3-8 shows the unevenness of the film. The gap between the two electrodes was changed and could not be used reliably. Furthermore, since the molecules on the surface were influenced easily by the corona treating, the surface was positively or negatively charged, impacting the test of capacitors.

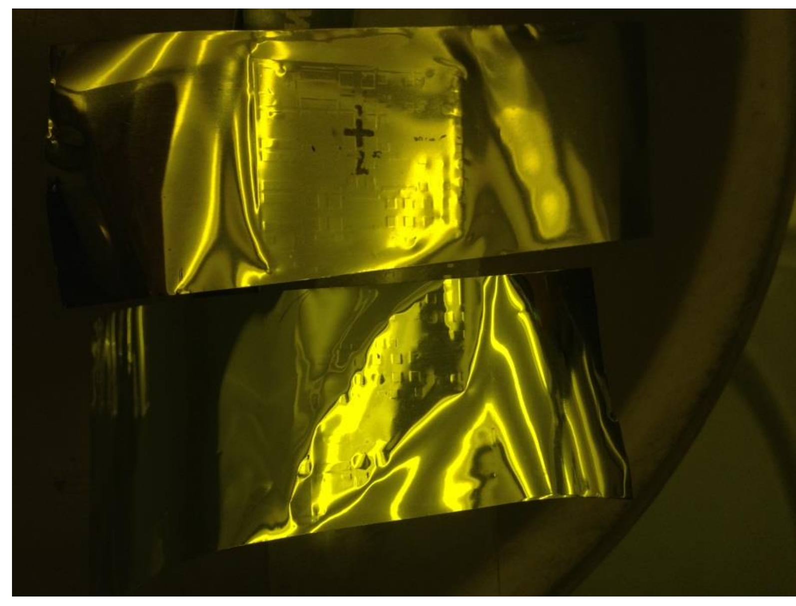


Figure 3-8: The unevenness of the film after Corona treatment

Metalized Polyimide

Polyimide with Aluminum layer on top was used to form the membrane. The thickness of polyimide was 25.4 μm (PIT1N-ALUM Series from Caplinq). The SU-8 3005 was diluted with SU-8 thinner in a ratio of 1:1. It was then mixed up by Ultrasonic Homogenizer (Figure 3-9). The pulse was 25s ON and 5s OFF per period. The time was 2 minutes each time. It was repeated for 3 times.

Figure 3-9: The photograph of Ultrasonic Homogenizer and spraying gun

The solution was then sprayed onto the film and was pressed against the solid SU-8 structure gently. The whole slide was then put into the oven for 30 minutes. The temperature was increased from 25°C to 150°C at the speed of 450°C/hr for curing. There is good adhesion between the film and SU-8 structure.

3.3. Fabrication Process

3.3.1. Fabrication Process for Capacitors

Figure 3-10 shows the steps and cross-sectional view of the proposed tunable capacitor. First, the bottom electrode was deposited on the wafer by sputtering and then patterned. Cr/Au was used as the bottom electrode, where Cr is the adhesive layer (50 nm) and Au is the actual layer for the electrode (200 nm). The metal layer was patterned, as shown in Figure 3-10 (c). Next, a 50 μm SU-8 was spin as the structural layer, as shown in Figure 3-10 (d). Photolithography for SU-8 was carried out to form the gap between the bottom electrode and the membrane, as shown in Figure 3-10 (e). In Figure 3-10 (f), a polyimide membrane was bonded on to SU-8 and formed the upper electrode.

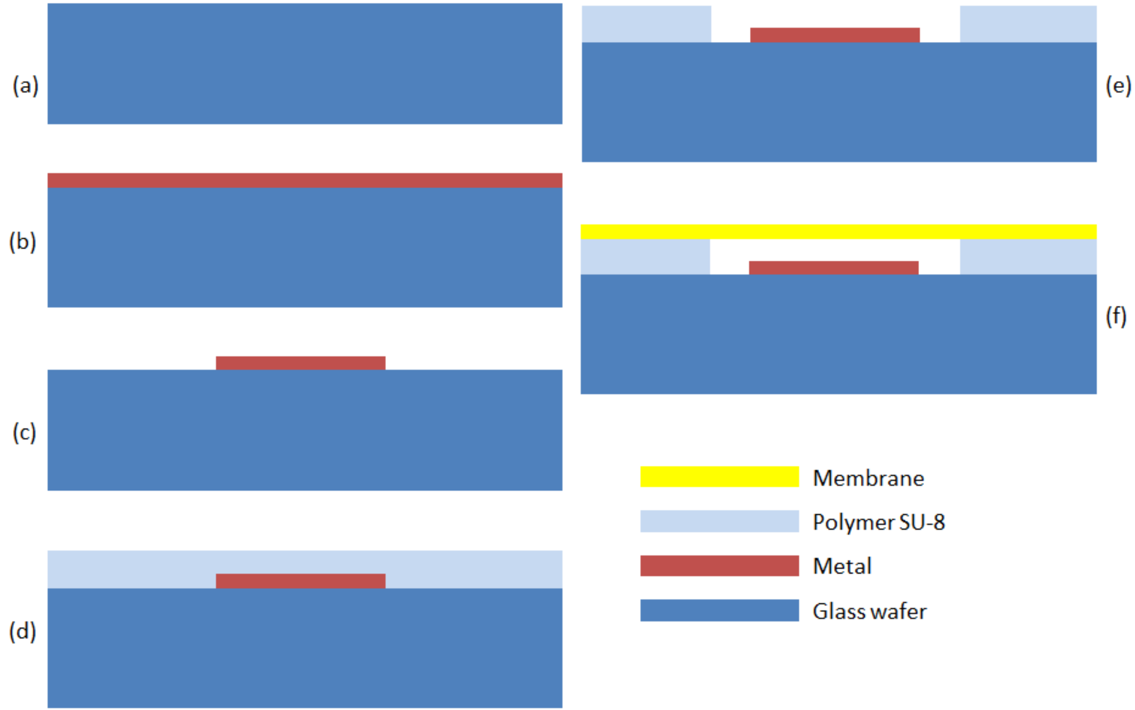


Figure 3-10: Fabrication steps and cross sectional view of the proposed tunable capacitor. (a) Wafer cleaning; (b) Metal deposition; (c) Metal etching; (d) SU-8 spinning; (e) SU-8 patterning; (f) Membrane bonding.

3.3.2. Fabrication Process for Inductors

Figure 3-11 shows the steps of the proposed tunable inductor. The first step was the same with the fabrication of proposed tunable capacitor. The metal layer was deposited and patterned, as shown in Figure 3-11 (c). Next, a 50 nm silicon dioxide layer was deposited on the metal by plasma-enhanced chemical vapor deposition (PECVD), as shown in Figure 3-11 (d). Metal 2 was also Cr/Au layer with the same thickness. It was deposited and patterned to desired shapes, as shown in Figure 3-11 (g). The SU-8 was spin as the structural layer, as shown in Figure 3-11 (h). Photolithography for SU-8 was carried out to form the gap between the bottom electrode and the membrane, as shown in Figure 3-11 (i). In Figure 3-11 (j), a polyimide membrane was bonded on to SU-8 and formed the upper electrode.

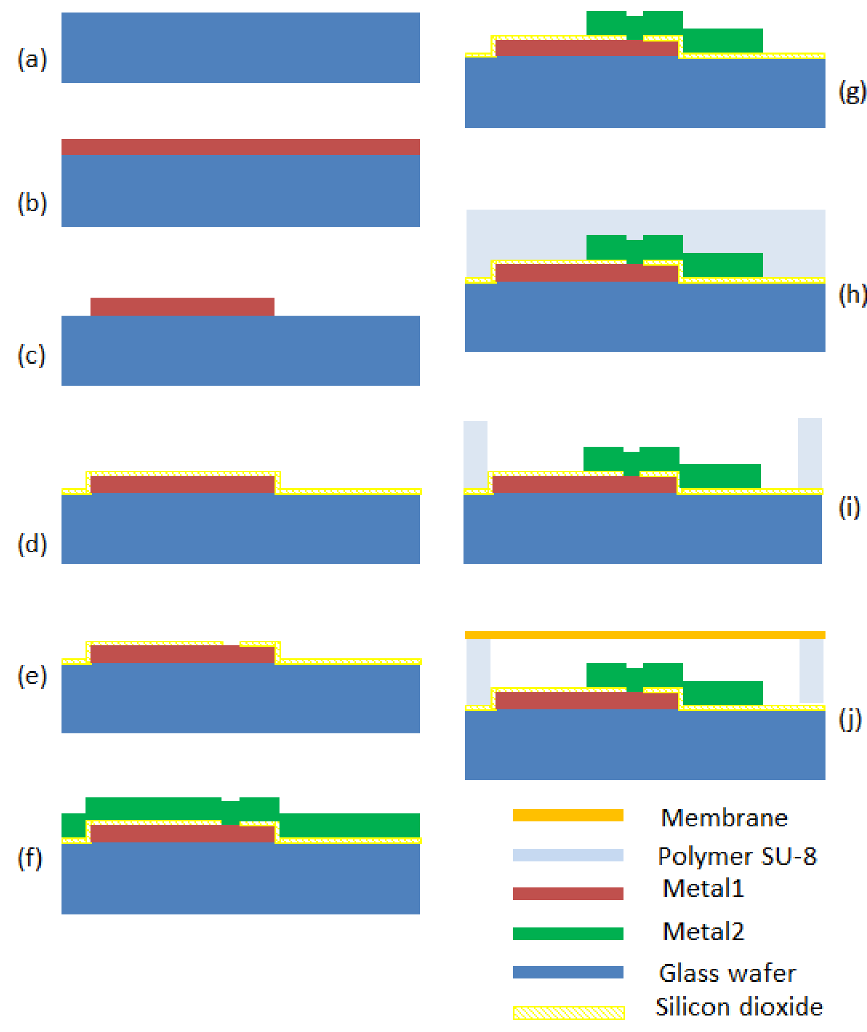


Figure 3-11: Fabrication steps and cross sectional view of the proposed tunable inductor. (a) Wafer cleaning; (b) Deposition of Metal 1; (c) Metal 1 etching; (d) Silicon dioxide deposition; (e) Silicon dioxide etching; (f) Deposition of Metal 2; (g) Metal 2 etching; (h) SU-8 spinning; (i) SU-8 patterning; (j) Membrane bonding.

Chapter 4. Tunable Inductors

In this chapter, different tunable inductors were simulated. Then inductors on PCB were designed, fabricated and tested.

4.1. Simulations

Tunable inductors were simulated with the aid of COMSOL Multiphysics. The purpose of simulation was to verify the variation tendency of the inductors. Two types of inductors were simulated, including the simplified solenoid inductors and the planar inductors. For the simplified solenoid inductors, the numbers of the coils were reduced. The properties of the materials were designated in COMSOL to characterize the portions of the inductors. The results were compared and explained.

4.1.1. Simplified Solenoid Inductors

The width of the sides of the coil was 20 μm. The whole length was 1000 μm. The conductivity of the coil material was 1e6 S/m and the relative permeability was 1, which indicated a metal material. While the conductivity and relative permeability of the core material were 1e7 S/m and 10 respectively, the core material was more like a magnetic material. The distance between the coil and core was changed. Three values, -800 μm, -300 μm and 200 μm were chosen (Figure 4-1). At the frequency of 10 MHz, the inductance data found from COMSOL simulation were respectively 9.232 nH, 9.034 nH and 9.275 nH.

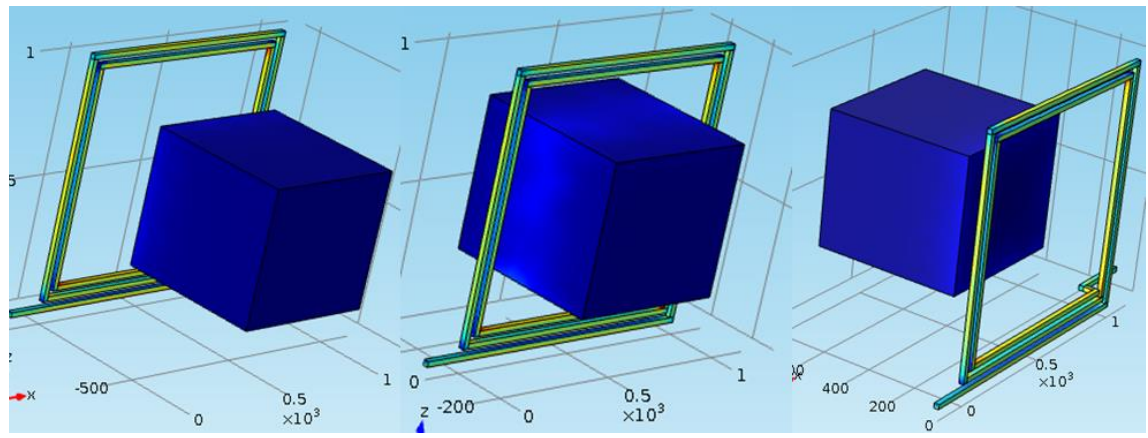


Figure 4-1: Schematics of three simulated inductors with different gap between the coil plate and the core

4.1.2. Planar Inductors

The conductivity and permeability of the coil material were 1e6 S/m and 1, as the material before. The simulation divided into two parts. First, a magnetic material was used to form the film. The electrical conductivity was 1e7 S/m and the relative permeability was 1e4. In the second simulation, a metal material was used to form the film. The electrical conductivity was 1e6 S/m and the relative permeability was 1.

When magnetic material was used, the film worked as the magnetic core. It enhanced the magnetic flux of the coil inductor. That means, if the film got closer to the coils, the inductance was larger. If the film moved away from the coils, the inductance was smaller. Figure 4-2 present the color change of the magnetic flux density. The result confirmed this theory. At the frequency of 100 MHz, the inductance was 1.166 nH with the distance of 30 μm, while the inductance was 0.830 nH with the distance of 80 μm.

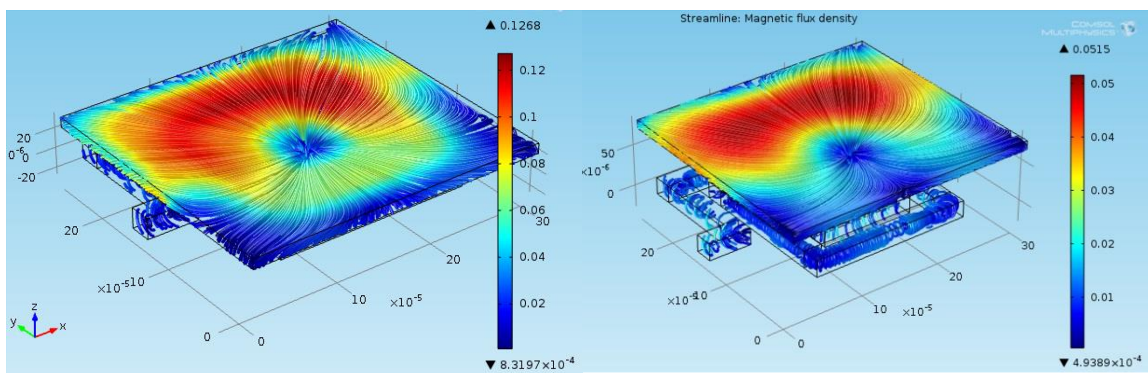


Figure 4-2: Schematic of two simulated planar inductors with different gap between the inductor and the film

When the metal was used as the film, instead of enhancing the magnetic flux, it had induced magnetically current in the film. This magnetically induced current created an opposite magnetic flux of the coil inductor. As a result, the total magnetic flux was reduced and the inductance became smaller when the film was moved closer to the coils. At the frequency of 100 MHz, the inductance was 0.465 nH with the distance of 30 μm, while the inductance was 0.734 nH with the distance of 80 μm. The data is shown in the table.

Table 4-1: The simulation results of planar inductors

Distance	Magnetic film	Metal film
30 μm	1.166 nH	0.465 nH
80 μm	0.830 nH	0.734 nH

4.2. Experiment

Ten planar inductors were designed by PCB software and manufactured. The thickness of FR4 was 0.062". The copper weight was 1 oz, which means one ounce per square foot [41]. The formula for copper weight (in oz) to thickness (in mils) conversion is:

Thickness (in mils) = thickness (in oz) * 1.37

So the thickness of the coils was 1.37 mils or 0.035 mm.

The parameters were shown in Table 4-2. As shown in Figure 4-3, ten planar inductors with different configurations were designed and fabricated.

Table 4-2: The different parameters of ten planar inductors

	Width(mm)	Pitch(mm)	Turns	Length of side(mm)
L1	0.152	0.152	28	19.99
L2	0.152	0.152	20	19.99
L3	0.152	0.152	10	19.99
L4	0.152	0.152	7	19.99
L5	0.305	0.152	20	19.99
L6	0.305	0.305	14	19.99
L7	0.152	0.152	10	7.62
L8	0.152	0.152	19	13.33
L9	0.305	0.610	10	19.99
L10	0.610	0.152	6	19.99

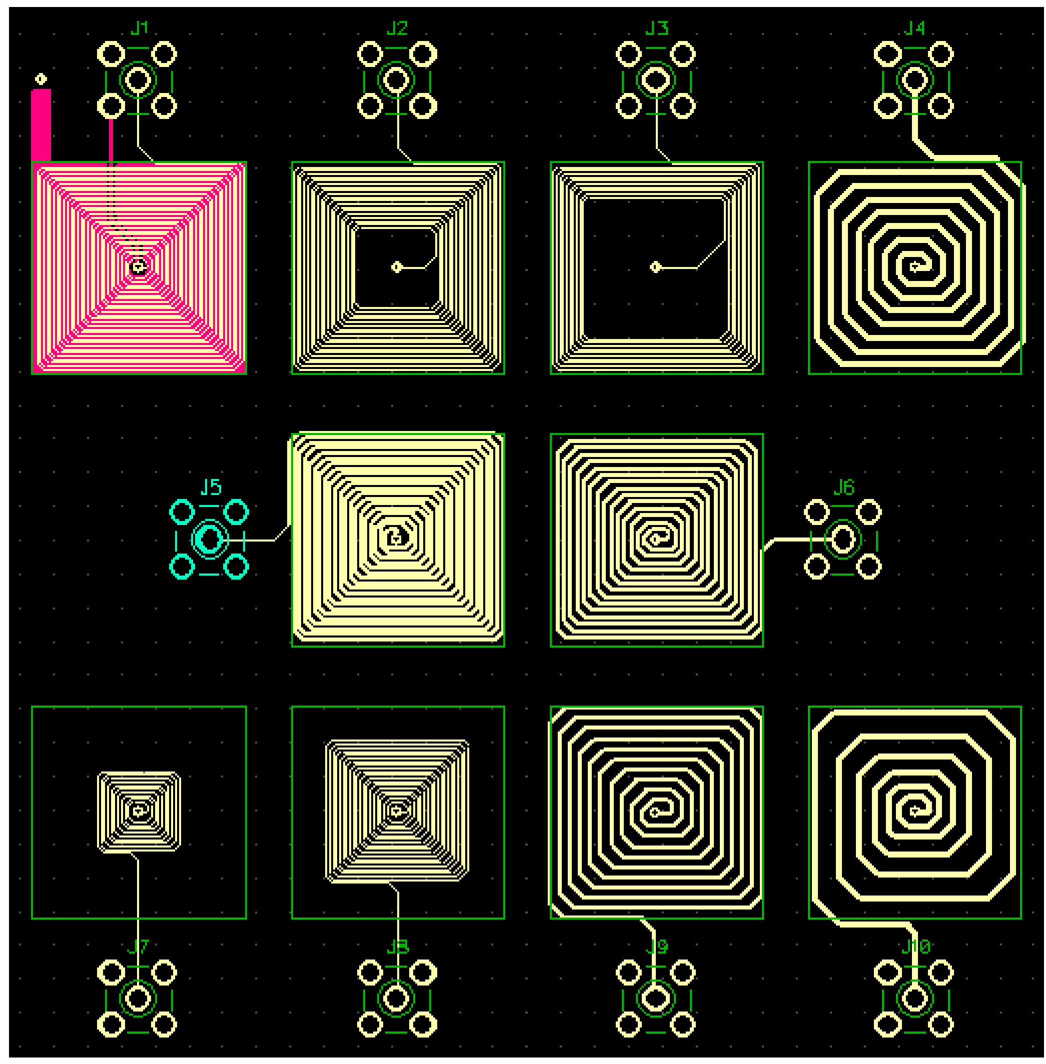


Figure 4-3: Schematic of ten planar inductors with different configurations

One of the fabricated inductors is shown in Figure 4-4. The planar inductor was connected to a 90 degree type screw SMA connector. It was then connected to a vector network analyzer through the cable.

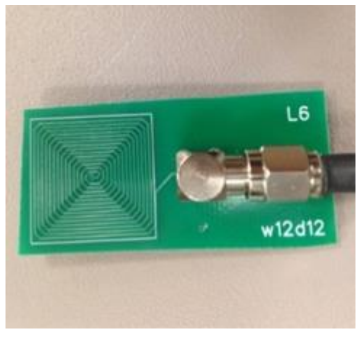


Figure 4-4: Top view of one planar inductor with cable

4.3. Test Results of Tunable Inductors

The inductors were tested with different films, including aluminum film, copper film, and magnetic film. The aluminum film and copper film had high conductivity, low electrical resistivity, and low permeability. The magnetic film was alloy 2714A from Matglas. It had relatively high electrical resistivity and its maximum annealed permeability was 10^6. Finally, a carbon nanoparticle film which has low conductivity and low permeability was added to compare the results. It can be regarded as non-conductive material.

Materials	Electrical Resistivity P (Ω*m) at 20°C	Permeability μ (H/m)	Reference
Aluminum film	2.82×10^{-8}	1.256665×10^{-6}	[42]
Copper film	1.68×10^{-8}	1.256629×10^{-6}	[43]
Magnetic film	142×10^{-8}	10^{6}	[44]

The inductances were tested by vector network analyzer ZVB4 from Rohde & Schwarz. The test frequency was 30 MHz. Y parameters were recorded in the form of

the real part and imaginary part in each situation. The distance between the inductor and the film was controlled manually. The fitting circuit was as shown in Figure 4-5.

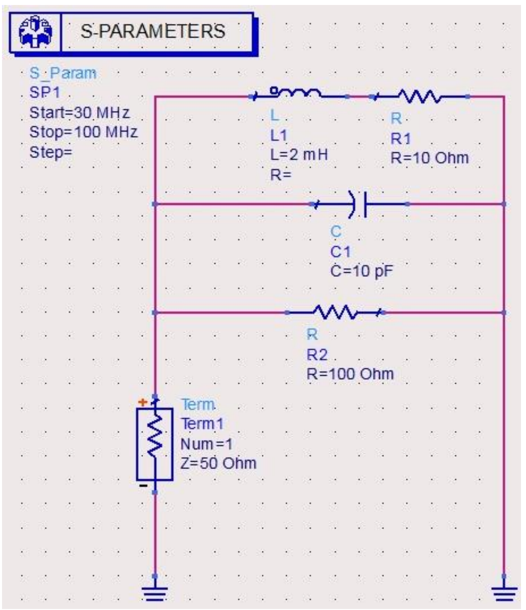


Figure 4-5: Fitting circuit of the PCB inductor

The inductor was in series with a parasitic resistor. This series branch was then in parallel with a parasitic capacitor and a parasitic resistor. After running the Matlab code (See Appendix A), the inductances can be calculated.

The test results of inductor L1 with two metal films were shown in Table 4-3. “Floating” meant the film was not connected. On the other hand, “Grounded” indicated that the film was connected to ground. As we can see from Figure 4-6, the inductance increased when the metal moved away from the coils.

Table 4-3: Test results of inductor L1

L1	160μm		320μm		480μm		640μm		800μm	
(μH)	F	G	F	G	F	G	F	G	F	G
Cu	2.72	4.39	4.0	5.73	5.22	7.11	6.37	8.27	7.27	9.50
Al	1.69	1.22	3.18	2.76	4.46	4.88	5.68	6.37	6.90	8.81

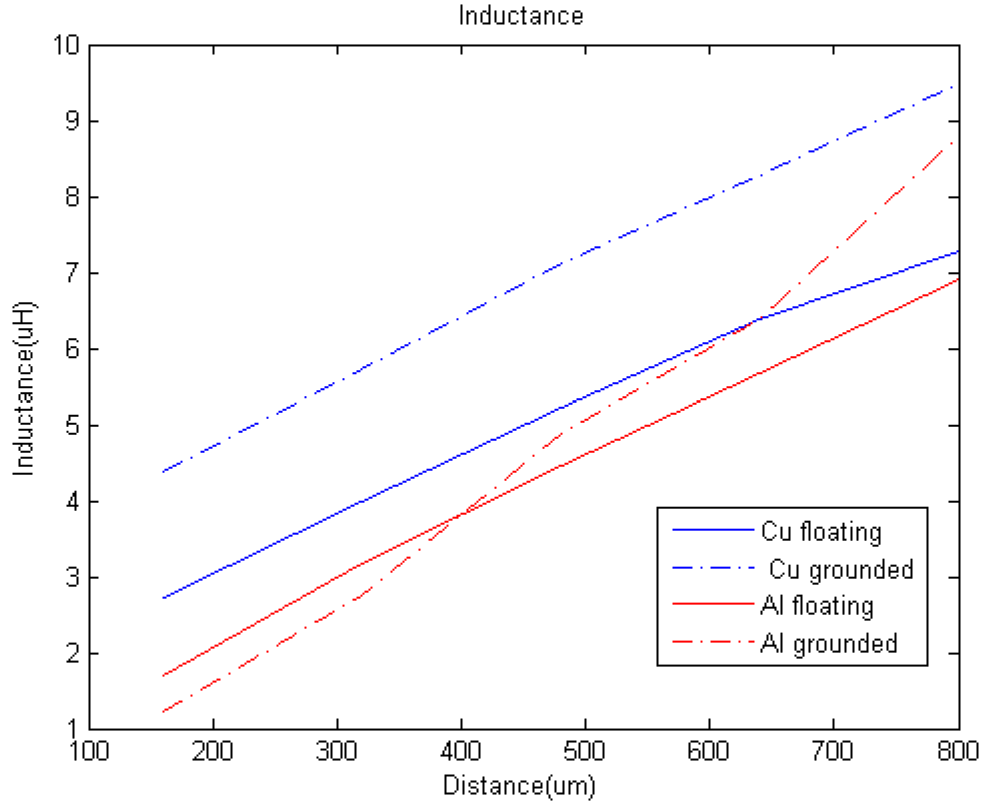


Figure 4-6: Test result of inductor L1

The test results of inductor L10 with four different films were shown in the following figures. In each group, the figure on the left was the result with floating film while the figure on the right was the result with grounded film. Figure 4-7 and Figure 4-8 presented the result with the aluminum film and copper film. The inductances increased with metal films moving away. Figure 4-9 showed the result with carbon nanoparticles film. Since the nanoparticles were non-conductive, regardless of whether the film was floating or grounded, the difference in the inductance was negligible. As shown in Figure 4-10, the inductance did not change significantly with floating magnetic film. But it decreased with grounded magnetic film.

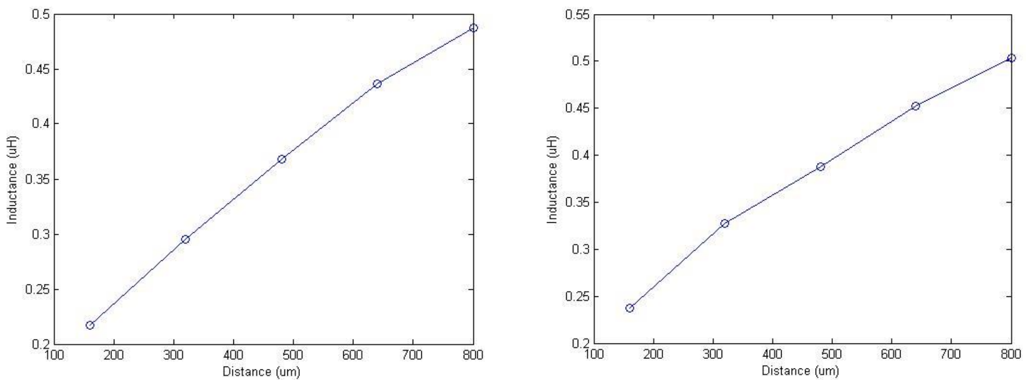


Figure 4-7: Test result of inductor L10 with aluminum film, floating (left) and grounded (right) respectively

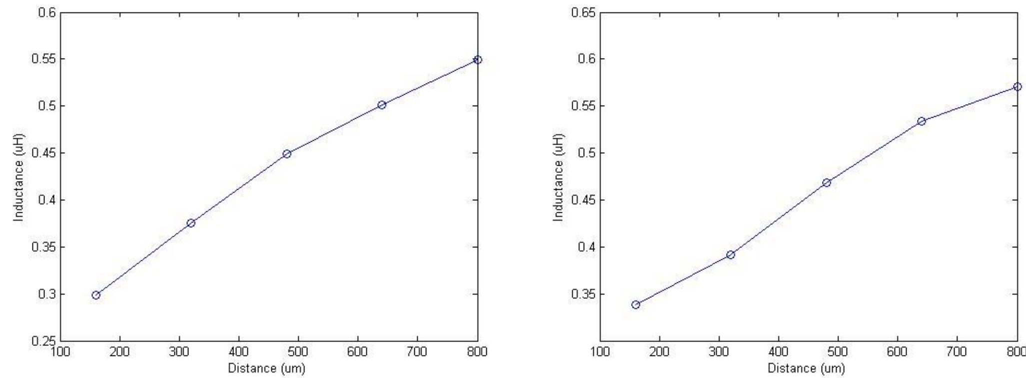


Figure 4-8: Test result of inductor L10 with copper film, floating (left) and grounded (right) respectively

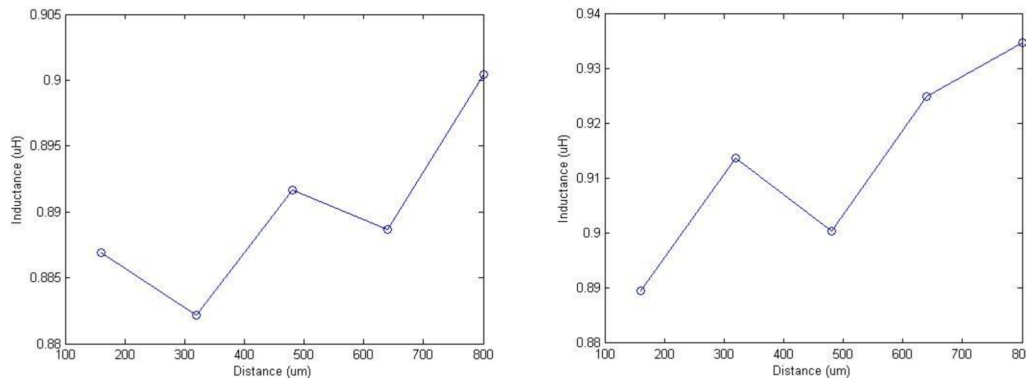


Figure 4-9: Test result of inductor L10 with carbon nanoparticles film, floating (left) and grounded (right) respectively

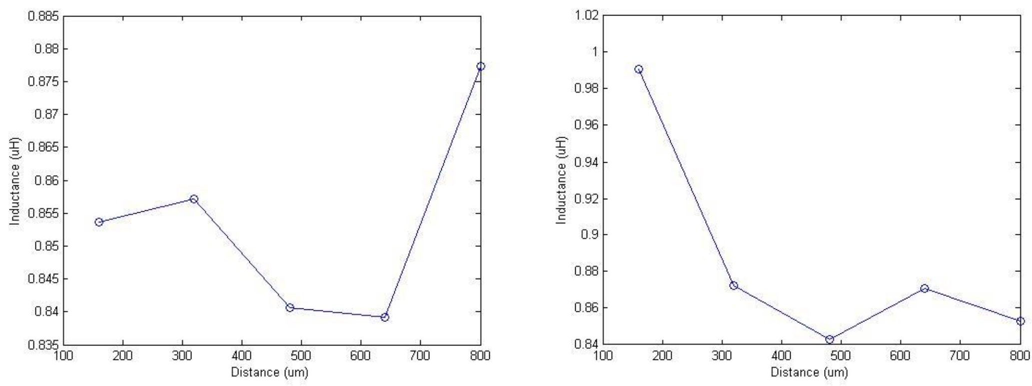


Figure 4-10: Test result of inductor L10 with magnetic film, floating (left) and grounded (right) respectively

In conclusion, the change in inductances with different films was consistent with the proposed method (Figure 4-11). Although two results were presented for each film, the result with floating film was more accurate. In the floating case, the films were not connected to the ground and the effecting induced current in the film was evident.

The magnetic film acted as the magnetic core. It enhanced the magnetic field created by the inductor. Effective permeability of the magnetic circuit increased with decreasing distance. This leaded to a resultant magnetic field being larger than the incident field in magnitude, and resulted in measured inductance being larger than its

intrinsic value. The inductance decreased when the magnetic film moved away. The film made of carbon nanoparticles is not conductive. It has negligible influence on the inductance. The metal films were conductive. Due to the eddy current induced in the metal films, the induced magnetic field was opposed to the original magnetic field. It decreased the inductance. If the distance between the metal film and inductor was larger, the impact on the inductor was smaller.

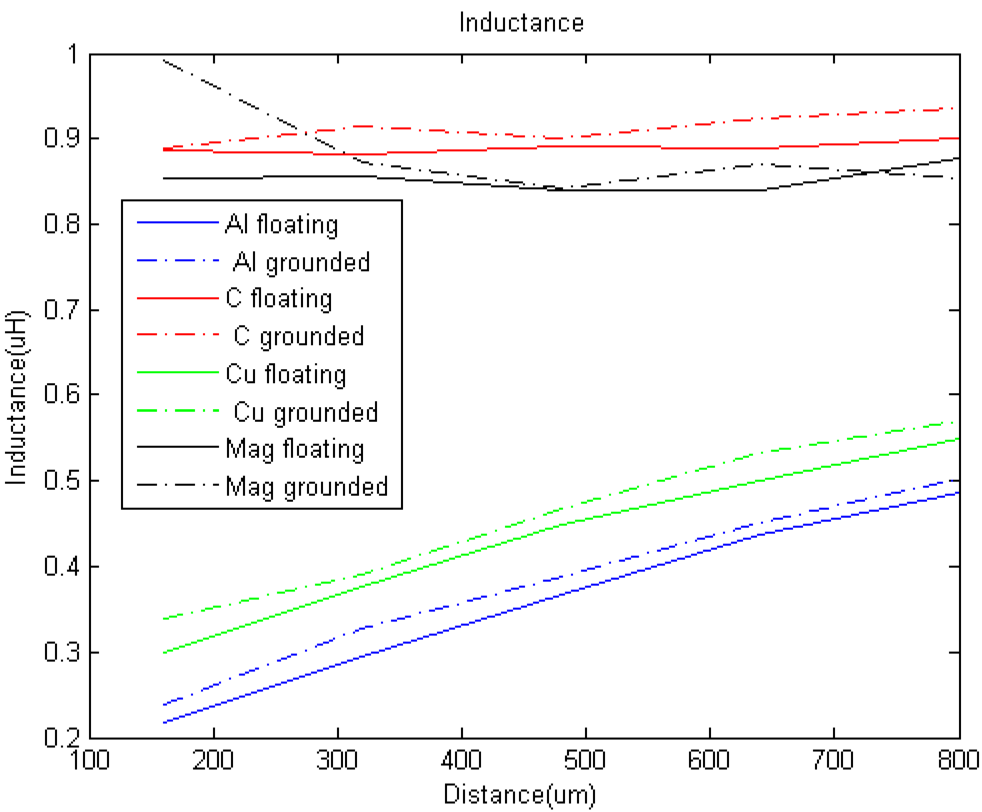


Figure 4-11: Test result of inductor L10 with different films

Chapter 5. Tunable Capacitors

In this chapter, the design steps of tunable capacitors were provided. In order to get maximum displacement for a capacitor with particular parameters, the size of the capacitor was carefully calculated. The masks were drawn in Coventor and exported as a dxf file. In order not to reduce the resolution, the dxf file was converted into ps file and pdf file. The pdf file was sent out to be printed on transparency with 2400 dpi resolution and emulsion down. Finally, the transparency was cut and attached to the 4-inch square glass to form a standard mask to be used in the exposure system.

5.1. Theory and Design

5.1.1. Maximum Displacement

Let's treat the parallel plates like two infinite planes, and then we can get the electric field between the plates by Gauss' Law.

$$E = \frac{\sigma}{2\varepsilon\varepsilon_0} \quad (5\text{-}1)$$

where σ is the sheet charge density in Coulombs per square meter, ε is the relative permittivity of the material and ε_0 is the permittivity of free space. If the Q is the charge on plate, the relation between Q and σ is:

$$\sigma = \frac{Q}{A} \quad (5\text{-}2)$$

where A is the area of the plate.

If the plates move towards each other, the electric field would be canceled outside the two plates. The electric field (Figure 5-1) between the plates is

$$E = \frac{\sigma}{\varepsilon\varepsilon_0} = \frac{Q}{A\varepsilon\varepsilon_0} \tag{5-3}$$

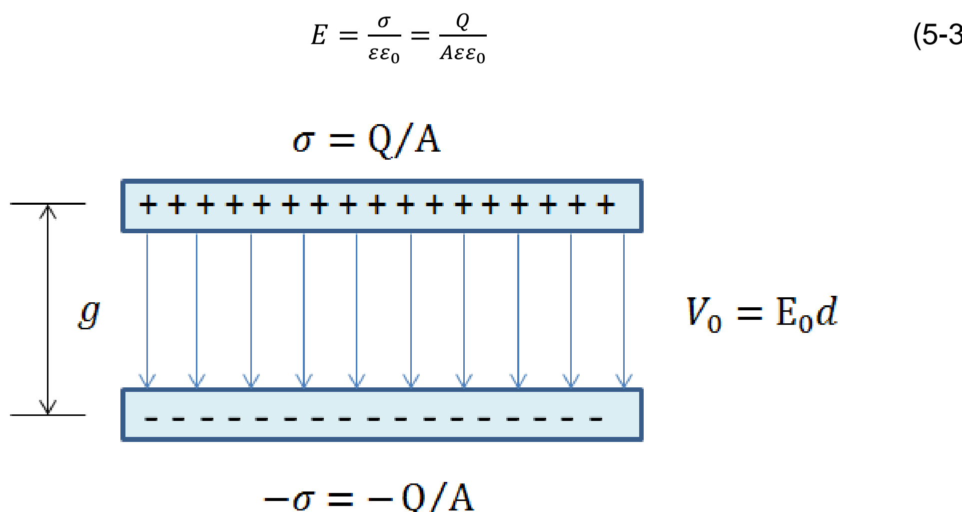


Figure 5-1: Schematic of electric field between two parallel plates

When a bias voltage is applied across the plates, the voltage difference between the two plates can be expressed by the electric field and the distance between two plates.

$$\mathrm{V} = \mathrm{Ed} = \frac{\mathrm{Qd}}{\mathrm{A}\varepsilon\varepsilon_0} \tag{5-4}$$

By definition, the capacitance C is given by

$$\mathrm{C} = \frac{\mathrm{Q}}{\mathrm{V}} = \frac{\varepsilon\varepsilon_0\mathrm{A}}{\mathrm{d}} \tag{5-5}$$

As we knew from Eq.(5-1), the electric field at points close to the surface of one plate is approximately:

$$\mathrm{E} = \frac{\sigma}{2\varepsilon\varepsilon_0} \tag{5-6}$$

Subsequently, the magnitude of the electrostatic force exerted on this plate by the other plate is given by:

$$\mathrm{F} = \mathrm{QE} = \frac{\mathrm{Q}^2}{2\mathrm{A}\varepsilon\varepsilon_0} \tag{5-7}$$

From Eq.(5-4), we know that

$$Q = \frac{\varepsilon\varepsilon_0 AV}{d} \tag{5-8}$$

Combining Eq.(5-7) and Eq.(5-8), we can get the relation between electrostatic force and the voltage.

$$F = \frac{\varepsilon\varepsilon_0 AV^2}{2d^2} \tag{5-9}$$

The pressure can be express as:

$$P = \frac{F}{A} = \frac{\varepsilon\varepsilon_0 V^2}{2d^2} \tag{5-10}$$

On the other hand, the flexure rigidity of diaphragm D is described by the following equation:

$$D = \frac{Eh^3}{12(1-v^2)} \tag{5-11}$$

where E is Young's modulus, h is the thickness of the membrane and v is Poisson's ratio [45]. For a circular diaphragm membrane under a uniform applied pressure loading p, the deflection is given by

$$w(r) = w_m\left(1 - \frac{r^2}{a^2}\right)^2 = \frac{pa^4}{64D}\left(1 - \frac{r^2}{a^2}\right)^2 \tag{5-12}$$

where p is the pressure which causes the deflection, and a is the radius of the circular diaphragm (Figure 5-2).

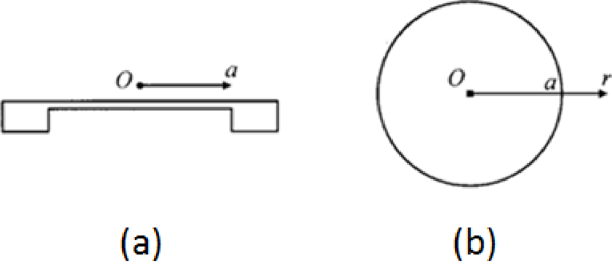


Figure 5-2: Schematic of the circular diaphragm membrane. (a) Side view; (b) Top view.

The maximum displacement at the center of the diaphragm can be written as:

$$w_m = \frac{pa^4}{64D} \tag{5-13}$$

It is useful to further manipulate Eq.(5-10) by Eq.(5-12) to find w_m as a function of applied voltage.

$$w_m = \frac{3}{32}\frac{(1-v^2)\varepsilon\varepsilon_0 V^2 a^4}{Ed^2h^3} \tag{5-14}$$

The average of the displacement across the membrane would be:

$$w_a = \frac{1}{20}\frac{(1-v^2)\varepsilon\varepsilon_0 V^2 a^4}{Ed^2h^3} \tag{5-15}$$

5.1.2. Breakdown Voltage

Paschen's Law characterizes the breakdown voltage as a function of gap distance and gas pressure in the uniform electric field [46]. It can be described by the equation:

$$V_B = \frac{Bpd}{\mathrm{In}(pdA/k)} \tag{5-16}$$

where V_B is the breakdown voltage in volts, p is the pressure in Bar, d is the gap distance, and the constants A, B and k depend on the composition of the gas. For air at standard atmospheric pressure of 1.013 Bar,

$$A = 6450\ (\mathrm{bar} \cdot \mathrm{cm})^{-1} \quad (5\text{-}17)$$

$$B = 190\mathrm{kV}\ (\mathrm{bar} \cdot \mathrm{cm})^{-1} \quad (5\text{-}18)$$

$$k = 13.3 \quad (5\text{-}19)$$

If the gap distance is $50\ um$, the minimum arc voltage can be found as Eq.(5-20).

$$V_B = 1071\ V \quad (5\text{-}20)$$

In small uniform gaps, it has been found empirically that, at standard pressure $(1\ bar = 101.3\ kPa = 760\ mm\ Hg)$ and temperature (20°C), the breakdown occurs at a field strength of approximately $30\ kV/cm$, which is the dielectric strength of air [47]. For the gap distance of $50\ um$, the breakdown voltage is $150\ V$.

5.1.3. Capacitance of the Tunable Capacitor

From $w_a = \frac{1}{20}\frac{(1-v^2)\varepsilon\varepsilon_0 V^2 a^4}{Ed^2h^3}$ (5-15), when the maximum distance between the two electrodes is y, the capacitor can be expressed as:

$$C = \frac{\varepsilon\varepsilon_0 \pi a^2}{y - w_a} \quad (5\text{-}21)$$

In the experiment, Poisson's ratio v of polyimide is 0.34. Young's modulus E is 2.5 Gpa. The permittivity of free space ε_0 is $8.854 \times 10^{-12}\ F/m$. The relative permittivity ε of air is 1.

For three different radii, the capacitances are listed in Table 5-1.

Table 5-1: Calculated capacitances of capacitors with three different radii for different amounts of deflection at the centre of the membrane

Voltage (V)	a=5mm		a=6mm		a=7mm	
	C(pF)	Wa(µm)	C(pF)	Wa(µm)	C(pF)	Wa(µm)
10	13.97	0.251	20.23	0.520	27.78	0.963
20	14.19	1.002	20.89	2.078	29.52	3.850
30	14.56	2.255	22.08	4.676	32.96	8.663
40	15.11	4.009	24.01	8.313	39.37	15.40
50	15.89	6.264	27.04	12.99	52.53	24.07
60	16.96	9.021	31.98	18.71	88.77	34.65
70	18.43	12.28	40.78	25.46	48.10	47.17
80	20.46	16.04	59.77	33.25	-	61.61
90	23.40	20.30	126.5	42.09	-	77.97
100	27.87	25.06	-	51.96	-	96.26

Figure 5-3 shows the results of deflections changing with the voltage.

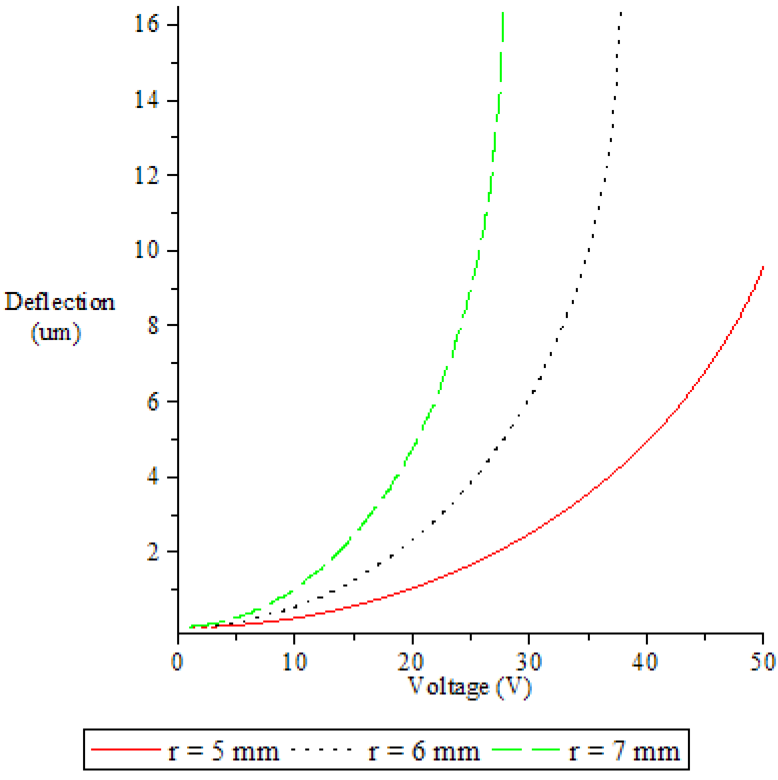


Figure 5-3: Changes in deflections with the voltages

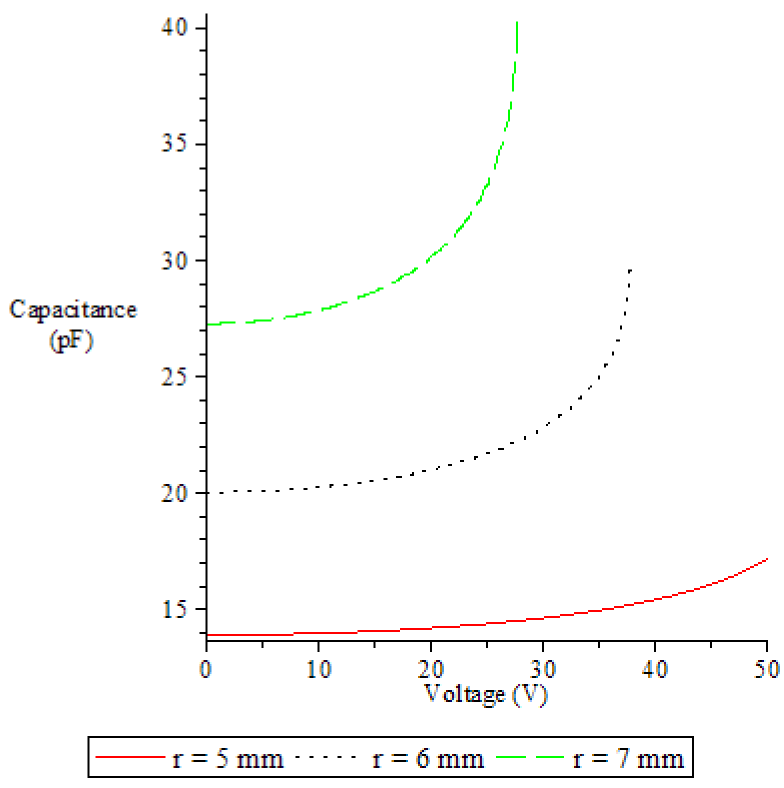


Figure 5-4: Changes in capacitances with the voltages

Figure 5-4 shows the changes in capacitances with the voltage. The maximum differences are from 31% to 42%. However, when the radius is too large, it easily reaches the pull-in position with relatively low voltage. So a radius of 6 mm was chosen in the mask to pattern the tunable capacitors.

5.2. Test Results of Tunable Capacitors

ZVB4 Vector Network Analyzers from Rohde & Schwarz was used to test the tunable capacitors. One electrode was connected to one port of the analyzer, and the top electrode was connected to ground. Thus, the capacitor was connected in the loop. The voltage was applied using bias tees from picosecond pulse labs. The circuit of bias tee was shown in Figure 5-5. The maximum voltage of this bias tee was 250V.

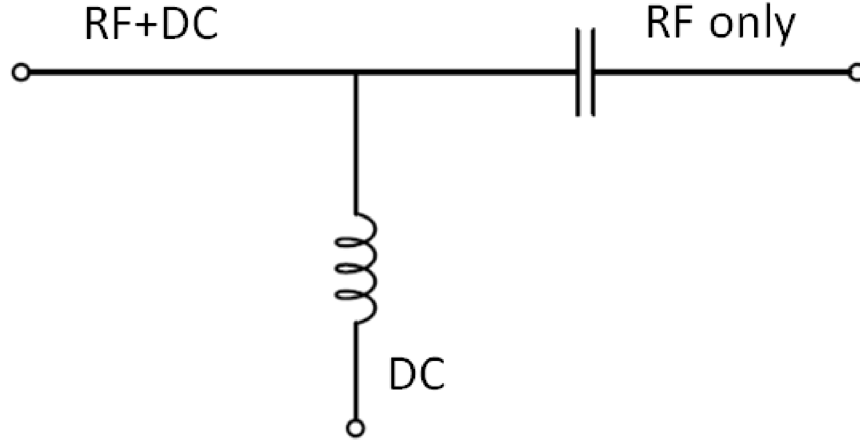


Figure 5-5: Schematic of bias tee

After calibration, the imaginary part of Y11 at the frequency of 2 MHz was collected. The capacitance can be calculated (See Appendix B). When the voltage increased from 0 V to 130 V, the capacitance increases from 13.3 pF to 17.7 pF. The variation is around 33%. When the voltage is decreased, the capacitance decreased. It can be seen from Figure 5-6 that below 50 V the capacitance increased rapidly with the increasing voltage. It is same with Figure 5-4. After 50 V, the pull-in effect appears. The speed of change in the capacitance dropped. The whole curve shows hysteresis due to the stress of the membrane.

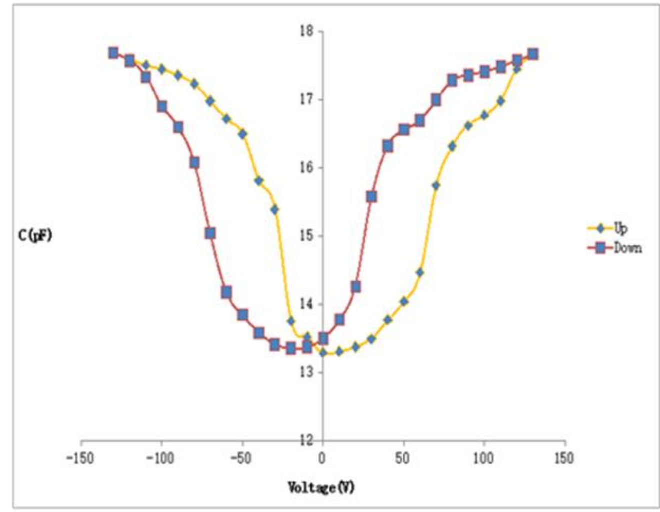


Figure 5-6: Test results for a tunable capacitor

Based on this result, many T matching network can be designed as follows:

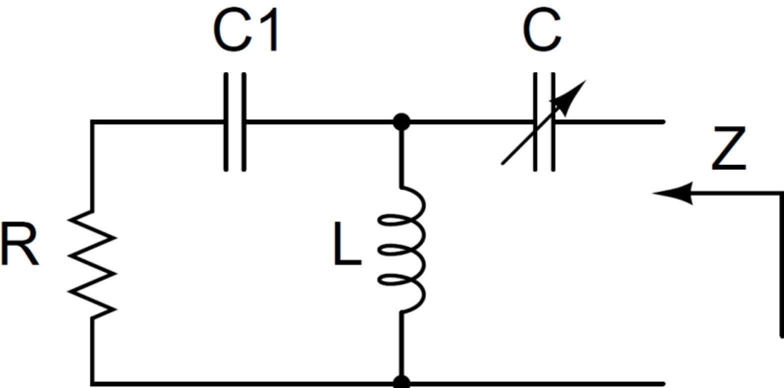


Figure 5-7: Schematic of T matching network with tunable capacitor

$$Z = \frac{1}{\frac{1}{R+\frac{1}{jwC1}}+\frac{1}{jwL}} + \frac{1}{jwC} \qquad (5\text{-}22)$$

Z^* is the impedance can be matched. When L is chosen to be 0.2 μH, C1=68 pF, the range of Z is given in Table 5-2 and was shown in Figure 5-8.

Table 5-2: The matched impedances with tunable capacitor

R(ohm)	L(uH)	C1(pF)	C(pF)	Z=Z*(Real)(Ω)	Z(imag)(Ω)	Z*(imag)(Ω)
50	0.2	68	12	60.949	-131.66	131.66
50	0.2	68	13	60.949	-121.45	121.45
50	0.2	68	14	60.949	-112.70	112.70
50	0.2	68	15	60.949	-105.12	105.12
50	0.2	68	16	60.949	-98.482	98.482
50	0.2	68	17	60.949	-92.627	92.627
50	0.2	68	18	60.949	-87.424	87.424

Figure 5-8: Range of matched impedances shown in the Smith Chart

Based on the results, the matched impedances can be expanded by connecting a capacitor in parallel with the tunable capacitor. The circuit becomes as below (Figure 5-9). The matched range of impedance is given in Table 5-3 and was shown in Figure 5-10.

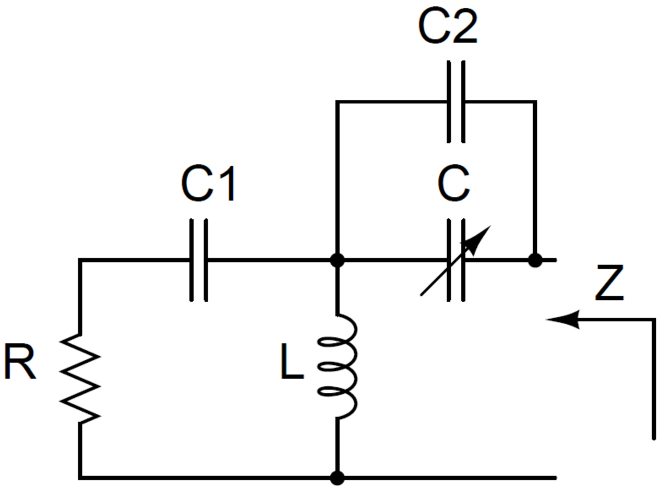


Figure 5-9: Schematic of improved T matching network with a fixed capacitor in parallel with the tunable capacitor

Table 5-3: The matched impedances of the improved T-type matching network

R(ohm)	L(uH)	C1(pF)	C2(pF)	C(pF)	Z=Z*(Real)(Ω)	Z(imag)(Ω)	Z*(imag)(Ω)
50	0.2	68	12	12	60.949	-65.308	65.308
50	0.2	68	12	13	60.949	-62.654	62.654
50	0.2	68	12	14	60.949	-60.204	60.204
50	0.2	68	12	15	60.949	-57.936	57.936
50	0.2	68	12	16	60.949	-55.829	55.829
50	0.2	68	12	17	60.949	-53.868	53.868
50	0.2	68	12	18	60.949	-52.038	52.038

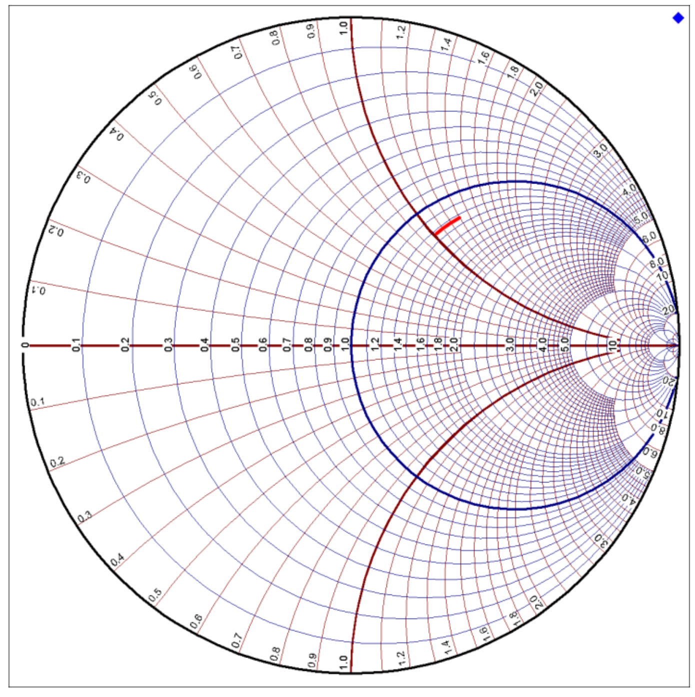


Figure 5-10: Schematic of matched impedances of the improved T-type matching network shown in the Smith Chart

The C2 can be replaced by a different value or it is also can be tunable. Here another value was chosen to find out the impact of C2. Table 5-4 shows the matched impedances and the results were also drawn in Figure 5-11.

Table 5-4: The matched impedances of the improved T-type matching network with a different C2

R(ohm)	L(uH)	C1(pF)	C2(pF)	C(pF)	Z=Z*(Real)(Ω)	Z(imag)(Ω)	Z*(imag)(Ω)
50	0.2	68	30	12	60.949	-36.873	36.873
50	0.2	68	30	13	60.949	-35.991	35.991
50	0.2	68	30	14	60.949	-35.149	35.149
50	0.2	68	30	15	60.949	-34.345	34.345
50	0.2	68	30	16	60.949	-33.576	33.576
50	0.2	68	30	17	60.949	-32.839	32.839
50	0.2	68	30	18	60.949	-32.133	32.133

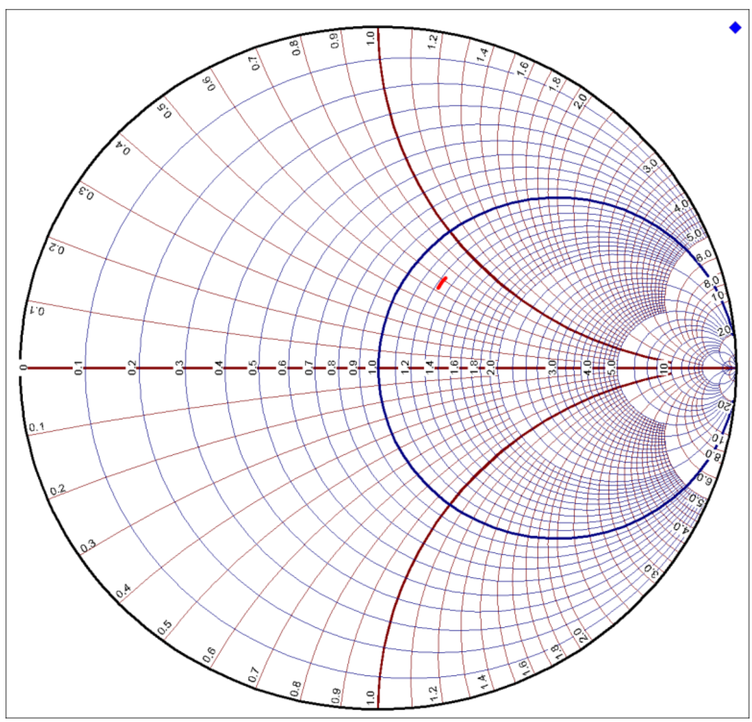


Figure 5-11: Schematic of matched impedances of the improved T matching network and different C2 shown in the Smith Chart

The matched impedance can cover a whole line in the Smith chart with the help of T matching network (Figure 5-12).

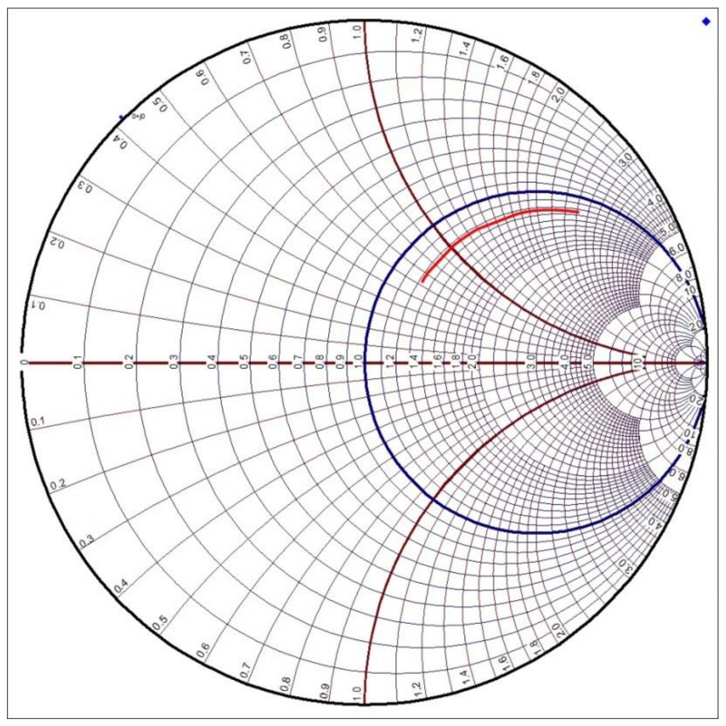


Figure 5-12: Summary of matched impedances of the T matching network with different C2

If C1 was tunable, the covered area can be expanded. Here, three values were 68 pF, 47 pF and 33 pF, respectively. The other parameters were the same. The impedances were shown in Figure 5-13.

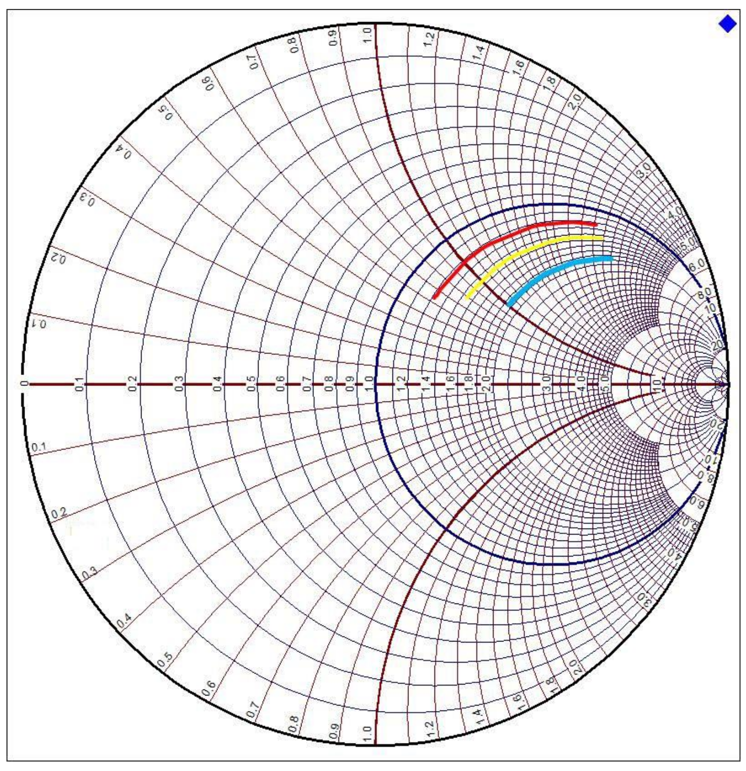
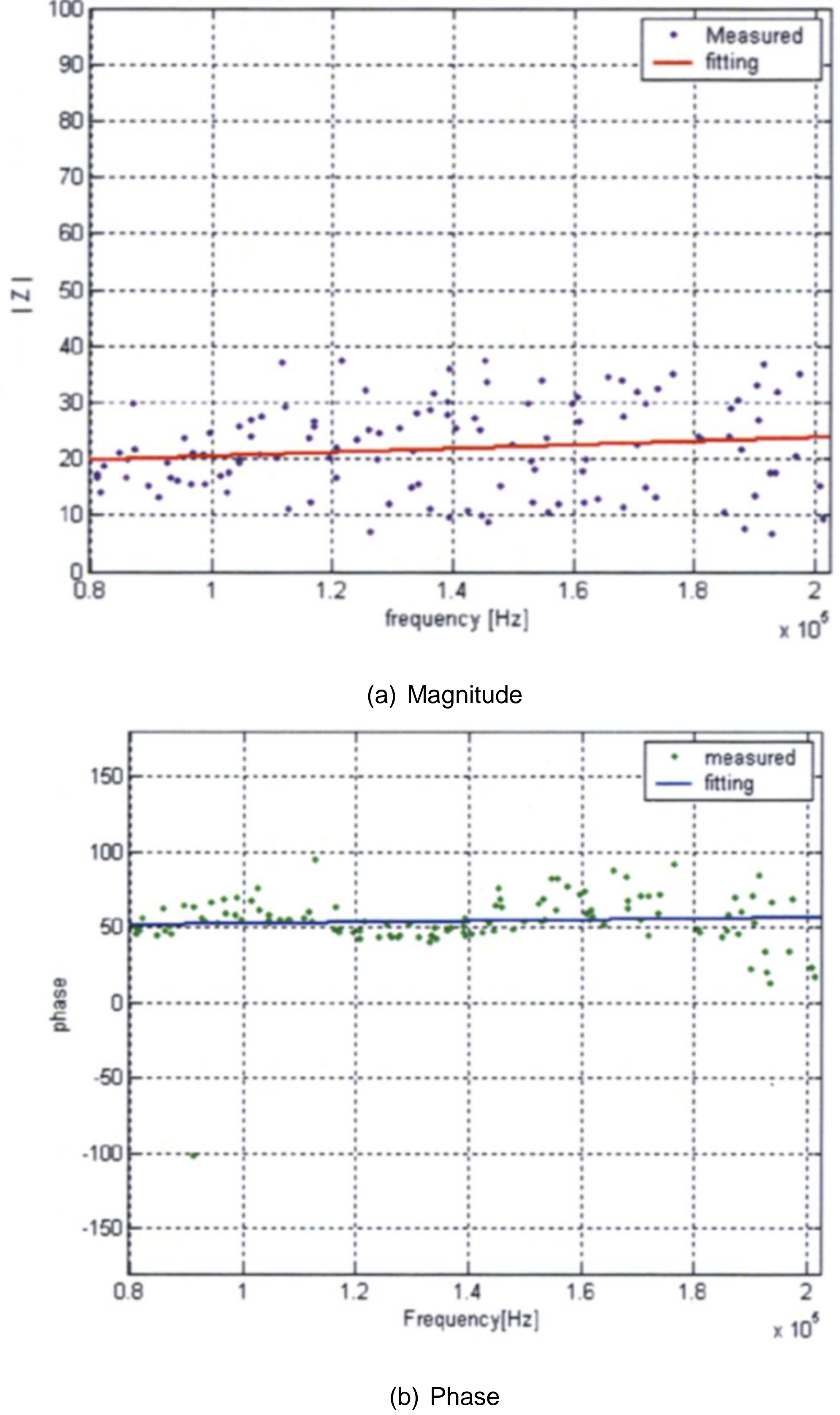


Figure 5-13: Schematic of matched impedances with tunable C1

Chapter 6. Tunable Impedance Matching Network

6.1. Access Impedance Range

The variation of the power line access impedance is according to ambient environment such as the varying load. In [48], the access impedance was measured. Figure 6-1 shows the magnitude and phase of the measured access impedances. The variation range of the access impedance is assumed to be within the measurement results (7 μH< $L_{acceess}$ <27 μH, 5 Ω< R_{access} <20 Ω).



(a) Magnitude

(b) Phase

Figure 6-1: The measured access impedances, (a) Magnitude; (b) Phase. [48] ©2008 IEEE.

In [49], the normalized real part of the impedance includes values below 5, which equals to 250 Ω (normalization was performed to 50 Ω), and the normalized imaginary part is between -3.5 and +3.0, which corresponds to -175 Ω and +150 Ω, respectively. It chose several points at the rim of the area.

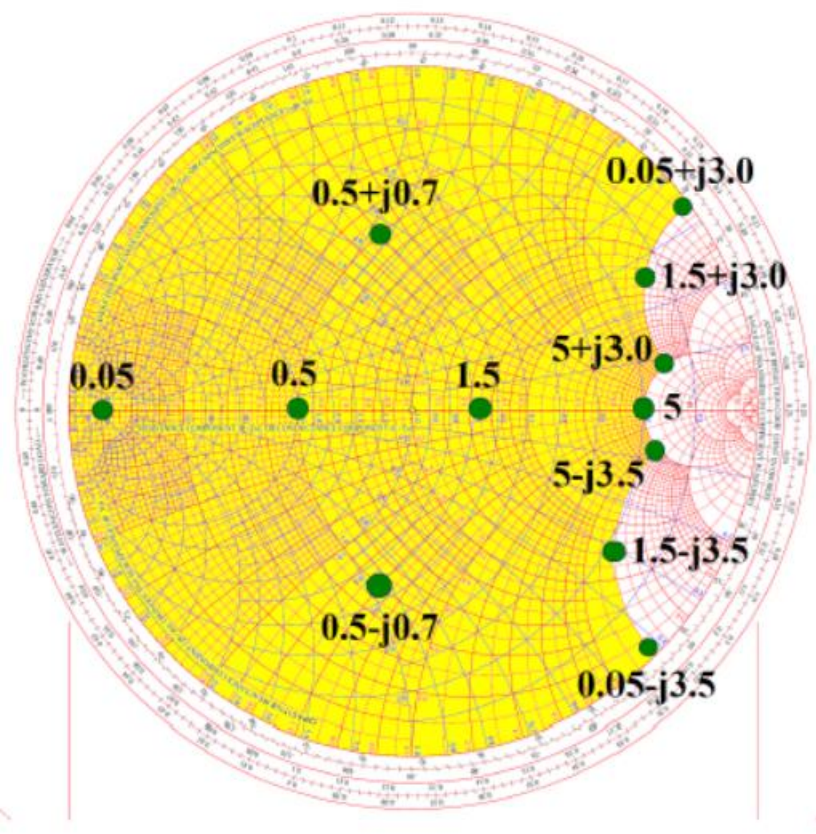


Figure 6-2: Access impedance range for VPLC applications using frequencies between 1-100 MHz. The values on the chart are normalized to 50 Ω. [49] ©2014 IEEE.

The impedance matching network can be designed based on the access impedance range.

6.2. Impedance Matching Simulation in ADS

The simulation can be performed using Advanced Design System (ADS). At the frequency of 2 MHz, the load can be chosen as 5+j*88 Ω, which is a resistor with the resistance 5 Ω in series of an inductor with the inductance 7 μH. The circuit can be

drawn in the schematic as Figure 6-3. The frequency range is from 1 MHz to 10 MHz with the step 1 MHz.

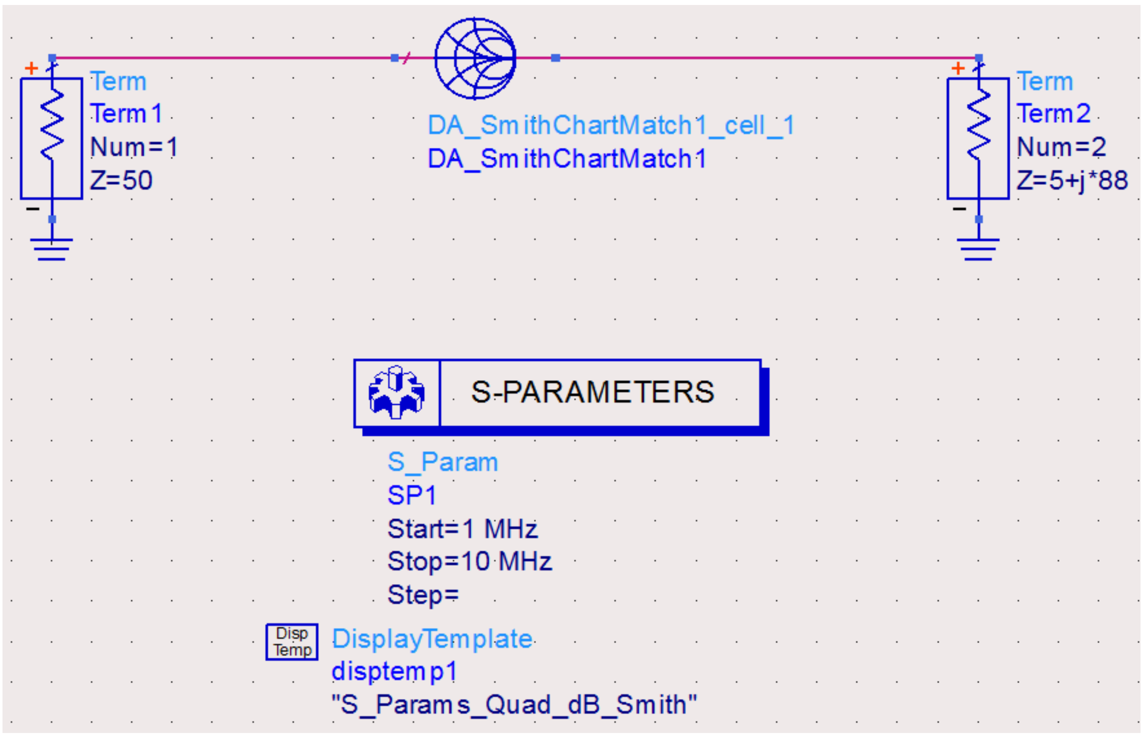


Figure 6-3: Schematic of the impedance matching simulation

After simulating the circuit, the result is shown in the "Smith Chart Utility". The load and source impedances are shown in the Smith Chart. The function "Auto 2-Element Match" provides four different configurations of L-type matching networks. Figure 6-8 presents the L-type networks and their components.

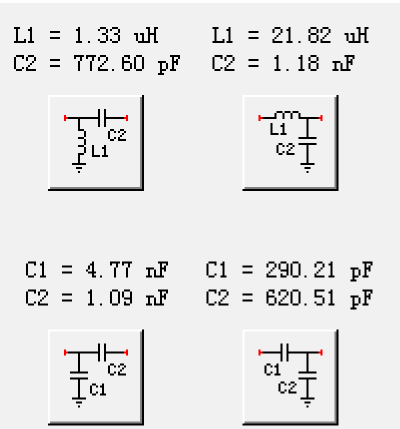


Figure 6-4: Four different configurations of the L-type matching networks

Corresponding to these matching networks, the paths in the Smith Chart from load to source are shown in Figure 6-5.

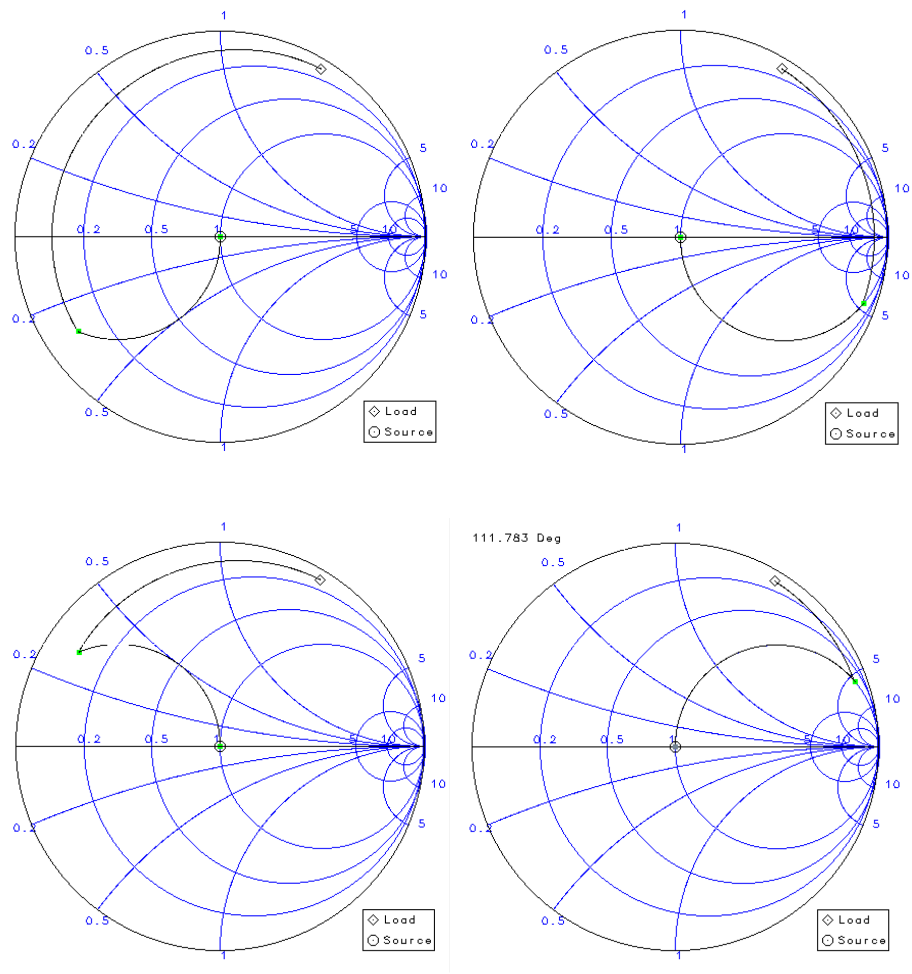
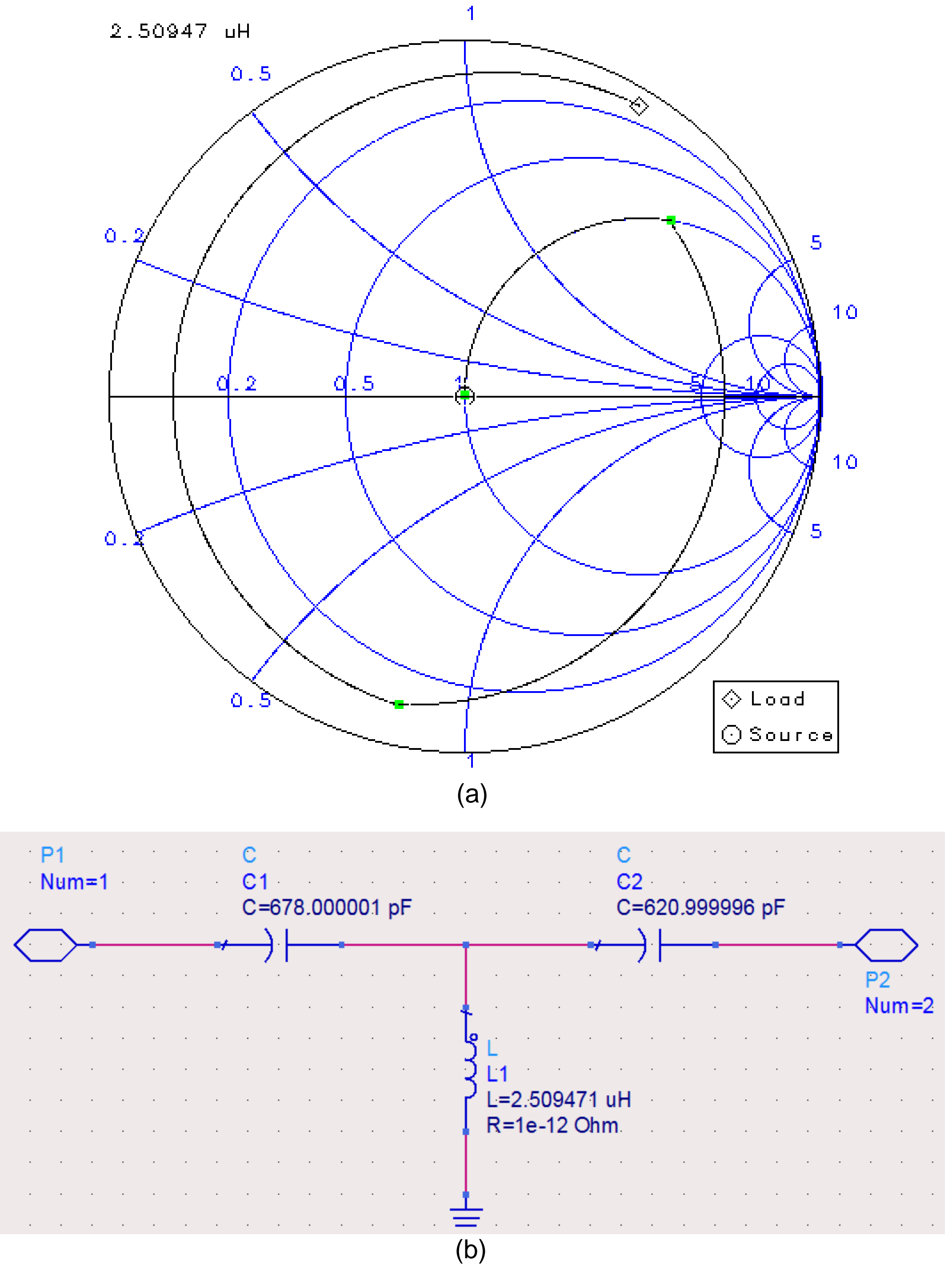


Figure 6-5: Paths in the Smith Chart of the matching networks

The T-type matching network can be configured as shown in Figure 6-6.



(a)

(b)

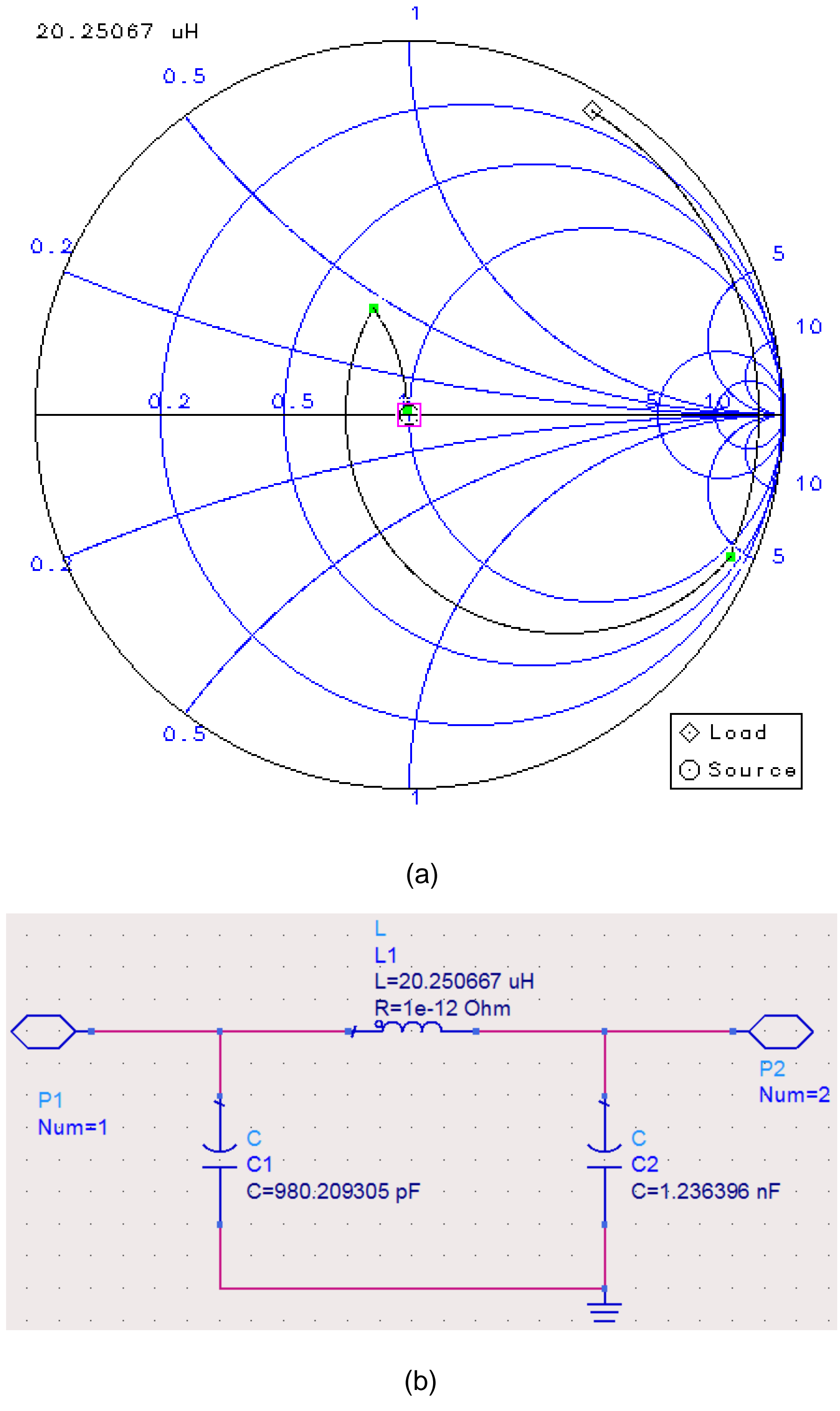
Figure 6-6: T-type matching network. (a) Paths in the Smith Chart; (b) Schematic of ADS circuit.

In order to verify the configuration, the impedance of P1 was calculated.

$$Z=48.05-j1.38\approx 50\ \Omega$$

The T-type matching network can be configured as shown in Figure 6-7.

$$Z=48.71+j0.207\approx 50\ \Omega$$



(a)

(b)

Figure 6-7: Pi-type matching network. (a) Paths in the Smith Chart; (b) Schematic of ADS circuit.

6.3. Test Result of the Matching Network

In order to use the common components in the lab and the tunable capacitor, the following T-type matching network was employed (Figure 6-8).

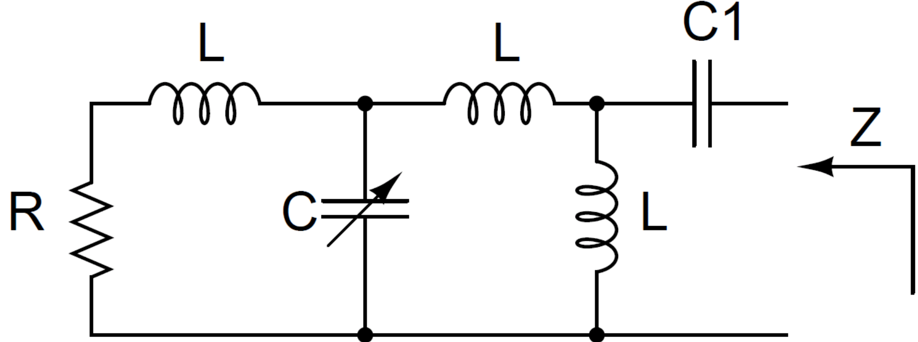


Figure 6-8: Circuit of matching network with a tunable capacitor

An HP 4195A network analyzer was used to measure the impedance Z.

R=50 Ω, f=10 MHz, Ct=10~20 pF, C2=12 pf, L1=L2=L3=10 nH

Table 6-1 provides the theoretical and measured results. Figure 6-9 shows the comparison of the real parts of impedances.

Table 6-1: Theoretical and measured results

Ct (pF)	Theoretical Z (Ω)	Measured Z (Ω)
10	10.23-j870	13.0-j609
12	11.86-j860	14.95-j606
15	15.15-j840	19.51-j588.8
20	24.68-j793.02	30.24-j556.2

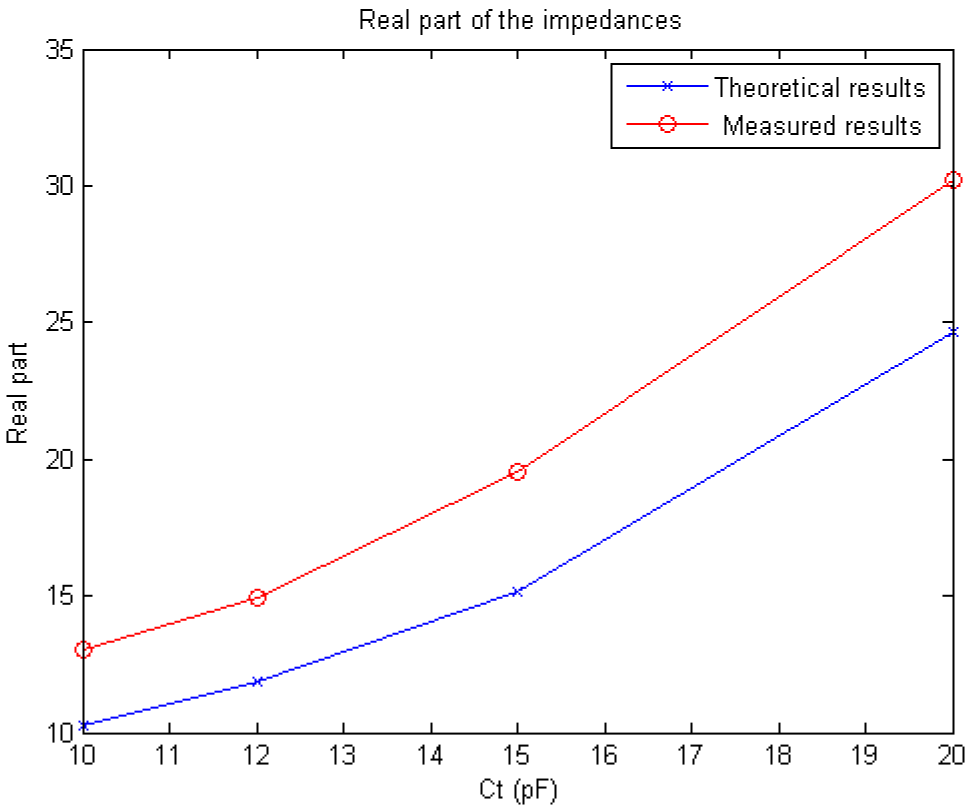


Figure 6-9: Comparison of the real part of the impedances with tunable capacitor changing from 10 pF to 20 pF

Figure 6-10 shows the comparison of the imaginary parts of impedances.

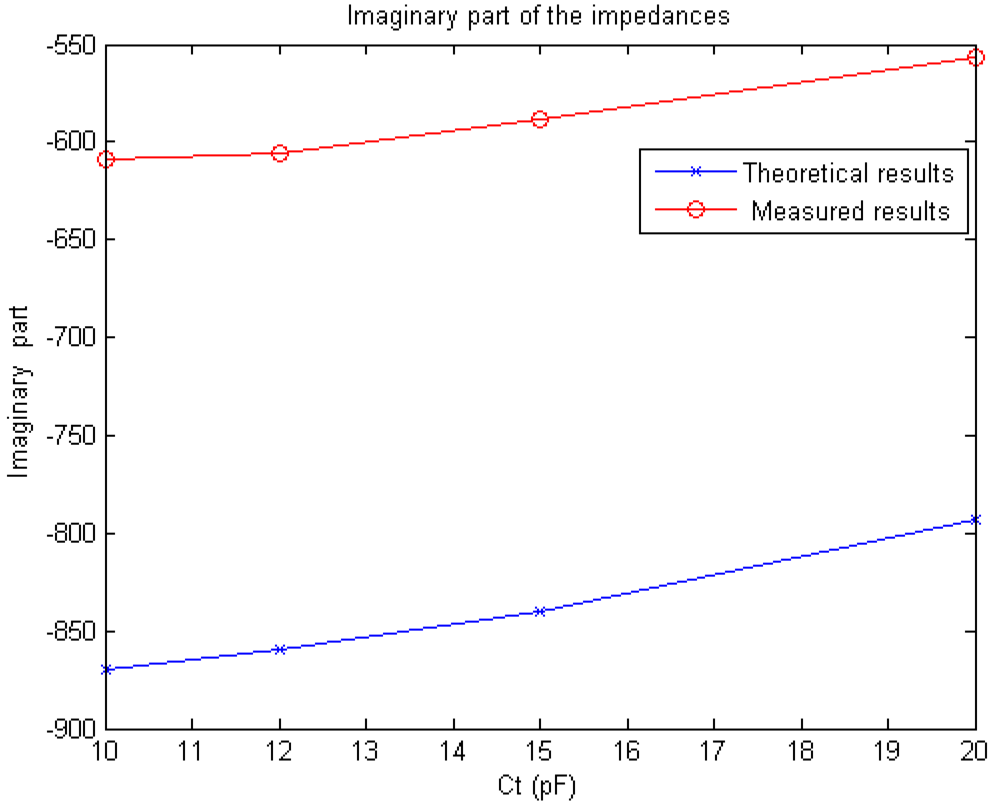


Figure 6-10: Comparison of the imaginary part of the impedances with tunable capacitor changing from 10 pF to 20 pF

The measured results were slightly larger than the theoretical results. The percentage difference can be calculated between a theoretical value and an experimental value by using the formula below:

$$\text{Percentage difference} = 100\frac{|theoretical - experimental|}{theoretical}\ \%$$

The percentage difference of each set of the real part was between 21.3% and 28.8%. For the imaginary part of the impedances, the percentage difference of each set was between 29.5% and 31.1%. The trends of the change were also the same. The results met the expectation. Therefore, the performance of T-type matching network was verified.

The tunable capacitor was then placed for testing in the matching network.

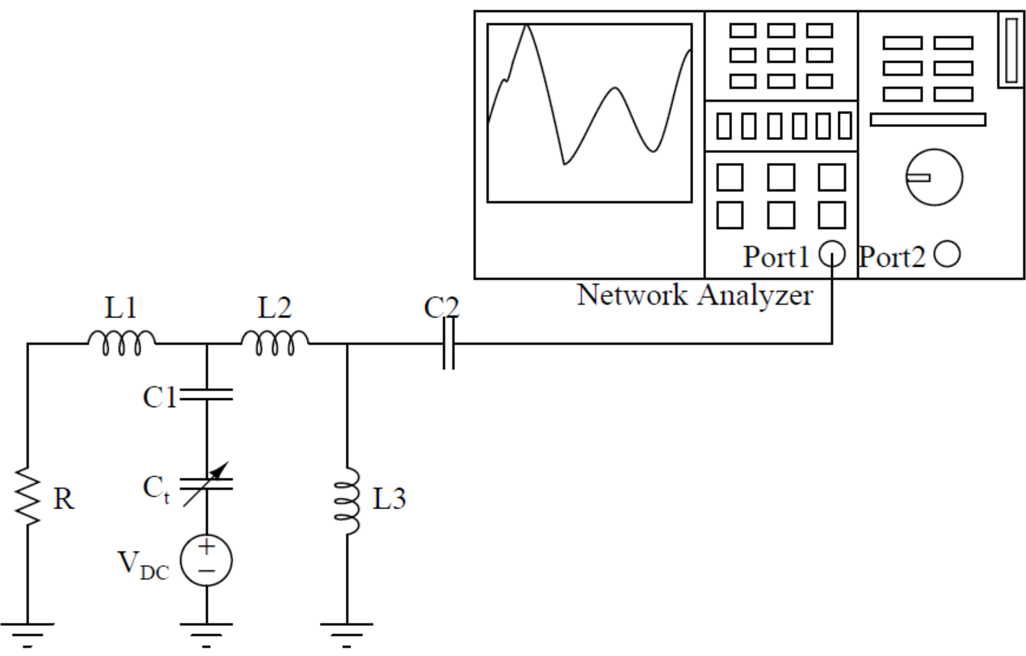


Figure 6-11: Set up of testing the matching network with a tunable capacitor

R is the impedance of PLC. C1 is a high voltage capacitor used to protect the circuit. Here C1=100 nF with maximum voltage 250 V. C_t is the tunable capacitor in series with C1. Since it is much smaller than C1, most of the applied voltage is on the tunable capacitor. VDC is the actuation voltage. In order to match inductive impedance, another capacitor is added.

When the voltage VDC changes, the capacitance changes, affecting the measured impedance. Table 6-2 shows the test results of the matching network with the tunable capacitor.

Table 6-2: Test results of the matching network with a tunable capacitor

Voltage (V)	0	10	20	30	40	50
Z (Ω)	84.7540-j150.652	85.5089-j149.474	85.8739-j150.313	88.3013-j154.420	92.0652-j101.494	94.0117-j174.764
	84.7686-j150.478	85.5377-j151.519	87.7355-j153.895	89.8392-j157.716	92.9054-j166.853	

Figure 6-12 shows the change of the real part of the impedances. The difference was relatively small. The stress of the membrane should be the reason of the hysteresis. The results are repeatable.

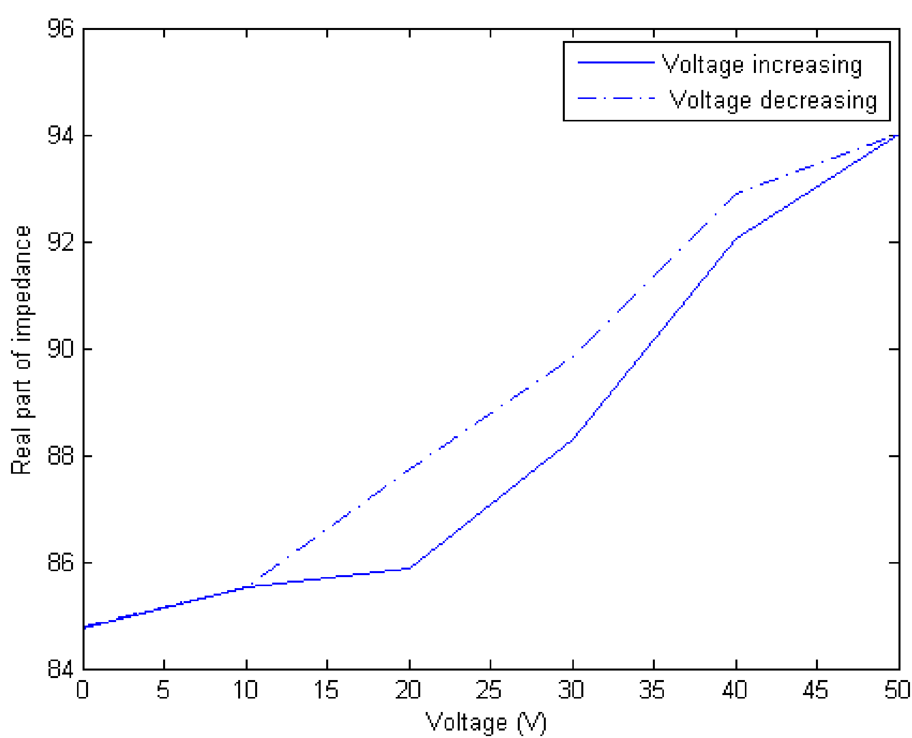


Figure 6-12: Change of the real part of the impedances

Chapter 7. Conclusion and Future work

The availability of power line makes PLC a promising solution. PLC Technology allows the use of the existing and widespread power distribution infrastructure to provide high-speed networking capabilities along with other benefits. However, the impedance mismatch in the interface of power line and the load leads to high attenuation. Due to the varying impedance in the PLC system, the maximum power transfer needs the impedance matching network between the power line and the load. The integrated circuits can perform the impedance matching electronically with the help of active inductors as well as varactors. Compared with the electronical solutions, MEMS devices have the advantages of small size, light weight, low power consumption, good durability, low cost and stable performance. The tunable MEMS devices were widely used in the impedance matching networks.

In this thesis, the design, fabrication, and test results of tunable inductors and capacitors were discussed.

Tunable inductors on PCB were fabricated and tested. They were tested with four films with different electrical resistance and permeability. The results were calculated under the help of Matlab code. The results were explained.

On the other hand, the tunable capacitors on glass wafer were also designed and tested. Basically, glass wafer was used. Metal was deposited and patterned as the electrode. Negative photoresist SU-8 was chosen to form the gap between the metal and movable membrane. Polyimide film was attached to the SU-8 structural layer to form the moving membrane. Based on the requirement, a T-type of matching network with tunable capacitor was build and tested.

This work has demonstrated that the impedance matching network can work properly for the designated environment. The proposed impedance matching network

adjusts the impedance for a given centre frequency through changing the applied voltage of the tunable capacitor. The performance results have demonstrated the effectiveness of the network. With this matching network, the load of power line communication can match the source and achieve the maximum power transfer.

In this work, the theoretical deflection of the membrane is based on the parameters of polyimide. Since the membrane in the device was covered with a thin layer of aluminum, the effect of the aluminum layer can be taken into consideration when further exploring the deflection.

In the future work, the expanded networks can be designed to cover larger area of the impedances in the Smith Chart. Based on this T-type matching network, more components can be added into the circuit to form a matching network according to the requirements. Furthermore, the characterization of the PLC can be performed. This impedance matching network can be place in the vehicle and tested. Besides, new methods for the moving membranes can be investigated to suit higher frequency.

References

[1] Yousuf, M.S.; El-Shafei, M., "Power Line Communications: An Overview - Part I," in Innovations in Information Technology, 2007. IIT '07. 4th International Conference on , vol., no., pp.218-222, 18-20 Nov. 2007

[2] Dange, H.V.; Gondi, V.K., "Powerline Communication Based Home Automation and Electricity Distribution System," in Process Automation, Control and Computing (PACC), 2011 International Conference on , vol., no., pp.1-6, 20-22 July 2011

[3] Ferreira, H.C.; Grove, H.M.; Hooijen, O.; Han Vinck, A.J., "Power line communications: an overview," in AFRICON, 1996., IEEE AFRICON 4th , vol.2, no., pp.558-563 vol.2, 24-27 Sep 1996

[4] Kim, C.J.; Chouikha, M.F., "Attenuation characteristics of high rate home-networking PLC signals," in Power Delivery, IEEE Transactions on , vol.17, no.4, pp.945-950, Oct 2002

[5] Gouret, W.; Nouvel, F.; El-Zein, G., "Powerline Communication on Automotive Network," in Vehicular Technology Conference, 2007. VTC2007-Spring. IEEE 65th , vol., no., pp.2545-2549, 22-25 April 2007

[6] David M. Pozar. Wiley: Microwave Engineering, 4th Edition. New York: John Wiley & Sons, 2001. Print.

[7] Taherinejad, N.; Lampe, L.; Mirabbasi, S., "Adaptive impedance matching for Vehicular Power Line Communication systems," in Power Line Communications and its Applications (ISPLC), 2014 18th IEEE International Symposium on , vol., no., pp.214-219, March 30 2014-April 2 2014

[8] Rahola, J., "Power Waves and Conjugate Matching," in Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.55, no.1, pp.92-96, Jan. 2008

[9] Hong-Teuk Kim; Sanghwa Jung; Kyungteh Kang; Jae-Hyoung Park; Yong-Kweon Kim; Youngwoo Kwon, "Low-loss analog and digital micromachined impedance tuners at the Ka-band," in *Microwave Theory and Techniques, IEEE Transactions on* , vol.49, no.12, pp.2394-2400, Dec 2001

[10] Vähä-Heikkilä, T.; Rebeiz, G.M., "A 20-50 GHz reconfigurable matching network for power amplifier applications," in Microwave Symposium Digest, 2004 IEEE MTT-S International , vol.2, no., pp.717-720 Vol.2, 6-11 June 2004

[11] Qizheng Gu; Morris, A.S., "A New Method for Matching Network Adaptive Control," in Microwave Theory and Techniques, IEEE Transactions on , vol.61, no.1, pp.587-595, Jan. 2013

[12] Domingue, F., Fouladi, S.; Mansour, R.R., "A reconfigurable impedance matching network using dual-beam MEMS switches for an extended operating frequency range," in Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International , vol., no., pp.1552-1555, 23-28 May 2010

[13] Fei Yuan. CMOS Active Inductors and Transformers. Springer US: Springer, 2008. Print.

[14] Santosh Vema Krishnamurthy, Kamal El-Sankary, and Ezz El-Masry, “Noise-Cancelling CMOS Active Inductor and Its Application in RF Band-Pass Filter Design,” International Journal of Microwave Science and Technology, vol. 2010, Article ID 980957, 8 pages, 2010

[15] Egidio Ragonese, Angelo Scuderi, Tonio Biondi, Giuseppe Palmisano, Integrated Inductors and Transformers: Characterization, Design and Modeling for RF and MM-Wave Applications, Boca Raton: Auerbach Publications, 2010. Print.

[16] El Gmati, I., P. Calmon, A. Boukabache, P. Pons, H. Boussetta, M.A. Kallala, K. Besbes, Liquid RF MEMS variable inductor, Procedia Engineering, Volume 5, 2010, Pages 1380-1383, ISSN 1877-7058, http://dx.doi.org/10.1016/j.proeng.2010.09.372.

[17] Gmati, Boussetta, H.; Kallala, M.A.; Besbes, K., "Wide-range RF MEMS variable inductor using micro pump actuator," in Signals, Circuits and Systems, 2008. SCS 2008. 2nd International Conference on, vol., no., pp.1-4, 7-9 Nov. 2008.

[18] El Bakkali, Francis Chan Wai Po, Emeric de Foucauld, Bernard Viala, Jean-Philippe Michel, Design of a RF matching network based on a new tunable inductor concept, Microelectronics Journal, Volume 42, Issue 1, January 2011, Pages 233-238, ISSN 0026-2692, http://dx.doi.org/10.1016/j.mejo.2010.08.004.

[19] Sarkar, N., Yan, D.; Horne, E.; Lu, H.; Ellis, M.; Lee, J.B.; Mansour, R.; Nallani, A.; Skidmore, G., "Microassembled tunable MEMS inductor," in Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on , vol., no., pp.183-186, 30 Jan.-3 Feb. 2005

[20] Shih, W. P., et al. (2004). Tunable solenoid microinductors utilizing Permalloy electro-thermal vibromotors. Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS).

[21] Tassetti, C.-M.; Lissorgues, G.; Gilles, J.P., "Tunable RF MEMS microinductors for future communication systems," in Microwave and Optoelectronics Conference, 2003. IMOC 2003. Proceedings of the 2003 SBMO/IEEE MTT-S International , vol.1, no., pp.541-545 vol.1, 20-23 Sept. 2003

[22] Imed, Z.-E.-A., et al. (2005). "Tunable radio frequency MEMS inductors with thermal bimorph actuators." Journal of Micromechanics and Microengineering 15(11): 2063.

[23] Sugawara, H.; Ito, H.; Okada, K.; Itoi, K.; Sato, M.; Abe, H.; Ito, T.; Masu, K., "High-Q variable inductor using redistributed layers for Si RF circuits," in Silicon Monolithic Integrated Circuits in RF Systems, 2004. Digest of Papers. 2004 Topical Meeting on , vol., no., pp.187-190, 8-10 Sept. 2004

[24] Okada, K.; Sugawara, H.; Ito, H.; Itoi, K.; Sato, M.; Abe, H.; Ito, T.; Masu, K., "On-Chip High- Q Variable Inductor Using Wafer-Level Chip-Scale Package Technology," in Electron Devices, IEEE Transactions on , vol.53, no.9, pp.2401-2406, Sept. 2006

[25] Stuart M. Wentworth, Fundamentals of Electromagnetics with Engineering Applications, Hoboken, NJ: John Wiley & Sons, 2006. Print.

[26] Colin Stevens, "Detection and Mitigation of Electrostatic Pull-in Instability in MEMS Parallel Plate Actuators," PhD dissertation, PhD dissertation, Department of Electrical and Computer Engineering, Auburn University, Auburn, AL, USA, 2013.

[27] Rijks, T. G. S. M; van Beek, J.T.M.; Steeneken, P.G.; Ulenaers, M.J.E.; De Coster, J.; Puers, R., "RF MEMS tunable capacitors with large tuning ratio," in Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS) , vol., no., pp.777-780, 2004

[28] Rahimi, M.; Jamuar, S.S.; Hamidon, M.N.; Ahmad, M.R.; Mousavi, S.A., "The design and simulation of an optimized MEMS varactor with high q factor for RF circuits," in Semiconductor Electronics, 2008. ICSE 2008. IEEE International Conference on , vol., no., pp.161-165, 25-27 Nov. 2008

[29] Fouladi, S.; Bakri-Kassem, M.; Mansour, R.R., "An Integrated Tunable Band-Pass Filter Using MEMS Parallel-Plate Variable Capacitors Implemented with 0.35µm CMOS Technology," in Microwave Symposium, 2007. IEEE/MTT-S International , vol., no., pp.505-508, 3-8 June 2007

[30] Bakri-Kassem, M.; "Novel High-Q MEMS Curled-Plate Variable Capacitors Fabricated in 0.35-µm CMOS Technology," in Microwave Theory and Techniques, IEEE Transactions on , vol.56, no.2, pp.530-541, Feb. 2008

[31] Marcaccioli, L.; Montori, S.; Gatti, R.V.; Chiuppesi, E.; Farinelli, P.; Sorrentino, R., "RF MEMS-reconfigurable architectures for very large reflectarray antennas," in Microwave Conference, 2009. APMC 2009. Asia Pacific , vol., no., pp.766-769, 7-10 Dec. 2009

[32] Tao Yang; Yi Lin; Xianji Tan; Yuehui Feng, "Modeling and analysis of piezoelectric bimorph cantilever used for vibration energy harvesting," in Control and

Automation (ICCA), 2010 8th IEEE International Conference on , vol., no., pp.1783-1788, 9-11 June 2010

[33] Safaie, B.K.; Shamshirsaz, M.; Bahrami, M., "Robust design under uncertainties of electro-thermal microactuator," in Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), 2014 Symposium on , vol., no., pp.1-6, 1-4 April 2014

[34] Nemirovsky, Y.; Zelniker, I.; Degani, O.; Sarusi, G., "A methodology and model for the pull-in parameters of magnetostatic actuators," in Microelectromechanical Systems, Journal of , vol.14, no.6, pp.1253-1264, Dec. 2005

[35] Richard C. Jaeger. Introduction to Microelectronic Fabrication (2nd Edition). New Jersey: Prentice Hall, 2001. Print.

[36] Reza Ghodssi, Pinyen Lin, MEMS Materials and Processes Handbook, Berlin: Springer, 2011. Print.

[37] Ciacchi, M.; Eder, H.; Hirscher, H., "Evaporation vs. Sputtering of metal layers on the Backside of Silicon wafers," in Advanced Semiconductor Manufacturing Conference, 2006. ASMC 2006. The 17th Annual SEMI/IEEE , vol., no., pp.99-103, 22-24 May 2006

[38] San Ping Jiang, Pei Kang Shen. Nanostructured and Advanced Materials for Fuel Cells. Florida: CRC Press, 2013. Print.

[39] Howland, F.L.; Poole, K.M., "Device photolithography: An overview of the new mask-making system," in Bell System Technical Journal, The , vol.49, no.9, pp.1997-2009, Nov. 1970

[40] MicroChem , "SU-8 3000 Permanent Epoxy Negative Photoresist," SU-8 3000 data sheet, Feb.2002

[41] PCB Copper Weight / Thickness Chart. (2013) Retrieved from http://baltimorehackerspace.com/2012/08/pcb-copper-weight-thickness-chart/

[42] Raymond A. Serway, Principles of Physics (2nd ed.). Fort Worth, Texas; London: Saunders College Pub, 1998. Print.

[43] Douglas Giancoli, Physics for Scientists and Engineers with Modern Physics (4th ed.). Upper Saddle River, New Jersey: Prentice Hall, 2009. Print.

[44] Matglas, "Magnetic Alloy 2714A (cobalt-based)", data sheet, ref:2714A04202011.

[45] Minhang Bao, Analysis and Design Principles of MEMS Devices, Amsterdam: Elsevier Science, 2005. Print.

[46] John Kuffel, Peter Kuffel, High Voltage Engineering Fundamentals, Oxford: Newnes, 2000. Print.

[47] Riley, Lewis A. Dielectrics. 1999-2000. Print.

[48] Chong-Yeun Park; Kwang-Hyun Jung; Won-Ho Choi, "Coupling circuitary for impedance adaptation in power line communications using VCGIC," in Power Line Communications and Its Applications, 2008. ISPLC 2008. IEEE International Symposium on , vol., no., pp.293-298, 2-4 April 2008

[49] Taherinejad, N.; Rosales, R.; Mirabbasi, S.; Lampe, L., "On the design of impedance matching circuits for vehicular power line communication systems," in *Power Line Communications and Its Applications (ISPLC), 2012 16th IEEE International Symposium on* , vol., no., pp.322-327, 27-30 March 2012

Appendix A.
Matlab Code to Calculate Inductance Values

```
function [ys,refit]= oneportfit(s,guess,lb,ub,dmbfileprefix)

global fhz;

% Obtain S and Y from input matrices

reysmea = s(:,2);

imysmea = s(:,3);

ys = reysmea + sqrt(-1)*imysmea;


fmeamin = min(fhz);

fmeamax = max(fhz);

fnew = fmeamin:3e4:fmeamax;

reys = interp1(fhz,reysmea,fnew);

imys = interp1(fhz,imysmea,fnew);


gs = guess;

%options=optimset('MaxFunEvals',10e9,'MaxIter',10e9,'TolFun',1e-10);

options = optimset('LargeScale','on');

lbs = [lb(1) lb(2) lb(3) lb(4)];

ysguess = [gs(1) gs(2) gs(3) gs(4)];
```

```
ubs = [ub(1) ub(2) ub(3) ub(4)];

for i = 1:200;
   func=@ysrefunc; % Imaginary function to be fit is ysrefunc.m
% Call lsqcurvefit for real part fitting;
[refit,reresnorm,reresidual,reexitflag,reoutput] = ...
lsqcurvefit(func,ysguess,fnew,reys,lbs,ubs,options);
func=@ysimfunc; % Imaginary function to be fit is ysimfunc.m
% Call lsqcurvefit for imaginary part fitting;
[ysguess,imresnorm,imresidual,imexitflag,imoutput] = ...
lsqcurvefit(func,refit,fnew,imys,lbs,ubs,options);
end % for i

s1=sprintf('\n##### Initial Ys real guess #####\n');
s2=sprintf('Lower limit [%6.3f %6.3f %6.3f %6.3f %6.3f]\n',lbs);
s3=sprintf('Guess [%6.3f %6.3f %6.3f %6.3f %6.3f]\n',ysguess);
s4=sprintf('Upper limit [%6.3f %6.3f %6.3f %6.3f %6.3f]\n',ubs);
disp(s1);disp(s2);disp(s3);disp(s4);
s1 = sprintf('\n############################\n');
s2 = sprintf('Ys real optimization output:');
s3 = sprintf('\n############################\n');
s4 = sprintf('Resnorm = %f\n',reresnorm);
s5 = sprintf('Exitflag = %f\n',reexitflag);
```

```
s6 = sprintf('Output = ');

disp(s1);disp(s2);disp(s3);disp(s4);disp(s5);disp(s6);disp(reoutput);


% fit=[R0,lambda,beta,Cf,Leff]

s1=sprintf('\n##### Initial Ys imaginary guess #####\n');

s2=sprintf('Lower limit [%6.3f %6.3f %6.3f %6.3f %6.3f]\n',lbs);

s3=sprintf('Guess [%6.3f %6.3f %6.3f %6.3f %6.3f]\n',refit);

s4=sprintf('Upper limit [%6.3f %6.3f %6.3f %6.3f %6.3f]\n',ubs);

disp(s1);disp(s2);disp(s3);disp(s4);

s1 = sprintf('\n####################################\n');

s2 = sprintf('Ys imaginary optimization output:');

s3 = sprintf('\n####################################\n');

s4 = sprintf('Resnorm = %f\n',imresnorm);

s5 = sprintf('Exitflag = %f\n',imexitflag);

s6 = sprintf('Output = ');

disp(s1);disp(s2);disp(s3);disp(s4);disp(s5);disp(s6);disp(imoutput);

disp(refit);

disp(ysguess);


s1 = sprintf('\n##### One-port inductor model #####\n');

s2 = sprintf('Rs = %6.4e\n',refit(1));

s3 = sprintf('Ls = %6.4e\n',refit(2));

s4 = sprintf('Cp = %6.4e\n',refit(3));
```

```
s5 = sprintf('Rp = %6.4e\n',refit(4));

disp(s1);disp(s3);disp(s2);disp(s4);disp(s5);

return;
```

Appendix B. Test Results for a Tunable Capacitor

The capacitance can be calculated based on the imaginary part of Y11. The voltage changed from 0 V to 130 V. It then decreased to -130 V and increased to 0 V. The schematic was shown in Figure 5-6.

#	V_{IN} (V)	$\mathrm{Im}(Y_{11})$ (Ohm)	C (pF)	#	V_{IN} (V)	$\mathrm{Im}(Y_{11})$ (Ohm)	C (pF)
1	0	0.167	13.29604	27	0	0.1696	13.50304
2	10	0.1672	13.31196	28	-10	0.168	13.37566
3	20	0.168	13.37566	29	-20	0.1678	13.35973
4	30	0.1695	13.49508	30	-30	0.1685	13.446
5	40	0.173	13.77374	31	-40	0.1706	13.58266
6	50	0.1764	14.04444	32	-50	0.1739	13.8454
7	60	0.1818	14.47437	33	-60	0.1781	14.17979
8	70	0.1978	15.74824	34	-70	0.189	15.04761
9	80	0.2051	16.32945	35	-80	0.2021	16.0906
10	90	0.2088	16.62403	36	-90	0.2086	16.60811
11	100	0.2108	16.78326	37	-100	0.2124	16.91065
12	110	0.2134	16.99027	38	-110	0.2178	17.34058
13	120	0.2193	17.46001	39	-120	0.2208	17.57943
14	130	0.222	17.67497	40	-130	0.2222	17.6909
15	120	0.2209	17.5874	41	-120	0.2211	17.60332
16	110	0.2197	17.49185	42	-110	0.22	17.51574
17	100	0.2188	17.4202	43	-100	0.2192	17.45205
18	90	0.2181	17.36447	44	-90	0.2181	17.36447
19	80	0.2172	17.29281	45	-80	0.2165	17.23708
20	70	0.2136	17.00619	46	-70	0.2134	16.99027
21	60	0.2098	16.70365	47	-60	0.2101	16.72753
22	50	0.2081	16.5683	48	-50	0.2073	16.5046
23	40	0.2051	16.32945	49	-40	0.1987	15.8199
24	30	0.1957	15.58105	50	-30	0.1934	15.39793
25	20	0.1792	14.26737	51	-20	0.1728	13.75782
26	10	0.173	13.77374	52	-10	0.1698	13.51897
				53	0	0.1674	13.32789