Employing Piezojunction Effect for Resonant Micro-Device Applications

by

Amin Rasouli

M.Sc., K.N. Toosi University of Technology, 2009
B.Sc., Shiraz University, 2005

Dissertation Submitted in Partial Fulfillment of the
Requirements for the Degree of
Doctor of Philosophy

in the
School of Mechatronic Systems Engineering
Faculty of Applied Sciences

SIMON FRASER UNIVERSITY

Spring 2016

Approval

Name:	**Amin Rasouli**
Degree:	**Doctor of Philosophy (Mechatronic Systems Engineering)**
Title:	***Employing Piezojunction Effect for Resonant Micro-Device Applications***
Examining Committee:	**Chair:** Dr. Woo Soo Kim Assistant Professor

Dr. Behraad Bahreyni
Senior Supervisor
Associate Professor

Dr. Marek J. Syrzycki
Supervisor
Professor

Dr. Ash M. Parameswaran
Supervisor
Professor

Dr. Glenn H. Chapman
Internal Examiner
Professor
School of Engineering Sciences

Dr. Boris Stoeber
External Examiner
Associate Professor
Electrical and Computer Engineering
The University of British Columbia

Date Defended/Approved: March 3, 2016

Abstract

This dissertation reports on the application of the piezojunction effect as a new mechanism for measurement of resonance frequency in silicon-based micro-systems. It has been known that mechanical stress can affect the electrical characteristics of diodes, transistors and electronic circuits. This phenomenon is recognized as piezojunction effect.

To explore the piezojunction effect as an effective detection mechanism in a micro-device, a micro-resonator structure is designed to employ the inherent mechanical amplification of displacements at resonance as an enabling platform. The proposed structure is capable of mechanically amplifying the sensing signal at the resonance frequency by its quality factor, which can be in the range of tens to hundreds of thousands. This amplified displacement makes the piezojunction effect a practical sensing method for resonator applications. In this technique, the sensing current is stemmed from the dependency of electrical characteristics of an embedded *p-n* junction to the periodic stress profiles inside the resonating body. The *p-n* junction is reverse-biased, therefore, due to low sensing current, the required power for detection of resonance is rather small.

To employ the piezojunction technique, the author has developed an in-house Silicon-On-Insulator (SOI) micro-machining process to fabricate the proof-of-concept micro-resonator and its embedded *p-n* junction. Fabricated resonators were packaged and experimentally tested to verify the feasibility of the design and to gauge the performance of the piezojunction mechanism for resonance sensing. The static and dynamic responses of the fabricated devices are experimentally verified. The extensional-mode frequency of the resonator was measured to be 7MHz with a mechanical quality factor of around 5,000. The required power consumption for this sensing mechanism was as low as 5nW. The experimental verifications demonstrate that the piezojunction effect is a promising addition to existing detection techniques in resonance-based applications, where small chip area, integration, and power consumption are key requirements.

Keywords: Micro-resonators, Piezojunction Effect, *P-N* Junction, Low-Power Sensing, Micro-machining.

Dedication

To my loved ones

Acknowledgments

First and foremost, I would like to express my deepest gratitude and respect to my advisor, Dr. Behraad Bahreyni, for his insightful guidance and continuous support throughout my Ph.D. program. I feel very fortunate to have had him as my mentor and advisor; He has been very generous with his knowledge and time and assisted me in each step of my research towards the completion of this dissertation. Through all the meetings I have had with him, he has always provided me with great ideas and I am very thankful for that. This thesis would not have been completed without his vision, advice and patient supervision.

I would like to extend my most sincere thanks to my thesis committee members, Professors Marek Syrzycki, Ash Parameswaran and Glenn Chapman for agreeing to be members of the committee, and read this dissertation and give me their invaluable feedback on my work.

I would like to thank Professor Syrzycki for his priceless comments, and technical recommendations to improve this dissertation. He has been always available and willing to have a discussion with me, even in his busiest days. He generously granted me the access to his labs, Deep Submicron CMOS Technology Laboratory and Micro-Systems Characterization Laboratory, for testing and characterization of my devices. I also learned a lot about analog and digital circuits as his student and teaching assistant. I am very much grateful to him for his invaluable support and guidance throughout my doctorate studies.

I have been sincerely indebted to Professor Ash Parameswaran for his kindness, guidance and support since the first day of starting my doctorate journey. He has been a great advisor, strong motivator, and a great inspiration to my research and teaching. It has been a great honor and privilege for me to know and work with him. He has been my role model as a scholar researcher, passionate mentor and excellent instructor. His exceptional passion for engaging teaching and innovative research has been an ongoing inspiration.

I extend my sincere gratitude to Professor Glenn Chapman for reading my thesis and invaluable feedback. I feel very fortunate to have had the opportunity to work with him as his teaching assistant for his micro-fabrication course, and to have had benefitted from his

indispensable technical knowledge of fundamental semiconductor physics and micro-fabrication. Indeed, my gratitude to him cannot be expressed in a few words.

Many thanks to senior members of the Institute of Micro-machine and Micro-fabrication Research (IMMR) cleanroom, Dr. Kourosh Khosraviani, Jamal Bahari and Dr. Sae Won Lee for training me on the cleanroom equipment and sharing their knowledge of micro-fabrication and recipe development with me. I would like to thank Mr. Andras Szigeti for his excellent services at IMMR facility and bearing patiently with my demanding technical requests. I would like to thank staff and technicians of Nanofabrication and Nanoimaging facilities at the 4D LABS for privileging me the access to their state-of-the-art equipment and their helpful technical discussions.

I would like to acknowledge the previous and current members of Integrated Multi-Transducer Systems (IMuTS) Laboratory with whom I have shared wonderful moments and memories. Special recognition must go to Dr. Sadegh Hajhashemi, Dr. Mona Aezinia, and Kelsey Corrigan for their friendship, companionship and helpful discussions. I would like to thank Mr. Zain Khanzada for providing a pleasant and organized characterization environment at IMuTS Lab. I am thankful to all my friends and colleagues at SFU for their friendship and support.

I would like to thank Natural Sciences and Engineering Research Council (NSERC) of Canada, CMC Micro-systems and Simon Fraser University for their financial support and funding of my research.

At last but certainly not least, I am deeply indebted to my dear parents, Manijeh and Jamshid, and my brothers, Shahram and Mehdi, for their unconditional love, constant support and endless encouragement in my life and through my graduate studies.

Table of Contents

List of Tables

List of Figures

List of Acronyms

AC	Alternative Current
BAW	Bulk Acoustic Wave
BOX	Buried Oxide Layer
CMOS	Complementary Metal-Oxide-Semiconductor
dB	Decibel
DC	Direct Current
DRIE	Deep Reactive Ion Etching
FBAR	Film Bulk Acoustic Resonator
FEA	Finite Element Analysis
HF	Hydrofluoric acid
IC	Integrated Circuit
IR	Infrared
LPCVD	Low-Pressure Chemical Vapor Deposition
LTO	Low Temperature Oxide
MEMS	Micro-Electro-Mechanical Systems
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
Si	Silicon
SIMS	Secondary Ion Mass Spectrometry
SiO_2	Silicon Dioxide
SOI	Silicon-On-Insulator
VNA	Vector Network Analyzer

List of Symbols

E	Young's modulus
Q	Mechanical quality factor
T	Temperature
g	Transduction gap
q	Elementary charge
t	Thickness
I_{diff}	Diffusion current
I_{gen}	Generation current
I_{rec}	Recombination current
K_{eff}	Effective spring constant
L_m	Motional inductance
L_n	Diffusion length of electrons
L_p	Diffusion length of holes
M_{eff}	Effective mass
N_A	Concentration of acceptor impurities
N_D	Concentration of donor impurities
N_c	Effective density of states at the edge of conduction band
N_v	Effective density of states at the edge of valence band
R_m	Motional resistance
V_P	Polarizing voltage
V_R	Reverse bias voltage
V_T	Thermal voltage
V_j	Applied junction voltage
V_{sub}	Applied substrate voltage
W_j	Depletion region width
b_{eff}	Equivalent effective damping
f_{res}	Resonant frequency
k_B	Boltzmann's constant
n_i	Intrinsic carrier concentration
n_p	Equilibrium concentration of electrons in p-type silicon

p_n	Equilibrium concentration of holes in n-type silicon
v_{ac}	Alternative voltage
x_j	Junction depth
η_i	Electro-mechanical coupling factor at input port
η_o	Electro-mechanical coupling factor at output port
η_{oe}	Electrostatic electromechanical coupling factor
η_{op}	Piezojunction electromechanical coupling factor
π_l	Longitudinal piezoresistive coefficient
π_t	Transverse piezoresistive coefficient
σ_l	Longitudinal stress
σ_t	Transverse stress
σ_{xx}	Mechanical stress along x
τ_{n0}	Life time of electrons
τ_{p0}	Life time of holes
ω_o	Natural angular frequency
ϵ_o	Permittivity of free space
ϵ_r	Relative permittivity
ε	Mechanical strain
ρ	Density
σ	Mechanical stress
γ_1	First-order stress sensitivity
γ_2	Second-order stress sensitivity

Chapter 1. Introduction

1.1. Background

Micro-electromechanical systems (MEMS) technology has revolutionized the field of conventional hybrid transducers in the past decades. Advancements in this field are motivated by improvements in the micro-machining techniques that originally were borrowed from the integrated circuit (IC) industry. Surface and bulk micro-machining techniques can be used to fabricate complex structures, devices and systems on the scale of microns. Surface micro-machining is conventionally achieved through the deposition and patterning of thin films on top a substrate wafer. On the other hand, bulk micro-machining is usually accomplished through the selective removal of a handle wafer to define the structures inside the wafer [1].

Many state-of-the-art processes are exclusively developed for fabrication of MEMS devices. Micro-machined transducers, which are fabricated with IC compatible processes, create the building blocks for integrated micro-systems. Batch fabrication of these devices with existing IC technology offers advantages such as, manufacturing cost reduction, high precision and added functionality for system-on-a-chip (SOC) applications. MEMS transducers are micro-devices that convert one type of energy into another by means of a wide variety of transduction mechanisms. These transduction mechanisms enable the conversion of the physical signals from one form of energy to another in micro-sensors and micro-actuators. Micro-sensors often convert the physical signals into electrical signals, which can be processed by electronic interfaces. On the other hand, micro-actuators transform the electrical stimuli into physical signals. These sensing and actuating mechanisms can be merged with electronic circuits to produce integrated micro-systems.

A growing interest for the potential influence of MEMS has provoked many efforts to commercialize a variety of new MEMS products. Numerous micro-machined transducers have been developed so far for a wide range of applications such as stress measurements [2], inertial sensors [3], micro-fluidic systems [4], biomedical analysis systems [5], optical switches [6], and RF devices [7].

Among these devices, mechanical micro-resonators are particularly attractive for precision measurements because of their high precision and high sensitivity to physical and chemical signals. Resonant micro-devices promise superior solutions for a wide range of sensing, timing and signal processing applications. Advancements in this field are motivated by potential applications in batch-fabricated integrated silicon micro-resonators. These devices promise new capabilities, as well as improved performance over their conventional hybrid counterparts.

1.2. Motivation and Objectives

The motivation behind this research is to introduce an alternative solution for sensing of vibrations in micro-electromechanical (MEM) resonators. This research investigates a transduction method that enables a combination of electrostatic drive with readout through the piezojunction effect in silicon micro-resonators to efficiently use the benefits of both these techniques. Electrostatic actuation is selected because of its straightforward fabrication, ease of design and low power consumption. The mechanical motion of a mechanical resonator is then detected through the variation in the electrical characteristics of the *p-n* junctions within the vibrating structure due to the piezojunction effect. The use of piezojunction effect is appealing for two reasons: 1) the power consumption of the resonator can be reduced by orders of magnitude [8], and 2) the device size can be reduced [9]. Therefore, employment of the piezojunction effect can be a promising addition to existing detection techniques in applications, where small chip area, integration, and power consumption are key requirements. However, the application of piezojunction effect in micro-devices depends on developing designs and optimized approaches, which can improve the sensitivity of this mechanism to stress.

This work proposes a micro-device in which we employ the inherent mechanical amplification of displacements at resonance as an enabling platform to utilize the piezojunction effect. The proposed structure is capable of mechanically amplifying the sensed signal at the resonance frequency by its quality factor, which can be in the range of tens to hundreds of thousands. This amplified displacement makes the piezojunction effect the practical sensing method for resonator applications. To employ the piezojunction effect in a micro-resonator, a bulk-mode resonator is chosen because of the potential for a higher Q-factor. A simple design of a beam resonator with an embedded *p-n* junction is illustrated in Figure 1-1(a). By applying an alternating electrostatic force through the input electrodes, the resonator vibrates in its extensional bulk-mode of vibration along its length. Expansion and contraction of the beam generate a stress profile at the location of the junction, which in turn can be used for detection of the resonance frequency via the piezojunction effect.

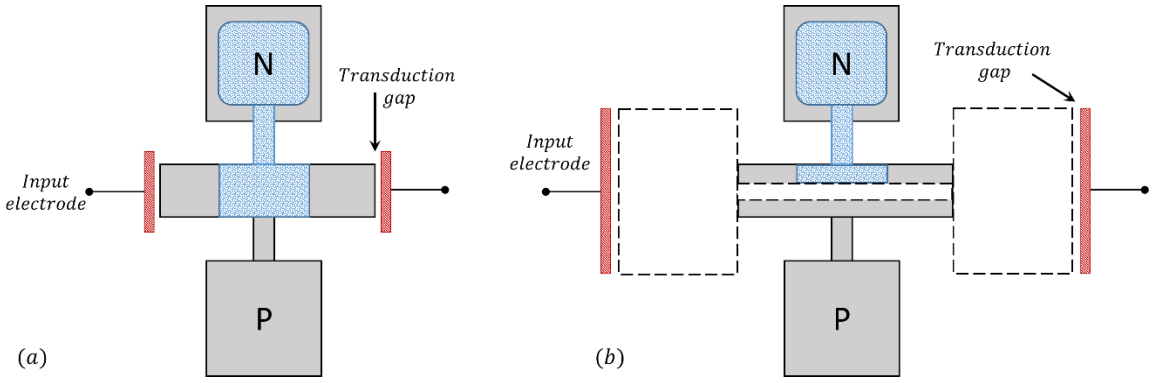

Figure 1-1: Schematic view of a resonator with an embedded *p-n* junction: (a) beam resonator and (b) dog-bone structure.

To provide an effective design, both actuation and sensing mechanisms should be optimized. Larger actuation area and smaller gap size are required for a higher electrostatic transduction coupling at the input ports. Also, piezojunction sensors are positioned at locations with high stresses in order to effectively use this technique. Considering these requirements, we are proposing the so-called dog-bone structure that is shown in Figure 1-1(b) to be used as a demonstration for the purposes of this dissertation. Two head pieces are added at both ends of the beam resonator to improve the electrostatic transduction at the input. In addition, a slit is made in the beam to amplify the input stress levels mechanically by using the stress concentration techniques.

Moreover, addition of this slit provides electrical access to both ends of the beam in reverse-biased condition when the diode is fully depleted.

The next step was to implement and fabricate the designed structure. There are no standard MEMS foundry processes that offer a doping step in their process flows. Therefore, the author developed a Silicon-On-Insulator micro-machining process with capability of adding doping to fabricate the prototype micro-devices of this work. This process provides means for integration of embedded *p-n* junctions with low leakage currents in the body of resonating devices. After successful fabrication of the designed micro-devices, precise characterization techniques and experimental test setups are used to verify and evaluate the operation of fabricated devices. Physical working principles of the resonator are discussed. An equivalent electrical representation is developed for this type of resonator. The resonator structure is then analyzed with respect to its static and dynamic characteristics. In this technique, the sensing current depends on the dependency of electrical characteristics of an embedded *p-n* junction to the periodic stress profiles inside the resonating body. The *p-n* junction is reverse-biased, therefore, due to low sensing current, the required power for detection of resonance is rather small. Experimental results confirm the effectiveness of application of this new technique in micro-resonators. It is validated that the combination of electrostatic actuation and piezojunction sensing, provides a low power transduction mechanism for MEM resonators.

1.3. Thesis outline

The dissertation is divided into seven chapters as follows:

Chapter 1 provides a general introductory description of background knowledge and motivation of this thesis work.

Chapter 2 discusses various transduction mechanisms which have been used in micro-machined transducers. Instances of application of such transductions are provided and these techniques are compared.

Chapter 3 focuses on micro-resonators and their application in timing, sensing and mechanical signal processing applications. Principles of resonance are discussed and typical modes of vibrations are presented and exemplified.

Chapter 4 of this dissertation explains a step-by-step description of the Silicon-On-Insulator (SOI) micro-machining process which is developed by the author to fabricate the prototype micro-devices. Detailed process steps are included in Appendix A of this dissertation.

Chapter 5 demonstrates the design and analysis of fabricated micro-resonator. Principles of its transduction mechanisms are elucidated and the piezojunction mechanism for sensing of resonance in such device is analyzed.

Chapter 6 provides the experimental test setup, electrical characterization of the SOI resonator as well as the frequency response of the resonator as a validation of the concept followed by experimental results and discussions.

Chapter 7 concludes the dissertation by revisiting the challenges of employing piezojunction mechanism in micro-resonators and by summarizing the fundamental contributions and achievements of the research. Also, it presents perspectives for future investigations and research.

Chapter 2. Transduction at micro-scales

The basic principle for both electromechanical sensing and actuation is the transduction of energy. There are two fundamental types of physical transduction mechanisms: The first category is based on the actions between multiple objects at a distance, and the second group exploits the deformations resulted from the inherent material properties [10]. The first category includes electrostatic and electromagnetic transductions while the second one includes transductions such as piezoelectric phenomenon and shape memory alloys [10].

In micro-systems a range of transduction techniques are used, including electrostatic forces [11], piezoelectricity [12], piezoresistivity [13], thermal [14], optical [15], magnetic [16]. Among these mechanisms, the most widely used transduction mechanisms in resonant micro-devices are electrostatic and piezoelectric methods. Following sections of this chapter present an overview of these mechanisms and piezojunction effect. Each section provides a brief overview of the mechanism principle followed by the implemented instances.

2.1. Electrostatic transduction

Electrostatic transduction in MEMS applications is based on the basic principle that two parallel plates with opposite charges will attract each other. Figure 2-1 demonstrates a simple parallel plate capacitor with a separation (g), and an overlap area (A). The capacitance of a parallel plate with a fixed electrode and a movable electrode is given by

$$C = \epsilon_0 \frac{A}{g - x} \tag{2.1}$$

where ϵ_0 and x are the permittivity of vacuum and the displacement along the x-axis, respectively.

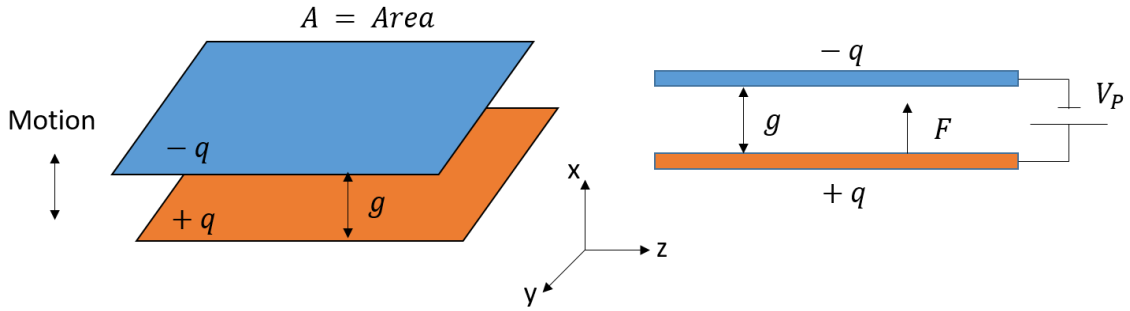

Figure 2-1: Schematic of a parallel plate capacitor with illustration of positive charge (+q) and negative charge (-q) on opposite plates when connected to a voltage source.

When a voltage source is connected to the plates, one electrode collects a positive charge (+q) while the other electrode acquires a negative charge (-q), resulting in an attractive electrostatic force between the two plates.

Electrostatic micro-resonators can be considered as a parallel plate capacitor system in which one plate is fixed and the other plate is attached to a spring, forming a spring-mass-damper system, which is essentially a resonator (Figure 2-2). By applying an input voltage signal comprised of a polarization DC bias (V_P), and an AC signal (v_{ac}), to the system, an alternating electrostatic force will be generated between the resonator body and the electrode plates. This electrostatic force can be written as:

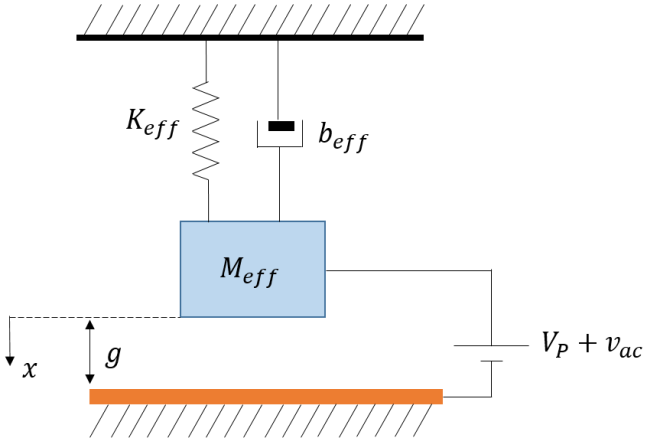

Figure 2-2: Electrostatic transduction and spring-mass-damper representation of a micro-resonator.

$$F = \frac{1}{2}\frac{\partial C}{\partial x}(V_P + v_{ac})^2 \tag{2.2}$$

where $\frac{\partial C}{\partial x}$ is the change in electrode-to-resonator overlap capacitance per displacement. Assuming the time-varying displacement x is much smaller than the gap spacing *(g)*, such that the nonlinearity can be ignored for now, the force component in (2.2) that has a frequency part the same as v_{ac} is given by:

$$F_{\omega_0} \cong V_P v_{ac} \frac{A\epsilon_r\epsilon_0}{g^2} \tag{2.3}$$

where ϵ_r is the relative permittivity of the electrode-to-resonator gap material. The electromechanical coupling coefficient (η_i) on the input side models how efficiently the input electrical signal is converted to a mechanical force. It can therefore be written as the magnitude of mechanical force generated per unit magnitude of input voltage:

$$\eta_i = \frac{F_{\omega_0}}{v_{ac}} = V_P \frac{A\epsilon_r\epsilon_0}{g^2} \tag{2.4}$$

Upon resonance, the vibration amplitude (x), modulates the gap spacing and therefore, the capacitance. With a constant DC polarization voltage applied across the parallel plate, the stored charge changes accordingly, resulting in an output current (i_{out}) when the output electrode is connected to a resistive load.

A key figure of merit for an electrostatic micro-resonator is its motional resistance (R_m), which is defined as [17]:

$$R_m = \frac{i_{out}}{v_{ac}} = \frac{\sqrt{K_{eff}M_{eff}}}{QV_P^2\,(\partial C/\partial x)^2} = \frac{g^4\sqrt{K_{eff}M_{eff}}}{Q(\epsilon_0\epsilon_r)^2V_P^2A^2} \tag{2.5}$$

where Q is the mechanical quality factor of the resonator. For electrostatic micro-devices, a smaller motional resistance is an important requirement to achieve. As it can be deduced from Equation (2.5), a smaller gap size can significantly reduce the amount of motional resistance. This requirement translates to the challenge of fabricating transduction gaps on the nanometer scale. Other approaches have been developed to increase the transduction area rather than the gap reduction method to attain improved

electromechanical coupling. A comb structure is an instance of such approach that provides a larger transduction area (Figure 2-3). By using these techniques, high-Q resonators with reasonably low motional resistances are made in the high frequency spectrum [18].

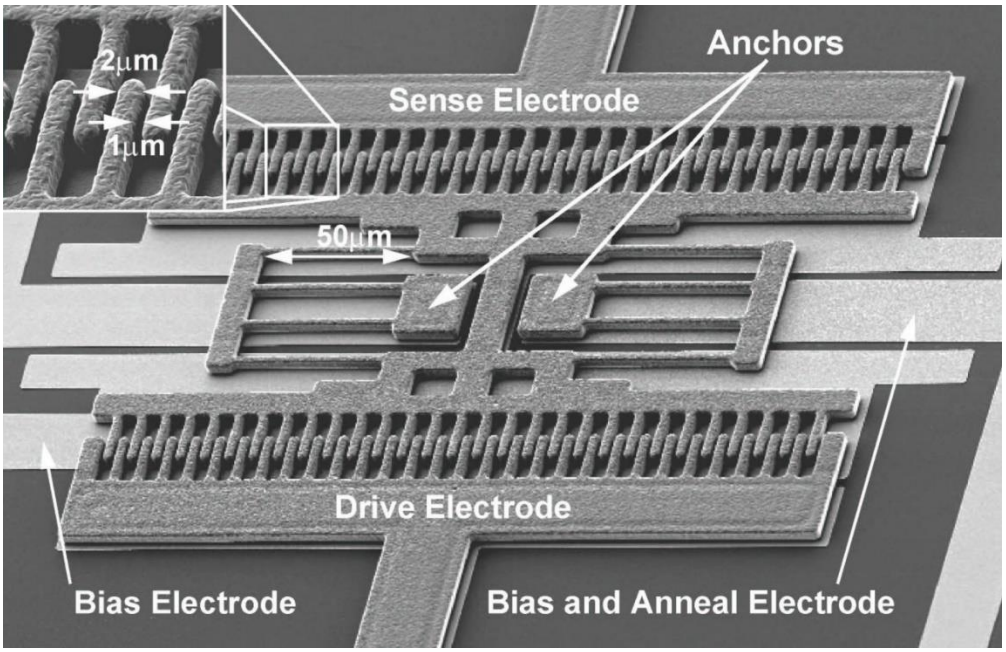

Figure 2-3: Comb resonator with electrostatic drive and sense [19] © 1997 IEEE.

Another approach uses a dielectric material with high permittivity as the filler within the transduction gap [20],[21]. This method is very attractive since it simplifies the fabrication process and eliminates the need for very small capacitive air gaps. In addition, the electric field is stronger in the dielectric compared to the air or vacuum and therefore very large electromechanical coupling values are expected. However, in practice the motional impedance is not improved as expected and the quality factor of the fabricated devices using this technique are lower compared to the devices operating with air gaps. Moreover, the parasitic capacitance between the electrode and the resonant body will be significantly increased as a result of the high permittivity of the material filling the gap. Consequently, unless the parasitic capacitance is separated, limitations will be imposed on the termination impedances that can be interfaced with the device.

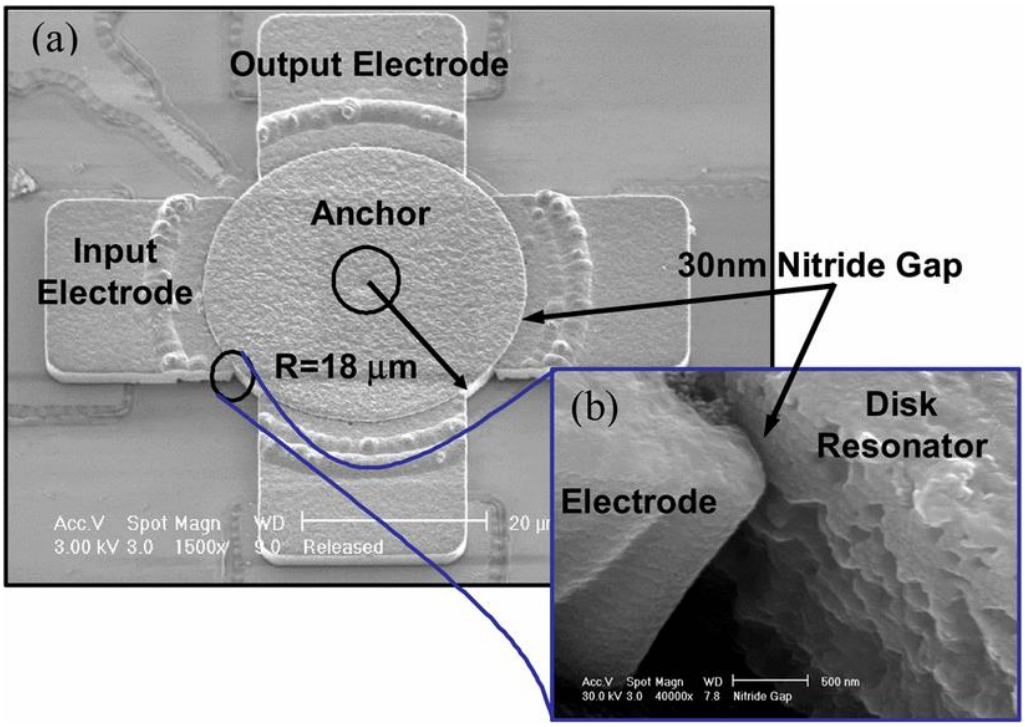

Figure 2-4: Nickel disk resonator with nitride-filled capacitive gaps [20] © 2006 IEEE.

Figure 2-4 presents an example of using a dielectric material such as silicon nitride in the capacitive actuation gap of a disk resonator to achieve lower motional resistance and hence, improved performance.

Electrostatic transduction have been widely used as an attractive mechanism in micro-devices because of its advantages; however, drawbacks and limitations of this method should be considered and rectified when designing such transducers.

2.2. Piezoelectric transduction

Piezoelectric mechanism is another common transduction method in micro-devices which utilizes the piezoelectric properties of some dielectric materials. In piezoelectric materials, a mechanical strain produces an electric polarization and conversely an electric field strains the material. Some widely used materials in MEMS which exhibit piezoelectricity include quartz, zinc oxide (ZnO), lead zirconate titanate (PZT), aluminum nitride (AlN) and polyvinylidene fluoride (PVDF). A piezoelectric

transducer consists of a piezoelectric material sandwiched between two electrodes which are often metal films (Figure 2-5).

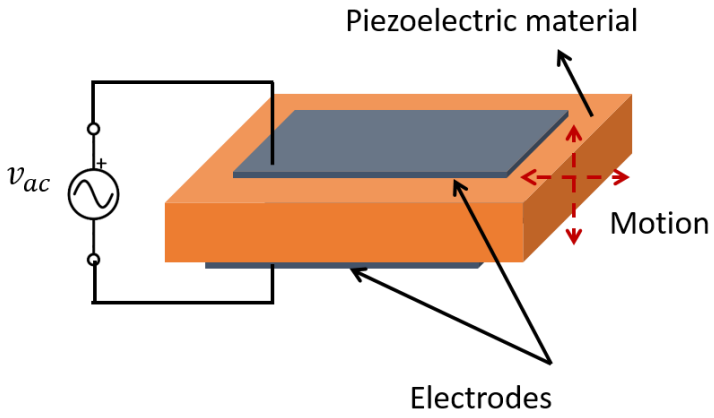

Figure 2-5: A schematic of a piezoelectric material that is sandwiched between two metal electrodes. By applying an alternating voltage between the electrodes, the piezoelectric structure can be driven to vibrate.

The piezoelectric effect have been used in transducers to convert electrical energy into mechanical energy and vice versa. Typical sensing applications include strain, force and displacement sensors. In resonators, this technique combines the resonance principle with the piezoelectric properties of material to decrease the motional impedance of micro-resonators.

Surface acoustic wave (SAW), bulk acoustic wave (BAW) and thin film bulk acoustic resonators (FBARs) are common types of piezoelectric resonators. Piezoelectric-on-silicon resonators use a piezoelectric layer (e.g. zinc oxide or aluminum nitride) for transduction of lateral-bulk single-crystal-silicon micro-resonators. The piezoelectric film is deposited on top of a silicon substrate between two metal electrodes which create the piezoelectric transducer. An SEM image of such a device is illustrated in Figure 2-6 [23]. Piezoelectric counter-mode resonators are made of a suspended piezoelectric material sandwiched between two electrode layers [24],[25].

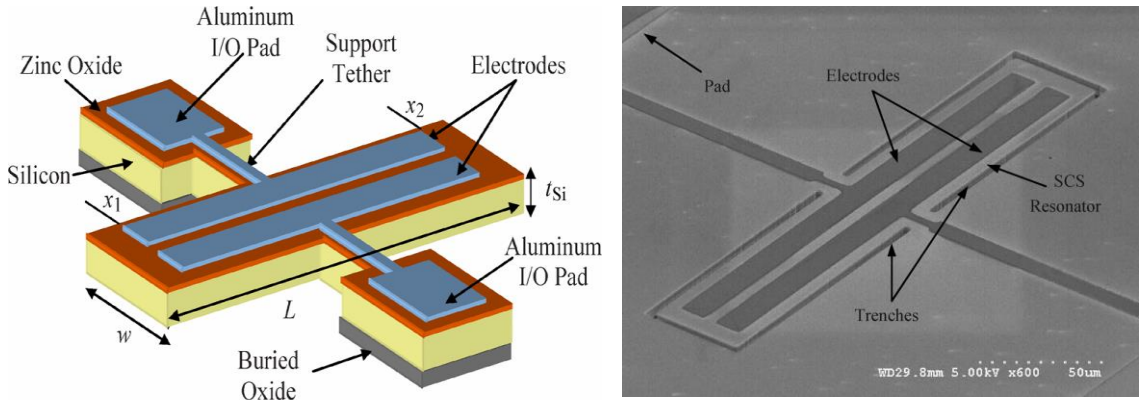

Figure 2-6: Piezoelectric-on-silicon lateral bulk acoustic micro-resonator.[23] © 2008 IEEE.

By applying an electric field on the metal electrodes, the piezoelectric resonant structure will resonate laterally and therefore it can be actuated to vibrate at frequencies defined by its in-plane dimensions. Various resonator structures such as rectangular plates [23] and rings [26] have been designed for various frequencies (i.e. 10 MHz to 500 MHz). Higher-order contour modes of rectangular plates with alternating polarity electrodes can be used for higher frequencies up to 2.5 GHz. For desired modes of these resonators motional resistances as low as 25 ohm and high quality factors in air are reported [27]. Different configurations such as one-port and two-port are presented for a range of applications. Depending on the target application, the pros and cons of each of these configurations can be evaluated for an optimized design. For instance, in the two-port configuration, the input and output ports are electrically isolated which offers improved transduction at higher frequencies; however unwanted spurious modes might be excited at the same time.

New wireless communication systems require high frequency oscillators in the range of 1-15 GHz. Bulk acoustic wave (BAW) resonators are a group of piezoelectric resonators that show a superior performance compared to their LC tanks counterparts in terms of quality factor, power consumption, and size. These attributes make them promising alternatives for mobile applications. In BAW oscillators, the piezoelectric resonator structure should be acoustically isolated from the substrate to minimize energy losses. By applying an electric field across the piezoelectric film and between the electrodes, the structural layer deforms and generates a bulk acoustic wave due to

piezoelectric effect. This bulk acoustic wave propagates and reflects into the resonator structure. A portion of the generated wave moves parallel to the electrodes and another fraction dissipates into the substrate. These energy losses are the main causes limiting the overall quality factor of the resonating system. In order to enhance the quality factor of BAW resonators, an effective acoustic isolation for the resonator structure is necessary.

2.3. Piezoresistive transduction

Piezoresistive mechanism has been utilized in devices such as commercial pressure sensors and accelerometers for several decades. Piezoresistive principle is based on the resistance changes that occur in a conductor or semiconductor due to the bandgap deformations caused by mechanical stress. Compressing and stretching a wire causes its resistance to decrease n increase respectively through piezoresistive effect and geometrical changes in the wire. This mechanism can be used to make strain gauges.

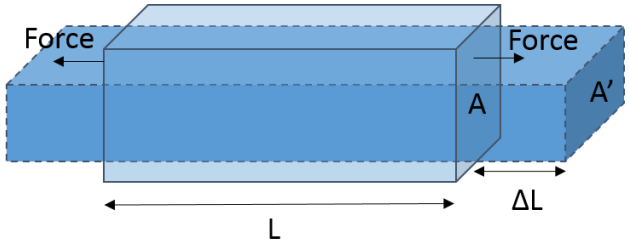

Figure 2-7: Deformation of a rectangular beam under applied axial force.

The electrical resistance of a material with the geometry shown in Figure 2-7 is given by Equation (2.6), where ρ, L and A are its resistivity, length and cross-sectional area, respectively.

$$R = \rho \frac{\mathrm{L}}{A} \tag{2.6}$$

Semiconductors act in the same way, as for the metal wire, under an applied stress. Semiconductor strain gauges have demonstrated several orders of magnitude greater resistance changes resulted from piezoresistive effect than those only due to their geometrical deformations [28],[29].

By introducing dopants into silicon, it is possible to make silicon piezoresistive sensors. Applied stress affects the electrical properties of these doped conducting regions and this in return changes the resistance. Silicon crystal lattice deforms under the applied strain which causes a change in the band-gap shape. Depending on the type of applied strain (i.e., compressive or tensile) this phenomena increases or decreases the number of charge carries in the doped region and thus affects its resistance [28]. The relative change in the total resistance can be written as [30]:

$$\frac{\Delta R}{\mathrm{R}} = \pi_l \sigma_l + \pi_t \sigma_t \tag{2.7}$$

where σ_l and σ_t are longitudinal and transverse component of applied stress, respecitvely. Coefficient π_l is the longitudinal pieozoresistive coefficient along the direction of σ_l and coefficient π_t is the transverse piezoresistive coefficient along the direction of σ_t.

A determinant parameter of sensitivity of a strain gauge is its gauge factor which is a dimensionless number and is defined as:

$$GF = \frac{\Delta R/R}{\Delta L/L} = \frac{\Delta R/R}{\varepsilon} \tag{2.8}$$

where ε represents the applied strain.

In MEMS resonators mechanical motion can be detected using the piezoresistive properties of Si. The piezoresistive readout allows for high transduction efficiency. This transduction technique can be implemented using simple micro-machining processes and allows for resonators with a low mechanical motional resistance. Moreover, this type of transduction is insensitive to geometric scaling and allows for the realization of miniaturized RF MEMS resonators and oscillators without performance reduction. The piezoresistive method has been shown to be a promising alternative for increasing the amplitude of the motional signal in MEM resonators [29]. Figure 2-8: depicts the schematic of a piezoresistive MEM resonator reported by [31].

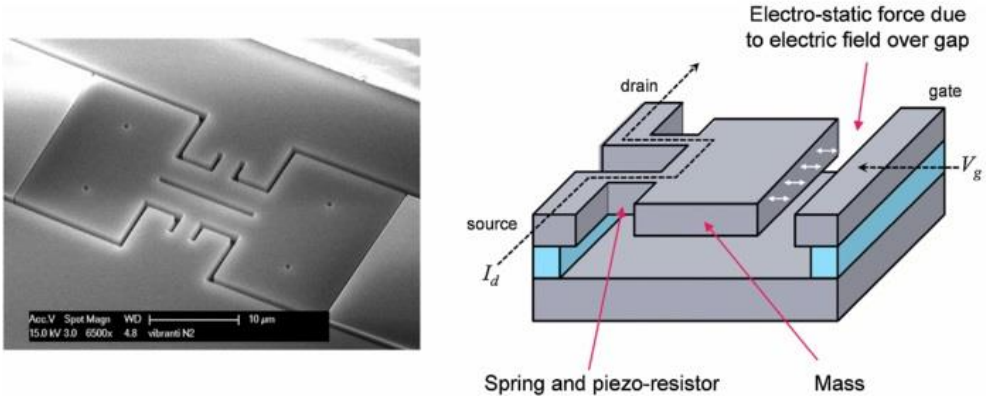

Figure 2-8: SEM and schematic view of a piezoresistive micro-resonator [31] © IOP Publishing. Reproduced with permission. All rights reserved.

For many MEMS applications, the doping of materials does not require accurate control over the doping profiles of the various layers. The doping levels are normally high since the purpose of doping is only to make the material conductive and in some cases to reduce temperature dependences. This could cause compatibility problems with the IC fabrication process when two processes are integrated on the same die.

Although doping is a viable addition for the regular MEMS fabrication processes, most of the standard foundry micro-machining processes such as the multi-user MEMS processes (MUMPs) suffer from lack of it. In piezoresistive sensing, the piezoresistors are often placed at locations that are under the maximum stress during sensor operation and are electrically isolated from the main body, which generally is a membrane, bridge, or similar structure. Electrical isolation is achieved by either employing the piezoresistors on top of an insulating layer or using reverse biased junctions [30],[32]. For instance, to achieve electrical insulation between the two released polysilicon layers in PolyMUMPs, the designer needs to leave the oxide layer underneath the first poly layer. However this will tether the released structure to the substrate and prevent it from moving. Additionally, due to the small deflections of single beams or cantilevers, it is not optimal to use them for piezoresistive sensing purposes. Previous works attempted to fabricate piezoresistive sensors in foundry processes required either very large deflections or additional process steps [33]. Regardless, as mentioned before, these configurations are not feasible in many standard MEMS processes, due to the need for an additional doping step which is not provided by the process.

Piezoresistive sensors are attractive devices owing to their simple design, ease of integration and direct signal processing. Therefore, some attempts have been made to fabricate them in CMOS foundry processes where the integration of conventional bulk micro-machining with post-CMOS processes allows realization of piezoresistive devices [34],[35]. Some techniques have been developed for fabrication of piezoresistive sensors in standard MEMS processes where multiple structural layers are introduced. These structures allow for the fabrication of piezoresistive sensors in low-cost standard MEMS foundry processes without requiring any additional fabrication steps [36].

2.4. Piezojunction transduction

The piezojunction effect is the change of the saturation current of a *p-n* junction caused by mechanical stress. This phenomenon was first discovered in 1951 by Hall, Bardeen and Pearson [37]. They studied the effect of hydrostatic pressure and temperature on electrical characteristics of Germanium *p-n* junctions. Their experimental verifications showed a good agreement with predicted results from Shockley's junction and bandgap theories for stressed junctions. One decade later, it was discovered that this effect is particularly significant for high anisotropic stresses. Therefore, researchers investigated the effect of large anisotropic stresses and pressures in the range of giga Pascal on the resistance of *p-n* diodes and transistors [38],[39]. In most experiments, a hard stylus was used to apply these high stresses onto the *p-n* junctions of transistors and diodes [40]. Their obtained results for high anisotropic stresses were several orders of magnitude larger in comparison with the ones reported by Hall et al. Figure 2-9 illustrates one of the earliest test setups, which was used by Rindner and Braun to apply compressive mechanical stress to a *p-n* junction with a stylus [41]. The changes in I-V characteristic under various stresses were recorded for both forward- and reverse-biased conditions. A large increase in the current of the *p-n* junction in both forward and reverse directions can be observed when anisotropic stresses are applied. Also, the contribution of junction depth, crystal orientation, dislocation density, and temperature on this effect were investigated experimentally.

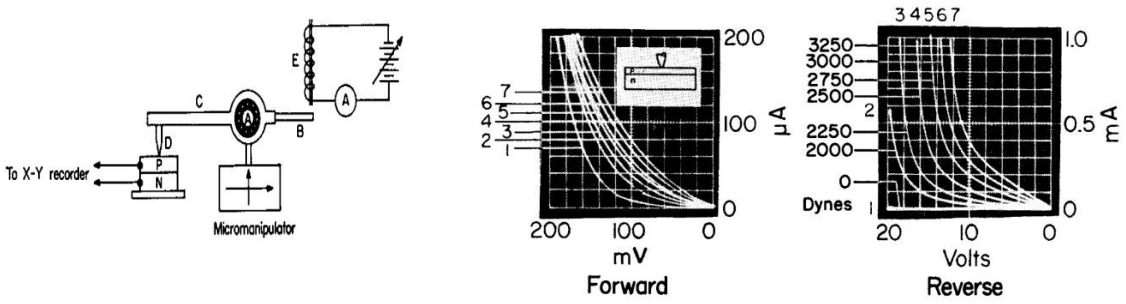

Figure 2-9: Experimental setup for stressing a *p-n* junction and obtained I-V characteristics for various stress levels [41] Copyright 1963, AIP Publishing LLC.

Mechanical sensors, such as accelerometers, microphones and pressure sensors were realized that employed piezojunction effect [8],[42]–[45]. Nevertheless, these sensors suffered from their high sensitivity to mechanical shock and temperature [45],[46]. Therefore, more research were conducted to model the behaviour of the piezojunction effect under high compressive stresses along certain crystal orientations and its dependency to temperature variations [47],[48]. Early techniques of applying stress by bending a silicon wafer or by pressing a stylus on a diode (or transistor) resulted in non-uniform distribution of stress throughout the device. This lack of means to apply precise and controllable stresses has complicated the calculation of piezojunction coefficients [49]. The emergence of micro-fabrication technology enabled improved methods to embed diodes and transistors within the micro-machined structures and to apply stresses in a controlled manner [50]. Micro-machined cantilever beams and membranes with integrated junctions were used to evaluate the piezojunction effect experimentally and to develop analytical models for both compressive and tensile stresses [51],[52].

Initially, the piezojunction phenomenon was studied as an undesirable effect with the focus on how the mechanical stress affects the performance of integrated circuits. It has been known that the stresses induced by fabrication process and packaging on integrated circuits and precision sensors can adversely affect their performance [53]. The majority of studies have been focused on the errors of bandgap references and temperature sensors as due to mechanical stress [54]. Later, this effect was applied for the design of mechanical stress sensors. The effect is known to be notable for the applied stresses on the order of hundreds of Mega Pa to a few Giga Pa [46]. One method to

achieve that high stress is to pre stress the structure and bring the stress level to the appropriate range. However, typical stresses in silicon micro-sensors are in the range of a few kPa to several MPa, making the change in electrical characteristics of *p-n* junctions rather small [8],[45].

The piezojunction effect and its analytical models have been investigated in several studies by physicists and researchers [38],[55],[56]. There are two main analytical models to describe the effect of mechanical stress on saturation current of diodes and transistors. The first model is based on that mechanical stress can deform the energy band structure of semiconductors and as a result changes their bandgap energy. This variation in bandgap energy affects the minority carrier concentration and therefore, the current of a *p-n* junction [39]. The second model accounts for the creation of temporary stress-induced generation-recombination centres within the *p-n* junction, which is a reversible phenomenon [41],[57]. Details of some of these theoretical and empirical models are explained below.

In silicon *p-n* junctions the intrinsic concentration (n_i) is related to the band gap energy (E_g) by [58]:

$$n_i = \sqrt{N_c N_v} e^{-E_g/2k_B T} \tag{2.9}$$

where k_B, T, N_c and N_v are Boltzmann's constant, temperature, effective density of states at the conduction and valence band edge, respectively. Therefore, a decrease in bandgap energy (i.e. bandgap narrowing) increases the intrinsic concentration significantly. On the other hand, the saturation current (I_s) of a diode consists of diffusion and generation components, which are proportional to ${n_i}^2$ and n_i, respectively [55]. Considering the dependence of bandgap (E_g) to mechanical stress (σ), the pre-factor of reverse saturation current (J_s) of a *p-n* junction is affected by stress through:

$$J_s = J_{diff} e^{-\frac{(E_g - \alpha\sigma)}{k_B T}} + J_{gen} e^{-\frac{(E_g - \alpha\sigma)}{2k_B T}} \tag{2.10}$$

where α is the stress coefficient and accounts for the stress-induced change in bandgap. The reported values of α in literature are in the range of $0.041 < \alpha < 0.14$ meV/MPa [39] [55].

Wortman et al. developed analytical models to study the effect of mechanical stress on *p-n* junction characteristics [39]. Stress affects the diffusion and generation-recombination components of saturation current of a diode. However, it is known that the contribution of the generation-recombination current (I_{gen}) in the total current of a silicon *p-n* junction (I_D) is more significant than the diffusion current (I_{diff}) for reverse and low forward biases. Thus, theoretical models were developed to predict the effect of stress on the generation-recombination current [57]. This current is generated by existence of permanent centres in the semiconductor. To simplify these terms, Wortman and Hauser suggested a model to demonstrate that the generation-recombination current is affected by stress-induced changes in the energy band structure and the trap levels of the semiconductor. A subsequent work by Kressel and Elsea on silicon diodes verified the applicability of the above mentioned models. Generation-recombination current can be expressed as [59],[60]:

$$I_{gen} = \frac{q{n_i}^2 W_j A_j \left(e^{\frac{qV_D}{k_B T}} - 1\right)}{\left(\tau_{p0} n_1 + \tau_{n0} p_1\right) + \left(\tau_{p0} + \tau_{n0}\right) n_i \left(e^{\frac{qV_D}{2k_B T}}\right)} \tag{2.11}$$

where W_j, A_j, τ_{p0}, τ_{n0}, n_1 and p_1 denote depletion region width, junction area, life time of holes, life time of electrons, and densities of carriers in conduction and valence band, respectively. Mechanical stress can alter W_j, τ_{p0}, τ_{n0}, n_1 and p_1 of a diode; However, the effect of these parameters on current of diode is rather negligible compared to stress-induced variations of intrinsic concentration (n_i) for stresses above 10 MPa [8]. Hence, it can be assumed that n_i is the only stress-dependant parameter of the current. This assumption was found to be in agreement with experimental verifications. A coefficient (γ_ϑ) is defined as follows to determine the effect of stress on the intrinsic carrier concentration:

$$\gamma_{\vartheta}(\sigma) = \frac{{n_i(\sigma)}^2}{{n_{i0}}^2} \tag{2.12}$$

where n_{i0} is the intrinsic carrier concentration with no stress applied. At high stress levels, γ_{ϑ} is exponentially related to stress (σ) by:

$$\gamma_{\vartheta}(\sigma) = C_1 e^{C_2 \sigma} \tag{2.13}$$

where C_1 and C_2 are constants that depend on material properties and orientation of the applied stress. Figure 2-10 depicts the coefficient γ_{ϑ} along the crystallographic axes of [100], [110] and [111] in silicon for stresses up to 1GPa.

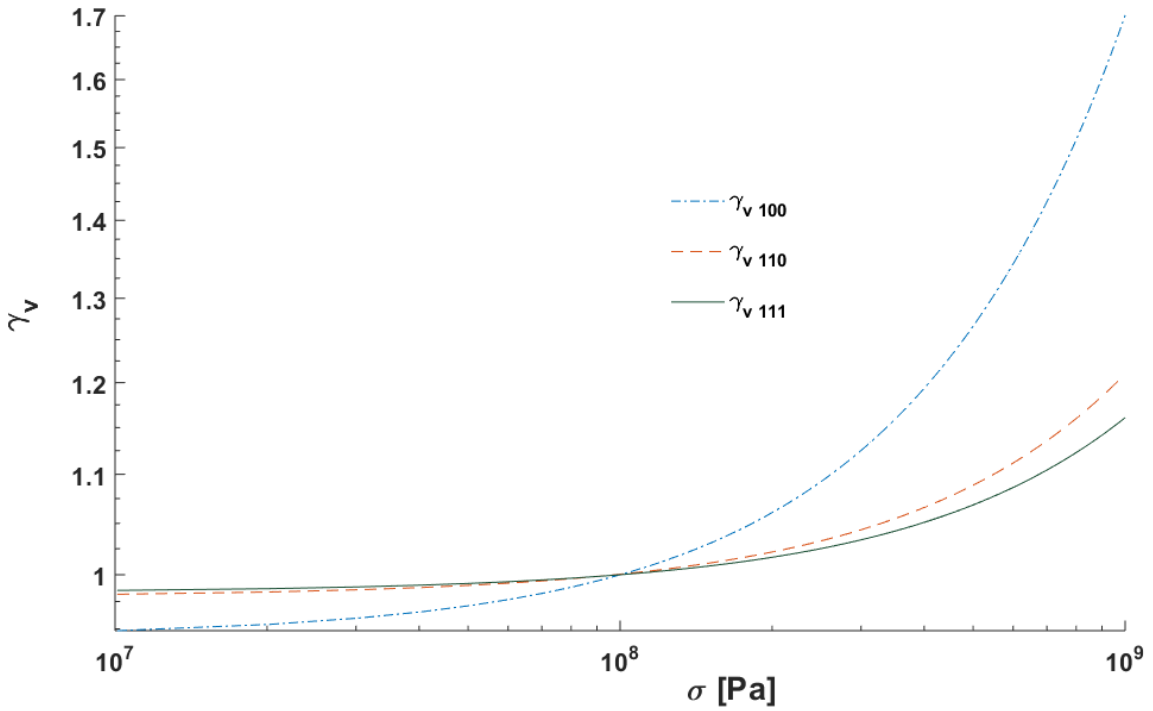

Figure 2-10: Dependence of γ_{ϑ} on the applied stress along different crystalline directions in silicon.

As can be seen, the value of $\gamma_{\vartheta,100}$ increases drastically for stresses greater than 100 MPa in respect to the values of $\gamma_{\vartheta,110}$ and $\gamma_{\vartheta,111}$. From Equation (2.11), Wortman et al. formulated the effects of stress on the generation-recombination current (I_{gen}) as [57],

$$I_{gen} = I_{gen0}\left(\frac{A_j - A_{js}}{A_j} + \frac{A_{js}}{A_t}\sqrt{\gamma_\vartheta}\right)e^{\frac{qV_D}{2k_BT}} \tag{2.14}$$

where I_{gen0}, A_j and A_{js} are the unstressed generation-recombination current, the total junction area and the stressed junction area near the edge of space-charge region, respectively. It should be noted that the effect of generation-recombination currents in the surface is neglected which might be important in specific applications. Similarly, the diffusion current (I_{diff}) of a stressed *p-n* junction can be expressed in the same manner as [39],

$$I_{diff} = I_{diff0}\left(\frac{A_j - A_{js}}{A_j} + \frac{A_{js}}{A_j}\gamma_\vartheta\right)\left(e^{\frac{qV_D}{k_BT}} - 1\right) \tag{2.15}$$

with:

$$I_{diff0} = qA_j\left(\frac{D_p}{L_p}p_n \coth\left(\frac{W_n}{L_p}\right) + \frac{D_n}{L_n}n_p \coth\left(\frac{W_p}{L_n}\right)\right) \tag{2.16}$$

where p_n, n_p, D_p, D_n, L_p, L_n, W_p, W_n are equilibrium concentration of holes in *n*-type silicon, equilibrium concentration of electrons in *p*-type silicon, diffusion coefficient for holes, diffusion coefficient for electrons, hole diffusion length, electron diffusion length, width of *p*-side and width of *n*-side, respectively. Assuming a symmetrical and uniform stress applied to the total area of the junction ($A_j = A_{js}$), the total current of a diode (I_D) at the presence of stress can be found from:

$$I_D = I_{diff0}\gamma_\vartheta e^{\frac{qV_D}{k_BT}} + I_{gen0}\sqrt{\gamma_\vartheta}e^{\frac{qV_D}{2k_BT}} \tag{2.17}$$

According to Equation (2.17), the stress-induced changes on the diffusion current component is larger than the generation-recombination current by a factor of $\sqrt{\gamma_\vartheta}$. In this expression, the component of stress in the depletion region affects the generation-recombination current mainly, while for the diffusion current the stress at the edges of the depletion region has the significant effect. For small biasing voltages, the generation-recombination current dominates the total current of the diode and therefore, its change due to stress outweighs the ideal component significantly.

Recent works by [61] and [62] propose numerical models to predict the influence of piezojunction effect on saturation current of bipolar junction transistors for moderate stresses below 200MPa [63]–[65]. Fruett and Creemer have developed an analytical model for piezojunction effect that can be used in circuit simulators for characterization of mechanical stress induced effects on diodes and junction transistors [66]. Their model is proved to be in agreement with empirical works particularly for moderate stress levels for which the previous models are not highly accurate. In this model, the diode current (I_D) is affected by the mechanical stress (σ) according to:

$$I_D(\sigma) = I_s(\sigma)(e^{\frac{V_D}{nV_T}} - 1) \tag{2.18}$$

with

$$I_s(\sigma) = I_{s0}(1 - \gamma_1\sigma + ({\gamma_1}^2 - \gamma_2)\sigma^2) \tag{2.19}$$

where I_{s0}, V_D, V_T and n are stress-free saturation current, diode voltage, thermal voltage and ideality factor, respectively. Typical values of first-order stress sensitivity (γ_1) and second-order stress sensitivity (γ_2) for silicon are about $1.4 \times 10^{-10}[Pa^{-1}]$ and $-0.7 \times 10^{-18}[Pa^{-2}]$ [62]. For stress levels below 200MPa, the linear term in Equation (2.19) dominates and the diode current can be written as:

$$I_D(\sigma) \approx I_{s0}\left(e^{\frac{V_D}{nV_T}} - 1\right)(1 - \gamma_1\sigma) \tag{2.20}$$

Figure 2-11 illustrates the change in the saturation current for tensile and compressive stresses in the range of 0 to 1 GPa. As it can be seen, effect of compressive stresses are more significant on the diode's current in comparison with tensile stresses. According to this model, a decrease in the saturation current happens for tensile stresses below 100 MPa.

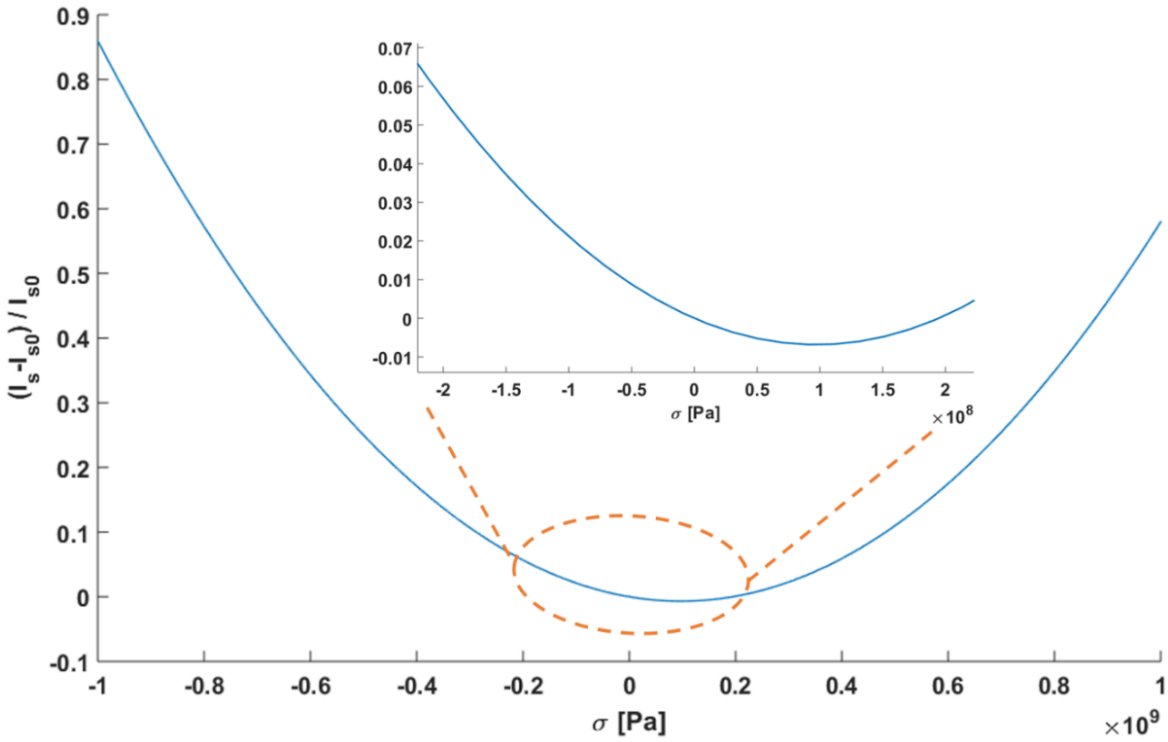

Figure 2-11: Normalized changes of the saturation current to the applied stress.

2.5. Other transduction mechanisms

Other major transduction methods that are employed in micro-devices include electromagnetic [67],[68], thermal [69], and optical [70]. In this part, we describe the thermal actuation that has drawn a great interest for use in micro-resonators recently.

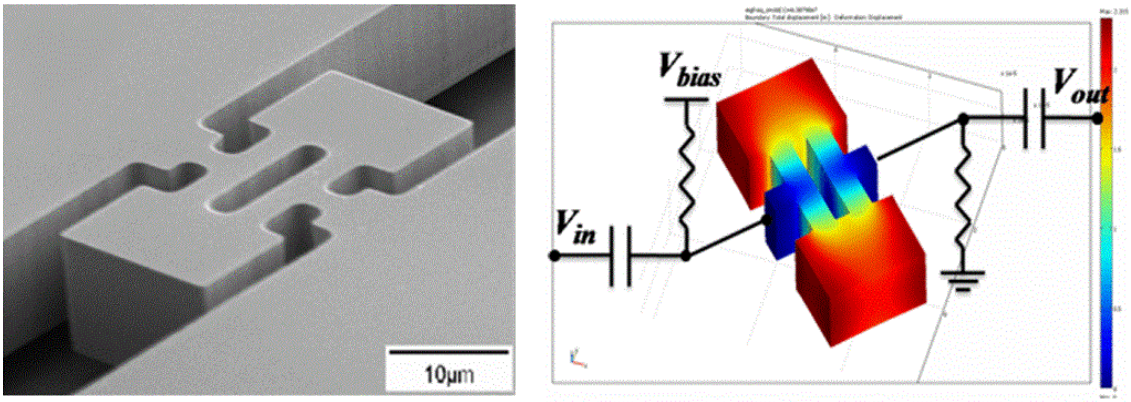

Figure 2-12: SEM image of I^2-BAR thermal resonator and schematic of one-port configuration for operation of resonator in its fundamental extensional-mode of vibration [71] © 2011 IEEE.

Thermal actuation technique has been employed in micro-systems for two main reasons: 1) ease of fabrication, and 2) straightforward integration. Moreover, thermal transducers provide significant benefits such as low operating voltage, large actuation force and simplicity of design. On the other hand, high power consumption and high bulk temperature restricts their use in some applications. Additionally, thermal transducers are typically known as slow actuators due to their thermal principles of operations, hence, they are only suitable for low frequency or DC cases. This is principally because of the time required for the temperature of a warming component to reach the desired level and provide the necessary force. Therefore, thermally actuated micro-machined resonators have been used for sensing applications in the frequency range of hundreds of kHz. Some research has been conducted to study the use of thermally actuated resonators in high frequency applications [71]. Figure 2-12 shows a SEM image and schematic of a thermal micro-resonator. The resonator is excited at its fundamental extensional mode with thermal actuation and the resonance frequency is picked up through piezoresistive sensing.

2.6. Comparison of transductions

In this section, a comparison of the aforementioned transduction mechanisms is provided to briefly discuss the advantages and disadvantages of each technique. Table 2-1 presents such comparison.

Table 2-1: Comparison of various transduction mechanisms in micro-devices.

Transduction	Advantages	Disadvantages
Electrostatic	Large dynamic range Low power consumption Ease of fabrication	Larger motional resistance Feedthrough capacitance
Piezoelectric	Small motional resistances Low insertion loss	Fabrication complexity
Piezoresistive	CMOS integration Large dynamic range Ease of fabrication	Thermal drift Thermal power dissipation Sensitive to resistor noise
Piezojunction	Small die area Low power consumption	Low transduction efficiency Sensitive to temperature
Thermal	Ease of fabrication	High power consumption Temperature sensitivity

Chapter 3. Micro-machined resonators

3.1. Resonance

Resonance is the inclination of a vibratory system to oscillate at greater amplitudes at certain frequencies which are called resonance frequencies of the system. Every structure has its own natural frequencies which depend on its mechanical and geometrical properties. A dynamic system would vibrate at its natural frequencies if an initial disturbance is applied to the system and then allow the system to vibrate freely. A commonly used technique to obtain natural frequencies and modes of continuous systems is Rayleigh's energy method. This method is based on the well-known principle of the conservation of total energy in a dynamic system. According to this principle, the total amount of kinetic energy (K.E.) and potential energy (P.E.) in an isolated system remains constant. Therefore, resonance frequencies of the system can be determined by equating the maximum kinetic energy to the maximum potential energy associated with the oscillation. However, in practical vibratory systems, damping and loss mechanisms will contribute to dissipation of the total energy.

Mechanical micro-resonators are often modelled as simple mass-spring-damper systems around their mode of operation (Figure 3-1). The equation of motion for such system is given by [17]:

$$M_{eff}\ddot{x} + b_{eff}\dot{x} + K_{eff}x = F(t) \tag{3.1}$$

where x is the displacement of the effective mass (M_{eff}), b_{eff} is the effective damping coefficient, K_{eff} is the effective spring constant and $F(t)$ is the dynamic force. This is a second-order linear differential equation with a characteristic equation of

$$M_{eff}s^2 + b_{eff}s + K_{eff} = 0 \tag{3.2}$$

where $s = j\omega$.

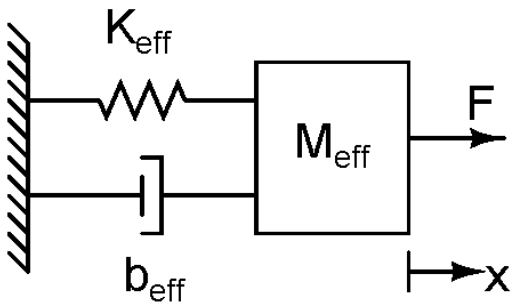

Figure 3-1: Equivalent mass-spring-damper model of a mechanical resonator.

The natural resonant frequencies of system are roots of the characteristic equation and can be found from:

$$\omega_{1,2} = \frac{-b_{eff} \pm \sqrt{{b_{eff}}^2 - 4M_{eff}K_{eff}}}{2M_{eff}} \tag{3.3}$$

Depending on the sign of $\Delta = {b_{eff}}^2 - 4M_{eff}K_{eff}$, one of the following three cases applies:

a. $\Delta < 0$: b_{eff} is relatively small compared to M_{eff} and K_{eff}. The system is underdamped and roots have non-real complex values.
b. $\Delta > 0$: b_{eff} is relatively large compared to M_{eff} and K_{eff}. The system is called to be overdamped with distinct real roots.
c. $\Delta = 0$: b_{eff} value is between (a) and (b). The system is critically damped with repeated real roots.

Figure 3-2 demonstrates the frequency response of the above systems along with the case of undamped system ($b_{eff} = 0$). Oscillators are considered to be underdamped systems. The natural undamped resonant frequency (ω_o) of such oscillators can be determined by using:

$$\omega_o = \sqrt{\frac{K_{eff}}{M_{eff}}} \tag{3.4}$$

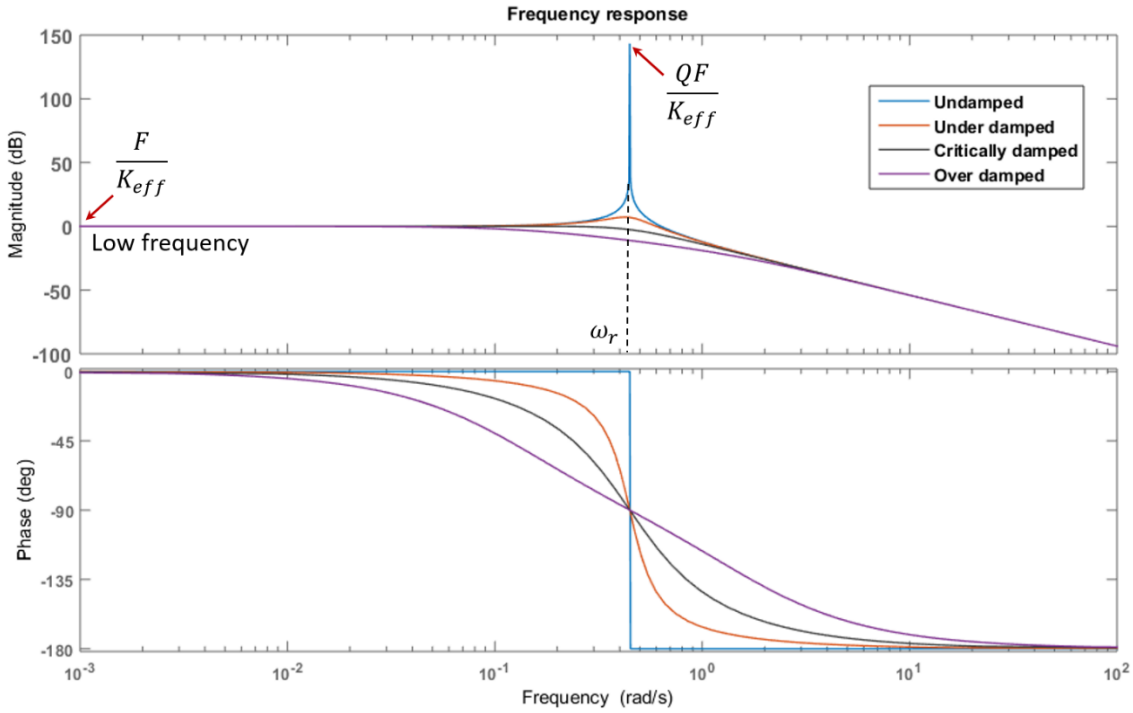

Figure 3-2: Magnitude and phase of frequency response for damped systems.

However, in the presence of damping, the amplitude of vibration decreases and the resonance peak occurs at a lower frequency. The resonant frequency (ω_r) of a second-order oscillatory system is related to its natural undamped frequency by [17]:

$$\omega_r = \omega_o \sqrt{1 - \frac{1}{2Q^2}} \tag{3.5}$$

Q is the mechanical quality factor of resonator and is given as:

$$Q = \frac{M_{eff}\omega_o}{b_{eff}} = \frac{K_{eff}}{b_{eff}\omega_o} \tag{3.6}$$

Quality factor, which is a common figure of merit for the performance of the micro-resonators, can be defined as:

$$Q = 2\pi \frac{Average\ stored\ energy}{Energy\ dissipated\ per\ cycle} \tag{3.7}$$

As it can be inferred from Equation (3.7), one should minimize the dissipated energy for a particular device in order to improve quality factor. In most applications of resonant micro-devices, a higher Q is desired, as the loss of energy during oscillations can lead to the generation of larger noise levels [30].

There are various dissipation mechanisms such as air damping, anchor loss, thermo-elastic damping, intrinsic material damping and surface damping that contribute to energy losses in MEM resonators. Each mechanism can individually limit the Q-value, while the largest energy damping source dominates the total Q of the micro-resonator [72]:

$$\frac{1}{Q_{Total}} = \frac{1}{Q_{Air}} + \frac{1}{Q_{Anchor}} + \frac{1}{Q_{TED}} + \frac{1}{Q_{Others}} \tag{3.8}$$

Among these mechanisms, air damping and anchor losses are known to be the dominant mechanisms that limit Q for micro-resonators operating in bulk modes. Anchor losses are dissipation of acoustic energy of vibrations from the resonator to the substrate through anchors and tethers. Also, vibrations of the resonator body lead to moving the gas in and out of the transduction gaps between the device and fixed structures around it. This results in the formation of a substantial pressure field which induces a force on the moving plate in the gap. Consequently, a portion of the device vibration energy is consumed to overcome this force, which results in energy loss. This effect is known as air damping. The contribution of air damping can be alleviated by operating the resonator under high vacuum conditions [73]–[75]; while anchor losses can be reduced by proper designs of support and anchor structures of a resonating device [22],[77],[78].

3.2. Resonator applications

Mechanical micro-resonators are fundamental constituents in a variety of MEMS applications including automotive industry [79],[80], biomedical devices [81],[82], and telecommunication industry especially in the radio-frequency (RF) domain [83],[84]. Resonant devices have received an extensive interest for commercial markets due to their appealing capabilities such as high sensitivity and accuracy, superiour signal to noise ratio, miniaturization, IC-compatible fabrication technology and large bandwitdh. Following

sub sections detail the use of silicon micro-machined resonators in a wide range of timing, sensing, and mechanical signal processing applications [85].

3.2.1. Timing

Clocks and frequency references are fundamental timing components of most electronic products. The timing market is mostly composed of quartz crystal resonators, active electronic oscillators and clock generators [31],[86]. Quartz crystal oscillators dominate the market due to their unique properties such as high Q, temperature stability, excellent phase noise and insensitivity to mechanical vibration and shock [87]. Owing to their superior performance, quartz crystal oscillators have prevailed as off-chip piezoelectric components for frequency control and time keeping purposes. However, these off-chip components must be interfaced with transistor circuits at board level to function, which takes the valuable space on the board and increases the manufacturing cost and complexity (Figure 3-3). Also, these time references are too bulky and have a high power consumption, which restricts their suitability for portable applications. Miniaturization has offered reduced cost and power consumption in micro-electronic systems. Conversely, shrinking quartz crystals into smaller cuts results in complications such as design difficulties, higher manufacturing cost, lower yields, worse performance (i.e. lower quality factor and worse phase noise) and limited frequency range. Consequently, their drawbacks including their bulky size and incompatibility with standard silicon micro-machining processes have hindered their application in monolithic electronic devices.

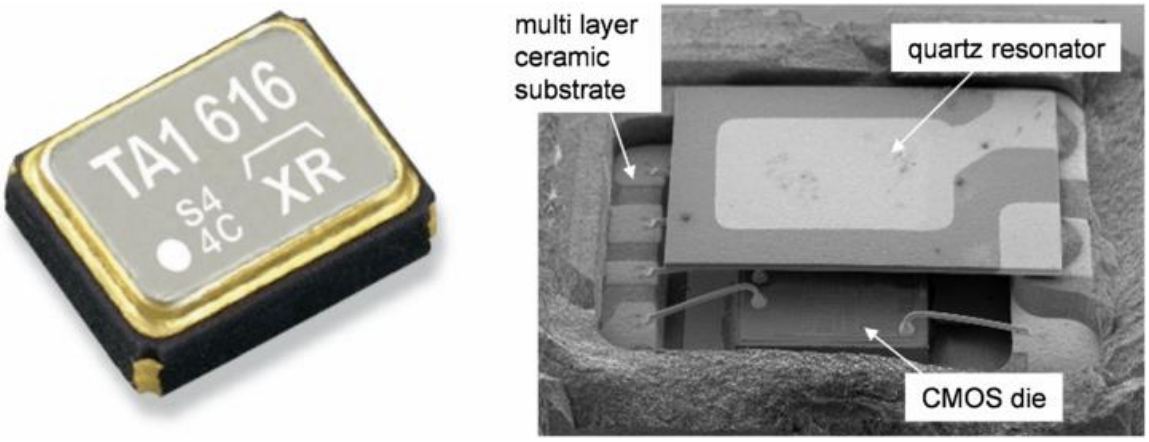

Figure 3-3: Quartz crystal resonator (Epson Toyocom SG-310) wire bonded to its CMOS die on a single ceramic package [31] © 2012 IEEE.

On the other hand, silicon micro-resonators are promising alternatives to quartz crystal resonators as the frequency selective devices for timing applications [85],[88]. The breakthroughs in MEMS resonator technology has enabled such micro-resonators to displace the quartz crystal in some timing products. Micro-mechanical resonators are smaller than their quartz crystal counterparts, which are typically in the range of few millimeters. It is possible to achieve multiple reference frequencies from a single MEMS oscillator, whereas, each quartz resonator can provide only one frequency. As a result, on-chip oscillators that are capable of providing various frequencies onto a single die from a single fabrication process can be realized [89],[90].

MEMS resonators can be fabricated with the state-of-the-art processes borrowed from IC technology onto a single die as CMOS or to be implemented within the same package as the CMOS chip. Integration of MEMS resonators in CMOS technology can alleviate the need for off-chip components such as external sustaining amplifiers and signal conditioning means (Figure 3-4). This integrated timing functionality offers benefits of higher reliability and simpler system design. Additionally, the high level of integration and compatibility result in reduced power and cost for timers providing a monolithic solution with enhanced performance for portable devices [31].

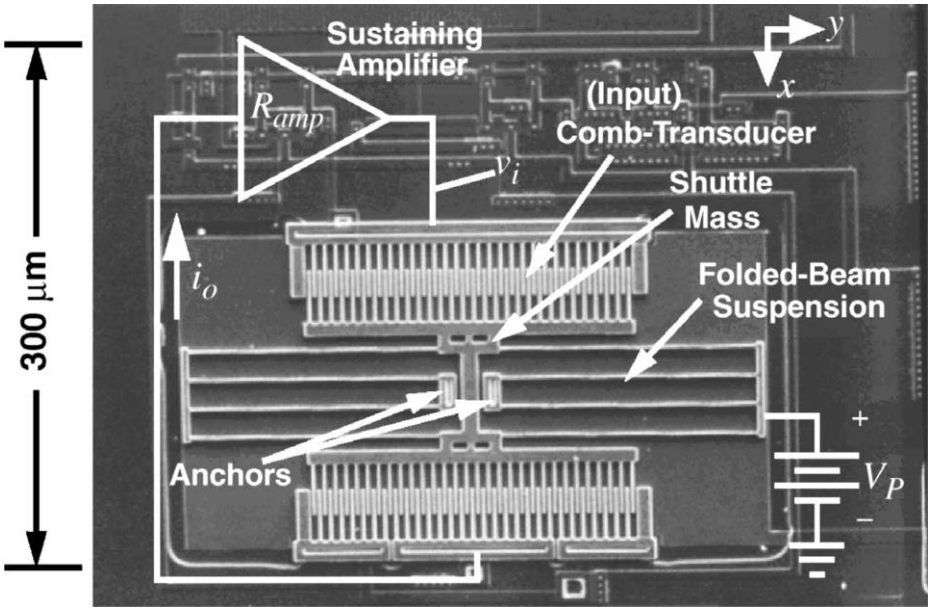

Figure 3-4: Fully integrated CMOS-MEMS oscillator [90] © 2007 IEEE.

Significant improvements in terms of quality factor, temperature stability, integration and packaging for MEMS resonators have ensured the viability of such resonators as substitutes for ceramic and quartz oscillators [86],[91],[92]. With the current miniaturization trend of MEM devices, the operating frequency is increased due to stiffness rise and mass decrease. Design of high-*Q* and high-frequency resonators is in particular pursued for high-accuracy timing applications. The high quality factor of the resonator will improve the near-carrier phase noise in oscillator circuits [93]. This has led to the use of $f \cdot Q$ product as a powerful figure of merit to compare the performance of various resonators with each other [94].

3.2.2. Resonant sensing

Resonant micro-sensors are electromechanical transducers whose potential or kinetic energy of vibration is sensitive to the measured signals [95]. A resonant sensor is a mechanical structure which is designed in such way that its resonant frequency changes as a function of the signal to be sensed. This change of frequency can be caused by a change in the stiffness, mass or geometry of the resonator. Initially, a resonant micro-sensor is excited at its resonant frequency by an actuating means such as electrostatic or piezoelectric mechanisms. A readout transduction (e.g. piezoresistive, capacitive, etc.) is

then employed to monitor the changes in the resonance frequency. The output of a resonator is a frequency that is a quasi-digital quantity. Resonant sensing has significant advantages such as large dynamic range, high sensitivity, low noise, long stability and good linearity compared to other sensing techniques. Compared to other detection techniques, resonance-based methods offer higher accuracy as frequency measurement provides higher precision. Resonance sensing has been employed in many devices to detect force [96], acceleration [97],[98], pressure [99], mass [100], temperature [101], magnetic field [102],[103] and biological entities [104].

A majority of resonant sensors are either mass or strain sensors. Mass sensing is a common application of resonant sensors. In this type of sensors, addition of a mass to the resonator decreases the resonant frequency. This frequency change can be used to measure the amount of added mass by,

$$\frac{\Delta f}{f_o} = -\frac{\Delta m}{2M_{eff}} \tag{3.9}$$

where Δf is the change in resonance frequency that is caused by the added mass (Δm). Figure 3-5 shows a piezoelectric-on-silicon resonant mass sensor for detection of aerosol particles [105]. The resonator is driven at its lateral-extensional mode of 54 MHz with a quality factor of greater than 18,000 in air. In sensing applications, a high Q results in a more stable resonant frequency and better resolution in the measurement of the changes in resonant frequency. Deposited particles on the surface of micro-resonator increase the effective mass of the resonator, and thus, accumulation of aerosol particles lead to a shift in its resonant frequency from which the amount of the added mass can be estimated.

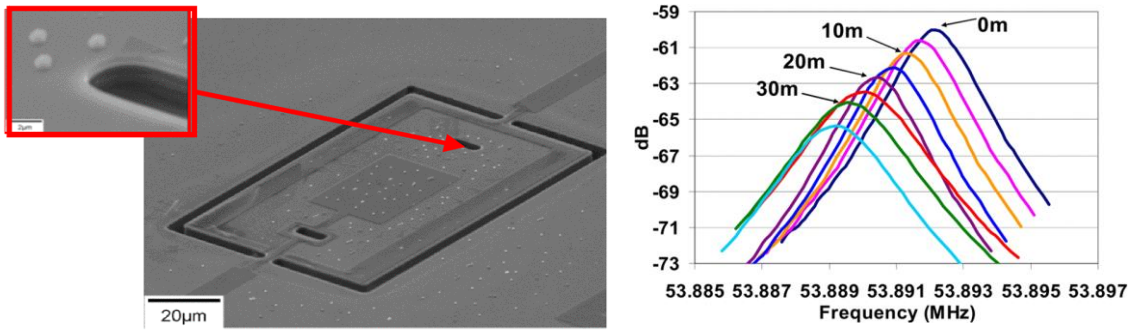

Figure 3-5: Resonant particle mass sensor: (left) SEM image and (right) frequency change by added mass over time [105] © 2010 IEEE.

On the other hand, if a measurand produces stress onto the resonator structure, the stiffness of resonator changes, and hence, the resonant frequency. This change in resonant frequency can be related to the change in the stiffness (ΔK) and therefore to gauge the parameter of interest.

$$\frac{\Delta f}{f_o} = \frac{\Delta K}{2K_{eff}} \tag{3.10}$$

For example, Figure 3-6 presents a resonant magnetic field sensor, in which, an external magnetic field affects the effective spring constant of the resonator structure and as a result alters the resonant frequency. Electrostatic actuation and sensing are used to drive the resonator at its fundamental resonant frequency and monitor the output frequency. When the resonator is exposed to a magnetic field, an axial force will be applied to the support beams that connect the shuttle to cross bars. This axial force will alter the resonant frequency of the device. By means of electronic signal processors, the resonance frequency change is used to measure the magnitude and direction of the magnetic field.

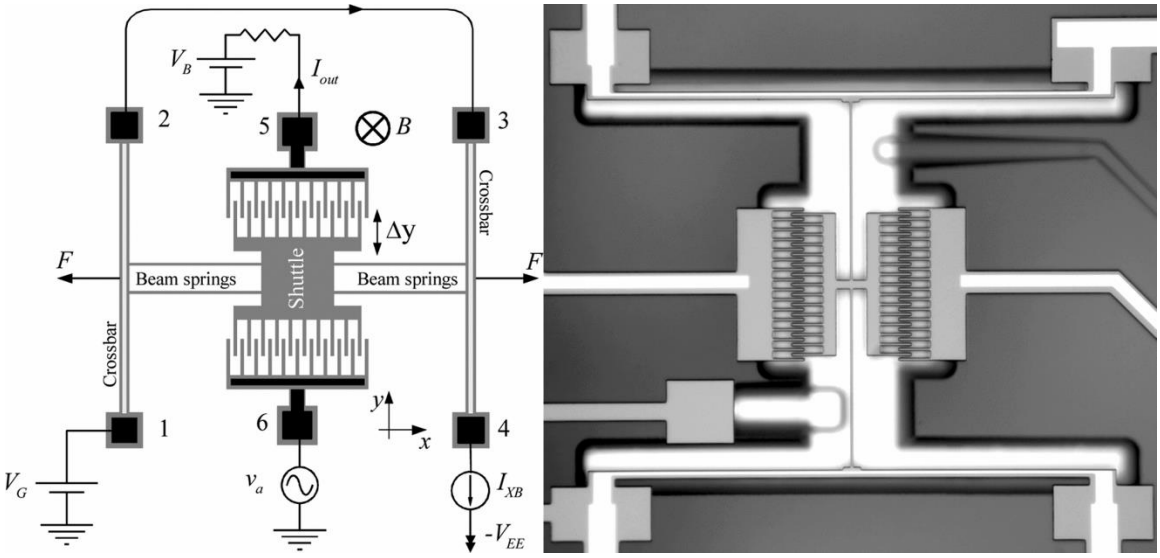

Figure 3-6: MEMS resonant magnetic field sensor [103] © 2007 IEEE.

Resonant sensors have been fabricated from materials including silicon, quartz and gallium arsenide [106]. Silicon resonant sensors are batch fabricated from single-crystal silicon using conventional surface and bulk micro-machining processes. Their compatibility with CMOS processes enables their integration with interface electronics on a single chip.

3.2.3. Signal processing

Micro-mechanical resonators have been used for mechanical signal processing in applications including RF MEMS filters, mixers and switches in communication systems [25],[107]. Figure 3-7 illustrates a system building block representation of using MEMS components instead of electronic elements in a super-heterodyne receiver, which is the basis of most of modern RF communication systems [108].

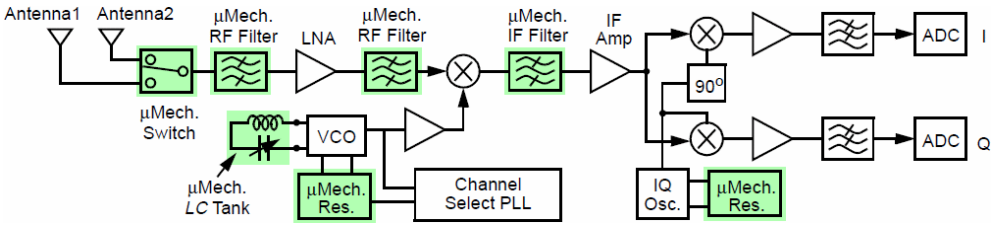

Figure 3-7: System architecture of a super-heterodyne receiver with MEMS components [108] © 2002 John Wiley & Sons, Inc.

RF MEMS filters are key signal processing components that have been widely used in mobile communication and satellite systems. Currently, filters have been successfully miniaturized using surface acoustic wave (SAW), bulk acoustic wave (BAW) and film bulk acoustic resonators (FBARs) [109],[110]. Such RF MEMS components offer substantial reduction in size, cost and power consumption through miniaturization. In filters, the steep slopes of the frequency response near the resonant frequency of a micro-resonator can be exploited to realize narrow bandpass filters [111].

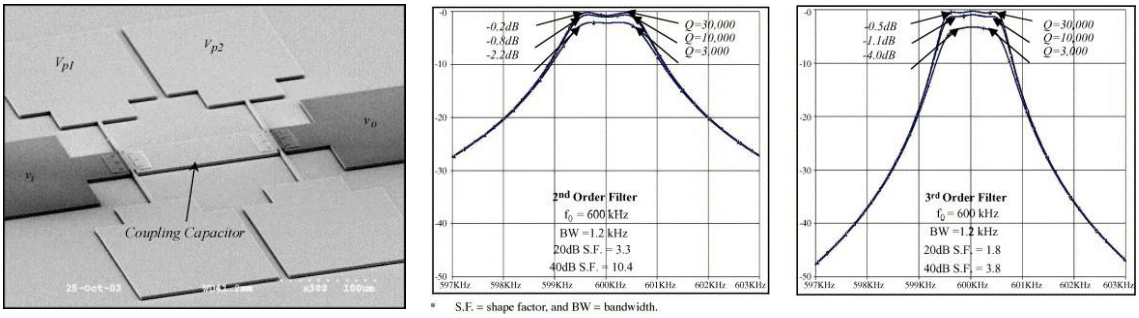

Figure 3-8: An electrically-coupled micro-machined bandpass filter and its frequency response [112] © 2005 Elsevier B.V.

Figure 3-8 shows an SEM image of a MEMS bandpass resonator that employs electrical coupling elements to realize a high-order narrow-bandwidth filter. The bandpass frequency response is achieved through the coupling of identical single micro-resonators with capacitors. A second-order filter is achieved by coupling of two resonators that generate two resonant frequencies with a tunable bandwidth. The separation of these frequencies is determined by the value of coupling capacitor. Higher orders of filters can be implemented by coupling of additional resonators. A high mechanical quality factor results in improvements in insertion loss, stop-band rejection, and dynamic range of the filter.

3.3. Resonance modes

MEM resonators take various shapes such as beams, plates, and comb structures [109]. Silicon micro-resonators are often operated in their flexural [113], bulk [76] or torsional [114] resonant modes. Flexural modes are due to the bending of various components in a structure. Most flexural micro-resonators use straight or curved beams to produce the mechanical restoring forces. Flexural modes of various structures such as cantilever beams [115], clamped-clamped beams [88],[116], free-free beams and tuning forks [117] have been studied in the literature.

Flexural micro-devices have high displacements and typically operate at frequencies in the range of 10 kHz to 10 MHz. Since the resonant frequencies of micro-structures are inversely proportional to the device dimensions, to attain higher frequencies very small dimensions on the order of a few microns should be used. This constraint causes complications in the fabrication and power handling capability of such devices. Quality factor of flexural devices is typically limited to several thousands to few tens of thousands. Figure 3-9 shows a flexural-mode micro-resonator and its corresponding mode of vibration.

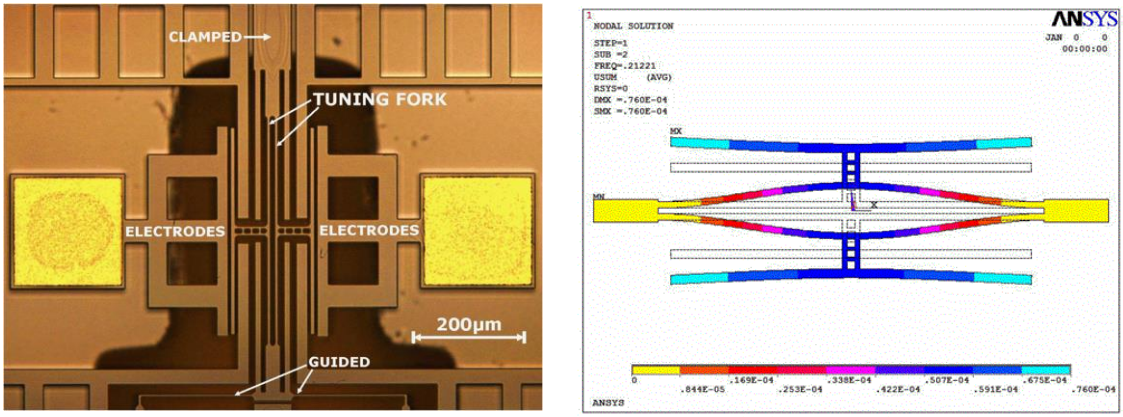

Figure 3-9: Double-ended tuning fork micro-resonator and its anti-phase flexural mode of vibration [113] © 2008 IEEE.

Bulk-mode resonators employ the whole structure as a distributed mass and spring system. In general, this results in higher stiffness for the structure compared to flexural resonators of similar dimensions, and thus, bulk-mode resonators usually have higher

resonant frequencies [26],[118]. As a result, bulk-mode resonators are often used when one needs to operate at frequencies beyond a few mega-hertz. However, the continuous trend towards higher resonant frequencies has resulted in developing smaller devices, which leads to smaller signals from these devices. One solution to this trade-off has been the coupling of several micro-resonators [116]. Another technique to achieve high oscillation frequencies using relatively large structures is to employ the higher resonant modes of the structure rather than relying on the fundamental mode [25],[119],[120]. Various groups have experimentally shown that it is possible to achieve high $f \cdot Q$ products by employing higher resonant modes of a device [76],[121], [122]. The design of high-*Q*, high-frequency resonators is of particular interest for timing applications. The availability of a device resonant frequency translates into simplifications in generation of RF reference signals; e.g., for local oscillators with high frequency. A bulk-mode square resonator and its lamé mode shape are illustrated in Figure 3-10.

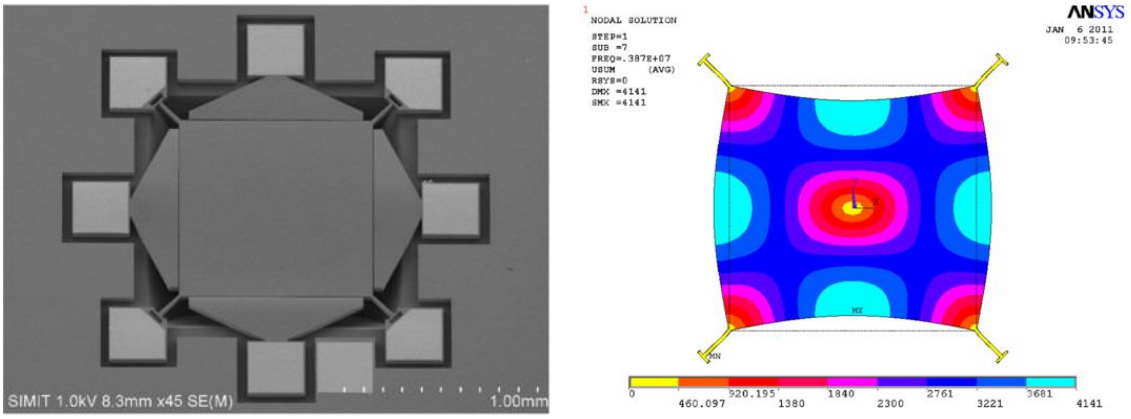

Figure 3-10: Square micro-resonator and its corresponding lamé mode[123] © IOP Publishing. Reproduced with permission. All rights reserved.

Since the resonant frequencies of micro-structures are inversely proportional to the device dimensions, for a given resonant frequency, the bulk resonators will be larger than the flexural devices. This translates into a larger area for signal transduction, which often leads to lower insertion losses. As a result, nearly all resonators that are designed for timing applications that operate at frequencies beyond a few megahertz employ the bulk modes of micro-structures. Additionally, the capacity of bulk resonators for vibration energy storage is also larger than that of flexural devices of similar dimensions.

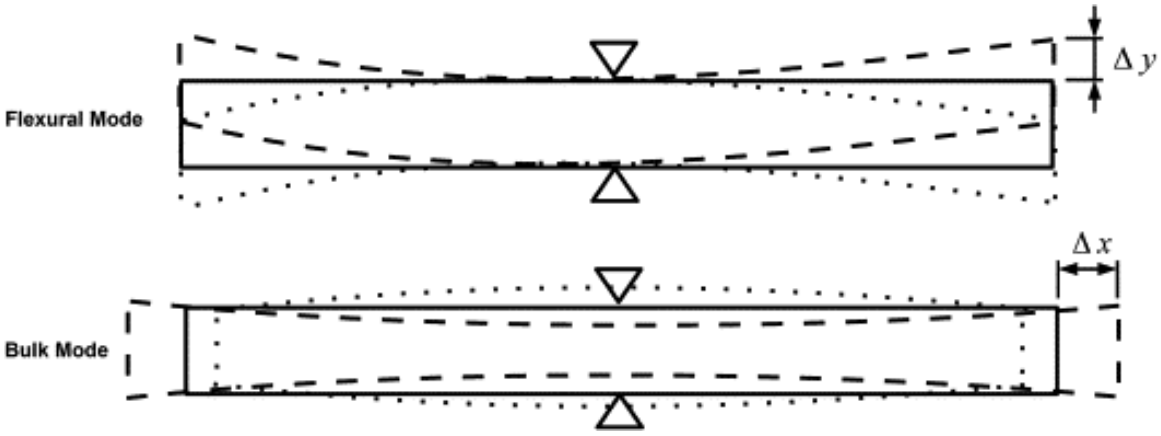

Figure 3-11: Flexural and bulk modes of vibration for a straight beam.

Another advantage of bulk resonators compared to flexural devices of similar dimensions is their higher capacity to store vibration energy. As an instance, consider the straight beam shown in Figure 3-11, which is pinned at its centre (i.e., free-free beam) [94],[124],[125]. This beam can be operated under its fundamental flexural or bulk extensional modes as shown in Figure 3-11. The stored energy (E_S) for each mode of vibration is given by:

$$E_S = \frac{1}{2} K_{eff} x^2 \tag{3.11}$$

where K_{eff} and x are the effective spring constant and displacement of the resonant structure, respectively. The effective spring constants for flexural and bulk extensional modes are $K_f = \acute{\alpha} \frac{EhW^3}{L^3}$ and $K_b = \frac{EhW}{L}$, where $\acute{\alpha}$ is a parameter in the range of $0.25 < \acute{\alpha} < 16$ depending on the mode shape and E is the modulus of the elasticity. Parameters W, L, and h are the beam's width, length, and thickness, respectively. Assuming the same maximum displacement (e.g., 5% of the gap for electrostatic devices) for both modes, we can calculate the ratio of stored energy per volume of the flexural mode (i.e., E_{SF}) to the stored energy per volume of the bulk mode (i.e., E_{SB}) as:

$$\frac{E_{SF}}{E_{SB}} = \frac{\acute{\alpha}(EhW^3/L^3)}{(EhW)/L} = \acute{\alpha}\left(\frac{W}{L}\right)^2 \tag{3.12}$$

Since the beam width, W, is much smaller than its length, L (typically $L > 10W$) we can deduce from Equation (3.12) that the energy storage capacity of the beam's bulk mode is

significantly greater than that of its flexural mode. The effective stiffness of bulk modes of typical MEMS structures are higher than those of the flexural modes. This leads to a higher kinetic energy for the bulk modes compared to the flexural modes of a structure assuming similar levels of vibration amplitude for both modes.

Torsional modes occur due to the twisting and rotating of resonating structures or their supporting beams. A sample mode shape of such vibration is shown in Figure 3-12. The resonator plate is suspended with a beam, which is connected through flexural support beams to anchors at both ends. Two electrodes are placed underneath of the resonator paddles on the substrate and are used for actuation and sense purposes. By applying an alternating electrostatic force to the drive electrode, the resonator will vibrate in its torsional mode.

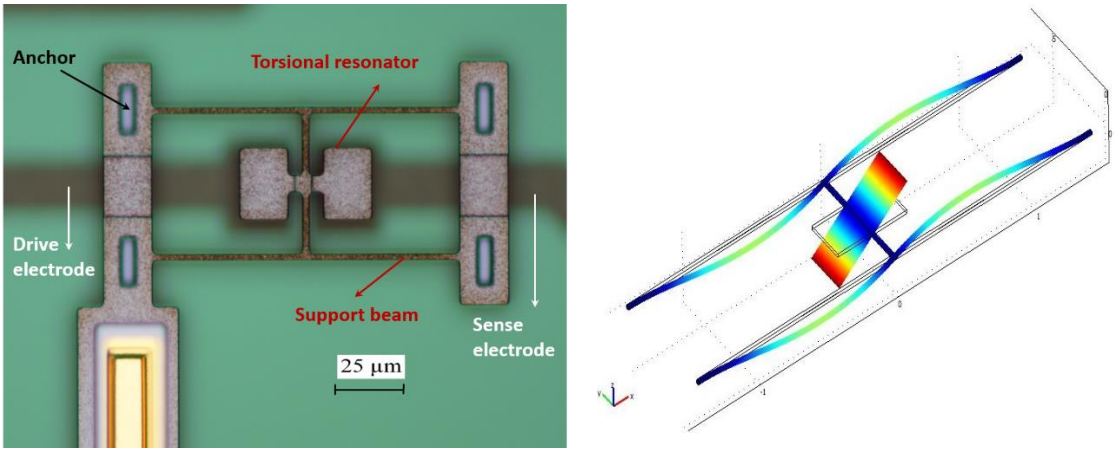

Figure 3-12: Torsional micro-resonator: (left) structure and (right) torsional mode of vibration.

Chapter 4. Fabrication process

A Silicon-On-Insulator (SOI) micro-machining process is developed and characterized to fabricate proof-of-concept resonators with embedded *p-n* junctions. The main steps of the process flow include: 1) selective doping of the silicon device layer to create the doped junctions at desired depths, 2) patterning of the silicon layer to define device structures, anchors and transduction gaps, 3) placing electrical routings and metal contacts, and 4) releasing the moving structures to fabricate functional devices. These steps are shown in Figure 4-1. All the process steps and design rules of the SOI fabrication process are developed and optimized by the author at the Institute of Micromachine and Microfabrication Research (IMMR) facility in School of Engineering Science and 4D LABs at Simon Fraser University.

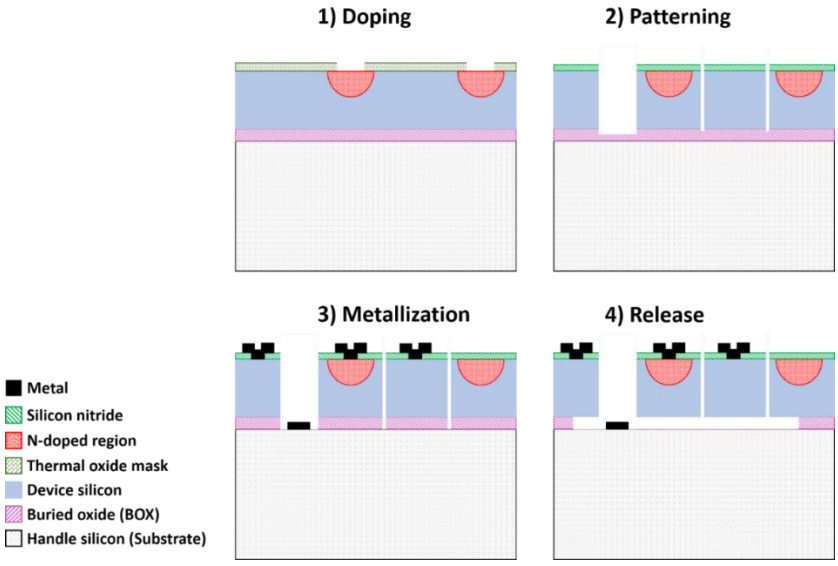

Figure 4-1: Main steps of the SOI fabrication process (not to scale).

The fabrication process is a 4-mask level SOI patterning and selective etching process. The process is designed and optimized to be a multi-user process. The process parameters and design rules are chosen in a way to support many various designs on a single substrate and not to be specific to a certain device. This process has a potential to provide high yield and high level of cleanliness which ensure the quality of fabricated

devices. Process steps and details of each step are described in Appendix A and following sections of this chapter.

4.1. Starting substrate

The term SOI refers to a three-layer material stack which comprises the following layers: a top layer of prime quality single crystal silicon (Device Layer) on an electrically insulating silicon dioxide layer (Buried Oxide, BOX), set over a substrate bulk silicon wafer (Handle wafer). SOI wafers have been widely used in MEMS and Radio Frequency (RF) for specific end-user applications. SOI wafers offer certain benefits such as reliable electrical insulation, sacrificial and etch-stop layer over standard silicon wafers. Also, they provide simplicity in fabrication process and improvement in device performance.

For the purposes of this research, a thicker device layer would allow for creating of high aspect ratio MEMS devices with larger actuation areas. Thus, a stronger electromechanical coupling factor can be achieved for electrostatic drive. However, the necessity of Deep Reactive-Ion Etching (DRIE) equipment for etching of high aspect ratio features, high rate etching and through-wafer etches imposes a limit on using thick SOI substrates for this work. Therefore, SOI wafers with device layer thicknesses in the range of 1.5 µm to 3 µm are chosen in congruence with our facility capabilities and purchased from UltraSil Corporation for this fabrication process. Figure 4-2 illustrates the cross-sectional view of such SOI wafers. Another important attribute of the silicon device is its electrical resistivity. The resistivity of the silicon layer depends on the dopant concentration. Proper selection of this specification is determinant to allow for manufacturing of diodes with desired junction depths and achieving electrical contacts with ohmic contacts during the metallization step. The thickness of the BOX layer determines the gap space between the moving structures and the substrate underneath. As well, it affects the duration of the release step at the end of process.

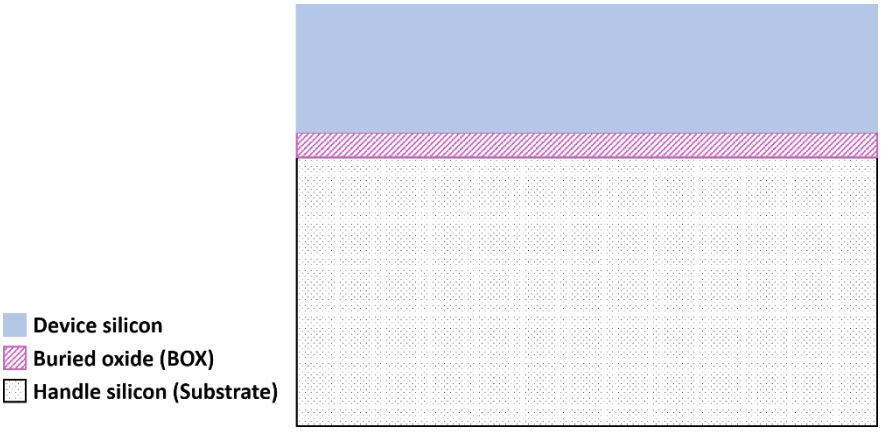

Figure 4-2: SOI wafer comprising of Device silicon, Buried oxide and Handle silicon layers.

After consideration of the above mentioned criteria, the thickness of layers and resistivity of device layer are chosen in a manner to satisfy our design requirements and to suit our technological constraints. In the course of this process development, SOI wafers with silicon device layers of both *n*-type and *p*-type kinds and resistivities in the range of 0.001 Ω-cm to 20 Ω-cm were used to find the optimal specifications for this fabrication process. Table 4-1 summarizes the specifications of the SOI wafers that have been used in fabrication of the reported micro-resonators of this thesis. The starting material is a (100)-oriented 4" SOI wafer with a 3 µm thick silicon layer and 1 µm buried oxide (BOX). The resistivity of the Boron-doped device layer was measured with a 4-point probe to be 5 Ω-cm, which corresponds to a dopant concentration of ~ $3x10^{15}$ cm^{-3} for *p*-type silicon device layer.

Table 4-1: Specifications of SOI wafer provided by the manufacturer.

Diameter	Type-orientation	Device thickness [µm]	Device resistivity [Ω-cm]	Handle thickness [µm]	Handle resistivity [Ω-cm]	Box thickness [µm]
100 mm	P/B-(100)	3±0.7	1-10	500±25	10-20	1

4.2. Doping

Creation of doped regions in the body of the micro-devices is one of the most critical steps of this SOI process. The outcome of this stage will determine the quality and performance of the *p*-*n* junctions that will be used for sensing purposes. Thermal diffusion is a common method for introducing doping to a semiconductor. In the diffusion step, the silicon device layer surface which is not protected by the SiO_2 mask is exposed to a solid source with high concentration of phosphorous impurity at temperatures above 900 °C. The *n*-type impurity moves into the silicon by solid-state diffusion. The oxide layer serves as a barrier to prevent exposure of the silicon layer to dopants in elsewhere than the opening windows.

Given that thermal diffusion requires the SOI wafer to undergo a very high temperature for quite long periods of time, raises concerns regarding the possible adverse effects of such high temperature process on the structure of the SOI wafer. The thermal process may generate high stresses in the structural layers due to the thermal mismatch of the constituent layers, which in turn can cause complications such as bending or breakage of the hanging structures after release. At the early stages of development of this SOI process, the thermal diffusion of dopants into the silicon layer from a liquid source was investigated. Fabrication details and characterization graphs of this process are provided in Appendix A. The benefits of using Spin-On-Dopants (SODs) in formation of shallow junctions include their simple process, compatibility with Rapid Thermal Annealing (RTA), and simultaneous diffusion of both *p*-type and *n*-type dopants. The use of RTA in the diffusion process allows for decreasing the thermal budget. Nonetheless, difficulties with processing of liquid dopants and resulted junctions with poor characteristics, compelled us to investigate using thermal diffusion with solid sources. The ramping rate of the diffusion furnace is optimized to avoid the creation of high thermal stresses in the layers of the SOI wafer during the diffusion process.

Initially, a high-quality silicon dioxide (SiO_2) is grown from the device layer with thermal oxidation process that functions as a selective mask for diffusion step. The oxide thickness used for masking can be determined experimentally to find the required thickness that prevents the impurity dopants from diffusing through the oxide mask to the

silicon surface underneath. Graphs of required oxide thickness for masking of boron and phosphorous for typical diffusion temperatures and times are provided in literature [126]. From such graphs, the typical oxide thicknesses are in the range of 400 nm-1 µm for common diffusion impurities and parameters. Wet thermal oxidation is commonly used to grow oxide mask because the growth rate is much higher than dry oxidation when the water vapor is presented in oxidation process. A cleaning step such as RCA cleaning is necessary before the oxidation to ensure a high quality grown oxide layer. An oxide layer with a thickness of 500 nm is formed all over the SOI wafer surface after 45 minutes of wet oxidation at 1100 °C (Figure 4-3). This oxide thickness is chosen to form an effective diffusion barrier for the following phosphorous diffusion process.

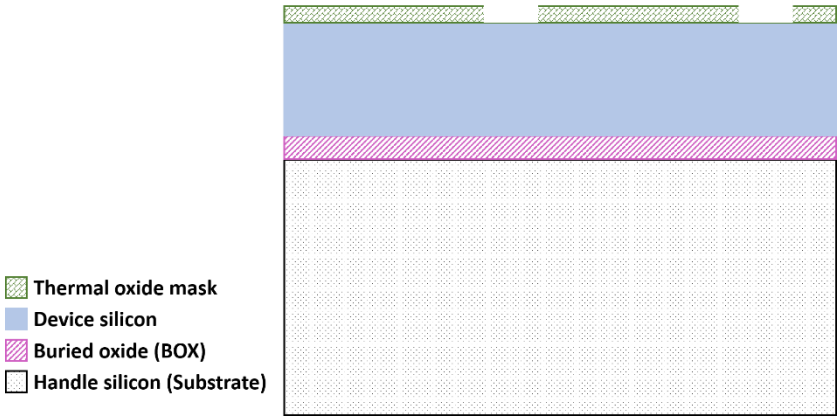

Figure 4-3: A thermal oxide layer is grown and patterned to serve as the diffusion mask.

The SiO_2 film is patterned with first photomask using photolithography followed with a Buffered Oxide Etchant (BOE) to define the geometry of *p-n* junction area. The wafer surface is coated with a Shipley 1813 photoresist, an ultraviolet (UV) light-sensitive material, which is spun with a spinner at 4000 rpm for 40 seconds. Subsequently, the wafer is baked on hotplate at a temperature about 115 °C for 60 seconds to dry and to harden the photoresist. The next step is to expose the resist to UV light using the patterned photomask and mask aligner with a UV light source. The regions exposed to light polymerize and become difficult to remove in a developer. By placing the wafer in MF319 developer for 1 min with constant agitation, the resist over unexposed areas dissolves and washes away. Afterward, the wafer is baked at 115 °C for 120 seconds to become a more resistant mask for the following oxide etch. Then, a buffered hydrofluoric acid (HF) etchant

removes the SiO_2 from the unprotected regions. At the end, the photoresist is stripped away in an acetone bath. A subsequent IPA and DI water rinse cleans the surface. Figure 4-3 shows the opened windows in the oxide layer. The wafer is now ready for forming of *n*-type diffused layers by the following thermal diffusion process.

Thermal diffusion in a furnace usually creates a deeper junction compared to ion implantation method. Therefore, diffusion parameters are optimized to form shallower junctions within the range of our device silicon thickness (~3 µm). Diffusion process is carried out with solid PH-1000N phosphorous sources from PDS® Products in a thermal diffusion furnace at 950 °C for 30 minutes. After the diffusion process, the *n*-type regions are formed in *p*-type silicon. This diffusion has a constant surface concentration profile in which the phosphorous dopants are transported from the solid source onto the silicon surface and into its crystal lattice. The solid source maintains a constant level of surface concentration (i.e. solid solubility of phosphorous in silicon at 950 °C) during the diffusion process (details are provided in Appendix A). As it can be seen in Figure 4-4, the width of the N-region is slightly wider than the openings in the oxide layer due to the lateral diffusion of the phosphorous impurities. This causes a design constraint on the minimum separation between the diffused geometries.

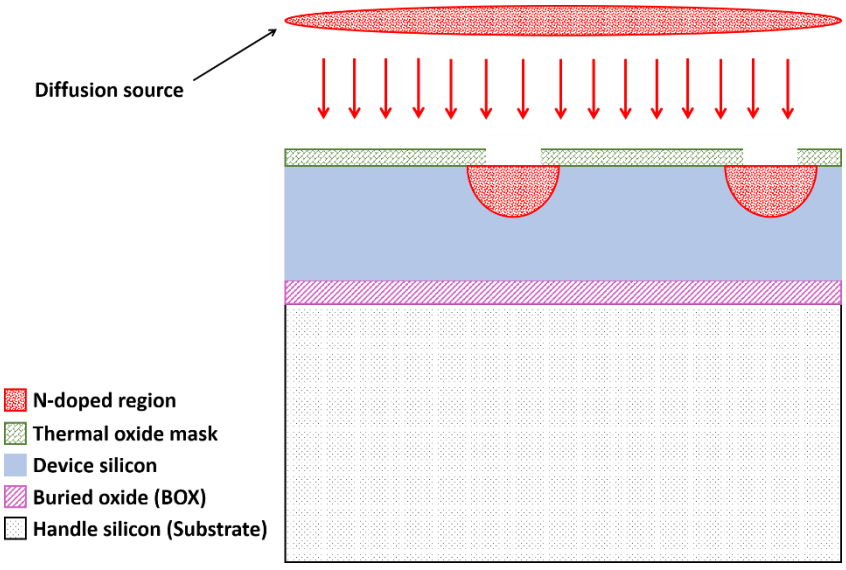

Figure 4-4: N-doped regions are formed in the *p*-type silicon device through thermal diffusion.

Subsequently, the oxide layer is removed to prepare the surface for the next deposition step and characterization of formed junctions (Figure 4-5). The resistivity of doped regions are measured with a 4-point probe to be about 0.001 Ω-cm.

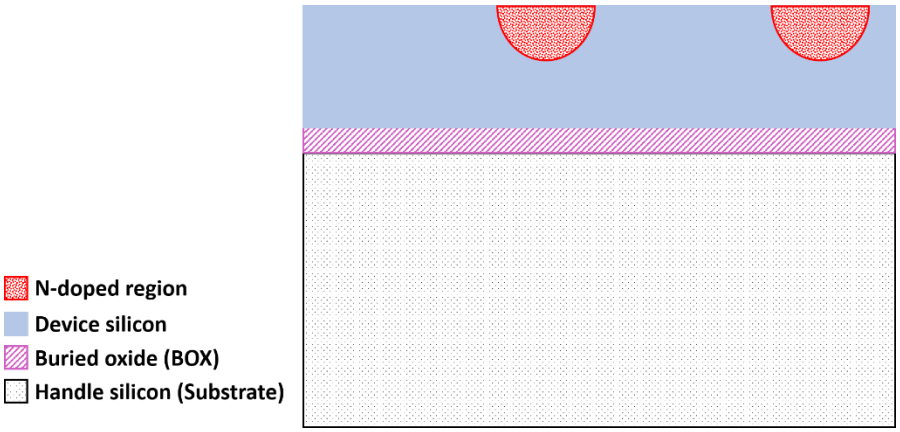

Figure 4-5: SOI wafer after removing of the oxide layer.

To find the junction depth and obtain the concentration profile of doped layer, Secondary Ion Mass Spectrometry (SIMS) is used, which is a precise technique. Figure 4-6 illustrates a SIMS tool and the inset shows the loaded chip under test.

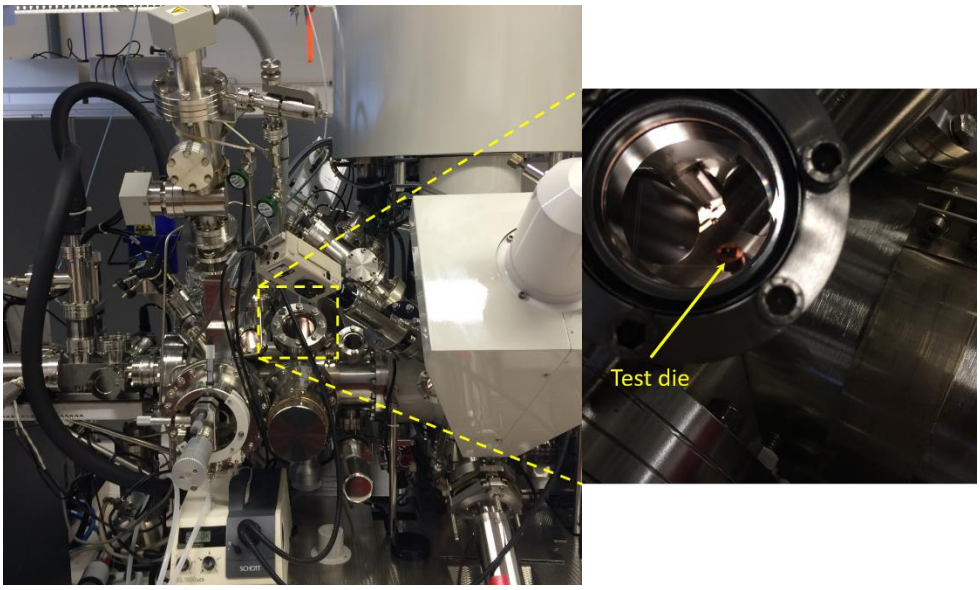

Figure 4-6: Secondary Ion Mass Spectrometry (SIMS) setup.

Obtained concentration profiles from SIMS are provided in Figure 4-7. The metallurgical junction depth is determined by SIMS to be ~1.3 µm.

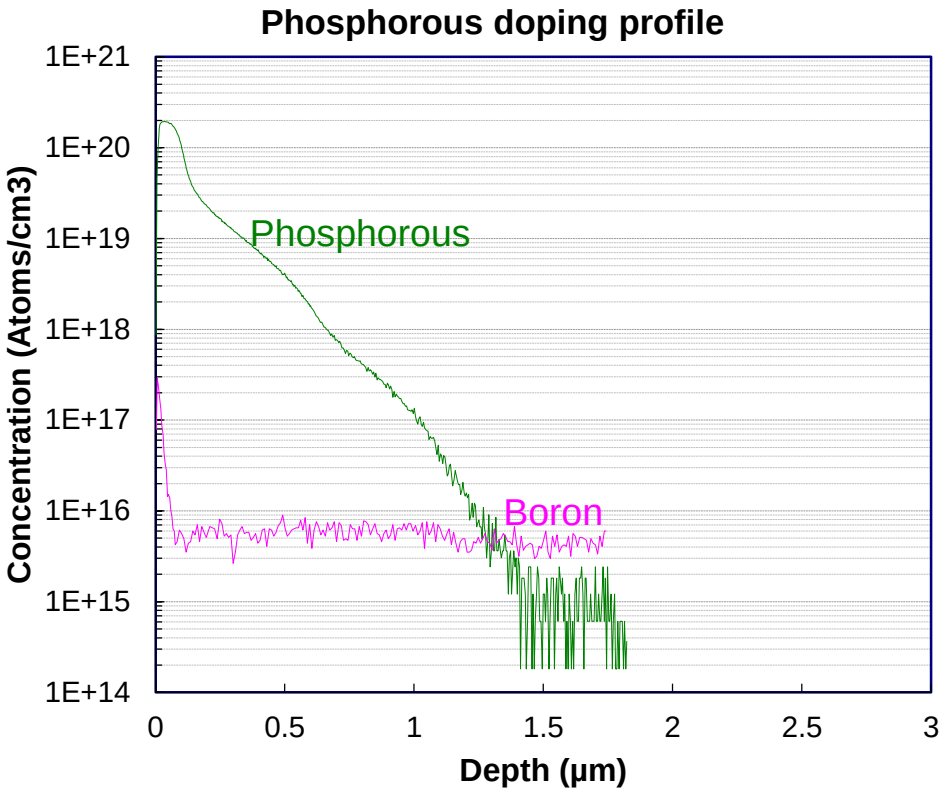

Figure 4-7: SIMS profiles of Phosphorous and Boron concentrations.

4.3. Passivation

In silicon *p-n* junctions with large exposed junction area, surface recombination can have a significant impact on the reverse saturation current. Therefore, passivation of doped regions is essential for the improvement of characteristics of a *p-n* junction. Passivation with silicon dioxide films is the most common method for passivation that has been used in industry. However, for this SOI process, the passivation layer needs to withstand the HF during the release step. Thus, silicon nitride is selected as the suitable passivation film. A Low Pressure Chemical Vapor Deposition (LPCVD) furnace is used to deposit low stress and stoichiometric silicon nitride film onto wafers (Figure 4-8). Silicon nitride layer is used as a passivation layer, electrical insulator and structural layer. The nitride film is deposited using dichlorosilane or DCS (SiH_2Cl_2) and ammonia (NH_3) in a flow ratio of 60:10 (DCS:NH_3) at a temperature of 835 °C and pressure of 200 mTorr for 43 minutes. The thickness of the deposited Si_3N_4 was measured to be about 115 nm with

an average tensile stress of near zero pascal across each wafer. By adjusting the process parameters (i.e. DCS to NH_3 ratio, pressure, total flow and temperature), it is possible to deposit films with considerably low tensile stress levels. As the structural layer of devices, films with appropriate internal tensile stress are beneficial for the stability and better mechanical properties of the device after release.

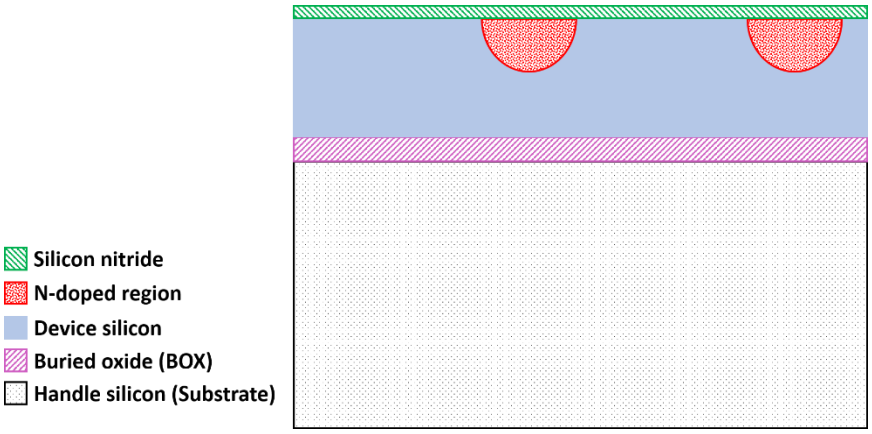

Figure 4-8: A layer of silicon nitride is deposited on top of the device silicon through LPCVD.

4.4. Silicon patterning

The next step is to selectively pattern the device silicon with the second mask level to define the geometry and structure of designed micro-devices. Anisotropic wet etching based on alkaline solutions (e.g. KOH, NaOH, TMAH or EDP) is one of the common technologies for anisotropic etching of silicon at higher etch rates with excellent selectivity towards the mask material [127]. However, the necessity of transferring complex geometries into a silicon wafer limits the capability of such techniques in MEMS technology. On the other hand, a fluorine- or chlorine-based plasma etching is capable of high accuracy silicon micro-machining and it is independent of crystal orientation. Etch rates are typically below 1 µm/min and selectivity is limited depending on the masking material. The latter requirement involves using hard metal masks such as Ni or Cr.

After consideration of our design requirements and experimenting with our dry etching tools, this step is performed using plasma dry etching of nitride and silicon layers in a Reactive Ion Etching (RIE) tool using a chemistry of SF_6/O_2 gases. The use of

materials such as photoresist, silicon oxide, silicon nitride and chromium with various thicknesses were investigated to find a mask material that provides excellent selectivity during the RIE process. Chromium is chosen as the hard mask for etching through the nitride and device layer to the buried oxide underneath. Trying different thicknesses of sputtered Cr suggested that a Cr thickness in the range of 320 nm to 350 nm is required for etching of a 3.5 µm-thick silicon layer. Considering the worst case scenario, a layer of Cr with a thickness of 350 nm was deposited through a DC sputtering process to serve as the mask layer for the dry etch process. The Cr layer was patterned with the second-level photomask through a photolithography process followed by a wet etching of the chromium for 5 minutes. Figure 4-9 shows the cross-sectional view of this process.

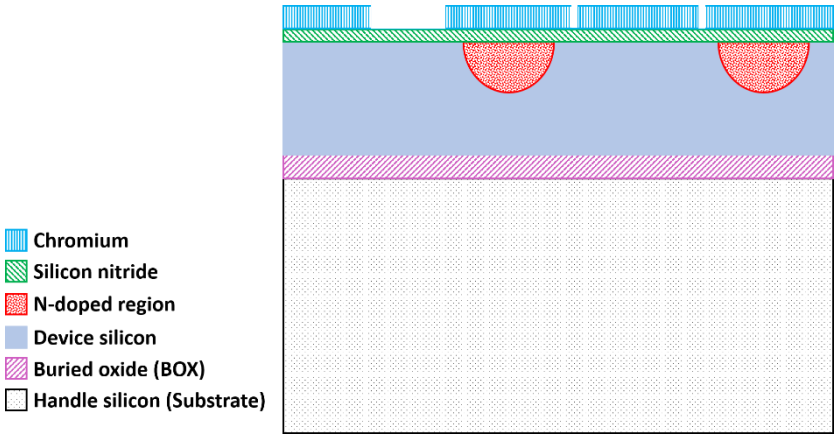

Figure 4-9: Chromium is sputtered and patterned as a hard mask for the following dry etching of nitride and device silicon layers.

Next, the nitride and silicon layers were etched with RIE to transfer the Cr mask patterns to the silicon layer and build the structures of the designed micro-devices (Figure 4-10). Different RIE recipes were examined for etching of the nitride and silicon layers. The objective was to obtain etching profiles with vertical sidewalls and minimum undercut. Effect of process parameters such as pressure, power and mixture of reactive gases on the etching profile were investigated. It was noted that to obtain a highly anisotropic profile high power and low pressure are required. However, a higher power means less selectivity to the masking material and a lower pressure translates to a slower etch rate.

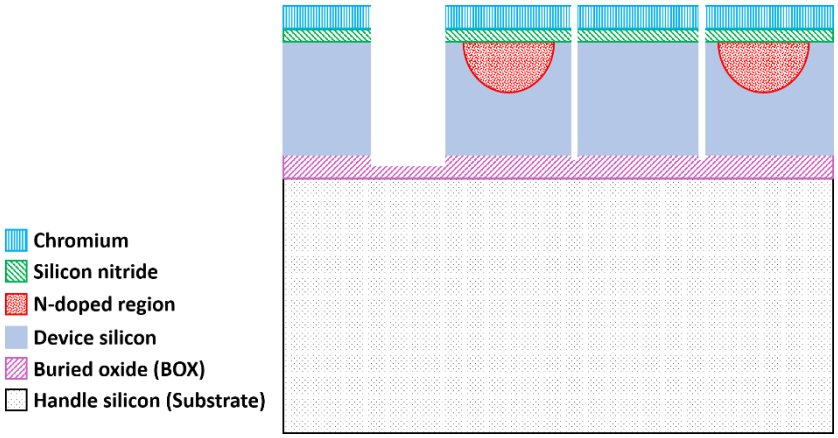

Figure 4-10: Nitride and device silicon are etched with reactive ion etching through a chromium mask.

As a preliminary test, the provided RIE recipe of Table 4-2 was used to etch the nitride and silicon device layer of a monitor wafer.

Table 4-2: Parameters of the RIE recipe for etching of silicon and nitride

Parameter	SF_6/O_2	Pressure [mTorr]	Power [W]	Etch rate (Si) [nm/min]	Etch rate (Nitride) [nm/min]
Value	12/7	30	200	380	270

Figure 4-11 shows SEM images of the obtained silicon etching profiles. The sidewalls were sloped and an undercut of about 0.75 µm was measured for vertical etching of 2.5 µm-thick silicon layer.

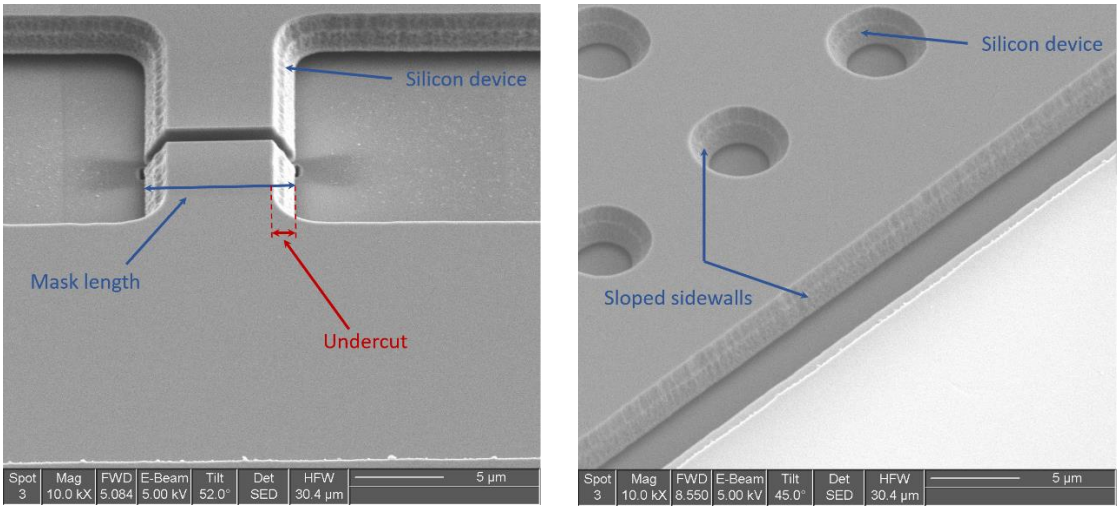

Figure 4-11: Silicon dry etching profiles obtained with the recipe of Table 4-2.

To improve the dry etching profile and achieve vertical side walls, an optimized etching recipe was developed to increase the anisotropy of the etching, maximum selectivity to the masking material and minimize any undercutting of the silicon layer. Table 4-3 provides the parameters of the RIE recipe that is used to etch the nitride and silicon device layers.

Table 4-3: Parameters of the RIE recipe for etching of silicon and nitride

Parameter	**SF_6/O_2**	**Pressure [mTorr]**	**Power [W]**	**Etch rate (Si) [nm/min]**	**Etch rate (Nitride) [nm/min]**
Value	12/7	15	250	350	250

This timed dry etching of silicon is stopped once the BOX layer is exposed to avoid any further undercutting. This is a particularly challenging problem to overcome, considering the device layer thickness variations of about %15 across wafer, which is given by the manufacturer. As mentioned earlier in Chapter 2, size of capacitive transduction gaps has a significant effect on improving the efficiency of electrostatic actuation. Narrower gaps also result in a smaller motional resistance and therefore, a larger capacitive motional current. This step is very dependent on etch end-point detection and it is critical to find the optimal etch time to achieve minimal undercut in order to obtain smaller capacitive gaps.

Figure 4-12 presents the SEM images of the etched silicon layer with excellent results, which are attained for vertical side walls and minimum possible gap sizes. This etch process achieves an etch rate of greater than 350 nm/min, high selectivity to Cr mask while maintaining a minimal undercutting across a 100 mm wafer.

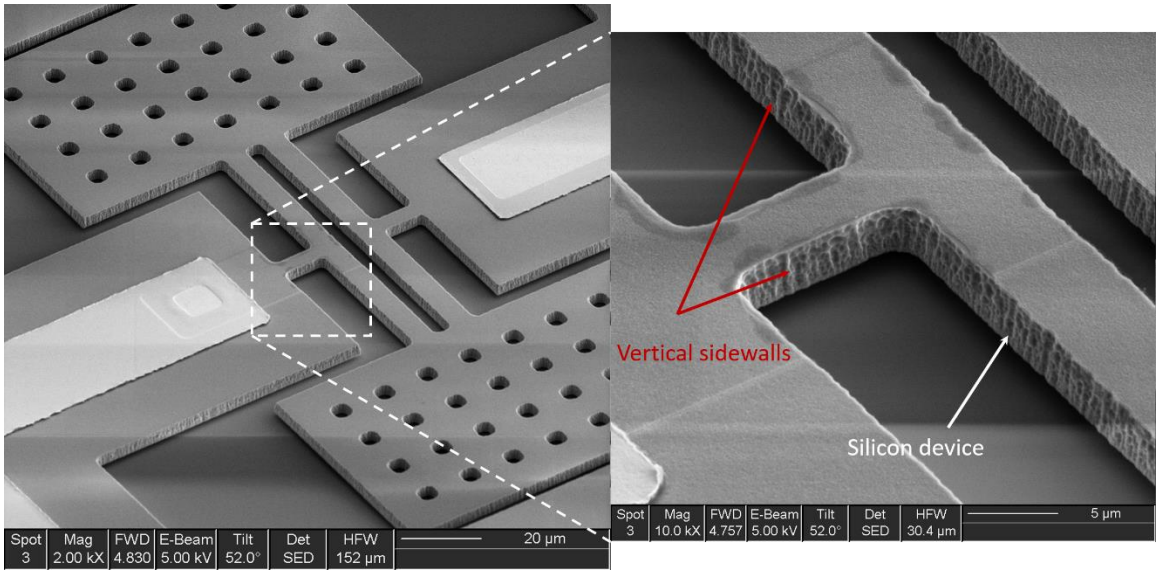

Figure 4-12: Silicon dry etching profiles obtained with the recipe of Table 4-4.

After completion of the dry etching, the Cr layer was stripped away by using a wet chromium etchant to prepare the wafer for the next patterning step (Figure 4-13).

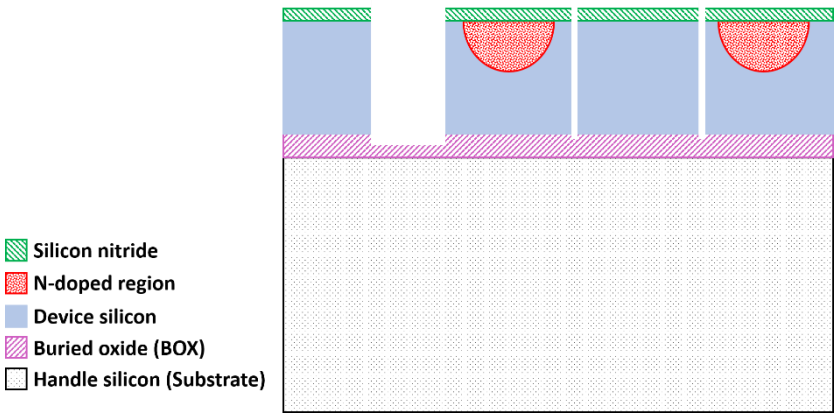

Figure 4-13: Chromium layer is removed with a Cr wet etchant after RIE step.

As it was mentioned earlier, the size of the transduction gap is a determinant parameter in fabrication of electrostatic micro-resonators. A smaller gap size translates to a higher transduction efficiency and smaller motional resistance of the resonator, which have a significant effect on the performance of the resonator. To obtain narrow transduction gaps with nanometer dimensions, milling with Focused Ion beam (FIB) was used on some test structures. Using this technique, electrostatic gaps with widths in the order of 300 nm to 1 µm were fabricated on a SOI wafer with 2 µm-thick silicon device layer. SEM images of these fabricated resonators are provide in Figure A-4 and Figure A-5 of Appendix A. However, this technique is only practical for creating gaps with smaller lengths and thicknesses. Also, this process is only suitable for fabrication of a limited number of test structures and not for batch fabrication as it is timely and costly. Other inconveniences include local contamination with gallium ions, possible amorphization of silicon and deposition of the removed material on the gap surfaces.

4.5. Metallization

Metallization is the next step in the fabrication sequence to produce conductive interconnections and bonding pads. To make contacts to the silicon device layer underneath the nitride layer, contact vias are etched through the nitride layer using a series of photolithography and dry etching pattering steps with the level-3 photomask (Figure 4-14).

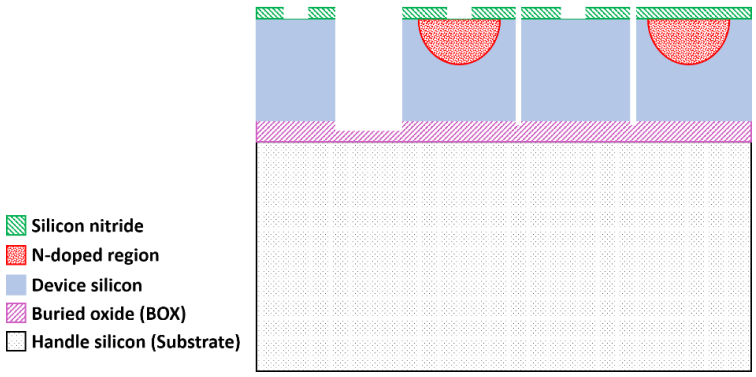

Figure 4-14: Silicon nitride layer is selectively etched with RIE to create through contacts to the device silicon underneath.

The nitride layer is patterned using photolithography with third-level photomask followed by dry etching of the nitride film using RIE with the recipe that is provided in Table 4-4.

Table 4-4: RIE recipe for creating contact vias in the nitride layer.

Parameter	CF_4/O_2	Pressure [mTorr]	Power [W]	Etch rate (Nitride) [nm/min]
Value	40/4	100	200	150

These contact vias provide access to both *n*-type and *p*-type regions underneath for the following metallization step. A SEM image of such contact vias is shown in Figure 4-15.

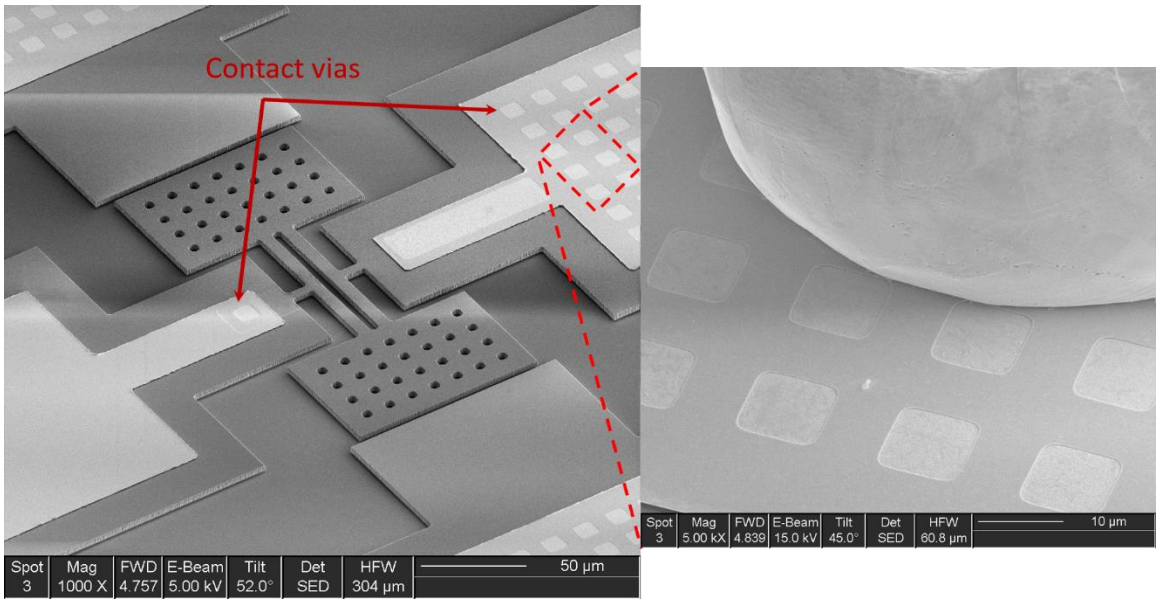

Figure 4-15: Contact vias through the nitride passivation layer.

Next, the exposed parts of the BOX layer are locally removed using a vapor HF process to allow for electrical contact to the handle wafer (Figure 4-16).

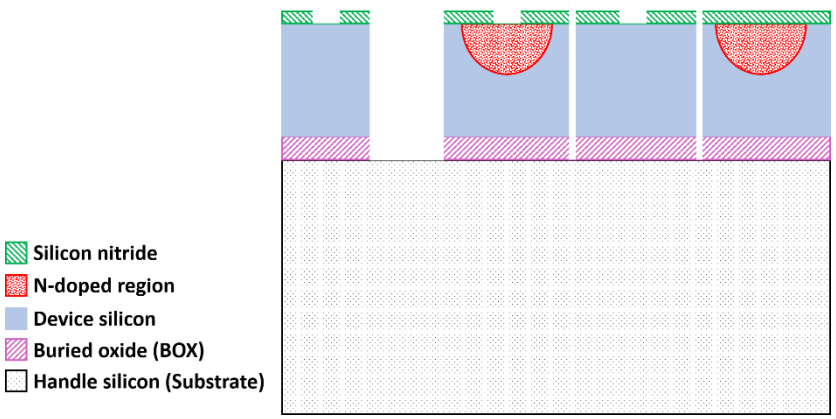

Figure 4-16: Selective removal of BOX layer in exposed areas.

The suitable metal film for this SOI process should satisfy the following requirements: 1) compatibility with the following release step using vapor HF, 2) good ohmic metal contact with both *p*-type and *n*-type silicon, 3) good adhesion with silicon and silicon nitride and 4) being easily wire bondable. Gold or a combination of Gold/Chromium is the typical metal option for most of the MEMS processes as the only requirement of such processes is to achieve electrical contacts to mechanical devices. Use of metals such as Chromium and Gold/Chromium were experimented in earlier SOI processes of this research. These metal contacts to silicon exhibited characteristics similar to that of Schottky junctions. Thus, we investigated the use of Aluminum and alloys of Aluminum for a metal contact. Aluminum is one of the most common metal films used in CMOS and IC fabrication that meets the given requirements. However, pure Al suffers from shortcomings such as reliability problem and spiking. To rectify these issues, alloys of Al with 1-2% added Si have been used in literature [126].

In this work, an alloy of Al with 1% added Si ($Al_{99}Si_1$) is chosen as the metal film. Lift-off metal patterning is used as the process for defining metallic contacts, electrical routings and bond pads because of its advantages over the process of deposition and etching of the metal. Before the lift-off process, SOI wafer goes through both RCA 1 and RCA 2 cleaning steps to remove any organic or metallic contaminations from its surface. Details of the lift-off process is provided in Appendix A of this thesis. The process employs a thick bi-layer (~4 µm) resist comprised of Shipley 1813 and Shipley 1827 photoresists. Patterning and developing of this bi-layer is done with the forth-level photomask to define

the conductive routings and pads. Lift-off process is continued by thermal evaporation of the Al film. Evaporation is chosen for AlSi 1% because it results in a more directional deposition in comparison with sputtering. Using a line-of-sight deposition process offers the easier removal of the resist as it avoids the deposition of metal on the sidewalls of the resist. A 250 nm $Al_{99}Si_1$ is deposited through the lift-off process to make metallic contacts to silicon device layer (Figure 4-17).

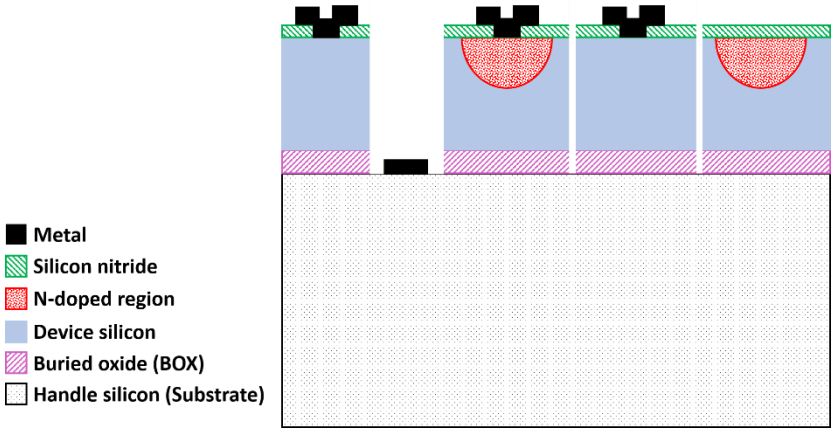

Figure 4-17: Metal layer is deposited and patterned through lift-off.

Wafers are annealed at a temperature of 475 °C for 40 minutes to promote the quality of contacts and to improve the low-resistance contact between the deposited $Al_{99}Si_1$ and the *p*-type and *n*-type silicon. As it is shown in Figure 4-18, pinholes appear in the Al film after this annealing step.

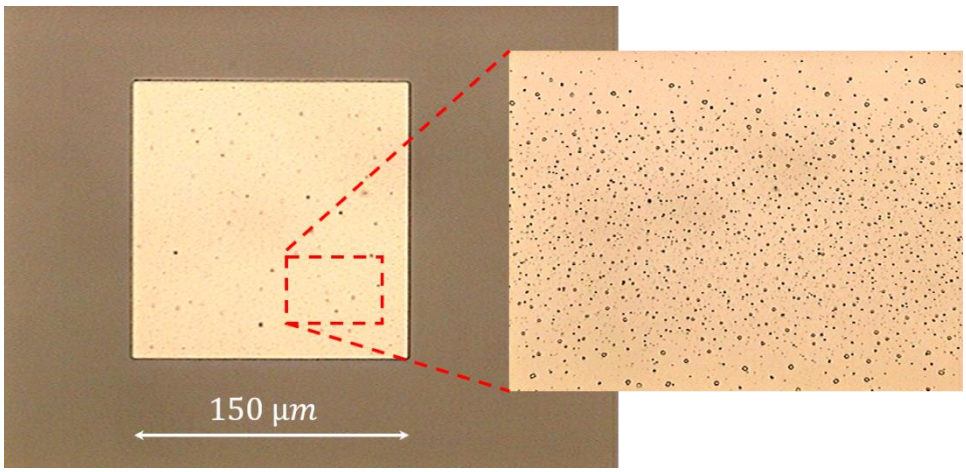

Figure 4-18: Pin holes in the Al film after annealing.

To evaluate the quality of contacts, the resistivity between two metal pads are probed with a Keithley 4200 parameter analyzer for test structures of Figure 4-19.

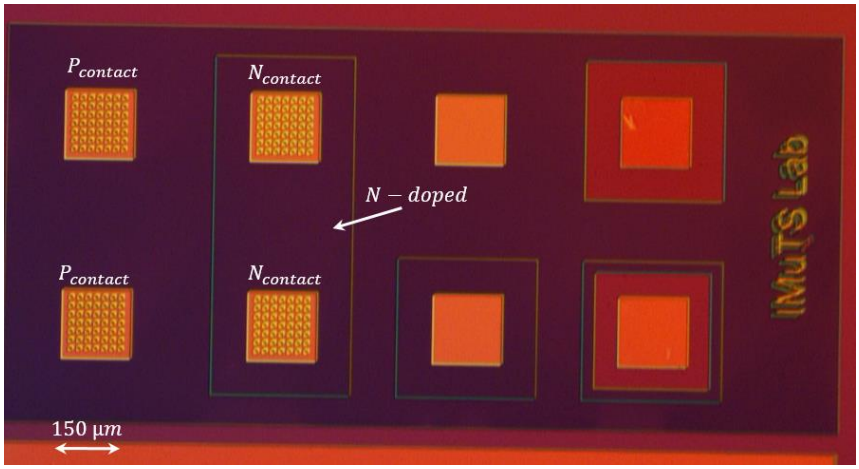

Figure 4-19: Test structures for characterization of contact resistance.

Figure 4-20 illustrates the I-V characteristics of $N_{contact} - N_{contact}$ before and after the annealing. As it can be seen, the contact between the $Al_{99}Si_1$ and heavily doped N-region is an ohmic contact with a low resistivity of about 30 Ω.

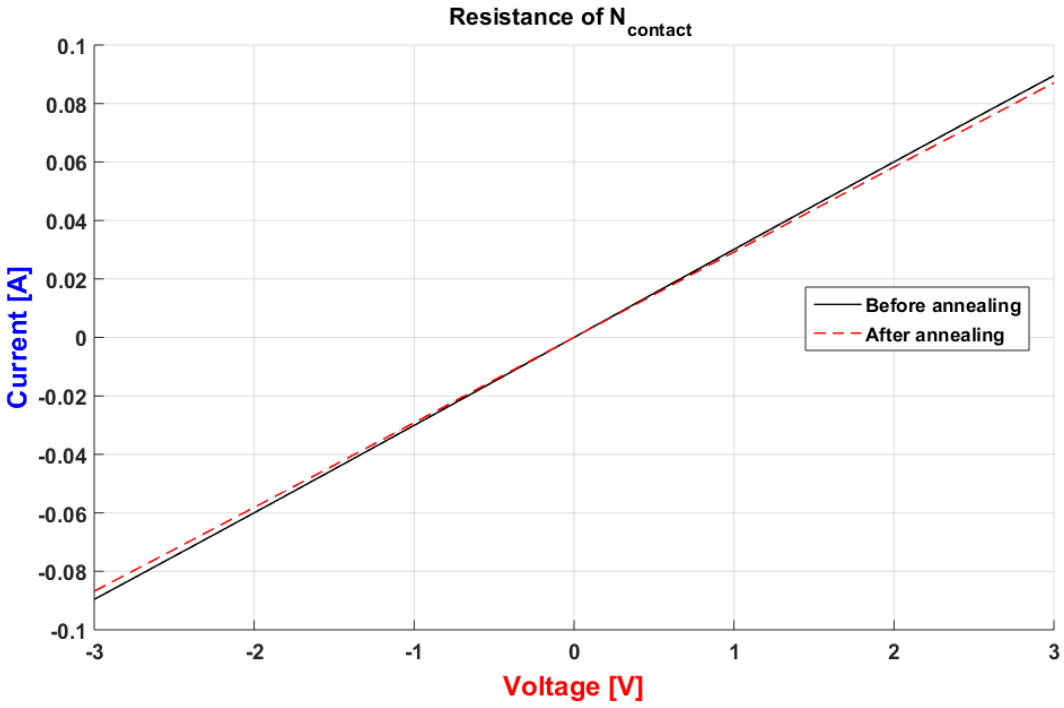

Figure 4-20: Measured electrical characteristic between two $N_{contact}$ before and after annealing.

Also, the measurement results of the resistivity between two $P_{contact}$ pads before and after annealing are shown in Figure 4-21and Figure 4-22, respectively. According to the obtained results, the contact resistivity of $Al_{99}Si_1$ to the lightly doped *p*-type silicon has a nonlinear characteristics before annealing. The post annealing measurements show that the sintering improves the contact resistivity about three orders of magnitude (from ~10 MΩ to 17 kΩ) for contacts to the *p*-type silicon. These characterizations verified that $Al_{99}Si_1$ provides a good ohmic metal contact to both *p*-type and *n*-type regions of the SOI wafer.

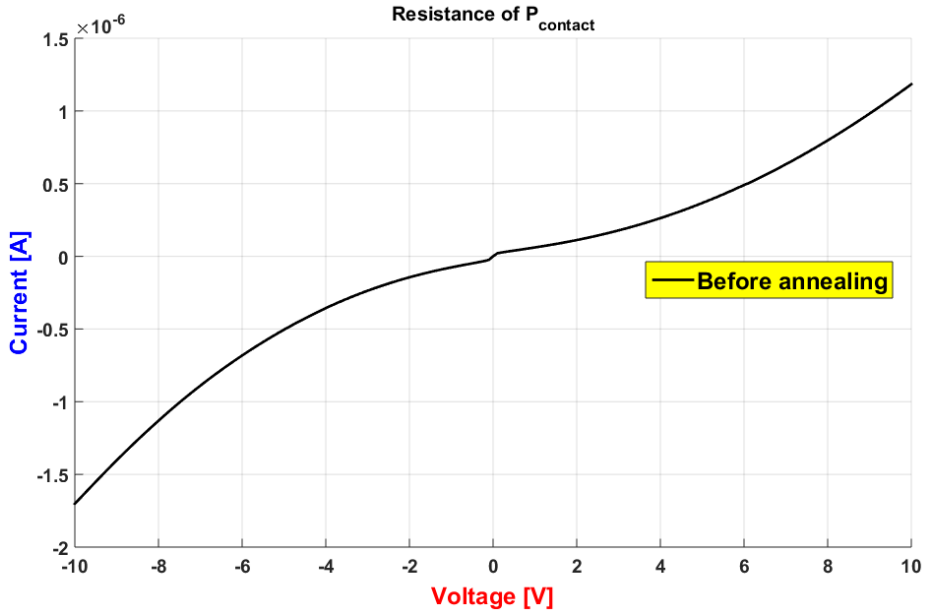

Figure 4-21: Measured electrical characteristic between two $P_{contact}$ pads before annealing.

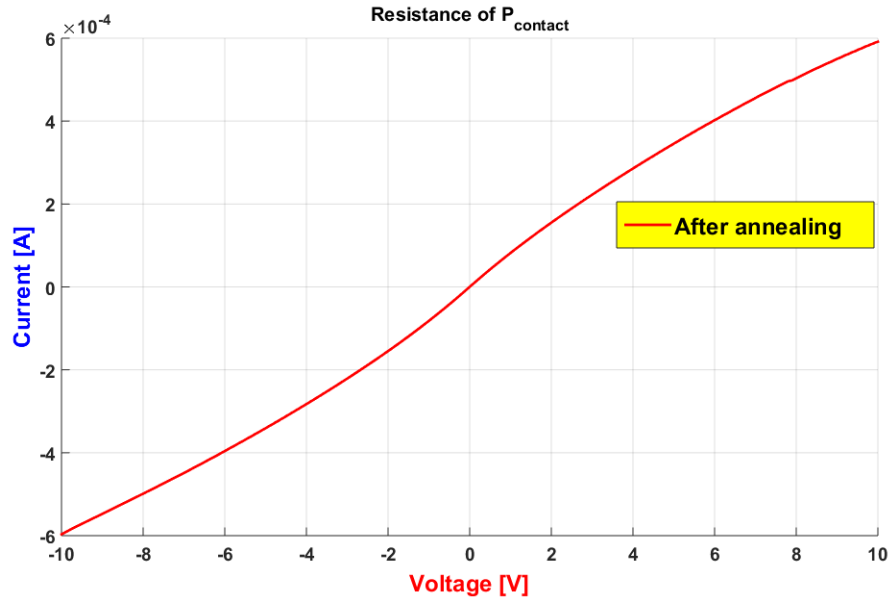

Figure 4-22: Measured electrical characteristic between two $P_{contact}$ pads after annealing.

4.6. Release

Subsequent to the successful metallization step, the SOI wafer is diced into dies of 7 mm x 7 mm with a mechanical dicer (Figure 4-23). The next step is to remove the BOX layer selectively and release the structures.

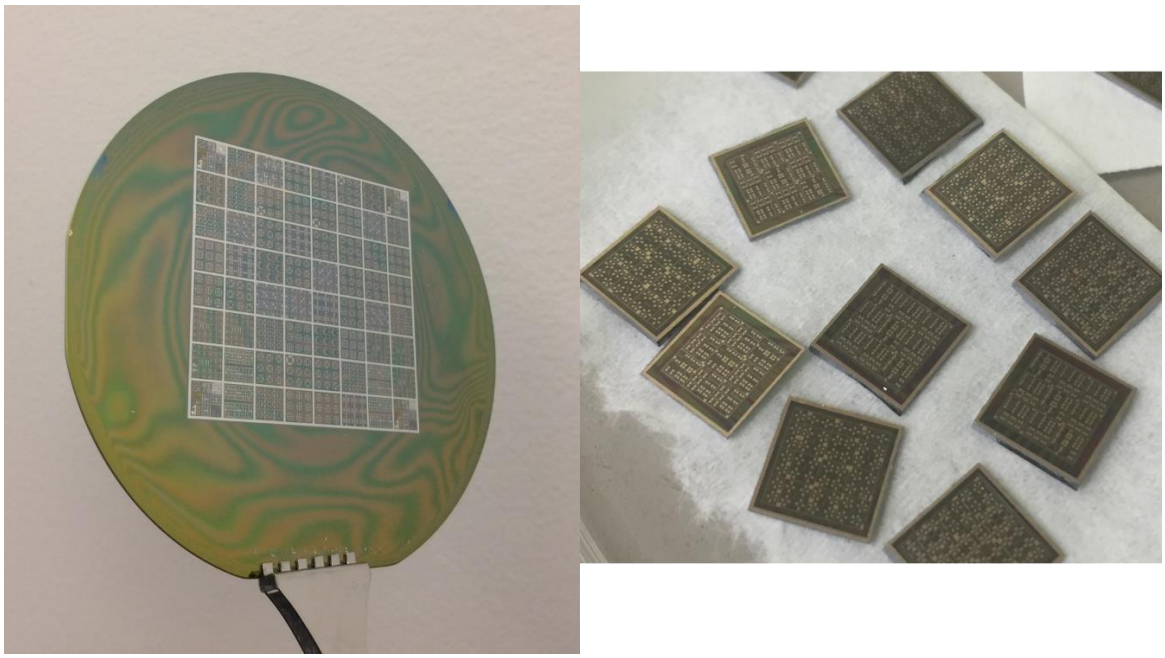

Figure 4-23: SOI wafer is diced into smaller dies after the metallization.

The processing step for the etching and releasing of micro-devices is shown in Figure 4-24. This step includes a controlled selective etching of the sacrificial BOX layer to freely suspend the moving parts of the structure.

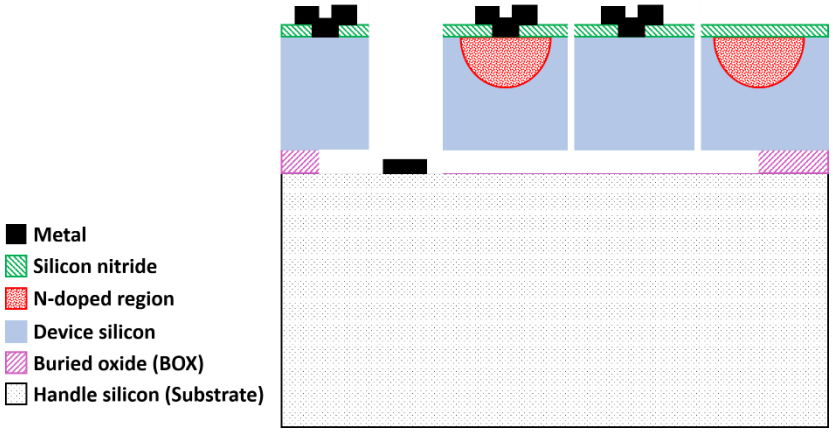

Figure 4-24: Release of the sacrificial BOX layer.

Release of micro-structures without the subsequent sticking of the freed structures to the substrate is one of the key challenges in surface micro-machining. This work uses HF vapor for releasing to avoid stiction and benefit from its compatibility with the metal film. The etching tool used in this work is a commercially available vapor phase etcher from idonus with a heated sample holder. The process runs at atmospheric pressure and works based on the evaporation of HF 48% solution, which forms a saturated HF environment for the sample. The oxide etch rate can be controlled by adjusting the sample holder temperature. A higher sample temperature results in a reduced etch rate. A temperature of 35 °C was found to provide the optimized etch rate for this step. Etched samples are inspected with an optical microscope during the etching process to monitor the progress of release. Figure 4-25 shows the optical graph of a sample during the etching process with BOX layer partially removed underneath the device structure.

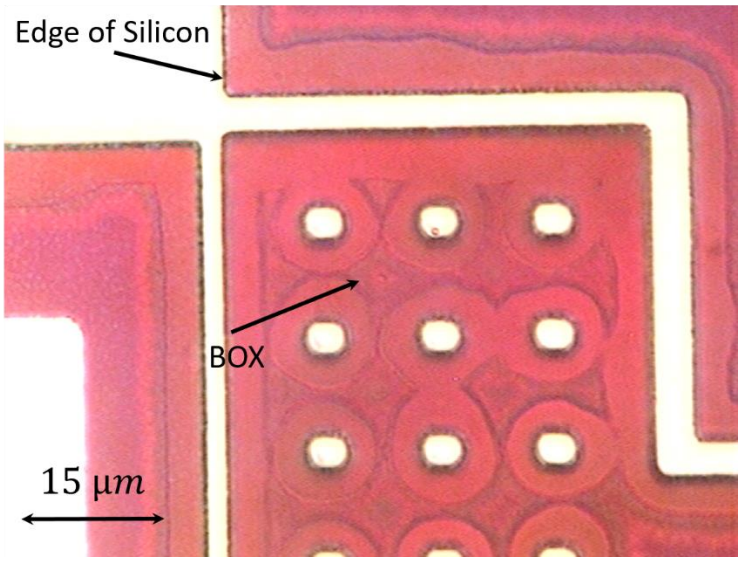

Figure 4-25: Removing of the BOX layer with HF vapor.

IR microscopy and Nomarski Interference Contrast (NIC) methods are used to inspect the lateral etch of the sacrificial BOX layer during the release process and to confirm the completion of release. A lateral etch of about 20 µm of the BOX layer in 35 minutes was sufficient to completely remove the oxide underneath the moving parts. A fully released micro-resonator using HF vapor is shown in Figure 4-26.

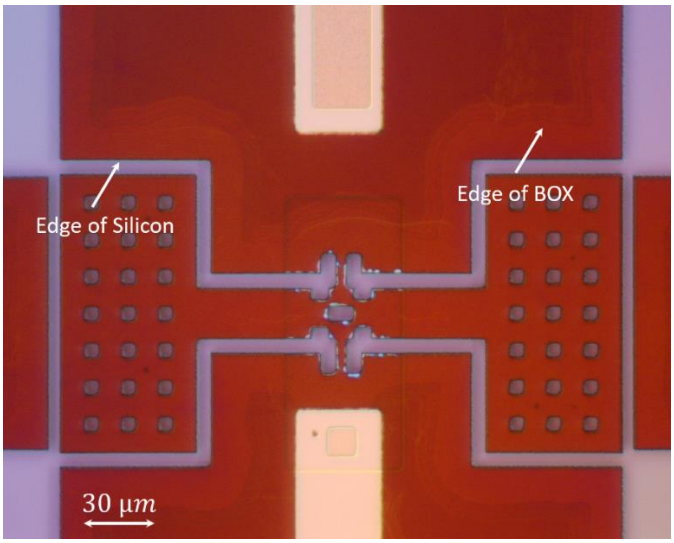

Figure 4-26: Fully released structures at the end of the release process.

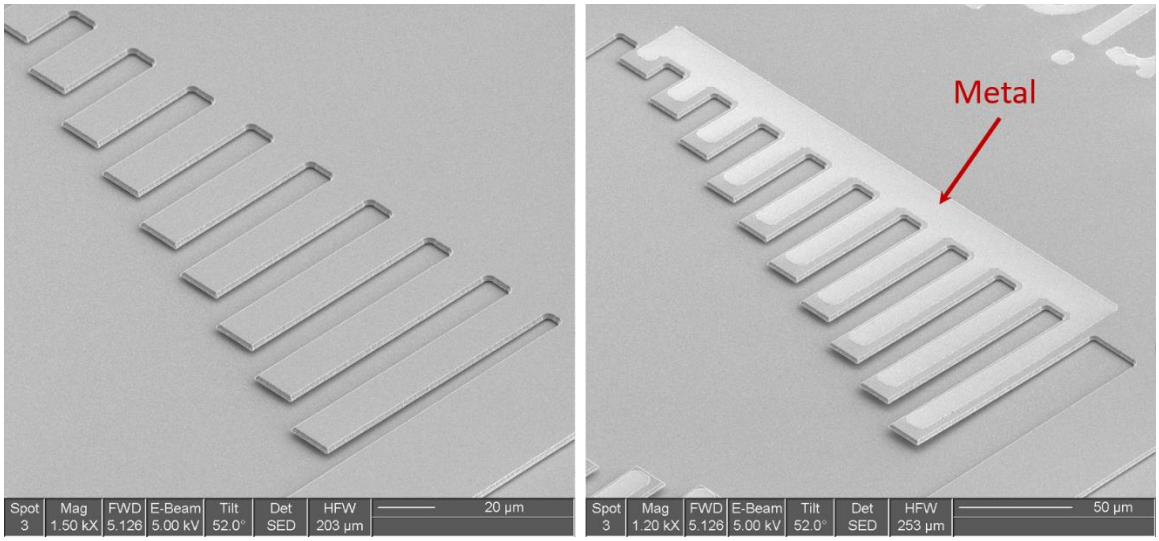

Figure 4-27: Silicon and bimorph cantilevers for characterization of the release.

Test structures such as cantilevers, bridges and hanging plates were inspected with optical microscope and SEM to observe any possible bending of such structures after the release step. Figure 4-27 demonstrates silicon cantilevers with different lengths and with a top metal layer after the release. Plates as big as 50 µm x 50 µm are fully released without the need of any etch holes. One of the important advantages of using HF vapor was the minimal attack of the HF on the metal and silicon nitride films. Also, no residue was left on the substrate or other surfaces at the end of this step.

4.7. Packaging

Following the releasing of the fabricated devices, some of the dies comprising of micro-resonators should be packaged for characterization purposes. Each individual die is mounted inside a Dual-In-Line (DIP) ceramic package and attached with an adhesive and conductive epoxy (Figure 4-28).

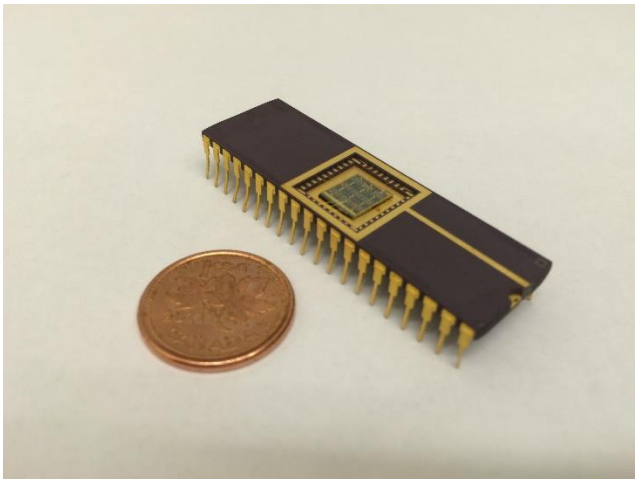

Figure 4-28: A DIP ceramic package containing the fabricated die.

The next step is to provide electrical wiring and interconnects between the die and its external components to it. Wire bonding with gold wires is used to connect the bonding pads on the die to the package terminals (Figure 4-29).

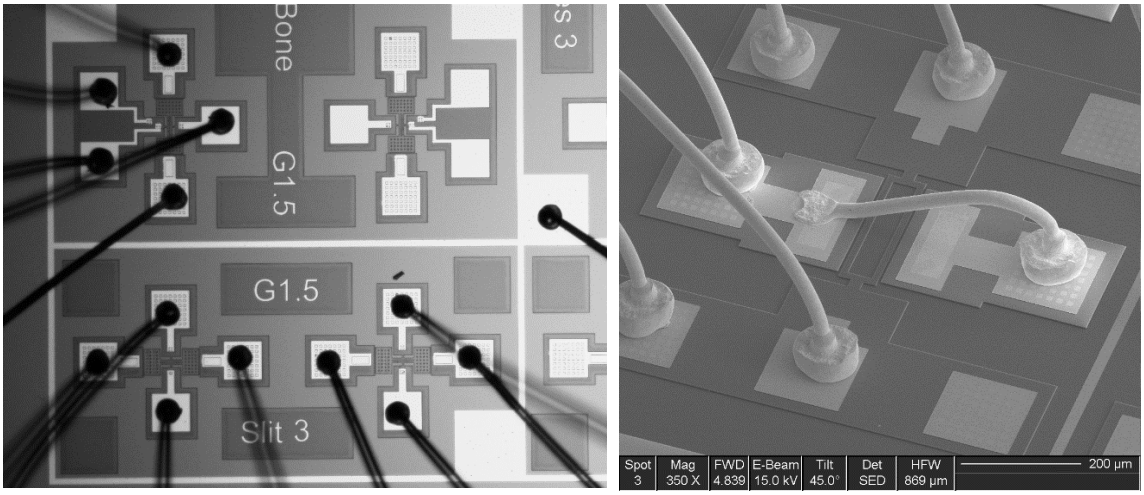

Figure 4-29: Optical and SEM images of the wire bonded micro-devices.

At the end, packages are covered with a metal lid to finalize the fabrication process. It is worth mentioning that packaging and wire bonding of the fabricated micro-resonators are necessary to reduce the parasitic and noisy effects of extra cables, probes and uncertainties resulted from them during the testing and characterization of such micro-devices.

Chapter 5. Micro-machined device design

This chapter presents the details of the structure of the micro-resonator that was designed and fabricated as a prototype for resonance measurements through employing piezojunction effect. In addition, working principles and mechanical analysis of the resonator are provided to elaborate on the device operation.

5.1. Device structure and design

The resonator is actuated using electrostatic forces. The vibrations are then measured using integrated piezojunction sensors. Electrostatic actuation is chosen because of its simplicity of design, ease of fabrication and near zero power consumption. Taking into account the limitations of the selected mechanisms, the designed structure is required to provide an effective electrostatic transduction at the input to induce a reasonable force on the body of the resonator, and therefore, larger displacements. Also, the quality factor of the resonator should be high to amplify displacements at the output in order to have a strong piezojunction signal.

Throughout this research, various resonating structures including rectangular beams, square plates and other structures in different flexural and bulk mode shapes were designed, fabricated and examined to find an effective structure for employment of piezojunction mechanism in a micro-resonator. Although the flexural-mode devices were able to provide larger displacements, their lower quality factor in comparison with the values for bulk-mode resonators was a constraint in their effectiveness for purposes of this thesis. One of the studied structures was a so-called dog-bone structure with an embedded *p-n* junction, which will be the focus of this thesis. A schematic view, cross-section and 3D solid model of the designed dog-bone resonator and a summary of the important design parameters are presented in Figure 5-1.

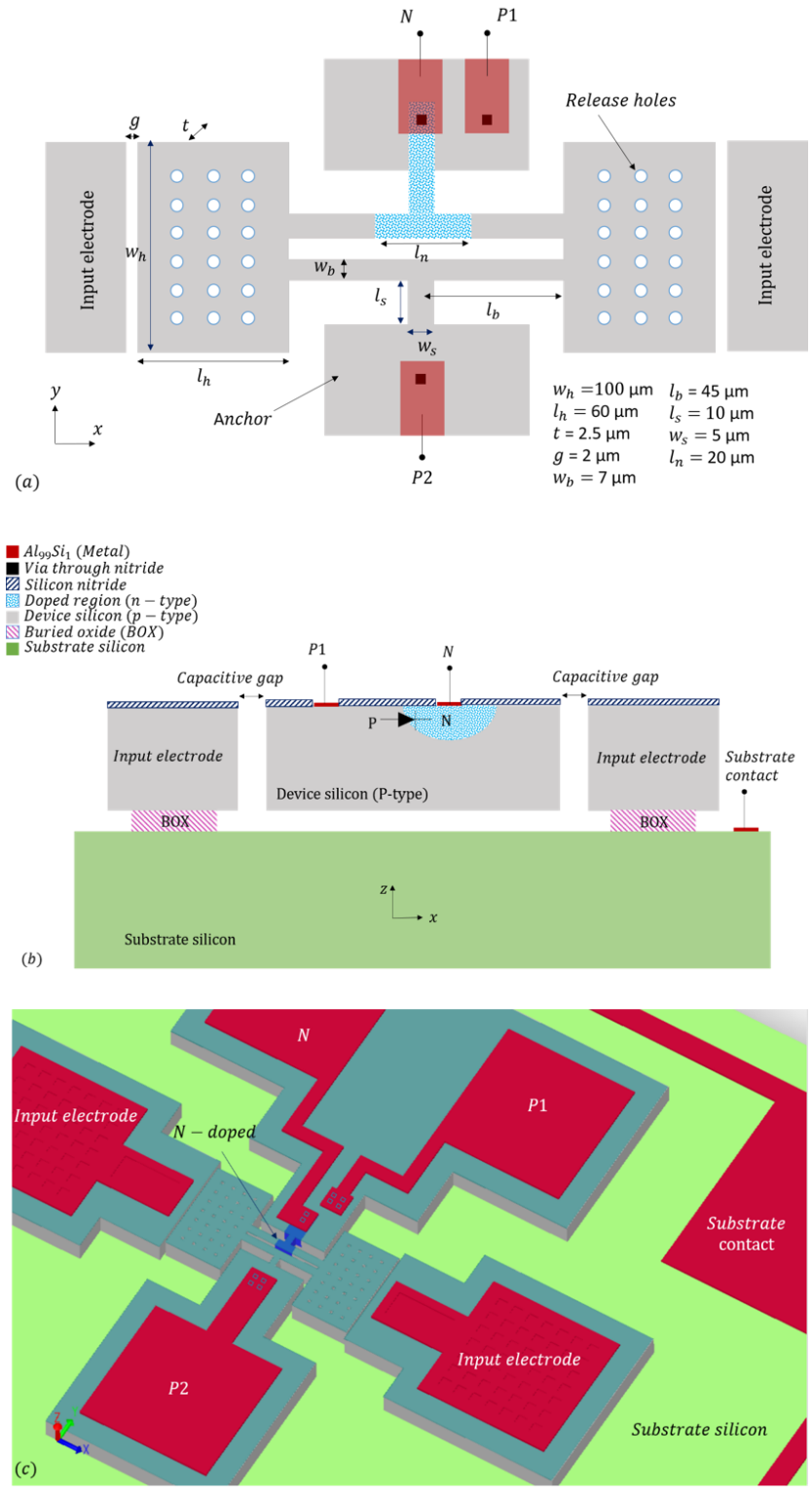

Figure 5-1: Dog-bone micro-resonator (a) top-view schematic of device structure and geometris, (b) cross-sectional view and (c) 3D solid model of the resonator.

The structure consists of two end pieces connected by two straight beams. At both ends of the structure, electrodes (i.e. Input electrodes) have been placed over 2 μm capacitive gaps for electrostatic drive. The purpose of spaced etch holes on the end pieces is to expose the BOX layer underneath of the micro-structure to the HF vapor during the release process.

By applying the input drive voltage, comprising a DC (V_P) and an AC ($v_{ac}\sin\omega t$) components to the electrodes, an electrostatic force (F_{in}) is generated between the resonator body and input electrodes. This electrostatic force at the frequency of the AC signal can be expressed as [30]:

$$F_{in} = \frac{1}{2}\frac{\partial C}{\partial x}(V_P + v_{ac})^2 \tag{5.1}$$

where $\frac{\partial C}{\partial x}$ is the change in the electrode to resonator capacitance per displacement. The electrostatic force at the frequency of the AC signal is:

$$F_{in,ac} = V_P v_{ac}\frac{A_e \epsilon}{g^2}\sin\omega t \tag{5.2}$$

where A_e is the effective area for electrostatic transduction; ϵ is the permittivity of the gap material and g is the gap between the electrodes and resonator body. This force produces a uniform longitudinal stress (σ_{xx}) along the connecting beams that is given by

$$\sigma_{xx} = \frac{F_{in,ac}}{2A_{beam}} \tag{5.3}$$

where A_{beam} is the cross-sectional area of each supporting beam. The resulting longitudinal stress modulates the sense current of the biased *p-n* junction of the resonator, due to the piezojunction effect. This piezojunction current is then measured to study the device response. Equation (5.3) suggests that with proper design, it is possible to increase the applied stress in the junction region by reducing the cross-section area of the supporting beam. However, the minimum feasible area is limited by the fabrication limits and mechanical stability of the support beams. A dog-bone shape is advantageous here because it allows to independently adjust the geometries of A_e and A_{beam} to obtain a

stronger applied stress at the input. This can partly compensate for minimum limit of the gap space (g) due to technological constraints from the fabrication process.

5.2. Device analyses

The desired mode of vibration for the bulk-mode dog-bone resonator is the extensional mode that is illustrated in Figure 5-2 schematically. In this mode, the resonator structure contracts and extends symmetrically on both sides along the length of main beams.

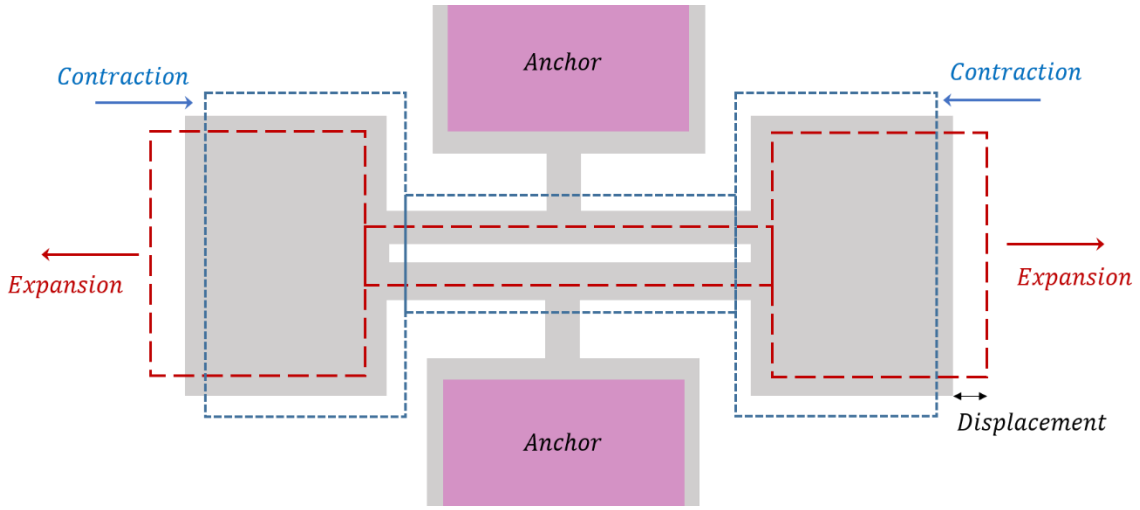

Figure 5-2: Extensional movement of the dog-bone micro-resonator.

The natural resonant frequency of this extensional bulk-mode can be determined from:

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{K_{eff}}{M_{eff}}} = \frac{1}{2\pi}\sqrt{\frac{2k_b}{M_{eff}}} \tag{5.4}$$

with,

$$k_b = \frac{Ew_b t}{2l_b} \tag{5.5}$$

where k_b, w_b, l_b, and t are the stiffness, width, length and thickness of each supporting beam, respectively. The resonant frequency of the structure with the dimensions provided

in Figure 5-1(a) is in the range of 7.05 MHz from theory and 7.12 MHz from numerical modal analysis.

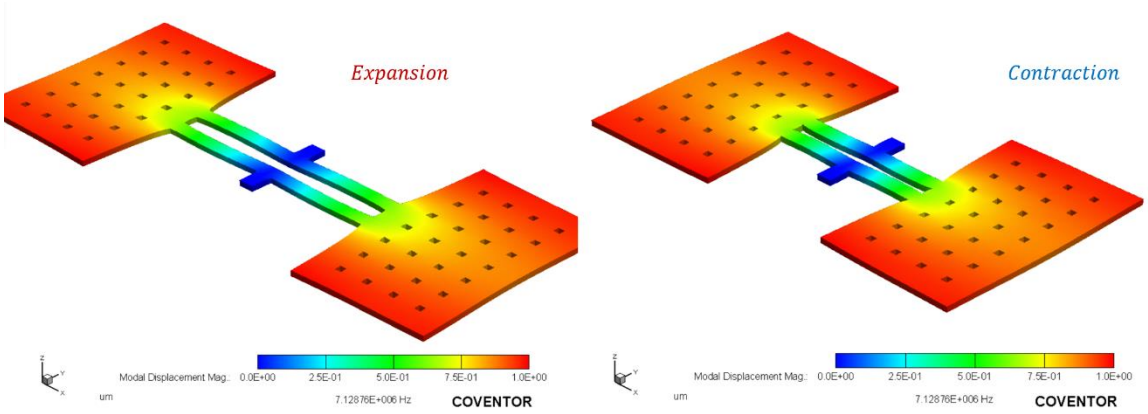

Figure 5-3: Modal analysis result for the desired mode of vibration.

The natural mode shape and frequency of the resonator were simulated with Coventorware software using modal analysis. The obtained mode shape with a frequency of 7.12 MHz is shown in Figure 5-3. Additionally, the longitudinal applied stress at the location of *p-n* junction from Equation (5.3) and static Finite Element Analysis (FEA) was calculated to be around 60 kPa.

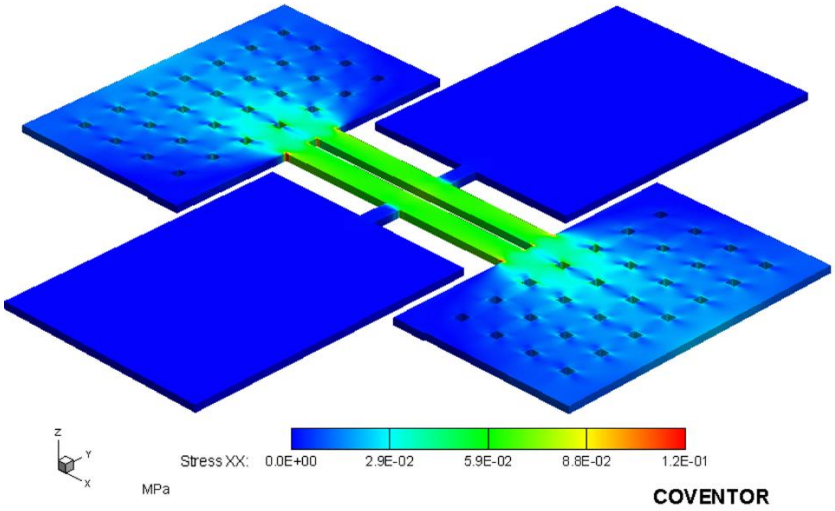

Figure 5-4: Stress distribution in connecting beams of the resonator.

By using force-voltage analogy between mechanical and electrical domains (Table 5-1), a mechanical resonator can be represented by its equivalent electrical model to allow the use of electrical network theory and circuit simulators for studying the dynamic response of the resonator [128]. As Figure 5-5 illustrates, the mechanical resonator is modeled with a series-resonant RLC electrical circuit with lumped elements, which are related to their mechanical counterparts [129].

Table 5-1: Analogy between electrical and mechanical domains.

Electrical domain	Mechanical domain
Current (I)	Force (F)
Voltage (V)	Velocity (v)
Capacitor (C)	Compliance ($1/K$)
Inductor (L)	Mass (M)
Resistor (R)	Damping (b)

The conversion of energy between electrical and mechanical domains are modeled with transformers, where η_i and η_o denote the electromechanical coupling factors at the input and output ports, respectively. The motional values of the equivalent electrical elements can be determined from absorbing the input and output electromechanical coupling coefficients:

$$R_m = \frac{\sqrt{K_{eff} M_{eff}}}{Q \eta_i \eta_o}, \quad C_m = \frac{\eta_i \eta_o}{K_{eff}}, \quad L_m = \frac{M_{eff}}{\eta_i \eta_o} \tag{5.6}$$

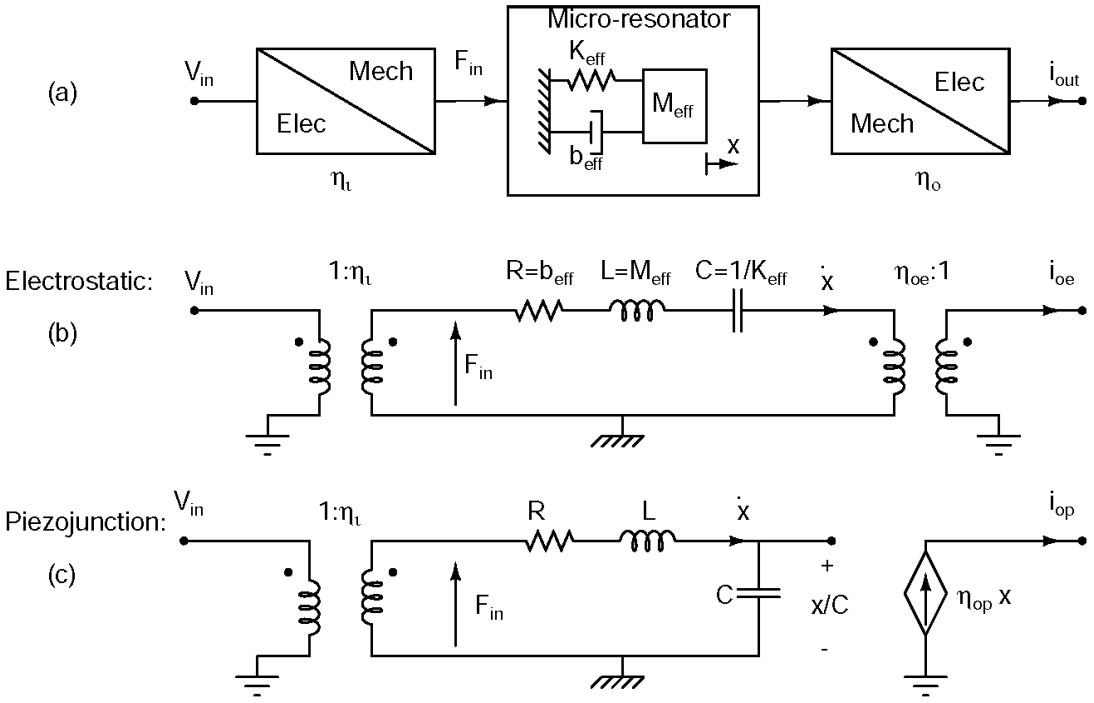

Figure 5-5: Illustration of (a) a simple mass-spring-damper model of a micro-resonator with illustration of energy transduction at its input and output ports, (b) Equivalent electrical representation of electrostatic and (c) piezojunction transduction mechanisms in a micro-resonator.

Equivalent electrical circuit representations of electrostatic and piezojunction transductions are used to compare the operation of these two mechanisms for resonance sensing. At the input port, the input signal (v_{in}), comprises DC polarization (V_P) and AC (v_{ac}) components, producing an alternating electrostatic force, which acts on the resonator body and initiates the oscillations. For the case of capacitive sensing (Figure 5-5 (b)), the output sense current (i_{oe}) is proportional to the velocity as:

$$i_{oe} = V_P \frac{\partial C}{\partial x}\dot{x} = \eta_{oe}\dot{x} \tag{5.7}$$

with $\frac{\partial C}{\partial x}$ is the rate of capacitance change at the output electrode. On the other hand, diode current (I_D) is related to the mechanical stress (σ) according to Equation (2.20). Hence, the change in diode current due to stress is calculated to be:

$$\frac{\partial I_D}{\partial \sigma} \approx -\gamma_1 I_{s0}\left(e^{\frac{V_D}{nV_T}} - 1\right) = -\gamma_1 I_{D0} \tag{5.8}$$

Assuming a uniform stress profile at the *p-n* junction region, the small-signal output current from the piezojunction sensing can be found from:

$$i_{op} = -\gamma_1 E I_{D0}\varepsilon(X) = -\frac{\pi\gamma_1 E I_{D0}}{L}\Delta x \tag{5.9}$$

where E, L, and $\varepsilon(X)$ are the Young's modulus of silicon, length of the resonator, and the generated strain at location X, respectively. Thus, the piezojunction current (i_{op}) is proportional to the induced strains in the resonating structure, and hence, is related to the displacement (Δx) at resonance. This dependence is represented in Figure 5-5 (c) through a voltage dependent current source with an electromechanical coefficient (η_{op}). η_{op} is the output piezojunction coupling coefficient found from:

$$\eta_{op} = -\frac{\pi\gamma_1 E I_{D0}}{L} \tag{5.10}$$

The electromechanical coefficient models the modulation of the DC current of diode at resonance resulting in the AC output current (i_{op}).

5.3. Device simulation of piezojunction

In this part, Silvaco Atlas tool is used to model and estimate the effect of mechanical stress on electrical characteristics of a silicon diode. Moreover, the obtained simulation results are compared against the analytical solution of Equation (2.18). Initially, process simulations are performed using Silvaco Athena tool to construct a two-dimensional device structure. The doping levels and thicknesses of layers are chosen similar to the actual values of parameters used in the developed fabrication process. Figure 5-6 demonstrates a cross-sectional view of the simulated structure.

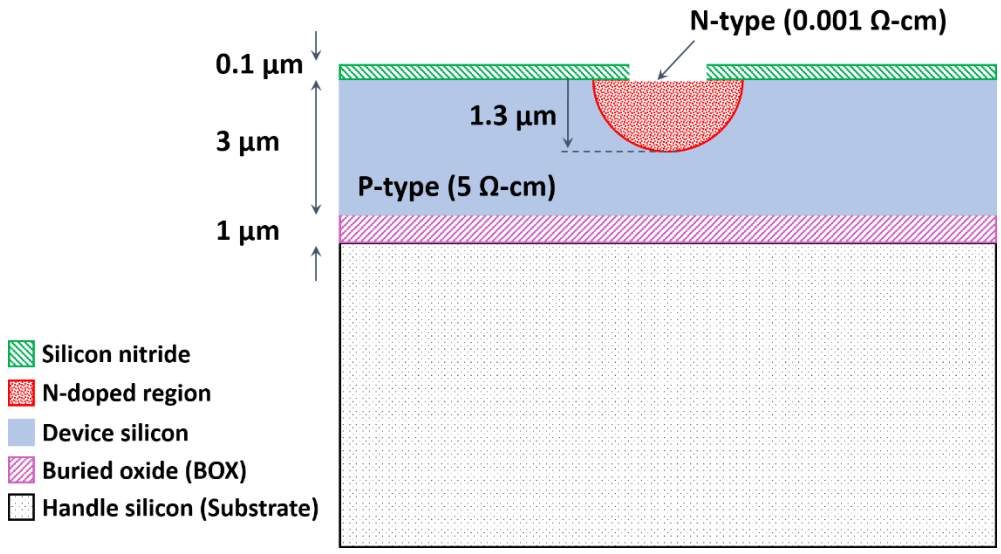

Figure 5-6: Schematic of the SOI structure, geometries and doping levels used for piezojunction simulations.

Next, the mesh, geometry, and doping level are loaded from Athena to Atlas under DeckBuild to simulate the device. To investigate the impact of mechanical stress on the electrical response of a *p-n* junction, accounting for the change of band structure and carrier mobility of silicon due to mechanical deformation are necessary. Proper calculations of the change in the strain-induced band structure are based on the deformation potential theory [130]. The implementation of the deformation potential model in Atlas is based on data and methods reported in the literature [39],[131],[131],[132]. Other methodologies such as [57] and [133] that are implemented in Atlas rely on the piezoresistivity phenomena. The employed carrier generation-recombination models are the Shockley-Read-Hall recombination model and Auger recombination model. Also, the carrier concentration-dependent low-field mobility model is used to calculate the mobility. Moreover, the stress induced mobility enhancement has been calculated using the piezoresistivity model. As well, Atlas solves the electrostatic Poisson's equation, Drift-Diffusion transport model and the carrier continuity equations altogether. By applying tensile stresses in the range of 0 to 1GPa to the structure of Figure 5-6, the effect of such stresses on I-V characteristics of the *p-n* junction in reverse-biased condition were analysed. Figure 5-7 presents the simulation results for a fixed reverse-bias voltage of 1 volt with an unstressed current density of 1.25 µA/cm^2 along the obtained data from the analytical model of Equation (2.18).

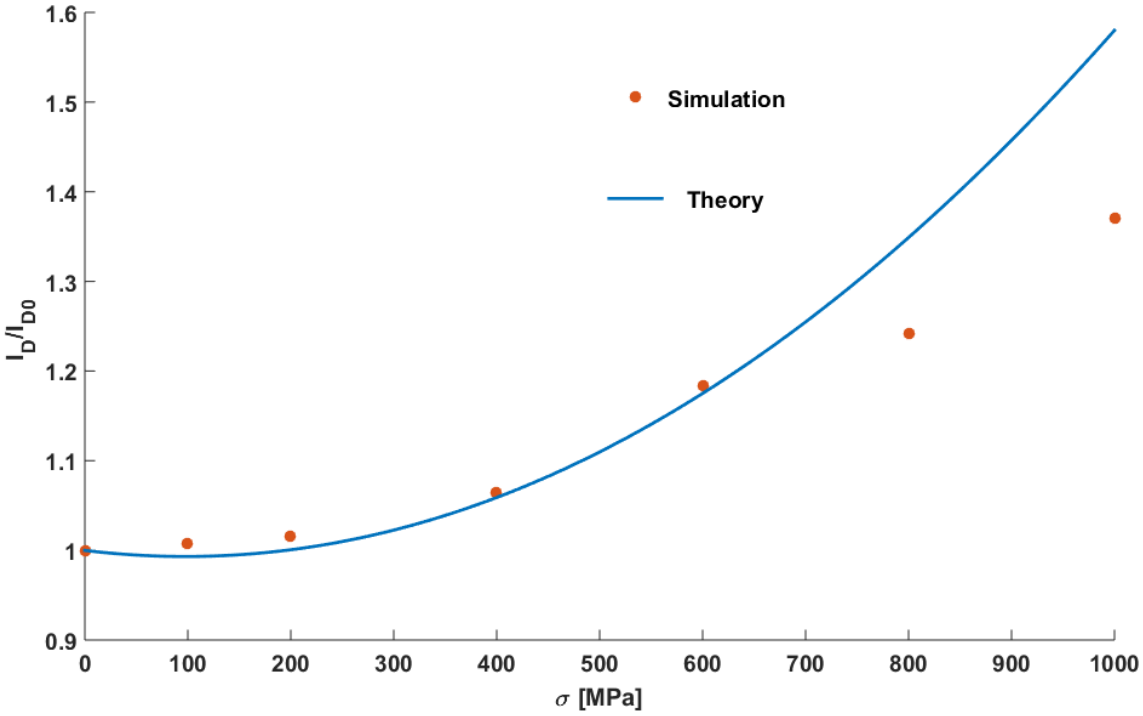

Figure 5-7: Comparing simulation results versus theory for a fixed reverse-bias voltage.

As it is shown in Figure 5-7, the simulation results for normalized diode current to the unstressed diode current (I_{D0}) are well consistent with the analytical equation for stresses below 600 MPa; however, for higher stresses a discrepancy between these two curves is noticeable. It should be noted that applicable stresses and pressures in MEMS devices, which are typically lower than 200 MPa, both models deliver similar responses.

Chapter 6. Experimental results

This chapter presents and discusses the characterization of the fabricated micro-resonators. A range of electrical and mechanical testing are performed to evaluate both DC and AC performance of the fabricated devices. Experimental results of such measurements and the test setups for each measurement are provided and described.

6.1. Device implementations

Devices from two different fabricated batches of micro-resonators were employed to test the feasibility of our design and to gauge the performance of the piezojunction mechanism for resonance sensing. These extensional bulk resonators were fabricated through the aforementioned SOI micro-machining process. The earliest devices tested are fabricated in a 2.5 μm-thick SOI device layer with a resistivity of about 10 Ω-cm, and designed for a resonant frequency of about 9 MHz. Figure 6-1 shows a Scanning Electron Microscopy image of such resonators.

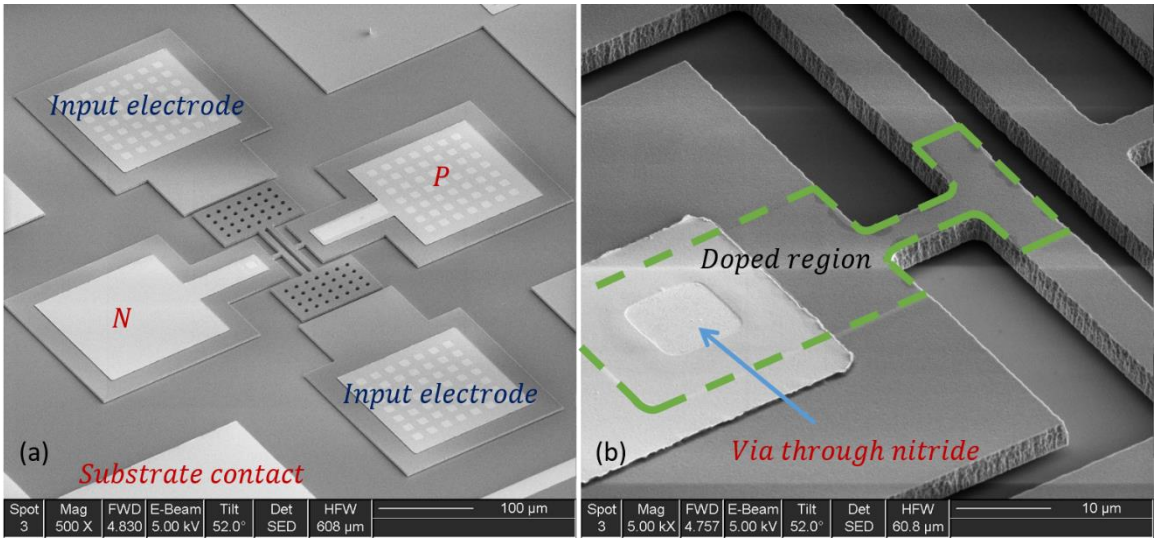

Figure 6-1: Scanning Electron Microscope (SEM) images of the fabricated resonator: (a) top-view of the micro-resonator and (b) a magnified image showing the *p-n* junction placement.

A transduction gap size of 2.5 µm and a junction depth of about 2 µm were estimated for these resonators. As it is shown in Figure 6-1, the sensing *p-n* junction is formed within one of the connecting beams of the resonator and electrical connections to the P and N contacts are placed on opposite sides of the device. Because of this contact arrangement and higher resistivity of the *p*-type device silicon, the series resistance of the diode is large. Consequently, the piezoresistive effect of silicon contributes as a strong interfering factor.

Another set of devices were fabricated in a 3 µm-thick SOI device layer, and designed for a resonant frequency of about 7 MHz. Figure 6-2 illustrates an optical image of these resonators. By optimizing the parameters of the silicon patterning process, smaller gap size of 2 µm is obtained for these devices. Also, the doping process is adjusted to achieve shallower junctions with a depth of 1.3 µm. As is can be seen in Figure 6-2, an extra connection to the *p*-type silicon (i.e. P1 contact) near the N contact is added to attain a lower series resistance for the diode compared to the previous design. However, this addition increases the total area of the top anchor of the resonator, which will result in a larger parasitic capacitance induced by each of P1 and N pads.

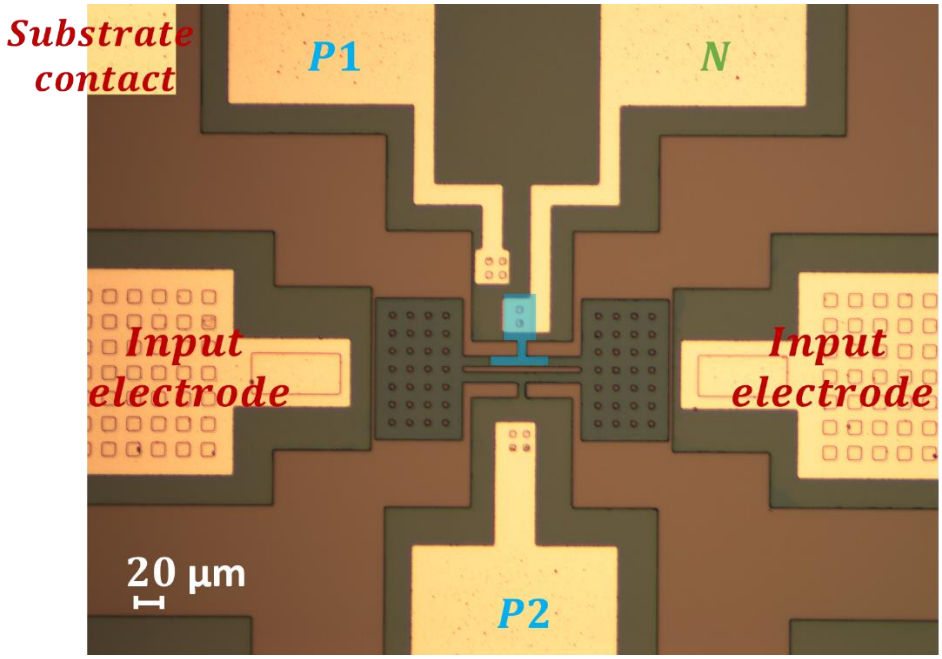

Figure 6-2: Optical image of the fabricated micro-resonator with a different bond pad configuration.

6.2. DC measurements

The first step in testing the fabricated resonators is to perform DC characterizations to obtain the electrical characteristics of the embedded *p-n* junctions. It is essential to evaluate the characteristics of fabricated diodes and investigate the possible effects of the substrate voltages and contact configurations before proceeding to the frequency response measurements of the resonators.

Figure 6-3 shows the configuration of the measurement setup that has been used for DC characterizations. A semiconductor parameter analyzer, Keithley 4200-SCS, and a probe station are used to experimentally verify the I-V characteristics of the integrated diodes on loose dies. All measurements are performed under ambient conditions (i.e. room temperature and atmospheric pressure), but stray light is blocked to eliminate the photovoltaic response.

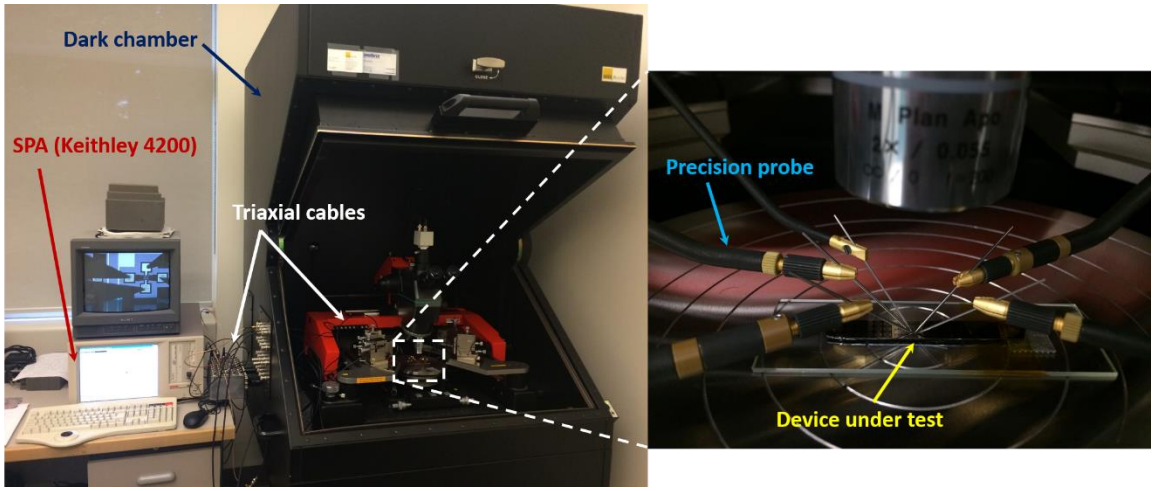

Figure 6-3: Experimental setup for DC characterizations.

First, I-V characteristics of the *p-n* junction of Figure 6-1 for both forward and reverse biased conditions were studied for the devices with no stress applied to the junction. A saturation current of 650 pA and was estimated from the measured data in the reverse condition. Figure 6-4 illustrates the obtained electrical characteristics of the diode for both forward- and reverse-biased conditions.

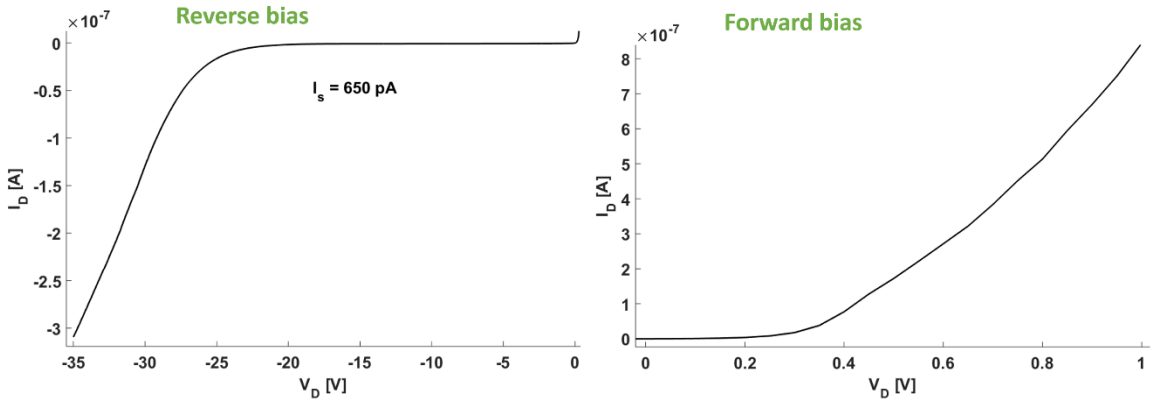

Figure 6-4: I-V characteristics of the embedded diode in (left) reverse- and (right) forward-biased conditions.

As well, by applying and varying a DC actuation voltage to the input electrodes, the effect of the resulting electrostatic force on the diode's characteristics was investigated. To evaluate the induced change in electrical characteristics of the reverse-biased diode due to the piezojunction effect, two cases were considered: 1) Effect of stress on *p-n* current change at several constant biasing voltages; and 2) Effect of stress on *p-n* voltage, particularly breakdown voltage, at various constant biasing currents. Initially the reverse-biased current at fixed biasing voltages is monitored for various actuation voltages that generate tensile stresses applied to the junction along the <110> direction. Measurement data for change of I_D versus stress at corresponding voltages are plotted in Figure 6-5. I_{D0} denotes the diode current with no stress applied. It should be noted that for each data point the measurements are performed for ten times and the average value is presented for each point. It was observed, that as the bias voltage increases towards the breakdown voltage, the changes to the diode current due to the mechanical stress jumps to a maximum value about the breakdown region. A maximum current change of nine times was measured at a bias voltage of -35 V for the stresses in the range of 0-120 kPa. Consequently, it was found that the ΔI_d, changes in the reverse current caused by stress, is strongly dependent on both the applied stress and biasing region of the *p-n* junction. However, the significant change in the diode current at larger reverse biasing voltages for such small stresses cannot be explained with the piezojunction effect. After careful characterization of various devices and observing the same trend, we realized that the effect of the generated electric field from the electrostatic actuation should be taken into account to interpret this data. The impact of the electric field is particularly substantial

as the biasing voltages reach near the break down region of the diode. In other words, the applied electrostatic field interferes with the electric field of the depletion region of the *p-n* junction causing a significant change to the break down voltage of the diode.

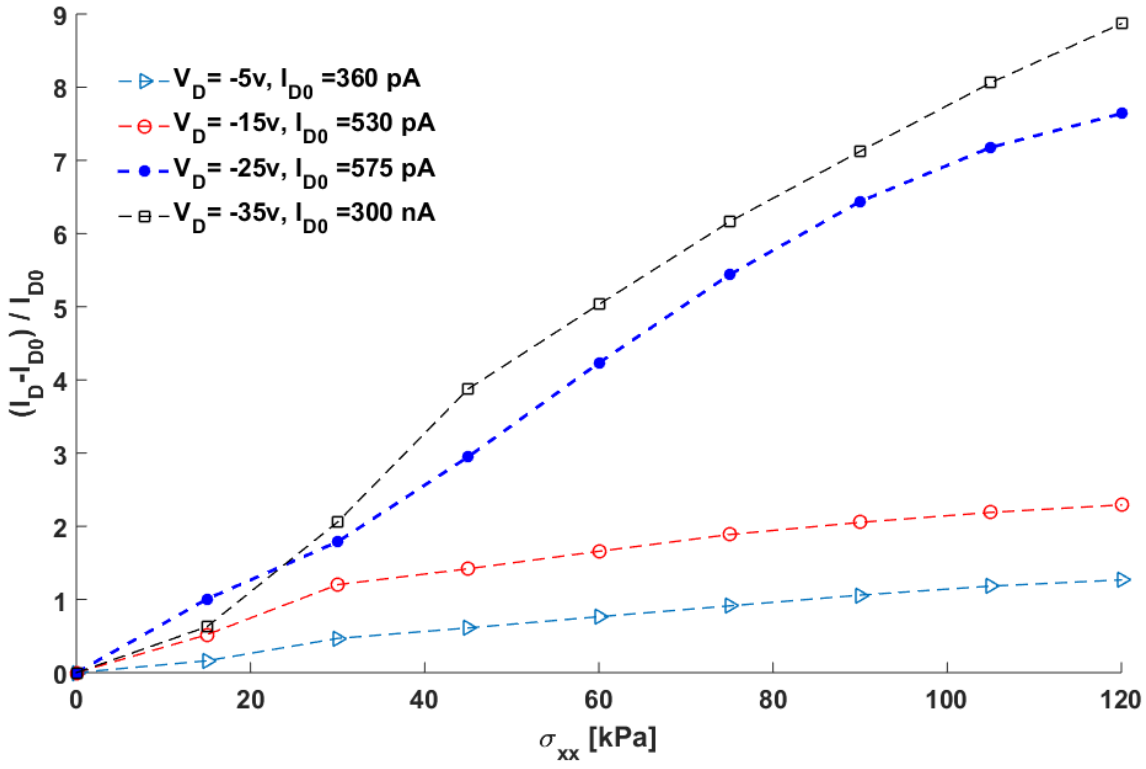

Figure 6-5: Measurement data for changes in the *p-n* junction current (I_D) versus the applied stress (σ_{xx}) to the junction through the input electrodes.

Diode voltage behavior due to the applied stress for several reverse biasing currents was studied in the same manner. Biasing currents in the range of 200 – 600 pA, are fed to the N contact of the diode. Obtained experimental data for voltage changes resulted from applied stresses in the range of 0-120 kPa are illustrated in Figure 6-6. It should be noted that for each data point the measurements are performed for ten times and the average value is presented for each point. An expected decrease in the diode voltage due to the increase in the applied stress and electric field was observed. The maximum diode voltage change is about -0.9 times for a bias current of I_D=-600 pA. Although, the changes in the diode reverse voltage are relatively smaller than the ones observed for diode current, a similar behavior for the changes near breakdown area of the diode I-V characteristic is noticeable.

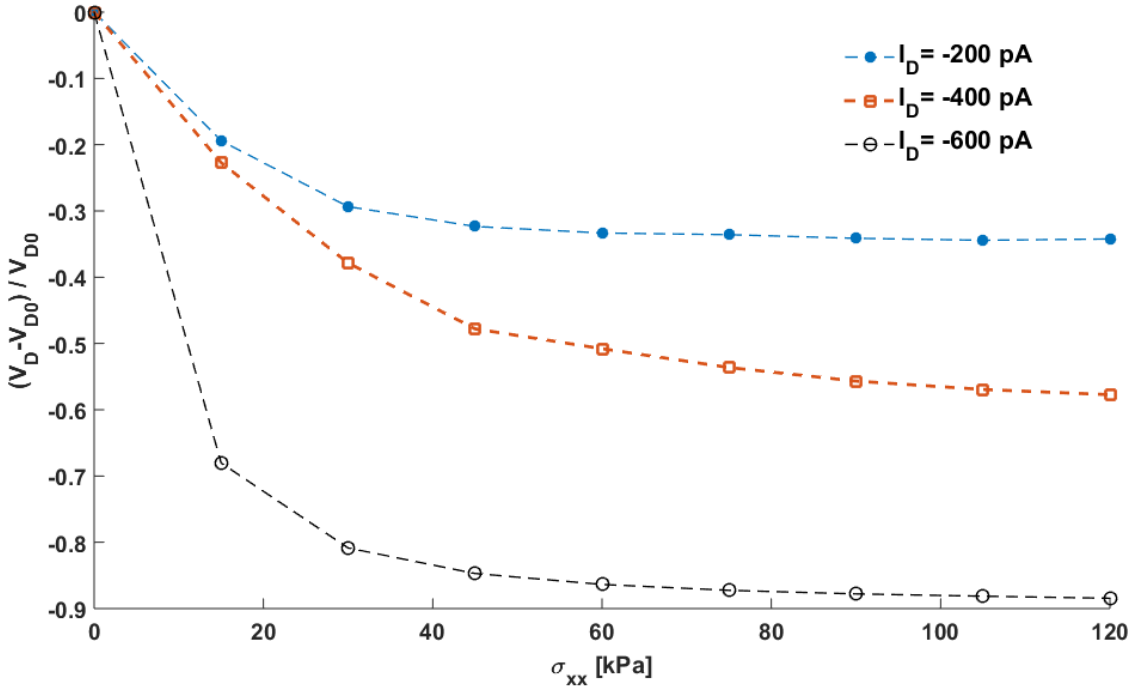

Figure 6-6: Measurement data for changes in the *p-n* junction voltage (V_D) versus the applied stress (σ_{xx}) to the junction through the input electrodes.

Additionally, the power consumption of this sensing mechanism was measured to evaluate the performance of this sensing mechanism in terms of power efficiency. Power consumption was measured to be as low as 0.4 to 30 nW, for reverse voltages in the range of 1-35 V, which demonstrates a superior performance regarding the required operating power.

Next, devices from the final fabrication run are tested. Figure 6-7 shows the probing setup that was used for DC characterization purposes. As it is illustrated in Figure 6-7, one contact to the N-doped region (N) and two electrical contacts to the p-type device layer, namely $P1$ and $P2$ are implemented. Figure 6-8 presents and compares the obtained I-V characteristic responses for these two configurations of diodes (N-P1 and N-P2). As it can be seen, the diode from near $P1$ contact exhibits significantly lower series resistance. The saturation current in reverse-biased condition was measured to be about 12 µA.

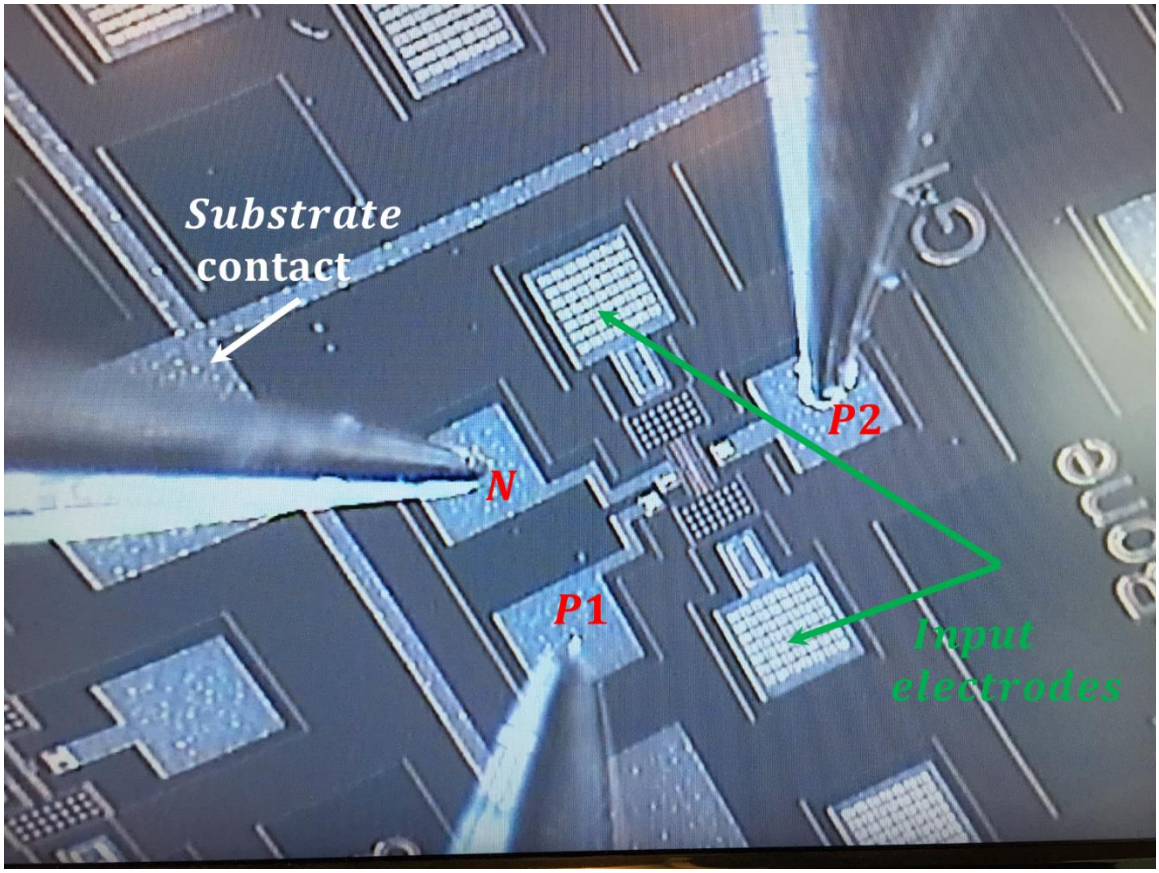

Figure 6-7: **DC probing of the micro-resonator with two contacts to the p-type silicon layer.**

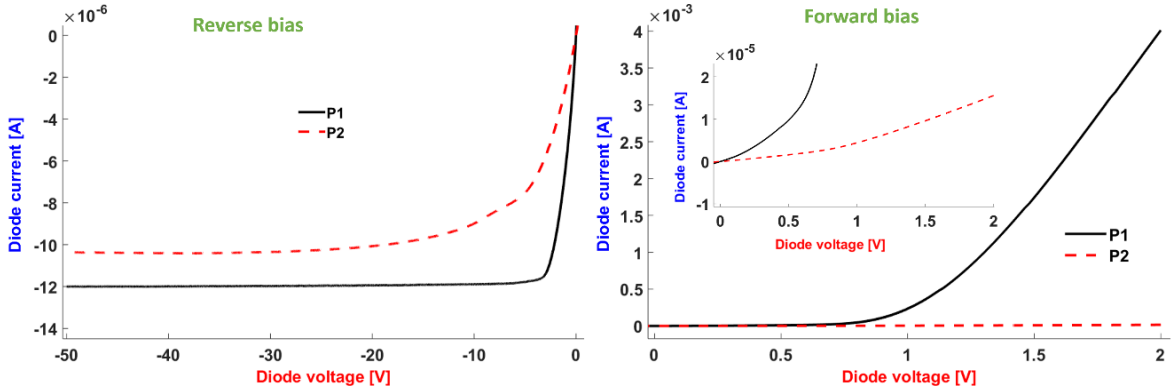

Figure 6-8: **DC electrical characteristics of diode configurations for reverse- and forward-biased conditions.**

The series resistance for diodes with these two configurations of P contacts (i.e. P1N and P2N) were measured from their semi-logarithmic I-V plots in forward-biased condition (Figure 6-9). The series resistances were estimated to be ~5 kΩ and ~280 kΩ for P1N and P2N junctions, respectively.

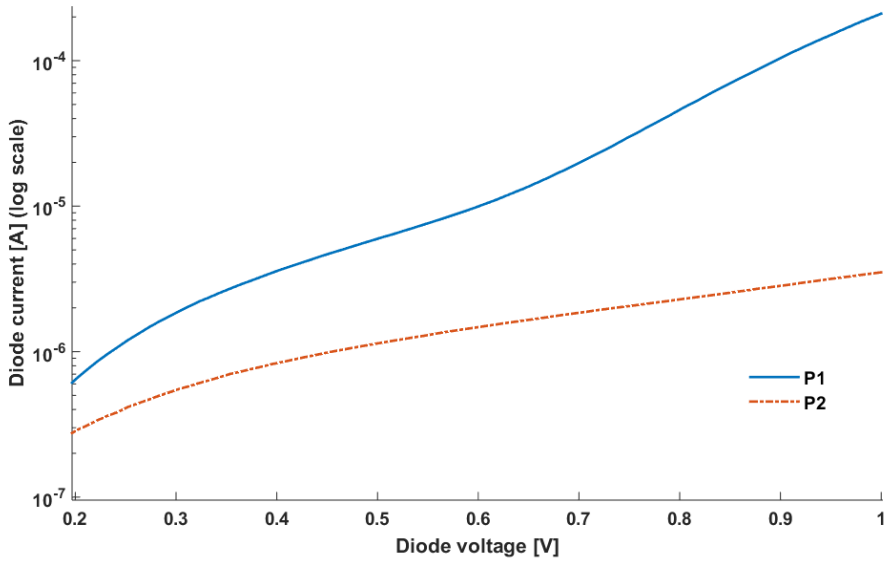

Figure 6-9: Semi-logarithmic I-V plot for P1N and P2N junctions for forward bias voltages.

Also, it was noticed that for reverse bias voltages larger than a certain value, the depletion region reaches the bottom of the silicon device layer at the *p*-side and begins to extend sideways afterward. An illustration of this effect is illustrated in Figure 6-10 for both partially and fully depleted cases.

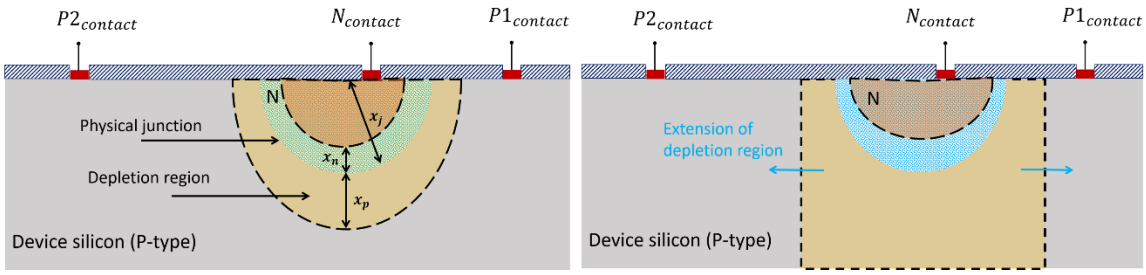

Figure 6-10: Schematic illustration of the depletion region in the reverse-biased silicon diode: (left) partially depleted and (right) fully depleted.

To further investigate this effect, an experiment is designed to determine the value of the voltages for which the *p-n* device becomes fully depleted. By applying a constant voltage of one volt between $P1_{contact}$ and $P2_{contact}$ and varying the voltage on $N_{contact}$, the current of $P2_{contact}$ is monitored. Figure 6-11 provides the results of this experiment.

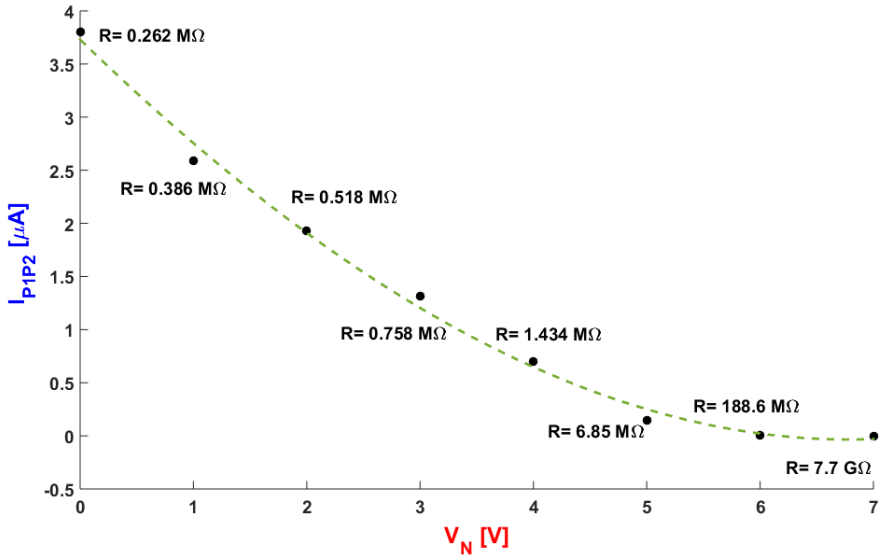

Figure 6-11: Change in the current flowing between P contacts for various applied voltages to the N contact in reverse-biased condition.

The resistance between two P contacts increases as the depletion region extends at the *p*-side and a pinched-off happens for reverse biases higher than 6 volts. Based on the DC results and to avoid the floating of $P2_{contact}$ for the fully-depleted condition, both P contacts are electrically shorted to each other for AC and frequency response measurements.

Moreover, the effect of substrate voltage on the electrical characteristics of N-P1 and N-P2 are investigated. Because the gap size between silicon device layer and the substrate underneath is only 1 µm, it is not possible to apply voltages greater than 10-20 volts without collapsing the resonator due to the strong electrostatic force between the plates. To overcome this limits, this characterization is performed before releasing the structures with the BOX layer remaining in place. This allows to apply positive and negative voltages as high as 200 volts without damaging any structures. Figure 6-12 and Figure 6-13 present the attained data for N-P1 and N-P2 diodes, respectively.

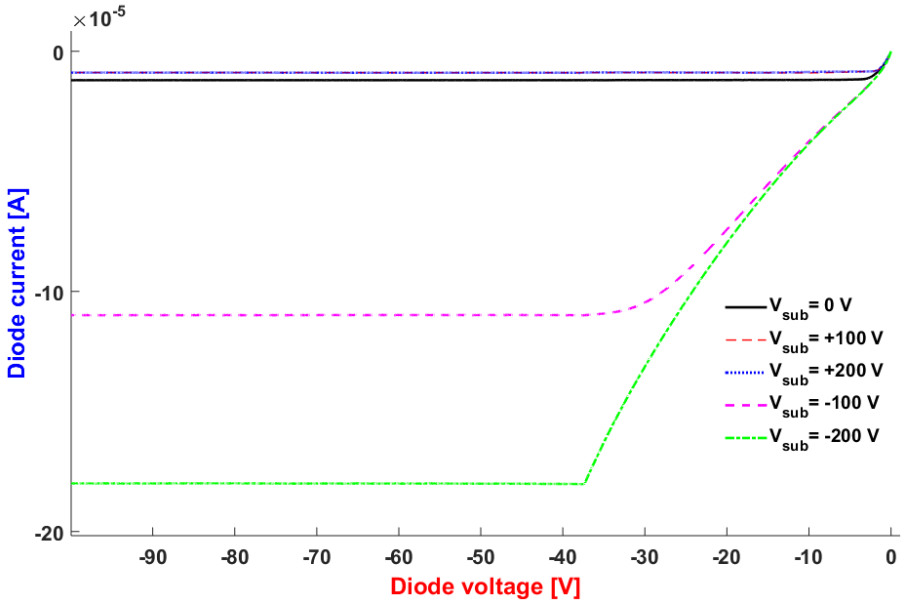

Figure 6-12: Reverse characteristics of N-P1 diode for different substrate voltages.

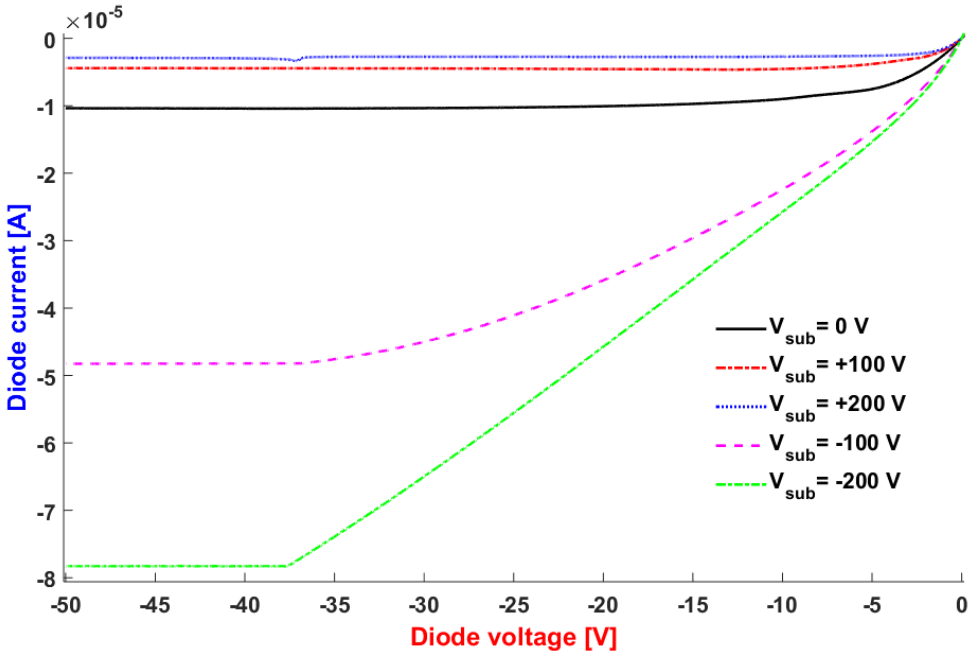

Figure 6-13: Reverse characteristics of N-P2 diode for different substrate voltages.

Applying a negative voltage to the substrate attracts the holes in the *p*-type device silicon and accumulates them closer to the surface of silicon and oxide layer, while applying a positive voltage depletes the volume from holes. As a result, by increasing the negative voltage, the resistance of the *p*-type silicon drops and diode current increases. Also, negative voltages cause the fully-depleted condition to occur at higher reverse bias voltages. This effect is the opposite for positive voltages applied to the substrate. To verify and evaluate this effect, the resistance between $P1_{contact}$ and $P2_{contact}$ are measured for different substrate voltages and the results are provided in Table 6-1.

Table 6-1: Changes in the resistance of the *p*-type device layer for positive and negative voltages applied to the substrate.

V_{sub} [V]	-200	-100	0	+100	+200
R_{P1P2} [kΩ]	112	140	288	330	345

6.3. AC measurements

Pursuant to the confirmation of DC and electrical performance of the integrated diodes, AC measurements are carried out to investigate the frequency response of the micro-resonators and to verify the employment of piezojunction for sensing of their resonant signal. A vector network analyzer (VNA) in a two-port configuration and a vacuum probe station were used to experimentally extract the frequency response of the resonators. All measurements were performed under vacuum (below 5mTorr) with the stray light blocked to prevent photovoltaic effects. Working under vacuum reduces the effect of air damping on electrostatic resonators, and hence, leads to higher quality factors and stronger signals at resonance. Figure 6-14 demonstrates the test setup that has been used for characterization of fabricated resonators from the earlier fabrication runs. This measurement setup allows for measurement and characterization of the frequency response of both capacitive and piezojunction transductions.

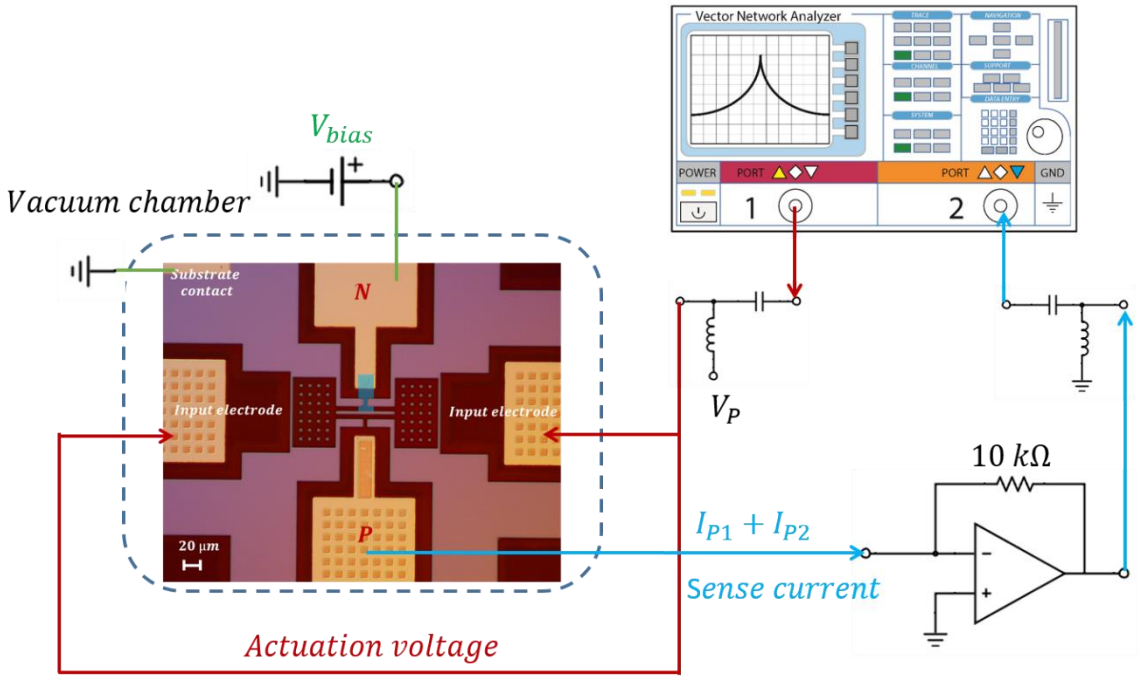

Figure 6-14: Experimental configuration for frequency response measurements.

Initially, the resonance frequency of the micro-resonator is determined and extracted using electrostatic actuation and capacitive sensing. The drive AC signal from the VNA and the DC polarization voltage (V_P) are applied to the input electrodes to excite the resonator in its extensional-mode of vibration. At this mode shape, the supporting beams experience extension and contraction along their lengths. The resonance sense current is picked up from *p*-type silicon and fed through a transresistance amplifier with the gain of 10 kΩ to port 2 of the VNA. A drive signal comprising of a 140V DC and 0.5V AC is used for electrostatic actuation of the resonator at its desired mode of vibration. For $V_{bias} = 0\ V$ the *p-n* junction is off and the sense current measured at the P contact is a result of modulation of the air gap capacitance. The measured frequency response for capacitive sensing is depicted in Figure 6-15 after removing the feedthrough signal.

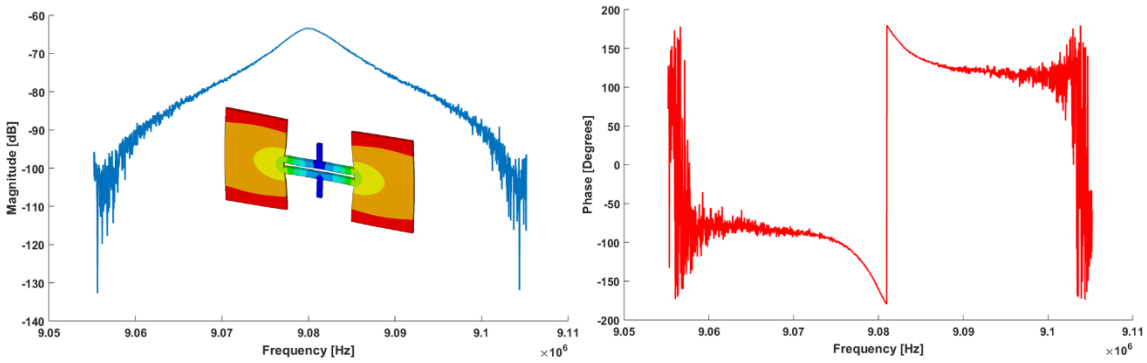

Figure 6-15: Transmission frequency characteristics of the dog-bone micro-resonator using capacitive sensing with a resonant frequency of about 9 MHz after feedthrough is removed.

The quality factor of the resonator can be estimated using the (amplitude or) phase response of the device versus frequency by [17]:

$$Q = \frac{f_{res}}{\Delta f_{-3dB}} = \frac{\omega_{res}}{2}\frac{d}{d\omega}\angle \mathrm{H}(\mathrm{j}\omega) \tag{6.1}$$

The quality factor was extracted from the measurement results to be about 2,100 at a resonant frequency of 9.084 MHz. In addition, the effect of DC polarization voltage (V_P) on the frequency response of the resonator was investigated. As it can be seen in Figure 6-16, increasing the DC voltage causes greater amplitude of resonance while moving the resonance frequency to lower frequencies because of the electrostatic spring softening in capacitive mechanical resonators.

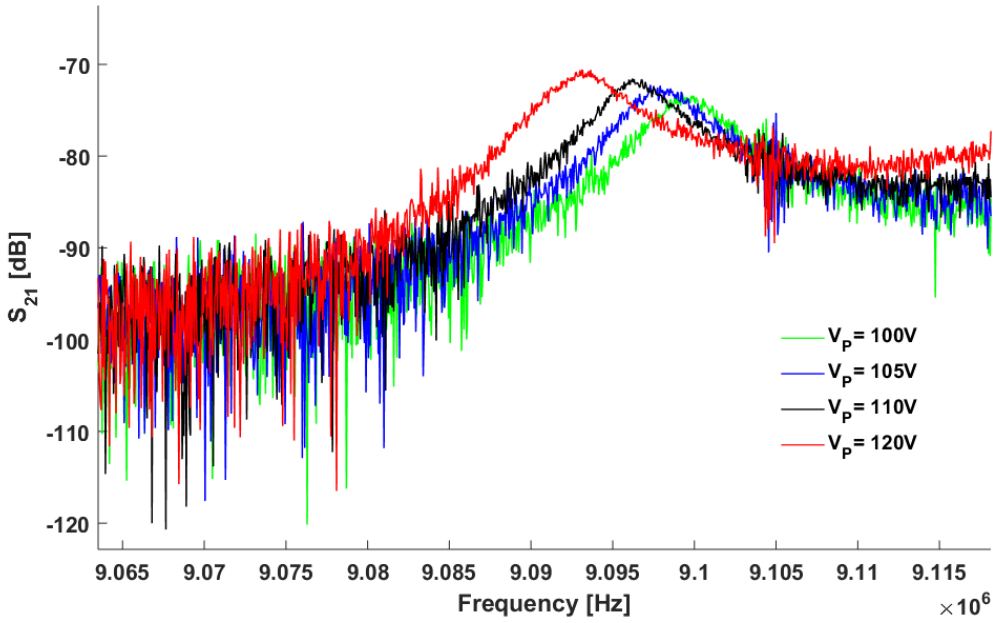

Figure 6-16: Effect of V_P on the amplitude and frequency of capacitive resonance signal after feedthrough removed.

The next objective was to detect the resonance peak caused by the modulation of *p-n* junction current due to the piezojunction effect. Therefore, subsequent to obtaining the resonant frequency of the device, the *p-n* junction is reverse biased by applying a bias voltage (V_{bias}) to the N contact. The resonator is excited at its resonance frequency with electrostatic drive in the same manner as for the capacitive sensing. The sense current from diode is picked up at the P contact and fed to the port 2 of the VNA via the transresistance amplifier with the gain of 10 kΩ. Figure 6-17 illustrates the transmission frequency results for various biasing voltages. We observed that changing the biasing condition of the diode can affect the amplitude of resonance signal and a shift in its base line, but the resonant frequency remains unchanged. The power consumption of this sensing technique is also evaluated to determine the power efficiency of piezojunction transduction for resonance sensing. The power in reverse-biased condition was measured to range from 0.25 nW to 6.5 nW. The obtained result shows excellent power efficiency factor of piezojunction transduction mechanism when used for resonance sensing.

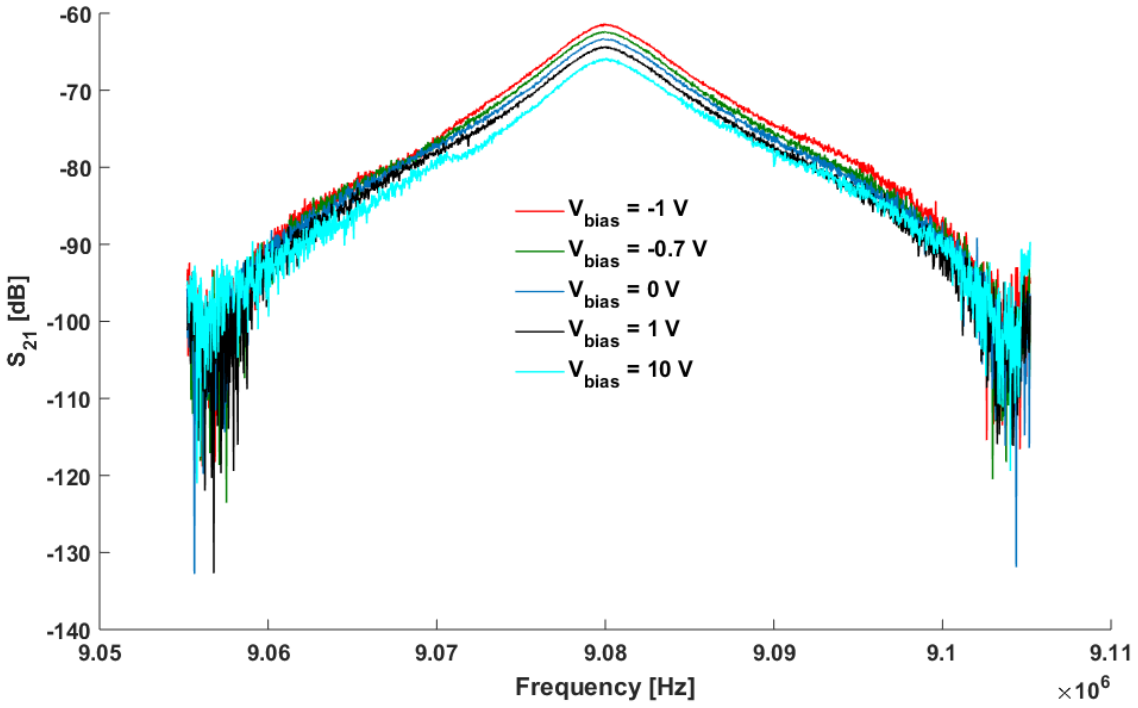

Figure 6-17: Transmission frequency characteristics (S_{21}) of the resonator for different diode biasing voltages after feedthrough removed.

The frequency response of the resonators from the final fabrication run were also characterized. This resonators has smaller transduction gap sizes (i.e. 2 µm) compared to the ones of earlier resonators (2.5 µm -3 µm). A narrower gap dimension results in a significantly higher electrostatic transduction coefficient (η_e) and lower motional resistance (R_m) according to Equations (2.4) and (2.5). Furthermore, these resonators have a different configuration of metal contacts that allows to achieve a smaller series resistance for their *p-n* junctions. Figure 6-18 and Figure 6-19 show the test setup configuration and actual test setup that have been used for frequency measurement and characterization.

First, the resonance frequency of the structure was determined from obtaining the resonance signal through electrostatic drive and sensing. A 0.5V AC drive signal on top of a 100V DC bias voltage was used for electrostatic actuation of the resonator at the desired extensional bulk-mode of vibration. For $V_D = 0V$, the *p-n* junction is off and the measured sense current at the P-type contact is from the modulation of the transduction gap capacitance. The feedthrough capacitance (C_f) has the most significant effect in obscuring the detection of the motional current.

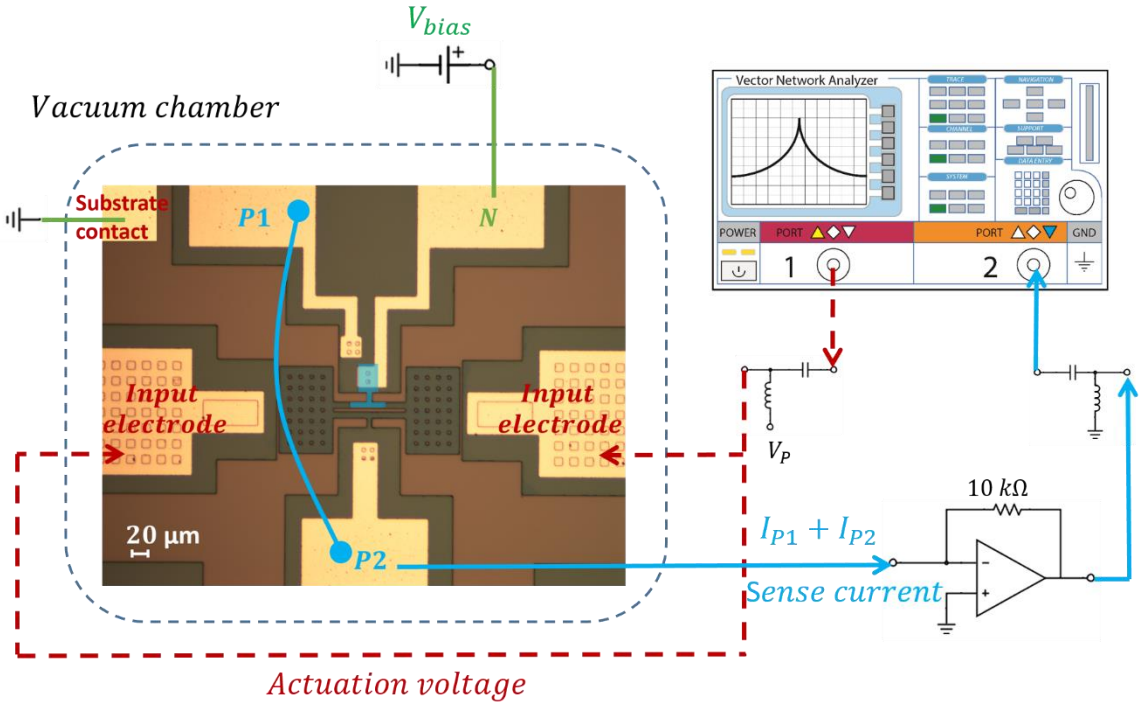

Figure 6-18: AC measurement setup configuration.

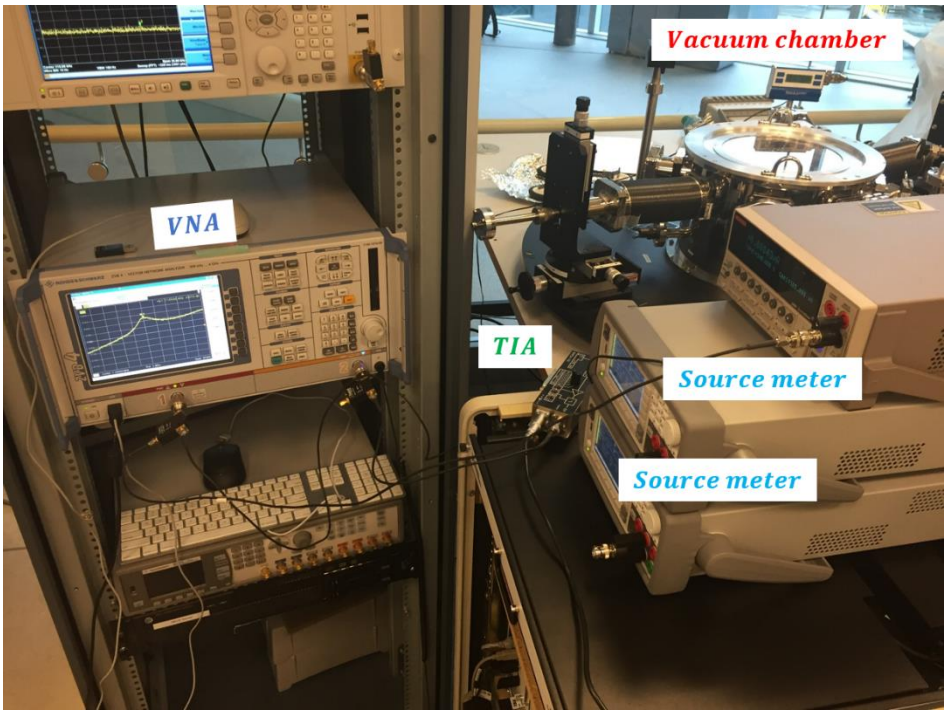

Figure 6-19: Actual test setup for frequency response measurements.

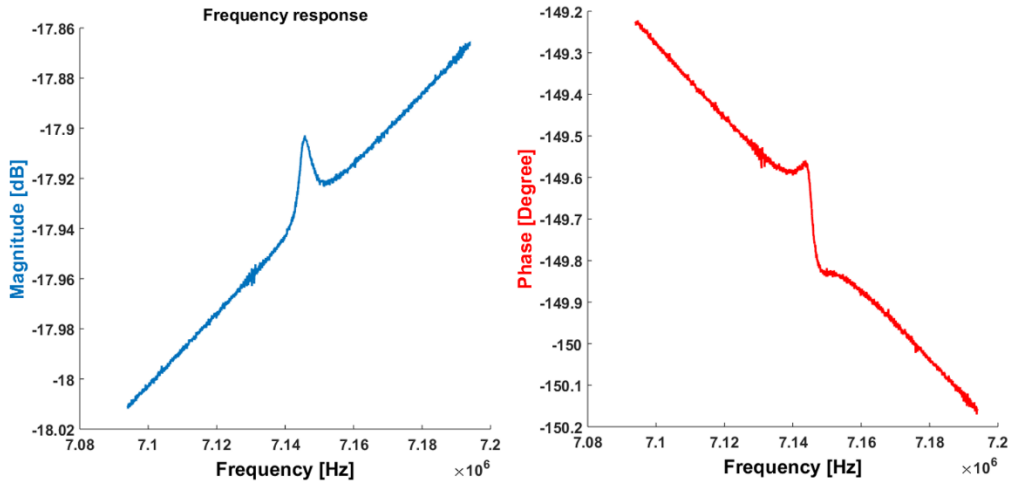

Figure 6-20: Magnitude and phase of the transmission response of the resonator via capacitive sensing before feedthrough removal.

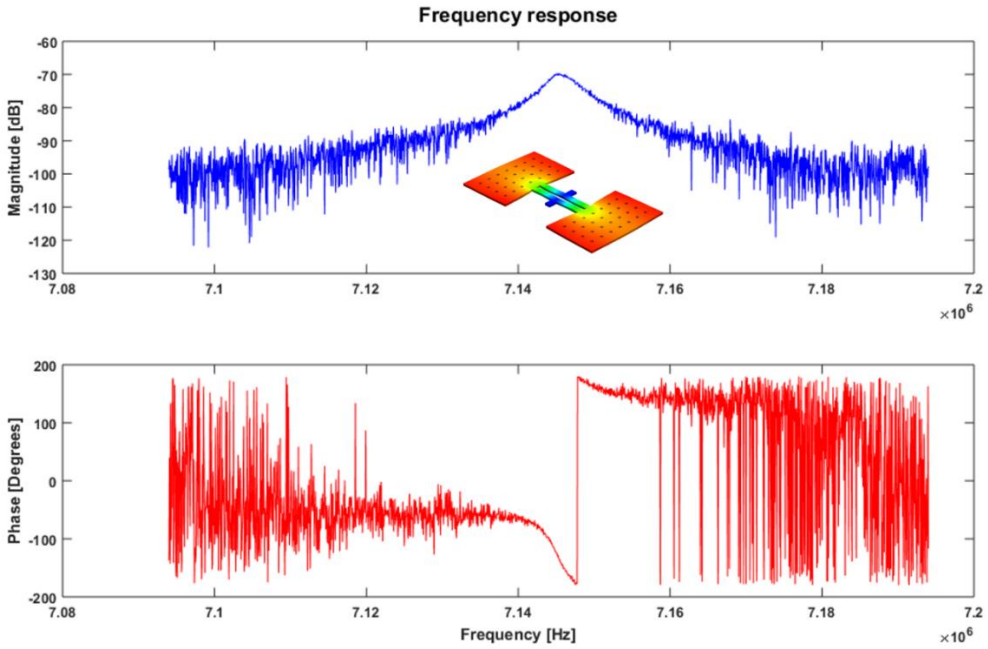

Figure 6-21: Extracted magnitude and phase of the capacitive transmission response (S_{21}) for experimental data (with feedthrough signal removed).

Measured magnitude and phase components of the frequency response before and after removing feedthrough current for capacitive sensing are shown in Figure 6-20 and Figure 6-21, respectively. A quality factor of about 3,000 was estimated at a resonant frequency of 7.15 MHz.

Next, the *p-n* junction is biased with the V_{bias} voltage which is applied to the N contact while $P1$ and $P2$ are connected to the virtual ground pin of the amplifier. To detect the resonance peak through the piezojunction effect, *p-n* junction was biased in the reverse condition (i.e. $V_D < 0$) with applying various biasing voltages to V_{bias}. The output AC current from the P-type contact of the diode is fed to the transresistance amplifier and monitored on VNA to obtain the open-loop transmission frequency response (S_{21}) of the micro-resonator. Measured S_{21} data for various biasing voltages was obtained with identical testing conditions as for the capacitive result. We observed that changing the biasing condition of the diode affects the amplitude of resonance and causes a shift in its base line, but the resonant frequency remains unaffected. Figure 6-22 illustrates the obtained results of the transmission frequency response of the micro-resonator for various biasing voltages of the diode.

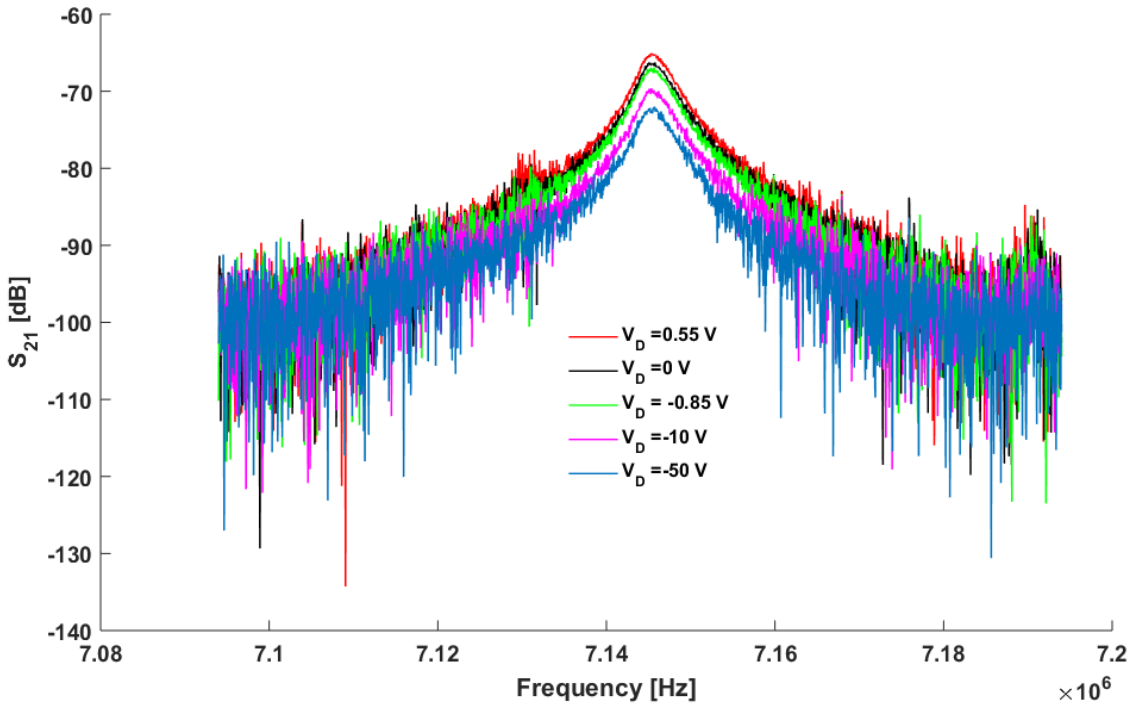

Figure 6-22: Frequency response of the resonator for various *p-n* junction biases.

Figure 6-23 illustrates the normalized magnitude results for both reverse- and forward-biased conditions compared to the capacitive signal (i.e. $V_D = 0$). The power consumption of this sensing technique is also evaluated to determine the power efficiency

of piezojunction transduction for resonance sensing. The power in reverse-biased condition was measured to be as low as 5nW for small reverse bias voltages and currents.

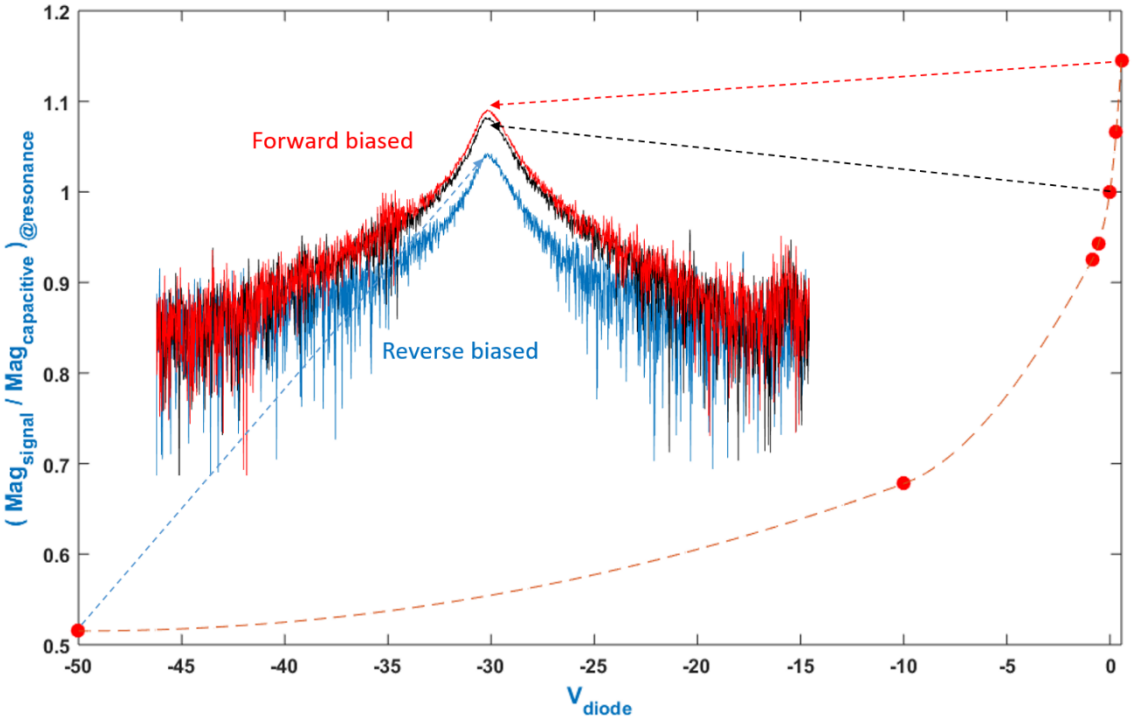

Figure 6-23: Effect of the diode bias voltage on the output signals in terms of maximum magnitude for various biasing voltages.

To better understand the occurring phenomena, the equivalent electrical model of the piezojunction transduction from Figure 5-5 (c) is extended to account for the effect of parasitic capacitances and diode biases on the frequency characteristics of the micro-resonator. Figure 6-24 demonstrates the developed equivalent electrical model of this transduction technique.

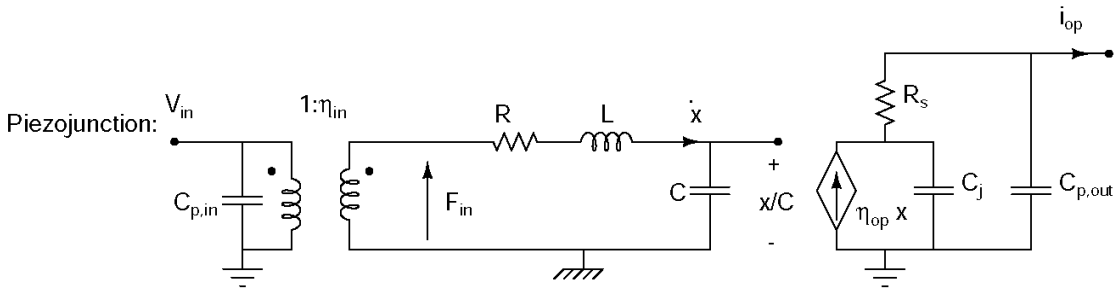

Figure 6-24: Equivalent electrical representation of electrostatic actuation and piezojunction sensing in a micro-resonator.

Parasitic capacitances $C_{p,in}$ and $C_{p,out}$ are respectively added to the input and output ports to include the effect of capacitances of bond pads, package pins and cables at these ports. Also, the *p-n* junction capacitance (C_j) and series resistance (R_s) are included to account for effect of diode biasing voltage on the frequency characteristics of the micro-resonator. First, the values of lumped elements of the equivalent electrical model are extracted from the frequency response of the resonator. Table 6-2 provides such values for the frequency response of Figure 6-21.

Table 6-2: Extracted parameters for the equivalent electrical model of the piezojunction sensing from experimental data.

Parameter	R_m **[Ω]**	C_m **[F]**	L_m **[H]**	C_f **[pF]**	$C_{p,in}$ **[pF]**	$C_{p,out}$ **[pF]**
Value	**7.5e6**	**1.51e-19**	**3.3e3**	**0.43**	**60**	**15**

Junction capacitance (C_j) is related to the biasing voltage of the diode (V_{bias}) according to:

$$C_j = \frac{\epsilon A_j}{W_d} = \epsilon A_j \sqrt{\frac{q}{2\epsilon(V_o - V_{bias})}\frac{N_d N_a}{N_d + N_a}} \qquad (6.2)$$

$$V_o = \frac{KT}{q}\ln\left(\frac{N_a N_d}{{n_i}^2}\right)$$

where A_j, W_d, V_o, N_d and N_a refer to the junction area, width of the depletion region, built-in voltage, concentration of donor impurities and concentration of acceptor impurities, respectively. As it can be inferred from Equation (6.2), the junction capacitance decreases as the reverse bias voltage increases. For the embedded diode of this work, the junction capacitance was estimated to decrease from 0.2 pF to 0.06 pF for a reverse voltage bias change from -0.85 V to -50 V. Based on our resonator's circuit model, a decrease in the junction capacitance raises the base line of the resonant peak; however, as it was mentioned earlier, as the depletion region extends for greater reverse voltages, the resistance in series with the diode increases significantly. This increase in the series resistance moves the base line downwards and dominates the effect of junction capacitance on the resonance peak. By using the LTSPICE circuit simulator, the AC response of the electrical model of the piezojunction mechanism was simulated for various reverse biasing voltages. Figure 6-25 presents the simulation results.

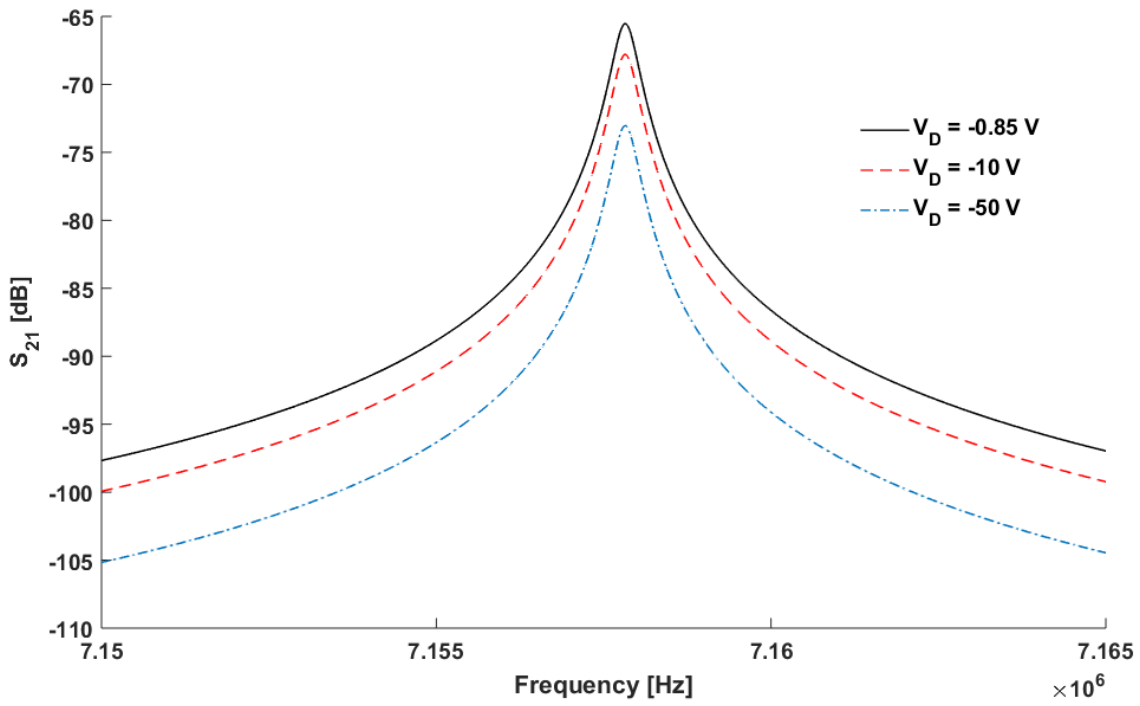

Figure 6-25: Effect of various biasing voltages on the transmission frequency characteristics of micro-resonator obtained from the circuit analysis of the equivalent electrical model.

A comparison between the simulation results (Figure 6-25) and actual measurement data (Figure 6-22) demonstrates a good agreement between such graphs. The developed circuit model allows to simulate the resonator's performance in SPICE circuit simulators and to evaluate the effect of various design parameters on the performance of piezojunction sensing in resonators.

Characterization results verified the employment of piezojunction effect for sensing of resonance in micro-mechanical resonators. As well, the experimental data demonstrated that this transduction method has a potential to be used in MEMS resonators where power consumption and high-level of integration are key design parameters.

Chapter 7. Conclusions and future work

7.1. Conclusions and contributions

In this dissertation, for the first time, the use of piezojunction mechanism as a viable transduction technique in resonant microsystems was investigated. Piezojunction method was introduced as an alternative solution for measurement of resonance and a promising addition to existing detection techniques such as electrostatic, piezoelectric and piezoresistive transductions. A micro-resonator amplifies the internal strains at the resonance frequency by its mechanical quality factor, and therefore, provides a suitable platform for employment of piezojunction. Piezojunction sensing requires low power consumption, small chip area and offers high level of integration.

This thesis proposed a mechanical micro-resonator as an enabling platform to utilize the piezojunction effect. A MEM resonator employs the inherent mechanical amplification of displacements at resonance, and therefore, it is capable of mechanically amplifying the piezojunction sensing signal at the resonance frequency by its quality factor. In order to devise an effective structure for employment of piezojunction in a micro-resonator, various flexural- and bulk-mode resonating structures including simple rectangular beams, square plates and other shapes were designed, fabricated and examined. A bulk-mode resonator is chosen because of the potential for a higher mechanical quality factor. The proposed design is an extensional bulk-mode resonator with an integrated *p*-*n* junction. The structure is a so-called dog-bone resonator, which is optimized in order to improve the mechanical and electrical responses of the resonator. A combination of electrostatic drive and piezojunction sensing transduces this micro-device. In addition, static and dynamic responses of the designed structures were analyzed through Finite Element Analysis (FEA) and modal analysis using CoventorWare software.

Author has developed a SOI micro-machining process to fabricate prototype micro-resonators with embedded diodes. This state-of-the-art process is devised to be a multi-

user multi-purpose process that supports fabrication of various designs on a single substrate. Each step of this process is carefully and precisely optimized to ensure the compatibility of the all the steps and a high quality output. A high yield of more than 85% in fabrication of about two hundreds devices for each fabrication run was estimated. In comparison with similar standard foundry processes, this in-house process features a doping step, which is essential for creation of doped junctions or piezoresistors. One of the main challenges in development of this process was the creation of narrow transduction gaps in silicon device layer for optimal transduction efficiency. This challenge is overcome by a combination of using SOI wafers with thicker device layers and creating of dry etching recipes with higher levels of anisotropy. Also, this process concerns both electrical and mechanical performances of the fabricated devices. Therefore, metal contacts are improved to obtain ohmic contacts to both *p*-type and *n*-type regions of device silicon. The release step was achieved with no signs of neither bending nor stiction of the free structures to the substrate.

As it was mentioned, the developed SOI process is a multi-user, which enables fabrication of micro-devices with sensing piezoresistors. Designs of other researchers from IMUTS group were fabricated along the piezojunction devices on a single substrate. A set of these devices were piezoresistive flexural-mode micro-resonators that employed strongly coupled resonators to achieve higher sensitivities [134],[135].

The physics of piezojunction and its analytical models were studied in detail to explore the applicability of this phenomenon for micro-device applications. Also, effect of mechanical stress on current-voltage characteristics of *p-n* junctions was simulated using Sentaurus Device from Synopsys® and Atlas from Silvaco. Simulation results and analytical models suggested that effective application of piezojunction in micro-electromechanical devices depends on developing designs and optimized approaches, which can improve the sensitivity of this mechanism to stress.

Piezojunction devices were fabricated through the SOI process and were experimentally tested to verify their operation. Experiments and test setups were designed to characterize both DC and AC performances with precision equipment. DC measurements evaluate the I-V characteristics of embedded junctions, electrical

resistivity, and effect of actuation voltages on them. On the other hands, AC characterizations provide capacitive and piezojunction frequency response of the resonators. The resonant frequencies are in the range of 7 MHz to 9 MHz with mechanical quality factors of 3,000-10,000. Due to use of electrostatic drive, a feedthrough capacitance between input and output ports obscures the motional signal. Thus, to present the transmission frequency response, the contribution of this feedthrough signal was extracted and removed from obtained data. Frequency responses of both capacitive and piezojunction signals with the same electrostatic drive are recorded and compared. Moreover, the effect of diode biasing voltages on the frequency response of piezojunction signal was investigated.

Based on the device operation and measured results, an equivalent electrical model of the resonator with piezojunction sensing was developed. This electrical model was simulated with LTSPICE circuit simulator and the results were compared against the experimental frequency graphs.

Characterization results demonstrated that the integration of microelectronic *p-n* junctions within the micro-mechanical resonating structures offers an effective ultra-low power method for detection of resonance and its application in sensing or timing.

7.2. Future work

This work founded the basis of application of piezojunction effect in resonant micro-devices. Further research and studies can be undertaken to investigate this technique further and improve its performance. Following provides a list of suggestions for future improvements of this method.

- SOI wafers with thicker silicon device layer and narrower transduction gaps are required to increase the efficiency of electrostatic transduction for actuation of bulk micro-resonators. As a result the motional resistance of the resonators will be some orders of magnitude smaller.
- Employing ion implantation for creation of embedded junctions can provide a more controllable process and better junctions. Also, effect of various doping

concentrations with different junction depths on the performance of this technique can be investigated.

- The use of Bipolar Junction Transistors (BJTs) and Junction Field Effect Transistors (JFETs) instead of a *p-n* junction will provide on-chip amplification of the output signal without the need of an external electronic amplifier.
- Thermal sensitivity of the resonance frequency and piezojunction current need to be characterized and compensated.
- Placement of the micro-resonator along with on-chip circuitry in a closed-loop feedback to realize an integrated oscillator.

Appendices

Appendix A Fabrication details

Silicon-On-Insulator (SOI) fabrication run sheet

The following process flow details the fabrication process and parameters that have been used in prototyping of micro-devices of this dissertation.

1. Oxidation

#	Process step	Process details
1-1	Wet thermal oxidation	Dry N_2 flow through bubbler: 4 scfh Vapor DI water Temperature: 1100 °C Time: 45 minutes
1-2	Oxide patterning	Spin Primer (HMDS) to promote adhesion Primer spinning: at 4000 rpm for 40 seconds Photoresist: Shipley 1813 Resist spinning: at 3500 rpm for 35 seconds Soft bake at 115 °C for 1 minute and 15 seconds Exposure: 7.5 seconds at 18 mW/cm^2 Develop: 1 minute and 10 seconds in MF319 at room temperature with mild agitation Hard bake at 115 °C for 2 minutes
1-3	Oxide etch	Buffer oxide etchant (BOE) Time: 6 minutes Room temperature
1-4	Photoresist removal	Photoresist strip by double bath Acetone

#	Process step	Process details
1-5	RCA SC-1 clean	Deionized (DI) H_2O: 5 parts Ammonium Hydroxide (NH_4OH), 30%: 1 part Hydrogen Peroxide (H_2O_2), 50%: 1 part Temperature: 80°C Time: 10 minutes
1-6	DI water rinse	>3 minutes
1-7	Modified HF dip	DI H_2O: 100 parts HF, 48%: 1 part Room temperature Time: 30 seconds
1-8	DI water dump rinse	>5 minutes, twice

2. Diffusion

#	Process step	Process details
2-1	Phosphorous diffusion	Solid source: PDS® products phosphorus n-type source wafer, PH-1000N Temperature:950°C Time: 30 minutes

#	Process step	Process details
2-2	Deglaze	DI water: 10 parts HF 48%: 1 part Time: 2minutes Room temperature
2-3	Low Temperature Oxidation (LTO)	Dry N_2 flow through bubbler: 4 scfh Vapor DI water Temperature: 800 °C Time: 50 minutes
2-4	Oxide strip	Remove all oxide with diluted HF (10 parts DI water and 1 part HF 48%) for 10 minutes at room temperature.
2-5	DI water dump rinse	>5 minutes, twice

3. Nitride deposition

#	Process step	Process details
3-1	RCA SC-1 clean	Deionized (DI) H_2O: 5 parts Ammonium Hydroxide (NH_4OH), 30%: 1 part Hydrogen Peroxide (H_2O_2), 50%: 1 part Temperature: 80°C Time: 10 minutes.

#	Process step	Process details
3-2	DI water rinse	>3 minutes
3-3	Drying	N_2 spin dry Oven dry at 100°C for 5 minutes
3-4	LPCVD Si_3N_4	Time: 43 minutes, Pressure: 200 mTorr Temperature: 835 °C Gases: DCS/NH3=60/10 Thickness: 115 nm

4. Device silicon patterning and etch

#	Process step	Process details
4-1	Chromium sputtering as hard mask for etching of silicon	DC plasma sputtering High vacuum pressure: ~9e-6 Torr 380 W*min @0.2 A in current mode 3 mTorr Ar pressure Thickness: 350 nm
4-2	Cr patterning	Spin Primer (HMDS) to promote adhesion Primer spinning: at 4000 rpm for 40 seconds Photoresist: Shipley 1813 Resist spinning: at 4200 rpm for 40 seconds Soft bake at 115 °C for 90 seconds

#	Process step	Process details
		Exposure: 7 seconds at 18 mW/cm^2 Develop: 1 minute and 10 seconds in MF319 at room temperature with mild agitation Hard bake at 115 °C for 2 minutes
4-3	Cr etch	Chromium etchant Time: 5 minutes Room temperature
4-4	DI water rinse	>3 minutes
4-5	Drying	N_2 spin dry Oven dry at 100°C for 5 minutes
4-6	Photoresist hard bake	Temperature: 115°C Time: 2 minutes
4-7	Nitride and Silicon Reactive Ion Etching (RIE)	SF_6 flow: 12 sccm O_2 flow: 7 sccm Pressure: 15 mTorr Power: 250 Watts Time: 9 minutes Nitride etch rate: ~250 nm/minute Silicon etch rate: ~350 nm/minute
4-8	Cr strip	Chromium etchant Time: 20 minutes

5. Contact vias through nitride

#	Process step	Process details
5-1	Contact patterning	Spin Primer (HMDS) to promote adhesion Primer spinning: at 4000 rpm for 40 seconds Photoresist: Shipley 1813 Resist spinning: at 3500 rpm for 40 seconds Soft bake at 115 °C for 70 seconds Exposure: 7 seconds at 18 mW/cm^2 Develop: 1 minute and 20 seconds in MF319 at room temperature with mild agitation Hard bake at 115 °C for 2 minutes
5-2	Nitride etch with RIE	CF_4 flow: 40 sccm, O_2 flow: 4 sccm Pressure: 100 mTorr Power: 200 Watts, Time: 1 minute Nitride etch rate: ~150 nm/minute
5-3	Photoresist removal (Ashing)	O_2 flow: 50 sccm Pressure: 100 mTorr Power: 250 Watts Time: 15 minutes

6. Metallization

#	Process step	Process details
6-1	Buried oxide layer etch	Vapor HF Temperature: 35°C Time: 7 minutes
6-2	DI water dump rinse	>5 minutes, twice
6-3	RCA SC-1 clean	Deionized (DI) H_2O: 5 parts Ammonium Hydroxide (NH_4OH), 30%: 1 part Hydrogen Peroxide (H_2O_2), 50%: 1 part Temperature: 80°C Time: 10 minutes
6-4	DI water rinse	>3 minutes
6-5	RCA SC-2 clean	Deionized (DI) H_2O: 6 parts Hydrochloric Acid (HCl), 30%: 1 part Hydrogen Peroxide (H_2O_2), 50%: 1 part Temperature: 80°C Time: 10 minutes
6-6	DI water rinse	>3 minutes
6-7	Drying	N_2 spin dry Oven dry at 100°C for 5 minutes

#	Process step	Process details
6-8	Lift-off preparation	Photoresist: Shipley 1827 Resist spinning: at 3500 rpm for 35 seconds Photoresist: Shipley 1823 Resist spinning: at 4000 rpm for 35 seconds Soft bake at 115 °C for 1 minute and 10 seconds Exposure: 8 seconds at 18 mW/cm^2 Develop: 1 minute and 30 seconds in MF319 at room temperature with mild agitation
6-9	Native oxide strip	DI H_2O: 10 parts HF, 48%: 1 part Temperature: room temperature Time: 30 seconds
6-10	DI water dump rinse	>5 minutes, twice
6-11	Drying	N_2 spin dry Oven dry 100°C for 2 minutes
6-12	Al deposition	Material: Al99Si1 from Goodfellow Ltd. Thermal evaporation Deposition rate: ~5 A°/second Thickness: 250 nm
6-13	Metal lift-off	Soaking in Acetone bath for 10 minutes Sonication for 10 minutes
6-14	IPA rinse	1 minute

#	Process step	Process details
6-15	DI water rinse	>3 minutes
6-16	Drying	N_2 spin dry Oven dry at 100°C for 5 minutes
6-17	Aluminum sintering	Dry N_2 flow: 8 scfh Temperature: 475 °C Time: 40 minutes

7. Release

#	Process step	Process details
7-1	Device release	Vapor HF Temperature: 35°C Time: ~35 minutes
7-2	Drying	Oven dry at 100°C for 2 minutes

Thermal diffusion with Spin-On Dopants (SODs)

Both N-SOD (P509) and P-SOD (B200) liquid dopants from Filmtronics were used to create *p-n* junctions in p-type and n-type silicon wafers with various resistivities. Silicon oxide is deposited through PECVD and patterned to serve as the diffusion mask. The liquid dopants are spun at recommended speeds in their data sheet (typical speeds in the range of 2000 to 6000 rpm) for 5 seconds. The uniformity of the spun layer is sensitive to the uniformity and thickness of the oxide layer, as well as the application method. A post spinning bake at 200 °C for 15 minutes is required to remove the excess solvent and prepare samples for the thermal diffusion process. Figure A-1 shows optical images of the SOD layer post baking process. In some cases, bubbles and non-uniformities were observed in the spun layer across the wafer.

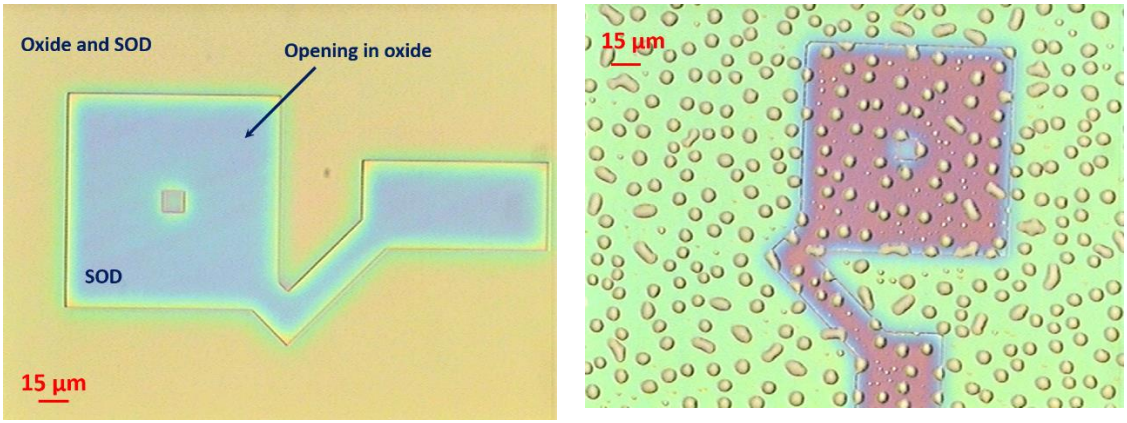

Figure A-1: Optical microscopy images of spun SOD after bake.

Thermal diffusion process was carried out in a Rapid Thermal Processor (RTP) at elevated temperatures in the range of 925 °C to 1000 °C for various durations between a 10 seconds to 15 minutes. In the longer processes, the SOD layer cracks during the thermal diffusion (Figure A-2).

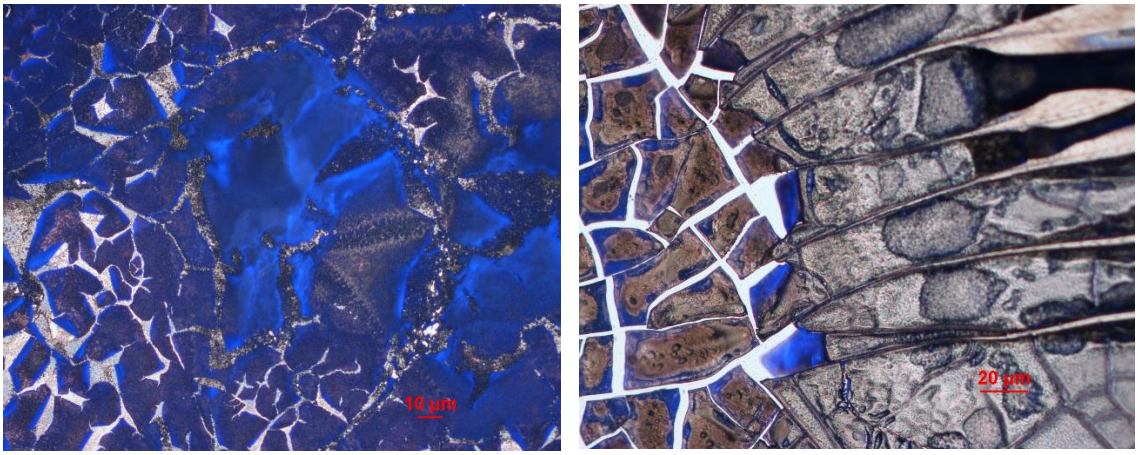

Figure A-2: Optical microscopy images of cracked SOD post thermal diffusion.

Post diffusion, samples are immersed in dilute HF to remove both SOD and oxide layer. It was noticed that for the case of P-SOD with Boron dopants, it is more challenging to remove the SOD film and it leaves a stain on the doped areas. Electrical characterization of resulted diodes shows that this diffusion techniques is more suitable for formation of shallower junctions with lower breakdown voltages. Figure A-3 shows the electrical characteristics of two sample diodes fabricated with P- and N-SODs.

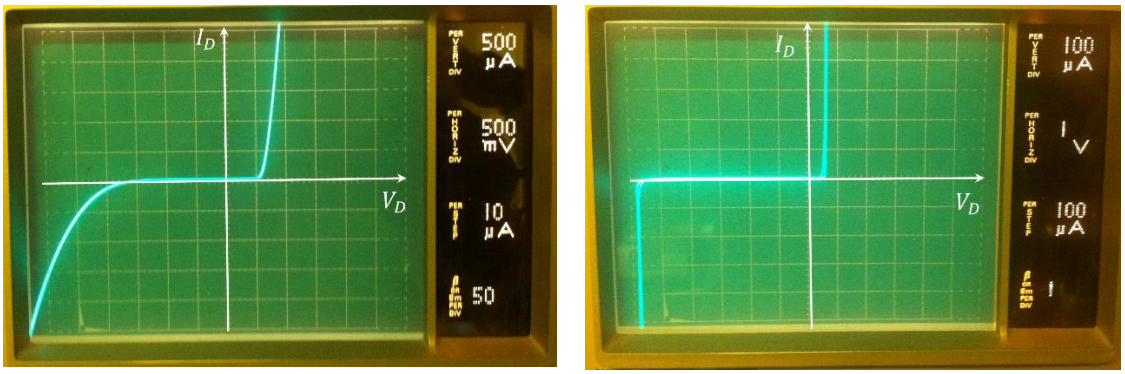

Figure A-3: I-V characteristics of diodes created with diffusion of SODs: (left) N-doped junction and (right) P-doped junction.

Nanometer-sized airgaps with Focused Ion Beam (FIB) milling

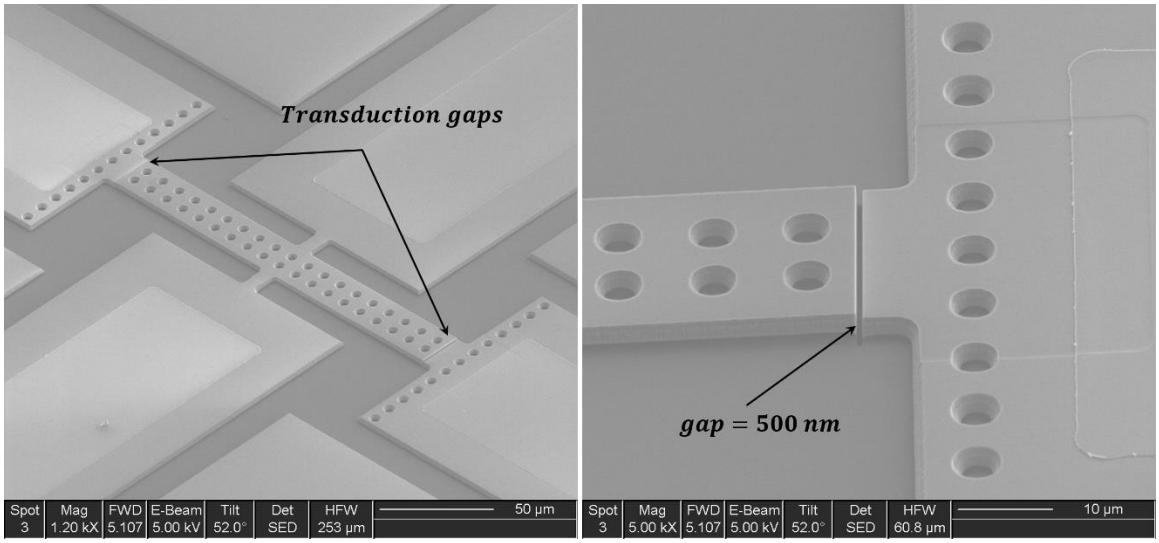

Figure A-4: SEM image of 500nm transduction gaps created with FIB in a beam resonator.

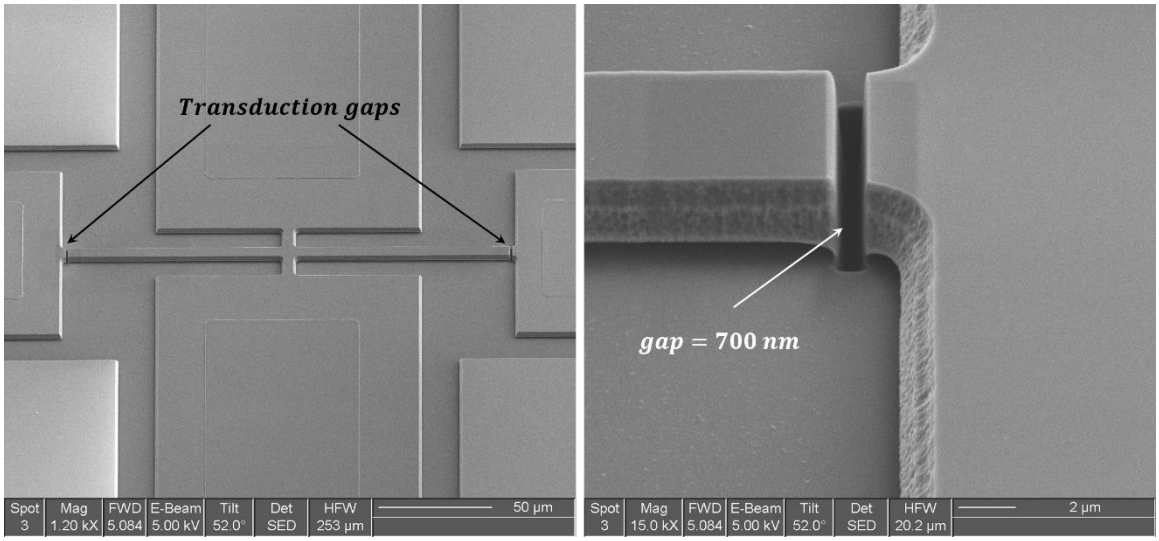

Figure A-5: SEM image of a fabricated longitudinal micro-resonator with a gap size of 700 nm.

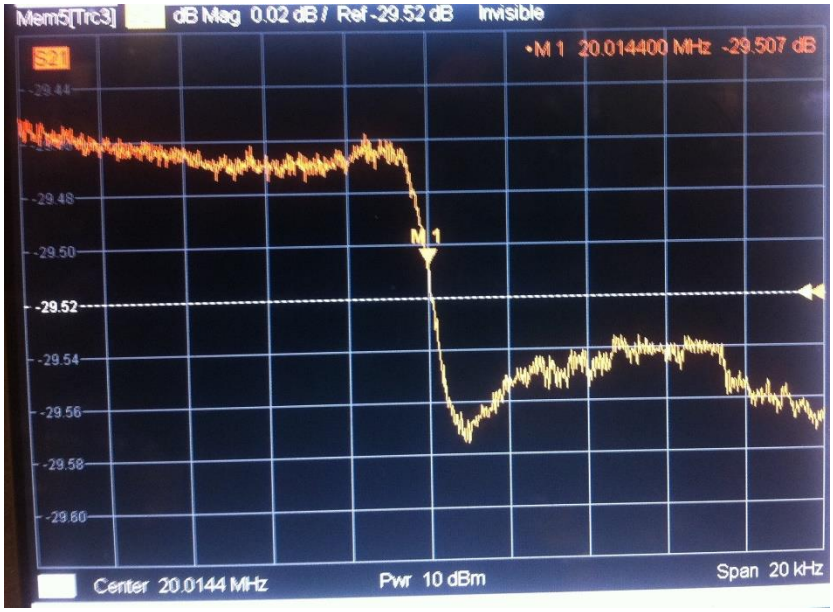

Figure A-6: Frequency response of the extensional beam resonator with a gap size of 700 nm and resonance frequency of 20 MHz.

Appendix B Extra Characterizations

In this part, the frequency response of a dogbone micro-resonator through the electrostatic actuation and piezoresistive sensing is provided. The micro-resonator is fabricated using the SOI process of Chapter 5. A doped N-region between N1 and N2 contacts form the embedded piezoresistor in the body of the resonator (Figure B-1). A DC current is passed through the piezoresistor with a DC bias of V_N applied to the N2 contact. At resonance, the movement of the resonator's structure causes the N-region to contract and expand. This contraction and expansion changes the resistance of the piezoresistor that results in the modulation of the current flowing through it. This modulated current it picked up and amplified using a transimpedance amplifier to sense the resonance signal. Figure B-2 presents the transmission frequency characteristics (S_{21}) of the resonator for various voltages applied to the N contact.

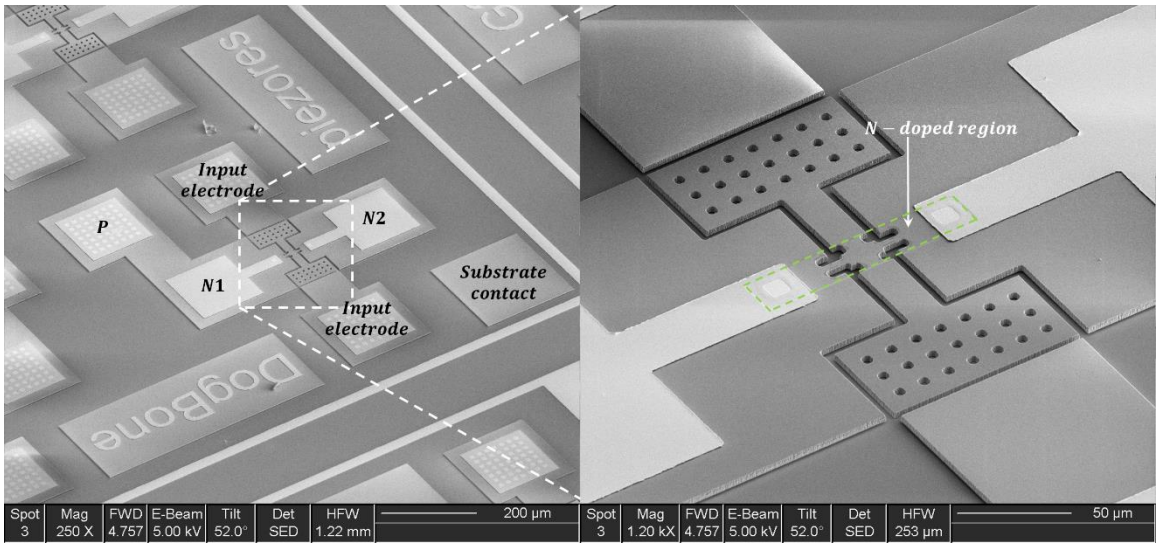

Figure B-1: SEM image of the piezoresistive SOI micro-resonator: (left) top view and (right) magnified image of placement of the doped region.

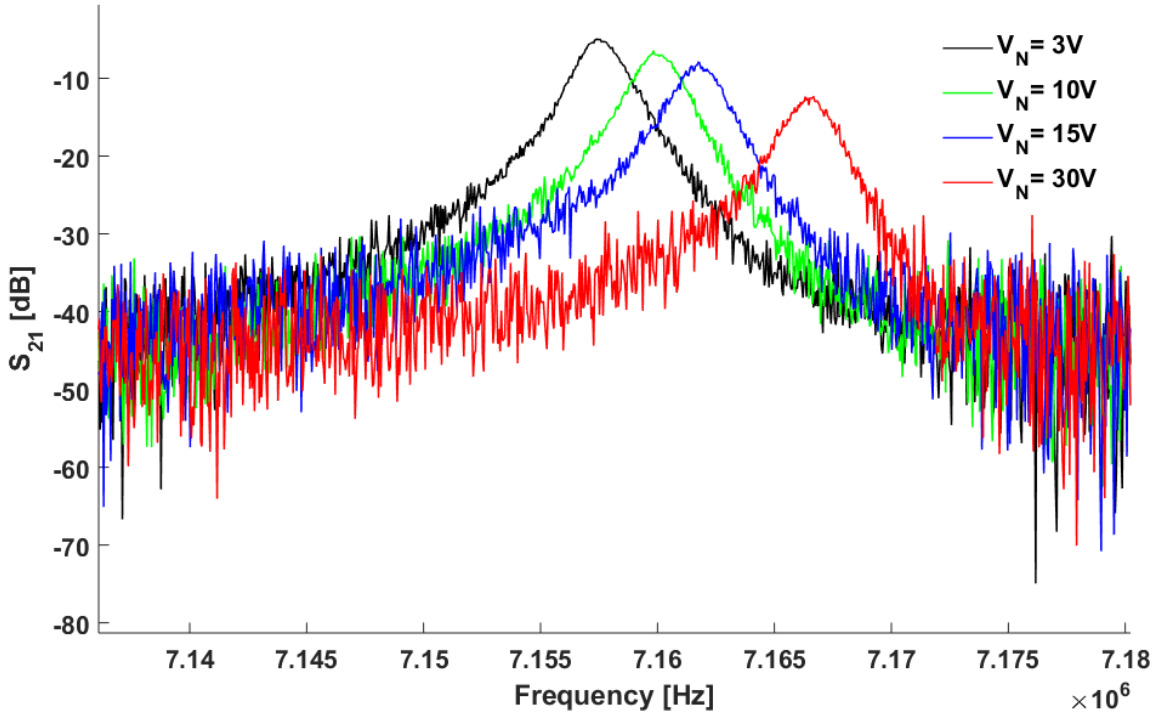

Figure B-2: Obtained frequency response of the micro-resonator employing piezoresistive sensing at various applied voltages.

References

[1] M. J. Madou, *Fundamentals of Microfabrication*. Taylor & Francis, 1997.

[2] Liwei Lin, A. P. Pisano, and R. T. Howe, “A micro strain gauge with mechanical amplifier,” *J. Microelectromechanical Syst.*, vol. 6, no. 4, pp. 313–321, Dec. 1997.

[3] A. Kourepenis, J. Borenstein, J. Connelly, R. Elliott, P. Ward, and M. Weinberg, “Performance of MEMS inertial sensors,” 1998, pp. 1–8.

[4] M. W. Ashraf, S. Tayyaba, and N. Afzulpurkar, “Micro Electromechanical Systems (MEMS) Based Microfluidic Devices for Biomedical Applications,” *Int. J. Mol. Sci.*, vol. 12, no. 12, pp. 3648–3704, Jun. 2011.

[5] C. Pramanik, H. Saha, and U. Gangopadhyay, “Design optimization of a high performance silicon MEMS piezoresistive pressure sensor for biomedical applications,” *J. Micromechanics Microengineering*, vol. 16, no. 10, pp. 2060–2066, Oct. 2006.

[6] J. W. Judy, “Microelectromechanical systems (MEMS): fabrication, design and applications,” *Smart Mater. Struct.*, vol. 10, no. 6, p. 1115, Dec. 2001.

[7] J.-W. Kim, H. Takao, K. Sawada, and M. Ishida, “Integrated Inductors for RF Transmitters in CMOS/MEMS Smart Microsensor Systems,” *Sensors*, vol. 7, no. 8, pp. 1387–1398, Jul. 2007.

[8] B. Puers, L. Reynaert, W. Snoeys, and W. Sansen, “A new uniaxial accelerometer in silicon based on the piezojunction effect,” *IEEE Trans. Electron Devices*, vol. 35, no. 6, pp. 764–770, Jun. 1988.

[9] R. C. Jaeger, J. C. Suhling, R. Ramani, A. T. Bradley, and J. Xu, “CMOS stress sensors on [100] silicon,” *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 85–95, Jan. 2000.

[10] R. H. Bishop, *Mechatronic Systems, Sensors, and Actuators: Fundamentals and Modeling*. CRC Press, 2007.

[11] W.-M. Zhang, G. Meng, and D. Chen, “Stability, Nonlinearity and Reliability of Electrostatically Actuated MEMS Devices,” *Sensors*, vol. 7, no. 5, pp. 760–796, May 2007.

[12] E. K. Akdogan, M. Allahverdi, and A. Safari, “Piezoelectric composites for sensor and actuator applications,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 52, no. 5, pp. 746–775, May 2005.

[13] A. Wisitsoraat, V. Patthanasetakul, T. Lomas, and A. Tuantranont, “Low cost thin film based piezoresistive MEMS tactile sensor,” *Sens. Actuators Phys.*, vol. 139, no. 1–2, pp. 17–22, Sep. 2007.

[14] J. H. Comtois, M. A. Michalicek, and C. C. Barron, “Electrothermal actuators fabricated in four-level planarized surface micromachined polycrystalline silicon,” *Sens. Actuators Phys.*, vol. 70, no. 1–2, pp. 23–31, Oct. 1998.

[15] S. Martellucci, A. N. Chester, and A. G. Mignani, Eds., *Optical Sensors and Microsystems*. Boston, MA: Springer US, 2000.

[16] J. S. Ko, M. L. Lee, D.-S. Lee, C. A. Choi, and Y. Tae Kim, “Development and application of a laterally driven electromagnetic microactuator,” *Appl. Phys. Lett.*, vol. 81, no. 3, p. 547, 2002.

[17] B. Bahreyni, *Fabrication and Design of Resonant Microdevices*, 1 edition. Norwich, NY: William Andrew, 2008.

[18] S. Pourkamali and F. Ayazi, “High frequency capacitive micromechanical resonators with reduced motional resistance using the HARPSS technology,” 2004, pp. 147–150.

[19] K. Wang, A.-C. Wong, W.-T. Hsu, and C. T.-C. Nguyen, “Frequency trimming and Q-factor enhancement of micromechanical resonators via localized filament annealing,” in *, 1997 International Conference on Solid State Sensors and Actuators, 1997. TRANSDUCERS ’97 Chicago*, 1997, vol. 1, pp. 109–112 vols.1.

[20] W.-L. Huang, Z. Ren, and C. T.-C. Nguyen, “Nickel Vibrating Micromechanical Disk Resonator with Solid Dielectric Capacitive-Transducer Gap,” in *2006 IEEE International Frequency Control Symposium and Exposition*, 2006, pp. 839–847.

[21] H. Chandrahalim, D. Weinstein, L. F. Cheow, and S. A. Bhave, “High-κ dielectrically transduced MEMS thickness shear mode resonators and tunable channel-select RF filters,” *Sens. Actuators Phys.*, vol. 136, no. 2, pp. 527–539, May 2007.

[22] M. A. Rasouli and B. Bahreyni, “Independent tuning of frequency and quality factor of microresonators,” *Appl. Phys. Lett.*, vol. 98, no. 24, p. 243508, Jun. 2011.

[23] G. K. Ho, R. Abdolvand, A. Sivapurapu, S. Humad, and F. Ayazi, “Piezoelectric-on-Silicon Lateral Bulk Acoustic Wave Micromechanical Resonators,” *J. Microelectromechanical Syst.*, vol. 17, no. 2, pp. 512–520, Apr. 2008.

[24] G. Piazza, P. J. Stephanou, J. M. Porter, M. B. J. Wijesundara, and A. P. Pisano, “Low motional resistance ring-shaped contour-mode aluminum nitride piezoelectric micromechanical resonators for UHF applications,” in *18th IEEE International Conference on Micro Electro Mechanical Systems, 2005. MEMS 2005*, 2005, pp. 20–23.

[25] G. Piazza, P. J. Stephanou, and A. P. Pisano, “One and two port piezoelectric higher order contour-mode MEMS resonators for mechanical signal processing,” *Solid-State Electron.*, vol. 51, no. 11–12, pp. 1596–1608, Nov. 2007.

[26] G. Piazza, P. J. Stephanou, and A. P. Pisano, “Piezoelectric Aluminum Nitride Vibrating Contour-Mode MEMS Resonators,” *J. Microelectromechanical Syst.*, vol. 15, no. 6, pp. 1406–1418, Dec. 2006.

[27] P. J. Stephanou and A. P. Pisano, “PS-4 GHZ Contour Extensional Mode Aluminum Nitride MEMS Resonators,” in *IEEE Ultrasonics Symposium, 2006*, 2006, pp. 2401–2404.

[28] J. T. M. van Beek, P. G. Steeneken, and B. Giesbers, “A 10MHz piezoresistive MEMS resonator with high Q,” in *2006 IEEE International Frequency Control Symposium and Exposition*, 2006, pp. 475–480.

[29] D. Weinstein and S. Bhave, “PIEZORESISTIVE SENSING OF A DIELECTRICALLY ACTUATED SILICON BAR RESONATOR,” presented at the Solid-State Sensors, Actuators, and Microsystems Workshop, 2008, pp. 368–371.

[30] S. D. Senturia, *Microsystem Design*, 1st ed. 2000. Corr. 2nd printing 2004 edition. Boston: Springer, 2004.

[31] J. T. M. van Beek and R. Puers, “A review of MEMS oscillators for frequency reference and timing applications,” *J. Micromechanics Microengineering*, vol. 22, no. 1, p. 13001, Jan. 2012.

[32] B. Bahreyni and C. Shafai, “Fabrication of Piezoresistive Sensors in Standard MEMS Foundry Processes,” 2005, pp. 215–218.

[33] T. Lomas, A. Tuantranont, and F. Cheevasuvit, “Micromachined piezoresistive tactile sensor array fabricated by bulk-etched MUMPs process,” in *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS ’03*, 2003, vol. 4, p. IV-856-IV-859 vol.4.

[34] G. Dahlmann, G. Hölzer, S. Hering, and U. Schwarz, “A Modular CMOS Foundry Process for Integrated Piezoresistive Pressure Sensors,” in *Advanced Microsystems for Automotive Applications 2005*, D. J. Valldorf and W. Gessner, Eds. Springer Berlin Heidelberg, 2005, pp. 413–424.

[35] G. K. Fedder, R. T. Howe, T.-J. K. Liu, and E. P. Quevy, “Technologies for Cofabricating MEMS and Electronics,” *Proc. IEEE*, vol. 96, no. 2, pp. 306–322, Feb. 2008.

[36] B. Bahreyni and C. Shafai, “Fabrication of piezoresistive sensors in standard MEMS foundry processes,” in *2005 IEEE Sensors*, 2005, p. 4 pp.-pp.

[37] H. H. Hall, J. Bardeen, and G. L. Pearson, “The Effects of Pressure and Temperature on the Resistance of p-n Junctions in Germanium,” *Phys. Rev.*, vol. 84, no. 1, pp. 129–132, Oct. 1951.

[38] W. Rindner, “Resistance of Elastically Deformed Shallow p-n Junctions,” *J. Appl. Phys.*, vol. 33, no. 8, pp. 2479–2480, Aug. 1962.

[39] J. J. Wortman, J. R. Hauser, and R. M. Burger, “Effect of Mechanical Stress on p-n Junction Device Characteristics,” *J. Appl. Phys.*, vol. 35, no. 7, p. 2122, 1964.

[40] *The Piezojunction Effect in Silicon Integrated Circuits and Sensors*, vol. 682. Boston: Kluwer Academic Publishers, 2003.

[41] W. Rindner and I. Braun, “Resistance of Elastically Deformed Shallow p-n Junctions. II,” *J. Appl. Phys.*, vol. 34, no. 7, p. 1958, 1963.

[42] M. E. Sikorski, P. Andreatch, A. Grieco, and H. Christensen, “Transistor Microphone,” *Rev. Sci. Instrum.*, vol. 33, no. 10, p. 1130, 1962.

[43] F. Krieger and H.-N. Toussaint, “A piezo-mesh-diode pressure transducer,” *Proc. IEEE*, vol. 55, no. 7, pp. 1234–1235, 1967.

[44] R. Schellin and R. Mohr, “A monolithically-integrated transistor microphone: Modelling and theoretical behaviour,” *Sens. Actuators Phys.*, vol. 37–38, pp. 666–673, Jun. 1993.

[45] J. Matovic, Z. Djuric, and A. Vujanic, “Piezojunction effect based pressure sensor,” *Electron. Lett.*, vol. 29, no. 6, pp. 565–566, Mar. 1993.

[46] F. Fruett, “The Piezojunction Effect in Silicon. Consequences and Applications for Integrated Circuits and Sensors,” Dissertation, TU Delft, Delft University of Technology, 2001.

[47] Y. Matukura, “Anisotropic Stress Effect of Silicon *p n* Junctions,” *Jpn. J. Appl. Phys.*, vol. 3, no. 15, pp. 256–261, 1964.

[48] Y. Kanda, “Effect of Stress on Germanium and Silicon p-n Junctions,” *Jpn. J. Appl. Phys.*, vol. 6, p. 475, Apr. 1967.

[49] J. F. Creemer, F. Fruett, G. C. M. Meijer, and P. J. French, “The piezojunction effect in silicon sensors and circuits and its relation to piezoresistance,” *IEEE Sens. J.*, vol. 1, no. 2, p. 98-, Aug. 2001.

[50] L. K. Monteith and J. J. Wortman, “Characterization of p-n junctions under the influence of a time varying mechanical strain,” *Solid-State Electron.*, vol. 16, no. 2, pp. 229–237, Feb. 1973.

[51] F. Fruett and G. C. M. Meijer, “Experimental investigation of piezojunction effect in silicon and its temperature dependence,” *Electron. Lett.*, vol. 37, no. 22, p. 1366, 2001.

[52] A. P. Friedrich, P. A. Besse, C. M. A. Ashruf, and R. S. Popovic, “Characterization of a novel piezo-tunneling strain sensor,” *Sens. Actuators Phys.*, vol. 66, no. 1–3, pp. 125–130, Apr. 1998.

[53] P. Smeys, P. B. Griffin, Z. U. Rek, I. De Wolf, and K. C. Saraswat, “Influence of process-induced stress on device characteristics and its impact on scaled device performance,” *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1245–1252, Jun. 1999.

[54] G. C. M. Meijer, P. C. Schmale, and K. van Zalinge, “A new curvature-corrected bandgap reference,” *IEEE J. Solid-State Circuits*, vol. 17, no. 6, pp. 1139–1143, Dec. 1982.

[55] M. Furuhashi and K. Taniguchi, “Additional stress-induced band gap narrowing in a silicon die,” *J. Appl. Phys.*, vol. 103, no. 2, p. 26103, Jan. 2008.

[56] J. R. Hauser, “Some Effects of Mechanical Stress on the Breakdown Voltage of p-n Junctions,” *J. Appl. Phys.*, vol. 37, no. 10, p. 3884, 1966.

[57] J. J. Wortman and J. R. Hauser, “Effect of Mechanical Stress on p—n Junction Device Characteristics. II. Generation—Recombination Current,” *J. Appl. Phys.*, vol. 37, no. 9, pp. 3527–3530, Aug. 1966.

[58] B. G. Streetman and S. Banerjee, *Solid state electronic devices*, 6th ed. Upper Saddle River, N.J: Pearson/Prentice Hall, 2006.

[59] H. Kressel and A. Elsea, “Effect of generation-recombination centers on the stress-dependence of Si p-n junction characteristics,” *Solid-State Electron.*, vol. 10, no. 3, pp. 213–224, Mar. 1967.

[60] J. R. Hauser, “An approximation for generation-recombination current in P-N junctions,” *Proc. IEEE*, vol. 53, no. 7, pp. 743–744, 1965.

[61] R. C. Jaeger, S. Hussain, J. C. Suhling, P. Gnanachchelvi, B. M. Wilamowski, and M. C. Hamilton, “Impact of mechanical stress on bipolar transistor current gain and Early voltage,” in *2013 IEEE SENSORS*, 2013, pp. 1–4.

[62] J. F. Creemer and P. J. French, “A new model of the effect of mechanical stress on the saturation current of bipolar transistors,” *Sens. Actuators Phys.*, vol. 97–98, pp. 289–295, Apr. 2002.

[63] J. L. Egley and D. Chidambarrao, “Strain effects on device characteristics: Implementation in drift-diffusion simulators,” *Solid-State Electron.*, vol. 36, no. 12, pp. 1653–1664, Dec. 1993.

[64] H. A. Rueda, S. Cea, and M. E. Law, “Mechanical stress modeling for silicon fabrication processes,” in *, 1997 International Conference on Simulation of Semiconductor Processes and Devices, 1997. SISPAD ’97*, 1997, pp. 53–55.

[65] H. Trujillo, A. Nagy, and P. Rodriguez, “Piezo-response of lateral bipolar transistors,” *Sens. Actuators Phys.*, vol. 64, no. 2, pp. 125–131, Jan. 1998.

[66] F. Fruett, F. Creemer, G. C. M. Meijer, and P. J. French, “A Theoretical and Experimental Study of the Piezojunction Effect in Silicon and its Exploitation in New Sensor Structures.,” in *Sensor Technology in the Netherlands: State of the Art*, A. van den Berg and P. Bergveld, Eds. Dordrecht: Springer Netherlands, 1998, pp. 191–195.

[67] D. Lange, C. Hagleitner, C. Herzog, O. Brand, and H. Baltes, “Electromagnetic actuation and MOS-transistor sensing for CMOS-integrated micromechanical resonators,” *Sens. Actuators Phys.*, vol. 103, no. 1–2, pp. 150–155, Jan. 2003.

[68] T. Fukuda, H. Morita, F. Arai, H. Ishihara, and H. Matsuura, “Micro resonator using electromagnetic actuator for tactile display,” 1997, pp. 143–148.

[69] A. Rahafrooz and S. Pourkamali, “Fully micromechanical piezo-thermal oscillators,” 2010, p. 7.2.1-7.2.4.

[70] J.-J. Li and K.-D. Zhu, “All-optical mass sensing with coupled mechanical resonator systems,” *Phys. Rep.*, vol. 525, no. 3, pp. 223–254, Apr. 2013.

[71] A. Rahafrooz and S. Pourkamali, “High-Frequency Thermally Actuated Electromechanical Resonators With Piezoresistive Readout,” *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1205–1214, Apr. 2011.

[72] S. P. Beeby and M. J. Tudor, “Micromechanical Resonators,” in *Wiley Encyclopedia of Electrical and Electronics Engineering*, John Wiley & Sons, Inc., 2001.

[73] W. Ye, X. Wang, W. Hemmert, D. Freeman, and J. White, “Air damping in laterally oscillating microresonators: a numerical and experimental study,” *J. Microelectromechanical Syst.*, vol. 12, no. 5, pp. 557–566, Oct. 2003.

[74] M. Bao and H. Yang, “Squeeze film air damping in MEMS,” *Sens. Actuators Phys.*, vol. 136, no. 1, pp. 3–27, May 2007.

[75] M. S. Hajhashemi, A. Rasouli, and B. Bahreyni, “Performance optimization of high order RF microresonators in the presence of squeezed film damping,” *Sens. Actuators Phys.*, vol. 216, pp. 266–276, Sep. 2014.

[76] M. A. Rasouli, M. S. Hajhashemi, and B. Bahreyni, “Higher-order Lamé mode square microresonator with improved quality factor and f-Q product,” in *2013 Transducers Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS EUROSENSORS XXVII)*, 2013, pp. 498–501.

[77] D. S. Bindel and S. Govindjee, “Elastic PMLs for resonator anchor loss simulation,” *Int. J. Numer. Methods Eng.*, vol. 64, no. 6, pp. 789–818, Oct. 2005.

[78] J. E.-Y. Lee, J. Yan, and A. A. Seshia, “Study of lateral mode SOI-MEMS resonators for reduced anchor loss,” *J. Micromechanics Microengineering*, vol. 21, no. 4, p. 45010, Mar. 2011.

[79] “Mems for Automotive and Aerospace Applications, 1st Edition | Michael Kraft, Neil White | ISBN 9780857096487.” [Online]. Available: http://store.elsevier.com/Mems-for-Automotive-and-Aerospace-Applications/isbn-9780857096487/. [Accessed: 23-Sep-2015].

[80] N. Yazdi, F. Ayazi, and K. Najafi, “Micromachined inertial sensors,” *Proc. IEEE*, vol. 86, no. 8, pp. 1640–1659, Aug. 1998.

[81] A. Gupta, D. Akin, and R. Bashir, “Detection of bacterial cells and antibodies using surface micromachined thin silicon cantilever resonators,” *J. Vac. Sci. Technol. B*, vol. 22, no. 6, pp. 2785–2791, Nov. 2004.

[82] A. K. Bryan, V. C. Hecht, W. Shen, K. Payer, W. H. Grover, and S. R. Manalis, “Measuring single cell mass, volume, and density with dual suspended microchannel resonators,” *Lab. Chip*, vol. 14, no. 3, pp. 569–576, Feb. 2014.

[83] C. T.-C. Nguyen, “Vibrating RF MEMS technology: fuel for an integrated micromechanical circuit revolution?,” in *The 13th International Conference on Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS ’05*, 2005, vol. 1, p. 243–246 Vol. 1.

[84] “Wiley: Resonant MEMS: Fundamentals, Implementation, and Application - Oliver Brand, Isabelle Dufour, Stephen Heinrich, et al.” [Online]. Available: http://ca.wiley.com/WileyCDA/WileyTitle/productCd-3527335455,subjectCd-NT70.html. [Accessed: 23-Sep-2015].

[85] J. Wang, L. Yang, S. Pietrangelo, Z. Ren, and C. T.-C. Nguyen, “RF MEMS Resonators: Getting the Right Frequency and Q,” in *IEEE Compound Semiconductor Integrated Circuit Symposium, 2007. CSIC 2007*, 2007, pp. 1–4.

[86] D. E. Serrano, R. Tabrizian, and F. Ayazi, “Tunable piezoelectric MEMS resonators for real-time clock,” 2011, pp. 1–4.

[87] C. S. Lam, “A review of the recent development of MEMS and crystal oscillators and their impacts on the frequency control products industry,” in *IEEE Ultrasonics Symposium, 2008. IUS 2008*, 2008, pp. 694–704.

[88] Y.-W. Lin, S. Lee, S.-S. Li, Y. Xie, Z. Ren, and C. T.-C. Nguyen, “Series-resonant VHF micromechanical resonator reference oscillators,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2477–2491, Dec. 2004.

[89] S. Tabatabaei and A. Partridge, “Silicon MEMS Oscillators for High-Speed Digital Systems,” *IEEE Micro*, vol. 30, no. 2, pp. 80–89, Mar. 2010.

[90] C. T.-C. Nguyen, “MEMS technology for timing and frequency control,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 54, no. 2, pp. 251–270, Feb. 2007.

[91] A. Uranga, J. Verd, and N. Barniol, “CMOS–MEMS resonators: From devices to applications,” *Microelectron. Eng.*, vol. 132, pp. 58–73, Jan. 2015.

[92] J. Wang, Z. Ren, and C. T.-C. Nguyen, “1.156-GHz self-aligned vibrating micromechanical disk resonator,” *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 51, no. 12, pp. 1607–1628, Dec. 2004.

[93] Y. Lin, T. Riekkinen, Wei-Chang Li, E. Alon, and C. T.-C. Nguyen, “A metal micromechanical resonant switch for on-chip power applications,” 2011, p. 20.6.1-20.6.4.

[94] K. Wang, A.-C. Wong, and C. T.-C. Nguyen, “VHF free-free beam high-Q micromechanical resonators,” *J. Microelectromechanical Syst.*, vol. 9, no. 3, pp. 347–360, Sep. 2000.

[95] M. A. Schmidt and R. T. Howe, “Silicon Resonant Microsensors,” in *14th Automotive Materials Conference: Ceramic Engineering and Science Proceedings*, W. Smothers, Ed. John Wiley & Sons, Inc., 1987, pp. 1019–1034.

[96] C. Gehin, C. Barthod, and Y. Teisseyre, “Design and characterisation of a new force resonant sensor,” *Sens. Actuators Phys.*, vol. 84, no. 1–2, pp. 65–69, Aug. 2000.

[97] T. A. Roessig, R. T. Howe, A. P. Pisano, and J. H. Smith, “Surface-micromachined resonant accelerometer,” 1997, vol. 2, pp. 859–862.

[98] V. Ferrari, A. Ghisla, D. Marioli, and A. Taroni, “Silicon resonant accelerometer with electronic compensation of input-output cross-talk,” *Sens. Actuators Phys.*, vol. 123–124, pp. 258–266, Sep. 2005.

[99] K. E. B. Thornton, D. Uttamchandani, and B. Culshaw, “Novel optically excited resonant pressure sensor,” *Electron. Lett.*, vol. 24, no. 10, pp. 573–574, May 1988.

[100] R.-C. Lin, Y.-C. Chen, W.-T. Chang, C.-C. Cheng, and K.-S. Kao, “Highly sensitive mass sensor using film bulk acoustic resonator,” *Sens. Actuators Phys.*, vol. 147, no. 2, pp. 425–429, Oct. 2008.

[101] C. M. Jha, G. Bahl, R. Melamud, S. A. Chandorkar, M. A. Hopcroft, B. Kim, M. Agarwal, J. Salvia, H. Mehta, and T. W. Kenny, “Cmos-Compatible Dual-Resonator MEMS Temperature Sensor with Milli-Degree Accuracy,” 2007, pp. 229–232.

[102] Z. Kádár, A. Bossche, P. M. Sarro, and J. R. Mollinger, “Magnetic-field measurements using an integrated resonant magnetic-field sensor,” *Sens. Actuators Phys.*, vol. 70, no. 3, pp. 225–232, Oct. 1998.

[103] B. Bahreyni and C. Shafai, “A Resonant Micromachined Magnetic Field Sensor,” *IEEE Sens. J.*, vol. 7, no. 9, pp. 1326–1334, Sep. 2007.

[104] B. Ilic, D. Czaplewski, M. Zalalutdinov, H. G. Craighead, P. Neuzil, C. Campagnolo, and C. Batt, “Single cell detection with micromechanical oscillators,” *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.*, vol. 19, no. 6, p. 2825, 2001.

[105] B. P. Harrington, R. Abdolvand, A. Hajjam, J. C. Wilson, and S. Pourkamali, “Thin-film piezoelectric-on-silicon particle mass sensors,” 2010, pp. 238–241.

[106] G. Stemme, “Resonant silicon sensors,” *J. Micromechanics Microengineering*, vol. 1, no. 2, p. 113, Jun. 1991.

[107] L. Lin, R. T. Howe, and A. P. Pisano, “Microelectromechanical filters for signal processing,” *J. Microelectromechanical Syst.*, vol. 7, no. 3, pp. 286–294, Sep. 1998.

[108] C. T.-C. Nguyen, “Transceiver front-end architectures using vibrating micromechanical signal processors,” 2001, pp. 23–32.

[109] J. Basu and T. K. Bhattacharyya, “Microelectromechanical resonators for radio frequency communication applications,” *Microsyst. Technol.*, vol. 17, no. 10–11, pp. 1557–1580, Oct. 2011.

[110] M. Rinaldi, C. Zuniga, C. Zuo, and G. Piazza, “AlN contour-mode resonators for narrow-band filters above 3 GHz,” 2009, pp. 70–74.

[111] D. Weinstein, S. A. Bhave, M. Tada, S. Mitarai, and S. Morita, “Mechanical Coupling of 2D Resonator Arrays for MEMS Filter Applications,” in *Frequency Control Symposium, 2007 Joint with the 21st European Frequency and Time Forum. IEEE International*, 2007, pp. 1362–1365.

[112] S. Pourkamali and F. Ayazi, “Electrically coupled MEMS bandpass filters,” *Sens. Actuators Phys.*, vol. 122, no. 2, pp. 307–316, Aug. 2005.

[113] J. E.-Y. Lee, J. Yan, and A. A. Seshia, “Anchor limited Q in flexural mode resonators,” 2008, pp. 2213–2216.

[114] M. A. Rasouli and B. Bahreyni, “Independent tuning of quality factor and resonant frequency of torsional micro-resonators for timing and sensing applications,” 2011, pp. 2490–2493.

[115] Z. J. Davis, W. Svendsen, and A. Boisen, “Design, fabrication and testing of a novel MEMS resonator for mass sensing applications,” *Microelectron. Eng.*, vol. 84, no. 5–8, pp. 1601–1605, May 2007.

[116] M. U. Demirci and C. T.-C. Nguyen, “Mechanically Corner-Coupled Square Microresonator Array for Reduced Series Motional Resistance,” *J. Microelectromechanical Syst.*, vol. 15, no. 6, pp. 1419–1436, Dec. 2006.

[117] J. Yan, A. A. Seshia, K. L. Phan, P. G. Steeneken, and J. T. M. van Beek, “Narrow Bandwidth Single-Resonator MEMS Tuning Fork Filter,” in *Frequency Control Symposium, 2007 Joint with the 21st European Frequency and Time Forum. IEEE International*, 2007, pp. 1366–1369.

[118] T. Mattila, J. Kiihamäki, T. Lamminmäki, O. Jaakkola, P. Rantakari, A. Oja, H. Seppä, H. Kattelus, and I. Tittonen, “A 12 MHz micromechanical bulk acoustic mode oscillator,” *Sens. Actuators Phys.*, vol. 101, no. 1–2, pp. 1–9, Sep. 2002.

[119] D. Weinstein and S. A. Bhave, “Internal Dielectric Transduction in Bulk-Mode Resonators,” *J. Microelectromechanical Syst.*, vol. 18, no. 6, pp. 1401–1408, Dec. 2009.

[120] F. Lochon, I. Dufour, and D. Rebière, “An alternative solution to improve sensitivity of resonant microcantilever chemical sensors: comparison between using high-order modes and reducing dimensions,” *Sens. Actuators B Chem.*, vol. 108, no. 1–2, pp. 979–985, Jul. 2005.

[121] G. K. Ho, R. Abdolvand, and F. Ayazi, “High-order composite bulk acoustic resonators,” 2007, pp. 791–794.

[122] K. Naeli and O. Brand, “Dimensional considerations in achieving large quality factors for resonant silicon cantilevers in air,” *J. Appl. Phys.*, vol. 105, no. 1, p. 14908, Jan. 2009.

[123] G. Wu, D. Xu, B. Xiong, and Y. Wang, “A high-performance bulk mode single crystal silicon microresonator based on a cavity-SOI wafer,” *J. Micromechanics Microengineering*, vol. 22, no. 2, p. 25020, 2012.

[124] S. Pourkamali, A. Hashimura, R. Abdolvand, G. K. Ho, A. Erbil, and F. Ayazi, “High-Q single crystal silicon HARPSS capacitive beam resonators with self-aligned sub-

100-nm transduction gaps," *J. Microelectromechanical Syst.*, vol. 12, no. 4, pp. 487–496, Aug. 2003.

[125] V. Kaajakari, T. Mattila, A. Lipsanen, and A. Oja, "Nonlinear mechanical effects in silicon longitudinal mode beam resonators," *Sens. Actuators Phys.*, vol. 120, no. 1, pp. 64–70, Apr. 2005.

[126] R. C. Jaeger, *Introduction to microelectronic fabrication*, 2nd ed. Upper Saddle River, N.J: Prentice Hall, 2002.

[127] P. N. Minh, O. Takahito, and E. Masayoshi, *Fabrication of Silicon Microprobes for Optical Near-Field Applications*. CRC Press, 2002.

[128] Y. Ahn, H. Guckel, and J. D. Zook, "Capacitive microbeam resonator design," *J. Micromechanics Microengineering*, vol. 11, no. 1, pp. 70–80, Jan. 2001.

[129] H. A. C. Tilmans, "Equivalent circuit representation of electromechanical transducers: I. Lumped-parameter systems," *J. Micromechanics Microengineering*, vol. 6, no. 1, pp. 157–176, Mar. 1996.

[130] J. Bardeen and W. Shockley, "Deformation Potentials and Mobilities in Non-Polar Crystals," *Phys. Rev.*, vol. 80, no. 1, pp. 72–80, Oct. 1950.

[131] *Atlas User's Manual*. Silvaco, Inc., 2013.

[132] I. Goroff and L. Kleinman, "Deformation Potentials in Silicon. III. Effects of a General Strain on Conduction and Valence Levels," *Phys. Rev.*, vol. 132, no. 3, pp. 1080–1084, Nov. 1963.

[133] M. Lades, J. Frank, J. Funk, and G. Wachutka, "Analysis of Piezoresistive Effects in Silicon Structures Using Multidimensional Process and Device Simulation," in *Simulation of Semiconductor Devices and Processes*, U.-P. D. H. Ryssel and D. P. Pichler, Eds. Springer Vienna, 1995, pp. 22–25.

[134] M. S. Hajhashemi, A. Rasouli, and B. Bahreyni, "Fabrication of resonant sensors with significantly improved sensitivity through strong mechanical coupling," 2015, pp. 149–152.

[135] M. S. Hajhashemi, A. Rasouli, and B. Bahreyni, "Improving Sensitivity of Resonant Sensor Systems Through Strong Mechanical Coupling," *J. Microelectromechanical Syst.*, vol. 25, no. 1, pp. 52–59, Feb. 2016.