TOPOLOGY ZERO:
ADVANCING THEORY AND EXPERIMENTATION FOR POWER ELECTRONICS EDUCATION

by

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Abstract

For decades, power electronics education has been based on the fundamentals of three basic topologies: buck, boost, and buck-boost. This thesis presents the analytical framework for the Topology Zero, a general circuit topology that integrates the basic topologies and provides significant insight into the behaviour of converters. As demonstrated, many topologies are just particular cases of the Topology Zero, an important contribution towards the understanding, integration, and conceptualization of topologies. The investigation includes steady-state, small-signal, and frequency response analysis. The Topology Zero is physically implemented as an educational system. Experimental results are presented to show control applications and power losses analysis using the educational system. The steady-state and dynamic analyses of the Topology Zero provide profuse proof of its suitability as an integrative topology, and of its ability to be indirectly controlled. As well, the implementation of the Topology Zero within an experimentation system is explained and application examples are provided.

Keywords: power electronics; education; converter

To the exceptional people who marked my life

"When the dogs bark we know we are riding on horseback"

Johann Wolfgang von Goethe

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I would like to particularly thank Nancy, the only reason this document exists.

The last but foremost, I would like to really thank my family, who are the ones I care for the most, especially my parents Ana and Clemar, who unconditionally supported me through the years in the decisions that I have made.

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Nomenclature

C	Capacitance
D	Diode
D, d	Duty cycle
F_{SW}	Switching frequency
G_{vd}	Control-to-output transfer function
I, i	Current
L	Inductance
P	Power
Q	Transistor
R	Resistance
SW	Switch
T_{SW}	Switching period
V, v	Voltage
V_i, v_i	Input voltage
V_o, v_o	Output voltage
Z	Impedance
η	Efficiency

$\hat{d}$	Duty cycle perturbation
$\hat{i}$	Current perturbation
$\hat{v}$	Voltage perturbation
$\mathbf{A}$	State matrix
$\mathbf{B}$	Input matrix
$\mathbf{C}$	Output matrix
$\mathbf{K}$	Coefficient matrix
$\hat{\mathbf{u}}$	Input vector perturbation
$\hat{\mathbf{x}}$	State vector perturbation
$\hat{\mathbf{y}}$	Output vector perturbation
$\mathbf{u}$	Input vector
$\mathbf{x}$	State vector
$\mathbf{y}$	Output vector
s	Laplace variable
t	Time

Chapter 1

Introduction

Power electronics is ubiquitous in everyday people's lives. For the past couple of decades it has been evolving at a fast pace, and it is being employed in areas where previously it was thought impossible. Additionally, the power range of the applications extends from extremely low power devices (thousandths of Watts) to very high power systems (millions of Watts). Any consumer electronics or high-power electric devices that do not already contain state-of-the-art power electronics circuitry probably will soon.

Successful designers of power electronic devices require expertise in several fields of applied science: analysis of power losses in the switches, heat management, parasitics in the physical layout of the circuit, electromagnetic noise susceptibility and emission, efficiency, control and protections, amongst other considerations. The process of learning power electronics and gaining practical skills in the area typically extends beyond the curriculum of undergraduate training and requires a number of years of graduate studies and/or industrial experience.

1.1 Motivation

In spring 2010, when the author started working toward this thesis, there was an urgent need for custom-made power converters for research purposes in the Renewal and Alternative Power Laboratory. No existing commercial products were able to meet the requirements for the particular projects that were performed at the time and are being performed today. In order to be able to carry out research experimentation in different areas of power electronics,

a decision was made to develop and implement a modular system based on several interconnected power converter platforms according to the topology required for research. As a result, a number of complex power platforms were implemented. However, there was often the need for new designs to cover the fast changing, specific needs of the research laboratory. Therefore, it was resolved to develop a power converter platform with enough flexibility to be adapted to several topologies without requiring changes in the layout. Furthermore, this platform should be able to measure, at different key points, voltage and current for each topology in order to allow the controller to implement suitable control strategies. Simultaneously with the development of the flexible platform, the concept of a new integrative topology emerged, was developed and called Topology Zero, whose basic schematic is shown in Figure 1.1.

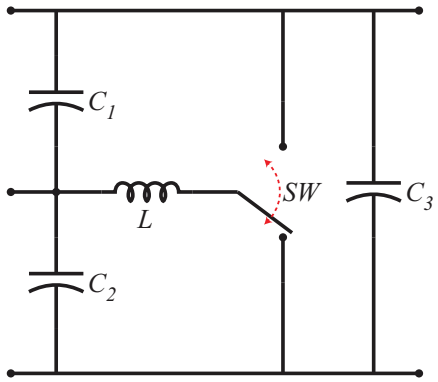


Figure 1.1: Topology Zero.

The name of this topology, Topology Zero, is taken after the term Patient Zero, which first appears in the 1980's in a epidemiological study to refer to the first person who brought the HIV to the USA and spread the disease to other people. In medical terms these individuals are called index cases. The term is currently used to refer to the index case of infectious disease outbreaks, computer virus outbreaks and, the more applicable, to the source of ideas or actions that have far-reaching consequences [1]. The author of this thesis, his senior research supervisor, and the fellow members of the laboratory believe the Topology Zero is the general case and origin of the basic topologies. Buck, boost, and buck-boost topologies (along with their derived topologies) have spread around in countless applications in an epidemic fashion.

1.2 Existing Methodologies in Education

Power electronics is a difficult subject to teach, mainly due to the broad spectrum that it covers, the theoretical background knowledge that is required from students to understand every aspect of the topics, and the experimentation needed for a thorough comprehension of the subject. Several pedagogical approaches to power electronics can be found in the literature.

Rui et al. [2] propose students develop predefined projects where power electronics concepts are employed, specifically H-bridge for motor control with torque feedback. However, the spectrum of power electronics applied in these projects is narrow. Other courses aim to gain good knowledge in component calculation, basic operation of converters and losses calculation [3], [4]. Even though the knowledge gained is important, these courses focus on few converters and do not cover control techniques. Web-based reconfigurable power electronics experimentation platforms are used for teaching and research purposes as well [5], [6]. The systems are remotely operated and a broad selection of converters can be chosen. The drawbacks of these systems are the implementation costs and mainly, the lack of contact that students have with the real devices, which could lead them to confuse real experiments with computer-based simulations. Additionally closed-loop operation can be applied to the topologies [6]. A similar, more modest approach is found in Hurley et al. [7]. Probst [8] shows a course based on both simulation and hands-on exercises. The simulation application and the physical platform are developed ad hoc. The system allows a variety of configurations and implementation of control techniques. However, these control loops are only basic linear controllers and, the processor employed only performs simple operations. Williams et al. [9] offer a power electronics system that permits interconnection among different modules. Although the platform is good for teaching purposes, it has limited use in research, due to the parasitics that that layout is susceptible to and the circuitry they use to generate the power signals. Max et al. [10] focus on a real problem in converters such as parasitics. The exercises are based on one converter and they require students to design solutions in order to improve the converter operation. Monroy-Berjillos et al. [11] developed a setup to control thyristors. Showing how mechanical switches can be replaced by semiconductor devices. The system helps to give an insight into this field of power electronics, though it does not extend to the other aspects of the subject. Power electronics is applied to motor control in some courses [12], [13]. They control the devices using virtual

instrumentation through a computer. One disadvantage of this systems is the high cost of the equipment and its maintenance. Web-browser-based simulation tools have been developed specifically for teaching purposes [14], [15]. The simulation only uses ideal components to perform the analyses. It is meant to give a qualitative idea of power system operation. Afterward, the results are compared with more realistic simulation software and educational setups. Jimenez-Martinez et al. [16] integrate hardware and simulation. The system adapts into several topologies and is controlled through a computer. However, it operates only in open-loop mode. Good examples of power electronics systems for educational purposes have been developed [17], [18], [19], [20]. They offer an adequate variety of topologies to implement, and sensors of voltage and current are added to allow closed-loop operation. Robbins et al. [17] employ the switching pole methodology for obtaining different topologies. Guseme at al. [18] implement a similar switching building block to achieve different converters. The switching pole and building block are very useful concepts but they are not a topology. Therefore, they lack the theoretical framework that power converters typically have, such as steady-state and dynamic analyses. Balog et al. [19] use the blue-box module concept, where the modules are first explained in detail, and then employed as closed modules. Additionally, Jakopovic [20] developed some simulation tools specially for the courses.

The aforementioned systems cover collectively a broad spectrum of approaches within power electronics. Some of the approaches focus on simulation or remote experimentation while others put emphasis on hands-on experiments. Although, the extent of the topics covered for each of them varies, their individual breadth is somewhat limited. A consideration for the remotely-connected physical setups is the need to have dedicated instruments attached to the system all the time. Another notable aspect is that not many programs offer control strategies, neither linear nor non-linear, of power converters. Additionally, analysis of parasitics is neglected in most of the setups described in the literature. Although there are good examples of setups, some proposed components, such as the current sensors present issues with range, frequency bandwidth and noise.

From the above concerns, there is a need to develop a platform able to cover the needs of both basic power electronics courses and advanced research experimentation. In addition, some specific requirements have to be met by this setup. First, it has to be flexible in order to select the topology desired; relatively low cost, with several options for parameter sensing. Second, it has to provide flexibility in the power devices employed, different technologies of

transistors and diodes according to the voltage and current specifications for the topology chosen. Moreover, isolation and modularity are key features to take into consideration. In addition, although the components of the platform need to be accessible for teaching purposes, layout constraints to avoid parasitics have to be observed. Finally, the possibility of implementing different control techniques is one of the most important aspect of the development. The consideration of these points in the context of the implementation of the Topology Zero as an integrative architecture constitute the subject of this thesis.

1.3 Contribution of This Thesis

This work consists of two main sections. The first part of this document explores a new approach in the style that basic DC-DC switching mode power converters are studied, introducing the Topology Zero that integrates the three basic conversion topologies, namely step-down, step-up and step-down-step-up; each of them with more than one option of implementation. The purpose of the Topology Zero is to facilitate the comprehension of power converters and to provide a different perspective in the analysis of switching converters and the way they can be controlled. Different methods of steady-state analysis are derived to demonstrate the operation of each configuration and equal outcomes are obtained. As well, a dynamic study in the form of small-signal analysis is performed and the results are compared with computer-based circuit simulation for frequency and step responses to confirm the outstanding match between the derivation and the simulation.

In the second part of this document, the physical implementation of the Topology Zero is discussed. The requirement for this implementation is to obtain a cost-effective and flexible system that allows different setups to evaluate the basic DC-DC power converters, including measurements and communication to a personal computer or other similar platforms. The system is intended to be used for senior undergraduate students in power electronics courses as well as graduate students in their research projects. Experimental results are presented to show control applications and power losses analysis using the Topology Zero educational setup, work that led to a number of IEEE research papers.

1.4 Thesis Outline

This work is organized in the following form:

Chapter 2 introduces the Topology Zero and then focuses on the derivation of the steady-state equations of each of the possible configurations that this topology offers, along with optional forms of derivation. Additionally, the Topology Zero is compared with well-known topologies to prove its suitability as a valid converter.

In Chapter 3, small-signal analysis is applied to obtain a transfer function for each configuration of the Topology Zero and to study their dynamic responses. The results of the analytical derivation are compared to computer-based circuit simulation to verify their accuracy.

In Chapter 4, more realistic switching elements are introduced. Many different configurations which involve particular cases of the original Topology Zero are explored. Afterwards, an introduction to power loss and efficiency is included for different configurations of the topology.

In Chapter 5, the physical implementation of the educational setup based on the Topology Zero is described. The different modules and their corresponding sub-modules are explained. Additionally, the experimental setups of three IEEE published research articles using the educational setup based on the Topology Zero are depicted. Afterwards, several examples of the successful implementation of the Topology Zero are mentioned.

Finally in Chapter 6, conclusions of this work, suggestions for improvement and future research are discussed.

Chapter 2

Topology Zero: Steady-state Analysis

This chapter introduces the Topology Zero, a general theoretical framework developed to study and perform experimentation of basic and derived power converter topologies. The Topology Zero provides remarkable insight into the steady-state and dynamic analyses of power converters, resulting in a unified theory that facilitates the comprehension of power electronics conversion. The Topology Zero consists of a circuit with only three power connections that allow it to implement step-down, step-up and step-down-step-up DC-DC topologies, as well as, more complex converters, by only changing the location of the power supply and the load among those three connections. The basic circuit is shown in Figure 2.1. The letters **A**, **B**, **C** and **D** denote the nodes of the Topology Zero, and facilitate their identification throughout the different configurations.

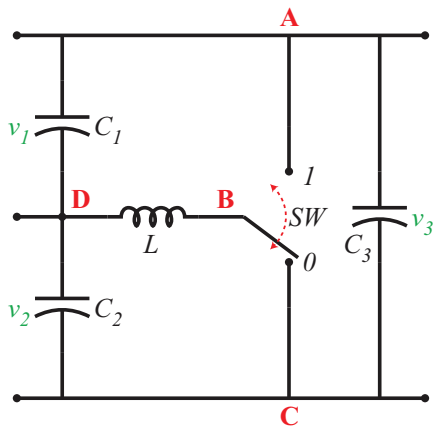


Figure 2.1: Topology Zero.

The power supply and the load can be connected in any of the connection ports indicated by v_1, v_2 or v_3. In addition, the relationship of these 3 voltages is given by

$$\boxed{v_3 = v_1 + v_2} \tag{2.1}$$

The ratio between the time that the switch is in state 1 ($t_{(1)}$) over the switching period (T_{SW}) is called duty cycle (D) and defined as

$$D = \frac{t_{(1)}}{T_{SW}}, \quad 0 \leq D \leq 1 \tag{2.2}$$

The graphic representation of the switching period and the duty cycle is shown in Figure 2.2

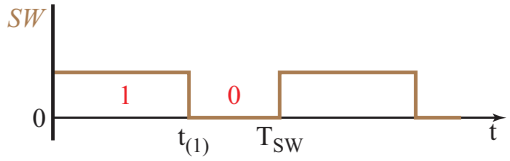


Figure 2.2: Switching cycle.

The different configurations that can be accomplished with the Topology Zero are listed in Table 2.1

Table 2.1: Topology Zero DC-DC configurations.

Power supply connected to	Load connected to	Configuration
v_1	v_2	Step-down-step-up configuration with negative reference
v_1	v_3	Step-up configuration with positive reference
v_2	v_1	Step-down-step-up configuration with positive reference
v_2	v_3	Step-up configuration with negative reference
v_3	v_1	Step-down configuration with positive reference
v_3	v_2	Step-down configuration with negative reference

The operation of these configurations with analysis of the steady-state are described next.

2.1 Step-down Configurations

Step-down converters are used to provide controlled power at lower voltage than the input. They are vastly used in consumer electronics devices such as AC-DC adapters or battery chargers. Step-down converters perform the same function as linear voltage regulators, however, switched regulators have higher efficiency. The circuit shown in Figure 2.3 represents the Topology Zero step-down configuration, where the power supply (V_i) is connected to v_3 and the load (R) to v_2. Here, the common point between input and output is the negative voltage of the power supply. The term negative reference is used to emphasize that the negative terminal of the input power supply is directly connected to the output voltage terminal. Figure 2.4 shows the waveforms for steady-state condition of the Topology Zero step-down configuration with negative reference.

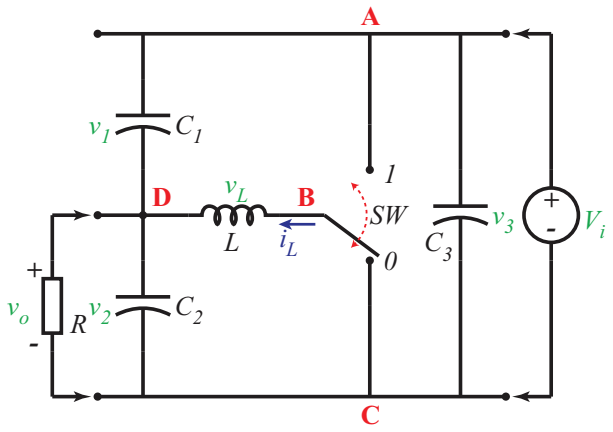


Figure 2.3: Step-down configuration with negative reference.

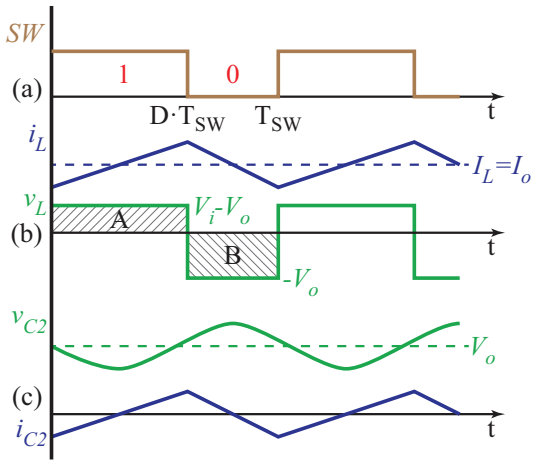


Figure 2.4: Step-down configuration steady-state waveforms. (a) Switch position. (b) Inductor current (i_L) and voltage (v_L). (c) C_2 current (i_{C2}) and voltage (v_{C2}).

The voltage across an inductor can be characterized by

$$v_L = L\frac{di_L(t)}{dt} \tag{2.3}$$

In steady-state the average voltage in the inductor (V_L) is equal to $0V$. In Figure 2.4b, the areas A and B are equal to maintain the voltage balance in the inductor. In other words, the integral of v_L in the interval $D \cdot T_{SW}$ is equal to the one in the interval $(1-D) \cdot T_{SW}$.

$$(V_i - V_o) \cdot D \cdot T_{SW} = V_o \cdot (1-D) \cdot T_{SW} \tag{2.4}$$

Deriving

$$V_i \cdot D - V_o \cdot D = V_o - V_o \cdot D$$

Then, the equation that describes the output-input voltage relationship in steady-state is

$$\frac{V_o}{V_i} = D \tag{2.5}$$

It can be stated from (2.5) that the output voltage V_o varies from 0 to V_i as D changes from 0 to 1. The step-down configuration reduces the input voltage by a factor of D.

If the load is connected to v_1 instead, the common point between input and output is the positive connection of the power supply. In this configuration, the inductor is charged when the switch is in state 0 and the current through it flows in opposite direction compared to the previous case. The circuit and the signals for this configuration can be observed in Figure 2.5 and Figure 2.6 respectively.

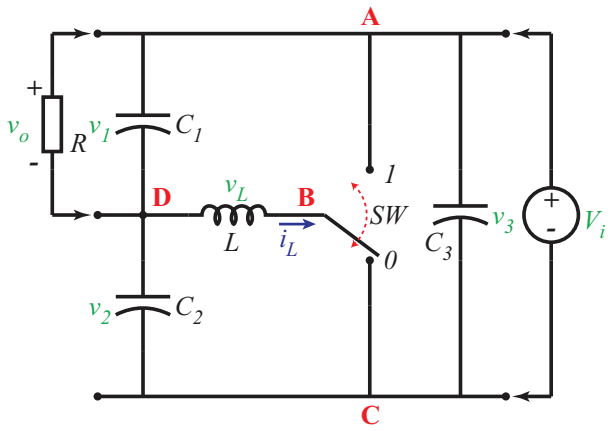


Figure 2.5: Step-down configuration with positive reference.

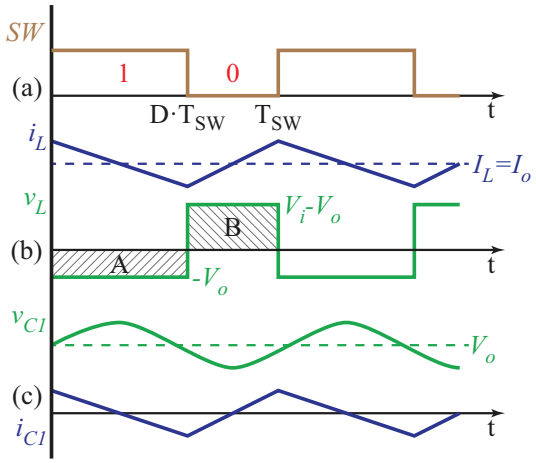


Figure 2.6: Step-down configuration steady-state waveforms. (a) Switch position. (b) Inductor current (i_L) and voltage (v_L). (c) C_1 current (i_{C1}) and voltage (v_{C1}).

The inductor voltage balance, in steady-state, can be expressed as

$$V_o \cdot D \cdot T_{SW} = (V_i - V_o) \cdot (1 - D) \cdot T_{SW} \tag{2.6}$$

Deriving

$$\begin{aligned} V_o \cdot D &= V_i - V_o - V_i \cdot D + V_o \cdot D \\ V_o &= V_i\,(1 - D) \end{aligned}$$

The output-input voltage ratio is

$$\frac{V_o}{V_i} = 1 - D \tag{2.7}$$

In this configuration, when D increases, V_o decreases. The variation of the output voltage in (2.7) responds in opposite fashion compared to (2.5).

2.2 Step-up Configurations

Step-up converters are used to supply output voltage greater than the input. They are employed in consumer electronics devices, and industrial grade systems such as power factor correctors (PFC). The circuit shown in Figure 2.7 represents the Topology Zero step-up configuration, where the power supply is connected to v_2 and the load to v_3. The reference point between power supply and load is the negative terminal of the supply. In this configuration the inductor is charged when the switch is in the position 0. Figure 2.8 shows

the waveforms for steady-state condition of the Topology Zero step-up configuration with negative reference.

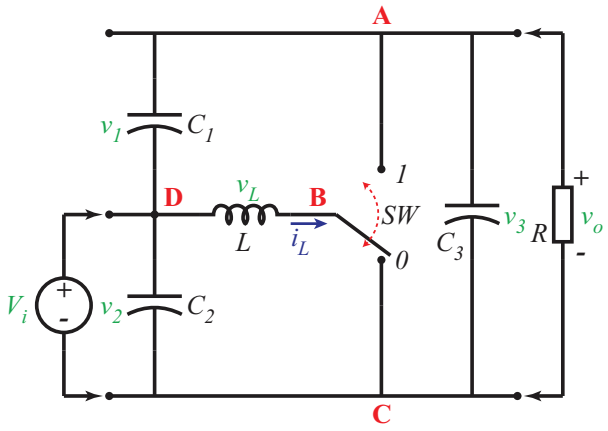


Figure 2.7: Step-up configuration with negative reference.

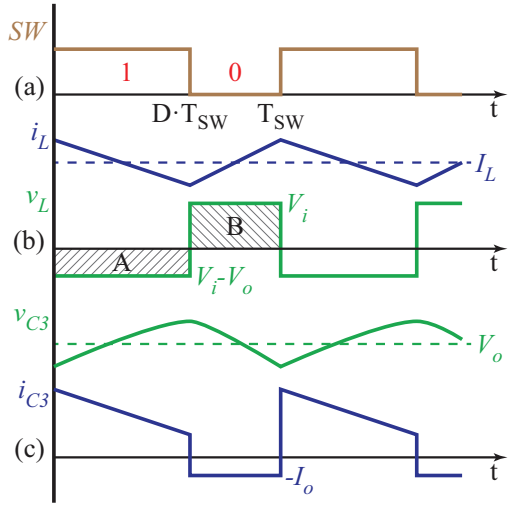


Figure 2.8: Step-up configuration steady-state waveforms. (a) Switch position. (b) Inductor current (i_L) and voltage (v_L). (c) C_3 current (i_{C3}) and voltage (v_{C3}).

In Figure 2.8b it can be seen that the voltage balance in the inductor has to be met in steady-state. Hence the areas A and B are equal. this can be written as follow

$$(V_o - V_i) \cdot D \cdot T_{SW} = V_i \cdot (1 - D) \cdot T_{SW} \tag{2.8}$$

Deriving

$$V_o \cdot D - V_i \cdot D = V_i - V_i \cdot D$$

Then, the equation that describes the output-input voltage relationship in steady-state is

$$\frac{V_o}{V_i} = \frac{1}{D} \tag{2.9}$$

Looking at (2.9), it can be observed that the output voltage ranges from V_i to ∞ (ideal), when D goes from 1 to 0. Hence, this configuration augments the input voltage by a factor $1/D$.

If the power supply is connected to v_1 instead, the reference point between supply and load is the positive end of the supply and the inductor is charged when the switch is in state 1, its current flows in opposite direction compared to the previous case. The circuit and the signals for this configuration can be observed in Figure 2.9 and Figure 2.10 respectively.

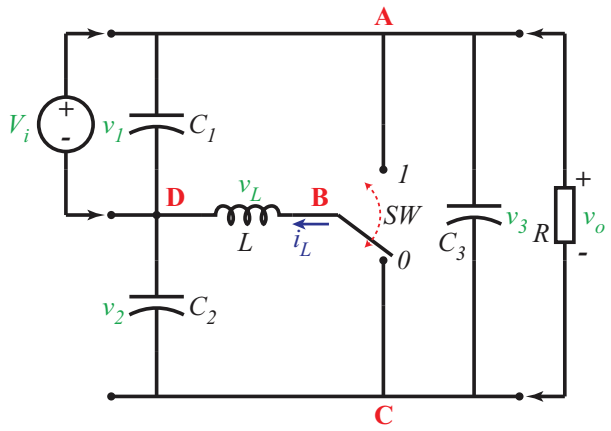


Figure 2.9: Step-up configuration with positive reference.

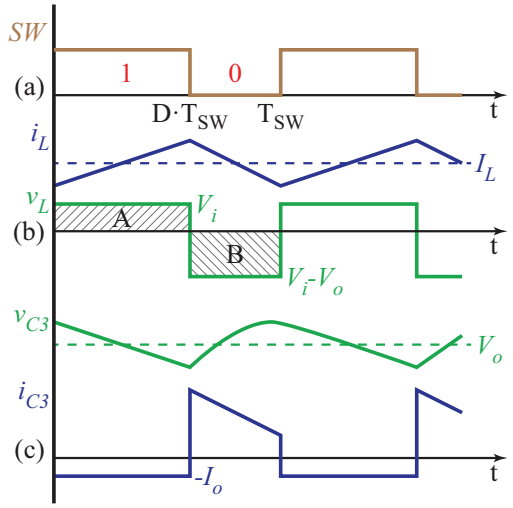


Figure 2.10: Step-up configuration steady-state waveforms. (a) Switch position. (b) Inductor current (i_L) and voltage (i_L). (c) C_3 current (i_{C3}) and voltage (v_{C3}).

The inductor voltage balance in steady-state, gives

$$V_i \cdot D \cdot T_{SW} = (V_o - V_i) \cdot (1 - D) \cdot T_{SW} \tag{2.10}$$

Deriving

$$\begin{aligned} V_i \cdot D &= V_o - V_i - V_o \cdot D + V_i \cdot D \\ V_i &= V_o\,(1 - D) \end{aligned}$$

The output-input voltage ratio is then

$$\frac{V_o}{V_i} = \frac{1}{1 - D} \tag{2.11}$$

This configuration acts in a complementary mode compared to the step-up with negative reference. Here the voltage increases from V_i to ∞, when D increases from 0 to 1, as expressed in (2.11).

2.3 Step-down-step-up Configurations

Step-down-step-up converters may be applied for power supplies where the output can be either higher or lower than the input voltage, another feature of this converter is that the load has opposite polarity than the input voltage referred to the common point between them, unlike the previous configurations. The circuit shown in Figure 2.11 represents the

Topology Zero step-down-step-up configuration, where the power supply is connected to v_1 and the load to v_2. In this arrangement, the common point between input and output is the negative terminal of the power supply. Figure 2.12 shows the waveforms for steady-state condition of the circuit.

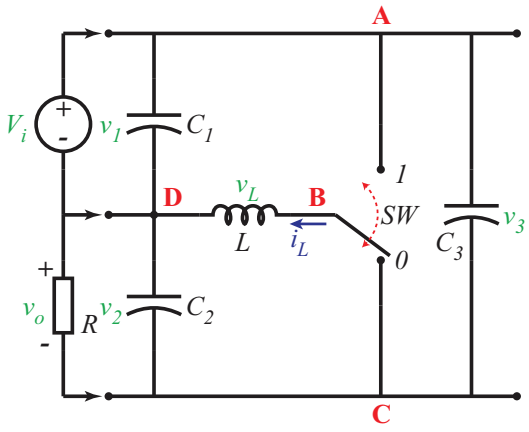


Figure 2.11: Step-down-step-up configuration with negative reference.

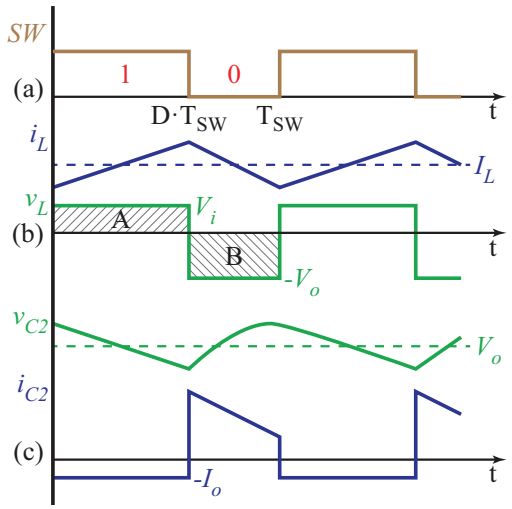


Figure 2.12: Step-down-step-up configuration steady-state waveforms. (a) Switch position. (b) Inductor current (i_L) and voltage (v_L). (c) C_2 current (i_{C2}) and voltage (v_{C2}).

In steady-state, the areas A and B in Figure 2.12b are equal to maintain the voltage

balance in the inductor. in equation form this is

$$V_i \cdot D \cdot T_{SW} = V_o \cdot (1 - D) \cdot T_{SW} \tag{2.12}$$

Then, the equation that describes the output-input voltage relationship in steady-state is

$$\frac{V_o}{V_i} = \frac{D}{1 - D} \tag{2.13}$$

Based on (2.13), the output voltage ranges from 0 to ∞, when D goes from 0 to 1. This configuration can make the output voltage greater or less than the input voltage. The output voltage equals the input voltage when $D = 0.5$.

If the power supply is connected to v_2 and the load to v_1, the common point is the positive end of the supply. In this configuration, the inductor is charged when the switch is in the state 0, its current flows in opposite direction compared to the previous case. The circuit and the signals for this configuration can be observed in Figure 2.13 and Figure 2.14 respectively.

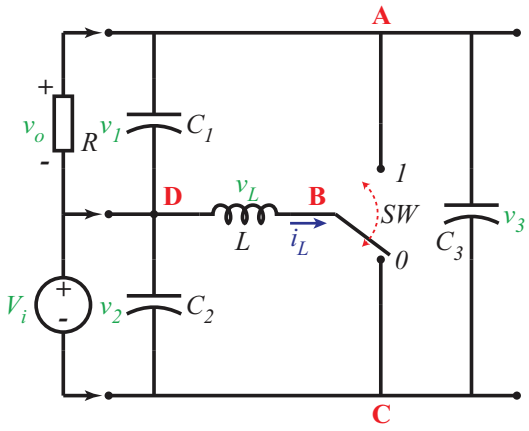


Figure 2.13: Step-down-step-up configuration with positive reference.

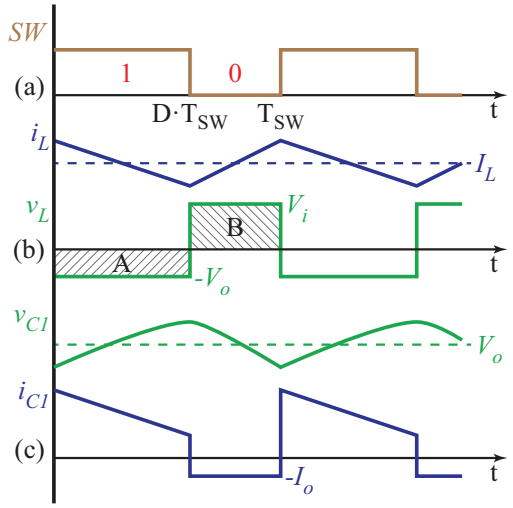


Figure 2.14: Step-down-step-up configuration steady-state waveforms. (a) Switch position. (b) Inductor current (i_L) and voltage (v_L). (c) C_1 current (i_{C1}) and voltage (v_{C1}).

The inductor voltage balance in steady-state, gives

$$V_o \cdot D \cdot T_{SW} = V_i \cdot (1 - D) \cdot T_{SW} \tag{2.14}$$

Then, the output-input voltage ratio is

$$\frac{V_o}{V_i} = \frac{1 - D}{D} \tag{2.15}$$

Based on (2.15), the output voltage ranges from 0 to ∞, when D goes from 1 to 0. This configuration responds in opposite form to the change of the duty cycle than the step-down-step-up with negative reference.

2.4 Alternative Derivation

Another approach to obtain the equations of the different configurations in steady-state operation, is combining the transfer ratio of one known topology with (2.1).

Consider the Topology Zero step-down configuration with negative reference shown in Figure 2.3 with its signals in Figure 2.4 and its transfer ratio is given by (2.5). The equation is restated using V_2 and V_3

$$V_2 = D \cdot V_3 \tag{2.16}$$

Having (2.16) then, V_1 as a function of V_2 and V_3 can be deduced, therefore, another configuration

$$V_1 = V_3 - V_2 = V_3 - D \cdot V_3$$

then,

$$V_1 = (1 - D)\, V_3 \tag{2.17}$$

This result is equivalent to (2.7) that belongs to the step-down configuration with positive reference shown in Figure 2.5.

Similarly,

$$V_1 = V_3 - V_2 = \frac{1}{D} V_2 - V_2$$

then,

$$V_1 = \frac{(1 - D)}{D} V_2 \tag{2.18}$$

This is equivalent to (2.15) of the step-down-step-up configuration with positive reference shown in Figure 2.13.

If the other variable is solved in each of (2.16), (2.17) and (2.18), the transfer functions of the remaining configurations are obtained.

$$V_3 = \frac{1}{D} V_2 \tag{2.19}$$

Equivalent to (2.9), step-up configuration with negative reference.

$$V_3 = \frac{1}{(1 - D)} V_1 \tag{2.20}$$

Equivalent to (2.11), step-up configuration with positive reference.

$$V_2 = \frac{D}{(1 - D)} V_1 \tag{2.21}$$

Equivalent to (2.13), step-down-step-up configuration with negative reference.

The diagram in Figure 2.15 shows the relationship among the different conversion configurations for the Topology Zero, based on the previous results.

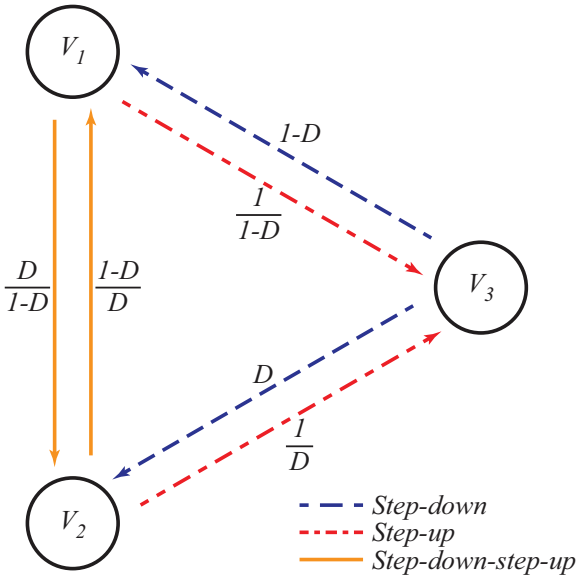


Figure 2.15: Relationship among conversions with Topology Zero.

These results have an important value in control, due to the fact that a desired configuration can be indirectly controlled using one of the other topologies' algorithm in order to simplify either the algorithm or the measurement. As an example consider the step-down-step-up configuration measuring the input voltage (v_1 or v_2) and controlling v_3 to obtain the output (v_2 or v_1).

Hitherto, a steady-state study has been carried out to show the different conversion modes of the Topology Zero. Furthermore, an alternative derivation has been presented, that takes the result of any known configuration and the other ones can be obtained with no complication. This derivation has the advantage of allowing indirect control of any configuration.

2.5 A General Topology: One Topology to Rule Them All

The comparison of the Topology Zero with other known topologies is developed in this section, highlighting similarities and advantages of using one topology that can operate as six different converters as it is required.

2.5.1 Buck Converter

A basic buck converter is shown in Figure 2.16 and its transfer ratio is.

$$\frac{V_o}{V_i} = k \tag{2.22}$$

where k is the fraction of the switching period when the inductor is connected to the power supply.

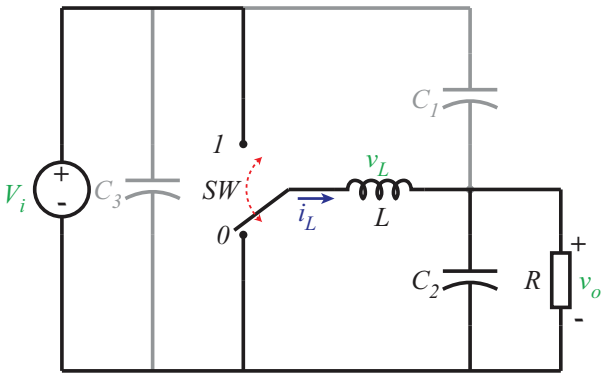


Figure 2.16: Buck converter.

It can be seen that (2.22) is the same as (2.5), Considering $k = D$. This equation corresponds to the Topology Zero step-down configuration with negative reference.

In order to implement a classic buck topology, derived from the Topology Zero, the value of the capacitor C_1 should be equal to 0F, as indicated in Figure 2.16 with a grey symbol. As well, the input voltage source is depicted as an ideal voltage source V_i, which is equivalent to an infinite capacitor C_3 charged at the desired input voltage.

2.5.2 Boost Converter

A boost converter can be represented by the circuit in Figure 2.17 and its transfer ratio is

$$\frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.23}$$

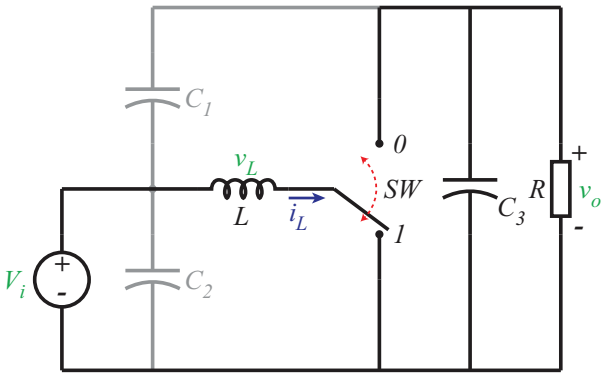


Figure 2.17: Boost converter.

The circuit looks similar to the Topology Zero step-up configuration with negative reference shown in Figure 2.7. The boost topology is implemented with the Topology Zero by setting the value of the capacitor C_1 to 0F, as indicated with a grey symbol in Figure 2.17. Additionally, the input voltage source is depicted as an ideal voltage source V_i, which is equivalent to an infinite capacitor C_2 charged at the desired input voltage. Apparently, the transfer ratio does not match with (2.9). The difference is that k reflects the portion of the switching period when the inductor is getting charged (when the switch is in 1 in Figure 2.17) and, on the other hand, D, in (2.9), describes the portion when the inductance is supplying its energy, in other words, when the switch is in position 1 in Figure 2.7. Thus, in this case $D = 1 - k$. The traditional analysis of the known topologies considers k as the fraction of the switching period when the inductor is charged. That consideration leads to an inversion in the form the switch operates for the boost converter, compared to the other two topologies. This constitutes a drawback in the analysis of the basic converters, due to the fact that, the switch position is not properly consolidated with the rest of the topologies. It can be stated that the operation of the boost converter is a particular case of the Topology Zero. The transfer ratio (2.9) reflects the position of the switch that is compatible with the other two basic configurations.

2.5.3 Buck-boost Converter

A basic buck-boost converter is represented in Figure 2.18 and its transfer ratio is

$$\frac{V_o}{V_i} = \frac{k}{1-k} \tag{2.24}$$

where k is the fraction of the switching period when the inductor is connected to the power supply.

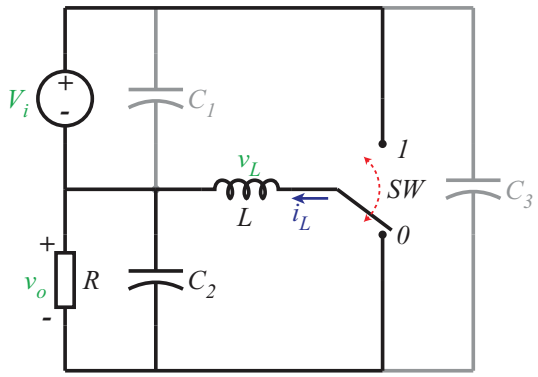


Figure 2.18: Buck-boost converter.

The buck-boost topology is implemented with the Topology Zero by setting the value of the capacitor C_3 to 0F, as indicated with a grey symbol in Figure 2.18. In addition, the ideal input voltage source V_i, can be thought as an infinite capacitor C_1 charged at the desired input voltage. The behaviour using the Topology Zero step-down-step-up configuration with negative reference, shown in Figure 2.13, is the same as the buck-boost topology. It can be noted that (2.24) has the same form as (2.13).

2.6 Summary

This chapter introduced the Topology Zero as a single circuit to cover the basic switching DC-DC converter topologies, step-down, step-up and step-down-step-up. The analysis covered the output-input voltage transfer equation derivation in steady-state and the comparison with known topologies. Additionally, alternative derivation have been demonstrated. From what above is described, it can be said that the Topology Zero can operate as the three basic known DC-DC converters, as well as, other configurations (three positive counter part). Furthermore, these known converters are special cases of the Topology Zero, which can be achieved by eliminating specific capacitors. The study of a single topology has the advantage of simplifying the analysis of each configuration and gives a clear insight into the knowledge of basic power converters. Other advantage of this topology is the possibility of the development of indirect control strategies, measuring one port to control another.

In the next chapter dynamic analyses of the Topology Zero are provided for all its configurations and the results are verified with the results of computer-based circuit simulations.

Chapter 3

Topology Zero: Small-signal Analysis

Switching mode converters inevitably require feedback control loops. The output voltage of the converter must remain constant regardless the variation of the input voltage or output current requirements. Moreover, the feedback control loop must not produce instability in the system, and it has to meet some specifications in the transient and the steady-state operation conditions.

Small-signal analysis for switching converters was first introduced in 1970's by Middlebrook et al. [21], who presented a linearized and averaged analysis intended to simplify the study of switching converters and characterize them, in order to design control strategies. This important contribution in the form of an analytical procedure has been used ever since [22]. Profuse literature can be found in power converter analyses where small-signal is applied to model different converter topologies. For example, the analysis of a three phase buck rectifier, where steady-state and dynamic studies are carried out [23]. As well, several switching schemes of a buck converter are analysed [24]. A boost converter in current mode control is also studied using small-signal [25]. Additionally, the influence of the steady-state operation over the small-signal condition in buck-boost converters is analysed[26]. When digital control schemes are to be applied or large-signals are considered, other complementary methods can be used to characterized power converters. Small-signal analysis gives a powerful insight into the behaviour of the switching systems and provides the foundation to control them. The goal of the small-signal procedure is to obtain a valuable transfer

function that models the converter and is further used to design the control loop.

In this chapter, the small-signal analysis is described for the six possible combinations of the Topology Zero. The analysis starts with the steady-state study of each configuration and then the small-signal is derived from it. Afterward, comparisons with circuit simulation are carried out to validate the results.

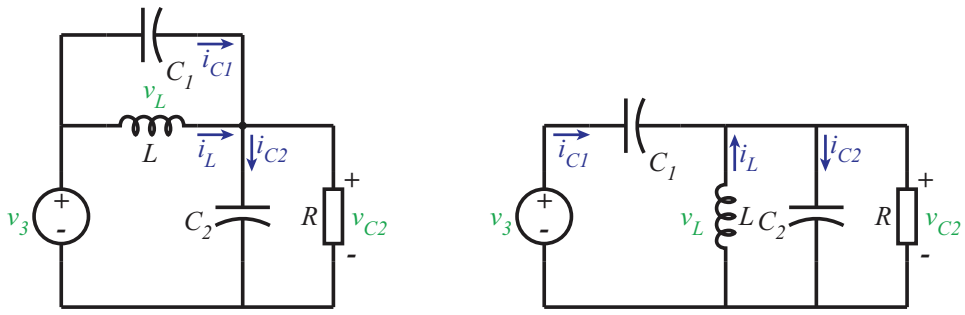
First, a detailed derivation of the analysis is described for the step-down configuration with negative reference. Following, the key equations and figures are shown for the other configurations.

3.1 Topology Zero Step-down Configurations

The small-signal analysis of the step-down configuration with negative reference is first presented in detail, followed by a shorter derivation of the configuration with positive reference.

3.1.1 Step-down Configuration with Negative Reference

Consider the circuit in Figure 2.3, the equivalent circuits for each position of the switch are shown in Figure 3.1.



(a) Switch in position 1 during $d(t)\,T_{SW}$. (b) Switch in position 0 during $d'(t)\,T_{SW}$.

Figure 3.1: Step-down configuration equivalent circuits.

Where $d'(t)$ is defines as

$$d'(t) = 1 - d(t) \tag{3.1}$$

A set of equations can be obtained from the circuit in Figure 3.1a. This circuit represents the configuration when the switch is in position 1 during $d(t)\,T_{SW}$, where $d(t)$ is the time

variant duty cycle.

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = v_{C1}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_3(t) - i_L(t) \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_3(t) - \frac{v_{C2}(t)}{R} \\ v_3(t) = v_{C1}(t) + v_{C2}(t) \end{cases} \tag{3.2}$$

When the switch is in position 0 during $d(t)'T_{SW}$, as shown in Figure 3.1b, the equations that represent the circuit are

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = -v_{C2}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_3(t) \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_3(t) + i_L(t) - \frac{v_{C2}(t)}{R} \\ v_3(t) = v_{C1}(t) + v_{C2}(t) \end{cases} \tag{3.3}$$

In matrix form

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} [i_3] \\ [v_3(t)] = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} \end{cases} \tag{3.4}$$

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & 0 \\ 1 & 0 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} [i_3] \\ [v_3(t)] = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} \end{cases} \tag{3.5}$$

(3.4) and (3.5) are written in state-space form, that has the general structure as

$$\begin{cases} \mathbf{K}\frac{d}{dt}\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} = \mathbf{C}\mathbf{x} \end{cases} \tag{3.6}$$

Where

A is the state matrix	**x** is the state vector
B is the input matrix	**u** is the input vector
K is a coefficient matrix	**y** is the output vector
C is the output matrix	

The averaged equation model is obtained adding each of the particular equations multiplied by the fraction of time they are valid.

$$\begin{aligned} \mathbf{A} &= d(t)\mathbf{A_1} + d'(t)\mathbf{A_2} \\ \mathbf{B} &= d(t)\mathbf{B_1} + d'(t)\mathbf{B_2} \\ \mathbf{C} &= d(t)\mathbf{C_1} + d'(t)\mathbf{C_2} \end{aligned} \tag{3.7}$$

$$\mathbf{A} = d(t)\begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & -\frac{1}{R} \end{bmatrix} + d'(t)\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & 0 \\ 1 & 0 & -\frac{1}{R} \end{bmatrix} = \begin{bmatrix} 0 & d(t) & -d'(t) \\ -d(t) & 0 & 0 \\ d'(t) & 0 & -\frac{1}{R} \end{bmatrix} \tag{3.8}$$

$$\mathbf{B} = d(t)\begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} + d'(t)\begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} \tag{3.9}$$

$$\mathbf{C} = d(t)\begin{bmatrix} 0 & 1 & 1 \end{bmatrix} + d'(t)\begin{bmatrix} 0 & 1 & 1 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \tag{3.10}$$

The averaged model is represented as follows

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & d(t) & -d'(t) \\ -d(t) & 0 & 0 \\ d'(t) & 0 & -\frac{1}{R} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix}[i_3] \\ [v_3(t)] = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} \end{cases} \tag{3.11}$$

If the system is in steady-state the derivative becomes null and a solution can be found for this equilibrium condition. The variables are considered constant in steady-state and are represented with capital letters for clarification.

$$\begin{cases} \mathbf{0} = \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} = \mathbf{CX} \end{cases} \tag{3.12}$$

Then (3.11) becomes

$$\begin{cases} [0] = \begin{bmatrix} 0 & D & -D' \\ -D & 0 & 0 \\ D' & 0 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} I_L \\ V_{C1} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} [I_3] \\ [V_3] = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_{C1} \\ V_{C2} \end{bmatrix} \end{cases} \tag{3.13}$$

Solving $\mathbf{X}$ and $\mathbf{Y}$ for(3.12) gives

$$\begin{cases} \mathbf{X} = -\mathbf{A^{-1}BU} \\ \mathbf{Y} = -\mathbf{CA^{-1}BU} \end{cases} \tag{3.14}$$

Then (3.13) becomes

$$\begin{cases} \mathbf{X} = \begin{bmatrix} I_L \\ V_{C1} \\ V_{C2} \end{bmatrix} = - \begin{bmatrix} 0 & \frac{1}{D} & 0 \\ -\frac{1}{D} & R\frac{D'^2}{D^2} & R\frac{D'}{D} \\ 0 & R\frac{D'}{D} & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} [I_3] \\ \begin{bmatrix} I_L \\ V_{C1} \\ V_{C2} \end{bmatrix} = \begin{bmatrix} \frac{I_3}{D} \\ I_3 R\frac{D'^2}{D^2} + I_3 R\frac{D'}{D} \\ I_3 R\frac{D'}{D} + I_3 R \end{bmatrix} \\ \mathbf{Y} = [V_3] = - \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} 0 & \frac{1}{D} & 0 \\ -\frac{1}{D} & R\frac{D'^2}{D^2} & R\frac{D'}{D} \\ 0 & R\frac{D'}{D} & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} [I_3] \\ [V_3] = \begin{bmatrix} I_3 R\frac{D'^2}{D^2} + I_3 R\frac{D'}{D} + I_3 R\frac{D'}{D} + I_3 R \end{bmatrix} \end{cases} \tag{3.15}$$

Solving (3.15) and expressing in algebraic form

$$\begin{cases} I_L = \frac{I_3}{D} \\ V_{C1} = I_3 R\frac{D'}{D^2} = V_3 D' \\ V_{C2} = I_3 R\frac{1}{D} = V_3 D \\ V_3 = I_3 R\frac{1}{D^2} \end{cases} \tag{3.16}$$

The results from (3.16) give the steady-state operation parameters of the configuration, as well as, its voltage conversion ratio.

The next step for achieving the AC small-signal model is to perturb the system by adding a small perturbation to the independent variables. These can be then defined as a constant value plus a small time-dependent variation

$$\begin{aligned} d(t) &= D + \hat{d}(t) \\ v_3(t) &= V_3 + \hat{v}_3(t) \end{aligned} \tag{3.17}$$

Then, the dependent variables will be affected as

$$\begin{aligned} i_L(t) &= I_L + \hat{i}_L(t) \\ v_{C1}(t) &= V_{C1} + \hat{v}_{C1}(t) \\ v_{C2}(t) &= V_{C2} + \hat{v}_{C2}(t) \\ i_3(t) &= I_3 + \hat{i}_3(t) \end{aligned} \tag{3.18}$$

Including (3.17) and (3.18) into (3.6) and solving, it produces 3 kind of terms, DC terms, linear AC terms and nonlinear terms. The derivative of DC terms becomes 0, the perturbation signal is small thus, the nonlinear terms, that include multiplication of more than one of the small variable components, can be neglected. Afterward the general form of the small-signal state-space equation is

$$\begin{cases} K\dfrac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \{(A_1 - A_2)\mathbf{X} + (B_1 - B_2)\mathbf{U}\}\hat{d}(t) \\ \hat{\mathbf{y}}(t) = \mathbf{C}\hat{\mathbf{x}}(t) + (C_1 - C_2)\mathbf{X}\hat{d}(t) \end{cases} \tag{3.19}$$

For the step-down configuration (3.19) has the following particular solution

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \end{bmatrix} = \begin{bmatrix} D\hat{v}_{C1}(t) - D'\hat{v}_{C2}(t) \\ -D\hat{i}_L(t) \\ D'\hat{i}_L(t) - \frac{\hat{v}_{C2}(t)}{R} \end{bmatrix} + \begin{bmatrix} 0 \\ \hat{i}_3(t) \\ \hat{i}_3(t) \end{bmatrix} + \begin{bmatrix} V_3 \\ -I_L \\ -I_L \end{bmatrix} \hat{d}(t) \\ [\hat{v}_3(t)] = \begin{bmatrix} \hat{v}_{C1}(t) + \hat{v}_{C2}(t) \end{bmatrix} \end{cases} \tag{3.20}$$

In algebraic form

$$\begin{cases} \hat{v}_L(t) = L\frac{d\hat{i}_L(t)}{dt} = D\hat{v}_{C1}(t) - D'\hat{v}_{C2}(t) + V_3\hat{d}(t) \\ \hat{i}_{C1}(t) = C_1\frac{d\hat{v}_{C1}(t)}{dt} = \hat{i}_3(t) - D\hat{i}_L(t) - I_L\hat{d}(t) \\ \hat{i}_{C2}(t) = C_2\frac{d\hat{v}_{C2}(t)}{dt} = \hat{i}_3(t) + D'\hat{i}_L(t) - I_L\hat{d}(t) - \frac{\hat{v}_{C2}(t)}{R} \\ \hat{v}_3(t) = \hat{v}_{C1}(t) + \hat{v}_{C2}(t) \end{cases} \tag{3.21}$$

Solving further (3.21) the following equation can be obtained

$$\begin{cases} \hat{v}_L(t) = D\hat{v}_3(t) - \hat{v}_{C2}(t) + V_3\hat{d}(t) \\ \hat{i}_L(t) = \hat{i}_{C2}(t) - \hat{i}_{C1}(t) + \frac{\hat{v}_{C2}(t)}{R} \end{cases} \tag{3.22}$$

Arranging (3.22) for control-to-output transfer function calculation

$$\begin{cases} \hat{v}_L(t) = D\hat{v}_3(t) - \hat{v}_{C2}(t) + V_3\hat{d}(t) \\ \hat{i}_L(t) = (C_1 + C_2)\frac{d\hat{v}_{C2}(t)}{dt} - C_1\frac{d\hat{v}_3(t)}{dt} + \frac{\hat{v}_{C2}(t)}{R} \end{cases} \tag{3.23}$$

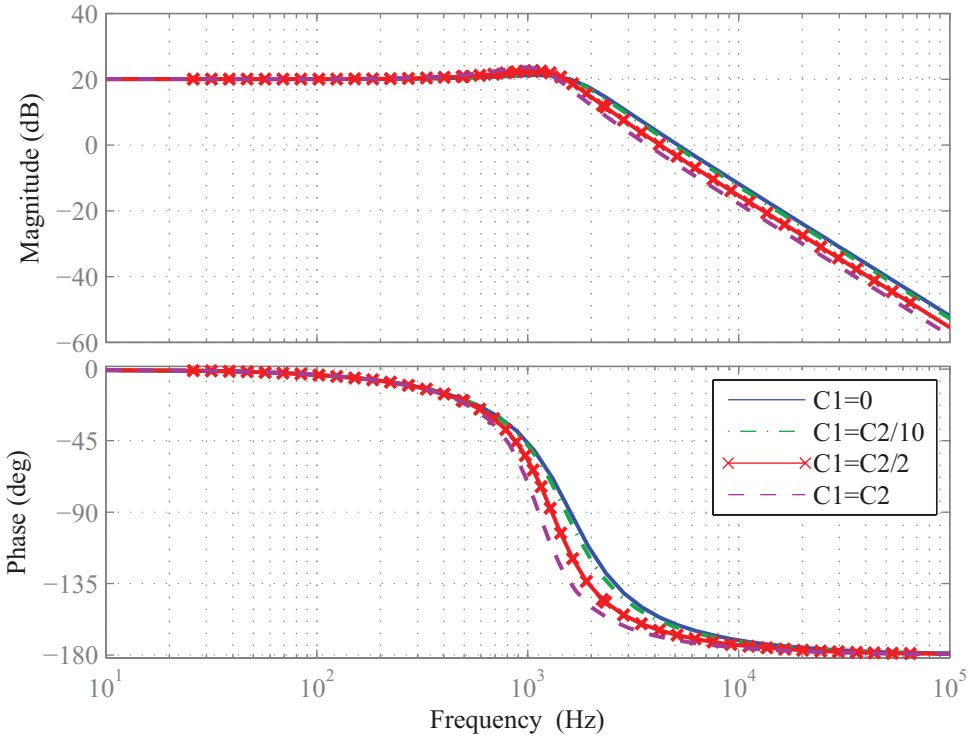
To obtain the control-to-output transfer function it is needed to set $\hat{v}_3 = 0$, this makes $\frac{d\hat{v}_3(t)}{dt} = 0$ as well. Hence, the result is

$$G_{vd}(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{d}(s)}\right|_{\hat{v}_3(s)=0} = V_3\frac{1}{1 + \frac{Ls}{R} + (C_1 + C_2)\,Ls^2} \tag{3.24}$$

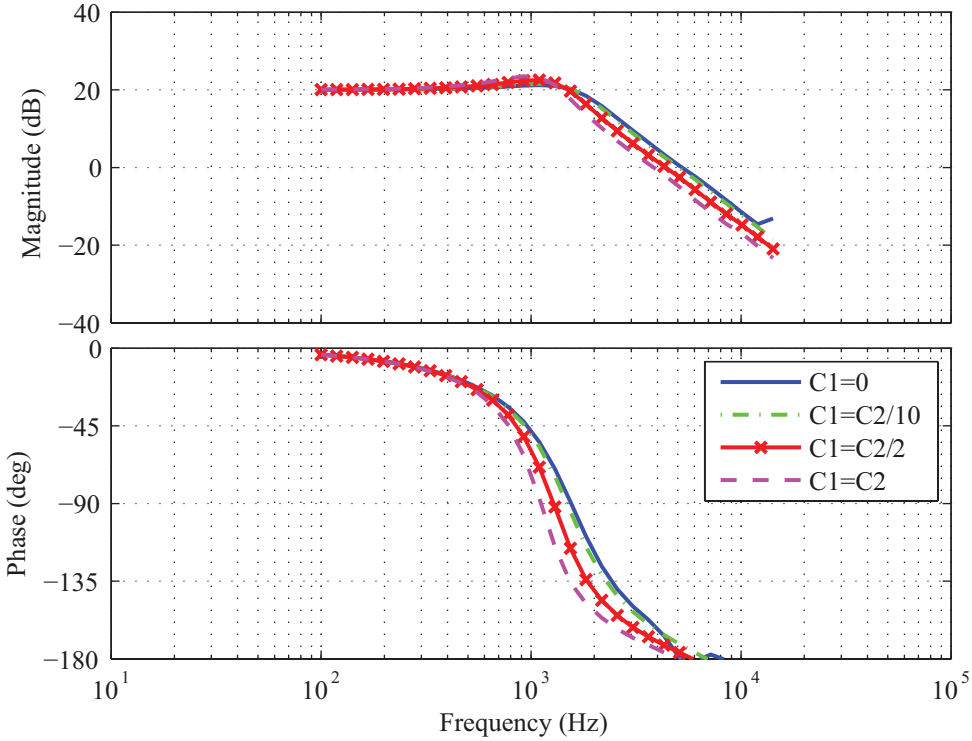
From (3.24) it can be seen that it is a 2^{nd} order system with 2 fixed poles. In addition, the capacitance C_1 adds to C_2, resulting in a larger combined total output capacitance. This characteristic can be exploited to modify the dynamic response of the system without modifying the output stage of the converter. The only variable that affects the transfer function is the input voltage, the function is independent of the steady-state operating point of the converter. The control-to-output transfer function depicts the behaviour of the output voltage $\hat{v}_{C2}$ when perturbations in the control input $\hat{d}$ occur. This transfer function is of crucial importance in the characterization of the system performance and, in the development of control strategies [22]. The function obtained in (3.24) is then compared with a computer-based simulation of the converter. Frequency and step responses of both, the transfer function and the circuit are shown in Figure 3.2 and Figure 3.3. The parameters considered for the numeric example are detailed in Table 3.1. Several curves are obtained for different values of C_1. In addition, the chosen switching frequency F_{SW} is kept high enough to avoid possible interference with the cutoff frequency of the linear system. This is one fundamental assumption of small-signal modelling.

Table 3.1: Step-down configuration parameters

$F_{SW} = 100KHz$	$R = 1\Omega$
$V_3 = 10V$	$L = 100\mu H$
$D = 0.75$	$C_2 = 100\mu F$
$\hat{d} = D/50$	

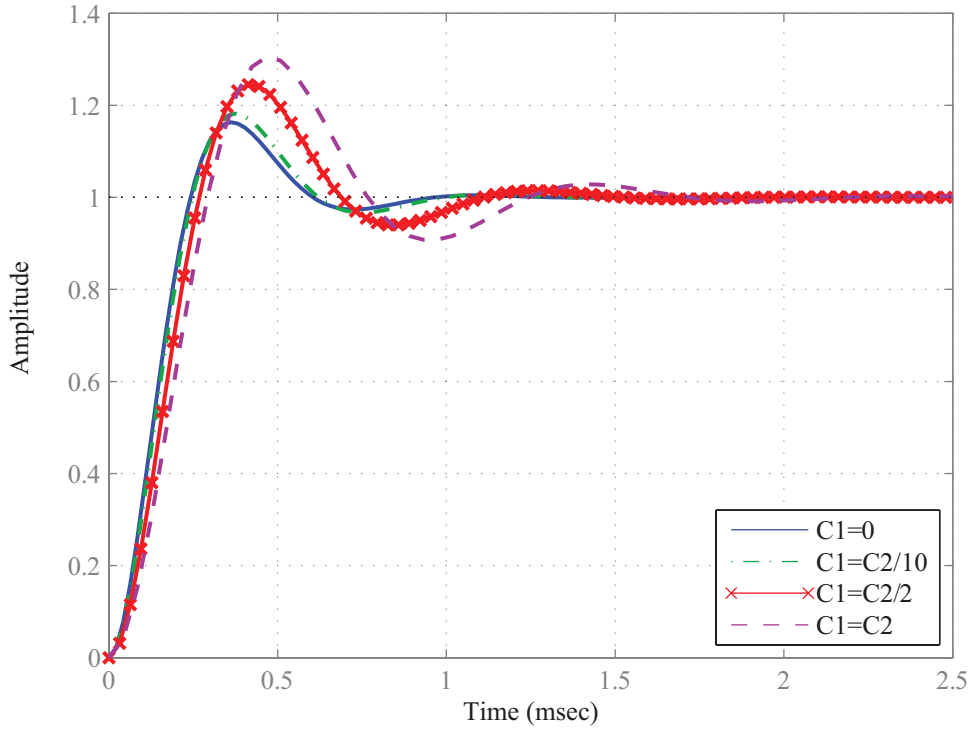


(a) Transfer function frequency response.

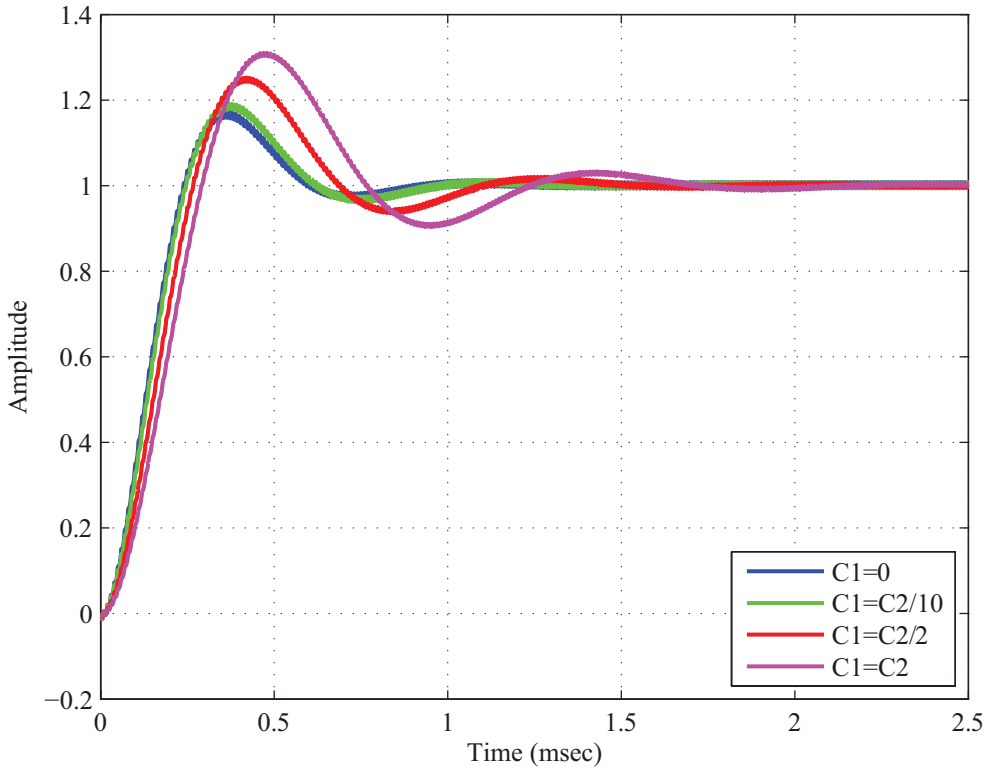


(b) Simulated circuit open-loop frequency response.

Figure 3.2: Frequency responses for step-down configuration with negative reference.



(a) Transfer function step response.



(b) Simulated circuit open-loop step response.

Figure 3.3: Step responses for step-down configuration with negative reference.

As it can be seen from Figure 3.2 and Figure 3.3, the frequency responses are similar between the transfer function and the circuit simulation for each value of C_1. The same can be observed with the step responses. A particular case is depicted, when $C_1 = 0$ the Topology Zero becomes a buck converter. The buck converter operation is well known and implies that C_1 does not exist. Nevertheless, the general transfer function of the Topology Zero remains valid by plugging in $C_1 = 0$.

The inclusion of the capacitance C_1 affects the cutoff frequency of the system according to

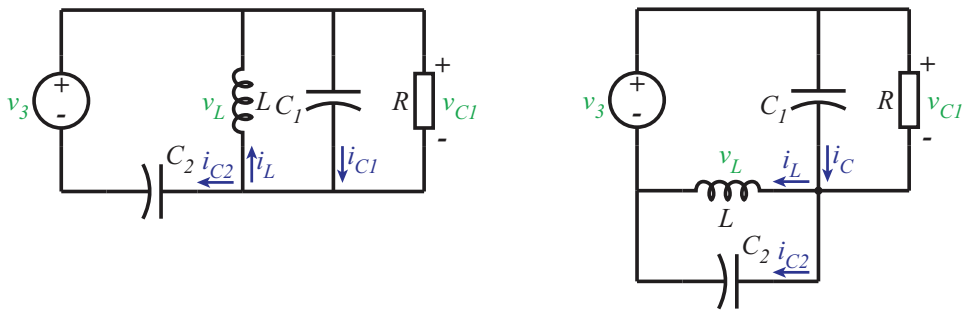
$$f_0 = \frac{1}{2\pi\sqrt{L\,(C_1 + C_2)}} \tag{3.25}$$

The effects of the frequency displacement can be observed in both the frequency and step responses. In the frequency response the phase shows a more appreciable change in its shape. When $C_1 = C_2$ the total capacitance doubles the case when $C_1 = 0$, and the cutoff frequency shifts to the right. In the step response there are changes in the oscillation frequency, the overshoot amplitude and the settling time. When the capacitance increases, the oscillation frequency decreases, and the settling time and overshoot amplitude increase.

3.1.2 Step-down Configuration with Positive Reference

Next, the results of the small-signal analysis of the step-down configuration with positive reference are shown.

The step-down configuration shown in Figure 2.5, presents two equivalent circuits for each position of the switch, displayed in Figure 3.4



(a) Switch in position 1 during $d(t)\,T_{SW}$. (b) Switch in position 0 during $d'(t)\,T_{SW}$.

Figure 3.4: Step-down configuration equivalent circuits.

During the time that the switch is in position 1 ($d(t)\,T_{SW}$), the equations for Figure 3.4a

are

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = -v_{C1}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_3(t) + i_L(t) - \frac{v_{C1}(t)}{R} \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_3(t) \\ v_3(t) = v_{C1}(t) + v_{C2}(t) \end{cases} \tag{3.26}$$

When the switch is in 0, during $d(t)'T_{SW}$, the equations for Figure 3.4b

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = v_{C2}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_3(t) - \frac{v_{C1}(t)}{R} \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_3(t) - i_L(t) \\ v_3(t) = v_{C1}(t) + v_{C2}(t) \end{cases} \tag{3.27}$$

The averaged model results in

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & -d(t) & d'(t) \\ d(t) & -\frac{1}{R} & 0 \\ -d'(t) & 0 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} [i_3] \\ [v_3(t)] = \begin{bmatrix} 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} \end{cases} \tag{3.28}$$

The equations that define the circuit in steady-state are

$$\begin{cases} I_L = \frac{I_3}{D'} \\ V_{C1} = I_3 R\frac{1}{D'} = V_3 D' \\ V_{C2} = I_3 R\frac{D}{D'^2} = V_3 D \\ V_3 = I_3 R\frac{1}{D'^2} \end{cases} \tag{3.29}$$

The small-signal model has the following expression

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \end{bmatrix} = \begin{bmatrix} -D\hat{v}_{C1}(t) + D'\hat{v}_{C2}(t) \\ D\hat{i}_L(t) - \frac{\hat{v}_{C1}(t)}{R} \\ -D'\hat{i}_L(t) \end{bmatrix} + \begin{bmatrix} 0 \\ \hat{i}_3(t) \\ \hat{i}_3(t) \end{bmatrix} + \begin{bmatrix} -V_3 \\ I_L \\ I_L \end{bmatrix} \hat{d}(t) \\ [\hat{v}_3(t)] = \begin{bmatrix} \hat{v}_{C1}(t) + \hat{v}_{C2}(t) \end{bmatrix} \end{cases} \tag{3.30}$$

Solving (3.30)

$$\begin{cases} \hat{v}_L(t) = D'\hat{v}_3(t) - \hat{v}_{C1}(t) - V_3\hat{d}(t) \\ \hat{i}_L(t) = \hat{i}_{C1}(t) - \hat{i}_{C2}(t) + \frac{\hat{v}_{C1}(t)}{R} \end{cases} \tag{3.31}$$

Arranging (3.31) for control-to-output transfer function calculation

$$\begin{cases} \hat{v}_L(t) = D'\hat{v}_3(t) - \hat{v}_{C1}(t) + V_3\hat{d}(t) \\ \hat{i}_L(t) = (C_1 + C_2)\frac{d\hat{v}_{C1}(t)}{dt} - C_2\frac{d\hat{v}_3(t)}{dt} + \frac{\hat{v}_{C1}(t)}{R} \end{cases} \tag{3.32}$$

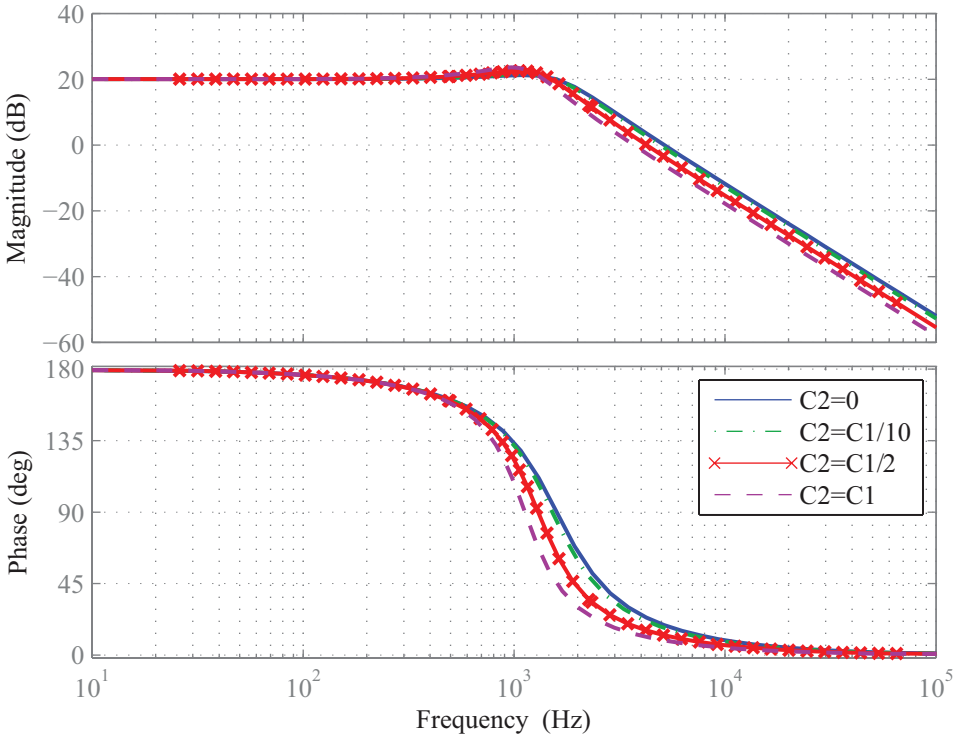
To obtain the control-to-output transfer function it is needed to set $\hat{v}_3 = 0$. The result is

$$G_{vd}(s) = \left.\frac{\hat{v}_{C1}(s)}{\hat{d}(s)}\right|_{\hat{v}_3(s)=0} = -V_3\frac{1}{1 + \frac{Ls}{R} + (C_1 + C_2)\,Ls^2} \tag{3.33}$$

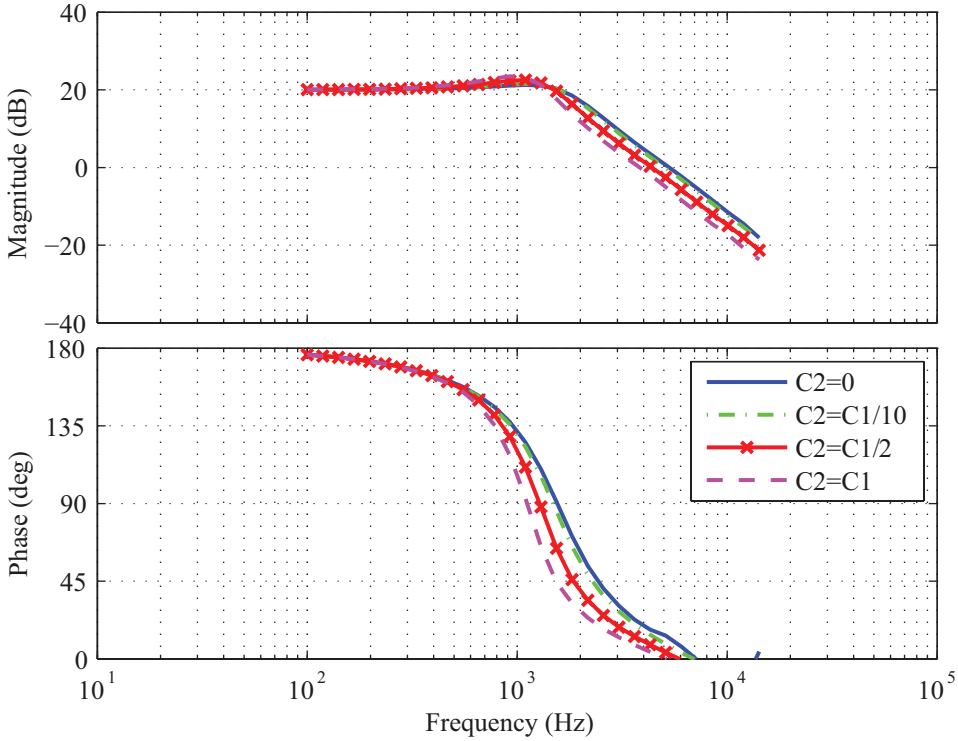
The function obtained in (3.33) is compared with a computer-based simulation of the converter. Frequency and step responses of both, the transfer function and the circuit are shown in Figure 3.5 and Figure 3.6. The parameters considered for calculation are detailed in Table 3.2. Several curves are obtained for different values of C_2.

Table 3.2: Step-down configuration parameters

F_{SW} = 100KHz	R = 1Ω
V_3 = 10V	L = 100μH
D = 0.75	C_1 = 100μF
$\hat{d}$ = D/50	

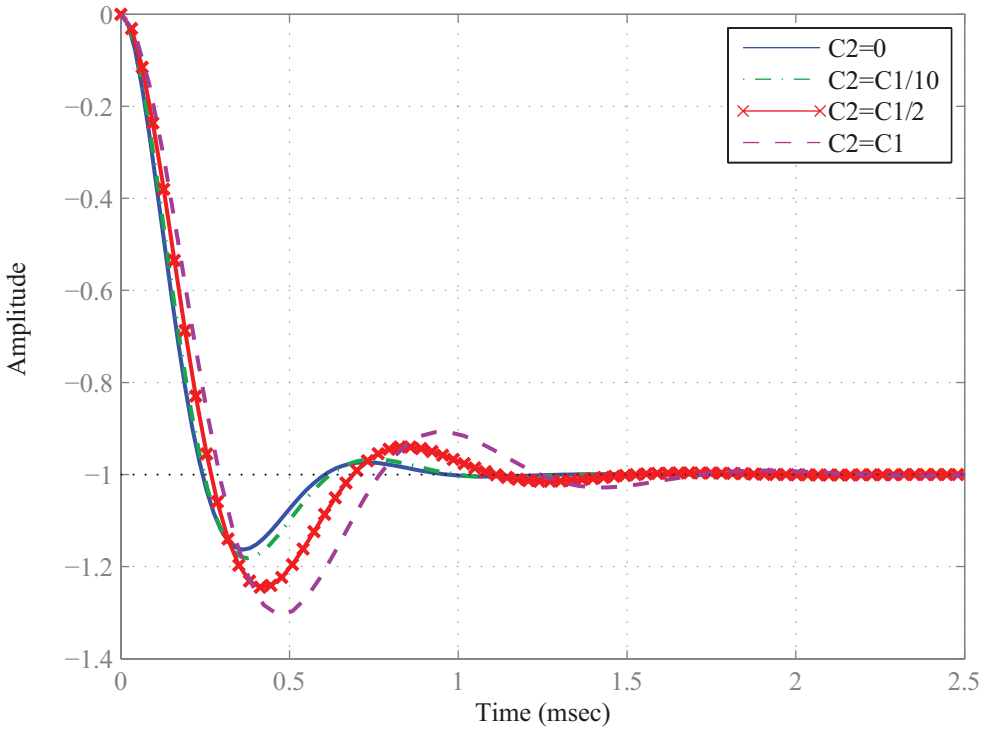


(a) Transfer function frequency response.

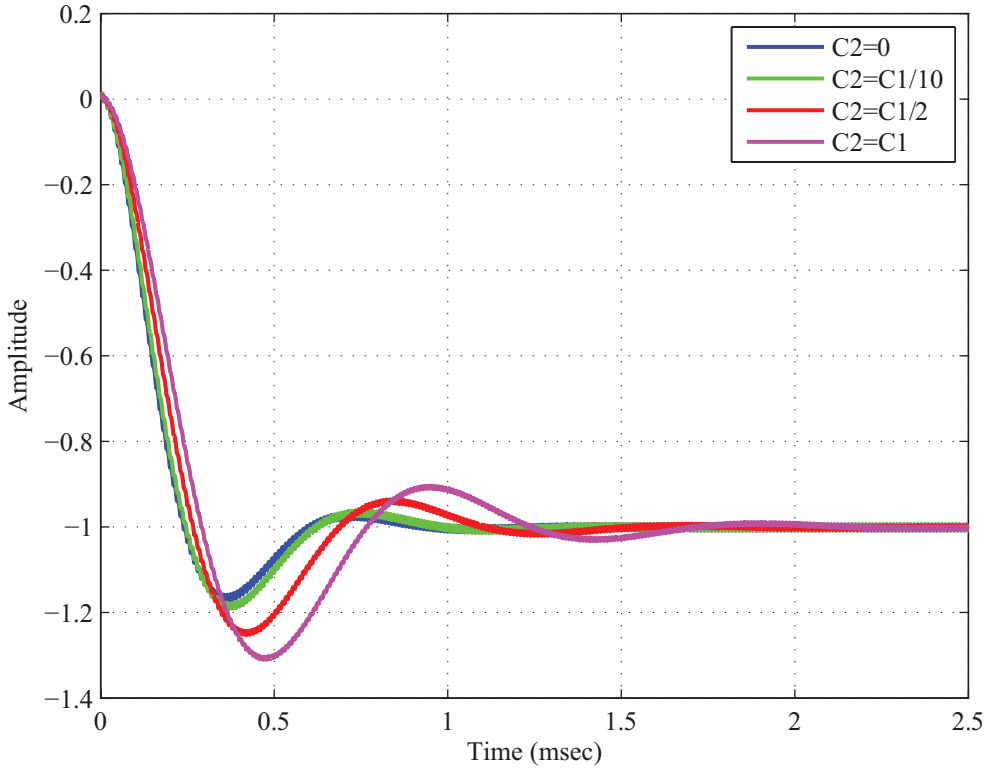


(b) Simulated circuit open-loop frequency response.

Figure 3.5: Frequency responses for step-down configuration with positive reference.



(a) Transfer function step response.



(b) Simulated circuit open-loop step response.

Figure 3.6: Step responses for step-down configuration with negative reference.

The transfer function for the step-down configuration with positive reference have opposite response to the one with negative reference, this is shown in the phase graphics and in the step response. Besides the sign, (3.24) and (3.33) are equal.

The inclusion of the capacitance C_2 affects the cutoff frequency of the system according to

$$f_0 = \frac{1}{2\pi\sqrt{L\,(C_1 + C_2)}} \tag{3.34}$$

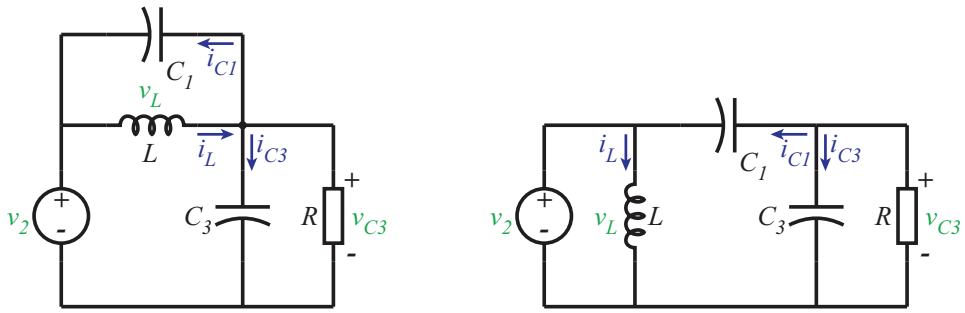
That is equal to (3.25). The effects of the frequency displacement can be observed in both the frequency and step responses. The cutoff frequency displaces to the right when the total capacitance increases, as it is observed in Figure 3.5. As well, when the capacitance increases, the oscillation frequency decreases, and the settling time and overshoot amplitude increase, as shown in Figure 3.6.

3.2 Topology Zero Step-up Configurations

Following, the results for the step-up configuration with negative and positive reference are shown.

3.2.1 Step-up Configuration with Negative Reference

Consider the step-up configuration with negative reference shown in Figure 2.7, the equivalent circuits for each position of the switch are shown in Figure 3.7.



(a) Switch in position 1 during $d(t)\,T_{SW}$. (b) Switch in position 0 during $d'(t)\,T_{SW}$.

Figure 3.7: Step-up configuration equivalent circuits.

A set of equations can be obtained from the circuit in Figure 3.7a. This circuit represents

the converter when the switch is in position 1 during $d(t)\,T_{SW}$

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = -v_{C1}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_L(t) - i_2(t) \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_2(t) - \frac{v_{C3}(t)}{R} \\ v_2(t) = v_{C3}(t) - v_{C1}(t) \end{cases} \tag{3.35}$$

When the switch is in position 0 during $d(t)'\,T_{SW}$, as shown in Figure 3.7b, the equations that represent the circuit are

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = v_{C3}(t) - v_{C1}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_L(t) - i_2(t) \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_2(t) - i_L(t) - \frac{v_{C3}(t)}{R} \\ v_2(t) = v_{C3}(t) - v_{C1}(t) \end{cases} \tag{3.36}$$

The averaged model results in

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C3}(t) \end{bmatrix} = \begin{bmatrix} 0 & -1 & d'(t) \\ 1 & 0 & 0 \\ -d'(t) & 0 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C3}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \\ 1 \end{bmatrix} [i_2] \\ [v_2(t)] = \begin{bmatrix} 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C3}(t) \end{bmatrix} \end{cases} \tag{3.37}$$

The equations that define the circuit in steady-state are

$$\begin{cases} I_L = I_2 \\ V_{C1} = I_2 RD'D = V_2\frac{D'}{D} \\ V_{C3} = I_2 RD = V_2\frac{1}{D} \\ V_2 = I_2 RD^2 \end{cases} \tag{3.38}$$

The small-signal model has the following expression

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C3}(t) \end{bmatrix} = \begin{bmatrix} -\hat{v}_{C1}(t) + D'\hat{v}_{C3}(t) \\ \hat{i}_L(t) \\ -D'\hat{i}_L(t) - \frac{\hat{v}_{C3}(t)}{R} \end{bmatrix} + \begin{bmatrix} 0 \\ -\hat{i}_2(t) \\ \hat{i}_2(t) \end{bmatrix} + \begin{bmatrix} -V_{C3} \\ 0 \\ I_L \end{bmatrix} \hat{d}(t) \\ [\hat{v}_2(t)] = \left[\hat{v}_{C3}(t) - \hat{v}_{C1}(t)\right] \end{cases} \tag{3.39}$$

Solving (3.39)

$$\begin{cases} \hat{v}_L(t) = \hat{v}_2(t) - D\hat{v}_{C3}(t) - V_3\hat{d}(t) \\ D\hat{i}_L(t) = \hat{i}_{C3}(t) + \hat{i}_{C1}(t) + \frac{\hat{v}_{C3}(t)}{R} - I_L\hat{d}(t) \end{cases} \tag{3.40}$$

Arranging (3.40) for control-to-output transfer function calculation

$$\begin{cases} \hat{v}_L(t) = \hat{v}_2(t) - D\hat{v}_{C3}(t) - V_3\hat{d}(t) \\ D\hat{i}_L(t) = (C_1 + C_3)\frac{d\hat{v}_{C3}(t)}{dt} - C_1\frac{d\hat{v}_2(t)}{dt} + \frac{\hat{v}_{C3}(t)}{R} - I_L\hat{d}(t) \end{cases} \tag{3.41}$$

To obtain the control-to-output transfer function it is needed to set $\hat{v}_2 = 0$. Hence, the result is

$$G_{vd}(s) = \left.\frac{\hat{v}_{C3}(s)}{\hat{d}(s)}\right|_{\hat{v}_2(s)=0} = -\frac{V_{C3}}{D}\frac{1 - \frac{Ls}{D^2R}}{1 + \frac{Ls}{D^2R} + \frac{(C_1+C_3)Ls^2}{D^2}} \tag{3.42}$$

From (3.42) it can be seen that the system has 2 poles and 1 zero whose positions depend on the steady-state of the converter. In addition, the capacitance C_1 adds to C_3. Also, the negative sign in the control-to-output transfer function means that an increase in the duty cycle produce a decreasing in the output voltage, which is expected.

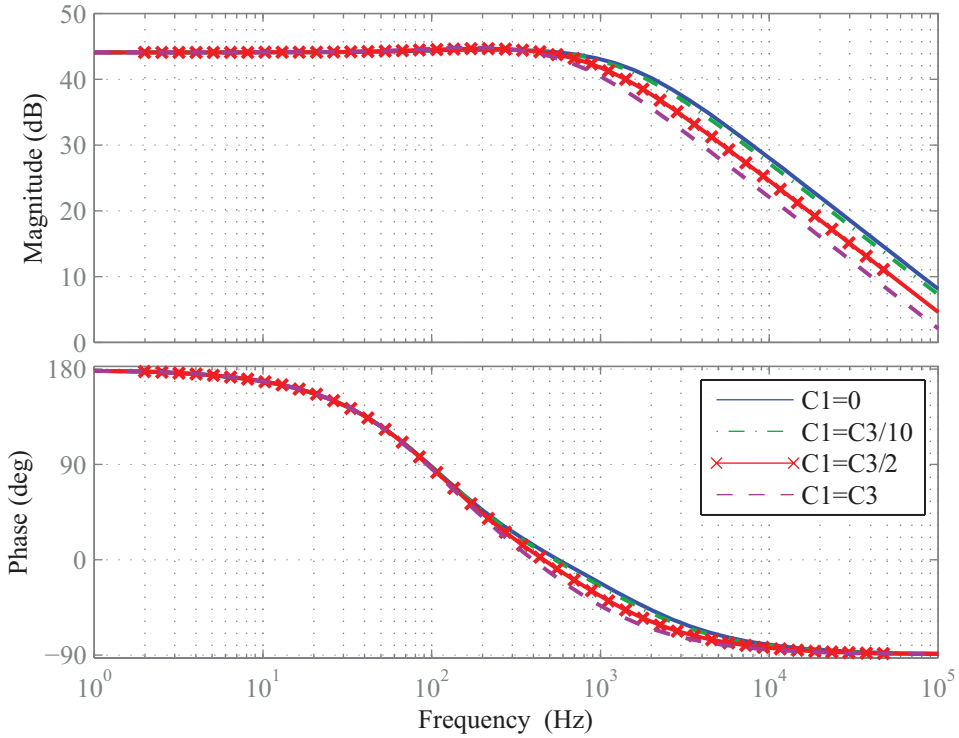
The zero of the step-up control-to-output transfer function lies in the right-half of the complex s-plane. The right-half plane zero (RHZ) or nonminimum phase zero produces phase inversion at high frequency. The magnitude response of a RHZ is similar to a left-half plane zero, however its phase response is similar to a left-half plane pole. The output tends to go in the opposite direction at high frequencies compared to the direction at low frequencies. In a step response, the output goes, initially, in the opposite direction of the final value. The RHZ have the tendency to create instability in wide-band feedback control loop, due to the opposite direction that the output voltage follows initially during transients [22].

The function obtained in (3.42) is then compared with a computer-based simulation of the converter. Frequency and step responses of both, the transfer function and the circuit

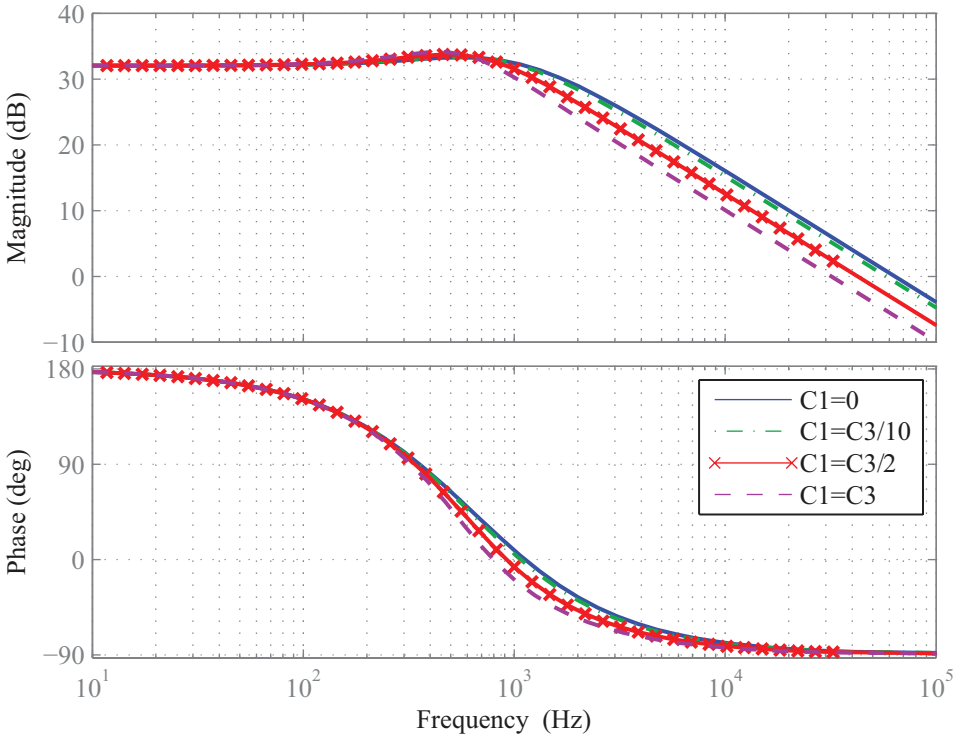
are shown in Figure 3.8 and Figure 3.9. The parameters considered for calculation are detailed in Table 3.3. Several curves are obtained for different values of C_1 and D.

Table 3.3: Step-up configuration parameters

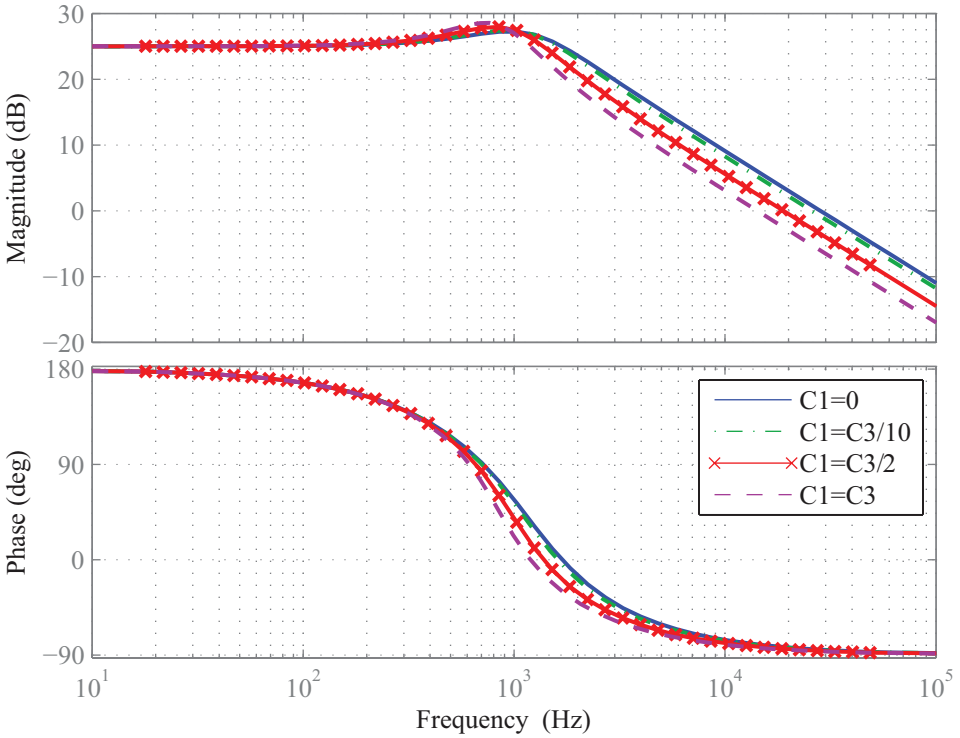
$F_{SW} = 100KHz$	$R = 1\Omega$
$V_2 = 10V$	$L = 100\mu H$
$\hat{d} = D/50$	$C_3 = 100\mu F$



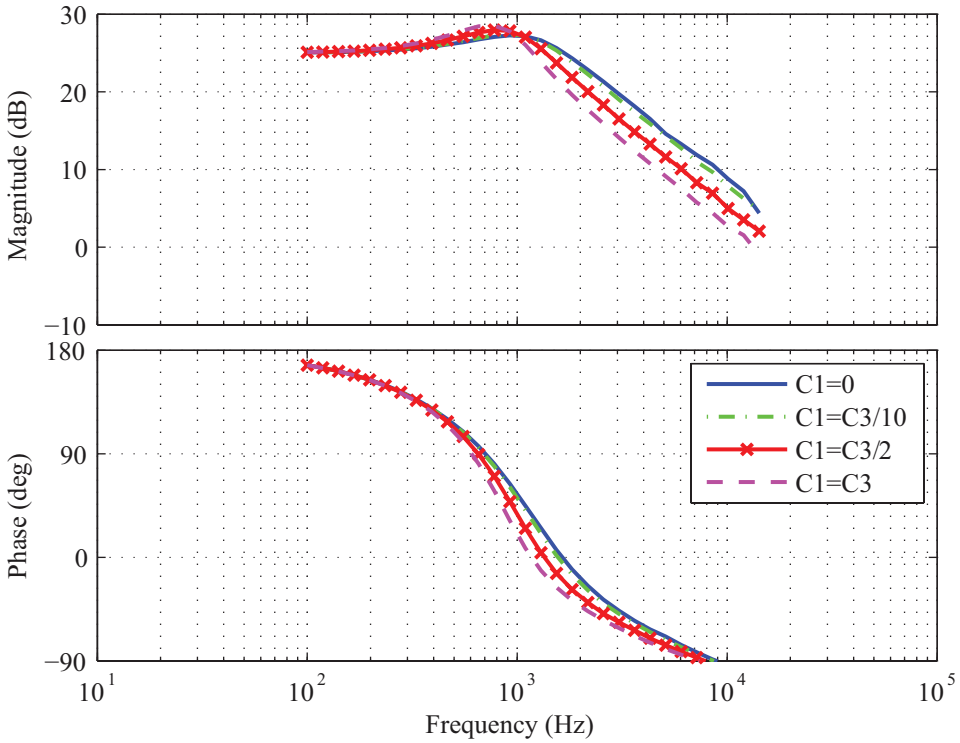
(a) Transfer function frequency response, $D = 0.25$.



(b) Transfer function frequency response, $D = 0.5$.

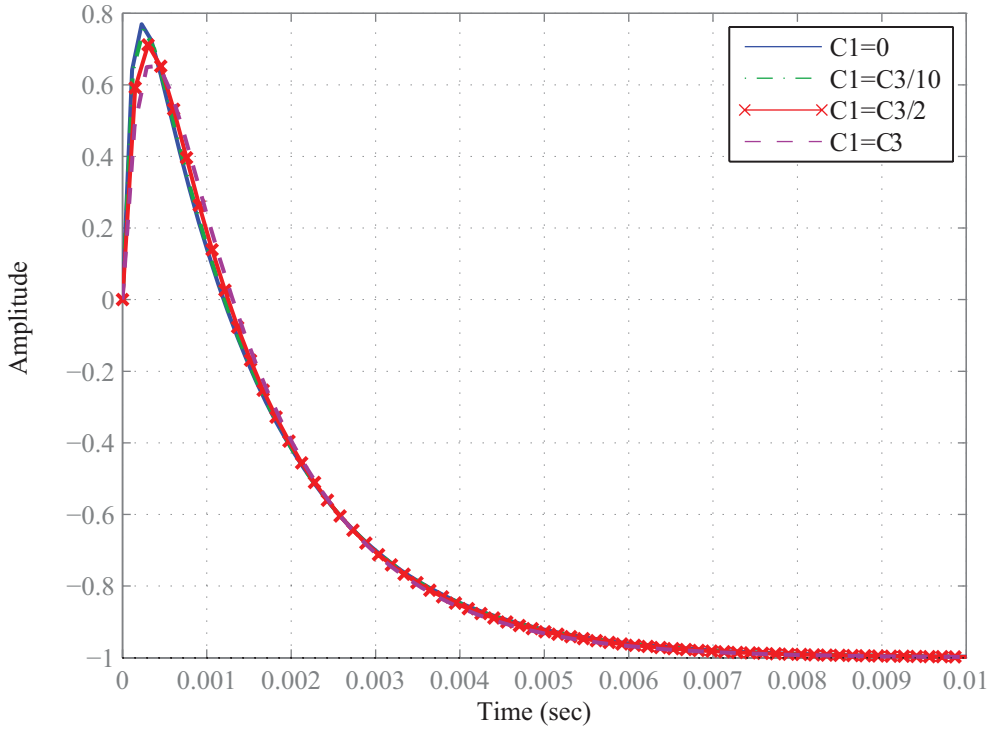


(c) Transfer function frequency response, $D = 0.75$.

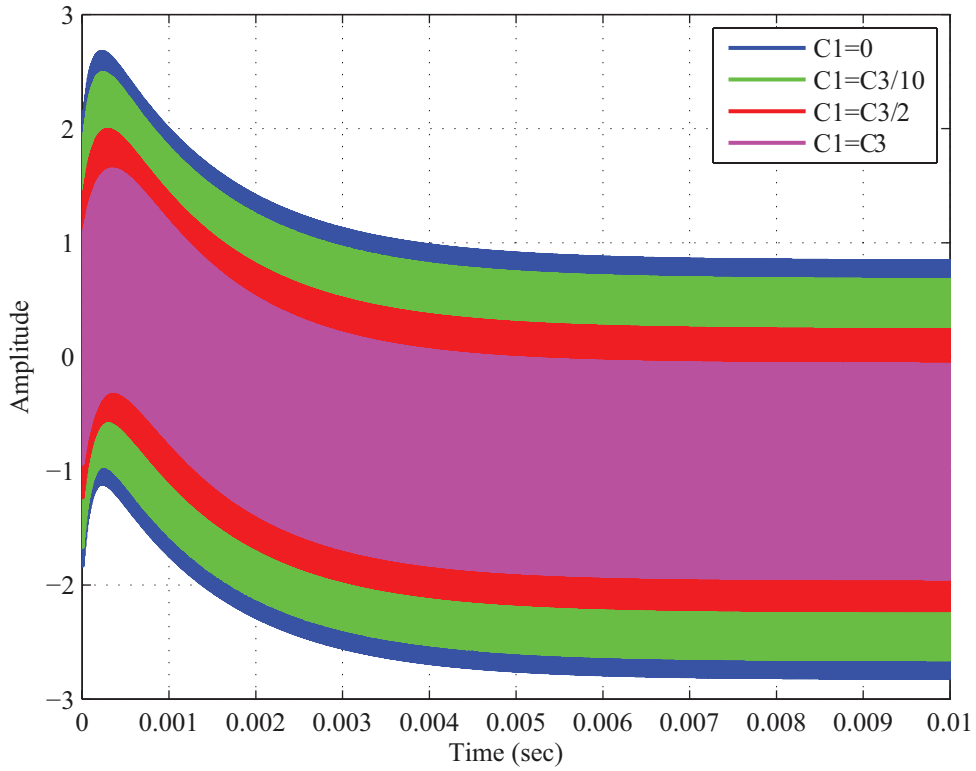


(d) Simulated circuit open-loop frequency response, $D = 0.75$.

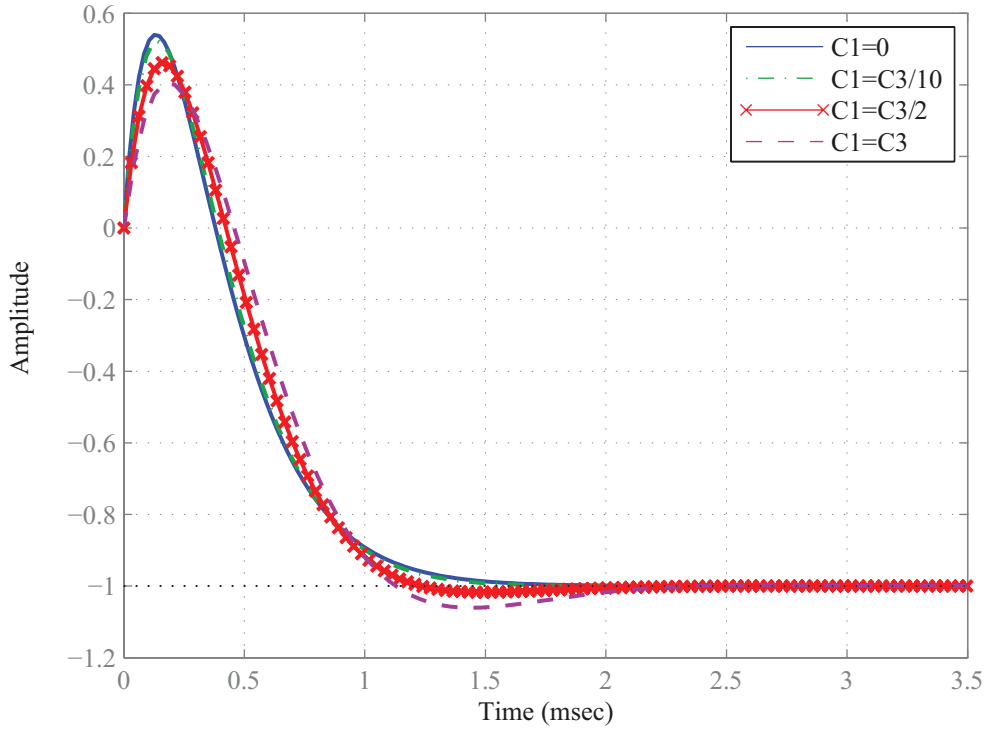
Figure 3.8: Frequency responses for step-up configuration with negative reference.



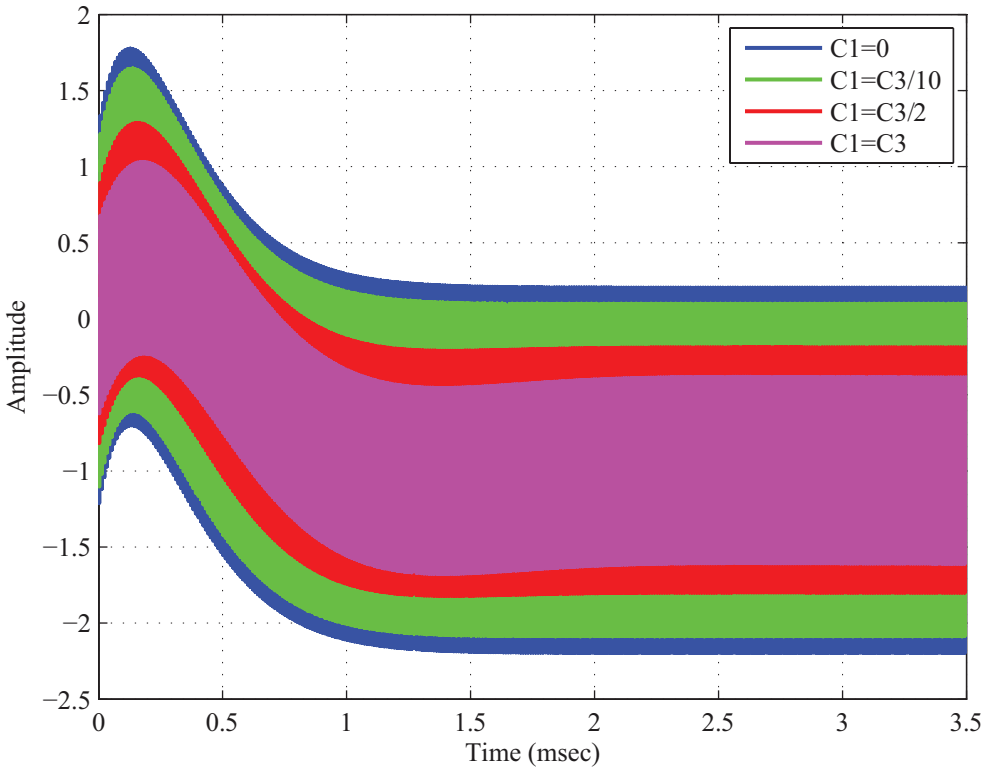
(a) Transfer function step response, $D = 0.25$.



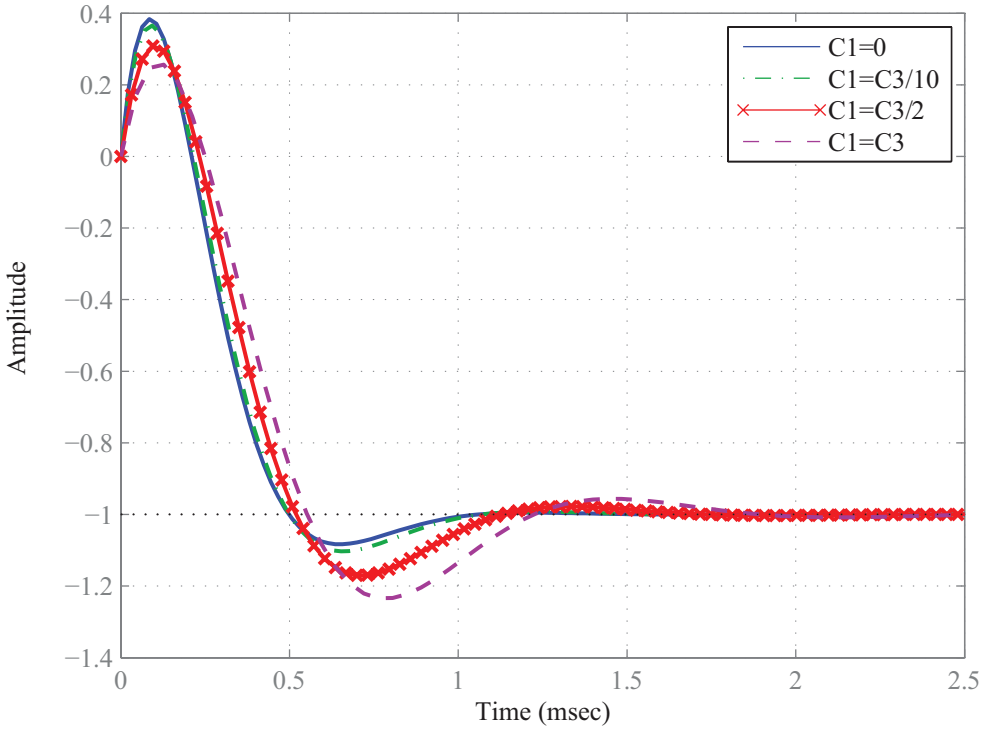
(b) Simulated circuit open-loop step response, $D = 0.25$.



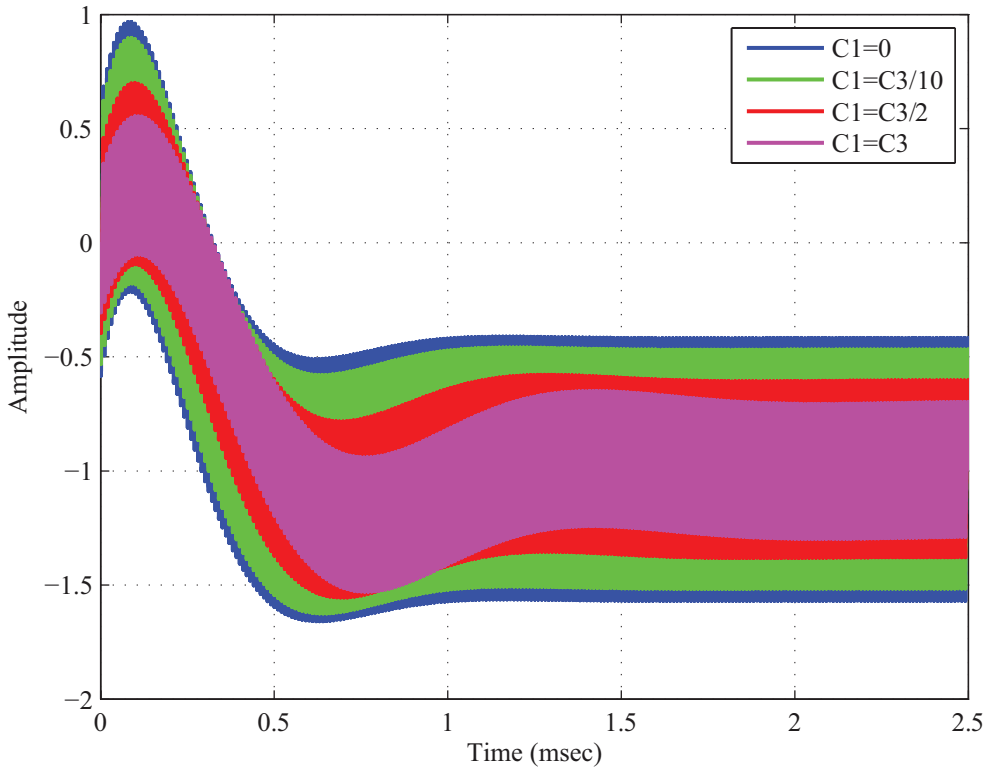
(c) Transfer function step response, $D = 0.5$.



(d) Simulated circuit open-loop step response, $D = 0.5$.



(e) Transfer function step response, $D = 0.75$.



(f) Simulated circuit open-loop step response, $D = 0.75$.

Figure 3.9: Step responses for step-up configuration with negative reference.

The comparison of the transfer function and the simulation exposes their similarities in the behaviour. This validates the small-signal analysis and its results to model the Topology Zero. When $C_1 = 0$ the Topology Zero becomes a boost converter. In other words, the boost converter is a particular case. The responses for this particular configuration are shown in the previous curves. The boost topology implies that C_1 does not exist. However, the transfer function of the Topology Zero (3.42) remains valid by plugging in $C_1 = 0$. The inclusion of the capacitance C_1 affects the cutoff frequency of the system according to

$$f_0 = \frac{D}{2\pi\sqrt{L\left(C_1 + C_3\right)}} \tag{3.43}$$

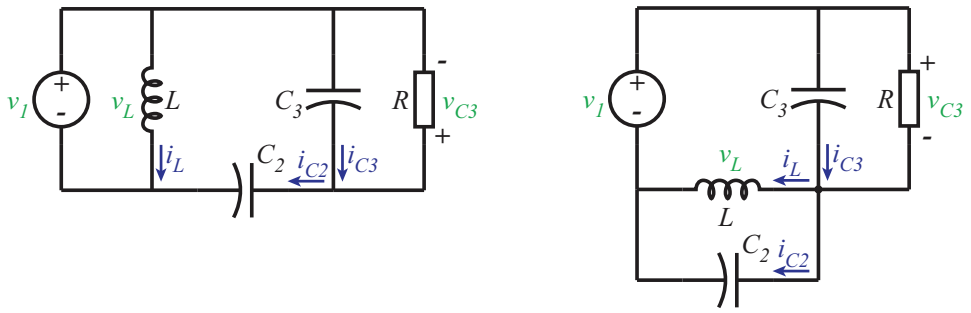
The effects of the frequency displacement can be observed in both the frequency and step responses. When $C_1 = C_3$ the total capacitance doubles the case when $C_1 = 0$, and the cutoff frequency shifts to the right. Additionally, the frequency response is affected by the RHZ and the duty cycle in steady-state. The frequency of the RHZ is given by

$$f_z = \frac{D^2 R}{2\pi L} \tag{3.44}$$

Unlike the poles, the position of this root is only dependent on the steady-state of the system. The relative positions of the zero and poles define the shape of the frequency response for different values of D. In the magnitude response (Figure 3.8), for lower values of duty cycle there is not peak in the gain near the cutoff frequency, whereas at high duty cycle, the peak in magnitude can be observed. The step response of the system, shown in Figure 3.9, is influenced by the relative position of the zero and the poles, and by the steady-state condition. At low duty cycle the response is overdamped, and when D increases the system becomes underdamped. The changes in the undershoot and overshoot amplitudes and times can be appreciated, as well. A secondary effect that can be observed in the step response of the circuit simulation in Figure 3.9 is the output ripple variations according to the duty cycle and the capacitance changes. The bigger the duty cycle the lower the ripple voltage. Additionally, the inclusion of C_1 helps to improve the output ripple of the converter.

3.2.2 Step-up Configuration with Positive Reference

Consider the step-up configuration with positive reference in Figure 2.9, the equivalent circuits for each position of the switch are shown in Figure 3.10.



(a) Switch in position 1 during $d(t)\,T_{SW}$. (b) Switch in position 0 during $d'(t)\,T_{SW}$.

Figure 3.10: Step-up configuration equivalent circuits.

A set of equations can be obtained from the circuit in Figure 3.10a. This circuit represents the converter when the switch is in position 1 during $d(t)\,T_{SW}$

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = v_{C3}(t) - v_{C2}(t) \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_L(t) - i_1(t) \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_1(t) - i_L(t) - \frac{v_{C3}(t)}{R} \\ v_1(t) = v_{C3}(t) - v_{C2}(t) \end{cases} \tag{3.45}$$

When the switch is in position 0 during $d(t)'\,T_{SW}$, as shown in Figure 3.10b, the equations that represent the circuit are

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = -v_{C2}(t) \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_L(t) - i_1(t) \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_1(t) - \frac{v_{C3}(t)}{R} \\ v_1(t) = v_{C3}(t) - v_{C2}(t) \end{cases} \tag{3.46}$$

The averaged model results in

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C2}(t) \\ v_{C3}(t) \end{bmatrix} = \begin{bmatrix} 0 & -1 & d(t) \\ 1 & 0 & 0 \\ -d(t) & 0 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C2}(t) \\ v_{C3}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \\ 1 \end{bmatrix} [i_1] \\ [v_1(t)] = \begin{bmatrix} 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C2}(t) \\ v_{C3}(t) \end{bmatrix} \end{cases} \tag{3.47}$$

The equations that define the circuit in steady-state are

$$\begin{cases} I_L = I_1 \\ V_{C2} = I_1 RD'D = V_1 \frac{D}{D'} \\ V_{C3} = I_1 RD' \quad = V_1 \frac{1}{D'} \\ V_1 = I_1 RD'^2 \end{cases} \tag{3.48}$$

The small-signal model has the following expression

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C3}(t) \end{bmatrix} = \begin{bmatrix} -\hat{v}_{C2}(t) + D\hat{v}_{C3}(t) \\ \hat{i}_L(t) \\ -D\hat{i}_L(t) - \frac{\hat{v}_{C3}(t)}{R} \end{bmatrix} + \begin{bmatrix} 0 \\ -\hat{i}_1(t) \\ \hat{i}_1(t) \end{bmatrix} + \begin{bmatrix} V_{C3} \\ 0 \\ -I_L \end{bmatrix} \hat{d}(t) \\ [\hat{v}_1(t)] = \left[\hat{v}_{C3}(t) - \hat{v}_{C2}(t)\right] \end{cases} \tag{3.49}$$

Solving (3.49)

$$\begin{cases} \hat{v}_L(t) = \hat{v}_1(t) - D'\hat{v}_{C3}(t) + V_3\hat{d}(t) \\ D'\hat{i}_L(t) = \hat{i}_{C2}(t) + \hat{i}_{C3}(t) + \frac{\hat{v}_{C3}(t)}{R} + I_L\hat{d}(t) \end{cases} \tag{3.50}$$

Arranging (3.50) for control-to-output transfer function calculation

$$\begin{cases} \hat{v}_L(t) = \hat{v}_1(t) - D'\hat{v}_{C3}(t) + V_3\hat{d}(t) \\ D'\hat{i}_L(t) = (C_2 + C_3)\frac{d\hat{v}_{C3}(t)}{dt} - C_2\frac{d\hat{v}_1(t)}{dt} + \frac{\hat{v}_{C3}(t)}{R} - I_L\hat{d}(t) \end{cases} \tag{3.51}$$

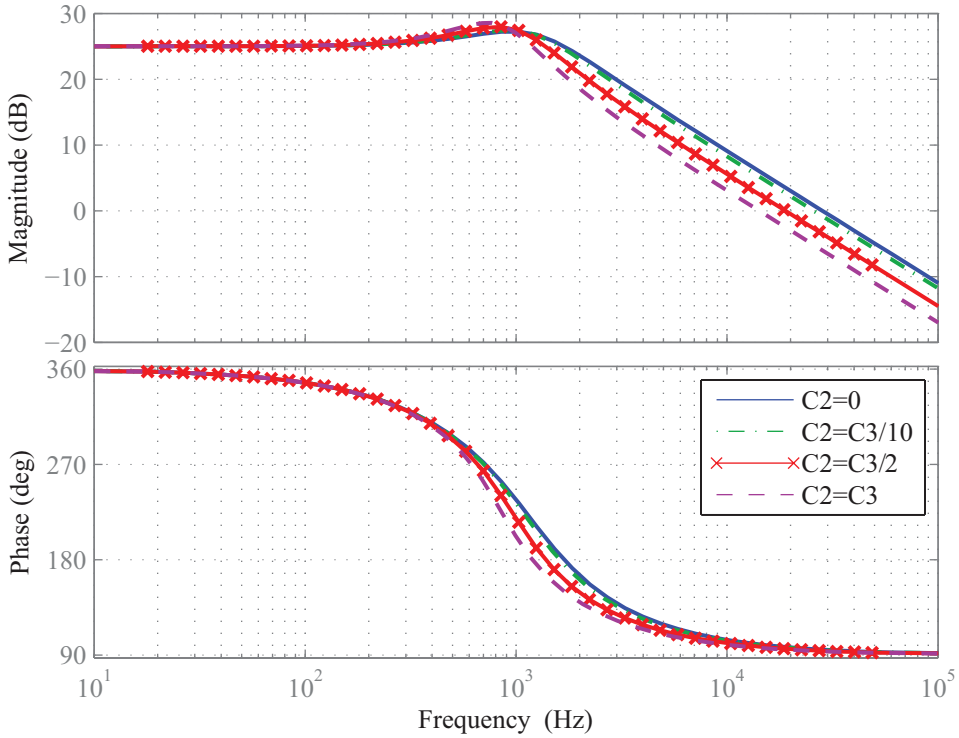
To obtain the control-to-output transfer function it is needed to set $\hat{v}_2 = 0$. Hence, the result is

$$G_{vd}(s) = \left.\frac{\hat{v}_{C3}(s)}{\hat{d}(s)}\right|_{\hat{v}_1(s)=0} = \frac{V_{C3}}{D'} \frac{1 - \frac{Ls}{D'^2R}}{1 + \frac{Ls}{D'^2R} + \frac{(C_2+C_3)Ls^2}{D'^2}} \tag{3.52}$$

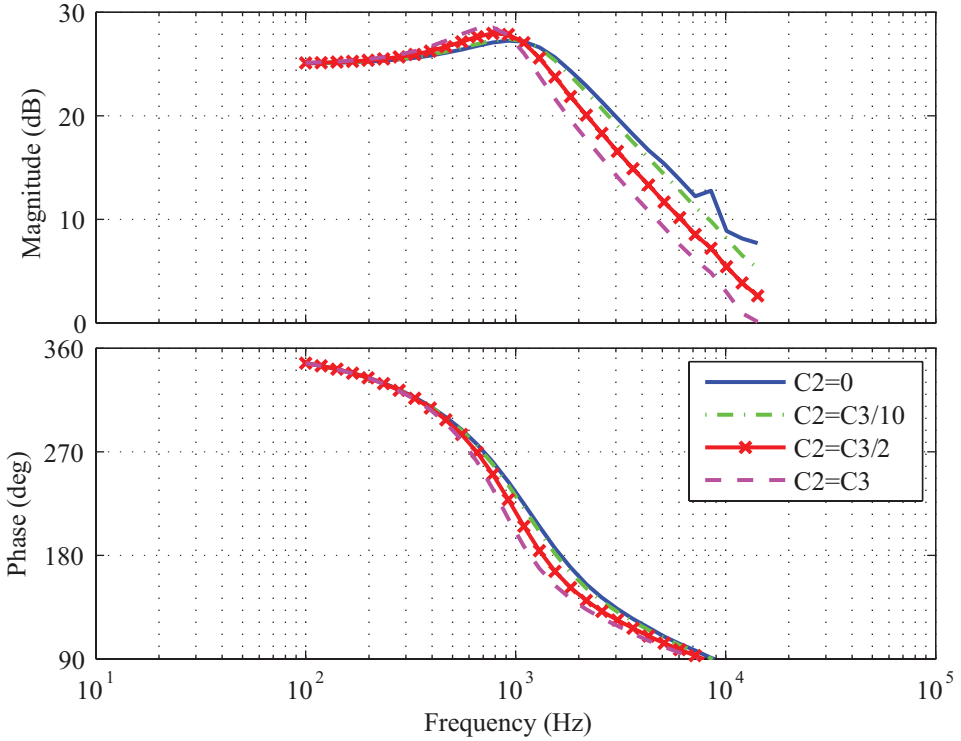
It can be seen in (3.52) that the system has 2 poles and 1 zero whose positions depend on the steady-state of the converter. In addition, the capacitance C_2 adds to C_3. The function obtained in (3.52) is compared with a computer-based simulation of the converter. Frequency and step responses of both, the transfer function and the circuit are shown in Figure 3.11 and Figure 3.12. The parameters considered for the example are detailed in Table 3.4. Several curves are obtained for different values of C_2 and D.

Table 3.4: Step-up configuration parameters

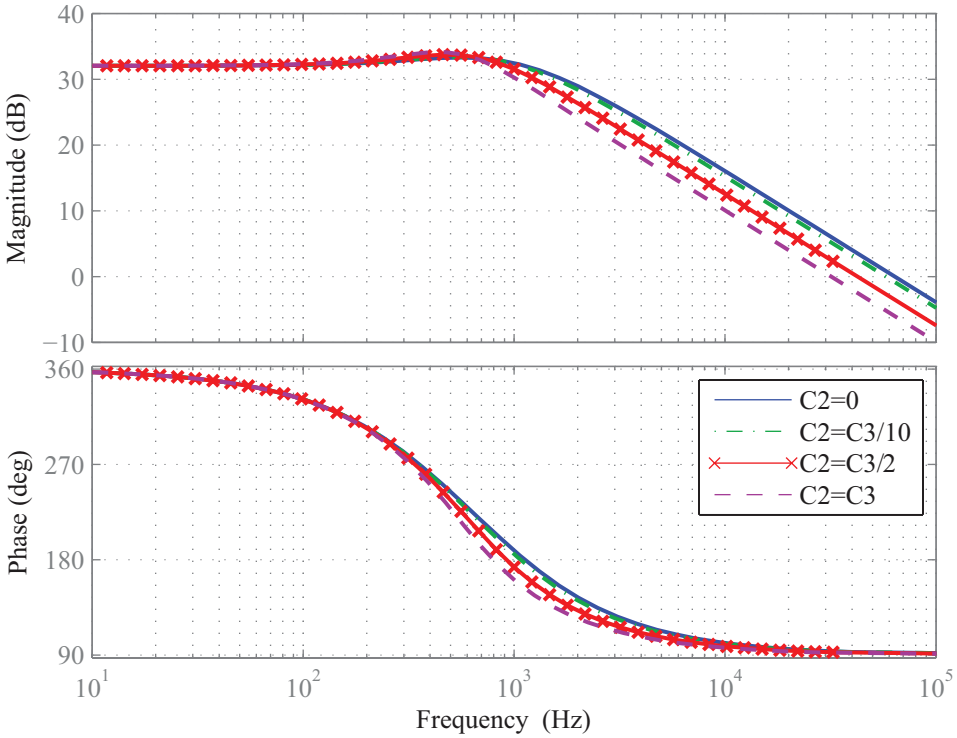
$F_{SW} = 100KHz$	$R = 1\Omega$
$V_1 = 10V$	$L = 100\mu H$
$\hat{d} = D/50$	$C_3 = 100\mu F$



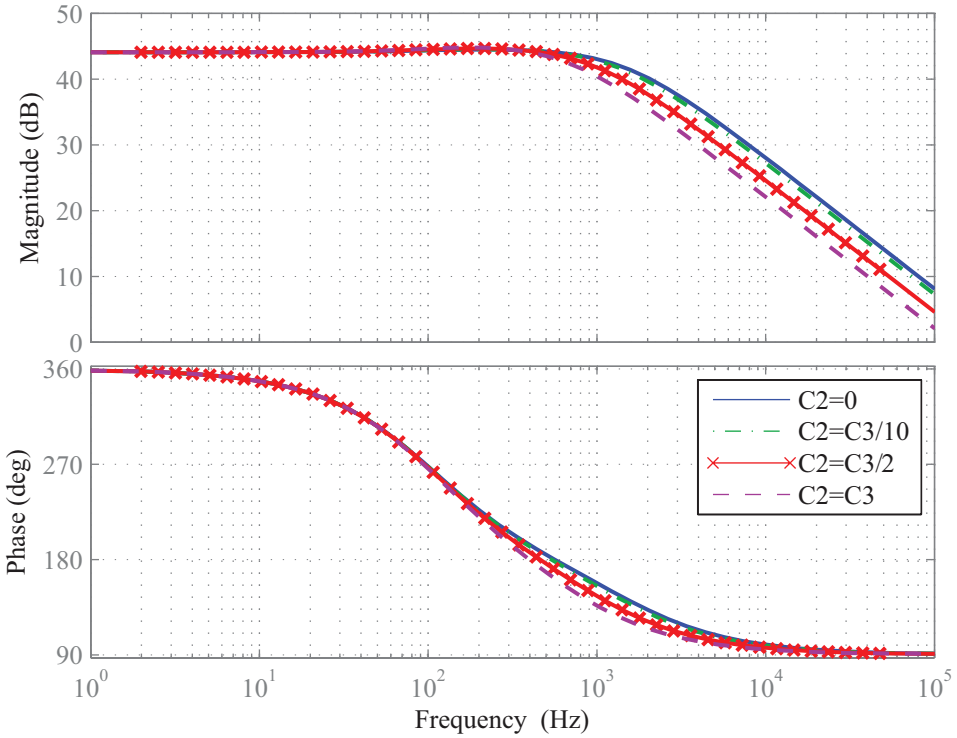
(a) Transfer function frequency response, $D = 0.25$.



(b) Simulated circuit open-loop frequency response, $D = 0.25$.

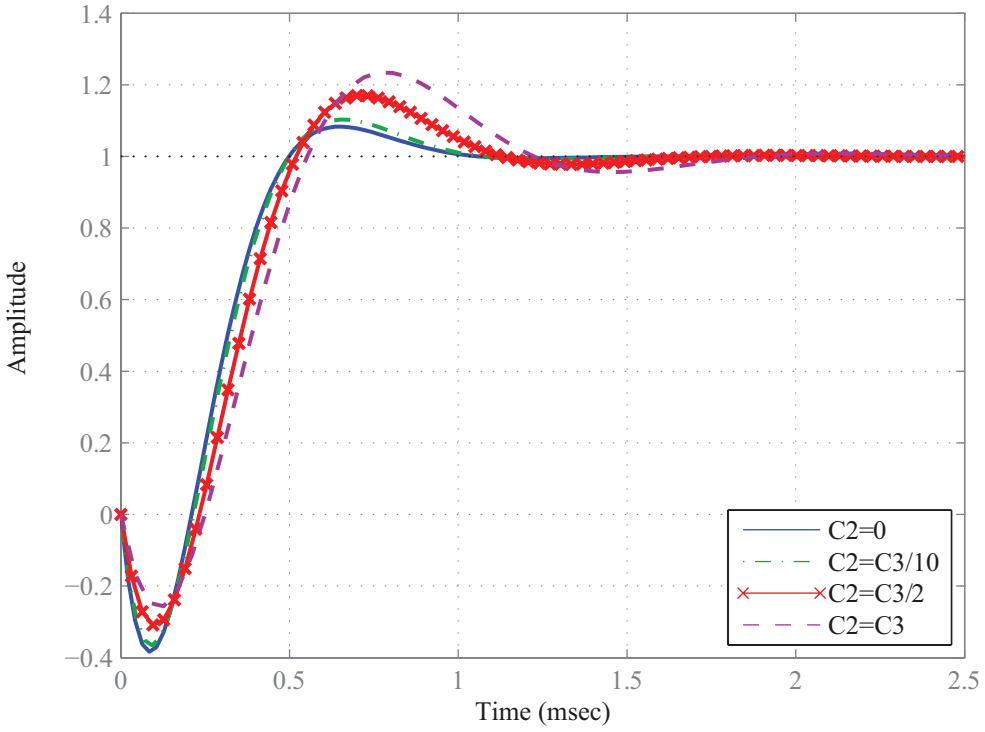


(c) Transfer function frequency response, $D = 0.5$.

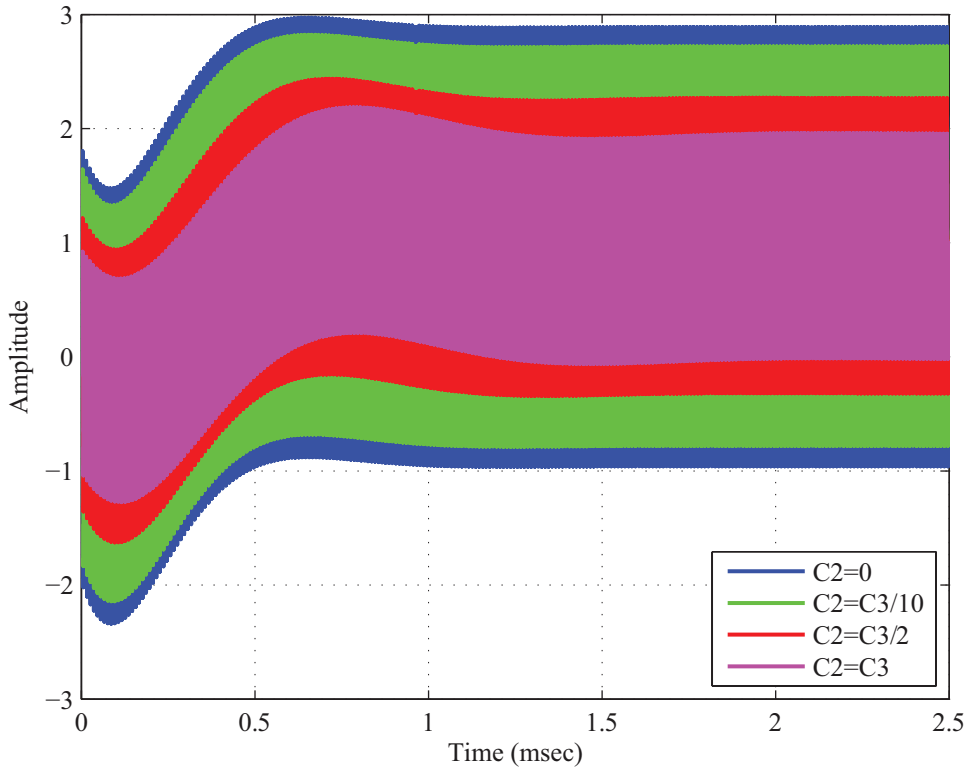


(d) Transfer function frequency response, $D = 0.75$.

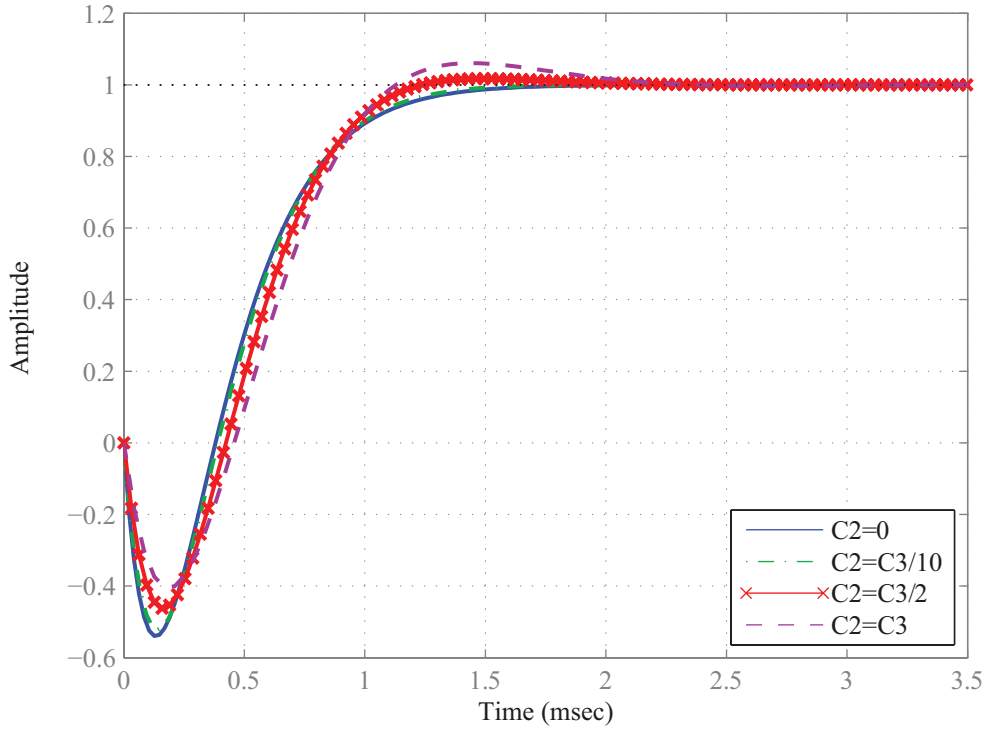
Figure 3.11: Frequency responses for step-up configuration with positive reference.



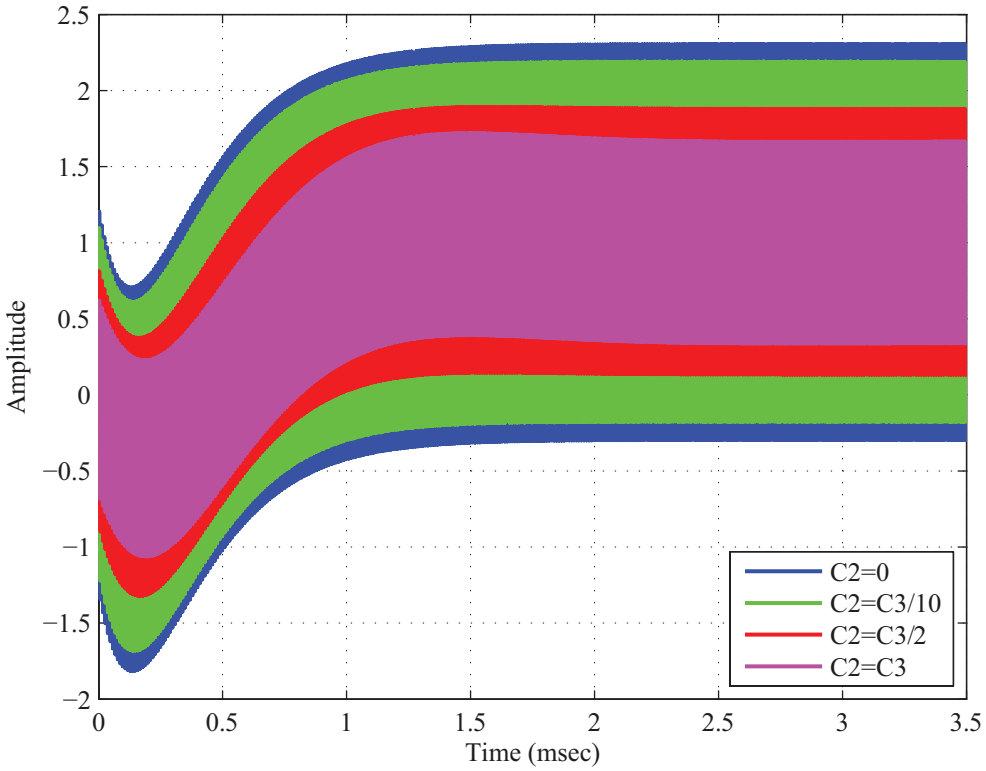
(a) Transfer function step response, $D = 0.25$.



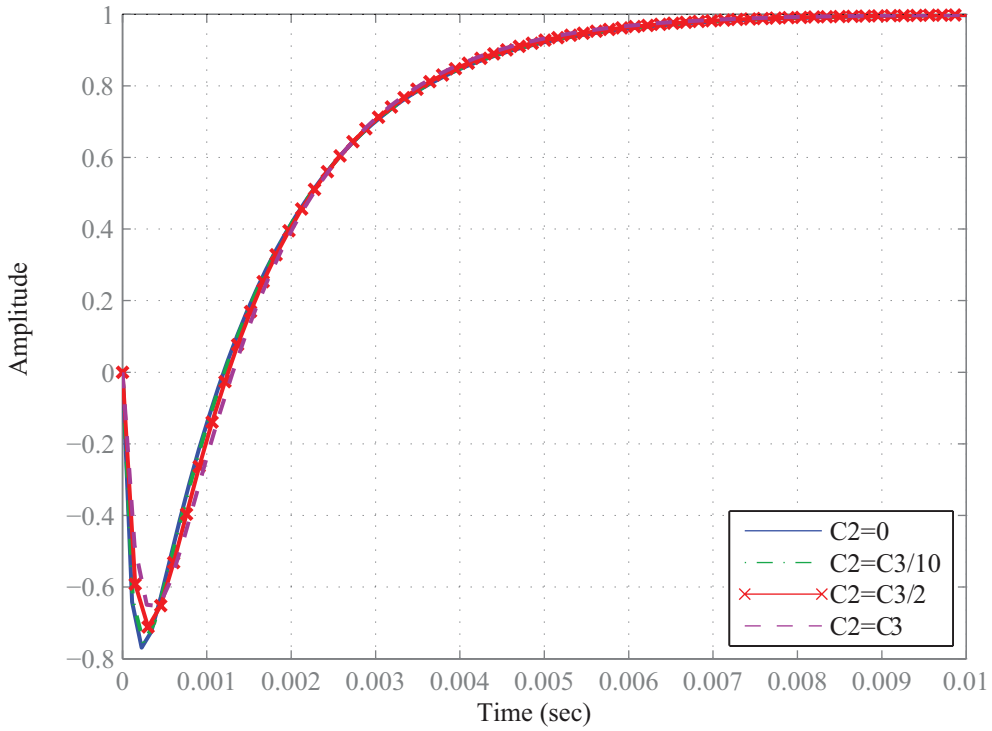
(b) Simulated circuit open-loop step response, $D = 0.25$.



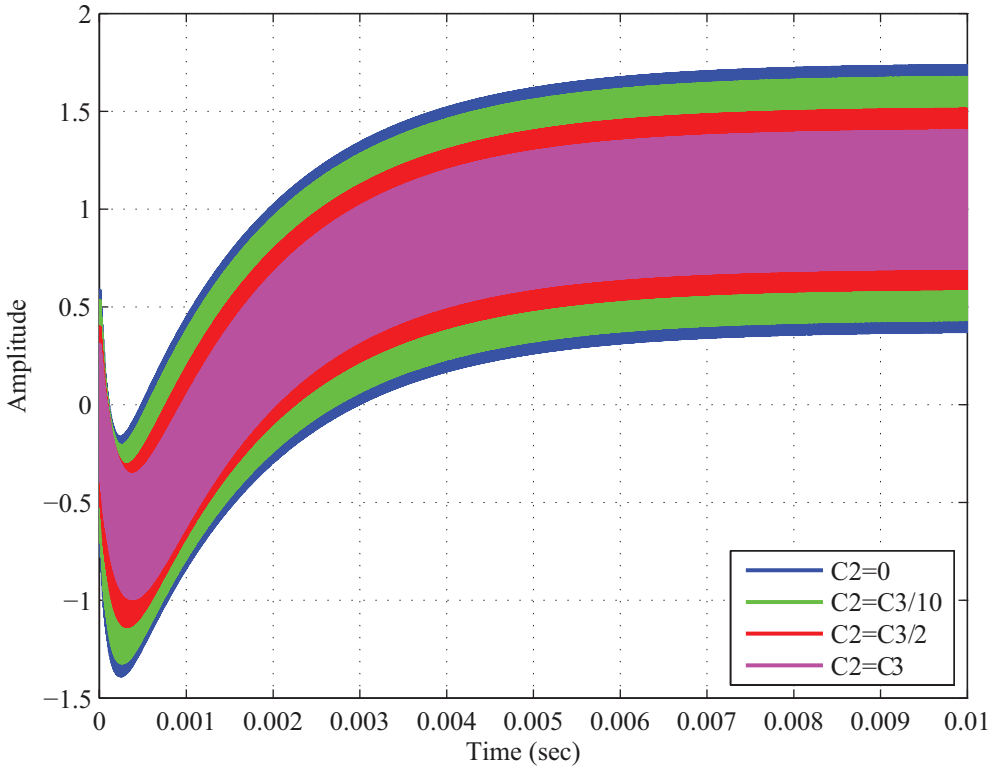
(c) Transfer function step response, $D = 0.5$.



(d) Simulated circuit open-loop step response, $D = 0.5$.



(e) Transfer function step response, $D = 0.75$.



(f) Simulated circuit open-loop step response, $D = 0.75$.

Figure 3.12: Step responses for step-up configuration with positive reference.

From the previous graphics it can be stated that there is strong correlation between the transfer function and the simulated circuit behaviour. This validates the small-signal analysis and its results to model the Topology Zero. The inclusion of the capacitance C_2 affects the cutoff frequency of the system according to

$$f_0 = \frac{D'}{2\pi\sqrt{L\left(C_2 + C_3\right)}} \tag{3.53}$$

The effects of the frequency displacement can be observed in both the frequency and step responses. When C_2 increases, the cutoff frequency decreases. Additionally, the frequency response is affected by the RHZ and the duty cycle in steady-state. The frequency of the RHZ is given by

$$f_z = \frac{D'^2 R}{2\pi L} \tag{3.54}$$

The relative positions of the zero and poles define the shape of the frequency response for different values of D. In the magnitude response (Figure 3.11), the gain peak near the cutoff frequency disappear when the duty cycle increases its value. In the step response of the system, the response changes from underdamped to overdamped when the duty cycle goes from lower values to higher ones. This can be appreciated in Figure 3.12.

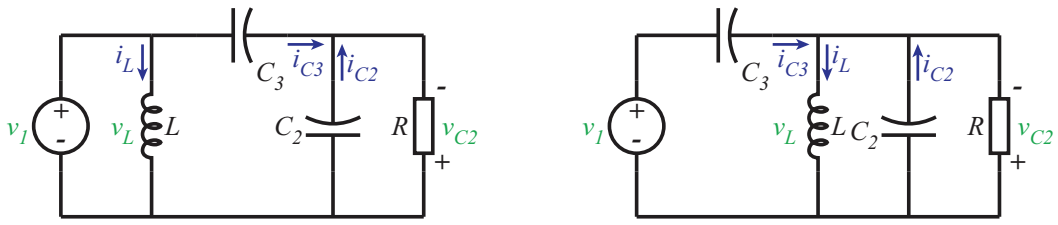
The responses for the Topology Zero in step-up configuration show similarities between positive and negative reference. Both transfer functions have gain and singularities affected by the steady-state of the converter. As well, the influence of the right-half plane zero is observed in the step responses graphics when initially the output voltage goes in opposite direction of the final value. In addition, one of the difference is that the output voltage changes in opposite form for either of the configurations when a step in duty cycle is applied. However the ripple voltage decreases when the duty cycle increases its steady-stated value.

3.3 Topology Zero Step-down-step-up Configurations

The summarized derivation of the small-signal analysis for step-down-step-up operation of the Topology Zero in its two variants is next presented.

3.3.1 Step-down-step-up Configuration with Negative Reference

Consider the step-down-step-up configuration with negative reference shown in Figure 2.11, the equivalent circuits for each position of the switch are shown in Figure 3.13.



(a) Switch in position 1 during $d(t)\,T_{SW}$.

(b) Switch in position 0 during $d'(t)\,T_{SW}$.

Figure 3.13: Step-down-step-up configuration equivalent circuits.

A set of equations can be obtained from the circuit in Figure 3.13a. This circuit represents the converter when the switch is in position 1 during $d(t)\,T_{SW}$

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = v_{C3}(t) - v_{C2}(t) \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_L(t) - i_1(t) - \frac{v_{C2}(t)}{R} \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_1(t) - i_L(t) \\ v_1(t) = v_{C3}(t) - v_{C2}(t) \end{cases} \tag{3.55}$$

When the switch is in position 0 during $d(t)'\,T_{SW}$, as shown in Figure 3.13b, the equations that represent the circuit are

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = -v_{C2}(t) \\ i_{C2}(t) = C_2\frac{dv_{C2}(t)}{dt} = i_L(t) - i_1(t) - \frac{v_{C2}(t)}{R} \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_1(t) \\ v_1(t) = v_{C3}(t) - v_{C2}(t) \end{cases} \tag{3.56}$$

The averaged model results in

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C2}(t) \\ v_{C3}(t) \end{bmatrix} = \begin{bmatrix} 0 & -1 & d(t) \\ 1 & -\frac{1}{R} & 0 \\ -d(t) & 0 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C2}(t) \\ v_{C3}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \\ 1 \end{bmatrix} [i_1] \\ [v_1(t)] = \begin{bmatrix} 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C2}(t) \\ v_{C3}(t) \end{bmatrix} \end{cases} \tag{3.57}$$

The equations that define the circuit in steady-state are

$$\begin{cases} I_L = \frac{I_1}{D} \\ V_{C2} = I_1 R \frac{D'}{D} = V_1 \frac{D}{D'} \\ V_{C3} = I_1 R \frac{D'}{D^2} = V_1 \frac{1}{D'} \\ V_1 = I_1 R \frac{D'^2}{D^2} \end{cases} \tag{3.58}$$

The small-signal model has the following expression

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C3}(t) \end{bmatrix} = \begin{bmatrix} -\hat{v}_{C2}(t) + D\hat{v}_{C3}(t) \\ \hat{i}_L(t) - \frac{\hat{v}_{C2}(t)}{R} \\ -D\hat{i}_L(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -\hat{i}_1(t) \\ \hat{i}_1(t) \end{bmatrix} + \begin{bmatrix} V_{C3} \\ 0 \\ -I_L \end{bmatrix} \hat{d}(t) \\ [\hat{v}_1(t)] = \left[\hat{v}_{C3}(t) - \hat{v}_{C2}(t)\right] \end{cases} \tag{3.59}$$

Solving (3.59)

$$\begin{cases} \hat{v}_L(t) = D\hat{v}_1(t) - D'\hat{v}_{C2}(t) + V_{C3}\hat{d}(t) \\ D'\hat{i}_L(t) = \hat{i}_{C2}(t) + \hat{i}_{C3}(t) + \frac{\hat{v}_{C2}(t)}{R} + I_L\hat{d}(t) \end{cases} \tag{3.60}$$

Arranging (3.60) for control-to-output transfer function calculation

$$\begin{cases} \hat{v}_L(t) = D\hat{v}_1(t) - D'\hat{v}_{C2}(t) + V_{C3}\hat{d}(t) \\ D'\hat{i}_L(t) = (C_2 + C_3)\frac{d\hat{v}_{C2}(t)}{dt} + C_3\frac{d\hat{v}_1(t)}{dt} + \frac{\hat{v}_{C2}(t)}{R} + I_L\hat{d}(t) \end{cases} \tag{3.61}$$

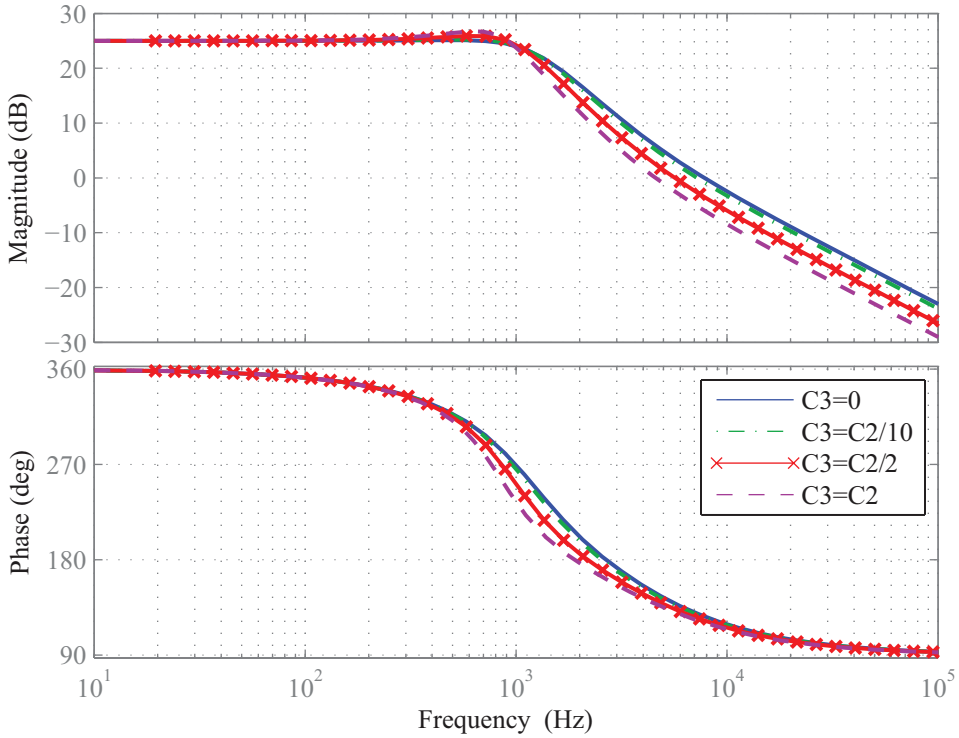
To obtain the control-to-output transfer function it is needed to set $\hat{v}_1 = 0$. The result is then

$$G_{vd}(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{d}(s)}\right|_{\hat{v}_1(s)=0} = \frac{V_{C3}}{D'} \frac{1 - \frac{DLs}{D'^2R}}{1 + \frac{Ls}{D'^2R} + \frac{(C_2+C_3)Ls^2}{D'^2}} \tag{3.62}$$

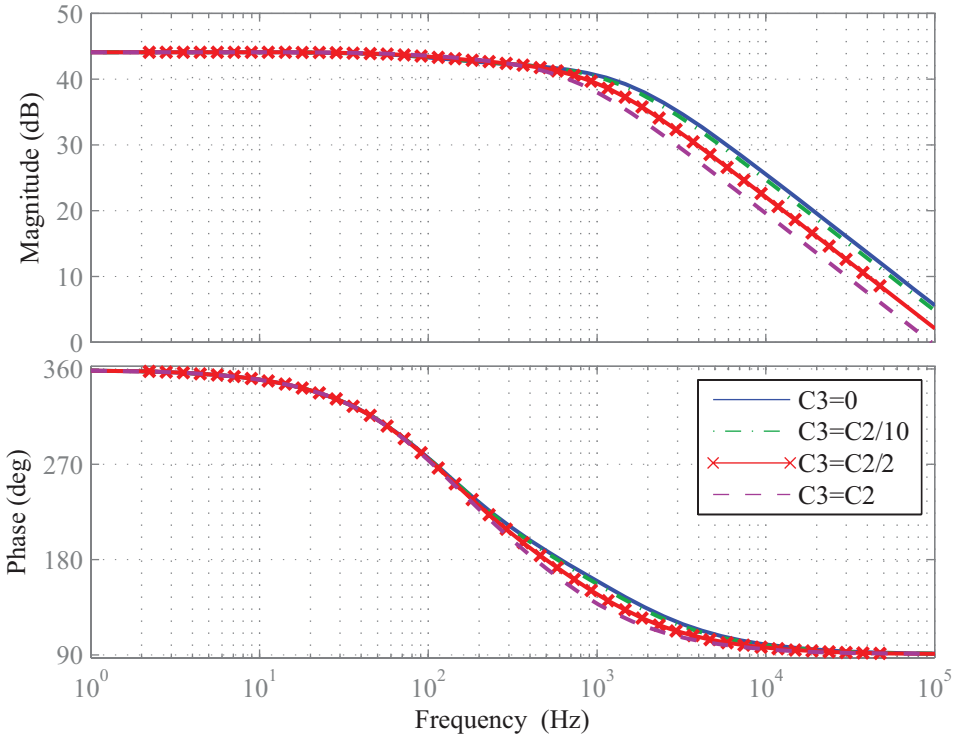
The system has 2 poles and 1 zero whose positions depend on the steady-state of the converter. In addition, the capacitance C_2 adds to C_3. The function obtained in (3.62) is compared with a simulation of the converter. Frequency and step responses of both, the transfer function and the circuit are shown in Figure 3.14 and Figure 3.15. The parameters considered for calculation are detailed in Table 3.5. Several curves are obtained for different values of C_3 and D.

Table 3.5: Step-down-step-up configuration parameters

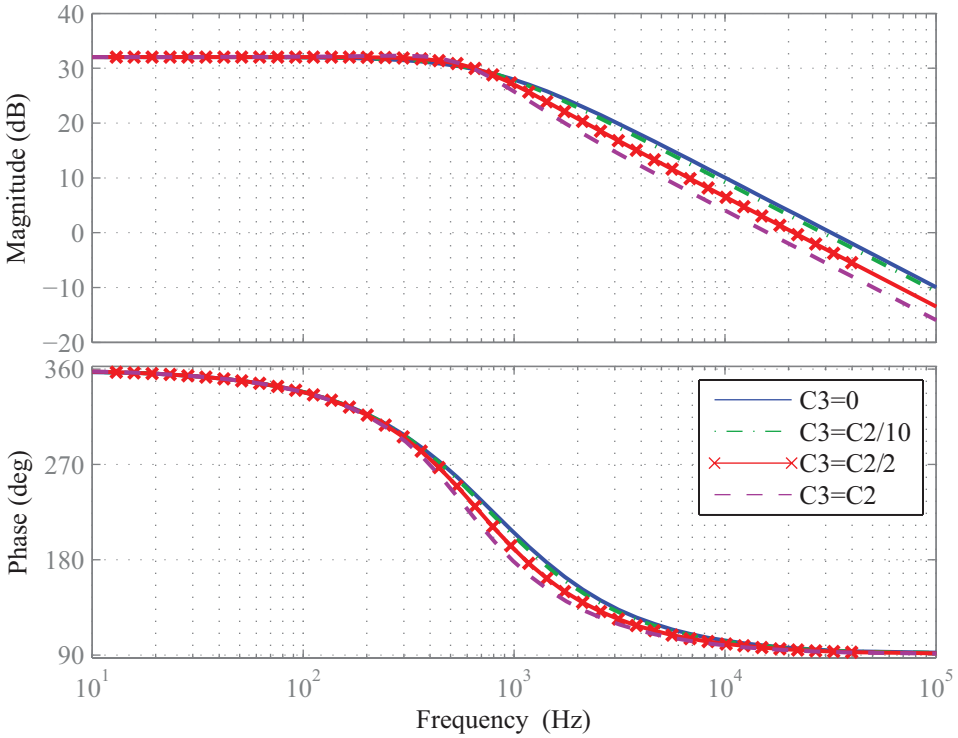
$F_{SW} = 100KHz$	$R = 1\Omega$
$V_1 = 10V$	$L = 100\mu H$
$\hat{d} = D/50$	$C_2 = 100\mu F$



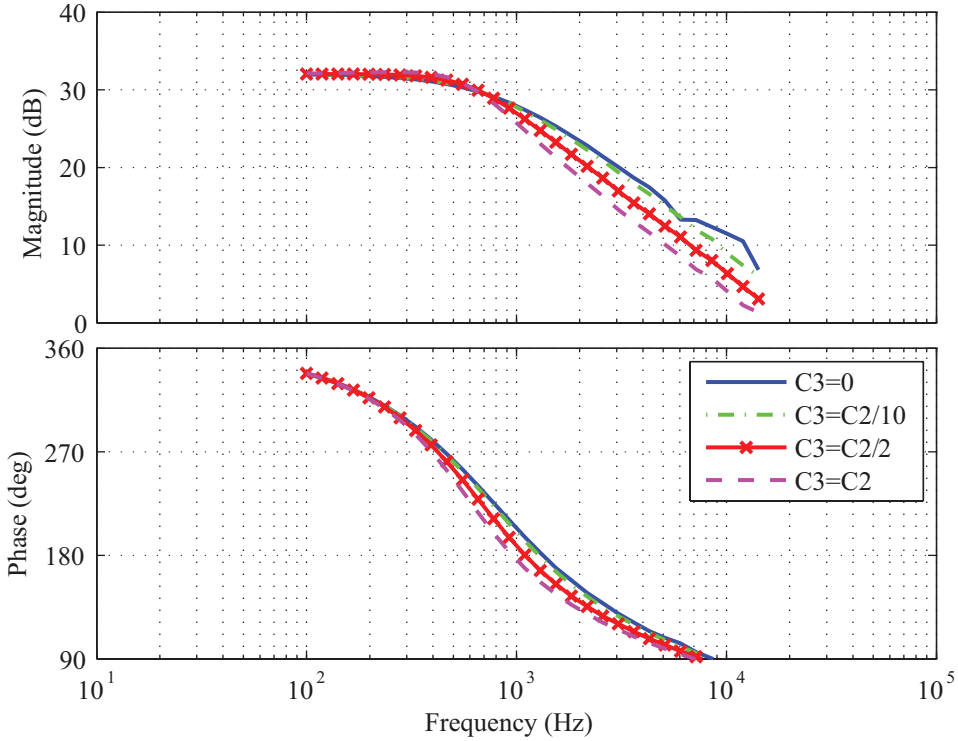
(a) Transfer function frequency response, $D = 0.25$.



(b) Transfer function frequency response, $D = 0.75$.

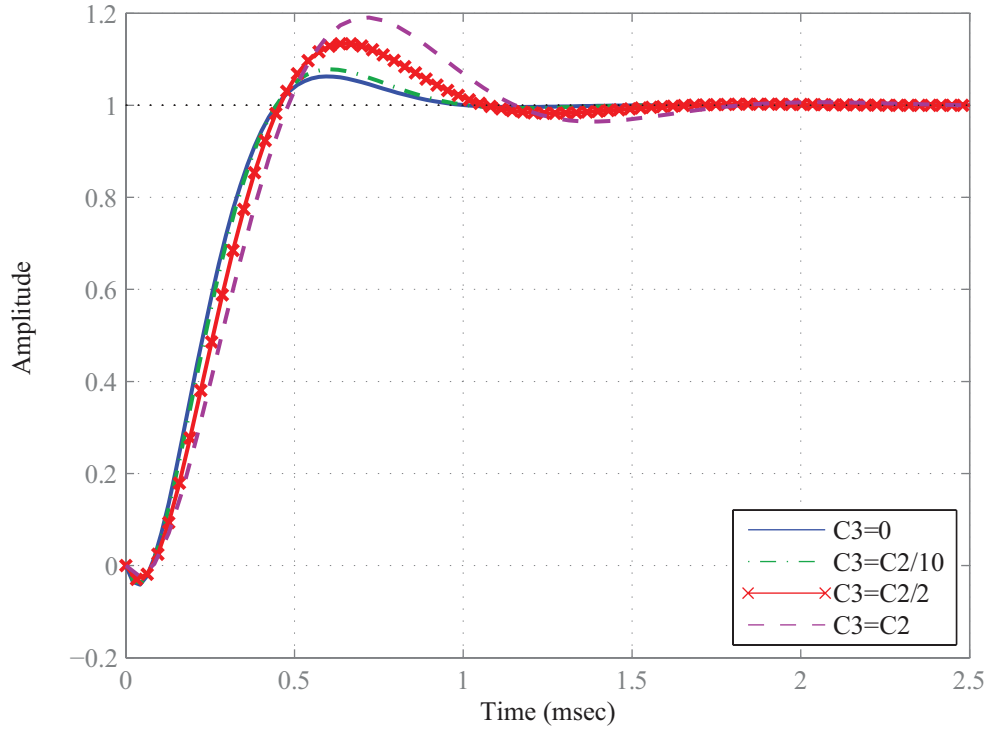


(c) Transfer function frequency response, $D = 0.5$.

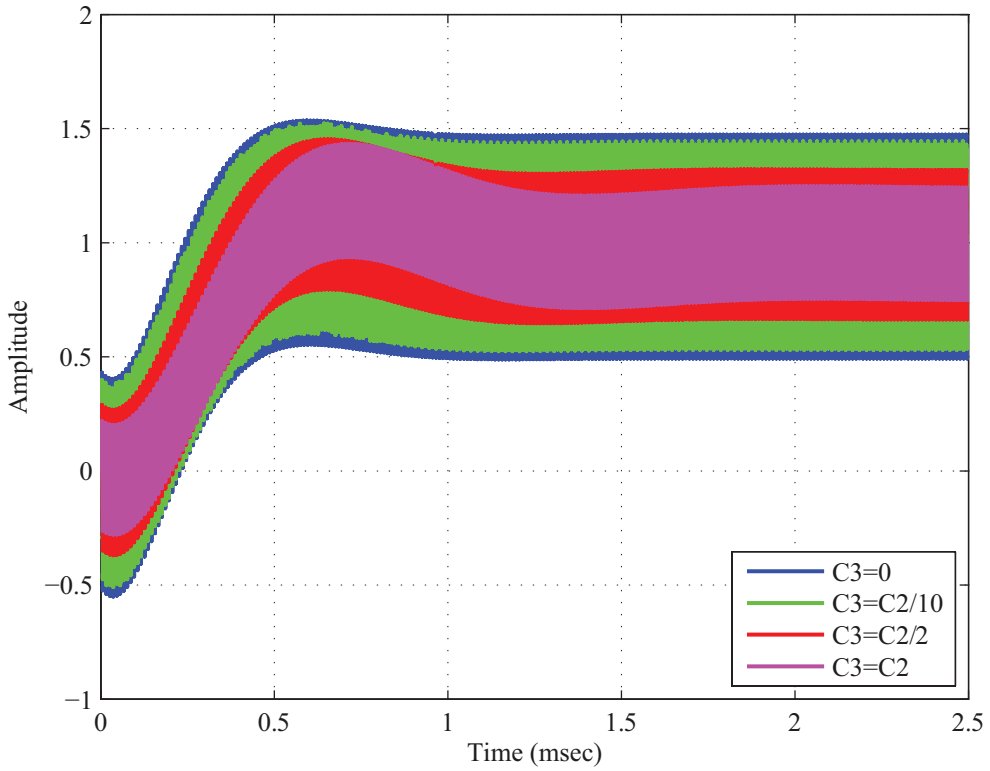


(d) Simulated circuit open-loop frequency response, $D = 0.5$.

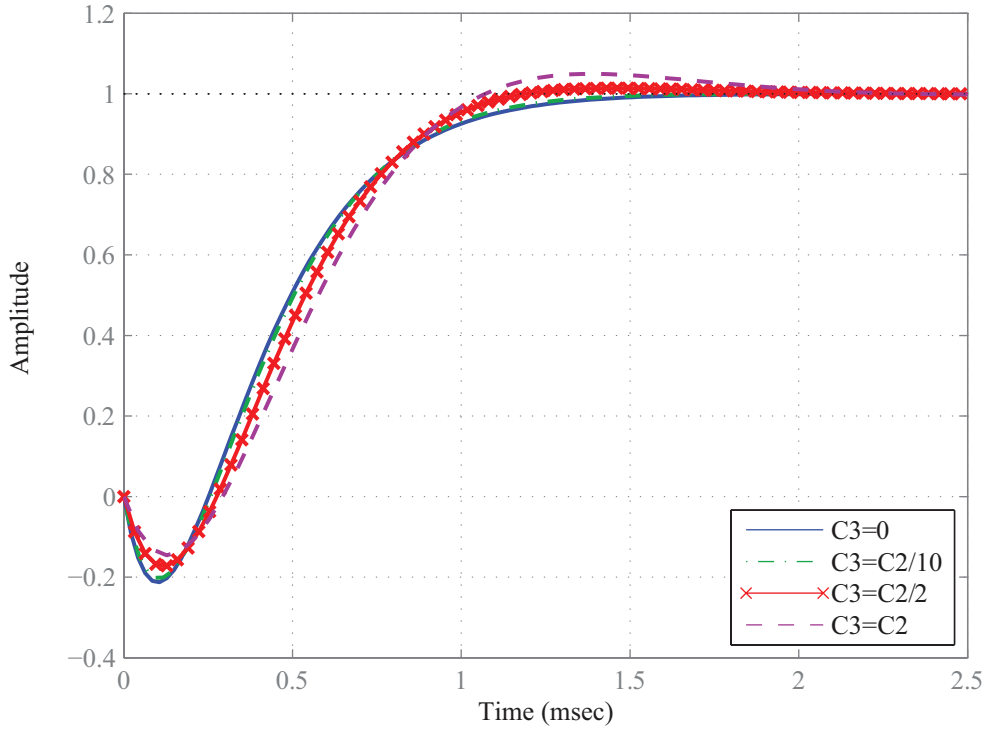
Figure 3.14: Frequency responses for step-down-step-up configuration with negative reference.



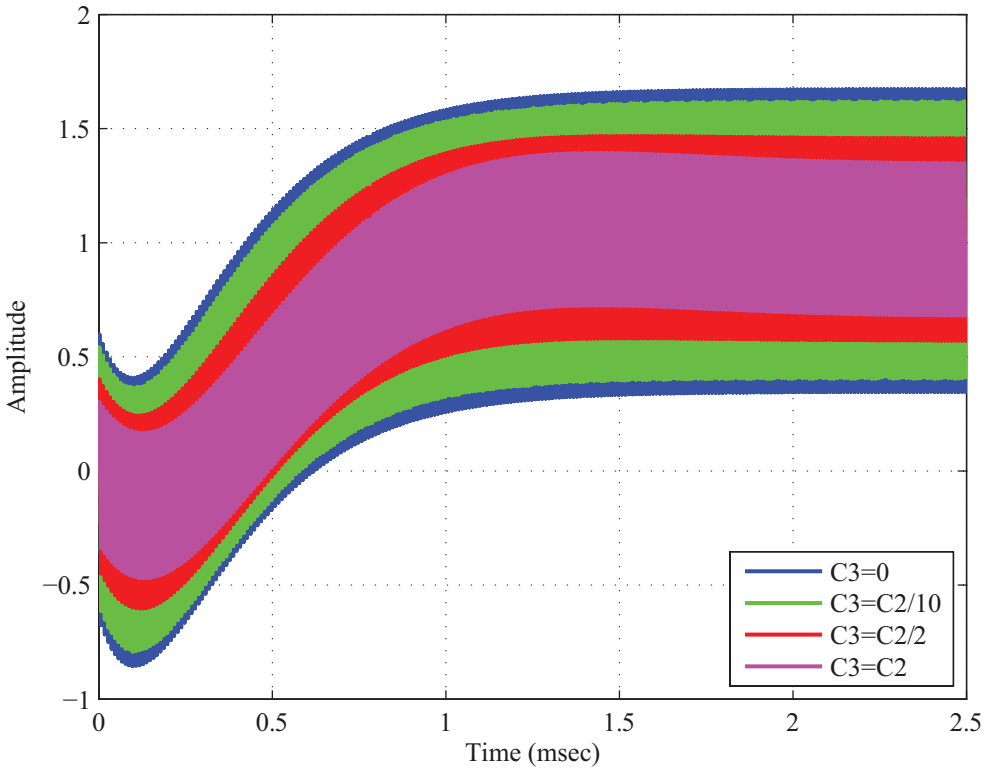
(a) Transfer function step response, $D = 0.25$.



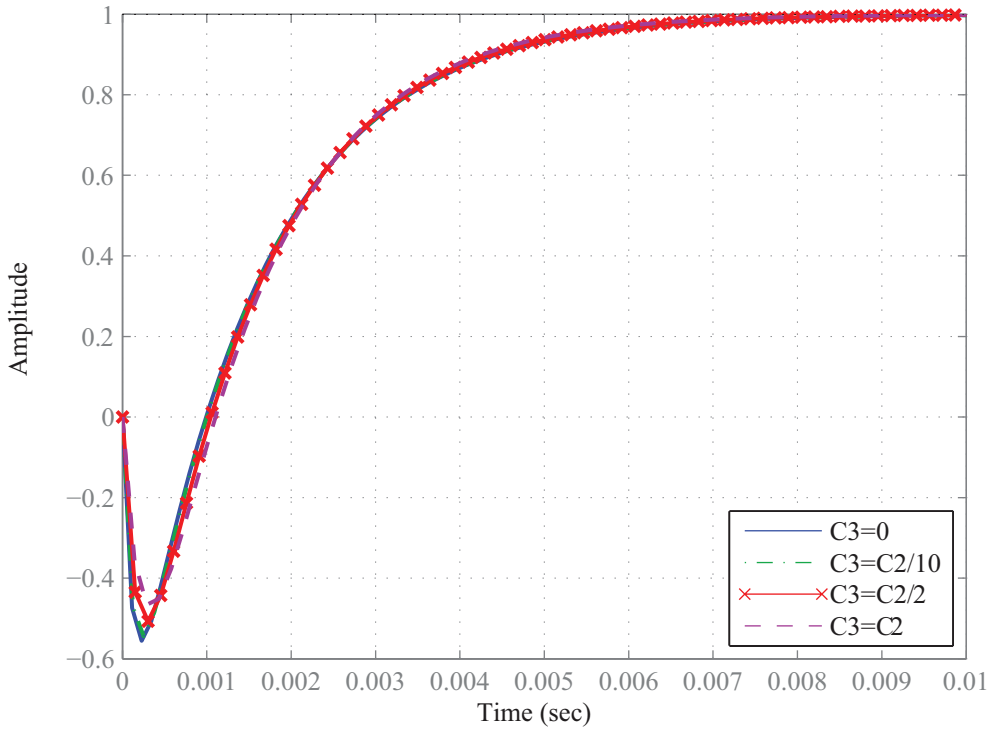
(b) Simulated circuit open-loop step response, $D = 0.25$.



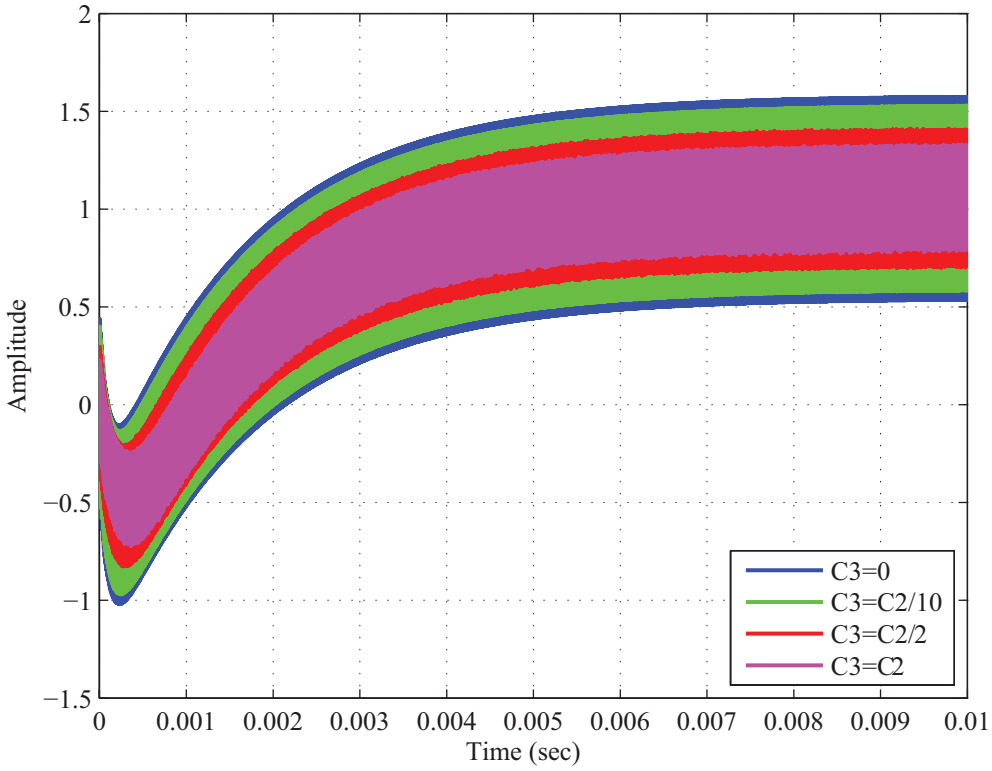
(c) Transfer function step response, $D = 0.5$.



(d) Simulated circuit open-loop step response, $D = 0.5$.



(e) Transfer function step response, $D = 0.75$.



(f) Simulated circuit open-loop step response, $D = 0.75$.

Figure 3.15: Step responses for step-down-step-up configuration with negative reference.

The comparison of the transfer function and the simulation exposes their similarities in the behaviour. This validates the small-signal analysis and its results to model the Topology Zero. When $C_3 = 0$ the Topology Zero becomes a buck-boost converter. The responses for this particular configuration are shown in the previous curves. The buck-boost converter does not consider C_3. Nevertheless, (3.62) remains valid with $C_3 = 0$. The inclusion of the capacitance C_3 alters the cutoff frequency, as expressed by

$$f_0 = \frac{D'}{2\pi\sqrt{L\,(C_2 + C_3)}} \tag{3.63}$$

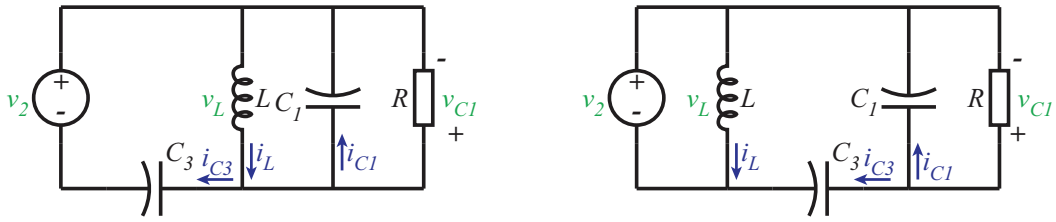
The effects of the root shift are seen in the frequency and step responses. When C_3 increases, the cutoff frequency decreases. Additionally, the dynamic response is affected by the RHZ and the duty cycle in steady-state. The frequency of the RHZ is expressed by

$$f_z = \frac{D'^2 R}{2\pi DL} \tag{3.64}$$

In the magnitude response (Figure 3.14), for lower values of steady-state duty cycle there is a peak in the gain near the cutoff frequency. The peak reduces when D increases. The step response of the system is influenced by the relative position of the zero and the poles, and by the steady-state condition. The response changes from underdamped to overdamped when D varies form lower to higher values (Figure 3.15). The influence of the RHZ is observed, as well, when in the step response the output goes initially in opposite direction of the final value.

3.3.2 Step-down-step-up Configuration with Positive Reference

Consider the step-down-step-up configuration with positive reference shown in Figure 2.13, the equivalent circuits for each position of the switch are shown in Figure 3.16.



(a) Switch in position 1 during $d(t)\,T_{SW}$.

(b) Switch in position 0 during $d'(t)\,T_{SW}$.

Figure 3.16: Step-down-step-up configuration equivalent circuits.

A set of equations can be obtained from the circuit in Figure 3.16a. This circuit represents the converter when the switch is in position 1 during $d(t)\,T_{SW}$.

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = -v_{C1}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_L(t) - i_2(t) - \frac{v_{C1}(t)}{R} \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_2(t) \\ v_2(t) = v_{C3}(t) - v_{C1}(t) \end{cases} \tag{3.65}$$

When the switch is in position 0 during $d(t)'\,T_{SW}$, as shown in Figure 3.16b, the equations that represent the circuit are

$$\begin{cases} v_L(t) = L\frac{di_L(t)}{dt} = v_{C3}(t) - v_{C1}(t) \\ i_{C1}(t) = C_1\frac{dv_{C1}(t)}{dt} = i_L(t) - i_2(t) - \frac{v_{C1}(t)}{R} \\ i_{C3}(t) = C_3\frac{dv_{C3}(t)}{dt} = i_2(t) - i_L(t) \\ v_2(t) = v_{C3}(t) - v_{C1}(t) \end{cases} \tag{3.66}$$

The averaged model results in

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C3}(t) \end{bmatrix} = \begin{bmatrix} 0 & -1 & d'(t) \\ 1 & -\frac{1}{R} & 0 \\ -d'(t) & 0 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C3}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -1 \\ 1 \end{bmatrix} [i_2] \\ [v_2(t)] = \begin{bmatrix} 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_{C1}(t) \\ v_{C3}(t) \end{bmatrix} \end{cases} \tag{3.67}$$

The equations that define the circuit in steady-state are

$$\begin{cases} I_L = \frac{I_2}{D'} \\ V_{C1} = I_2 R\frac{D}{D'} = V_2\frac{D'}{D} \\ V_{C3} = I_2 R\frac{D}{D'^2} = V_2\frac{1}{D} \\ V_2 = I_2 R\frac{D^2}{D'^2} \end{cases} \tag{3.68}$$

The small-signal model has the following expression

$$\begin{cases} \begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C3}(t) \end{bmatrix} = \begin{bmatrix} -\hat{v}_{C1}(t) + D'\hat{v}_{C3}(t) \\ \hat{i}_L(t) - \frac{\hat{v}_{C1}(t)}{R} \\ -D'\hat{i}_L(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -\hat{i}_2(t) \\ \hat{i}_2(t) \end{bmatrix} + \begin{bmatrix} -V_{C3} \\ 0 \\ I_L \end{bmatrix} \hat{d}(t) \\ [\hat{v}_2(t)] = \left[\hat{v}_{C3}(t) - \hat{v}_{C1}(t)\right] \end{cases} \tag{3.69}$$

Solving (3.69)

$$\begin{cases} \hat{v}_L(t) = D'\hat{v}_2(t) - D\hat{v}_{C1}(t) - V_{C3}\hat{d}(t) \\ D\hat{i}_L(t) = \hat{i}_{C1}(t) + \hat{i}_{C3}(t) + \frac{\hat{v}_{C1}(t)}{R} - I_L\hat{d}(t) \end{cases} \tag{3.70}$$

Arranging (3.70) for control-to-output transfer function calculation

$$\begin{cases} \hat{v}_L(t) = D'\hat{v}_2(t) - D\hat{v}_{C1}(t) - V_{C3}\hat{d}(t) \\ D\hat{i}_L(t) = (C_1 + C_3)\frac{d\hat{v}_{C1}(t)}{dt} + C_3\frac{d\hat{v}_2(t)}{dt} + \frac{\hat{v}_{C1}(t)}{R} + I_L\hat{d}(t) \end{cases} \tag{3.71}$$

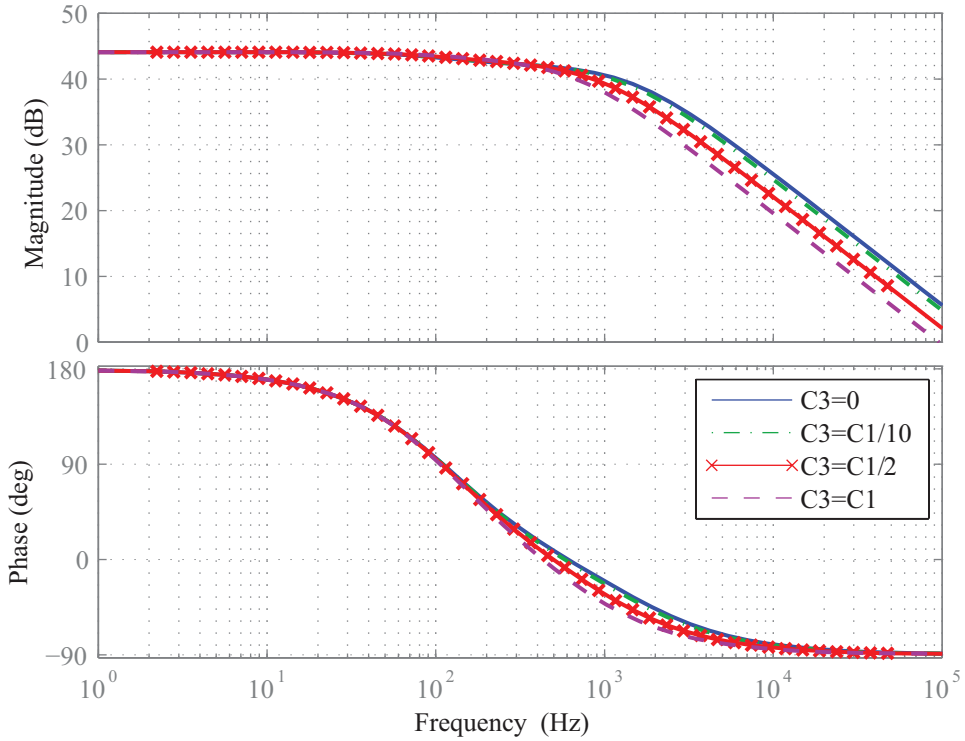
To obtain the control-to-output transfer function it is needed to set $\hat{v}_2 = 0$. The result is then

$$G_{vd}(s) = \left.\frac{\hat{v}_{C1}(s)}{\hat{d}(s)}\right|_{\hat{v}_2(s)=0} = -\frac{V_{C3}}{D}\frac{1 - \frac{D'Ls}{D^2R}}{1 + \frac{Ls}{D^2R} + \frac{(C_1+C_3)Ls^2}{D^2}} \tag{3.72}$$

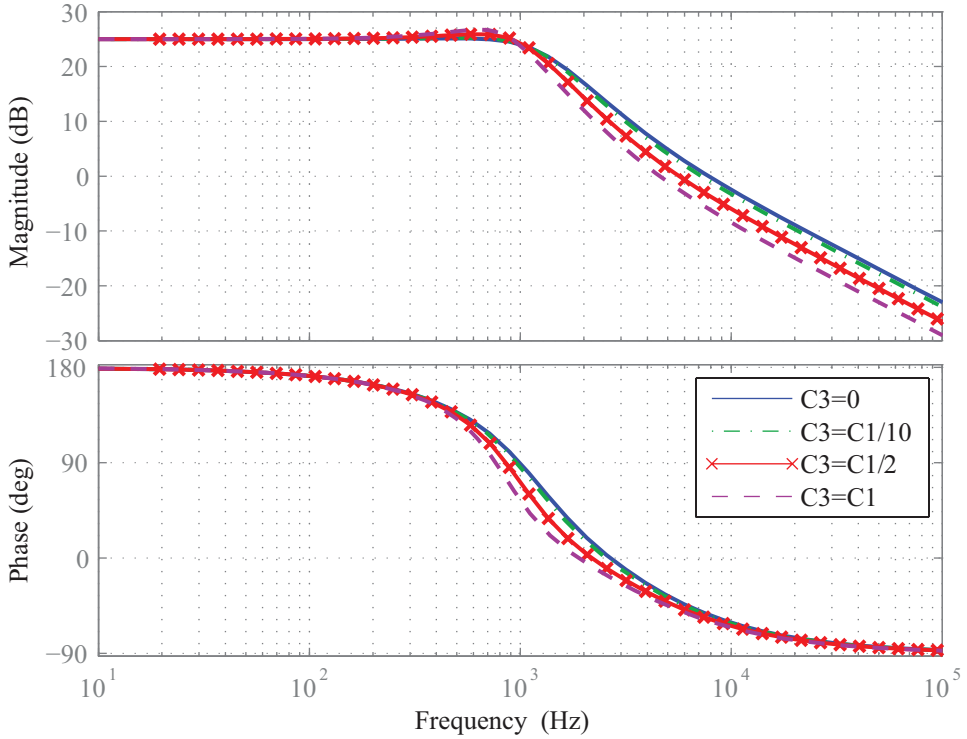
The system has 2 poles and 1 zero whose positions depend on the steady-state of the converter. In addition, the capacitance C_1 adds to C_3. The function obtained in (3.72) is compared with a simulation of the converter. Frequency and step responses of both, the transfer function and the circuit are shown in Figure 3.17 and Figure 3.18. The parameters considered for calculation are detailed in Table 3.6. Several curves are obtained for different values of C_3 and D.

Table 3.6: Step-down-step-up configuration parameters

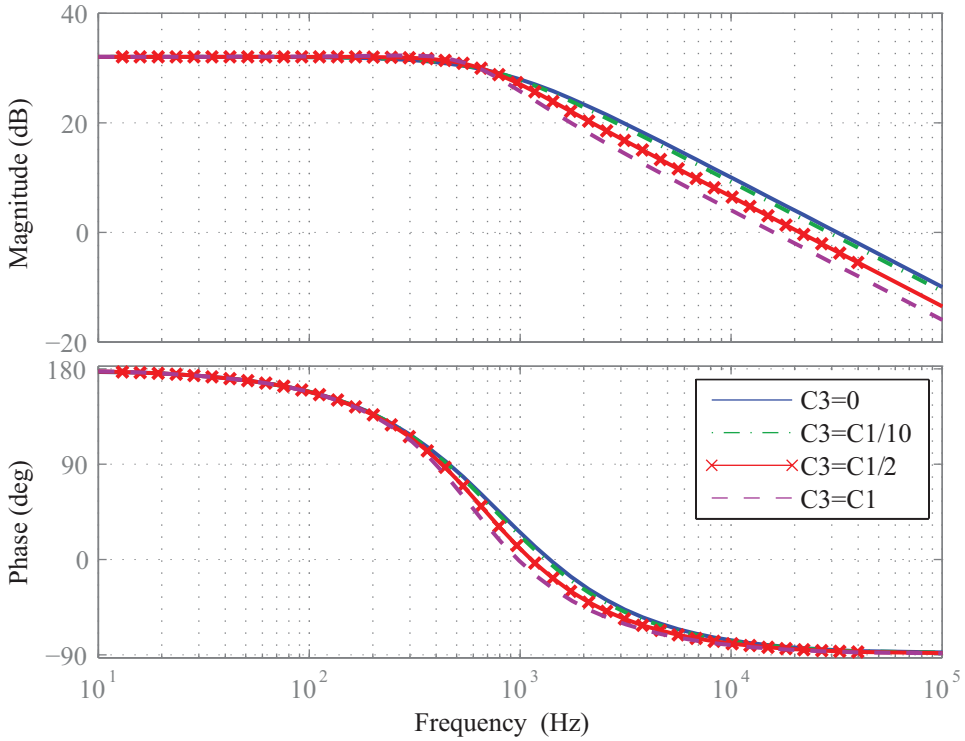
F_{SW} = 100KHz	R = 1Ω
V_2 = 10V	L = 100μH
$\hat{d}$ = D/50	C_1 = 100μF



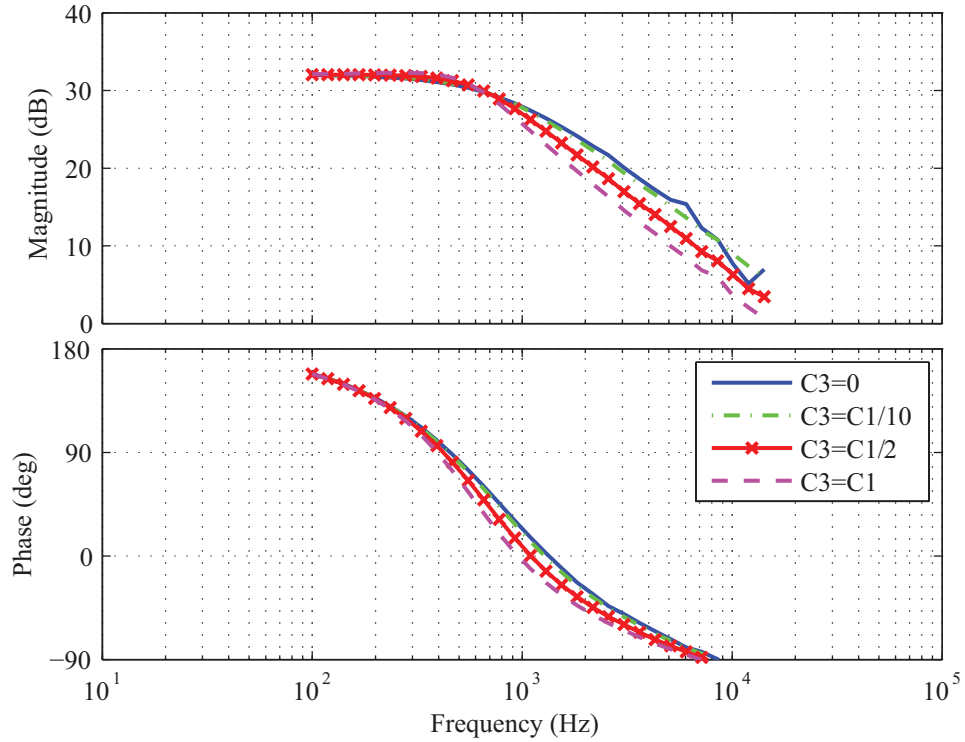
(a) Transfer function frequency response, $D = 0.25$.



(b) Transfer function frequency response, $D = 0.75$.

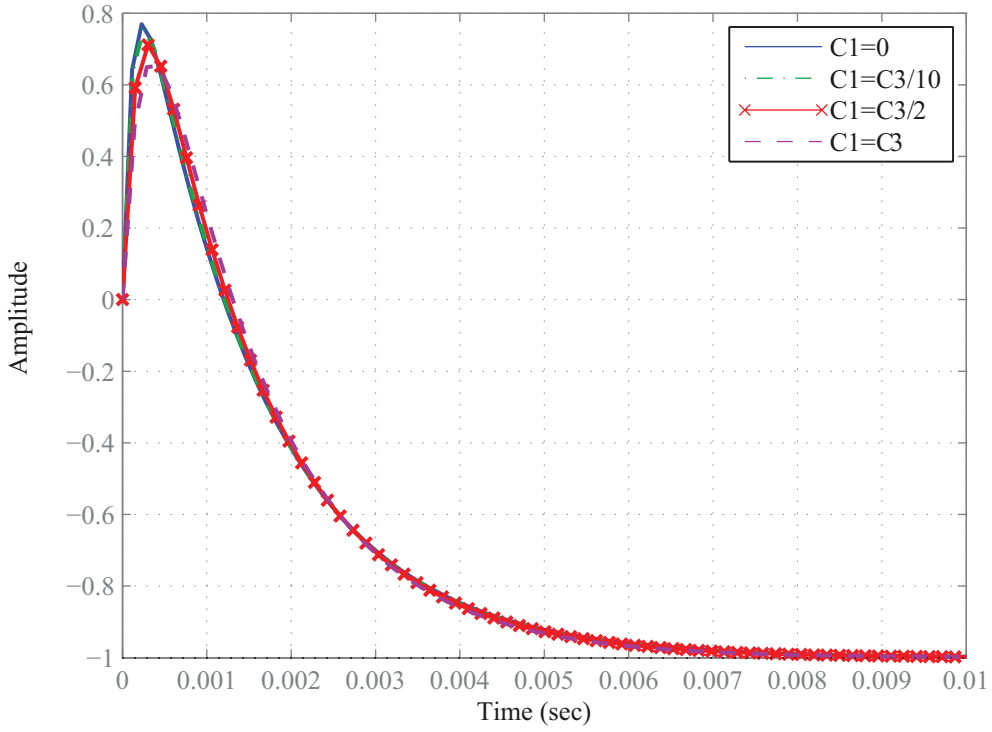


(c) Transfer function frequency response, $D = 0.5$.

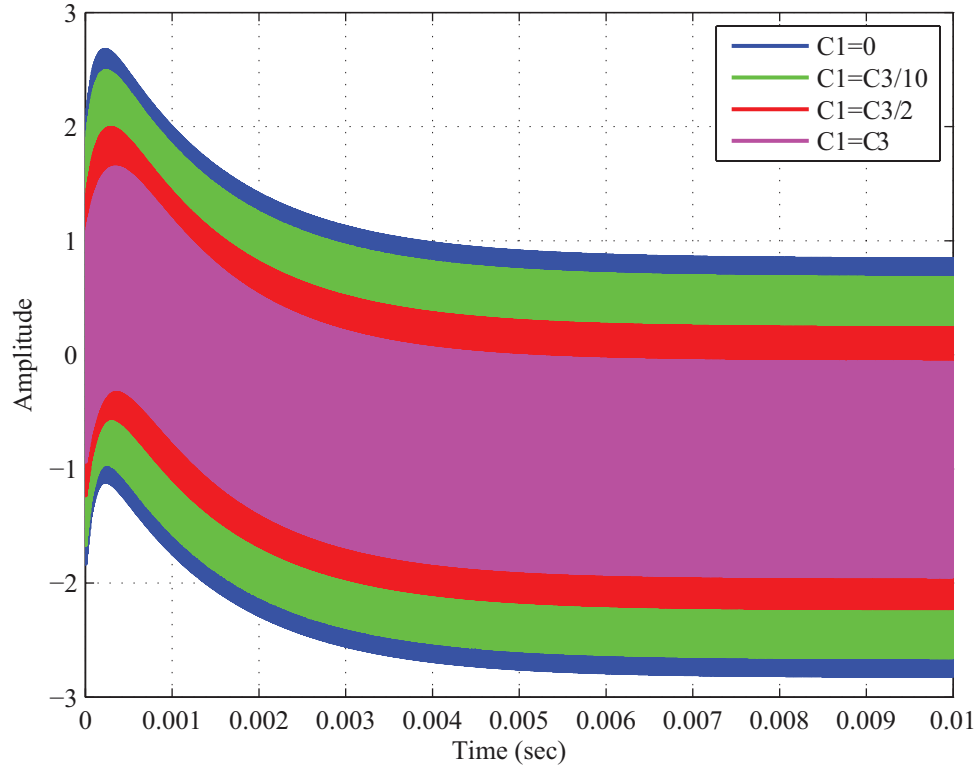


(d) Simulated circuit open-loop frequency response, $D = 0.5$.

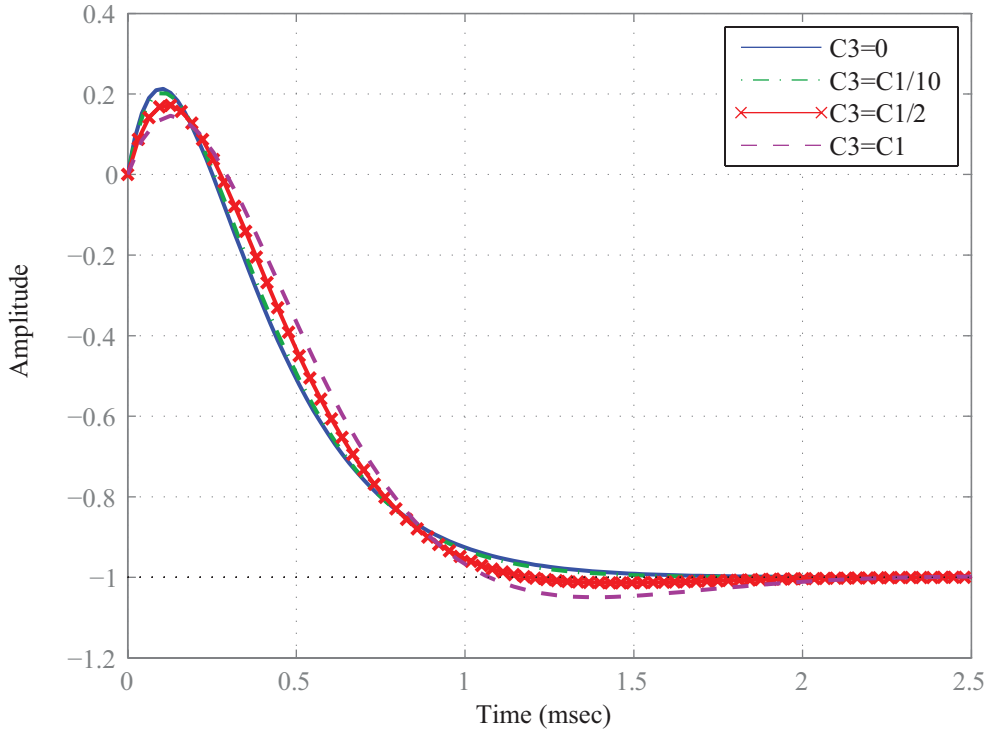
Figure 3.17: Frequency responses for step-down-step-up configuration with positive reference.



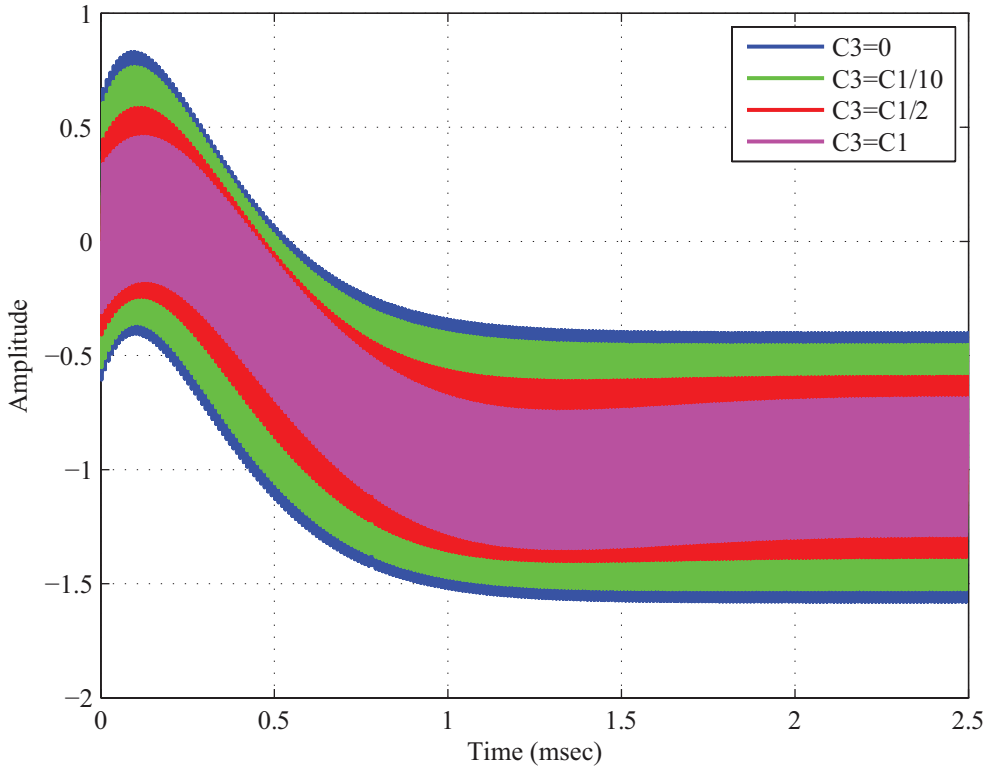
(a) Transfer function step response, $D = 0.25$.



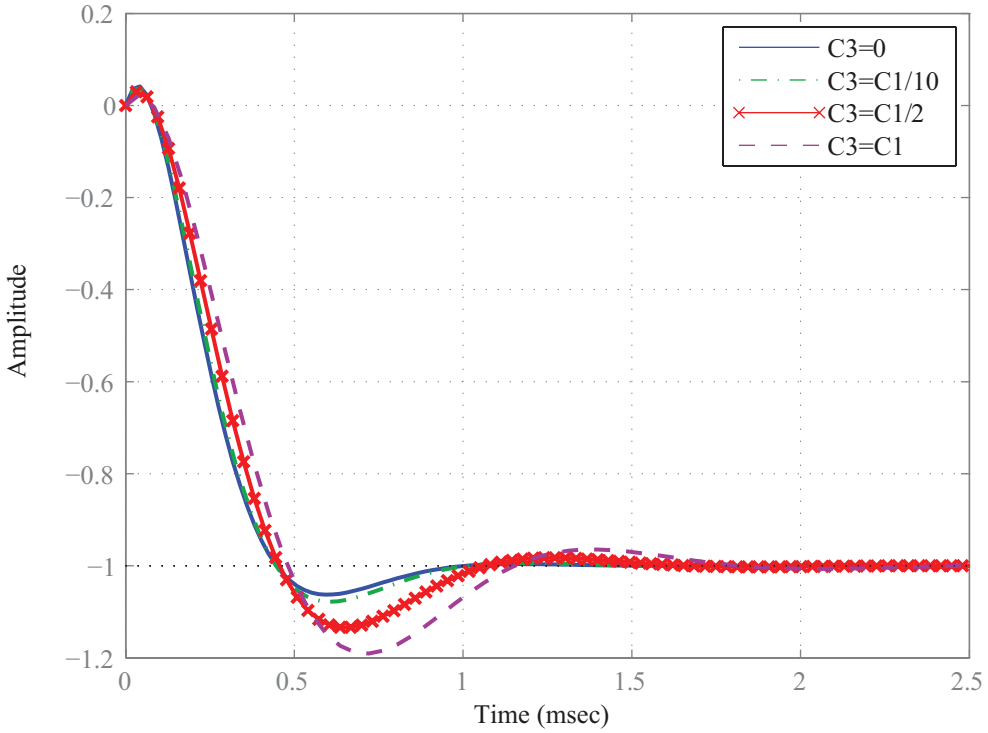
(b) Simulated circuit open-loop step response, $D = 0.25$.



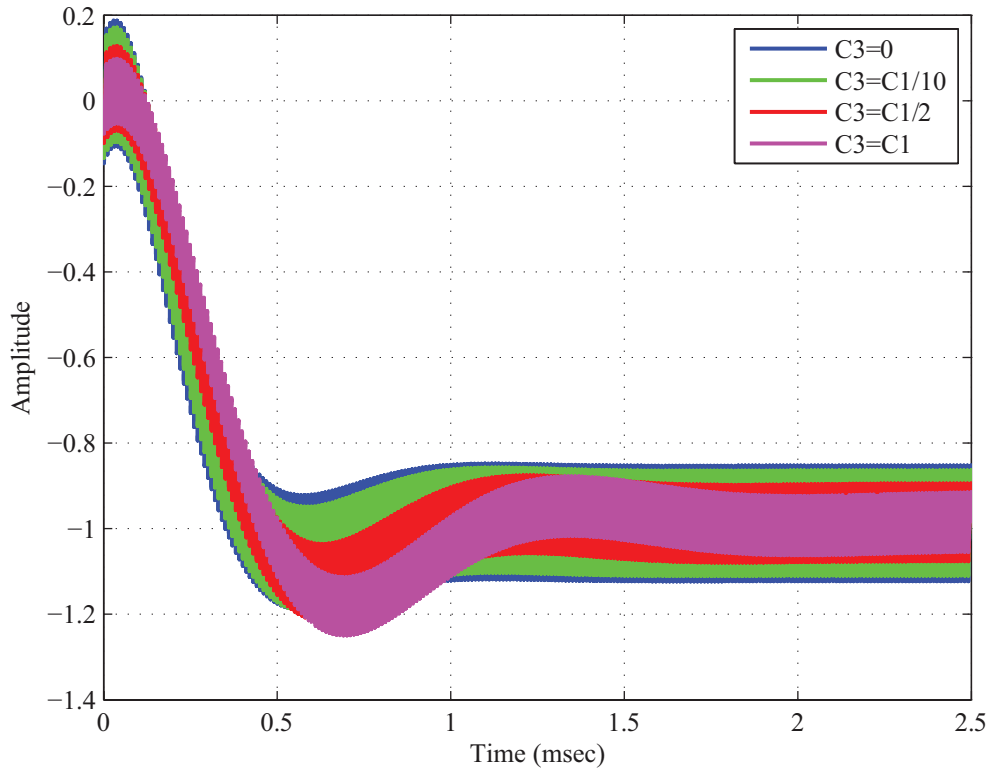
(c) Transfer function step response, $D = 0.5$.



(d) Simulated circuit open-loop step response, $D = 0.5$.



(e) Transfer function step response, $D = 0.75$.



(f) Simulated circuit open-loop step response, $D = 0.75$.

Figure 3.18: Step responses for step-down-step-up configuration with positive reference.

The transfer function and the simulated circuit show similar behaviours. This confirms the small-signal analysis and its results as a good approach to model the Topology Zero.

The inclusion of the capacitance C_3 alters the cutoff frequency, as expressed by

$$f_0 = \frac{D}{2\pi\sqrt{L\left(C_1 + C_3\right)}} \tag{3.73}$$

The effects of the root shift are seen in the frequency and step responses. When C_3 increases, the cutoff frequency decreases. Additionally, the dynamic response is affected by the RHZ and the duty cycle in steady-state. The frequency of the RHZ is expressed by

$$f_z = \frac{D^2 R}{2\pi D' L} \tag{3.74}$$

In the magnitude response (Figure 3.17), for higher values of steady-state duty cycle there is a peak in the gain near the cutoff frequency. The peak reduces when D decreases. The step response changes from overdamped to underdamped when D varies form lower to higher values (Figure 3.18). The influence of the RHZ is observed, as well; the output goes initially in opposite direction of the final value when the duty cycle step happens.

The responses for the Topology Zero in step-down-step-up configuration show similarities between positive and negative reference. Both transfer functions have gain and singularities affected by the steady-state of the converter, as well, by the sum of the capacitances. In addition, the output voltage changes in opposite form for either of the configurations when a step in duty cycle is applied. The step-down-step-up configuration has a right-half plane zero in the transfer functions of both negative and positive reference. The influence of the RHZ is manifested in similar form as in the step-up configuration, when a step in the control input occurs, initially the output voltage goes in opposite direction of the final value, that is afterwards reached.

3.4 Summary

This chapter continued the analysis of the Topology Zero started in Chapter 2. However, the focus here was on its dynamic response. The small-signal derivation showed how is possible to model the Topology Zero in all its configurations, and how the basic known topologies are special cases of the Topology Zero, proving that one single circuit can cover the whole basic configuration spectrum. In addition, some peculiarities in the transfer functions are mentioned such as the RHZ which needs to be specially considered when control strategies

are to be designed. As well, in the circuit simulations, the ripple variation can be observed as a function of the additional capacitance.

In the next chapter, the ideal switch is replaced by realistic semiconductor components and a broad set of configurations of the Topology Zero are explored. Additionally, an introduction of power losses is given for the basic conversion configurations.

Chapter 4

Topology Zero: Possible Configurations and Power losses

In previous chapters the electric components of the Topology Zero were considered ideal for all the analyses. More realistic elements are introduced in this chapter. First, the switch is replaced by switching semiconductors. This broaden the possible configurations for the Topology Zero. Afterwards, passive components are considered non-ideal, and power losses analysis is introduced for different configurations of the Topology Zero to fulfill the theoretical study of this topology.

4.1 Topology Zero Possible Configurations

The basic configurations analysed in previous chapter are reconsidered here replacing the switch by switching semiconductors. As well as, in addition to the multiple topologies that derive from the Topology Zero, two additional configurations are described. The switching semiconductors that replace the ideal switch can be two transistors or one transistor and one diode. The schematic of the implementation of the switch with semiconductors is shown in Figure 4.1.

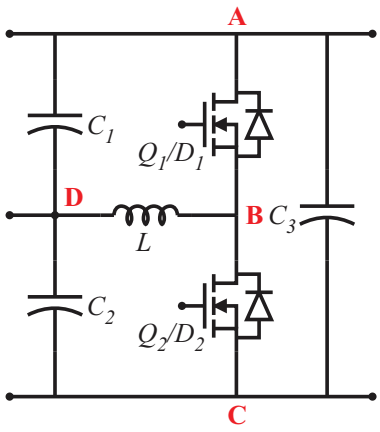


Figure 4.1: Topology Zero schematic implemented with MOSFETs.

The schematic is implemented with two metaloxidesemiconductor field-effect transistor (MOSFET) that have built-in diodes in the devices. Thus, if the transistors are both controlled, they act as transistors and the configuration operates in synchronous mode. On the other hand, if only one of the transistor is controlled, the other one acts as diode, and the configuration operates in asynchronous mode. Which transistor is controlled in asynchronous mode depends on the selected configuration. Next, possible configurations of the Topology Zero are explored.

4.1.1 Topology Zero Step-down Configurations

The Topology Zero step-down configurations implemented with switching semiconductors permit some variations in the topology operation and control. Two groups can be first defined according to the reference, negative and positive reference configurations, as stated previously. The Topology Zero step-down configuration with negative reference group can, in turn, be divided into synchronous and asynchronous modes of operation.

The Topology Zero step-down configuration with negative reference in synchronous mode requires the two transistors switching in complementary mode. In this category, some options can be identified: the step-down configuration and a special case where the capacitance C_1 is set to 0F, resulting in a synchronous buck converter. If the Topology Zero step-down configuration with negative reference operates in asynchronous mode, only the transistor Q_1 is controlled for switching and, the diode D_2 conducts when is forward biased. An asynchronous configuration is much simpler to control and to physically implement than a

synchronous version, resulting in an acceptable cost efficient end product. The configurations that can be identified in asynchronous mode are the step-down configuration and a special case with C_1 set to 0F, the buck converter in asynchronous mode.

The Topology Zero step-down configuration with positive reference in synchronous mode employs the two transistors switching in complementary fashion. The options that can be identified in synchronous mode are the step-down configuration and a special case where the capacitance C_2 is set to 0F. This configuration could be called synchronous inverted buck converter, for the analogy to the known topology. When the Topology Zero step-down configuration with positive reference operates in asynchronous mode, the conduction of the transistor Q_2 is controlled and, the diode D_1 conducts if it is forward biased. The options in this operating mode are the step-down and a special case that could be called asynchronous inverted buck converter.

The Topology Zero step-down configurations above mentioned are summarised in Figure 4.2.

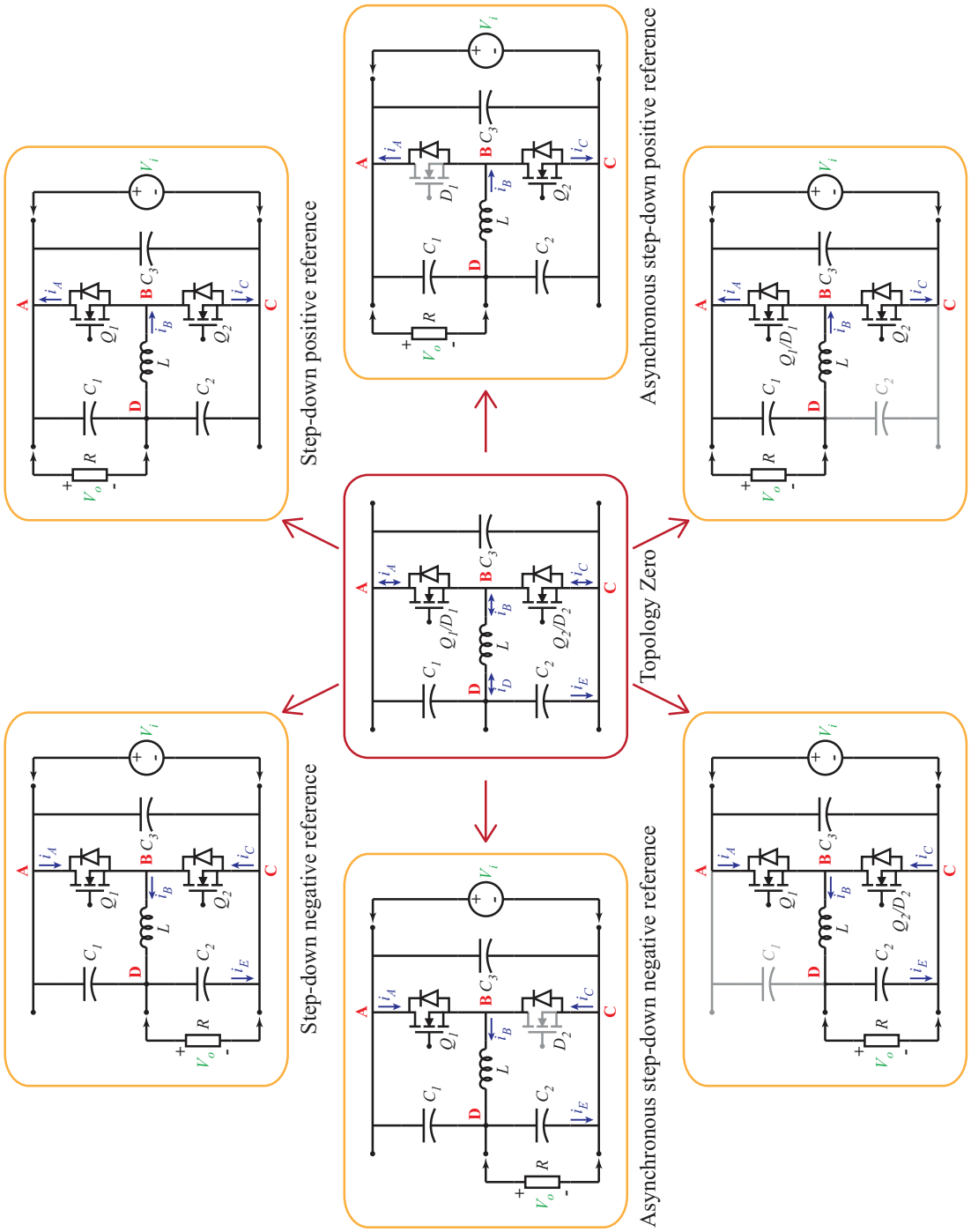


Figure 4.2: Step-down configurations implemented with the Topology Zero.

4.1.2 Topology Zero Step-up Configurations

Some variations in operation and control can be acquired for the Topology Zero step-up configurations implemented with switching semiconductors. The negative and positive reference groups can be defined. The Topology Zero step-up configuration with negative reference group can, in turn, be divided into synchronous and asynchronous modes of operation.

In synchronous mode, the configuration requires the two transistors switching in complementary mode. The variations that can be found in this operation mode are the Topology Zero step-up configuration with negative reference and a special case where the capacitance C_1 is set to 0F, the synchronous boost converter. If the Topology Zero step-up configuration with negative reference operates in asynchronous mode, only the switching of the transistor Q_2 is controlled and, the diode D_1 conducts when is forward biased. The configurations included in the asynchronous mode category are the step-up configuration and a special case with C_1 set to 0F, the boost converter in asynchronous mode.

The Topology Zero step-up configuration with positive reference in synchronous mode employs the two transistors switching in complementary mode. The options in synchronous mode are the step-up configuration and a special case where the capacitance C_2 is set to 0F. This configuration could be called synchronous inverted boost converter, for the analogy to the known topology. When the Topology Zero step-up configuration with positive reference operates in asynchronous mode, only the conduction of the transistor Q_1 is controlled and, the diode D_2 conducts if it is forward biased. The options in this operating mode are the step-up and a special case that could be called asynchronous inverted boost converter, when C_2 is set to 0F.

The Topology Zero step-up configurations above enumerated are summarised in Figure 4.3.

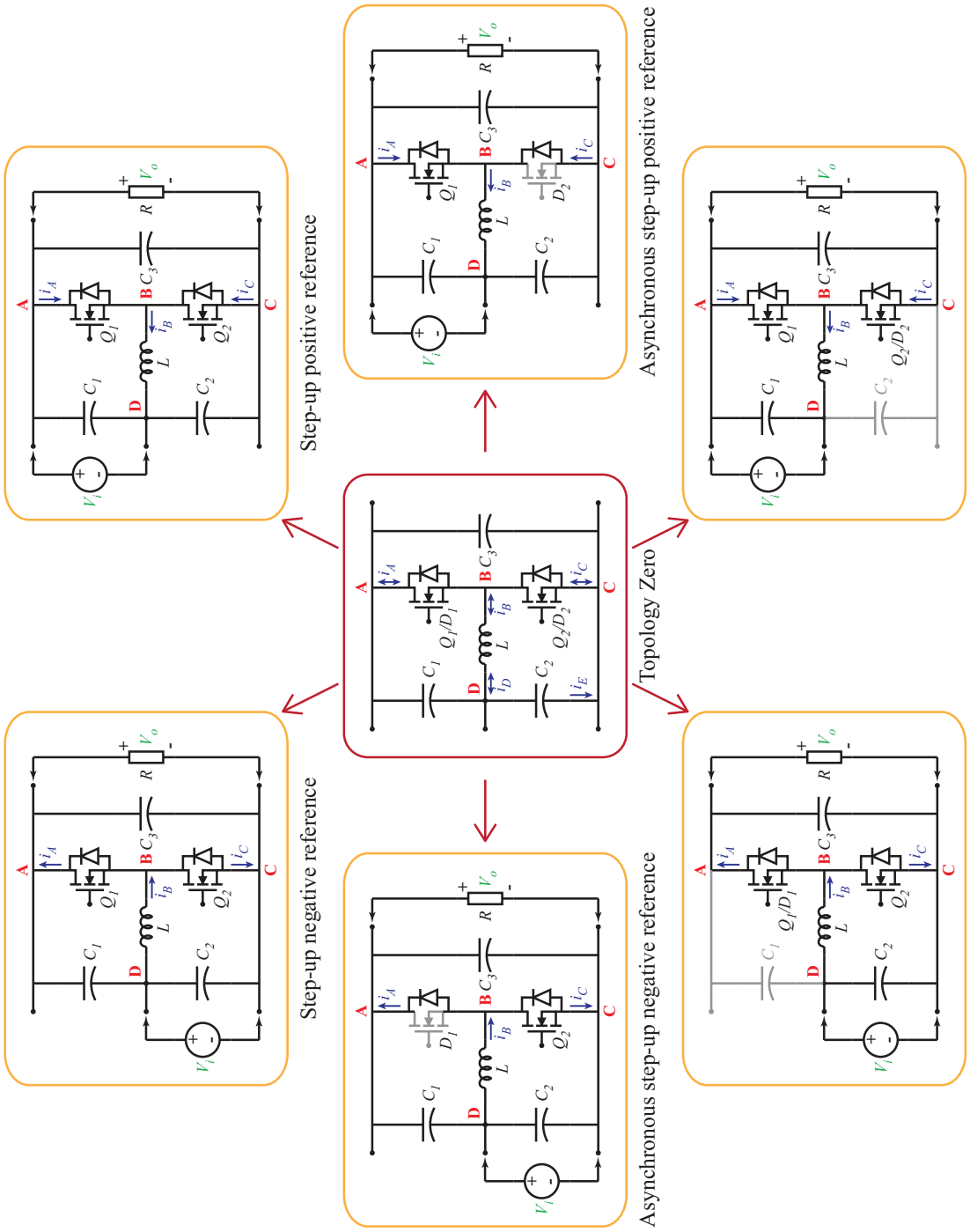


Figure 4.3: Step-up configurations implemented with the Topology Zero.

4.1.3 Topology Zero Step-down-step-up Configurations

The Topology Zero step-down-step-up configurations implemented with switching semiconductors can be categorized in similar form as the other two basic types of configurations. The negative and positive reference groups can be defined. The Topology Zero step-down-step-up configuration with negative reference group can be classified into synchronous and asynchronous modes.

The Topology Zero step-down-step-up configuration with negative reference in synchronous mode operates with the two transistors switching in complementary mode. In this group the options identified are the step-down-step-up configuration and a special case where the capacitance C_3 is set to 0F, the synchronous buck-boost converter. If the Topology Zero step-down-step-up configuration with negative reference operates in asynchronous mode, only the switching action of the transistor Q_1 is controlled and, the diode D_2 conducts when is forward biased. The configurations that can be distinguished in asynchronous mode are the step-down-step-up configuration and a special case with C_3 set to 0F, the buck-boost converter in asynchronous mode.

The Topology Zero step-down-step-up configuration with positive reference in synchronous mode shows two variations: the step-down-step-up configuration and a special case where the capacitance C_3 is set to 0F. This configuration could be called synchronous inverted buck-boost converter. When the Topology Zero step-down-step-up configuration operates in asynchronous mode, only the conduction of the transistor Q_2 is controlled and, the diode D_1 conducts if it is forward biased. The options in this operating mode are the step-down-step-up and a special case that could be called asynchronous inverted buck-boost converter, when C_3 is set to 0F.

Figure 4.4 summarise the configurations above mentioned of the Topology Zero step-down-step-up.

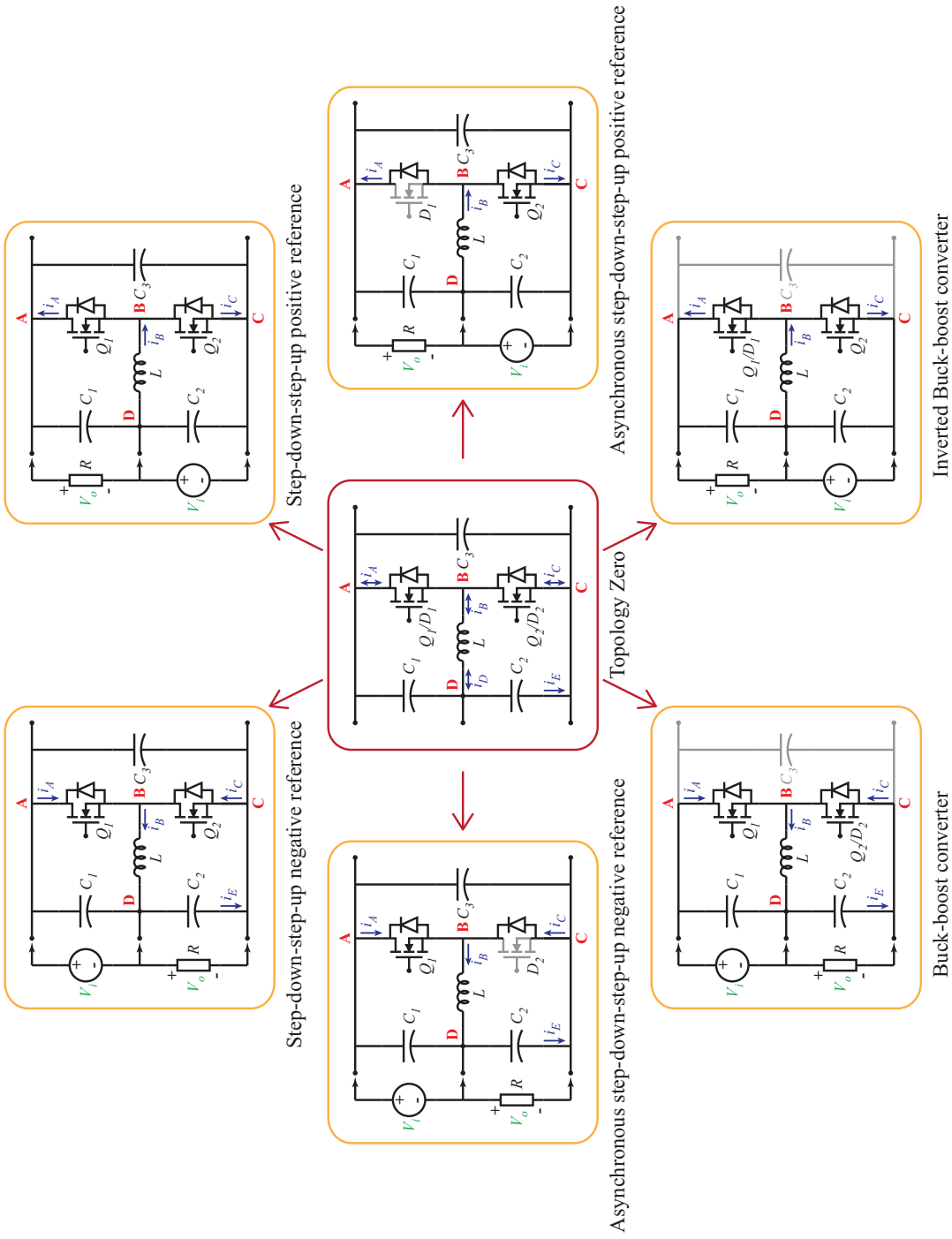


Figure 4.4: Step-down-step-up configurations implemented with the Topology Zero.

4.1.4 Topology Zero Bridge Configurations

In the physical implementation of the Topology Zero, few changes in the components allow the operation as converters other than the ones above mentioned, the half-bridge converter and the full-bridge converter.

Half-bridge converters allow to provide both AC and DC output. In this topology the two transistors are alternatively in on-state. This converter is used for DC-Motor drives, inverters and for isolated converters. Furthermore, it is able to work bidirectionally, returning energy from the load to the DC input power supply. In order to implement a half-bridge converter with the Topology Zero, the inductance needs to be replaced for a load.

Full-bridge converters have similar applications to the half-bridge. However, they employ 4 switches, which allows to have more control in the operation as a converter. The drawback of this type of converters is the complexity in driving the switches. To implement a full-bridge converter, two replicas of the Topology Zero are interconnected and their inductances need to be removed.

In Figure 4.5 the bridge configurations of the Topology Zero are shown.

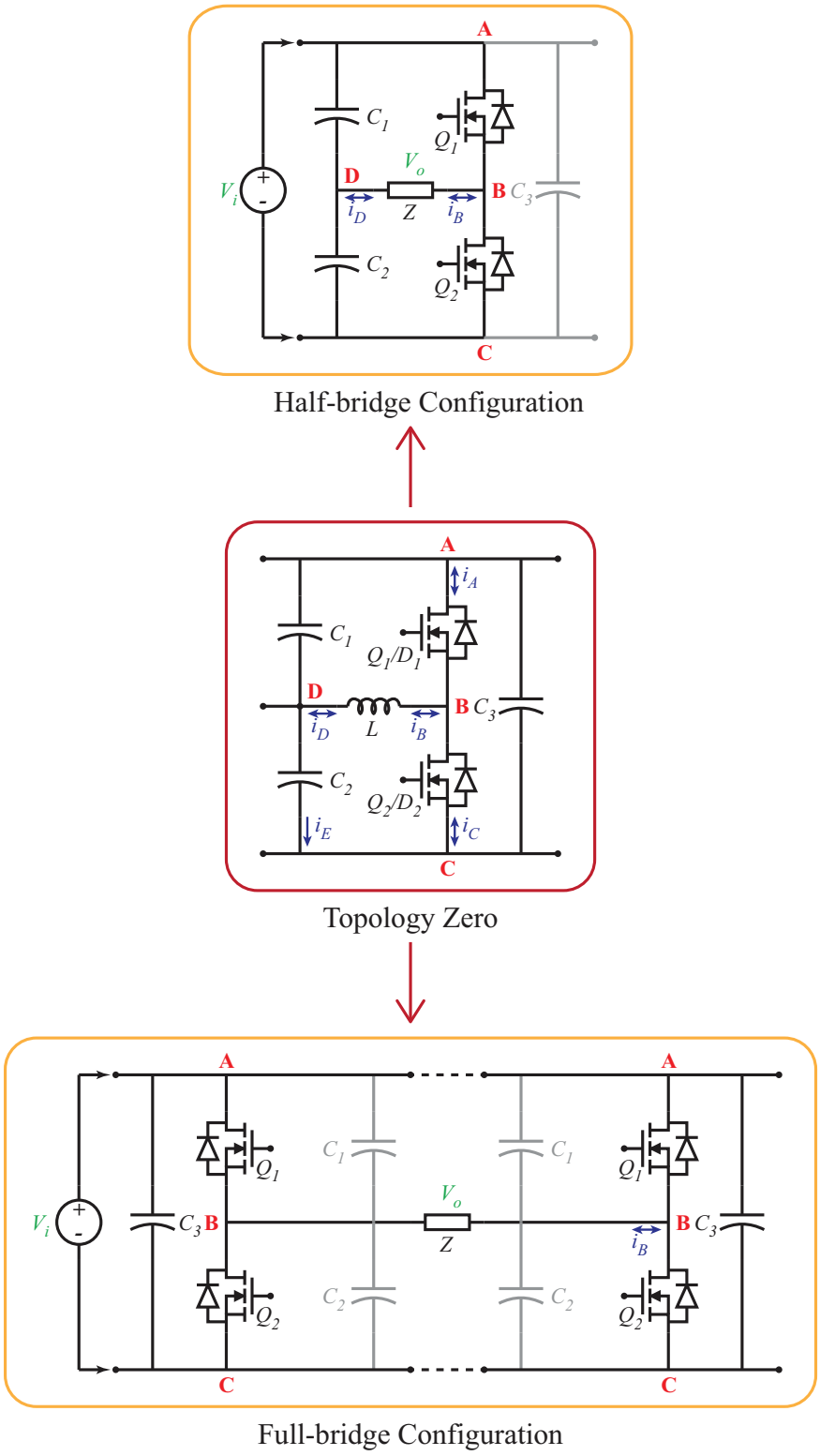


Figure 4.5: Bridge configurations implemented with the Topology Zero.

4.2 Topology Zero Power Losses

Real circuits have not ideal elements. Previously, real switches have been introduced to replace the ideal switch. However, passive components are neither ideal. Real elements produce losses that are manifested as heat. Next, resistive losses in the inductor and conduction semiconductor losses are considered. The latter contemplate the configuration working in asynchronous and in synchronous modes.

Inductors are winded with wire that has an associated resistance. Thus, a simple equivalent circuit for a non-ideal inductor can be thought as series connection of ideal inductance L and parasitics resistance R_L. The conduction power loss in a MOSFET is given by its on resistance R_{on}. An equivalent circuit that takes into account a diode conduction power loss is a series connection of a voltage drop and resistance R_D [22]. All these circuits are shown in Figure 4.6

(a) Equivalent circuit of a non-ideal inductor.

(b) Equivalent circuit of a MOSFET in *on* state.

(c) Equivalent circuit of a diode in *on* state.

Figure 4.6: Equivalent circuits for non-ideal components.

4.2.1 Inductor Losses in Step-down Configuration

Losses in the inductor for the Topology Zero in step-down configuration with negative reference as shown in Figure 4.7 are next considered.

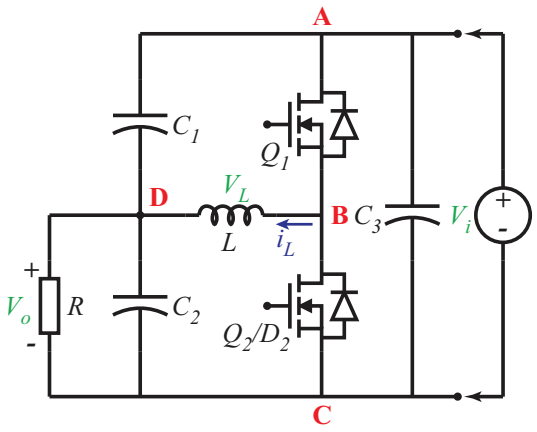


Figure 4.7: Step-down configuration.

Its transfer ratio can be written as

$$\frac{V_o}{V_i} = \frac{1}{D}\frac{1}{1+\frac{R_L}{D'^2R}} \tag{4.1}$$

The efficiency of this non-ideal circuit is

$$\eta = \frac{P_o}{P_i} = \frac{V_o I_L}{D V_i I_L} \tag{4.2}$$

from (4.1) and (4.2)

$$\eta = \frac{1}{1+\frac{R_L}{R}} \tag{4.3}$$

As it can be seen in (4.3), to obtain high efficiency the inductor copper loss has to be smaller than the load resistor.

How the transfer ratio of the step-down configuration is affected by the inductor resistive losses, given a load resistance, is shown in Figure 4.8

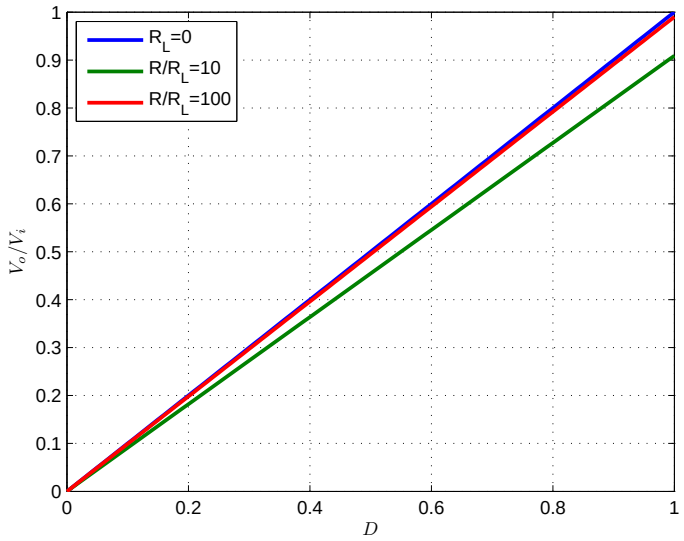


Figure 4.8: Transfer ratio considering different relationship between load resistance and resistive copper losses.

4.2.2 Semiconductor Losses in Step-down Configuration

4.2.2.1 Transitor and Diode Losses

Consider the Topology Zero in step-down configuration shown in Figure 4.7 working in asynchronous mode. The output voltage equation accounting conduction losses in the transistor and the diode, as well as the inductor copper loss, is given by

$$V_o = DV_i\left(1 - \frac{D'V_{D2}}{DV_i}\right)\frac{1}{1 + \frac{R_L + DR_{on1} + D'R_{D2}}{R}} \tag{4.4}$$

From (4.2) and (4.4), the efficiency of a step-down configuration, considering conduction and copper losses, can be expressed as

$$\eta = \frac{1 - \frac{D'V_{D2}}{DV_i}}{1 + \frac{R_L + DR_{on1} + D'R_{D2}}{R}} \tag{4.5}$$

High efficiency can be obtained if $DV_i \gg D'V_{D2}$ and $R \gg R_L + DR_{on1} + D'R_{D2}$

4.2.2.2 Transistors Losses

If the Topology Zero is operating in synchronous mode, that is, two transistors are used as switches, the output voltage can be expressed as

$$V_o = DV_i \frac{1}{1 + \frac{R_L + DR_{on1} + D'R_{on2}}{R}} \tag{4.6}$$

If the transistors are similar, then $R_{on1} = R_{on2} = R_{on}$ and (4.6) becomes

$$V_o = DV_i \frac{1}{1 + \frac{R_L + R_{on}}{R}} \tag{4.7}$$

The efficiency is expressed as

$$\eta = \frac{1}{1 + \frac{R_L + R_{on}}{R}} \tag{4.8}$$

In order to obtain high efficiency the parasitics resistances have to be kept low.

4.2.3 Inductor Losses in Step-up Configuration

Losses in the inductor for the Topology Zero in step-up configuration with negative reference as shown in Figure 4.9 are analysed next.

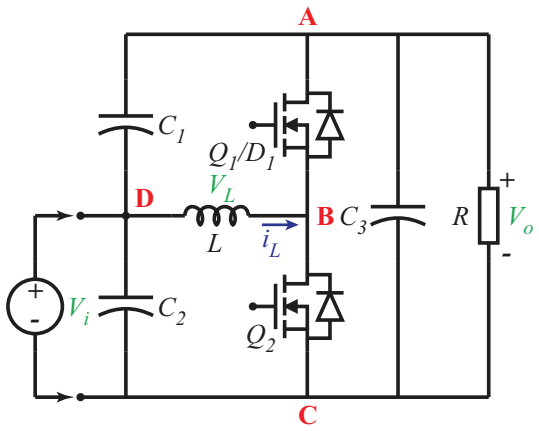


Figure 4.9: Step-up configuration.

The transfer ratio considering the losses in the inductor is

$$\frac{V_o}{V_i} = \frac{1}{D} \frac{1}{1 + \frac{R_L}{D^2 R}} \tag{4.9}$$

The efficiency under this configuration is

$$\eta = \frac{P_o}{P_i} = \frac{DV_oI_L}{V_iI_L} \tag{4.10}$$

Combining (4.9) and (4.10)

$$\eta = \frac{1}{1 + \frac{R_L}{D^2R}} \tag{4.11}$$

In order to obtain high efficiency, the inductor copper resistance has to be low.

How the transfer ratio of the step-up configuration is affected by the inductor resistive losses, given a load resistance, is shown in Figure 4.10.

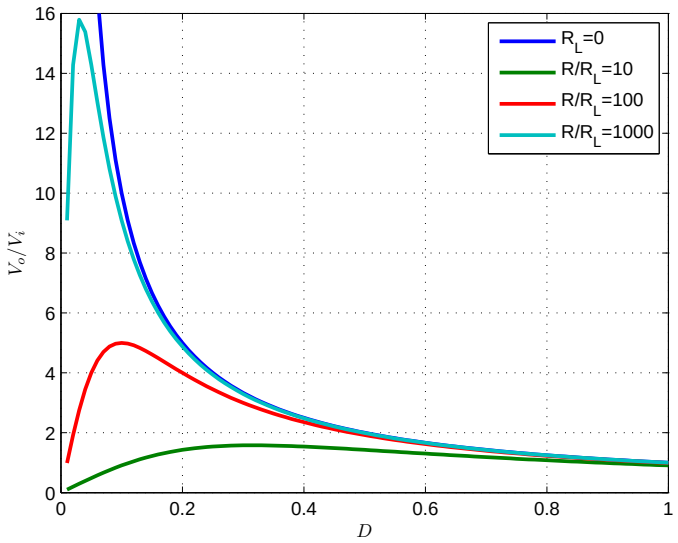


Figure 4.10: Transfer ratio considering different relationship between load resistance and resistive copper losses.

4.2.4 Semiconductor Losses in Step-up Configuration

4.2.4.1 Transistor and Diode Losses

Consider the Topology Zero in step-up configuration shown in Figure 4.9 working in asynchronous mode. The output voltage equation accounting conduction losses in the transistor and the diode, as well as the inductor copper loss, is given by

$$V_o = \frac{V_i}{D}\left(1 - \frac{DV_{D1}}{V_i}\right)\frac{1}{1 + \frac{R_L + DR_{D1} + D'R_{on2}}{D^2R}} \tag{4.12}$$

Using (4.10) and (4.12), the efficiency of the step-up configuration is expressed as

$$\eta = \frac{1 - \frac{DV_{D1}}{V_i}}{1 + \frac{R_L + DR_{D1} + D'R_{on2}}{D^2R}} \tag{4.13}$$

High efficiency can be obtained if $\frac{V_i}{D} \gg V_{D1}$ and $D^2R \gg R_L + DR_{D1} + D'R_{on2}$. Taking into account that $\frac{V_i}{D} = V_o$ for an ideal circuit, it can be said that the voltage across the diode should be much lower than the output voltage.

4.2.4.2 Transistors Losses

If the Topology Zero is operating in synchronous mode, the output voltage can be described as

$$V_o = \frac{V_i}{D} \frac{1}{1 + \frac{R_L + DR_{on1} + D'R_{on2}}{D^2R}} \tag{4.14}$$

If the transistors are similar, then $R_{on1} = R_{on2} = R_{on}$ and (4.14) becomes

$$V_o = \frac{V_i}{D} \frac{1}{1 + \frac{R_L + R_{on}}{D^2R}} \tag{4.15}$$

The efficiency under this configuration is

$$\eta = \frac{1}{1 + \frac{R_L + R_{on}}{D^2R}} \tag{4.16}$$

In order to obtain high efficiency the parasitics resistances have to be kept low. A consideration about this converter is that the efficiency is affected by the duty cycle.

4.2.5 Inductor Losses in Step-down-step-up Configuration

Losses in the inductor for the Topology Zero in step-down-step-up configuration with negative reference as shown in Figure 4.11 are analysed next.

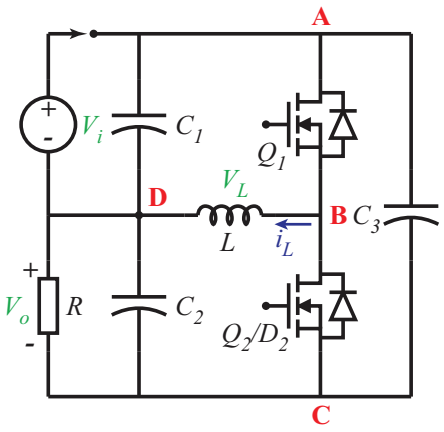


Figure 4.11: Step-down-step-up configuration.

The transfer ratio considering the losses in the inductor is

$$V_o = \frac{DV_i}{D'} \frac{1}{1 + \frac{R_L}{D'^2 R}} \tag{4.17}$$

The efficiency for this setup is given as

$$\eta = \frac{P_o}{P_i} = \frac{D'V_o I_L}{DV_i I_L} \tag{4.18}$$

Incorporating (4.17) into (4.18)

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}} \tag{4.19}$$

In order to obtain high efficiency, the inductor copper resistance has to be low.

How the transfer ratio of the step-down-step-up configuration is affected by the inductor resistive losses, given a load resistance, is shown in Figure 4.12.

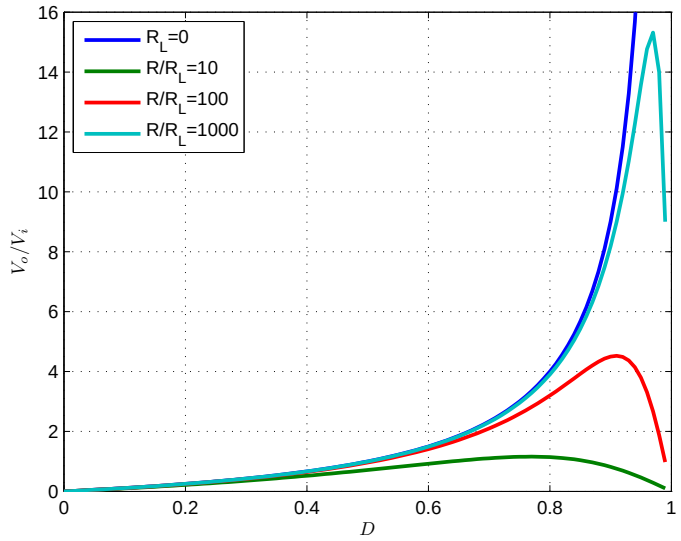


Figure 4.12: Transfer ratio considering different relationship between load resistance and resistive copper losses.

4.2.6 Semiconductor Losses in Step-down-step-up Configuration

4.2.6.1 Transitor and Diode Losses

Consider the Topology Zero in step-down-step-up configuration shown in Figure 4.11 working in asynchronous mode. The output voltage equation accounting conduction losses in the transistor and the diode, as well as the inductor copper loss, is given by

$$V_o = \frac{DV_i}{D'}\left(1 - \frac{D'V_{D2}}{DV_i}\right)\frac{1}{1 + \frac{R_L + DR_{on1} + D'R_{D2}}{D'^2R}} \tag{4.20}$$

Then, using (4.18) and (4.20), the efficiency of a step-down-step-up configuration results in

$$\eta = \frac{1 - \frac{D'V_{D2}}{DV_i}}{1 + \frac{R_L + DR_{on1} + D'R_{D2}}{D'^2R}} \tag{4.21}$$

To achieve high efficiency, $\frac{DV_i}{D'} \gg V_{D2}$ and $D'^2R \gg R_L + DR_{on1} + D'R_{D2}$. Taking into account that $\frac{DV_i}{D'} = V_o$ for an ideal circuit, it can be assumed that the voltage across the diode should be much lower than the output voltage.

4.2.6.2 Transistors Losses

If the Topology Zero is operating in synchronous mode, the output voltage is expressed as

$$V_o = \frac{DV_i}{1-D}\frac{1}{1+\frac{R_L + DR_{on1} + D'R_{on2}}{D'^2R}} \tag{4.22}$$

If the transistors are similar, then $R_{on1} = R_{on2} = R_{on}$ and (4.22) becomes

$$V_o = \frac{DV_i}{1-D}\frac{1}{1+\frac{R_L + R_{on}}{D'^2R}} \tag{4.23}$$

The efficiency is expressed as

$$\eta = \frac{1}{1+\frac{R_L + R_{on}}{D'^2R}} \tag{4.24}$$

In order to obtain high efficiency the parasitics resistances have to be kept low. Like the step-up configuration, the efficiency is affected by the duty cycle. If the losses are considerable, it is possible that the converter fails in providing the output estimated.

The analysis given for losses only considered conduction losses in the semiconductors and resistive losses in the inductor. However, A thorough loss analysis would include switching losses, skin effect, saturation of the core, parasitics in the capacitors and layout parasitics, among others. These considerations were kept out of the scope of this analysis, to maintain a simple study of the losses and at the same time give insight into the actual converter characteristic. Equivalent results can be obtained for the configurations of the Topology Zero with positive reference.

4.3 Summary

In this chapter real switching components were introduced. The basic converter topologies can be thoroughly implemented by using the Topology Zero with real components. Few small changes need to be done in the original topology to easily implement the half-bridge and the full-bridge converters. Additionally, an introduction to power losses for the Topology Zero was given considering inductor and semiconductor conduction losses.

The next chapter describe the actual system designed to implement the Topology Zero. Additionally, some application examples using this valuable educational/research tool are presented.

Chapter 5

Educational Setup Implementation Based on the Topology Zero

The implemented power converter includes several functions in order to provide the output power within specifications of voltage, current and transient response, as well as, fault protection and communication with other devices. The system implemented is intended to be modular for adding flexibility in the applications. The basic setup is formed by a power supply, the Control and Communication Platform (CCP), the Topology Zero Platform (TZP) and the load to be attached. Figure 5.1 shows the control of one or more TZP by the CCP and the communication amongst CCPs through serial communication protocols.

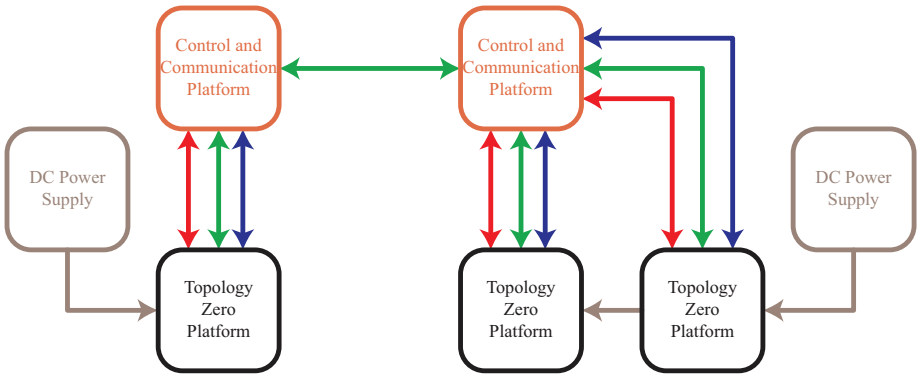


Figure 5.1: Power system diagram.

Next, the conforming components of the power system are explained.

5.1 Control and Communication Platform (CCP)

The CCP is the main component of the power system. Its functions are adapt the level of analog signals to the controller level, isolate digital communication and protection signal to prevent malfunctioning in the system, and to drive PWM signals for the TZPs. In addition, other tasks are realized in the CCP, such as implementing the control algorithms into the TZP, processing the measurements from the TZP, attending any fault condition in a TZP and proceed accordingly, and taking care of any communication with other CCP or a computer. Figure 5.2 shows a diagram of the components of the CCP.

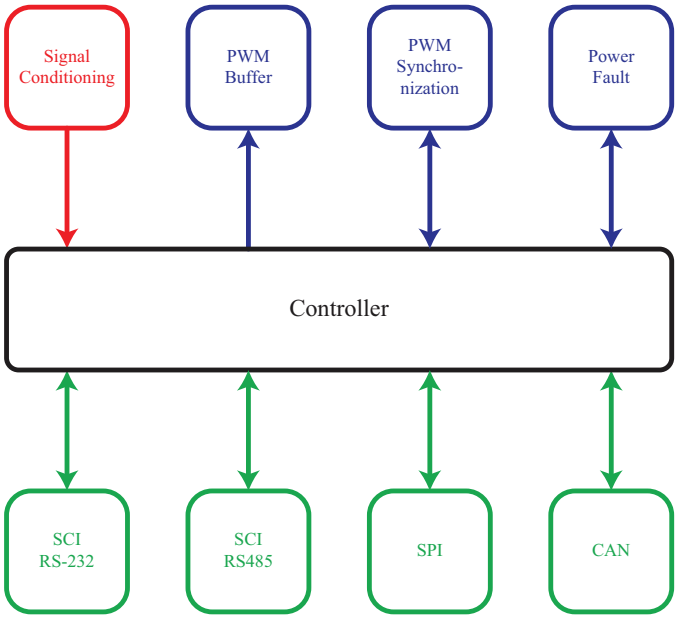


Figure 5.2: Control and Communication Platform (CCP).

What follows is the explanation of the submodules that conform the CCP.

A power supply stage provides filtered and regulated electrical energy to the different components of the CCP. The provision of power is split into two power supplies, analog and digital. The analog circuitry, composed of the signal conditioning, needs low noise power source in order to prevent adding extra noise to the signal processed. Digital circuitry are prone to generate more noise and less susceptible to noise than the analog stage; thus, it has independent voltage regulators and capacitor filters. In addition, the grounds of both subcircuits are only connected at the unregulated input voltage point to keep the digital

noise from affecting the analog stage.

The controller is the core section of the entire system. The controller is a Texas Instrument C28xx family digital signal processor (DSP) that has the program code in it; which is responsible to process the data coming form the readings in the power converter through the signal conditioning, put this numbers in the control algorithm and calculate and send the next PWM output to the TZPs. In addition, it has to look after any fault condition occurred in any TZP and proceed to the shut down of the converters to prevent any damage, and to keep communication with other CCPs in the case they are working in synchronous operation or with any computer with which the CCP is sharing information.

The function of the signal conditioning module is to adapt the level of the signal of the different sensors in the TZPs to levels that can be applied into the analog to digital converter (ADC) of the controller. It also has to limit the frequency bandwidth to comply with the Nyquist sampling theorem and to keep non-desired frequencies from enter the system. These operations have to be performed without losing key information of the measurement nor adding significant delay. If either occurs, it will provide false information to the control algorithm and result in erroneous functioning of the converter.

The pulse width modulation (PWM) stage is one of the most important components of any power converter. The signals generated by it command the opening or closure state of the switches in the power stage. The PWM signals are generated by the controller and they need to be transmitted to the TZPs. In addition, synchronization may be needed among CCPs, thus, the controller that operates as master has to send that signal and the ones that act as slaves, receive it and synchronize with the master. Any fault condition generated in a converter needs to be known by the controllers. Hence, a protection circuitry has to cover this necessity. The PWM buffer module of the CCP separates the outputs of the controller, that does not have high current capacity, from the PWM inputs of the TZPs. In this part of the platform the signal is converted into differential to allow its transmission with reduced noise susceptibility. The delay that this conversion adds is minimum, otherwise it would affect considerably the correct operation of the system. The main function of the PWM synchronization module is to isolate and buffer the signals to synchronize PWM among CCPs, in the case they are working in synchronous mode. One of the CCP acts as a master and send the synchronism signal to other CCPs acting as slaves, which in turn, receive it through optical isolators and their PWM modules can be synchronized. Delay time is kept below 20ns in the circuitry. The power fault module, receives and transmits any fault signal

generated by an anomaly in the power converter. The signals can be received from the signal conditioning, from a TZP or from another CCP. The last two signals are connected through optoisolators for protection. The signal generated are sent to the controller and/or can be sent to other components of the system (CCP or TZP).

The communication stage of the CCP implements several protocols to facilitate the connection with sensors, computer or other CCPs. The protocols supported are serial communication interface (SCI) (RS-232 and RS-485), serial peripheral interface (SPI) and controller area network (CAN). The SCI module can hold communication using both RS-232 and RS-485 protocols. The circuitry needed for each of them is included in the system providing isolation to prevent damage in case of any external voltage disruption. The SPI module of the CCP provides isolation for this point-to-point high speed communication protocol. The main use of this communication channel is to have fast connectivity between two CCPs that need to share information. The CAN module allows communication with different sensors and controllers. The main features of this protocol are the speed of communication and length of the network, up to 1Mbit/s below 40m extension. In addition, it allows multinode communication with priority bus arbitration. Figure 5.3 shows an image of the control and communication platform.

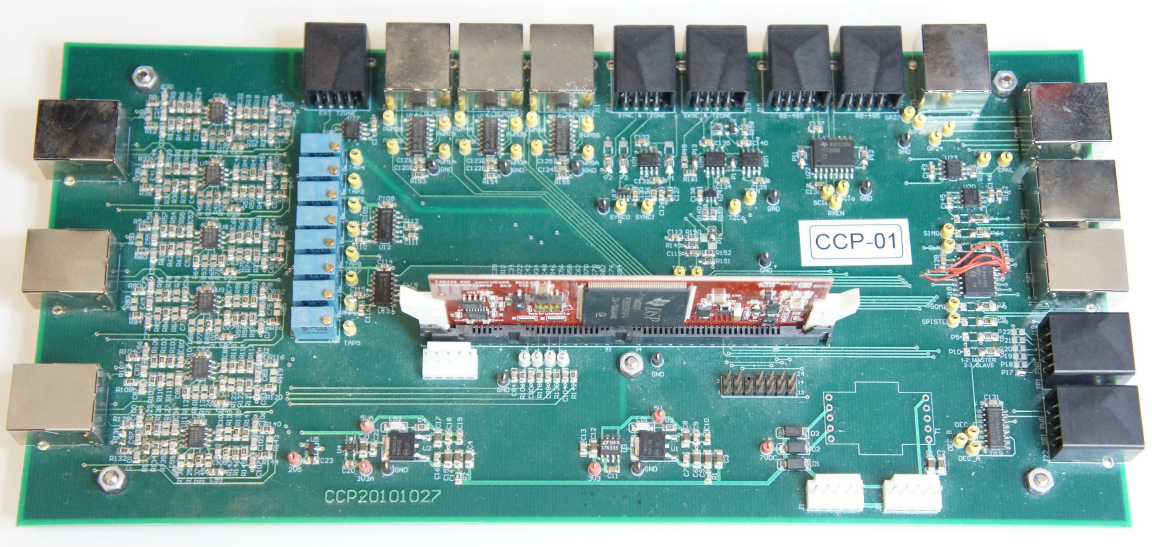


Figure 5.3: Control and Communication Platform (CCP).

5.2 Topology Zero Platform (TZP)

The Topology Zero platform has the task of providing the power to the load according to the control strategy instructed by the CCP, sending measurements back to the CCP for closed-loop operation and transmitting any detected fault condition that has been setup (if enabled in the platform).

To develop this, the platform has several subsystem with specific functions. Figure 5.4 shows a diagram of the power converter with its subsystems.

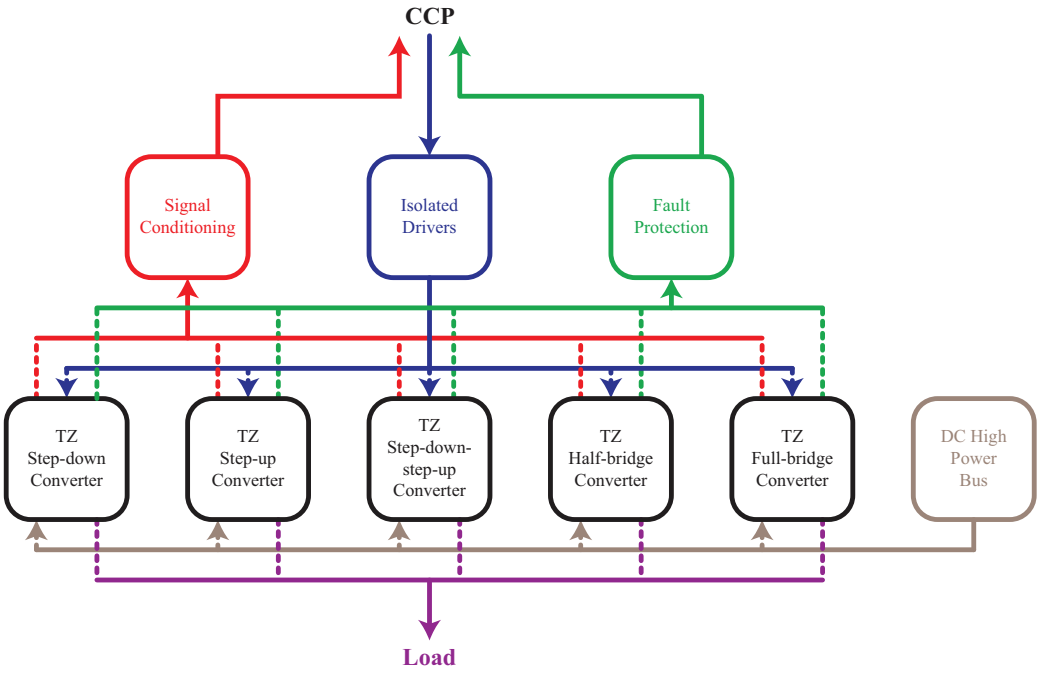


Figure 5.4: Power conversion system based on Topology Zero Platforms.

A low voltage power supply provides filtered and regulated electrical energy to the drivers receivers and to the signal conditioning stage. Additionally, through transformers, it gives power to the isolated transistor drivers. The transformer for the drivers are carefully chosen and tested in order to provide high dv/dt isolation to prevent shoot-through that can damage the power switches and associated electronics.

The signal conditioning module plays a very important role in the system. The signal conditioning stage is used for measuring current and voltage in key points of the converter and allows operating the converter in closed-loop. The latter is fundamental for testing

the system in several operation conditions, as well as, testing control strategies. The most important features of this module are low noise in the output signals, high voltage common mode rejection in the input, the accuracy in the measurement and the minimum delay. The current measurements are made by hall-effect sensors or shunt resistors. The use of shunts is preferred over hall-effect due to their lower price, higher bandwidth and more options are allowed for current range. However, shunt signal needs to be conditioned by operational amplifiers, which cannot manage high common mode measurement with acceptable accuracy and bandwidth, thus, shunt are limited to ground referenced current measurement. On the other hand, hall-effect sensors are isolated from the circuit to measure, which makes them suitable for high common mode voltage measurement. However, these closed-loop hall effect sensors have high frequency ripple in the signal output caused by their internal oscillator, the bandwidth is limited, the current range options are reduced, and they are substantially more expensive [27]. In order to add flexibility in the measurements, the TZP is designed to accept both types of sensors.

The platform counts with isolated driver module that has as a function to drive each gate of the transistors as it is commanded by CCP through the PWM signals. Each driver is connected to one transistor and has its own isolated power supply. The PWM signal is optocoupled to have the driver fully isolated. the optocoupler and the driver are chosen to allow high switching frequency with small delay, and the driver can handle high current to quickly drive the gate of the transistor and in this form reduce the switching losses.

Any fault condition that is sensed in the power converter, such as over current, short circuit or high temperature in the switches, can shut down the converter and send the fault condition to the CCP and other components of the system for them to proceed accordingly. This function is carried out by the fault protection module.

The DC bus supplies filtered DC power to the the switching devices. The power for this stage is provided by a power supply different than the aforementioned and its voltage ranges from few volts to over 300V. In addition, it has to be able to filter high current demands. For each application, capacitors have to be chosen accordingly to meet the needs of voltage and current.

The TZP is meant to provide flexibility in the research needs, adopting the topology that is required. The main feature of the platform is its versatility, which can operate as a step-down, step-up or step-down-step-up converter, the three of them in either synchronous or asynchronous mode, as well as a half-bridge inverter. The full-bridge inverter can be

implemented by coupling two boards back to back, one operates as a master, the other as a slave. In addition, several boards can be interconnected to form more complex converter topologies. Figure 5.5 shows an image of the Topology Zero Platform.

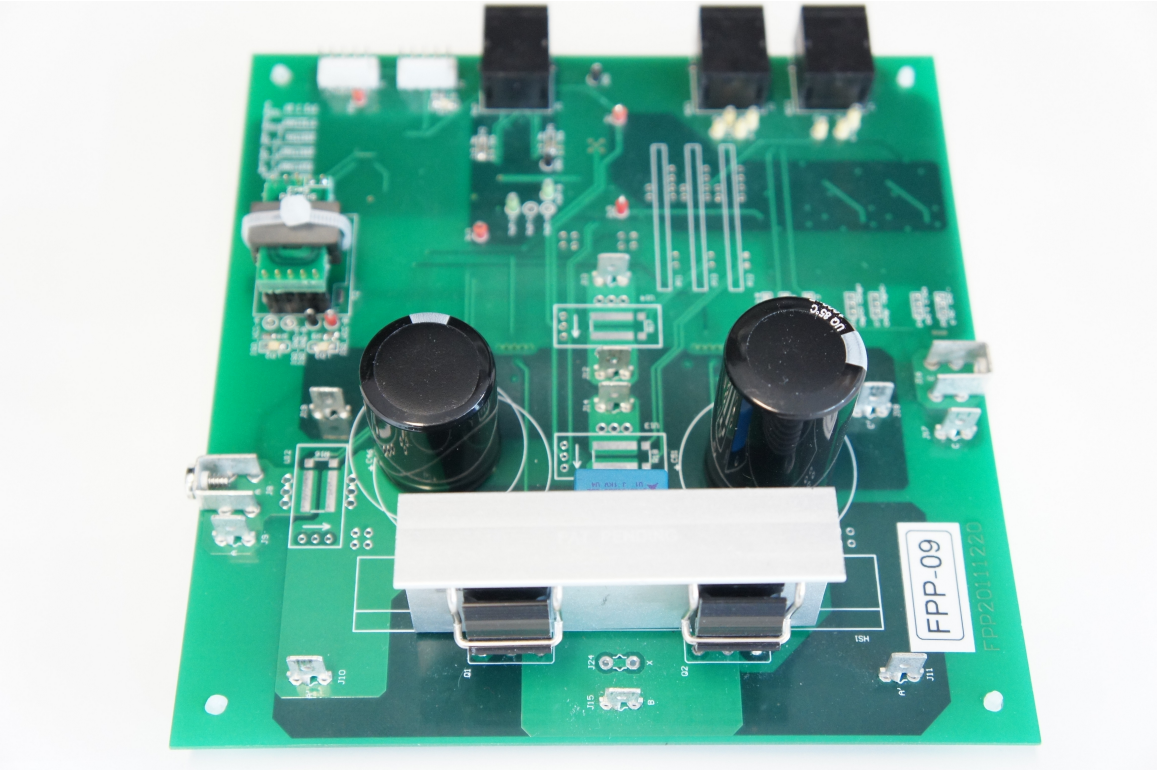


Figure 5.5: Topology Zero Platform.

5.3 Applications

The advantage of the platform is its versatility to implement different converters with a single system. Furthermore, advanced control strategies can be studied as well. In this section, some application examples of the system are mentioned.

5.3.1 Power Losses Analysis in Power MOSFET

This section explains how the power losses of a power MOSFET were evaluated using the TZP. Due to the flexibility of the setup, the valuation can be extended to other modes of operation or derived topologies. Power loss characterization and modeling are topics with

critical importance in power electronics design. The possibility of accurately estimating the total power losses enables the prediction of efficiency for different operating points and converter parameters. The ability to calculate power loss distribution allows optimizing the converter under study. Thus, higher switching frequencies can be obtained that result in higher bandwidth, improved dynamics and smaller filter components. While analytical loss models use closed-form complex mathematical equations, the analysis can be simplified by assuming a linear switching characteristic to derive loss equations. These methods yield closed-form mathematical expressions that can be used to produce optimization curves for different topologies. The main challenge of analytical modeling is to improve accuracy while minimizing complexity. One of the most popular analytical switching loss models is the piecewise linear mode. Although the losses can be calculated through numerical simulation, the process results in excessive calculation time when the simulation involves a full fundamental cycle of the output current for a variety of different converter parameters. In an attempt to reduce computation time, approximations of analytical expressions were developed for the different loss components. Opportunities to further reduce computation time and experimentation burden remain open in this active area of research [28], [29].

Two key topics that are not covered in the power electronics literature are introduced in this application example of the TZP: experimental response surface modeling and surrogate modeling of closed-form analytical equations. This novel contribution allows the characterization of power MOSFETs losses with a comprehensive multivariate model that includes many effects simultaneously. The method is based on statistical Design of Experiments (DoE), which brings n-dimensional response surfaces with accuracy, mathematical simplicity, and statistical validity. The methodology is presented to cover an experimental response surface and the surrogate model of a complex analytical model. As a result, only a few experiments or data points are required, making the method much more efficient than traditional 2-D plots [30].

This experiment is meant to analyse the behaviour of a MOSFET transistor power dissipation under certain conditions and to obtain a model capable of determining the best setting for any given constraint in the variables. Additionally, the analysis provides information about which factors are important in the determination of the power loss. The circuit implemented for this study is a boost type converter, which is a particular case of the Topology Zero. Therefore, the system implementation is done with the TZP. The frequency of operation (f_{SW}) is set at 800kHz and the duty cycle is fixed at 0.25. Further details of

this experimental work are discussed in [31], by the author of this thesis (F. Luchino et al.).

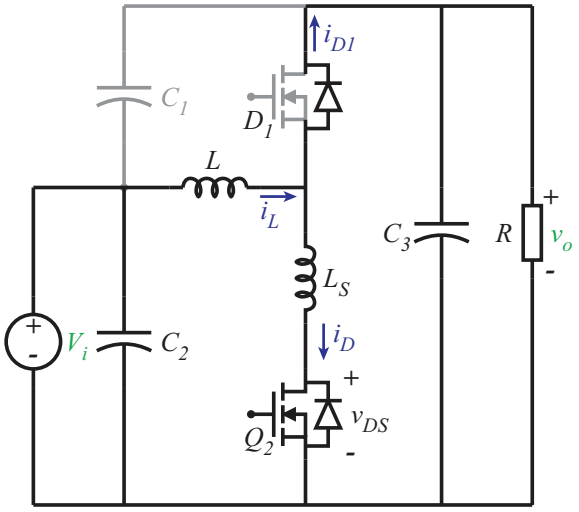


Figure 5.6: Boost converter.

The equation that represents the transistor power loss characteristic for the variables analysed is

$$\begin{aligned} P_T(mW) = {} & 2795 - 70.9 \cdot v_{DS} - 1129 \cdot i_D - 14.3 \cdot R_G + 7.37 \cdot L_S \\ & +19.0 \cdot v_{DS} \cdot i_D + 0.439 \cdot v_{DS} \cdot R_G - 2.93 \cdot i_D \cdot R_G \\ & -0.0646 \cdot R_G \cdot L_S + 103.5 \cdot i_D^2 + 0.0173 \cdot R_G^2 \end{aligned} \tag{5.1}$$

Where the variables considered are: Gate resistance (R_G), drain-source voltage (v_{DS}), drain current (i_D) and stray inductance (L_S). The stray inductance is externally added to the circuit to emulate parasitics related to the layout of the board. From (5.1) several graphics can be obtained applying some restrictions. In addition, the equation can be used to simulate the behaviour of the transistor in an algebraic form in a complex system simulation, without adding burden to the computational analysis. Two graphics, as examples, are shown in Figure 5.7 and in Figure 5.8. The graphics show the transistor power dissipation as function of the interaction of the drain-source voltage versus gate resistance, and drain current versus gate resistance, respectively.

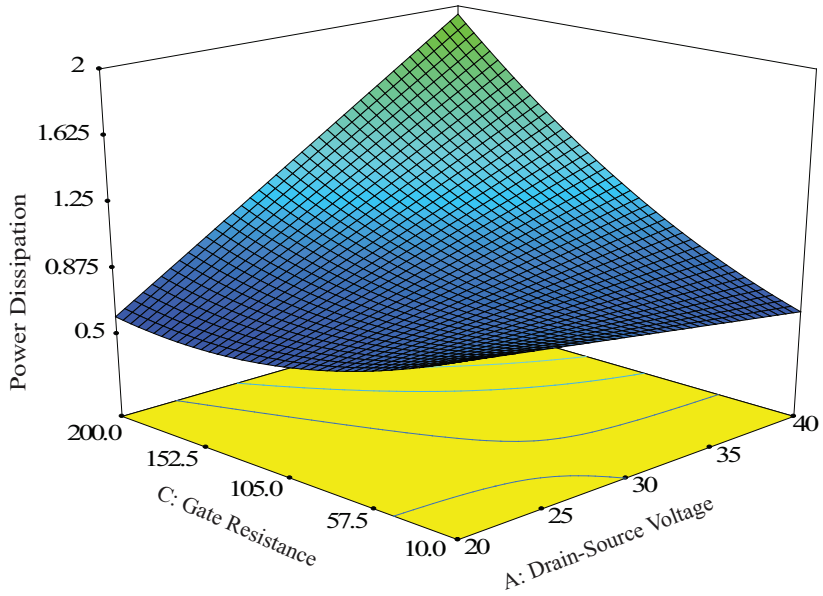


Figure 5.7: Drain-source voltage versus gate resistance interaction in the power dissipation model.

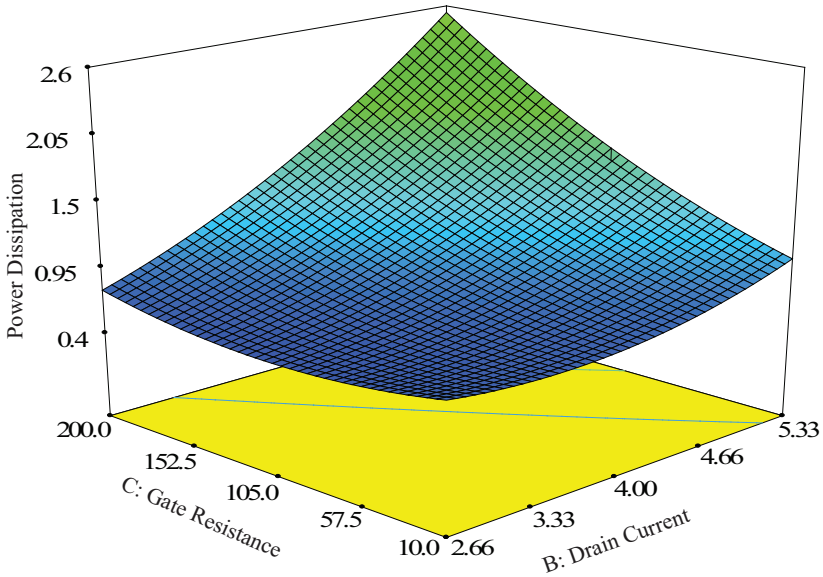


Figure 5.8: Drain current versus gate resistance interaction in the power dissipation model.

As can be seen in this power losses application example, the TZP is able to provide the flexibility to evaluate the behavior of the switching semiconductor devices, in either

synchronous or asynchronous mode, under any possible converter configuration.

5.3.2 Advanced Control Strategies: Boundary Control of Boost Converter

The platform based on the CCP and the TZP was employed to perform advanced controls of a boost converter. The TZP and its signal conditioning presented an optimal tool to carry out experimental work on non-linear control.

Boundary control is a non-linear technique that represents the operation of a converter as state-space equations, whose state vector is composed of energy storage element parameters, such as inductors' currents and capacitors' voltages. This technique is a geometrical control method, based on a switching surface that serves as boundary and, both on-state trajectories and off-state trajectories, each one of them at opposite sides of the boundary [34], [35], [36]. Several boundary techniques have been developed to control different converters. All of them require accurate information about the state variables of the converter. Thus, the measurement of those parameters is crucial for the success of the operation. Between them, current measurement represents a real challenge when it is done at high common mode voltage, such as in inductor current of boost converter or buck converter, or output current in a full bridge inverter. The sensor for this acquisition has to have low noise, high frequency bandwidth (including DC current), high dynamic range and able to handle common mode voltage, in order to be suitable for that duty. Two kind of sensors can meet these requirements to wit, hall effect sensors and shunts resistors. The former satisfies most of the needs, except for noise [27]. On the other hand, shunts need to have extra circuitry to extract worthwhile information from them. For that purpose, an isolated signal conditioning for shunts have been developed to make possible current measurement with the requirements needed. Furthermore, the parameters of the signal conditioning can be modified to adapt it to fit particular requirements, such as bandwidth, gain or offset.

Natural switching surface (NSS) is a curved surface boundary control technique, which has been applied to boost converter to provide a fast transient response without overshoot under start-up or large load transient. Papers [37] and [38], coauthored by the author of this thesis provides more details about this application of the TZP. The switching action is controlled by the state variables and the natural sliding of these states. At first, the switch turns on. When the boundary that depends on the desired target is crossed, the switch turn off. The energy stored in the reactive elements is then delivered to the output without

over voltage. In steady-state, the system switch periodically to keep the output voltage. In case of a load or input voltage change, the target changes as well, and the system reach that target in only one switching action. The schematic of the implemented boost converter employed for these test is shown in Figure 5.9. Since the boost converter is a particular case of the Topology Zero, C1 was eliminated and the upper MOSFET worked as a diode. The converter is therefore operating in asynchronous mode with the upper diode.

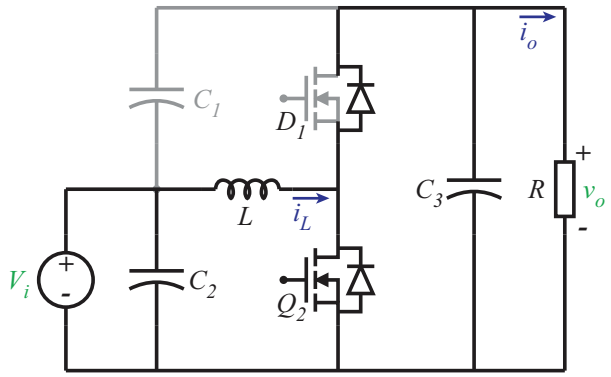


Figure 5.9: Boost converter based on the Topology Zero Platform.

The power of the converter is 30W, the input voltage is 10V and output voltage of 22V. The measured parameters are inductor current (i_L), output current (i_o) and output voltage (V_o). The state variables i_L and V_o have to be acquire with high precision to precisely control the converter. In Figure 5.10, it can be seen the response when a step in constant current load change occurs, and Figure 5.11 shows the response to a resistance change. In both transients, the system measures and controls the opening of the switch according to the control law. The result is an output voltage with no overshoot.

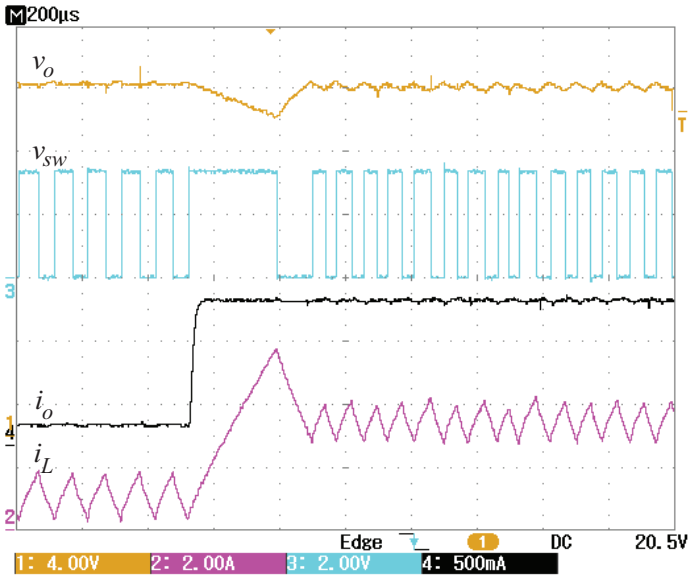


Figure 5.10: Transient response using the NSS for constant current load change: Output voltage (Ch1), inductor current (Ch2), switch state (Ch3), and output current (Ch4).

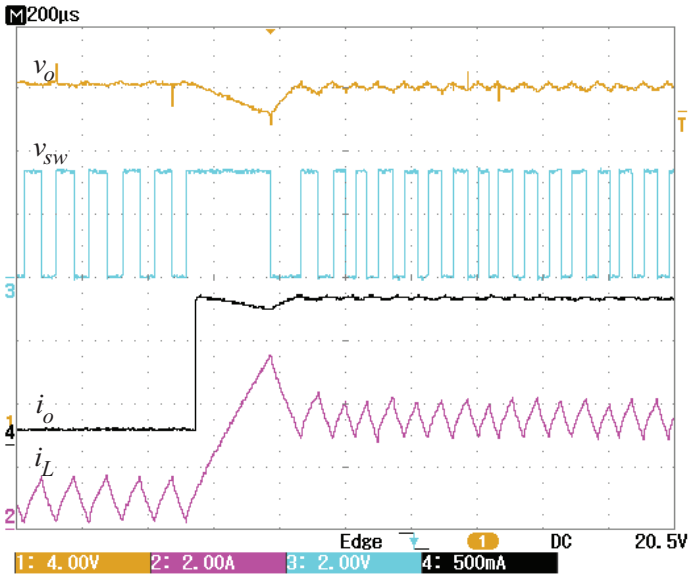


Figure 5.11: Transient response using the NSS for resistive load change: Output voltage (Ch1), inductor current (Ch2), switch state (Ch3), and output current (Ch4).

5.3.3 Planar Transformer Characterization and LLC Converter

This subsection explains the use of the TZP to develop a complex resonant power conversion topology, the LLC resonant topology. The setup based on TZPs is employed to evaluate planar transformers.

Transformers play an integral role in a variety of power electronics converter topologies. They are considered bulky and heavy components in switching mode power supplies and considerable design time is required to make sure that cost is minimized while maintaining good performance. Small planar transformers have the benefit of being light and compact, and they can be placed directly on multi-layer printed circuit boards in high frequency power conversion applications. Combined with exceptional thermal characteristics, low leakage inductance, high reproducibility, and easy manufacturability, they are desirable for many applications in consumer electronics and renewable power. The winding design of planar transformers is a challenging trade off process in which the winding structure affects the transformer's electromagnetic, thermal, power flow, and parasitic behaviour simultaneously. Further details about this interesting and complex application are described in [32] and [33], coauthored by the author of this thesis.

Design of Experiment (DoE) is a powerful statistical tool that permits the analysis of complex and multivariate system by evaluating relatively few operating points. The analysis highlights which variables and their associated interactions are important in the characterization of the system. Response Surface Methodology (RSM) permits obtaining a parametric equivalent model of the system with a second or higher order polynomial equation. RSM is applied, in this case, to planar transformers. The variables analysed are track width ratio, air gap length, clearance distance and the number of turns per winding. And the parasitic responses investigated: leakage inductance, intra-winding capacitances, inter-winding capacitances, winding resistance and magnetizing inductance.

The experimentation consists of computer-based simulations of the windings and actual transformer winding measurements. Afterwards, further test are made to validate how the model can predict parasitics in different windings.

The accuracy and effectiveness of the model is demonstrated through a real application, the design of the transformer of an isolated LLC resonant converter. The circuit diagram is contained in Figure 5.12. The topology employed is a full-bridge converter to drive the transformer and a full-wave rectifier at the DC output. The converter is implemented employing

the platform working in open loop mode. However, the frequency and the deadtime of the switches need to be tuned in by the controller in order to obtain the resonant frequency of the transformer for the required gain.

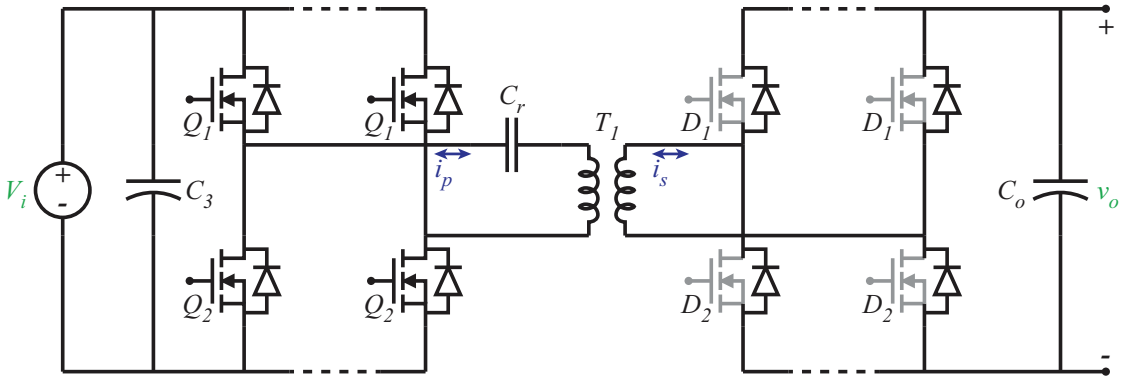


Figure 5.12: Full-bridge LLC resonant converter based on the Topology Zero.

The implementation of the LLC resonant converter is done as an application example to prove the accuracy and simplicity of the design of planar transformers using DoE. In addition, this tool helps to predict the parasitics of the transformers. Two operating conditions of the transformer obtained in experimental tests are shown in Figure 5.13 and Figure 5.14. These operating condition are identified as region 1 and region 2. In region 1, the converter behaves as a series resonant converter, thus the magnetizing inductance does not resonate with the series capacitance because it is clamped to the output voltage. In Region 2, there is a combination of series and parallel converter behaviour. The use of the TZP greatly simplified the research task described above and serves as an actual validation example for the Topology Zero educational and research platform.

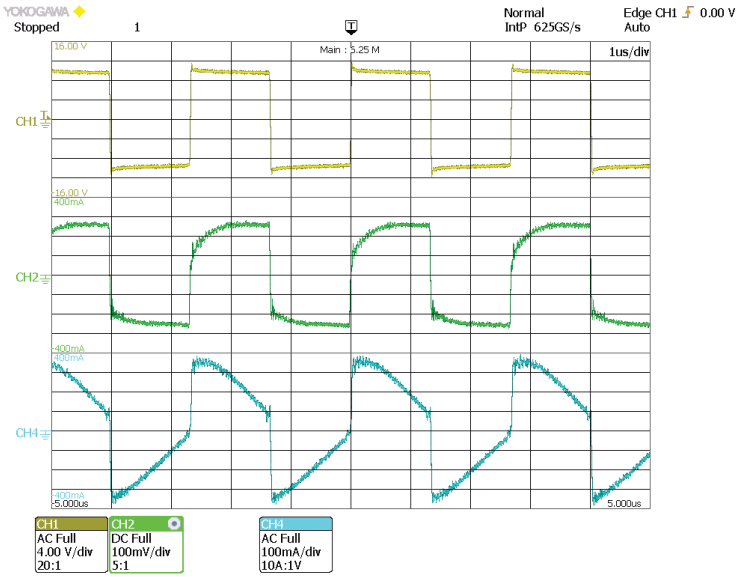


Figure 5.13: LLC case study waveforms operating in region 1: voltage applied to resonant tank (Ch1), primary current (Ch2), and secondary current (Ch4).

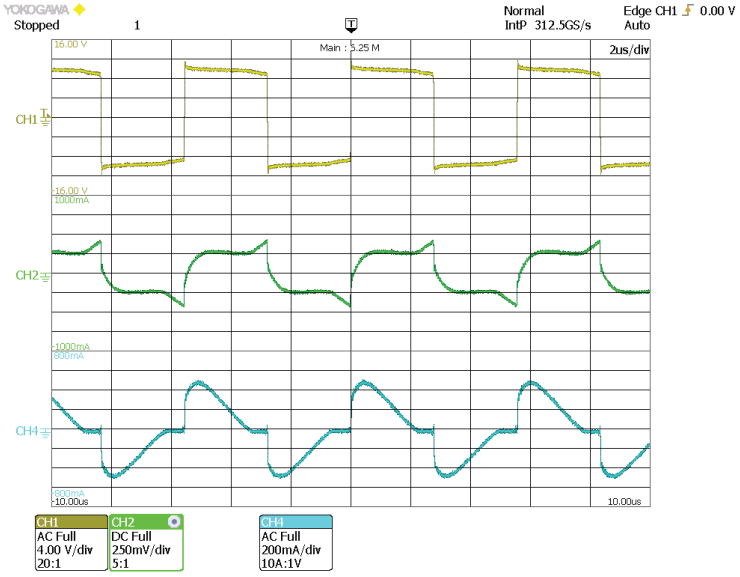


Figure 5.14: LLC case study waveforms operating in region 2: voltage applied to resonant tank (Ch1), primary current (Ch2), and secondary current (Ch4).

5.3.4 Other Applications

The system that employs the Topology Zero has been used to implements a buck converter, a buck-boost converter and a dual active bridge converter; the three of them controlled by NSS. In addition, a high voltage half-bridge and a full-bridge inverters, a three phase power factor corrector and three phase inverter have been accomplished. In all cases with outstanding results in the control strategy employed and power delivered. The versatility of the platform and the Topology Zero has hence been proved. In Figure 5.15 it can be observed the implementation of an inverter using 2 TZPs coupled and controlled by a CCP.

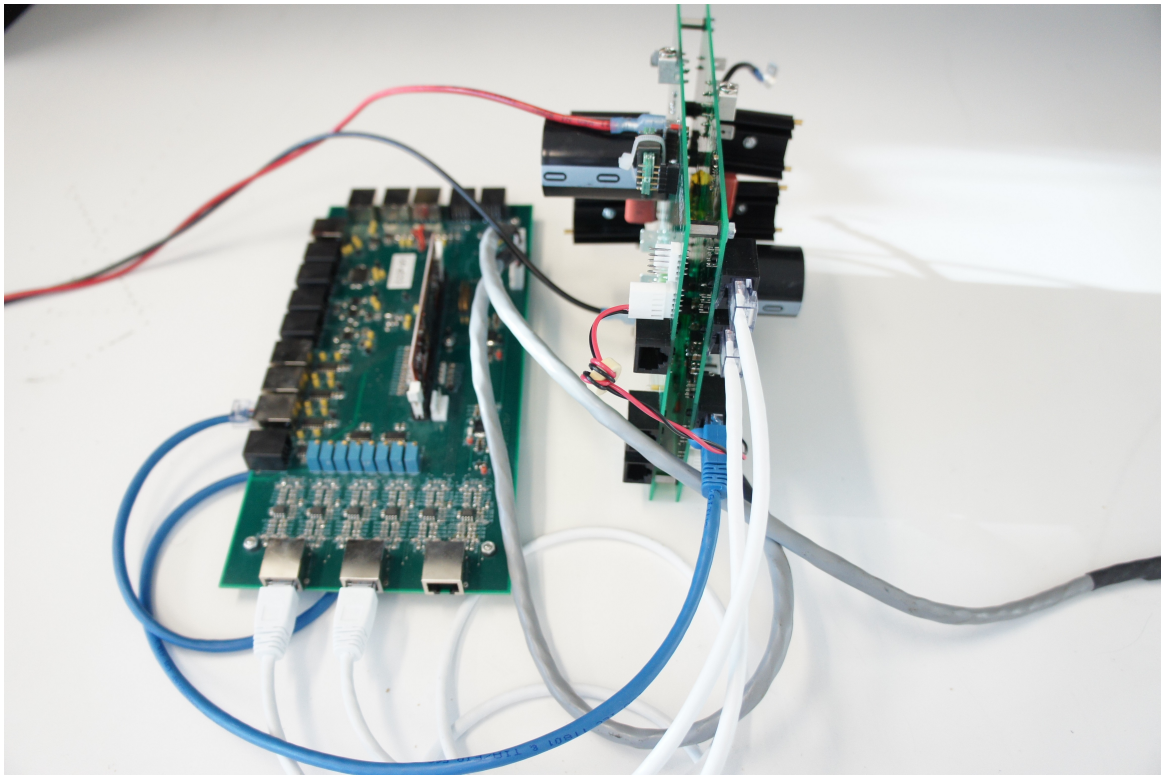


Figure 5.15: Inverter with CCP and 2 TZPs.

5.4 Summary

In this chapter, the implementation of research and educational setups based on the Topology Zero was presented. The essential components to allow the topology to operate were described such as the control and communication platform and the Topology Zero platform.

Later in this chapter, specific examples, that are already published as articles, were explained with some of their results shown. Additionally, other examples of successful implementation of the system were mentioned.

In the next chapter, the general conclusions of the work described in the previous an current chapters are discussed. Moreover, improvements and future work to be done are suggested.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The Topology Zero has been proposed here as a new, simple and excellent means to understand the basis of power electronics, introducing a new concept that offers a new insight into the analysis of basic DC-DC switching mode power converters. This topology can be presented in power electronic courses as an introductory to basic power converters or as a summary or general case of these converters. Derivations for all the possible configurations of the Topology Zero have been described for steady-state condition, as well, alternative derivations have been shown. Moreover, the comparison with known topologies has been carried out and the results proven to match. Additionally, the 3 ports of the Topology Zero have been demonstrated to allow indirect measurements of any port; measuring any given 2 ports, the other is immediately determined. This important characteristic allows for future experimentation of other control schemes, in particular, if the calculation and the processing time in a physical implementation is simplified. Furthermore, dynamic analyses have been also performed for all the configurations of the Topology Zero using small-signal analysis. The results obtained have been correlated with a reliable piece of circuit simulation software. Once again, the outcomes of the comparison were outstanding. Together, steady-state and small-signal analyses have proven that the Topology Zero is the general case circuit to obtain any type of DC-DC switching mode converter. An introduction to power losses calculation for the Topology Zero has been given in order to present a comprehensive analysis of this architecture. The strengths of the Topology Zero are its simplicity, its flexibility and its symmetry; with a single circuit, without any modification, up to 12 topologies can be achieved.

Furthermore, with minor modifications, additional configurations can be obtained, such as, the half-bridge and full-bridge topologies.

The physical implementation of the Topology Zero was embedded with an integral system controller and described in the second part of this document. The educational system is composed of 2 platforms, namely Control and Communication Platform (CCP), and Topology Zero Platform (TZP). Each of the different modules that conform the platforms were explained along with their features. In order to demonstrate the characteristic features and flexibility of the developed platform, real research application examples were presented. The results achieved in the application examples resulted in various journal and conference articles. Other topologies are currently being implemented with the same architecture for research purposes as well. The educational setup based on the Topology Zero was used for a number of research activities. Part of the results has been published and is listed below:

- J. M. Galvez, M. Ordonez, F. Luchino, J. E. Quaicoe, "Improvements in Boundary Control of Boost Converters Using the Natural Switching Surface, IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3367-3376, Nov. 2011. ©2011 IEEE

- S. R. Cove, M. Ordonez, F. Luchino, J. E. Quaicoe, "Applying Response Surface Methodology to Planar Transformer Winding Design, in Press, IEEE Transactions on Industrial Electronics, 2011. ©2012 IEEE.

- F. Luchino, M. Ordonez, G. G. Oggier, J. E. Quaicoe, "MOSFET Power Loss Characterization: Evolving into Multivariate Response Surface,in Proc. IEEE Energy Conversion Congress and Exposition, Phoenix (USA), Sept. 2011. ©2011 IEEE.

- J. M. Galvez, M. Ordonez, F. Luchino, J. E. Quaicoe, "Improvements in Boundary Control of Boost Converters Using the Natural Switching Surface, in Proc. IEEE Energy Conversion Congress and Exposition, Phoenix (USA), Sept. 2011. ©2011 IEEE.

- S. R. Cove, M. Ordonez, F. Luchino, J. E. Quaicoe, "Integrated Magnetic Design of Small Planar Transformers for LLC Resonant Converters, in Proc. IEEE Energy Conversion Congress and Exposition, Phoenix (USA), Sept. 2011.©2011 IEEE.

- G. G. Oggier, M. Ordonez, J. M. Galvez, F. Luchino, "Fast Transient Boundary Control of the Dual Active Bridge Converter Using the Natural Switching Surface,

presented at IEEE Energy Conversion Congress and Exposition, Raleigh (USA), Sept. 2012.

6.2 Future Work

The Topology Zero educational platform will be used to offer a variety of training activities for undergraduate students. This new innovation opens the possibility of replacing traditional power electronics education based on buck, boost, etc. with the general Topology Zero case. Teaching an introductory course on power electronics with the Topology Zero will open a number of publication opportunities in IEEE Transactions on Education.

Further and deeper analysis are projected for the theoretical study of the Topology Zero as integrative converter. The derivation of a single small-signal model, from which the transfer functions of each configuration could be easily obtained, is one of these goals.

Future work also includes the optimization of the layout of the power board to reduce to a minimum the parasitics in the DC power distribution path, in the switches and in the path to the load. The reduction of the parasitics is vital not only for EMI emission to the environment, but for noise that can be introduced in the digital and analog signals. The increment of power rating is one of the goals as well. All these improvements have still to meet the IPC standards of creepage and clearance for the voltage and current the system handles. Further improvements should be done to develop a high voltage/high current converters. Isolation for the drivers is extremely important, the transformers that supply power to the drivers and the gate signal driver isolators are currently in the process of being further optimized, in order to handle higher voltage and switching frequency. Improvements to current sensors for high common mode voltage are being carried out, to provide good current measurements with high bandwidth and low noise. There are two challenges for this circuit to be optimal. First, the isolated power supply needed cannot be shared with other stages of the system and need to provide extremely low noise DC voltage. Second, high dv/dt changes in the common mode need to be seized to avoid distortion in the signal produced. In the newest power conversion platform, the fault protection is managed by the control and communication platform. Faster responses can be obtained if the protections are handled in the same power converter platform. Thus, it is suggested to add protection circuitry to the power module. In the research field, the operation of the Topology Zero as a multiple port bidirectional converter could be investigated. Another area of interest is

the integration of the Topology Zero into a power device package that would provide more versatility in complex topologies and simplify their implementation.

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