Designing Shallow Trench Isolation Diodes as Electrostatic Discharge Protection for Applications in Deep Submicron CMOS Technology

by

Thomas Chung Kin Au

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Approval

Name: **Thomas Chung Kin Au**

Degree: **Master of Applied Sciences**

Title of Thesis: ***Designing Shallow Trench Isolation Diodes as Electrostatic Discharge Protection for Applications in Deep Submicron CMOS Technology***

Examining Committee:

Chair: **Dr. Glenn Chapman, P. Eng**
Professor

Dr. Marek Syrzycki, P. Eng
Senior Supervisor
Professor

Dr. Behraad Bahreyni, P. Eng
Supervisor
Assistant Professor

Dr. Ash M. Parameswaran, P.Eng
Internal Examiner
Professor
School of Engineering Science

Date Defended: May 24, 2013

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Abstract

Developing electrostatic discharge (ESD) protection devices has traditionally relied on fabricating test chips during early stages of the integrated circuit design and subsequently testing the devices for optimization. However, in deep-submicron (DSM) CMOS technologies, fabricating test chips are unfeasible due to the cost and timing constraints. As a result, using 2-D device simulations to predict the failure point and to optimize ESD protection devices are becoming the preferred approach. Shallow trench isolation (STI) diodes available in DSM CMOS technologies have been widely used for ESD protection in high-speed mixed-signal and RF applications. In this thesis, 0.13 μm CMOS STI diodes have been calibrated and simulated using SEQUOIA Device Designer and the results allow to accurately predict the failure point and to optimize diode geometries for high-speed mixed-signal and RF applications. The proposed methodology can also be used in practice to aid the design of ESD protection in future deep submicron CMOS technologies.

Keywords: Electrostatic discharge (ESD) protection circuits; deep-submicron CMOS ICs; shallow trench isolation diodes; ESD event models

To my family and my love

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List of Acronyms

CDM	Charge device model
DSM	Deep-submicron
DUT	Device under test
ESD	Electrostatic discharge
HBM	Human body model
IC	Integrated circuits
I/O	Input/output
MM	Machine model
RCL	Resistors, capacitors, and inductors
RT	Response time
SDD	Sequoia device designer
SCR	Silicon controlled rectifier
STI	Shallow trench isolation
TLP	Transmission line pulse

1. Introduction to electrostatic discharge (ESD)

One of the classical examples of electrostatic discharge (ESD) is when you exit a car on a dry winter day and get shocked when touching the car door. The static electricity is built up when your clothes rub against the car seat and discharges as you touch the car door. The voltage can be in the order of thousands of volts, depending on the humidity of the environment. Although you can barely feel the shock, the high voltage poses a significant threat to modern electronic circuits. With continuous decrease in device size and demand for high speed performance, ESD protection becomes a crucial component of each CMOS integrated circuit (IC) fabricated in deep submicron technology, and designing of ESD protection have become an important part of the CMOS IC design process. Along with the technology scaling and the increase in circuit speed, ESD standards are also constantly changing to improve reproducibility and reduce the cost of testing. Traditionally, there are three ESD qualification standards: human body model (HBM), machine model (MM), and charge device model (CDM). These standards will be examined, followed by a discussion on newer ESD qualification standards emerging in recent years.

1.1. ESD events and testing standards

In order to replicate real ESD events, three simplified models have been widely used over the past few decades. Each model has been represented by a unique combination of resistors, capacitors, and inductors (RCL). In the human body model (HBM) (Figure 1.1a), the human body has been represented by a resistance value of 1.5 kΩ, a capacitance value of 100 pF, and an inductance value of 7.5 μH. Initially, the capacitor is fully charged to hold a potential of 1 kV or less, and subsequently discharged through the RCL circuits into the device under test (DUT). This model represents a scenario of a person touching one pin of the chip, while one or more of the other pins of the chip remain grounded. Another type of ESD event, known as the

machine model, simulates the scenario taking place during the assembly of modern integrated circuits, in which a robotic arm is used to pick and place the circuit during system assembly. In this case, a 200 pF capacitor and a 0.75 μF inductor are used to represent the robotic device. Similar to the HBM, the machine model (MM) is also initially charged to reach a potential of a few hundred volts. Subsequently, the capacitor is discharged through the RCL circuit to the device via one of the pins, while one or more of the other pins of the chip remain grounded. In contrast with the HBM and MM, the third model, known as the charged device model (CDM), represents a different phenomenon, in which the device itself stores an initial charge and discharges it on contact with another surface [1]. Figure 1.2 shows the current output waveforms for all three ESD models. The HBM produces the slowest pulse with a rise time of 10 ns and decay time of 150 ns, while the MM represents a slightly faster bipolar current pulse. Finally, the CDM has the fastest pulse, similar to a damped sinusoid but lasting only a few nanoseconds, with the highest peak current much larger than both the HBM and MM. In general, HBM failures are shown to cause thermal failures, whereas CDM failures are typically associated with gate oxide failures.

Even with simplified models to represent real life ESD events, it has been extremely difficult to implement the above testing methods due to parasitic capacitances, inductances, and resistances associated with different ESD testers and cables. The implications of existing ESD testers are one of the many reasons for introduction of a new, more effective tool for characterizing ESD devices. The transmission line pulse (TLP) technique, developed by T.J. Maloney and N. Khurana, uses a series of high current pulses with 100 ns width to examine the I-V characteristics of ESD devices [2]. Because of the short time exposure, this technique has the ability to examine the high current characteristics without damaging the ESD devices. TLP testing has become the standard for characterizing ESD devices. Although there are many advantages in using the TLP testing method, one on-going challenge is to appropriately correlate the results obtained from TLP testing to the existing ESD models [3].

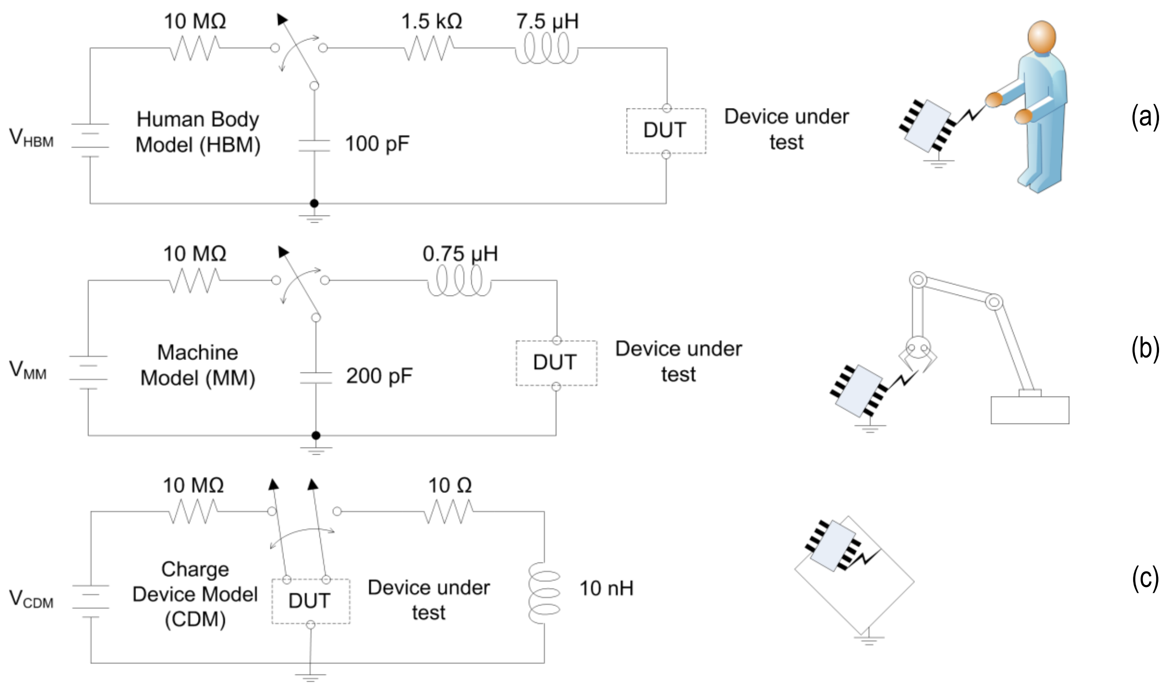


Figure 1.1. ESD models: (a) Human body model (b) machine model (c) charge device model

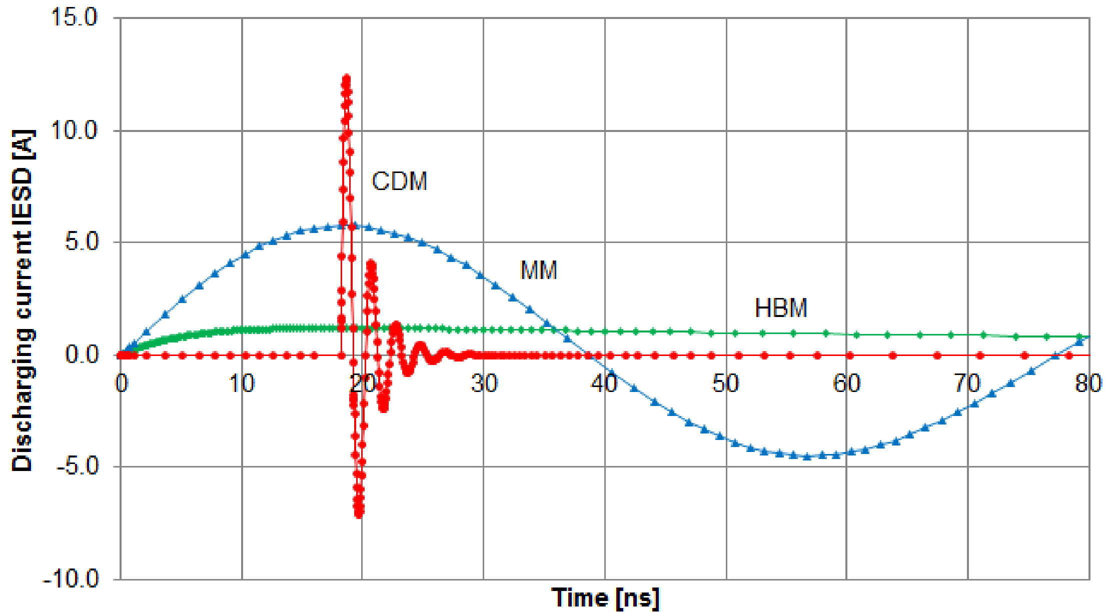


Figure 1.2. Spice simulated current output waveform for different ESD events

1.2. Different types of devices for ESD protection

The purpose for ESD protection devices is to provide a low impedance path to discharge high spikes in current during an ESD event and clamp the voltage to prevent dielectric breakdown of gate oxide in MOS transistors. In addition, ESD protection devices are also required to have low parasitic capacitances, low parasitic on-resistances, and high off-impedances during normal operation to minimize their impact on the internal circuitry. Other considerations include the ability to construct devices within existing technology featuring a high ESD robustness within an available layout area. Diodes, MOSFET transistors, and silicon controlled rectifiers (SCR) are the most commonly used ESD devices that meet the above requirements.

1.2.1. Diodes

Diodes are one of the simplest and most effective ESD protection devices that have been in use for decades. In this protection strategy, two back to back diodes are connected at the input/output (I/O) pins of the circuit, as shown in Figure 1.3. These forward biased diodes are capable of handling high levels of current, but have a fixed forward turn-on voltage approximately equal to 0.60 V for typical CMOS process. One solution to resolve the fixed turn-on voltage is to cascade the diodes (connect in series), which is used in mixed-voltage I/O interface.

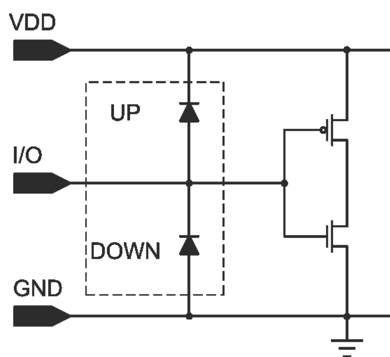


Figure 1.3. Typical ESD diode protection circuit

1.2.2. Grounded-gate NMOS

MOS transistors operating in the $V_{GS} = 0$ condition, known as the grounded-gate configuration, can also be used as an ESD protection device (Figure 1.4a). The drain of the grounded-gate NMOS transistor is connected to the I/O pin of the circuit, while the gate and source terminals of the transistor are both shorted to V_{SS} (NMOS) or V_{DD} (PMOS) supplies. In this condition, a parasitic bipolar transistor is formed (Figure 1.4b). Under normal operations, both the grounded-gate NMOS protection device and the parasitic device remain in the off-state. During an ESD event, the drain-to-substrate p-n junction enters avalanche breakdown. This causes the parasitic npn transistor to turn-on, and consequently discharge the ESD current and prevent damages to the other parts of the circuit.

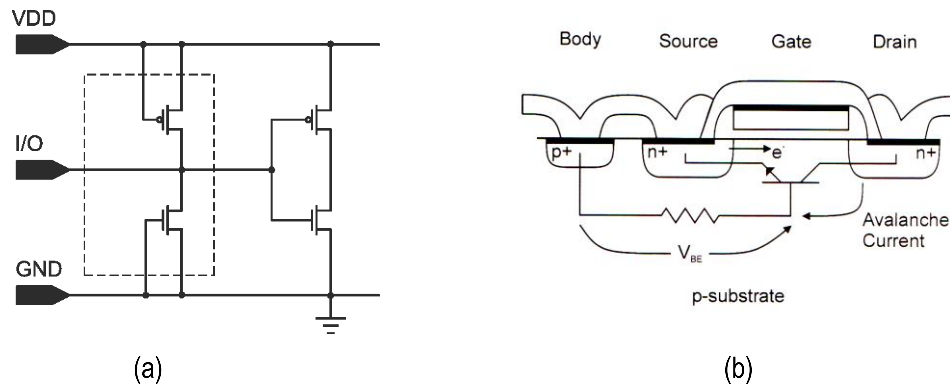
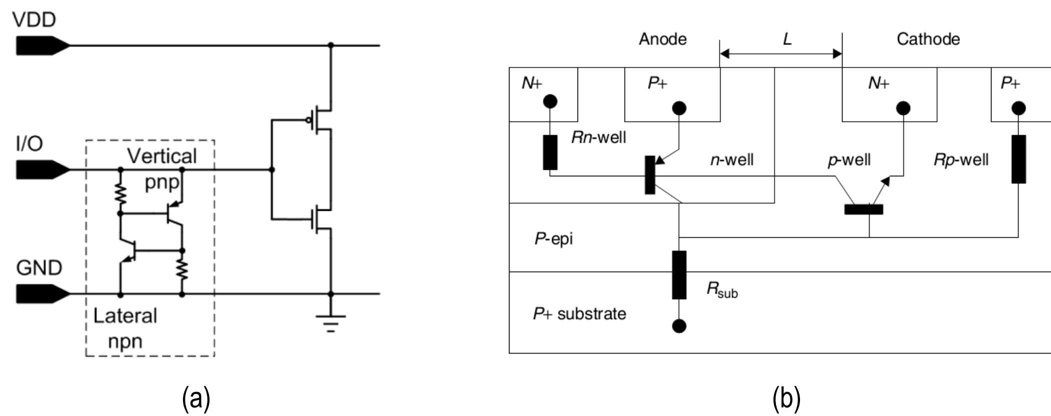


Figure 1.4. (a) Grounded-gate NMOS ESD protection circuit (b) cross section of NMOS transistor [4]

1.2.3. Silicon-Controlled Rectifiers (SCR)

Silicon controlled rectifiers, also known as thyristors, are normally used for high power applications. As an ESD protection device, the SCR is connected to the I/O of the circuit as shown in Figure 1.5a with an anode connected to the I/O pin and cathode connected to ground. The structure of the device can be viewed as a combination of two bipolar transistors: a vertical pnp transistor and a lateral npn transistor (Figure 1.5b). During an ESD event, the p-n junction of the vertical pnp transistor enters avalanche breakdown, which triggers a voltage to build up between the base and emitter of the lateral transistor. Finally, the lateral pnp transistor is turned on, thus providing a low resistance path to discharge the ESD voltage.



(a) (b)

Figure 1.5. (a) SCR protection circuit (b) cross section of SCR ESD device [5]

1.2.4. Comparison of ESD protection devices

Due to the area efficiency of diodes and SCRs, both of these devices are used for ESD protection in DSM CMOS technologies. The two main disadvantages of grounded-gate NMOS are the area consumption and large parasitic capacitance, which makes this device less ideal for high-speed applications. Basic comparisons of the three ESD protection devices are shown in Table 1.1. The main advantage of using diodes is a lower trigger voltage compared to SCR or grounded-gate NMOS. Although modifications can be made to the SCR design to lower the trigger voltage, it is usually a very complex task and is highly dependent on the technology process. For the purpose of this research, diodes will be used due to lower trigger voltage and availability of the devices in CMOS technology.

Table 1.1. Advantage and drawbacks of different ESD protection devices

Device	**Advantages**	**Drawbacks**
Diodes	• Area efficient • Lower trigger voltage • Small junction capacitance • Available in standard technology	• Fixed forward turn-on voltage (0.6-0.7 V for silicon) • On-resistance reduce current handling capabilities
Grounded-gate NMOS	• Available in standard technology	• Area consumption • Higher trigger voltage • Large parasitic capacitance
Silicon controlled rectifier	• Area efficient	• Higher trigger voltage • Strong dependence on technology

1.3. Design methodologies of ESD protection devices

Traditionally, the development cycle (Figure 1.6) for ESD protection devices has heavily relied on fabrication of test chips because ESD protection is unique in every circuit and is sensitive to technology processes. During the preliminary stages of IC chip development, circuit designers are provided with a set of ESD requirements along with some technology data provided by the fabrication process manufacturer. Based on their previous experience with an earlier technology, circuit designers will develop a large number of test devices to be manufactured. Upon receiving the test chips, each of the ESD devices will be tested and characterized. Devices that could potentially meet the ESD requirements will be further investigated. Usually a second or third set of test chips will be manufactured in order to optimize the performance of the ESD protection devices. Due to recent advancements in CMOS technologies, this development cycle has become unaffordable because of the increased cost and time associated with newer technologies. For example, the cost for prototyping 0.13 μm CMOS process using STMicroelectronics available through Multi-Project Circuits (CMP) is 2200 Euro/mm^2. The price significantly increases to 12000 Euro/mm^2 while attempting to use STMicroelectronics to manufacture 28 nm CMOS process [6]. In addition, the expected cost reduction and performance gain also forces companies to move to a newer technology as quickly as possible, thereby reducing the design timeframe for ESD protection devices. The development cycle has been refocused to perform initial ESD simulations and optimization prior to design of test chips.

The simulation-based ESD design process flow (Figure 1.7) relies on the same technology data, requirements, and prior experience during the initial design phase of the device. The main distinction in the simulation approach is that performing the optimization during the earlier stages of design must replace the development of a large number of test structures. The simulation-based ESD design process can be started even before the newer technology becomes available. For example, based on the description of the process steps in the newer technology, along with some of the parameters from the previous technology, commercial simulators can generate 2-D structures of semiconductor devices. These 2-D structures can be simulated in mixed-mode environments to examine the ESD performance, provided that proper calibration

and doping profile has been used. Some of the commercial software available for ESD design and optimization includes ATLAS (Silvaco), DESSIS (ISE), MEDICI (Synopsys), and Device Designer (Sequoia Device Systems). The simulation results can necessitate only a limited number of test structures that need to be designed, manufactured, and tested. ESD simulations can also provide insight on hypothetical changes to many physical or process variations that would otherwise not be possible to examine using the traditional ESD design process flow due to cost and time constraints.

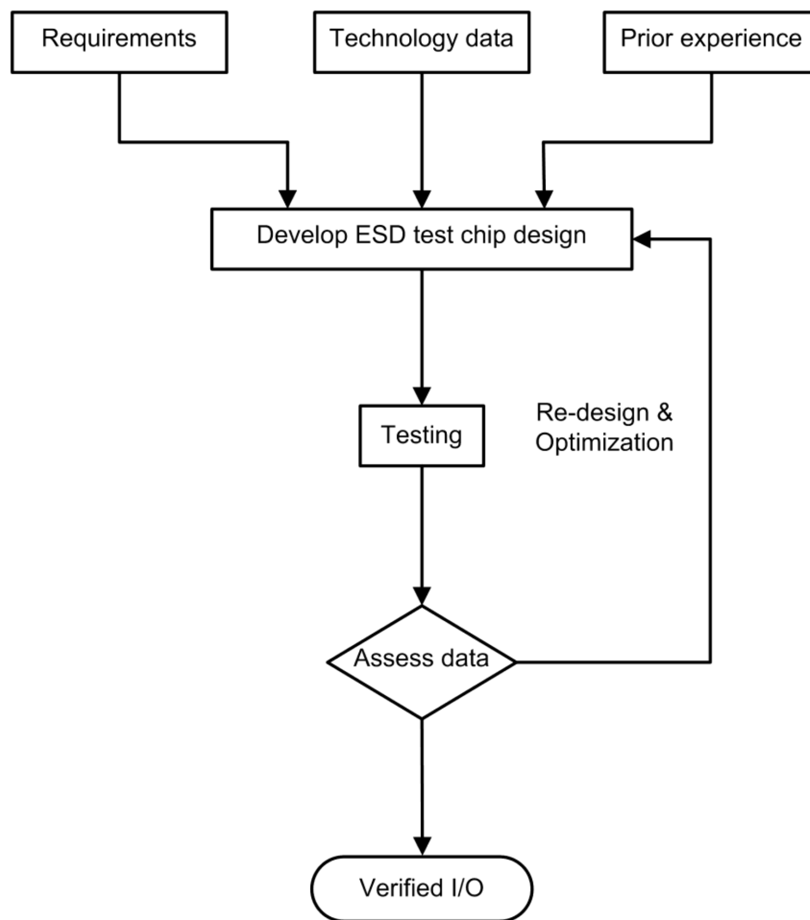


Figure 1.6. Traditional ESD design process flow

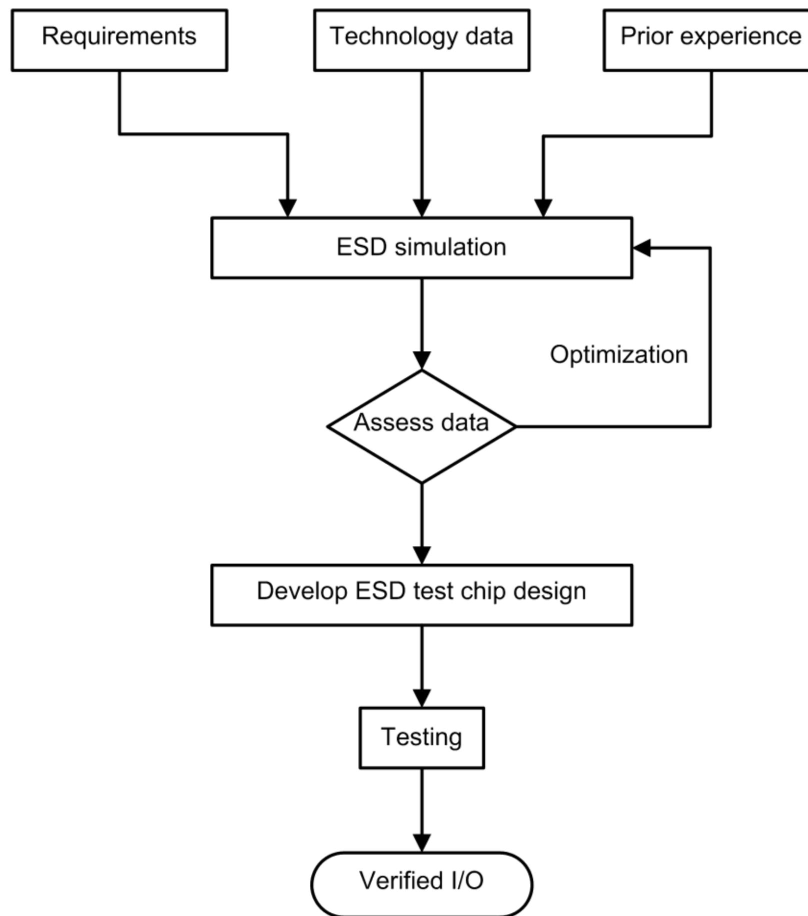


Figure 1.7. Simulation-based ESD design process flow

1.3.1. SPICE simulation limitations

An alternative to generating 2-D structures for device simulations is to create equivalent circuits to simulate the electrical behaviour of ESD protection devices, rather than the physical behaviour. The HSPICE circuit simulator is a software tool that uses compact device models to represent complex circuits in modern CMOS technologies. The advantage of using SPICE simulation is the ability to examine the impact of the ESD protection devices on the overall performance of the internal circuit. However, due to the simplicity of the models, there is a trade-off between complexity and accuracy of the model. The focus of this section is to provide an overview of the development of the SPICE models for diodes in literature. By examining the cross-section of an STI diode, one can come up with a compact model, shown in Figure 1.8a. The model consists of two parasitic capacitors ($C_{diffusion}$ & $C_{junction}$), a P-N junction, and a parasitic series resistor

(R_S). This compact model can be translated into a standard SPICE model of a p-n diode as shown in Figure 1.8c, which consists of a current source (I_D), combined parasitic capacitance (C_D), and the same parasitic resistance (R_S). The current source is a function of the diode junction voltage (V_{D0}) and has three regions of operation. Referring to Figure 1.9, the first region of operation is governed by the Shockley diode equation. The second region occurs when V_{D0} is equal to the breakdown voltage (V_{BD}). The current at the breakdown voltage corresponds to the breakdown current (I_{BD}). The third region of operation occurs when V_{D0} is less than the V_{BD}. Equations 1 through 3 summarize the characteristics of a typical diode, where the saturation current (I_S) is a function of temperature and the emission coefficient (n) is a positive number ranging from 1 to 2.

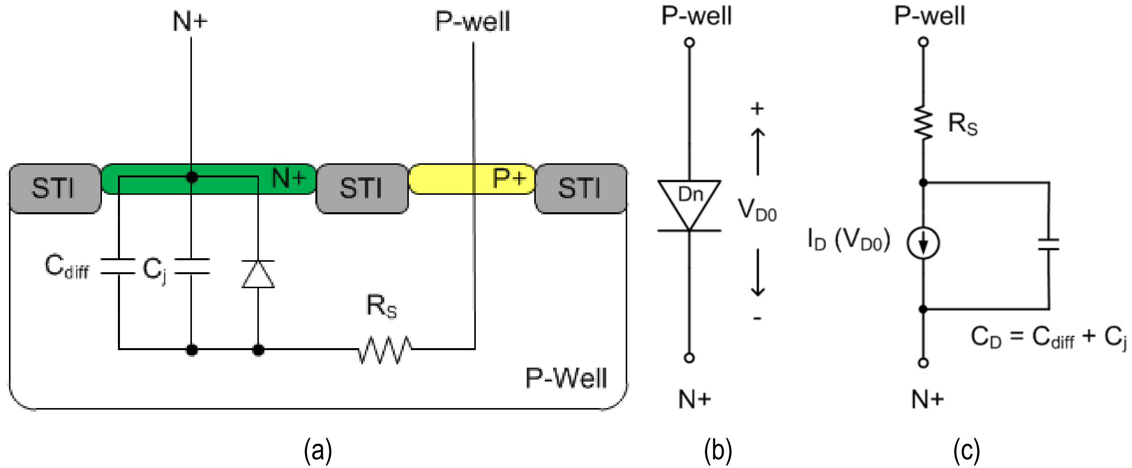


Figure 1.8 (a) Cross-section of diode with compact model [1] (b) Equivalent symbol (c) SPICE model of diode [7]

For region I: $$I_D(V_{D0}) = I_S\left(e^{V_{D0}/nV_T} - 1\right) \quad (1)$$

For region II: $$I_D(V_{D0}) = -I_{BD} \quad (2)$$

For region III: $$I_D(V_{D0}) = -I_S\left[e^{(V_{BD}+V_{D0})/V_T} - 1 + \frac{V_{BD}}{V_t}\right] \quad (3)$$

The total parasitic capacitance (C_D) is comprised of the depletion capacitance ($C_{junction}$) and the storage-charge capacitance ($C_{diffusion}$). Under reversed-biased conditions, $C_{diffusion}$ is dependent on V_{D0}, the zero bias junction capacitance (C_d), the built-in voltage

(V_{bi}), and the grading coefficient (m). The built-in voltage is also a function of temperature. The grading coefficient ranges from 1/3 to 1/2, depending on whether the diode has a linear junction or step junction. $C_{diffusion}$ is the dominating capacitance and is related to the transit time (τ_t), the change in voltage, and the change in current of the diode.

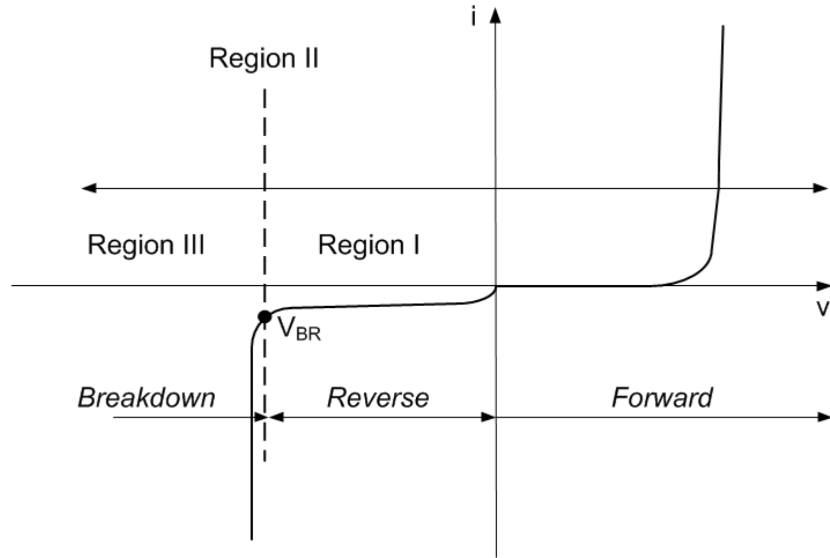


Figure 1.9. I-V characteristic of a typical diode

$$C_{\mathrm{D}} = C_{\mathrm{junction}} + C_{\mathrm{diffusion}} \tag{4}$$

$$C_{\mathrm{D}} = C_{\mathrm{d}} \left(1 + \frac{V_{D0}}{V_{bi}}\right)^{-m} + \tau_T \frac{dI_D}{dV_D} \tag{5}$$

In Equation 5, parameters such as I_S, n, R_S, C_d, V_{bi}, and m are process dependent and require experimental data to determine the approximate value. Linear regression and curve fitting are two possible methods to determine these parameters which are typically not provided by the foundry. Furthermore, typical SPICE models are only valid for low currents, low voltages, and forward operations. In addition, these models do not account for electrothermal properties during an ESD event. To account for these discrepancies, standard models can be extended to incorporate these effects [8]–[10]. For STI diodes, Torres [11] proposes using the Standard Gummel Poon model (a model typically used for bipolar transistors for SPICE) as a starting point to create a valid model in the high-current mode of operation. The new model adds a base resistance to model high-level

injection and carrier velocity. Although such a model is very useful for ESD protection design, this particular model is only scalable in terms of perimeter and neglects the effect of device capacitances. Similarly, Teng et al. [12] proposed using BSIM4 model for MOSFET as a starting point to describe the behavior of the poly-bounded diode, due to the similarity of the device structure. The new model incorporates extra substrate resistances and disables certain parameters to account for the differences between MOSFETs and poly-bounded diodes. This model was scalable in terms of the number of fingers, the diode length, and the diode width. In contrast with the STI diode model, this model accounts for the device capacitance but the model is only valid for normal operating conditions and is not valid under ESD stress.

Currently, existing diode models available in the standard SPICE are inadequate in predicting ESD failures because of the high currents associated with an ESD event. Newer SPICE models for ESD diodes have been recommended in literature but all the models described in this section require recalibration and are often not scalable. The goal of this research is to predict ESD failures in newer DSM CMOS technologies and to reduce the number of iterations required for ESD device protection. As a result, SPICE models can only be used for verifying the impact on internal circuits, rather than the initial design of ESD protection devices.

1.4. Thesis organization

This thesis first highlights the ESD models and measurement techniques that exist for deep submicron CMOS integrated circuits. Descriptions of two design methodologies are presented. Chapter 2 discusses the performance parameters for ESD protection devices, followed by a literature review of STI diodes for high-speed mixed-signal and RF applications. In Chapter 3, a software-based device simulator is used to construct an STI diode and is calibrated with data provided by the technology manufacturer. Chapter 4 examines the effects of changing different geometry parameters on the ESD performance parameters through electrothermal and device simulation. Chapter 5 focuses on the optimization of the STI diodes and presents several ESD test structures that meet the design criteria. Finally, Chapter 6 presents the conclusions and possible future work.

2. ESD performance criteria in DSM CMOS

As described in Chapter 1, there are many ESD testing standards thoroughly described in literature. The human body model (HBM) standard is the most commonly used standard for evaluating ESD diode performance in high-speed mixed-signal and RF applications. A standard initially proposed in [13] defines an ESD performance target of 2 kV HBM protection level, with a parasitic capacitance of 200 fF, for RF applications in 0.18 µm CMOS technology. This has been widely accepted and applied by other research groups for 130 nm CMOS technologies [14], as well as 65 nm CMOS technologies [15]. In order to quantify the effectiveness of different ESD protection devices, several ESD parameters will be introduced, followed by a discussion on commonly used ESD metrics that are used by other research groups in this area.

2.1. Standard ESD performance parameters

Maximum HBM voltage (V_{HBM})

The robustness of an ESD protection device is characterized by the level of HBM voltage (V_{HBM}) that the device can withstand. For simulation purposes, the HBM setup described in Chapter 1 has been used. An ESD failure criterion was defined by the ESD device's peak lattice temperature exceeding 800 K (melting point of aluminum). A much higher temperature failure criterion could be used since the melting point of silicon is 1685 K, but a more conservative criterion was chosen to allow for a higher safety margin.

Secondary breakdown current (I_{t2})

The secondary breakdown current (I_{t2}) is defined as the highest current the device can tolerate under ESD stress [14], as shown in Figure 2.1. In this particular example, if a

correlation value of 1.5 kV/A is used, the V_{HBM} tolerance would be 4.1 kV, corresponding to an I_{t2} value of 2.73 A. A higher value of I_{t2} corresponds to a higher ESD tolerance.

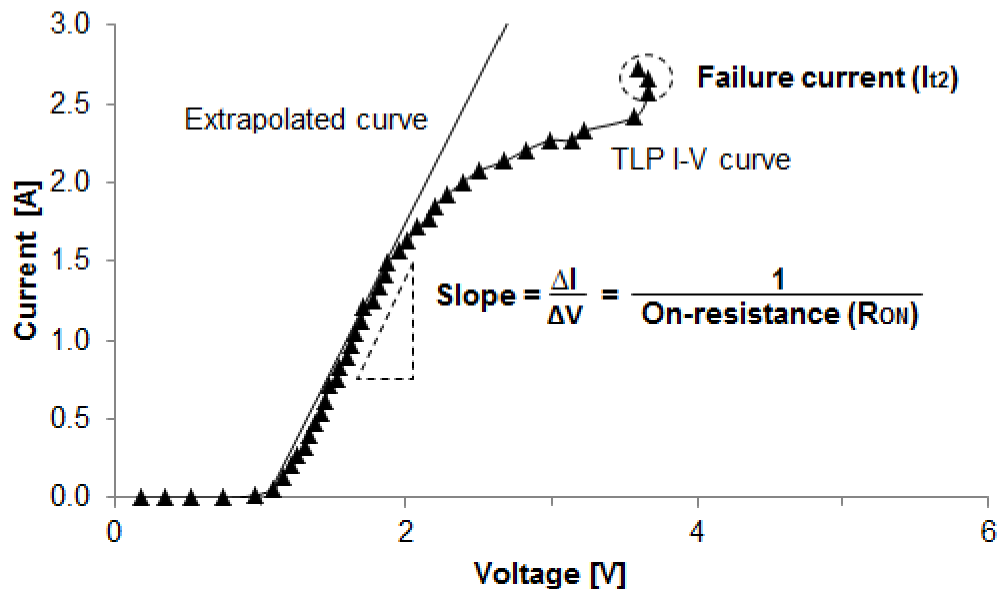


Figure 2.1. Failure current and on-resistance definition

Correlation value (kV/A)

Alternatively, TLP testing provides a method of predicting the device's V_{HBM} tolerance which is related to the secondary breakdown current (I_{t2}) during TLP testing. The correlation value is defined as the ratio between the maximum HBM voltage and the secondary breakdown current (V_{HBM}/I_{t2}). According to reference [16], different technology sizes have different correlation values. In 0.35 µm CMOS technology, the correlation value is 2.1 kV/A, whereas for 0.18 µm CMOS technology, this value is approximately 1.5 kV/A. Due to many uncertainties between different ESD testing equipment, this correlation value can only be determined by performing statistical analyses [16].

On-resistance (R_{ON})

The on-resistance of a diode (R_{ON}) is defined as the linear region of the forward I-V characteristic [17], as shown in Figure 2.1. The R_{ON} corresponds to the inverse value of the slope, which is 0.55 Ω in this example. A lower value of R_{ON} is desirable for ESD protection devices. R_{ON} is dependent on the area and perimeter of the diode [18].

Parasitic Capacitance (C_{diode})

The parasitic capacitance of a diode (C_{diode}) corresponds to intrinsic junction capacitance when the diode is under reversed-biased conditions, which is typically in the order of femto-farads per unit area. As reported by Hsiao and Ker [19], this parasitic capacitance can be estimated by using parameters provided by the foundry such as the zero-bias capacitance per unit junction area of the flat portion of the p-n junction, and the zero-bias side-wall capacitance per unit junction perimeter. The estimated capacitance neglects the parasitic effects of metal layers. Again, a small value of C_{diode} is desirable to minimize the impact of the parasitic capacitance on the internal circuitry.

2.2. Performance parameters for the CDM-type ESD events

With an ever increasing demand for faster and smaller sized transistors over the past decade, examining only the forward I-V characteristics of ESD protection devices has been found insufficient. According to the studies performed by R. Gaertner [20], and the white paper published by Industry Council on ESD Target Levels [21], the gate oxide failures originating from HBM-type ESD events are not expected to happen in future CMOS technology nodes, but most of the ESD failures will be associated with the gate oxide failures related to CDM-type ESD events. Due to the short rise time in the order of a few nanoseconds in the time domain during a CDM event, new characterization methods have been introduced by Wolf et al. [22] to analyze the transient behavior of ESD protection devices. This method of characterization has been adapted to examine the physical effects of various ESD protection devices [23]–[27]. The most important parameters in characterizing the transient behavior are the response time (RT) and overshoot voltage (V_{OS}) [28].

Input signal

The input signal of the ESD stress is a 10 V square pulse, with a rise time of 55 ps, pulse duration of 9 ns, and a delay of 2 ns as shown in Figure 2.2.

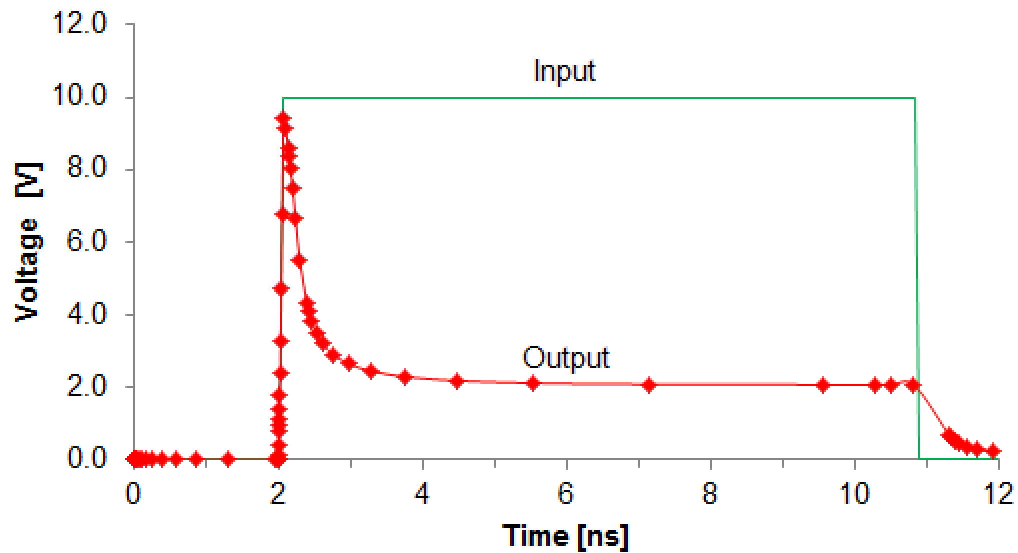


Figure 2.2. Input and output pulse to examine transient characteristics

Output response

An overshoot voltage can be seen from the output response. For the purpose of evaluating the performance of STI diodes, only the turn-on behaviour is important [28] (Figure 2.3 only shows the time range from 2 ns to 3 ns).

Response Time (RT)

The response time is defined as the time between 10% and 110% of the steady state output value (average value of V_0 between 4 ns to 9 ns).

Overshoot Voltage (V_{OS})

The overshoot voltage is defined as the peak output voltage of the transient output response.

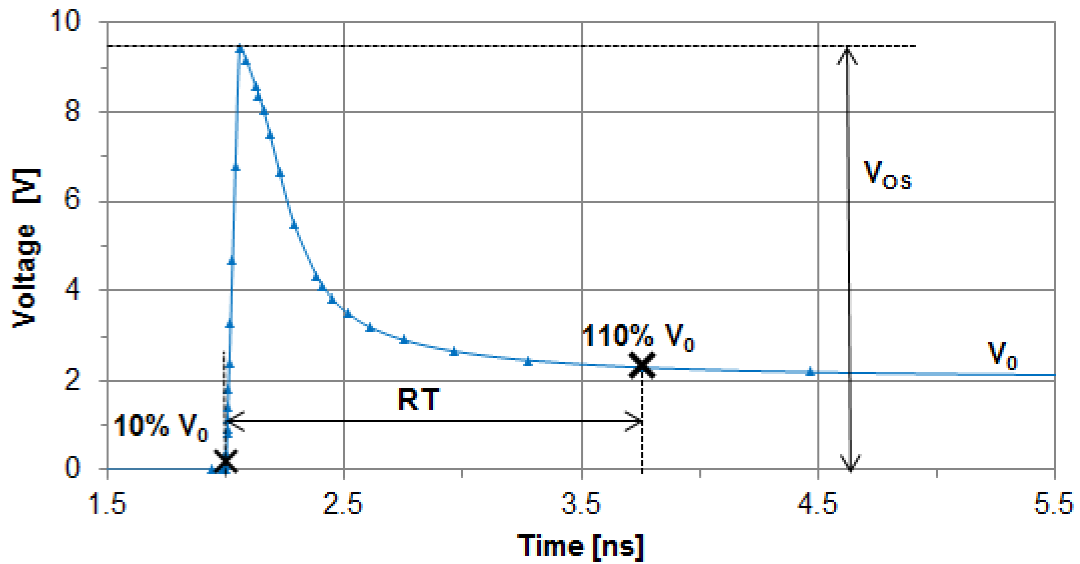


Figure 2.3. Definition of response time (RT) and overshoot voltage (V_{OS})

2.3. Discussion on ESD metrics

Failure current, on-resistance, parasitic capacitance, response time, and overshoot voltage are different parameters that are used to compare the effectiveness of different ESD protection devices. The failure current parameter can be improved by increasing the dimensions of the ESD protection diode, but this will result in a larger area, and cause an increase in parasitic capacitance. Some of the parameters are more important than others. For example, in mixed-signal high speed and RF applications, the parasitic capacitance is more important compared to the on-resistance because a higher parasitic capacitance will limit the switching speed and the frequency of operation. To further quantify ESD protection devices for specific applications, several ESD metrics are defined in literature [29]–[33]. These ESD metrics are useful to compare the effectiveness of one ESD protection device with another ESD protection device.

- Conductivity per unit area: defined as the slope of I-V characteristic divided by the diode area (mS/μm^2)
- Failure current per unit area (mA/μm^2)
- Failure current per unit junction perimeter (mA/μm)
- RC product or time constant: defined as the on-resistance times the parasitic capacitance (fs)

- HBM voltage failure per unit of parasitic capacitance (V/fF)
- Failure current per unit parasitic capacitance (A/pF)

2.4. Literature review of diodes as ESD protection in DSM CMOS technologies

Diodes are one of the simplest ESD protection devices that have been proven throughout different technologies ranging from 0.35 μm CMOS technology to advanced 40 nm CMOS technology for high speed mixed-signal I/O interfaces and RF applications. In the past decade, ESD diodes have been widely studied through SPICE simulations, physical level 2-D or 3-D simulations, and fabrication of test chips. In most of the CMOS processes, there are two main types of diodes available for ESD protection. The most common type of diode is the shallow-trench-isolation (STI) diode. An example of the P+/N-well diode is shown in Figure 2.4. The second type of diode proposed in [34] is the polysilicon bounded diode (also referred to as lateral ESD diode or poly-bounded diode) that has been claimed as featuring lower on-resistance due to a shorter path between p+ and n+ regions (Figure 2.5). There are other innovative diode structures that can be found in literature such as the MOS-bounded diodes (also referred to abutted body tied diodes) [35], [36] but have not been extensively used elsewhere (Figure 2.6).

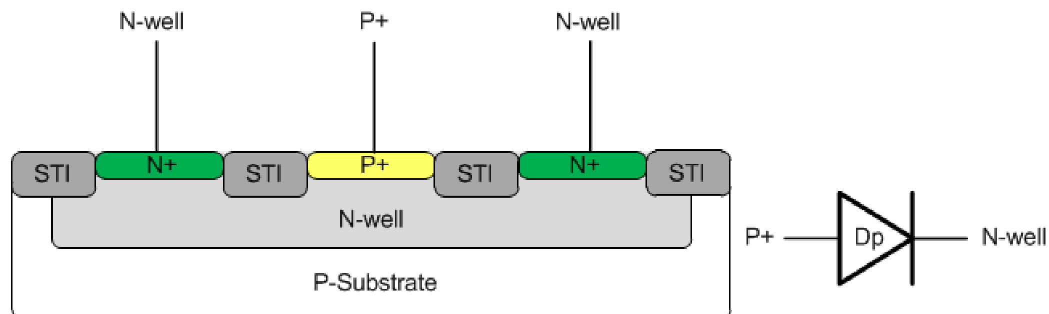


Figure 2.4. Cross-section and symbol of P+/N-well STI diode

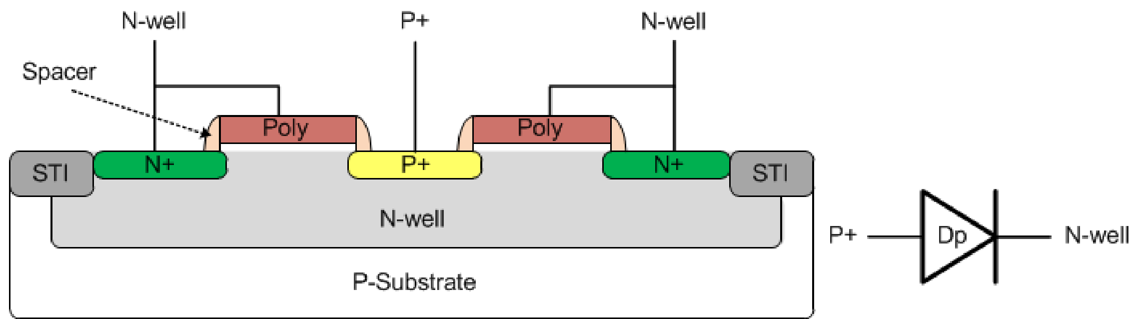


Figure 2.5. Cross section and symbol of P+/N-well poly-bounded diode

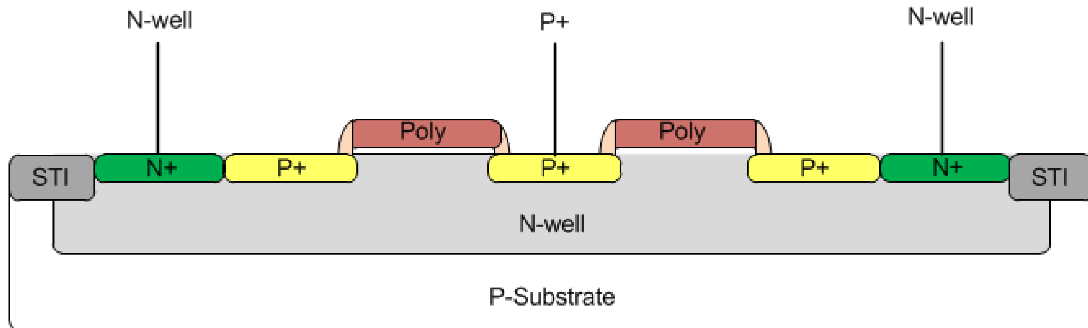


Figure 2.6. Cross section of PMOS bounded diode

In a study presented by Richier et al. [13] for 0.18 μm CMOS technology, STI diodes and poly-bounded diodes were investigated along with other ESD protection devices. The study concluded that ESD diodes performed better compared with SCR or NMOS protection devices due to the low parasitic capacitances associated with diodes. Diode optimization achieved a protection level of 2 kV HBM with a 200 fF parasitic capacitance. The study stated that the capacitance of poly-bounded diodes is nearly double that of STI diodes, but poly-bounded diodes have better ESD performance. In another study for 0.25 μm CMOS technology [37], STI test structures have been verified to provide 2 kV HBM ESD protection and less than 200 fF parasitic capacitance, which makes these devices an excellent choice for RF applications.

For 0.13 μm CMOS technology, experimental results show that diodes with 40 μm perimeter junction have been effective ESD protection devices capable of protecting a gigahertz speed I/O interface with lower than 200 fF parasitic capacitance and meeting 2 kV HBM ESD requirements [14]. The ESD protection diodes proposed were further studied by examining the parasitic capacitance and implemented as an input protection in a transceiver design. Diodes with 45 μm perimeter junction were verified to pass 2 kV

HBM ESD level operating within 2.5 Gb/s high speed receiver [19]. Similar findings were achieved in 0.13 μm CMOS technology with 50 μm perimeter junction and 160 fF parasitic capacitance for 2 kV HBM ESD level [18]. STI diodes were compared with poly-bounded diodes and demonstrated that STI diodes are more suitable in this technology due to lower on-resistance and parasitic capacitance.

ESD protection diodes in 90 nm CMOS technology were also explored and test structures have been fabricated based on minimum design rules [36]. The results demonstrated that MOS bounded diodes were unsuitable for CDM ESD protection, and poly-bounded diodes had higher current failure per layout area compared to STI diodes. Based on experimental testing for a 6 GHz LNA, STI diodes with 65 μm perimeter junction with an estimated parasitic capacitance of 145 fF are capable of handling 2 kV HBM ESD stress [31]. Poly-bounded diodes were found to have larger junction capacitance (125 fF for a 50 μm junction perimeter diode) compared to STI diodes (20 fF for 25 μm junction perimeter diode) [17]. Furthermore, many researchers [33], [38], [39] attempt to optimize the different layout configurations in order to increase the performance of ESD diodes. As an example, in 90 nm CMOS technology, STI diodes with the octagon and hollow-octagon layouts and a perimeter junction of less than 30 μm have been reported to be capable of handling 2 kV HBM stress and having less than 20 fF of parasitic capacitance [40]. The details of this layout configuration will be discussed in Chapter 5.

In more recent publications, STI diodes were used in 40 nm CMOS technology for a 6 Gbit/s high speed serializer and deserializer I/O application as a preferred solution due to the lower parasitic capacitance [41]. They have achieved an ESD protection level of 2 kV HBM with 135 fF parasitic capacitance; however, the size of the diode has not been reported [41]. In a separate study, 65 nm CMOS technology showed advantages in using poly-bounded diodes with a 40 μm junction perimeter for CDM ESD protection in a low noise amplifier application due to a better turn-on speed compared to STI diodes.

2.5. Research objectives

ESD protection is of a great importance for high-speed mixed-signal and RF applications and STI diodes have proven to be effective ESD protection devices in literature. The objectives of this thesis are:

- To investigate the trade-off between the ESD performance and different geometrical parameters of STI diodes in 0.13 μm CMOS technology
- To optimize the failure voltage (V_{HBM}), the on-resistance (R_{ON}), and the parasitic capacitance (C_{diode}) for the forward I-V characteristic of STI diodes
- To optimize the overshoot voltage (V_{OS}), and the response time (RT) during transient behavior for a CDM event
- To propose a test structure that meets the design target of 2 kV HBM for P+/N-well STI diode with the capacitance of less than 200 fF

This research serves as a framework to develop an ESD solution suitable for deep-submicron scaling for applications in 65 nm CMOS technologies and beyond.

3. Design of STI diodes as ESD protection

Circuit simulations are usually intended only for low voltage operating conditions. Therefore, circuit simulators lack models allowing for characterization of physical properties related to the temperature distribution, current density, and electrical field within a semiconductor device. While experimental testing is possible, it is prohibitively costly and time-consuming. Two dimensional (2-D) device simulators provide a method of creating 2-D cross-sections of semiconductor devices to simulate the electrical and thermal characteristics of a user-defined silicon, oxide, and electrode region of different sizes or doping profiles. In this research, a 2-D physical device simulator, Sequoia Device Designer (SDD), is used to build models of ESD protection diodes under investigation. SDD is a physics based tool which models devices by solving sets of general semiconductor equations such as the Poisson's equation, the current continuity equation, and the Shockley-Read-Hall Generation-Recombination to evaluate device's electrical behaviour. For electro-thermal properties, SDD uses classical heat flow equations to model temperature changes within the semiconductor device due to processes taking place during an ESD event [42].

3.1. Structure definition

The standard 2-D diode device model (Figure 3.1) available in SDD is based on a standard bipolar technology, and must be modified to a standard CMOS technology process. For the purpose of this research, 0.13 μm bulk CMOS technology with shallow trench isolation (STI) and a 17 Å oxide thickness is used [18]. Within the standard CMOS process, two STI diode structures can be built: (a) *P+/N-well* and (b) *N+/P-well*. A *P+/N-well* diode consists of P+ region and N-well region, on top of p-substrate (Figure 3.2a). The size of P+ and N+ regions are defined by STI isolation such that the minimum permitted STI dimension determines the diode lateral size. As for the *N+/P-well* diode, the P+ region and N+ region are located in a p-well rather than n-well (Figure 3.2b).

General information related to the technology process can be found in the technical documents available from the manufacturing foundry, but the doping characteristics are usually not available due to proprietary reasons. Two methods can be used to obtain the doping profile. The first, experimental method, requires fabricated test samples and involves the use of secondary ion mass spectrometry (SIMS) experiments to generate the doping profile. The second, theoretical method, involves the use of a process simulator to arbitrarily define the 2-D doping profiles. Due to the unavailability of SIMS experimental data, process simulations has been used and tuned-up to the available technology data.

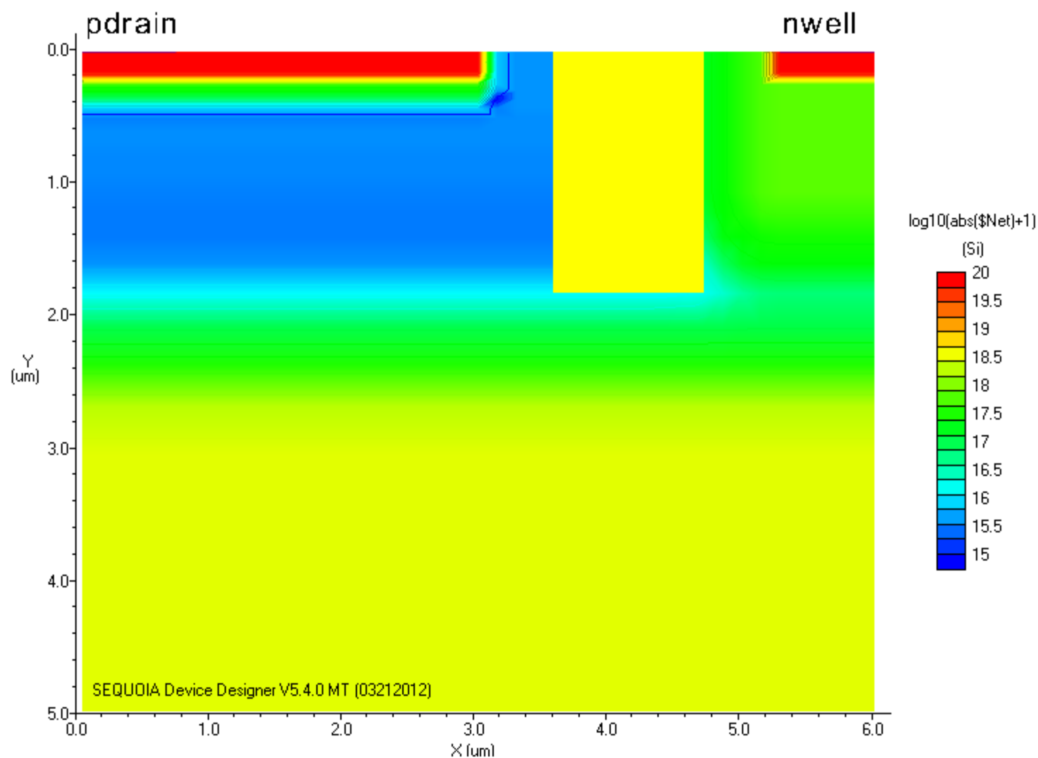


Figure 3.1. Default diode structure from Sequoia Design Designer

The STI diode design parameters available for DSM CMOS process are shown in Figure 3.3 below, which include: the width of the p+ region (W_{p+}), the width of the n+ region (W_{n+}), the spacing between n+ and p+ regions in n-well (W_{np}), and the length of the device in the direction perpendicular to the cross-section of the device (L). Other parameters that are usually not available for designers in the standard process are the depth of STI region (dSTI) and the doping profiles in the different regions of the diode.

The traditional definition of perimeter (P) is the sum of the lengths and widths of the higher doped region multiplied by the number of fingers (n). Assuming the length is much greater than the width, the perimeter can be simplified to twice the length (2L).

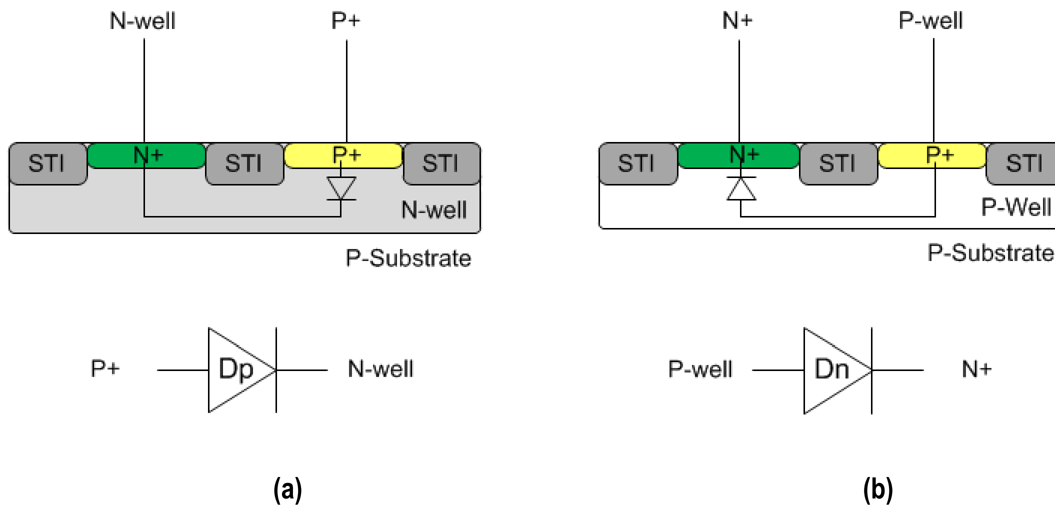


Figure 3.2. (a) Cross-section of P+/N-well diode and (b) N+/P-well diode in DSM CMOS process

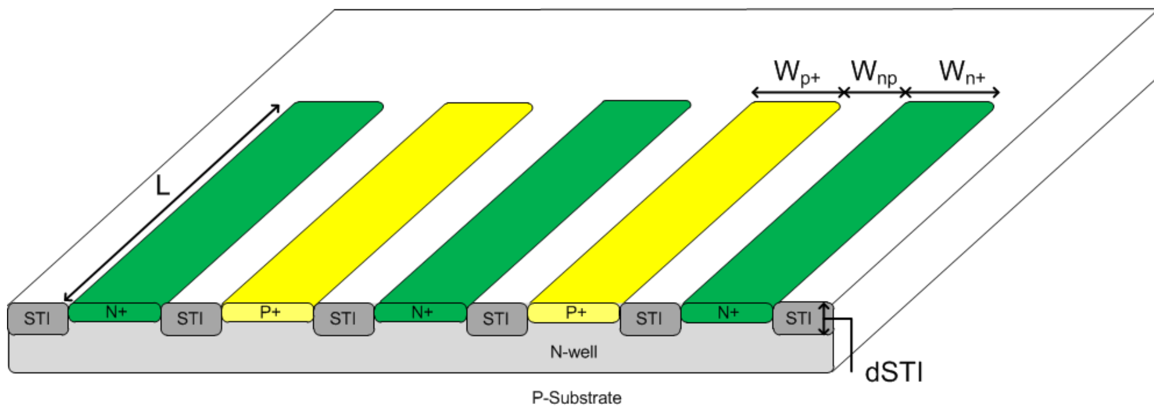


Figure 3.3. The cross-section of the STI diode illustrating diode design parameters

3.2. Calibration of STI diode

In order to verify the accuracy of the model, an initial framework of the 2-D device P+/N-well STI diode model has been created using minimum layout dimensions defined in the process design rules set along with a standard CMOS process doping profile. This model has been subsequently calibrated to mimic the electrical performance of similar

diodes available in literature [18]. The calibration process involves simulating the forward I-V characteristics of three STI diodes of different perimeters: P = 50 μm, P = 100 μm, and P = 300 μm, and comparing the results with the actual TLP data provided in the design manual. As seen from Figure 3.4, the initial model does not agree with the experimental data. After multiple iterations of changing the doping profile densities of the p-well and n-wells, sufficiently good agreement between the experimental TLP characteristic data and the simulated data has been achieved, as presented in Figure 3.5.

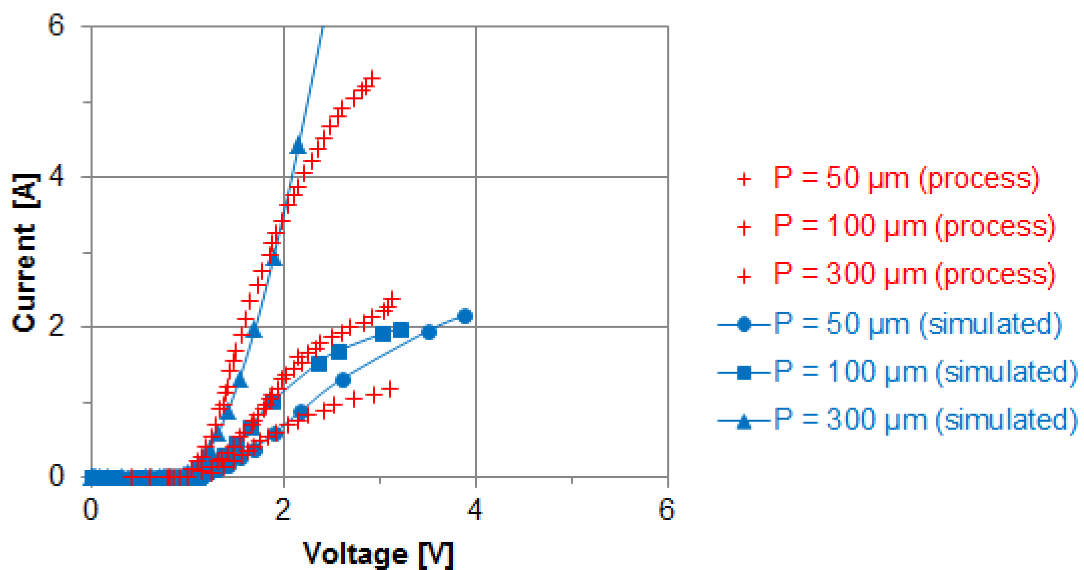


Figure 3.4. The comparison of simulated forward I-V characteristic of a un-calibrated P+/N-well STI diodes with experimental data from [43]

The second part of the calibration process was to match the ESD performance of the STI diode to the failure characteristic presented in literature [18]. Both N+/P-well and P+/N-well diodes with perimeters: P = 20 μm, P = 50 μm, and P = 100 μm were simulated. The HBM setup described in Chapter 1 has been used to simulate the 2-D electro-thermal effects. A sample of the peak lattice temperature for N+/P-well STI diode is shown in Figure 3.6 and the temperature distribution for the same diode is shown in Figure 3.7, with a maximum lattice temperature occurring near the STI corner region. Table 3.1 shows a close fit between the simulated data compared to the tested data published in literature. Due to the similarity in performance of both types of diodes, only P+/N-well diodes were investigated further.

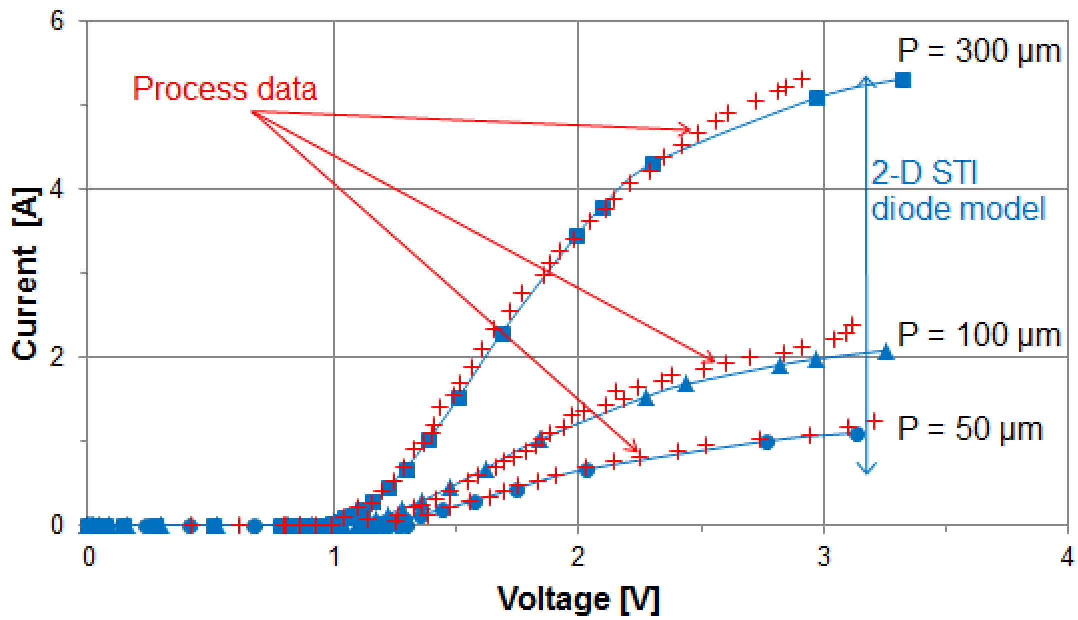


Figure 3.5. The comparison of simulated forward I-V characteristic of a calibrated P+/N-well STI diodes with experimental data from [43]

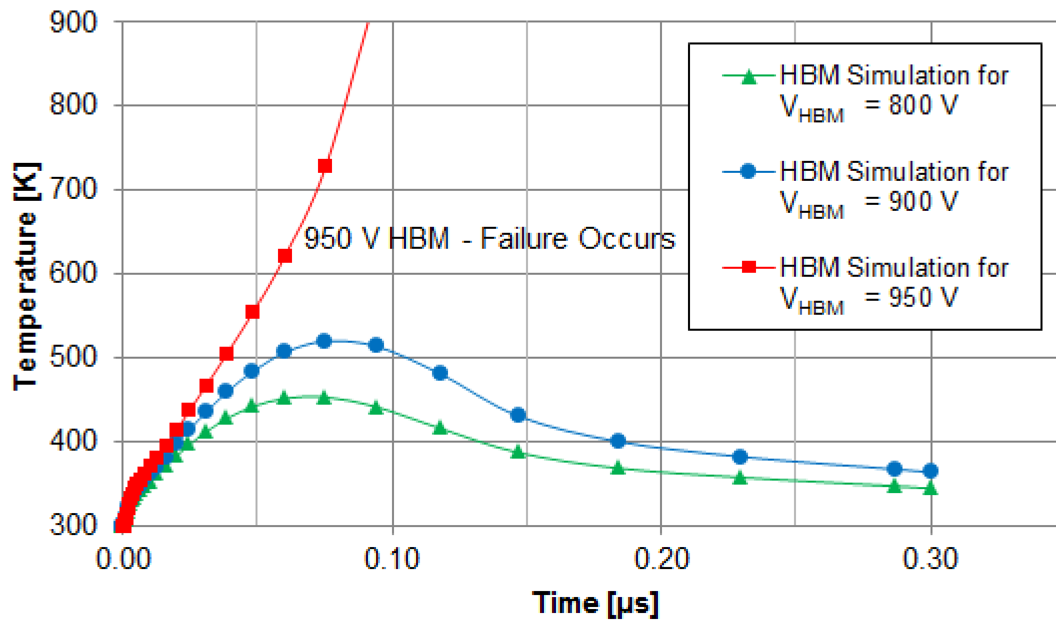


Figure 3.6. Lattice temperature of N+/P-well diode (P = 25 µm) with 950 V HBM failure

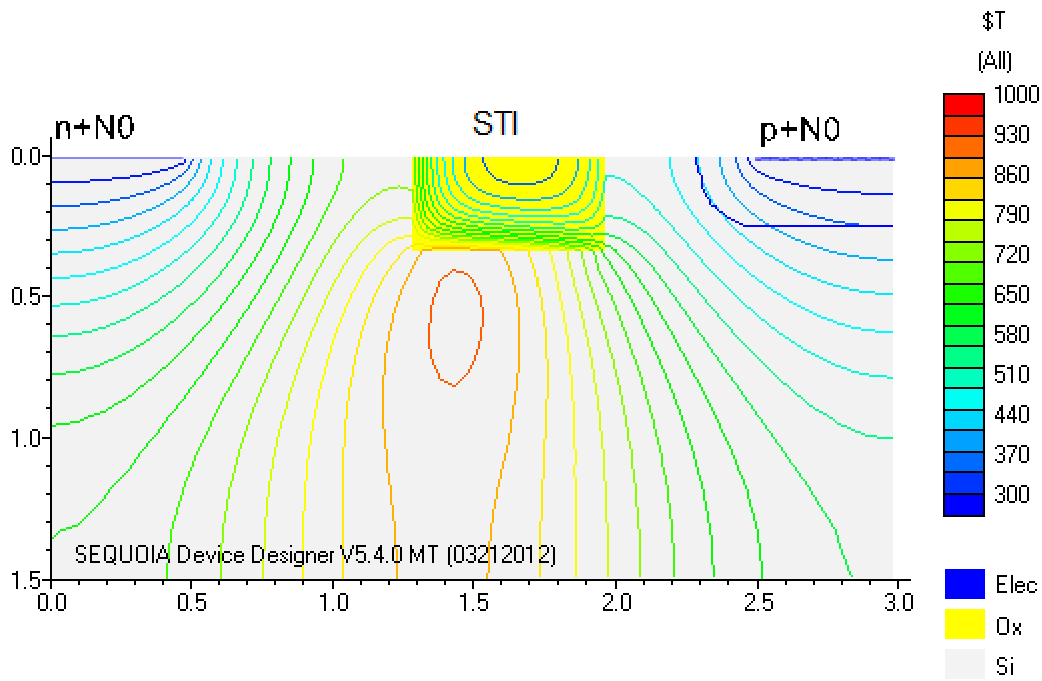


Figure 3.7. Lattice temperature cross section profile of N+/P-well diode (P = 25 µm) illustrating device failure

Table 3.1. Comparison of ESD HBM performance of differently sized ESD diodes: 2-D model vs. experimental data from [18]

Junction perimeter (µm)	HBM ESD level (kV)			Junction perimeter (µm)	HBM ESD level (kV)	
N+/P-well	[18]	2-D Model		P+/ N-well	[18]	2-D Model
20	1.08	0.90		20	1.08	0.85
50	2.16	1.80		50	2.16	1.75
100	4.32	3.65		100	4.32	3.50

4. Investigation of STI diode geometry as ESD protection

In the previous chapter, a 2-D P+/N-well STI diode model with minimum dimensions has been created and calibrated to match both the forward I-V characteristics and the electrothermal failure voltage of experimental results found in literature and information provided by the process manufacturer. With the 2-D STI diode model, each of the different geometry parameters shown in Figure 3.3 is varied independently. Section 4.1 examines the effect of changing the diode's geometries on the standard ESD performance parameters, while Section 4.2 examines the effect of changing the diode's geometries on the advanced ESD performance parameters.

4.1. Impact of STI diode geometry on standard ESD performance parameter

For each of the STI diode parameters discussed in the previous section, a 2-D P+/N-well device model with dimensions of: W_{p+} = 0.50 µm, W_{n+} = 0.75 µm, W_{np} = 1.5 µm, and P = 300 µm has been used to simulate the forward and reverse I-V characteristics. The forward I-V characteristics have been used to extract the R_{ON} parameter, and the reverse I-V characteristics have been used to extract the parasitic capacitance C_{diode}.

4.1.1. Effect of diode's length

The lengths of ESD diodes are often increased to sustain higher levels of ESD stress. A P+/N-well diode have been simulated to determine the impact of the diode's length on the ESD performance parameters with lengths ranging from L = 25 µm to L = 400 µm. The large L value will result in large diode perimeter; this situation requires the use of the multiple-finger type layout which will be discussed in a later section. The

simulations results, shown in Figure 4.1 demonstrate an increase in current handling capability due to the device size increases, which was to be expected due to the increase in device area. The relationship between the HBM failure voltage and R_{ON} has also been studied and presented in Figure 4.2. As the device size increases, R_{ON} decreases and the HBM failure voltage increases, which are both advantageous for ESD circuit protection. Additionally, when the perimeter becomes greater than 300 μm, R_{ON} does not decrease significantly. Based on this study, even if multiple-finger type layout is used, the perimeter should not be scaled greater than 300 μm for the purpose of decreasing R_{ON}, unless a higher HBM failure voltage level is necessary.

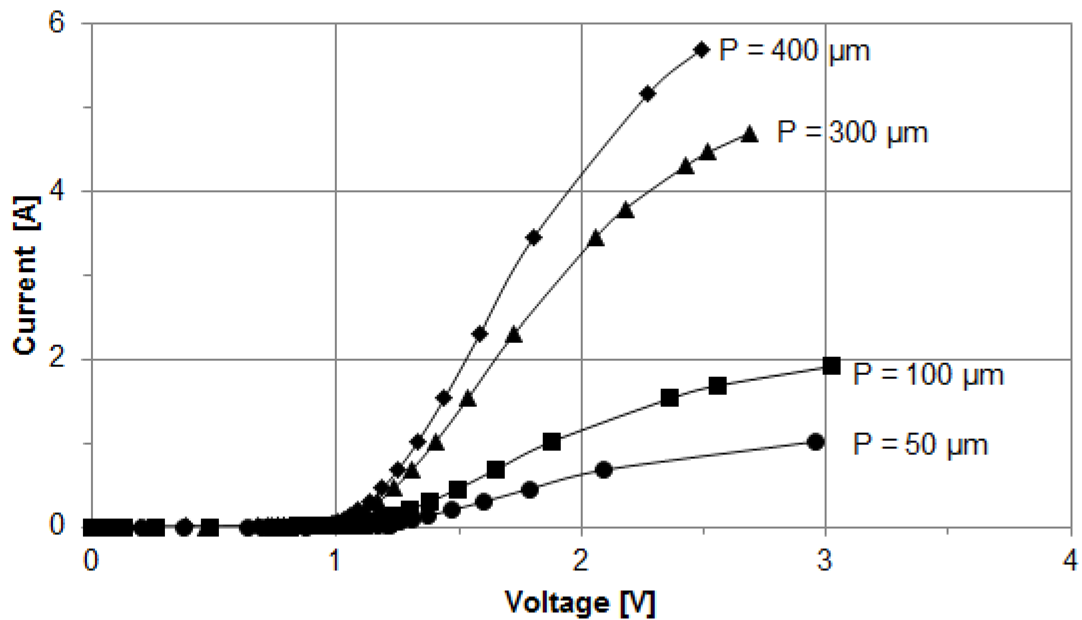


Figure 4.1. Forward characteristic of P+/N-well diodes with different perimeter

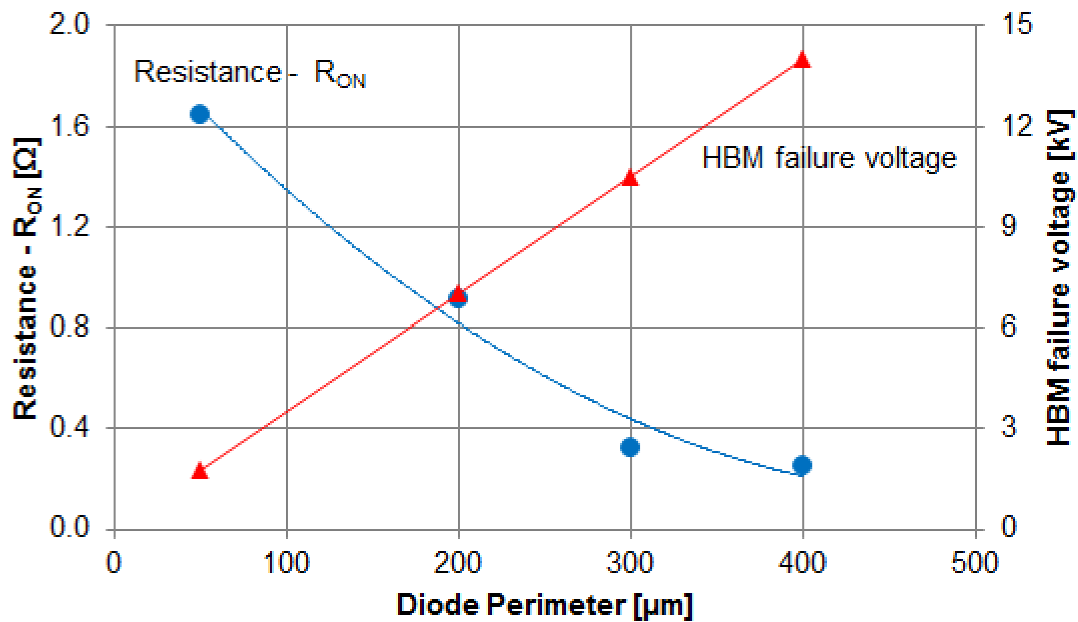


Figure 4.2. HBM failure voltage and R_{ON} of P+/N-well diodes with different perimeter sizes

4.1.2. Effect of p+ region width

Based on both the theoretical and experimental findings for 0.5 µm technology [44], a linear relationship exists between the width of p+ region and V_{HBM}. 2-D device simulation has been used to investigate the impact of the p+ region width varying from W_{p+} = 0.30 µm to 1.8 µm on parasitic R_{ON} and C_{diode}. The simulation results demonstrate that the width of p+ region for P+/N-well diode does not impact on R_{ON} but increases C_{diode} from 66 fF to 199 fF (Figure 4.3). The increase in capacitance is expected due to the increase junction area of the diode.

4.1.3. Effect of the n+ region width

Similarly, the impact of the n+ region width has also been studied by simulating STI diodes varying from W_{n+} = 0.4 µm to 1.8 µm. The result from Figure 4.4 shows that increasing the width of the n+ region decreases R_{ON} from 0.66 Ω to 0.46 Ω, but does not significantly increase C_{diode}. These simulation results confirms the result presented in [17].

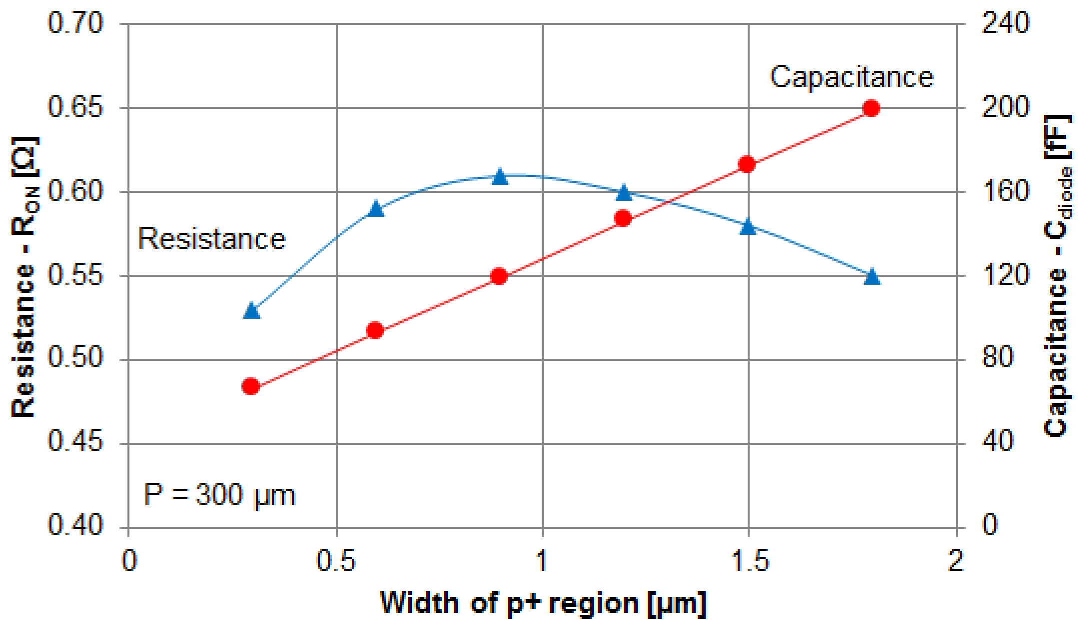


Figure 4.3. Effect of the p+ region width for P+/N-well diode on R_{ON} and C_{diode}

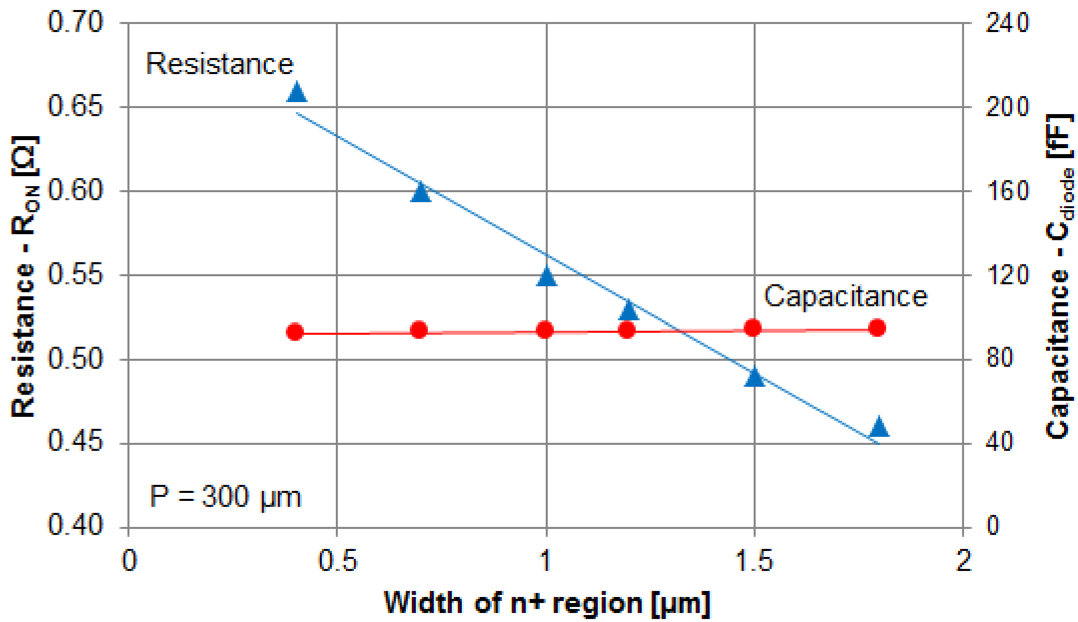


Figure 4.4. Effect of the n+ region width for P+/N-well diode on R_{ON} and C_{diode}

4.1.4. Effect of n+ to p+ spacing in n-well

The spacing between the n+ and p+ regions in n-well have also been studied by performing 2-D device simulations by changing from W_{np} = 1.5 µm to 2.1 µm. From the forward I-V characteristic (Figure 4.5), the n+ to p+ spacing has a negligible impact on R_{ON} for W_{np} = 1.7 µm to 2.1 µm, and minor changes on R_{ON} for W_{np} = 1.5 µm. The simulation results (Table 4.1) also demonstrate that the capacitance has not been impacted due to changes in p+ and n-well spacing. On the other hand, Voldman [44], [45] suggests that the p+ and n+ spacing should be minimized to provide a low resistance path between the p+ and n+ regions, but his experimental results also show that this spacing has minimal impact on the HBM voltage level tolerance.

Table 4.1. Effect of n+ to p+ spacing on C_{diode}

p+ and n-well spacing [µm]	**1.5**	**1.7**	**1.9**	**2.1**
Capacitance [fF]	86.7	86.4	86.1	85.8

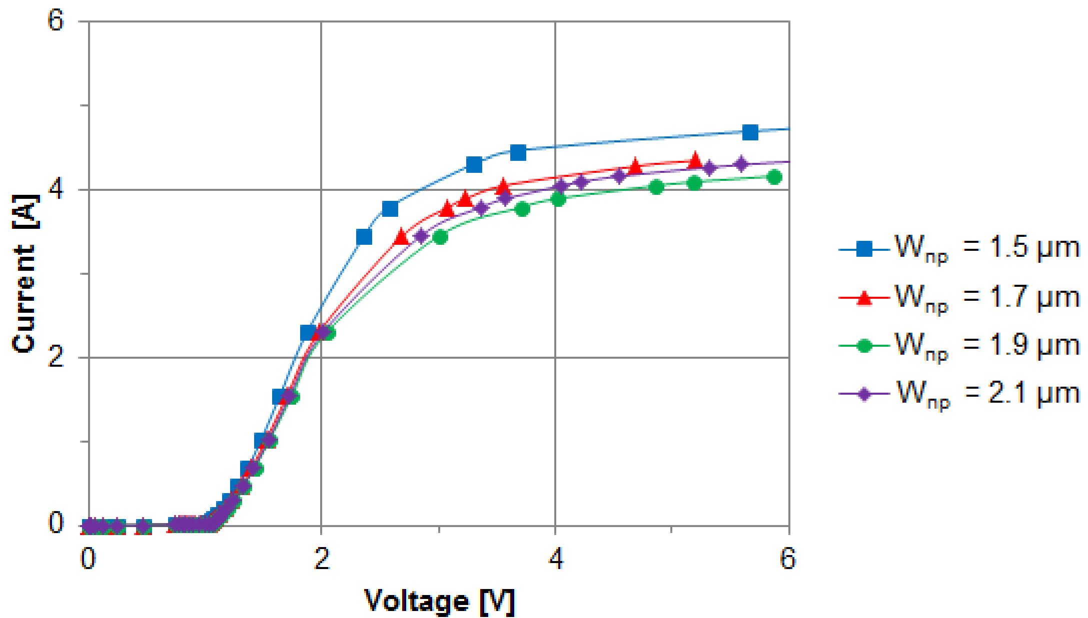


Figure 4.5. Forward characteristic of P+/N-well diodes with different p+ and n-well regions spacing

4.1.5. Effect of the STI depth

The depth of the STI region of a diode is usually fixed in the standard CMOS process, yet process variation may influence this parameter and for this reason the STI depth has been investigated. From the forward I-V characteristics shown in Figure 4.6, R_{ON} can be extracted and the STI depth has marginal impact on R_{ON}. C_{diode} is not impacted by the STI depth variation either (Table 4.2).

Table 4.2. Effect of STI depth on R_{ON} and C_{diode}

STI depth [μm]	**0.30**	**0.35**	**0.40**	**0.45**
R_{ON} [Ω]	0.32	0.35	0.34	0.38
Capacitance [fF]	87.3	87.1	87.0	86.7

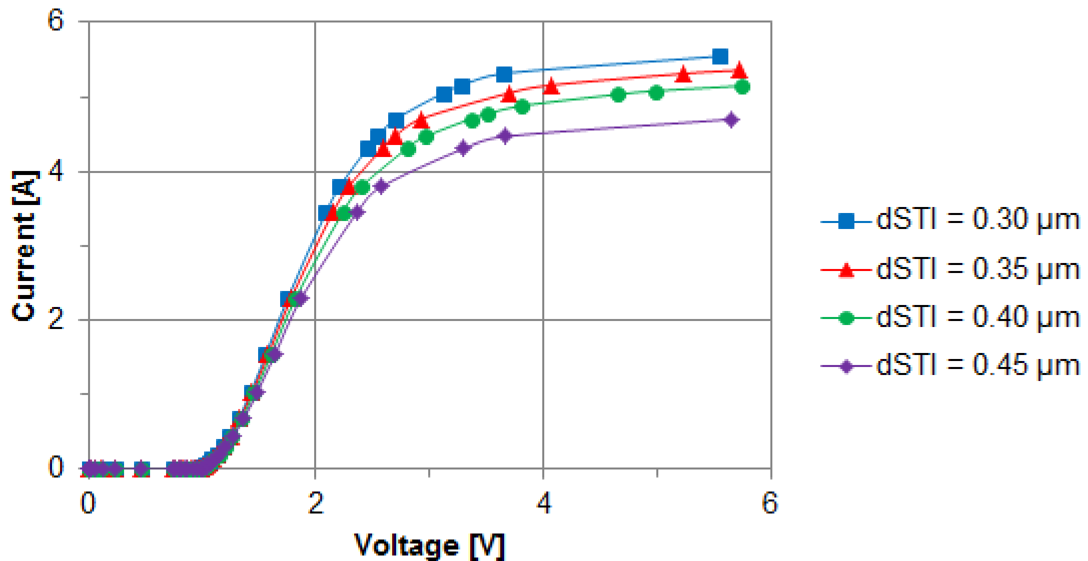


Figure 4.6. Forward characteristic of P+/N-well diodes with different STI depths

4.2. Impact of STI diode geometry on advanced ESD performance parameters in charge device model (CDM) time frame

The 2-D P+/N-well STI diode device model with dimensions: W_{p+} = 0.50 μm, W_{n+} = 0.75 μm, W_{np} = 1.5 μm, and L = 40 μm has been used to simulate the ESD performance in the CDM time domain and to examine the response time (RT) and the overshoot voltage (V_{OS}) with respect to different diode geometries.

4.2.1. Effect of diode's length

The CDM time domain output responses of a 10 V square wave with 55 ps rise time with different lengths are shown in Figure 4.7 and Figure 4.8. As the length increases from 5 μm to 40 μm, the overshoot voltage decreases from 9.44 V to 6.31 V, and the response time also decreases from 1.75 ns to 1.40 ns. From the simulation results, it has been proven that a greater diode length contributes to better ESD performance in the CDM time domain.

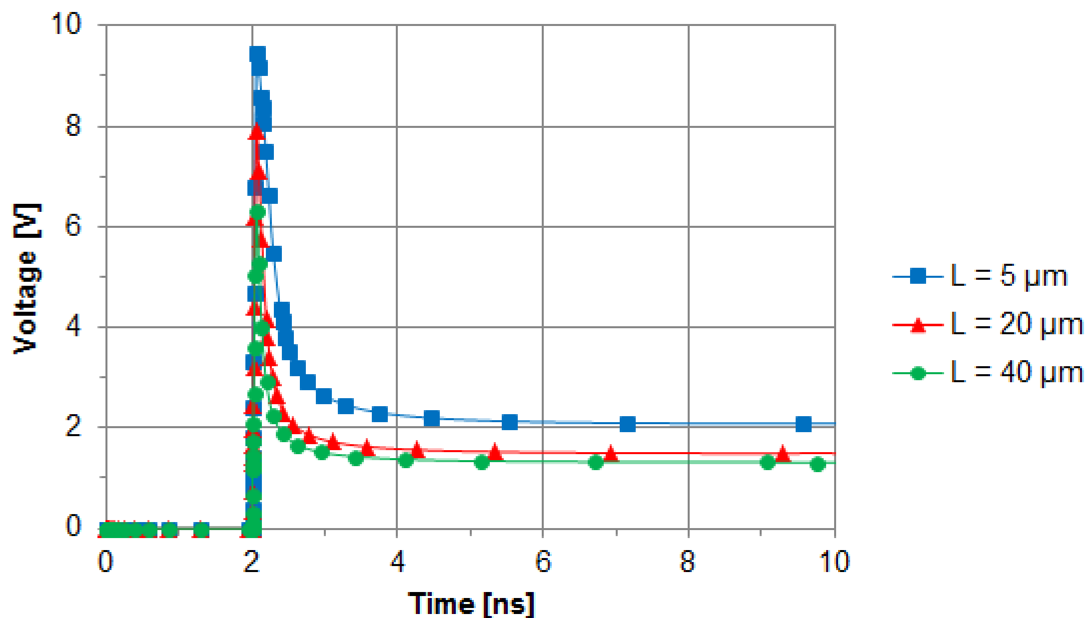


Figure 4.7. Transient response for P+/N-well diode with different lengths

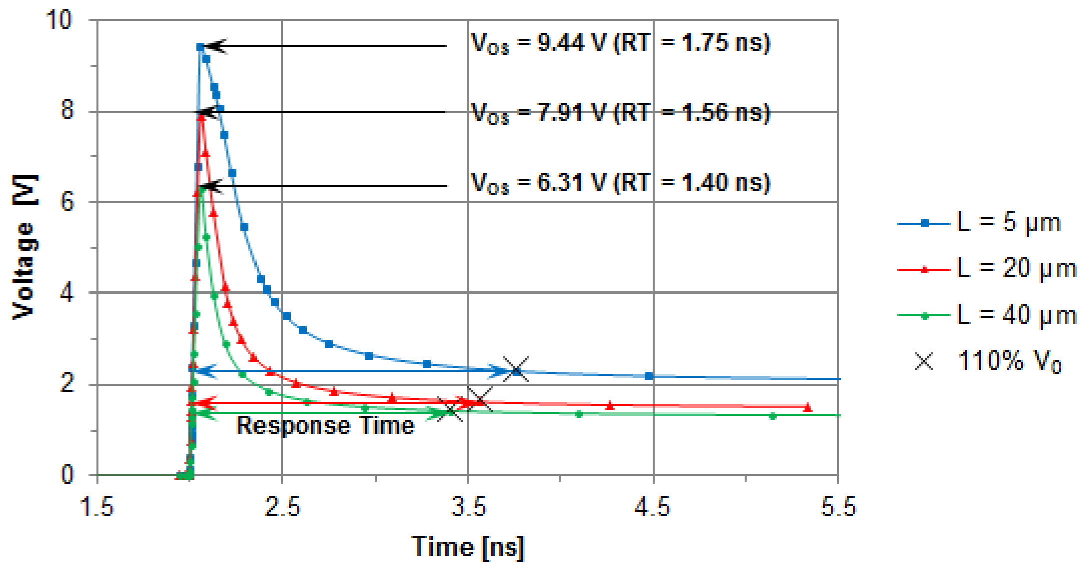


Figure 4.8. Transient response for P+/N-well diode with different lengths (close-up view), where x denotes 110% V_0

4.2.2. Effect of p+ region width

The response time and overshoot voltage are extracted from Figure 4.9. As the p+ region width increases from 0.30 µm to 1.80 µm, the overshoot voltage decreases from 7.84 V to 7.41 V. On the contrary, the response time remains relatively constant around 3.10 ns. Based on this study, an STI diode with a larger p+ region is advantageous for ESD performance in CDM time domain.

4.2.3. Effect of n+ region width

Similarly, as the n+ region width increases from 0.30 µm to 1.80 µm, the overshoot voltage decreases from 7.90 V to 7.60 V, while the response time remains constant around 3.14 ns (Figure 4.10). In order to optimize for lower overshoot voltage and smaller response time, the n+ region width should be maximized.

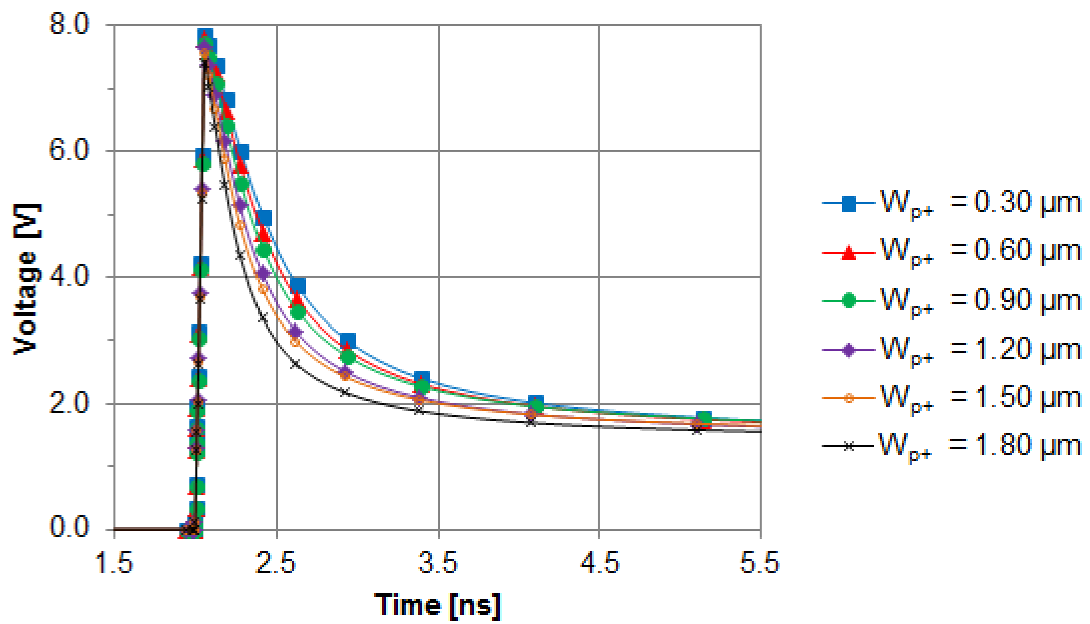


Figure 4.9. Transient response for P+/N-well diode with different p+ region widths

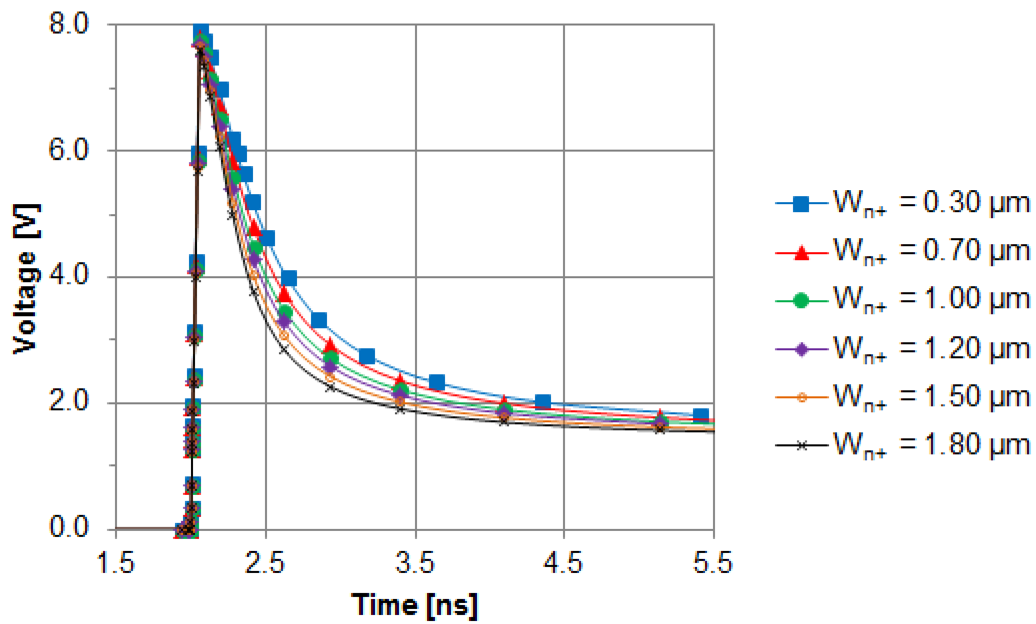


Figure 4.10. Transient response for P+/N-well diode with different n+ region widths

4.2.4. Effect of n+ to p+ spacing in n-well

In contrast, the increase of the n+ to p+ spacing in n-well from 1.50 μm to 2.10 μm results in an increase of the voltage overshoot from 6.84 V to 7.50 V (Figure 4.11). The response time increases from 1.40 ns to 2.10 ns. In order to optimize for ESD performance in the CDM time domain, the n+ to p+ spacing must be minimized to decrease voltage overshoot and response time.

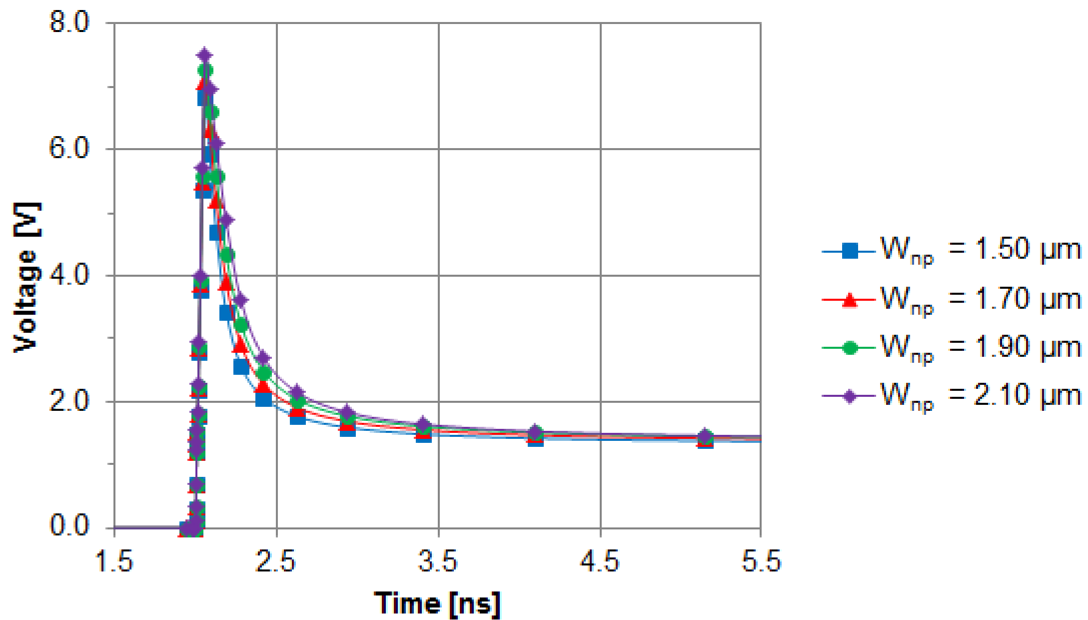


Figure 4.11. Transient response for P+/N-well diode with different spacing between n+ and p+ in n-well

4.2.5. Effect of STI depth

Finally, the voltage overshoot increases from 6.09 V to 6.84 V when STI depths increase from 0.30 μm to 0.45 μm, and the results shows the response time remains constant at 1.40 ns. This simulation result shows the consequence of process variation on the ESD performance in the CDM time. An increase in the STI depth will only impact on a greater voltage overshoot but will not change the response time of the STI diode.

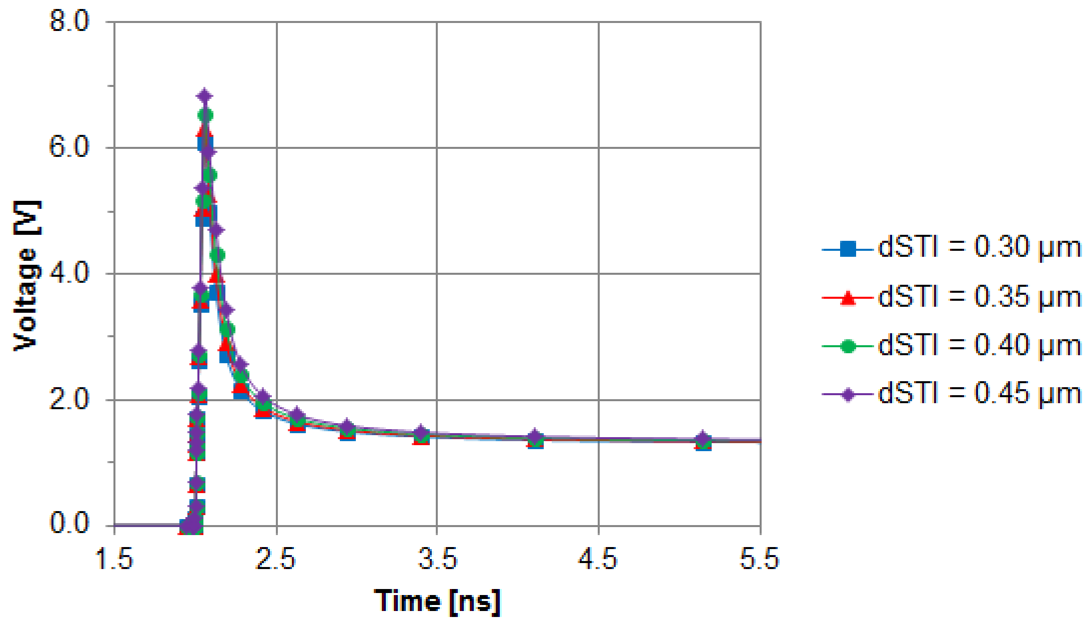


Figure 4.12. Transient response for P+/N-well diode with different STI depths

4.3. Summary

In the previous two sections, STI diodes with different geometries have been simulated, and ESD parameters (such as R_{ON}, C_{diode}, V_{OS}, and RT) have been extracted from the forward I-V characteristics, the reverse I-V characteristics, and the transient response. A junction perimeter of greater than 50 µm is required for 2 kV HBM ESD level protection. Depending on which ESD performance parameters are important, different STI diode geometries should be maximized. For example, to minimize R_{ON}, the STI diode's length and n+ region width should be maximized. In comparison, the length and width of the p+ region of an STI diode should be minimized to reduce C_{diode}. For optimization of V_{OS}, the STI diode's length, p+ region width, and n+ region width should be increased, while the n+ to p+ spacing and depth of STI should be decreased. Finally, in order to minimize RT, the n+ to p+ spacing should also be decreased.

5. Optimization of STI diode as ESD protection

As seen from Table 5.1, there is a trade-off between different ESD performances when increasing the geometry of each of the design parameters. The benefits of increasing the diode's perimeter are higher HBM ESD voltage tolerance, reduced R_{ON}, and lower overshoot voltage, but at the expense of higher C_{diode} and a greater silicon area. By increasing the p+ region width, C_{diode} increases but results in a lower V_{OS} and better HBM ESD voltage tolerance. Interestingly, increasing the n+ region width will decrease R_{ON} and V_{OS} without any negative ESD performance. Finally, decreasing n+ to p+ spacing is beneficial to both V_{OS} and RT. In this chapter, some layout considerations and floor-planning are studied. A final optimization is presented, along with a few test structures satisfying the requirements for high-speed mixed-signal and RF applications.

Table 5.1. Impact of increasing different geometry parameter on the electrical performance of P+/N-well STI diode

Design parameters	Forward I-V characteristic		Fast transient performance	
	R_{ON}	C_{diode}	V_{OS}	RT
Increasing perimeter (P)	↓	↑	↓	↓
Increasing p+ region width (W_{p+})	–	↑	↓	–
Increasing n+ region width (W_{n+})	↓	–	↓	–
Increasing spacing between n+ and p+ regions (W_{np})	–	–	↑	↑
Increase depth of STI (dSTI)	–	–	↑	–

5.1. Layout considerations

Layout optimization for ESD protection devices has been extensively studied in literature [30], [33], [38], [39]. The two most commonly used layout configurations for ESD protection devices are multiple-finger layout configuration and the squared waffle layout configuration (Figure 5.1). The multiple-finger layout configuration consists of one

p+ region surrounded by two n+ regions with the dimensions shown in Figure 5.1a. For P+/N-well STI diodes, the junction area is defined as the area of the p+ region, and the junction perimeter is defined as twice the length of the p+ region (assuming L >> W_{p+}). When the current density is the largest along the perimeter of the p+ region, one option to optimize the ESD figure of merit V_{HBM}/C_{diode} is to maximize the junction perimeter to junction area ratio. As proposed by Velghe [37], the squared waffle layout configuration (Figure 5.1b) can be used to maximize the junction perimeter to junction area ratio. The squared waffle layout configuration consists of a square p+ region, surrounded by an n+ region, with the dimensions shown in Figure 5.1b. Due to the square shape of the layout configuration, the only way to increase the length of the device is to combine two or more of the devices in an array configuration, where the length is n times the width of p+ region; the same applies to the multiple-finger layout.

Two other layouts of interest have also been recently proposed by Yeh and Ker [32]: octagon (Figure 5.2a) and octagon-hollow layout configuration (Figure 5.2b). Experimental results show that the octagon layout has no performance advantages compared to the waffle layout configuration. The study also concluded that an octagon-hollow layout configuration only has better performance in large sizes, compared to the waffle layout configuration. Similarly, from [38], experimental results demonstrated that waffle layouts have better performance compared to multiple-finger layouts due to an increased junction perimeter to junction area ratio. Bhatia and Rosenbaum [39] also concluded that for small widths, the current flow is mainly area-based and not perimeter-based.

In addition to placements of the p+ and n+ regions of the diode, different metal routing schemes has been found to impact the performance of STI bounded diodes [38]. The parallel routing scheme (Figure 5.3a) consists of metal lines placed above the p+ and n+ regions. Metal layer 1 (M1) is strapped with metal layer 2 (M2) in order to lower the on-resistance while also introducing some fringe capacitances. In contrast, the perpendicular routing scheme (Figure 5.3b) places M2 perpendicular to M1. Based on the findings from [39], a large number of short fingers should be used for the parallel routing scheme, but a small number of long fingers should be used for the perpendicular routing scheme. Finally, other studies [46] attempt to reduce the parasitic capacitance between the metal layer and substrate by routing the p+ region with the highest metal

and the p+ region with the lowest metal (Figure 5.4). It should be noted that routing both the p+ and n+ regions with the highest metal will result in higher side-wall capacitance due to the small distance between the via stack. The use of higher level metals also impacts on the series resistance and needs to be carefully selected based on the technology. For example, higher-level metals have thicker lines, which results in smaller metal resistances, but adds extra resistances from the via.

In summary, for the purpose of high speed mixed-signal and RF applications, multiple-finger layout configurations should be used as compared to waffle or octagon-hollow layout configuration because waffle or octagon-hollow layout configurations have higher sidewall capacitances. Furthermore, to lower the parasitic capacitance, the p+ region should be routed with the highest metal layer and the n+ region routed with the lowest metal layer. This will minimize the capacitance between the metal and substrate, as well as the sidewall capacitance between the via.

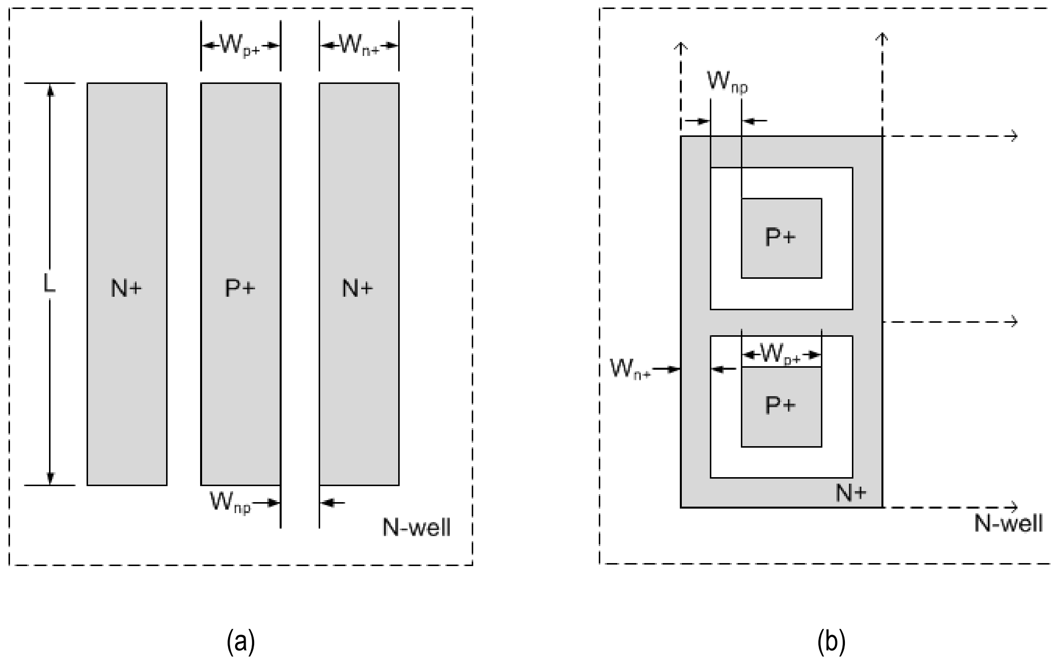


Figure 5.1. (a) P+/N-well STI diode with multiple finger layout (b) squared waffle layout

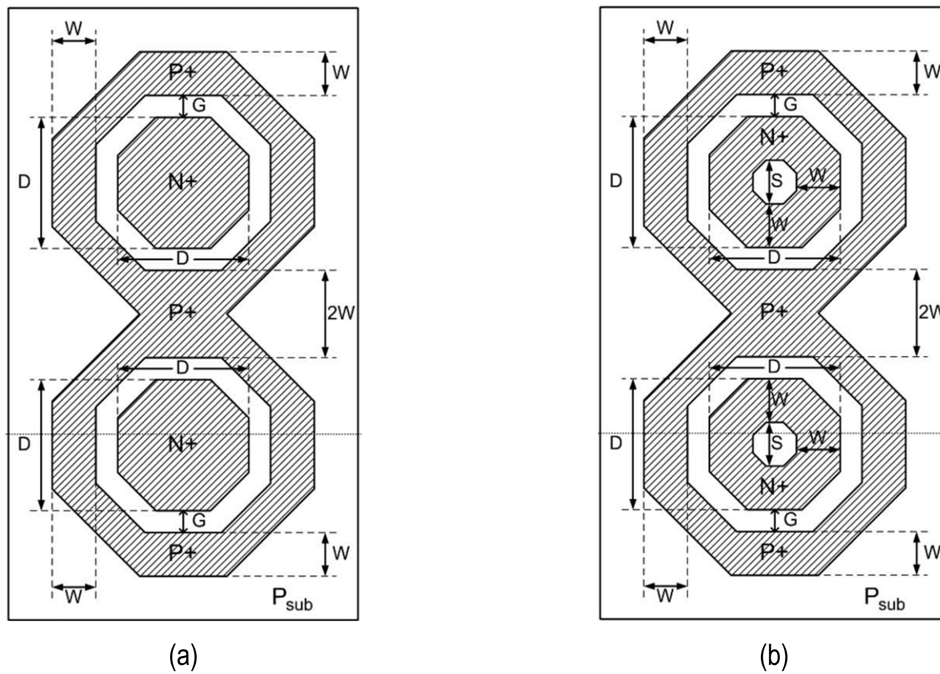


Figure 5.2 (a) N+/P-well diode with octagon layout (b) N+/P-well with hollow-octagon layout [32]

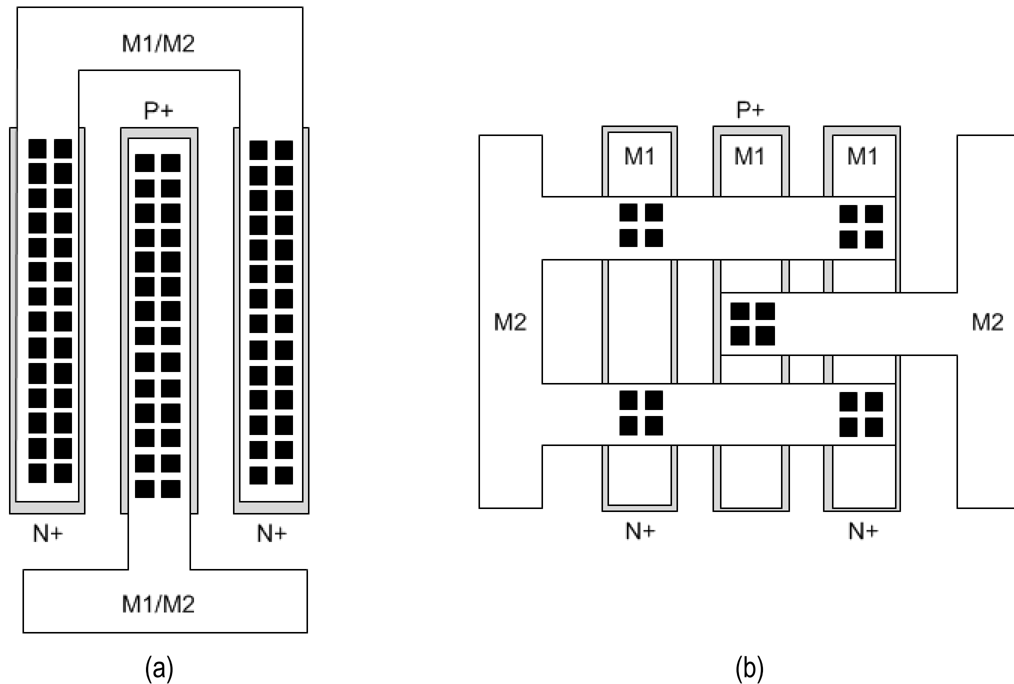


Figure 5.3. (a) P+/N-well STI diode with parallel layout configuration (b) perpendicular layout configuration

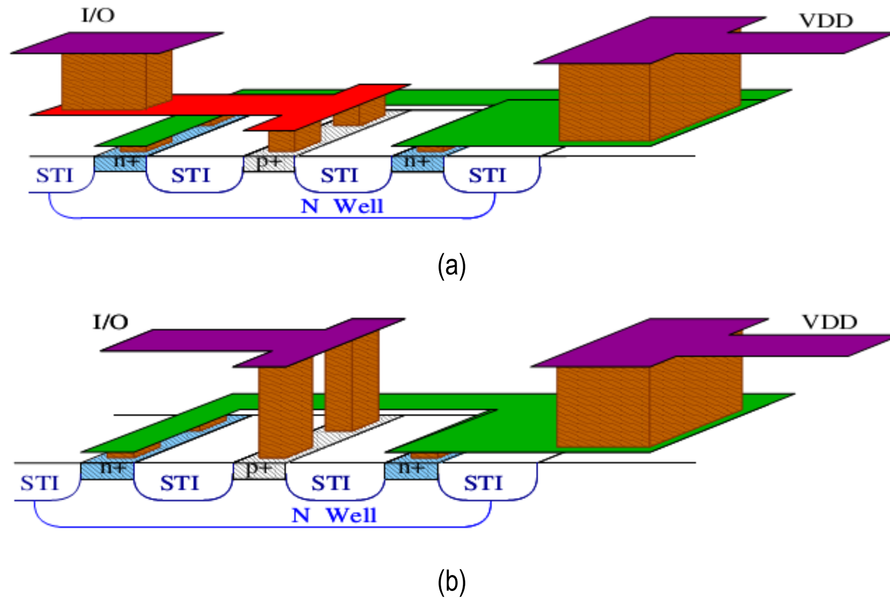


Figure 5.4. P+/N-well diode with (a) typical metal routing (b) higher-level routing [46]

5.2. Optimization study and ESD metrics discussion

Based on the conclusions from the previous sections, eight devices with different combinations of p+ region width, n+ region width, and n+ to p+ spacing are shown in Table 5.2, with an STI depth fixed at 0.35 μm. The junction perimeter has been designed to withstand 2 kV HBM ESD level of protection for high speed mixed-signal and RF applications. These devices have been simulated, and the ESD performance parameters have been examined in more detail to identify the impact of changing more than one design parameter on the overall performance of STI diodes. From R_{ON}, C_{diode}, V_{OS}, and RT, several ESD metrics can be calculated. The RC product ($R_{ON} \cdot C_{diode}$) and HBM voltage failure per unit parasitic capacitance (V_{HBM}/C_{diode}) are used to characterize the suitability of the ESD protection device for high speed mixed-signal and RF applications. As described in previous sections, lower values of R_{ON} and C_{diode} are ideal characteristics of ESD protection diodes. Therefore, the RC product combines the two ESD performance parameters. On the other hand, HBM voltage failure per unit junction perimeter ($V_{HBM}/P_{junction}$) and HBM voltage failure per unit junction area ($V_{HBM}/A_{junction}$) are used to characterize the area efficiency of the ESD protection device. An ideal ESD

diode should have a low RC product, high V_{HBM}/C_{diode}, high $V_{HBM}/P_{junction}$, and high $V_{HBM}/A_{junction}$.

Table 5.2. Junction perimeter and area of diodes with different geometry

Device	Dimensions of device (µm)			Junction perimeter (µm)	Junction area (µm²)	Junction perimeter / junction area
	W_{p+}	W_{n+}	W_{np}			
A	0.3	0.4	2.1	65	9.75	6.67
B	1.8	0.4	2.1	77	69.3	1.11
C	0.3	1.8	1.5	52	7.8	6.67
D	1.8	1.8	1.5	63	56.7	1.11
E	0.3	0.4	1.5	64	9.6	6.67
F	1.8	1.8	2.1	84	75.6	1.11
G	1.8	0.4	1.5	72	64.8	1.11
H	0.3	1.8	2.1	70	10.5	6.67

Referring to Figure 5.5, devices A, D, F, and H have approximately the same on-resistance, but the parasitic capacitance can differ from 11.7 fF to 53.9 fF. Similarly, devices A, C, E, and F have similar parasitic capacitances but the on-resistance can vary from 1.32 Ω to 1.56 Ω. The RC product has been used to determine which devices are suitable for simultaneously optimizing the on-resistance and parasitic capacitance. From Figure 5.6, it is apparent that devices A, C, E, and H have a lower RC product compared to devices B, D, F, and G.

Examining both the V_{HBM}/C_{diode} and $V_{HBM}/A_{junction}$ ESD metrics shows that devices A, C, E, and H are more suitable than devices B, D, F, and G (Figure 5.7). Devices A, C, E, and H have a smaller p+ region width compared to other devices, which yields to a smaller parasitic capacitance (since the parasitic capacitance is proportional to the junction area). Furthermore, the $V_{HBM}/P_{junction}$ ESD metric for P+/N-well STI diodes has values ranging from 24 V/µm to 38 V/µm (Table 5.3). Examining the different ESD metrics concludes that the width of the p+ region is the most important factor that should be optimized first to improve the performance of P+/N-well STI ESD diodes. Next, the advanced ESD performance parameters must be considered. The results show that devices C and E perform better than device A and H in terms of voltage overshoot and

response time. Based on the optimization study, the following two STI diodes are more preferable compared to other devices that were simulated in this section:

- Device C: W_{p+} = 0.3 μm, W_{n+} = 1.8 μm, W_{np} = 1.5 μm, P = 52 μm
- Device E: W_{p+} = 0.3 μm, W_{n+} = 0.4 μm, W_{np} = 1.5 μm, P = 64 μm

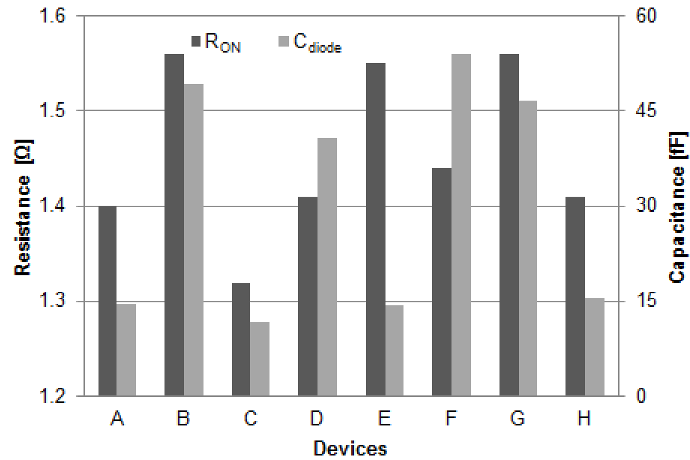


Figure 5.5. R_{ON} and C_{diode} of P+/N-well diodes with different geometries

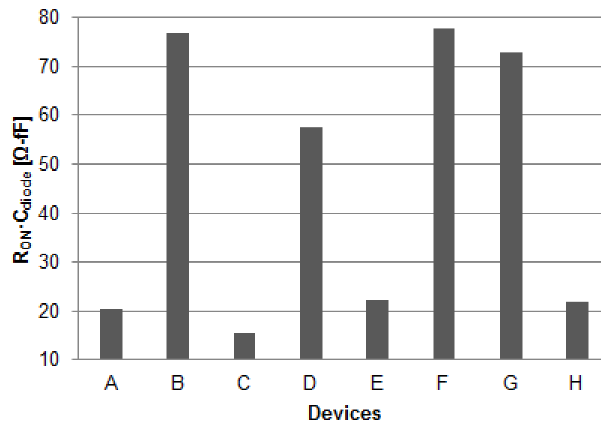


Figure 5.6. The $R_{ON}{\cdot}C_{diode}$ ESD metric for P+/N-well diode with different geometries

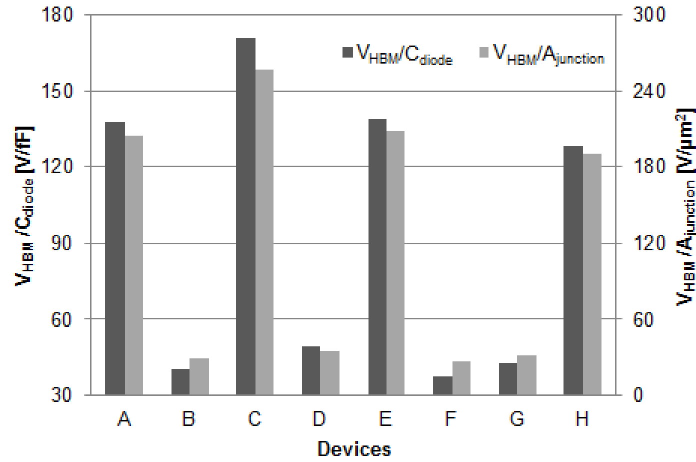


Figure 5.7. The ESD metric of V_{HBM}/C_{diode} & $V_{HBM}/A_{junction}$ for P+/N-well diode with different geometries

Table 5.3. Simulation results and ESD metrics of P+/N-well diodes with different geometry

Device	Simulation parameters				ESD metrics			
	R_{ON} [Ω]	C_{diode} [fF]	V_{OS} [V]	RT [ns]	R_{ON} x C_{diode} [Ω-fF]	V_{HBM}/C_{diode} [V/fF]	V_{HBM}/ junction perimeter [V/um]	V_{HBM}/ junction area [V/um²]
A	1.40	45.5	7.69	2.22	20	138	31	205
B	1.56	49.3	7.43	2.19	77	41	26	29
C	1.32	11.7	7.32	1.56	15	171	38	256
D	1.41	40.8	6.96	1.56	58	49	32	35
E	1.55	14.4	7.06	1.48	22	139	31	208
F	1.44	53.9	7.06	2.07	78	37	24	26
G	1.56	46.6	6.90	1.46	73	43	28	31
H	1.41	15.6	7.37	2.10	22	128	29	190

5.3. Proposed test structures

Two test structures are proposed based on the optimization in the previous section; devices C and E are presented in Figure 5.8 and Figure 5.9 respectively. Multiple-finger layout configuration has been used. Both of these P+/N-well STI diodes have four fingers, with L = 6.5 µm for device C and L = 8 µm for device E. Since the

number of fingers is relatively large, a parallel metal layout configuration should be used. Furthermore, the p+ region should be routed with the highest metal layer and the n+ region routed with the lowest metal to minimize the parasitic capacitance between the metal and substrate.

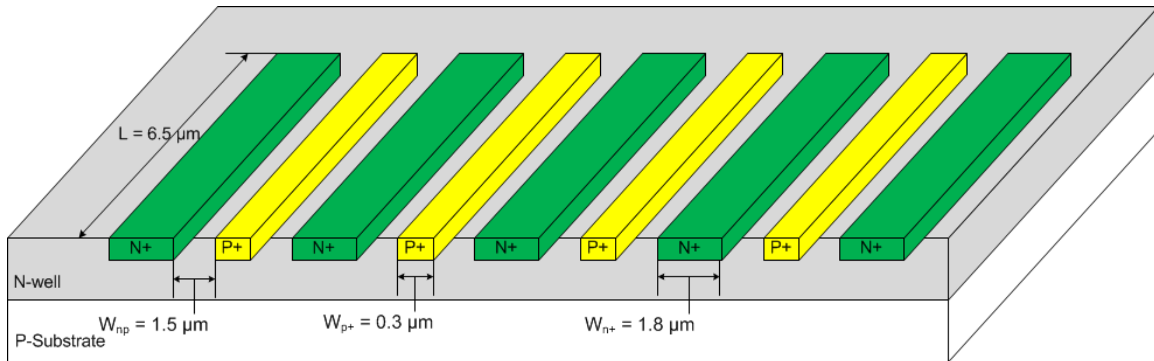


Figure 5.8. Device C with 4 p+ fingers layout

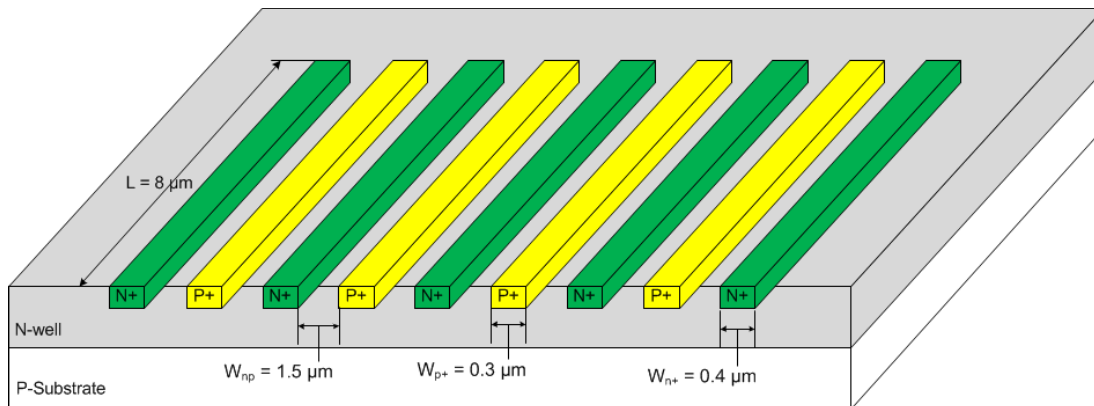


Figure 5.9. Device E with 4 p+ fingers layout

5.4. ESD diode chip integration

Several options are available for integrating STI diodes with the voltage rails and bonding pads. In the standard pad ring configuration shown in Figure 5.10a, each I/O pin is connected to two ESD diodes and a supply clamp. Supply clamps are placed at the corner of the chip, and the signal pads are placed around the core of the chip, as shown in Figure 5.10b. Depending on the availability of chip area, ESD diodes are placed either around signal pads (Figure 5.11 and Figure 5.12) or underneath the signal pad (Figure 5.13). ESD diodes should be placed in an unused area of the chip to reduce the height

or width of the cell. Depending on the particular application and the technology being used, placing ESD diodes underneath the bonding pad is prohibited. For example, in RF applications, placement of ESD diodes under the bonding pad impacts the s-parameter [45].

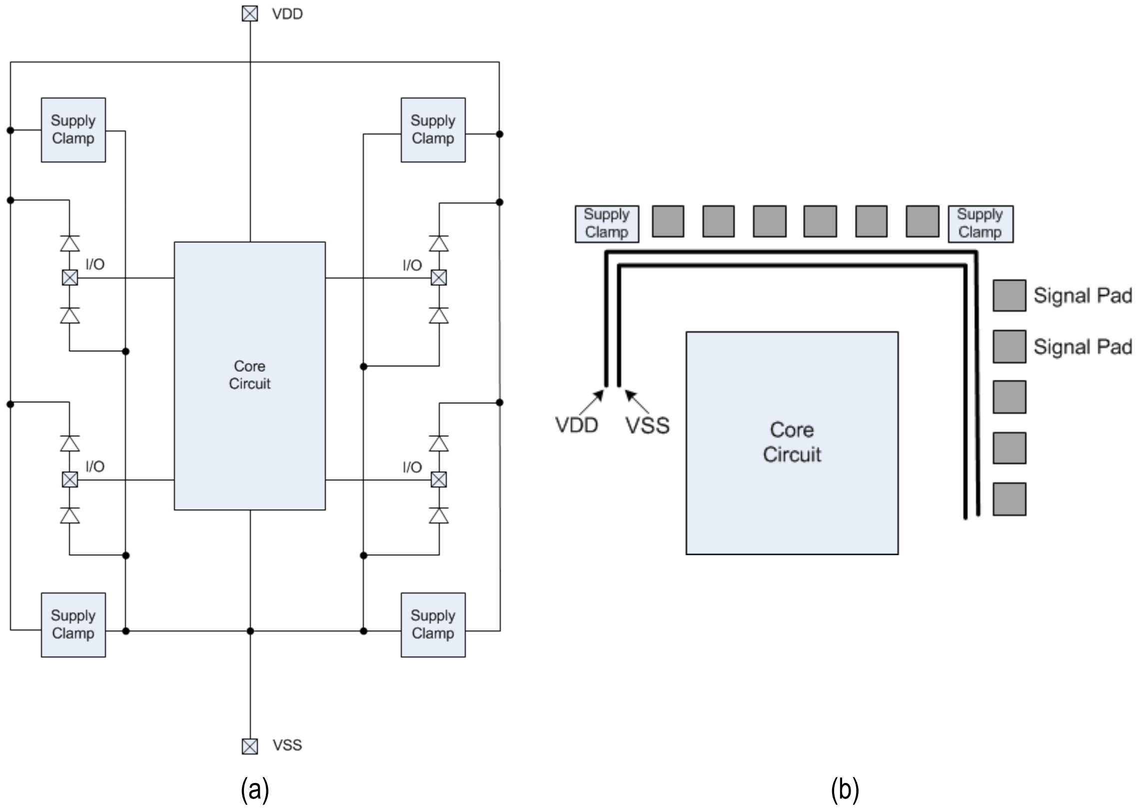


Figure 5.10. (a) Schematic-level ESD protection device for 4 I/O pads (b) corner region of chip

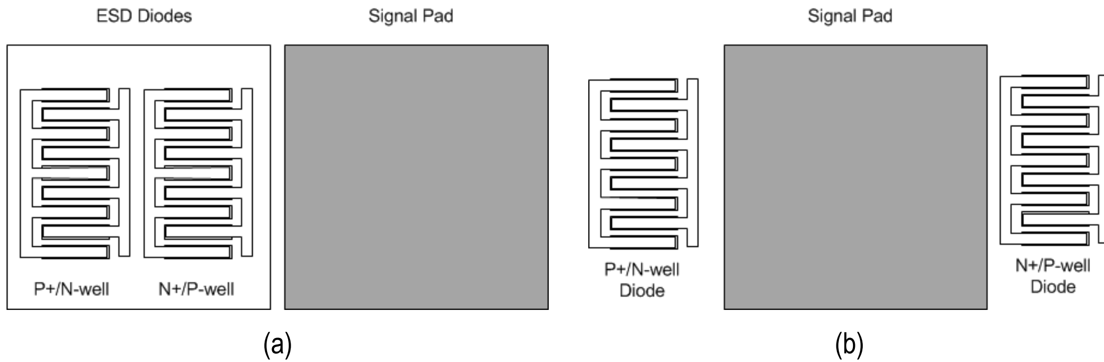


Figure 5.11. (a) ESD diodes next to bonding pad (b) ESD diodes split by the signal pad

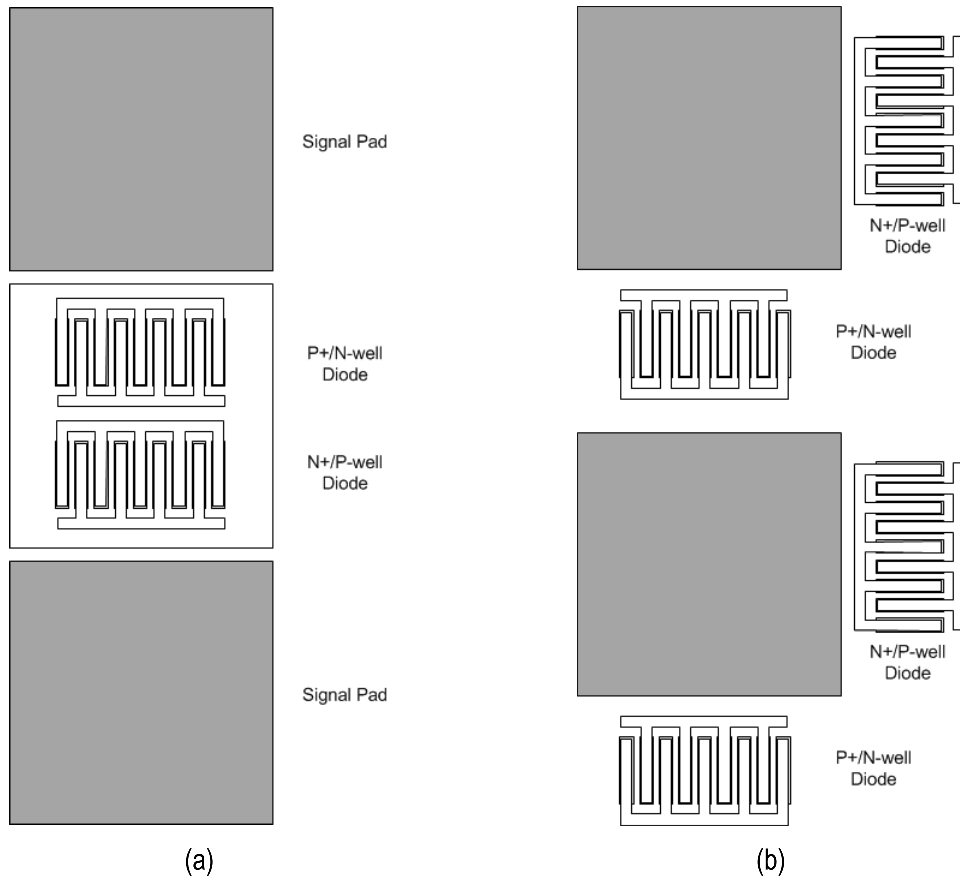


Figure 5.12. (a) ESD diodes between bonding pads (b) ESD diodes split between bonding pads

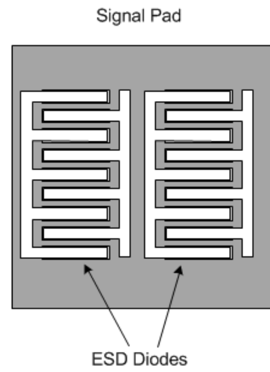


Figure 5.13. ESD diode placed underneath bonding pad

6. Conclusion

This thesis presented a methodology for designing ESD STI diodes for high speed mixed-signal and RF applications in 0.13 μm DSM CMOS technology. A 2-D P+/N-well STI diode device-level model has been created in Sequoia Device Designer and verified with experimental results published in literature. Using the standard human body model and charge device event model, different geometric design parameters of the STI diode has been optimized based on several ESD metrics.

Simulation results show that the width of the p+ region and n+ region must be minimized to achieve good ESD performance. The spacing between the p+ and n+ region does not significantly impact on the forward and reverse characteristic of the STI diode but affects the overshoot voltage and response time, which are two very important ESD performance parameters in the CDM time domain. Two STI diode test structures with multiple-finger layout have been proposed with junction perimeters of 52 μm and 64 μm, capable of handling an ESD performance target of 2 kV HBM protection level. Higher level metals have been used to route the p+ regions, and lower level metals to route the n+ regions in order to reduce the parasitic capacitances between the metal layer and substrate.

The use of 2-D device simulations during early stages of the design process has been proven to be advantageous in evaluating the performance of STI diodes intended for high speed mixed-signal and RF applications in DSM CMOS technologies. This methodology can be used to aid the design of ESD protection devices in 45 nm CMOS technology and beyond to reduce the development cost and time of new CMOS IC chips in DSM technologies.

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