# On-Chip Time-Domain Metrology Using Time-to-Digital Converters and Time Difference Amplifier in Submicron CMOS

**by**

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# Abstract

Over the past few decades, the advancement in the deep-submicron CMOS process technology has dramatically improved the performance and functionality of modern System-on-Chips (SoC). However, as the complexity and operational speed of today's SoCs increase, characterizing the timing performance of SoCs is becoming more challenging. Embedded measuring techniques for system characterization are therefore becoming necessities. A Time-to-Digital Converter (TDC) is a device that has been widely used for on-chip time measurements due to its excellent reliability and precision. However, accurate TDCs are few and most implementations are challenging, especially for the time resolution of 10ps and below. In this thesis, a new single-stage Vernier Time-to-Digital Converter (VTDC) has been implemented using 0.13μm IBM CMOS technology, and analyzed using HSPICE simulator in Cadence Analog Design Environment. The single-stage VTDC presented in this work utilizes a dynamic-logic phase detector and a Time Difference Amplifier (TDA). The zero dead-zone characteristic of dynamic-logic phase detector allows for the single-stage VTDC to deliver sub-gate delay time resolution. At the same time, the constant gain TDA further improves the VTDC's resolution by pre-amplifying the input time intervals. The developed single-stage VTDC with TDA has demonstrated a linear measurement characteristic for an input dynamic range from 0 to 100ps with a 2.5ps time resolution.

**Keywords:** On-chip Time Measurement, Time-to-Digital Converter, and Time Difference Amplifier

*To my family…*

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# Table of Content

# List of Figures

# List of Tables

# Glossary

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| BIST | Built-In Self-Test |
| CMOS | Complementary Metal Oxide Semiconductor |
| DIP | Delayed-Input Pulse |
| DLL | Delay Locked Loop |
| PLL | Phase Locked Loop |
| INL | Integral Nonlinearity |
| DNL | Differential Nonlinearity |
| LSB | Least Significant Bit |
| NMOS | N-channel Metal Oxide Semiconductor |
| PFD | Phase Frequency Detector |
| PD | Phase Detector |
| PET | Positron Emission Tomography |
| PMOS | P-channel Metal Oxide Semiconductor |
| PVT | Process, Voltage, and Temperature |
| TDA | Time Difference Amplifier |
| TDC | Time-to-Digital Converter |
| TOF | Time-of-Flight |
| VCDL | Voltage Controlled Delay Line |
| VTDC | Vernier Time-to-Digital Converter |

# CHAPTER 1 INTRODUCTION

Verification of integrated circuits (IC) is an important step of VLSI production which ensures the performance and functionality of the products. However, as the operational speed and complexity of today's System-on-Chips (SoC) increase, measuring and characterizing the timing performance of SoC's building blocks are becoming more challenging. Embedded measuring techniques for system characterization, such as Built-In Self-Test (BIST), are therefore becoming necessities. In order to precisely characterizing high speed SoC, several new embedded time measurement techniques have been developed. This chapter describes an overview of on-chip time metrology, introduces the concept and parameters of Time-to-Digital Converter (TDC) and Time Difference Amplifier (TDA), and summarizes the content of this thesis.

## 1.1. Motivations and Overview

Over the past few decades, the submicron CMOS technology development has been progressing rapidly. The advancement in the process technology has allowed IC designers to create SoC's with more functionalities and faster operational speeds. As the operational speed and complexity of the modern SoC increase, IC manufacturers face many new challenges, which include developing effective solutions for measuring and characterizing timing performances of ICs.

Conventionally, verification of IC performance is performed using external automated test equipment (ATE), as shown in Figure 1.1. In an industrial verification setup, the device-under-test (DUT) is placed on the device-interface board. The tester mainframe generates the pre-programmed testing signals and applies the testing signals through the input test heads to the DUT while the output test heads captures the outputs from the DUT.

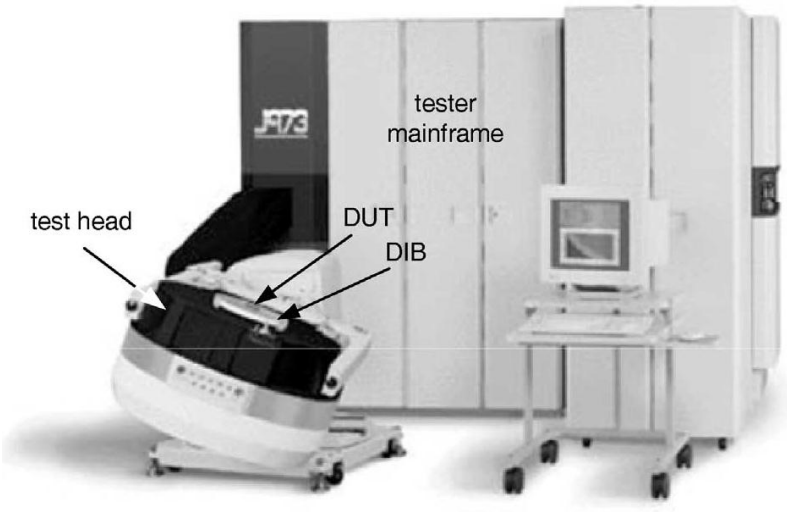



Figure 1.1: Typical mixed-signal VLSI production tester [1]

ATE's like the production testers are designed using electronics with higher speed and better noise performance than CMOS technology, such as gallium arsenide. Hence, they are capable of providing more accurate measurements. However, the increased integration and performance of modern SoC have produced limitations in the traditional verification processes. For example, attenuation and skew caused by bonding wires, electrostatic discharge (ESD) circuitries, and test heads deteriorate the accuracies of the measurements [1]. It is difficult for production testers to provide effective accuracies for characterizing multi-gigahertz SoCs. Verification processes that use external testing

equipment have another drawback. As the packing density and complexity of today's SoC continuously increase, routing deeply buried signals to the chip boundary for testing measurements also becomes impractical. Moreover, production testers require careful system calibrations and regular maintenances. Verification processes using ATE are therefore becoming more expensive and impractical for characterizing high speed SoC's. This has driven IC manufactures to develop more cost-effective and feasible verification processes.

As an alternative to verification process using ATE, embedded time measuring techniques for SoC characterization, such as Built-In Self-Test (BIST), are the more effective methods [2]. Unlike the external ATE, the embedded measuring circuitries are designed to be located close to the DUT. The attenuations and skew on the measuring signals are minimized, and the length of the routing wire can also be much shorter to reduce any loading effects. Time-to-Digital Converter (TDC) and Time Difference Amplifier (TDA) have been widely used for on-chip time measurements and time signal processes. A TDC can quantize time intervals between two or more consecutive signal events to digital outputs, allowing precise on-chip time measurements; while, TDA can be integrated with TDC to magnify the input time intervals and enhance the measurement accuracy. The integration of on-chip TDC and TDA can effectively measure timing parameters, such as jitter, skew, and delay. Figure 1.2 shows the common setup of TDC with TDA.

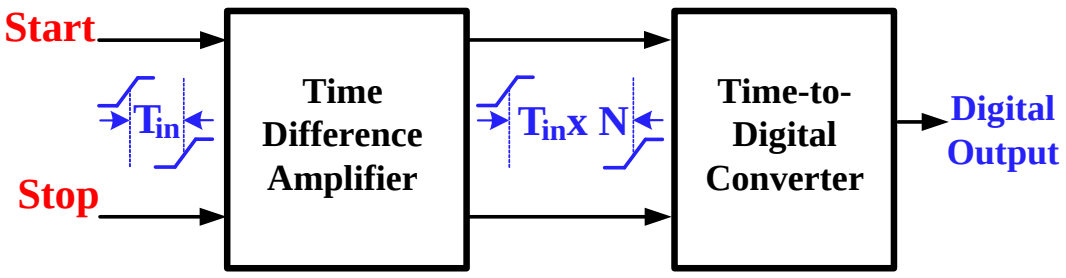



Figure 1.2: Concept of time-to-digital converter with time difference amplifier setup

The input time interval between signals *Start* and *Stop*, $T_{in}$, is first pre-amplified by the TDA with a gain of N. The amplified time interval, $T_{in}$×N, is then measured using the TDC. With the digital output generated by the TDC, the input time interval can be determined using the equation like the following:

$$T_{in} = \frac{Resolution_{TDC}}{N} \times Digital\ Output \tag{1.1}$$

The excellent measurement accuracy and performance in on-chip time measurement have made TDC and TDA popular devices in a multitude of applications. With different performance parameters, TDC and TDA have been utilized in applications of laser range-finding, nuclear science, Phase Locked Loops (PLL), and Analog-to-Digital Converters (ADC). In the applications of laser range-finding, TDCs have been used in laser range finders to measure the time for a laser beam to reach an object and to bounce back. TDCs with time resolutions around 6.5ns can be implemented in hand-held range finding devices to provide a minimum measuring resolution of 1m [3]. In nuclear science, TDCs are commonly used for measuring the Time-of-Flight of particles and the lifetime of positrons [4]. The applications of TDCs in nuclear sciences can also be found in nuclear medical imaging systems, such as Positron Emission Tomography (PET) and Single-

Photon Emission Computed Tomography (SPECT) [5,6]. These medical imaging systems utilize semiconductor radiation detector such as Cadmium Zinc Telluride (CZT) radiation sensors to convert X-ray or Gamma-ray photons into electron and hole pairs. The TDCs are used in these systems to measure the drift times of electron and holes to the electrodes and hence to analyze gamma photon event depth, as shown in Figure 1.3. The typical time resolutions of TDCs required in these nuclear science applications range from few hundred picoseconds to few nanoseconds.

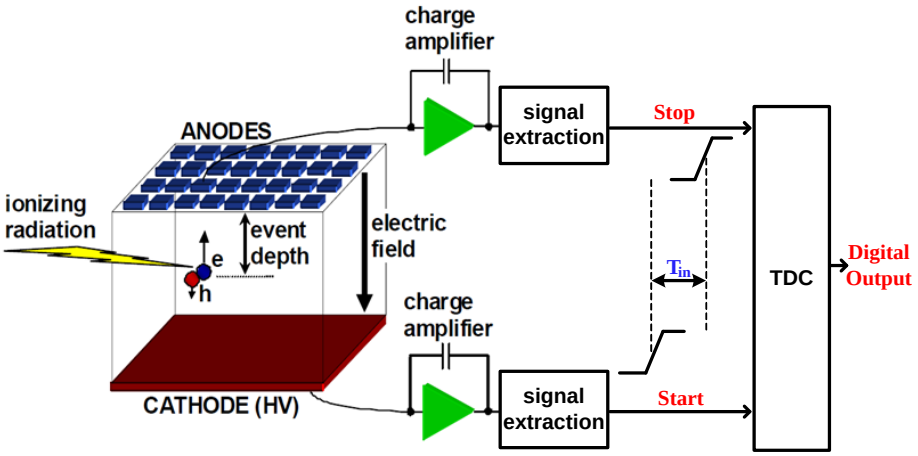



Figure 1.3: TDC application in CZT radiation sensor

The time resolution of the TDC has greatly improved due to the advance in TDC architectures and the CMOS technology. TDCs with the time resolutions in the order of tens of picoseconds are implemented as sub-blocks to improve the performance of all-digital Phase Locked Loops (PLL) [7] and Analog-to-Digital Converters (ADC) [8]. In order to explore this area, this thesis will focus on researching and developing TDC architectures with picosecond time resolutions which can be utilized in a variety of applications, from nuclear medical imaging to PLLs and ADCs.

## 1.2. Operations and Parameters of Time-to-Digital Converter

A TDC is a device that quantizes time intervals between two or more consecutive timing events and converts them to digital output values. Figure 1.4 shows the block diagram of a general TDC, where a time interval between *Start* and *Stop*, $T_{in}$, is being measured using a TDC.


Figure 1.4: Block diagram of general TDC

The input-output characteristic of an ideal TDC is given by a quantizer characteristic shown in Figure 1.5. The input time interval, $T_{in}$, being measured is plotted on the x-axis, and the corresponding digital output is represented by the y-axis.

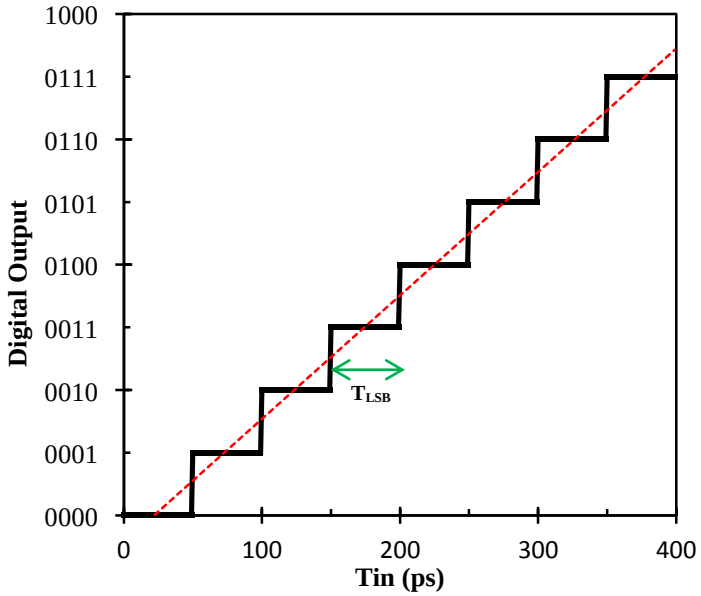



Figure 1.5: Ideal TDC input-output characteristic with a 50ps time resolution

With the digital output of TDC, the input time intervals can be determined using the following equation:

$$T_{in} = Resolution_{TDC} \times Digital\ Ouput \tag{1.2}$$

Many TDC architectures have been developed to meet requirements of different applications. In order to characterize the performance of TDCs, a set of unique parameters has been defined. The essential TDC parameters are introduced below.

***Time Resolution***

The time resolution of the TDC is the smallest time interval that can be distinguished by a TDC. It is sometimes also referred as the Least Significant Bit (LSB) of a TDC, as shown in Figure 1.5. TDCs with smaller time resolutions enable measurements of time intervals with lower quantization errors and achieve better measurement accuracies.

***Input Dynamic Range***

The input dynamic range of TDC is the time interval range that TDC can accurately measure. It is also sometimes referred as TDC dynamic range for simplicity. The input dynamic ranges of TDCs can vary dramatically with different TDC architectures. More TDC architecture design tradeoffs will be discussed in Chapter 2.

***Non-Linearity Error***

TDCs suffer from non-linearity error caused by layout mismatches and noise, causing the output characteristics to deviate from a linear function of input time intervals. These errors can be minimized in some TDC architectures [9,10,11], but they cannot be completely eliminated. The non-linearity errors of TDCs are often evaluated in terms of

Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). The DNL of TDC is a measure of the separation between adjacent codes measured at each vertical step in LSBs. On the other hand, the INL of TDC is the maximum difference between the actual time resolution characteristic and the ideal time resolution characteristic measured vertically and expressed in LSBs. Low DNL and INL errors of TDCs indicate linear input-output characteristic. The INL and DNL are most sensitive to temperature, noises, and process variation; therefore, they are often only measured with the actual chip, but not simulated intensely throughout the design process.

***Measurement Rate***

The measurement rate of TDC is the speed of converting input time intervals to digital output values in a continuous conversion mode. It is sometimes referred as the frequency of TDC and often being evaluated in sample per second or hertz. For example, TDC that takes average 100ns to convert one time interval is said to have a measurement rate of 10MHz.

## 1.3. Operations and Parameters of Time Difference Amplifier

A TDA is an integrated circuit that magnifies the input time interval between edges of two consecutive signals by a gain factor, N. Figure 1.6 shows the block diagram of common TDA, in which the time interval between two input signals has been amplified N-times using TDA.

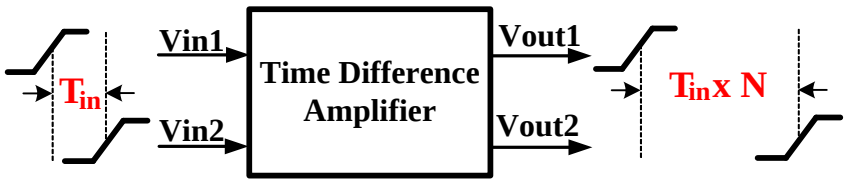



Figure 1.6: Block diagram of general TDA

An ideal TDA should have a linear input-output characteristic with a constant gain throughout all the input time interval ranges, as shown in Figure 1.7. The input time interval, $T_{in}$, is plotted on the x-axis, and the amplified output time interval is represented by the y-axis.

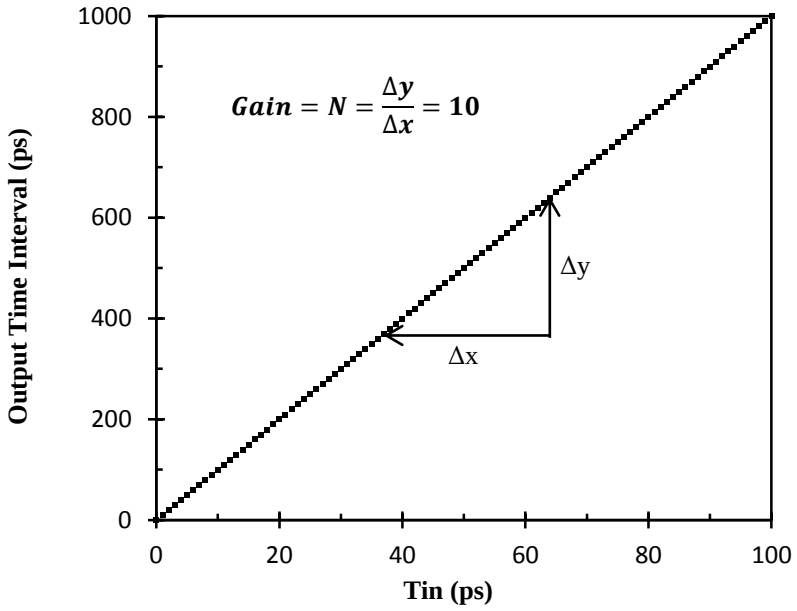



Figure 1.7: Ideal TDA input-output characteristic with a gain of 10

With an ideal gain, the output time interval of a TDA can be determined using the following equation:

$$T_{output} = \mathrm{N} \times T_{in} \tag{1.3}$$

Some performance parameters of TDA are essential when utilizing TDA for enhancing TDC's time resolutions. These TDC parameters are introduced below.

***TDA Gain***

The TDA gain is a measure of the ability of TDA to magnify an input time interval to an output time interval. The gain of TDA is defined as the ratio of the output time interval to the input time interval, as shown in Figure 1.7. Unlike the gains of voltage or current amplifiers, the gain of TDA refers to the magnifying factor in time domain.

***Time Offset***

The time offset of TDA is the amount of output time interval when a zero input time interval is applied to the TDA, as shown in Figure 1.8. Although the time offset of an ideal TDA is zero, most TDA architectures have some minor time offset.

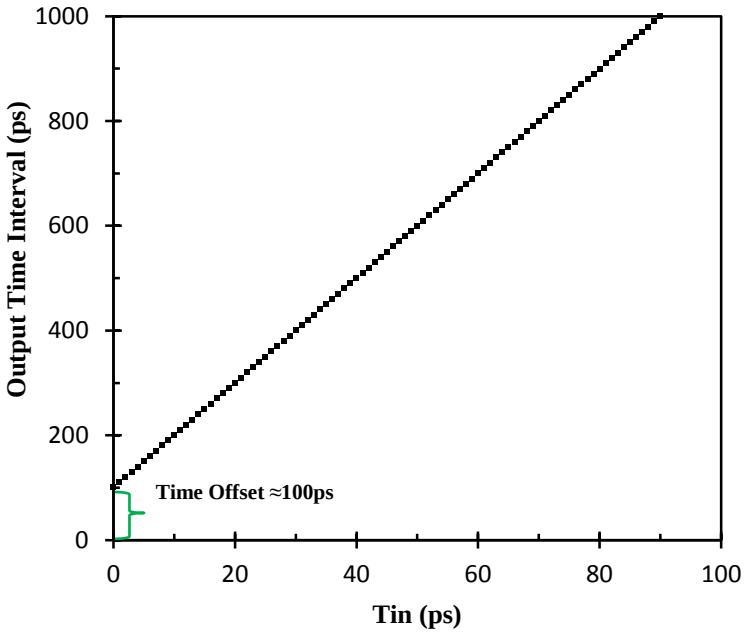



Figure 1.8 Non-ideal TDA input-output characteristic with a 100ps time offset

***Input Range***

The input range of TDA is the range of time intervals for which the TDA can provide a stable gain with a linear input-output characteristic, as shown in Figure 1.9. TDA cannot properly amplify input time intervals beyond the input range.

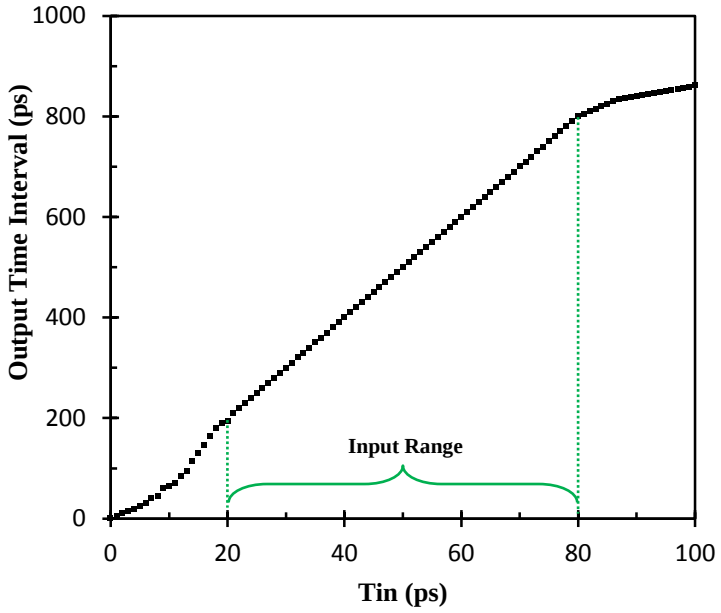



Figure 1.9: Non-ideal TDA input-output characteristic with a limited input range

***Frequency***

The frequency of TDA is defined as the number of proper time amplifications a TDA can perform per second. A higher frequency of TDA indicates that a TDA can amplify an input time interval to an output time interval at a higher speed.

## 1.4. Research Goals

The concept of on-chip TDC and TDA have been widely adopted in many applications for their reliable and precise time measuring and processing abilities. The designs of most TDC and TDA architectures are application-specific. However, accurate on-chip time

measuring devices are scarce and their implementation are challenging with 10ps time resolution or less. In order to explore this area, this thesis focuses on developing new TDC architecture with TDA to provide time measurement function with time resolution in tens of picosecond range.

The research goals are as the follows:

- To investigate the existing on-chip time-domain metrology and develop possible techniques to improve the time resolution of TDC and the performance of TDA
- To propose a new TDC architecture that incorporates a TDA to achieve effective finer time resolutions after a time amplification
- To implement the TDC architecture using IBM 0.13μm CMOS process technology in Cadence environment
- To analyze and evaluate the performance of the implemented TDC architecture using HSPICE simulator

The proposed TDC design should also meet the following design specifications:

- The TDC should achieve a time resolution smaller than ten picoseconds
- The TDC should have a linear input/output characteristic
- The TDC should have a minimum conversion rate of 1MHz

The final deliverable TDC architecture should be a reliable on-chip time measuring device with time resolution below 10ps, which can be used towards on-chip timing verifications or time signal processes. The performance analyses of the TDC architecture

should also provide design aspects for the future modifications and applications of the TDC architecture.

## 1.5. Thesis Organization

This thesis outlines the background of on-chip time metrology and the research work accomplished in developing high resolution TDC architecture. Chapter 2 provides an introduction to state-of-art TDC architectures and their operation concepts and implementations. A summary on the performance of the TDC architectures is presented in the end of Chapter 2. Chapter 3 describes the newly developed single-stage Vernier TDC with a constant gain TDA. The HSPICE analyzed results of the implemented TDC architecture is presented in Chapter 4. Chapter 5 concludes this thesis and discusses possible future work.

# CHAPTER 2 HIGH RESOLUTION TDC ARCHITECTURES

High resolution time measuring applications have driven the developments of various TDC architectures. Various time measurement principles have been implemented as different TDC architectures. These TDC architectures have different characteristics, and the choice of TDC architectures can have significant impacts on the time measurement performance of the applications. This chapter describes some common TDC architectures used for on-chip time metrology. By comparing the advantage and drawbacks of these TDC architectures, methods to improve the time resolutions of TDC architectures will be discussed in a summary section.

## 2.1. Delay Line TDC

A common method to perform time measurement with picosecond resolution is by utilizing a delay line TDC, as shown in Figure 2.1. In a delay line TDC, the *START* signal propagates through a multi-stage delay line. The delayed *START* signals from each delay stage are sampled by the *STOP* signal using an array of registers. The Figure 2.2 shows the timing diagram of the delay line TDC.

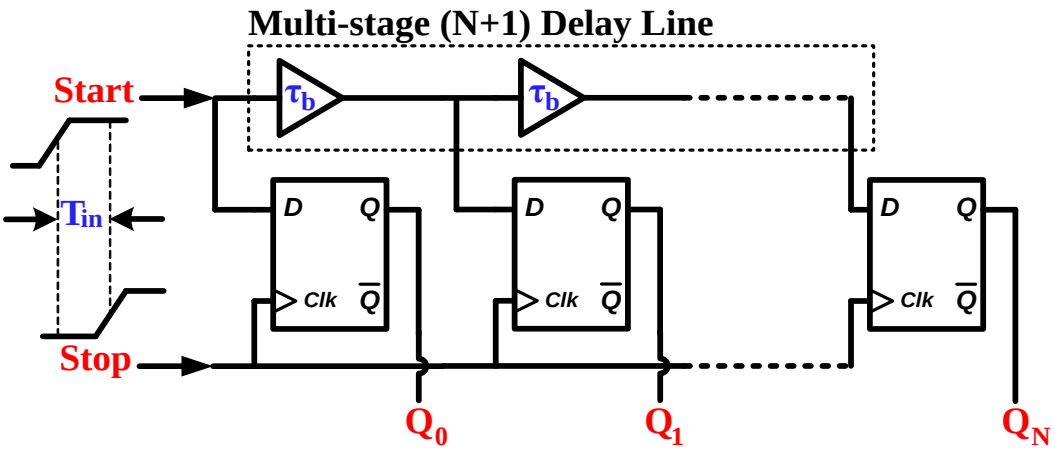



Figure 2.1: Delay line TDC with CMOS Buffers

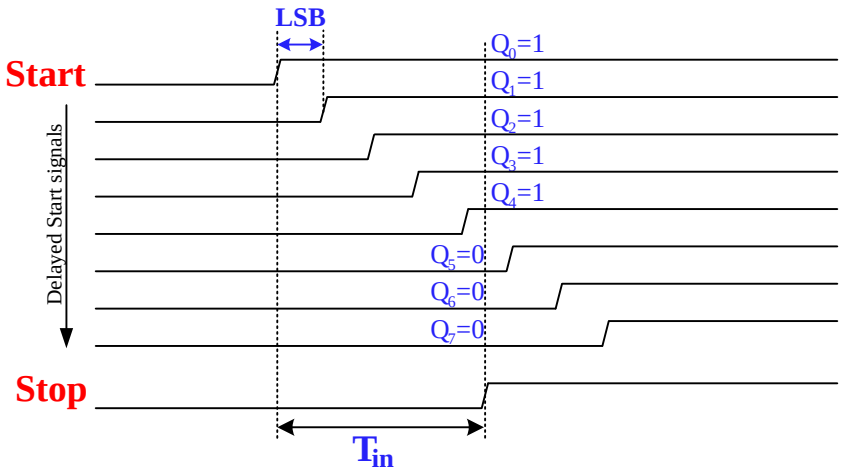



Figure 2.2: Timing diagram of delay line TDC

The digital output of the delay line TDC is interpreted by adding the number of high outputs of the registers' output [Q0:QN]. This digital output code scheme is often referred as thermometer code [12], and it provides a digital representation of the input time intervals. The input time interval can be determined using the following equation:

$$T_{in} = \tau_b \times CNT \tag{2.1}$$

where the CNT is the number of high outputs from the registers' outputs, and the $\tau_b$ is the propagation delay time of the single delay stage. The measurement resolution of the delay line TDC is determined by the propagation delay time of the delay elements. Most delay line TDCs use non-inverting CMOS buffers as the delay elements for the simplicity of digital designs. Some delay line TDCs attempt to use CMOS inverters with shorter propagation delay to achieve better measurement resolutions [12].

Although the delay line TDC makes the measurement resolution in the picosecond level possible, it has some major drawbacks. The dynamic range of the delay line TDC is proportional to the number of delay stages. Measuring longer time intervals will require longer delay lines. This will increase the chip area and the power consumption of the circuit. Meanwhile, as the number of the delay stages increases, the delay mismatches become more significant and affect the measurement linearity of the delay line TDC [11]. A delay line TDC with 1ns dynamic range and 40ps time resolution has been adopted in an all-digital PPL as a phase frequency detector [12]. A multistage delay line TDC designed with DLLs has achieved a linear dynamic range of 3.2μs and 34ps time resolution [13], but the overall power consumption and chip area are relative large. The achievable time resolution of a delay line TDC is limited to the minimum gate delay time in the given process technology, which is generally around 40ps in 0.13μm CMOS technologies. The demand for finer measurement resolution has led the research towards different TDC architectures.

## 2.2. Vernier TDC

The measurement resolution of the delay line TDC can be further improved by adopting the Vernier principle into the designs [7,14,15]. These TDC designs with the Vernier delay lines are generally referred as Vernier TDCs (VTDC). In a VTDC, two multi-stage delay lines with a small, well defined delay difference are used for time measurement as shown in Figure 2.3.

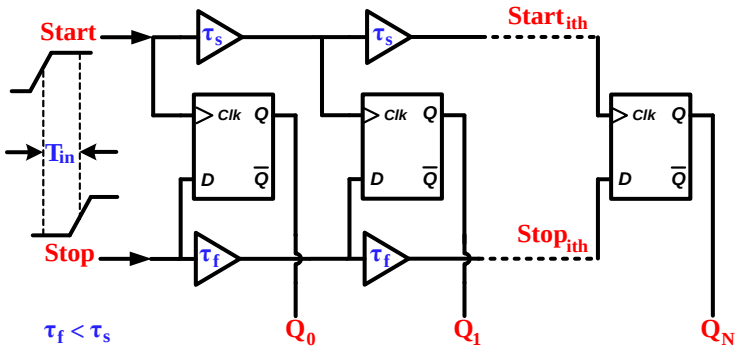



Figure 2.3: Concept of Vernier delay line TDC

The *START* signal is connected to the delay line with a single-stage propagation delay $\tau_s$. The *STOP* signal is connected to the second delay line with a shorter single-stage propagation delay $\tau_f$. Since the *STOP* signal propagates faster than the *START* signal, the phase difference between $START_{ith}$ and $STOP_{ith}$ signals reduces after every Vernier delay stage by a delay difference of $(\tau_s - \tau_f)$. At the Vernier stage where the *STOP* signal catches up with the *START* signal, the register at that stage and the following stages will produce low outputs. The output digital code scheme of VTDC is also thermometer code, and the input time interval, $T_{in}$, can be determined using the following equation:

$$T_{in} = (\tau_s - \tau_f) \times CNT \tag{2.2}$$

where the CNT is the number of high outputs from the registers' outputs. The effective measurement resolution of a Vernier delay line TDC is equal to the propagation delay difference ($\tau_s - \tau_f$); therefore, sub-gate delay time resolution can be achieved by adopting the Vernier principle. Similar to the delay line TDC, the dynamic range of the Vernier delay line TDC is linearly proportional to the number of Vernier delay line stages. In order to reduce the chip area, the VTDC architecture has evolved from multistage VDL to 2-dimensional [16] and 3-dimensional [10] delay-space scheme, leading to a smaller chip area but at the cost of dramatic increase in circuit complexity. This increased complexity, however, makes the circuit more susceptible to mismatches and process variations.

## 2.3. Single-stage VTDC

In order to eliminate the problems caused by the large structures of VDL, single-stage VTDC designs have been proposed [9]. In a single-stage VTDC circuit, the linear VDL has been replaced by a single Vernier stage that consists of two triggerable oscillators featuring different oscillation periods, $T_s$ and $T_f$ (Figure 2.4).

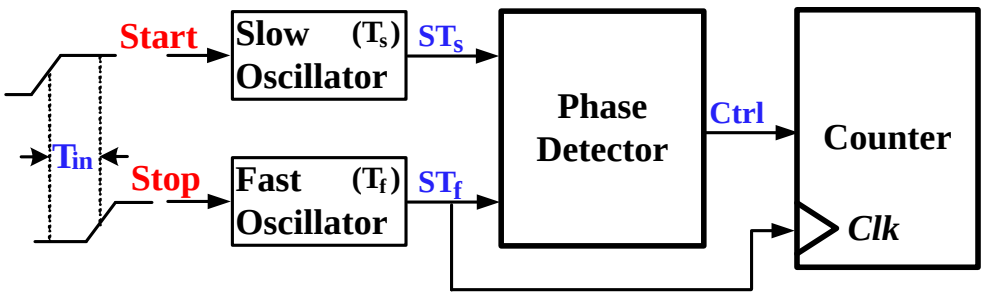



Figure 2.4: Concept of Vernier oscillator TDC with single counter

The input signals of the single-stage VTDC, *START* and *STOP*, are used to trigger oscillators. When the *START* signal arrives at the single-stage VTDC, the slow oscillator is triggered and starts to oscillate with a period of $T_s$. On the arrival of the *STOP* signal, the fast oscillator is activated to oscillate with a period of $T_f$, and the counter starts to count the number of its oscillations. After both oscillators have been triggered, the phase difference between signals $ST_s$ and $ST_f$ is initially equal $T_{in}$. Since $T_f$ is smaller than $T_s$, the phase difference between $ST_f$ and $ST_s$ gets reduced every one cycle by an oscillation period difference of ($T_s$ - $T_f$), and the signal edge of $ST_f$ gradually catches up with $ST_s$. When these two signal edges are coincident, the phase detector signal will disable the counter. The input phase difference, $T_{in}$, can be determined using the following equation:

$$T_{in} = (T_s - T_f) \times CNT \tag{2.3}$$

where CNT is the number of oscillation cycles counted by the counter. The performance of the single-stage VTDC surpasses the conventional VTDC in measurement accuracy, chip size, and power consumption. However, the measurement resolution of a single-stage VTDC is limited by the phase detectors' performance. The resolution of a single-stage VTDC cannot be smaller than the minimum detectable phase error of its phase detector. The measurement range of the single-stage VTDC is also limited by the detection range of the phase detector.

In a previously reported implementation of the single-stage VTDC [9], the classic phase detector with two D-type registers and an AND gate has been utilized to control the timing measurement process, as shown in Figure 2.5.

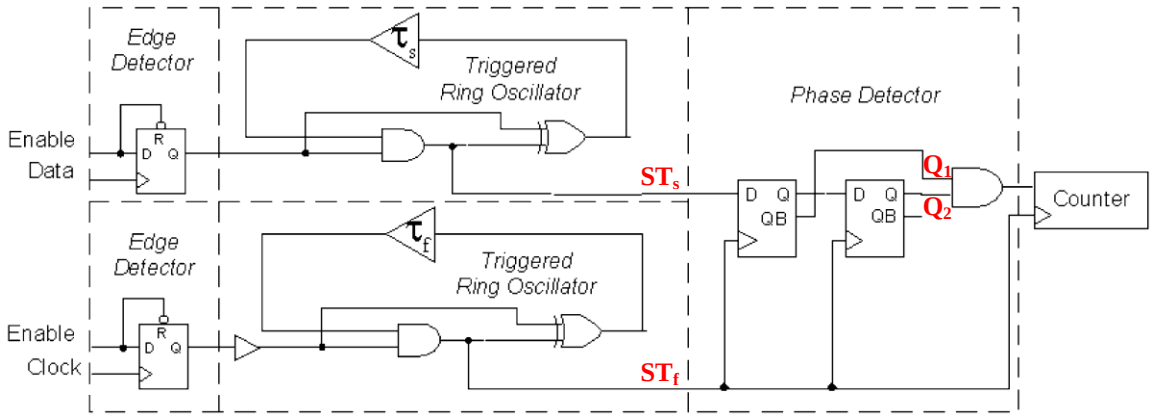



Figure 2.5: Single-stage VTDC with classic two-register phase detector [9]

The phase detector keeps track of the history of the phase difference between two oscillators and stops the measurement process once $ST_f$ begins to lead $ST_s$. On the first rising $ST_f$ edge after the rising edge of $ST_s$, the output of the first register *Q1* goes high. On the following rising edge of $ST_f$, the second register keeps the value of *Q1* and switches *Q2* to high. When the signal edge of $ST_f$ catches up with $ST_s$, the output *QB1* rises, and switches the output of the AND gate to generate the Phase Detected signal, as shown in Figure 2.6. The Phase Detected signal is fed to the counter where it stops the time measurement process.

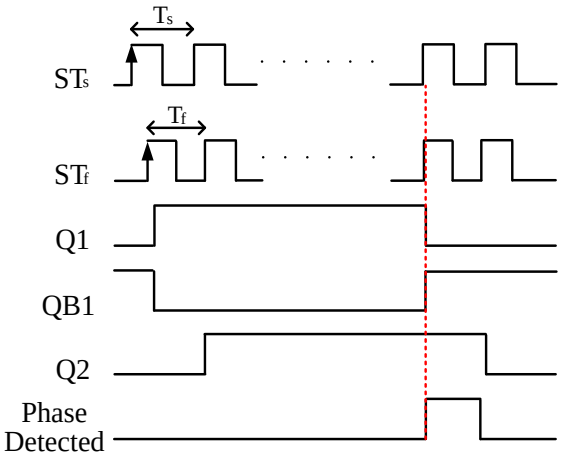



Figure 2.6: Timing diagram of the correct phase detection [9]

The classic two-register phase detection mechanism relies on the proper operation of D-type register. However, if the time difference between the rising edges of *Clock* and *Data* signals violates the setup time constraint of the registers, the outputs of the registers will not be correct. This problem is generally referred as meta-stability [17]. In order to prevent the meta-stability, the Data signal should be held steady for certain amount of time before the clock event, and the minimum value of this time constraint is called a setup time. The meta-stability is likely to happen in the classic two-register phase detector, when the $ST_f$ signal catches up with $ST_s$ signal and the phase difference between these two signals is smaller than the required setup time. The unpredictable outputs of the registers will further cause the phase detector unable to stop the measurement process accurately. Therefore, the requirement for the non-zero setup time in the classic two-register phase detector is equivalent to the dead-zone characteristic of the phase detector. Due to the dead-zone characteristic, the single-stage VTDC designed with a classic two-register phase detector will feature a serious limitation on the time measurement resolution. The single-stage VTDC with the two-register phase detector built in 0.18μm CMOS technology has been reported to achieve only a 54.5ps measurement resolution [9]. Although the use of single-stage VTDC alleviates the component mismatch problems in the conventional VTDC, the single-stage VTDC can be still unable to achieve sub-gate delay time resolution due to the limitations of the adopted phase detector [9].

## 2.4. Time Amplified TDC

The time resolution of a TDC is often the most important requirement for time measurement applications. When the required time resolution is higher than the time

resolution of the TDCs, some TDC architectures utilize TDA to pre-amplify input time intervals and enhance the time resolution.

However, the gain of the TDA is usually sensitive to PVT variations. In order to reduce the sensitivity over PVT variation, "closed-loop" circuits such as DLL have been utilized in TDA designs. One of the reported time difference amplifier TDC for narrow time intervals measurements uses a DLL to set up the gain of the TDA [18].

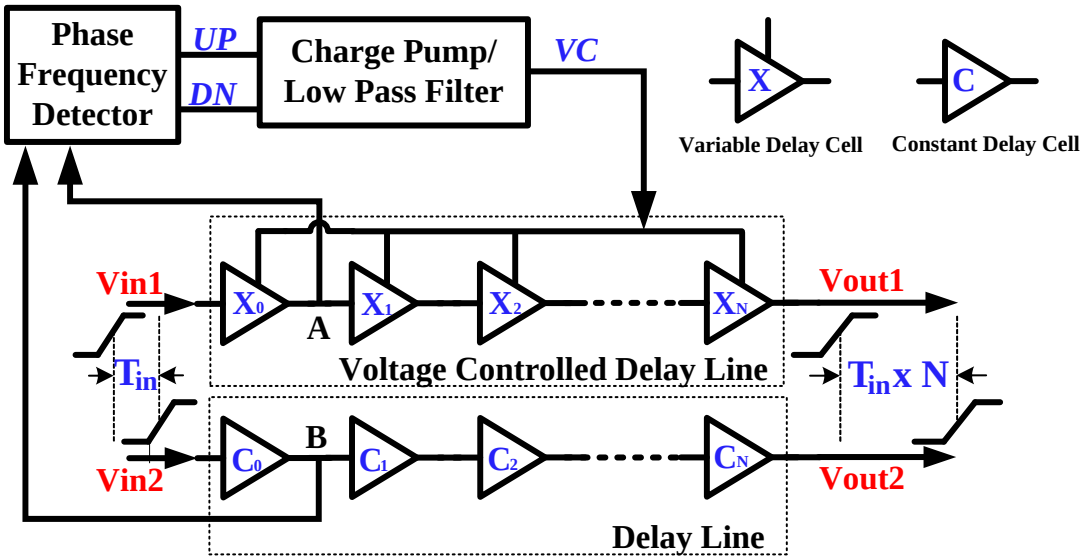



Figure 2.7: DLL based time difference amplifier [17]

The DLL based TDA [18] uses two delay lines: one built of N+1 delay elements of constant delay, and the other built of N+1 elements of voltage controlled delay, as shown in Figure 2.7. The phase difference between two input signals, Vin1 and Vin2, is sensed at the output of the first delay elements (nodes A and B) by a phase frequency detector that produces the UP and DN pulses to control the charge pump. The low-pass filtered output of charge pump is fed back as a control voltage to adjust the delay of all variable

delay cells. It can be shown [18] that, in locked condition, the difference between delay times of two input signals, $T_{in1}$ and $T_{in2}$ is equal:

$$T_{in1} - T_{in2} = T_{C0} - T_{X0} \tag{2.4}$$

where $T_{C0}$ and $T_{X0}$ are the delay times of $C_0$ and $X_0$ cells, respectively. Given the same control voltage from the charge pump, this time difference will be multiplied N times while propagating through the next N delay stages. The time difference measured at the output is equal [18]:

$$T_{out1} - T_{out2} = N \times (T_{in1} - T_{in2}) \tag{2.5}$$

The resulting TDA featuring a gain factor of 10 built in 0.18μm CMOS technology [18] achieved a linear gain characteristic for the input range larger than 60ps. The DLL based TDA was utilized in a delay line TDC to pre-amplify the input time intervals [18]. The overall time measurement resolution was improved by a factor of 10. With the pre-amplification of the DLL based TDA, the delay line TDC has achieved a time resolution of 14.4ps. However, due to the unstable gain of the TDA for the input time intervals below 60ps, the reported TDC with DLL based TDA cannot measure input time intervals below 60ps.

## 2.5. Summary

This chapter has presented an overview of the state-of-the-art of high resolution TDC architectures for on-chip time measurement. The time resolution of the delay line TDC is limited to the minimum gate delay time in the given process technologies. This limitation

has been overcome in the VTDC. Yet similar to the delay line TDC, increasing the dynamic range of a VTDC will increase its chip area and power consumption. The measurement accuracy of the VTDC architecture also suffers from inevitable component mismatch problems just like the delay line TDC. The compact design of the single-stage VTDC replaces the large delay line structures in VTDC by utilizing two oscillators and a phase detector. The performance of the single-stage VTDC surpasses the conventional VTDC in measurement accuracy, chip size, and power consumption. However, the prior designs of single-stage VTDC cannot achieve sub-gate delay time resolution due to the dead zone characteristic of the register-type phase detectors. Based on the time measurement techniques discussed in this chapter, a single-stage VTDC may achieve a reliable sub-gate delay time resolution by utilizing phase detectors with minimum dead zone or pre-amplifying the input time intervals with a constant gain time difference amplifier. This has led this research to focus on developing TDA and single-stage VTDC that is reported in the next Chapter.

# CHAPTER 3 DESIGN OF SINGLE-STAGE VTDC WITH TIME DIFFERENCE AMPLIFIER

This chapter presents the design of a single-stage VTDC that utilizes a dynamic-logic phase detector and a constant gain TDA. The zero dead-zone characteristic of dynamic-logic phase detector allows for the single-stage VTDC to deliver sub-gate delay time resolution with minimum circuit components. At the same time, the constant gain TDA further improves the resolution by pre-amplifying the input time intervals. The proposed single-stage VTDC with TDA overcomes the time resolution limitation of the conventional single-stage VTDC, allowing to achieve reliable time resolution below 10ps for on-chip time domain metrology. The single-stage VTDC with TDA presented in this thesis has been designed using 0.13μm IBM CMOS technology with 1.2V power supply. Partial design and performance analyses presented here have been published in [19] and [20].

## 3.1. Architecture and Operation Principles

The single-stage VTDC with constant gain TDA presented in this work exploits the concept of the single-stage Vernier circuits, similar to the circuit proposed by [9]. In order to improve the measurement resolution of the single-stage VTDC, a zero dead-zone dynamic-logic phase detector and a constant gain time difference amplifier are

incorporated in this design. Different from the classic register type phase detector used in the previously reported single-stage VTDCs [9,11], the dynamic-logic phase detector used here has an extended phase detection range and zero dead-zone characteristics [21], allowing for a reliable sub-gate delay time resolution. Moreover, the time resolution of the single-stage VTDC has also been enhanced by pre-amplifying the input time intervals with a stable gain of 10 using a modified DLL based TDA.

The single-stage VTDC with a constant gain TDA presented in this work measures an input time interval, $T_{in}$, between the input signals, *START* and *STOP*. The input time interval is first pre-amplified using the modified DLL based TDA with a gain of 10 and then measured by the single-stage VTDC with dynamic-logic phase detector, as shown in Figure 3.1.

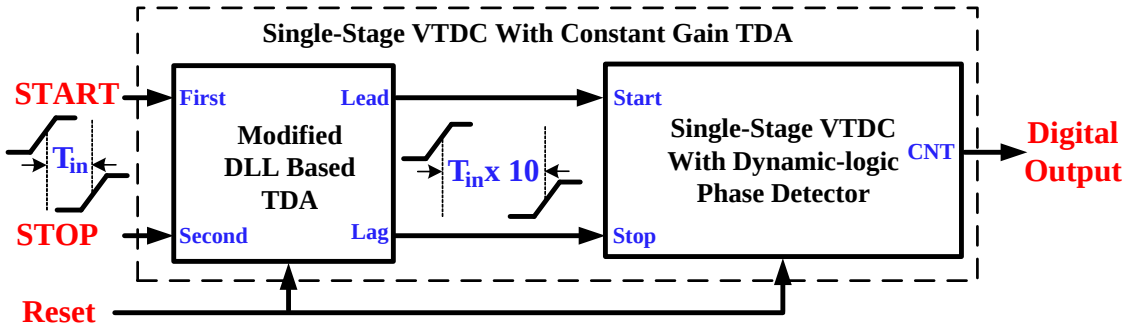



Figure 3.1: Block diagram of single-stage Vernier TDC with TDA

The design details and operation principles of the modified DLL based TDA and the single-stage VTDC with dynamic-logic phase detector are described in the following sections.

## 3.2. Design of Modified DLL Based TDA

An ideal TDA that can be utilized to pre-amplify input time intervals of a TDC must have a stable gain that is insensitive to PVT variations and be capable to handle the time interval ranges smaller than the time resolution of the given TDC. Although the closed-loop gain controlled DLL based TDAs reported in literature mostly maintain a stable gain that is insensitive to PVT variations [18,22], they have been incapable of maintaining the gain stability for very small input time intervals below 60ps [18]. Since the time amplification mechanism of the TDA is based on the locking condition of the DLL, the gain instability for input time intervals below 60ps is likely caused by the phase error of the DLL. Therefore, it seems feasible to improve the gain stability of the TDA for the picosecond time range by improving the locking condition of the DLL. The design of the modified DLL based TDA presented in this section focuses on modifying the DLL by eliminating the dead-zone of the PFD and balancing the charging/discharging current of the charge pump.

The block diagram of the modified DLL based TDA is shown in Figure 3.2. It is composed of an 11-stage Voltage Controlled Delay Line (VCDL), an 11-stage constant delay line, a dynamic-logic phase frequency detector [23], a balanced charge pump, and output stage. The modified DLL based TDA presented in this work exploits the phase-locking mechanism of the DLL system, similar to the circuit proposed by [18].

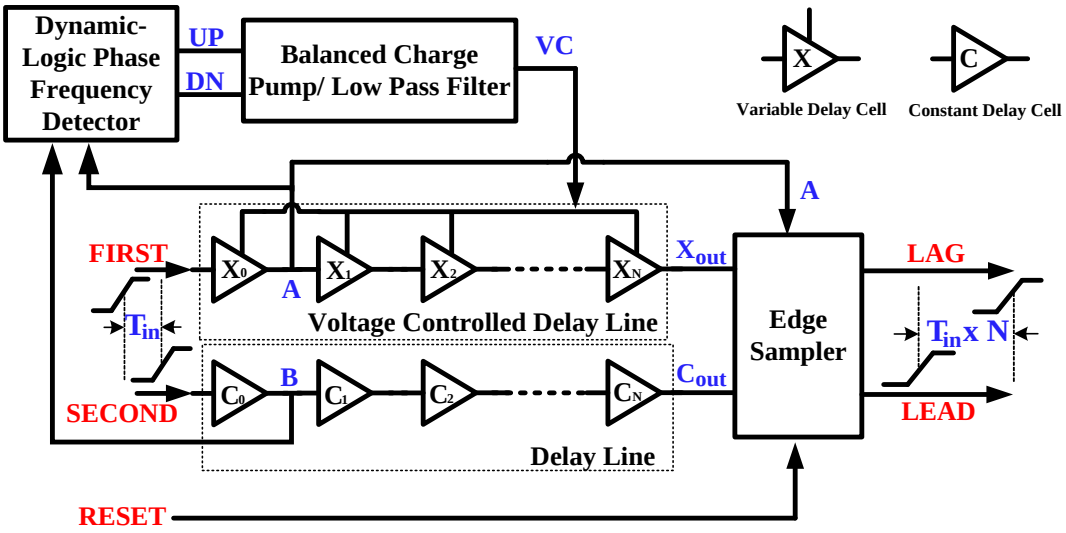



Figure 3.2: The modified DLL based time difference amplifier

The phase difference between two input signals, FIRST and SECOND, is sensed at the output of the first delay elements (nodes A and B) by a dynamic-logic phase frequency detector [23] that produces the UP and DN pulses to control the charge pump. The low-pass filtered output of the charge pump is fed back as a control voltage to adjust the delay of all variable delay elements. It can be shown that, in the locking condition, the input time interval between the rising edges of signal *FIRST* and *SECOND* is equal:

$$T_{FIRST} - T_{SECOND} = T_{C0} - T_{X0} \tag{3.1}$$

where $T_{C0}$ and $T_{X0}$ are the delay values of $C_0$ and $X_0$ cells, respectively. The delay time difference between constant delay cells and the variable delay cells will be multiplied by a factor of 10 while propagating through the next 10 delay stages. The output time interval between the signals $X_{out}$ and $C_{out}$, is equal:

$$T_{C_{out}} - T_{X_{out}} = 10 \times (T_{FIRST} - T_{SECOND}) \tag{3.2}$$

The output signals of the delay lines, $X_{out}$ and $C_{out}$, are then converted to two rising signal edges, *LAG* and *LEAD*, for measurements using the single-stage VTDC. The designs of the modified DLL based TDA's functional blocks are described in the following sections.

### 3.2.1. Dynamic-logic Phase Frequency Detector

In a DLL, the PFD detects the phase and frequency difference between two input signals, and generates the error pulses with pulse width difference proportional to the phase difference of the two input signals. An accurate phase difference detection of a PFD is a critical factor that affects the DLL performance. However, conventional PFDs may suffer from dead-zone problem. A dead-zone problem occurs when two input signals are very close to each other and the small phase difference cannot be detected by the PFD. The dead-zone is a major factor that limits accuracy of the PFD and deteriorates the DLL locking characteristics. Therefore, it seems feasible to improve the TDA linear in the picosecond time range by utilizing the PFD that eliminates the dead-zone problem.

The dynamic-logic CMOS PFD [23] has been chosen for the modified DLL based TDA. This PFD eliminates the dead-zone and minimizes the blind-zone, partially due to its very short reset phase. A PFD compares the phase and frequency of the input signals and generates *UP* and *DN* error pulses based on their phase and frequency difference. In the dynamic-logic PFD used in this design (Figure 3.3), when *ΦB* and *ΦA* are low, the *U1* and *D1* nodes are precharged high. When *ΦA* rises, the *UPb* node is discharged, and *UP* pulse is generated. On the arrival of the rising edge of *ΦB*, the *DNb* node is pulled low, thus generating *DN* pulse. When both outputs *UP* and *DN* are high, the *U1* and *D1* node

will be pulled low, causing the *UPb* and *DNb* node to go high. This condition will deactivate the *UP* and *DN* pulses and reset the PFD. The difference in the pulse width between the *UP* and *DN* signals is therefore equal to the input phase difference. Since the dynamic-logic PFD uses its own output signals directly to reset itself, there is virtually no dead-zone problem in this design. Therefore, the dynamic-logic PFD will be a good solution to eliminate the time amplifier nonlinearity for the very short time intervals.

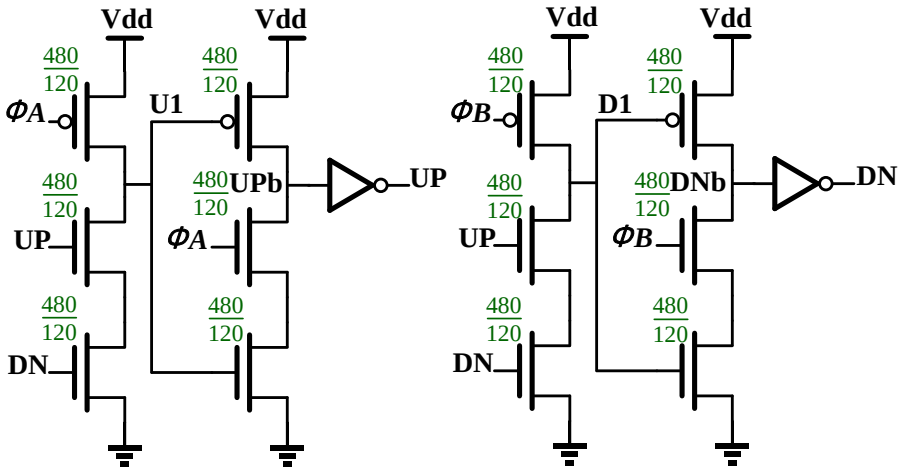



Figure 3.3: Dynamic-logic phase frequency detector

### 3.2.2. Balanced Charge Pump

The output signals of the PFD, *UP* and *DN*, are applied to the charge pump. The charge pump generates a current to charge/discharge the control voltage, *VC*, and adjusts the delay time of the voltage controlled delay line. When the DLL establishes a locking condition, the UP and DN signals have the same pulse width and *VC* should remain stable to maintain DLL in the locking condition. However, if the charging and discharging currents generated by the charge pump are not equal, *VC* would fluctuate and introduce phase error to the DLL's locking condition.

A balanced charge pump [24] built only of NMOS transistors is used here (Figure 3.4), to avoid the possible imbalance in charging and discharging current due to the PMOS and NMOS mismatch. When the *UP* signal is high and *DN* signal is low, M3 is activated to allow the current to flow through M3 and M6. The current mirror (M6 and M5) sources the same amount of the current into the node *VC*. Meanwhile, if the *DN* is high and *UP* is low, the node *VC* will discharge through M1 and no current will flow in M5 and M6. The transistors M7 and M8 serve as constant current sources/sinks to power all other transistors and to charge/discharge the *VC* output.

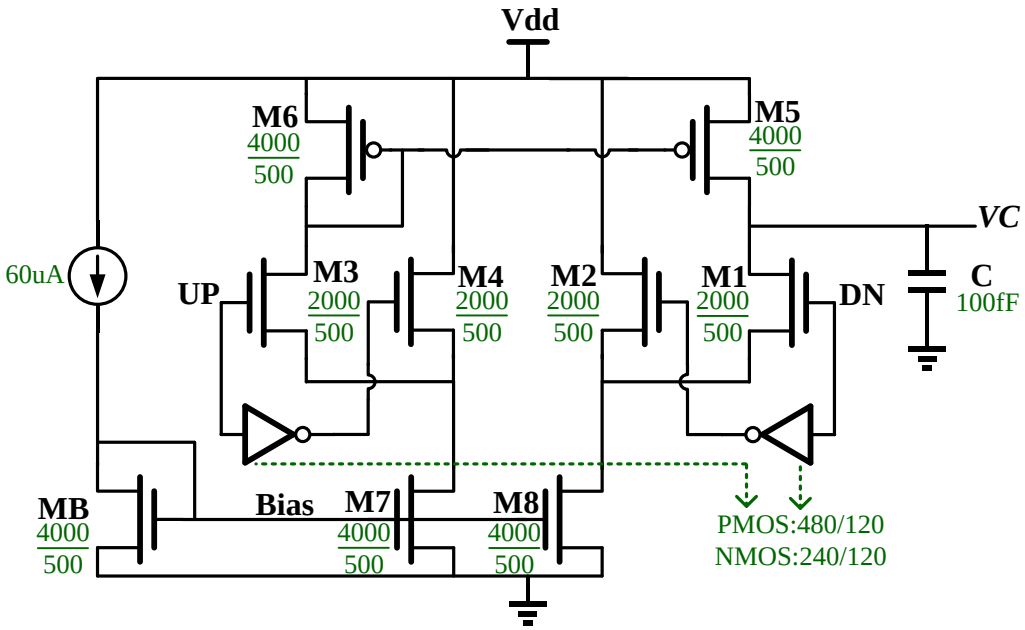



Figure 3.4: Balanced charge pump

### 3.2.3. Delay Elements

The input time interval range is determined by the range of the delay difference between the variable and constant delay cells in the DLL. The minimum delay time of the variable delay cell should be smaller than the constant delay cell, and its maximum delay time

should be as large as possible to provide a large linear output range. The Figure 3.5 shows the variable delay circuit used in the VCDL and the constant delay circuit used in the constant delay line is illustrated in Figure 3.6.

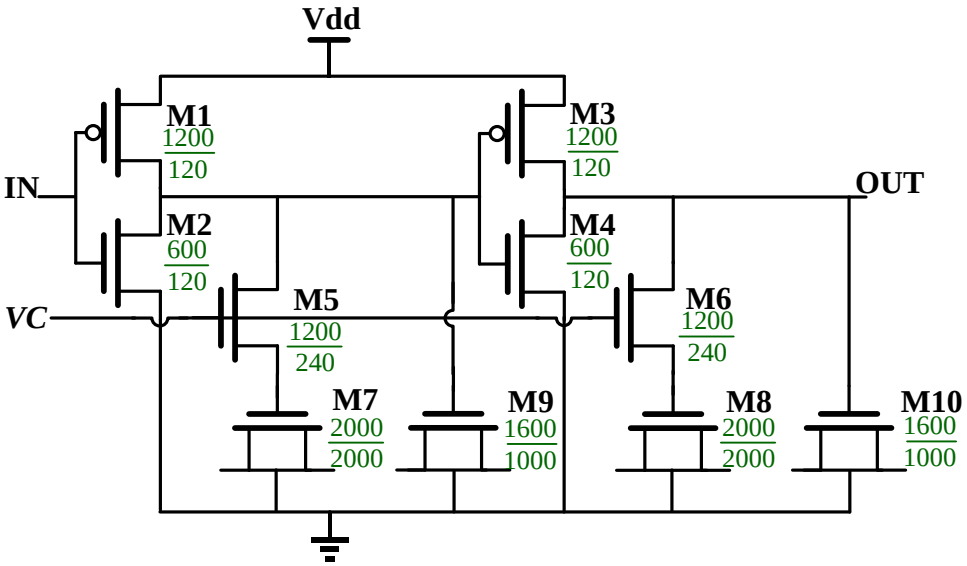



Figure 3.5: Variable delay cell

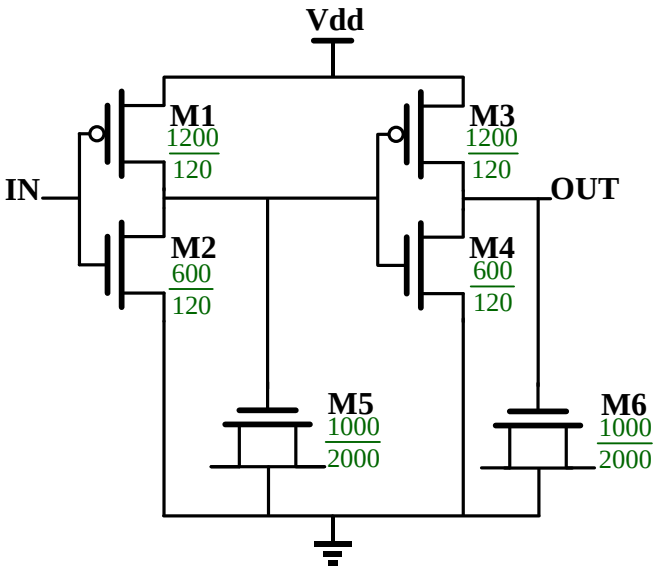



Figure 3.6: Constant delay cell

Both variable delay cell and constant delay cell are designed based on simple non-inverting CMOS buffer structure with NMOS transistors used as capacitive loads. The transistor M7-M9 in the variable delay cell and the transistor M5-6 in the constant delay cell are being used as capacitors. In order to provide the controllability over the delay time on the variable delay cell, two additional control transistors, M5 and M6, are added to control the charging and discharging current of transistor M7 and M8, as shown in Figure 3.5. Decreasing the constant delay value can extend the output linear region of the modified DLL based TDA, yet the constant delay value must be kept larger than the minimum variable delay time to ensure the locking condition for the very short input time interval. Therefore, instead of a constant delay value as small as the minimum variable delay time, the constant delay time was designed to be slightly larger than the minimum variable delay time to avoid poor locking condition due to variations in different process corners.

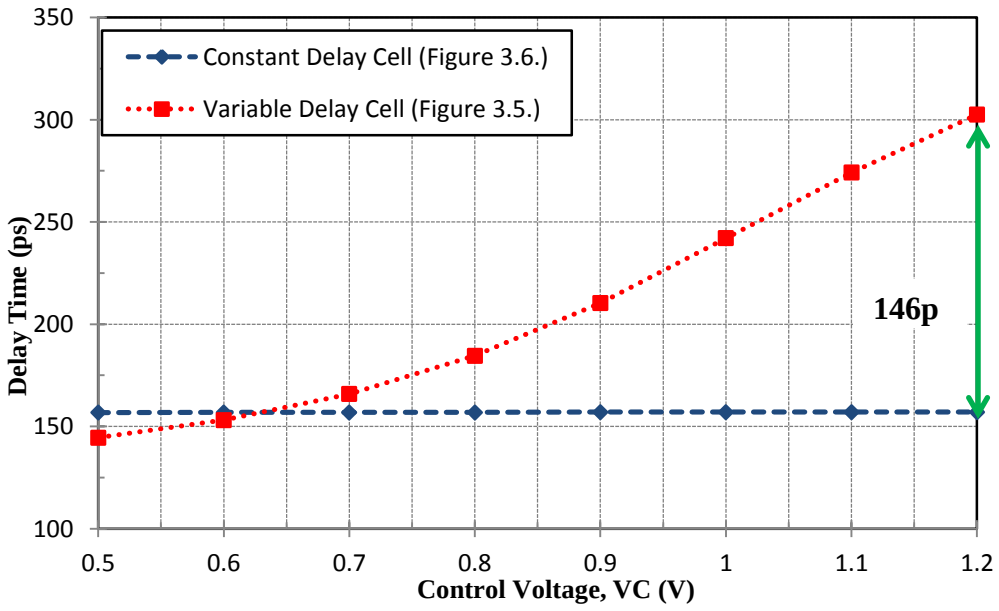



Figure 3.7: Delay times of the variable delay cell and constant delay cell versus control voltage

The designed variable delay cell features a variable delay from 145 to 303ps that depends linearly on the control voltage within the 0.6V to 1.2V voltage range, while the constant delay cell has a delay of 157ps, as shown in Figure 3.7. The slight nonlinearity below 0.7V is caused by the M5 and M7 (or M6 and M8) operating in weak inversion. Hence by adjusting the control voltage (0.7V to 1.2V), it is possible to vary the delay difference from 0 to 146 ps.

### 3.2.4. Edge Sampler

The oscillating output signals of the delay lines, $X_{out}$ and $C_{out}$, are connected to an edge sampler circuit, as shown in Figure 3.8. After the process of the time amplification, the edge sampler converters the oscillating signals to two rising signals, *LAG* and *LEAD*.

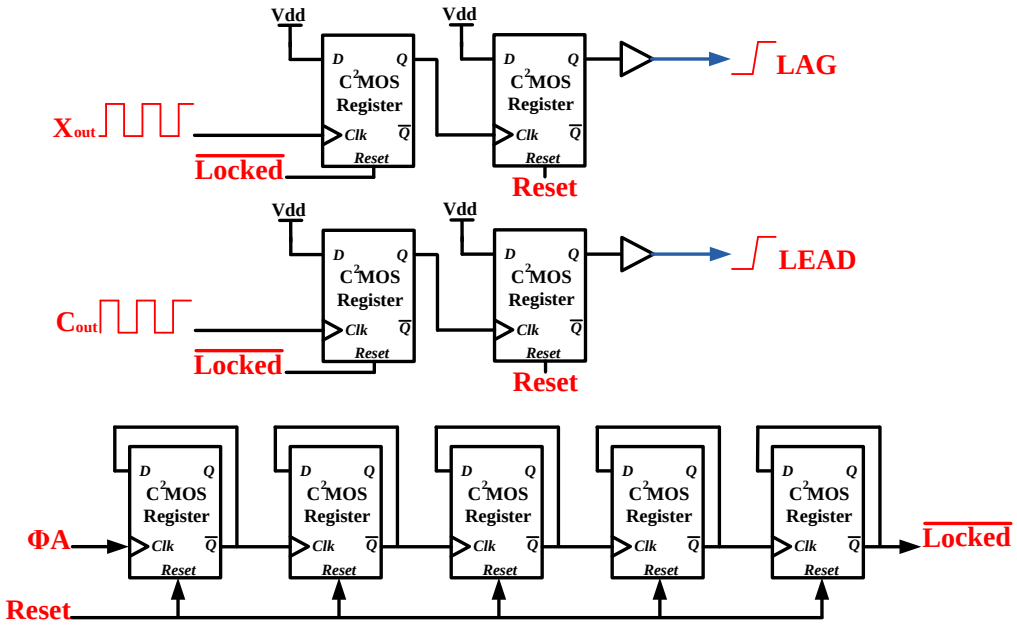



Figure 3.8: Edge sampler circuit of the modified DLL based TDA

From simulation in different process corners, the modified DLL based TDA has shown a process time of 12 oscillation cycles in the corner with the slowest performance. Hence, the edge sampler circuit utilizes a 5-bit counter to count the number of the oscillation cycles in the DLL. After counting 15 cycles, the counter enables the double registers capturing the first rising signal edges of $X_{out}$ and $C_{out}$. The captured signal edges are converted to two rising signals, *LAG* and *LEAD*, where the time difference between them will be measured using the single-stage VTDC.

The edge sampler circuit has been design using primarily C$^2$MOS registers with reset. The transistor level schematic of the C$^2$MOS register is shown in Figure 3.9. In the design of the C$^2$MOS register, two NOR gates have replaced the inverters to accommodate the Reset signals. When the Reset signal is high, the stored values of both stage registers will be discharged to zero.

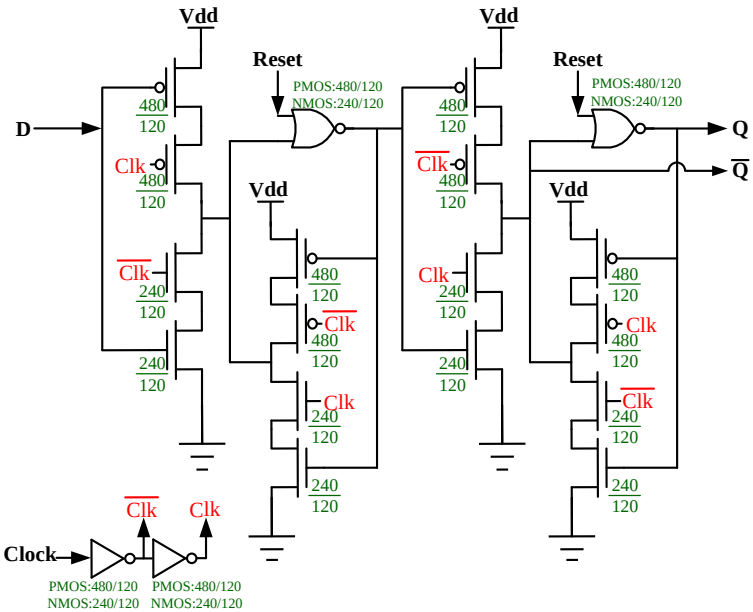



Figure 3.9: C$^2$MOS register with reset

## 3.3. Design of Single-stage VTDC with Dynamic-Logic Phase Detector

The second stage of the proposed TDC architecture is a single-stage VTDC with dynamic-logic phase detector. After the input time intervals being amplified by the DLL based time difference amplifier, the amplified time interval is measured by the single-stage VTDC. The proposed single-stage VTDC exploits the concept of the single-stage Vernier circuit, similar to the circuit proposed by [9]. In order to further improve the time resolution of the single-stage VTDC, a dynamic-logic phase detector with zero dead-zone has been developed and incorporated in the proposed single-stage VTDC. The Delayed-Input-Pulse Dynamic Phase Frequency Detector (DIP-PFD) is known to have zero dead-zone and an extended detection range [21]. Therefore it is a promising candidate to help VTDC to achieve a better time resolution. The proposed single-stage VTDC, shown in Figure 3.10, consists of two triggerable ring oscillators, termed slow and fast oscillators, a dynamic-logic phase detector, and a 5-bit counter. The single-stage VTDC's functional blocks are described in the following sections.

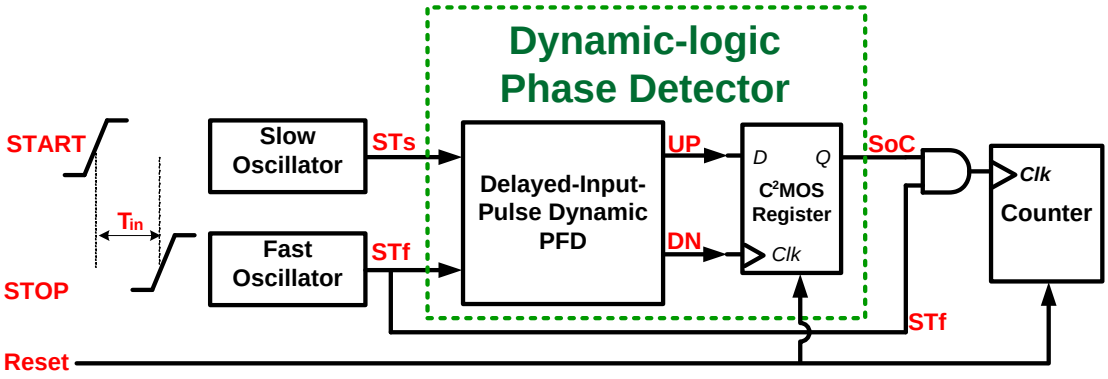



Figure 3.10: Single-stage VTDC with dynamic-logic phase detector

### 3.3.1. Triggerable Ring Oscillator

The triggerable voltage-controlled ring oscillators are built similarly to the circuit proposed by [11]. However, for the simplicity, we do not use Phase-Locked Loops (PLL) to stabilize the oscillator frequencies. The triggerable ring oscillators have been designed using voltage controlled delay cells and NAND gates, as shown in Figure 3.11.

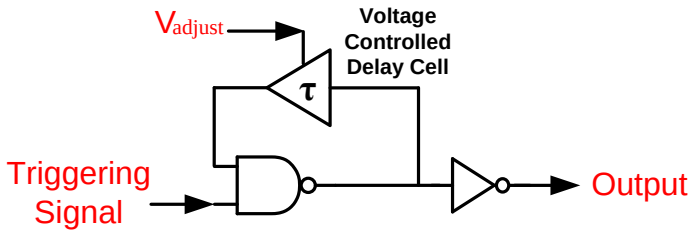



Figure 3.11: Triggerable voltage-controlled oscillator

Instead of generating different oscillation frequencies by using PLLs as in [11], the different oscillation frequencies are generated by using voltage-controlled delay cells. This solution is sufficient for the proof of concept and also provides a degree of controllability to the time measurement resolution. The oscillation frequency of the triggerable voltage-controlled oscillator is given by the following equation:

$$F_{oscillation} = {}^{1}/_{T} = \frac{1}{2\times(\tau_{VCD}+\tau_{NAND})} \quad (3.3)$$

where T is the period of output signal, $T_{VCD}$ represents the delay of voltage-controlled delay cell, and $T_{NAND}$ represent the delay of the NAND gate.

The NAND gate is used to accommodate the triggering signal, *START* or *STOP*. When the triggering signal is high, the NAND gate operates as an inverter closing the feedback

loop, and creating the conditions for oscillations to take place. When the triggering signal is low, the NAND gate deactivates the feedback loop and stops the circuit from oscillating. The schematic of the triggerable voltage-controlled oscillator is shown in Figure 3.12.

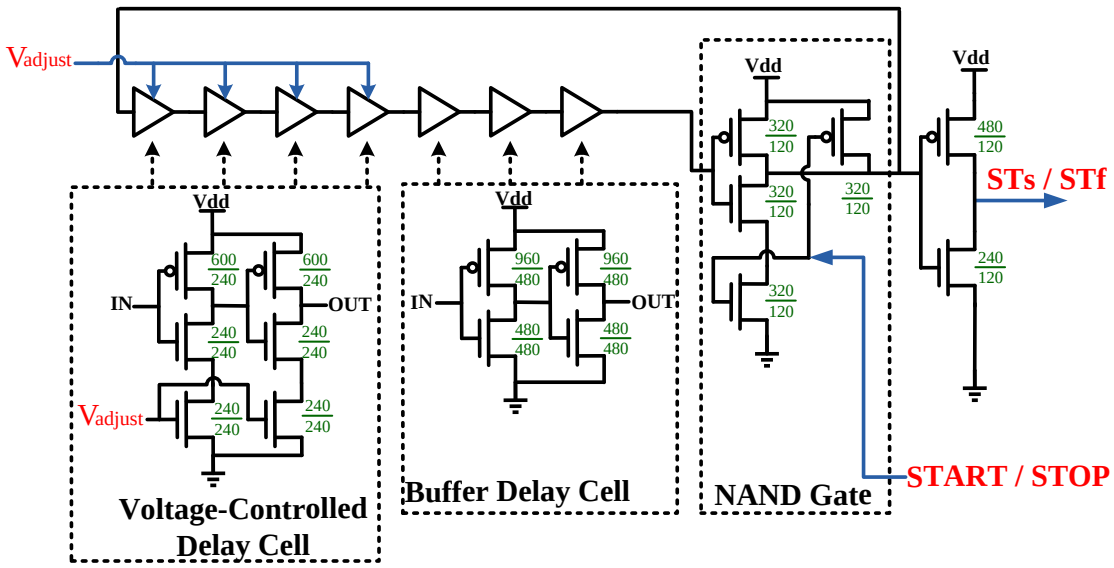



Figure 3.12. Schematic of the triggerable voltage-controlled oscillator

The slow and fast triggerable voltage-controlled oscillators have the same architecture. The adjust voltage, $V_{adjust}$, of the fast oscillator is connected to the $V_{DD}$ allowing a fast oscillation frequency. Meanwhile, the adjust voltage of the slow oscillator is connected to an externally controlled voltage (lower than VDD), producing a slower but tunable oscillation frequency, as shown in Figure 3.13. The slow oscillator features a tunable oscillation period of 4.470ns down to 2.610ns that depends on the control voltage within the 0.5V to 1.2V range, while the fast oscillator has a steady oscillation period of 2.610ns. In order to establish a time resolution of 25ps for the proposed single-stage VTDC, the

oscillation period of the slow oscillator is kept at 2.635ns by applying the adjust voltage around 1.1V.

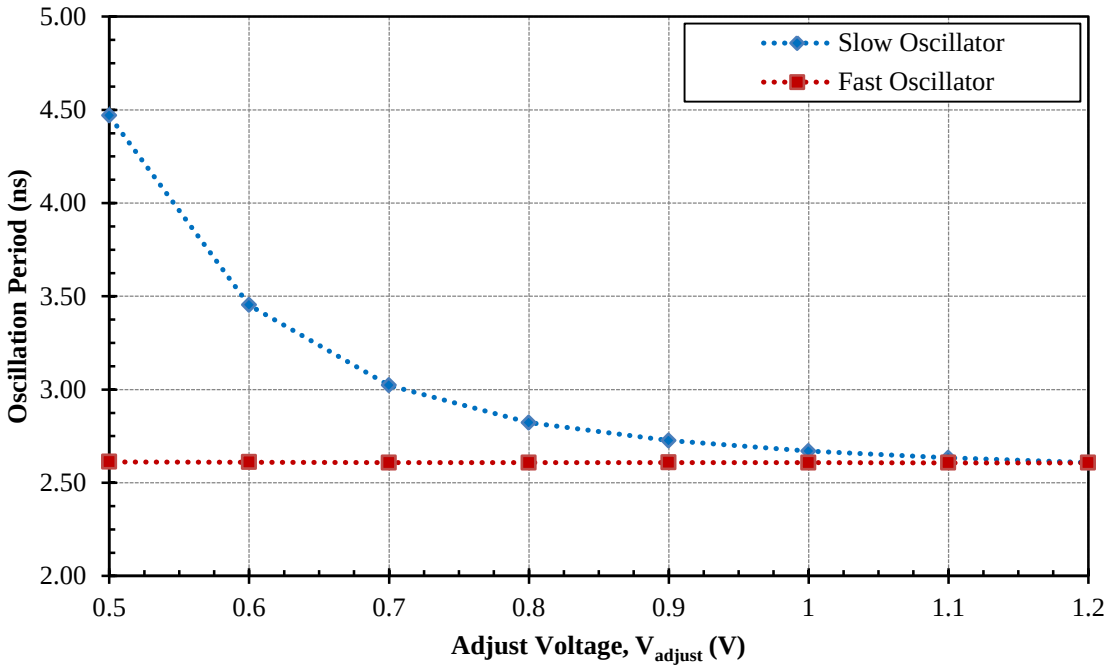



Figure 3.13: Oscillation periods of the voltage-controlled oscillators versus adjust voltage

### 3.3.2. Dynamic-logic Phase Detector

The dynamic-logic phase detector is a two stage phase detector constructed with a Delayed-Input-Pulse Dynamic Phase Frequency Detector (DIP-PFD) [21] followed by a $C^2$MOS register (Figure 3.14). The dynamic-logic phase detector compares the phase difference between the $ST_s$ and the $ST_f$ signals and generates the *Start-of-Conversion signal* (SoC) to control the measurement process.

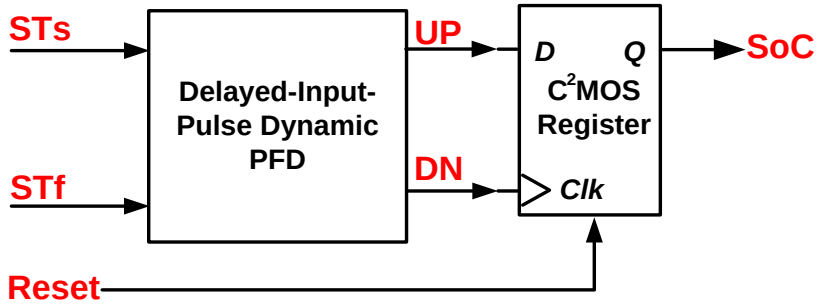



Figure 3.14: Dynamic-logic phase detector

The first stage of the dynamic-logic phase detector is the Delayed-Input Pulse Phase-Frequency Detector (DIP-PFD) proposed in [21]. It has been chosen because of its zero dead-zone and extended detection range characteristics. The PFD (Figure 3.15) compares the phases and frequencies of the input signals, and generates the *UP* and *DN* error pulses based on the phase and frequency difference between the input signals.

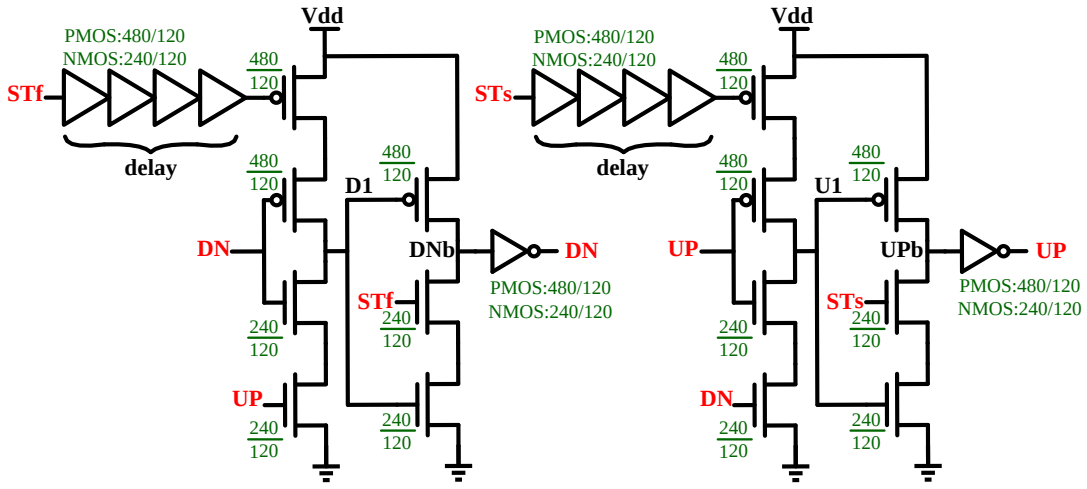



Figure 3.15: Delayed-Input-Pulse Phase Frequency Detector [20]

In this DIP-PFD, when the $ST_s$ and $ST_f$ signals are low, the *U1* and *D1* nodes are precharged high. When $ST_s$ rises, the *UPb* node is discharged, producing the *UP* pulse. On the arrival of the rising edge of $ST_f$, the *DNb* node is pulled low, generating the *DN*

pulse. When both outputs *UP* and *DN* are high, the *U1* and *D1* nodes will be pulled low, causing the *UPb* and *DNb* nodes to go high. This condition will deactivate the *UP* and *DN* pulses and reset the PFD. The difference in the pulse width between the *UP* and *DN* signals is therefore equal to the phase difference between $ST_s$ and $ST_f$. Since the dynamic-logic PFD uses its own output signals directly to reset itself, there is virtually no dead-zone in this design.

The second stage of the dynamic-logic phase detector (Figure 3.14) is a $C^2$MOS register. The error signals, *UP* and *DN*, generated by the DIP-PFD are connected to a $C^2$MOS register (Figure 3.16).

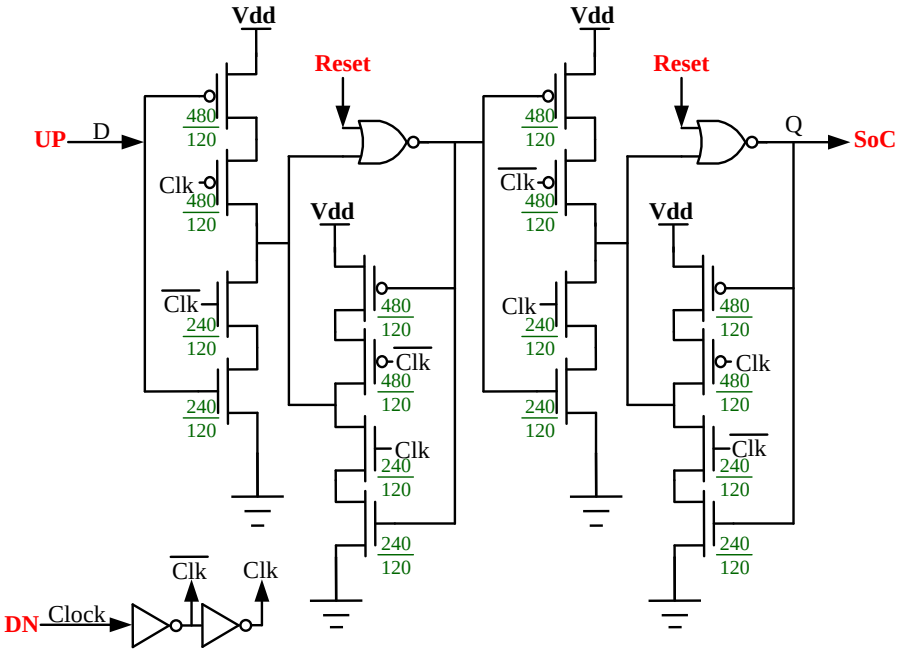



Figure 3.16: $C^2$MOS register used in the dynamic-logic phase detector

The register is used to sample the *UP* signal by the *DN* signal as the clock. In the case when the *UP* signal leads the *DN* signal, the $C^2$MOS register will generate *SoC* signal to

enable the counter clock. When $ST_f$ catches up to $ST_s$, the *UP* and *DN* signals will overlap each other. The Data input signal of the $C^2$MOS register will change at the same time as the Clock signal so that the output signal, *SoC*, will fall to deactivate the counter clock, as shown in Figure 3.17.

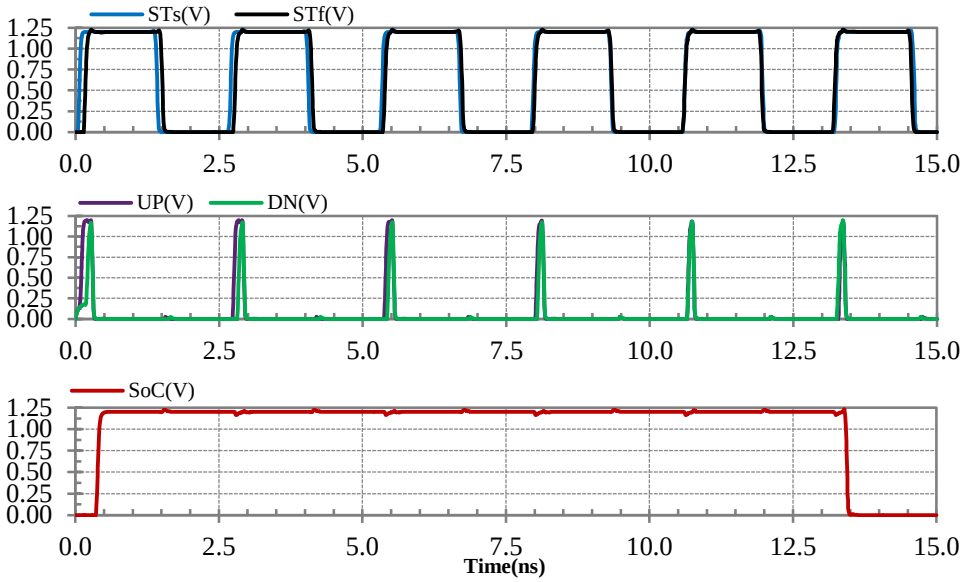



Figure 3.17: Timing diagram of dynamic-logic phase detector

However, since the required setup time of the C2MOS register is sensitive to process variation, the *SoC* signal may remain high for additional oscillation cycles. This will result a minor time offset to the time measurement. This time offset can be easily determined and removed by measuring zero input phase difference [9]. Due to the offset, the input phase different Tin calculation must be modified. Taking offset into account, the measured input phase difference $T_{in}$ is equal:

$$T_{in} = (T_s - T_f) \times (CNT - offset) \tag{3.4}$$

### 3.3.3. Counter

The *SoC* signal generated by the dynamic-logic phase detector controls the operation of a counter, which counts the number of cycles the measurement takes (CNT). A 6-bit counter has been designed with $C^2MOS$ registers, as shown in Figure 3.18. The counter is enabled by the *SoC* signal and clocked by the $ST_f$ signal. Each stage of the counter divides the clock frequency signal by half. Therefore, the output signal of each register oscillates two times slower than its input clock signal. The final output signal levels [Q0:Q5] can be interpreted as the binary value of the CNT. The input phase difference, $T_{in}$, can be calculated with the CNT by using Equation 3.3.

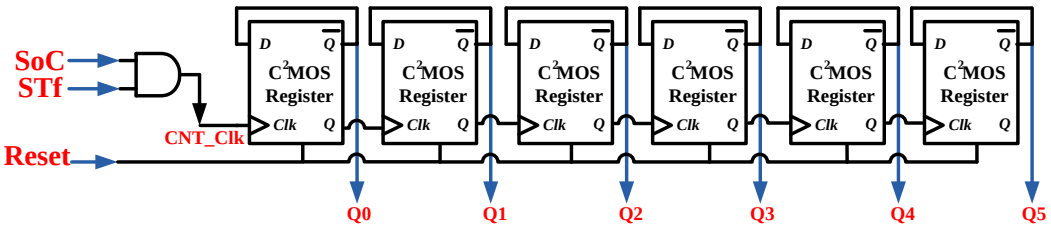



Figure 3.18: Block diagram of the 6-bit counter

# CHAPTER 4 PERFORMANCE ANALYSES OF TDA AND VTDC

The design of the single-stage VTDC with TDA integrates the modified DLL based TDA and the single-stage VTDC with dynamic-logic phase detector. With single-stage VTDC's 25ps time resolution and a time amplification gain of 10 from the modified DLL based TDA, the proposed TDC architecture, single-stage VTDC with TDA, is expected to achieve a 2.5ps time resolution. This chapter analyzes the performances and characteristics of the modified DLL based TDA, the single-stage VTDC with dynamic-logic phase detector, and the single-stage VTDC with TDA. The designs of the circuitries presented in the last chapter have been designed using 0.13μm IBM CMOS process available through CMC, and analyzed using HSPICE simulator in Cadence Analog Design Environment. This chapter describes the accuracy setup of the analysis in HSPICE and presents the performance analysis results with process corner, supply voltage, and temperature variations. The netlist of the single-stage VTDC with TDA can be found in the Appendix A.

## 4.1. Accuracy Setup of Transient Analysis in HSPICE

The transient analysis in HSPICE has many control options that can modify the analysis for trading in the simulation accuracy for speed. With different control options related to the method, tolerance, and limit, the transient analysis computes results using different algorithms and parameters. The default control option of the transient analysis uses

algorithms that balance between simulation speed and accuracy and provides moderate, albeit sufficient in most cases, simulation accuracies. Meanwhile, the ACCURATE option of the transient analysis can provide results with higher accuracies using more complex algorithms with slower speed [25].

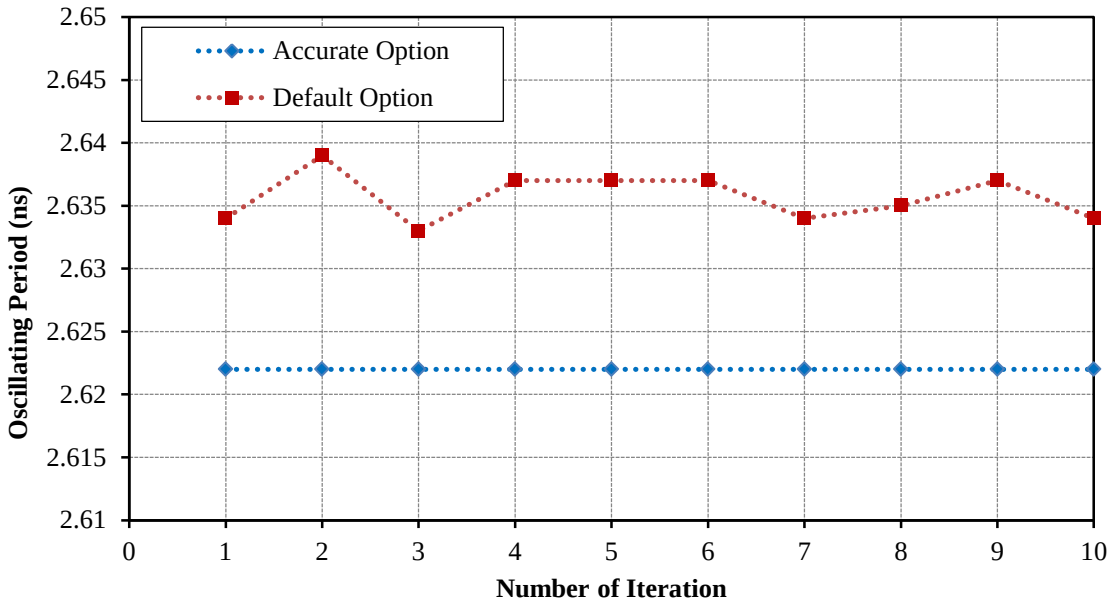



Figure 4.1: Period variations of an oscillator with and without enabling ACCURATE option

The accuracies of the transient analyses with the default control option are generally sufficient for common circuit analyses. However, since the designed TDC architecture in this thesis deals with picosecond time interval measurements, ACCURATE option in the transient analyses is necessary for the performance analyses. The differences between the analyzed results with the default control option and with the ACCURATE option can be easily observed in the performance analyses of the triggerable ring oscillator, as shown in Figure 4.1. The result of the transient analysis without ACCURATE option shows irregular variations on the oscillating periods due to the computational errors, while the result of the transient analysis with ACCURATE option enabled shows stable oscillating

periods. This shows that enabling the ACCURATE option in the transient analysis can minimize the computational error and provide more precise simulation results. Although the transient analyses with ACCURATE option require about 130% longer simulation time, enabling the ACCURATE option is necessary for evaluating the performance of the designed TDC architecture.

## 4.2. Modified DLL Based TDA

The schematic diagram of the modified DLL based TDA is shown in Figure 4.2. It consists of the dynamic-logic PFD, the balanced charge pump, the delay element, and edge sampler circuit designs from chapter 3. The modified DLL based TDA has been simulated in the typical-typical (TT), fast-fast (FF), and slow-slow (SS) process corners to verify the circuit performance versus process variations.

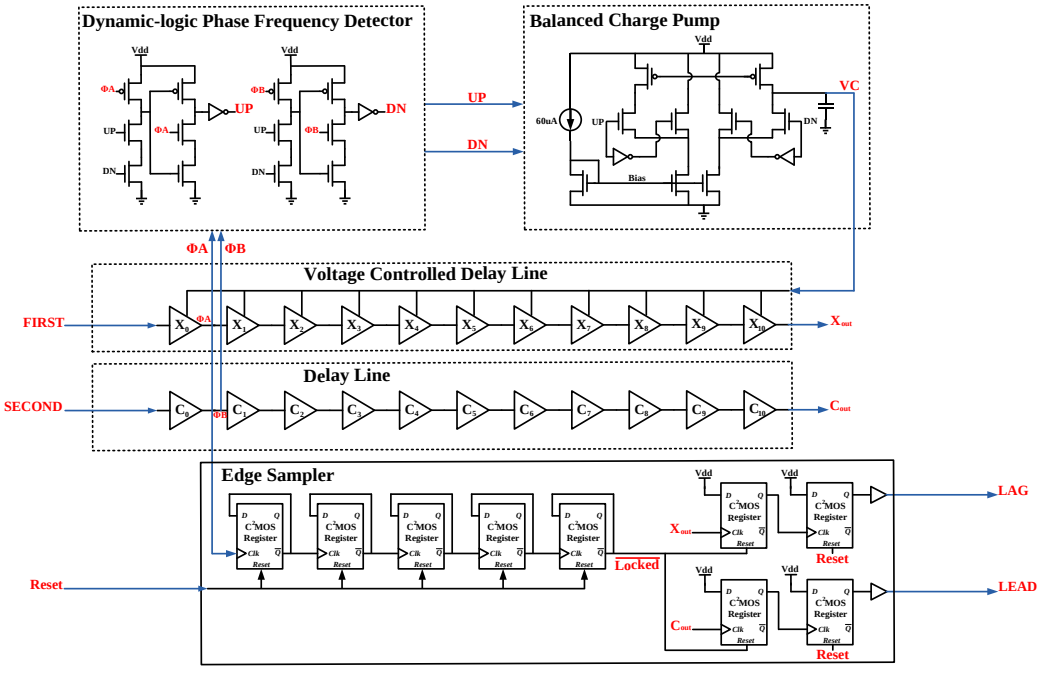



Figure 4.2: The schematic diagram of the modified DLL based TDA

The Figure 4.3 shows the output time intervals as a function of the input time intervals, $T_{in}$, in the three different process corners. As shown in Figure 4.3 and Figure 4.4, the modified TDA has a linear output characteristic within the input range from 0 to 100 ps. In comparison with the original DLL based TDA [18], the modified TDA outperforms in gain linearity for the very short input time intervals. A detailed analysis of TDA developed here has revealed its almost perfect linear gain characteristics within the 0 to 10ps time range (Figure 4.4). The linearity starts to deteriorate for the input time intervals larger than 110ps because of exceeding the maximum delay time difference in the FF process corner. This determines the input range of the modified DLL based TDA to be 100ps in the worst process corner.

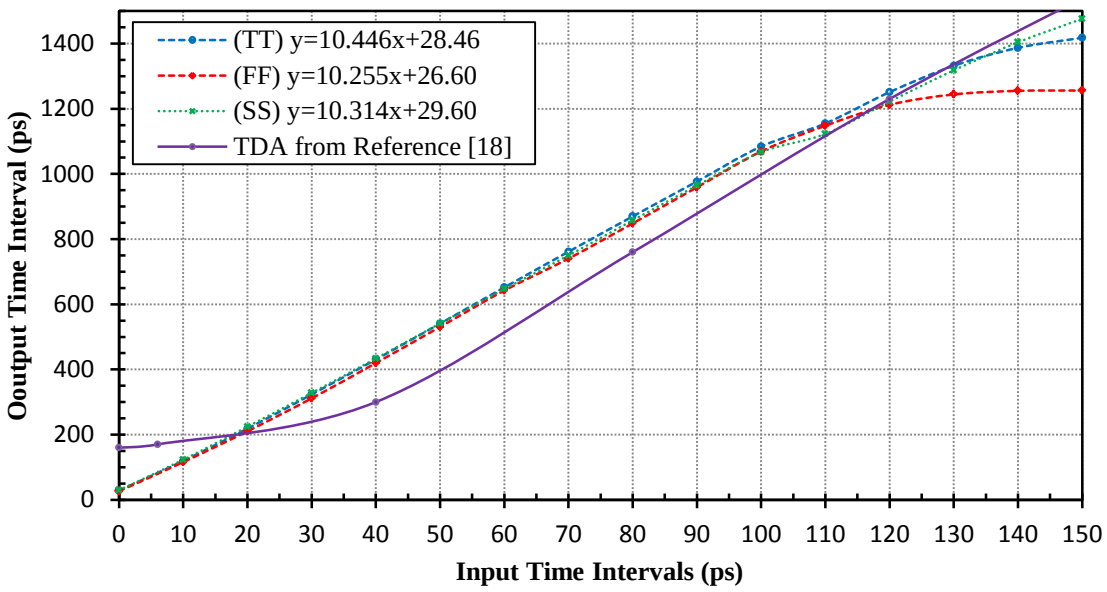



Figure 4.3: Output time intervals for the modified TDA

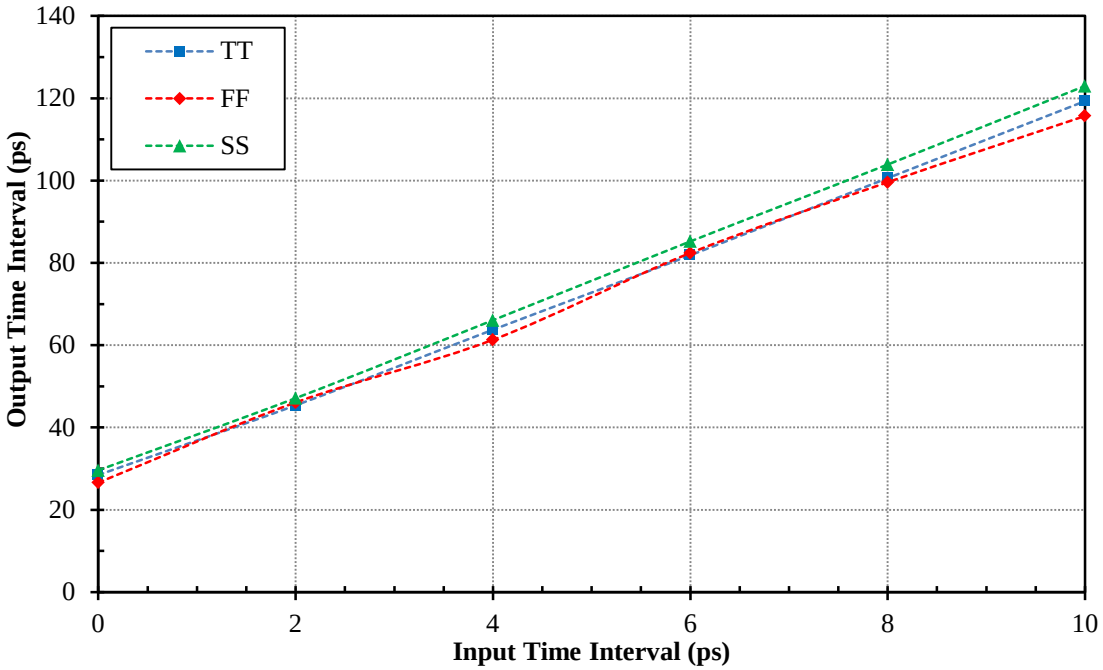



Figure 4.4: Output time intervals for the modified TDA with short input time intervals

Table 4.1 summarizes the gain and time offset variations of the modified TDA with different process corners. The simulated results reveal a maximum 1.1% gain variation and an average time offset of 28ps. These results indicate that the process variations have little impact on the gain and time offset.

Table 4.1: The TDA performance parameters with process variations

| Performance Parameters of TDA | SS | TT | FF |
|---|---|---|---|
| Gain | 10.31 | 10.45 | 10.26 |
| Time Offset | 29.6ps | 28.5ps | 26.6ps |
| Input Range | 150ps | 140ps | 100ps |

The Figure 4.5 shows the output time intervals as a function of the input time interval in the presence of ±10% supply voltage variation. The gain of the modified TDA is very

close to the theoretical value of N=10 at nominal power supply voltage 1.2V and it varies less than 5.8% for ±10% power supply variation.

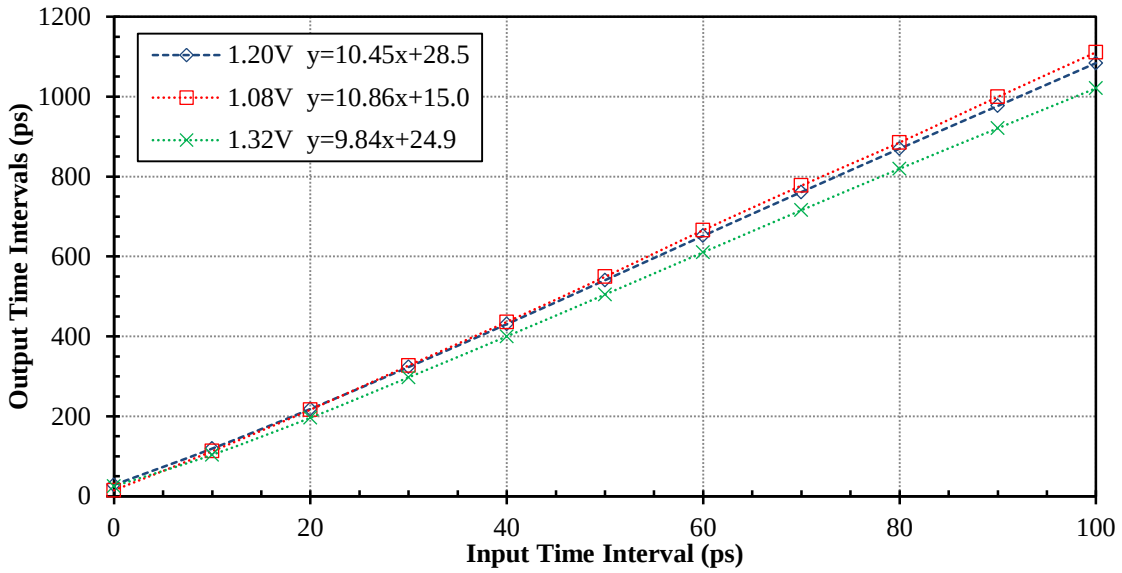



Figure 4.5: Output time intervals in case of ±10% supply voltage variation (TT Corner)

The gain of the modified TDA with respect to different ambient temperatures is shown in Figure 4.6. The gain of the modified TDA varies with temperature, however the variations are small (±1% over the temperature range of 0 ºC to 80 ºC).

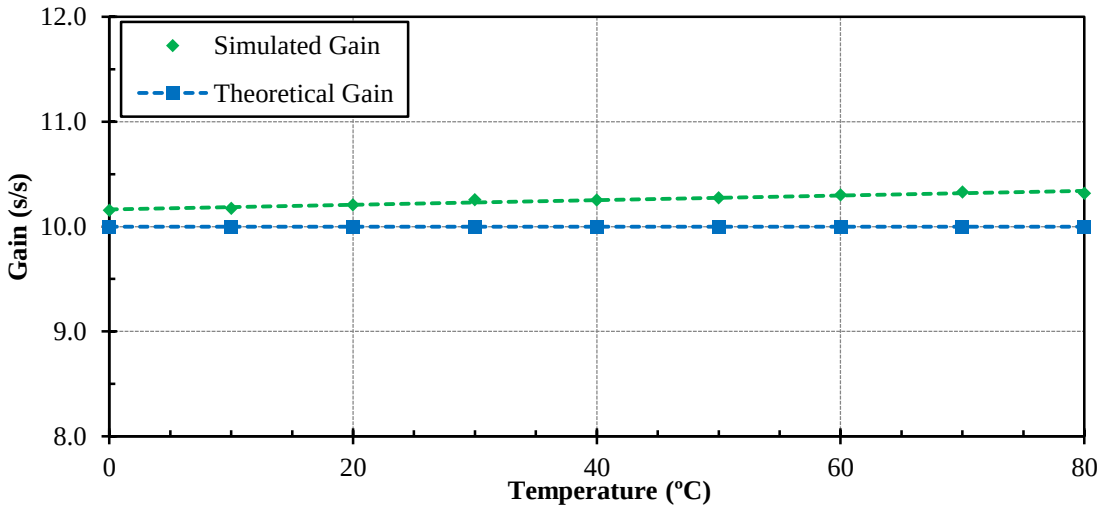



Figure 4.6: Gain fluctuations with temperature

The modified DLL based TDA has demonstrated a stable gain for input time intervals range from 0 to 100ps, with excellent linearity for very short time intervals, 0 to 10ps. With the DLL based design, the modified DLL based TDA has shown reliable performance against process, supply voltage, and temperature variations. The presented simulation results have confirmed the very important role of the DLL quality for the performance improvement of the DLL based TDA. Table 4.2 shows the performance comparison to the other closed-loop TDA designs.

Table 4.2: Performance comparison of the TDA circuits

| | [18] | [22] | This work |
|---|---|---|---|
| Technology | 0.18μm | 65nm | 0.13μm |
| Gain | 1~32 | 4 | 10 |
| Abs. Gain Error | N/A | 19.5% | 4.5% |
| Linear Output Range | 60~480ps | 0~300ps | 0~100ps |
| Gain Variation (Supply Voltage) | N/A | 1.4% | 5.8% |
| Gain Variation (Temperature) | N/A | N/A | <1% |
| Gain Variation (Process Corners) | N/A | N/A | 1.1% |

## 4.3. Single-stage VTDC with Dynamic-logic Phase Detector

The Figure 4.7 shows the schematic diagram of the single-stage VTDC with dynamic-logic phase detector. It consists of the triggerable ring oscillator, the dynamic-logic phase detector, and the 6-bit counter designs presented in chapter 3.

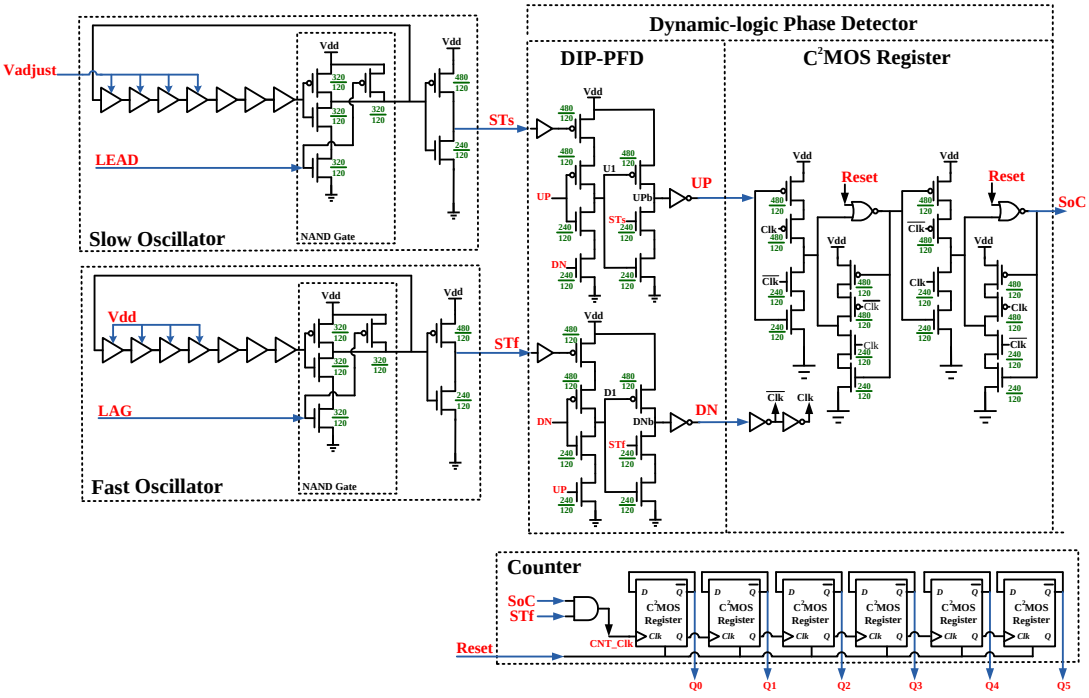



Figure 4.7: Schematic diagram of the single-stage VTDC

The Figure 4.8 shows digital output as a function of the input phase difference, simulated in the TT technology corner. The resolution control voltage, $V_{adjust}$, has been set to 1.10V to achieve the resolution approximately 25ps. The output characteristics of the single-stage VTDC with dynamic-logic phase detector are linear within the time range from 0 to 1600ps. These results demonstrate that the circuit can correctly detect the phase difference and control the measurement process even at an oscillation period difference of 25ps.

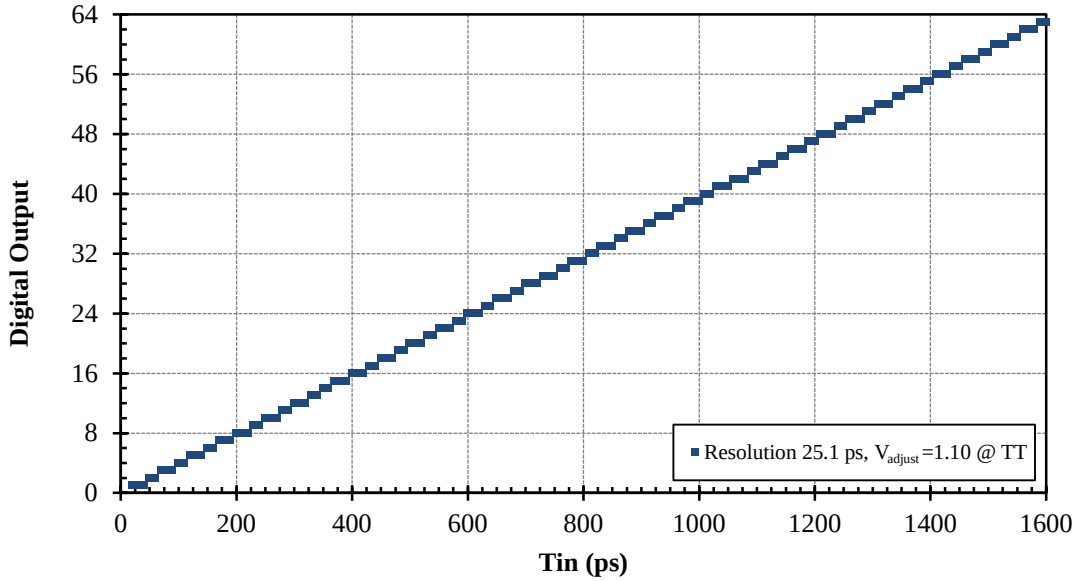



Figure 4.8: Digital Output characteristic of the single-stage VTDC with the dynamic-logic phase detector in TT process corner

The digital output characteristic of the single-stage VTDC with the dynamic-logic phase detector is compared with the single-stage VTDC with a classic register-type phase detector implemented in the TSMC 0.35µm CMOS as reported in [11]. As shown in Figure 4.9, the corresponding time resolution of this design was 37.5ps, and the characteristics offset estimated as 125ps [11]. The single-stage VTDC with the dynamic-logic phase detector has much smaller offset, in the order of 25ps. The large offset of this VTDC [11] is likely due to the classic register-type phase detector. This offset results from a substantial dead zone of the classic register-type phase detector. When the input time differences, $T_{in}$, is smaller than the width of the detector's dead-zone, the VTDC is unable to produce a digital output. Using the DIP-PFD dynamic-logic phase detector clearly decreases the characteristics offset and makes measurements of small phase differences possible.

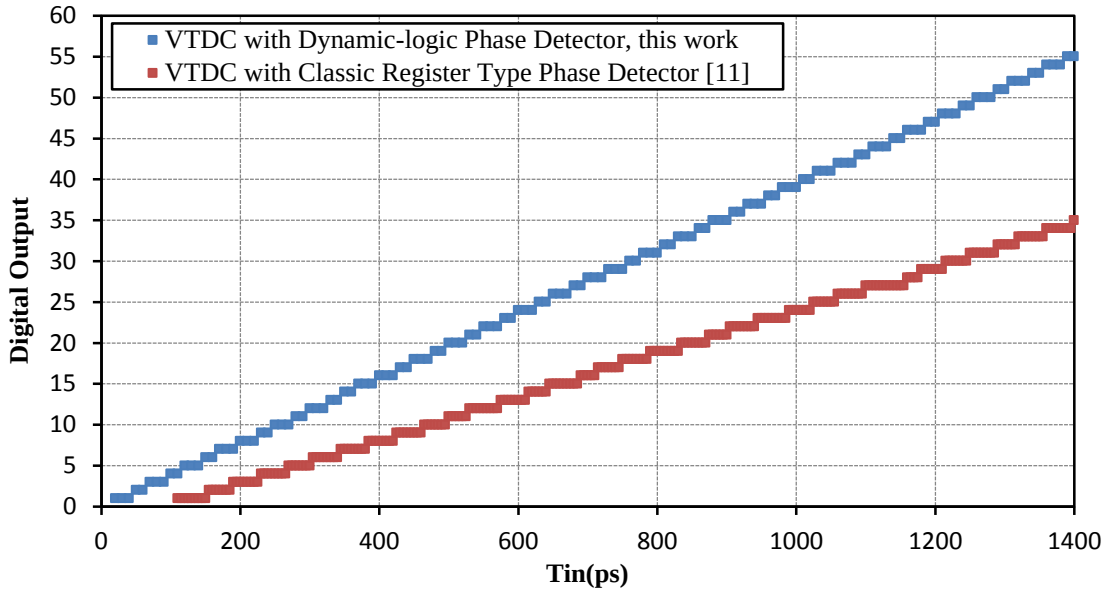



Figure 4.9: Comparison of the digital output characteristics of the single-stage VTDC with the dynamic-logic phase detector with the characteristics of the single-stage VTDC with the classic register-type phase detector from [11]

The ability to vary the VCO's oscillation frequency can be used to control the resolution of the single-stage VTDC with the dynamic-logic phase detector. As shown in Figure 4.10, by varying $V_{adjust}$, one can achieve better resolutions of the time measurements and further minimization of the offset. In the simulation results shown in Figure 4.10, $V_{adjust}$ has been chosen to achieve two different time resolutions. In comparison with the lower voltage setup of $V_{adjust}$, setting the $V_{adjust}$ to higher voltage value allows the designed single-stage VTDC to achieve better time resolution. However, the increased time resolution also leads to a smaller input dynamic range. Hence, the resolution control voltage adjustment can be used for applications that require different time resolutions and dynamic ranges.

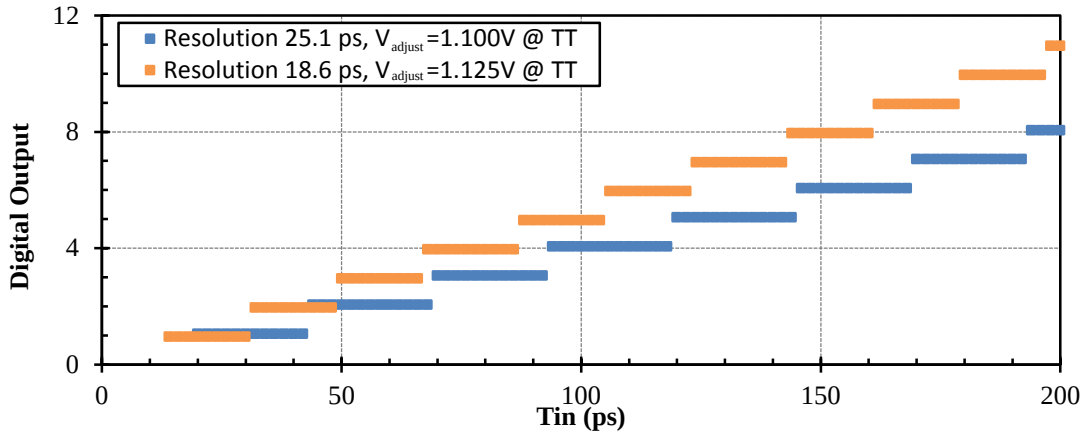



Figure 4.10: Time resolution comparison of the designed single-stage VTDC with different resolution control voltages, $V_{adjust}$

Without the PLL-type stabilization of the VCO, the single-stage VTDC characteristics will vary with process variations. The results presented in Figure 4.11 show significant variations in time measurement resolution, and in the circuit gain and offset. In order to diminish this effect while keeping the circuit architecture simple, $V_{adjust}$ has been appropriately adjusted to vary the VCO oscillation frequency and also to compensate for the process variations.

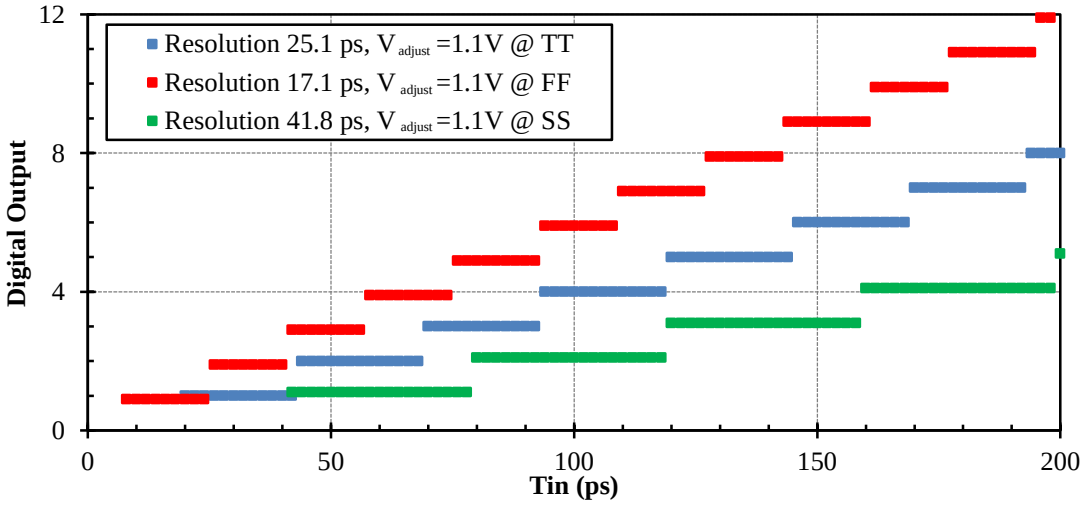
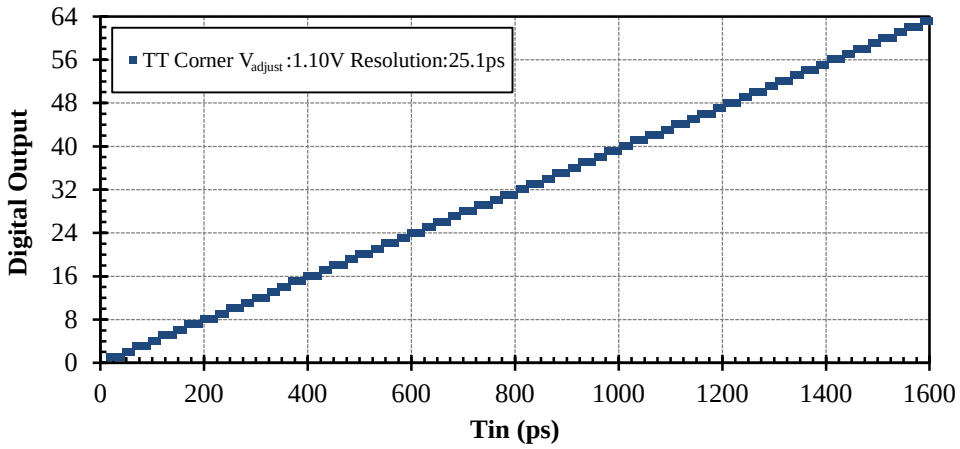
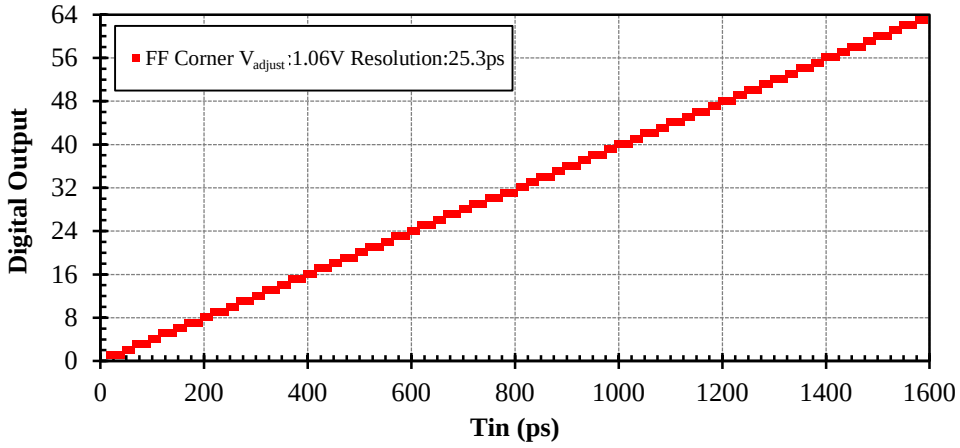



Figure 4.11: Variability of the digital output characteristics of the single-stage VTDC with the dynamic-logic phase detector as a function of process variations with a constant control voltage, $V_{adjust}$=1.10V.

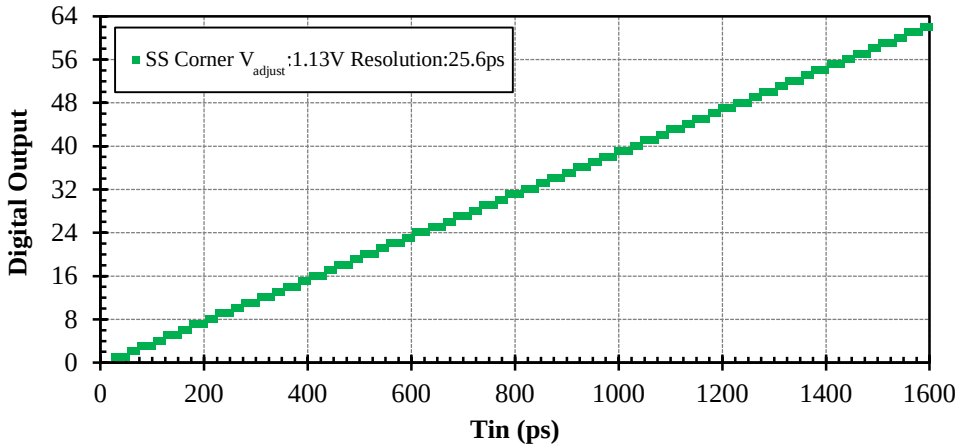
The compensated results are shown in Figure 4.12, demonstrating that it is possible to obtain nearly identical output characteristics in different process corners by adjusting the $V_{adjust}$. The digital output characteristics of the designed single-stage VTDC in the TT corner ($V_{adjust}$=1.10V, Figure 4.12a), are almost the same as in the FF corner (bur for the $V_{adjust}$=1.06V, Figure 4.12b), and as in the SS corner (but for the $V_{adjust}$=1.13V, Figure 4.12c). Hence, the resolution control voltage, $V_{adjust}$, can be used not only for setting up the parameters of the single-stage VTDC, but also for calibration if necessary.




(a) Typical-Typical corner




(b) Fast-Fast corner




(c) Slow-Slow corner

Figure 4.12: Digital output characteristics of the single-stage VTDC with the DIP-PFD dynamic-logic phase detector in the different process corners (a) TT (b) FF (c) SS compensated using different values of the control voltage

By utilizing the dynamic-logic phase detector that eliminated the dead-zone problem, the designed single-stage VTDC has demonstrated a linear digital output characteristic with a 25ps time resolution. The presented analysis results have confirmed the very important role of the phase detector quality for the performance of single-stage VTDC with sub-gate delay resolutions.

## 4.4. Single-stage VTDC with TDA

The design of the single-stage VTDC with TDA is a time amplified TDC. It consists of the single-stage VTDC with dynamic-logic phase detector and the modified DLL based TDA. The detail schematic of the single-stage VTDC with TDA is shown in Figure 4.13. The input time interval between input signals, *START* and *STOP*, is first amplified with a factor of 10 using the modified DLL based TDA. The amplified output time interval of TDA is then measured using the single-stage VTDC with dynamic-logic phase detector.

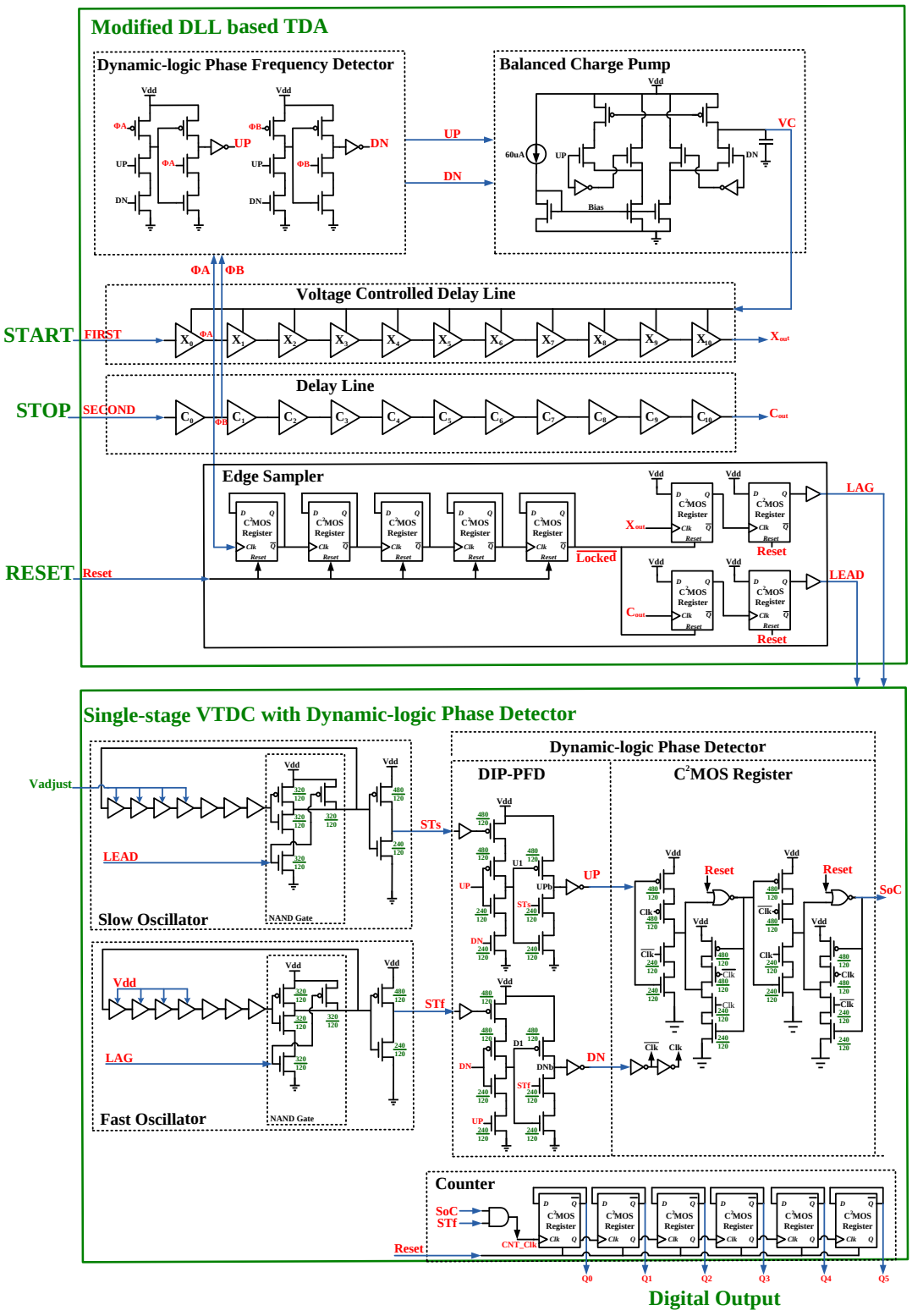
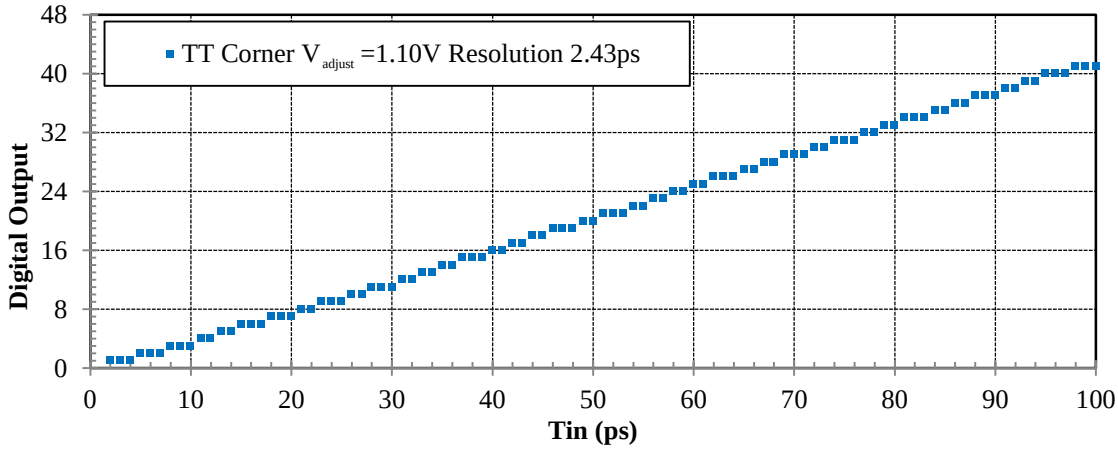


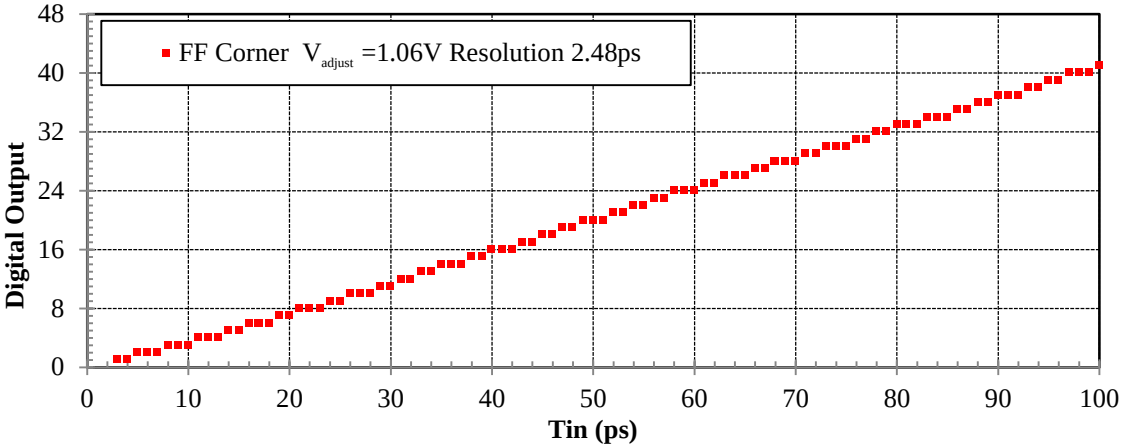

Figure 4.13: Schematic of the single-stage VTDC with TDA

The modified DLL based TDA pre-amplifies the input time interval with a gain of 10, and the amplified time intervals is then measured using the single-stage VTDC with dynamic-logic phase detector with a 25ps time resolution. With the input time interval pre-amplification, the single-stage VTDC with TDA is expected to achieve a 2.5ps time resolution. However, the single-stage VTDC with TDA has a relative short dynamic range, 100ps, which is mainly limited by the short input range of the modified DLL based TDA.

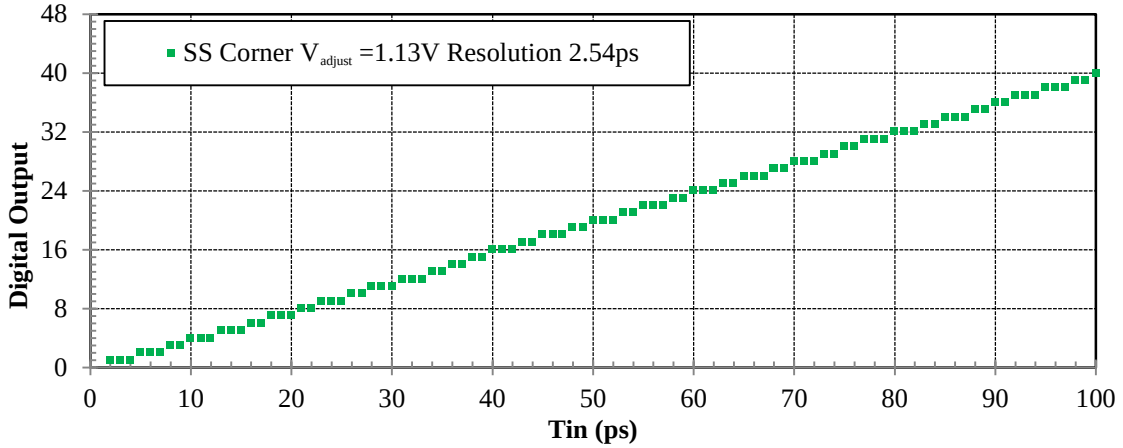
The performance of the single-stage VTDC with TDA designed using 0.13µm IBM CMOS process has been analyzed using HSPICE simulator in Cadence Analog Design Environment. The single-stage VTDC with TDA was simulated in the TT, FF, and SS process corners to verify the performance against process variations. In order to diminish the process variations of the single-stage VTDC, the resolution control voltage, $V_{adjust}$, has been appropriately adjusted. The Figure 4.14 shows the digital output characteristics of the single-stage VTDC with TDA in different process corners.




(a) Typical-Typical corner




(b) Fast-Fast corner




(c) Slow-Slow Corner

Figure 4.14: Digital output characteristics of the single-stage VTDC with TDA in the difference process corners a) TT b) FF c) SS

As shown in Figure 4.14, the single-stage VTDC with TDA has linear output characteristics in three different process corners for a dynamic range from 0 to 100ps in difference process corners. The performance analyzed results reveal a 4.5% of time resolution variation in different process corners. These results indicate that the process variations have little impact on the time resolution. Table 4.3 shows the performance comparison to other TDC designs.

Table 4.3: Performance summary of the single-stage VTDC with TDA

| | [18] | [11] | This Work |
|---|---|---|---|
| Technology | 0.18μm | 0.35μm | 0.13μm |
| Supply Voltage | 1.8V | 3.3V | 1.2V |
| Resolution @ TT corner | 5.1ps | 37.5ps | 2.43ps |
| Resolution Variation (Process Corners) | N/A | N/A | 4.53% |
| Dynamic Range | 60~460ps | >50ns | 0~100ps |
| Gain of TDA | 1~32 | N/A | 10.43 |
| Resolution Without Time Amplification | 170ps | 37.5ps | 24.3ps |
| Measurement Rate | 1.5M sample/s | 100K sample/s | 6M sample/s |

# CHAPTER 5 CONCLUSIONS

Over the past few decades, the advancement in the deep-submicron CMOS technology has opened the possibility for creating SoCs with multi-gigahertz frequencies and high-level integrations. As the modern SoCs progress toward higher operational speed and greater complexity, measuring and characterizing the timing performance are becoming more challenging. Embedded time measuring devices are therefore becoming necessities for IC verification and characterization. TDCs have been widely used for on-chip time measurements for their reliable and precise time measuring performance. The time resolutions of the TDCs can vary from few nanoseconds to few picoseconds. However, accurate TDC architectures are scare and most implementations are challenging with 10ps time resolution or less.

The TDC architecture presented in this thesis has adopted the concepts of both time amplified TDC and single-stage VTDC to achieve sub-gate delay time resolution with minimum component mismatches. This thesis presents a new single-stage VTDC with a constant gain TDA. The circuit has been implemented using 0.13µm IBM CMOS technology, and analyzed using HSPICE simulator in Cadence Analog Design Environment. The TDC architecture presented in this work utilizes a dynamic-logic phase detector and a modified DLL based TDA. The zero dead zone characteristic of dynamic-logic phase detector allows for the single-stage VTDC to deliver a 25ps time resolution.

At the same time, the modified DLL based TDA further improves the time resolution by pre-amplifying the input time intervals with a gain of 10. The performance analyzed results of the developed single-stage VTDC with TDA has shown a linear measuring characteristic and an input dynamic range from 0 to 100ps with a 2.5ps time resolution. The result of the corner analyses has indicated that the process variation have little impact of the performance of the designed TDC architecture.

In conclusion, a single-stage VTDC with TDA has been developed and analyzed in this thesis. With the linear measuring characteristic and a 2.5ps time resolution, the developed TDC architecture can be utilized in very accurate time measurements application. The future research of the single-stage VTDC with TDA will target toward designing the circuit layout and verifying the effects of the parasitics and mismatches to the circuit operation. After the design verification, the designed layout will be submitted for fabrication process. Further research work will continue on circuit validation and evaluation for application to time-of-flight measurement in semiconductor nuclear radiation detectors for nuclear medical imaging systems.

# Appendices

# Appendix A: Netlist of Single-stage VTDC with TDA

```
** Generated for: hspiceD
** Design library name: thesis
** Design cell name: TDCTDA
** Design view name: schematic

** Library name: TDA
** Cell name: cap_var_delay_symbol
** View name: schematic
.subckt cap_var_delay_symbol gnd in out vc vdd
xm4 out net101 vdd vdd pfet l=120e-9 w=1.2e-6 nf=1 m=1 par=1 ngcon=1 ad=660e-15
as=660e-15 pd=3.5e-6 ps=3.5e-6
xm1 net101 in vdd vdd pfet l=120e-9 w=1.2e-6 nf=1 m=1 par=1 ngcon=1 ad=660e-15
as=660e-15 pd=3.5e-6 ps=3.5e-6
xt10 gnd net101 gnd gnd nfet l=1e-6 w=1.6e-6 nf=1 m=1 par=1 ngcon=1 ad=880e-15
as=880e-15 pd=4.3e-6 ps=4.3e-6
xt68 gnd out gnd gnd nfet l=1e-6 w=1.6e-6 nf=1 m=1 par=1 ngcon=1 ad=880e-15
as=880e-15 pd=4.3e-6 ps=4.3e-6
xt58 gnd net037 gnd gnd nfet l=2e-6 w=2e-6 nf=1 m=1 par=1 ngcon=1 ad=1.1e-12
as=1.1e-12 pd=5.1e-6 ps=5.1e-6
xt28 gnd net057 gnd gnd nfet l=2e-6 w=2e-6 nf=1 m=1 par=1 ngcon=1 ad=1.1e-12
as=1.1e-12 pd=5.1e-6 ps=5.1e-6
xt30 net101 vc net057 gnd nfet l=240e-9 w=1.2e-6 nf=2 m=1 par=1 ngcon=1 ad=264e-
15 as=660e-15 pd=2.08e-6 ps=4.6e-6
xt31 out vc net037 gnd nfet l=240e-9 w=1.2e-6 nf=2 m=1 par=1 ngcon=1 ad=264e-15
as=660e-15 pd=2.08e-6 ps=4.6e-6
xm5 out net101 gnd gnd nfet l=120e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
xm2 net101 in gnd gnd nfet l=120e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
.ends cap_var_delay_symbol
** End of subcircuit definition.

** Library name: thesis
** Cell name: VCDL
```

```
** View name: schematic
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xi161 gnd net28 net8 vcn vdd cap_var_delay_symbol
xi173 gnd net48 net13 vcn vdd cap_var_delay_symbol
xi139 gnd net23 net18 vcn vdd cap_var_delay_symbol
xi133 gnd net53 net23 vcn vdd cap_var_delay_symbol
xi147 gnd net18 net28 vcn vdd cap_var_delay_symbol
xi183 gnd net13 net33 vcn vdd cap_var_delay_symbol
xi107 gnd in a vcn vdd cap_var_delay_symbol
xi108 gnd a net43 vcn vdd cap_var_delay_symbol
xi170 gnd net8 net48 vcn vdd cap_var_delay_symbol
xi109 gnd net43 net53 vcn vdd cap_var_delay_symbol
xi182 gnd net33 out vcn vdd cap_var_delay_symbol
.ends VCDL
** End of subcircuit definition.

** Library name: TDA&TDC
** Cell name: 40ps_delay
** View name: schematic
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xt10 net8 in gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15
as=132e-15 pd=1.58e-6 ps=1.58e-6
xt1 out net8 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15
as=132e-15 pd=1.58e-6 ps=1.58e-6
xt0 out net8 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt12 net8 in vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
.ends _sub2
** End of subcircuit definition.

** Library name: TDA&TDC
** Cell name: c2mos_ff_reset
** View name: schematic
.subckt c2mos_ff_reset clk data gnd out outb reset vdd
xt20 outb net95 net0145 vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1
ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt21 net0145 net0363 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1
ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt13 net0157 net0363 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1
ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt11 net104 net95 net0157 vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1
ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt6 net29 data vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
```

xt4 net104 net87 net29 vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt0 net87 net95 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt2 net95 clk vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt24 outb net87 net0177 vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt25 net0177 out vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt9 net54 reset vdd vdd pfet l=120e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1 ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt27 net0363 net104 net54 vdd pfet l=120e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1 ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt30 out outb net58 vdd pfet l=120e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1 ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt31 net58 reset vdd vdd pfet l=120e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1 ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt16 outb net87 net0206 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt17 net0206 net0363 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt14 net0210 net0363 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt12 net104 net87 net0210 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt7 net0218 data gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt1 net87 net95 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt3 net104 net95 net0218 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt5 net95 clk gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt22 outb net95 net0238 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt23 net0238 out gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt8 net0363 net104 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt26 net0363 reset gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt28 out reset gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt29 out outb gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6

```
.ends c2mos_ff_reset
** End of subcircuit definition.

** Library name: thesis
** Cell name: ES
** View name: schematic
.subckt ES a cout xout gnd lag lead reset vdd
xi254 gnd net27 lead vdd _sub2
xi253 gnd net21 lag vdd _sub2
xi0 net40 vdd gnd net27 net077 reset vdd c2mos_ff_reset
xi1 net75 vdd gnd net21 net070 reset vdd c2mos_ff_reset
xi22 a net31 gnd net33 net31 reset vdd c2mos_ff_reset
xi21 cout vdd gnd net40 net39 b_lock vdd c2mos_ff_reset
xi26 net59 b_lock gnd net47 b_lock reset vdd c2mos_ff_reset
xi25 net66 net52 gnd net54 net52 reset vdd c2mos_ff_reset
xi24 net52 net59 gnd net61 net59 reset vdd c2mos_ff_reset
xi23 net31 net66 gnd net68 net66 reset vdd c2mos_ff_reset
xi20 xout vdd gnd net75 net74 b_lock vdd c2mos_ff_reset
.ends ES
** End of subcircuit definition.

** Library name: thesis
** Cell name: DL_PFD
** View name: schematic
.subckt DL_PFD a b dn gnd up vdd
xt0 net54 net50 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt3 up net54 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt5 net62 net70 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt6 dn net62 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt1 net50 a vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt4 net70 b vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt8 net34 net50 gnd gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt9 up net54 gnd gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt11 net42 dn gnd gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt13 net46 net70 gnd gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
```

```
xt59 net50 up net58 gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt7 net54 a net34 gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt2 net58 dn gnd gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt12 net62 b net46 gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt14 dn net62 gnd gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt10 net70 up net42 gnd nfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
.ends DL_PFD
** End of subcircuit definition.

** Library name: TDA
** Cell name: cap_con_delay_symbol
** View name: schematic
.subckt cap_con_delay_symbol gnd in out vdd
xt11 gnd out gnd gnd nfet l=2e-6 w=1e-6 nf=1 m=1 par=1 ngcon=1 ad=550e-15
as=550e-15 pd=3.1e-6 ps=3.1e-6
xt10 gnd net053 gnd gnd nfet l=2e-6 w=1e-6 nf=1 m=1 par=1 ngcon=1 ad=550e-15
as=550e-15 pd=3.1e-6 ps=3.1e-6
xm2 net053 in gnd gnd nfet l=120e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
xm5 out net053 gnd gnd nfet l=120e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
xm1 net053 in vdd vdd pfet l=120e-9 w=1.2e-6 nf=1 m=1 par=1 ngcon=1 ad=660e-15
as=660e-15 pd=3.5e-6 ps=3.5e-6
xm4 out net053 vdd vdd pfet l=120e-9 w=1.2e-6 nf=1 m=1 par=1 ngcon=1 ad=660e-15
as=660e-15 pd=3.5e-6 ps=3.5e-6
.ends cap_con_delay_symbol
** End of subcircuit definition.

** Library name: thesis
** Cell name: CDL
** View name: schematic
.subckt CDL b gnd in out vdd
xi146 gnd net39 net7 vdd cap_con_delay_symbol
xi132 gnd net27 net11 vdd cap_con_delay_symbol
xi160 gnd net7 net15 vdd cap_con_delay_symbol
xi172 gnd net43 net19 vdd cap_con_delay_symbol
xi180 gnd net19 net23 vdd cap_con_delay_symbol
xi123 gnd net31 net27 vdd cap_con_delay_symbol
xi117 gnd b net31 vdd cap_con_delay_symbol
xi179 gnd net23 out vdd cap_con_delay_symbol
```

```
xi138 gnd net11 net39 vdd cap_con_delay_symbol
xi171 gnd net15 net43 vdd cap_con_delay_symbol
xi116 gnd in b vdd cap_con_delay_symbol
.ends CDL
** End of subcircuit definition.

** Library name: thesis
** Cell name: B_CP
** View name: schematic
.subckt B_CP n_60ua dn gnd up vc vdd
xt20 net46 up vdd vdd pfet l=130e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt21 vc net15 vdd vdd pfet l=500e-9 w=4e-6 nf=2 m=1 par=1 ngcon=1 ad=880e-15
as=2.2e-12 pd=4.88e-6 ps=10.2e-6
xt2 net15 net15 vdd vdd pfet l=500e-9 w=4e-6 nf=2 m=1 par=1 ngcon=1 ad=880e-15
as=2.2e-12 pd=4.88e-6 ps=10.2e-6
xt22 net42 dn vdd vdd pfet l=130e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt41 vc dn net29 gnd nfet l=500e-9 w=2e-6 nf=1 m=1 par=1 ngcon=1 ad=1.1e-12
as=1.1e-12 pd=5.1e-6 ps=5.1e-6
xt40 vdd net42 net29 gnd nfet l=500e-9 w=2e-6 nf=1 m=1 par=1 ngcon=1 ad=1.1e-12
as=1.1e-12 pd=5.1e-6 ps=5.1e-6
xt39 vdd net46 net37 gnd nfet l=500e-9 w=2e-6 nf=1 m=1 par=1 ngcon=1 ad=1.1e-12
as=1.1e-12 pd=5.1e-6 ps=5.1e-6
xt9 net15 up net37 gnd nfet l=500e-9 w=2e-6 nf=1 m=1 par=1 ngcon=1 ad=1.1e-12
as=1.1e-12 pd=5.1e-6 ps=5.1e-6
xt23 net42 dn gnd gnd nfet l=130e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt19 net46 up gnd gnd nfet l=130e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt45 net37 n_60ua gnd gnd nfet l=500e-9 w=4e-6 nf=2 m=1 par=1 ngcon=1 ad=880e-15
as=2.2e-12 pd=4.88e-6 ps=10.2e-6
xt43 n_60ua n_60ua gnd gnd nfet l=500e-9 w=4e-6 nf=2 m=1 par=1 ngcon=1 ad=880e-
15 as=2.2e-12 pd=4.88e-6 ps=10.2e-6
xt44 net29 n_60ua gnd gnd nfet l=500e-9 w=4e-6 nf=2 m=1 par=1 ngcon=1 ad=880e-15
as=2.2e-12 pd=4.88e-6 ps=10.2e-6
.ends B_CP
** End of subcircuit definition.

** Library name: thesis
** Cell name: TDA
** View name: schematic
.subckt TDA first lag lead n_60ua reset second gnd vdd
c0 vc gnd cap
xi4 a vc gnd first xout vdd VCDL
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xi3 a cout xout gnd lag lead reset vdd ES
xi2 a b dn gnd up vdd DL_PFD
xi1 b gnd second cout vdd CDL
xi0 n_60ua dn gnd up vc vdd B_CP
.ends TDA
** End of subcircuit definition.

** Library name: thesis
** Cell name: DL_PD
** View name: schematic
.subckt DL_PD reset stf sts soc gnd vdd
xi0 dn up gnd soc net9 reset vdd c2mos_ff_reset
xt22 up net133 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt70 net133 net121 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt71 net121 up net24 vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt72 net24 net61 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt50 net137 net65 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt54 net141 net101 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt35 net145 net105 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt30 dn net149 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt24 net49 net109 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt11 net173 stf vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt41 net177 net145 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt58 net61 net113 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt47 net65 sts vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt51 net101 net137 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt27 net105 net49 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt12 net109 net173 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt55 net113 net141 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-
15 as=264e-15 pd=2.06e-6 ps=2.06e-6
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xt65 net88 net177 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt64 net161 dn net88 vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt63 net149 net161 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt48 net65 sts gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt52 net101 net137 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt29 net105 net49 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt13 net109 net173 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt56 net113 net141 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt23 up net133 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt69 net121 up net125 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt68 net125 dn gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt67 net129 net121 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt66 net133 sts net129 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt49 net137 net65 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt53 net141 net101 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt32 net145 net105 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt59 net149 stf net153 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt60 net153 net161 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt61 net157 up gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt62 net161 dn net157 gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt36 dn net149 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt14 net49 net109 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt10 net173 stf gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6

```
xt42 net177 net145 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-
15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt57 net61 net113 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-
15 as=132e-15 pd=1.58e-6 ps=1.58e-6
.ends DL_PD
** End of subcircuit definition.

** Library name: vernier
** Cell name: nand
** View name: schematic
.subckt nand a b gnd out vdd
xt4 out a vdd vdd pfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
xt1 out b vdd vdd pfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
xt3 out a net21 net21 nfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
xt0 net21 b gnd gnd nfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
.ends nand
** End of subcircuit definition.

** Library name: TDA&TDC
** Cell name: delay
** View name: schematic
.subckt delay adjust gnd in out vdd
xt69 net0183 net0191 vdd vdd pfet l=480e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1
ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt66 net0288 net104 vdd vdd pfet l=480e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1
ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt77 net0175 net0183 vdd vdd pfet l=480e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1
ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt76 out net0175 vdd vdd pfet l=480e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1 ad=528e-15
as=528e-15 pd=3.02e-6 ps=3.02e-6
xt67 net0199 net0288 vdd vdd pfet l=480e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1
ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt68 net0191 net0199 vdd vdd pfet l=480e-9 w=960e-9 nf=1 m=1 par=1 ngcon=1
ad=528e-15 as=528e-15 pd=3.02e-6 ps=3.02e-6
xt8 net76 net84 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
xt30 net68 in vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
xt4 net60 net80 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
xt3 net80 net64 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15
as=330e-15 pd=2.3e-6 ps=2.3e-6
```

xt0 net64 net68 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15 as=330e-15 pd=2.3e-6 ps=2.3e-6
xt12 net104 net72 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15 as=330e-15 pd=2.3e-6 ps=2.3e-6
xt7 net84 net60 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15 as=330e-15 pd=2.3e-6 ps=2.3e-6
xt11 net72 net76 vdd vdd pfet l=240e-9 w=600e-9 nf=1 m=1 par=1 ngcon=1 ad=330e-15 as=330e-15 pd=2.3e-6 ps=2.3e-6
xt106 out net0175 gnd gnd nfet l=480e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt98 net0288 net104 gnd gnd nfet l=480e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt100 net0191 net0199 gnd gnd nfet l=480e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt107 net0175 net0183 gnd gnd nfet l=480e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt101 net0183 net0191 gnd gnd nfet l=480e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt99 net0199 net0288 gnd gnd nfet l=480e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15 as=264e-15 pd=2.06e-6 ps=2.06e-6
xt75 net0260 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt74 net0264 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt48 net0257 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt32 net0265 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt50 net0285 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt47 net0293 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt49 net0305 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt51 net0309 adjust gnd gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt6 net84 net60 net0285 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt2 net80 net64 net0257 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt10 net72 net76 net0264 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt1 net64 net68 net0293 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt28 net68 in net0265 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6

```
xt9 net76 net84 net0309 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1
ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt5 net60 net80 net0305 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1
ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
xt13 net104 net72 net0260 gnd nfet l=240e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1
ad=132e-15 as=132e-15 pd=1.58e-6 ps=1.58e-6
.ends delay
** End of subcircuit definition.

** Library name: thesis
** Cell name: TRO
** View name: schematic
.subckt TRO trigger vadjust gnd out vdd
xi53 net21 trigger gnd net19 vdd nand
xt6 out net19 vdd vdd pfet l=120e-9 w=480e-9 nf=1 m=1 par=1 ngcon=1 ad=264e-15
as=264e-15 pd=2.06e-6 ps=2.06e-6
xt4 out net19 gnd gnd nfet l=120e-9 w=240e-9 nf=1 m=1 par=1 ngcon=1 ad=132e-15
as=132e-15 pd=1.58e-6 ps=1.58e-6
xi59 vadjust gnd net19 net21 vdd delay
.ends TRO
** End of subcircuit definition.

** Library name: vernier
** Cell name: and
** View name: schematic
.subckt and a b gnd out vdd
xt5 out net17 gnd gnd nfet l=120e-9 w=640e-9 nf=1 m=1 par=1 ngcon=1 ad=352e-15
as=352e-15 pd=2.38e-6 ps=2.38e-6
xt0 net13 b gnd gnd nfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
xt3 net17 a net13 net13 nfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
xt2 out net17 vdd vdd pfet l=120e-9 w=1.28e-6 nf=1 m=1 par=1 ngcon=1 ad=704e-15
as=704e-15 pd=3.66e-6 ps=3.66e-6
xt1 net17 b vdd vdd pfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
xt4 net17 a vdd vdd pfet l=120e-9 w=320e-9 nf=1 m=1 par=1 ngcon=1 ad=176e-15
as=176e-15 pd=1.74e-6 ps=1.74e-6
.ends and
** End of subcircuit definition.

** Library name: thesis
** Cell name: 6bit_Counter
** View name: schematic
.subckt thesis_6bit_Counter_schematic q0 q1 q2 q3 q4 q5 reset stf soc gnd vdd
xi16 soc stf gnd cnt_clk vdd and
```

```
xi6 net053 q5 gnd net046 q5 reset vdd c2mos_ff_reset
xi4 net060 q4 gnd net053 q4 reset vdd c2mos_ff_reset
xi3 net047 q3 gnd net060 q3 reset vdd c2mos_ff_reset
xi2 net054 q2 gnd net047 q2 reset vdd c2mos_ff_reset
xi1 net061 q1 gnd net054 q1 reset vdd c2mos_ff_reset
xi0 cnt_clk q0 gnd net061 q0 reset vdd c2mos_ff_reset
.ends thesis_6bit_Counter_schematic
** End of subcircuit definition.

** Library name: thesis
** Cell name: SSVTDC
** View name: schematic
.subckt SSVTDC lag lead q0 q1 q2 q3 q4 q5 reset vadjust gnd vdd
xi3 reset stf sts soc gnd vdd DL_PD
xi2 lead vadjust gnd sts vdd TRO
xi1 lag vdd gnd stf vdd TRO
xi0 q0 q1 q2 q3 q4 q5 reset stf soc gnd vdd thesis_6bit_Counter_schematic
.ends SSVTDC
** End of subcircuit definition.

****Parameter Setup****
.PARAM delay=20p period=3n adjust=1.1 cap=100f

****Initial Conditions****
.IC
+   V(xi1.soc)=0
+   V(xi1.stf)=0
+   V(xi1.sts)=0
+   V(xi0.vc)=0.6
+   V(xi0.up)=0
+   V(xi0.dn)=0
+   V(net18)=0
+   V(net19)=0

****Trans Analysis****
.TRAN 20e-9 200e-9 START=0.0
.OP

.TEMP 25
.OPTION
+   ACCURATE
+   ARTIST=2
+   INGOLD=2
+   MEASOUT=1
+   PARHIER=LOCAL
+   PSF=2
```

```
.INCLUDE "/ensc/grad1/cla115/Cadence/cmosp13/hspice_TT.include"
*.INCLUDE "/ensc/grad1/cla115/Cadence/cmosp13/hspice_FF.include"
*.INCLUDE "/ensc/grad1/cla115/Cadence/cmosp13/hspice_SS.include"

****Input Signal****
v6 stop gnd PULSE 1.2 0 delay 10e-12 10e-12 '500e-3*period' period
v8 start gnd PULSE 1.2 0 0 10e-12 10e-12 '500e-3*period' period

****Power Supply****
v2 vdd gnd DC=1.2
i2 vdd n_60ua DC=60e-6

****Resolution Adjustment****
v0 vadjust gnd DC=adjust

****Reset Signal****
v1 reset gnd PWL 0 1.2 1e-9 1.2 1.01e-9 0 TD=0

****Modified DLL Based TDA****
xi0 start net18 net19 n_60ua reset stop gnd vdd TDA

****Single-stage VTDC With Dynamic-logic Phase Detector
xi1 net18 net19 q0 q1 q2 q3 q4 q5 reset vadjust gnd vdd SSVTDC

.END
```

# Reference


[1] P. M. Levine and G. W. Roberts, "High-resolution flash time-to-digital conversion and calibration for system-on-chip testing," *Computers and Digital Techniques*, vol. 152, no. 3, pp. 415-426, May 2005.

[2] Matthew Collins and Bashir M. Al-Hashimi, "On-Chip Time Measurement Architecture with Femtosecond Timing Resolution ," in *11th IEEE European Test Symposium*, 2006, pp. 103-110.

[3] Zheng-hua Ma and Min Li, "Research on pulse hand-held laser rangefinder based TDC-GP2," in *International Conference on Computer Engineering and Technology (ICCET)*, Chengdu, China , 2010, pp. 670-672.

[4] ANTTI MÄNTYNIEMI, "An Integrated CMOS High Precision Time-to-Digial Converter Based On Stabilised Three-Stage Delay Line Interpolation," university of Oulu, Oulu, Finland, PhD Dissertation 2004.

[5] Wu Gao, Deyuan Gao, David Brasse, Christine Hu-Guo, and Yann Hu, "Precise Multiphase Clock Generation Using Low-Jitter Delay-Locked Loop Techniques for Positron Emission Tomography Imaging," *IEEE TRANSACTIONS ON NUCLEAR SCIENCE*, vol. 57, no. 3, pp. 1063-1070, June 2010.

[6] Brian K. Swann, Benjamin J. Blalock,Lloyd G. Clonts,David M. Binkley,James M. Rochelle, and K. Michelle Baldwin, "A 100-ps Time-Resolution CMOS Time-to-Digital Converter for Positron Emission Tomography Imaging Applications," *K. Michelle Baldwin*, vol. 39, no. 11, pp. 1839-1852, November 2004.

[7] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 3, pp. 220-224, 2006.

[8] Muung Shin, Masayuki lkebe, lunichi Motohisa and Eiichi Sana, "Column Parallel Single-Slope ADC with Time to Digital Converter for CMOS Imager ," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, 12-15 Dec. 2010, pp. 863 - 866.

[9] Antonio H. Chan and Gordon W. Roberts, "A Jitter Characterization System Using a Component-Invariant Vernier Delay Line," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 1, pp. 79-95, Jan. 2004.

[10] Jianjun Yu and Fa Foster Dai, "A 3-Dimensional Vernier Ring Time-to-Digital Converter in 0.13μm CMOS," in *IEEE Custom Integrated Circuit Conference (CICC)*, San Jose, 2010, pp. 1-4.

[11] Poki Chen, Chun-Chi Chen, Jia-Chi Zheng, and You Sheng Shen, "A PVT Insensitive Vernier-Based Time-to-Digital Converter With Extended Input Range and High Accuracy," *IEEE Transactions on Nuclear Science*, vol. 54, no. 2, pp. 294-302, April 2007.

[12] R. B. Staszewski, D. Leipold, Chih-Ming Hung, and P. T. Balsara, "TDC-based frequency synthesizer for wireless applications," in *IEEE Digest of Papers. Radio Frequency Integrated Circuits (RFIC) Symposium*, 2004, pp. 215-218.

[13] M. Mota and J. Christiansen, "A four-channel self-calibrating high-resolution time to digital converter," in *IEEE International Conference on Electronics, Circuits and Systems*, vol. 1, 1998, pp. 409-412.

[14] P. Dudek, S. Szczepanski and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 240-247, Feb 2000.

[15] C. S. Hwang, P. Chen, and H. W. Tsao., "A high-precision time-to-digital converter using a two-level conversion scheme," *IEEE Transactions on Nuclear Science*, vol. 51, no. 4, pp. 1349-1352, 2004.

[16] L. Vercesi, A. Liscidini, and R. Castello, "Two-Dimensions Vernier Time-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1504-1512, Aug. 2010.

[17] T. A. Jackson and A. Albicki, "Analysis of metastable operation in D latches," *IEEE Transactions on Circuits and Systems*, vol. 36, no. 11, pp. 1392-1404, Nov 1989.

[18] R. Rashidzadeh, R. Muscedere, M. Ahmadi, W.C. Miller, "A delay generation technique for narrow time interval measurement," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 7, pp. 2245-2252, July 2009.

[19] Chin-Hsin Lin and Marek Syrzycki, "Pico-second time interval amplification," in *International SoC Design Conference*, Incheon, Korea, 2010, pp. 201-204.

[20] Chin-Hsin Lin and Marek Syrzycki, "Single-stage Vernier Time-to-Digital Converter with Sub-Gate Delay Time Resolution," *Circuits and Systems, Scientific Research Publishing, USA*, vol. 2, no. 4, October 2011.

[21] Z. Cheng and M. Syrzycki, "Modifications of a Dynamic-Logic Phase Frequency Detector for extended detection range," in *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 53rd*, 2010, pp. 105-108.

[22] T. Nakura, S. Mandai, M. Ikeda, K. Asada, "Time difference amplifier using closed-loop gain control," in *2009 Symposium on VLSI Circuits Digest of Technical Papers*, 2009, pp. 208-209.

[23] S. Li and M. Ismail, "A high-Performance dynamic-logic phase-frequency detector," in *Trade-offs in analog circuit design: the designer's companion*, C. Toumazou et al., Ed. Netherlands: Kluwer Academic Publishers, 2002, ch. 28, pp. 821-842.

[24] W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," *International Symposium on Circuits and Systems (ISCAS)*, vol. 12, pp. 545-548, July 1999.

[25] "Transient Analysis," in *HSPICE User's Manual: Simulation and Analysis*. Campbell, CA, USA: Meta-Software, Inc., 1996, ch. 6, pp. 1-19.

[26] Mona Safi-Harb and Gordon Roberts, "DFT and BIST techniques for analogue mixed-signal test," in *Test and Diagnosis of Analogue, Mixed-signal and RF Integrated Circuits*, Yichuang Sun, Ed. London, UK: The Institution of Engineering and Technology, 2008, ch. 5, pp. 154-164.

[27] S. Tabatabaei and A. Ivanov, "Embedded timing analysis: A SOC infrastructure," *IEEE Design and Test of Computer*, vol. 19, no. 3, pp. 22-34, 2002.

[28] K. Maatta and J. Kostamovaara, "“A high-precision time-to-digital converter," *IEEE Trans. Instrum. Meas.*, vol. 47, no. 2, pp. 521-536, April 1998.

[29] Sally Safwat, Ezz El-Din Hussein, Maged Ghoneima, and Yehea Ismail, "A 12Gbps all digital low power SerDes transceiver for on-chip networking ," in *International Symposium on Circuits and Systems*, 2011, pp. 1419-1422.