Analysis and Design of a Low-Power Low-Noise CMOS Phase-Locked Loop

by

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ABSTRACT

This thesis covers the analysis, design and simulation of a low-power low-noise CMOS Phase-Locked Loop (PLL). Starting with the PLL basics, this thesis discussed the PLL loop dynamics and behavioral modeling.

In this thesis, the detailed design and implementation of individual building blocks of the low-power low-noise PLL have been presented. In order to improve the PLL performance, several novel architectural solutions has been proposed. To reduce the effect of blind-zone and extend the detection range of Phase Frequency Detector (PFD), we proposed the Delayed-Input-Edge PFD (DIE-PFD) and the Delayed-Input-Pulse PFD (DIP-PFD) with improved performance. We also proposed a NMOS-switch high-swing cascode charge pump that significantly reduces the output current mismatches. Voltage Controlled Oscillator (VCO) consumes the most power and dominates the noise in the PLL. A differential ring VCO with 550MHz to 950MHz tuning range has been designed, with the power consumption of the VCO is 2.5mW and the phase noise -105.2dBc/Hz at 1MHz frequency offset. Finally, the entire PLL system has been simulated to observe the overall performance. With input reference clock frequency equal 50MHz, the PLL is able to produce an 800MHz output frequency with locking time 400ns. The power consumption of the PLL system is 2.6mW and the phase noise at 1MHz frequency offset is -119dBc/Hz. The designs are implemented using IBM 0.13μm CMOS technology.

Keywords: PLL, Phase noise/Jitter, Delay-Input-Edge PFD (DIE-PFD), Delay-Input-Pulse PFD (DIP-PFD), blind-zone, NMOS-switch high-swing cascade charge pump, differential ring oscillator VCO

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LIST OF ABBREVIATIONS AND SYMBOLS

CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
CSA	Current steering amplifier
DIE-PFD	Delayed-Input-Edge Phase Frequency Detector
DIP-PFD	Delayed-Input-Pulse Phase Frequency Detector
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
PLL	Phase Locked Loop
PFD	Phase Frequency Detector
TSPC	True Single Phase Clock
VCO	Voltage Controlled Oscillator

K_{vco}	VCO gain (Hz/V)
I_P	Charge pump UP/DN current (A)
K_ϕ	PFD gain
N	Frequency divider division ratio
$Z(s)$	Loop filter transfer function
$G(s)$	PLL forward-loop gain
$H(s)$	PLL reverse-loop gain
$H(s)G(s)$	PLL open-loop gain
$CL(s)$	PLL closed-loop gain
$L_{SSB}(\Delta\omega)$	Single Side Band phase noise power spectral density to carrier ratio (dBc/Hz)
ϕ_{pm}	Phase margin (°)
f_{bw}	Loop Bandwidth (MHz)
ω_{bw}	Loop Bandwidth (Rad/s)
V_{ov}	Transistor over-drive voltage
V_{GS}	Transistor gate-to-source voltage
V_{TH}	Transistor threshold voltage

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1 INTRODUCTION

1.1 PLL Basics

Phase-Locked Loops (PLLs) are essential components in variety of modern electronic devices. While the concept of phase locking has been proposed decades ago, the demand for monolithic implementation of PLLs grows rapidly. The reasons for increasing popularity of the monolithic PLLs are high performance, low price, and the advance of integrated-circuit (IC) technologies in terms of speed and complexity.

A PLL is a circuit synchronizing an output signal with a reference signal in both frequency and phase. The phase error between the output signal and reference signal should be maintained at zero. If a phase error builds up, a PLL control mechanism forces the phase error reducing to minimum. It can be seen that the phase of the output signal is "locked" to the phase of the reference signal. This is the reason it is referred to as "phase-locked loop" [1].

1.2 Motivation

The use of PLLs for generating phase synchronous and frequency multiplied clocks are popular in applications such as communications, wireless systems, microprocessors, and

disk drive electronics. Some important examples of PLL application areas are illustrated in Tab. 1-1 [2].

Table 1-1. PLL Applications

Clock synthesis and synchronization circuits	Clock generation for microprocessors, DSP, memory
Frequency synthesizers	Local oscillator generation for wireless transceivers
Clock and data recovery circuits	Fiber optic data transceivers, disk drive electronics, local area network transceivers, DSL transceivers, Serial link transceivers
Modulator and demodulator circuits	Non-coherent modulator/demodulator in communication systems
Phase-locked receivers	Radar, Spacecraft

There are several figures of merit that determine PLL's performance, among which locking time, phase noise and jitter performance, and power consumption are the most important three. Locking time is the time it takes for PLL to produce the desired output frequency to within a certain frequency error tolerance [3]. Jitter is a random variation of the clock edges in time domain. Phase noise is the frequency domain representation of random fluctuations in the phase of a waveform. Jitter and phase noise represents the same phenomenon but in different domains. The application clock frequencies increase as new generations of CMOS technology become available; more stringent noise requirements are imposed on PLL because clocks with shorter periods are less tolerant to the random variation of clock edges. For noise sensitive applications such as wireless

transceivers and high speed data processing, one of the primary tasks is to minimize phase noise and jitter [2]. This requires special attention to both noise performance of individual block as well as PLL system behavior. Power consumption is another important parameter of PLL performance. It is especially important in portable applications such as cellular phones. Minimizing the power consumption usually means sacrificing the noise and jitter performance [3]. Therefore, the design and implementation of a high performance PLL requires excellent knowledge and experience in analog, digital, high frequency circuit design, as well as of the system level design tradeoffs.

The objectives of this thesis are

- To study PLL individual building blocks, PLL system level behavior, phase noise and jitter of PLL, as well as system design tradeoffs.
- To optimize individual building blocks of PLL for better performance.
- To design and implement a low-power, low-noise PLL system with IBM 0.13μm CMOS technology.

The design specification of the PLL is shown in Tab. 1-2.

Table 1-2. PLL design specification

Input Reference Clock Frequency	50 MHz
PLL Output Frequency	800 MHz
Feedback Frequency Division Ratio	16
Power Supply	1.2 V
Power Consumption	< 5 mW
Device Technology	IBM 0.13 μm CMOS

1.3 Thesis Organization

This thesis is organized as follows. The analysis, the mathematical modeling and phase noise and jitter of Charge-Pump PLL (CP-PLL) are discussed in Chapter 2. Chapter 3 presents the circuit design and simulation of the building blocks of the PLL system. In this chapter, novel architectural solutions of the PLL components have been proposed. In Chapter 4, system level simulations of PLL are presented and analyzed. The summary, conclusions and future work are discussed in Chapter 5.

2 ANALYSIS AND MODELING OF CHARGE-PUMP PHASE-LOCKED LOOP

There are several architectures of Phase-Locked Loops, among which Charge-Pump based structure is becoming recently one of the most popular. The reasons for its popularity include extended lock range and low cost [3]. The focus in this thesis is primarily on Charge-Pump Phase-Locked Loop (CP-PLL). All Phase-Locked Loops (PLL) from this point onwards are assumed to be Charge-Pump based Phase-Locked Loops unless stated otherwise. The main function of the PLL is to reproduce an output clock with a synchronized phase and frequency of the reference clock. This chapter will review and analyze the operation of the PLL.

2.1 Basic PLL System Overview

The block diagram of a PLL is shown in Fig. 2-1. The entire PLL is a feedback system that consists of five building blocks: Phase Frequency Detector (PFD), Charge-Pump (CP), Loop Filter (LF), Voltage-Controlled Oscillator (VCO), and Frequency Divider (FD). In the PFD, the feedback clock (F_{fb}) from the frequency divider is compared with the reference clock (F_{ref}) in phase and frequency and outputs a signal proportional to the difference between the two inputs. This output signal from PFD is converted into current pulse train by CP. The CP output is filtered through LF (usually a low pass filter) and is converted into continuous-time voltage signal to control VCO. The control voltage

adjusts the VCO frequency and the VCO's output is divided by FD and fed back to the PFD.

If we define the frequency division ratio as N, we can see that when the loop is locked, the two inputs of the PFD are synchronized. The frequency of F_{fb} is forced to be equal to the frequency of F_{ref}, from which we can derive the formula of the PLL output:

$$F_{out} = N \cdot F_{ref} \tag{2.1}$$

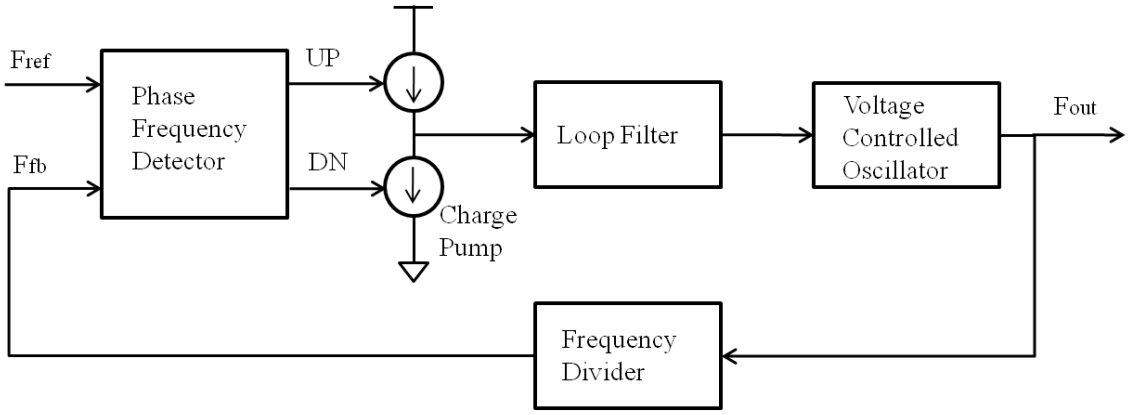


Figure 2-1. Block diagram of PLL

2.2 PLL Building Blocks

2.2.1 Phase Frequency Detector

A phase detector is one of the most vital building blocks in a PLL circuit. It converts the differences between the two phases of two input signals into an output voltage. There are two types of phase detectors: analog multiplier (or mixer) devices and digital sequential devices. In the history of PLL developments, multipliers are a popular choice. When the

PLL has moved to digital territory, digital sequential phase detectors become popular [1]. There are several types of digital phase detectors: EXOR gate, JK-FlipFlop, and Phase-Frequency Detector (PFD). The PFD is the most popular choice because it detects not only the phase difference but also frequency difference. The PFD senses the phase and frequency differences between the reference input and the feedback input, and generates voltage pulses to charge pump for further processing.

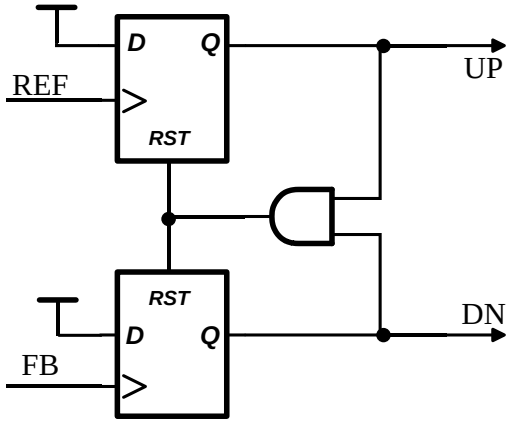
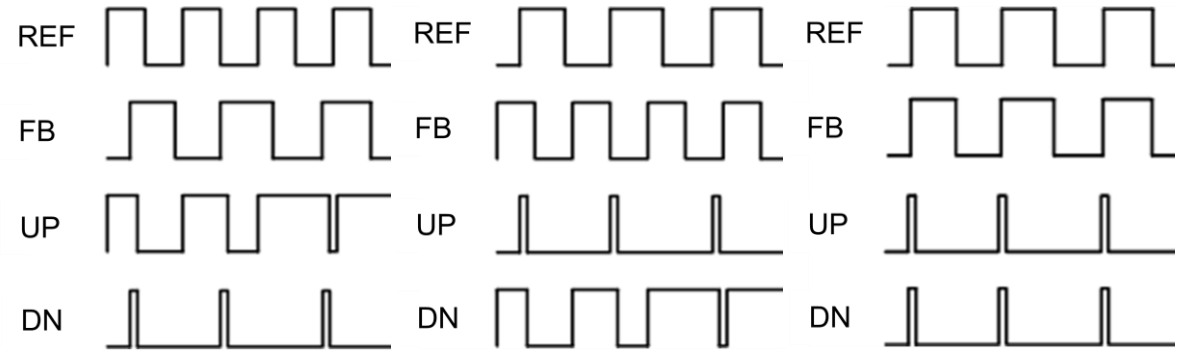


Figure 2-2. Traditional Phase Frequency Detector

The traditional static logic phase frequency detector (Fig. 2-2) consists of two D-Flip-Flops (DFFs) and an AND gate. In this circuit, when the reference input (*REF*) signal leads the feedback input (*FB*), the PFD output *UP* goes high during the period of time corresponding to a phase difference between *REF* and *FB*. At the same time, output *DN* stays low. However, due to the delay of AND gate and the reset time of DFFs, the *DN* output produces a narrow pulse. When *REF* lags that of *FB*, the output *DN* stays high during the interval from the rising edge of *FB* to the rising edge of *REF*. At the same time, a very narrow *UP* will be produced. If *REF* and *FB* have no phase difference, then

both outputs *UP* and *DN* stay low. In reality, both *UP* and *DN* will rise for a very short time. The operation is illustrated as Fig. 2-3 [4].



(a) REF Leads FB (b) REF lags FB (c) REF and FB in-phase

Figure 2-3. Operation of PFD

Since there are two flip-flops in the PFD, there are four possible states. One of the states is invalid, namely the one when both flip-flops are set, since the outputs of both flip-flops immediately reset both flip-flops. As a result, the PFD shown in Fig. 2-2 is sometimes also referred as "Tri-state PFD". Fig. 2-4 shows the state diagram of the PFD.

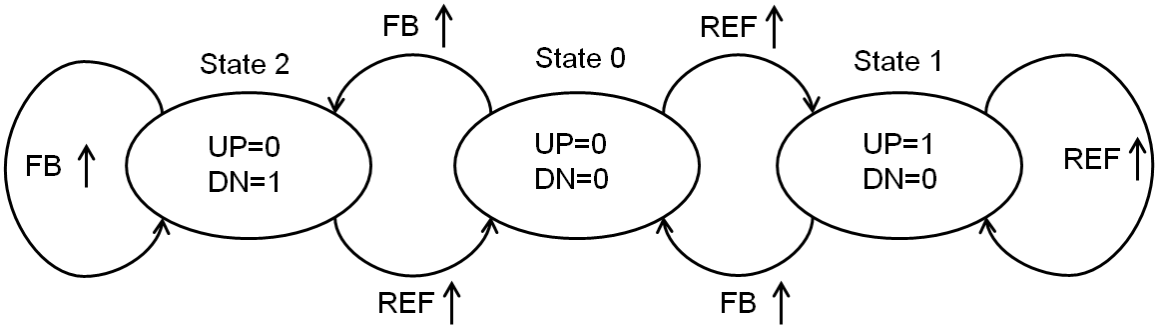
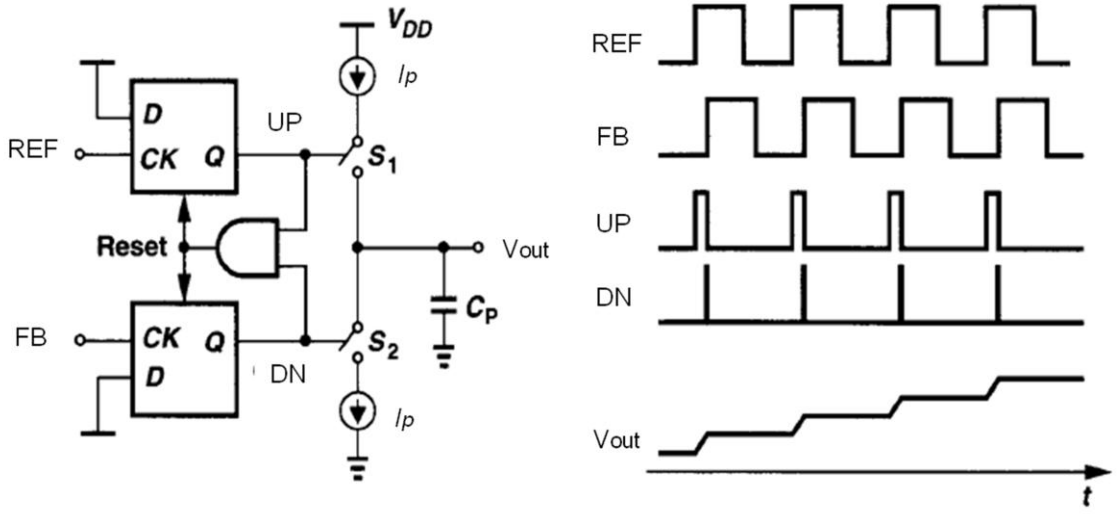


Figure 2-4. PFD state diagram

2.2.2 **Charge Pump**

In modern PLL design, the Charge Pump (CP) is usually paired with PFD due to its wide locking range and low cost. The function of CP is to inject a constant amount of current into the loop filter [3]. A simple charge pump consists of two switched current sources that pump charge into or out of the loop filter according to the PFD outputs. Fig. 2-5 (a) shows a simple charge pump driven by a PFD and driving a capacitor load [5].



(a) (b)

Figure 2-5. Charge pump and operation

The operation of the charge pump is shown in Fig. 2-5 (b). The two switches of the charge pump are controlled by the *UP* and *DN* signals from PFD. When *UP* is high and *DN* is low, the current source of charge pump is active and sources the current I_P into the load. When *UP* is low and *DN* is high, the current sink is active and current I_P sinks into the load. When *UP* and *DN* are either both high or both low, there isn't any net current flow to or from the load. In this way, the output current of the charge pump is

proportional to the pulse width difference of *UP* and *DN* signals, which is the phase difference of the two inputs to PFD. A good charge pump should feature equal charge and discharge currents, minimum switching errors such as charge injection, charge sharing, and clock feedthrough, and minimum output current mismatches.

If we define the phase of the reference signal *REF* as θ_{ref}, and the phase of the feedback signal *FB* as θ_{fb}, then the PFD output is the phase difference θ_e between the *REF* and *FB* signals:

$$\theta_e = \theta_{ref} - \theta_{fb} \tag{2.2}$$

The output current of the charge pump i_d, can be expressed as:

$$i_d = I_P \frac{\theta_e}{2\pi} = I_P \frac{\theta_{ref} - \theta_{fb}}{2\pi} \tag{2.3}$$

2.2.3 **Loop Filter**

The loop filter at the output of the charge pump serves two functions. First, the loop filter integrates the current pulses from charge pump to produce a continuous-time voltage for voltage controlled oscillator (VCO). Second, it compensates the feedback loop, adjusts the PLL dynamics and guarantees the stability of PLL. Therefore, choosing a proper loop filter is critical in PLL design.

There are two types of loop filters, passive and active filters. Passive filters consist of only resistors and capacitors while active filters also contain amplifiers. Very often, the loop filter is implemented as a passive structure. Although active loop filters may be used to reduce the PLL area, they are typically not employed due to their inferior noise performance [3].

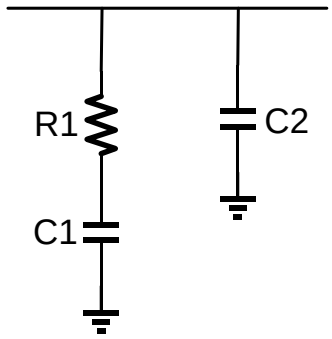


Figure 2-6. Typical loop filter for charge-pump PLL

A possible 2nd order passive loop filter is shown in Fig. 2-6. This low-pass filter serves as a device to filter out high frequency harmonics and to provide a continuous-time signal output, which becomes the tuning voltage for the VCO. The main capacitor C1 is used to integrate the charge pump current. The resistor R1 is required for stability since it produces a zero in the 2nd order continuous-time linear closed loop model for the PLL, as will be discussed in Section 2.3. A secondary capacitor C2 is used to filter out the ripples produced by periodic injection of charge by the charge pump [3].

2.2.4 **Voltage Controlled Oscillator**

The voltage controlled oscillator (VCO) is responsible for generating the desired output frequency. The VCO is perhaps the most critical part in the entire PLL design since it dominates the phase noise contribution and power consumption.

Figure 2-7. VCO model

The VCO (Fig. 2-7) receives the control voltage V_{ctrl} from the charge pump and generates a clock f_{vco} with its frequency tuned by the magnitude of the V_{ctrl}. The tuning characteristics of the VCO should be as linear as possible (Fig. 2-8). The slope of output frequency versus control voltage is the VCO gain K_{vco}.

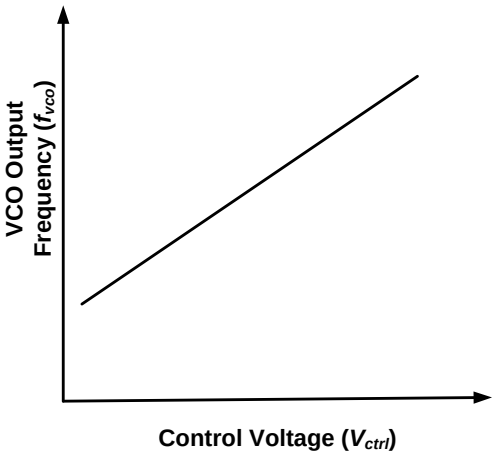


Figure 2-8. VCO tuning characteristics

Several parameters of a VCO operating in the PLL must be taken into consideration: tuning range, tuning linearity, phase noise and jitter, power supply and substrate noise rejection.

The tuning range is the range between the lowest and the highest operating frequency of VCO. The tuning range must accommodate the PLL requirements as well as process and temperature variations in the VCO frequency range. The tuning linearity is the variation of K_{vco} over the tuning range. A high performance VCO should have a high tuning linearity, which decreases the locking time and ensures the loop stability. Phase noise and jitter performance is determined by timing accuracy and spectral purity of the VCO output signal. If the VCO is integrated on the same substrate as digital circuits, it should be highly immune to the power supply and substrate noise. Such effects become more prominent if a PLL shares the same substrate and package with large digital circuits.

The VCO topologies that have been commonly used for PLL design: LC-tank oscillators and ring oscillators. The LC-tank oscillator utilizes monolithic inductors and capacitors to build passive resonant circuits (Fig. 2-9). The VCO's frequency can be controlled by tuning the capacitance using varactor diodes. The LC-VCO features high frequency output and low phase noise. However, it has drawbacks such as limited tuning range, high power consumption, and large area.

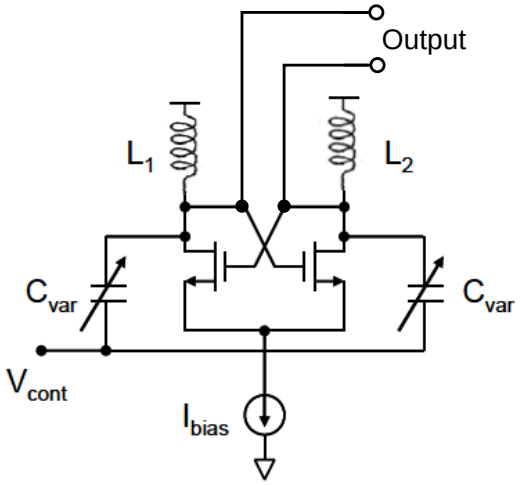


Figure 2-9. Typical structure of LC-VCO

The other common type of VCO is the ring oscillator VCO which consists of a number of delay cells. In comparison to LC-VCO, the ring oscillator VCO has a wide tuning range, low power consumption and is more suitable for integration in CMOS processes due to its small area. Commonly used solutions are single ended ring oscillators and differential ring oscillators.

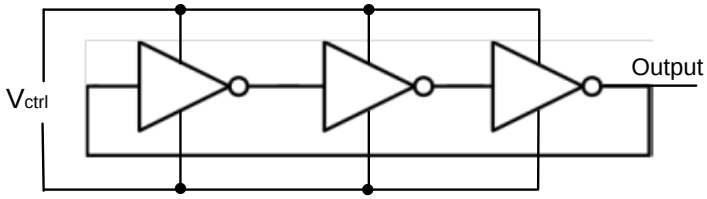


Figure 2-10. 3-stage single-ended ring oscillator

A simple single-ended ring oscillator consisting of three inverters is shown in Fig. 2-10. There should be odd number of stages in single-ended oscillator to ensure oscillation. Current is consumed in inverters during transition while their output capacitances are being charged and discharged. In inverters with current source or current sink, the

amount of current is determined by tail current source or current sinks. Changing the amount of current varies the charge/discharge duration of the output capacitance, thus controlling the transition time of delay cells. The current which flows through the tail current source or sink is controlled by the VCO control voltage. Therefore VCO control voltage controls the current flow and the frequency of oscillation [4].

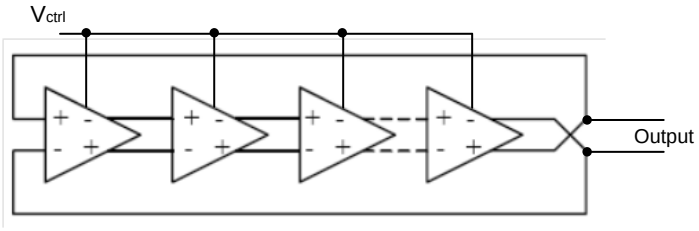


Figure 2-11. 4-stage differential ring oscillator

A differential ring oscillator (Fig. 2-11) is composed of differential delay cells. The delay of each stage is determined by the time constant of its output node. Differential ring oscillators may have either odd or even number of delay stages. Compared to single-ended ring oscillator, differential ring oscillator has better common-mode noise rejection properties, such as power supply noise and substrate noise [4].

2.2.5 **Frequency Divider**

The function of the frequency divider is to divide the output frequency to achieve frequency multiplication in PLL. The frequency divider is a digital building block consisting of gates and flip-flops.

There are various types of frequency dividers, which can be classified according to their function, and logic structures. Based on the functionality, they can be classified as fixed ratio dividers and programmable dividers. Fixed ratio divider is used to generate output frequency with fixed reference frequency. If a programmable divider is used, the reference frequency can vary depending on allowable division ratios to generate desired output frequency [4]. Based on the logic structures, the frequency dividers can be classified as synchronous and asynchronous types. The speed of synchronous frequency dividers is higher than asynchronous ones but sacrifice the amount of circuitry and power. The asynchronous dividers are commonly used for low power and relatively low frequency operation.

When the divider input frequency is too high for proper operation of a regular programmable divider (counter), a prescaler can be employed to lower the input frequency. A prescaler is a high speed divider which prescales (divides) the input frequency to a lower frequency and feed it into a programmable divider. There are two types of prescaler dividers, fixed prescaler dividers and dual modulus prescaler dividers. As shown in Fig. 2-12, if the fixed prescaler frequency division ratio is P and the programmable counter frequency division ratio is N, then the total frequency division ratio is P·N.

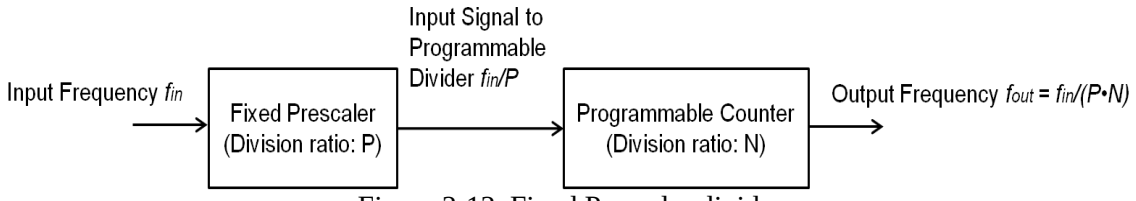


Figure 2-12. Fixed Prescaler divider

2.3 Linear Analysis of PLL as Feedback Loop

The transient response of a PLL is basically a non-linear process. However, one can develop a linear approximation of the PLL to understand its behavior. This section analyzes the transfer function of the PLL, which is critical in order to analyze the phase noise, lock time and the overall PLL design.

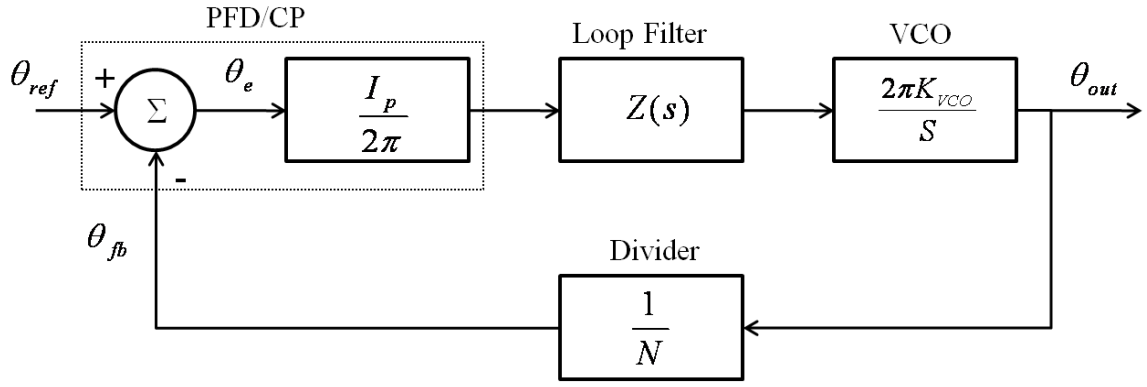


Figure 2-13. PLL loop diagram

In order to proceed with the linear approximation, each building block of the PLL has been replaced with its linear model (Fig. 2-13). From Section 2.2.2, we know that the transfer function of the PFD-CP is

$$i_d = I_P \frac{\theta_e}{2\pi} = \frac{I_P}{2\pi}(\theta_{ref} - \theta_{fb}) \tag{2.4}$$

where $\frac{I_P}{2\pi}$ is the gain of the PFD-CP.

For VCO, the angular frequency is given by [6]

$$\omega_{VCO}(t) = \omega_0 + \Delta\omega_{VCO}(t) = \omega_0 + K_0 v_{VCO}(t) \tag{2.5}$$

where K_0 is the VCO gain (rad/s·V). The phase of VCO can be derived by integrating its angular frequency

$$\theta_{VCO}(t) = \int \Delta\omega_{VCO}(t)dt = K_0 \int v_{VCO}(t)dt \tag{2.6}$$

Applying the Laplace transformation to the above equation, one obtains the VCO transfer function in S-domain

$$\theta_{VCO}(s) = \frac{K_0}{s} V(s) \tag{2.7}$$

One can modify the above equation as

$$\theta_{VCO}(s) = 2\pi \frac{K_{VCO}}{s} V(s) \tag{2.8}$$

Hence the updated VCO gain is now K_{VCO} expressed in units of Hz/V.

The term 2π in PFD-CP and VCO transfer functions cancel each other. Therefore, the updated PLL loop diagram will look like the one shown in Fig. 2-14. The gain of the PFD-CP (I_P in Fig. 2-13) has been defined as K_ϕ (unit: A).

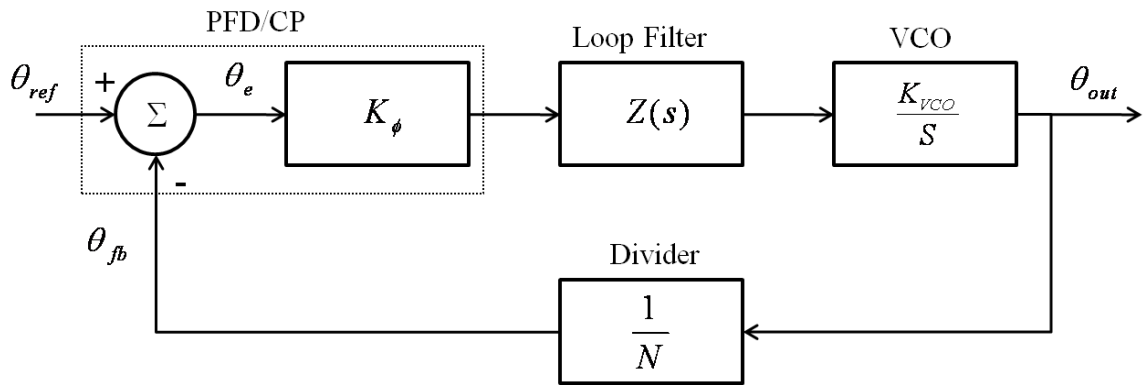


Figure 2-14. Updated PLL loop diagram

One can analyze the feedback loop transfer function as a combination of the individual building block transfer functions, expressing the most important PLL transfer functions as below,

$$\text{Forward-loop transfer function:} \quad G(s) = \frac{\theta_{out}}{\theta_e} = \frac{K_\phi Z(s) K_{vco}}{s} \tag{2.9}$$

$$\text{Reverse-loop transfer function:} \quad H(s) = \frac{\theta_{div}}{\theta_{out}} = \frac{1}{N} \tag{2.10}$$

$$\text{Open-loop transfer function:} \quad H(s)G(s) = \frac{\theta_{div}}{\theta_e} = \frac{K_\phi Z(s) K_{vco}}{Ns} \tag{2.11}$$

$$\text{Closed-loop transfer function:} \quad CL(s) = \frac{\theta_{out}}{\theta_{ref}} = \frac{G(s)}{1 + H(s)G(s)} \tag{2.12}$$

Out of those, the open-loop transfer function $H(s)G(s)$ is the most often used to determine the loop filter parameters to ensure the loop stability.

There are two important terms which contain the characteristic information of the loop, namely order and type. The order of a PLL is determined by the highest order of the polynomial (power of "s") in the denominator of closed-loop transfer function. Loop type is determined by the number of integrators within the loop, each integrator contributes to a pole. Open-loop transfer function is used to determine loop type. Because of the inherent integration in the VCO, a PLL is always at least type-I [4] [6].

For the 2nd order passive loop filter shown in Fig. 2-6, the transfer function is

$$Z(s) = (R_1 + \frac{1}{sC_1}) \| \frac{1}{sC_2} = \frac{1 + s(R_1 \cdot C_1)}{s^2(R_1 \cdot C_1 \cdot C_2) + sC_1 + sC_2} \tag{2.13}$$

A charge pump based PLL with the 2nd order passive loop filter is usually a type-II 3rd order loop. The Bode plot of the open-loop transfer function of the type-II 3rd order PLL is shown in Fig. 2-15.

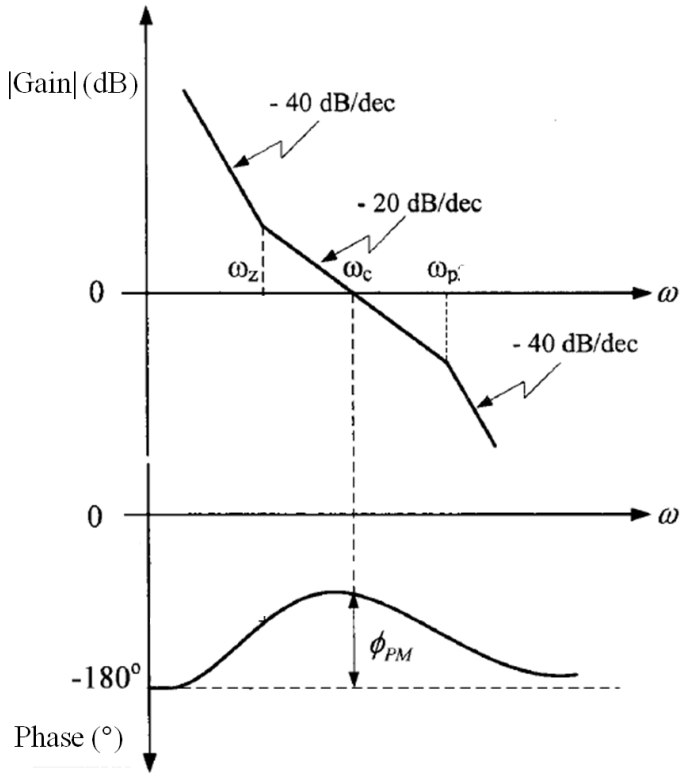


Figure 2-15. Typical type-II 3rd order PLL open-loop transfer function Bode plot

The frequency ω_c at which the open-loop gain drops to unity is called the gain cross-over frequency. The phase margin ϕ_{pm} is defined as the difference between 180 degrees and the open loop phase value at the cross-over frequency. The phase margin is usually chosen between 50 and 70 degrees [7]. Further discussion of this topic will follow (Section 3.4).

2.4 Behavioral Modeling of PLL

Behavioral modeling of the PLL verifies the loop stability and dynamics. It is an important step before the transistor level circuit design. Based on the previous discussions of the PLL system, the behavioral model of the Type-II 3rd order PLL (Fig. 2-1) has been developed in Matlab. The model is built based on the PLL design parameters and the loop filter component values that are derived in Section 3.4. The Matlab code is attached in the Appendix B.

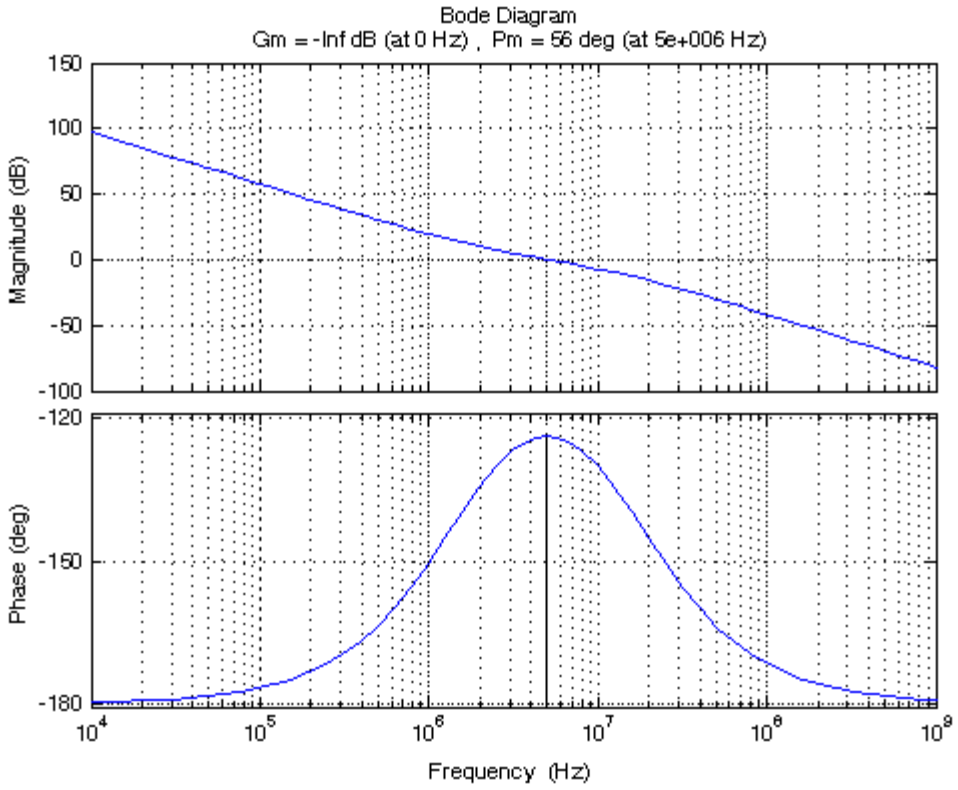


Figure 2-16. Bode plot of the open-loop transfer function of the Type-II 3rd order PLL

The simulation of the behavioral PLL model resulted in the open-loop transfer function Bode plot (Fig. 2-16). The phase margin of 56° satisfies the condition for loop stability at the crossover frequency 5MHz.

The behavioral model has been also used to investigate the closed-loop step response of the PLL (Fig. 2-17). It illustrates the time behavior of the output of the PLL with a unity step function applied to the input. This simulation could approximate the settling time of the PLL system. From the figure, one can observe that the PLL's settling time is around 400ns.

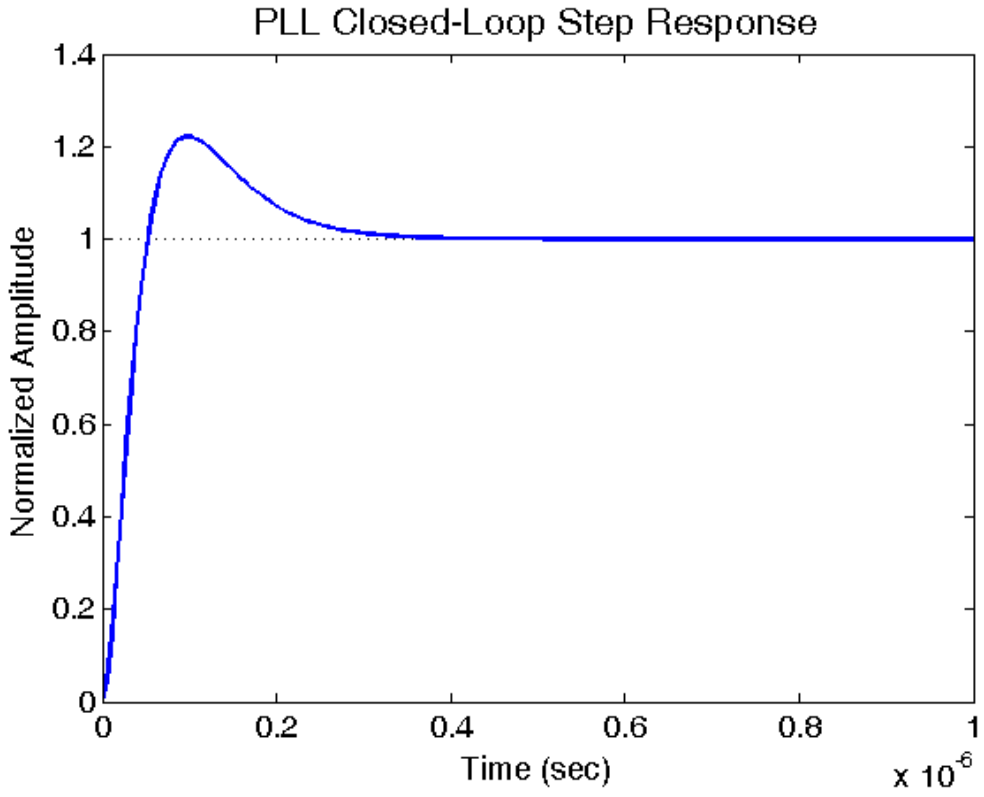


Figure 2-17. Closed-loop step response of the PLL for settling time approximation

2.5 Phase Noise and Jitter

The quality of the PLL output signal is heavily dependent on the phase noise and time jitter performance. In this section, we introduce the phase noise and time jitter. The noise property of individual building blocks in PLL system is studied next. Finally, the noise in PLL system is analyzed and the design tradeoff between noise and loop bandwidth is discussed.

2.5.1 Phase Noise

An ideal clock source would generate a clean sine or square wave. All signal power should be generated at the desired clock frequency. However, in actuality, all clock signals have some degree of phase noise. This noise spreads the power of the clock signal to adjacent frequencies, resulting in noise sidebands. Phase noise is the frequency domain representation of the clock noise. The phase noise is typically expressed in dBc/Hz and represents the amount of signal power at a given sideband or offset frequency from the ideal carrier frequency [8].

The output of the PLL can be expressed as

$$V_{out}(t) = V_0 \sin(\omega_0 t + \phi(t)) \tag{2.14}$$

where $\omega_0 t$ is the desired phase of the output signal and $\phi(t)$ is the phase perturbation of the output signal.

We can assume the phase perturbation $\phi(t)$ has a sinusoidal form

$$\phi(t) = \phi_p \sin(\Delta\omega t) \tag{2.15}$$

where $\Delta\omega$ is the offset frequency from the carrier, and ϕ_p is the peak phase fluctuation.

Substituting the Eqn. (2.21) into Eqn. (2.20), we get

$$V_{out}(t) = V_0 \left\{ \cos(\omega_0 t) - \frac{\phi_p}{2} \left[\cos\left(\omega_0 + \Delta\omega\right)t - \cos\left(\omega_0 + \Delta\omega\right)t \right] \right\} \tag{2.16}$$

In the above equation, the carrier signal tone is at ω_0 and two symmetric sidebands with amplitude of $20\log(\phi_p / 2)$ are at arbitrary offset frequency $\pm\Delta\omega$. The Single-sideband (SSB) phase noise is defined as the ratio of power in one sideband per one Hertz of bandwidth at an offset $\Delta\omega$ away from the carrier to the total carrier signal power. The SSB phase noise power spectral density to carrier ratio, in units [dBc/Hz], is defined as

$$L_{SSB}\left(\Delta\omega\right) = 10\log\left[\frac{P_{SSB}\left(\omega_0 + \Delta\omega, 1Hz\right)}{P_{carrier}(\omega_0)} \right] \tag{2.17}$$

The spectrum of phase noise profile for a typical signal is shown in Fig. 2-18 [2]. To evaluate the phase noise performance, both the noise density and the offset frequency need to be specified, e.g., -100dBc/Hz at 1MHz offset from the carrier frequency.

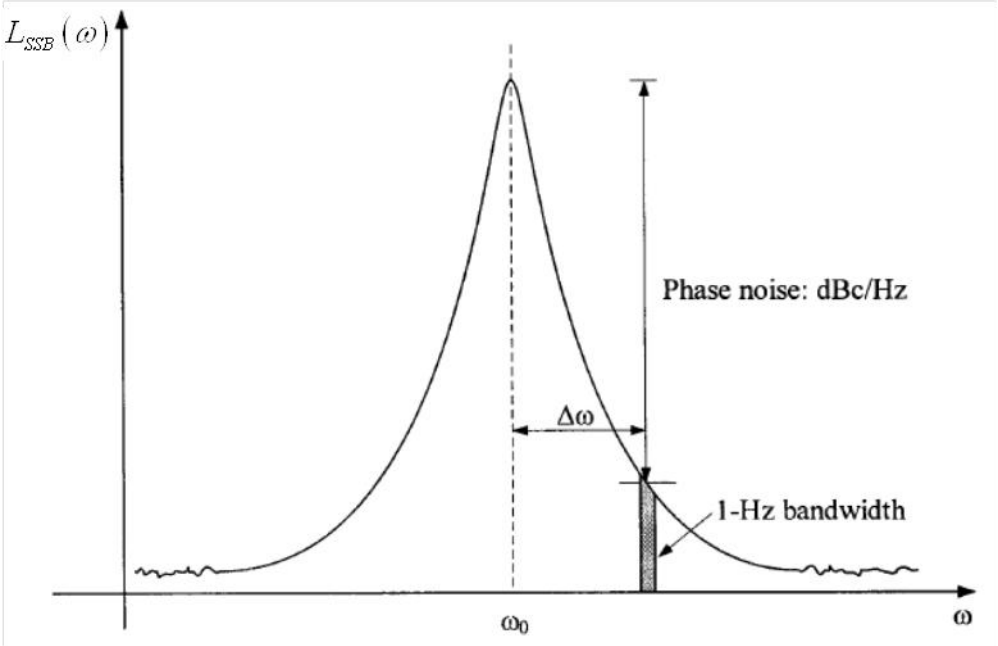


Figure 2-18. Phase noise spectrum of a typical clock signal

2.5.2 **Time Jitter**

Time jitter can be described as the random variation in the actual clock signal's edges in reference to its ideal waveform. Hence jitter is the time domain instability of the clock signal, usually expressed in picoseconds (ps). Based on the measurement method, there are three types of jitter: edge-to-edge jitter, k-cycle jitter and cycle-to-cycle jitter.

Edge-to-edge jitter (J_{ee}) is the variation between ideal clock edge and the actual clock edge, which is sometimes referred as absolute jitter. k-cycle jitter (J_k) is the measurement of clock edge uncertainty in k cycles, which is also referred as long-term jitter. Cycle-to-cycle jitter (J_{cc}) measures the difference of a clock period between adjacent cycles. The three definitions of jitter are illustrated in Fig. 2-19 [9].

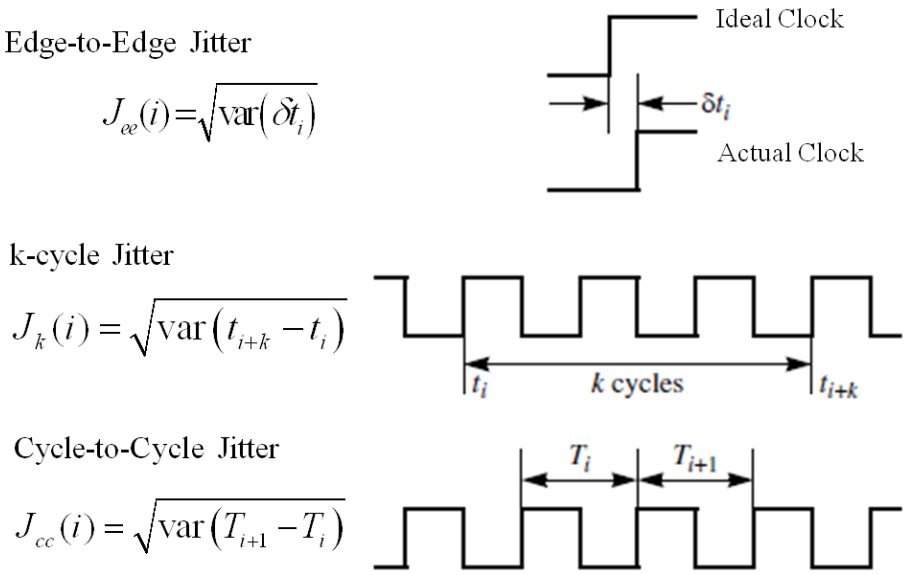


Figure 2-19. Definitions of jitter

2.5.3 **Phase Noise Properties of VCO**

VCO contributes the most noise inside the PLL loop. A typical free running VCO (i.e. control voltage is 0) has a phase power spectrum shown in Fig. 2-20 [2]. There are three regions in the sideband that can be recognized (slightly exaggerated). The flat region ($1/f^0$) at large offset frequency is the noise floor. The $1/f^2$ region is referred to as the "white frequency" variation region, since it is due to white, or uncorrelated, fluctuations in the period of the oscillator. The behavior in this region is dominated by the thermal noise in the devices of the oscillator circuit. At sufficiently low offset frequencies the flicker noise of devices usually comes into play and the spectrum in this region falls as $1/f^3$ [2].

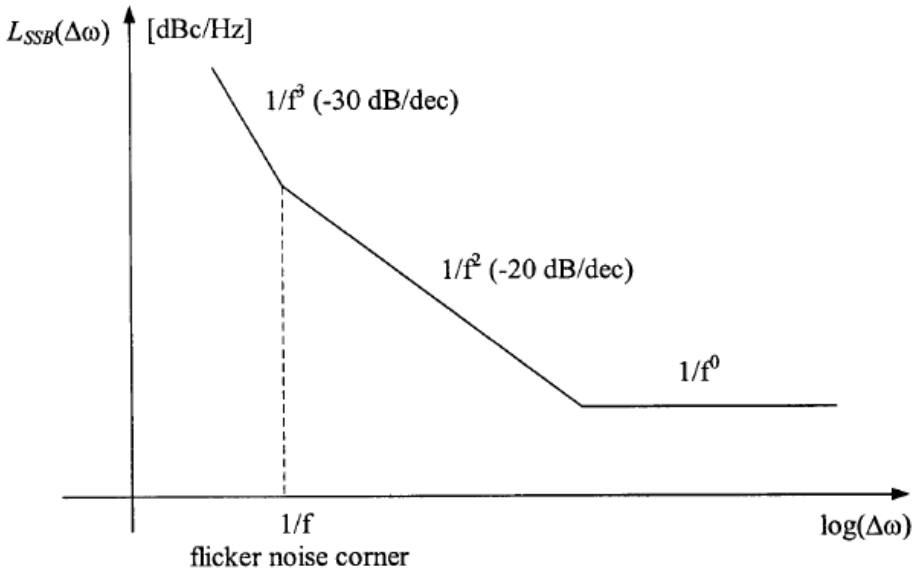


Figure 2-20. Phase power spectrum of free running VCO

2.5.4 **Noise Properties in PLL**

The noise coming from individual components contribute to the overall PLL system noise. A loop diagram of PLL with noise sources is shown in Fig. 2-21.

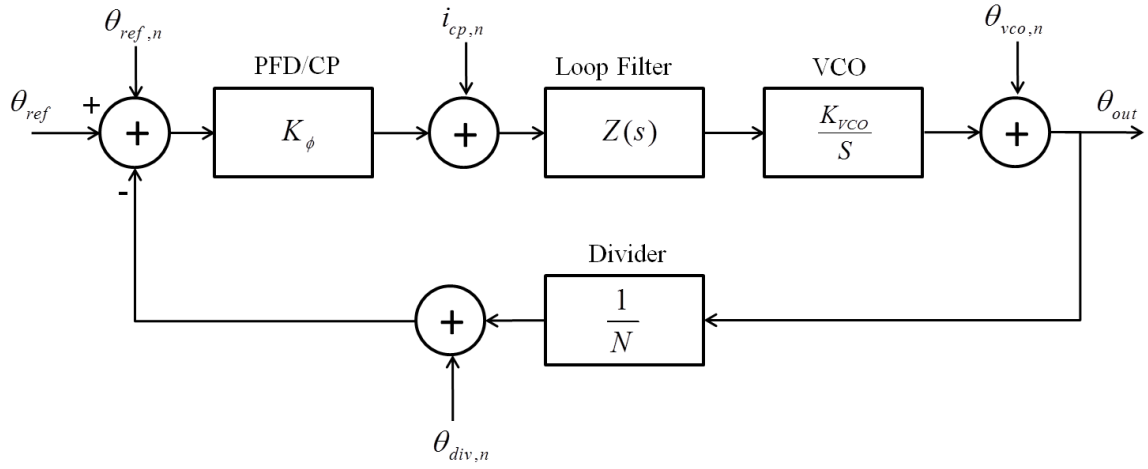


Figure 2-21. PLL loop diagram with noise sources

Based on the loop transfer functions derived from Section 2.3, one can obtain the following noise transfer functions from each individual components.

The noise transfer function of VCO is

$$H_{vco} = \frac{\theta_{out}}{\theta_{vco,n}} = \frac{1}{1+G(s)H(s)} \tag{2.18}$$

The noise transfer function of PFD and CP is

$$H_{pfd\_cp} = \frac{\theta_{out}}{i_{cp,n}} = \frac{Z(s)}{1+G(s)H(s)} \frac{K_{vco}}{s} \tag{2.19}$$

The noise transfer function of frequency divider is

$$H_{div} = \frac{\theta_{out}}{\theta_{div,n}} = -\frac{G(s)}{1+G(s)H(s)} \tag{2.20}$$

The noise transfer function of input reference signal is

$$H_{ref} = \frac{\theta_{out}}{\theta_{ref,n}} = \frac{G(s)}{1+G(s)H(s)} \tag{2.21}$$

The Bode plot of PLL noise transfer functions of individual components calculated using Matlab are shown in Fig. 2-22. The noise transfer function model is built based on the PLL design parameters and the loop filter components value that are derived in Section 3.4. The Matlab code is attached in Appendix C.

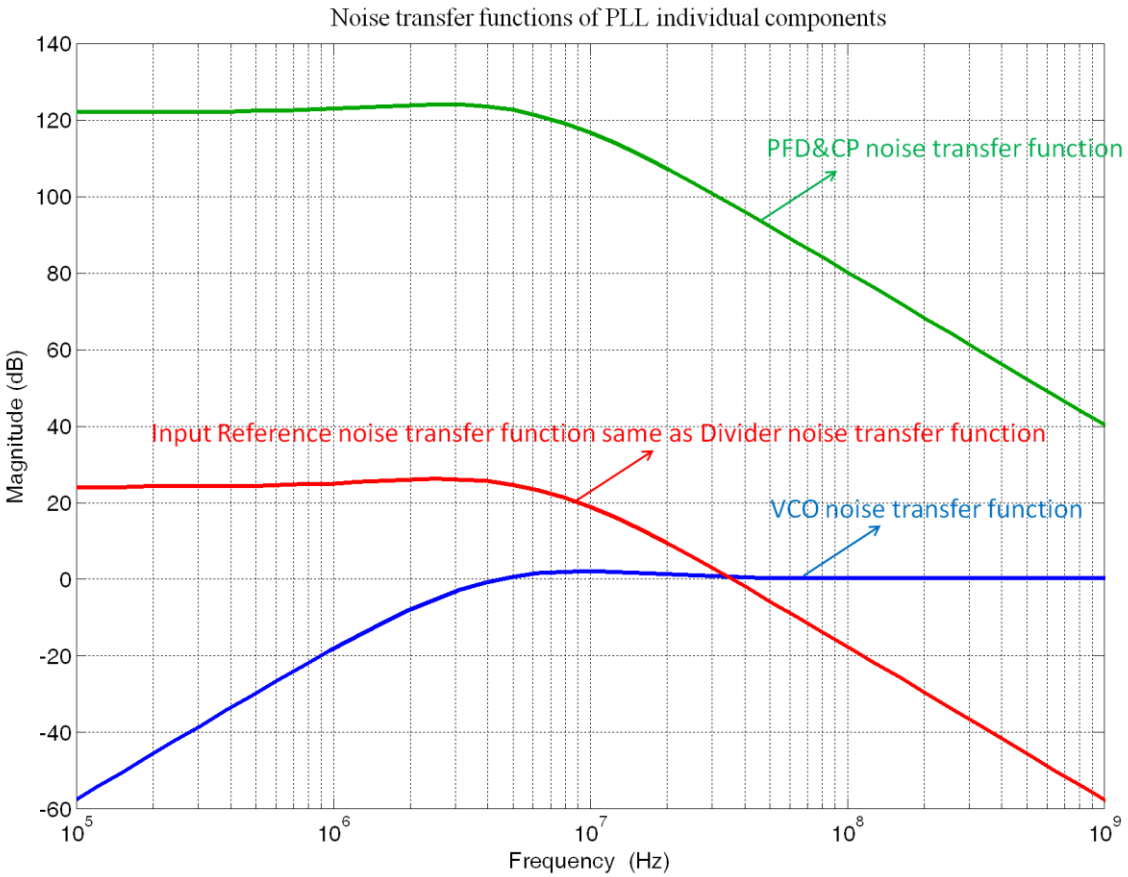


Figure 2-22. Noise transfer functions Bode plot of PLL individual components

It can be seen from the Fig. 2-22 that the input reference signal noise and feedback divider noise exhibits identical low-pass response, while VCO noise exhibits high-pass response. Therefore, a design trade-off exists when choosing the loop bandwidth f_{bw}. Reducing the loop filter bandwidth increases the amount of noise attenuation on the reference clock. If the reference clock has a significant amount of noise, using a low PLL bandwidth to filter this noise is preferred. However, the contribution of VCO noise to a PLL's output noise increases as the loop bandwidth decreases. Unless the PLL has a very low noise VCO, the impact of using a low PLL bandwidth can have the detrimental effect

of actually increasing the output clock noise [8]. For this research, the reference clock is assumed to be a clean signal. This assumption allows the reference noise to be ignored. The goal is to achieve a low PLL internal noise. As a result, the loop bandwidth is chosen to be a relatively high value. The input reference clock frequency is 50MHz and typical loop bandwidth $f_{bw} \leq f_{ref} / 10$. Therefore, the loop bandwidth is chosen as 5MHz.

3 CIRCUIT DESIGN OF LOW-POWER LOW-NOISE PLL

3.1 Introduction

This chapter describes the detailed design and implementation of individual building blocks of the low-power low-noise PLL. In order to improve the PLL performance, several novel architectural solutions has been proposed to the PLL sub-blocks. Section 3.2 describes the design of PFD. To reduce the effect of blind-zone and extend the detection range of PFD, we proposed the Dynamic-logic PFD with delayed input pulse/edge. We also proposed an improved design of the Charge Pump in Section 3.3. The proposed Charge Pump utilizes NMOS-Switch only to reduce the switching mismatches, and a high-swing cascode current mirror output stage was used to increase the output resistance for better current matching. The design of loop filter is discussed in Section 3.4. VCO consumes the most power and dominates the noise in the PLL. An 800MHz ring type VCO design is described in Section 3.5. Finally, Section 3.6 presents the design of frequency divider. To save power and area, the True Single Phase Clock (TSPC) logic has been used for the divider. Each section provides the simulation results for the individual building blocks. The designs are implemented using IBM 0.13um CMOS technology.

3.2 Phase Frequency Detector

Conventional PFDs may suffer from such drawbacks as dead-zone and blind-zone. A dead-zone problem occurs when two input clocks are very close to each other and the small phase difference can't be detected by the PFD. A blind-zone problem occurs when the phase difference of two input clocks approaches $\pm 2\pi$, and it usually results in missing clock edges and output polarity reversal. The blind-zone is a major factor that limits the detection range of PFDs and may deteriorate the PLL locking characteristics.

A conventional tri-state PFD (Fig. 3-1) offers a relatively good phase and frequency detection. With a proper modification, it also eliminates the dead-zone. However, the static logic that is used in the conventional design limits the operating speed and requires more transistors. In this research, the architecture of PFD utilizing dynamic logic has been implemented [10].

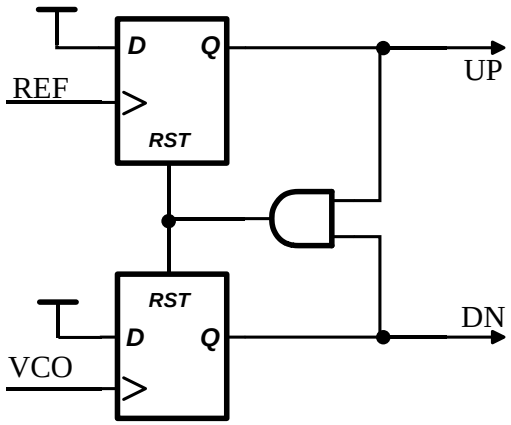


Figure 3-1. Conventional tri-state FPD

One of the PFD architectures that virtually eliminates dead-zone is a design based on dynamic CMOS logic, in which the PFD's output signals are directly used to reset the PFD without any intermediate logic [11]. This design has been further modified by Li and Ismail [12] to eliminate the probability of short-circuit current (Fig. 3-2). The

reported Dynamic-Logic Phase Frequency Detector features near zero phase error. However, its performance is still vulnerable to blind-zone effect and requires further improvement.

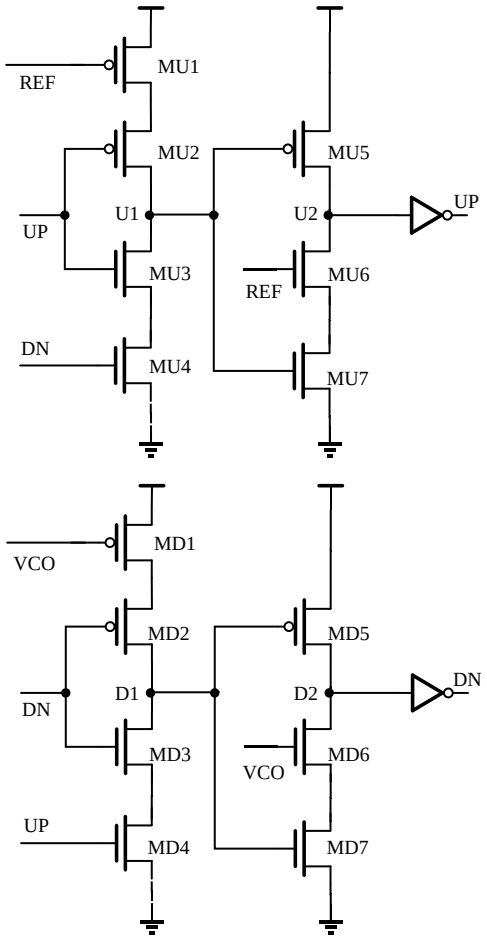


Figure 3-2. Circuit diagram of Dynamic-Logic PFD [2]

3.2.1 **Blind-Zone Analysis**

The PFD shown in Fig. 3-2 is insensitive to any transition of the input signal during the reset phase (*UP* & *DN* being both high). The time range of this edge insensitivity during the reset phase is defined as the blind-zone. This problem usually happens when the input phase difference approaches $\pm 2\pi$. The detector may encounter a polarity reversal problem

in the blind-zone that can be better explained using the timing waveform shown in Fig. 3-3. A rising edge of *REF* clock takes place during the reset phase (T_{RST}), but this transition can't be detected by the PFD. Consequently, the leading *REF* signal is incorrectly indicated by the PFD as lagged (*DN* is wider than *UP*) in the subsequent cycle [12]. The ideal linear phase detection range of the Dynamic-Logic PFD should cover [-2π, +2π] range (Fig. 3-4 (a)). However, in reality, the full detection range can't be achieved due to the blind-zone problem as shown in Fig. 3-4(b).

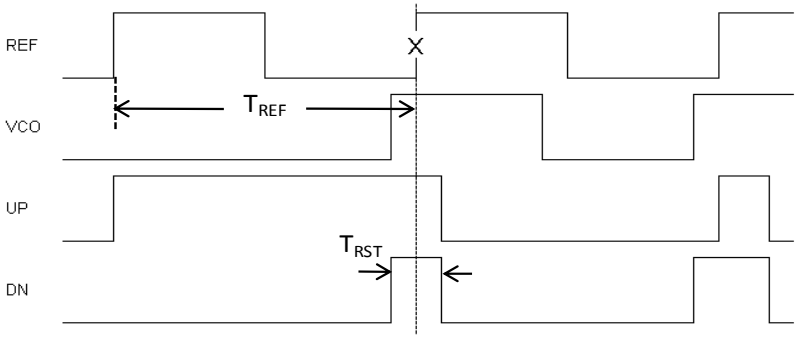


Figure 3-3. Blind-zone timing waveform

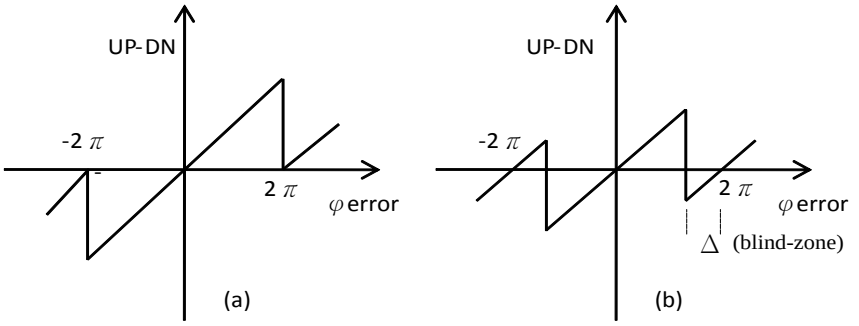


Figure 3-4. Phase-frequency characteristics of an ideal (a) and real (b) PFD

If the *REF* signal is leading the *VCO* signal, and assuming the reset phase width and period of the *REF* signal are denoted as T_{RST} and T_{REF}, then a polarity reversal happens when input phase difference φ_{error} is in between $2\pi-\Delta$ and 2π, where $\Delta=2\pi\times(T_{RST}/T_{REF})$.

The blind-zone value is equal to T_{RST} in time domain and Δ in phase domain. In general, the blind-zone of a PFD limits the PFD detection range.

3.2.2 **Proposed Dynamic-Logic PFD for Extended Detection Range [10]**

3.2.2.1 Delayed-Input-Pulse Dynamic PFD

The proposed modification of the Dynamic-Logic PFD is shown in Fig. 3-5. The goal of this design is to create delayed versions of input signals, *REF1* and *VCO1*, with a delay larger than that of the blind-zone; therefore, it is termed as the Delayed-Input-Pulse Dynamic PFD (DIP-PFD). The *REF* and *VCO* signals are buffered at the input by a predetermined delay τ that is larger than the blind-zone ($\tau > T_{RST}$). When the PFD is operating in the blind-zone, a delayed version of the input signal is activated so that its rising edge comes after the reset phase and allows the PFD to properly detect the rising pulse edge. The operation in linear range ($\varphi_{error} \in [0, 2\pi\text{-}\Delta]$) is described below. Initially, both *REF* and *VCO* are low. The nodes *U1* and *D1* are precharged high. When the *REF* signal is leading the *VCO* signal, *U2* is pulled low on the rising edge of the *REF* signal and the circuit generates *UP* pulse. When the *VCO* signal arrives, *D2* is pulled low on the rising edge of *VCO* signal and the circuit generates a *DN* pulse. The *UP* and *DN* pulses initiate a reset operation that deactivate the outputs, hence the width difference between *UP* and *DN* pulses is equal to the phase difference of two input signals.

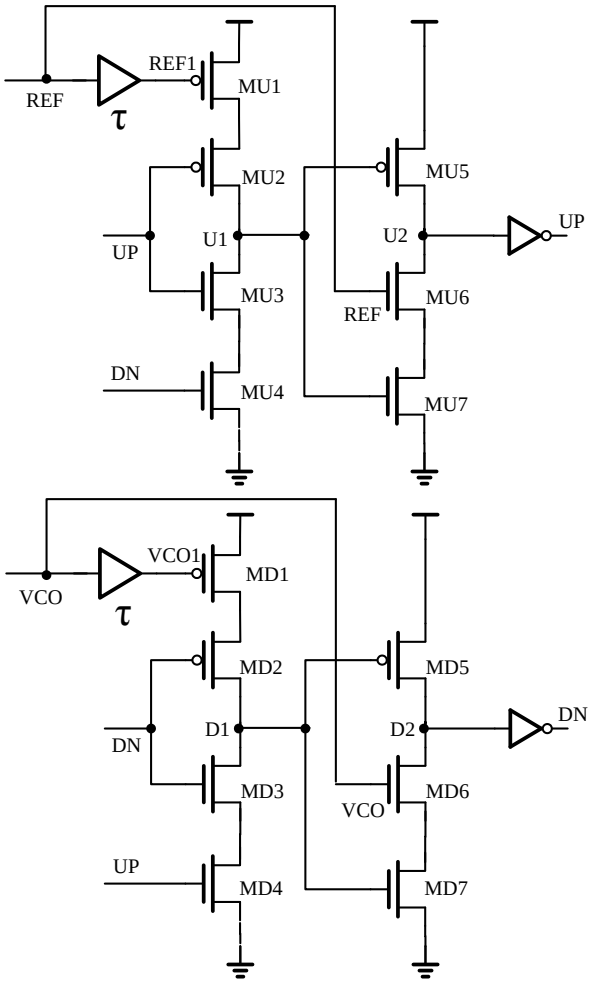


Figure 3-5. Circuit diagram of the DIP-PFD

A typical example of a timing waveform for the operation in the blind-zone ($\varphi_{error} \in [2\pi-\Delta, 2\pi]$) is shown in Fig. 3-6. The *UP* pulse is generated if the input *REF* signal is leading the *VCO* signal. This *UP* pulse turns off MU2 to block any changes through MU1. Then the *DN* pulse is generated on the *VCO* rising edge. Reset operation is initiated and at the end the *UP* and *DN* signals are pulled low. If the *REF* rising edge comes during the reset phase, it will be delayed by τ to produce *REF1*. Since the delay is larger than the reset phase width ($\tau > T_{RST}$), *REF1* rising edge comes after the reset phase, and it can be

detected by PFD. Hence, the DIP-PFD eliminates the possibility for polarity reversal at its outputs.

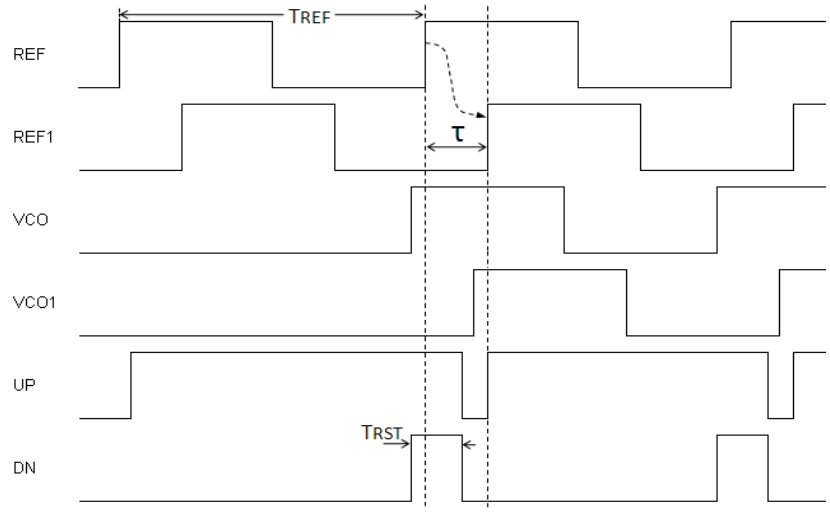


Figure 3-6. Timing waveform of DIP-PFD operating in the blind-zone

3.2.2.2 Delayed-Input-Edge Dynamic PFD

Another possible approach is to delay the input rising edge instead of delaying the entire input pulse. It is termed as the Delayed-Input-Edge Dynamic PFD (DIE-PFD). The concept of this design comes from K. Park and I. Park [13] who used it to solve missing edge problem in a conventional PFD. Their approach has been modified here to fit the architecture of Dynamic-Logic PFD. The circuit diagram is shown in Fig. 3-7. The basic idea is to use NMOS pass transistor at the input to delay the rising edge of input signal during the reset phase. The pass transistors (MU0 & MD0) are controlled by their controlling signals (*CTRL1* & *CTRL2*) and should be OFF only during the reset phase. When the reset phase is not initiated, the pass transistor is ON, and it allows the *REF* and *VCO* signals to pass. During the reset phase, any input transition is blocked and the previous value is maintained at the PFD input. Therefore, if an input rising edge comes

during the reset phase, it will be temporarily blocked and then propagated through pass transistor after the reset phase. Ideally, the controlling signals *CTRL1* and *CTRL2* should be composed of *UP* & *DN* signals as shown in the dashed box. However, due to the delay of the NAND gate, the rising edge may not be properly blocked. By designing the controlling signals as illustrated in Fig. 3-7, the pass transistors will be turned off earlier (by the amount of $\Delta t = T_{RST} - T_{NAND}$) than the actual reset phase.

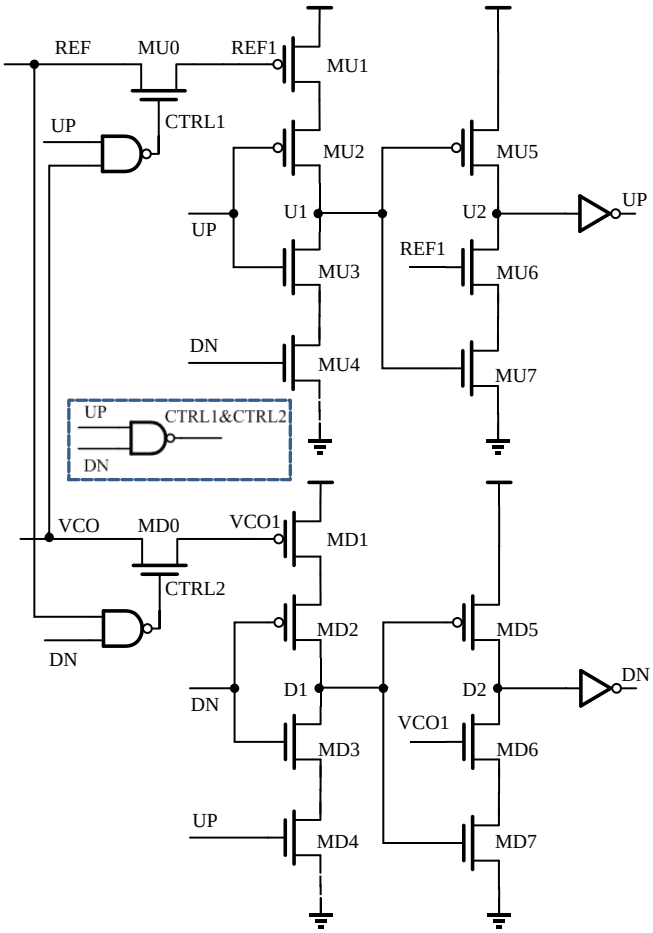


Figure 3-7 Circuit diagram of the DIE-PFD

A timing waveform in Fig. 3-8 shows the DIE-PFD operating in the blind-zone. When the *REF* signal is leading the *VCO* signal with phase difference between 2π-Δ to 2π, the

rising transition of *REF* occurs during the reset phase. Because *UP* and *VCO* are both high at that time, *CTRL1* signal is low and the pass transistor MU0 is OFF. The rising edge of *REF* is blocked by the MU0 until the reset phase is finished. Then the *REF* rising edge is propagated through MU0 and allows the PFD to correctly detect the *REF* edge. Therefore, the DIE-PFD also eliminates the blind-zone problem, extending the detection range.

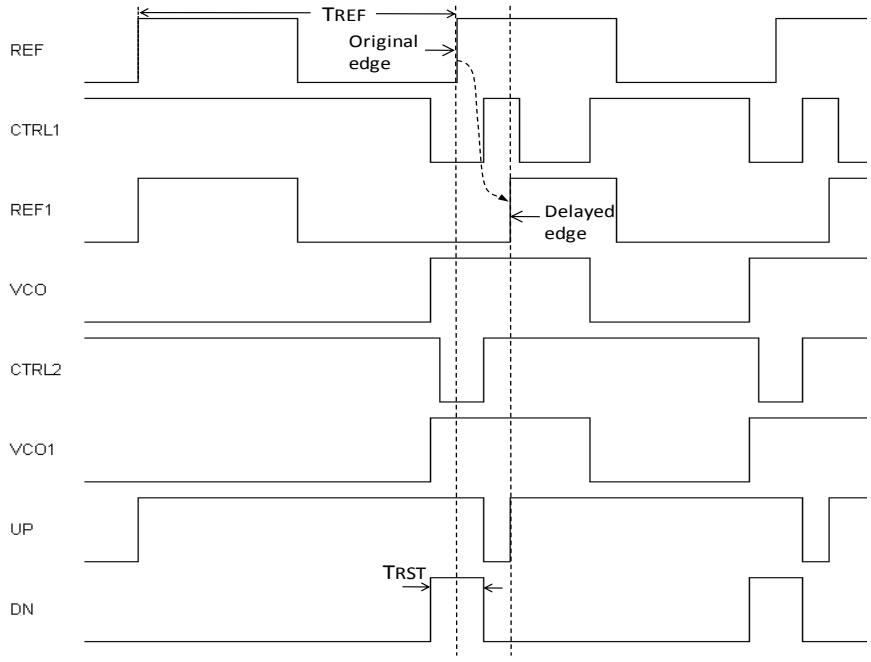


Figure 3-8. Timing waveform of DIE-PFD operating in the blind-zone

3.2.3 **Simulation and Comparison of Phase Frequency Detectors**

To demonstrate the improvement in the phase detection range, the original Dynamic-Logic PFD [12], DIP-PFD and DIE-PFD (Fig. 3-2, 3-5 and 3-7) have been designed using the IBM 0.13µm CMOS technology.

Fig. 3-9 shows the phase characteristics of Dynamic-Logic PFD, DIP-PFD and DIE-PFD. The operating frequency is 500MHz with the supply voltage 1.2 V. It can be observed that when the phase difference approaches 2π, the phase curve of Dynamic-Logic PFD (dashed line) drops down, producing a blind-zone of 27° (0.152π). The proposed DIP-PFD and DIE-PFD reveal identical phase curves shown as the solid line in Fig. 3-9. Their output is linear and identical to Dynamic-Logic PFD outside of the blind-zone region ($\varphi_{error} \in [0,\ 2\pi-\Delta]$), whereas it maintains a constant value inside the blind-zone region ($\varphi_{error} \in [2\pi-\Delta,\ 2\pi]$). Although the phase curve is not completely linear in this range, it preserves the correct polarity of output signals. This feature increases the PLL efficiency because the correct polarity is more important than the magnitude of *UP* and *DN* phase difference in the blind-zone region.

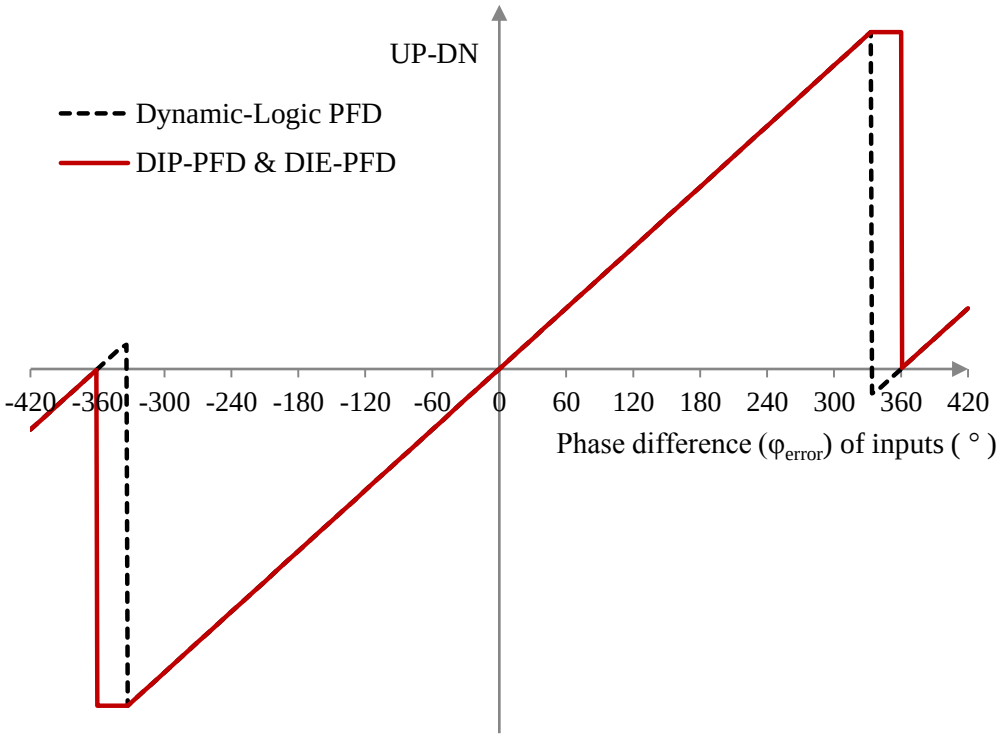


Figure 3-9. Phase characteristics of the three PFDs at 500MHz

Since the reset time T_{RST} has been fixed, increasing the input frequency will reduce the time period of the input signal and result in a larger blind-zone. Therefore, the detection range would decrease with the increasing input frequency [14]. The three architectures discussed above have been simulated using various input frequencies to see how the input frequency affects the detection range. Fig. 3-10 shows the detection range as a function of input frequency at the 1.2V supply voltage. It can be seen that as input frequency increases, the detection range of original Dynamic-Logic PFD decreases linearly, whereas the DIP-PFD and DIE-PFD still maintain better detection range. For the input frequency lower than 500MHz, both DIP-PFD and DIE-PFD have 360° (2π) detection range.

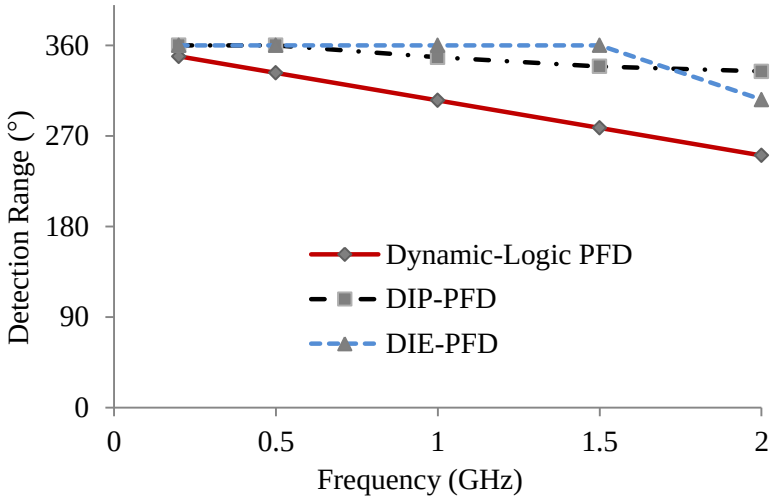


Figure 3-10. Detection range of three PFDs as a function of input frequency

As shown in Tab. 3-1, at 500MHz, the power consumption of the DIP-PFD and DIE-PFD is higher than of the conventional Dynamic-Logic PFD, as a result of static components being added to the modified architectures. However, the power increment is not significant compared to the performance improvement.

Table 3-1. Performance for PFDs @ 500MHz with Supply Voltage 1.2 V

Parameters	Original PFD	DIP-PFD	DIE-PFD
Detection range (°)	333	360	360
Blind-zone (ps)	152	0	0
Power (μW)	5.6	15.9	10.5

In order to verify the system performance, a simple PLL [15] has been designed as a test bed, allowing for comparison of three different PFDs in the same PLL system. The reference clock frequency has been set to 650MHz. The simulation of acquisition process for PLL with each one of the three PFD architectures is illustrated in Fig. 3-11. The result demonstrates that the acquisition time of the DIP-PFD and DIE-PFD has been reduced by approximately 14% in comparison to the conventional Dynamic-Logic PFD.

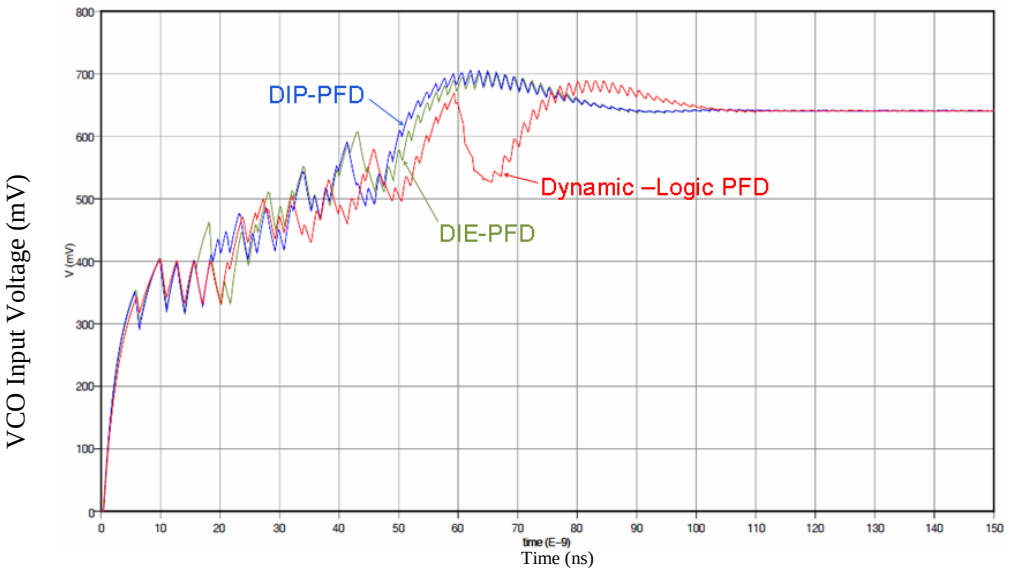


Figure 3-11. Acquisition process of the PLL with three PFDs

3.3 Charge Pump

The conventional charge pump is shown in Fig. 3-12. Theoretically, an ideal charge-pump provides constant current immediately after one of the switches closed. However, in a real phase-locked loop, the charge pump suffers from mismatches and current leakages [16]. These non-idealities could cause glitches on the VCO control voltage and lead to noisy PLL output. Therefore, the non-idealities of a charge pump should be carefully considered during circuit design.

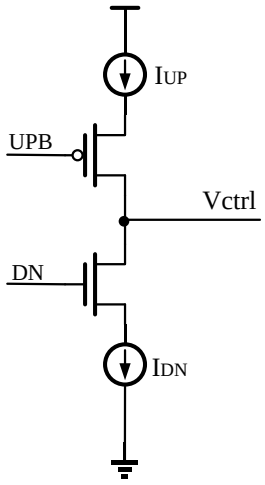


Figure 3-12. Conventional charge pump

3.3.1 Non-ideal Effects

Mismatches are one type of non-ideal effects of a charge pump, which consists of *current mismatch* and *timing mismatch*. The current sources I_{UP} and I_{DN} are usually implemented using either current mirrors or biased transistors. Mismatch originates in the different type of transistors used to implement the N-type current sources and the P-type current

sources. The resulting *current mismatch* occurs during charging and discharging the loop filter. Another type of mismatch is the *timing mismatch*. The *UPB* signal in Fig. 3-12 is active low. Therefore, an additional inverter is needed to produce *UPB* signal from the *UP* signal of PFD. The extra delay of the inverter produces the *timing mismatch*.

The second type of the non-ideal effect is current leakage, which affects the voltage stored in the loop filter. *Charge injection*, *charge sharing* and *clock feedthrough* are the main sources of the leakage current. In ON state, the switch transistors in Fig. 3-12 hold charge in their channel. When one of the switches is turned OFF, a portion of the charge will flow to the load capacitance via its drain terminal, giving rise to *charge injection* error and resulting V_{ctrl} spike. *Charge sharing* occurs when switches in charge pump are in the transition from OFF to ON state. The charge pump output voltage is floating when the switches are OFF. When the switches are turned ON, the *charge sharing* among the parasitic capacitances of the charge pump and the output node will occur, resulting in a deviation in the output voltage. *Clock feedthrough* occurs when the fast rise and fall edges of a clock signal are coupled into the signal node via the gate-to-source and gate-to-drain overlap capacitances. This rise in signal level could forward bias the MOSFET's p-n junction resulting in electron injection into the substrate that can potentially lead to faulty operation, especially if it propagates through a nearby high-impedance node [17]. The output voltage V_{ctrl} glitches due to these non-ideal effects are indicated in Fig. 3-13. Therefore, a high performance charge pump should feature minimum current leakage, and zero mismatch between I_{UP} and I_{DN} current sources.

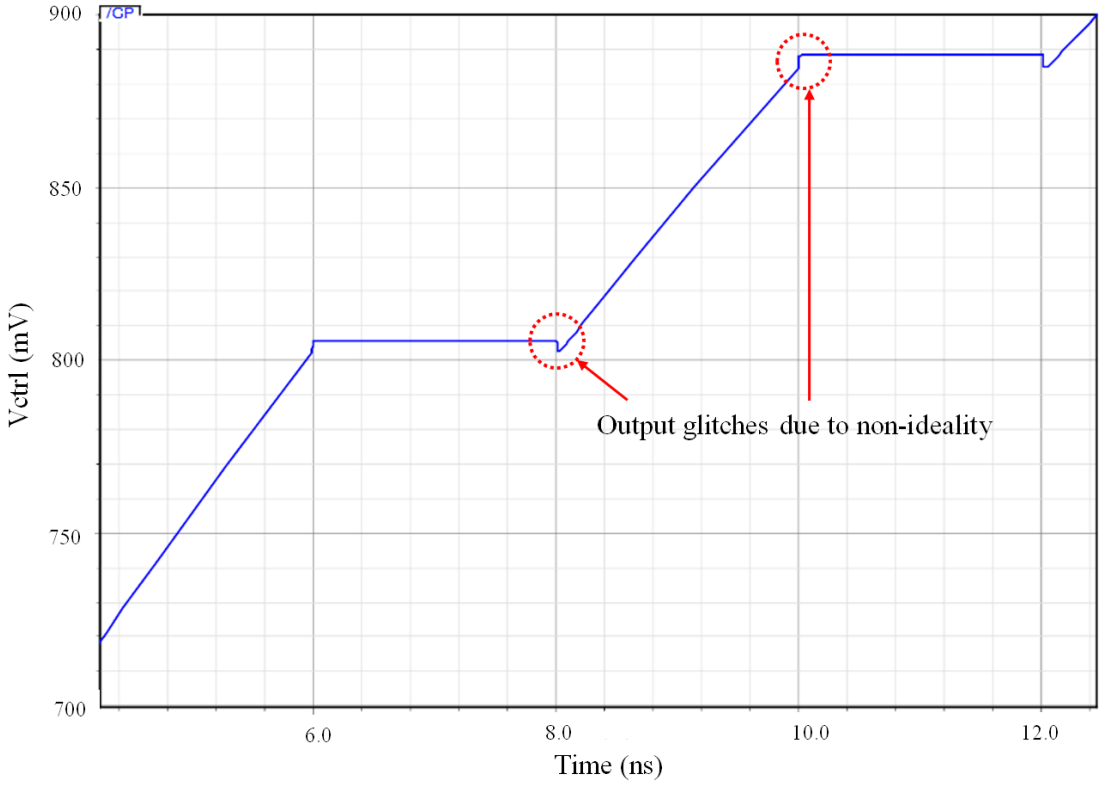
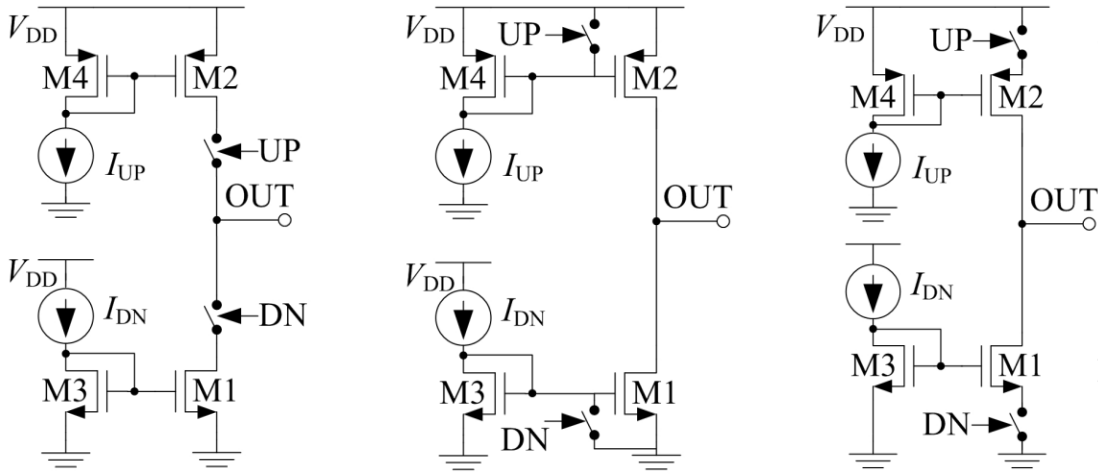


Figure 3-13. Conventional charge pump non-ideal effects

3.3.2 **Basic Structures of Charge Pump**

There are many different structures of a charge pump, among which single-ended charge pumps are popular since they do not need additional loop filter and offer tri-state operation with low-power consumption. According to the location of their switches, there are three basic architectures (Fig. 3-14).



(a) switch-at-drain (b) switch-at-gate (c) switch-at-source

Figure 3-14. Three basic structures of charge pump

Fig. 3-14(a) shows the model of the switch-at-drain charge pump. It can be seen that this structure is actually the conventional charge pump (Fig. 3-12). This circuit suffers from charge-injection error at drain of M1 and drain of M2. Having the switches close to the output makes the circuit susceptible to charge-sharing and clock feedthrough errors. Moreover, it also suffers from current mismatch across the NMOS and PMOS transistors [17].

The charge pump in which the gate is switched instead of the drain is another type of CPs (Fig. 3-14(b)). This circuit suffers from high power-consumption and low speed due to the large parasitic capacitances at the gates of the current mirror [18].

The charge pump with switches located at the source of current mirrors is another popular type of simple CPs (Fig. 3-14(c)). Since the switches are not connected to the output node directly, the charge-injection and clock feedthrough problems are improved [18].

However, since the switching time for NMOS and PMOS transistors are different, switching mismatch still exists in this structure.

3.3.3 **NMOS-switch Current Steering Charge Pump**

To improve the switching speed and minimize the switching mismatch issue of the conventional charge pumps, an NMOS-switches only charge pump in Fig. 3-15 had been proposed [19]. It consists of two differential pairs (MN4 - MN5 and MN6 - MN7) that act as switches.

The NMOS-switch current-steering charge pump operates as follows. When the *UP* signal is high and *DN* signal is low, MN4 is turned ON, which turns on the PMOS current mirror (MP1-MP2). Hence the charge pump current will flow in the MP2 and the output signal V_{ctrl} will be charged up. Meanwhile, MN7 is turned OFF since the *DN* signal is low. The discharge current is steered to MN6. Similarly, when *UP* is low and *DN* is high, current is drawn through MN7 and output signal V_{ctrl} is discharged. When *UP* and *DN* signals are driven high simultaneously, the current will be steered to MP2 and MN7. If the charge and discharge currents are equal, the output signal V_{ctrl} will remain the same. Finally, when both *UP* and *DN* signals go low, both MN4 and MN7 will be turned OFF. All current mirrored from I_{cp} will be steered into MN5 and MN6. Therefore, no current will be flowing in or out of the output node to change the output voltage.

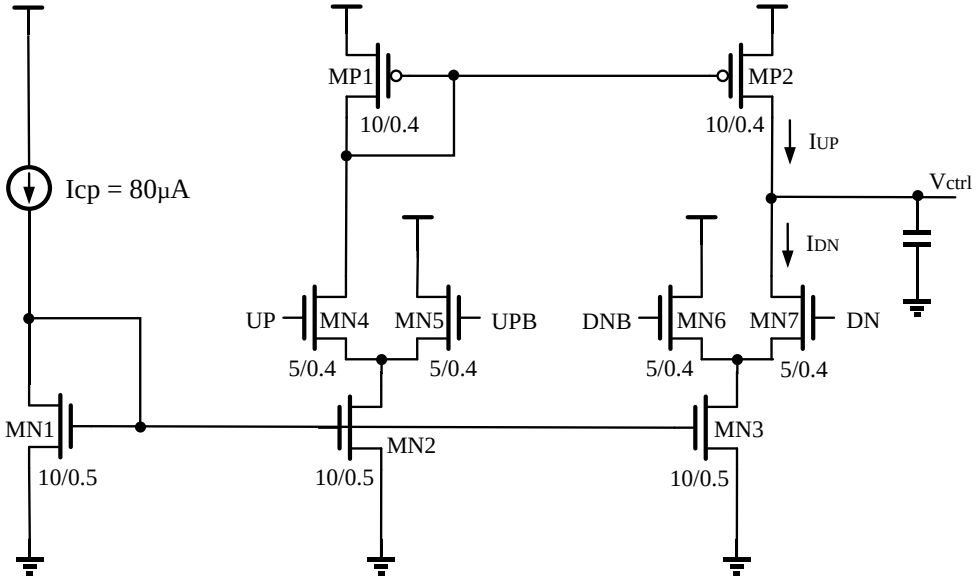


Figure 3-15. NMOS-switch current steering charge pump (W/L transistor dimensions in microns)

This NMOS-switch current steering charge pump has been designed for the pump current 80µA. Fig. 3-16 shows the process of charging up of the output voltage V_{ctrl} of the NMOS-switch current steering charge pump circuit. It can be seen that the output glitches due to the non-ideal effects have been reduced in comparison to the conventional charge pump reported in Fig. 3-13. This charge pump, however, suffers from potential output current mismatch due to the limited output resistance (r_o) of MN7 and MP2 transistors. This disadvantage may become more significant in modern submicron CMOS technologies, since the output resistance of short channel transistors is smaller than long channel devices. The current mismatch resulted from moderate values of output resistances is well illustrated through comparison of charge pump output currents (I_{UP} and I_{DN}) as shown in Fig. 3-17.

Moreover, the charge pump also suffers from a slow-path node at the gate of MP2. In the transition from *UP* to *DN*, MN5 is switched ON, MN4 is switched OFF, I_{UP} is supposed

to immediately drop to 0. However, MP1 still conducts current until its parasitic capacitance at the slow-node is fully discharged, thus slowing down the decrease of I_{UP} to 0 (shown inside the circle in Fig. 3-16). This slow node problem also exists during the transition from *DN* to *UP*.

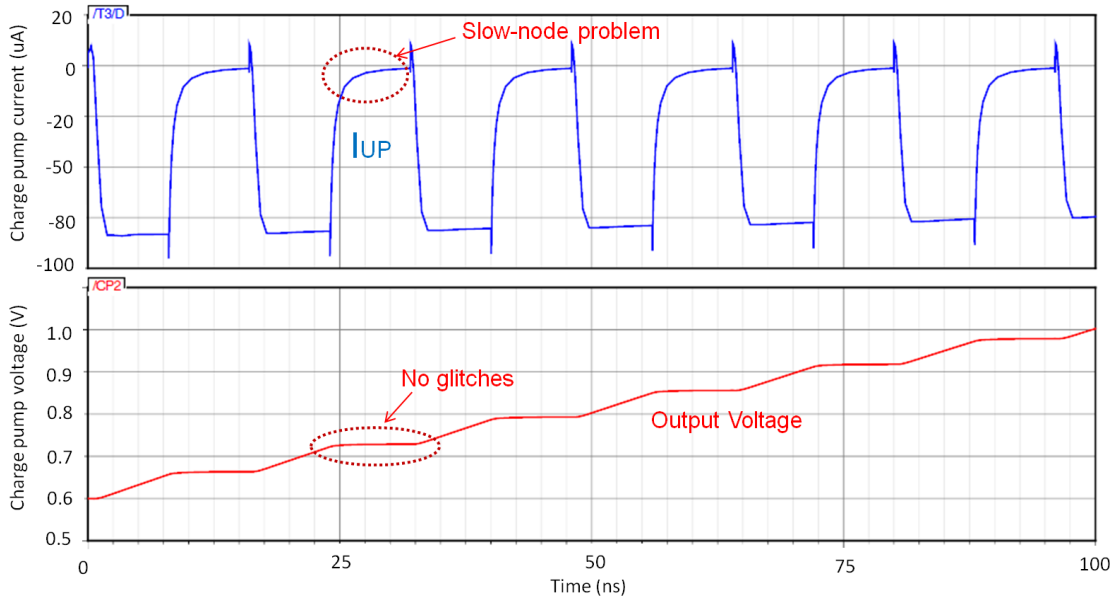


Figure 3-16. NMOS-switch current steering charge pump transient operation – charge up

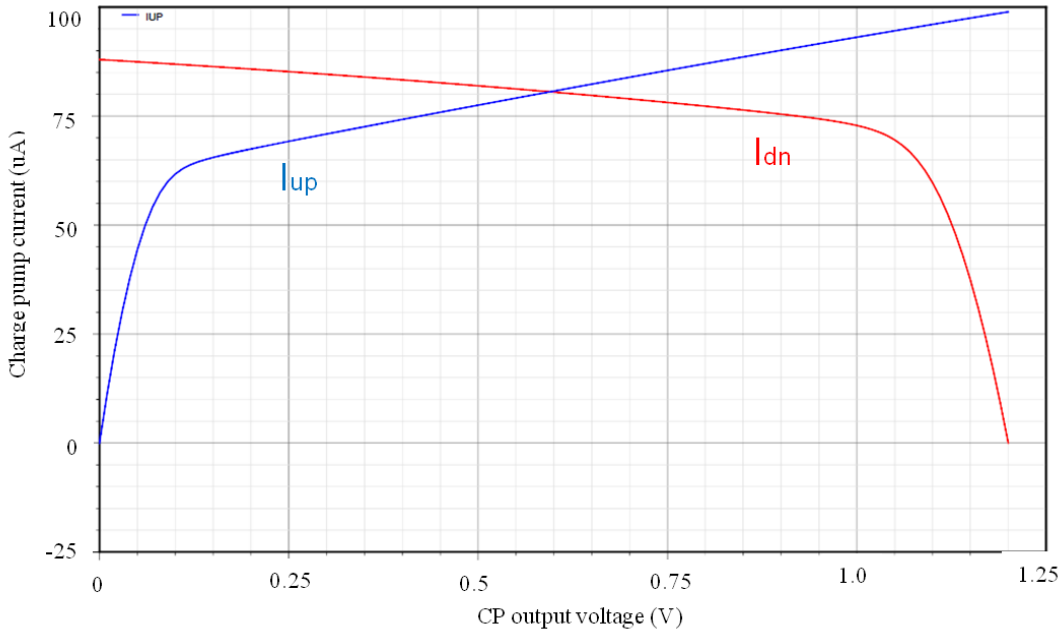


Figure 3-17. NMOS-switch current steering charge pump output current mismatch due to limited r_o

3.3.4 **NMOS-switch High-Swing Cascode Charge Pump**

A NMOS-switch high-swing cascode charge pump with improved output current matching and fast discharging is proposed in this research (Fig. 3-18). In order to increase the output resistance of current mirrors of the output stage, two high-swing cascode current mirrors are used for charge-up current I_{UP} and discharge current I_{DN}. The charge-up current is provided by the p-channel high-swing cascode current mirror (MP1, MP2, MP3, MP4 and MP5), and the discharge current is provided by the n-channel high-swing cascode current mirror (MN1, MN8, MN9, MN10 and MN11). By using the cascode structure, the output resistance is proportional to $g_m r_o^2$ instead of proportional to r_o in the original NMOS-switch charge pump shown in Fig. 3-15. With increased output resistance, the output current matching is improved.

To solve the slow-node problem, a pull-up mirror was used in the proposed charge pump design [20] and this idea is also utilized in this research. The pull-up mirror for I_{UP} is formed by MN4, MP8 and MP9. When *UP* is low, the current in MP3 starts to drop to zero. MP8 mirrors I_{cp} to MP9 and it pulls up the gate of MP3 to VDD so that MP3 could be turned off faster. This action remedies the slow-node problem and the cascode current source MP4 and MP5 can be quickly shut off. For the discharge current I_{DN}, the extra pull-down mechanism to remedy the slow node problem has been achieved by connecting the drain of MN7 to the gate of MN9.

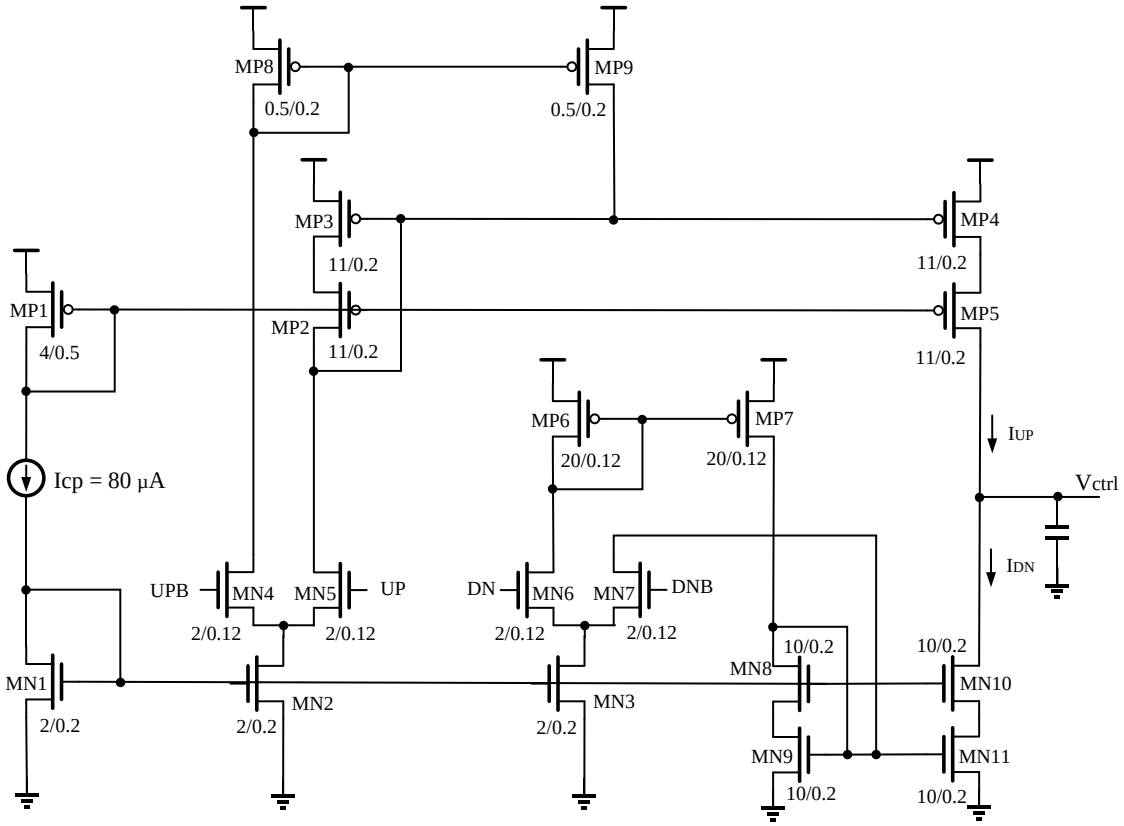


Figure 3-18. NMOS-switch high-swing cascode charge pump (W/L transistor dimensions in microns)

The proposed NMOS-switch high-swing cascode charge pump has been designed for pump current of 80µA. The DC and transient operation of the design was simulated to examine the charge pump performance. Fig. 3-19 shows the DC operation of the charge pump, revealing the current matching significantly improved (compared to Fig. 3-16). Fig. 3-20 and Fig. 3-21 shows the process of charging up and down of the output voltage V_{ctrl} of the NMOS-switch high-swing cascode charge pump circuit, respectively. It can be seen that the new charge pump circuit has a fast charging and discharging process compared to the NMOS-switch current steering charge pump.

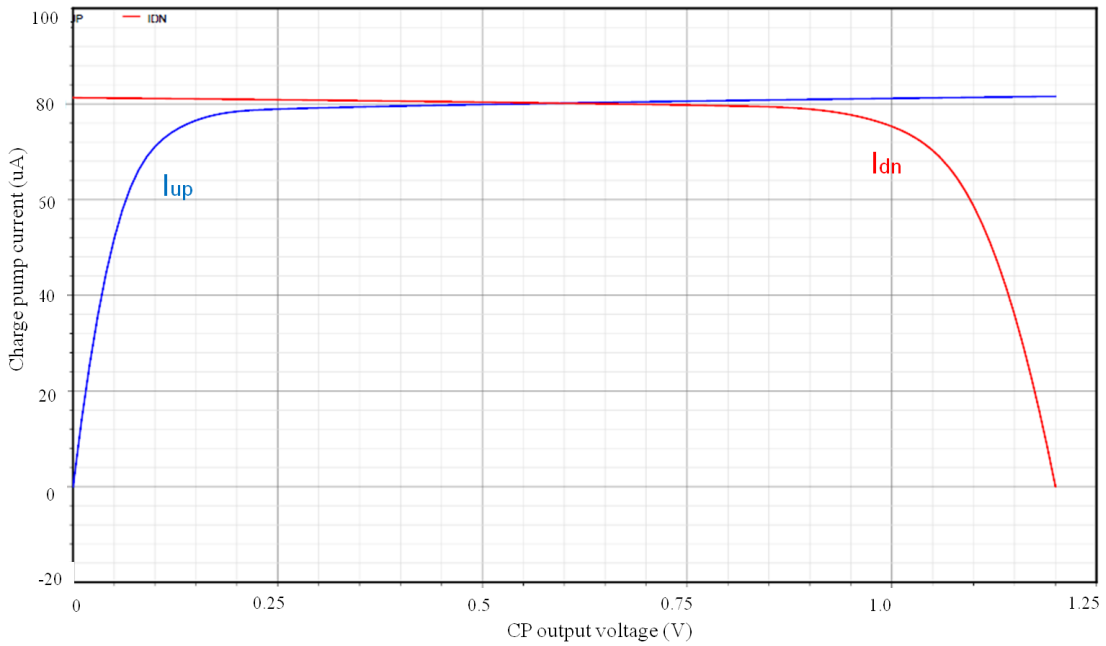


Figure 3-19. Output current DC analysis of the NMOS-switch high-swing cascode charge pump

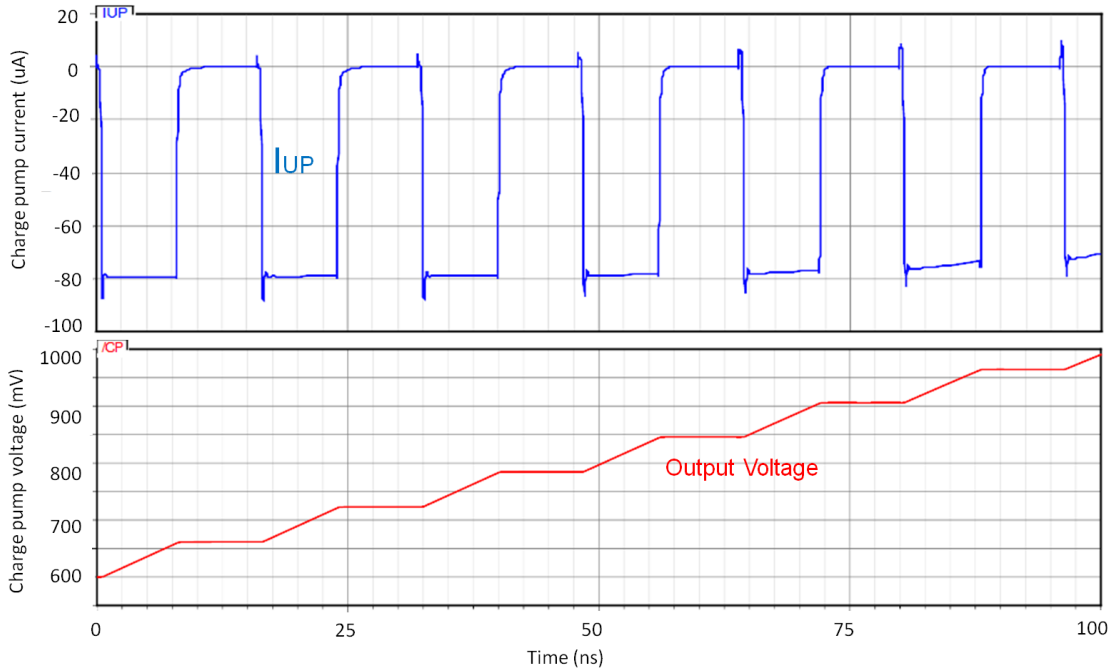


Figure 3-20. NMOS-switch high-swing cascode charge pump transient operation – charge up

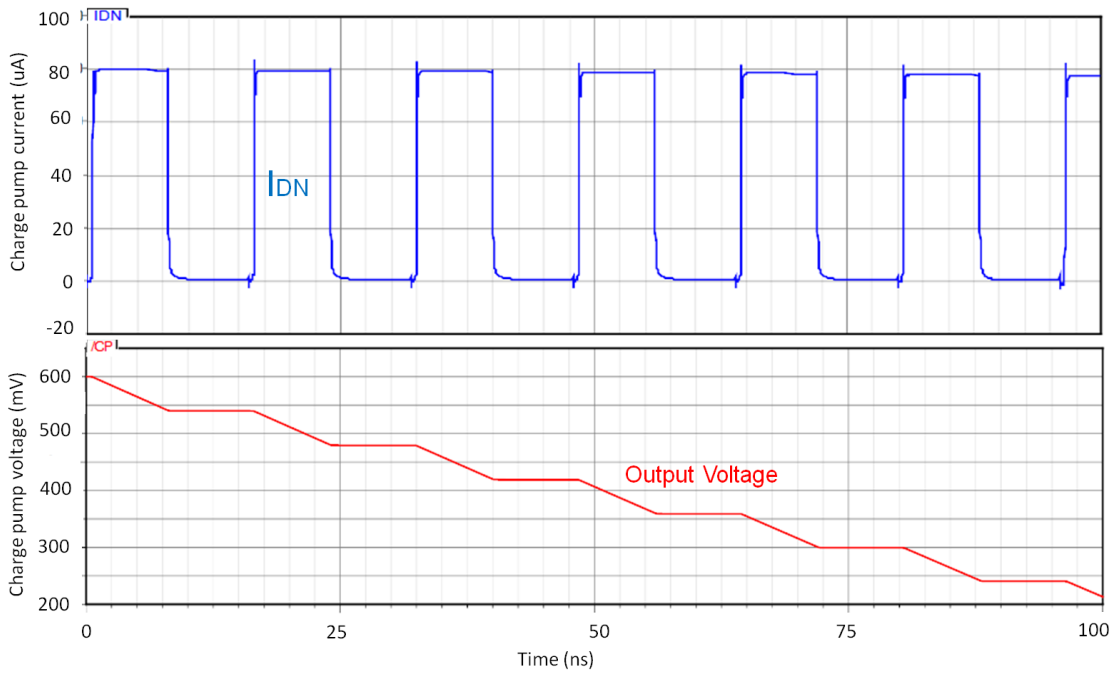


Figure 3-21. NMOS-switch high-swing cascode charge pump transient operation – discharge

To observe the superiority of the NMOS-switch high-swing cascade charge pump noise performance, the two charge pumps paired with the same Dynamic-Logic PFD (Fig. 3-2) have been simulated using SpectreRF noise analysis (Fig. 3-22). Comparing with the existing charge pump, the new NMOS-switch high-swing cascode charge pump paired with the Dynamic-Logic PFD demonstrated 9dB attenuation in terms of current noise power spectral density.

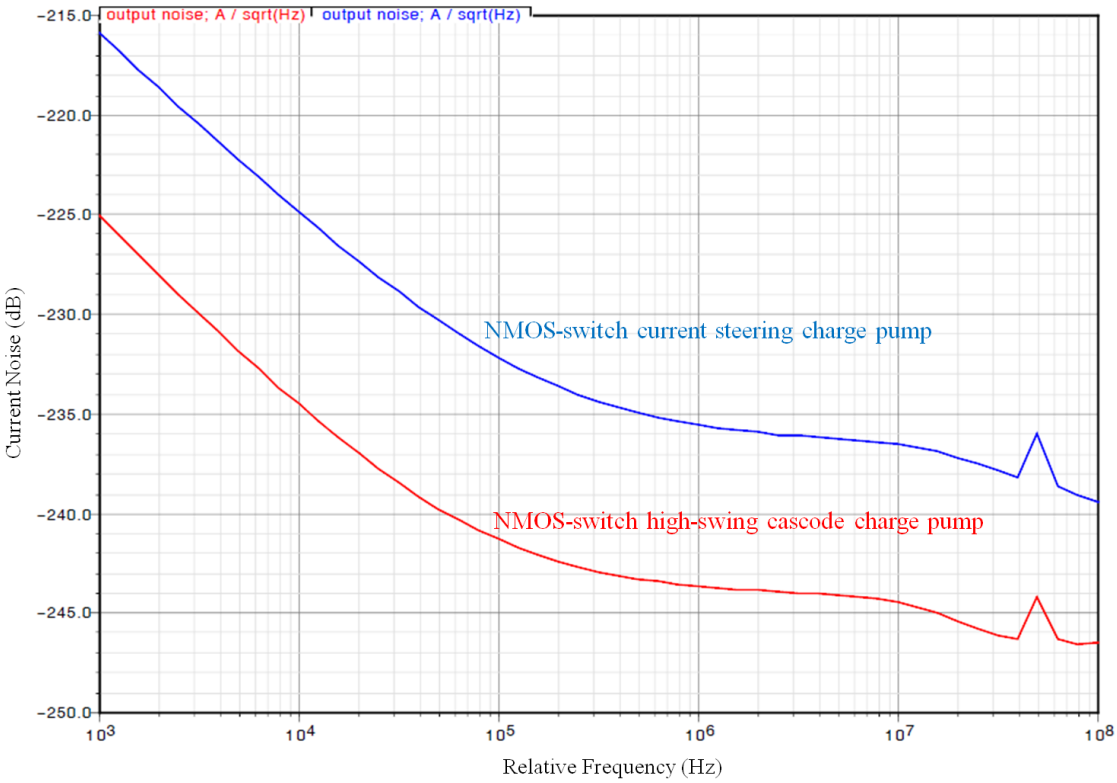


Figure 3-22. Noise comparison of charge pumps

3.4 Loop Filter

The loop filter that was designed in this thesis is a 2nd order passive low-pass filter (Fig. 3-23). The main loop filter capacitor (C1) converts the charge pump current to the VCO control voltage. However, it brings additional pole at zero, causing 180° phase shift that leads to unstable behavior. A loop filter resistor (R1) connected to the main filter capacitor in series brings a zero and therefore it stabilizes the loop. However, adding a resistor will introduce high frequency ripples in output voltage. To eliminate those high frequency components an additional filter capacitor (C2) is connected to those in parallel [4]. To explore the design procedure, some of the loop dynamics analysis from Chapter 2 is repeated here.

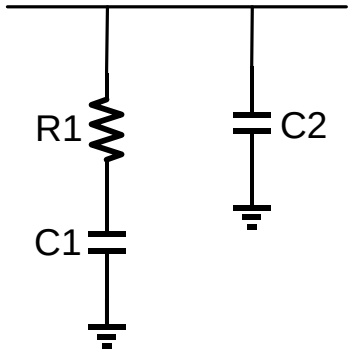


Figure 3-23. 2nd order passive loop filter

The PLL loop diagram is shown in Fig. 3-24. The loop transfer functions can be obtained using the feedback theory [21].

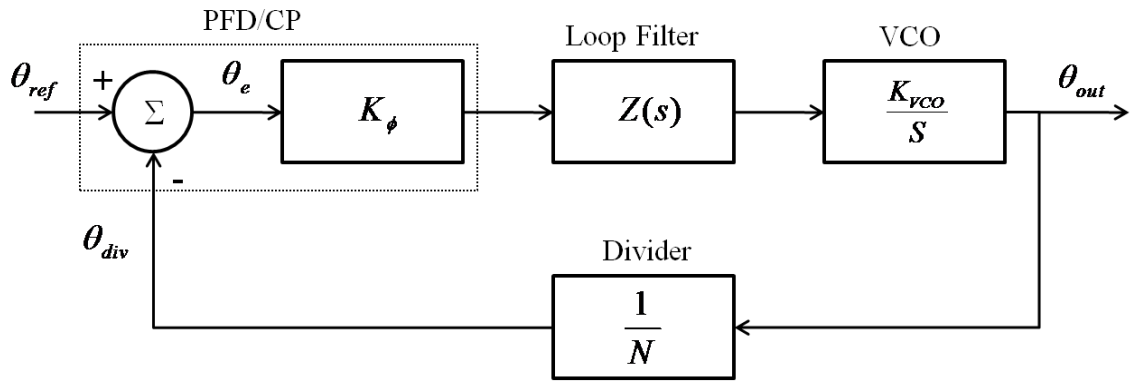


Figure 3-24. PLL loop diagram

$$\text{Forward loop gain:} \quad G(s) = \frac{\theta_{out}}{\theta_e} = \frac{K_\phi Z(s) K_{vco}}{s} \tag{3.1}$$

$$\text{Reverse loop gain:} \quad H(s) = \frac{\theta_{div}}{\theta_{out}} = \frac{1}{N} \tag{3.2}$$

$$\text{Open-loop gain:} \quad H(s)G(s) = \frac{\theta_{div}}{\theta_e} = \frac{K_\phi Z(s) K_{vco}}{Ns} \tag{3.3}$$

$$\text{Closed-loop gain:} \quad CL(s) = \frac{\theta_{out}}{\theta_{ref}} = \frac{G(s)}{1 + H(s)G(s)} \tag{3.4}$$

The impedance of the loop filter shown in Fig. 3-23 is,

$$Z(s) = (R_1 + \frac{1}{sC_1}) \| \frac{1}{sC_2} = \frac{1 + s(R_1 \cdot C_1)}{s^2(R_1 \cdot C_1 \cdot C_2) + sC_1 + sC_2} \tag{3.5}$$

Defining two time constants T_1 and T_2 as

$$T_1 = R_1(C_1 \| C_2) = \frac{R_1 \cdot C_1 \cdot C_2}{C_1 + C_2} \tag{3.6}$$

$$T_2 = R_1 \cdot C_1 \tag{3.7}$$

The impedance of the loop filter can be written as,

$$Z(s) = \frac{1}{sC_2} \cdot \frac{T_1}{T_2} \cdot \frac{1+sT_2}{1+sT_1} \tag{3.8}$$

Hence, the open loop gain of the PLL in terms of frequency ω is,

$$H(s)G(s)|_{s=j\omega} = -\frac{K_\phi K_{vco}}{Ns^2C_2} \cdot \frac{1+j\omega T_2}{1+j\omega T_1} \cdot \frac{T_1}{T_2} \tag{3.9}$$

One can see that the zero (ω_z) and the pole (ω_p) of the open-loop transfer function are directly related to the time constants, T_1 and T_2, respectively,

$$T_1 = \frac{1}{\omega_p} \tag{3.10}$$

$$T_2 = \frac{1}{\omega_z} \tag{3.11}$$

The design of filter components values are related to the open-loop transfer function bandwidth (ω_{bw}) and the phase margin (ϕ_{pm}). A typical open-loop transfer function magnitude and phase plot is shown in Fig. 3-25. The phase shift at DC frequency is -180° because of two poles at zero frequency, and thus amplitude slope is -40dB/decade. The phase shift is -135° and the magnitude slope is -20dB/decade at the frequency of the zero $\omega_z = 1/T_1$. At the pole $\omega_p = 1/T_2$, the slope of magnitude is -40dB/decade and phase shift is -135° again. The phase margin, ϕ_{pm}, is defined as the difference between 180° and the phase of the open loop transfer function at the crossover frequency, ω_c, corresponding to 0-dB gain. The phase margin is usually chosen between 30° and 70°. For this design, the phase margin is chosen to be 56°, which is a typical value for Type-II 3rd order PLL design.

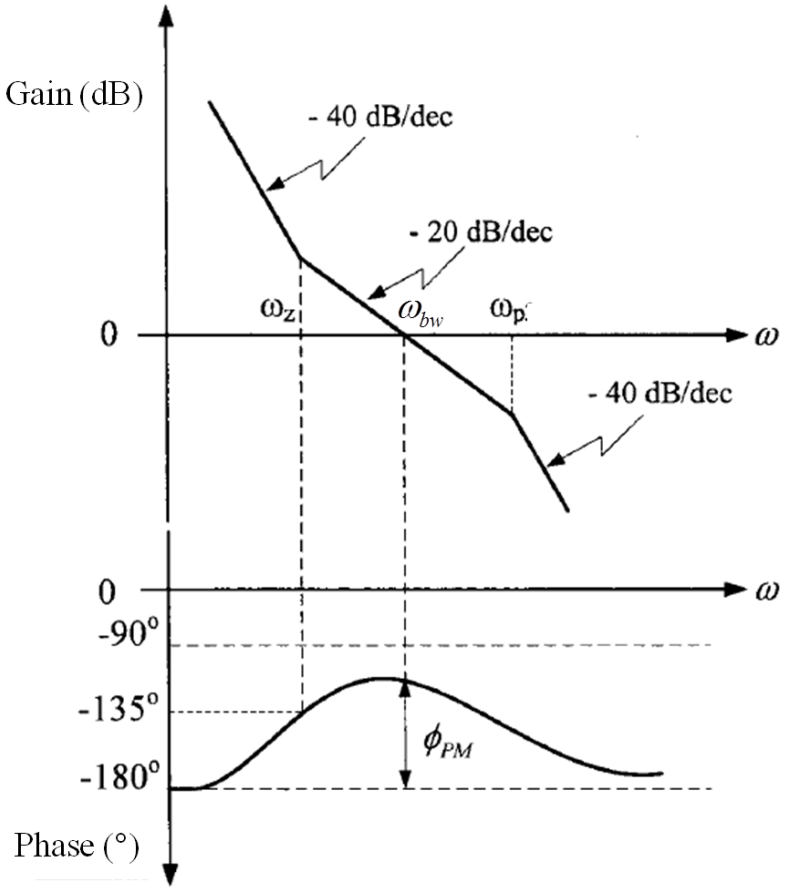


Figure 3-25. Typical type-II 3rd order PLL open loop gain and phase plot

Therefore, the phase margin is

$$\phi_{pm} = \tan^{-1}(\omega_{bw} \cdot T_2) - \tan^{-1}(\omega_{bw} \cdot T_1) + 180° \tag{3.12}$$

The phase margin is maximized at the crossover frequency by setting the derivative of the phase margin equal to 0,

$$\frac{d\phi_{pm}}{d\omega_{bw}} = \frac{T_2}{1+(\omega_{bw} \cdot T_2)^2} - \frac{T_1}{1+(\omega_{bw} \cdot T_1)^2} = 0 \tag{3.13}$$

From the above equation, we can find the loop bandwidth (ω_{bw}),

$$\omega_{bw} = \frac{1}{\sqrt{T_1 \cdot T_2}} \tag{3.14}$$

Solving the equations (3.4.12) and (3.4.14), we calculate T_1 and T_2,

$$T_1 = \frac{\sec\phi_{pm} - \tan\phi_{pm}}{\omega_{bw}} \tag{3.15}$$

$$T_2 = \frac{1}{\omega_{bw}(\sec\phi_{pm} - \tan\phi_{pm})} \tag{3.16}$$

The magnitude of the open loop gain is 0 dB at the crossover frequency (ω_{bw}), therefore,

$$\left\| H(j\omega_{bw})G(j\omega_{bw}) \right\| = \frac{K_\phi K_{vco}}{N\omega_{bw}^{\ 2}C_2} \cdot \frac{T_1}{T_2} \cdot \left\| \frac{1+ j\omega_{bw}T_2}{1+ j\omega_{bw}T_1} \right\| = 1 \tag{3.17}$$

Given the open loop gain bandwidth (ω_{bw}) and the phase margin (ϕ_{pm}), the loop filter components R1, C1and C2 can be obtained in the following equations.

$$C_2 = \frac{K_\phi K_{vco}}{N\omega_{bw}^{\ 2}} \cdot \frac{T_1}{T_2} \cdot \sqrt{\frac{1+(\omega_{bw}T_2)^2}{1+(\omega_{bw}T_1)^2}} \tag{3.18}$$

$$C_1 = C_2 \cdot (\frac{T_2}{T_1} - 1) \tag{3.19}$$

$$R_1 = \frac{T_2}{C_1} \tag{3.20}$$

The target specifications of PLL are shown in Tab. 3-2.

Table 3-2. PLL design specifications

VCO Gain K_{vco}	510MHz/V
FPD/CP Gain K_{ϕ}	80uA
Divider Ratio N	16
Loop Bandwidth f_{bw}	5MHz
Phase Margin ϕ_{pm}	56°

In the above table, the VCO gain is obtained from the VCO design, which can be found in Section 3.5. The components values of loop filter were calculated using the above derivations and the PLL design specifications. The calculation has been performed using Matlab, and the code is attached in Appendix A. The loop filter components values are summarized in Tab. 3-3.

Table 3-3. Loop filter components values

R1	13.59kΩ
C1	7.66pF
C2	0.79pF

With the selected filter components values, the PLL open-loop transfer function Bode plot can be determined. As shown in Fig. 2-16, at cross frequency 5MHz (which equals loop bandwidth), the phase margin is 56°. The zero before the cross frequency is located at 1.5MHz, while the pole after the cross frequency is located at 10.6MHz. Loop filter components can be realized with on-chip devices. For example filter capacitors can be implemented with NMOS capacitance and resistor can be implemented with high resistivity poly resistor. The design of on-chip loop filter is beyond the scope of this thesis.

3.5 Voltage Controlled Oscillator

3.5.1 **Differential VCO Structure**

The VCO in this design is a differential ring oscillator based VCO. The advantage of differential VCO compared to single-ended VCO is the superior common-mode noise (i.e. power supply and substrate noise) rejection ability. Therefore, the differential VCO is more suitable for modern mixed-signal IC on-chip environment, in which the digital circuitry will generate a substantial amount of power supply and substrate noise.

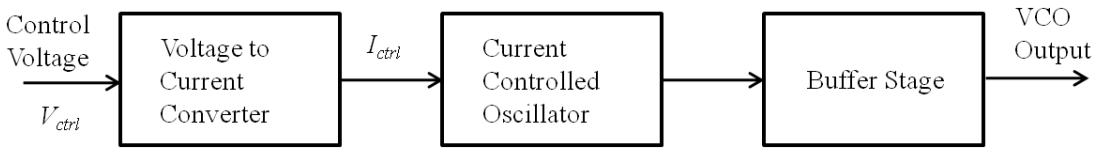


Figure 3-26. VCO block level diagram

The structure of the VCO in this design is shown in Fig. 3-26. The control voltage from loop filter feeds into the voltage to current converter and generates the control current. The current controlled oscillator is tuned by this control current to generate differential clock signals. Finally, the buffer stage converts the differential signals to single-ended and square wave clock signal. In this thesis, an 800 MHz low-power low-noise 3-stage differential ring oscillator VCO is designed.

3.5.2 **Voltage to Current Converter**

The linear voltage to current conversion characteristic is going to be achieved by using the large aspect ratio transistor, M1, shown in Fig. 3-27, characterized by a very small over-drive voltage (V_{ov}). A first-order relationship between the control voltage (V_{ctrl}) and the control current (I_{ctrl}) has been derived below. The gate-to-source voltage, V_{GS} , of the transistor M1 in Fig. 3-27 is

$$V_{GS} = V_{TH} + V_{OV} = V_{TH} + \sqrt{\frac{2I_{ctrl}}{K'(W/L)}} = V_{ctrl} - I_{ctrl} \cdot R \tag{3.21}$$

If W/L is large enough, the above equation can be simplified as

$$V_{ctrl} - V_{TH} \approx I_{ctrl} \cdot R \tag{3.22}$$

thus producing almost linear voltage-to-current conversion [22]. Transistors M2 and M3 form a current mirror which provides the control current to each delay stage in the current controlled oscillator.

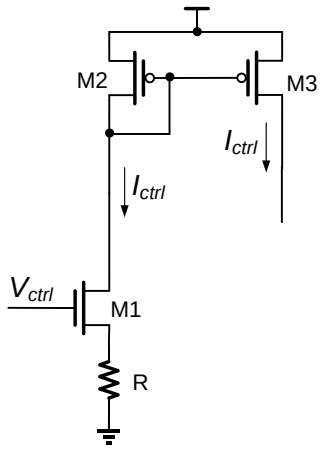


Figure 3-27. Linear voltage-to-current converter

3.5.3 **Current Controlled Oscillator**

The current controlled oscillator core is a current controlled current steering amplifier (CSA) delay cell proposed in [23] as shown in Fig. 3-28.

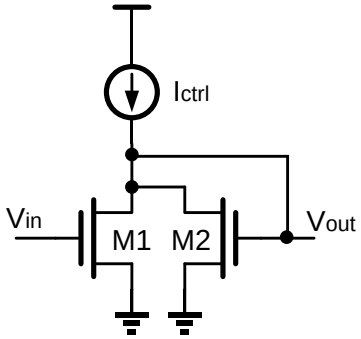


Figure 3-28. CSA delay cell

The CSA cell consists of a current source and a pair of NMOS transistors. M1 is the input device and M2 is the diode connected load. When V_{in} is high, M1 turns on. It sinks the control current I_{ctrl} and shuts off M2. Under this condition, the on resistance of M1 and I_{ctrl} defines the output low voltage V_{OL}. When V_{in} is low, M1 turns off and I_{ctrl} is steered to M2. Under this condition, the resistance of the diode-connected M2 defines the output high voltage V_{OH}. By varying the control current I_{ctrl}, a current-controlled CSA-based ring oscillator is formed with an output voltage swing of [24]

$$\Delta V = V_{OH} - V_{OL} = V_{TH} + \sqrt{\frac{(W/L)_1 - (W/L)_2}{(W/L)_1 \cdot (W/L)_2} \cdot \frac{2I_{ctrl}}{K'}} \tag{3.23}$$

The relationship between the oscillation frequency and the control current can be approximated as

$$f_{osc} \propto \frac{I_{ctrl}}{N \cdot C_L \cdot \Delta V} \propto \sqrt{I_{ctrl}} \tag{3.24}$$

where N is the number of delay stages in the ring oscillator and C_L is the load capacitance. From Eqn. (3.24), we see that the frequency is proportional to the square root of the control current. For a fixed range of the I_{ctrl} current, this can be approximated as a quasi-linear relationship. An advantage of the CSA delay stage is that ground noise coupled from other circuitry within the chip is rejected by the CSA as a common mode noise because both its output and input are referred to the same ground.

In this design, the differential delay cell (Fig. 3-29) exploits the concept of the CSA [24]. The delay cell consists of two input transistors M5 and M6, and of two CSA cell pairs M1, M2 and M3, M4. Being driven by the differential input signals, M1 and M4 pull each output node to ground, creating a relatively constant output swing even with large variations in I_{ctrl}. The output voltage swing of the differential delay cell is

$$\Delta V = V_{TH} + \sqrt{\frac{2I_{ctrl}}{K'(W/L)_2}} \tag{3.25}$$

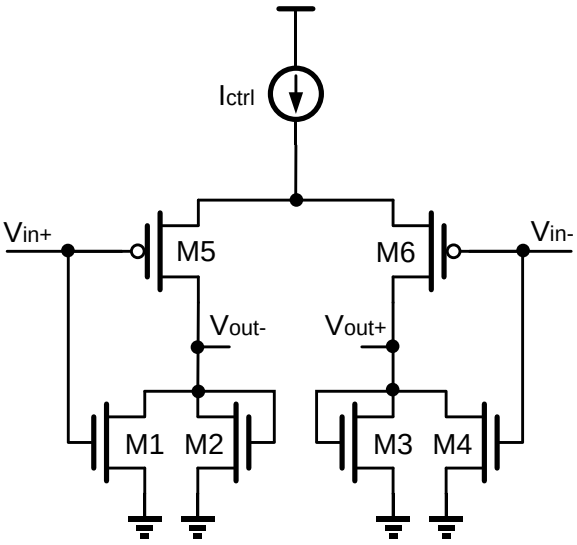


Figure 3-29. Differential delay cell

3.5.4 **Phase Noise and Jitter in Differential Ring Oscillator**

According to [25], the phase noise of the differential ring oscillator, $L(\Delta\omega)$, has an inverse relationship with the control current and the voltage swing,

$$L(\Delta\omega) \propto \frac{kT}{I_{ctrl} \cdot \Delta V} \cdot \frac{f_0^2}{\Delta f^2} \tag{3.26}$$

We can draw several scenarios to optimize noise performance from Eqn. (3.26),

1) Use high supply voltage and provide as much current as budget allows
2) Increase the delay cell voltage swings

In this thesis, both of above methods have been used to optimize noise performance within available power consumption limits.

3.5.5 **Differential VCO circuit design**

The 800 MHz 3-stage differential VCO schematic is shown in Fig. 3-30. M10 and R form a linear voltage-to-current converter which provides the control current to the delay cells. M1 to M8 form the differential delay cell. Based on Eqn. (3.25) and discussion in Section 3.5.4, transistors M2 and M3 should have a small W/L ratio in order to obtain high voltage swings and thus decrease oscillator noise. In addition, a high control current is preferred for low noise performance; however, increasing the control current also increases the power consumption. Therefore, there is a design tradeoff between noise performance and power consumption. Transistor M8 is added to provide additional bias current for the delay cell. This extra current decreases the VCO gain (i.e. the tuning sensitivity). High tuning sensitivity affects the noise performance in the entire PLL

system. A small variation in the control voltage will cause a large deviation of the oscillator frequency from its desired value.

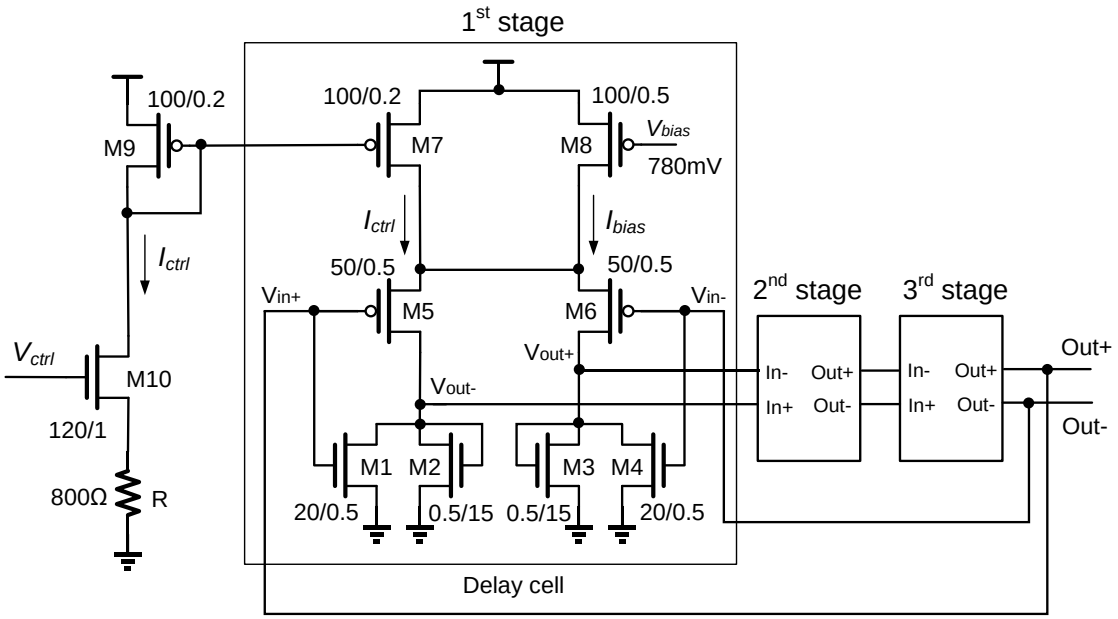


Figure 3-30. Differential VCO circuit schematic (W/L transistor dimensions in microns)

The waveform of the VCO output is nearly a sinusoidal periodic waveform with a limited voltage swing. It must be shaped before being applied in digital circuit. In order to convert the VCO output signal to a square rail-to-rail switching signal, a buffer stage as shown in Fig. 3-31 is added at the end of the VCO delay cells.

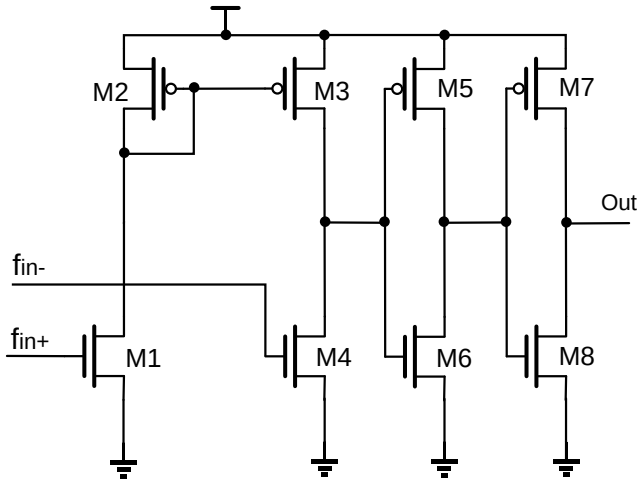


Figure 3-31. Buffer stage

3.5.6 **VCO Simulation Results**

Fig. 3-32 illustrates the simulated VCO frequency as a function of the control voltage (VCO gain K_{vco}). The figure shows a quasi-linear relationship in the frequency range from 550MHz to 950MHz. The gain K_{vco} is 510MHz/V at the 800MHz operating frequency.

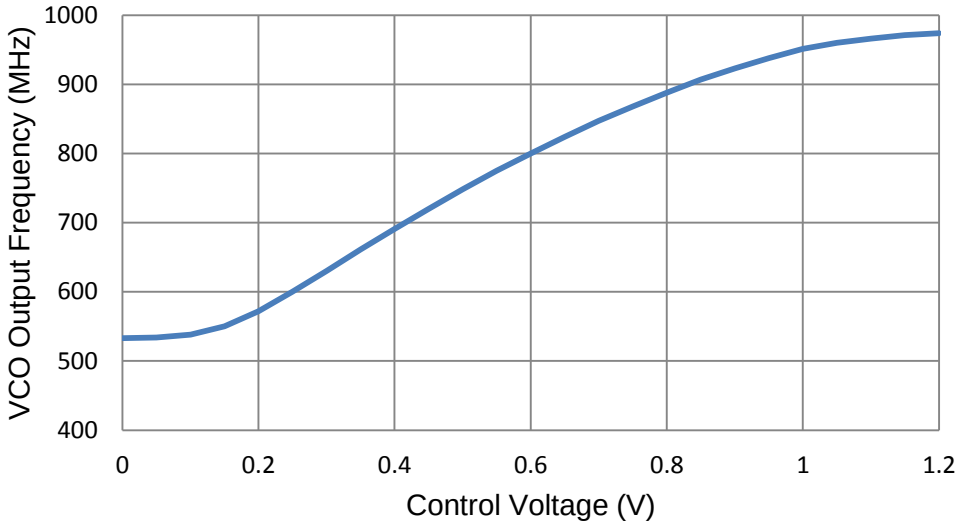


Figure 3-32. VCO Frequency versus Control Voltage (VCO gain)

The phase noise of the VCO operating at 800MHz is simulated using SpectreRF and the phase noise measured at offset frequency 1MHz has been found equal to -105.2dBc/Hz (Fig. 3-33).

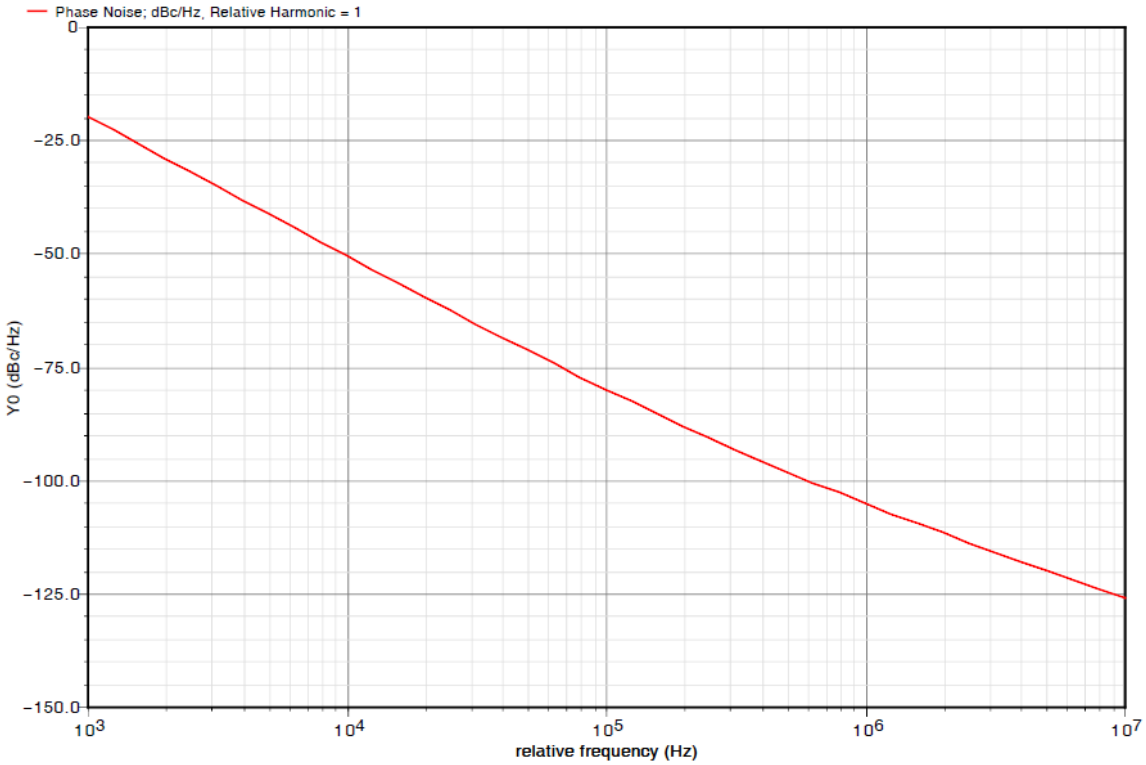


Figure 3-33. VCO phase noise at 800MHz

The average VCO power consumption as a function of the control voltage is simulated (Fig. 3-34). As operating frequency increases, the power consumption of the VCO also increases. At the operating frequency 800MHz, the VCO consumes 2.5mW power.

The performance of the differential VCO designed in this thesis has been compared to the performance of other published oscillators (Tab. 3-4).

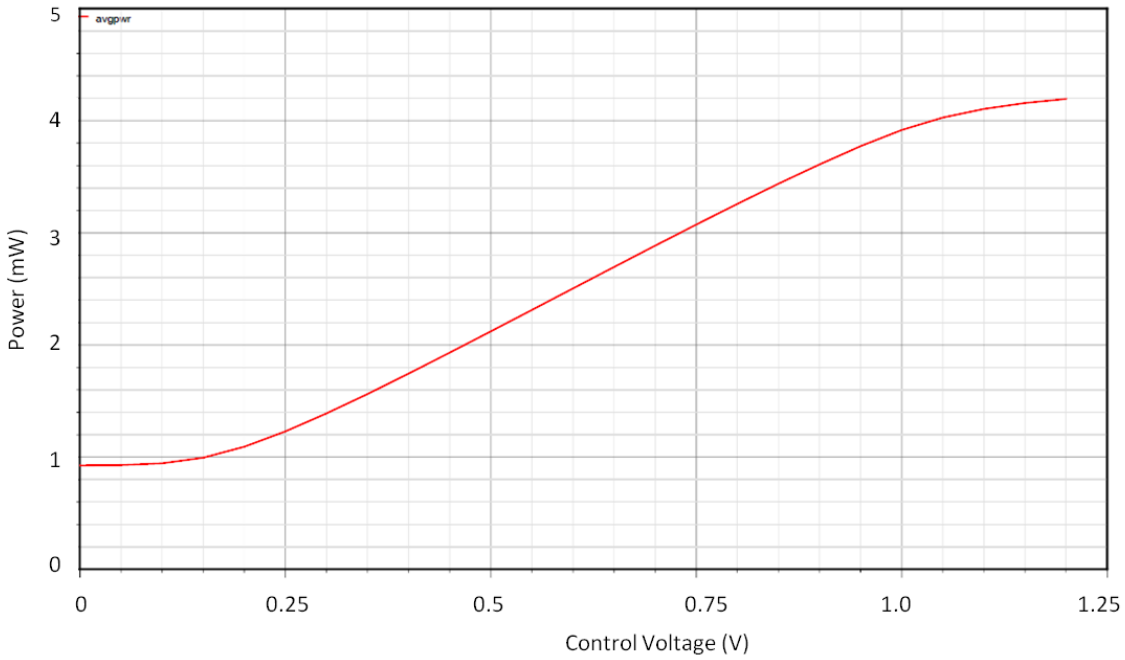


Figure 3-34. VCO power consumption

Table 3-4. Comparison of VCO performance

	[26]	[27]	[28]	[29]	[30]	[31]	This Work
No. of stages	2	3	2	4	2	2	3
Technology (um)	0.18	0.35	0.18	0.18	0.18	0.18	0.13
Tuning range (MHz)	730 - 1430	381 - 1150	440 - 1595	450 - 1150	440 - 1400	475 - 1000	550 - 950
Operating frequency (MHz)	900	866	-	1000	881	900	800
Phase noise (dBc/Hz)	-106.1	-105.5	-93	-94	-90	-109	-105.2
Offset frequency (MHz)	0.6	1	1	1	0.6	0.6	1
Power dissipation (mW)	65.5	7.48	26	3	<16	19.2	2.5

In comparison with other published CMOS ring oscillator VCOs operating at similar frequencies, the VCO in this design provides good noise performance (-105.2dBc/Hz @ 1MHz offset frequency) while maintained quite low power consumption (2.5mW).

3.6 Frequency Divider

The targeted output clock frequency of the PLL in this thesis is 800MHz. In the case of the input reference clock frequency of 50MHz, a divide-by-16 frequency divider is required. The frequency divider in this thesis consists of 4 cascaded divide-by-2 stages.

Among many possible architectures of divide-by-2 circuits, we chose the TSPC D-flip-flop divider topology (Fig. 3-35). The topology of divide-by-16 frequency divider is depicted in Fig. 3-36.

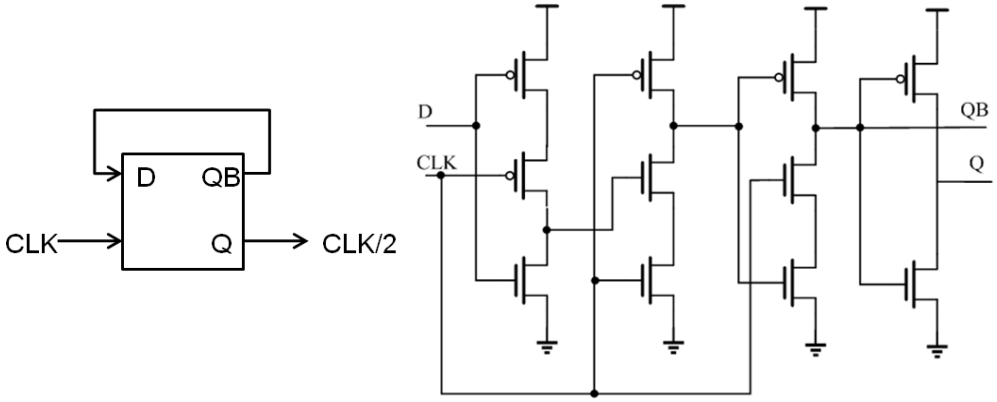


Figure 3-35. Divide-by-2 diagram and circuit implementation

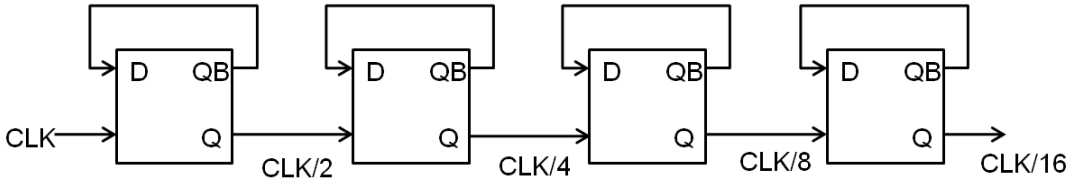


Figure 3-36. Divide-by-16 block diagram

The frequency divider is simulated for an input frequency of 800MHz (Fig. 3-37). One can see the relationship between input (CLK) and output (DIV_OUT) in terms of period is $T_{DIV\_OUT} = 16 \times T_{CLK}$. Therefore, the output frequency is 1/16 of input frequency.

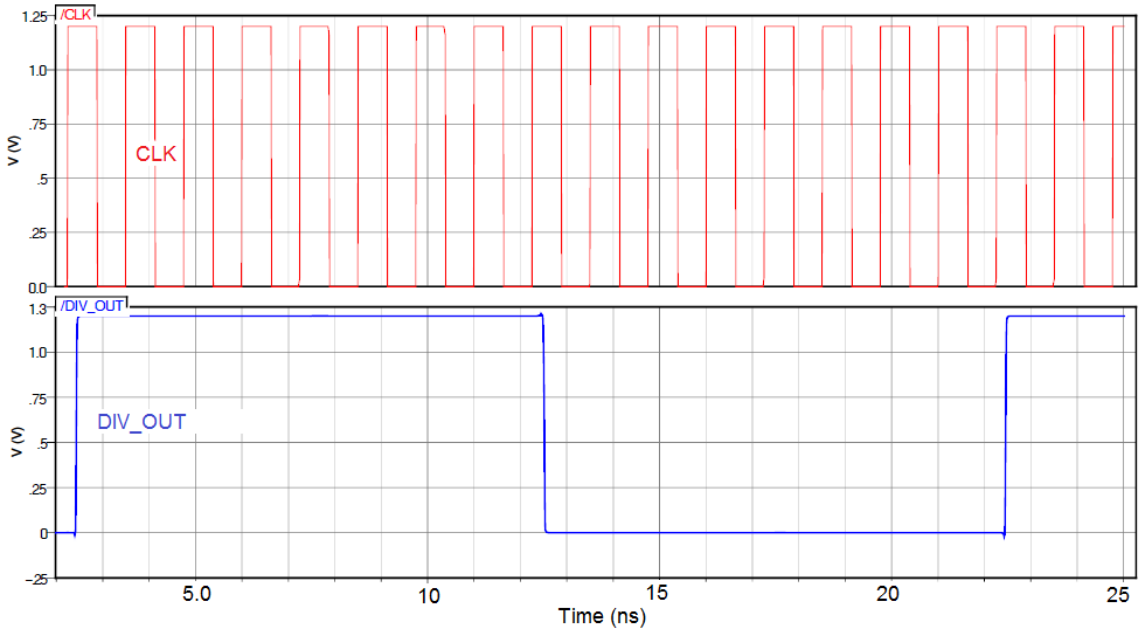


Figure 3-37. Frequency divider simulation with input frequency @ 800MHz

The frequency divider shows linear relationship between the input and output frequency with a slope of 1/16 for the input frequency up to 7GHz, as shown in Fig. 3-38.

The phase noise of frequency divider has been simulated using SpectreRF (Fig. 3-39). As one can see, the phase noise decreases as the relative frequency offset increases. Comparing to the phase noise of VCO (Fig. 3-33), the frequency divider noise contribution to the PLL system is insignificant.

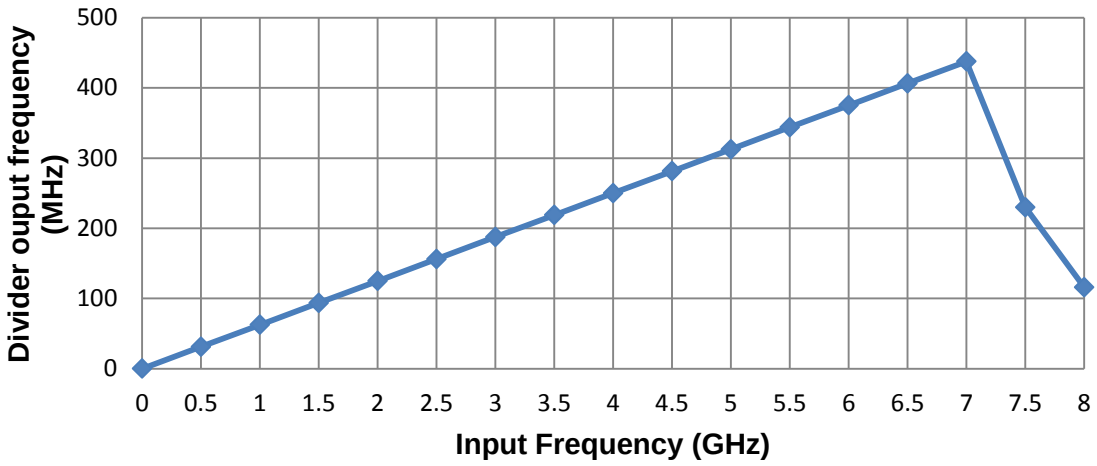


Figure 3-38. Linear operation range of frequency divider

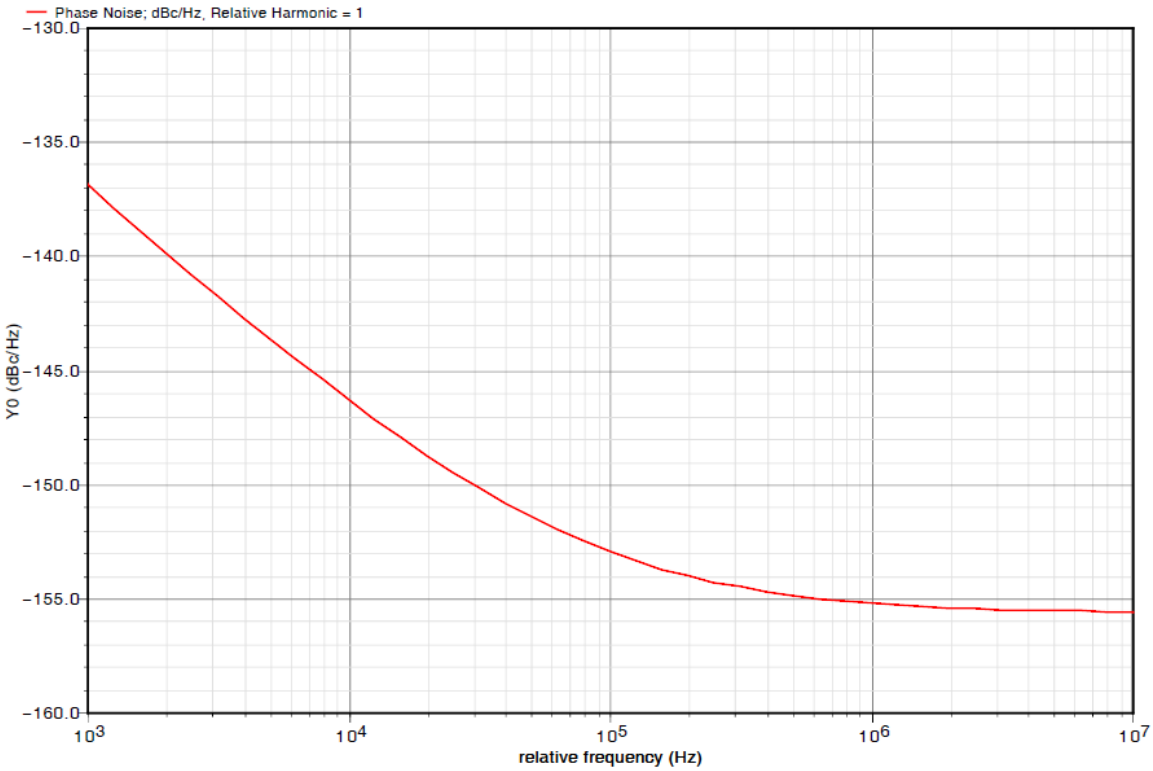


Figure 3-39. Frequency divider phase noise

4 SYSTEM-LEVEL PLL SIMULATION AND DISCUSSION

4.1 Transient Simulation

The PLLs with three PFDs (Section 3.2) have been simulated to observe the locking process. Since the reference clock frequency is quite low, the blind-zone issue is insignificant. The simulation results show PLLs with three PFDs have identical locking behavior. Therefore, for simplicity, only the simulation results of the PLL with Dynamic-Logic PFD (as shown in Fig. 3-2) are shown.

The PLL locking process in terms of VCO control voltage (VCO's control voltage as a function of time) is illustrated in Fig. 4-1. At the locking state, the VCO control voltage is 580mV, which is in the middle range between ground and power supply. The PLL locking process in terms of output frequency (PLL frequency as a function of time) has also been simulated (Fig. 4-2). At the locking state, the PLL output frequency is stabilized at 800MHz, as design specifications required. The simulations results indicate the estimated locking time is around 400ns. This result agrees with the behavioral modeling analysis presented in Fig. 2-19 in Section 2.4.

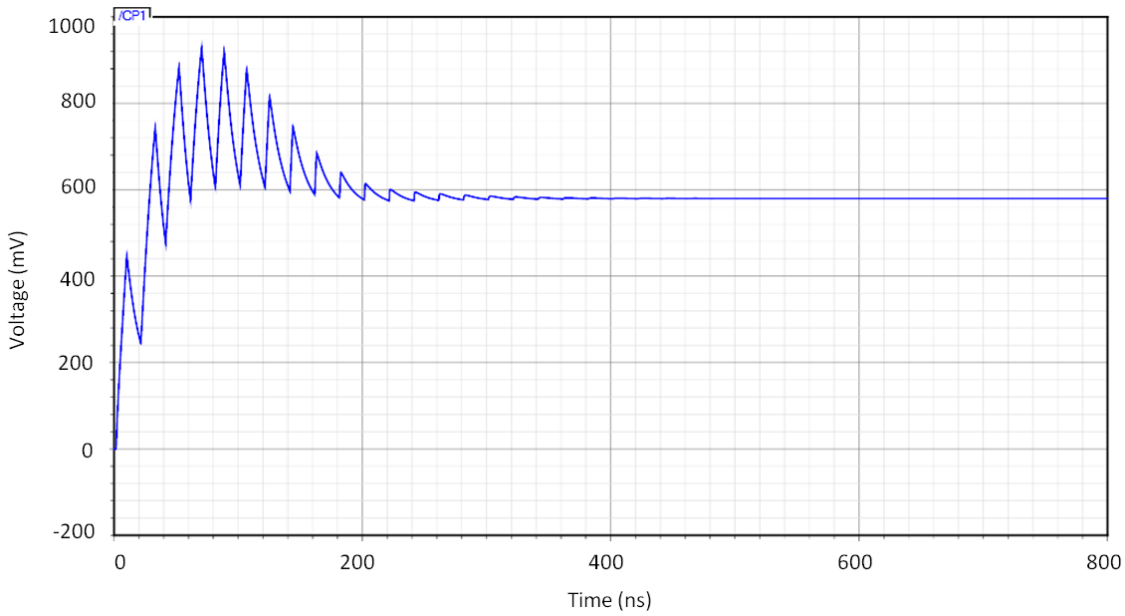


Figure 4-1. PLL locking process in terms of VCO control voltage

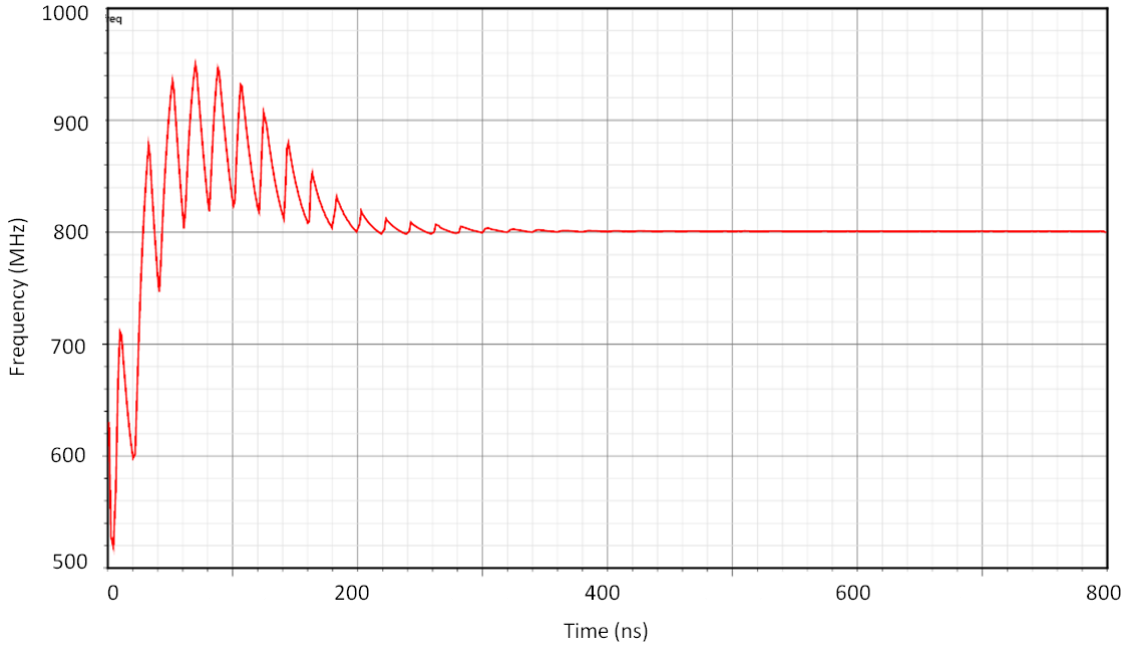


Figure 4-2. PLL locking process in terms of output frequency

The reference signal (top), feedback signal (second), VCO signal (third) and PLL output signal (bottom) at the locking state are shown in Fig. 4-3. The reference signal (*REF*) and feedback signal (*FB*) are synchronized at the locking state with operation frequency 50MHz. The VCO output has a voltage swing of 0.9 mV. One can also observe that the time for 1 period of feedback signal is equal to 16 periods of PLL output clock, which indicates the frequency of PLL output clock is 800MHz.

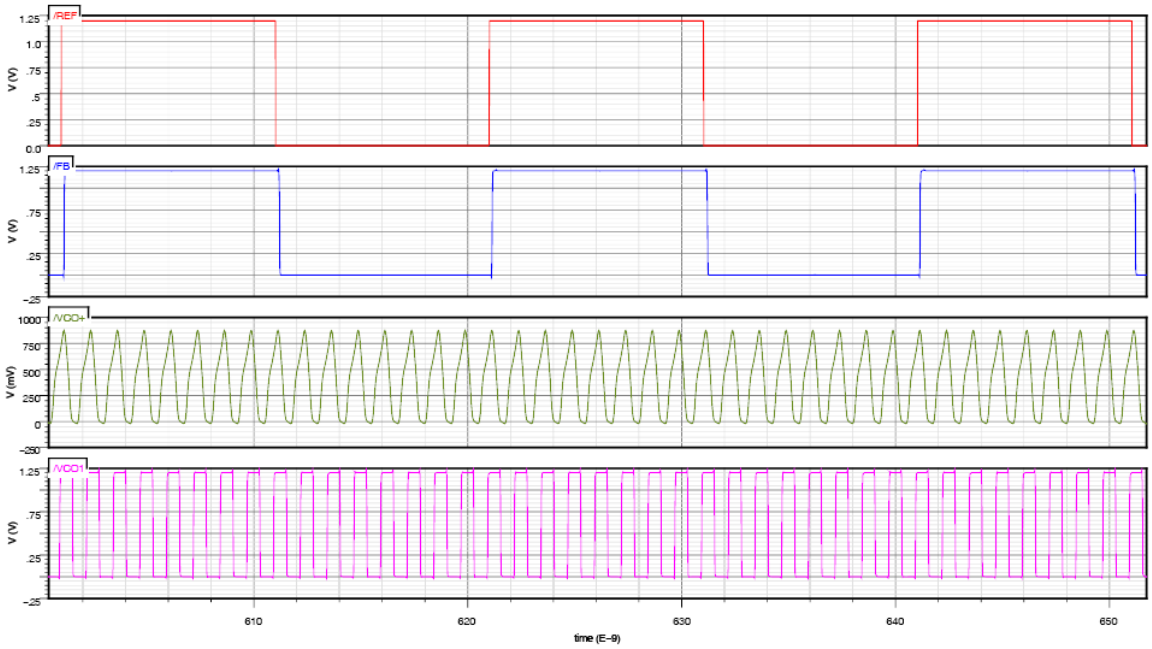


Figure 4-3. PLL input & output signals at locking state

The power consumption of the PLL is shown in Fig. 4-4. The peak power during the acquisition process is around 4.4mW, which is due to the VCO frequency overshoot. At locking state, the average PLL power consumption is 2.6mW with certain range of fluctuation. The main reason of the fluctuation is that transistors in VCO alternately turn ON and OFF due to oscillation.

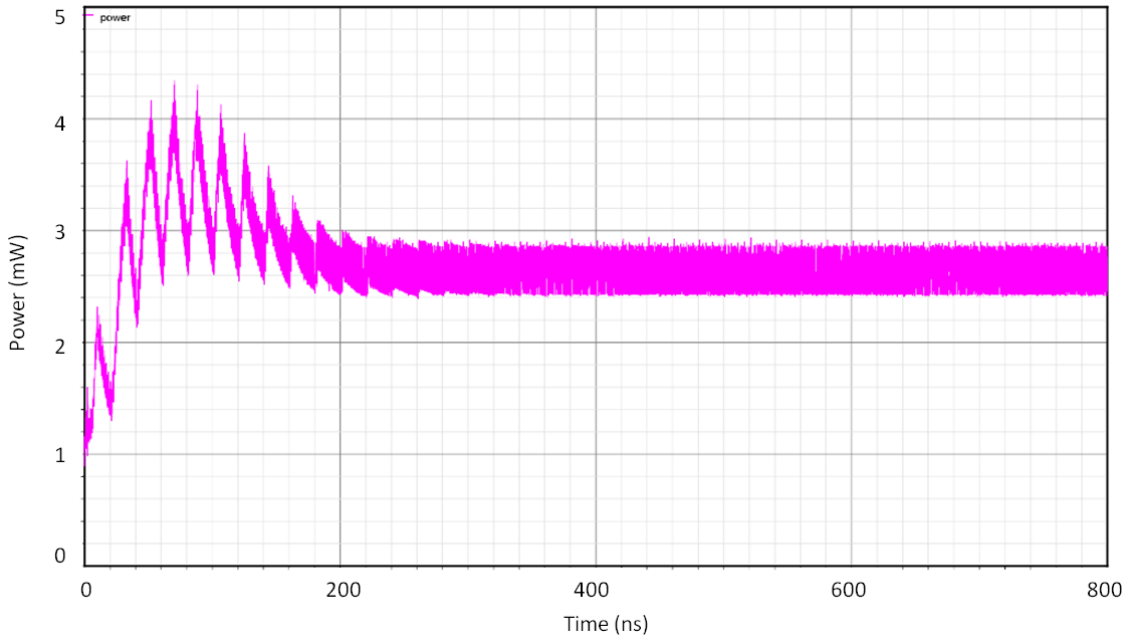


Figure 4-4. PLL power consumption

4.2 Process Corner and Temperature Variations

To check the robustness of the PLL system, the design has been simulated in presence of process corner and temperature variations. The process corners that have been considered are Fast PMOS - Fast NMOS (FF), Typical PMOS - Typical NMOS (TT), Slow PMOS – Slow NMOS (SS) corners. Fig. 4-5 and Fig. 4-6 show the locking process for the PLL at FF and SS corners. Comparing to the TT corner (Fig. 4-2), the locking time at FF corner is approximately same as TT corner; whereas the SS corner has a slower acquisition process. The reason is mainly due to the loop filter is optimized for TT corner. The design has also been simulated for temperature at 80°C, and the locking process is shown in Fig. 4-7.

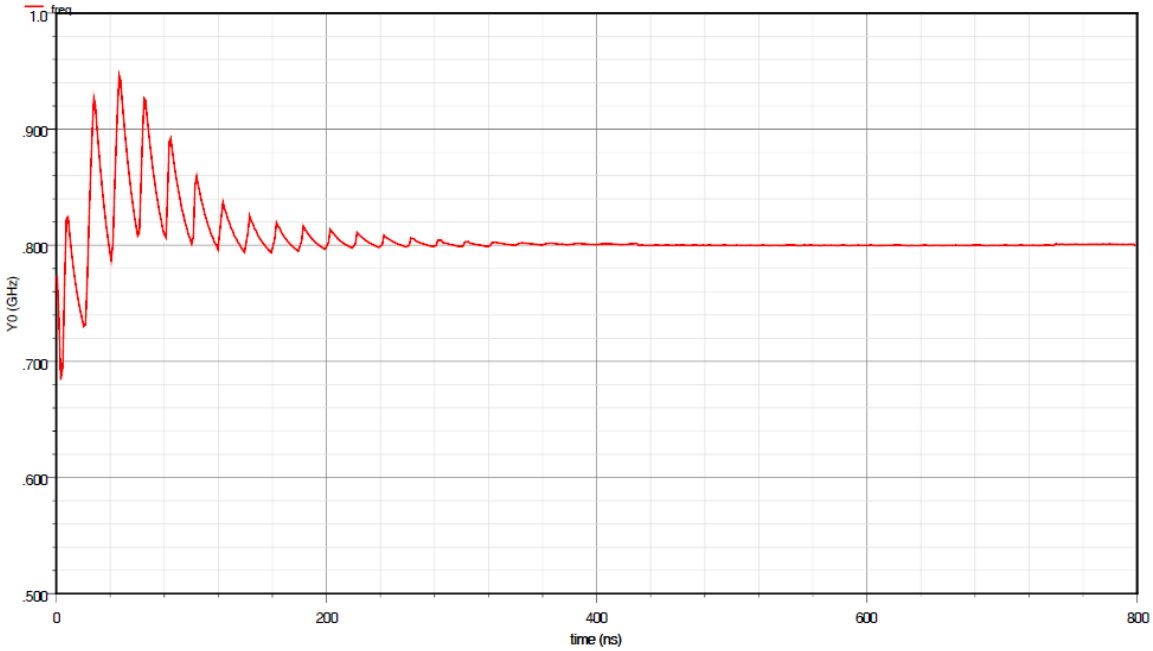


Figure 4-5. Locking process for FF corner

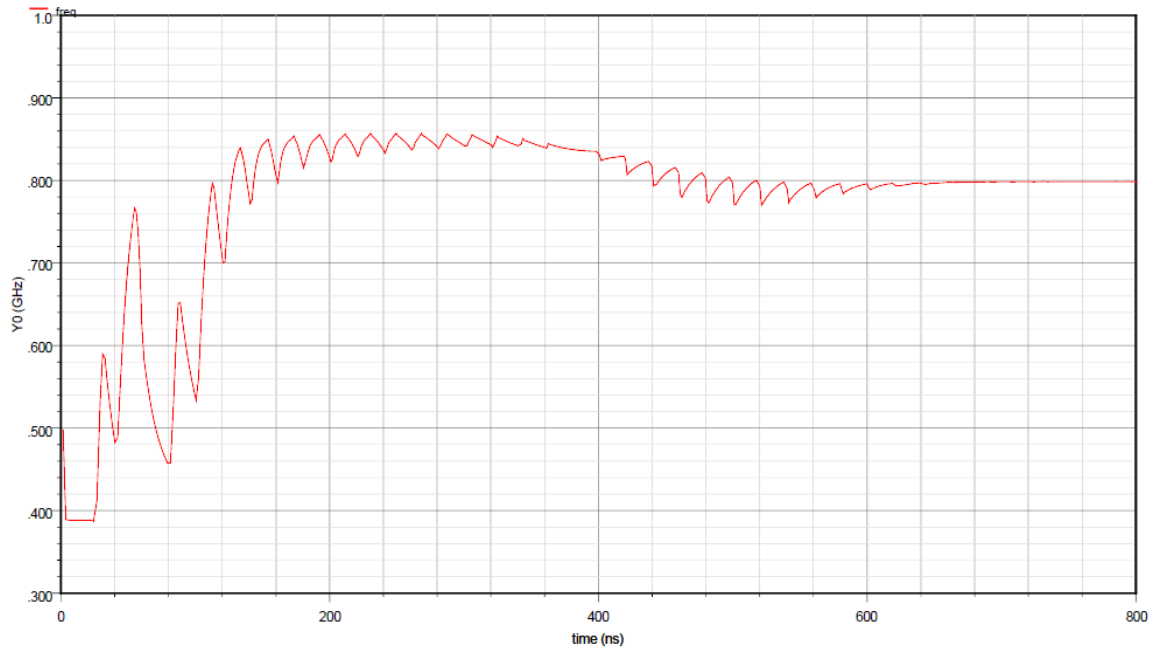


Figure 4-6. Locking process for SS corner

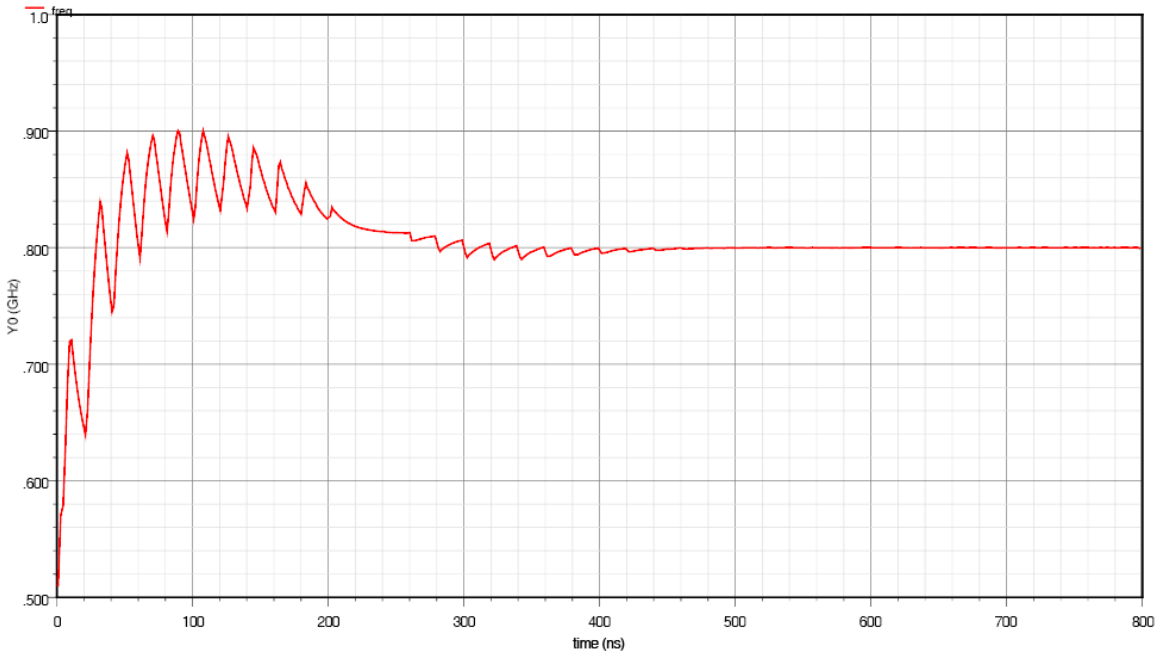


Figure 4-7. Locking process for temperature at 80°C

The PLL performance in presence of process corner and temperature variation has been summarized in Tab. 4-1.

Table 4-1. PLL performance comparison for corner and temperature variation

	Locking Time	Power Consumption
TT	400 ns	2.6 mW
FF	420 ns	2.2 mW
SS	640 ns	3.1 mW
80°C	450 ns	2.7 mW

4.3 Noise Simulation

It is difficult and time consuming to simulate the entire PLL system noise. The common method to predict PLL noise is to simulate the noise of individual components and combine them together by noise transfer functions as discussed in Section 2.5.

Based on the noise analysis in Section 2.5.4 and the noise simulation results of individual building blocks (Fig. 3-22 for PFD+CP, Fig. 3-33 for VCO and Fig. 3-39 for frequency divider), the contribution of noise from each building block to the PLL system can be derived.

The noise contribution of VCO to PLL is

$$\begin{aligned}\theta_{pll,vco,n} &= \theta_{vco,n} \cdot \frac{1}{1+G(j\omega)H(j\omega)} \\ &= \theta_{vco,n,dBc} + 20\log_{10}\left(\frac{1}{1+G(j\omega)H(j\omega)}\right)\end{aligned} \tag{4.1}$$

in which $\theta_{vco,n,dBc}$ is the phase noise of VCO that was obtained using SpectreRF (Fig. 3-33).

The noise contribution of PFD paired with CP to PLL is

$$\begin{aligned}\theta_{pll,pfd-cp,n} &= i_{cp,n} \cdot \frac{Z(j\omega)}{1+G(j\omega)H(j\omega)} \frac{K_{vco}}{j\omega} \\ &= i_{cp,n,dB} + 20\log_{10}\left(\frac{Z(j\omega)}{1+G(j\omega)H(j\omega)} \frac{K_{vco}}{j\omega}\right)\end{aligned} \tag{4.2}$$

in which $i_{cp,n,dB}$ is the current noise of PFD paired with CP (Fig. 3-22).

Finally, the noise contribution of frequency divider to PLL is

$$\begin{aligned}\theta_{pll,div,n} &= \theta_{div,n} \cdot \left(\frac{-G(j\omega)}{1+G(j\omega)H(j\omega)}\right) \\ &= \theta_{div,n,dBc} + 20\log_{10}\left(\frac{-G(j\omega)}{1+G(j\omega)H(j\omega)}\right)\end{aligned} \tag{4.3}$$

In which $\theta_{div,n,dBc}$ is the phase noise of frequency divider (Fig. 3-39).

Therefore, the total PLL phase noise is the sum of noise contribution from each individual building blocks. The PLL phase noise and individual components noise

contribution in the loop are plotted as Fig. 4-8 using Matlab. The Matlab code is attached in Appendix D. From the plot, it can be seen that due to the high-pass response of VCO, the noise from VCO within loop bandwidth (in-band) is greatly suppressed, but it dominates PLL noise outside of the loop bandwidth (out-band). In-band noise is dominated by PFD & CP noise due to the high-pass response. The PLL noise at 1MHz offset is -119dBc/Hz.

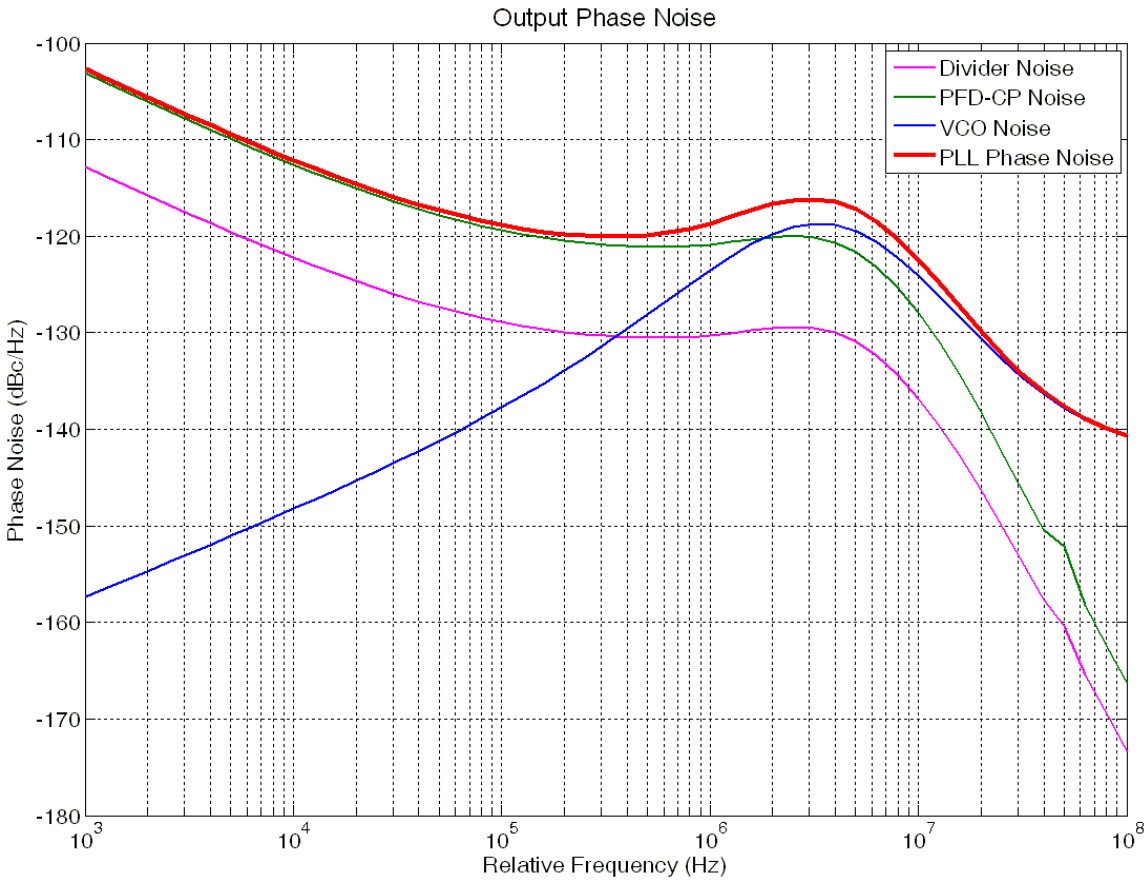


Figure 4-8. PLL phase noise

5 CONCLUSIONS AND FUTURE WORK

In this thesis, the analysis and design of a low power low noise charge-pump based Type-II 3rd order Phase-Locked Loop has been presented. To better understand the PLL dynamics, the system behavioral modeling and noise analysis have been discussed.

Blind-zone of a Phase Frequency Detector could lead to missing detection of the input clock rising edge. It is a major factor that limits the detection range of PFDs. Two novel PFDs, Delay-Input-Edge PFD (DIE-PFD) and Delay-Input-Pulse PFD (DIP-PFD) have been proposed that delay the input clock rising edge or the input clock pulse, hence the rising edge of the input clock would not be missed. Comparing it to the conventional Dynamic-Logic PFD, the proposed PFDs eliminate the blind-zone problem and extend the detection range. The circuits have demonstrated a detection range improvement in comparison to previously existing solutions.

The current mismatch is a major limitation of conventional charge pumps that could lead to noisy PLL output. A new NMOS-switch high-swing cascode charge pump has been proposed based on the existing NMOS-switch current steering charge pump. The new charge pump improved output current match and solved slow node issue which affects performance in the existing current steering charge pumps. The new design decreases the noise contribution to the PLL in comparison with the NMOS-switch current steering charge pump.

Voltage Controlled Oscillator is the most important building block in the PLL. It dominates the power consumption and the noise of the entire PLL system. A 3-stage differential VCO based on current steering amplifier has been designed in this research. The VCO frequency tuning range is 550MHz to 950MHz. At 800MHz operating frequency, the VCO power consumption is 2.5mW and phase noise at 1MHz offset frequency is -105.2dBc/Hz so that the circuit features both low-power and low-noise performance.

A Type-II 3rd order Phase-Locked Loop has been designed using IBM 0.13µm CMOS technology. The PLL generates an 800MHz clock at 50MHz input reference frequency. The loop bandwidth is 5MHz and locking time is approximately 400ns. The PLL features quite low power consumption (2.6mW) as well as low phase noise (-119dBc/Hz @ 1MHz offset). The overall PLL performance is summarized in Tab. 5-1.

Table 5-1. Overall PLL Performance

Input reference clock frequency	50 MHz
PLL output frequency	800 MHz
VCO tuning range	550MHz – 950MHz
Frequency division ratio	16
PLL loop bandwidth	5 MHz
PLL locking time	~ 400ns
VCO power consumption	2.5 mW
PLL power consumption	2.6 mW
VCO phase noise @ 1MHz offset	-105.2 dBc/Hz
PLL phase noise @ 1MHz offset	-119 dBc/Hz
Power Supply	1.2 V
Device Technology	IBM 0.13 µm CMOS

In future work, power supply regulators should be added, since the power supply noise is one of the important factors that affect the PLL noise performance. The PLL output frequency for this design is fixed at 800MHz. For modern PLL applications such as frequency synthesis and clock generation, variable output frequencies are preferred. To achieve the task, variable frequency division ratio is required and it could be realized by replacing the fixed division ratio frequency divider with a programmable frequency divider.

APPENDIX A. CALCULATION OF LOOP FILTER COMPONENT

The Matlab code to calculate the 2nd order loop filter components (Fig. 3-23) is attached in this section.

```
% Matlab code for calculating 2nd order loop filter component.
%
% Input
% ipump is the charge pump current in Amperes
% vco_gain is the VCO sensitivity in Hertz/Volt
% fout is the output frequency in Hertz
% fref is the reference frequency in Hertz
% bandwidth is the open loop bandwidth in Hertz
% phase_margin is the phase margin in degrees

% Output
% c is the capacitors of the loop in Farads
% r is the resistors of the loop in Ohms

%% Design Parameters
ipump = 80e-6;
vco_gain = 510e6;
fref = 50e6;
fout = 800e6;
bandwidth = 5e6;
phase_margin = 56;

% Conversion of parameters
Kpd = ipump/2/pi; % phase detector gain
Kvco = vco_gain*2*pi; % vco gain
omega = 2*pi* bandwidth; % open loop bandwidth in radians/sec
N = fout/fref; % division ratio
pm = phase_margin*pi/180; %phase margin in radians/sec

%% Find T1 and T2
T1 = (sec(pm)-tan(pm))/omega;
T2 = 1/(omega*(sec(pm)-tan(pm)));

%% Solving for Loop Components
C2=Kpd*Kvco/(N*omega^2)*T1/T2*sqrt((1+(omega*T2)^2)/(1+(omega*T1)^2));
C1 = C2*(T2/T1-1);
R1 = T2/C1;
```

APPENDIX B. BEHAVIORAL MODELING OF THE PLL

This section illustrates the Matlab code for behavioral modeling of the type-II 3rd order PLL loop. The code generates the Bode plots of the PLL and a step response which could be used to approximate the PLL locking response.

```
% Behavioral modeling of type-II 3rd order PLL loop
%
% Input
% c is the capacitors of the loop in Farads
% r is the resistors of the loop in Ohms
% ipump is the charge pump current in Amperes
% vco_gain is the VCO gain in Hertz/Volt
% fout is the output frequency in Hertz
% fref is the reference frequency in Hertz

%% Setup Parameters
C1 = 75.107e-12;
C2 = 7.7442e-12;
R1 = 6.931e3;
ipump = 80e-6;
vco_gain = 510e6;
fref = 50e6;
fout = 800e6;

% Conversion of parameters
Kpd = ipump/2/pi; % phase detector gain
Kvco = vco_gain*2*pi; % vco gain
N = fout/fref; %division ratio

%% Filter Transfer Function
s = tf('s');
num = [0 R1*C1 1];
den = [R1*C1*C2 C1+C2 0];
flt = tf(num,den);

%% VCO Transfer Function
Gvco = Kvco/s;

%% Forward Path Transfer Function
G = Kpd*Gvco*flt;

%% Open Loop Transfer Function
OL = G/N;
```

```
%% Open Loop Bode Plot
P = bodeoptions;
P.Grid = 'on';
P.FreqUnits = 'Hz';
figure;
bodeplot(OL,'r',P);hold on
margin(OL);
%title('Open-Loop Bode Diagram');

%% Closed Loop Transfer Function
CL = feedback(OL,1);

%% Closed Loop Bode Plot
P = bodeoptions;
P.Grid = 'on';
P.FreqUnits = 'Hz';
figure;
bodeplot(CL,'r',P);hold on
title('Closed-Loop Bode Diagram');

%% Step Response
figure;
step(CL,3e-6);
title('Loop Step Response');
```

APPENDIX C. NOISE TRANSFER FUNCTION MODELING OF THE PLL

This section shows the Matlab code to generate the Bode plots for the noise transfer functions of the type-II 3rd order PLL (Fig. 2-22).

```
% Noise transfer function modeling of type-II 3rd order PLL loop
%
% Input
% c is the capacitors of the loop in Farads
% r is the resistors of the  loop in Ohms
% ipump is the charge pump current in Amperes
% vco_gain is the VCO gain in Hertz/Volt
% fout is the output frequency in Hertz
% fref is the reference frequency in Hertz

%% Setup Parameters
C1 = 7.661e-12;
C2 = 7.9e-13;
R1 = 13.59e3;
ipump = 80e-6;
vco_gain = 510e6;
fref = 50e6;
fout = 800e6;

% Conversion of parameters
Kpd = ipump/2/pi; % phase detector gain
Kvco = vco_gain*2*pi; % vco gain
N = fout/fref; %division ratio

%% Filter Transfer Function
s = tf('s');
num = [0 R1*C1 1];
den = [R1*C1*C2 C1+C2 0];
flt = tf(num,den);

%% VCO Transfer Function
Gvco = Kvco/s;

%% Forward Path Transfer Function
G = Kpd*Gvco*flt;

%% feedback Transfer Function
FB = 1/N;

%% Open Loop Transfer Function
OL = G*FB;
```

```
%% VCO noise Transfer Function
Hvco = 1/(1+OL);

%% PFD_CP noise Transfer Function
Hpfd = -flt*Gvco/(1+OL);

%% DIV noise Transfer Function
Hdiv = G/(1+OL);

%% VCO noise Transfer Function Bode Plot
P = bodeoptions;
P.Grid = 'on';
P.FreqUnits = 'Hz';
figure;
bodeplot(Hvco,P);hold on

%% PFD_CP noise Transfer Function Bode Plot
bodeplot(Hpfd,P);hold on

%% DIV noise Transfer Function Bode Plot
bodeplot(Hdiv,P);hold on
title('Noise Transfer Function');
```

APPENDIX D. PHASE NOISE MODELING OF PLL

The Matlab code to estimate the total PLL phase noise is illustrated in this section. The code reads noise output file that generated from SpectreRF and generates the noise profile that is shown in Fig. 4-5.

```
% Matlab code for estimating total PLL phase noise

% Input
% c is the capacitors of the loop in Farads
% r is the resistors of the  loop in Ohms
% ipump is the charge pump current in Amperes
% vco_gain is the VCO gain in Hertz/Volt
% fout is the output frequency in Hertz
% fref is the reference frequency in Hertz
% div_pn is divider phase noise profile (from SpectreRF)
% pfd_pn is PFD & CP current noise profile (from SpectreRF)
% vco_pn is VCO phase noise profile (from SpectreRF)

% Read noise simulation result from individual components
[f,div_n]=textread('div_pn.txt','%f%f');
[f1,pfd_n]=textread('pfd_pn.txt','%f%f');
[f2,vco_n]=textread('vco_pn.txt','%f%f');

w=2*pi*f; %f is the frequency step read from noise file

%%%% PLL Parameters %%%%
C1 = 7.661e-12;
C2 = 7.9e-13;
R1 = 13.59e3;
ipump = 80e-6;
vco_gain = 510e6;
fref = 50e6;
fout = 800e6;

% Conversion of parameters
Kpd = ipump/2/pi;      % phase detector gain
Kvco = vco_gain*2*pi; % vco gain
N = fout/fref;         %division ratio

% Filter Transfer Function
flt=(R1*C1*(1i*w)+1)./(R1*C1*C2*(1i*w).^2+(C1+C2)*(1i*w));

% VCO Transfer Function
Gvco = Kvco./(1i*w);
```

```
% Calculate the Loop Transfer Functions
G = Kpd*Gvco.*flt;  %forward gain
FB = 1/N;      % feedback gain
OL = G*FB;  %open loop gain
H = G./(1+OL);  % clos loop gain

% plot close loop Transfer function
figure;
semilogx(f,20*log10(abs(H)));
title('Closed-Loop Transfer Function');
grid ON;

% plot open loop Transfer function
figure;
semilogx(f,20*log10(abs(OL)));
title('Open-Loop Transfer Function');
grid ON;

%%%% Divider phase noise
PN_out_div = div_n + 20*log10(abs(H));

%%%% PFD & CP phase noise
PN_out_pfd = pfd_n + 20*log10(abs((flt.*Gvco)./(1+OL)));

%%%% VCO phase noise
PN_out_vco = vco_n + 20*log10(abs(1./(1+OL)));

%%%% Total output phase noise
PN_out =
10*log10(10.^(PN_out_div/10)+10.^(PN_out_pfd/10)+10.^(PN_out_vco/10));

figure;
grid ON;
semilogx(f,PN_out_div, f,PN_out_pfd, f,PN_out_vco, f,PN_out);
title('Output Phase Noise');
xlabel('Freq (Hz)');
ylabel('Phase Noise (dBc)');
text(2e4,-140, ['Phase noise at 1MHz = ',num2str(PN_out(31))]);
axis([min(f),max(f),min(PN_out),max(PN_out)]);
axis 'auto y';
```

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