ELECTROMIGRATION PHENOMENA IN 0.13 MICRON COPPER INTERCONNECTS

by

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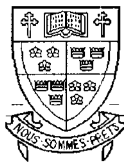

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Abstract

Cu/low-k interconnects have replaced many Al interconnects recently in Integrated Circuits with 0.13 μm technology and beyond. These technologies confine many recent fabrication processes, such as Chemical Mechanical Polishing with dual-damascene Cu electrodepositing, new materials and via processes. This thesis focuses on new reliability challenges that have developed with the changes in materials and processes. In particular, electromigration dominates the failure mechanisms in interconnects. We report an unusual circuit failure mode induced by short-lived extrusions observed during DC and bidirectional electromigration tests. This novel "soft" failure mode consists of extrusions forming, then self-dissolving before the traditional permanent void or extrusion failure. These failures shorten the lifetime significantly and bring new challenges to reliability tests. Two self-dissolution mechanisms under DC test conditions are discussed and extrusion shape evolution is modeled assuming both capillary and electron wind forces are present. Our model confirms that the electrical stress will accelerate the shape evolution process.

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Chapter 1

Introduction and Background

Reliability is key to success in the microelectronics industry, as important as performance. Integrated Circuits (ICs) must not only perform as desired, but also work for sufficient time without failure or loss of speed, typically for 10 years or more. In addition, reliability must be maintained as design complexity increases. As Very/Ultra Large Scale Integration (VLSI/ULSI) technology develops, the interconnect is becoming the dominant factor determining system performance and power dissipation [1]. Electromigration accompanied by stress-induced effects is limiting the lifetime and the maximum current density in today's ICs. Since the year 2000, when copper (Cu) metallization started to replace aluminium (Al) in interconnects, new materials and fabrication processes have created new reliability problems. New electromigration failure modes and phenomena have been widely reported, including permanent extrusions and global thinning failures.

Electromigration has become an inherent "associate" of IC design and manufacture ever since the first IC failure was attributed to it[2]. In short, it is the result of the momentum exchange between conducting electrons and diffusing metal atoms. It is always combined with stress-induced effects both mechanical and thermal. Hillocks (extrusions) and voids are common electromigration phenomena. Generally, hillocks

form where atoms accumulate and they may cause short circuit failures if they connect to neighboring metal lines. Meanwhile, voids form in regions where atoms are depleted and contribute to a rise in resistance. As voids grow and coalesce together, resistance increases and open circuit failures may be generated. Examples can be found in references [3] and [4].

1.1 Classical Electromigration Physics

1.1.1 Electromigration Mechanisms

1.1.1.1 Driving Force

In a strong current, electron drift results in many collisions with metal atoms, like a wind blowing through the conductor. Electromigration is driven by this electron wind force, F_e, and the resulting atomic flux can be expressed rather simply as [5, 6]:

$$J_{flux} = nv_e = n\frac{D_{eff}}{kT}F_e \quad , \tag{1.1}$$

where v_e is the atomic transport velocity, n is the density of atoms ($/cm^3$) which are diffusing with effective diffusivity, D_{eff} (there are various diffusion mechanisms), T is the absolute temperature, and k is the Boltzmann constant. F_e is the electromigration driving force which can be characterized by the expression [5]

$$F_e = Z^*eE = Z^*e\rho I \quad , \tag{1.2}$$

where E is the electric field, e is the magnitude of an electron charge, Z^* is the effective charge value, ρ is the electrical resistivity, and I is the current.

1.1.1.2 The Blech Effect

Another transport mechanism opposes electromigration called atomic back-flow, and happens in metal conductors due to the electromigration-induced stress gradient

(Blech effect) [7]. Electromigration depletes the cathode and accumulates atoms near the anode, inducing a net volume contraction and expansion, respectively. As a result, the gradient in atomic density will drive atoms back to the cathode. This "back-stress" driving force can be simply presented as [8]:

$$F_b = \nabla\mu = -\nabla\sigma\Omega \qquad , \tag{1.3}$$

where μ is the chemical potential (or free energy difference) between the cathode and anode, Ω is the atomic volume and σ is the stress which is normal to the diffusion path.

Combined with Equation 1.1, the net flux is [9]:

$$J_{net} = nv_{net} = n(v_e - v_b) = n\frac{D_{eff}}{kT}(Z^*e\rho J - \frac{\partial\sigma\Omega}{\partial x}) \qquad , \tag{1.4}$$

where x represents the electromigration direction. It is interesting to note that a critical value β can be obtained from Equation 1.4 when $J_{net} = 0$ [9].

$$\beta = jL_c = \frac{\triangle\sigma\Omega}{Z^*e\rho} \qquad , \tag{1.5}$$

where j is the given current density and L_c is defined as the Blech Length. This deduction reveals that electromigration will only happen when the driving stress is beyond a critical product of current density and metal conducting length. Otherwise, the back-stress flux is able to balance the electromigration flux and the conductor will not fail. This phenomenon has already been widely observed and acknowledged [10, 11].

The above discussion has covered the classical theory of electromigration. It is applicable to both Al and Cu interconnects. However, some other issues need to be considered for Cu systems due to interfacial effects. These will be discussed in Sections 1.2 and 4.1.

1.1.1.3 Diffusion

Several types of diffusion mechanisms are possible in metal lines: bulk diffusion, grain-boundary diffusion, dislocation diffusion, and interfacial / surface diffusion. Each is thermally activated with a diffusion coefficient D given by [16]:

$$D = D_0 \exp(\frac{-E_a}{kT}) \quad , \tag{1.6}$$

where E_a is the activation energy and D_0 is a pre-exponential factor that both depend on the diffusion mechanism. For crystalline materials including Cu, E_a(bulk)>E_a(grain boundary)>E_a(interface/surface) [13]. This fact determines that at a low temperature compared to the bulk melting point, interface/surface diffusion dominates the electromigration in general. If temperature increases, the difference in the exponential term in Equation 1.6 will be reduced, so grain boundary diffusion becomes comparable to surface diffusion. In addition, at a fairly high temperature, typically greater than half of the melting point, bulk diffusion becomes the major mechanism because of its large cross-sectional area. Reference [17] provides evidence for this conclusion.

The effective diffusivity of atoms in interconnects is defined as [12]:

$$D_{eff} = \frac{A_{gb}D_{gb} + A_{bulk}D_{bulk} + A_{int}D_{int} + A_{dis}D_{dis}}{A_{gb} + A_{bulk} + A_{int} + A_{dis}} \quad , \tag{1.7}$$

where the A variables are the relative cross-sectional areas of grain boundary, interface/surface, lattice and dislocation diffusion as denoted in the subscripts.

Although bulk diffusion occupies a quite large cross-sectional area, it can still be neglected under typical low T conditions of test and service due to a high activation energy. Dislocation diffusion has a similar activation energy to grain boundary and interfacial diffusion, however, it is also ignored in general cases because the cross-sectional area of a single dislocation is small [12].

Many interfaces between metals and dielectrics are in significant disorder. Therefore, a relatively high diffusivity can exist there. This is true for Cu interconnects where particularly, the surface has the highest diffusivity compared to any other diffusion paths [12]. It is important to note that the quality of interfaces is fairly sensitive to fabrication variations, which is part of the reason why capping layers in Cu interconnects affect electromigration lifetimes dramatically [13, 14].

Grain boundaries are regions of disorder between misoriented crystals. Thus, the diffusional activation energy, E_a, is rather small and the diffusivity is high. Grain boundaries and metal/dielectric interfaces can have similar effective diffusivities [15]. Generally, grain boundary diffusion is the primary mechanism in Al interconnects while interfacial diffusion dominates Cu interconnects. Extensive research has already confirmed that electromigration lifetime can be improved notably by removing the principal diffusion path [6]. Reference [14] reports that only bulk-like diffusion exists in the Cobalt Tungsten Phosphide (CoWP) capped Cu interconnects where the top surface diffusion of Cu is minimized.

1.1.2 Black's Law

The most common method of predicting the median time to failure (MTF) t_{50}, as a function of temperature T and current density J, is through the use of Black's law [18]:

$$t_{50} = \frac{A}{J^n} \times \exp(\frac{E_a}{kT}) \quad , \tag{1.8}$$

where t_{50} is a statistical quantity at which time 50% of samples tested have failed, n is the current density exponent (typically, $n = 1 \sim 2$), E_a is the activation energy of the dominant diffusion process, and A is a material and geometry-dependent constant[17,

18].

The lifetime of an IC (t_1) under one test condition (J_1 and T_1) can be extracted with the t_{50} of accelerated electromigration tests under different conditions (J_{acc} and T_{acc}) through the following equation:

$$t_1 = t_{50}\frac{(J_{acc})^n}{(J_1)^n} \times \exp(\frac{E_a}{k}(\frac{1}{T_1} - \frac{1}{T_{acc}})). \tag{1.9}$$

This equation is a simple model and very sensitive to test conditions and parameters. An accurate knowledge of n and E_a is vital to extrapolate the lifetime correctly. For example, as n varies over the common range of $1 \sim 2$, the extrapolated lifetime changes by 45 times in some cases [5]. Generally, E_a is determined by the dominant diffusion process and n depends on the failure mechanisms.

There are two void failure mechanisms in interconnects, nucleation-dominated and growth-dominated failures. For extrusion failures, the mechanism also involves a void formation process or is related to dielectric failure. In the case where only void failures are present, the total time to failure, t_f, can be considered as two parts:

$$t_f = t_i + t_g \qquad [19], \tag{1.10}$$

where t_i is the incubation or void nucleation time and t_g is the period for an initial void to grow to the final failure.

The void failures in a system without surrounding refractory layers, are nucleantion-dominated. In this case, electromigration generates a gradient of mass density along the metal line. Thus, a high stress accumulates in the system. Meanwhile, vacancies aggregate at high energy sites, such as dislocations and grain boundaries in the crystal. Whenever a critical vacancy concentration is reached, a void will form and a tremendous release of strain energy will take place. This can further

accelerate the growth of the void and an open circuit failure happens in a short period. In this situation, t_i dominates the total time to failure and n = 2 in Black's law, following $1/j^2$ kinetics. This result can be deduced from the vacancy continuity equation and has already been confirmed by many experiments [2, 19, 20, 21].

With the implementation of a refractory interfacial layer, such as the diffusion barrier in Cu interconnects, the void failure rate is determined by void growth time, and t_g is the major part of the t_f. In this situation, the refractory layer is able to provide an extra pathway for conducting electrons when voids exist in the primary conductor. Because of that, the growth of voids is relatively slower than in the pervious case and open circuit failure will be less likely to happen. Nevertheless, significant resistance increase will still be observed, which can cause failure. (For instance, a 10% change will lower the frequency limit of the circuit and produce timing errors[22].) Since void growth is due to the flux divergence of vacancies and atoms, which depends linearly on current density (Equation 1.1 and 1.2), this failure formation process will follow 1/j kinetics[20, 82].

The void failure mechanism of an actual interconnect is a mixture of nucleation dominated and growth-dominated failures. Often, as might be expected, the behavior is complicated and cannot be described by a simple power law in J [22] [20].

Generally speaking, Black's law is able to describe t_{50} as the function of temperature and current density. On the other hand, the microstructure is also a critical issue, perhaps the most important one. It can affect the values of quantities in the Black equation, such as E_a and n. Moreover, both the strength of the crystallographic texture and the composition of metal conductors have effects on the lifetime [4, 15].

1.1.3 Joule Heating

Joule Heating causes thermal stress-induced problems and it exists in all electromigration tests. When current passes metal lines, thermal energy will be generated as a result of the collision between carriers and metal atoms. Such behavior is Joule Heating. If the current is low, generated thermal energy will be conducted out immediately. However, at fairly high current densities, such as $1MA/cm^2$, heating occurs and temperature gradients as high as $10^4 \sim 10^5$ °C/cm are easily found in ICs[22]. Since diffusion depends exponentially on the temperature, such high thermal gradients will cause significant atomic flux divergences, meaning the depletion of metal atoms and the appearance of hillocks.

The flux induced by a thermal gradient can be represented as [23]

$$J_{thermalflux} = n\frac{D_{eff}}{kT}F_{thermal} \propto \frac{dT}{dx}exp(\frac{-E_a}{kT}) \quad , \tag{1.11}$$

where $F_{thermal}$ is the thermal driving force and x indicates the migration direction. Figure 1.1 shows a typical situation: a constant current passes a non-uniform metal line. The flux to the left and right of the dash lines is different due to different local Joule heating. Thus, a void will probably be found at the right dash line if the current flows from left to right. Similar phenomena have already been widely detected in real ICs and other reliability tests [24].

Joule heating can be estimated through the Temperature Coefficient of Resistance (TCR) in electromigration tests. The TCR, in units of relative resistance change per °C, reveals the temperature dependence of resistance and it can be determined by measuring the resistance of the test conductor at a series of temperatures and taking the slope. 0 °C or room ambient temperature is the standard reference in this

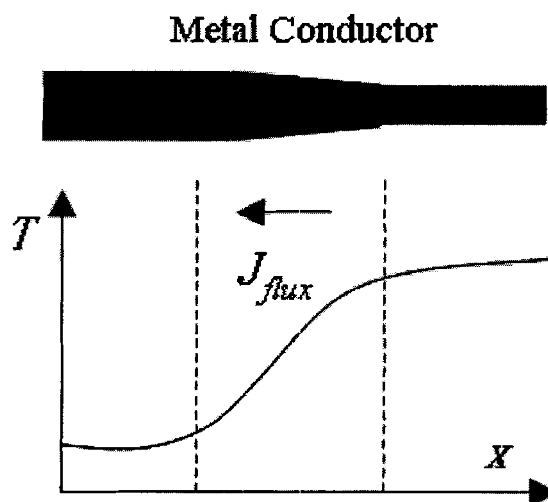


Figure 1.1: Schematic of the temperature profile along a conductor due to Joule Heating [12]

measurement (20 °C is chosen in our tests [25]) and Equation 1.12 is employed [25].

$$T_{actual} = \frac{(\frac{R_{withstress}}{R_{20}} - 1)}{TCR} + 20 \quad , \tag{1.12}$$

where R_{20} is the resistance of the test lead at 20 °C. The difference between T_{actual} and the furnace ambient temperature is the temperature increment due to Joule heating.

Black's Law cannot be used to extract the lifetime under real working conditions accurately until Joule heating effects are minimized. If Joule heating is significant, the current exponent in Equation 1.9 will be different under accelerated tests and real working conditions. In electromigration tests, if the actual temperature T is too much higher than the ambient temperature and cause an unexpectedly shorter lifetime. This behavior results in a relatively larger n, which causes false optimism in the IC's lifetime [20] (Figure 1.2).

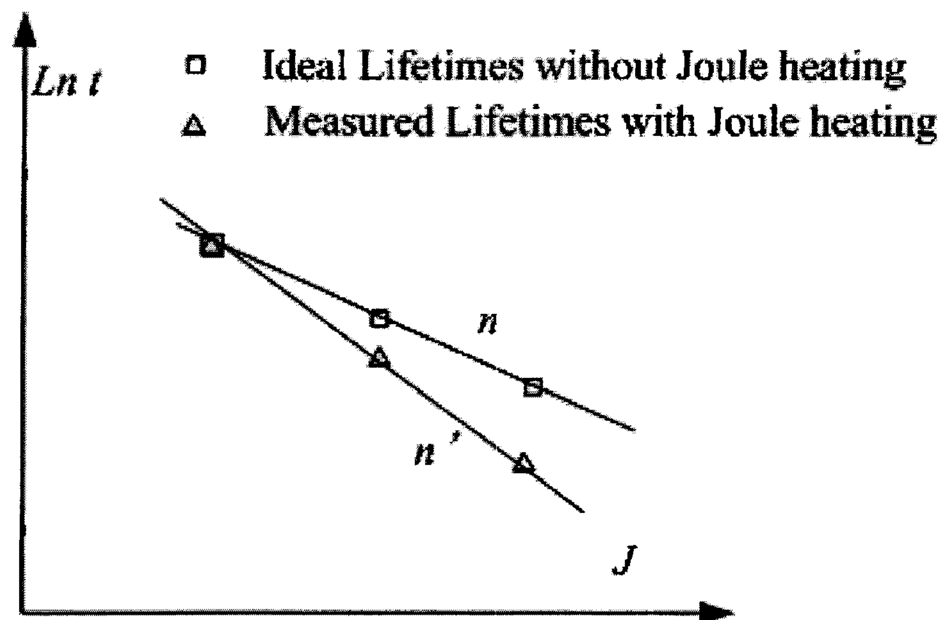


Figure 1.2: $\ln t$ versus J model curves show that Joule heating will induce an incorrect result in current component measurement.

1.1.4 Mechanisms of Pulsed-DC and AC Electromigration

Generally, the activation energy E_a and the peak current density component n in Black's Law for non-DC stress is the same as those under DC conditions. No obvious differences in the failure mechanisms and locations have been detected [26], however, the lifetime is enhanced significantly under non-DC conditions, showing a clear frequency dependence.

1.1.4.1 Pulsed-DC Conditions

Pulsed DC stress is common in real circuits. Abundant electromigration research has been conducted in this area. However, although experimental results are consistent in general, a variety of inconsistent theories were proposed [20, 26, 27, 28, 58, 60, 61, 62, 63, 64, 65]

Typically, the duty factor r is defined as the fraction of time in which the current

is flowing. For pure DC, $r = 1$. Based on the theory of J. R. Lloyd (IBM)[20], when the width of pulses is long enough, vacancies can reach their DC equilibrium concentration and an atomic gradient is built up during the on-time period [27]. It is true that during the current-off period, such atomic gradients can bring relaxation to the test structure. However, in most cases, since the structure is much longer than the Blech length, this relaxation is insignificant compared to the electromigration stress in the stress-on phase. Therefore, within the low frequency range, pulsed DC stress can be considered as DC periods interlaced with off-periods. The lifetime t_{50} depends on the root mean square (RMS) current density, called the RMS mode, as in Equation 1.13.

$$t_{50} = \frac{1}{rJ^n} \exp(\frac{E_a}{kT}) \qquad [20]. \tag{1.13}$$

Within a high frequency range, particularly, if the frequency is higher than the jumping frequency of a vacancy (for example, 10 kHz in Al alloys at 100 °C [20]), neither can the system respond to the current change dynamically, nor can vacancies set up DC equilibrium in such a short period [27]. Meanwhile, atoms cannot react to the stress on and off periods and only feel an average current density, rJ. In this circumstance, the lifetime observed follows Equation 1.14 (the average current density mode) [20].

$$t_{50} = \frac{1}{(rJ)^n} \exp(\frac{E_a}{kT}) \qquad . \tag{1.14}$$

Various transition frequencies between these two modes have been reported. Typically, it ranges from 100 Hz to 100k Hz and it changes with the temperature, current density and material composition [28, 29]. Reference [17] provides an experimental result for the frequency dependence of the lifetime under a pulsed-dc stress condition supporting the above discussion.

1.1.4.2 AC conditions

It is easy to imagine that since the net transport is zero under pure AC stress conditions, there should be no electromigration. However, this assumption is too simple.

Figures in reference [30] have revealed that in both Al and Cu interconnects, if the frequency is less than a critical $f_0 = 1/2(MTF_{dc})$, the interconnect will follow DC electromigration behavior. In this situation, the system fails even before the onset of the reverse current. When frequency is beyond f_0, a gradual enhancement in MTF happens along with the frequency increment. There is a widely held belief that such a phenomenon results from the improved effectiveness of damage healing during the reverse stress period. According to this theory, at the beginning of positive and negative pulses, atoms and vacancies start to migrate along grain boundaries or interfaces. This migration is able to recover with the opposing stress. A shorter stress period means a relatively smaller displacement of atoms and vacancies, which is easy to be healed. Therefore, the lifetime can be improved along with the increase of frequency. Moreover, within a quite high frequency range, the damage healing process can overcome all defects which are brought during the other half period. So there should be no electromigration at all and the MTF should go to infinity. However, in fact, an interconnect is never immortal. Thermal stress alone is able to induce significant temperature gradients as discussed before. This temperature gradient brings flux divergences and causes the failure without electromigration stress. In this situation, Joule heating sets the lifetime limit based on the RMS current density and this conclusion is supported in the literature [30]. In addition, it is important to emphasize that if a high frequency AC current density has a DC offset, the DC component will determine the actual electromigration lifetime [20].

Based on the above theory, at a relatively high frequency, the lifetime of interconnects follows [26]:

$$t = \frac{A}{(J_+ - mJ_-)^n}\exp(\frac{E_a}{kT}) \quad , \tag{1.15}$$

where m is the effectiveness of damage healing during the reverse stress period improved with increase in frequency [23].

$$m = 1 - 2(\frac{f_0}{f})^{1/n} \quad , \tag{1.16}$$

where f_0 is the transition frequency between low frequency and high frequency ranges. Furthermore, Equation 1.17 predicts the frequency dependence of AC lifetimes in ICs [31].

$$MTF_{AC} = 2 \times f \times (MTF_{DC})^2 \propto \frac{f}{J^{2n}}\exp(\frac{2E_a}{kT}) \quad . \tag{1.17}$$

Additionally, the lifetime limit due to the thermal stress at a very high frequency can be obtained through the following equations [23]:

$$J^+_{flux} = \frac{nD}{kT}(F^+_{em} + F^+_{thermal}) \qquad J^-_{flux} = \frac{nD}{kT}(F^-_{em} + F^-_{thermal}), \tag{1.18}$$

where the "+" and "-" signs represent the forward and reverse periods, respectively. The F variables are driving forces. If m = 1, F^+_{em} can be canceled by F^-_{em} and [23]

$$J_{flux} = J^+_{flux} + J^-_{flux} = \frac{nD}{kT}F_{thermal-grad} \propto 1/(MTF_{AC}). \tag{1.19}$$

Finally, there is another issue which deserves comment. The waveform of the stress also has impact on failure rates. For example, local melting will happen and cause failures for very large peak current densities even if the RMS current density is not very high. [32].

1.2 Electromigration in Cu Interconnects

1.2.1 Cu Interconnects

1.2.1.1 The Transition from Al Interconnects to Cu Interconnects

Cu is considered a better candidate than Al in interconnects due to its physical properties. First of all, it has a much lower resistivity than Al (Table 1.1). Lower resistivity helps to reduce the RC delay and improve the working frequency. It can also assist to minimize Joule heating and shrink potential thermal flux divergences.

Secondly, Cu has an inherently larger resistance to electromigration. Table 1.1 clearly reveals that Cu has a stronger lattice and much smaller atomic diffusivity than Al. Thus, the electromigration damage in Cu interconnects is less severe than in Al interconnects. Moreover, this advantage of Cu allows a higher IC operation temperature.

Material	Resistivity	Melting Point	Diffusivity at 100 °C (cm^2/s)		
	($u\Omega cm$)	(°C)	Lattice	GB	Surface
Cu	1.67	1083	7×10^{-28}	3×10^{-15}	10^{-12}
Al	2.67	660	1.5×10^{-19}	6×10^{-11}	
Al-Cu Alloy	$3.3 \sim 3.5$				

Table 1.1: Al and Cu Properties [12, 45]

Although Cu is the desired material in interconnects due to the above two advantages, there are still some issues troubling the industry. Cu unfortunately suffers from a poor quality oxide, which is non-uniform, porous and which cannot prevent Cu atoms from entering dielectrics. Al oxide in comparison is not only extremely stable, but also adherent and continuous. In addition, as a noble metal, Cu can create

deep levels in the silicon energy band gap [12]. The induced diffusion of Cu atoms inside dielectrics to the Si is undesired and brings deadly effects to ICs. It is apparent from the above discussion, that a diffusion barrier is necessary in Cu interconnects to overcome potential reliability problems.

The ideal diffusion barrier is metallic, and can provide good adhesion to the Cu conductor so that mass transport along barriers is suppressed [34]. Titanium (Ti) and Tantalum (Ta) based barriers are common in current interconnects and nitrogen is often doped in the barrier to increase the adhesion [33][59]. Physical Vapor Deposition (PVD) is the conventional deposition method. However, Atomic Layer Deposition(ALD) has started to be implemented with the 90 nm generation technology and beyond. Engineers expect it can achieve a smaller sheet resistivity and better electromigration performance. [38]

Another challenge for Cu integration is that Cu is incompatible with Reactive Ion Etch (RIE) processes which are widely used in the conventional fabrication processes. This problem was solved by the implementation of the damascene process with Chemical Mechanical Polishing (CMP), introduced in the next section.

1.2.1.2 Dual Damascene Process

The damascene process was invented to produce planar layers and to reduce fabrication steps. Since it did not require reactive ion etching of Cu, it was applicable to Cu interconnects and soon dominated IC fabrication. The single damascene process refers to the fabrication of vias and metal lines separately, while a dual damascene process fabricates them together. Obviously, the latter is more efficient and costs less, shown in detail in Figure 1.3. In this process, trenches for vias and metal lines are made first by etching dielectrics. Then a diffusion barrier is deposited as discussed in the previous section. After that, Cu seeds are deposited by the PVD method. The Cu

vias and metal lines are then grown by electroplating which is an inexpensive process and can provide larger grains than by CVD Cu [4]. CMP is then implemented to smooth the surface and remove extra barrier materials and Cu. The achieved planar surface is not only essential for high-resolution lithography, but also enhances process margin and yield [1]. After CMP, a surface treatment is carried out and the deposition of a capping layer, which can improve the adhesion between the Inter Layer Dielectrics (ILD) and Cu underneath, and simultaneously reduces Cu surface diffusion. This dual damascene process not only succeeds in integrating Cu interconnects, but also brings some extra advantages. For example, with this technology, vias and metal lines are fabricated by the same material and so unlike W vias in Al interconnects no large flux divergence exists between them. This reduction in flux divergence increases electromigration resistance significantly. Furthermore, the dual damascene process reduces complexity by reducing the number of steps.

1.2.2 New Electromigration Behaviors in Cu Interconnects

Although traditional open circuit failure is still common in Cu interconnects, new electromigration behaviors have been widely reported with the transition in materials and fabrication processes. This section will discuss the current weaknesses in Cu dual damascene interconnects and related electromigration phenomena.

1.2.2.1 Potential Reliability Problems

The Atomic Diffusion inside Cu Conductors Atomic diffusion in Cu interconnects has been researched thoroughly. C. K. Hu's contributions (IBM) are acknowledged as the fundamental work in this area. His conclusions, combined with other literature reports, confirms that the primary diffusion mechanism is via surface diffusion (for large grain bamboo-like and near bamboo Cu conductors) with an activation

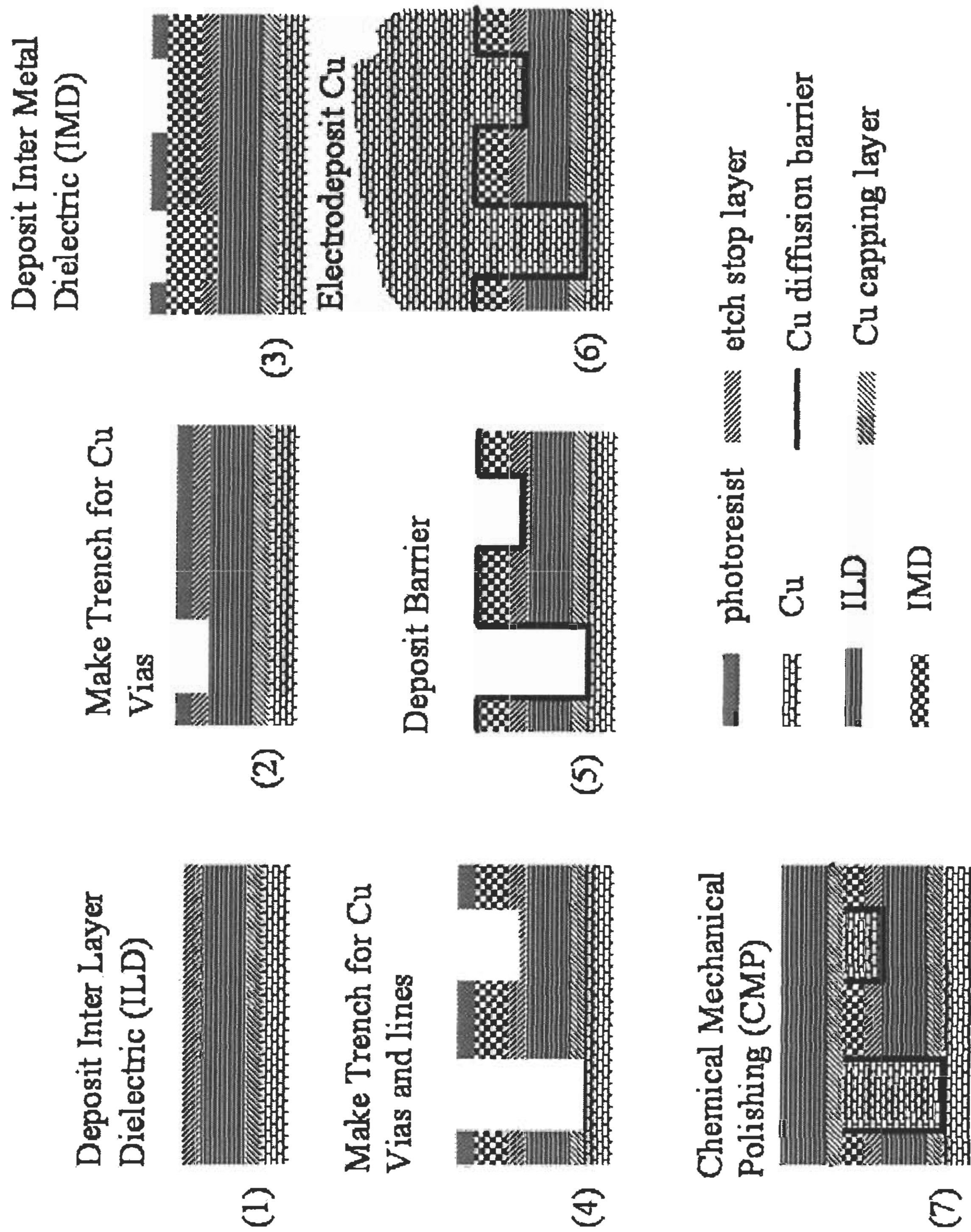


Figure 1.3: Diagram of a dual damascene process.

energy between 0.7-0.9 eV [13, 20, 24, 47]. It is also possible to observe a mixture of grain boundary and surface diffusion (in polycrystalline Cu films) where the activation energy of grain boundary diffusion is about 0.2 eV higher than surface diffusion [13].

Surface diffusion is reduced in actual ICs by depositing three sides of the Cu line on metallic diffusion barriers. However, the remaining top surface of Cu lines suffers from a dusty and moist CMP process, where some dishing and erosion are likely [46]. This damage can provide potential failure nucleation sites and deteriorates electromigration performance dramatically although an appropriate capping layer can ameliorate this problem [34](Figure 1.3).

The current density dependence in Cu electromigration tests has also been investigated. However, whether the current exponent n in Black Equation is 1, 2, or a larger number has been controversial [45]. As discussed in Chapter 1.1.2, n is suggested to be 1 because the existence of diffusion barriers reduces the grown rate of voids and t_g dominates the total lifetime. In addition, voids in Cu interconnects tend to grow laterally along the surface instead of locally to open circuit failure like in Al interconnects. This phenomenon also delays the formation of void failures by increase t_g. From this point of view, n should be 1 and C. K. Hu (IBM) has measured n = 1.1 ± 0.2 if the current density is less than 2.5 MA/cm^2 [82]. On the other hand, C. K. Hu also has observed n = 1.8, close to a j^2 power law, when the stress current density is more than 2.5 MA/cm^2. They declared that it was reasonable if the local Joule heating was taken into account [82].

Adhesion Problems Besides the CMP-related problems, adhesion in a multi-layer Cu interconnect is always a concern because Cu adhesion to dielectrics is poor. The adhesion is quantified by the total energy required to separate an interface. It can

be measured by four-point bending tests where the critical value of the interface debond energy, $G_c(J/m^2)$, or the debond strain energy release rate is determined. This energy includes two parts: the breaking of chemical bonds across the interface and plastic deformation in any adjacent ductile layers [33]. The former part relates to the activation energy of surface diffusion directly [34] and the latter can be improved by increasing the dimension of the Cu line [33, 44]. An adhesion energy of 5-10 J/m^2 is the general requirement for CMP and package compatibility [40, 42]. Interfaces with measured adhesion less than that are likely to be at a high risk of delamination. However, Cu/glass interfaces show an adhesion energy of only about 2-5 J/m^2 [37]. It is apparent that the direct contact between Cu and oxide should be avoided in interconnects and a capping layer is necessary. The capping layer can also work as a stop layer for subsequent ILD etching [41] (Figure 1.3). SiC, SiN_x, $SiCN$, and $CoWP$ are common candidates for capping material. Based on current reports, higher fractions of carbon reduces the interfacial adhesion, and selectively deposited $CoWP$ is the best solution in terms of low electromigration and good stability [14, 34, 39].

The Implementation of Low-k Dielectrics The motivation for implementing low-k dielectrics is to reduce the total capacitance of the interconnect, however, it also induces new reliability concerns.

The capacitance in interconnects consists of two parts: line-to-line cross talk capacitance and line-to-substrate capacitance [1]. According to the parallel-plate capacitance model, both of these are proportional to the dielectric constant k. This fact indicates that the reduction in k will significantly decrease the total capacitance and improve the working frequency. On the other hand, it is not easy to find a good candidate which has enough mechanical strength, good thermal stability/conductivity,

and excellent compositional and dimensional stability. Besides these, integration capability is another fundamental requirement, including sufficient adhesion to Cu and its barrier metals, compatibility with CMP and etching, and no liner or cap film requirements [43].

Currently, a Fluorinated Silicate Glass (FSG) has been found to reduce k slightly to 3.5 - 3.7 without changing the mechanical and thermal properties significantly (the standard plasma silicon dioxide has a k around 4.1). Aggressive integration techniques employ dielectrics with a k no more than 3, such as inorganic (SiO_2-based) – HSQ (Hydrogen Silsesquioxane k = 3) and organic (carbon-based) dielectrics – Silk (polyphenylene polymer k = 2.65), and Black diamond (SiOC or organosilicate glass k= 2.8). The further reduction in k (less than 2.5) can be achieved by porous inorganic or organic materials, although porosity will deteriorate physical properties and increase moisture or chemical adsorption [1].

Generally speaking, with low-k materials, the adhesion, mechanical and thermal dissipation capabilities of Inter Metal Dielectrics (IMD) and ILD deteriorate, raising more reliability problems. In particular, extrusion failures happen more frequently in Cu/low-k systems [49, 50].

1.2.2.2 New Electromigration Phenomena

Global Thinning Void failure mechanisms change in Cu interconnects. Since surface diffusion dominates the electromigration in Cu lines, voids prefer to grow laterally along the surface of Cu lines, in a large area instead of at localized points leading to catastrophic open circuit failures. This phenomenon has been characterized carefully in references [15] and [47]. As a result, resistance increases only gradually in Cu electromigration tests and open circuit failures are less likely to happen. In some cases, the whole Cu conductor separates from the barrier due to stripe-like voids, without

an open circuit failure [47]. This phenomenon is defined as Global Thinning and our group has developed a diffusional void shape evolution model to explain this behavior [48]. This model is also applicable to the discussion of temporary extrusion failures which will be introduced in this thesis.

Permanent Extrusion Failures Another important new electromigration phenomenon is the extrusion failure, which is rare in Al interconnects but common in Cu/low-k systems due to the interfacial problems discussed above [6, 20, 24, 41, 66, 67]. Some groups have recorded that nearly 46% of their samples failed by extrusions [36]. The formation process of extrusions can be explained by presenting both electromigration behavior and accumulation of mechanical stress in dielectrics.

Due to electromigration, compressive stress accumulates at the anode end of a metal conductor, inducing a large tensile stress locally in the surrounding oxide. In reference [24], two dimensional finite-element modeling (FEM) reveals that such tensile stress typically is constrained to the capping layer at the damascene top corners. Whenever the accumulated stress reaches a threshold, a crack or delamination happens. Subsequent to that, Cu atoms will extrude at both sides of damascene lines to reduce the compressive stress in the conductor and cause failure. A cartoon in reference [41] shows clearly such a process. Furthermore, the time for crack formation, t_c, is discussed in references [24] [35] and is presented as:

$$t_c = A_c T j^{-2} \exp(\frac{E_a}{kT}), \tag{1.20}$$

where A_c is a constant, j is the current density, T is the absolute temperature and E_a is the effective activation energy corresponding to the major diffusion mechanism.

Generally, an extrusion failure happens after the first void, but before the final void failure [24]. However, since several single voids cannot affect the resistance

significantly due to their strip-like shape, in many cases, t_c determines the lifetime of the sample. This is considered as the reason why extrusion failures prevail in Cu interconnects.

Equation 1.20 also indicates that the current density dependence of the lifetime will follow $1/j^2$ kinetics if extrusion failures dominate. Based on the discussion in Chapter 1.2.2.1, the author tends to adopt 2 as the current exponent in the Black Equation when the current density is relatively large or extrusions dominates the failure behavior, while 1 is taken if the stress current density is less than 2.5 MA/cm^2 and the major failure mechanism is void failure. (This issue is still controversial among engineers.)

It is important to note that due to the above two new failure modes, electromigration failure criteria have also been changing from open circuit failure in Al interconnects to a mixture of a certain percentage change in resistance (such as 10 or 20%) and the occurrence of a critical leakage current (such as 50 or 100 μA) [24, 42]. These criteria are also implemented in our electromigration tests.

All reported extrusions so far are permanent or lack any further characterization of their evolution [6, 24, 36, 41, 66, 67]. In our accelerated electromigration tests, we found extrusions that existed for only a short period and then self-dissolved, which we call temporary extrusion failures. Nevertheless, they would have deadly effects on ICs and would cause an over-estimation of lifetime if they are missed. The following chapters will characterize these interesting and important electromigration failures in detail and try to reveal their properties and self-dissolving kinetics.

Chapter 2

Experiment Design

2.1 Test Structure

Our IC wafer was fabricated by 0.13 μm Cu dual damascene technology in a leading foundry company. Since it is a commercial wafer, all fabrication processes should be mature and standard. The interconnect structure had a total of 9 metal layers. Layer 1, closed to the Si substrate, had the minimum dimension while layers 8 and 9 at the surface had the maximum feature size. Our tests were carried out on intermediate layers 2-7 which had the same structure. The thickness of each intermediate layer was 0.37 μm and the vertical space between them was 0.50 μm. Figure 2.1 shows a secondary electron scanning electron microscopy (SEM) image of the interconnect stacks. The dimension are listed in Table 2.1. All vias were composed of Cu except the plugs between metal layer 1 and the substrate, which were tungsten (W). TaN was implemented as the diffusion barrier, 40 nm in thickness. In addition, the Inter Layer Dielectrics (ILD) and Inter Metal Dielectrics (IMD) were FSG, and SiN_x was employed as both a Cu capping layer and an etch stop layer. The interconnect structure of each stack is the same as the one shown in Figure 1.3. (All of the above information was obtained from the foundry company and confirmed by cross-sectional scanning electron microscopy (XSEM) and Energy Dispersive X-Ray Spectrometry

(EDS) analysis.)

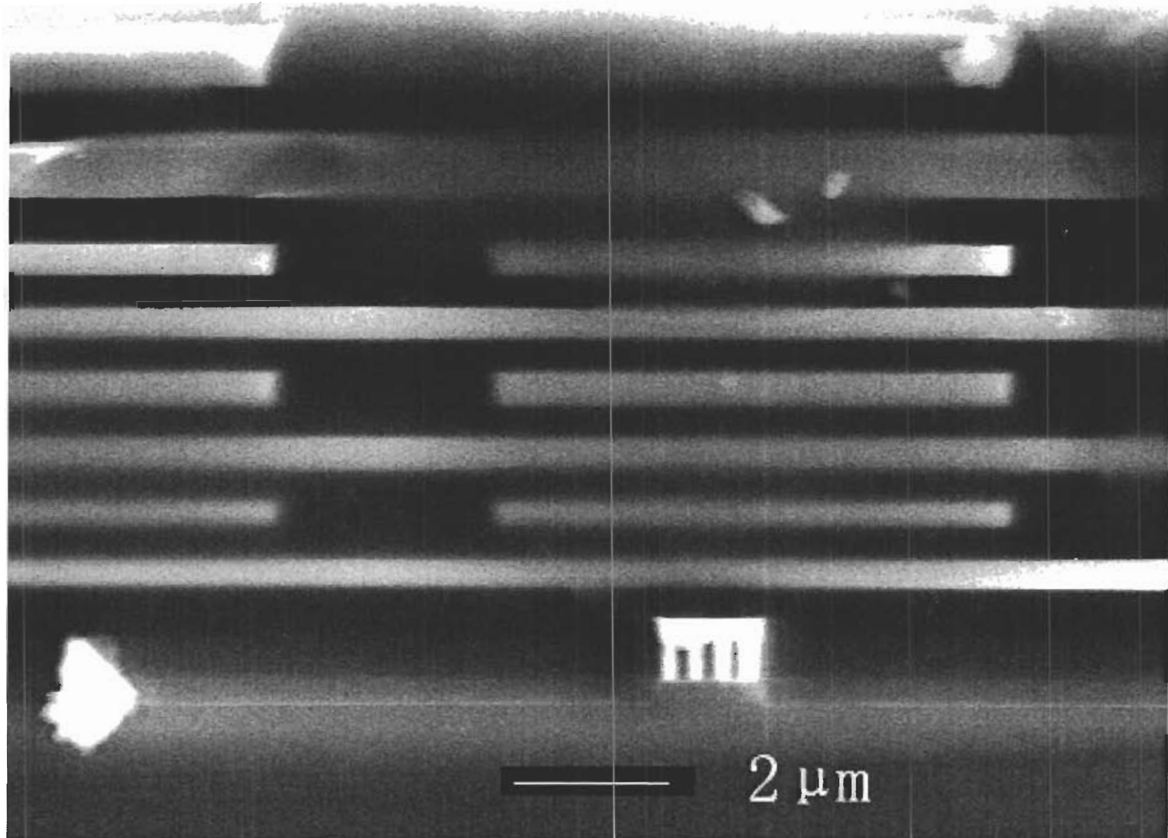
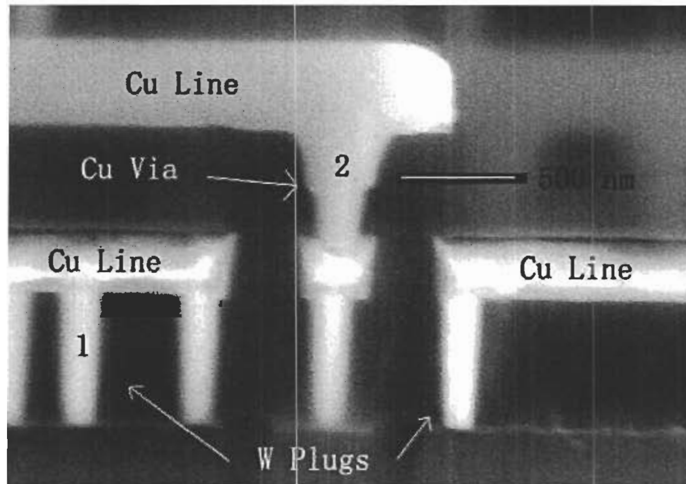
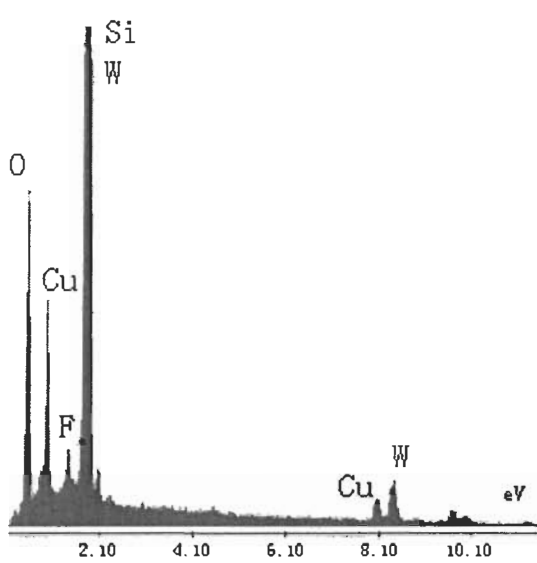


Figure 2.1: A secondary electron SEM image showing 9 interconnect layers of a test wafer ($V_{Ebeam} = 15kV$).

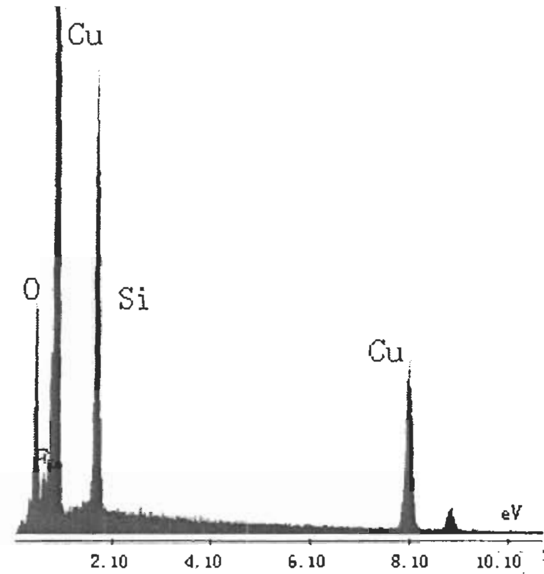
A continuous planar metal structure without any vias was employed as the electromigration test structure. These were located in the boundary regions between the main chips. A test structure consisted of two sets of bond pads connected to a serpentine test line and one monitor line which ran parallel to the test line but was electrically isolated from it. The space between these two lines was 160 ± 10 nm (Figure 2.4). The monitor line was not uniform in width (0.34 ± 0.01 μm (min) 4.2 ± 0.1 μm(max)) with its narrowest part wider than the test line (0.25 μm)(Figure



(a) A secondary electron SEM image of metal layer 1 and 2 showing W plugs and Cu vias.



(b) EDS analysis of point 1.



(c) EDS analysis of point 2.

Figure 2.2: Chemical composition of plugs and vias ($V_{Ebeam} = 15kV$).

<table>
<tr><th>Metal Layer</th><th>Structure</th><th>Width/Separation (μm)</th><th>Length (μm)</th><th>Thickness/ Height (μm)</th></tr>
<tr><td rowspan="6">$2-7$</td><td>Bond Pads (Cu)</td><td>69.8 ± 0.3</td><td>69.7 ± 0.1</td><td rowspan="3">0.37 ± 0.03</td></tr>
<tr><td>Test Line</td><td>0.25 ± 0.02</td><td>1800 ± 50</td></tr>
<tr><td>Monitor Line</td><td>min: 0.340 ± 0.01
max: 4.2 ± 0.1</td><td>N/A</td></tr>
<tr><td>Inter Layer Dielectric</td><td>N/A</td><td>N/A</td><td>0.50 ± 0.04</td></tr>
<tr><td>TaN Diffusion Barrier</td><td>N/A</td><td>N/A</td><td>0.04 ± 0.03</td></tr>
<tr><td>Separation A</td><td>0.16 ± 0.01</td><td>N/A</td><td>N/A</td></tr>
<tr><td rowspan="6">$8-9$</td><td>Bond pad (Al cap)</td><td rowspan="2">69.8 ± 0.3</td><td rowspan="2">69.7 ± 0.1</td><td>1.00 ± 0.03</td></tr>
<tr><td>Bond pad (Cu)</td><td>0.82 ± 0.03</td></tr>
<tr><td>TaN Diffusion Barrier</td><td>N/A</td><td>N/A</td><td>0.09 ± 0.03</td></tr>
<tr><td>The Edge of Bond Pad</td><td>N/A</td><td>N/A</td><td>Inside:
0.91 ± 0.03
Outside:
1.51 ± 0.03</td></tr>
<tr><td>Separation B</td><td>10.1 ± 0.1</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Separation C</td><td>5.2 ± 0.1</td><td>N/A</td><td>N/A</td></tr>
</table>

Table 2.1: The dimensions of the tested interconnect layers (as measured by SEM). Separation A: between the test line and the monitor line; Separation B: between corresponding AW and DW bond pads; Separation C: between DW bond pads and the boundary line of the main chip.

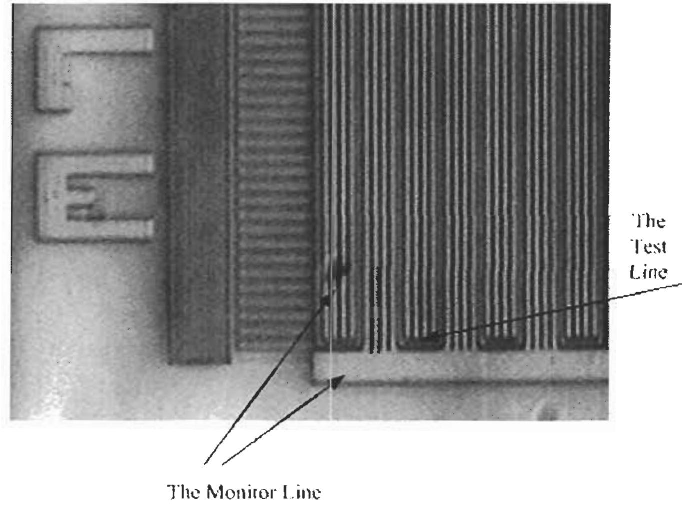
2.3). Table 2.1 lists the dimension in detail.

Eight test structures (one for each metal layer, M1, M2 and so on) were connected serially and formed one unit (called a DW module). Beside the DW, there were other test structures including an AW module. These neighboring test structures were transistors, sheet resistors, or gate oxide. On the other side of the DW, there was a boundary metal line of the main IC chip (Figure 2.4). Spaces between DW and AW bond pads, and between DW bond pads and the boundary line were 10.1 ± 0.1 μm and 5.2 ± 0.1 μm, respectively (Table 2.1).

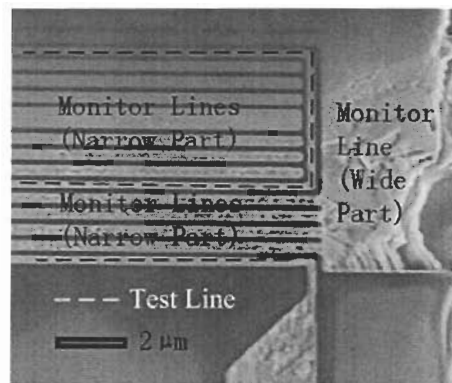
The cross-sectional structures of the test line and monitor line are the same as seen in Figure 1.3. The bond pads had an Al cap which provided good contact to a gold (Au) bonding ball and protected the Cu pads underneath [57]. Each bond pad consisted of 9 layers of pads, one for each layer of the interconnect. These pads were connected vertically through dozens of vias which are displayed in Figure 2.5 and 2.8. The test line in a particular layer connected the pad in this layer directly (Figure 2.5). In electromigration tests, the current flowed into the bonding ball first, entered the Al cap pad, continued down to the pad of the Cu layer under test through vias and the passed through the test line (Figure 2.5).

There are two issues which deserve comment. First of all, Figure 2.8 shows that there are approximately 50-100 vias between different layers of bond pads. As a result, only 1-2% of the total stress current would pass each of them in electromigration tests, meaning that vias here are not the primary electromigration failure sites.

Secondly, all bond pads, the test line and the monitor line are electrically isolated from the substrate. To confirm this, the resistance between two bond pads were measured before and after the test line was cut by Focus Ion Beam (FIB) milling. The resistance was measured by sweeping an applied voltage from -20 V to +20 V at

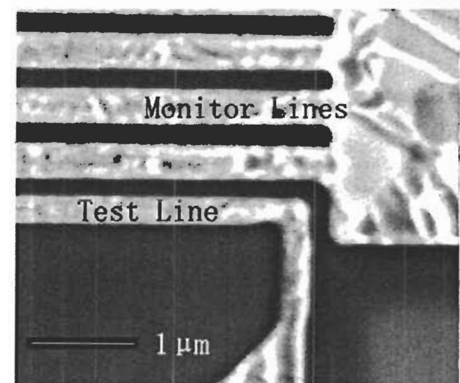


(a) Optical plan-view image.



(b) A secondary electron SEM planview image.

($V_{Ebeam} = 5kV$)



(c) The first corner in the test line.

($V_{Ebeam} = 5kV$).

Figure 2.3: Planview images of the test structure at metal line 7 (M7).

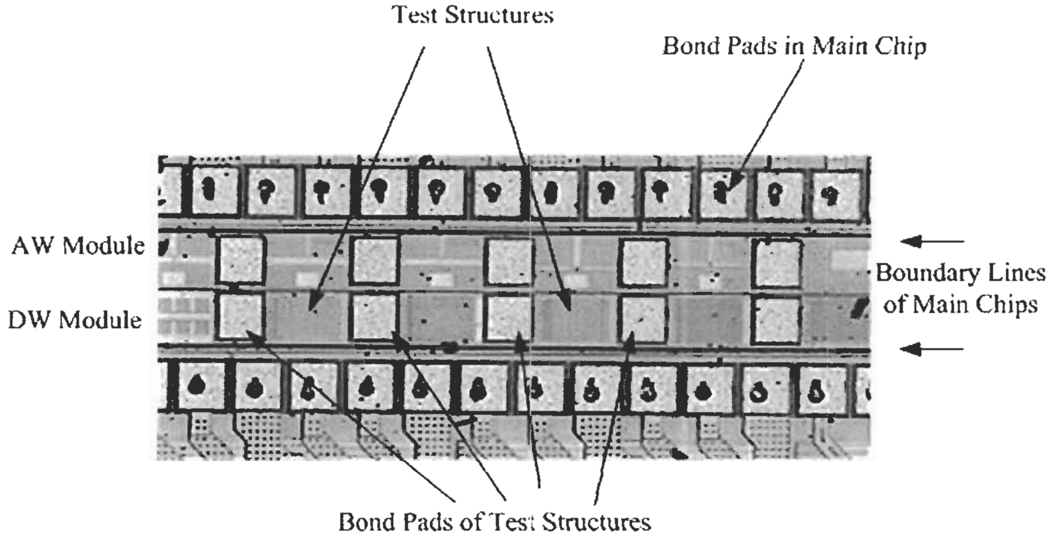


Figure 2.4: An optical, planview image showing the location of the test structure.

a step of 0.1 V with an HP 4156A Parameter Analyzer. The current was measured for each step and the differential resistance (R^x_{diff}) at each data point was calculated by the following equation:

$$R^{diff}_x = \frac{V_x - V_{x-1}}{I_x - I_{x-1}}, \tag{2.1}$$

where V_{x-1} and I_{x-1} are the specific voltage and current at the previous data point. Subsequent to the resistance measurement, the test line was cleaved by FIB. (The cutting depth was 10 μm, which is deep enough to deny all possible metal contact between two bonding pads.) Finally, the differential resistance was measured again by the same method.

These experiments were carried out with M2 and M6 test structures. Both of them showed that the cutting process would isolate two bonding pads completely (the resistance between bond pads after cutting was greater than 1 $M\Omega$), indicating that there were no extra current paths between bond pads and the whole test structure was isolated from the substrate (Figure 2.6).

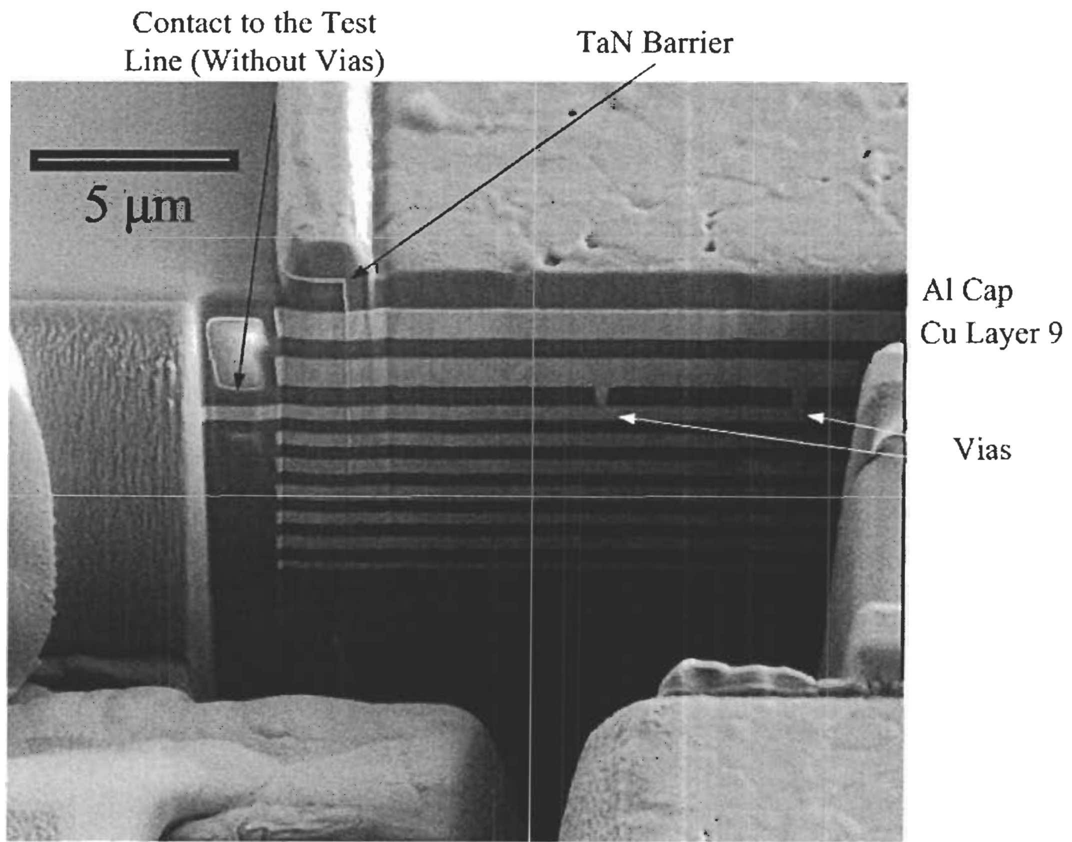


Figure 2.5: A secondary electron cross-sectional SEM image of a bond pad at the test structure M7 ($V_{Ebeam} = 5kV$).

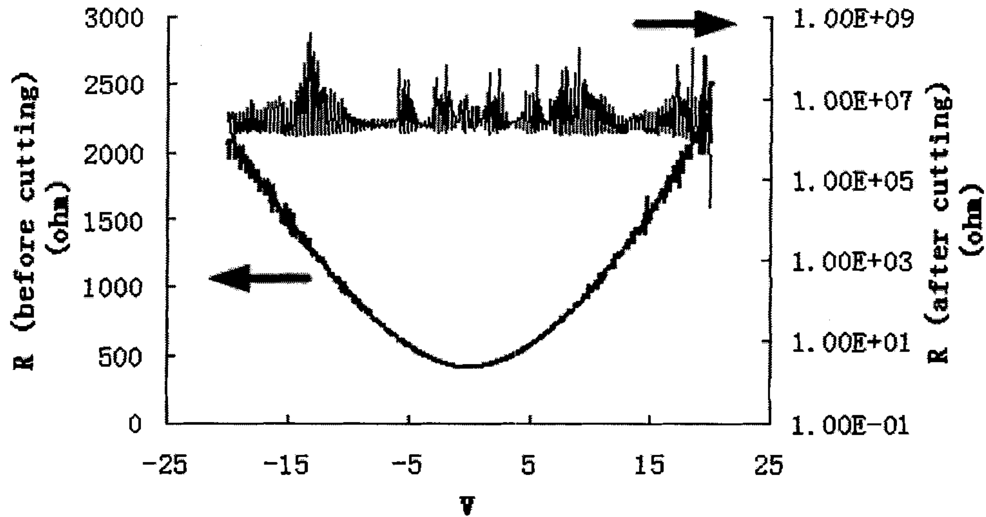


Figure 2.6: Electrical measurements of the test structure M6 before and after cutting with FIB. The test structure resistance increased to more than 1 $M\Omega$ after the cutting, indicating electrical isolation from above the substrate.

2.2 Sample Preparation

The goal of sample preparation was to build sample packages which could be tested under a temperature up to 400 °C for more than 1000 hours. The test current should pass the test structure without disturbance.

2.2.1 Challenges

Wire bonding must be employed to connect the test structure to the package. Due to equipment limitations, the minimum size of a bonding ball had a diameter of 70 μm. This was larger than the bond pad and was very likely to touch either the neighboring pads or the boundary lines of the main IC chips. The situation is shown in Figure 2.7. Measurement results showed that if a bonding ball touched the AW module, part of the current would pass into the neighboring circuits. Alternatively, if the ball

touched the boundary line of the main chip, the electromigration test structure would be shorted. So, these adjacent structures had to be isolated by a lithography process. In order to simplify the patterning work, we could have just deactivated one side and put the bonding ball far away from the other side when we bonded. However, the space between AW and DW bond pads was larger than between the boundary line and DW bond pads (Table 2.1). Therefore, isolating AW neighboring circuits was easier.

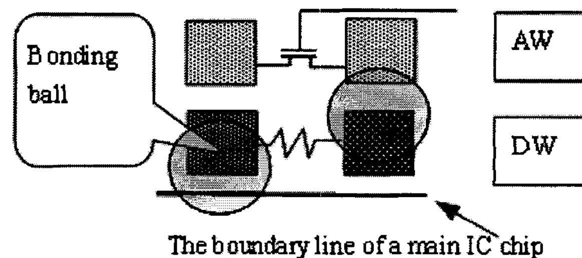


Figure 2.7: Bonding balls were larger than the bond pads of the test structure and overlapped with the adjacent structures.

There were two methods for this isolation task. One was to cover the neighboring bond pads with SiN_x, and the other was to etch them away. The resulting step coverage of SiN_x at the pad edges was always unsatisfactory by the first method. Hence, we chose the second strategy and a sample preparation process was developed.

2.2.2 Sample Preparation Procedure

2.2.2.1 Lithography and Etching Process

The scheme was to etch away all of the top metal in the AW bond pads, while protecting the DW pads. Over-etching was needed to remove the vias underneath for good isolation. An overhead transparency mask (made by Imagesetter) was employed in the lithography process, providing 5 μm resolution. The patterning process is

shown in Table 2.2, while Figure 2.8 shows the result, showing that the top metal layers in an AW pad had been removed. In addition, the etchant entered metal layers underneath through vias and attacked some Cu there as well.

2.2.2.2 Process Confirmation

Several experiments were designed to judge whether the process succeeded in isolating unwanted neighboring circuits.

Optical Examination Optical images, for example Figure 2.9, showed that the top metal of the AW bond pads had been removed and that all bonding balls were away from the boundary line of the main IC chip. Hence, the test current should only pass through the test line.

Electrical Measurement

Resistance Measurement There were 17 bond pads for 8 test structures and 1 monitor line in each DW module. All pads were bonded and the resistance between every two bonding balls was measured. Measurement results showed that all bonding balls were isolated unless there was a test structure between them. Since this wouldn't be the case if neighboring circuits were active, such measurement results indicated the success of the isolation work.

Furthermore, the accurate resistance of each test line was measured by a probe station before the sample preparation process and bonding ("Reference Values" in Table 2.10). After wire bonding, this resistance was measured again by a multimeter ("measured results" in Table 2.10). Table 2.10 shows that these two results were the same (taking the bonding balls resistance into account), indicating the success of the sample preparation.

1	Spin photoresist	3000 RPM, 30 sec	Shipley
2	Soft bake	100 °C, 20 min	
3	Expose	24 sec	Near UV
4	Develop	1 min 30 sec	MF319
5	Hard bake	120 °C, 20 min	
6	Al etch	40 ~ 50 °C, 5 min	Commercial Al etchant (Type A:Phosphoric, Nitric and Acetic Acid. 100 A/s at 50 °C)
7	TaN, Cu and TaN layers etch	27 sec	$HF(48\%) : H_2O_2(50\%) : H_2O = 1:1:2$ (volume ratio)
8	Sample cut	Split the sample into pieces to fit the package	Diamond pen
9	Remove photoresist	1 min 30 sec	Acetone
10	Glue the sample to the package	Anneal at room temperature, 93 °C, 204 °C and 372 °C, 1 hour for each stage.	Ultra-Temp 516 : Ultra-Temp 516T = 9:1 (Weight Ratio), Sidebrazer 24 pins package
11	Wire bond	~ 145 °C	The diameter of the Au line is 25 μm

Table 2.2: Sample Preparation Process.

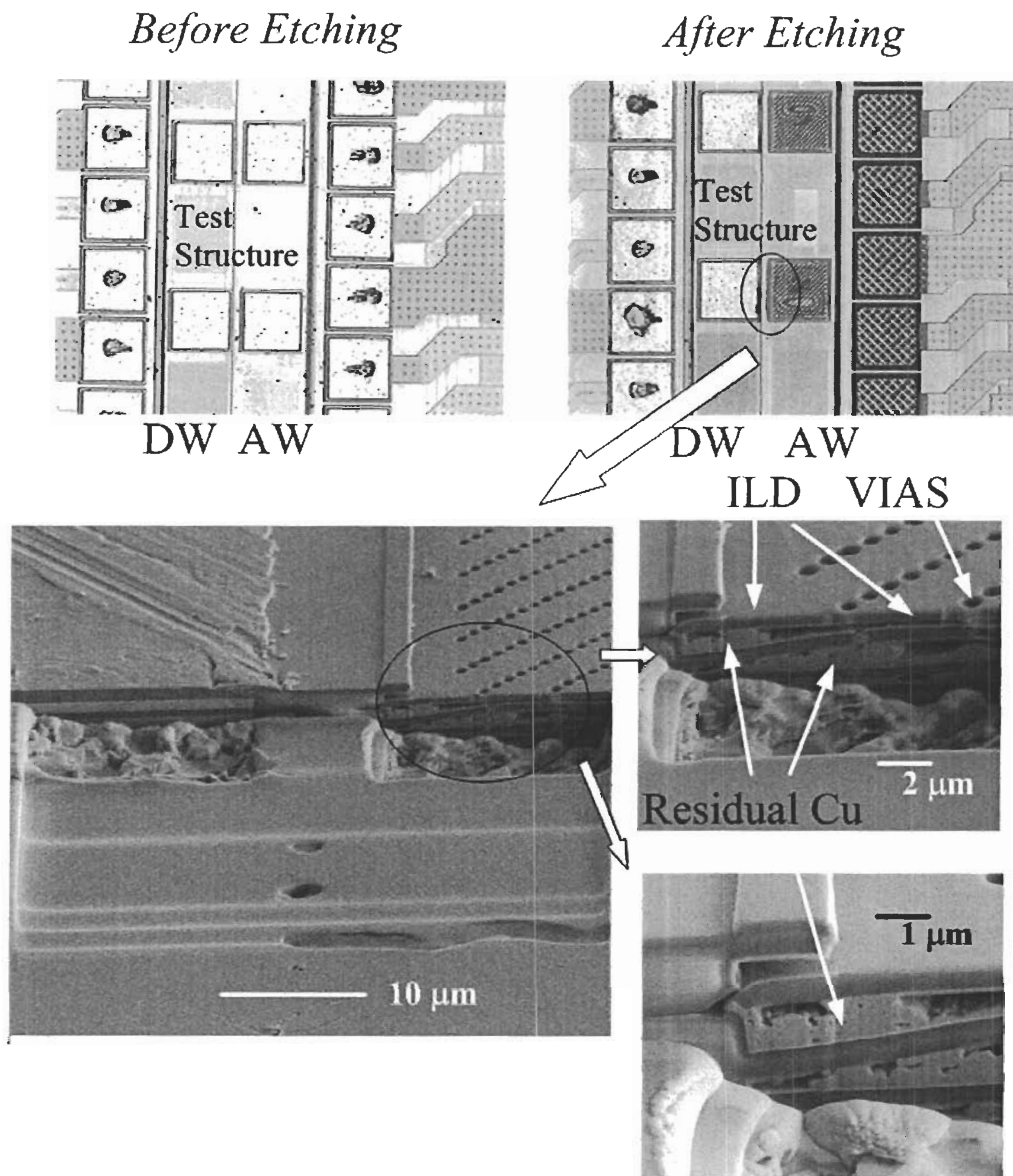


Figure 2.8: Optical and secondary electron SEM images of patterning results (for SEM images, $V_{Ebeam} = 5kV$).

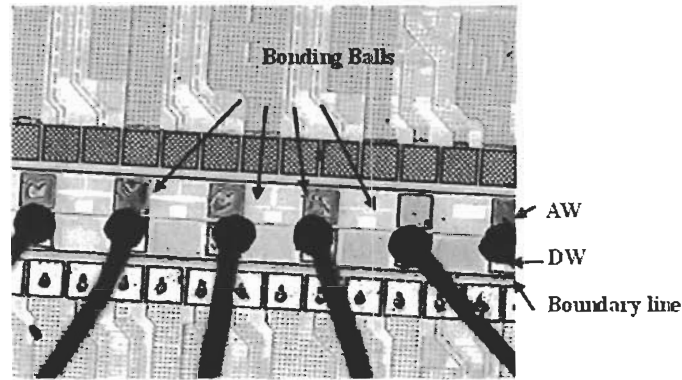


Figure 2.9: An optical image of bonding results.

Structure	M2	M3	M4	M5	M6	M7	M8
Reference (Ω)	495 ± 1	476 ± 1	428 ± 1	456 ± 1	453 ± 1	426 ± 1	75.4 ± 0.1
Measured Results (Ω)	507 ± 9	493 ± 8	425 ± 12	453 ± 10	451 ± 8	427 ± 10	78.6 ± 1.5

Figure 2.10: Resistance measured (by a probe station) before sample preparation and (by a multimeter) after wire bonding for metal layers M2 to M8. The values were the same (within experimental error), indicating the success of the patterning process.

***V* versus *I* and *R* versus *I* Characteristics** Wire bonding was conducted on both patterned and unpatterned samples. The V versus I and R versus I characterization curves were compared. Figure 2.3 shows typical results. Patterned samples had ideal ohmic characteristics and the resistance matched the results in Table 2.10, while unpatterned samples displayed non-ohmic behavior. These results indicated that neighboring current paths were isolated successfully.

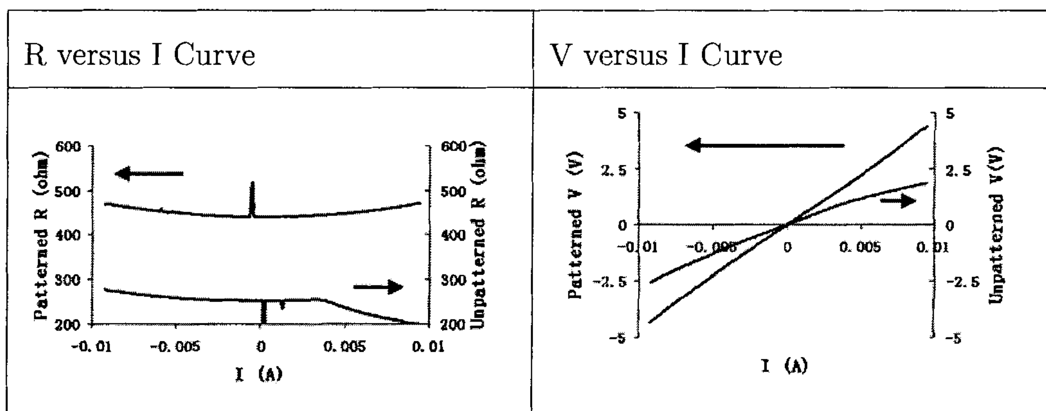


Table 2.3: Patterned and unpatterned R vs I and V vs I curves between the 5th and 6th bonding balls (M4) showing the success of the isolation process.

TCR Extraction TCR is a material parameter. If neighboring circuits are activated, the measured TCR should be different from that of Cu, which would be a good indicator of a failure in isolation. Table 2.4 shows measured TCR values compared to literature reports, also supporting successful pattern isolation.

2.3 Test Strategy

A constant current density was applied to the test structure. The initial resistance of the test line with the current stress was measured. (The measurement was carried out 3 times within the first 2 minutes of the test. The average value was considered

Material	Bulk Cu	Cu Film in ICs *	Measured Results
TCR (10^{-3} °C)	4.29	3.0-3.5 [51][52][56]	3.051 ~ 3.238
	Ref Temp: 20 °C	Ref Temp: 0 or 20 °C	Ref Temp: 20 °C

Table 2.4: TCR measurement results.
* The TCR of metal decreases with a reduction in feature size, resulting in a lower TCR for the Cu film in ICs compared to bulk Cu, shown in this table. [51, 52, 56].

as the $R_{initial}$.) This resistance was both the reference resistance for failure criteria and a parameter to calculate the Joule heating effect through Equation 1.12.

The test circuit is shown in Figure 2.11. During tests, the potential drop in the test line, V_{total}, and external resistor, V_1, were measured every 15 seconds. The resistance of the test line, R, and the leakage current between the test line and monitor line, $I_{leakage}$ were calculated from V_{total}/I_{total} and V_1/R_1, respectively. An increase in R normally indicated the existence of a void, while a drop in R and the simultaneous jump of $I_{leakage}$ must occur with the formation of an extrusion. In particular, when short circuit failures happened, a portion of the stress current would pass through the extrusion, monitor line, R_1 and to the ground as a leakage current. Typically, R was around 900 Ω at 350 °C and the total resistance of the monitoring line was less than 10% of R. Therefore, R_1 controlled whether the neighboring current path had a high or low resistance, and would therefore determine the magnitude of changes in R and $I_{leakage}$ if an extrusion formed. An R_1 of 47.00 or 19,980 Ω was implemented in our tests to simulate a strong or weak current inside an extrusion. With the 47.00 Ω R_1, according to the test circuit, the electrical stress inside the extrusion was expected to be 20 times larger than for the other case. It is interesting to note that because the monitor line was grounded through R_1, the location of an extrusion would also affect

its voltage drop.

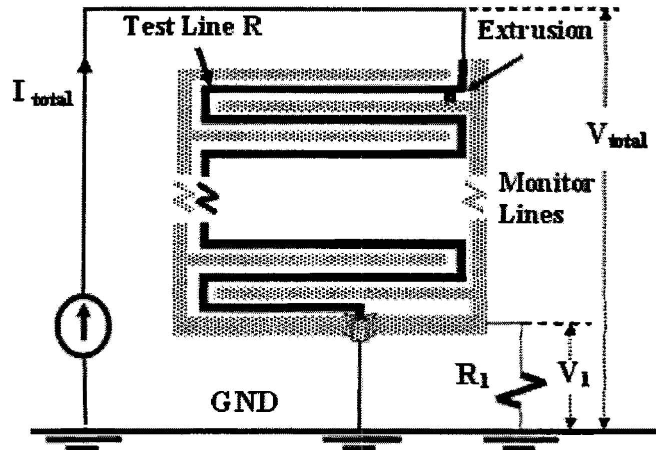


Figure 2.11: The test circuit.

2.3.1 Test Equipment

An automatic measurement system was set up in Prof. Karen Kavanagh's lab at Simon Fraser University. It included a furnace (Lindberg 59344), two oscilloscopes (Tektronix 340 and 2022), one programmable current source (Keithley 220), one dual voltage source (HP 6209B), two digital multimeters (Agilent 3478A and Fluke 77) and a control computer. All equipment was connected via IEEE 488 protocol and a GPIB interface. The control software was developed using "Labview 6i".

2.3.2 Test Parameters

The current density and ambient temperature are two critical test parameters in electromigration tests. They also impact each other and must be considered together when designing a successful experiment. The following rules were summarized from the literature and guided our tests.

First, the current should be high enough to generate electromigration failures. According to Chapter 1.1.1, the jL product has to be more than a threshold value, otherwise the back-flow stress will counteract the electromigration flux. Based on the literature, the critical product of jL within common test temperature ranges for Cu metallization is between $1200 - 9000A \cdot cm$, meaning the test current density should be more than $0.5MA/cm^2$ in our experiments [10, 11, 24].

Secondly, a Joule heating effect should be minimized. According to Chapter 1.1.3, large Joule heating will cause inaccurate lifetime. The temperature increase induced by Joule heating is typically less than 50 °C (up to 70 °C [24]) in literature reports [54, 55].

Thirdly, the time limitation has to be considered. It would be nice if only a tiny current is applied to eliminate any observable Joule heating but we then must wait half a year for a result. A lifetime of less than 1 week for dc tests and 2 weeks for one or two directional square wave stress tests was acceptable in our project.

In addition, the test structure also determines the suitable current density. For example, due to the extra flux divergence, J is generally limited to be under $3MA/cm^2$ when vias are present in the test structure [10, 50, 53, 62]. Since our test line is a planar structure and the inherent flux divergence is relatively small, a larger current density was feasible and assisted in obtaining test results more quickly.

For the test temperature, accelerated Cu electromigration tests typically are carried out between $220 \sim 410$ °C to shorten the lifetime, higher than in Al tests due to the better performance of Cu in electromigration (Chapter 1.2.1) [11, 13, 15, 24]. The selection of test temperatures is determined by three issues. First, it must be high enough to speed up the test. Our ICs have 10 year warranties if they operate under 110 °C. Hence, the temperature should be generally higher than 200 °C in accelerated

tests.

Secondly, the test structure should be thermally stable in the test environment. It is acknowledged that Cu/low-k interconnects are safe at a temperature as high as $400 - 450\,^{\circ}C$. For instance, the forming gas annealing process, the last step in Back End of Line (BEOL) fabrication, operates within this range .

Thirdly, the primary diffusion mechanism in an accelerated test environment should be the same as under the real working conditions. According to Table 1.1 and the discussion in Chapter 1.1.1, the test temperature is best to be limited to under $450\,^{\circ}C$.

Based on the above discussion, a current density of $5 \sim 9MA/cm^2$ was employed in our dc electromigration tests [24, 54]. For one and two directional square wave tests, both peak and RMS current densities were limited to within this range as well. Our ambient furnace temperatures were either $300\,^{\circ}C$ or $350\,^{\circ}C$. The maximum Joule heating in our tests was $39\,^{\circ}C$ with a $9MA/cm^2$ DC stress. Furthermore, most of our tests were carried out on metal layer 5 to 7. We believe that these three layers were good representatives because they endured medium mechanical and thermal stress. (The bottom layers have the maximum mechanical stress from layers above and the minimum Joule heating because they are close to the substrate). We have confidence that our tests were valid and efficient for Cu electromigration tests according to the discussed guideline.

Chapter 3

Experimental Results

3.1 Lifetime Measurement

A total of 20 samples were measured and their test conditions and measurement results are listed in Table 3.1.

Typical examples of measured resistance and leakage current versus time curves are shown in Figure 3.1 and 3.2. The sample (No. 18 in Table 3.1) in Figure 3.1 was located at metal layer 6, M6, and tested at 350 °C with an bidirectional square wave stress current density of 8 MA/cm^2, 100Hz and 0.5 duty factor. The initial resistance with stress, R_0, was 909.58 Ω. The normalized resistance versus time curve had two clear increases, at the moments of 278.3 hours and 302.8 hours, respectively. These increases must indicate the formation of significant voids. $R/R_0 = 1.2$ was our void failure criterion and the second increase reached that, causing the failure. The mechanism of initial fluctuations in resistance was not clear, probably it was due to the shape evolution of small voids or the surface annealing of Cu lines. The leakage current also increased a little bit after the final failure. This is believed to be due to structural damage along with the formation of a significant void. The plot in Figure 3.2 shows a different scenario (Sample #1). This sample was located at metal layer 8, M8, and tested at 350 °C with a dc stress current density of 2 MA/cm^2. Instead

No. #	Temp °C ±5	Metal Layer	Current Density MA/cm^2 ±0.6	TCR % ±0.002	Lifetime hours ±0.004	Normalized Results	Failure Modes
1	345	8	2	0.348	52.514	N/A	Extrusion
2	142	5	15	N/A	128.681		Temporary Extrusion
3	177	7	15	0.321	6.974		Extrusion
4	177	5	15	0.317	15.847		Extrusion
5	222	6	10	0.319	44.264		Extrusion
6	222	5	15	N/A	35.697		Extrusion
7	345	5	3	0.317	> 174		N/A
8	295	6	5.0	0.320	182.197	20 ± 4	Temporary Extrusion
9	345	6	5.0	0.316	114.129	71 ± 16	Void
10	345	6	8.0	0.315	10.538	14 ± 3	Temporary Extrusion
11	345	7	8.0	0.320	54.901	83 ± 10	Void
12	345	7	6.0	0.325	24.838	60 ± 12	Temporary Extrusions
13	345	7	9.0	0.321	26.481	87 ± 17	Extrusion
14	345	5	8.0	0.312	8.986	21 ± 4	Extrusion

No. #	Temp °C ±5	Metal Layer	Current Density MA/cm^2 ±0.6	TCR % ±0.002	Lifetime hours ±0.004	Normalized Results	Failure Modes
15	345	7	8.0	0.309	16.847	39 ± 7	Void
16	345	5	5.0	0.320	22.200	13 ± 3	Extrusion
17	345	6	8.0 (Peak) 0 DC offset, square waveform, r=0.5, 100 Hz	0.328	54.430	76 ± 10	Temporary Extrusion
18	345	6	8.0 (Peak) 0 DC offset, square waveform, r=0.5, 100 Hz	0.326	302.804	375 ± 80	Void
19	345	7	8.0 (Peak) 0 DC offset, square waveform, r=0.5, 1 Hz	0.317	186.125	105 ± 21	Temporary Extrusion
20	345	6	8.0 (Peak) 0 DC offset, square waveform. r=0.5, 100 Hz	0.331	> 518	N/A	N/A

Table 3.1: The test conditions, TCR, measured and normalized lifetimes, and failure modes of test samples. Samples #1-16 were tested under dc conditions. Sample #17 was tested under pulse-dc condition and samplea #18-20 were tested under bidirectional square wave conditions. r in the table represents the duty factor. For samples tested under proposed dc stress conditions (No. 8 -16), $t_{50} = 39 \pm 7$ hours and $t_{max} = 87$ hours. (Failure criterion is 20% change in resistance or 50 μA increase in leakage current with an observable drop in resistance.)

of increasing, the resistance of the test line dropped suddenly after 52.5 hours with a simultaneous increase by 4 mA in leakage current. Since our failure criterion for extrusions was a 50 μA increase in leakage current along with the observable drop in resistance (Chapter 1.3), this sample was considered as failed by an extrusion. Oscilloscopes employed to measure the leakage current, inducing a relatively large ground noise, particularly with bidirectional current stress.

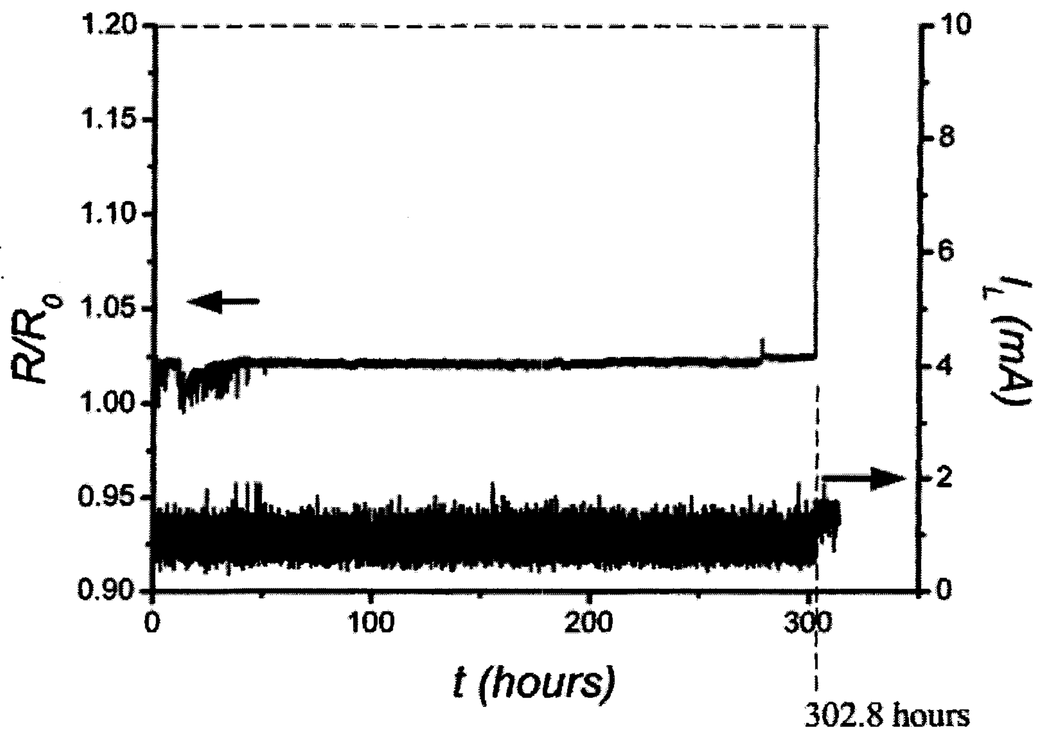


Figure 3.1: Normalized resistance R/R_0 and leakage current I_L versus time curves of sample #18 which failed by voids, M6, bidirectional square wave stress, 0 DC offset, peak current density is 8 MA/cm^2, duty factor 0.5, frequency 100 Hz, $R_1 = 47\ \Omega$, $R_0 = 909.58\ \Omega$.

Samples #1-7 in Table 3.1 were tested using the conditions proposed in Chapter 2.3.2. They were used to debug our automatic testing system and to estimate lifetimes

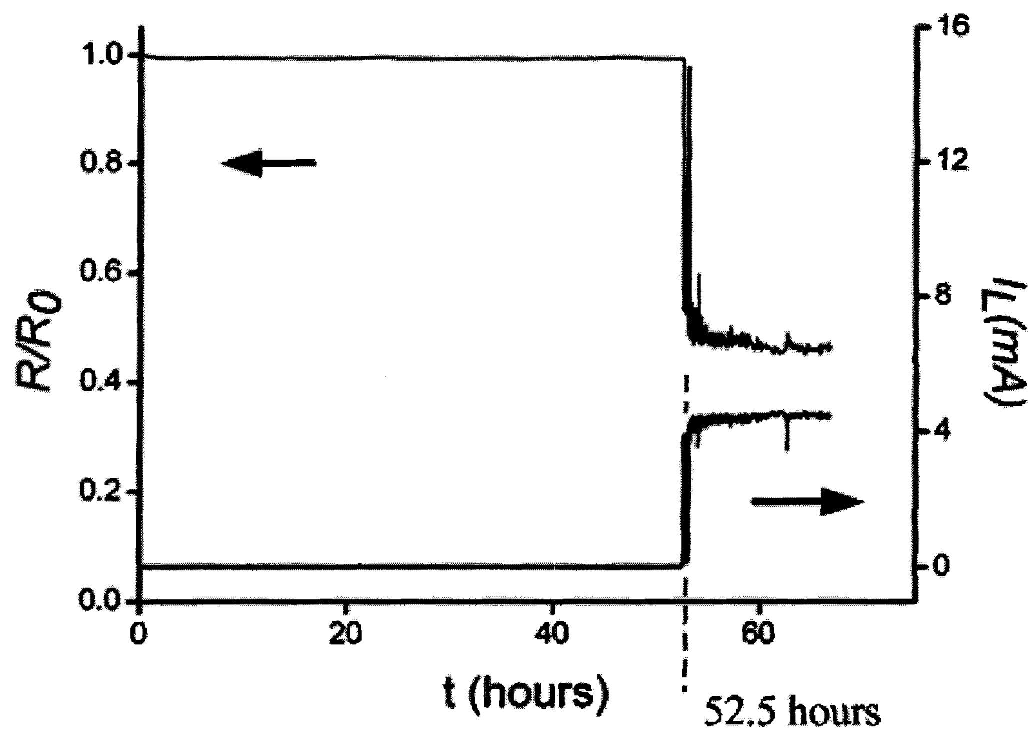


Figure 3.2: Normalized resistance R/R_0 and leakage current I_L versus time curves of sample #1 which failed by an extrusion, M8, DC stress 2 MA/cm^2, R_1 = 47 Ω, R_0 = 169.37 Ω.

under proposed test conditions. Furthermore, metal layer 8, M8, was stressed at 350 °C and $2MA/cm^2$ (sample 1) to examine whether the thickness of the dielectrics above the test structure could affect the electromigration failure behaviors. (Sample #7 was the reference.)

Samples #8-16 were tested under our proposed dc test conditions (Chapter 2.3.2). For metal layers 5-7, they were 300 or 350 °C and between 5 and 9 MA/cm^2. Test results were then normalized to the exactly same test condition (350 °C, 8 MA/cm^2) based on Black's Law (Chapter 1.1.2 and Equation 1.8, 1.9). The current exponent n and the activation energy E_a employed in the normalization process were provided by the foundry company, which were 2 and 0.8 eV, respectively. An E_a of 0.8 eV is consistent with the fact that surface diffusion is dominant (Chapter 1.2.2.1), and n = 2 is coherent with our discussion in Chapter 1.2.2.2 as well. A rough verification test of E_a was conducted (Sample #2, 4 and 6) and the measurement result (Figure 3.3) showed $E_a = 0.85 \pm 0.05$ eV, consistent with the foundry value. Due to the lack of samples, we did not carry out any verification tests for n. The normalization error was determined by the measurement errors of resistance, real lifetime and TCR, and the accuracy of furnace temperature and applied current density.

Electromigration failure distributions have been widely acknowledged to be log-normal [6, 25, 53] and the probability density function (PDF), $f(t)$, is given by [6, 53]

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} exp(-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2}) \quad , \tag{3.1}$$

where σ is the standard deviation, in units of logarithmic time. σ can also be considered as the shape parameter for such lognormal distribution. The integration of the PDF from time 0 to t is the cumulative distribution function (CDF), $F(t)$, which can be described as a Gaussian integral [6]:

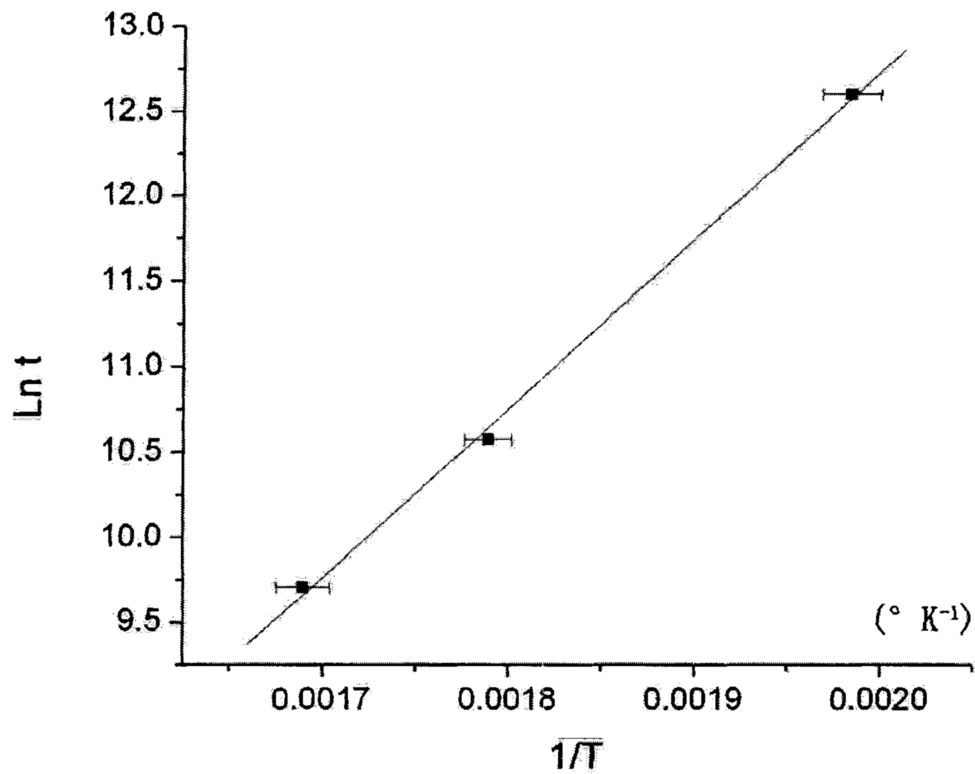


Figure 3.3: An Arrhenius plot of lognormal lifetimes. The slope gave an activation energy, $E_a = 0.85 \pm 0.05$ eV, with a correlation coefficient of the linear fit, r = 0.99912. Sample #2, 4 and 6 were employed in this measurement.

$$F(t) = \int_0^t f(u)du = \int_{-\infty}^{z} \frac{1}{\sqrt{2\pi}} exp(\frac{-v^2}{2})dv \quad , \tag{3.2}$$

where, $z = (\ln t - \ln t_{50})/\sigma$ and $t > 0$. The above equation describes the failure probability of an interconnect within the time interval [0, t].

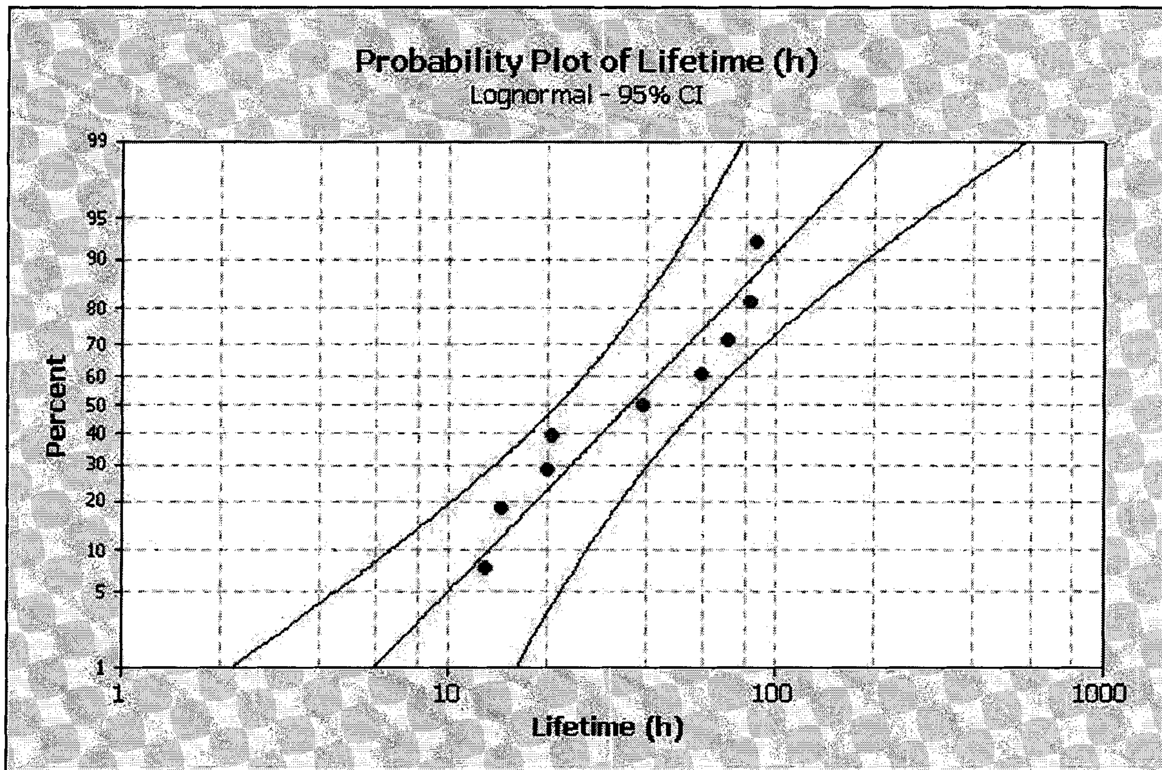


Figure 3.4: Experimental cumulative failure percent probability versus log scale lifetime. The middle line is the result of lognormal curve fitting and the other two lines indicate the deviation.

Figure 3.4 is the cumulative failure percent probability vs lognormal lifetime curve of our experimental results (Sample 8-16). If all data points follow a straight line, the distribution will be a perfect lognormal. Figure 3.4 only shows a rough lognormal distribution, indicating the existence of multiple failure modes [6, 67, 68]. The t_{50} is 39.09 hours, and σ is 0.33. Based on other reports which also have significant numbers

of samples that failed by extrusions, our σ is acceptable, not too big. (For example, a $\sigma > 0.67$ in Ref. [36].)

It is important to note that due to the lack of samples, our experiments did not follow the guideline of JEDEC [25], requiring engineers to test 25 samples under each stress condition. We tested at most 2 samples under each specific condition. Hence, a full statistical analysis was not feasible.

We have also conducted one and two directional square wave electromigration tests in a low frequency range. Sample 17 was tested under pulsed-dc condition and samples 18-20 were tested under bidirectional square wave test conditions. All of these conditions were 8 MA/cm^2 peak stress current density without dc offset and with a square waveform, at 350 °C. The duty factor was fixed at 0.5 and the test frequency varied from 1 to 100 Hz. The same failure criteria as dc tests were applied. In order to normalize those results, Equation 1.13 and 1.15 were employed, instead of 1.9. All other normalization steps were the same as for dc normalization. According to Table 3.1, bidirectional square wave stress conditions increased the lifetime significantly (about one order) and multiple failure mechanisms also happened as for dc conditions. For pulsed-dc test, the lifetime of sample 17 doubled the t_{50} of dc results (sample 8-16), as expected from Equation 1.13.

3.2 Failure Modes

Understanding the nature of the electromigration failure mode is one focus of our experiments. Besides the traditional permanent extrusion and void failures, we succeeded in finding a novel failure behavior which we define as temporary extrusion failures.

3.2.1 Extrusion Failures

Extrusion failures were widely detected in our experiments under both dc and bidirectional square wave stress conditions. Table 3.2 shows that more than 2/3 of the samples failed by extrusions. Moreover, some of the others also had extrusions after their initial void failures.

Failure Mode	Voids	Extrusions	
		Permanent Extrusion	Temporary Extrusion
Number of Failed Samples	5	8	6 + 3*

Table 3.2: The number of samples failing by each failure mode.

* Temporary extrusion failure existed in these 3 samples, happening after their first void or extrusion failures.

It is interesting to note that our extrusions were distributed widely in the test structure, whereas they generally happened near the anode in conventional tests [50]. The serpentine shape of our test line with many corners was considered as the reason. These corners induced extra flux divergence, facilitating both extrusion and void failures. Typically, extrusions formed close to "local" anodes, where the atomic flux was blocked by the corner.

3.2.1.1 Permanent Extrusion Failures

As discussed in Chapter 2.3 and 3.1, the decrease in R combined with a simultaneous increase in I_L is the indicator of an extrusion. In our tests, many extrusions were permanent and they caused final failures. Generally, these extrusions occurred after an increase in resistance, indicating that voids formed first. This phenomenon has

been explained in Chapter 1.2.2.2 . Figure 3.5 shows an example of a plot of R versus t and I versus t, where a void formed first (sample 14)(resistance increased before the increase of leakage current), and then the drop of resistance and the jump of leakage current happened together, indicating the occurrence of an extrusion.

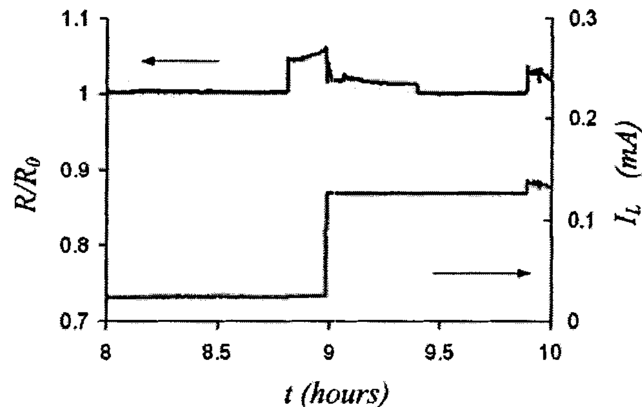


Figure 3.5: An example of an electrical measurement result showing clearly a void forming before an extrusion, with the latter causing the permanent failure. (Sample 14, M5, 350 °C, dc $8MA/cm^2$, $R_1 = 19.98k\ \Omega$, $R_0 = 939.25\ \Omega$.)

Large extrusions could be physically observed through an optical microscope because the covering dielectrics were transparent (Figure 3.6 (sample 11)). Further characterization was carried out by FIB and EDS techniques with SEM. Figure 3.7 is a back-scattered electron SEM image, showing an extrusion extending not only to the neighboring monitor line, but also to other lines (sample 11). This phenomenon indicates that severe damage is associated with the formation of extrusions in ICs.

3.2.1.2 Temporary Extrusion Failures

According to Table 3.2, a significant percentage of extrusions were not permanent, showing a novel behavior which had never been reported. These extrusions formed first, but after a short period, the R and $I_{leakage}$ went back to their initial values

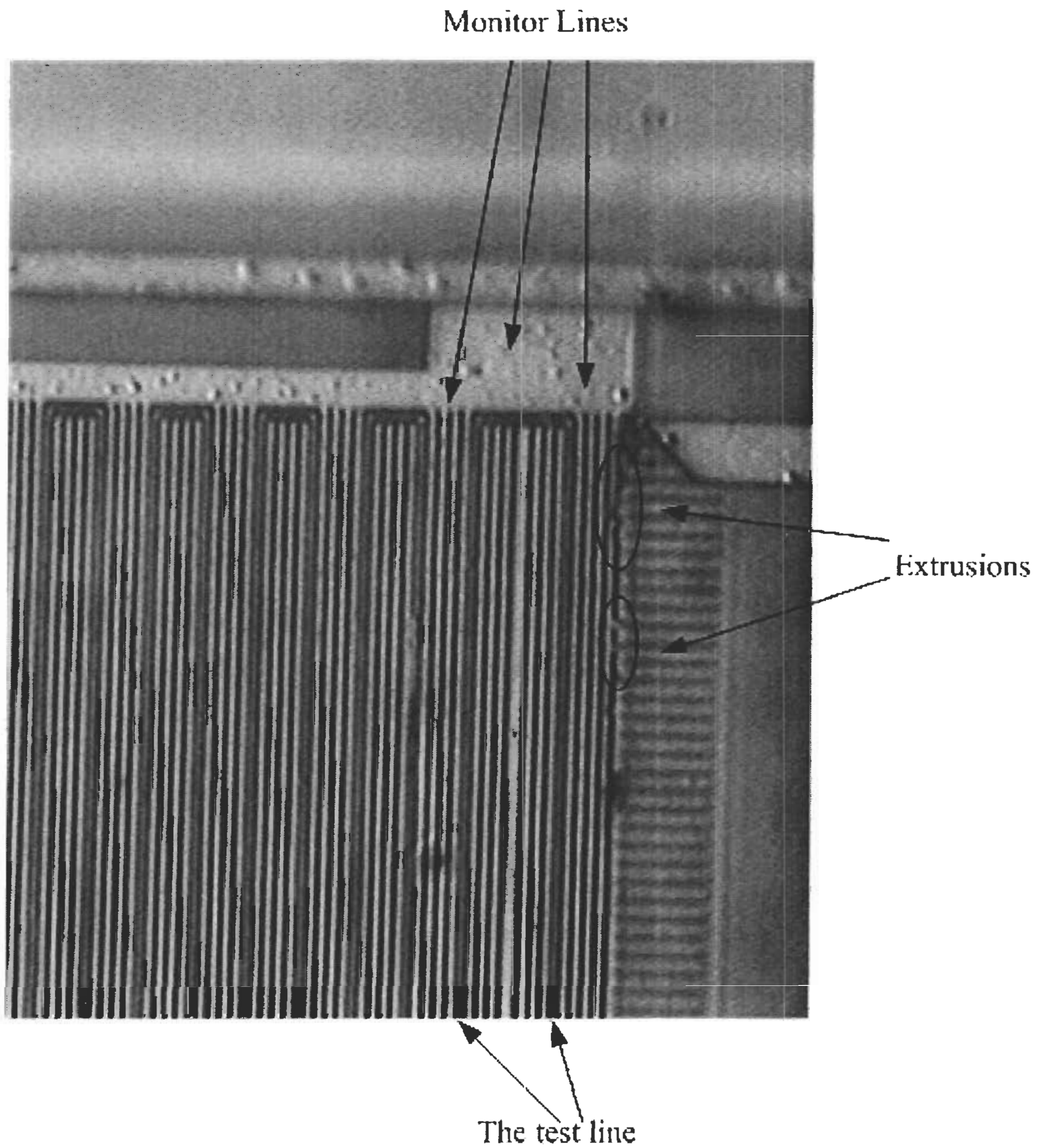


Figure 3.6: Extrusions observed by an optical microscope (The sample was failed by voids according to our failure criteria, but extrusion was the final failure). (Sample 11, M7, 350 °C, dc $8MA/cm^2$, $R_1 = 47\ \Omega$).

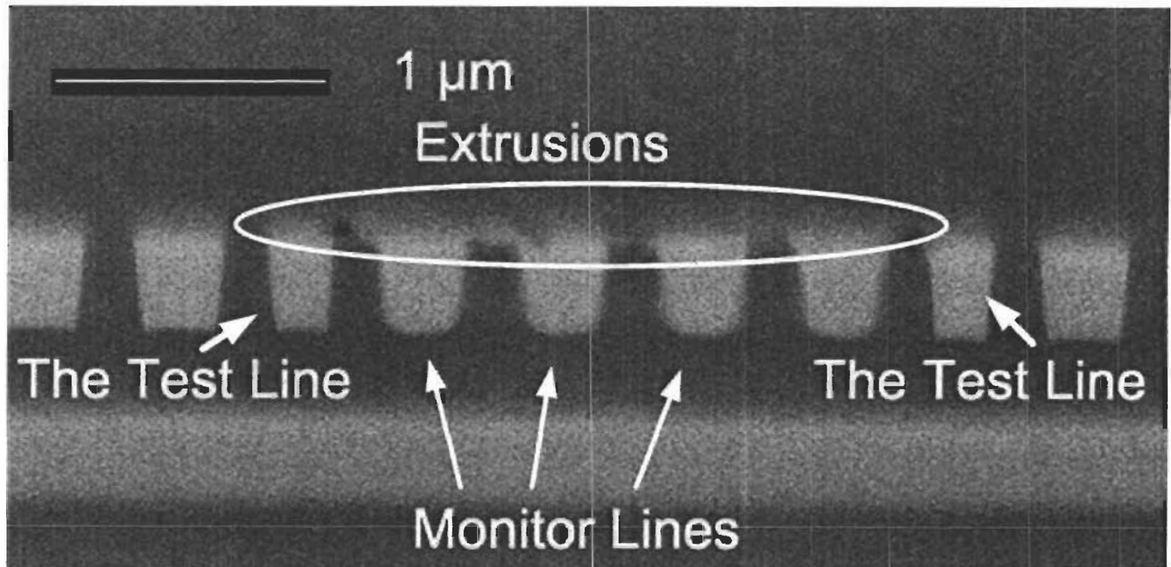


Figure 3.7: A back-scatter electron cross-sectional SEM image of an extrusion, extending across several neighboring lines ($V_{Ebeam} = 10kV$). (Sample 11, M7 at 350 °C, dc $8MA/cm^2$, $R_1 = 47\ \Omega$).

and became relatively stable again. Typically, whenever such phenomenon happened in one sample, it replicated multiple times, shortening the lifetime dramatically in some cases. (The lifetime could be reduced by as much as 9/10, as shown in Figure 3.9 (sample 19).) This behavior was defined by us as a temporary extrusion failure. Further characterization revealed that R and $I_{leakage}$ typically changed suddenly at the beginning, corresponding to a short circuit. Subsequent to that, failure behaviors were different if different external resistors, R_1, were implemented. An equivalent test circuit (Figure 3.8) shows that for a small R_1, a large portion of the stress current would pass extrusions. These extrusions typically existed for only several minutes (minimum 1 minute) and both R and I_L returned to their initial values quickly in the recovering process, indicating a rapid self-dissolution, as shown in Figure 3.10 (sample 10). For the situation where R_1 was much larger than R, less then 5% of the stress current passed the extrusion and the change in R was only barely detected.

Furthermore, R and $I_{leakage}$ decayed back gradually over more than 1 hour in Figure 3.11 (sample 12), instead of jumping back. Table 3.3 shows that temporary extrusion failures happened more frequently with a small R_1 (6 out of 14) than with a large R_1 (1 out of 7). The fact that extrusions appeared permanent with a weak electrical stress possibly resulted from extremely long self-dissolving processes.

The above behaviors revealed clearly that a strong electrical stress inside the extrusion would accelerate the self-dissolving process. Table 3.1 shows that temporary extrusion failures existed not only under dc conditions, but also under both one and two directional square wave stress conditions. In addition, the location of the extrusion would affect the electrical potential across it as well. If the extrusion was close to the global anode end, the electrical stress inside it would be stronger than at other locations. The equivalent circuit of Figure 3.8 illustrates this issue clearly.

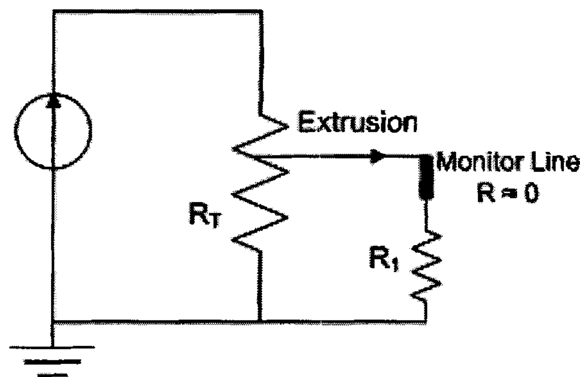


Figure 3.8: Equivalent test circuit.

A suspicious temporary extrusion failure site was cross-sectioned by FIB and imaged using back-scattered electron SEM. The image in Figure 3.12 clearly shows an extrusion with a thickness of 40 nm at a corner of the test line, extruding along the interface between the Cu-IMD/SiNx capping layer (sample 8). EDS analysis confirmed that the material consisted of Cu.

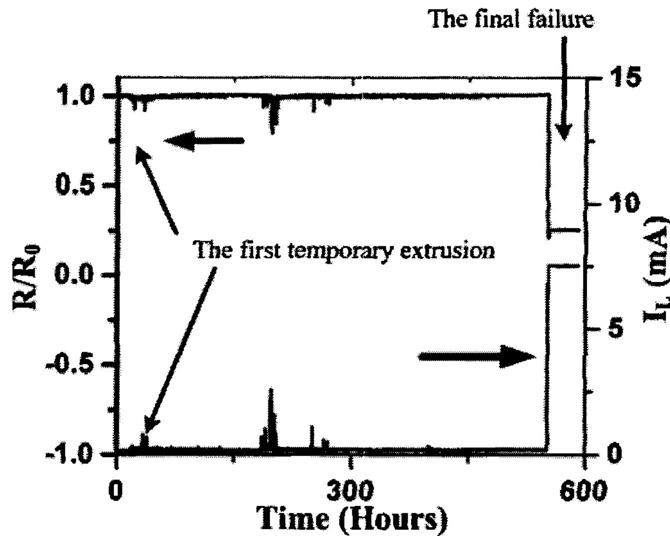


Figure 3.9: Normalized resistance R/R_0 and leakage current I_L versus time curves showing that temporary extrusion failures can reduce the lifetime tremendously. (Sample 19, M7, 350 °C,bidirectional square wave (0 dc offset), $8MA/cm^2$ (peak), f = 1Hz, $R_1 = 47\ \Omega$, $R_0 = 939.04\ \Omega$).

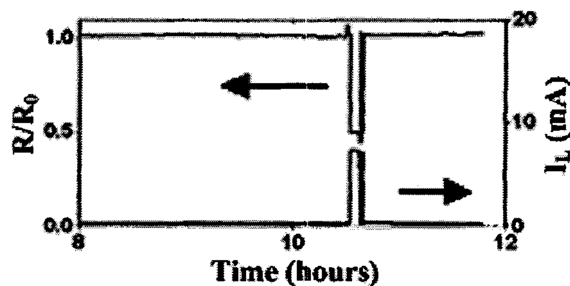


Figure 3.10: Normalized resistance R/R_0 and leakage current I_L versus time: Sample 10, M6 at 350 °C, dc $8MA/cm^2$, $R_1 = 47\ \Omega$, showing a temporary extrusion forming and self-dissolving rapidly due to the small monitor line series resistor, R_1, $R_0 = 933.11\ \Omega$.

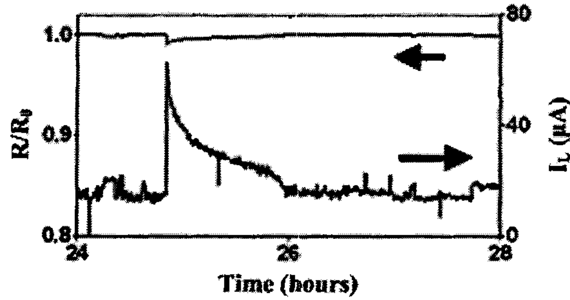


Figure 3.11: R/R_0 and I_L versus time: Sample 12, M7 at 350 °C, dc $6MA/cm^2$, $R_1 = 19.98k\ \Omega$, showing a temporary extrusion forming and self-dissolving slowly due to the large monitor line series resistor, R_1, $R_0 = 887.01\ \Omega$.

Electrical Stress inside Extrusion	Number of failed samples	
	Tested	With temporary extrusions
High	14	7
Low	6	1

Table 3.3: Temporary extrusions happened more frequently with a strong electrical stress inside the extrusion.

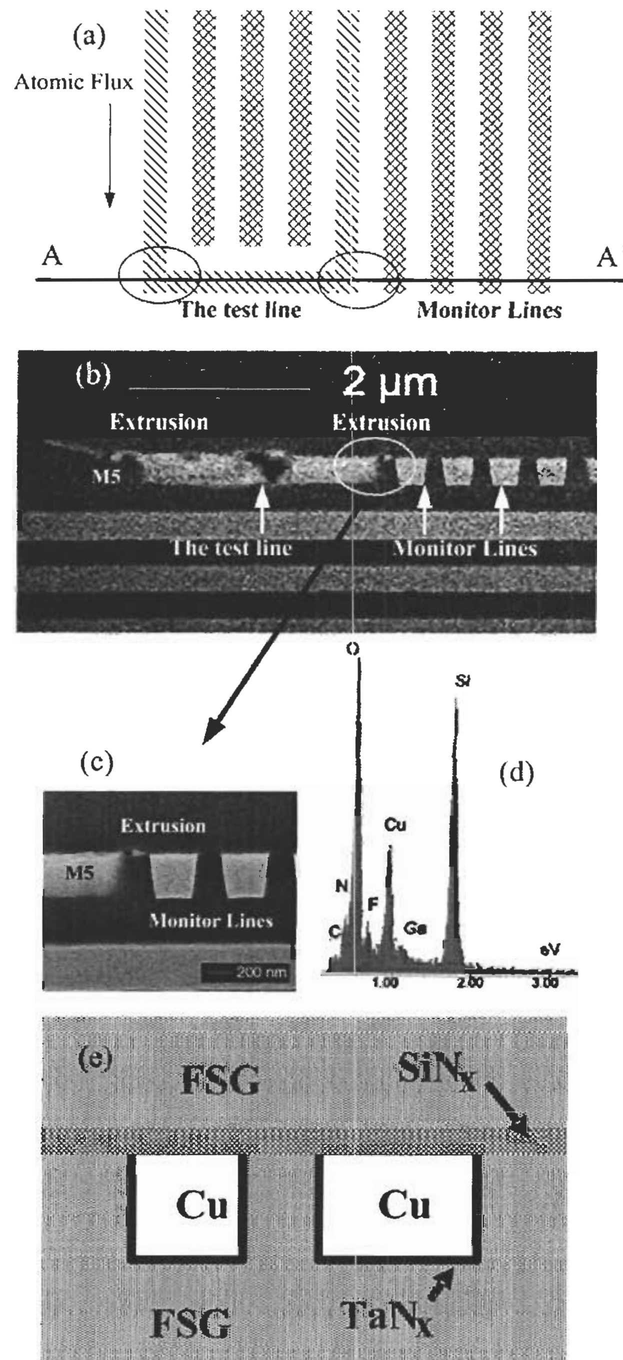


Figure 3.12: Failure analysis of a test structure at M5 tested under 300 °C, dc $5MA/cm^2$, $R_0 = 854.70\ \Omega$ (Sample 8). (a) A diagram shows the location of the cross-section interface indicated by A-A'. (b)The back-scattered electron SEM cross-sectional image shows extrusions formed at corners and a void was located in the test line ($V_{Ebeam} = 5kV$). (c) A high magnitude image of a likely temporary extrusion failure site ($V_{Ebeam} = 5kV$). (d) EDS spectrum of the extrusion in (b)(c) (Ga comes from the FIB). (e) A cross-sectional diagram of the material composition of the failure site.

3.2.2 Void Failures

Voids existed in all of our samples although they were probably not deadly to the circuit. They were also distributed everywhere in the test line as were extrusions, for the same reasons discussed in Chapter 3.2.1. In particular, the first corner of the test line (from the cathode end) had the highest probability to form a void. This was where the transition region occurred between a wide and a narrow part of the test line, and the corner here also induced extra flux divergence, Figure 2.3(c). These two geometrical characteristics resulted in the weakest point of the test line. Figure 3.13 shows a failure in this location (sample 15).

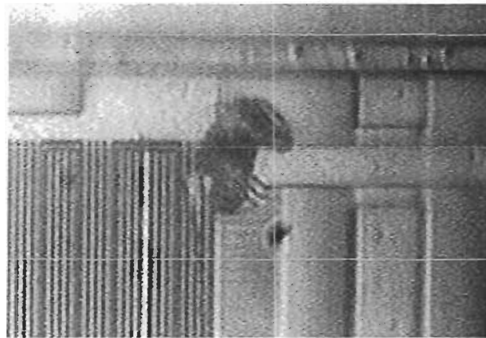


Figure 3.13: An optical image showing a failure site located in the first corner of the test line (M7) (close to the cathode end). The sample was tested at 350 °C, dc $8MA/cm^2$, $R_1 = 19.98k\ \Omega$, $R_0 = 939.25\ \Omega$, and failed by open circuit (Sample 15).

As we discussed in previous sections, the shape of voids tended to be stripe-like, extending along the top surface of the metal line without open circuit failures. Figure 3.14 shows an SEM image of an example failure (sample 11).

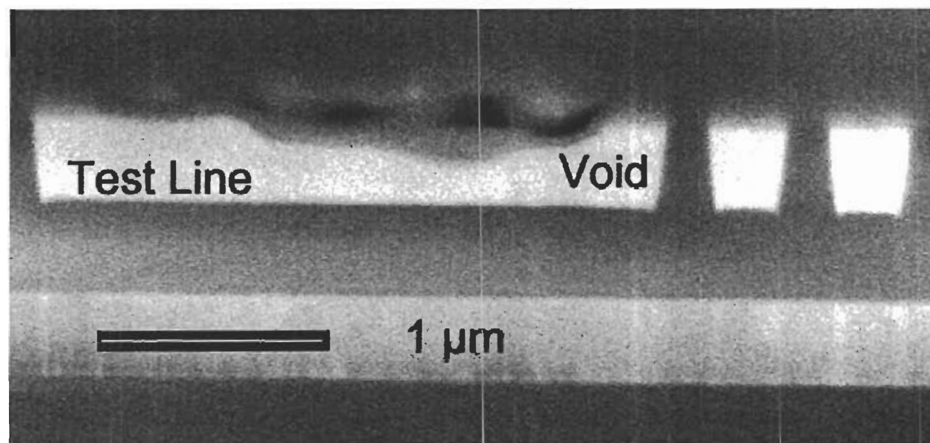


Figure 3.14: A scanning electron SEM cross-sectional image showing a stripe-like void extending along the top surface of the metal line ($V_{Ebeam} = 10kV$). The sample (M7) was tested at 350 °C, dc $8MA/cm^2$, $R_1 = 47\ \Omega$. (Sample 11)

Chapter 4

Discussion

4.1 Dissolution Mechanisms of Temporary Extrusions

Two mechanisms for the dissolution of temporary extrusion failures are proposed according to literature reports and our previous research. These include local melting and shape evolution by diffusion.

4.1.1 Local Melting

Local melting has been reported in electromigration stress tests with Al interconnects, generating voids by evaporation [83]. This results from strong Joule heating and can cause failure within a short period.

Since extrusions typically have much smaller cross-sectional areas than the test line, significant Joule heating is expected to occur when a fraction of the stress current passes through an extrusion. It is therefore easy to suspect that local melting would happen in this situation and a high local temperature could "burn" the extrusion away. This mechanism is able to explain the self-dissolution of temporary extrusions that experienced a large current density. However, local melting was not applicable to the case shown in Figure 3.11. In this situation, since a large R_1 was implemented,

only a tiny current passed the extrusion and the increase of the temperature should be negligible. For example, if we take the width of a typical extrusion as 0.5 μm according to Figure 3.6 and the thickness as 40 nm according to Figure 3.7, when a current of 60 μA passes the extrusion (similar to the case R_1=19.98 $k\Omega$, Figure 3.11) the corresponding current density will be 0.3 MA/cm^2, less than the current density inside the test line and a Joule heating effect can be ignored.

4.1.2 Shape Evolution Model of Extrusions

Since local melting cannot explain all temporary extrusion failures, another mechanism is proposed. The shape evolution of Cu extrusions under both capillary and electron wind forces were modeled in this project. Our modeling results showed that an extrusion could self-rupture due to its varying shape, resulting in a temporary failure, as we described in the last chapter.

The shape evolution model of Cu extrusions was developed from our previous void model. Extensive research has been conducted on void shape evolution of Al interconnects under electromigration stress. With the transition from Al to Cu interconnects, voids tend to extend laterally along the surface instead of undergoing localized growth, causing catastrophic open circuit failure. Along with other universities and companies, our group has developed a novel model to explore this new situation and it is the basis of the shape evolution model for extrusions presented here.

4.1.2.1 Void Shape Evolution Model of Cu Conductors

An axisymmetric model void, using a cylindrical Cartesian coordinated system, is considered, as shown in Figure 4.1. The shape evolution of an initial semi-circular void, located at the copper/dielectric interface, is simulated. The surrounding material is insulating dielectrics and the contact angle between the void boundary and the

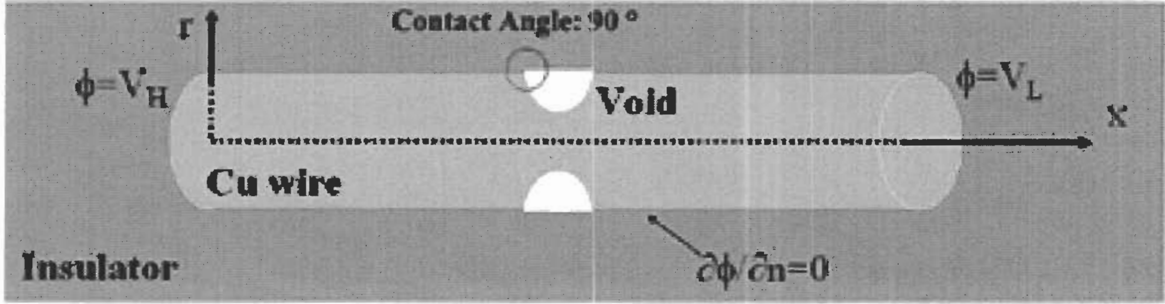


Figure 4.1: Schematic of axisymmetric 3D modeling where a void is located on Cu/insulator interface.

surface of the Cu conductor was fixed as 90°. Since nearly all failures happen along the top surface of metal lines in Cu interconnects, we have not taken the Cu/barrier interfaces into account. The volume of the void was assumed to be constant. As we discussed in Chapter 1, diffusion along the void surface was assumed to dominate.

The surface atomic flux gives the rate of mass transport, proportional to the gradient in potential energy. Generally speaking, the surface potential energy includes two parts: the electrical potential and the chemical potential, and the latter can be described as [69]:

$$\mu = \mu_0 + \Omega(\phi - \gamma_s \kappa) \quad , \tag{4.1}$$

where μ_0 is the bulk chemical potential, Ω is the atomic volume, $\phi = \frac{1}{2}\sigma\varepsilon$ is the elastic strain energy density, σ and ε are local stress and strain tensors, respectively [70], γ_s is the surface free energy and κ is the surface curvature. κ will be positive if the surface is concave (such as a void surface) and negative if the surface is convex (a hillock, for example).

The total surface atomic flux, J_s can be obtained through Fick's law [71]:

$$J_s = -M\nabla_s \mu = MF \quad , \tag{4.2}$$

where M is the surface atomic mobility which is given by the Einstein relation, defined

as $(D_s\delta_s)/(\Omega kT) * \exp(-Q_s/kT)$ [69][71], where D_s is the surface diffusivity at a specific temperature, δ_s is the thickness of the surface layer, Q_s is the activation energy for surface diffusion, k is the Boltzmann constant, T is the temperature, ∇_s is the surface gradient operator $(\partial/\partial s)$ and F can be considered as the driving force of the atomic diffusion. With the implementation of both electrical and chemical potentials, the following formula was obtained [70]:

$$J_s = M[\Omega\gamma_s\nabla_s\kappa - \Omega\nabla_s\phi - \nabla_s U_e] \quad , \tag{4.3}$$

where U_e is the electric potential, eZ^*V, e is the charge of an electron, Z^* is the effective charge number, and V is the voltage. $(\partial V)/(\partial s) = E_s$, where E_s is the tangential component of the electric field along the void surface.

Equation 4.3 describes the general atomic flux in Cu conductors. The first item reveals that the atomic migration can result from the divergence of surface curvature, atoms moving from the location with high curvature to low curvature to reduce the surface energy. This means that the capillary force drives the migration. The third item indicates that the atomic movement is also due to the gradient of electrical potential. This item points out that the electron wind force (electromigration driving force) is able to move atoms from the cathode to the anode. The second item shows that the atomic migration relates to the difference in elastic strain energy as well. This kinetics induces the atomic back-flow phenomenon [6, 45], as discussed in Chapter 1.1.1.2. However, it has been acknowledged that the divergence of elastic strain energy can be ignored in this model, [72, 73, 74, 77], for two reasons. First, surface diffusion in Cu interconnects dominates instead of grain boundary diffusion as in Al interconnects, resulting in the major migration being due to capillary and electron wind forces. Secondly, Cu extrusions are typically located inside cracks, meaning that they have more free space than regular metal lines to change volume and shape, releasing strain

energy more easily [24, 41]. Therefore, the gradient of stain energy potential will become much less important with Cu extrusions. Due to the above two reasons, we can ignore the mechanical stress in the simulation for both voids and extrusions and equation 4.3 can be simplified to [72, 73, 74, 77]:

$$J_s = M[\Omega\gamma_s\nabla_s\kappa - Z^*eE_s] \quad . \tag{4.4}$$

J_s is the atomic flux, indicating the number of atoms per time crossing unit length on the surface [71]. A positive J_s divergence means the loss of materials and a negative gradient relates to the accumulation of materials. The rate at which material is deposited or removed from a region (measured by the normal velocity of the surface v_n) relates to the divergence of surface flux, J_s, by mass conservation [69, 74, 77, 78]. Accordingly, the following continuity equation was obtained [74, 77]:

$$V_n = -\Omega\nabla_s \cdot J_s \quad , \tag{4.5}$$

For a three-dimensional interfacial evolution, the following partial differential equation was used [73]:

$$V_n = -(\Omega/r)\nabla_s \cdot (J_s r) \quad . \tag{4.6}$$

This equation was used to solve the surface profile, $r(x)$, which showed the surface evolution. In our simulation, Cu lines and extrusions were assumed as perfect conductors and surrounding dielectrics were taken as perfect insulators as well. A finite-difference method was implemented to obtain 1 dimensional grids along the void surface. The electric field required for the flux computation can be expressed as [72, 73, 74]

$$E_s = -\nabla_s\Phi \quad , \tag{4.7}$$

where the electrostatic potential Φ can be calculated from Laplace's equation [72, 73, 74] and the boundary conditions:

$$\nabla^2\Phi = 0. \tag{4.8}$$

$$(\partial\Phi)/(\partial n) = 0. \tag{4.9}$$

Figure 4.2 introduces the simulation process.

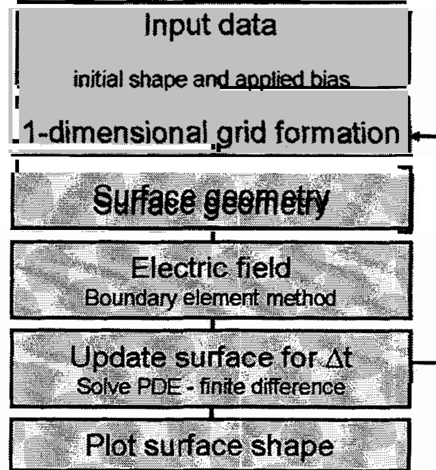


Figure 4.2: A flow chart of the modeling process.

As a result, our void shape evolution model revealed that the capillary force alone was able to rupture a Cu conductor in some specific cases (depending on the volume and the shape of the initial void), while it was formerly considered as only a healing force. This model also showed that the electron wind force and the capillary force could interact with each other, causing different shape evolutions (depending on their ratio, and the initial volume and shape of the void). In some particular cases, the two forces would facilitate the void to extend along the interface, causing global thinning as experimentally observed (Chapter 1.2.2.2).

4.1.2.2 Shape Evolution of Cu Extrusions

Since the shape evolution of both Cu extrusions and voids relies on surface migration due to gradients in chemical potential and electrical potential (Equation 4.4), the theoretical model developed for void shape evolution is also valid for extrusions. However, at the current stage, a two dimensional model is sufficient to simulate extrusions,

while the void has already been simulated by a more complicated three dimensional model.

For a two dimensional model, equation 4.6 changes to [73]:

$$V_n = -(\Omega/y)\nabla_s \cdot (J_s y) \qquad , \tag{4.10}$$

where $y(x)$ is solved to obtain the surface profile of an extrusion and its shape evolution. 1 dimensional grids along the extrusion surface were generated by a finite-difference method. Figure 4.3 is a schematic diagram of a model extrusion of width, 2w, connecting two parallel copper stripes separated by a distance, L. In our simulation, rectangular extrusions were assumed to be long and narrow, such as L/w = 10. They were also assumed to form along the CMP interface between the IMD and capping layers, according to our observations and literature reports [36, 79]. A constant electric potential ($\Delta\Phi$) was assumed to be maintained across the extrusion length. The dashed computational box is shown to indicate the simulated area. (Due to the symmetry, only the upper half of the extrusion was considered.)

For an initial rectangular extrusion without electrical stress, the curvature is zero along the whole surface except at the two connection points to the Cu stripes, where κ is $-\infty$. The surface atomic flux divergence here induces the original driving force for extrusion shape evolution and, finally, the extrusion ruptures itself in the center according to our simulation results. With the integration of electrical stress, electron wind forces start to have effects on the shape evolution. The extrusion is still able to self-rupture, but, the initial rupture point moves to the cathode end.

Our modeling results were explained in terms of two important parameters, the electron wind intensity χ, and the numerical time τ. χ refers to the relative strength of the electron wind force with respect to the capillary force, and was defined as $\chi = Z^{*}ew^2E_0/(\gamma\Omega)$ [73, 74, 80]. Here, Z^{*} is 5 for Cu [74], e is $1.6 \times 10^{-19}C$, w is

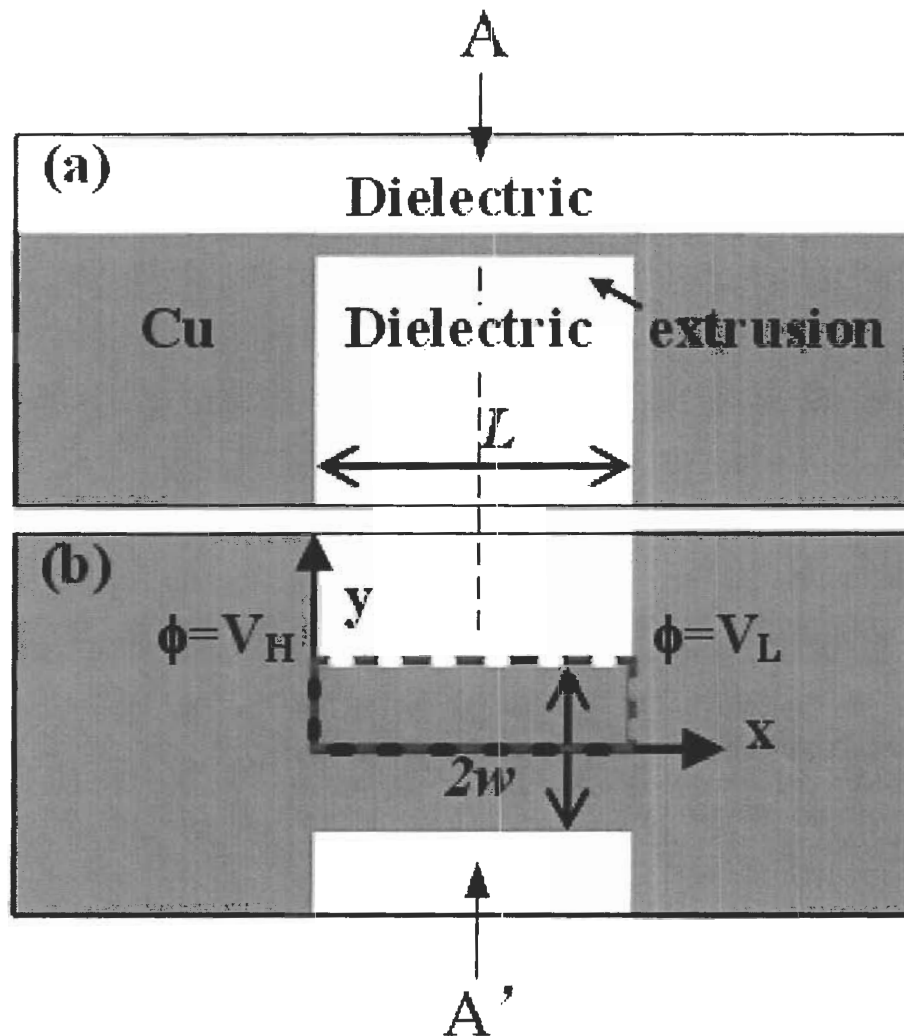


Figure 4.3: Schematic of a copper extrusion developed along the interface between two dielectrics. The extrusion connects the two adjacent copper stripes with space, L. (a) cross-sectional view, (b) planview at the extrusion level. Electrostatic boundary conditions are specified. In (b), the dashed computational box is shown where a two-dimensional rectangular extrusion with length, L, and half-width, w, is considered. The simulation results for the shape evolution of this box will be illustrated in following figures. y=0 is the mirror plane.

characteristic width, E_0 is the electric field across the extrusion, Ω is the Cu atomic volume, $1.2 \times 10^{-29} m^3$, and the specific Cu interface free energy γ is 1.7 $Joules/m^2$ [81]. All physical parameters here are appropriate for a Cu wire, a quarter micron in width at 600 K [72]. When w is taken as the line width, 0.25 μm, and the applied current density, $J = 3MA/cm^2$, $\chi \sim 1$, representing a typical electromigration stress condition. In our particular case, since $L/w = 10$ and L was measured as 0.16 μm (Table 2.1), w was taken as 16 nm.

The numerical time τ is a dimensionless quantity $= tD_s\delta\Omega\gamma/[w^4kT]$, where t is the actual simulation time, D is $3.3 \times 10^{-14} m^2/s$, and δ is $3.5 \times 10^{-10} m$ [72, 73, 80]. With our model extrusion, when $t = 2.3$ seconds, τ is 1. Furthermore, an appropriate $\Delta\tau$ can optimize the computation performance. A large $\Delta\tau$ may speed up the computing time, however it may result in a numerically unstable solution such as a saw-tooth type profile. In order to improve the efficiency of the modeling, $\Delta\tau$ was not fixed in our simulation process and an adaptive $\Delta\tau$ was implemented, which increased its magnitude during the iteration as long as the solution convergence was guaranteed. For a fixed $\Delta\tau$ throughout the computation, the total evolution time, τ was given by $\Delta\tau \times N$, where N was the number of iterations. If the adaptive method was implemented, actual τ could be obtained by $\sum \Delta\tau_i$. The usual number of iterations in our calculation was about 1 million and the simulation program would check whether the extrusion was ruptured when the number of iterations increased by one order (i.e. $10 \rightarrow 100$). Whenever the rupture happened, the simulation would stop automatically.

The leakage current, I_L at each moment was calculated after the simulation as well. Since we assumed the Cu extrusion was a perfect conductor, its resistivity should be uniform everywhere and the resistance of a small slice of the extrusion, R_i, should totally depend on its cross-sectional area (along A-A' interface in Figure 4.3).

Therefore, we divided the whole extrusion into nearly a hundred elements according to the 1 dimensional grids along the extrusion surface. The total resistance of the extrusion $R_{ex} = \sum R_i$. When the extrusion approached rupture, R_{ex} would increase to ∞ and I_L would drop to zero.

The shape evolution was simulated under three conditions, χ was 0, 0.1 and 1, representing an electron wind force increasing from 0 to a strong force. When χ equaled 0.1 and 1, E_0 would be $9.961 \times 10^3 V/m$ and $9.961 \times 10^4 V/m$, respectively. In all three cases, the extrusion did finally self-rupture. When χ was 0, the rupturing site was the center of the extrusion and the Cu conductor was prone to shrink to 2 spheres by the capillary force, minimizing the surface energy. With the increase in electron wind force, the rupturing site moved to the cathode end because the electromigrating atoms moved to the anode end.

Figure 4.4, 4.5 and 4.6 show the simulation results. The electric field direction was from left to right. Only the upper half of the extrusion shape (the dashed computational box in figure 4.3(b)) was shown on a normalized x and y scales, y = 0 plane was assumed a mirror plane.

This simulation work successfully explained why our extrusions only lived temporarily in all cases, modeling a self-rupturing process. Furthermore, extrusion lifetimes were simulated by τ and I_L, comparable to measured I_L versus t curves. When I_L dropped to zero, extrusion failures were considered to have self-dissolved and the moment in τ was the lifetime of our temporary extrusions. Figure 4.7 is the time dependent leakage current and reveals that with increasing χ, the time for extrusion to rupture, τ, reduces significantly. This fact is consistent with our experimental observations. When a small R_1 was implemented, temporary extrusions happened more

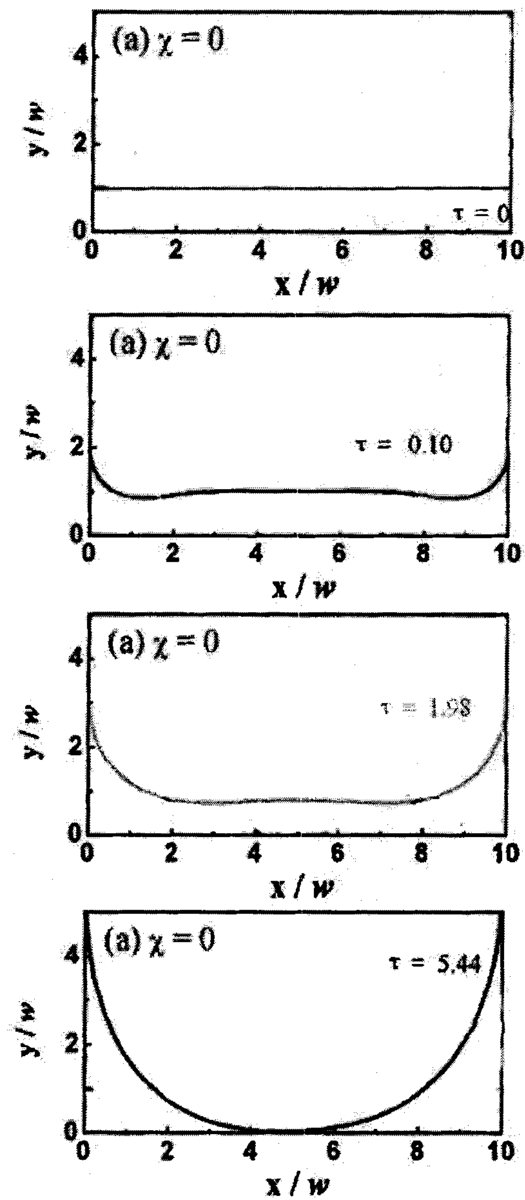


Figure 4.4: The shape evolution of the upper half of an extrusion introduced in Figure 4.3, for no electron wind force $\chi = 0$. L = 0.16 μm and L/w = 10.

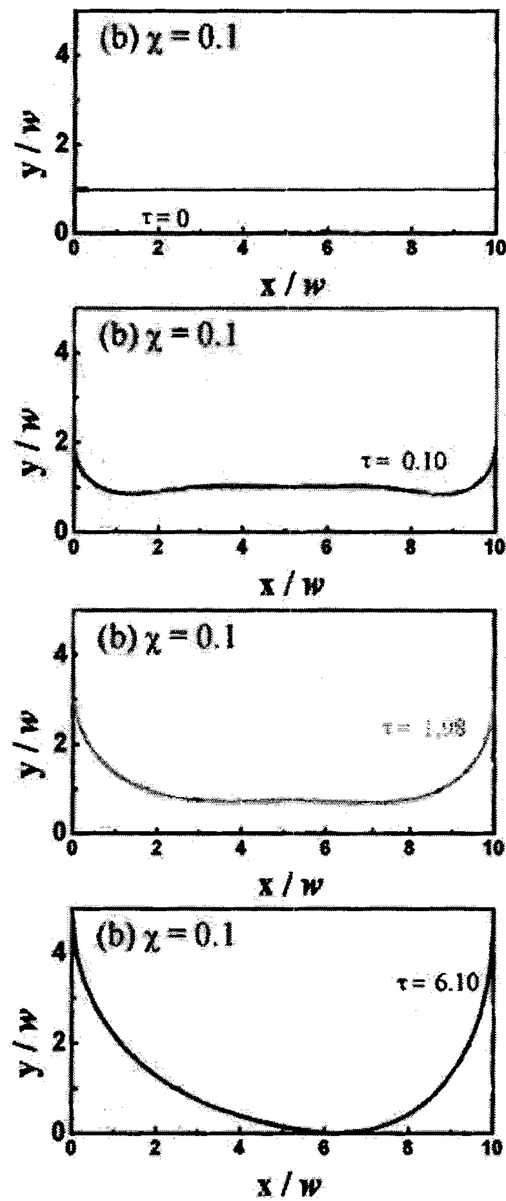


Figure 4.5: The shape evolution of the upper half of an extrusion introduced in Figure 4.3, for a relative electron wind force $\chi = 0.1$ (directed from left to right). L = 0.16 μm and L/w = 10.

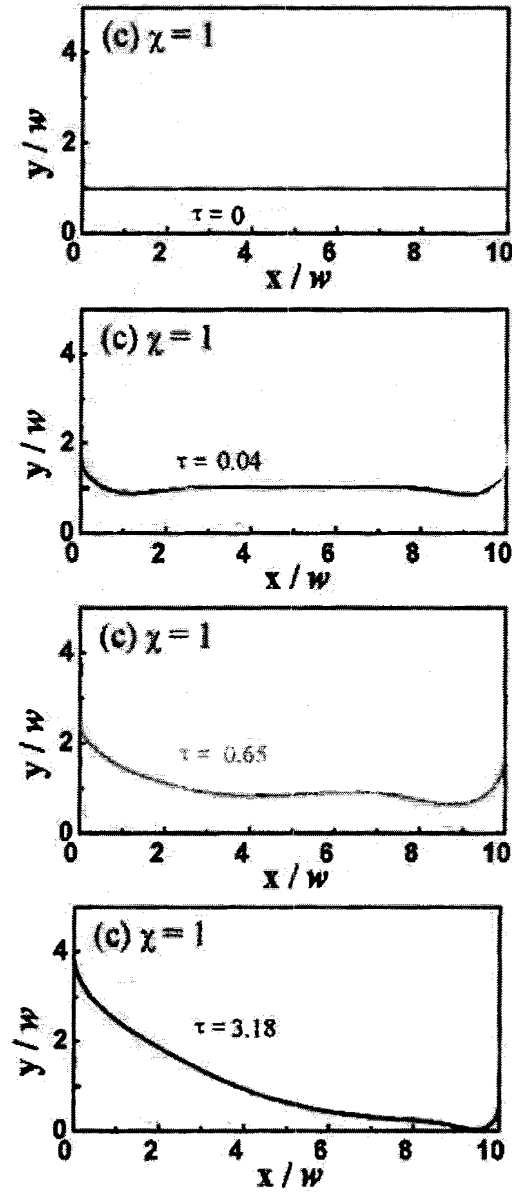


Figure 4.6: The shape evolution of the upper half of an extrusion introduced in Figure 4.3, for a relative electron wind force $\chi = 1$ (directed from left to right). L = 0.16 μm and L/w = 10.

frequently and their lifetimes were shorter than when a large R_1 was used. Particularly, the shape of I_L versus τ curves at $\chi = 0.1$ and 1 look similar as the one in Figure 3.11, while the shape at $\chi = 5$ is the same as the one in Figure 3.10.

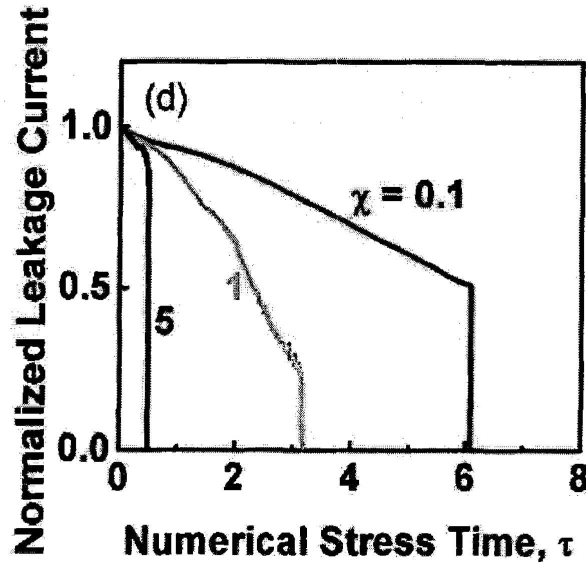


Figure 4.7: Leakage current, I_L, normalized by the initial current passing through the extrusion for $\chi = 0.1$, 1 and 5, are plotted as a function of numerical stress time τ, assuming a constant potential across the extrusion. L = 0.16 μm and L/w = 10.

It is important to note that so far, the lifetimes of our model extrusions can only qualitatively match the experimental results. More details have to be considered if a quantitative analysis is necessary. Further work needs to be conducted to extend this model to bidirectional test conditions.

4.2 The Effects of Temporary Extrusion Failures

Our group was the first to report temporary extrusion failures, while permanent extrusion failures are well known. This is probably because in standard electromigration

tests, the stress and data gathering will typically stop whenever a failure happens. Moreover, since it is common that an electromigration test takes several days to a month, engineers do not sample parameters at high frequencies (we used every 15 seconds). In this case, temporary failures are likely missed.

For ICs working under normal conditions, the current density and working temperature are much lower than ICs in accelerated tests. Therefore, whenever an extrusion forms, the surface diffusion will be slow due to a low temperature, and the χ inside the extrusion will be relatively small because of the low current density. As a result, although temporary extrusion failures exist for short times in accelerated-stress tests, they would qualify as long-term failures under real working conditions.

Temporary extrusion failure detection is also important when engineers estimate the lifetime of ICs to validate the fabrication process. This new failure mode can shorten the lifetime up to 90% in our results. If they are missed, an over-optimistic lifetime evaluation will be made from accelerated stress tests.

Chapter 5

Conclusions

The nature of electromigration was reviewed in this thesis, particularly for electromigration in Cu interconnects. DC electromigration tests were carried out on 0.13 μm technology, Cu dual-damascene interconnects. Preliminary one and two directional square wave tests were also conducted. The failure behaviors of our samples were carefully examined. As a result, a novel failure mode, temporary extrusions, was found. These extrusions formed based on a sudden decrease in resistance and increase in leakage current, self-dissolving after a short period with the circuit resistance and leakage current returning to relative stability again. Such temporary failures typically existed for a minute to more than an hour. Compared to the final permanent failures, they shortened the lifetime by as much as 90%. Further characterization also showed that temporary extrusion failures happened more frequently, existed within a shorter period, and the recovering process occurred more quickly, when a large electrical stress existed inside the extrusion compared to a small stress. We also developed a two-dimensional shape evolution model of the extrusions which successfully modeled the temporary failure as a self-rupture of the extrusion. The capillary force and the electron wind force interact together inside extrusions, determining the shape evolution. Finally, a recommendation is made for a high data sampling frequency in

electromigration tests, to prevent missing the detection of these temporary failures.

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