DESIGN METHODOLOGY FOR CONTINUOUS–TIME BANDPASS SIGMA–DELTA MODULATORS

by

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Abstract

This dissertation concerns the investigation of current problems associated with the analysis and design of *tunable continuous time bandpass* (CT BP) *sigma–delta* ($\Sigma\Delta$) modulators. This specific modulator group is particularly promising within the context of software–defined radios. However, due to the nonlinear sampling element within a closed–loop s–domain system, the high level of analytical complexity makes current CT BP $\Sigma\Delta$ modulators difficult to implement.

Specific problems addressed in this research were the fundamental principles of the $\Sigma\Delta$ modulation process, analytical and design methodology, loop delay compensation techniques, monolithic implementation and possible application areas. Theoretical general closed form solutions for the center frequency tunable CT BP $\Sigma\Delta$ modulator with fractional delays were derived, defining a new sub–class of fractional CT BP $\Sigma\Delta$ modulators. The developed sub–class offers numerous possible solutions to existing problems in $\Sigma\Delta$ modulator based circuits, such as loop delay compensation and signal upconversion. A theoretical CT BP $\Sigma\Delta$ design methodology was then modified to be suitable for mixed–signal integrated circuit (IC) design flow, currently used in both industrial and academic environments. In order to experimentally demonstrate these new analytical concepts, an IC prototype of the proposed fractional $\Sigma\Delta$ modulator was designed, manufactured in SiGe technology, and tested.

This research showed that the developed fractional CT BP $\Sigma\Delta$ modulator concept is a feasible option for future wireless networks; thus providing the crucial element required for software–defined radios.

To Anna and Allen

" I do not know what I may appear to the world, but to myself I seem to have been only a boy playing on the sea–shore, and diverting myself in now and then finding a smoother pebble or a prettier shell than ordinary, whilst the great ocean of truth lay all undiscovered before me....

If I have seen farther than others, it is because I was standing on the shoulder of giants. "

— Sir Isaac Newton (1642 – 1727)

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Abbreviations

A/D	Analog–to–digital
ADC	Analog–to–digital converter
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar junction transistor
BP	Band–pass
BW	Band width
CMOS	Complementary Metal Oxide Semiconductor
CM	Common–mode
CT	Continuous–time
D/A	Digital–to–analog
DAC	Digital–to–analog converter
DFT	Discrete Fourier transformation
$\mathbf{DC}_{pwr}$	Direct current power
DR	Dynamic range
DT	Discrete–time
ECL	Emitter–coupled logic
FFT	Fast Fourier transformation
f_s	Sampling frequency
$f\Sigma\Delta$	CT BP $\Sigma\Delta$ modulator with fractional delay
GaAs	Gallium–Arsenide
g_m–C , $\mathbf{G}_m$–**C**	Transconductance–capacitor
HF	High frequency
HZ	Hold–return–to–zero
IF	Intermediate frequency
IIP3	Input third–order intercept point

InGaAs	Indium–Gallium–Arsenide
LP	Low–pass
LC	Inductor–Capacitor
NTF	Noise transfer function
NRZ	Non–return–to–zero
RF	Radio frequency
RZ	Return–to–zero
OSR	Oversampling ratio
PA	Power amplifier
PLL	Phase–locked–Loop
RZ	Return–to–zero
rms, RMS	Root–mean–square
SC	Switched–capacitor
SI	Switched–current
SiGe	Silicon–Germanium
$\Sigma\Delta$	Sigma–Delta
SNDR	Signal–to–noise–plus–distortion ratio
SNR	Signal–to–noise ratio
STF	Signal transfer function
UI	Unit interval
VCO	Voltage–controlled oscillator

Preface

Despite its long history, apparent simplicity, and elegance, a sigma–delta ($\Sigma\Delta$) modulator remains one of the most elusive circuits in microelectronics. So far, no researcher has presented a comprehensive analysis and model which completely and accurately describes all aspects of the circuit's operation. Rather, circuit developments have resulted from work carried out by a large number of contributors, with only incremental advances in inner circuit operation knowledge.

The goal of this dissertation was to investigate current problems associated with the analysis and design of a center frequency tunable continuous time bandpass (CT BP) $\Sigma\Delta$ modulator, in the high frequency (HF) signal range. Although the concept of $\Sigma\Delta$ modulation has existed for more than 40 years, there are still a number of outstanding problems related to this particular group of modulators; for example, loop delay compensation, center frequency tunability, and higher order stability. However, in the HF range, this group of modulators could potentially resolve some of the critical issues of the software–defined radio. It appears that $\Sigma\Delta$ modulators have the potential to include a tunable frequency element, combined with frequency mixing, A/D conversion, and a filtering function, in a single device. Clearly, there is enough motivation to invest more research efforts in this area.

This research proposes to investigate and solve numerous interesting and important questions regarding $\Sigma\Delta$ modulators, including:

- Can the SNR level of a HF signal become as high as the levels previously demonstrated in the audio frequency range?
- What is the closed form solution for the 4^{th} and 6^{th} order center frequency tunable CT BP $\Sigma\Delta$ modulators?

- What design methodology should be used and how should it fit into the current IC design flow?
- What IC implementation issues are to be resolved?
- How can the loop delay compensation problem be solved?
- How does noise contribution affect the system?
- What architecture has the lowest nonlinearity?
- Can higher order stability be accurately predicted, particularly for the maximum SNR?

Naturally, while attempting to solve these problems, others may be exposed. It is hypothesized that both theoretical and experimental work presented in this dissertation will offer some partial answers to, at least, some of these questions.

After completing the theoretical work, it is important to consider the operational speed for design implementation. Higher operational speeds are generally achieved by exploiting fast technologies, such as GaAs. In addition, a higher SNR can be achieved using a higher oversampling ratio; however, power consumption then becomes an issue. The conclusion is reached that modulators of higher order are needed; this implies that system stability must first be examined. Conversely, if the modulators are tuned to any frequency relative to the sampling clock, i.e. f_s/n type as opposed to the $f_s/4$ type, there is the potential for better utilization of the modulator functionality (frequency translation) and a reduction in power consumption through the use of lower clock frequencies.

The problem of achieving higher SNR values in high frequency CT BP $\Sigma\Delta$ modulators is still far from being solved; especially when compared to the $150\,dB$ (24bit) accuracy already achieved in the audio frequency range. The oversampling method has an upper limitation imposed by the power consumption. Thus, the exploitation of either oversampling or undersampling systems with f_s/n may be a better alternative.

Traditionally, initial analysis and behavioral models are developed in environments that are incompatible with the tools used during actual IC design. For example, a standard approach is to develop the internal behavioral $\Sigma\Delta$ models in a programming language, such as C or MATLAB. Thus, during the design process, this design flow requires that some form of manual interfacing, data remapping, and translation occur. Furthermore, all lower level IC blocks must be finished prior to simulating the top level. In closed–loop systems, such

as phase–locked loop (PLL) and $\Sigma\Delta$ loops, the simulation time becomes a limiting factor in the top level design; this means that only a fraction of the transistor level simulations can be performed within the allocated design time. Development of behavioral models that are compatible with the standard IC design environment creates new possibilities for better system verification. In these cases, simulation setup can contain one of the transistor–level sub–blocks, with the rest of the system remaining in behavioral form; thus, significantly reducing the simulation time.

System tunability is an aspect that still requires additional analytical research. While the numerical methods generally used to design the loop filter function do produce valid results, analytical methods may contribute more to the fundamental understanding of the problem.

The loop delay in CT systems also requires further exploration. In this dissertation, a novel method of compensating the loop delay was proposed, which introduced a new sub–class of fractional $\Sigma\Delta$ modulators. Rather than trying to remove the unavoidable loop delay, an argument was made for its utilization and incorporation in the loop filter design. The development of the fractional delay scheme allowed for the possibility of tolerating loop delays that are only fractions of a sampling period.

Chapter 1

Introduction

The principles of Delta–Modulation were first introduced in patent by C.C. Cutler, filed in 1954 and granted in 1960 [9]. Since that time, numerous papers, designs, books and chapters have been published on the topic [36, 27]. Today, a large number of circuit designs have emerged from this classical feedback loop concept, known as the sigma–delta ($\Sigma\Delta$) modulator. Regardless of the specific design, all $\Sigma\Delta$ modulator loops contain at least the following functional blocks: summing circuit at the input, loop filter, sampled A/D converter at the output, and D/A converter in the feedback loop.

In order to define the focus of this dissertation, the following classifications are arbitrarily introduced. Conceptually, the family of $\Sigma\Delta$ circuits can be divided into two groups: discrete–time (DT) and continuous–time (CT). This categorization is based solely on the time domain characteristics of the $\Sigma\Delta$ loop filter. If the filter was designed in the z–domain, i.e. implemented as either a switched capacitor (SC) or switched current (SI) filter, then the $\Sigma\Delta$ modulator is referred to as a DT $\Sigma\Delta$ modulator. Similarly, if the filter was designed in the s–domain, then the $\Sigma\Delta$ modulator is designated as a CT $\Sigma\Delta$ modulator. The next level of classification is based on the filter type: low–pass (LP) or band–pass (BP) $\Sigma\Delta$ modulator. Regardless of the filter type, a connection can be made to either a one–bit or multi–bit A/D converter. The general assumption is that the feedback D/A converter has the same number of bits as the A/D converter.

Lastly, the relationship between the input signal frequency and the A/D sampling frequency is investigated. According to the Nyquist criteria, oversampled and undersampled $\Sigma\Delta$ modulators are defined.

1.1 Analog to digital conversion

The conversion of CT signals into their corresponding DT signals (and vice–versa) has been one of the most important tasks in signal processing since the digital age began; particularly due to the VLSI explosion which occurred during the last 30 years of the 20^{th} century. Digital signal processing enabled simpler design methodologies, resulting in noise margin and circuit reliability increases and reductions in both integrated circuit (IC) chip area and power consumption.

At the most fundamental level, all signals are continuous, regardless of the mathematics (z–domain or s–domain) used to describe them. From a practical implementation perspective, z–domain based circuits suffer from speed limitations, as they require an operational sampling clock; s–domain based circuits suffer from complex design methodology, generally lower signal margins and potentially higher power consumption. A modern mixed–signal approach, which merges the two design methodologies into the same circuit, often results in the most efficient designs. Consequently, new models, design methodologies and tools are being developed to facilitate the merger of these two widely separated domains.

1.2 State of the art

With the exception of a few milestone works, referenced for completeness, this section reviews CT BP $\Sigma\Delta$ modulator designs which were supported by the experimental data. Note that a large number of publications related to z–domain and s–domain (simulation results only) designs are beyond the scope of this work.

In the late 1980s contributions to the fundamental understanding of bandpass $\Sigma\Delta$ modulation operation have been very significant. In 1989, Schreier *et al.* [47] published one of the first theoretical works dedicated to the bandpass transfer function. Several papers by Jantzi *et al.* [23, 24] contributed a working methodology for calculating the noise transfer function (NTF) and signal transfer function (STF) for a $\Sigma\Delta$ loop.

The first CT BP $\Sigma\Delta$ modulator was presented in 1990 by Dressler [12], where the low–pass filter inside $\Sigma\Delta$ loop was intuitively replaced with a resonator to achieve the bandpass effect. A summary of the experimental data for this 2^{nd} order, discrete implementation design is as follows: signal to noise ratio (SNR) $= 55\,dB$, center frequency $f_0 = 2.5\,MHz$, bandwidth (BW) $= 80\,kHz$, and clock frequency $f_{clk} = 10\,MHz$.

Further advances were made in 1991 by Thurston *et al.* [55], who suggested a method for determining the analytical expression for a bandpass loop filter transfer function, $H(s)$, in the s–domain. Their research demonstrated the first application of the impulse invariant transformation technique for performing the domain transformation $H(z) \rightarrow H(s)$, in order to solve for the CT BP $\Sigma\Delta$ loop filter transfer function. This concept, driven by emerging cellular networks, was proved through experiment, thus paving the way for future CT BP $\Sigma\Delta$ research. A summary of the experimental data for this 2^{nd} order, discrete implementation design is as follows: $SNR = 50\,dB$, $f_0 = 7.5\,MHz$, $BW = 100\,kHz$, and $f_{clk} = 10\,MHz$. Also in the same year, while not strictly in the CT category, Horrocks [20] proposed a tunable center frequency, 2^{nd} order z–domain bandpass filter.

In May of 1992, Jantzi *et al.* [25] published the first monolithic implementation of a BP $\Sigma\Delta$ modulator. A summary of the 4^{th} order, switched capacitor (SC) implementation design is as follows: $3\mu m$ CMOS technology, $SNR = 63\,dB$, $f_0 = 455\,kHz$, $BW = 10\,kHz$ and $f_{clk} = 1.82\,MHz$. Then in June, Tröster *et al.* [56] published the first monolithic implementation of a CT BP $\Sigma\Delta$ modulator. With cellular network application in mind, they used a BiCMOS analog/digital array. A summary of the 2^{nd} order monolithic implementation, with an external LC resonator is as follows: $1.2\mu m/7\,GHz$ BiCMOS analog/digital array technology, $SNR = 55\,dB$, $f_0 = 6.5\,MHz$, $BW = 200\,kHz$, and $f_{clk} = 26\,MHz$.

In 1995, Shoaei [48] contributed an analytical methodology for s–domain CT BP $\Sigma\Delta$ modulator analysis and design, covering both 2^{nd} and 4^{th} order modulators. In addition, an alternative method for $H(s)$ synthesis, for the quarter of the sampling frequency ($f_s/4$) CT BP $\Sigma\Delta$ modulator, was introduced.

A 2^{nd} order tunable g_m–C based CT BP $\Sigma\Delta$ modulator, with programmable center frequency $f_0 = 24.4MHz/62.5\,MHz$, was developed by Raghavan *et al.* in 1997 [41]. Taking advantage of the high clock speed, i.e. high oversampling ratio (OSR), in fast InGaAs technology, an $SNR = 92\,dB$ was achieved. The reported data for this implementation was: InGaAs technology, area $750\mu m \times 750\mu m$, power dissipation $DC_{pwr} = 1.4W$, $SNR = 92\,dB$, $f_0 = 55.6\,MHz$, $BW = 366\,kHz$, and $f_{clk} = 4\,GHz$. Also published in 1997, was a 4^{th} order modulator design developed by Jayaraman [26]. He investigated the application of a power amplifier (PA) in combination with a $\Sigma\Delta$ modulator. A summary of the reported data is as follows: GaAs technology, $SNR = 63\,dB$, $f_0 = 800\,MHz$, $BW = 200\,kHz$, and $f_{clk} = 3.2\,GHz$.

In 1998, Gao *et al.* [16] developed a 2^{nd} order design, claiming it to be the first design

in the GHz range including on–chip LC components. This design exhibited: $0.5\mu m$ BJT technology, $SNR = 57\,dB$, $f_0 = 950\,MHz$, $BW = 200\,kHz$, and $f_{clk} = 3.8\,GHz$. Currently, this design has the highest reported center frequency. In the same time he reported a 4^{th} order design with the following data [15]: $V_{CC} = 5.0V$, $DC_{pwr} = 350mW$, area $0.85mm \times 1.46mm$, $f_{clk} = 4.0\,GHz$, $BW = 4\,MHz$, $f_0 = 1\,GHz$, $SNR = 53\,dB$.

The first working design of a 6^{th} order CT BP $\Sigma\Delta$ modulator was developed by van Engelen *et al.* in 1999 [57]. Published data for this implementation is as follows: $0.5\mu m$ CMOS technology, $SNDR = 67\,dB$, $f_0 = 10.7\,MHz$, $BW = 200\,kHz$, $f_{clk} = 30/80\,MHz$. During the same year, Tao [54] demonstrated his downconversion frequency translation approach, using a 2^{th} order modulator as the downconverter. This design used discrete inductors with an SC integrator. A summary of the reported data is as follows: $0.35\mu m$ CMOS technology, $SNDR = 54\,dB$, $f_0 = 100\,MHz$, $BW = 200\,kHz$, and $f_{clk} = 400\,MHz$.

A comprehensive study on the excess loop delay, with a novel approach to compensation, was published in 2000 by Maurino *et al.* [35]. A summary of the experimental data for this 4^{th} order design is as follows: SiGe technology, $SNR = 68\,dB$, $f_0 = 200\,MHz$, $BW = 200\,kHz$, and $f_{clk} = 800\,MHz$. The following year, Raghavan *et al.* [40] developed the second generation of their InGaAs design, a 4^{th} order CT BP $\Sigma\Delta$ modulator. They reported the following data for their implementation: power supply $V_{CC} = \pm 5V$, power dissipation $DC_{pwr} = 3.2W$, area $3.3mm \times 1.7mm$, $SNR = 75.8\,dB$, $f_0 = 180\,MHz$, $BW = 1\,MHz$, and $f_{clk} = 4\,GHz$.

One of the most accomplished designs so far was developed in 2002 by Schreier *et al.* [46], where a robust industrial mixed–signal approach was used to design their commercially available chip. Their 6^{th} order CT design used external inductors for the first resonator, RC (with trimming capacitors tolerant to within 1%) for the second resonator, and SC for the third resonator. They reported the following data for their implementation: $0.35\mu m$ BiCMOS technology, power supply $V_{CC} = 2.7V$, power dissipation $DC_{pwr} = 50mW$, area $5.0mm^2$, tunable range $10/300\,MHz$, $BW = 333\,kHz$, $SNR = 81\,dB$, and $f_{clk} = 3/32\,MHz$. In the same journal issue, the group lead by Henkel published their design of 4^{th} order CT design in $0.65\mu m$ BiCMOS technology [18]. Their results demonstrated that if quadrature CT $\Sigma\Delta$ modulation is used, the anti–aliasing IF bandpass filter can be eliminated. Furthermore, use of a CT polyphase filter eliminates the problem of an I and Q channel mismatch, while reducing the sensitivity of the circuit to excess loop delays. They reported the following data: power supply $V_{CC} = 2.7V$, power dissipation $DC_{pwr} = 21.8mW$, area

$2.1mm \times 2.9mm$, $f_0 = 1\,MHz$, $BW = 1\,MHz$, $SNDR = 56.2\,dB$, and $f_{clk} = 25/100\,MHz$.

The third generation of the original design proposed by the Raghavan group was published in 2004 by Cosand *et al.* [8]. A summary of the 4^{th} order CT is as follows: InGaAs technology, power supply $V_{CC} = \pm 5V$, power dissipation $DC_{pwr} = 3.5W$, area $3.3mm \times 2.6mm$, tunable center frequency range $f_0 = 140/210\,MHz$, $BW = 1\,MHz$, $SNDR = 78\,dB$, and $f_{clk} = 4\,GHz$.

This dissertation introduces the concept of CT BP $\Sigma\Delta$ modulators with *fractional delays* [50]. This novel 4^{th} order CT BP concept was confirmed by experimental data as follows: SiGe technology, power supply $V_{CC} = 3.3V$, power dissipation $DC_{pwr} = 1.0/1.2W$, total chip area is $2.3mm \times 2.3mm$, tunable center frequency range $f_0 = 185/289\,MHz$, $BW = 20\,MHz$, maximal $SNR = 50\,dB$, and $f_{clk} = 0.6/1.2\,GHz$.

1.2.1 Current design trends

Although there are numerous publications available concerning CT BP $\Sigma\Delta$ modulators, on average, only one successful design per year has been reported over the last fifteen years; illustrating that casual attempts at modulator designs are very likely to fail. This leaves room for further improvement on both theoretical and practical sides of the problem.

From the overview presented in the previous section, it would appear that the major development directions relate to increasing both the center frequency and SNR. However, there are many other desirable circuit features that could be emphasized, such as wider bandwidth, higher filter order, lower power requirements and tunability of the center frequency. Researchers have used all means available to achieve these goals; advances in theoretical work, fast technologies, and higher OSRs are the most commonly exploited methods. Typical limiting constraints are power consumption and stability. Higher order topologies may deliver higher SNR values, however, they are inherently unstable. Conversely, designing modulators that are tunable to any frequency relative to the sampling clock, i.e. f_s/n type as opposed to the $f_s/4$ type, creates the potential for better utilization of the modulator functionality (frequency translation) and a reduction in power consumption through the use of lower clock frequencies. While the numerical methods generally used to design the loop filter function do produce valid results, analytical methods may contribute more to the fundamental understanding of the problem.

Due to the simplistic methods used to define the design space, the CT BP $\Sigma\Delta$ center frequency and maximal SNR, fair comparisons of various designs proved to be difficult.

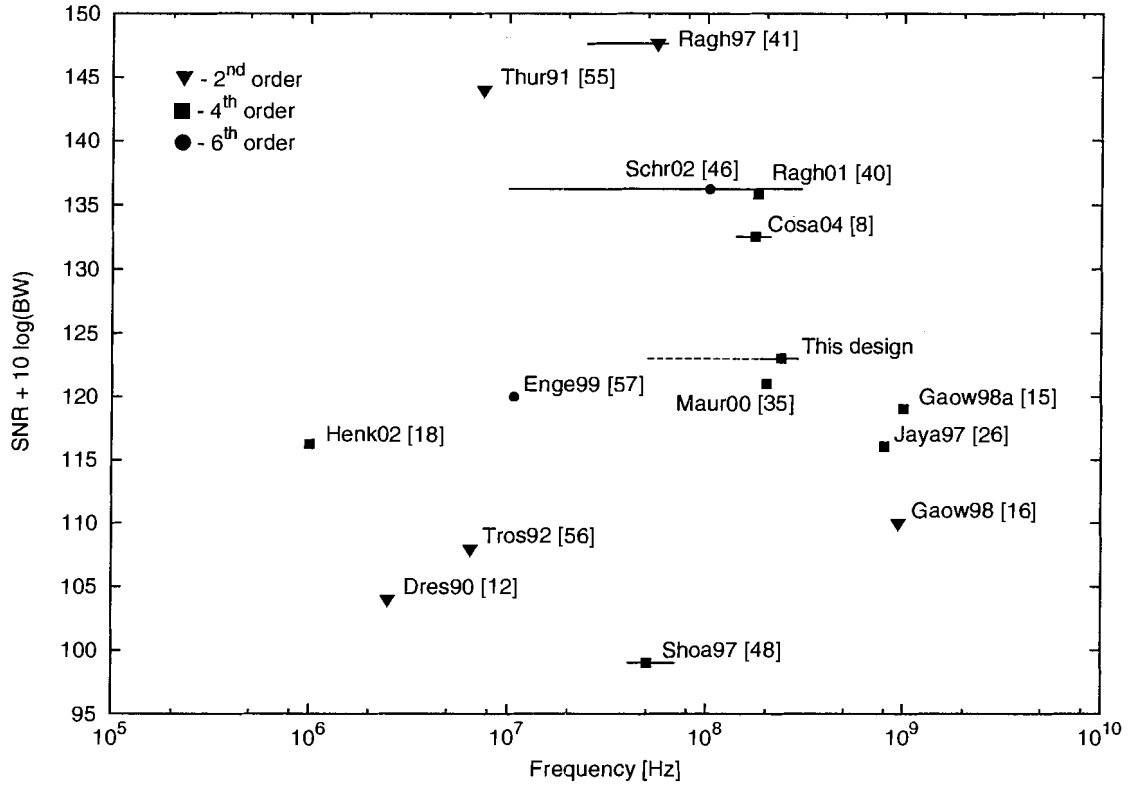


Figure 1.1: A comparison of CT BP $\Sigma\Delta$ modulator designs.

The designs exhibit various levels of performance depending on their specific combination of modulator order, number of slicing levels in the A/D and D/A blocks, bandwidth and oversampling ratio. A qualitative figure of merit for the performance of the modulators listed in this section are shown in Fig. 1.1; the horizontal axis is the signal frequency, the vertical axis is the maximal *SNR* normalized over $BW = 1Hz$, and the tunability range is given by the horizontal line.

1.3 Motivation and contributions

The desire to create an efficient and versatile global wireless network is the dominant force behind both industrial and academic efforts to study the bandpass version of the modulator. The main focus of this work is analytical and behavioral modeling of a tunable 4^{th} order CT BP $\Sigma\Delta$ modulator. There are two problems specifically related to CT type modulators

which motivated this work.

Firstly, the tunability aspect of $\Sigma\Delta$ modulators is very promising in the context of a software–defined radio. The primary focus was to develop the analytical modeling methodology which would enable fine tuning of the center frequency. Secondly, the loop delay problem in CT systems still requires further exploration. Models prior to this work always assumed that the system had an integer number of clock delays, with the loop delay being dealt with separately from the loop filter design. In this dissertation, a novel way of dealing with the loop delay is proposed, where the loop delay is incorporated into the loop filter design. The final outcome is a new sub–class of fractional delay modulators.

The contributions of this dissertation are as follows:

1. The overall design methodology for the CT BP $\Sigma\Delta$ modulators includes the following steps and elements:

   1.1 The CT models were generalized to include tunability; i.e, instead of only using $f_s/4$ models, f_s/n is introduced, where n is a rational positive number. In order to perform the generalization by means of an impulse invariant transformation, a new class of mapping functions was introduced.

   1.2 The loop delay problem was addressed by introducing a new class of CT BP $\Sigma\Delta$ modulators with a fractional delay. Using the general zero–delay analytical models as a starting point, the time–domain shift was introduced by means of Laplace and inverse Laplace transforms.

   1.3 The proposed models were verified in the traditional IC design environment, using a behavioral simulation modeling technique. Behavioral models of the lower level $\Sigma\Delta$ blocks were developed first, followed by the creation and simulation of the top level topology. As a result, throughout the whole design process, only one software tool is required for the top level $\Sigma\Delta$ simulation. Thus, the problems relating to design data exchange between the various software tools used during the design process were eliminated. Furthermore, the transistor level sub–blocks were verified within the behavioral model.

2. The introduction of the fractional delay class of modulators created the following possibilities:

   2.1 The integer delay requirement, a limiting factor in the modulators design, was

removed; this implies that the traditional feedback DAC could be replaced with an adaptive analog delay line. As a result, the loop delay time was accounted for during the loop filter design phase.

2.2 A novel loop architecture was proposed where the DAC was replaced with a programmable analog delay line.

3. The design and implementation of a fully monolithic 4^{th} order CT BP $\Sigma\Delta$ modulator in $0.5\mu m$ BiCMOS SiGe technology.

3.1 A g_m–C prototype chip was designed and implemented, using the architecture, design methodology and analytical models developed in this dissertation. Experimental results were shown to confirm the proposal and explain the discrepancies. Suggestions for future designs are presented.

4. Possible applications of this newly proposed topology were explored.

4.1 By exploiting the frequency tunability and replacing the traditional BP modulators, the developed technique may be applied to cases where the overall system operates with multiple frequencies, such as cell phones intended for worldwide usage.

4.2 Frequency upconversion is one of the required functions in a signal transmitting path. Inherently, a $\Sigma\Delta$ modulator is a frequency multiplier circuit. This multiplication property, combined with the fractional delay approach, enabled the introduction of a fractional delay $\Sigma\Delta$ upconverter.

4.3 The inclusion of a power amplifier within the $\Sigma\Delta$ loop created the potential for transmitter power efficiency improvement. A novel architecture was proposed and discussed.

1.4 The dissertation organization

The remainder of this thesis is organized as follows. Chapter 2 introduces the basic concepts of $\Sigma\Delta$ modulations, including the quantization of a CT signal and its corresponding terminology. A linear model which was extended through the describing function model described in [2] is then shown.

In Chapter 3, theoretical details of CT BP $\Sigma\Delta$ modulators with fractional delays are presented. A new family of mapping functions, which enabled the theoretical development, are described. Systematic methodologies for obtaining models of 2^{nd}, 4^{th} and 6^{th} order modulators, along with their respective limitations, are described. Next, the creation of fractionally delayed modulator models via Laplace and inverse Laplace transforms is introduced.

The concept of the behavioral modeling technique is described in Chapter 4. This technique enabled the development of practical ICs using a standard set of IC design software tools. In Chapter 5, implementation details of the SiGe prototype chip are presented; the basic blocks are analyzed in the context of the proposed g_m–C architecture. The experimental setup and results are presented in Chapter 6. In Chapter 7, two new circuit architectures are proposed: a fractional delay upconverter and power amplifier within the $\Sigma\Delta$ loop. Possible applications are then discussed. Lastly, Chapter 8 provides a general discussion of presented results, along with plans for future work.

Chapter 2

Basic principles of $\Sigma\Delta$ modulation

This chapter introduces the basic principles behind $\Sigma\Delta$ modulation, along with the adopted terminology used in this dissertation. Although the basic principles are intuitively simple, a detailed analysis of the $\Sigma\Delta$ modulator is still under development; a complete closed–form analytical model covering all aspects of $\Sigma\Delta$ modulation does not currently exist. As a result, researchers are forced to develop their own semi–empirical solutions. This chapter gives a brief introduction of $\Sigma\Delta$ modulation; a more detailed introduction can be found in [27].

First, general reviews of signal quantization and quantization noise are presented, followed by basic assumptions and shortcomings. Secondly, an advanced linear $\Sigma\Delta$ loop model, based on the describing function method [2], is presented in detail. This provides an illustration of an analytical model, which correctly predicts the existence of the maximal signal–to–noise–ratio (SNR) value for the 2^{nd} and 3^{rd} order loops.

Readers who are intimately familiar with the fundamental concepts and terminology may safely proceed to Chapter 3.

2.1 Quantization of a continuous signal

In this section, a set of basic definitions are introduced, the quantization noise power is calculated for both sawtooth and sinusoidal signals, and the SNR formula for an ideal A/D converter is derived.

Inherently, digital logic circuits process only two levels of an input signal, while analog logic circuits operate with continuous signals. Therefore, a quantizer is required to provide an interface between these two signal domains; i.e., it converts the continuous signal into an

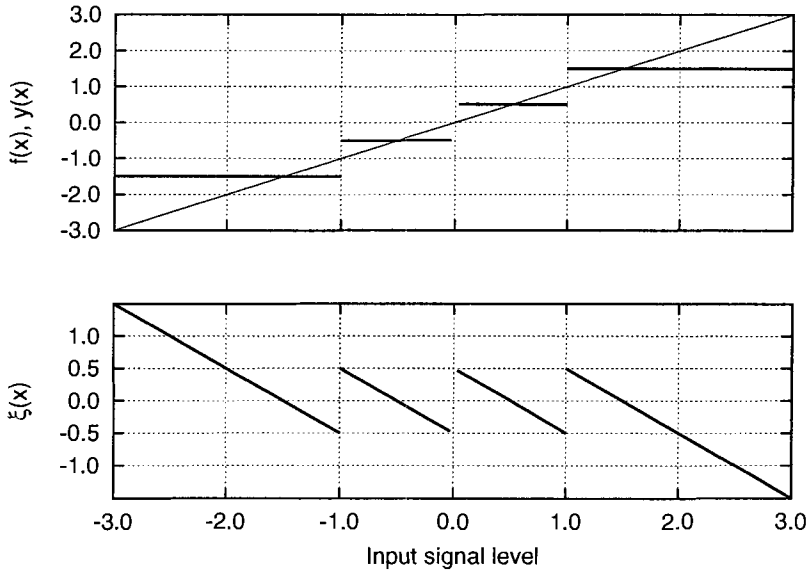


Figure 2.1: Ideal four level quantizer: (top) input signal $f(x)$, output signal $y(x)$; (bottom) quantization error.

n–level discrete step function. The output function for the linear signal $f(x) = G\,x$, where G is the signal gain, at the output of the quantizer resembles

$$y(x) = \begin{cases} -1.5, & \text{if } (x \leq -1.0); \\ -0.5, & \text{if } (-1.0 \leq x < 0.0); \\ +0.5, & \text{if } (0.0 \leq x < +1.0); \\ +1.5, & \text{if } (x \geq +1.0); \end{cases} \tag{2.1}$$

where $y(x)$ is a four–level discrete output function and x is the input signal. A quantizer is said to be *uniform* if the step size, Δ, between any two of the output levels is constant. For now, the assumption is made that the quantizer input and output have the same Δ value.

Function (2.1) represents an ideal four–level quantizer, as shown in Fig. 2.1. Without loss of generality, we will assume $G = 1$ in the following paragraphs.

A quantizer is said to be *mid–rise* if the output state changes at the midpoint of its input range; otherwise, it is said to be a *mid–tread* quantizer [39]. Fig. 2.1 depicts a mid–rise quantizer. In addition, a mid–rise quantizer has an even number of output levels, while the mid–tread quantizer has an odd number of output levels.

The quantization error $\xi(x)$ is defined as

$$\xi(x) = y(x) - f(x) \tag{2.2}$$

where $y(x)$ and $f(x)$ are the output and input signals of the quantizer, respectively.

The quantizer input range R_I corresponds to the range of the input signal for which $\xi(x) \leq \frac{\pm\Delta}{2}$. Outside of R_I, $\xi(x)$ is unbounded; this situation is referred to as overloading. Periodic signals can also cause overloading if their amplitude is larger than R_I. The input range corresponding to the signal in Fig. 2.1 is $R_I = \pm 2$.

The output range R_O of a quantizer is defined by the same boundary conditions as $\xi(x)$. In a uniform n–bit quantizer, R_I is partitioned into equal width segments, each mapping onto a single output code. The output range corresponding to the signal in Fig. 2.1 is $R_O = \pm 2$.

Setting $G = 1$ results in $R_I = R_O$; based on this assumption, Δ can be calculated as either *output referred*

$$\Delta = \frac{R_O}{2^n - 1} \tag{2.3}$$

or, as *input referred*

$$\Delta = \frac{R_I}{2^N} \tag{2.4}$$

where n is the internal quantizer resolution and N is the effective number of bits.

When the maximal input signal amplitude is mapped onto $2N$ output levels, where N is any integer greater than zero ($N = 1, 2, \ldots$) the system is referred to as an *N–bit quantizer*. Figure 2.1 depicts a 2–bit quantizer, with 2^2 output levels. Using (2.3) and (2.4), we can easily relate n to N.

The term Δ, as defined previously, is also commonly referred to as the least significant bit (LSB). In the special case where $N = 1$, the gain G is arbitrarily set. In general, unity gain approximation is used, which loosely states that the 1–bit quantizer has $G = 1$. Therefore, it is inherently linear as $f(x)$ passes through only two points, selected arbitrarily; this is the main reason for its widespread use.

2.1.1 Quantization noise

It can be concluded from the previous section, that quantization errors occur even in ideal quantizers and subsequently, in all A/D converters. Since the quantization error signal is

fundamental to the ΣΔ modulator's operation, its rms and average values are derived in this section.

The error signal's rms and average values were determined by applying a stochastic approach, used for general input signals [27]. Two assumptions are made: 1) the quantization error signal is random, with its amplitude always bounded by $\pm\Delta/2$; i.e., only the non–overloaded quantizer is considered; and 2) the input signal is sampled at a sufficiently high sampling frequency, $f_s = 1/T$. Furthermore, a linear ramp input signal is applied, as shown in Fig. 2.1.

By definition, the average value of $\xi(x)$ is calculated using a probability density function $pdf(\xi)$. Following the first of the two assumptions, $pdf(\xi) = 0$ for $\xi > |\pm\Delta/2|$.

Therefore, the probability density function is

$$\int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} pdf(\xi)\, d\xi = 1 \Rightarrow \xi_{awg} = 0 \tag{2.5}$$

Similarly, for the root mean square value ξ_{rms} we find

$$\xi_{rms}{}^2 = \int_{-\infty}^{+\infty} \xi^2\, pdf(\xi)\, d\xi = \frac{1}{\Delta} \int_{-\frac{\Delta}{2}}^{+\frac{\Delta}{2}} \xi^2\, d\xi = \frac{\Delta^2}{12} \tag{2.6}$$

From (2.6) we see that that ξ_{rms} is *not* a function of f_s. When a quantized signal is sampled at $f_s = \frac{1}{T}$, where T is sampling period, all of its power is contained within the frequency band $f \leq \frac{f_s}{2}$; a two–sided definition of power. Furthermore, the quantization error signal's spectral density $S_q(f)$ is constant within the frequency range defined by f_s and is calculated using either

$$\xi_{rms}{}^2 = \int_{-\frac{f_s}{2}}^{+\frac{f_s}{2}} |S_q(f)|^2\, df = |S_q(f)|^2 \int_{-\frac{f_s}{2}}^{+\frac{f_s}{2}} df = |S_q(f)|^2 f_s \tag{2.7}$$

or,

$$|S_q(f)|^2 = \frac{\Delta^2}{12}\frac{1}{f_s} = \xi_{rms}{}^2 \tag{2.8}$$

After quantization, the signal is passed through a brick wall profile LP filter with a cut–off frequency of f_0, $H(f) = 1$ for $f \leq \pm f_0$. The signal power remains unchanged as its

content is below f_0. However, the quantization error power $P_n(f)$ is reduced to

$$P_n(f) = \int_{-\frac{f_s}{2}}^{+\frac{f_s}{2}} S_q(f)^2 H(f)^2 \, df = \int_{-f_0}^{+f_0} S_q(f)^2 \, df$$
$$= \frac{\Delta^2}{12}\frac{1}{f_s}2f_0 = \frac{\Delta^2}{12}\frac{1}{OSR} = \frac{{\xi_{rms}}^2}{Z_0} \tag{2.9}$$

where OSR is defined as the ratio of f_s to the Nyquist frequency $2f_0$.

$$OSR \equiv \frac{f_s}{2f_0} \tag{2.10}$$

It is assumed that the load impedance is $Z_0 = 1$, which conveniently allows the rms value to be calculated as $\sqrt{power}$. In addition, by doubling the OSR in (2.9), the quantization noise power decreases by $3\,dB$. Thus, an increase in f_s alone is not an efficient way to improve the SNR.

2.1.2 Sinusoidal and sawtooth input signals

The SNR will now be calculated for two well known input signals: sawtooth and sinusoidal. For a sawtooth signal with period T and an amplitude equal to the maximal input range $A_m = R_I$, the rms power is given by

$$w_{rms} = \frac{A_m}{\sqrt{12}} \tag{2.11}$$

Assuming an input referred Δ, where $A_m = R_I = \Delta 2^N$, and equations (2.11) and (2.4), we find

$$SNR_{max} \equiv 10\log\left(\frac{P_s}{P_n}\right) = 20\log\left(\frac{\frac{\Delta 2^N}{\sqrt{12}}}{\frac{\Delta}{\sqrt{12}}}\right)$$
$$= 20\log 2^N = (6.02N)\,dB \tag{2.12}$$

Similarly, for a sinusoidal signal with period $T = 2\pi$ and peak–to–peak amplitude equal to the maximal R_I, i.e. $A_m = \frac{V_{ref}}{2}$, we write

$$s_{rms} = \frac{A_m}{\sqrt{2}} \tag{2.13}$$

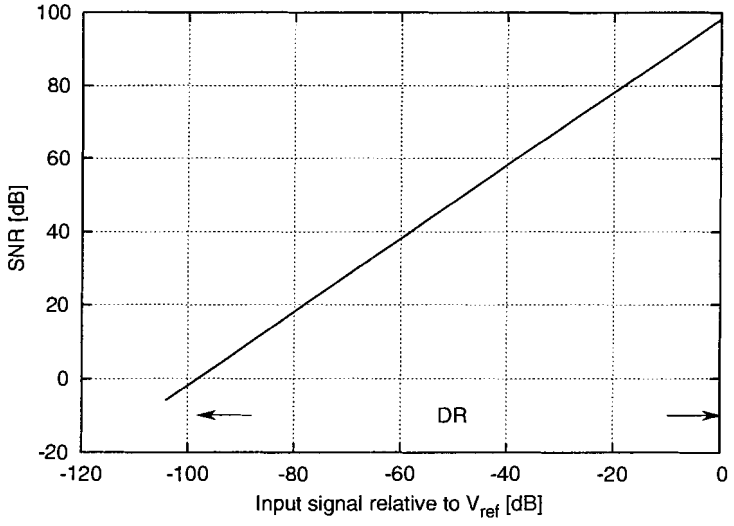


Figure 2.2: Ideal SNR versus input signal level (N=16).

Thus, calculation of the *SNR* for the sinusoidal input signal yields

$$SNR_{max} \equiv 10\log\left(\frac{P_s}{P_n}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}}\right)$$
$$= 20\log\left(\sqrt{\frac{3}{2}}2^N\right) = (6.02N + 1.76)\,dB \qquad (2.14)$$

From (2.14) and (2.12), we conclude that a sinusoidal signal has $1.76\,dB$ more power than the corresponding sawtooth signal. Equation (2.14) is a well known result, generally used to estimate N relative to SNR_{max}, for an A/D converter.

2.1.3 SNR of an ideal A/D converter

Formulas for the ideal cases, derived in (2.12) and (2.14), are used as first estimates of the *SNR* and dynamic range (DR) for an ideal A/D converter. When $G = 1$, the DR is equivalent to SNR_{max}. Figure 2.2 depicts the relationship between the *SNR*, input signal magnitude and DR, for a sinusoidal signal with a maximal amplitude of V_{ref} and a quantizer with $N = 16$. From equation (2.14), it is readily found that for $N = 16$, the SNR_{max} is approximately $98\,dB$.

The quantization noise inside the non–saturated region was shown to be bounded by $\pm\Delta/2$. For a 1–bit quantizer, the maximal peak–to–peak amplitude of a sinusoidal signal is Δ; i.e, based on (2.14), $SNR_{max} \approx 7.78dB$, implying that an additional technique is required to improve the *SNR*.

At least two obvious methods exist to increase the *SNR*, each of which have their practical limitations. In the first method, N is increased in order to increase the input signal range relative to $\pm\Delta/2$, thereby reducing the quantization noise. An increase in N reduces the *SNR* by approximately $6\,dB$ per each added bit. However, implementation problems become quite challenging; design of a multi–bit quantizer is a non–trivial task, as linearity problems become dominant at an early stage. In the second method, the *OSR* is increased and the noise power within f_0 is reduced by approximately $3\,dB$/octave, in accordance with (2.9). Using a simple 1–bit quantizer is very straightforward to implement, however, the gain resulting from an *OSR* increase is modest.

Clearly, these two choices do not achieve a practical 16–bit resolution; therefore, additional techniques are required to achieve that goal. One possible solution is using a noise shaping technique, which is the main product of ΣΔ modulation.

2.2 Linear Model of a ΣΔ Modulator

Figure 2.3 depicts a block diagram for a linear ΣΔ loop. The quantizer has been replaced by a summing node, where $e[n]$ is Gaussian error signal. The following assumptions are made regarding the quantization error signal:

- the error signal is a stationary random process
- the error signal and input signals are not correlated
- the error signal has a white noise profile
- the error signal has a uniform probability distribution

These assumptions are referred to as the soft version of the white noise approximation [37, 36]. This approach will be used to describe the noise shaping operational principles. Furthermore, the white noise model allows for a precise calculation of the quantization error's root mean square, for a large variety of inputs and non–loading systems. The main

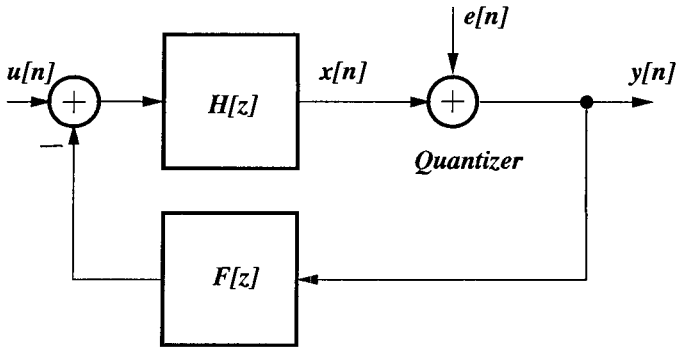


Figure 2.3: Block diagram of a linear model for a ΣΔ modulator loop.

drawback of this approach is the inability to predict idle tones and noise patterns; it also does not account for excess noise due to overload [36].

Two independent transfer functions are available to describe the feedback loop in Fig. 2.3. The first is a signal transfer function (STF), which connects the input signal $u[n]$ and output signal $y[n]$ according to

$$STF[z] = \frac{Y[z]}{U[z]} = \frac{H[z]}{1 + H[z]F[z]} \tag{2.15}$$

The second is a noise transfer function (NTF), which follows the loop according to the assumption that $e[n]$ is the input node and $y[n]$ is the output node and is defined by

$$NTF[z] = \frac{Y[z]}{E[z]} = \frac{1}{1 + H[z]F[z]} \tag{2.16}$$

Due to the existence of a sampled quantizer inside the loop, it is convenient to describe the loop functions in the z–domain. In order to demonstrate the noise shaping principle, both the $H[z]$ and $F[z]$ functions need to be specified. Without loss of generality, we select $F[n] = 1$ and $H[n]$ to be an integrator of order m. For this configuration, the STF degenerates into a delay function and the NTF drops to zero at DC. Consequently, the STF remains constant regardless of frequency, while the noise is shaped away from the low frequency region. For example, substituting $H[z] = z^{-1}/(1 - z^{-1})$ into equations (2.15) and (2.16), results in

$$STF[z] = z^{-1} \tag{2.17}$$

$$NTF[z] = (1 - z^{-1})^m \tag{2.18}$$

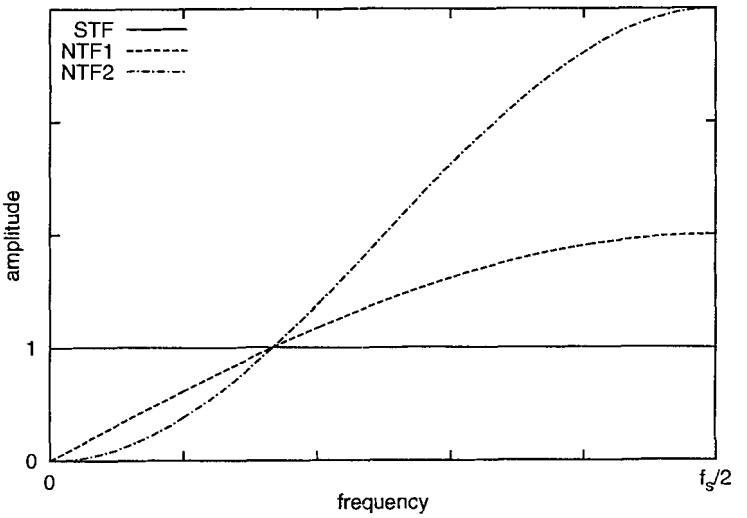


Figure 2.4: Graph of $STF(z) = z^{-1}$ and $NTF(z) = (1 - z^{-1})^m$, $m = 1, 2$ functions.

A plot of these two functions for $m = 1, 2$ is given in Fig. 2.4, with the frequency ranging from DC to $f_s/2$. Clearly, the noise is shaped away from DC, with the higher order function having a lower noise floor inside the DC region.

2.2.1 SNR of m^{th}–order ΣΔ modulator

In this section, a more general form of equation (2.14) is derived for the *SNR*. It is important to consider the initial estimate of the *SNR* relative to the *OSR*, the *NTF* order m, and number of bits n, when determining the ΣΔ architecture capable of achieving the required system specifications.

After applying complex algebra transformations to (2.18), the amplitude of the m^{th} order *NTF* is calculated according to

$$NTF(z) = (1 - z^{-1})^m \Rightarrow |NTF(f)| = \left[2\sin(\pi\frac{f}{f_s})\right]^m \tag{2.19}$$

Using the results from (2.9) and (2.19), a more general expression for the quantization error

power is

$$P_n(f) = \int_{-\frac{f_s}{2}}^{+\frac{f_s}{2}} S_q(f)^2 NTF(f)^2 = \left[\frac{\Delta}{\sqrt{12}} \frac{\pi^m}{\sqrt{2m+1}} OSR^{-(m+\frac{1}{2})}\right]^2 \tag{2.20}$$

where the assumption $f \ll f_s$ (or equivalently $OSR \gg 1$) allowed for the approximation $sin(x) \approx x$. A system with the following configuration is selected: an output referred sinusoidal signal, with maximal amplitude $A_m = R_O/2$, a unity quantizer gain, i.e. $R_I = R_O$, an m–order loop filter and an n–bit internal resolution quantizer. Then, from equations (2.3), (2.14) and (2.20), it follows that

$$SNR_{max} \equiv 10 \log\left(\frac{P_s}{P_n}\right) = 20 \log\left[(2^n - 1)\sqrt{\frac{3}{2}} \frac{\sqrt{2m+1}}{\pi^m} OSR^{(m+\frac{1}{2})}\right] \tag{2.21}$$

The SNR, as calculated using (2.21), for various loop orders ($m = 0, 1, \ldots 8$) and a 1–bit quantizer ($N = 1$) is shown in Fig. 2.5. This graph illustrates the trade–offs between complexity (ΣΔ loop order) and clock speed (OSR), for a given SNR_{max}. There are many different configurations that will achieve an $SNR_{max} \approx 110dB$, such as a 2^{nd} order loop with $OSR = 256$, a 3^{rd} order loop with $OSR = 64$, or a 4^th order with $OSR = 32$. In addition, by doubling the OSR, different gains in SNR can be achieved; for example, $3\,dB$ for a zero order shaping loop, $9\,dB$ for a 1^{st} order shaping loop and $15\,dB$ for 2^{nd} order shaping loop. For a detailed mathematical analysis of the quantization error, refer to [37, 27, 36].

2.3 Describing function method

The model described in the previous sections is useful for a first estimate of the SNR. However, the model's main shortcoming is its incorrect prediction of the input signal's maximal amplitude and hence, the maximal SNR. In addition, the model does not provide any information regarding ΣΔ modulator stability. These inaccuracies are due to the nonlinearity of the quantizer, making it difficult to describe and solve for analytically [29]. Therefore, previously published designs used simulations to estimate both the maximum SNR and stability region.

The first model which predicts the existence of the maximal amplitude for the input signal was published by Ardalan and Paulos [2]. While the Ardalan model results are conservative compared to the simulation results, they are still similar to actual systems [50].

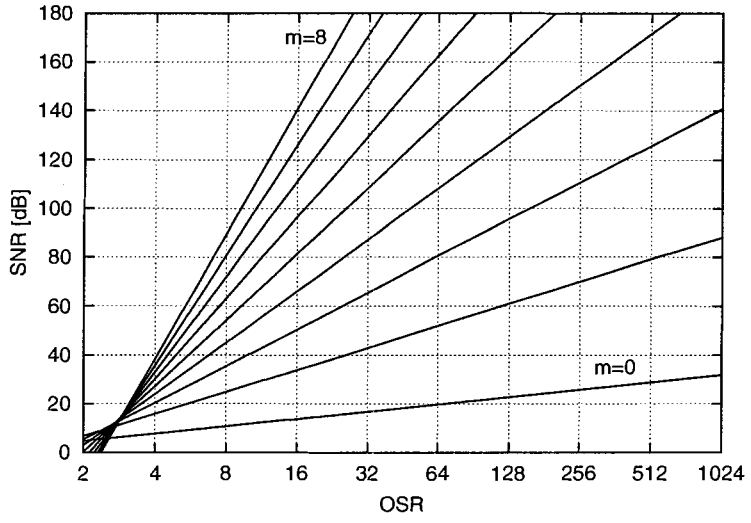


Figure 2.5: SNR of m^{th}–order ΣΔ modulator, $m = 1, 2, \ldots, 8$.

Although subsequent research has produced more sophisticated models [42, 13], the Ardalan model will be used to introduce the problem of maximal *SNR*.

2.3.1 Generalized ΣΔ loop mapping

By selecting appropriate $H_i[z]$ and $H[z]$ functions, it can be shown that any CT signal or multi–loop block can be mapped into the general z–domain architecture (Fig. 2.6). Without loss of generality, the Ardalan model is essentially a remapping of the general model (Fig. 2.6) into a distributed feedback ΣΔ topology (Fig. 2.7). This is accomplished by equating the loop equations for both architectures, thereby producing the following equations

$$H_i = \frac{\alpha_1 \alpha_2 \ldots \alpha_{n-1} H_1 H_1 \ldots H_{1(n-1)}}{1 + \alpha_{n-1} H_1 (1 + \cdots + \alpha_2 H_1 (1 + \alpha_1 H_1))} \tag{2.22}$$

$$H = \alpha_n H_2 (1 + \alpha_{n-1} H_1 (1 + \cdots + \alpha_2 H_1 (1 + \alpha_1 H_1))) \tag{2.23}$$

where $\alpha_1 \ldots \alpha_n$ are gain stage parameters. For example, for a 2^{nd} order ΣΔ loop ($n = 2$) equations (2.22) and (2.23) become

$$H_i[z] = \frac{\alpha_1 H_1[z]}{1 + \alpha_1 H_1[z]} \tag{2.24}$$

$$H[z] = (1 + \alpha_1 H_1[z])\, \alpha_2 H_2[z] \tag{2.25}$$

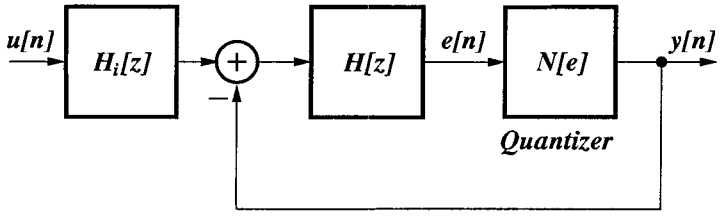


Figure 2.6: Block diagram of a general ΣΔ modulator loop.

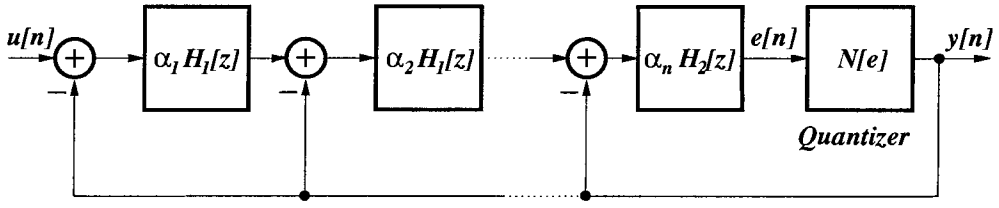


Figure 2.7: Block diagram of a distributed feedback ΣΔ modulator architecture.

where both $H[z]$ functions are integrator blocks described by

$$H_1(z) = \frac{z}{z-1} \qquad H_2(z) = \frac{1}{z-1} \tag{2.26}$$

Note that for loop orders of $n \geq 3$, selecting the appropriate α_i parameters becomes very difficult, as they also control the ΣΔ loop stability. In the following sections, the examples used $\alpha_i = [1\ 1]$ for the 2^{nd} order loop and $\alpha_i = [0.1\ 0.1\ 1]$ for the 3^{rd} order loop.

2.3.2 Nonlinear quantizer

It is common practice in control theory to neglect the feedback error signal $y(t)$, as it is small in comparison to the input signal $x(t)$. For a ΣΔ modulator loop, however, the amplitude of $y(t)$ is almost the same as $x(t)$; this is particularly true in the case of a 1–bit quantizer.

In order to model the nonlinear quantizer $N(x + y)$, a two–path linearized model is introduced, consisting of two gain stages K_x and K_y (Fig. 2.8). The input signal $x(t)$ is processed in path K_x, while the path K_y processes the feedback error component (i.e., the noise). In a traditional quantizer model, there is no distinction between the two paths.

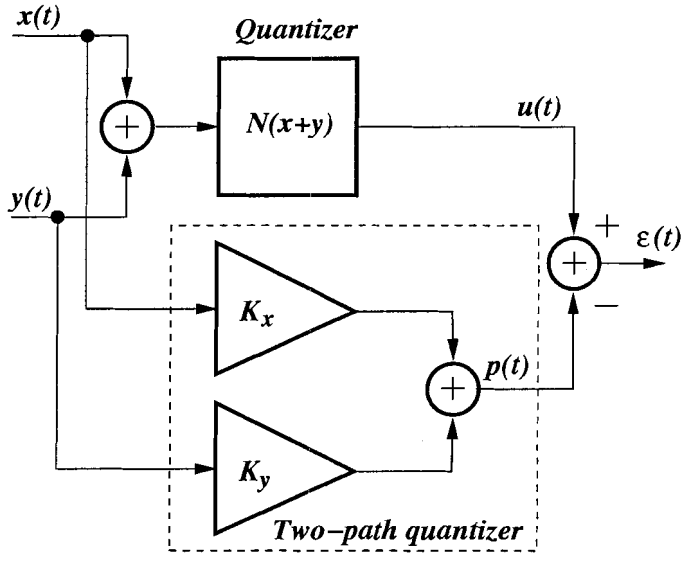


Figure 2.8: Block diagram of a linearized two–path model quantizer.

The output of the two–path model $p(t)$ is compared to the output of the real quantizer $u(t)$, in order to determine the values for K_x and K_y. The difference between $u(t)$ and $p(t)$ is defined as the difference signal $\varepsilon(t)$; the goal is to minimize the mean square value of $\varepsilon(t)$.

By definition, the *SNR* is [2]

$$SNR = \frac{\sigma_x^2}{\sigma_{nb}^2} \tag{2.27}$$

where σ_x^2 is the input signal variance (power) and σ_{nb}^2 is the noise variance (i.e. noise power within the signal bandwidth). The input signal variance is dependent upon the input signal statistics. Two commonly used input signals in ΣΔ loop analysis are DC and sinusoidal signals. The DC case is trivial since $\sigma_x^2 = m_x^2$, where m_x^2 is the DC value of the input signal. For a sinusoidal signal, $\sigma_x^2 = a_x^2/2$, where a_x is the sinusoidal amplitude as given in (2.13).

Substituting the two–path model into the general ΣΔ modulator loop (Fig. 2.6) and remapping (K_x, K_y) into (K_x, K_n), leads to the following two systems of equations:

DC input signal:

$$\sigma_n^2 = \Delta^2 \left[1 - \frac{m_x^2}{\Delta^2} - \frac{2}{\pi} \exp\left(-2 \left[\text{erf}^{-1}\left(\frac{m_x}{\Delta} \right) \right]^2 \right) \right] \tag{2.28}$$

$$\sigma_e^2 = \frac{\sigma_n^2}{2\pi} \int_{-\pi}^{\pi} \frac{\left| H(e^{j\omega}) \right|^2}{\left| 1 + K_n H(e^{j\omega}) \right|^2} d\omega \tag{2.29}$$

$$K_n = \frac{2\Delta}{\sigma_e \sqrt{2\pi}} \exp\left(-\rho^2 \right) \tag{2.30}$$

$$K_x = \frac{\Delta}{m_e} \text{erf}(\rho) \tag{2.31}$$

$$p(k) = e(k) K_n + n(k) + m_e K_x \;\rightarrow$$

$$\Delta^2 = \sigma_e^2 K_n^2 + \sigma_n^2 + (m_e K_x)^2 \tag{2.32}$$

Thus we have five equations and four unknown variables in this system: the error signal variance σ_e^2, the noise variance σ_n^2, K_n and K_x. In addition, two dummy variables, ρ and m_e, are defined as $\rho = \text{erf}^{-1}(m_x/\Delta)$ and $m_e = \rho\sqrt{2\,\sigma_e^2}$. One of the equations may be used as a check function in order to estimate the convergence of the algorithm used to solve the nonlinear coupled equations.

SIN input signal:

$$\rho^2 M^2\left(\frac{1}{2}, 2, -\rho^2 \right) = \frac{\pi}{4} \frac{a_x^2}{\Delta^2} \tag{2.33}$$

$$\sigma_n^2 = \Delta^2 \left[1 - \frac{a_x^2}{2\Delta^2} - \frac{2}{\pi} M^2\left(\frac{1}{2}, 1, -\rho^2 \right) \right] \tag{2.34}$$

$$K_n = \sqrt{\frac{2}{\pi}} \frac{\Delta}{\sigma_n} M\left(\frac{1}{2}, 1, -\rho^2 \right) \tag{2.35}$$

$$\sigma_{en}^2 = \frac{\sigma_n^2}{2\pi} \int_{-\pi}^{\pi} \frac{\left| H(e^{j\omega}) \right|^2}{\left| 1 + K_n H(e^{j\omega}) \right|^2} d\omega \tag{2.36}$$

$$\Delta^2 = \sigma_n^2 + (K_x\, \sigma_{ex})^2 + (K_n\, \sigma_{en})^2 \tag{2.37}$$

Again, the system has five equations and four unknown variables. The function $M(\alpha, \gamma, x)$ is the confluent hyper–geometric function [1], defined as

$$\frac{\Gamma(\gamma - \alpha)}{\Gamma(\gamma)} M(\alpha, \gamma, x) = \int_0^1 e^{xt}\, t^{\alpha - 1}\, (1 - t)^{\gamma - \alpha - 1}\, dt \tag{2.38}$$

where $\Gamma(x)$ is the well known *gamma function.*

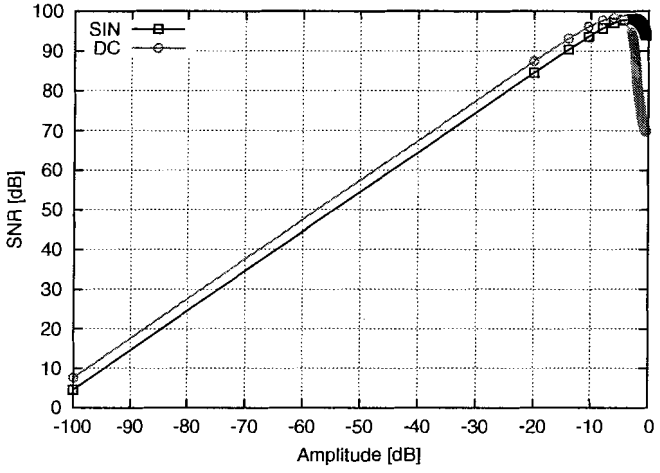


Figure 2.9: Calculated SNR for DC and SIN signals ($f_s/f_b = 256$).

Numerical solutions of (2.28) through (2.37) yield *SNR* values for the two cases of input signals (Fig. 2.9). In comparison to Fig. 2.2, we see that the Ardalan model correctly predicted the existence of a maximal input signal, which could be processed before the ΣΔ loop became unstable; this led into a collapse of the *SNR* value. In comparison to Fig. 2.5, we see that the ideal model of the 2^{nd} order loop with $OSR = 256$ predicted an $SNR_{max} \approx 110dB$, while Fig. 2.9 gives an $SNR_{max} \approx 98dB$. The numerical solutions also show that (K_x, K_n) are dependent on the amplitude of the DC input. It is believed that the maximum *SNR* is produced by this phenomena, which also causes instability in higher order ΣΔ modulators.

2.4 Summary

The fundamental principles and definitions required for ΣΔ modulator operation were introduced. The ideal quantization process was described in the context of maximal *SNR* calculations. A linear model of a ΣΔ modulator was presented, along with common assumptions about the quantization error signal. The Ardalan model, the first model that could predict the existence of a maximal input signal that could be processed prior to the modulator becoming unstable, was then discussed. In the following chapter, an s–domain tunable CT BP ΣΔ modulator model with fractional delays is presented.

Chapter 3

Fractional $\Sigma\Delta$ modulators

Chapter 2 introduced the basic principles and terminology required to understand the material presented in the following sections. This chapter focuses on the development of an analytical procedure for obtaining a *closed–form* transfer function for the loop filter of a *tunable* CT BP $\Sigma\Delta$ modulator. Analytical models for tunable versions of 2^{nd} and 4^{th} order CT BP $\Sigma\Delta$ loops, as well as the $f_s/4$ variant of the 6^{th} order system, are presented.

The developed procedure is extended to introduce a new concept of $\Sigma\Delta$ modulators with *fractional delays* [50] ($f\Sigma\Delta$). Equation details for 2^{nd}, 4^{th} and 6^{th} order tunable CT BP $\Sigma\Delta$ modulator designs are shown. A novel $\Sigma\Delta$ loop architecture, which has the traditional CT BP loop filter function replaced by a fractional filter function, is proposed.

3.1 Theoretical background

One challenge in designing a CT BP $\Sigma\Delta$ modulator is the lack of an s–domain analytical expression for the tunable loop filter transfer function. Hence, the first BP $\Sigma\Delta$ designs were achieved simply by following intuition and replacing the LP $\Sigma\Delta$ loop filter with a BP loop filter [55, 20]. As a result, the designs were non–optimal for the given loop order. Shortly after, an analytical form of the second and fourth order $f_s/4$ CT BP loop transfer functions were published by Shoaei in [48]. These functions were derived through the application of the impulse invariant transformation.

The current trend is to create a *tunable*, higher order CT BP $\Sigma\Delta$ modulator for RF frequencies [49] [52]. As analytical results for a tunable CT BP $\Sigma\Delta$ modulator do not exist, virtually all currently published tunable designs were developed with the help of numerical

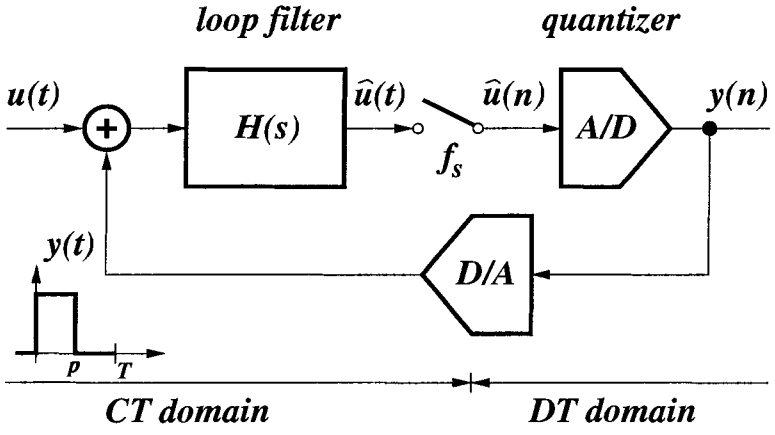


Figure 3.1: Block diagram of a CT ΣΔ modulator.

filter design methods. However, analytical solutions are almost always preferable as they can offer more insight and flexibility in the design process.

Control and compensation of the excess loop delay is another important property that is considered during CT BP ΣΔ design [6] [19]. The analytical procedure outlined in this chapter enables the proposal of a novel ΣΔ loop architecture, where the traditional CT BP loop filter function is replaced by a filter function with fractional delays. The architecture exploits the fact that the *overall* ΣΔ loop timing (including the excess loop delay) must be equal to a *fractional* multiple of the sampling period, which is matched by the CT loop filter transfer function.

A block diagram of a CT ΣΔ modulator loop is shown in Fig. 3.1. The CT domain signals $u(t)$ and $y(t)$ are added before being processed by the CT loop filter $H(s)$. The output signal from the filter $\hat{u}(t)$ is sampled by a switch at a frequency of f_s. The DT signal $\hat{u}(n)$ is then quantized by the A/D block. The feedback loop consists of a D/A converter, which is usually modeled with a zero–order–hold (ZOH) function. The output of the ZOH is the CT pulse function $y(t)$.

Clearly, the overall ΣΔ loop gain is a DT function. Therefore, an exact correspondence between the CT filter $H(s)$ and its equivalent DT filter $H(z)$ can be derived only at the sampling points.

In the following subsections, the mathematical principles used in this chapter are outlined.

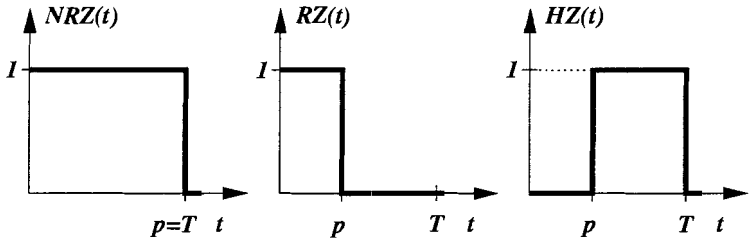


Figure 3.2: DAC pulse forms for NRZ, RZ, and HZ.

3.1.1 DAC pulses

A ZOH block can deliver three forms of pulse shapes: non–return–to–zero (NRZ), return–to–zero (RZ) and hold–return–to–zero (HZ) [32], as shown in Fig. 3.2. For 50% RZ duty-cycle pulses, the pulse width p is $T/2$; in general, $0 \leq p \leq T$. Depending upon the value of p, the RZ pulse degenerates into two cases: for $p = 0$, it results in the theoretical $\delta(t)$ function, while for $p = T$, it becomes the NRZ pulse.

Time domain definitions

The time domain definition of a pulse $R_p(t)$ is based upon the step function $u(t)$ as follows

$$R_p(t)|_{NRZ} = u(t) - u(t-T) \tag{3.1}$$

$$R_p(t)|_{RZ} = u(t) - u(t-p) \tag{3.2}$$

$$R_p(t)|_{HZ} = u(t-p) - u(t-T) \tag{3.3}$$

S–domain pulse forms

The Laplace transform of (3.1) to (3.3) results in

$$\mathcal{L}\,[NRZ(t)] = \frac{1-e^{-sT}}{s} \tag{3.4}$$

$$\mathcal{L}\,[RZ(t)] = \frac{1-e^{-sp}}{s} \tag{3.5}$$

$$\mathcal{L}\,[HZ(t)] = \frac{e^{-sp}-e^{-sT}}{s} \tag{3.6}$$

3.1.2 Discrete time to continuous time transformation

The mathematical equivalence between the $H(z)$ and $H(s)$ functions can exist only at the sampling points. In other words, at the sampling points, the inverse z–transform of $H(z)$

must be equivalent to the inverse Laplace transform of $H(s)$; a mathematical description is as follows

$$\mathcal{Z}^{-1}\left[H(z)\right] = \mathcal{L}^{-1}\left[\frac{1-e^{-sT}}{s}H(s)\right]_{t=kT} \tag{3.7}$$

$$\mathcal{Z}^{-1}\left[H(z)\right] = \mathcal{L}^{-1}\left[\frac{1-e^{-sp}}{s}H(s)\right]_{t=kT} \tag{3.8}$$

$$\mathcal{Z}^{-1}\left[H(z)\right] = \mathcal{L}^{-1}\left[\frac{e^{-sp}-e^{-sT}}{s}H(s)\right]_{t=kT} \tag{3.9}$$

where T is the sampling period, p is the pulse width, k is the sampling index, $H(z)$ is the z–domain representation and $H(s)$ is the equivalent s–domain representation of the loop filter.

A time domain form of (3.7) to (3.9) can be written as

$$\begin{aligned} h(kT) &= \left[R_p(t) * \hat{h}(t)\right]_{t=kT} \\ &= \left[\int_{-\infty}^{+\infty} R_p(\tau)\hat{h}(t-\tau)d\tau\right]_{t=kT} \end{aligned} \tag{3.10}$$

where $R_p(t)$ is the corresponding time domain pulse, $\hat{h}(t)$ is the impulse response of the CT function $H(s)$, $h(kT)$ is the impulse response of the DT function $H(z)$, and $*$ denotes convolution. Relations (3.7) through (3.9) along with (3.10) are known as the pulse invariant transformation.

Single–pole function transformation

In order to solve (3.10), the exact form of both the pulse $R_p(t)$ and the filter impulse response $\hat{h}(t)$ are required. The residual form of a DT transfer function with only a single pole is given by

$$H(z) = \sum_{k=1}^{N} \frac{a_k z^{-1}}{1 - z_k z^{-1}} = \sum_{k=1}^{N} \frac{a_k}{z - z_k} \tag{3.11}$$

where z_k is the single pole, [29]. At the same time, the equivalent s-domain transfer function can be written as:

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{s - s_k} \tag{3.12}$$

with the impulse response in the form of

$$\hat{h}(t) = \sum_{k=1}^{N} \hat{a}_k e^{s_k T} u(t) \tag{3.13}$$

where the hat (ˆ) is used to indicate continuous time parameters [32].

By substituting (3.1) and (3.13) into (3.10), it was shown [48] that the impulse invariant transformation requires that

$$a_k = \frac{\hat{a}_k}{-s_k}\left(1 - e^{s_k T}\right) \text{ and } z_k = e^{s_k T} \tag{3.14}$$

Multiple–pole function transformation

The same procedure applied to the single–pole system can be applied to multiple–pole systems as well. All results presented in this chapter assumed an NRZ pulse shape; however, the same procedure applies to other pulse shapes as well. Furthermore, the following three cases of the $H(s)$ function are considered:

1) $H(s)$ contains only single poles

2) $H(s)$ contains double poles

3) $H(s)$ contains triple poles

and are referred to as the single–pole, double–pole and triple–pole functions, respectively. In Table 3.1, transformation functions for the partial fraction terms with pole orders of up to three are listed. Note that the analytical complexity of the required derivations becomes too complicated for the pole orders greater than three; in these cases, the help of a mathematical tool is required.

3.2 ΣΔ loop filter transfer function

The underlying assumption in most of the z–domain ΣΔ loops expressions, is that the sampling frequency is four times higher than the signal frequency. The equivalent description is that the complex signal frequency is at the $\theta = \pi/2$ angle. Indeed, the ΣΔ loop transfer functions within this category are referred to as the $f_s/4$ functions.

The natural starting point for determining tunable versions of the ΣΔ transfer functions is the $f_s/4$ case, as the z–plane location of the input signal frequency is at the mid–point between the DC frequency ($\theta = 0$) and half the sampling frequency ($\theta = \pi$). This symmetry

$\Psi(z)$	$\Psi(s)$	$\hat{a}_0 \mapsto a_z$ mapping	
$\dfrac{a_z}{z-p_0}$	$\dfrac{\hat{a}_0}{s-s_0}$	$\hat{a}_0 = \dfrac{-s_0\, a_z}{1-e^{s_0 T}}$	[48]
$\dfrac{a_z}{(z-p_0)^2}$	$\dfrac{\hat{a}_0}{(s-s_0)^2}$	$\hat{a}_0 = a_z\left[C_1\, s + C_0\right], C_1 = \dfrac{1-e^{-s_0 T}-s_0 T}{T\left(1-e^{s_0 T}\right)^2}, C_0 = \dfrac{s_0^2}{\left(1-e^{s_0 T}\right)^2}$	[48]
$\dfrac{a_z}{(z-p_0)^3}$	$\dfrac{\hat{a}_0}{(s-s_0)^3}$	$\hat{a}_0 = \left(a_z e^{-2s_0 T}\right)\left[C_2 s^2 + C_1 s + C_0\right], C_2 = \dfrac{1}{2T}\dfrac{2s_0 T - 3 + 4\,e^{-s_0 T} - e^{-2s_0 T}}{e^{3s_0 T} - 3e^{2s_0 T} + 3e^{s_0 T} - 1}$ $C_1 = \dfrac{1}{2T^2}\left[\dfrac{-4T^2}{e^{3s_0 T} - 3e^{2s_0 T} + 3e^{s_0 T} - 1}\, s_0^2 + \dfrac{3T + T\,e^{-2s_0 T} - 4T\,e^{-s_0 T}}{e^{3s_0 T} - 3e^{2s_0 T} + 3e^{s_0 T} - 1}\, s_0 + \right.$ $\left. + \dfrac{2 - 4\,e^{-s_0 T} + 2\,e^{-2s_0 T}}{e^{3s_0 T} - 3e^{2s_0 T} + 3e^{s_0 T} - 1}\right], C_0 = \dfrac{1}{2T^3}\dfrac{2s_0^3 T^3}{e^{3s_0 T} - 3e^{2s_0 T} + 3e^{s_0 T} - 1}$	[52]

Table 3.1: Transformation functions of the partial fraction terms, with pole orders of up to three.

enables the relative change of the input signal frequency to the sampling frequency equally in both directions.

3.2.1 ΣΔ $f_s/4$ loop filter functions

CT BP ΣΔ loop function development starts with the z–domain description of the $f_s/4$ ΣΔ noise transfer function (NTF). One way to create the NTF is to place n resonators on the signal path of the ΣΔ loop [36]

$$NTF(z) = (1 + z^{-2})^n \tag{3.15}$$

$$H_m(z) = \frac{NTF - 1}{NTF} \tag{3.16}$$

where $n = 1, 2, 3, ...$ is the number of resonators which identifies the BP ΣΔ order as $m = 2n$. Substitution of (3.15) into (3.16) for $m = 2, 4, 6$ results in second, fourth and sixth order $f_s/4$ filter transfer functions, respectively, as follows

$$H_2(z) = \frac{1}{z^2 + 1} \tag{3.17}$$

$$H_4(z) = \frac{2z^2 + 1}{(z^2 + 1)^2} \tag{3.18}$$

$$H_6(z) = \frac{3z^4 + 3z^2 + 1}{(z^2 + 1)^3} \tag{3.19}$$

Each of the transfer functions $H_m(z)$ can be written as a sum of its partial fraction terms, where each of the terms has the following general form

$$\Psi(z) = \frac{a_z}{(z - p_0)^x} \tag{3.20}$$

where a_z is either in complex form $a_z = j\,a_{z0}$ or in real form $a_z = a_{z0}$, $(a_{z0} \in \mathcal{R})$, p_0 is a pole, $x = 1, 2, \ldots, n$ and n is the number of resonators. The poles in (3.17) through (3.19) have their real part equal to zero; therefore, $p_0 = \pm j$.

Specifically, (3.17) to (3.19) are rewritten in the following forms

$$H_2(z) = \frac{\frac{1}{2}j}{z + j} + \frac{-\frac{1}{2}j}{z - j} \tag{3.21}$$

$$H_4(z) = \frac{\frac{3}{4}j}{z + j} + \frac{-\frac{3}{4}j}{z - j} + \frac{\frac{1}{4}}{(z + j)^2} + \frac{\frac{1}{4}}{(z - j)^2} \tag{3.22}$$

$$H_6(z) = \frac{\frac{15}{16}j}{z+j} + \frac{-\frac{15}{16}j}{z-j} + \frac{\frac{9}{16}}{(z+j)^2} + \frac{\frac{9}{16}}{(z-j)^2} + \frac{-\frac{1}{8}j}{(z+j)^3} + \frac{\frac{1}{8}j}{(z-j)^3} \tag{3.23}$$

A partial fraction form is always symmetrical. If the partial fraction term $\Psi(z)$ has complex a_z, then it is always paired with a partial fraction term having complex conjugate a_z^*. The first and last two terms in (3.23) are examples of partial fraction terms with a complex conjugate pair of a_z.

If the partial fraction term $\Psi(z)$ contains real a_z, then its pair always has the same real a_z; for example, the third and fourth terms in (3.23). We will return to this observation in the following sections.

3.2.2 The partial fraction terms generalization

Clearly, equations (3.18) and (3.22) are identical. However, the general a_z term in (3.20) does not have its real part equal to zero. For example, a function with two double poles (3.22) corresponds to the following general form

$$H_4(z) = \frac{a_{z1}}{(z-p_1)} + \frac{a_{z1}^*}{(z-p_1^*)} + \frac{a_{z2}}{(z-p_2)^2} + \frac{a_{z2}^*}{(z-p_2^*)^2} \tag{3.24}$$

where $a_{zk} = a_{zkr} + j\,a_{zki}$, $(k = 1, 2)$, $(a_{zkr}, a_{zki} \in \mathcal{R})$ are the real and imaginary parts of the partial fraction coefficients, respectively, and the "*" denotes the complex conjugate operation. Similar expressions can also be derived for the other two cases.

An interesting observation can be made by comparing the numerator in (3.18) with its corresponding expanded numerator in (3.24). The numerator in (3.18) consists of even order terms only, while the numerator in (3.24) consists of both even and odd order terms. Moreover, the maximum order of the numerator in (3.24) is one step higher then the order of the numerator in (3.18).

The above observation points to one of the possible ways to convert the $f_s/4$ transfer function, (3.21) to (3.23), into an equivalent tunable expression. Intuitively, we could assume that the a_{zk} partial fraction constants in (3.24) have a trigonometric (i.e., complex) form $a_{zk} = f(\theta, \sin\theta, \cos\theta)$.

For example, the odd order numerator terms in (3.24) could be multiplied by $\cos\theta$, while the even order terms could be multiplied by $\sin\theta$. In this case, letting $\theta = \pi/2$ would be correct as the newly created "tunable" function would collapse into the $f_s/4$ case. However,

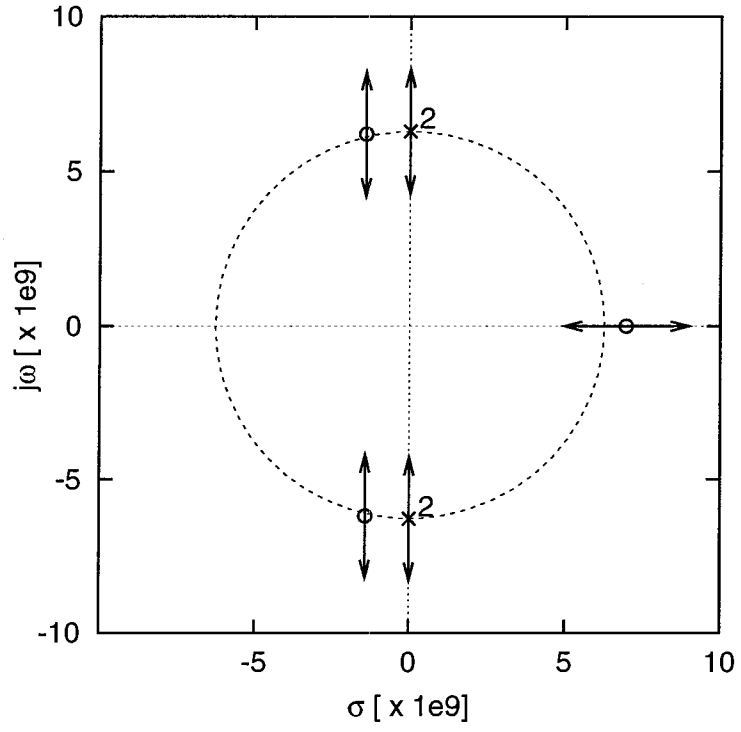


Figure 3.3: The s–domain pole–zero plot for a 4^{th} order $(f_s/4)$ CT BP ΣΔ, with $f_s = 4\,GHz$.

as one would expect, this approach is oversimplified and would not produce a correctly working ΣΔ loop filter function for any other value of θ. In the following subsection, additional arguments to help us determine the shape of the a_{zk} function are introduced. With the help of those arguments, we intend to further reduce the set of possible a_{zk} functions from the infinitely large number of choices down to some finite and manageable number.

3.2.3 The amplitude response

Any rational function can be presented in the following form

$$\begin{aligned} H(\omega) &= A(\omega)e^{j\phi(\omega)} \\ &= K\frac{(j\omega - z_1)(j\omega - z_2)\ldots(j\omega - z_m)}{(j\omega - p_1)(j\omega - p_1)\ldots(j\omega - p_n)} \end{aligned} \tag{3.25}$$

where $A(\omega)$ is the complex magnitude, $\phi(\omega)$ is the complex angle, n is the number of poles, m is the number of zeros, K is the gain factor, z_i are zeros and p_i are poles of $H(\omega)$.

Also, each of

$$A_i = |j\omega - z_i|, \quad B_i = |j\omega - p_i| \tag{3.26}$$

in the s–plane represents a vector length from the current $j\omega$ to the respective pole or zero. After substituting (3.26) into (3.25), the magnitude of the $H(\omega)$ function can be written as

$$A(\omega) = |H(\omega)| = K\frac{A_1 A_2 \dots A_m}{B_1 B_2 \dots B_n} \tag{3.27}$$

By inspection of (3.27), it can be reasoned that the *shape* of the magnitude function $|H(\omega)|$ will not change, if the poles and zeros are moved together and the relative pole–zero ratios are kept constant.

For example, the s–domain $f_s/4$ version of (3.18) has pole–zero locations as shown in Fig. 3.3. As long as the relative positions of the poles and zeros are the same, moving the poles along the $j\omega$ axis will not change the shape of the familiar BP ΣΔ loop NTF and STF response plots. At the same time, the maximal gain of (3.25) can be observed to ensure that it complies with Lee's rule [34].

Obviously, there are an infinite number of possible s–plane trajectories for the poles and zeros, which would still preserve the same transfer function shape. Some of the possible paths are suggested in Fig. 3.3. Also, note that the movement of poles along the $j\omega$ axis in the s–plane is equivalent to tuning the center frequency of a ΣΔ loop transfer function.

An interesting observation from Fig. 3.3 is that the poles and complex pairs of zeros have almost the same absolute values, which puts them close to the same circle. That being the case, the goal is to propose a $a_z(j) \rightarrow a_z(j, \theta, \sin\theta, \cos\theta)$ mapping, such that the pole–zero trajectories come close to the ones in Fig. 3.3.

3.3 Mapping functions

Following the arguments made in the previous section, the conclusion is reached that the process of converting the $f_s/4$ partial fraction terms $\Psi(z)$ into their corresponding tunable versions is not unique; this is due to the infinite number of $\Psi(z, \theta)$ functions that would collapse into the $\Psi(z)$ form at $\theta = \pi/2$. Thus, the exact analysis of this unconstrained problem is not possible. A more intuitive approach must be taken in defining the necessary set of a_{zk} function constraints.

Type	Mapping function
I	$a_z(j,\theta) = -\frac{\sin 2\theta}{2\sin\theta} - j\,2\,a_{z0}\frac{\cos 2\theta}{2\sin\theta}$
II	$a_z(j,\theta) = \frac{e^{j\frac{1}{2}\theta} + 4e^{-j\frac{3}{2}\theta} - 3e^{-j\frac{1}{2}\theta}}{4\left[e^{j\frac{1}{2}\theta} - e^{-j\frac{1}{2}\theta}\right]}$
III	$a_z(j,\theta) = -\frac{\sin 2\theta}{2\sin\theta} - j\left[-a_{z0} + \frac{\cos\theta}{\sin\theta}\right]$
IV	$a_z(j,\theta) = -\cos\theta + j\,a_{z0}\sin\theta$
V	$a_z(j,\theta) = -a_{z0}\,e^{2j\theta}$

Table 3.2: Mapping functions

In this section, one of the possible mapping function families for $a_z(j) \mapsto a_z(j,\theta,\cos\theta,\sin\theta)$ is presented. The mapping functions are applicable to tunable CT BP ΣΔ modulators of the second and fourth order. The direction of the functions is very important, so let us define *positive type* as the clockwise rotation and *negative type* as the counter–clockwise rotation of the mapping functions. In addition, the complex conjugate pair of each mapping function is also included. As discussed in Section 3.2, a_z can be either real or complex. The two possible cases are considered separately.

3.3.1 Mapping functions for complex a_z

In order to reduce the number of possible a_z functions, the following set of s–plane constraints is introduced:

(a) $a_z(\theta) = j\,a_{z0}$ for $\theta = \pi/2$, i.e. $a_z(\theta)$ crosses the imaginary axis at $j\,a_{z0}$. This constraint was already introduced in Section 3.2.2 as the most logical way of guaranteeing that at least the $f_s/4$ case is covered.

(b) $|\mathcal{R}\{a_z(\theta)\}| \leq 1$, i.e. $a_z(\theta)$ is bounded by ± 1 on the real axis. Even though the real boundaries can be anywhere, the ± 1 limit seems a logical choice, considering that the imaginary parts are a fraction of one and the sin and cos functions are always equal to or less than one.

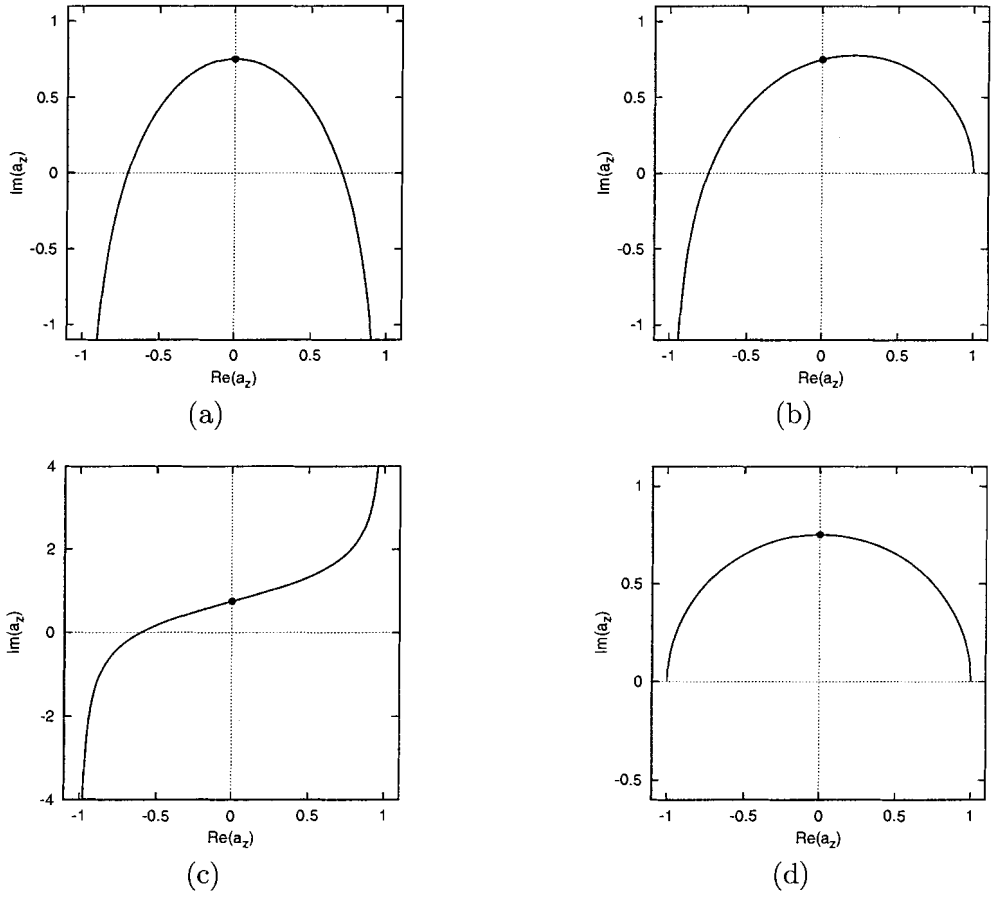


Figure 3.4: Mapping functions of: (a) type I; (b) type II; (c) type III; and (d) type IV. In this example, $a_z = j\,3/4$; the $f_s/4$ case is marked with a black dot.

(c) $a_z(\theta)$ has no loops. The introduction of non–smooth curves with loops would certainly result in higher order analytical forms that are too complicated.

Surprisingly, the above constraints result in only four possible function shapes for the complex a_z, which are shown in Fig. 3.4. The four functions are referred to as type I, II, III and IV. Analytical forms of these four functions are shown in Table 3.2, for positive cases only without the complex conjugate pairs. All four functions cross through the point $a_z(\pi/2) = j\,a_{z0}$, which corresponds to the $f_s/4$ case (black dot on the plots).

Mapping function of type I

The type I function has an imaginary part limited by $\mathcal{I}\{a_z(\theta)\} = -\infty$ for $\theta = 0, \pi$.

Mapping function type II

The type II function has an imaginary part with the following limits: $\mathcal{I}\{a_z(\theta)\} = -\infty$ for $\theta = \pi$ and $\mathcal{I}\{a_z(\theta)\} = 0$, $\mathcal{R}\{a_z(\theta)\} = 1$ for $\theta = 0$.

The analytical result shown in Table 3.2 and Fig. 3.4 is for $a_{z0} = 3/4$ and is easy to adjust for other values of a_{z0}, while still preserving the same function shape.

Mapping function of type III

The type III function has an imaginary part with the following limits: $\mathcal{I}\{a_z(\theta)\} = -\infty$ for $\theta = \pi$ and $\mathcal{I}\{a_z(\theta)\} = +\infty$ for $\theta = 0$.

Mapping function of type IV

The type IV function has the following limits: $\mathcal{I}\{a_z(\theta)\} = 0$, $\mathcal{R}\{a_z(\theta)\} = -1$ for $\theta = \pi$ and $\mathcal{I}\{a_z(\theta)\} = 0$, $\mathcal{R}\{a_z(\theta)\} = 1$ for $\theta = 0$.

3.3.2 Mapping function for real a_z

Our constraining condition for a real a_z corresponds to constraint (a) in the complex a_z case: the crossing point on the real axis (i.e. the $f_s/4$ case) is satisfied for $a_z(\pi/2) = a_{z0}$, $a_{z0} \in \mathcal{R}$.

A complex function that satisfies the above condition, among an infinite number of other choices, is the mapping function which describes a full circle, as $\theta = -\pi, \ldots, +\pi$ in the s–plane. This function is referred to as type V and its analytical form is shown in Table 3.2.

3.4 Zero delay CT BP ΣΔ modulators

The transformation functions outlined in Sections 3.1 and 3.3 can now be applied to deliver the corresponding s–domain filter transfer functions. The following sections show results for the second, fourth and sixth order CT BP ΣΔ modulators. Unless otherwise stated, all examples used the following settings: $f_s = 4\,GHz$, SNR measured over $BW = 20\,MHz$, input signal amplitude $v_{in} = 0.27\,V$, comparator output levels $\pm 1V$ and 16384 point FFT.

3.4.1 Second order CT BP ΣΔ

The application of type I to IV mapping functions and the transformation functions listed in Table 3.1 to (3.17) and (3.21) yields eight possible outcomes. However, only four of them

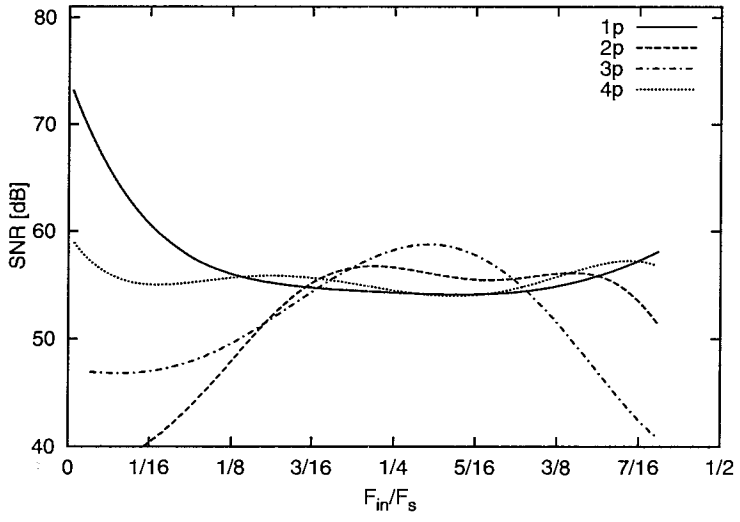


Figure 3.5: A comparative plot of 2^{nd} order CT BP ΣΔ functions corresponding to the four types of positive mapping functions; averaged curves shown. The legend refers to the type of mapping function used; for example, "1p" refers to the positive mapping function of type I.

produce correctly working CT BP ΣΔ modulators, all of which are associated with the positive type mapping functions. Each of the four resulting s–domain functions exhibits a different tuning range, shown in Fig. 3.5. The legend refers to the type of mapping function used; for example, "1p" refers to the positive mapping function of type I.

The analytical s–domain expression of the transfer function associated with the positive mapping function of type I is

$$H_0(s) = \frac{-\frac{1}{2}\frac{(2\cos\theta+1)}{\sin\theta}\frac{\theta}{T}s + \frac{1}{2}\frac{(2\cos\theta-1)}{(\cos\theta-1)}\frac{\theta^2}{T^2}}{s^2+\frac{\theta^2}{T^2}} \tag{3.28}$$

with the other three functions having similar expressions. Note that application of the positive mapping function of type I exhibits the widest tuning range. However, for signal frequencies of $f_s/16$ and lower, the modulator practically degenerates into a very good low–pass ΣΔ modulator. Application of the type IV mapping function yields a function with a very uniform and wide tuning range. The last two functions exhibit a narrower tuning range, as well as a larger amount of overtones in the frequency domain response.

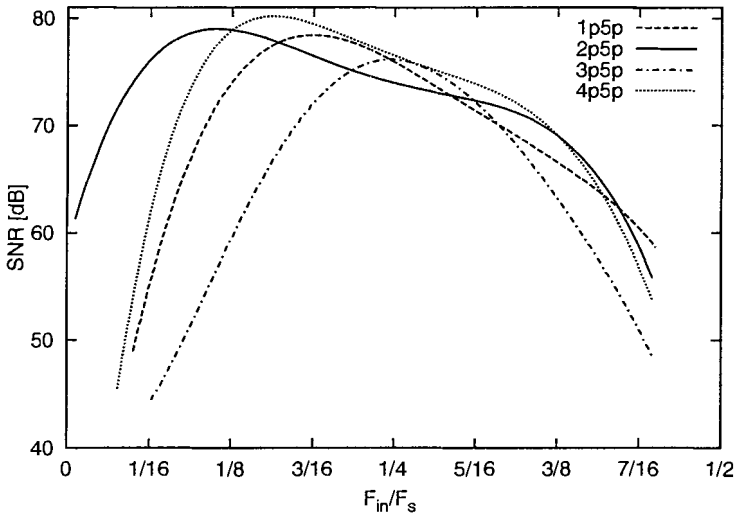


Figure 3.6: A comparative plot of 4^{th} order CT BP ΣΔ functions corresponding to the four types of positive mapping functions; averaged curves shown.

3.4.2 Fourth order CT BP ΣΔ

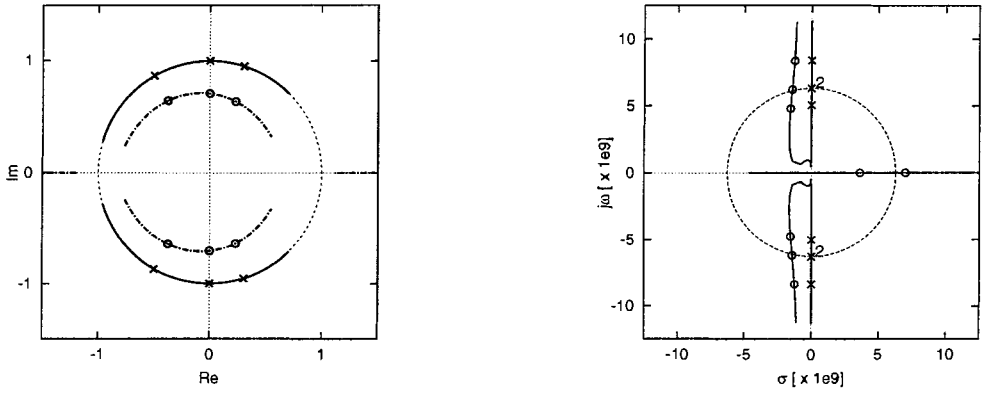
The application of type I to V mapping functions and the transformation functions listed in Table 3.1 to (3.18) and (3.22) yields sixteen possible outcomes.

Again, only four of them produce correctly working CT BP ΣΔ modulators, all of which are associated with the positive types of mapping functions.

Continuous time transfer function

The loop filter transfer function $H(s)$, associated with type II and V mapping functions, produced the modulator with the widest tuning range, shown in Fig. 3.6 under label "2p5p". The exact form of the s–domain function "2p5p" consists of a third order numerator and two double poles displaced from the center frequency by $\pm\delta$:

$$H_0(s) = \frac{\frac{H_{03}}{T}s^3 + \frac{H_{02}}{T^2}s^2 + \frac{H_{01}}{T^3}s + \frac{H_{00}}{T^4}}{\left[s^2 + \left(\frac{\theta-\delta}{T}\right)^2\right]\left[s^2 + \left(\frac{\theta+\delta}{T}\right)^2\right]} \tag{3.29}$$



z–plane s–plane

Figure 3.7: Pole–zero plots for a 4^{th} order ΣΔ modulator, with $\theta = \pi/1.1, \ldots, \pi/4$ and $f_s = 4\,GHz$. The complex poles and zeros move clockwise in the z–plane; the real zero first moves to $-\infty$ for $\theta = \pi/2$ and then approaches the origin from $+\infty$. At the same time, the complex poles and zeros move outwards in the s–plane, while the real zero moves from left to right.

where,

$$H_{03} = -\frac{\theta}{2}\frac{\sin\theta}{(1-\cos\theta)} - \frac{1}{4}$$

$$H_{02} = \frac{\theta^2}{4}\frac{(3-4\cos\theta)}{(1-\cos\theta)} - \frac{\theta}{2}\frac{\sin\theta}{(1-\cos\theta)}$$

$$H_{01} = -\frac{\theta^3}{2}\frac{\sin\theta}{(1-\cos\theta)} + \frac{\theta^2}{4}$$

$$H_{00} = \frac{\theta^4}{4}\frac{3-4\cos\theta}{(1-\cos\theta)}$$

and δ is the separation angle between the pole pairs and the center notch frequency [52]. For $\delta = 0$, the two pairs of poles collapse into a double pole.

Tuning range

Each of the resulting four s–domain functions exhibits a different tuning range, shown in Fig. 3.6. The code used in the legend is as follows: the first two alphanumerics specify the mapping function type being used for the first and second term in (3.22). For example, "1p" specifies a positive mapping function of type I. Similarly, the last two alphanumerics specify the mapping function being used for the third and fourth term in (3.22). Note the use of the complex conjugate mapping functions in both cases.

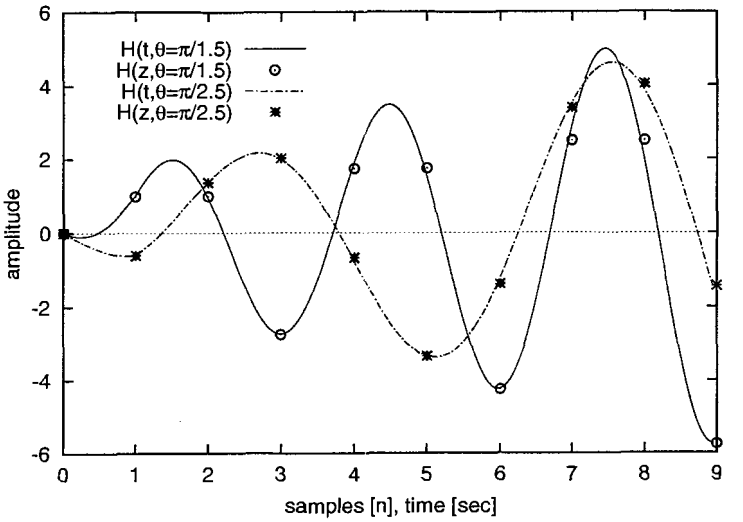


Figure 3.8: Impulse response $h(t)$ and corresponding tunable $h[n]$.

The actual pole–zero trajectories of (3.29) are shown in Fig. 3.7, for $\theta = \pi/1.1, \ldots, \pi/16$. Pole–zero locations for $\theta = \pi/1.5, \pi/2$, and $\pi/2.5$ are shown for comparative purposes. For a tuning range of $\theta = \pi/1.1, \ldots, \pi/4$, the s–plane pole–zero trajectories are similar to the ones shown in Fig. 3.3.

Impulse response

The pulse invariance equivalence corresponding to the tunable z–domain version of (3.18) and its corresponding s–domain function (3.29) is shown in Fig. 3.8, for $\theta = \pi/1.5, \pi/2.5$. The first two samples of this function are equal to zero in the case of the $f_s/4$ modulator [48]. A change in the tuning parameter θ causes the second sample to move away on either side, while the rest of the samples follow accordingly.

The plot confirms the impulse invariance equivalence of the s–domain function with its counterpart in the z–domain.

Maximal SNR

A commonly used linear model for predicting theoretical maxima of SNR was described in [36] by the following formula

$$SNR_{max} = (2^b - 1)\sqrt{\frac{3}{2}}\frac{\sqrt{2n+1}}{\pi^n} OSR^{(n+\frac{1}{2})} \tag{3.30}$$

where b is the number of the quantizer bits, n is the modulator order as defined in (3.15), and OSR is the oversampling ratio. For the results presented in this chapter $OSR = f_s/(2\,BW) = 100$, which means the linear model predicts $SNR_{max} \approx 88.9\,dB$.

Another often cited model for predicting the maximal SNR was published in [2]. It was based on the describing method and later modified in [42]. The original "Ardalan bound" version was used as a comparison, with simulation results of (3.29). In the simulations, a sinusoidal input signal was used to generate plots for the three values of θ, shown in Fig. 3.9. While the Ardalan bound is more conservative then the linear model and predicts $SNR_{max} \approx 77.6\,dB$, the actual simulations show a value of $SNR_{max} \approx 86\,dB$.

STF and NTF functions

The AC simulation results for NTF and STF related to (3.29) are shown in Fig. 3.10 and Fig. 3.11, respectively. The tuning parameter θ controls the position of the notch in the NTF response, as well as the centering of the STF pass–band response. One of the commonly cited criteria for ΣΔ loop stability is referred to as Lee's rule [34]. In its original version, the maximal allowed gain for these two functions was set at two (i.e., 6dB). However, most researchers further constrained this rule to 1.6 to allow for process variations.

The NTF and STF maximum gain plots corresponding to $\theta = \pi/4 \ldots \pi/1.3$ are shown in Fig. 3.12. The plots show that the maximum gain for both the NTF and the STF are well below Lee's limit, indicating that the loop is stable.

3.4.3 Sixth order CT BP ΣΔ

The analytical approach presented here has its limitations. For example, the set of mapping functions shown in Section 3.3 is not sufficient to produce a *tunable* version of the sixth order CT BP ΣΔ function. Also, the complexity of the working equations becomes very high. For example, the intermediate equations required for the sixth order modulator reach as many as one thousand terms. For all practical purposes, the work becomes impossible without the help of symbolic mathematical software. One possible solution for a simpler CT BP $f_s/4$ ΣΔ sixth order variant is as follows

$$H_0(s) = \frac{\frac{H_{05}}{T}s^5 + \frac{H_{04}}{T^2}s^4 + \frac{H_{03}}{T^3}s^3 + \frac{H_{02}}{T^4}s^2 + \frac{H_{01}}{T^5}s + \frac{H_{00}}{T^6}}{\left[s^2 + \left(\frac{\theta-\delta}{T}\right)^2\right]\left[s^2 + \left(\frac{\theta}{T}\right)^2\right]\left[s^2 + \left(\frac{\theta+\delta}{T}\right)^2\right]} \tag{3.31}$$

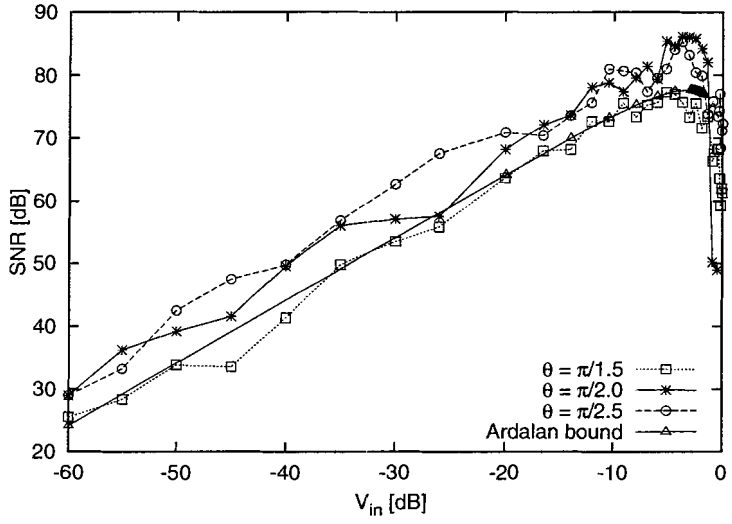


Figure 3.9: Relationship between the SNR and normalized input signal, for three values of θ. The Ardalan bound is also indicated.

where,

$$
\begin{aligned}
H_{05} &= -\frac{49}{256}\pi - \frac{69}{128} \\
H_{04} &= +\frac{121}{512}\pi^2 - \frac{73}{128}\pi - \frac{1}{64} \\
H_{03} &= -\frac{49}{512}\pi^3 + \frac{3}{128}\pi \\
H_{02} &= +\frac{121}{1024}\pi^4 - \frac{73}{512}\pi^3 + \frac{3}{256}\pi^2 \\
H_{01} &= -\frac{49}{4096}\pi^5 + \frac{69}{2048}\pi^4 - \frac{1}{512}\pi^3 \\
H_{00} &= +\frac{121}{8192}\pi^6
\end{aligned}
$$

and δ is the separation angle between the pole pairs and the center notch frequency. For $\delta = 0$, the three pairs of poles become equal, resulting in triple poles.

Both the AC and transient simulations of (3.31) show that the NTF and STF functions exhibit appropriate maximal gains according to Lee's rule. However, even though the maximal SNR is in relatively close agreement with the Ardalan bound, it falls short of the $120dB$ value predicted by the linear model, Fig. 3.13. Furthermore, the maximal SNR is much worse that the one achieved by (3.29), which indicates that some form of numerical optimization is required if the optimal SNR is to be reached for this modulator.

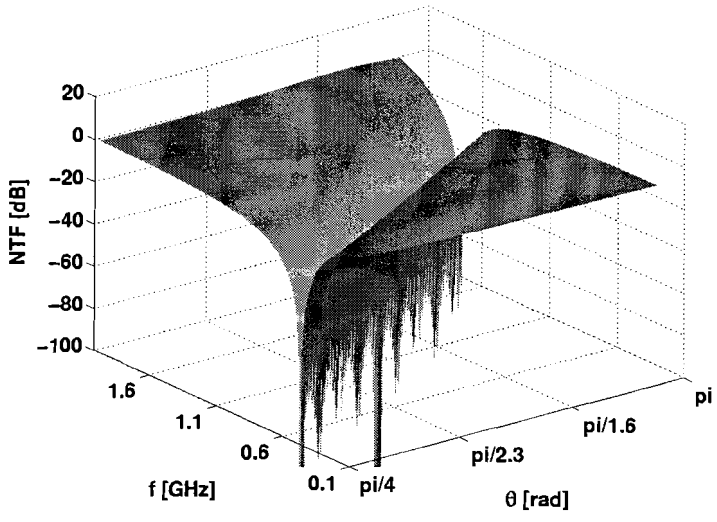


Figure 3.10: AC simulation of NTF for 4^{th} order tunable CT BP ΣΔ model.

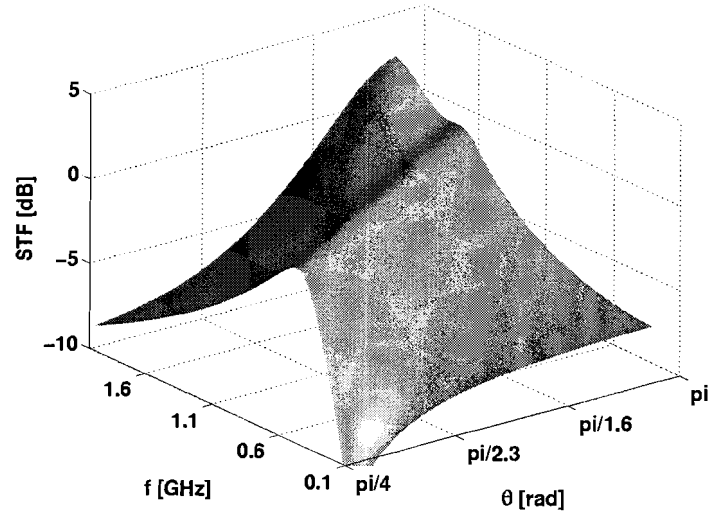


Figure 3.11: AC simulation of STF for 4^{th} order tunable CT BP ΣΔ model.

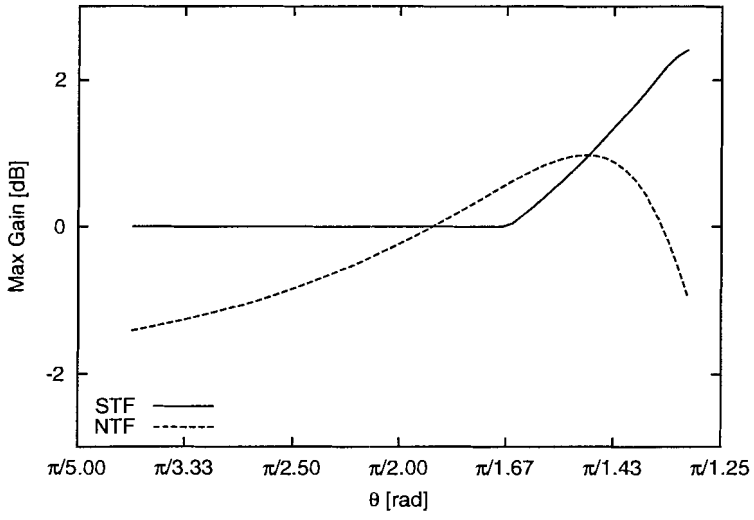


Figure 3.12: Maximum gain corresponding to the NTF in Fig. 3.10 and the STF in Fig. 3.11.

3.5 Delayed CT BP ΣΔ modulators

The equations shown so far describe *zero delay* ΣΔ loops. The zero delay term refers to ΣΔ architectures without the feedback latch. In other words, the loop transfer function is completely determined by the loop filter transfer function, $H_0(z)$ or $H_0(s)$.

To emphasize the importance of the zero delay formulation of the loop function, the following statement should be kept in mind. The *overall* loop delay around any CT ΣΔ loop must be equivalent to the zero delay formulation. In other words, any delay introduced inside the loop path, due to circuitry propagation times, must be subtracted from the loop filter transfer function. This situation is the main cause of problems related to the loop delays encountered in CT ΣΔ modulators. Analytical methodologies inherited from z–domain mathematics allow for the calculation of the loop filter functions with an integer number of clock delays. Usually, a latch is used to introduce a one clock period delay in the feedback part of the loop. Consequently, the loop filter must be modified to exclude the one clock delay from its own transfer function, so that the overall ΣΔ loop transfer function is still equivalent to the zero delay scheme.

For example, the division of (3.17) to (3.19) by z^{-1} results in a *one delay filter* transfer function. Since the numerators in (3.17) to (3.19) are just one order lower than their corresponding denominators, this procedure can only accommodate up to two delay transfer

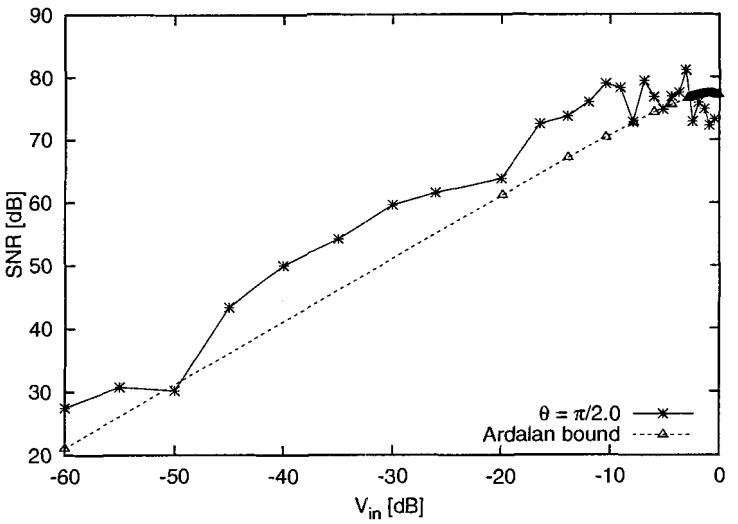


Figure 3.13: Maximal SNR versus normalized input signal for a 6^{th} order CT BP ΣΔ function ($f_s/4$ case).

functions.

Instead of creating the delayed versions in the z-domain, we start from the s–domain equations. The Laplace transformation of (3.28) to (3.31) creates the time domain equivalent expression of $H_0(s)$. The newly created time domain function is then shifted in the time domain by *fractional* multiples of the clock period T. Finally, the application of the inverse Laplace transformation produces the delayed s–domain version of $H_0(s)$.

In theory, the above procedure should produce loop transfer functions with any fractional number of clock delays. The mathematical description of the three step procedure is as follows

$$H_0(t) = \mathcal{L}\{H_0(s)\} \tag{3.32}$$

$$H_k(t) = H_0(t + kT) \tag{3.33}$$

$$H_k(s) = \mathcal{L}^{-1}\{H_k(t)\} \tag{3.34}$$

where k is the fractional number of clock period delays being introduced. Transient simulations demonstrate that clock period delays less than or equal to four are not enough to destabilize a fourth order ΣΔ loop.

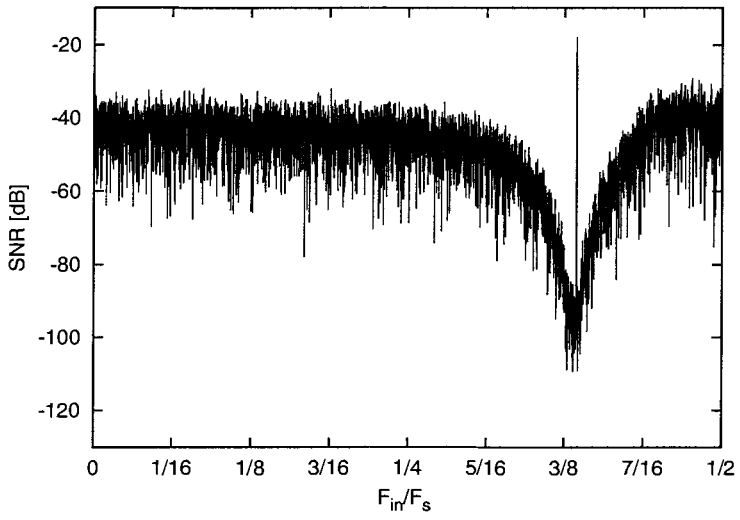


Figure 3.14: Transfer function of tunable 4^{th} order CT BP ΣΔ with fractional delay. This modulator transfer function has an overall loop delay of $td = T/8$ and $\theta = \pi/1.3$.

Applying (3.32) through (3.34) to (3.29) and setting $k = 1/8$ yields the following s–domain function

$$H_0(s) = \frac{\frac{H_{03}}{T}s^3 + \frac{H_{02}}{T^2}s^2 + \frac{H_{01}}{T^3}s + \frac{H_{00}}{T^4}}{32\,(\cos\theta - 1)\left[s^2 + \left(\frac{\theta-\delta}{T}\right)^2\right]\left[s^2 + \left(\frac{\theta+\delta}{T}\right)^2\right]} \tag{3.35}$$

where,

$$\begin{aligned} H_{03} &= a\,\theta - 8\,b \\ H_{02} &= c\,\theta^2 + 16\,d\,\theta \\ H_{01} &= a\,\theta^3 + 8\,b\,\theta^2 \\ H_{00} &= c\,\theta^4 \end{aligned}$$

and

$$\begin{aligned} a &= \left(25\sin\frac{9}{8}\theta - 8\sin\frac{7}{8}\theta - 25\sin\frac{1}{8}\theta\right) \\ b &= \left(\cos\frac{9}{8}\theta - \cos\frac{1}{8}\theta\right) \\ c &= \left(25\cos\frac{9}{8}\theta + 8\cos\frac{7}{8}\theta - 25\cos\frac{1}{8}\theta\right) \\ d &= \left(\sin\frac{9}{8}\theta - \sin\frac{1}{8}\theta\right) \end{aligned}$$

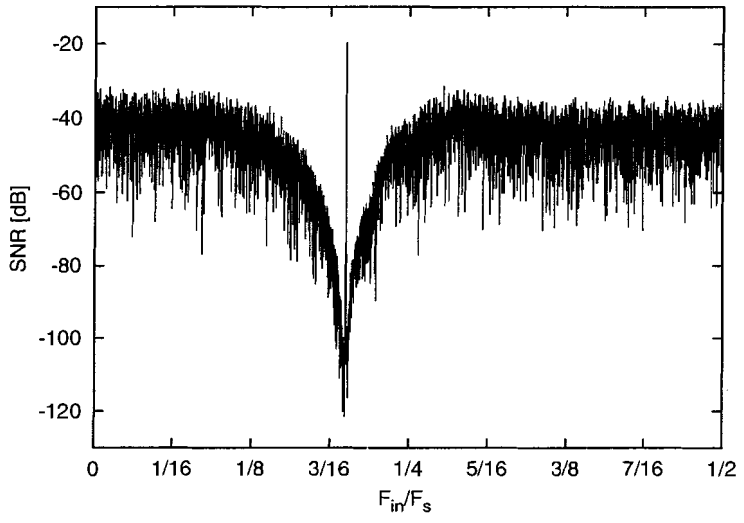


Figure 3.15: Transfer function of a tunable 4^{th} CT BP ΣΔ with fractional delay. This modulator transfer function has an overall loop delay of $td = T/8$ and $\theta = \pi/2.5$.

and δ is the separation angle between the pole pairs and the center notch frequency. For $\delta = 0$, the two pairs of poles collapse into a double pole.

The importance of being able to design a fractional multiple clock delay CT ΣΔ loop version becomes more evident at high frequencies. The high frequency input signals are associated with even higher frequencies of the sampling clocks. To make the situation even worse, the parasitic layout capacitances become more dominant factors at high frequencies. It is easy to visualize a situation where the *overall* loop delay is longer then one clock period due to parasitic capacitances alone.

An example of a fractional delay ΣΔ loop function output (3.35), which is set to match an overall loop delay of $T/8$, is shown in Fig. 3.14. If no additional numerical optimization of the loop filter function is performed, then according to Fig. 3.6, the overall circuit would have a somewhat lower SNR relative to the $f_s/4$ case. On the other hand, setting the input signal frequency closer to DC would result in an increased SNR relative to the $f_s/4$ case, Fig. 3.15. The dependence of the SNR upon introduced delay is shown in Fig. 3.16, for a $f_s/4$ ΣΔ transfer function.

The argument being made is that instead of trying to cancel the unavoidable loop delay, it should be incorporated in the design.

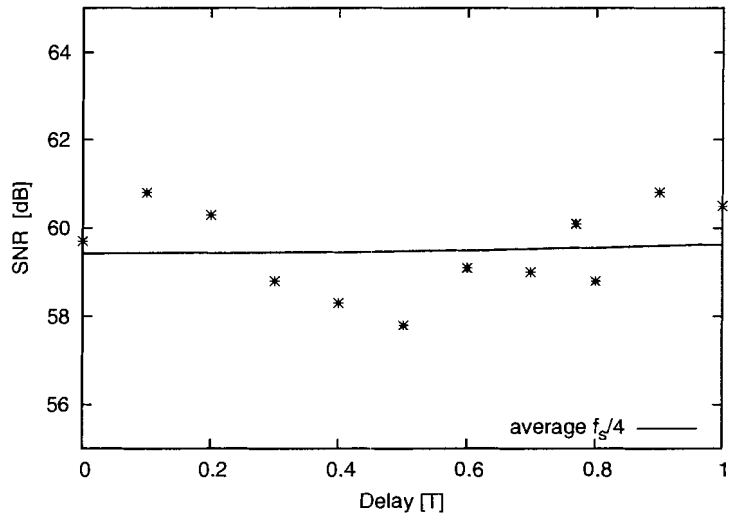


Figure 3.16: Dependence of a 4^{th} order $f_s/4$ fractional CT BP ΣΔ transfer function on the delay time (relative to the clock period T).

3.6 Summary

An analytical design methodology for tunable continuous time bandpass ΣΔ modulators with fractional delays ($f\Sigma\Delta$) has been presented. The procedure has been successfully used to develop working models of second and fourth order CT BP $f\Sigma\Delta$ loops. The models have been verified via simulations and compared in terms of tunability range, maximal SNR and stability. As a result, this approach allows the excess loop delay to be incorporated into the transfer function.

Chapter 4

Behavioral modeling

In Chapter 3, a detailed concept for a CT BP $f\Sigma\Delta$ modulator was introduced. The purpose of this chapter is to describe the simulation methodology used in this dissertation.

CT $\Sigma\Delta$ modulators are, by nature, mixed–signal systems. This creates a discontinuity in the traditional IC design flow, which assumes that "discrete" and "continuous" time domain systems require separate design tools. In this chapter, a top level behavioral CT $\Sigma\Delta$ modeling methodology [51] is presented, which can be used within the analog IC design environment. Mixed–signal models of the CT $\Sigma\Delta$ sub–blocks were built using primitives available in *SPICE* [45] and *Verilog–A*^{TM} . Due to the mixed–signal nature of the circuits, we used *Spectre*^{TM} for all simulations.

4.1 Simulation flow

Traditionally, the behavior of a $\Sigma\Delta$ modulator is simulated by creating z–domain models and using a DT simulator, such as *MATLAB*©. This approach is logical since $\Sigma\Delta$ modulators are sampled systems by nature. As a result, most of the $\Sigma\Delta$ implementations were done by using techniques such as switched capacitors and switched current. The increased interest in the high speed continuous time $\Sigma\Delta$ modulators created a problem with the traditional IC design flow, which is not well suited to this application. The principle reason is that the discrete domain simulators were not well connected to the back end IC design tools; at the same time, continuous time simulators were lacking top level behavioral modeling capability. However, mixed–signal simulators are now becoming more practical and are incorporated into the analog IC design environment. Previously published works on $\Sigma\Delta$

modeling were based either on $SIMULINK^{®}$ models [3], custom made C programs, or $Verilog\text{–}A^{TM}$ [58, 44].

A general high speed CT $\Sigma\Delta$ modulator loop architecture was shown in Fig. 3.1. The loop filter $H(s)$ is typically either LP or band–pass. Due to the presence of a high speed clock and quantizer, CT simulators exhibit very long simulation times and DT simulators use high level models, which do not offer enough insight into the circuit's behavior.

Today, DT IC design tools are well developed, making it possible to design very complicated switched capacitor ICs, without having to use any of the CT tools such as $SPICE$. However, in order to design an analog CT IC, one must use a tool that is capable of simulating in the CT domain. A CT $\Sigma\Delta$ modulator is an example of a mixed–signal circuit that creates discontinuities in the IC design flow. It requires a smooth connection between the behavioral models developed in DT and the physical realization of the IC circuits. Bridging these two worlds is one of the motivations behind the work presented in this chapter.

One method used to reduce simulation time is to create circuit behavioral models using methodologies and tools developed for analog CT IC design. Unfortunately, $SPICE$ based simulators have limited behavioral modeling capability. This problem was recognized in the early days of analog simulators, which resulted in the development of "mixed–signal" simulators. Fortunately, it is now possible to create behavioral model sub–blocks using primitives from $SPICE$ along with ones from $Verilog\text{–}A^{TM}$. Depending upon the circuit complexity and architecture, this arrangement can reduce the simulation time by orders of magnitude.

4.2 Basic functional blocks

In this section, behavioral models of the basic functional blocks required to create a complete CT $\Sigma\Delta$ modulator are introduced. The models are developed in $SPICE$ [45] and $Verilog\text{–}A^{TM}$ [14]; the simulator used was $Spectre^{TM}$ within $Analog\text{–}Artist^{TM}$. In order to implement functional block diagram in Fig. 3.1 the following set of DT/CT behavioral modules is used: general s–transfer function $H(s)$, comparator, D flip–flop (DFF), DAC with NRZ, RZ and HZ pulses, summing block, the loop delay block, and clock with controlled jitter. Another important requirement was that all the modules have a controlled propagation delay. Transition from the functional diagram in Fig. 3.1 into the behavioral domain in Fig. 4.3 is achieved by introducing the following behavioral block–level models.

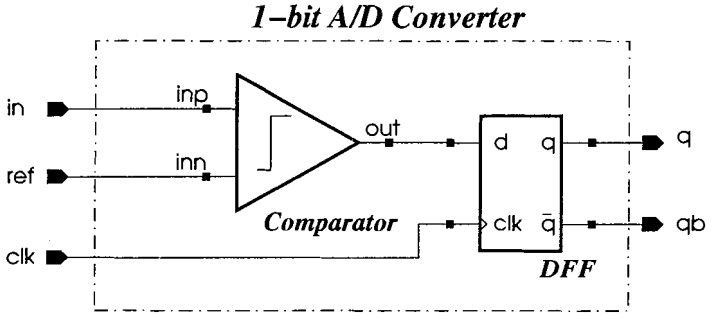


Figure 4.1: Schematic for a 1–bit quantizer.

4.2.1 s–domain transfer function $H(s)$ model

A general s–domain transfer function is needed to create a higher order CT $\Sigma\Delta$ filter loop function $H(s)$. The *Verilog–A*^{TM} `laplace_nd` function was used to create the transfer function $H(s) = N(s)/D(s)$, where `n0, n1, .. nN` are the $N(s)$ polynomial coefficients, `d0, d1, .. dD` are the $D(s)$ polynomial coefficients, and $N + 1 \leq D$.

4.2.2 A/D converter model

The A/D block in Fig. 3.1 is modeled as a 1–bit quantizer and implemented with a comparator and a DFF, Fig. 4.1. It is possible to create an s–domain comparator using *SPICE* behavioral primitives [44, 7], however *Verilog–A*^{TM} code is used is this research. Both models have similar simulation times.

Comparator: The `tanh` function was used to simulate the maximal signal levels of the comparator. The code that implements the comparator function is

```
V(out) <+ 0.5*(outHigh-outLow)
          * tanh(slope*(V(in, ref)
          - inOffset))
          + 0.5*(outHigh + outLow);
```

One of the problems with using *SPICE* to model a comparator, is that the *min–max* range used in the *VCVS* function is not exported by the *Analog–Artist*^{TM} netlister. These small syntax differences that are not supported by the *Analog–Artist*^{TM} netlister

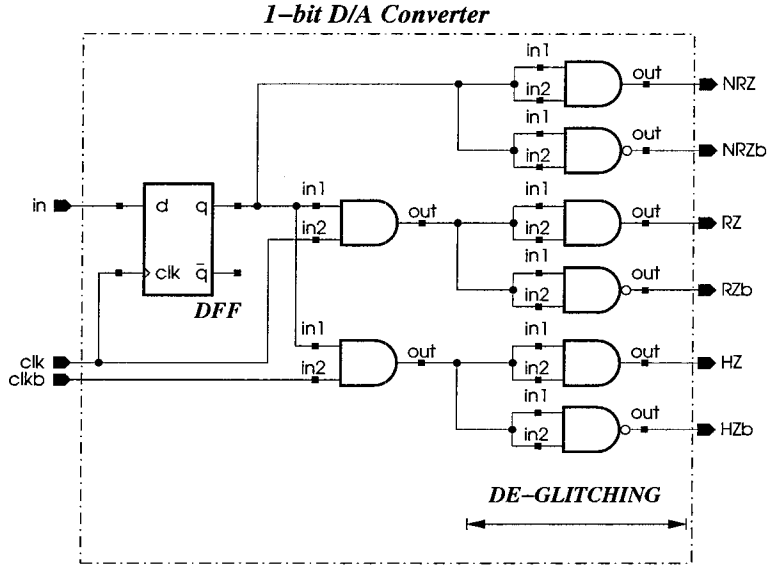


Figure 4.2: DAC schematic.

are important factors, which must be taken into consideration when the goal is to make a versatile model that works within the *Analog-Artist*^{TM} environment and as a stand-alone model.

4.2.3 D/A converter model

A schematic of the DAC is shown in Fig. 4.2, consisting of the DFF and digital AND gates. One of the assumptions in DT analysis is that the pulse is NRZ. However, as previously mentioned, in CT systems the pulse can take on various forms, such as: RZ, HZ, and NRZ, [49], [48], [5]. Also, during implementation there is often a need for the inverted pulses, $\overline{\text{NRZ}}$, $\overline{\text{RZ}}$, and $\overline{\text{HZ}}$, as well (labeled NRZb, RZb, and HZb on the schematic).

For the purposes of our DAC, we used `high=1` and `low=-1`. The DFF delivers NRZ data at the rising edge of the clock. By using both phases of the clock and eight AND/NAND gates, we created NRZ, RZ, and HZ data. The total propagation time of the circuit can be controlled at the output gates, while the rest of the gates in the circuit can have a delay time equal to zero.

Finite rising and falling times of the pulse edges cause glitches in the switching logic. These glitches are one source of the "rising noise floor". The usual practice in CT design is to add "de-glitching" buffers at the interface between DT and CT domains.

D flip–flop (DFF): A *Verilog–A*^{TM} model of the DFF is created, which is a basic delay unit equivalent to z^{-1}. The key code lines for the DFF are

```
@(cross(V(CLK)-Vth, +1)) x=(V(d) > Vth);
V(q)    <+ transition(voutHigh*x  +
           voutLow*!x, delay, transitTime);
V(qbar) <+ transition(voutHigh*!x +
           voutLow*x,  delay, transitTime);
```

AND/NAND gates: The digital AND/NAND gates are implemented with the following code

```
out = (logic1 && logic2) ?
            vlogicHigh : vlogicLow;
V(vout) <+ transition(out, delay,
           trise, tfall);
```

4.2.4 Summing function model

Note that the $\Sigma\Delta$ loop (Fig. 3.1) can be designed to work both with the "+" and the "-" sign in the summing block. The summing block with propagation delay code is as follows

```
V(out) <+ absdelay(V(in1)+V(in2),delay);
```

4.2.5 Loop delay function model

Similarly, the loop delay function model (Fig. 4.3) is given by

```
V(out) <+ absdelay(V(in)*k,delay);
```

4.2.6 Sampling clock model

The most convenient way to implement an ideal clock that has no jitter is by using the `vpulse` function from *SPICE*. A two–phase ideal clock reference is created by using two `vpulse` sources.

Clock jitter is a very important element in CT $\Sigma\Delta$ modulators, [5]. Unfortunately, there is no straightforward method to create a clock pulse with added jitter in *SPICE*. However, both *MATLAB*© and *Verilog–A*^{TM} have a random number generator function.

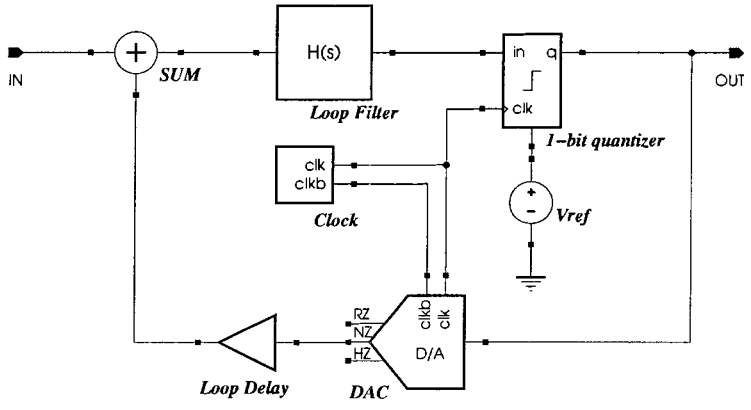


Figure 4.3: Schematic of a general CT ΣΔ modulator.

The main problem with modeling clock jitter in the time domain is that the jitter distribution is not known prior to starting the simulation. The mean value and variance (zero and one in this case, respectively) are defined over the *length of the simulation*, measured in the number of the clock cycles. Generating jitter on the clock edges is not possible during the simulation, therefore some initial work is required. A `randn` (*MATLAB*©) function is used to generate a vector of random numbers with a normal distribution and $var = 1$ over a given number of clock cycles.

Generating data for 2^N clock cycles simplifies the FFT analysis. The *SPICE* `vpwlf` was used to import this two-column clock data file into the simulations. A number of data files were generated, incorporating various amounts of jitter.

4.3 Simulation examples

The set of basic blocks described in the previous sections allowed for behavioral model simulations of a CT ΣΔ modulator. The models are generic and used inside *Analog–Artist*^{TM}. The obvious implication of this approach is that in subsequent phases of the IC development, we can swap transistor level *SPICE* models for the various sub–blocks and evaluate model performance with the rest of the circuit being "ideal". Due to the mixed–signal nature of the circuits, we used *Spectre*^{TM} for all simulations. In this section, examples of simulation results are shown for two categories of the CT ΣΔ modulators: first order low–pass and fourth order band–pass.

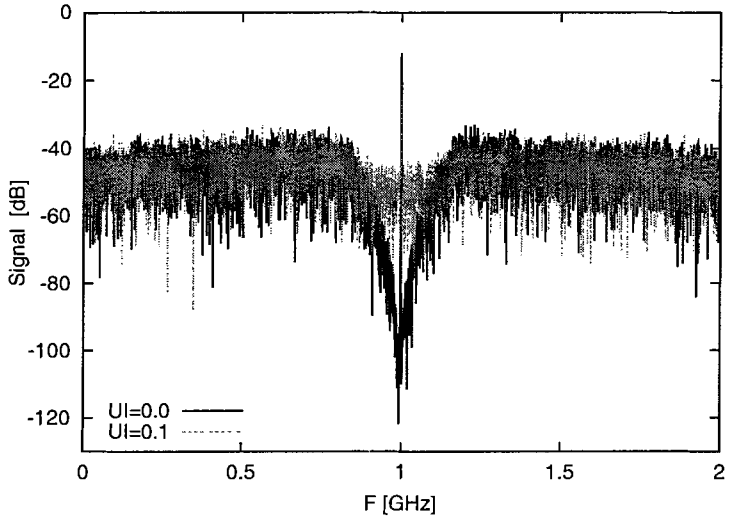


Figure 4.4: 4^{th} order CT BP $\Sigma\Delta$ modulator output.

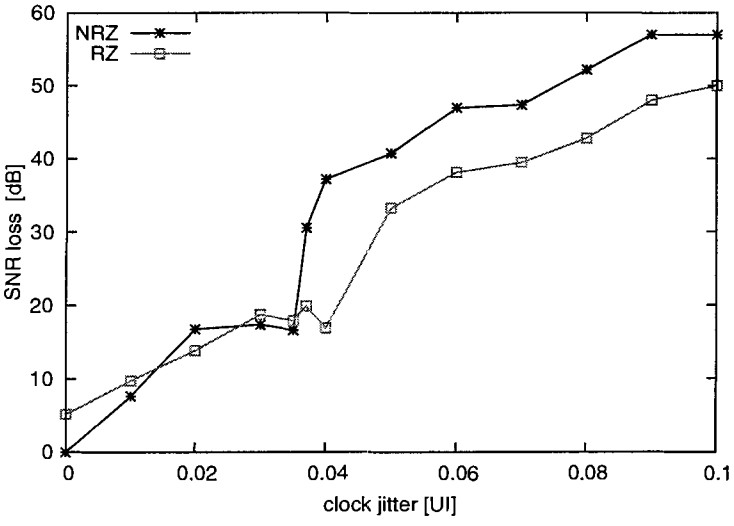


Figure 4.5: *SNR* versus clock jitter for a 4^{th} order CT BP $\Sigma\Delta$ modulator.

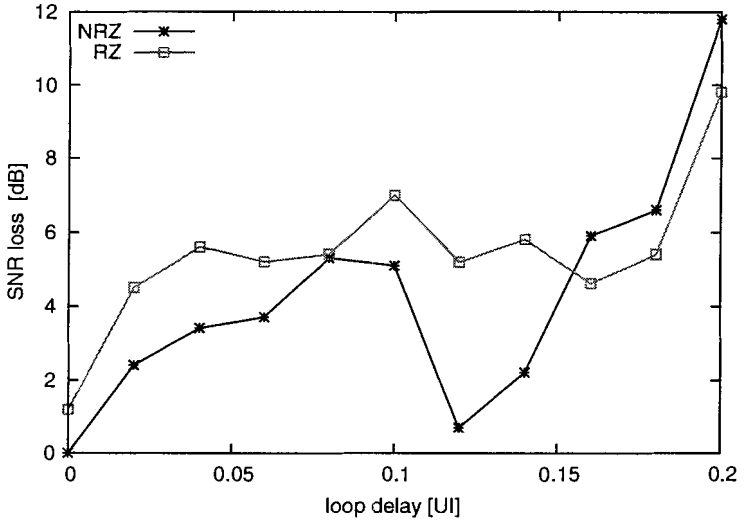


Figure 4.6: *SNR* versus loop delay for a 4^{th} order CT BP $\Sigma\Delta$ modulator.

Continuous time low–pass (CT LP)

The simulation setup is shown in Fig. 4.3, where $H(s) = 1/s$ was implemented using an LP filter with a single integrator and was used to simulate a first order CT LP $\Sigma\Delta$ modulator. A single simulation run, including a 16384 point FFT plot, took less then 2 minutes of CPU time on a SUN Blade1000 computer, when using a $1GHz$ clock, $2MHz$ single tone input signal, and running 16384 clock cycles.

Continuous time band–pass (CT BP)

The schematic shown in Fig. 4.3 was also used to simulate the fourth order CT BP $\Sigma\Delta$ modulator, where a BP filter function was implemented using the general s–function block. The $\Sigma\Delta$ modulator was simulated with and without jitter, for a $1\,GHz$ signal, sampled by a $4\,GHz$ clock over $4096\,ns$; the output plot is shown in Fig. 4.4 for jitter values of $UI = 0$ and $UI = 0.1$. This structure can also be implemented with one RZ clock delay. A plot showing the maximal *SNR* vs. clock jitter for the two cases is shown in Fig. 4.5, while the *SNR* vs. loop delay is shown in Fig. 4.6.

The examples shown in this section demonstrate an efficient way to simulate CT $\Sigma\Delta$ modulators in the time domain, within the standard IC design flow. Behavioral modeling methodology was used throughout this work.

4.4 Summary

A mixed–signal behavioral modeling methodology for a CT $\Sigma\Delta$ modulator circuit has been presented. It was shown that by using a mixed–signal approach for behavioral modeling and using only one design environment throughout the design process, high simulation speeds can be achieved and meaningful results can be produced. A mixture of *Verilog–A*^{TM} and *SPICE* models allows for rapid behavioral level simulations within the *Analog–Artist*^{TM} environment commonly used by analog IC designers.

Chapter 5

CT BP $f\Sigma\Delta$ modulator design

The previous chapters introduced the theoretical background for CT BP $f\Sigma\Delta$ modulators, followed by a behavioral modeling methodology. In this chapter, a transistor level design of a fourth–order tunable CT BP $f\Sigma\Delta$ modulator in $0.5\mu m/f_T = 47\,GHz$ SiGe technology is presented.

The modulator is a fully differential g_m–C based circuit, that demonstrates a practical implementation of the analytical methodology used in designing the fractional CT loop transfer functions $H(s)$ presented in Chapter 3. A loop filter transfer function is designed to compensate for the unavoidable loop delay. As a result, a new topology for the CT BP $f\Sigma\Delta$ modulator is suggested.

5.1 Design architecture

Currently, CT BP $\Sigma\Delta$ modulators are being designed for RF frequencies [8, 40, 35]. Since a complete analytical model of a *tunable* CT BP $\Sigma\Delta$ modulator did not exist, virtually all published tunable designs were developed using numerical filter design methods [46, 41]. However, closed–form analytical solutions are generally preferred, as they offer more insight into circuit operation fundamentals and provide flexibility in the design process [50].

A diagram of the top level modulator architecture, based on the analytical model published in [50], is shown in Fig. 5.1. The CT loop filter transfer function $H(s)$ and summing circuit are both g_m–C based structures. This design employs a 1–bit comparator and, instead of a conventional 1–bit DAC, a programmable analog delay line. The length of the delay line is controlled by the mixed–signal control bus; it can generally be programmed

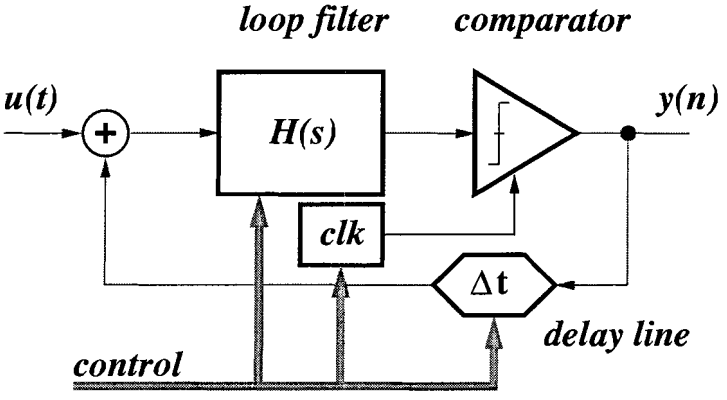


Figure 5.1: Block diagram for a CT $f\Sigma\Delta$ modulator.

to have a value ranging from zero to several clock cycles. The maximum delay length is hardwired by the number of on–chip delay elements.

Conventionally, in order to correctly synthesize both the NTF and STF of the modulator, $H(s)$ is calculated to have a delay around the loop of either zero or an integer multiple of the clock cycle. Using this approach, the unavoidable parasitic loop delays must be dealt with separately [19]. However, in order to correctly calculate the fractional delay $H(s)$, the time delay required by the filter should be set to the loop delay value; this results in the proper synthesis of both the NTF and STF. The same analytical model enables the calculation of the center frequency within the range f_s/n, where n is now a positive real number instead of an integer. The last two statements outline the main features of the design methodology presented in this chapter.

As stated in Chapter 3, the numerator and denominator coefficients in (3.29) have too many significant digits; therefore, they can not be implemented with absolute accuracy. The numerator coefficients determine the position of the of zeros in (3.29); they will have little influence on the notch location, as long as the overall loop is still stable. Conversely, the denominator coefficients have to be implemented with relatively high accuracy, in order to preserve the notch location and high SNR. Simulation results for the SNR sensitivity versus the numerator coefficients for (3.29) are shown in Fig. 5.2. The figure indicates that if the SNR loss is to be held at less than approximately $6\,dB$, then the required accuracy of the coefficients should be greater than $\pm 0.25\%$. A further implication is that a relatively high

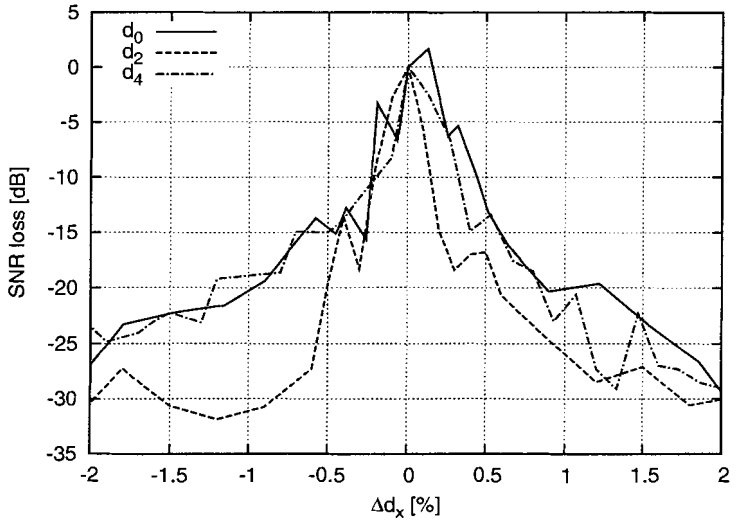


Figure 5.2: Numerator coefficient sensitivity.

Coefficient	Value	Coefficient	Value
H_{03}	-4.1416e+09	d_4	1.0000e+00
H_{02}	1.7042e+19	d_3	0.0000e+00
H_{01}	-8.4547e+28	d_2	7.8957e+19
H_{00}	1.1689e+39	d_1	0.0000e+00
		d_0	1.5585e+39

Table 5.1: Ideal coefficients for the $f_s/4$ CT $f\Sigma\Delta$ modulator configuration.

Q is required to implement the resonator $H(s)$. There are several rules of thumb used to determine the minimum Q requirement, which claim that $Q \geq 60$ [48] or $Q \geq 100$ [33]. We will return to this topic in the discussion of experimental results.

Using (3.29), numerous different CT BP $f\Sigma\Delta$ transfer functions could be found for various center tuning frequencies. For example, letting $\theta = \pi/2$ (i.e. $f_s/4$), $f_s = 1/T = 4\,GHz$ and $\delta = 0$, a set of coefficients is obtained that corresponds to a zero delay $f_s/4$ $\Sigma\Delta$ modulator, with no pole splitting (Table 5.1).

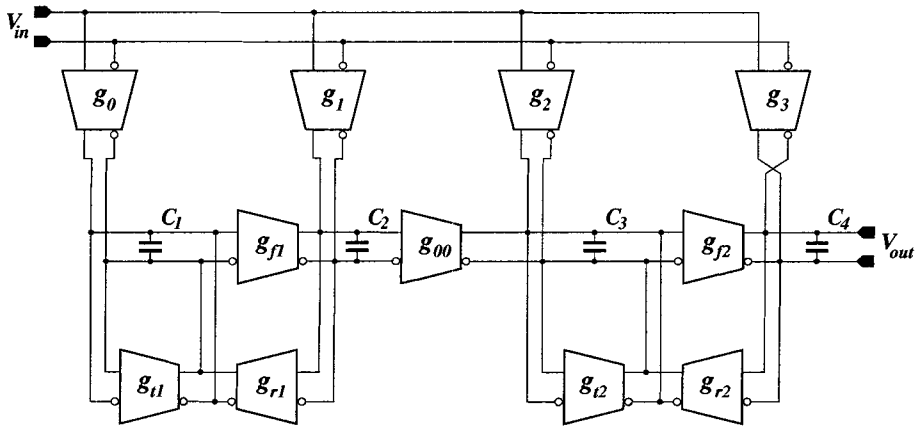


Figure 5.3: Block diagram of a 4^{th} order g_m–C resonator.

5.2 Gm–C resonator

The set of coefficients from Table 5.1 must be further mapped into the final resonator architecture. A discussion of several practical architectures, whose transfer functions have a one–to–one mapping corresponding to (3.29), is given in [48].

In this work, the g_m–C biquad resonator based architecture shown in Fig. 5.3 was used (each of the g_m blocks is tuned with its own biasing current; not shown for simplicity). There are two resonators built around $g_{r1}, g_{f_1}, C_1, C_2$ and $g_{r2}, g_{f_2}, C_3, C_4$ structures. Circuit blocks g_{t1} and g_{t2} are required to fine tune the rather poor Q–factor of g_m–C based resonators. The numerator coefficients $H_i, (i = 01, \ldots, 03)$ from Table 5.1 are implemented through $g_0, \ldots, g_3$. Finally, the g_{00} block is used to satisfy the one–to–one mapping requirement.

The transfer function of the resonator in Fig. 5.3 is

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{\frac{g_3}{C_4}s^3 + \frac{g_2 g_{f2}}{C_3 C_4}s^2 + \left(\frac{g_1 g_{00} g_{f2}}{C_2 C_3 C_4} + \frac{g_3 g_{f1} g_{r1}}{C_1 C_2 C_4}\right)s + \frac{g_0 g_{f1} g_{00} g_{f2} + g_2 g_{f1} g_{f2} g_{r1}}{C_1 C_2 C_3 C_4}}{\left(s^2 + \frac{g_{f1} g_{r1}}{C_1 C_2}\right)\left(s^2 + \frac{g_{f2} g_{r2}}{C_3 C_4}\right)} \tag{5.1}$$

The ideal coefficients from Table 5.1 are mapped into g_m values by equating the numerator and denominator coefficients in (3.29), with their respective counterparts in (5.1), where $C = C_1 = C_2 = C_3 = C_4 = 26pF$. Ideal values for a g_m–C configuration of the resonator are shown in Table 5.2. (For detailed derivation of (5.1) see Appendix A.)

Depending upon the θ, T and δ values used in (3.29), the g_m values in Table 5.2 can map onto either positive or negative numbers or zero. From an implementation perspective, this forces the designer to make some practical choices. Firstly, a g_m circuit capable of

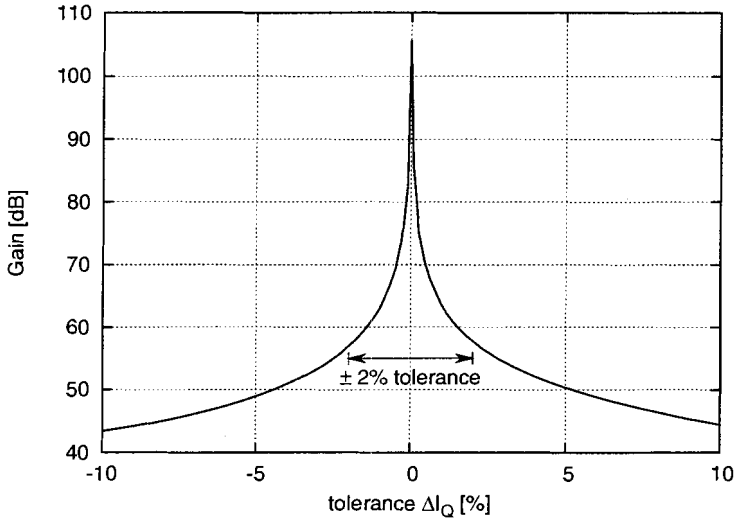


Figure 5.4: A Q–enhancement sensitivity plot.

g_m	[mS]	g_m	[mS]	g_m	[mS]
g_3	-107.6814	g_{f1}	163.3628	g_{00}	163.3628
g_2	70.5221	g_{r1}	163.3628	g_{t1}	163.3628
g_1	52.0000	g_{f2}	163.3628	g_{t2}	163.3628
g_0	52.0000	g_{r2}	163.3628		

Table 5.2: g_m–C coefficients for the $f_s/4$ CT $f\Sigma\Delta$ modulator configuration.

implementing both positive and negative g_m values requires approximately double the area and power consumption when compared to a g_m circuit capable of implementing only single polarity g_m values. Furthermore, the number of current biasing lines required for the g_m blocks doubles, resulting in a complexity increase in the control circuitry used to program the g_m values. Secondly, the use of the unipolar input g_m stages simplifies the resonator design; however, this is at the cost of a reduced programming range that can be implemented, when compared to the resonator built out of bipolar input g_m stages. As shown in the schematic of Fig. 5.3, unipolar input g_m stages were used in this work. As a result, the negative value required for the g_3 stage was implemented by twisting the g_3 differential output lines.

Another important design parameter is the dependence of the Q–factor on the correct biasing current value for g_{t1} and g_{t2}, Fig. 5.4. Simulation results indicated that the control current of the tuning g_m stages had to be close to $\pm 2\%$ tolerance of its nominal value, to

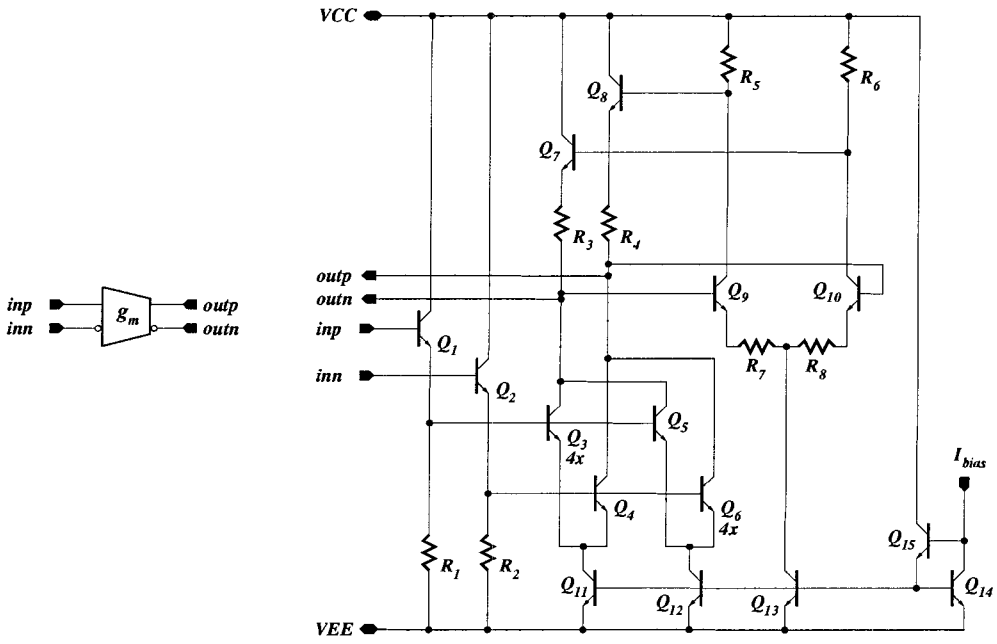


Figure 5.5: Symbol and schematic for the g_m circuit.

maintain a gain requirement of $> 60\,dB$. We will return to this issue when discussing the experimental results in Chapter 6.

5.3 Design of the g_m stage

The schematic for the g_m stage used throughout the design is shown in Fig. 5.5. The circuit topology is based on the multi–tanh architecture [17]. Transistors Q_3–Q_4 make first asymmetric differential pair and transistors Q_5–Q_6 make the second. The DC gain transfer functions for the two input stages, together with the overall transfer function, are shown in Fig. 5.6. A size ratio of four was used for the Q_3–Q_4 and Q_5–Q_6 transistor pairs, which created an offset of $\pm 55mV$ relative to the input voltage. Their combined gain was approximately 30% larger than the gain of the two input stages alone. The linear range is now extended relative to the single differential pair; the maximal ripple in the gain function is shown in Fig. 5.7.

The differential input stage consists of two C–E stages Q_1–Q_2. The function of the input stage is twofold: 1) it serves as the signal level shifter; and 2) it increases the input impedance of the g_m stage by effectively creating Darlington configurations when combined

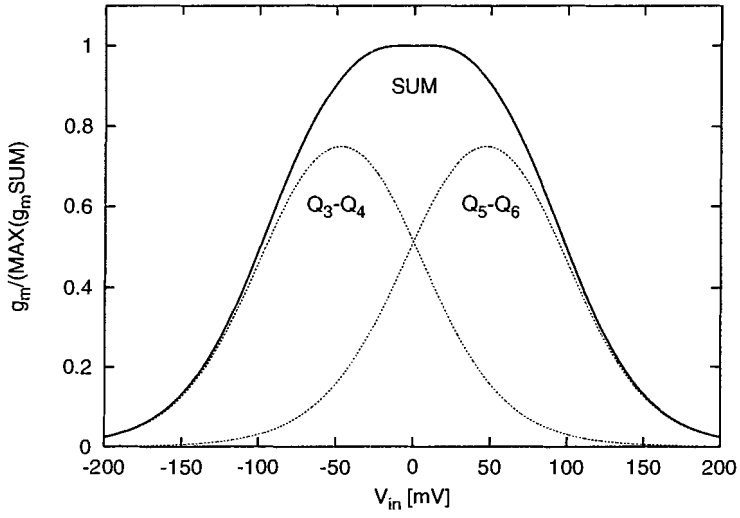


Figure 5.6: The multi–tanh g_m doublet gain function.

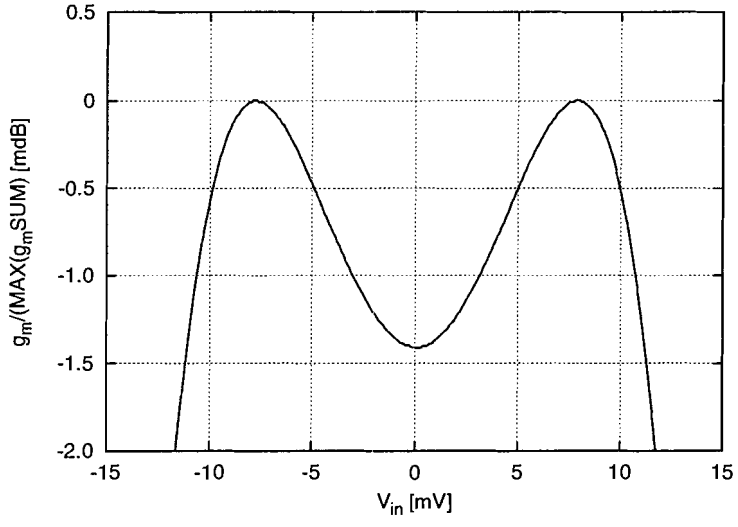


Figure 5.7: The g_m gain ripple.

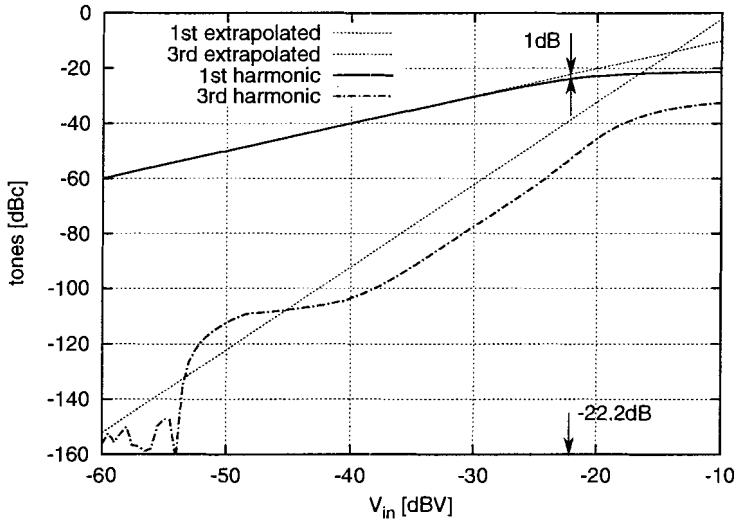


Figure 5.8: The g_m harmonic signature.

with the differential pairs.

Resistors R_3–R_4 present a passive load for the g_m stage, implying that a method is required to increase the output impedance of the g_m stage. In this design, a feedback approach was used: differential pairs Q_7–Q_8 and Q_9–Q_{10}, together with R_6–R_8, create a loop used to keep a constant common mode voltage at the output nodes. This mechanism effectively increases the output impedance of the g_m stage. At the same time, the input and output common mode voltages are matched ($2.4V$ in this case), allowing the g_m stages to be easily cascaded to each other.

The tail currents for the differential pairs are produced by replicating appropriate multiples of the I_{bias} current, within a current mirror consisting of transistors Q_{11}–Q_{15}.

The tunability of the g_m stage is achieved simply by controlling the bias current. The coefficients shown in Table 5.2 are once again mapped; in this case, according to the g_m vs. I_{bias} relationship.

The linearity of the g_m stage can be estimated from the simulated harmonic signature plot shown in Fig. 5.8. The $1\,dB$ compression point was found to be at $V_{in} = -22.2\,dBc$. However, when using the multi–tanh doublet, the IIP3 point is insignificant as it is dependent on the input signal level [17].

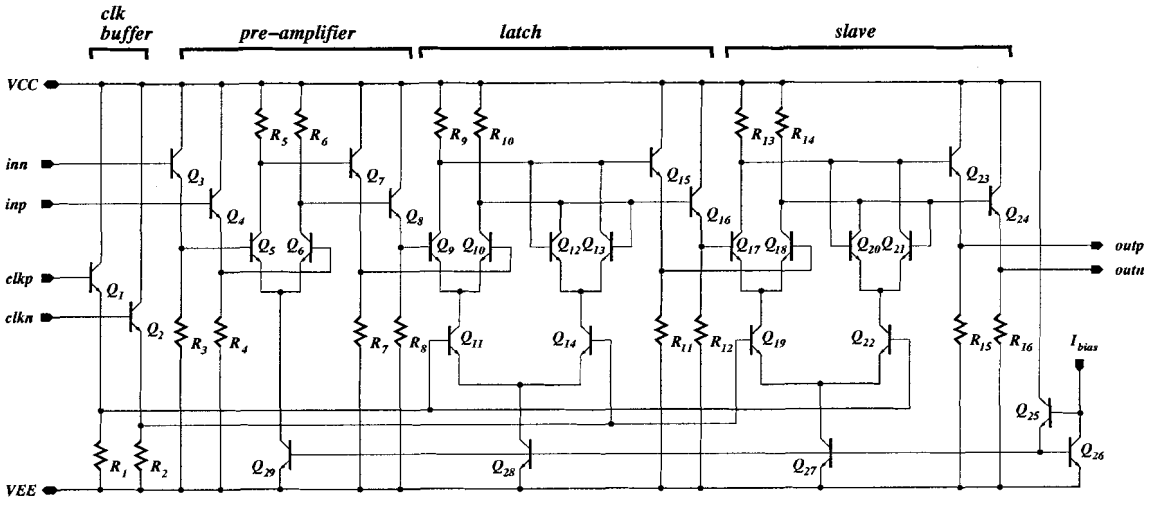


Figure 5.9: A detailed schematic of the NRZ comparator.

5.4 Comparator

A traditional latch–slave configuration for a high–speed comparator [21] is shown in Fig. 5.9. In accordance with the requirements of (3.29) transfer function, the NRZ pulse shape is used.

The signal input stage consists of a differential pre–amplifier, which performs the following three functions: 1) it amplifies weak signals at the loop filter output; 2) it shifts the common mode voltage; and 3) it buffers possible kick–back signals, which are reflected back from subsequent latch and slave stages. The input buffer stage consists of the common–collector voltage buffers Q_3 and Q_4, along with the passive loads R_3 and R_4. Similar buffering stages are inserted between the pre–amplifier and the latch, between the latch and slave stages, and at the output of the comparator. At the input stage, common–collector voltage buffers Q_1–Q_2 and passive load R_1–R_2 are used for the differential clock signal. Differential pairs Q_{11}–Q_{14} and Q_{19}–Q_{22} serve as the current switching elements for the latch and slave stages, respectively. Biasing currents for the differential pairs are provided by the current mirror, which consists of transistors Q_{25}–Q_{29}.

This circuit was simulated with clock frequencies of up to $5\,GHz$. However, the implemented $f\Sigma\Delta$ circuit works at much lower speeds, which greatly relaxes the design margins of the implemented comparator circuit.

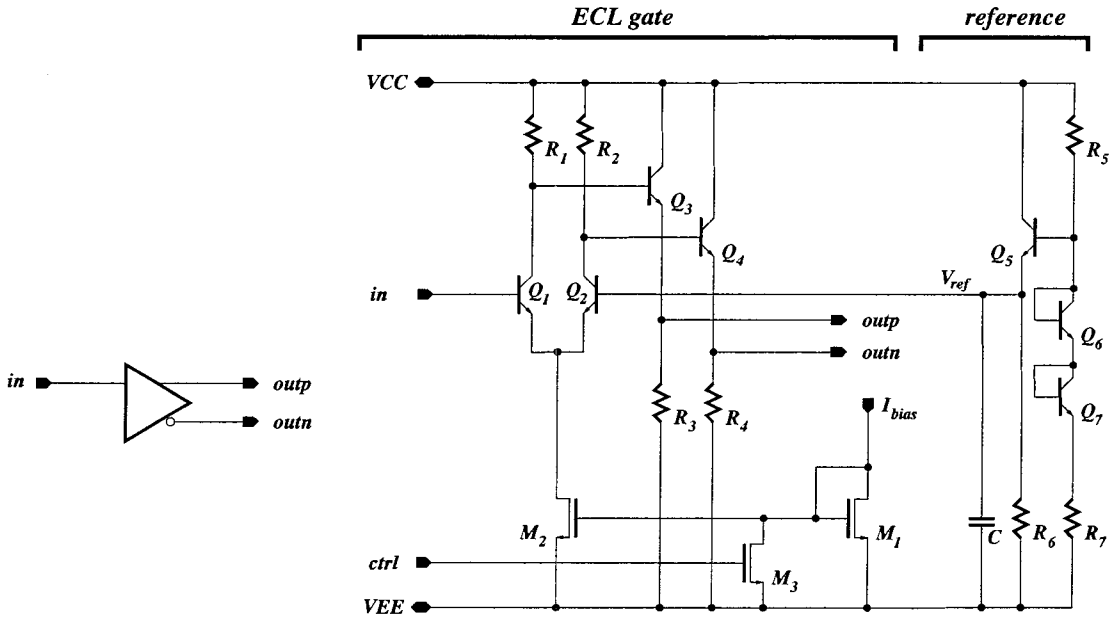


Figure 5.10: Symbol and schematic for the ECL based delay line segment with voltage reference generator.

5.5 Delay line

The suggested general architecture shown in Fig. 5.1 implies that a programmable delay line could be used instead of a traditional DAC circuit. Sampled DAC circuits are traditionally used in the feedback loop in order to accommodate integer clock delay values for the loop delay. However, analytical results presented in Chapter 3 effectively removed the integer clock delay requirement. Thus, a variety of fractional loop delay times can be incorporated into the loop filter design. The minimal loop delay that can be used will be determined by the parasitic and propagation delays encountered inside the loop, relative to the sampling clock edge. Therefore, there are at least two options available to the designer. First, the loop filter could be designed to accommodate for the parasitic and propagation delays only; the delay line would be set to zero delay or omitted completely. Second, if required, any combination of delay times (parasitic, propagation or delay line) could be incorporated in the loop filter design.

Implementing an analog delay line is somewhat more difficult than implementing a digital delay line. One possible analog design method assumes that the tuning range boundaries are not necessarily fixed, provided that they are wide enough to meet the given requirements. In

other words, the boundaries are allowed to fluctuate with the process variations, as long as the *minimal tuning steps* are matched. Generally, this matching is achieved by replicating the same cell layout for the delay segment blocks.

The single delay segment, shown in Fig. 5.10, is based on an ECL gate structure. The core of the circuit consists of the differential pair Q_1–Q_2 and passive loads R_1–R_2, followed by the output voltage buffer Q_3–Q_4 and their respective passive loads R_3–R_4. In the same schematic, a typical voltage reference used in ECL gate structures is shown [10]. In order to save space and DC power consumption, the voltage reference is usually shared by up to four ECL gates. Depending on the technology used, the propagation time of this circuit can be set to be within the 5–20ps range. If the same cell layout is replicated throughout the design, an excellent matching of the propagation times is achieved.

In order to apply the structure in Fig. 5.10 to a programmable delay line design, a current switch is implemented consisting of a M_1–M_2 current mirror and M_3. A high voltage level at the *ctrl* input node turns on the M_3 transistor and shorts the gate node of the current mirror to the ground; this effectively turns off the differential pair tail current. A practical architecture for the delay line in Fig. 5.11 is created by implementing an $(n-1) \times n$ matrix of delay elements, followed by an ECL based NOR gate and the final delay element. For the sake of simplicity, the control lines are not shown. By turning the upper row delay elements ON and OFF, thereby redirecting the signal to the lower row, the length of the delay line can be controlled. The signal always terminates at the input of the NOR gate. This architecture has a tuning range from $(n+1)t_d$ to $2n\,t_d$, where t_d is a single cell delay.

5.6 Summing circuit

The last sub–block of the architecture in Fig. 5.1 is the summing block, comprised of three g_m stages (Fig. 5.12). The use of identical g_m stages throughout the design makes the overall design and layout simpler, while also providing for better matching between the g_m values.

5.7 Post–layout simulation

With the transistor level design of the $f\Sigma\Delta$ modulator finished and the final layout completed, the last stage of the design process was to perform a post–layout simulation. A

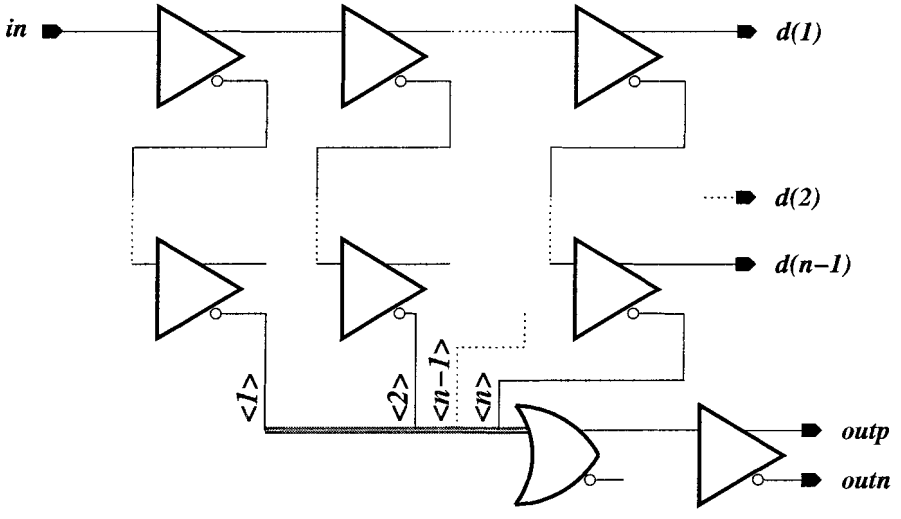


Figure 5.11: Programmable delay line schematic.

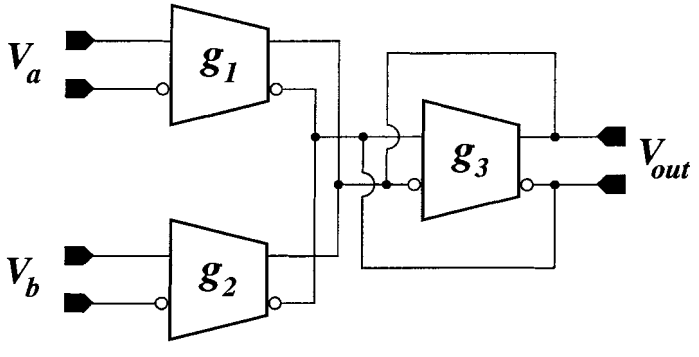


Figure 5.12: Voltage summing circuit schematic.

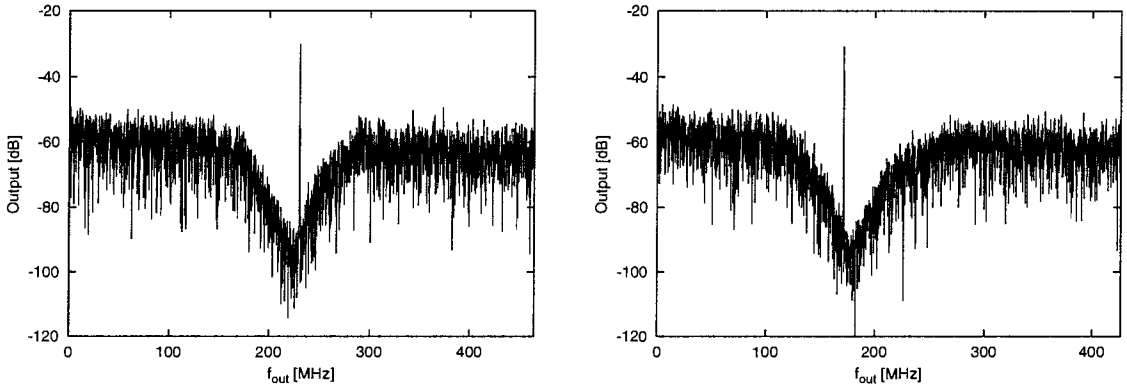


Figure 5.13: Simulated post–layout $f\Sigma\Delta$ response, using 8192 clock cycles and an FFT of 65536, for: (left) an $f_s/4$ configuration; and (right) an $f_s/5$ configuration.

mapping process is required to map the g_m coefficients listed in Table 5.2 into the actual biasing currents required by the transistor level g_m blocks; a detailed description will be given in Chapter 6. The results of the post–layout simulations for two different tuning positions, $f_s/4$ and $f_s/5$ configurations, are shown in Fig. 5.13; further descriptions will be given in Chapter 6. Fig. 5.13 was the last verification point prior to beginning chip manufacturing.

5.8 Summary

A practical implementation of the theoretical models discussed in Chapter 3 has been presented. Transistor level schematics of all sub–blocks are shown. In the following chapters, experimental results for the implemented modulator are shown.

Chapter 6

Prototype chip testing

In the previous chapters, analytical models and design details of the CT BP $f\Sigma\Delta$ modulator were introduced. This chapter describes the prototype SiGe chip, the details of the test procedure and the measured results confirming the validity of the proposed methodology.

6.1 Chip description

The test chip was manufactured in $0.5\mu m/f_T = 47\,GHz$ SiGe technology, with five packaged parts and 35 dice received. A microphotograph of the chip is shown in Fig. 6.1. The total size of the layout, including the bonding pads and on–chip test VCO circuit, is $2.3mm \times 2.3mm$. The chip was bonded to an HF 80–pin ceramic package and soldered onto a test board. An operating frequency range of up to $4.8\,GHz$ was specified for the package and test board combination.

The overall design assumed a 50Ω environment; therefore, all on–board HF differential lines were laid out as 50Ω microstrip transmission lines. Subsequently, the input signal and clock lines were terminated with on–chip 50Ω resistors, while the output pad drivers were designed to drive the same load. Due to space limitations, this version of the chip does not have a programmable delay line within the $f\Sigma\Delta$ feedback loop (Fig. 6.2); thus, the loop filter function should only be programmed to compensate for parasitic loop delay times. The signal and clock lines are fully differential throughout the design and 20 control lines carrying DC currents are provided for the chip control. The tuning and control of the $f\Sigma\Delta$ requires 16 DC currents, while the on–chip test VCO requires 4 DC currents. Neither voltage nor current references were implemented on–chip, which implies that the biasing voltages

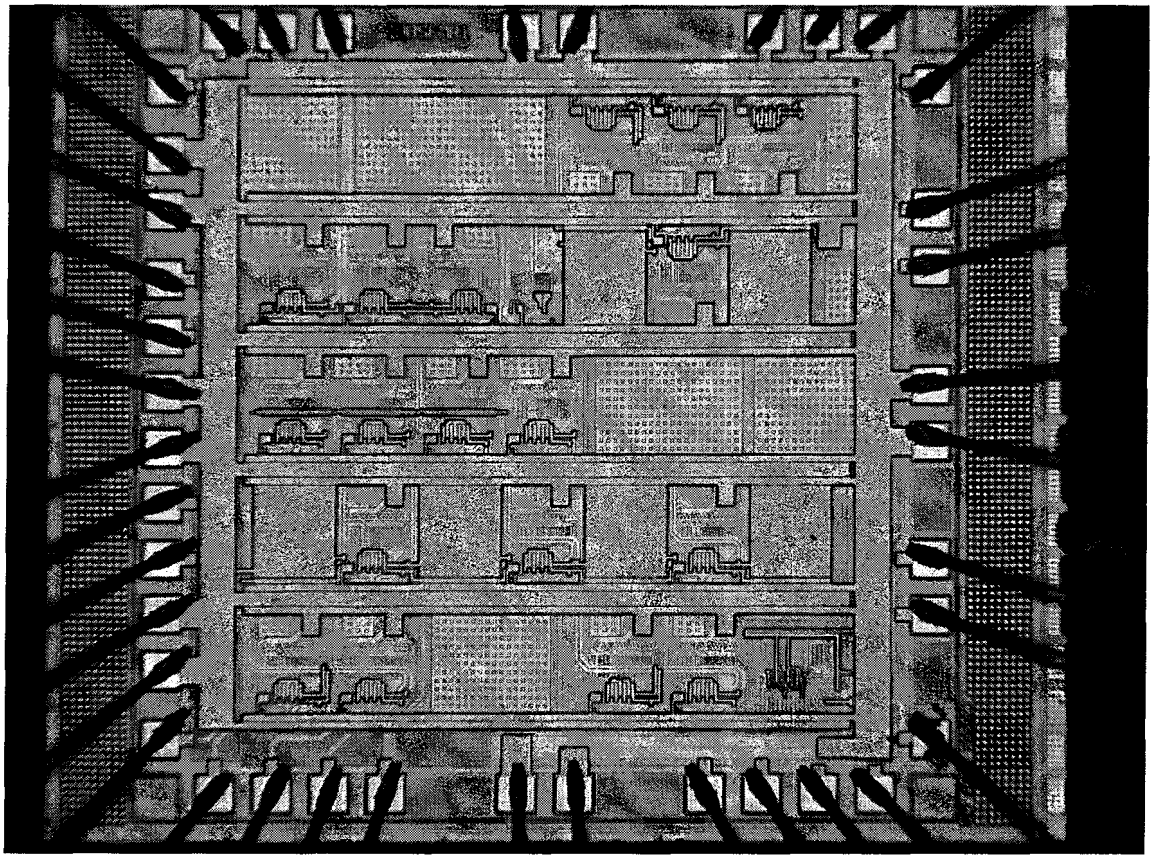


Figure 6.1: Microphotograph of the $f\Sigma\Delta$ chip.

and currents required by the chip must be delivered by off–chip sources. The power supply lines used 6 bonding pads for ground and 4 bonding pads for the positive rail.

6.2 Test setup

The development of a a successful and efficient testing strategy for a mixed–signal design is a non–trivial task. Modern testing setups are very complex and sophisticated [4]; therefore, planning for successful testing is an important aspect for mixed–signal chip design. The test setup used in this research consisted of: a signal generator, a clock generator, a spectrum analyzer, a PCI bus compatible 16–channel DAC which generated the DC control currents (range $0mA$ to $+20mA$), two power supplies (one for DC power and one for signal biasing), two 180° phase splitters (one for the input signal and one for the clock signal), and two

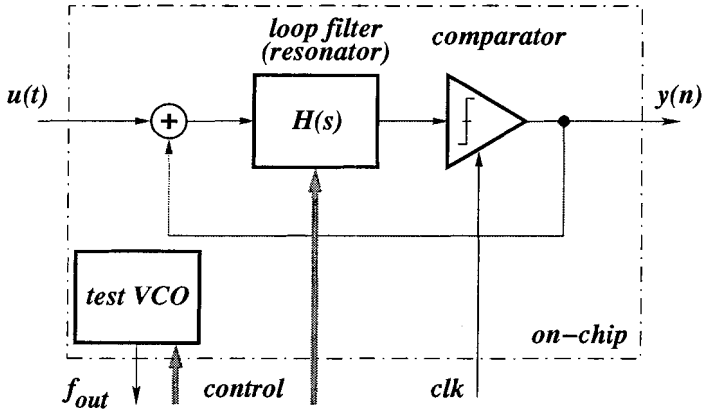


Figure 6.2: Block diagram of the implemented version of the $f\Sigma\Delta$ chip.

pairs of bias–T circuits; refer to Fig. 6.3. Optionally, an HF sampling storage oscilloscope was required to capture time–domain pulse streams.

Typically, standard signal generators create single–ended signals, which means that phase splitter circuits must be used to create the appropriate differential signal required by the chip. In addition, DC biasing of the signal is provided by means of a DC source and a pair of bias–T circuits. This configuration is preferable for an experimental chip as it provides more flexibility and lower design risk. Alternatively, one could design an on–chip single–ended to differential converter, with on–chip biasing references.

6.3 Experimental results

As the chip is essentially a continuous time filter design, a method of estimating the process variations is required. In order to establish correlation between the simulation results and the measurement results, a number of different methods have been used within both industry and academia. The approach used in this research, to find a mapping between the theoretical coefficients and the control currents, relied on a simple g_m–C based VCO, which was implemented on–chip by using replicas of the g_m and capacitor layouts used to create the $f\Sigma\Delta$ modulator. In the initial VCO test, the same conditions were used for both simulation and measurement. The comparative plot given in Fig. 6.4 shows the relatively good agreement between the two results, indicating that the current wafer batch is close to

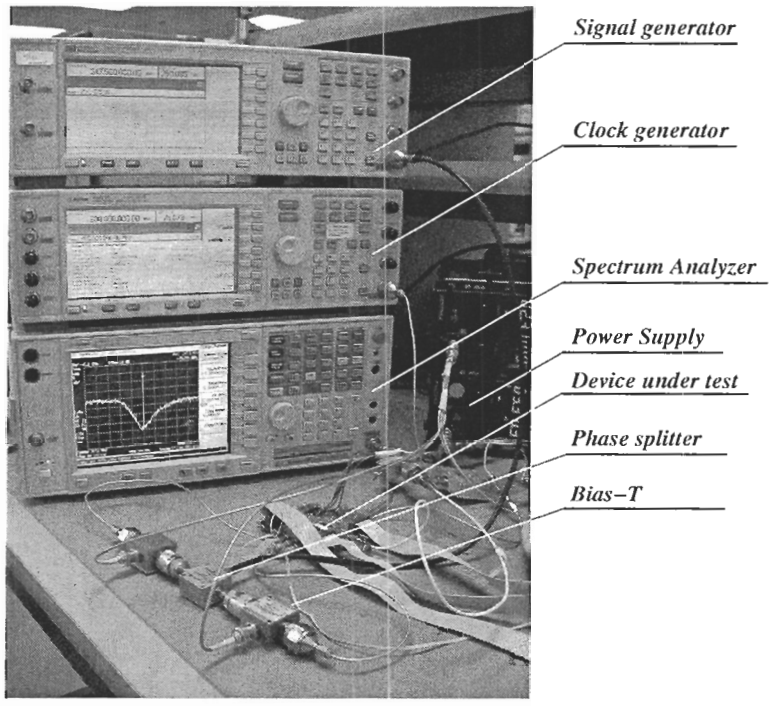


Figure 6.3: Photograph of the test bench.

the typical case.

Since the capacitor values used in both the VCO and $f\Sigma\Delta$ are identical, the output frequency values f_{out} in Fig. 6.4 can be easily converted into the g_m/C ratios from (5.1), as the VCO output frequency is $\omega_{out} = 2\,\pi\,f_{out} = g_m/C$. Therefore, Fig. 6.4 provided the means to determine the biasing current I_{bias} required to achieve the g_m/C ratios in (5.1), which were calculated from the analytical model (3.29). It should be noted that the output frequency f_{out} corresponds to the frequency location of the notch in the NTF function and consequently, the location of the input signal.

The control currents (i.e. biasing currents), obtained using the aforementioned procedure, yielded an NTF which was very close to a correct $f\Sigma\Delta$ frequency plot. There are two main sources for the discrepancies: 1) the resonator structure in Fig. 5.3 does not include any "dummy" g_m blocks, which should be used to match the internal impedances of the resonator [30]; and 2) the biasing current values required for the Q–enhancement g_m blocks do not come from the analytical model; they must be determined experimentally.

Once the mapping procedure for the control currents is established, the biasing currents

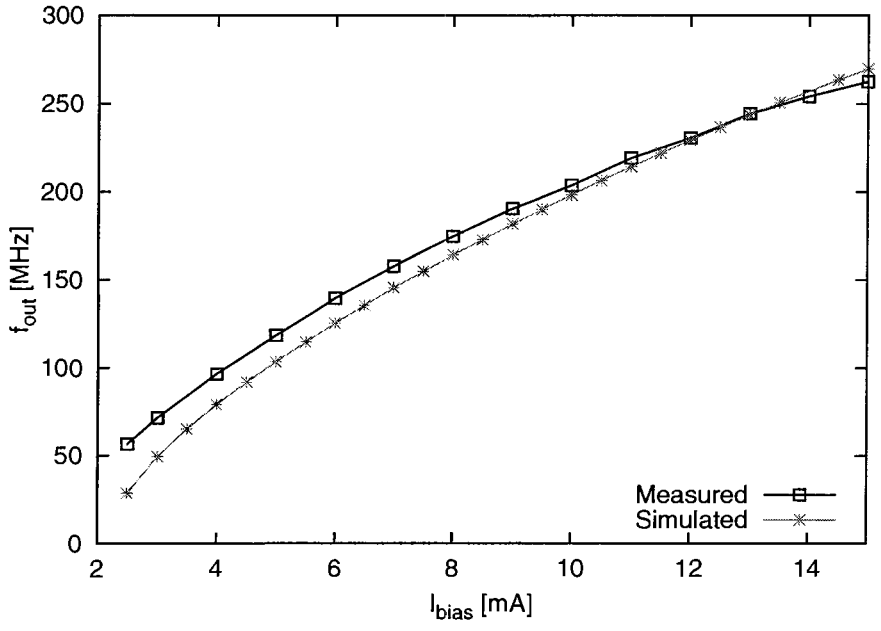


Figure 6.4: A comparison of measured and simulated control currents for the internal resonator.

must then be recalculated for various signals, sampling frequencies, f_s/n and delays, using (3.32) to (3.34) and Fig. 6.4. It should be noted that for practical implementation of this chip, not all tuning positions predicted by the analytical model may be achieved. In order to realize the full uninterrupted wide tuning range, the practical implementation would require both positive and negative g_m values; this implies a more complicated structure than illustrated in Fig. 5.5. For example, in this design, both the positive and negative g_m values calculated in Table 5.2 were hardwired; this limited the $f\Sigma\Delta$ tuning range to the cases exhibiting the same combination of positive and negative g_m values. Furthermore, the control currents would also need to be outside of the PCI DAC card's available range. For the purposes of this experimental prototype chip, satisfying the full theoretical range becomes impractical. Although the currently implemented resonator can be tuned to a much wider frequency range, in order to have the overall $f\Sigma\Delta$ tuned to the same range, some of the control current values (used to control the numerator coefficients in (5.1)) would have to be larger then $20mA$. Thus, the specification list in Table 6.1 includes both achieved tunability range of the $f\Sigma\Delta$, as well as the resonator by itself.

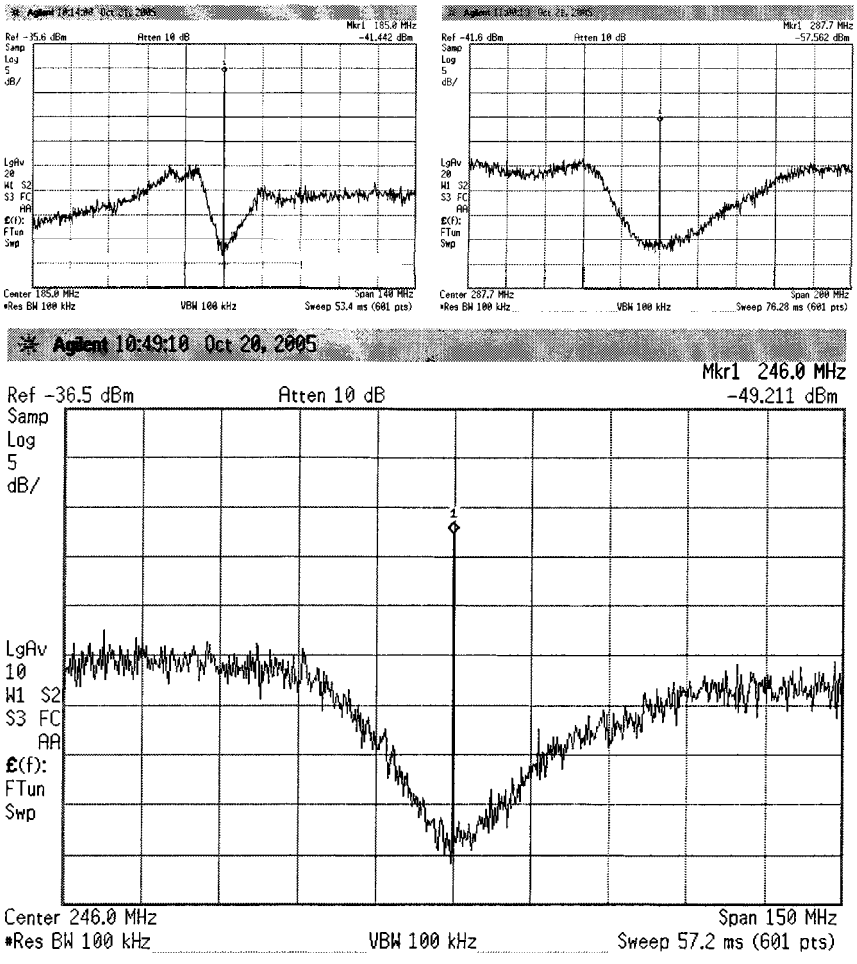


Figure 6.5: Measured frequency response for three signal frequencies within the tuning range: (top left) 185 MHz; (top right) 287.7 MHz; and (bottom) 246 MHz.

The experimental results shown in Fig. 6.5 demonstrate the operation of the $f\Sigma\Delta$ modulator, for three signal frequencies within the maximal tuning range of 185 MHz to 289 MHz. The graphs show that correctly tuning the NTF functions at the outskirts of the tuning range becomes more difficult, due to the reasons previously mentioned.

The theoretical calculation for a sampling frequency $f_s = 800\,MHz$ and $n = 3$ (i.e $f_{in} = 266.67\,MHz$) yields the following values for the control currents, required to set zeros in the transfer function (5.1): $I_{g_3} = 4.921mA$, $I_{g_2} = 10.030mA$, $I_{g_1} = 1.911mA$, and $I_{g_0} = 0.117mA$. The control current required to set the resonant frequency (i.e. coefficients in denumerator of (5.1)) was calculated to be $I_{bias} = 15.440mA$ for g_{f1}, g_{r1}, g_{00}, g_{f2} and g_{r2}.

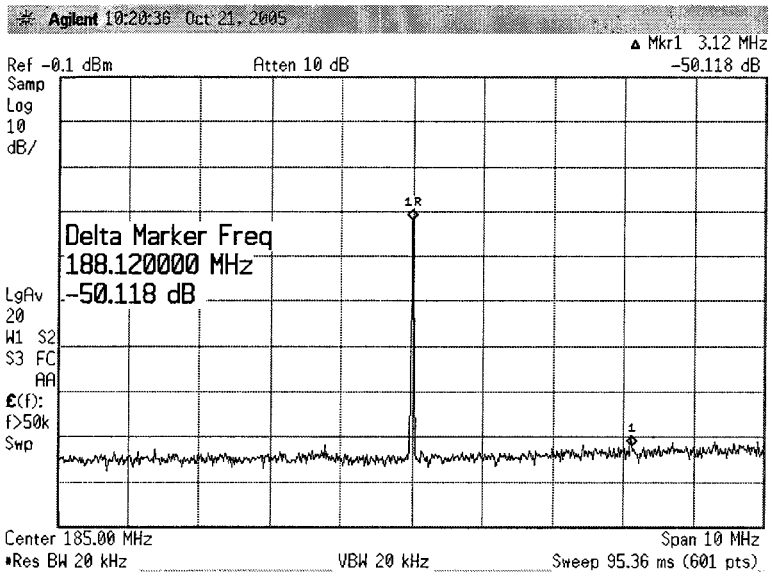


Figure 6.6: Measured maximal SNR.

After providing the biasing currents $I_{qt1} = 5.450mA$ and $I_{qt2} = 8.470mA$ to the respective Q–enhancement g_m blocks inside the resonator, the NTF notch formed at 246 MHz; refer to the bottom figure of Fig. 6.5. The application of the delayed versions to the $f\Sigma\Delta$ transfer function revealed that the parasitic loop delay was less than $0.1\,T$ at the given sampling frequency.

A comparison of the bottom plot in Fig. 6.5 with a similar plot in Fig. 5.13 shows that the Q factor of the resonator is lower than predicted by the post–layout simulations. The expected notch depth was approximately $35\,dB$, while the measured notch was close to $20\,dB$. There are several possible causes for this behavior; for example, the presence of noise inside the chip substrate, non–perfect single–ended to differential conversion in the 180° power splitter (causing common–mode noise and timing jitter), and jitter injected by the test equipment and setup. However, this issue is not pursued further in this research.

The maximal SNR and dynamic range (DR) are two very important characteristics of a $\Sigma\Delta$ modulator. Figure 6.6 shows one of the measured SNR values to be at approximately $50\,dB$ (within resolution $BW = 20\,kHz$). Reducing the input signal to very small values eventually leads to measurements of the minimal input signal amplitude, which is needed to determine the DR; this occurs at the moment when the input signal level becomes equal to the noise–power level. Note that at the bottom of the notch, the noise floor is not flat but

Table 6.1: Measured specifications for the $f\Sigma\Delta$.

technology	BiCMOS $0.5\mu m$ SiGe $f_T = 47\,GHz$
total die size	$2.3mm \times 2.3mm$
power supply	$3.3V \pm 10\%$
power consumption	$1.0/1.2W$ (DC total)
output HF power	$40mW$
operational bandwidth	$20\,MHz$
sampling frequency	$f_s = 0.6/1.2\,GHz$
maximal SNR $(resBW{=}20\,kHz)$	$50\,dB$
maximal DR	$47dB$
$f\Sigma\Delta$ tunability range	$185\,MHz$ to $289\,MHz$
resonator range	$60\,MHz$ to $295\,MHz$

slightly concave; thus, the minimal signal that is still above the noise level is approximately $3\,dB$ within the operational $BW = 20\,MHz$, which means that the maximal $DR \approx 47\,dB$. A summary of the measured results is given in Table 6.1.

6.4 Summary

Test results for the prototype CT BP $f\Sigma\Delta$ modulator, designed to demonstrate the design methodology, have been presented. The initial results confirmed the validity of the theoretical approach. At the same time, the design is comparable to the other published designs, as shown in Fig. 1.1.

Chapter 7

CT BP $f\Sigma\Delta$ Applications

In this chapter a couple of possible applications for tunable CT BP $f\Sigma\Delta$ modulators are proposed. First, a new architecture for IF to RF conversion is presented. The architecture is based on a tunable CT BP $f\Sigma\Delta$ modulator in combination with Manchester coder and decoder [53]. Second, a combination of a power amplifier (PA) and CT BP $f\Sigma\Delta$ modulator in either open or closed loop configuration is presented. The ability to accomodate for the PA propagation delay during the loop filter design phase, and therefore include the PA inside the loop, opens possibility for further integration of a transmitting path [28].

7.1 A Fractional Delay $\Sigma\Delta$ Upconverter

A software–defined radio is one of the most active research areas in modern circuit design. Specifically, an efficient way to continuously program the input/output RF converter needs to be developed. A number of researches have found that a pulse–width modulated (PWM) signal has potential for efficient RF transmission [38]. More recently, $\Sigma\Delta$ modulators were used for supporting both down–conversion of an RF signal [54] and upconversion [31, 26] of an IF signal.

However, there are still several unsolved problems related to application of $\Sigma\Delta$ modulators for an IF signal upconversion.

First, carrier frequencies required by modern communication systems are on the order of multiples of *GHz*. Implication is that the $\Sigma\Delta$ circuits, if used as in the references above, have to be sampled at least twice the signal rate, most often four times. Subsequently, application of the traditional z–domain $\Sigma\Delta$ modulators is severely limited. Continuous time

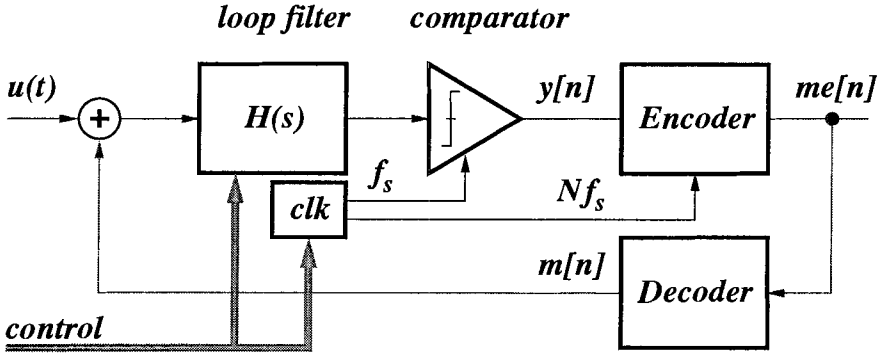


Figure 7.1: Block diagram of a fractional delay ΣΔ upconverter.

class of modulators is somewhat better suited for the task. However, the loop filter has to be implemented either with passive L–C circuits, which is not suitable for IC implementation, or with on–chip low–Q inductors, which necessitates a Q–enhancement circuit. Alternatively, a g_m–C filter implementation can be used with a cost of reduced working frequency and increased nonlinearity.

Second, a ΣΔ modulator by itself is a frequency multiplier which generates predictable images of the input signal. Even though that signal to noise ratios of the images and the input signal are close, the image power levels decline rather quickly.

Third, the loop delay associated with CT ΣΔ modulators presents additional difficulty especially when additional circuit blocks, such as a modulator and power amplifier (PA), are added inside the loop.

Circuit architecture presented in this section addresses all three of the above problems. Further, it demonstrates a potentially big advantage of using tunable CT BP fΣΔ modulators, in combination with an encoding technique, for IF signal upconversion.

7.1.1 Circuit description

In Fig. 7.1 a block diagram of a fractional delay ΣΔ upconverter is shown. A CT BP fΣΔ loop consists of the summing node, CT loop filter $H(s)$ and a one–bit quantizer in a form of a comparator. The *clk* block generates both f_s and Nf_s pulse streams, which are used by the quantizer and the encoder respectively. The first novelty of the circuit is the addition of two alien blocks inside the loop, namely Manchester encoder and decoder. If a PA is included

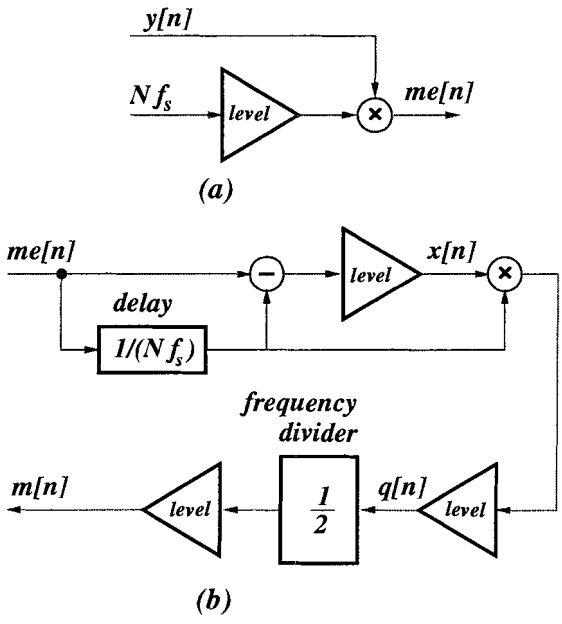


Figure 7.2: A behavioral model of: (a) a Manchester encoder; and (b) a Manchester decoder.

as the last block of the encoder then $me[n]$ signal is ready to enter the antenna interfacing circuit. Second novelty is in application of CT BP $f\Sigma\Delta$ loop filter [50] to compensate for the additional delays introduced by the alien circuits.

A continuous time signal $u(t)$ is converted by the CT BP $f\Sigma\Delta$ part of the upconverter into a NRZ pulse–width modulated signal $y[n]$, which is then upconverted into a RF $me[n]$ signal by the Manchester encoder. The upconverted signal $me[n]$ is decoded before being returned into the $f\Sigma\Delta$ loop again as $m[n]$. Two NRZ pulse trains $y[n]$ and $m[n]$ are identical except for some time delay. Effectively, the alien circuits are "visible" to the $f\Sigma\Delta$ loop only as a fractional time delay, which is compensated for in the loop filter $H(s)$ transfer function. The delay, which is caused by non–zero propagation times of the alien circuits, is a fraction of the sampling period $T = 1/f_s$. Behavioral models of the Manchester encoder and decoder are shown in Fig. 7.2, where the signal notation is taken from Fig. 7.1, *level* is a combination of limiter and level shifting functions, *delay* is half a clock delay element and a standard asynchronous *frequency divider* (factor of two) is used to recreate the NRZ pulse train. The internal time–domain signals of the Manchester encoder/decoder are shown in Fig. 7.3,

The important advantage of architecture in Fig. 7.1 is that the $f\Sigma\Delta$ upconverter allows the loop filter to operate at a much lower variable IF frequency then the RF output frequency.

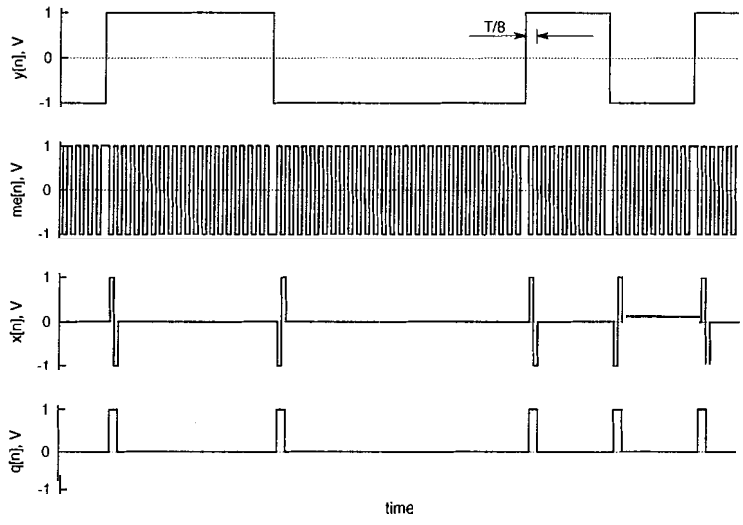


Figure 7.3: Internal time–domain signals of the Manchester encoder and decoder.

This advantage, aside from relaxing the tuning problem, translates into greatly reduced circuit implementation requirements. Also, the $f\Sigma\Delta$ may be tuned so that IF and the half sampling frequency $f_s/2$ are closer, with further reduction in circuit complexity, $f\Sigma\Delta$ loop stability requirements and power. Limiting factor to this approach is the loop stability which must obey the Lee's rule [34].

7.1.2 Simulation results

A mixed–signal simulator, within a standard analog IC design environment, was used to perform verification of the proposed topology. There are a number of possible combinations for the sampling frequency f_s and Nf_s which produce desired RF image of the input signal. Simulated IF frequency of $100\,MHz$ and the sampling frequency used in this example is $f_s = 448\,MHz$ and $N = 5$, shown in Fig. 7.4 from DC to $f_s/2$. Frequency spectrum of upconverted WCDMA RF output signal $y[n]$ is shown in Fig. 7.5 from DC to Nf_s. The small zoom–in window shows frequency spectrum around the $f_{RF} = 2.24\,GHz - 100\,MHz = 2.14\,GHz$. Finally, the time delay of the alien circuits is estimated to be $T/8$ which is accounted for during the design of the $H(s)$ transfer function. The Manchester modulation suppresses the DC component while enhancing the RF signal.

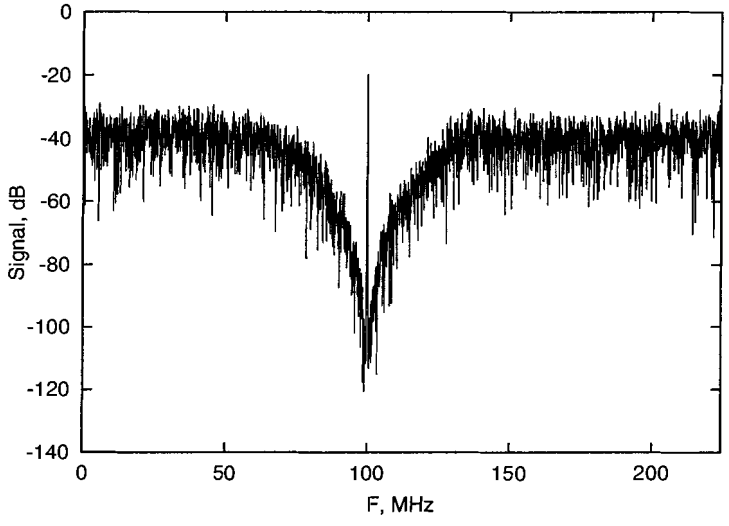


Figure 7.4: A WCDMA 100 *MHz* IF signal, $y[n]$, $m[n]$.

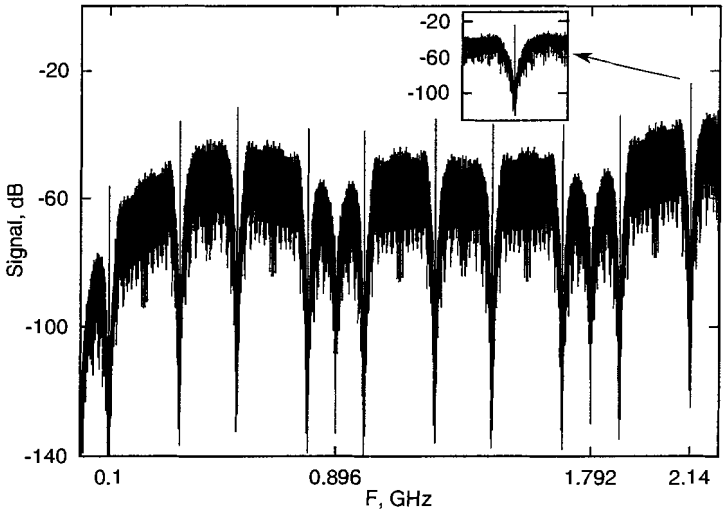


Figure 7.5: A WCDMA 2.14 *GHz* RF signal, $me[n]$.

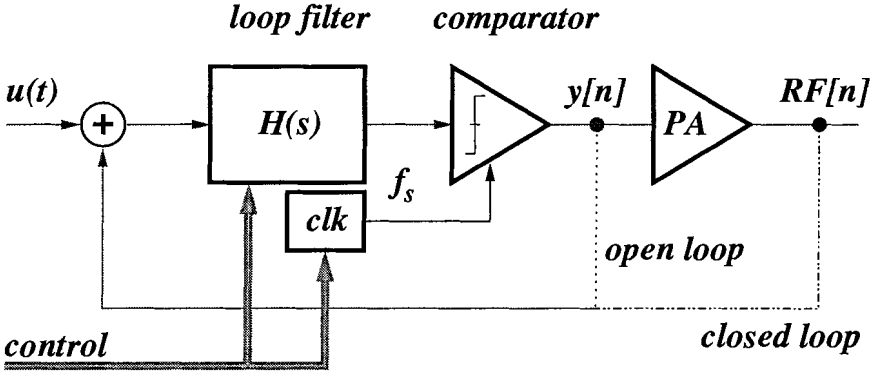


Figure 7.6: Block diagram of a power amplifier with $f\Sigma\Delta$ modulator.

7.2 $f\Sigma\Delta$ based PA

An architecture for power amplification with high power efficiency is presented. Simulation of a class–S amplifier in combination with CT BP $f\Sigma\Delta$ modulator shows power added efficiency (PAE) of 40.1% and $SNR = 60\,dB$ for a two–tone signal spaced at $4.64\,MHz$. A WCDMA signal with peak–to–average ratio (PAR) of $8.7\,dB$ demonstrates $PAE = 16.6\%$ and $SNR = 42\,dB$.

7.2.1 Introduction

Searching for newer and more efficient technologies, researchers are moving from traditional class–AB power amplifier (PA), which used to be the most commonly used type of amplifier for mobile phones, to switched PA in order to achieve higher power efficiencies. A number of researches have found that a pulse–width modulated (PWM) signal has potential for efficient RF transmission [38]. More recently, ΣΔ modulators were used for improving power added efficiency (PAE) of an RF power amplifier [31, 22].

However, in order to create a PWM signal suitable for mobile applications, such as software–defined radio, a tunable version of a BP ΣΔ modulator is needed. Further, the ΣΔ modulator is required to operate in RF range, which imposes very high design challenges. Viable solutions to these two requirements, based on CT BP $f\Sigma\Delta$ modulators, have been shown in [50, 53].

In this section we show a power amplification architecture which demonstrates potential

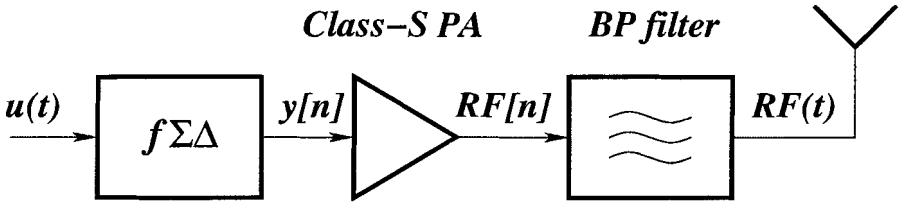


Figure 7.7: Block diagram of a fractional ΣΔ class-S PA.

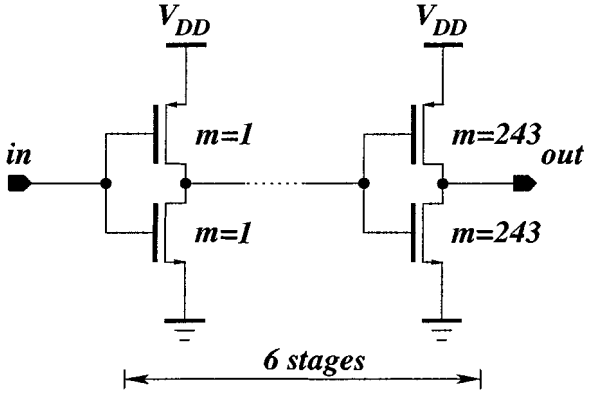


Figure 7.8: Class–S PA schematic.

of achieving high PAE in hand–held transmitters. A working version of CT BP $f\Sigma\Delta$ modulator, which may include encoding upconverter [5], is used with a CMOS class–S PA designed in $0.5\mu m/f_T = 47\,GHz$ BiCMOS SiGe technology, Fig. 7.6.

7.2.2 Circuit description

In Fig. 7.7 we show a block diagram of a fractional ΣΔ class–S amplifier. Depending upon the frequency range of operation an encoding upconverter [5] can be added as the output stage of the modulator. A continuous time signal $u(t)$ is converted by the CT BP $f\Sigma\Delta$ modulator into a NRZ PWM signal $y[n]$, which is then used to drive class–S PA. Out of band switching noise is removed with the BP filter so that $RF(t)$ signal is created and delivered into the antenna.

Internal structure of the PA is shown in Fig. 7.8. Each of the six stages is built as an inverter, where both PMOS and NMOS transistors in the first stage have scaling factor

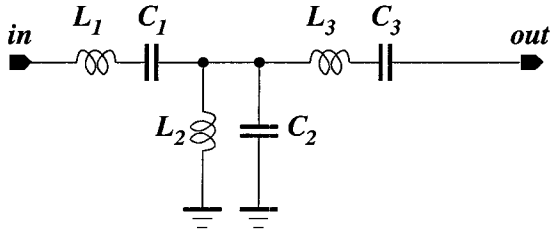


Figure 7.9: Bandpass filter schematic.

L_3	$31.83nH$	C_3	$24.29pF$
L_2	$48.58pH$	C_2	$15.92nF$
L_1	$31.83nH$	C_1	$24.29pF$

Table 7.1: Component values for a bandpass filter, with $f_0 = 181\,MHz$, $BW = 10\,MHz$.

$m = 1$, each subsequent stage has a three times larger scaling factor, with the sixth stage transistors having $m = 243$. In the given technology the achieved PA bandwidth is $BW = 1\,GHz$ and output impedance is $R_{out} = 2\Omega$. With power supply voltage $V_{DD} = 3.3V$ consumed DC power is $PWR_{DC} = 1.059W$.

Maximally flat third order LC filter, Fig. 7.9, is used to remove out of band switching noise. For compatibility with WCDMA signal, the filter bandwidth is set to $BW = 10\,MHz$. Calculated component values for center frequency $f_0 = 181\,MHz$ and input/output impedance of $R_0 = 2\Omega$ are listed in Table 7.1.

7.2.3 Simulation results

A mixed–signal simulator, within a standard analog IC design environment, was used to perform verification of the proposed topology. For purposes of this experiment, the CT BP $f\Sigma\Delta$ modulator is sampled with sampling frequency $f_s = 800\,MHz$ and noise transfer function (NTF) notch was set at $181\,MHz$, i.e. $f_s/4.42$. First, two-tone test is performed with two signals centered around $f_0 = 181\,MHz$ with separation of $\pm 2.32\,MHz$ from the center. Simulated spectrum of a two–tone signal at the PA output is shown in Fig. 4 over bandwidth of $20\,MHz$.

This configuration achieved $SNR = 60\,dB$ within $BW = 10\,MHz$, where the third–order intermodulation product (IM3) is at $41\,dB$ below the signal level. Power added efficiency is

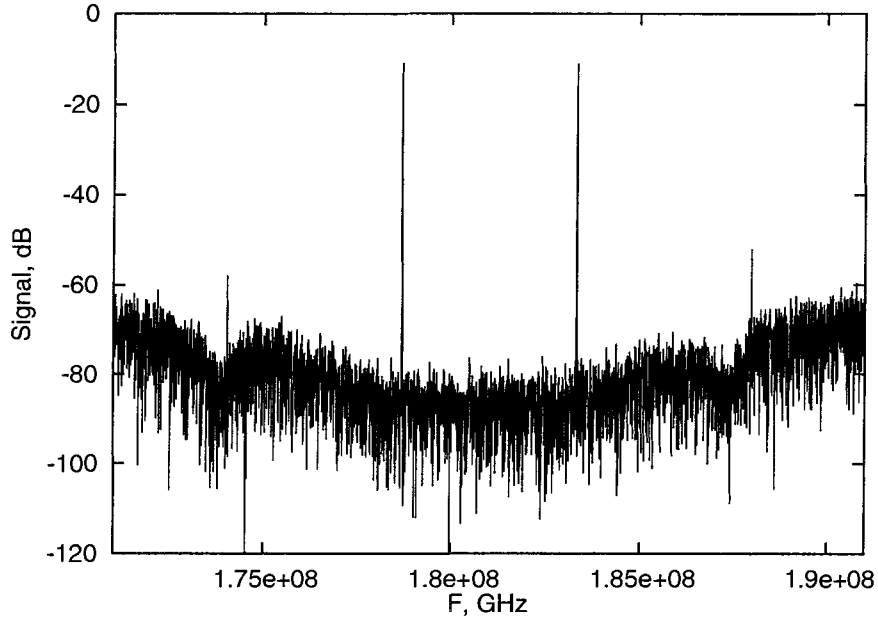


Figure 7.10: Two–tone output of PA.

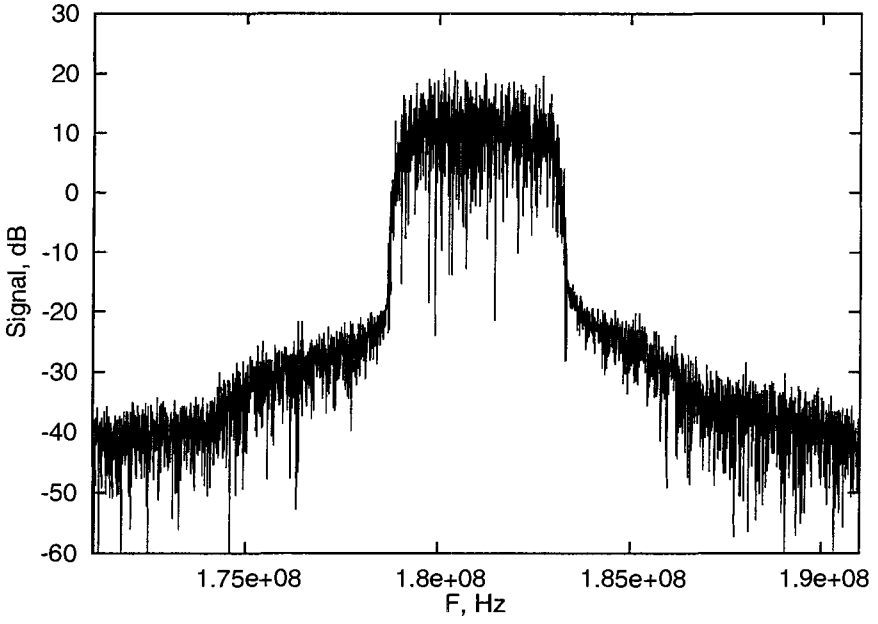


Figure 7.11: WCDMA output of PA.

found to be $PAE = 40.1\%$.

Second, WCDMA signal centered at the same frequency f_0, with peak–to–average ratio (PAR) of $8.7\,dB$, $SNR = 42\,dB$ within $BW = 10\,MHz$. In this case power added efficiency is $PAE = 16.6\%$.

Spectrum of WCDMA signal at the BP filter output is shown in Fig. 7.11 The currently reported PAE numbers for class–AB amplifiers are in range of 30–44% [11].

7.3 Summary

A novel fractional delay ΣΔ upconverter circuit architecture suitable for IF to RF upconversion inside a software–defined radio is presented. Mixed–signal behavioral simulations have confirmed validity of the upconverter concept.

Power efficient combination of a class–S PA and ΣΔ modulator topology suitable for wireless communications has been presented. It has been shown that PWM signal generated by a CT BP $f\Sigma\Delta$ modulator improves power efficiency and *SNR* of a class–S power amplifier. This topology offers a promising solution for future software–defined radio transmitters.

Chapter 8

Conclusions

In the previous chapters, the basics of $\Sigma\Delta$ modulation were first introduced, followed by the development of an analytical model for a CT BP $f\Sigma\Delta$ modulator transfer function. Then, a mixed–signal behavioral modeling technique was presented, which facilitated the transistor level design of the modulator prototype. Details of the tuning coefficient mapping from the analytical model to the behavioral model and from the behavioral model to the physical model were shown. A short review of the experimental results was followed by a discussion of possible applications that would benefit from the properties of the $f\Sigma\Delta$ modulators. In this section, closing comments are made regarding the results presented in this dissertation, concluding with suggestions for future work.

In Fig. 1.1, a total of 15 experimental designs were shown, which fell into the continuous time category. Various methodologies, architectures and technologies were used to create the designs. Some research groups explored design methodologies used to achieve high SNR, for example by using measurements over a very narrow BW, with high OSR [41, 55]. Other groups pushed the limits for higher signal frequencies, using either on–chip or passive components for the HF resonator ([26, 16, 15]). The architecture presented in this dissertation aimed to demonstrate the validity of the proposed design methodology and analytical models. The realized prototype circuit was comparable to other designs in terms of general circuit specifications; however, it was created from a complete analytical model capable of dealing with various signal and sampling frequencies, as well as various loop delays. Various exciting application possibilities were shown and practical implications of the achieved $f\Sigma\Delta$ model will be demonstrated in the future.

Although a large amount of knowledge related to CT BP $\Sigma\Delta$ modulators has been

accumulated, numerous outstanding issues open up many opportunities for future work:

1. A tuning algorithm for controlling the CT $\Sigma\Delta$ coefficients, which is robust enough for use in industrial applications, has still not been demonstrated. A relatively large number of control lines are required to tune the CT BP $\Sigma\Delta$ modulator center frequency, presenting a considerable implementation problem. This is particularly true for the case presented in this dissertation, where a continuous spectrum of tuning frequencies is targeted.

2. The elegance and versatility of the tunable bandpass filter implies that number of possible applications is very large. Potentially, the modulator may be applied to all forms of signal processing, from communication circuits and sensors to medical instrumentation. Having the analytical model, one can now work on various configurations optimized for specific solutions, such as low–power, small area, and specific frequency range.

3. As the design incorporates a mixed–signal model with a nonlinear element inside the loop, it may be possible to further simplify the analytical modeling or practical implementation through the use of log–domain [43] filter circuits.

4. Successful mapping functions were introduced in Chapter 3 for the 2^{nd} and 4^{th} order modulator cases. Only a partially successful mapping function was introduced for the 6^{th} order case; however, we are hopeful that an equally successful analytical model for $f\Sigma\Delta$ modulator of 6^{th} order can be found.

Appendix A

G_m–C resonator transfer function

The derivation of (5.1) is based on the notation shown in Fig. A.1; for simplicity, the single–ended version of the resonator is shown.

The currents at the capacitor nodes are:

$$i_{C_1} = sC_1V_0 \tag{A.1}$$

$$i_{C_2} = sC_2V_1 \tag{A.2}$$

$$i_{C_3} = sC_3V_2 \tag{A.3}$$

$$i_{C_4} = sC_4V_{out}. \tag{A.4}$$

The currents at the g_{a0} to g_{a3} output nodes are:

$$i_{a0} = g_{a0}V_{in} \tag{A.5}$$

$$i_{a1} = g_{a1}V_{in} \tag{A.6}$$

$$i_{a2} = g_{a2}V_{in} \tag{A.7}$$

$$i_{a3} = g_{a3}V_{in}. \tag{A.8}$$

Similarly, the currents at the g_1, g_2, g_{21}, g_{f1}, and g_{f2} output nodes are:

$$i_1 = g_1V_0 \tag{A.9}$$

$$i_{21} = g_{21}V_1 \tag{A.10}$$

$$i_2 = g_2V_2 \tag{A.11}$$

$$i_{f1} = -g_{f1}V_1 \tag{A.12}$$

$$i_{f2} = -g_{f2}V_{out}. \tag{A.13}$$

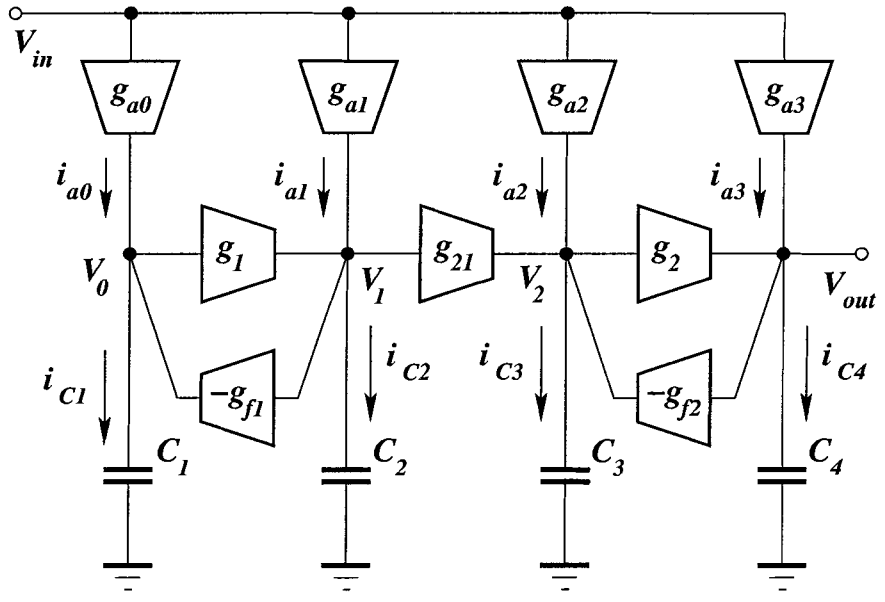


Figure A.1: Circuit diagram for a 4^{th} order single–ended g_m–C resonator.

After solving systems (A.1) to (A.13), we have:

$$H(s) = \frac{s^3 C_1 C_2 C_3 g_{a3} + s^2 C_1 C_2 g_{a2} g_2 + (C_1 g_{a1} g_{21} g_2 + C_3 g_{a3} g_1 g_{f1})\, s + g_{a0} g_1 g_{21} g_2 + g_{a2} g_1 g_2 g_{f1}}{(s^2 C_1 C_2 + g_1 g_{f1})\,(s^2 C_3 C_4 + g_2 g_{f2})}$$
$$= \frac{\frac{g_{a3}}{C_4} s^3 + \frac{g_{a2} g_2}{C_4 C_3} s^2 + \left(\frac{g_{a1} g_{21} g_2}{C_2 C_3 C_4} + \frac{g_{a3} g_1 g_{f1}}{C_2 C_1 C_4}\right) s + \frac{g_{a0} g_1 g_{21} g_2 + g_{a2} g_1 g_2 g_{f1}}{C_1 C_2 C_3 C_4}}{\left(s^2 + \frac{g_1 g_{f1}}{C_2 C_1}\right)\left(s^2 + \frac{g_2 g_{f2}}{C_4 C_3}\right)} \qquad \text{(A.14)}$$

Appendix B

Impulse invariant transformation

This appendix describes three time–domain pulse shapes: non–return to zero (NRZ), return–to–zero (RZ), and hold–return–to–zero (HZ); refer to Fig. B.1. In general, $p = T/2$ (for 50% RZ duty-cycle pulses); however, all values within $0 \leq p \leq T$ are possible. Setting $p = 0$ results in the theoretical $\delta(t)$ function, while setting $p = T$ gives the NRZ pulse.

B.1 Time domain definitions

The time domain definition of a pulse is based on the step function $u(t)$, which is defined as:

$$u(t) = \begin{cases} 0, & (t < 0); \\ 1, & (t \geq 0); \end{cases} \tag{B.1}$$

where t indicates the time. Clearly, by adding two step functions shifted in time, we arrive at the following definitions:

- **NRZ pulse**:

$$NRZ(t) = u(t) - u(t - T) \tag{B.2}$$

- **RZ pulse**:

$$RZ(t) = u(t) - u(t - p) \tag{B.3}$$

- **HZ pulse**:

$$HZ(t) = u(t - p) - u(t - T). \tag{B.4}$$

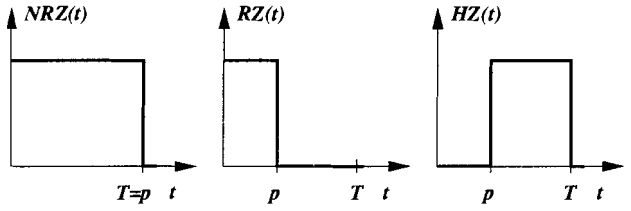


Figure B.1: DAC pulse forms for NRZ, RZ, and HZ

B.2 s–domain pulse forms

The Laplace transform of the step function is:

$$\mathcal{L}\left[u(t)\right] = \frac{1}{s}, \tag{B.5}$$

while the delayed step function Laplace transform is:

$$\mathcal{L}\left[u(t-T)\right] = \frac{e^{-sT}}{s}. \tag{B.6}$$

From (B.2), (B.3), and (B.4), it follows that:

$$\mathcal{L}\left[NRZ(t)\right] = \frac{1-e^{-sT}}{s} \tag{B.7}$$

$$\mathcal{L}\left[RZ(t)\right] = \frac{1-e^{-sp}}{s} \tag{B.8}$$

$$\mathcal{L}\left[HZ(t)\right] = \frac{e^{-sp}-e^{-sT}}{s}. \tag{B.9}$$

B.3 Pulse invariance

At all sampling instances, the inverse z–transform and inverse Laplace transform of a function must be equal. Therefore, the selected pulse shape delivered by the DAC must be accounted for in the pulse invariant transformation, given as follows:

$$\mathcal{Z}^{-1} = \mathcal{L}^{-1}\left[\frac{1-e^{-sT}}{s}\hat{H}(s)\right]_{t=nT} \tag{B.10}$$

$$\mathcal{Z}^{-1} = \mathcal{L}^{-1}\left[\frac{1-e^{-sp}}{s}\hat{H}(s)\right]_{t=nT} \tag{B.11}$$

$$\mathcal{Z}^{-1} = \mathcal{L}^{-1}\left[\frac{e^{-sp}-e^{-sT}}{s}\hat{H}(s)\right]_{t=nT}. \tag{B.12}$$

This appendix describes two cases of $\hat{H}(s)$:

1. $\hat{H}(s)$ only has a multiple number of single poles

2. $\hat{H}(s)$ only has a multiple number of double poles

These two cases are sufficient to create 2^{nd} and 4^{th} order CT BP $\Sigma\Delta$ functions, while the 6^{th} order $\Sigma\Delta$ function requires a mapping to deal with the triple poles. The 6^{th} order function is derived via the same methodology used for the 2^{nd} and 4^{th} order functions; however, the complexity of the equations is much higher and the function must be evaluated using symbolic mathematical software.

B.4 Single pole H(z) case

A general z–domain transfer function with N single poles is:

$$H(z) = \sum_{k=1}^{N} \frac{a_k z^{-1}}{1 - z_k z^{-1}} = \sum_{k=1}^{N} \frac{a_k}{z - z_k}, \tag{B.13}$$

where z_k is a single pole [29]. The equivalent s–domain function is given by:

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{s - s_k}, \tag{B.14}$$

with the impulse response function being:

$$\hat{h}(t) = \sum_{k=1}^{N} \hat{a}_k e^{s_k T} u(t), \tag{B.15}$$

where ($\hat{}$) is used to indicate a continuous time parameter.

In order to perform the transformation $H(z) \rightarrow \hat{H}(s)$, the relationship between the discrete time coefficient a_k and its continuous time equivalent $\hat{a}_k$ must first be determined. One possible approach is to start with the time domain impulse response and convolve it with the pulse:

$$h(nT) = \left[R_p(t) * \hat{h}(t)\right]_{t=nT} = \left[\int_{-\infty}^{+\infty} R_p(\tau)\hat{h}(t-\tau)d\tau\right]_{t=nT}, \tag{B.16}$$

where $R_p(t)$ is the time domain pulse shape.

B.5 NRZ impulse response

From (B.16) and Fig. B.1, we can derive:

$$h(t) = R_{NRZ}(t) * \hat{h}(t)$$

$$= \int_{-\infty}^{+\infty} R_{NRZ}(\tau)\hat{h}(t-\tau)d\tau = \begin{cases} 0, & (t<0) \\ \int_0^t \hat{h}(t-\tau)d\tau, & (0 \le t < T) \\ \int_0^T \hat{h}(t-\tau)d\tau, & (t \ge T). \end{cases} \quad \text{(B.17)}$$

Then, substituting $\hat{h}(t)$ from (B.15) results in:

1. $(0 \le t < T)$

$$h(t) = \int_0^t \left[\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)}\right] d\tau$$

$$= \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^t e^{-s_k \tau} d\tau\right] = \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k t}}{-s_k} \left(e^{-s_k t} - 1\right) \quad \text{(B.18)}$$

2. $(t \ge T)$

$$h(t) = \int_0^T \left[\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)}\right] d\tau$$

$$= \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^T e^{-s_k \tau} d\tau\right] = \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k t}}{-s_k} \left(e^{-s_k T} - 1\right) \quad \text{(B.19)}$$

Thus, at $t = nT$:

$$h(nT) = \begin{cases} 0, & (0 \le t \le T) \\ \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k nT}}{-s_k} \left(e^{-s_k T} - 1\right), & (t \ge T). \end{cases} \quad \text{(B.20)}$$

B.6 RZ impulse response

From (B.16) and Fig. B.1, we can derive:

$$h(t) = R_{RZ}(t) * \hat{h}(t)$$

$$= \int_{-\infty}^{+\infty} R_{RZ}(\tau)\hat{h}(t-\tau)d\tau = \begin{cases} 0, & (t<0) \\ \int_0^t \hat{h}(t-\tau)d\tau, & (0 \le t < p) \\ \int_0^p \hat{h}(t-\tau)d\tau, & (t \ge p). \end{cases} \quad \text{(B.21)}$$

Then, substituting $\hat{h}(t)$ from (B.15) results in:

1. $(0 \leq t < p)$

$$h(t) = \int_0^t \left[\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)}\right] d\tau$$
$$= \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^t e^{-s_k \tau} d\tau\right] = \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k t}}{-s_k} \left(e^{-s_k t} - 1\right) \tag{B.22}$$

2. $(t \geq p)$

$$h(t) = \int_0^p \left[\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)}\right] d\tau$$
$$= \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_0^p e^{-s_k \tau} d\tau\right] = \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k t}}{-s_k} \left(e^{-s_k p} - 1\right) \tag{B.23}$$

Thus, at $t = nT$:

$$h(nT) = \begin{cases} 0, & (0 \leq t \leq p) \\ \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k nT}}{-s_k} \left(e^{-s_k p} - 1\right), & (t \geq p) \end{cases} \tag{B.24}$$

B.7 HZ impulse response

From (B.16) and Fig. B.1, we can derive:

$$h(t) = R_{HZ}(t) * \hat{h}(t)$$
$$= \int_{-\infty}^{+\infty} R_{HZ}(\tau)\hat{h}(t-\tau)d\tau = \begin{cases} 0, & (t < p) \\ \int_p^t \hat{h}(t-\tau)d\tau, & (p \leq t < T) \\ \int_p^T \hat{h}(t-\tau)d\tau, & (t \geq T). \end{cases} \tag{B.25}$$

Then, substituting $\hat{h}(t)$ from (B.15) results in:

1. $(p \leq t < T)$

$$h(t) = \int_p^t \left[\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)}\right] d\tau$$
$$= \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_p^t e^{-s_k \tau} d\tau\right] = \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k t}}{-s_k} \left(e^{-s_k t} - e^{-s_k p}\right) \tag{B.26}$$

2. $(t \geq T)$

$$h(t) = \int_p^T \left[\sum_{k=1}^{N} \hat{a}_k e^{s_k(t-\tau)}\right] d\tau$$
$$= \sum_{k=1}^{N} \hat{a}_k e^{s_k t} \left[\int_p^T e^{-s_k \tau} d\tau\right] = \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k t}}{-s_k} \left(e^{-s_k T} - e^{-s_k p}\right) \quad \text{(B.27)}$$

Thus, at $t = nT$:

$$h(nT) = \begin{cases} 0, & (p \leq t \leq T) \\ \sum_{k=1}^{N} \frac{\hat{a}_k e^{s_k nT}}{-s_k} \left(e^{-s_k T} - e^{-s_k p}\right), & (t \geq T). \end{cases} \quad \text{(B.28)}$$

B.8 DT to CT mapping

1. $H(z)$: NRZ transformation function

$$H(z) = \sum_{n=-\infty}^{+\infty} h(n) z^{-n}$$
$$= \sum_{n=1}^{+\infty} \left[\sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} e^{s_k nT} \left(e^{-s_k T} - 1\right)\right] z^{-n}$$
$$= \sum_{k=1}^{N} \left[\frac{\hat{a}_k}{-s_k} \left(e^{-s_k T} - 1\right) \sum_{n=1}^{\infty} e^{s_k nT} z^{-n}\right]$$
$$= \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} \left(e^{-s_k T} - 1\right) \frac{e^{s_k T}}{(-e^{s_k T} + z)}$$
$$= \sum_{k=1}^{N} \frac{\hat{a}_k}{-s_k} \frac{\left(1 - e^{s_k T}\right)}{\left(1 - e^{s_k T} z^{-1}\right)} z^{-1}$$
$$= \sum_{k=1}^{N} \frac{a_k z^{-1}}{1 - z_k z^{-1}}$$

where:

$$a_k = \frac{\hat{a}_k}{-s_k} \left(1 - e^{s_k T}\right) \text{ and } z_k = e^{s_k T} \quad \text{(B.29)}$$

2. $H(z)$: RZ transformation function

$$\begin{aligned}
H(z) &= \sum_{n=-\infty}^{+\infty} h(n)z^{-n} \\
&= \sum_{n=1}^{+\infty}\left[\sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}e^{s_k nT}\left(e^{-s_k p}-1\right)\right]z^{-n} \\
&= \sum_{k=1}^{N}\left[\frac{\hat{a}_k}{-s_k}\left(e^{-s_k p}-1\right)\sum_{n=1}^{\infty}e^{s_k nT}z^{-n}\right] \\
&= \sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}\left(e^{-s_k p}-1\right)\frac{e^{s_k T}}{(-e^{s_k T}+z)} \\
&= \sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}\frac{\left(e^{s_k p}-e^{s_k T}\right)}{(1-e^{s_k T}z^{-1})}z^{-1} \\
&= \sum_{k=1}^{N}\frac{a_k z^{-1}}{1-z_k z^{-1}}
\end{aligned}$$

where:

$$a_k = \frac{\hat{a}_k}{-s_k}\left(e^{s_k p}-e^{s_k T}\right) \text{ and } z_k = e^{s_k T} \tag{B.30}$$

3. $H(z)$: HZ transformation function

$$\begin{aligned}
H(z) &= \sum_{n=-\infty}^{+\infty} h(n)z^{-n} \\
&= \sum_{n=1}^{+\infty}\left[\sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}e^{s_k nT}\left(e^{-s_k T}-e^{-s_k p}\right)\right]z^{-n} \\
&= \sum_{k=1}^{N}\left[\frac{\hat{a}_k}{-s_k}\left(e^{-s_k T}-e^{-s_k p}\right)\sum_{n=1}^{\infty}e^{s_k nT}z^{-n}\right] \\
&= \sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}\left(e^{-s_k T}-e^{-s_k p}\right)\frac{e^{s_k T}}{(-e^{s_k T}+z)} \\
&= \sum_{k=1}^{N}\frac{\hat{a}_k}{-s_k}\frac{(1-e^{s_k p})}{(1-e^{s_k T}z^{-1})}z^{-1} \\
&= \sum_{k=1}^{N}\frac{a_k z^{-1}}{1-z_k z^{-1}}
\end{aligned}$$

where:

$$a_k = \frac{\hat{a}_k}{-s_k}\left(1 - e^{s_k p}\right) \text{ and } z_k = e^{s_k T} \tag{B.31}$$

B.9 Double pole H(z) case

The general z–domain transfer function with N double poles z_k:

$$H(z) = \sum_{k=1}^{N} \frac{a_k z^{-2}}{\left(1 - z_k z^{-1}\right)^2} = \sum_{k=1}^{N} \frac{a_k}{\left(z - z_k\right)^2}, \tag{B.32}$$

has an equivalent s–domain function given by:

$$\hat{H}(s) = \sum_{k=1}^{N} \frac{\hat{a}_k}{\left(s - s_k\right)^2}. \tag{B.33}$$

An effective approach for this transformation is to apply a limit to the two single pole case, in order to cause convergence of the two poles [48].

B.10 Double pole NRZ case

For $s_{k1} \neq s_{k2} \rightarrow s_k$

$$\begin{aligned} H(z) &= \frac{a_k}{\left(z - e^{s_k T}\right)^2} \\ &= \frac{a_k}{\left(z - e^{s_{k1} T}\right)\left(z - e^{s_{k2} T}\right)} \\ &= \frac{A_1}{\left(z - e^{s_{k1} T}\right)} + \frac{A_2}{\left(z - e^{s_{k2} T}\right)} \\ &= \frac{A_1\left(z - e^{s_{k2} T}\right) + A_2\left(z - e^{s_{k1} T}\right)}{\left(z - e^{s_{k1} T}\right)\left(z - e^{s_{k2} T}\right)} \\ &= \frac{z\left(A_1 + A_2\right) - \left(A_1 e^{s_{k2} T} + A_2 e^{s_{k1} T}\right)}{\left(z - e^{s_{k1} T}\right)\left(z - e^{s_{k2} T}\right)}. \end{aligned}$$

After solving for the A_i $(i = 1, 2)$ constants:

$$\begin{aligned} A_1 &= \frac{-a_k}{e^{s_{k2} T} - e^{s_{k1} T}} \\ A_2 &= \frac{a_k}{e^{s_{k2} T} - e^{s_{k1} T}}, \end{aligned}$$

it follows that

$$H(z) = \frac{\frac{-a_k}{e^{s_{k2}T} - e^{s_{k1}T}}}{\left(z - e^{s_{k1}T}\right)} + \frac{\frac{a_k}{e^{s_{k2}T} - e^{s_{k1}T}}}{\left(z - e^{s_{k2}T}\right)}.$$

From the relations between $H(z)$ and $\hat{H}(s)$ and between a_k and $\hat{a}_k$, we can write:

$$\begin{aligned}
\hat{H}(s) =& \frac{\hat{a}_{k1}}{s - s_{k1}} + \frac{\hat{a}_{k2}}{s - s_{k2}} \\
=& \frac{\frac{-s_{k1}}{\left(1 - e^{s_{k1}T}\right)} a_{k1}}{s - s_{k1}} + \frac{\frac{-s_{k2}}{\left(1 - e^{s_{k2}T}\right)} a_{k2}}{s - s_{k2}} \\
=& \frac{\frac{-s_{k1}}{\left(1 - e^{s_{k1}T}\right)} \frac{-a_k}{e^{s_{k2}T} - e^{s_{k1}T}}}{s - s_{k1}} + \frac{\frac{-s_{k2}}{\left(1 - e^{s_{k2}T}\right)} \frac{a_k}{e^{s_{k2}T} - e^{s_{k1}T}}}{s - s_{k2}} \\
=& \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[\frac{s_{k1}(s - s_{k2})}{(1 - e^{s_{k1}T})(e^{s_{k2}T} - e^{s_{k1}T})} + \frac{-s_{k2}(s - s_{k1})}{(1 - e^{s_{k2}T})(e^{s_{k2}T} - e^{s_{k1}T})} \right] \\
=& \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[\frac{s_{k1}\left(1 - e^{s_{k2}T}\right)(s - s_{k2})}{(1 - e^{s_{k1}T})(1 - e^{s_{k2}T})(e^{s_{k2}T} - e^{s_{k1}T})} - \right. \\
& \left. - \frac{s_{k2}\left(1 - e^{s_{k1}T}\right)(s - s_{k1})}{(1 - e^{s_{k1}T})(1 - e^{s_{k2}T})(e^{s_{k2}T} - e^{s_{k1}T})} \right] \\
=& \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[\frac{(s_{k1} - s_{k2}) + \left(s_{k2}e^{s_{k1}T} - s_{k1}e^{s_{k2}T}\right)}{(1 - e^{s_{k1}T})(1 - e^{s_{k2}T})(e^{s_{k2}T} - e^{s_{k1}T})} s + \frac{s_{k1}s_{k2}}{(1 - e^{s_{k1}T})(1 - e^{s_{k2}T})} \right] \\
=& \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[C_1 s + C_0\right],
\end{aligned}$$

where

$$\begin{aligned}
C_1 &= \frac{(s_{k1} - s_{k2}) + \left(s_{k2}e^{s_{k1}T} - s_{k1}e^{s_{k2}T}\right)}{(1 - e^{s_{k1}T})(1 - e^{s_{k2}T})(e^{s_{k2}T} - e^{s_{k1}T})} \\
C_2 &= \frac{s_{k1}s_{k2}}{(1 - e^{s_{k1}T})(1 - e^{s_{k2}T})}.
\end{aligned}$$

For $s_{k1} \to s_{k2} \Rightarrow C_1 \to \frac{0}{0}$; therefore L'Hopital's rule must be applied:

$$\begin{aligned}
&\lim_{s_{k1}, s_{k2} \to s_k} C_1 = \\
&= \frac{1}{(1 - e^{s_k T})^2} \lim_{s_{ki} \to s_k} \frac{\left[s_{k1} - s_{k2} + s_{k2}e^{s_{k1}T} - s_{k1}e^{s_{k2}T}\right]'_{s_{k2}}}{\left[e^{s_{k2}T} - e^{s_{k1}T}\right]'_{s_{k2}}} \\
&= \frac{1}{(1 - e^{s_k T})^2} \lim_{s_{ki} \to s_k} \frac{-1 + e^{s_{k1}T} - s_{k1}Te^{s_{k2}T}}{Te^{s_{k2}T}} \\
&= \frac{1}{(1 - e^{s_k T})^2} \frac{1 - Ts_k - e^{-s_k T}}{T}.
\end{aligned}$$

Finally, we arrive at:

$$\hat{H}(s) = \frac{a_k}{(s-s_k)^2} \lim_{s_{k1},s_{k2}\to s_k} [C_1 s + C_0] = \frac{a_k}{(s-s_k)^2}\left[\frac{1 - Ts_k - e^{-s_k T}}{(1-e^{s_k T})^2}\frac{s}{T} + \frac{s_k^2}{(1-e^{s_k T})^2}\right].$$

B.11 Double pole RZ case

For $s_{k1} \neq s_{k2} \to s_k$

$$\begin{aligned} H(z) &= \frac{a_k}{(z-e^{s_k T})^2} \\ &= \frac{a_k}{(z-e^{s_{k1}T})(z-e^{s_{k2}T})} \\ &= \frac{A_1}{(z-e^{s_{k1}T})} + \frac{A_2}{(z-e^{s_{k2}T})} \\ &= \frac{A_1(z-e^{s_{k2}T}) + A_2(z-e^{s_{k1}T})}{(z-e^{s_{k1}T})(z-e^{s_{k2}T})} \\ &= \frac{z(A_1+A_2) - (A_1 e^{s_{k2}T} + A_2 e^{s_{k1}T})}{(z-e^{s_{k1}T})(z-e^{s_{k2}T})}. \end{aligned}$$

After solving for the A_i $(i = 1, 2)$ constants:

$$\begin{aligned} A_1 &= \frac{-a_k}{e^{s_{k2}T} - e^{s_{k1}T}} \\ A_2 &= \frac{a_k}{e^{s_{k2}T} - e^{s_{k1}T}}, \end{aligned}$$

it follows that

$$H(z) = \frac{\frac{-a_k}{e^{s_{k2}T}-e^{s_{k1}T}}}{(z-e^{s_{k1}T})} + \frac{\frac{a_k}{e^{s_{k2}T}-e^{s_{k1}T}}}{(z-e^{s_{k2}T})}.$$

From the relations between $H(z)$ and $\hat{H}(s)$ and between a_k and $\hat{a}_k$, we can write:

$$\begin{aligned} \hat{H}(s) =& \frac{\hat{a}_{k1}}{s-s_{k1}} + \frac{\hat{a}_{k2}}{s-s_{k2}} \\ =& \frac{\frac{-s_{k1}}{(e^{s_{k1}p}-e^{s_{k1}T})}a_{k1}}{s-s_{k1}} + \frac{\frac{-s_{k2}}{(e^{s_{k2}p}-e^{s_{k2}T})}a_{k2}}{s-s_{k2}} \\ =& \frac{\frac{-s_{k1}}{(e^{s_{k1}p}-e^{s_{k1}T})}\frac{-a_k}{e^{s_{k2}T}-e^{s_{k1}T}}}{s-s_{k1}} + \frac{\frac{-s_{k2}}{(e^{s_{k2}p}-e^{s_{k2}T})}\frac{a_k}{e^{s_{k2}T}-e^{s_{k1}T}}}{s-s_{k2}} \\ =& \frac{a_k}{(s-s_{k1})(s-s_{k2})}\left[\frac{s_{k1}(s-s_{k2})}{(e^{s_{k1}p}-e^{s_{k1}T})(e^{s_{k2}T}-e^{s_{k1}T})} + \right. \\ &\left. + \frac{-s_{k2}(s-s_{k1})}{(e^{s_{k2}p}-e^{s_{k2}T})(e^{s_{k2}T}-e^{s_{k1}T})}\right] \end{aligned} \tag{B.34}$$

$$\begin{aligned}\hat{H}(s) =& \frac{a_k}{(s-s_{k1})(s-s_{k2})}\left[\frac{\left[s_{k1}\left(e^{s_{k2}p}-e^{s_{k2}T}\right)-s_{k2}\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\right]s}{\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\left(e^{s_{k2}p}-e^{s_{k2}T}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)}-\right.\\ &\left.-\frac{s_{k1}s_{k2}\left(e^{s_{k2}p}-e^{s_{k2}T}-e^{s_{k1}p}+e^{s_{k1}T}\right)}{\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\left(e^{s_{k2}p}-e^{s_{k2}T}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)}\right]\\ =& \frac{a_k}{(s-s_{k1})(s-s_{k2})}\left[C_1 s - C_0\right],\end{aligned}$$

where

$$\begin{aligned}C_1 &= \frac{s_{k1}\left(e^{s_{k2}p}-e^{s_{k2}T}\right)-s_{k2}\left(e^{s_{k1}p}-e^{s_{k1}T}\right)}{\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\left(e^{s_{k2}p}-e^{s_{k2}T}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)}\\ C_0 &= \frac{s_{k1}s_{k2}\left(e^{s_{k2}p}-e^{s_{k2}T}-e^{s_{k1}p}+e^{s_{k1}T}\right)}{\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\left(e^{s_{k2}p}-e^{s_{k2}T}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)}.\end{aligned}$$

For $s_{k1} \to s_{k2} \Rightarrow C_1 \to \frac{0}{0}$; therefore L'Hopital's rule must be applied:

$$\begin{aligned}\lim_{s_{k1},s_{k2}\to s_k} C_1 &= \lim_{s_{ki}\to s_k} \frac{\left[s_{k1}\left(e^{s_{k2}p}-e^{s_{k2}T}\right)-s_{k2}\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\right]'_{s_{k2}}}{\left[\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\left(e^{s_{k2}p}-e^{s_{k2}T}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)\right]'_{s_{k2}}}\\ &\lim_{s_{ki}\to s_k} \frac{\left[s_{k1}e^{s_{k2}T}\left(e^{-s_{k2}p}-1\right)-s_{k2}e^{s_{k1}T}\left(e^{-s_{k1}p}-1\right)\right]'_{s_{k2}}}{\left[e^{2s_{k2}p}\left(1-e^{s_{k2}(T-p)}\right)\left(1-e^{s_{k2}(T-p)}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)\right]'_{s_{k2}}}\\ &\vdots\\ &= \frac{1-e^{-s_kp}-s_kT\left(1-\frac{1}{2}e^{-s_kp}\right)}{\left[e^{s_kp}\left(1-e^{s_k(T-p)}\right)\right]^2T}\end{aligned}$$

and

$$\begin{aligned}\lim_{s_{k1},s_{k2}\to s_k} C_0 &= \lim_{s_{ki}\to s_k} \frac{\left[s_{k1}s_{k2}\left(e^{s_{k2}p}-e^{s_{k2}T}-e^{s_{k1}p}+e^{s_{k1}T}\right)\right]'_{sk2}}{\left[\left(e^{s_{k1}p}-e^{s_{k1}T}\right)\left(e^{s_{k2}p}-e^{s_{k2}T}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)\right]'_{sk2}}\\ &\lim_{s_{ki}\to s_k} \frac{\left[-s_{k1}s_{k2}\left[-e^{s_{k2}T}\left(1-e^{-s_{k2}p}\right)+e^{s_{k1}T}\left(1-e^{-s_{k2}p}\right)\right]\right]'_{sk2}}{\left[e^{2s_{k1}p}\left(1-e^{s_{k1}(T-p)}\right)\left(1-e^{s_{k2}(T-p)}\right)\left(e^{s_{k2}T}-e^{s_{k1}T}\right)\right]'_{sk2}}\\ &\vdots\\ &= \frac{s_k^2\left(1-\frac{1}{2}e^{-s_kp}\right)}{\left[e^{s_kp}\left(1-e^{s_kp}\right)\right]^2}.\end{aligned}$$

Finally, we arrive at:

$$\begin{aligned}\hat{H}(s) &= \frac{a_k}{(s-s_k)^2}\lim_{s_{k1},s_{k2}\to s_k}\left[C_1 s + C_0\right]\\ &= \frac{a_k}{(s-s_k)^2e^{2s_kp}}\left[\frac{1-e^{-s_kp}-s_kT\left(1-\frac{1}{2}e^{-s_kp}\right)}{(1-e^{s_k(T-p)})^2}\frac{s}{T}+\frac{s_k^2\left(1-\frac{1}{2}e^{-s_kp}\right)}{(1-e^{s_k(T-p)})^2}\right].\end{aligned}$$

B.12 Double pole HZ case

For $s_{k1} \neq s_{k2} \rightarrow s_k$

$$\begin{aligned} H(z) &= \frac{a_k}{(z - e^{s_k T})^2} \\ &= \frac{a_k}{(z - e^{s_{k1} T})(z - e^{s_{k2} T})} \\ &= \frac{A_1}{(z - e^{s_{k1} T})} + \frac{A_2}{(z - e^{s_{k2} T})} \\ &= \frac{A_1 (z - e^{s_{k2} T}) + A_2 (z - e^{s_{k1} T})}{(z - e^{s_{k1} T})(z - e^{s_{k2} T})} \\ &= \frac{z(A_1 + A_2) - (A_1 e^{s_{k2} T} + A_2 e^{s_{k1} T})}{(z - e^{s_{k1} T})(z - e^{s_{k2} T})} \end{aligned}$$

After solving for the A_i $(i = 1, 2)$ constants:

$$\begin{aligned} A_1 &= \frac{-a_k}{e^{s_{k2} T} - e^{s_{k1} T}} \\ A_2 &= \frac{a_k}{e^{s_{k2} T} - e^{s_{k1} T}}, \end{aligned}$$

it follows that

$$H(z) = \frac{\frac{-a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{(z - e^{s_{k1} T})} + \frac{\frac{a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{(z - e^{s_{k2} T})}.$$

From the relations between $H(z)$ and $\hat{H}(s)$ and between a_k and $\hat{a}_k$, we can write:

$$\begin{aligned} \hat{H}(s) =& \frac{\hat{a}_{k1}}{s - s_{k1}} + \frac{\hat{a}_{k2}}{s - s_{k2}} \\ =& \frac{\frac{-s_{k1}}{(1 - e^{s_{k1} p})} a_{k1}}{s - s_{k1}} + \frac{\frac{-s_{k2}}{(1 - e^{s_{k2} p})} a_{k2}}{s - s_{k2}} \\ =& \frac{\frac{-s_{k1}}{(1 - e^{s_{k1} p})} \frac{-a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{s - s_{k1}} + \frac{\frac{-s_{k2}}{(1 - e^{s_{k2} p})} \frac{a_k}{e^{s_{k2} T} - e^{s_{k1} T}}}{s - s_{k2}} \\ =& \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[\frac{s_{k1} (s - s_{k2})}{(1 - e^{s_{k1} p})(e^{s_{k2} T} - e^{s_{k1} T})} + \frac{-s_{k2} (s - s_{k1})}{(1 - e^{s_{k2} p})(e^{s_{k2} T} - e^{s_{k1} T})} \right] \\ =& \frac{a_k}{(s - s_{k1})(s - s_{k2})} \left[\frac{s_{k1} (1 - e^{s_{k2} p})(s - s_{k2})}{(1 - e^{s_{k1} p})(1 - e^{s_{k2} p})(e^{s_{k2} T} - e^{s_{k1} T})} - \right. \\ & \left. - \frac{s_{k2} (1 - e^{s_{k1} p})(s - s_{k1})}{(1 - e^{s_{k1} p})(1 - e^{s_{k2} p})(e^{s_{k2} T} - e^{s_{k1} T})} \right] \end{aligned} \tag{B.35}$$

$$\begin{aligned}\hat{H}(s) =& \frac{a_k}{(s-s_{k1})(s-s_{k2})}\left[\frac{(s_{k1}-s_{k2})+(s_{k2}e^{s_{k1}p}-s_{k1}e^{s_{k2}p})}{(1-e^{s_{k1}p})(1-e^{s_{k2}p})(e^{s_{k2}T}-e^{s_{k1}T})}s+\right.\\ &\left.+\frac{s_{k1}s_{k2}(e^{s_{k2}p}-e^{s_{k1}p})}{(1-e^{s_{k1}p})(1-e^{s_{k2}p})(e^{s_{k2}T}-e^{s_{k1}T})}\right]\\ =& \frac{a_k}{(s-s_{k1})(s-s_{k2})}\left[C_1 s + C_0\right],\end{aligned}$$

where

$$\begin{aligned}C_1 &= \frac{(s_{k1}-s_{k2})+(s_{k2}e^{s_{k1}p}-s_{k1}e^{s_{k2}p})}{(1-e^{s_{k1}p})(1-e^{s_{k2}p})(e^{s_{k2}T}-e^{s_{k1}T})}\\ C_0 &= \frac{s_{k1}s_{k2}(e^{s_{k2}p}-e^{s_{k1}p})}{(1-e^{s_{k1}p})(1-e^{s_{k2}p})(e^{s_{k2}T}-e^{s_{k1}T})}.\end{aligned}$$

For $s_{k1} \to s_{k2} \Rightarrow C_1 \to \frac{0}{0}$; therefore L'Hopital's rule must be applied:

$$\begin{aligned}\lim_{s_{k1},s_{k2}\to s_k} C_1 &= \lim_{s_{ki}\to s_k} \frac{\left[(s_{k1}-s_{k2})+(s_{k2}e^{s_{k1}p}-s_{k1}e^{s_{k2}p})\right]'_{s_{k2}}}{\left[(1-e^{s_{k1}p})(1-e^{s_{k2}p})(e^{s_{k2}T}-e^{s_{k1}T})\right]'_{s_{k2}}}\\ &\vdots\\ &= e^{-skp}\frac{1-\frac{T}{2}s_k-e^{-s_kp}}{(1-e^{s_kp})^2}\frac{1}{T}\end{aligned}$$

and

$$\begin{aligned}\lim_{s_{k1},s_{k2}\to s_k} C_0 &= \lim_{s_{ki}\to s_k} \frac{\left[s_{k1}s_{k2}(e^{s_{k2}p}-e^{s_{k1}p})\right]'_{s_{k2}}}{\left[(1-e^{s_{k1}p})(1-e^{s_{k2}p})(e^{s_{k2}T}-e^{s_{k1}T})\right]'_{s_{k2}}}\\ &\vdots\\ &= e^{-skp}\frac{\frac{1}{2}s_k^2}{(1-e^{s_kp})^2}\frac{1}{T}.\end{aligned}$$

Finally, we arrive at:

$$\begin{aligned}\hat{H}(s) &= \frac{a_k}{(s-s_k)^2}\lim_{s_{k1},s_{k2}\to s_k}\left[C_1 s + C_0\right]\\ &= \frac{a_k}{(s-s_k)^2}e^{-skp}\left[\frac{1-\frac{T}{2}s_k-e^{-s_kp}}{(1-e^{s_kp})^2}\frac{s}{T}+\frac{\frac{1}{2}s_k^2}{(1-e^{s_kp})^2}\right].\end{aligned}$$

Appendix C

A 4^{th} order $\Sigma\Delta$ transfer function

In this Appendix, the derivation of (3.29) is described in detail.

The development of the CT BP $\Sigma\Delta$ loop function starts with the z–domain description of the $f_s/4$ $\Sigma\Delta$ NTF. One way to create a 4^{th} order NTF is to place 2 resonators on the signal path of the $\Sigma\Delta$ loop [36]

$$NTF(z) = (1 + z^{-2})^2 \tag{C.1}$$

$$H_m(z) = \frac{NTF - 1}{NTF}, \tag{C.2}$$

where m is the filter order. Substitution of (C.1) into (C.2) results in the 4^{th} order $f_s/4$ filter transfer function $H_4(z)$:

$$H_4(z) = \frac{2z^2 + 1}{(z^2 + 1)^2}. \tag{C.3}$$

(C.4)

The partial fraction form is given by:

$$H_4(z) = \frac{\frac{3}{4}j}{z + j} + \frac{-\frac{3}{4}j}{z - j} + \frac{\frac{1}{4}}{(z + j)^2} + \frac{\frac{1}{4}}{(z - j)^2}, \tag{C.5}$$

where the poles are $z_{k1} = -j$, $z_{k2} = j$, $z_{k3} = -j$, and $z_{k4} = j$. The mapping functions used in this example are:

$$a_{k1} = \frac{e^{j\frac{\theta}{2}} + 4\,e^{-j\frac{3\theta}{2}} - 3\,e^{-j\frac{\theta}{2}}}{4\,e^{j\frac{\theta}{2}} - 4\,e^{-j\frac{\theta}{2}}} \tag{C.6}$$

$$a_{k2} = -\frac{e^{-j\frac{\theta}{2}} + 4\,e^{j\frac{3\theta}{2}} - 3\,e^{j\frac{\theta}{2}}}{4\,e^{j\frac{\theta}{2}} - 4\,e^{-j\frac{\theta}{2}}} \tag{C.7}$$

$$a_{k3} = -\frac{1}{4} e^{-2j\theta} \tag{C.8}$$

$$a_{k4} = -\frac{1}{4} e^{2j\theta}. \tag{C.9}$$

Each of the partial fraction terms in (C.5) are generalized in the z–domain using the following transformation:

$$H_{pf}(z) = \frac{a_{ki}}{(z - z_{ki})^n}, \tag{C.10}$$

where $i = 1, 2, 3, 4$ and $n = 1, 2$ is z_{ki} pole order; poles z_{k1}, z_{k2} are single poles, while poles z_{k3}, and z_{k4} are double poles.

The application of (C.10) to each term in (C.5) results in the following generalized tunable z–domain transfer function:

$$H(z,\theta) = \frac{-4\cos(\theta)z^3 + (-\cos(\theta) + 3\cos(2\theta) + 7)z^2 - \cos(\theta) + (-8\cos(\theta) + \cos(2\theta) + 1)z + 2}{2z^4 - 8\cos(\theta)z^3 - 8\cos(\theta)z + (4\cos(2\theta) + 8)z^2 + 2}. \tag{C.11}$$

The conversion from the z–domain to s–domain is first done for the single–pole partial fraction terms, using the following transformations:

$$s_{ki} = \frac{1}{T\ln(z_{ki})} \tag{C.12}$$

$$\hat{a} = -\frac{a_{ki}\, s_{ki}}{1 - e^{s_{ki}T}} \tag{C.13}$$

$$H_{sk} = \frac{\hat{a}}{s - s_{ki}}, \tag{C.14}$$

resulting in:

$$H_{s1} = \frac{j\left(e^{j\frac{\theta}{2}} + 4e^{-j\frac{3\theta}{2}} - 3e^{-j\frac{\theta}{2}}\right)\theta}{\left(4e^{j\frac{\theta}{2}} - 4e^{-j\frac{\theta}{2}}\right)T\left(1 - e^{-j\theta}\right)\left(s + \frac{j\theta}{T}\right)} \tag{C.15}$$

$$H_{s2} = \frac{j\left(e^{-j\frac{\theta}{2}} + 4e^{j\frac{3\theta}{2}} - 3e^{j\frac{\theta}{2}}\right)\theta}{\left(4e^{j\frac{\theta}{2}} - 4e^{-j\frac{\theta}{2}}\right)T\left(1 - e^{j\theta}\right)\left(s - \frac{j\theta}{T}\right)}. \tag{C.16}$$

Next, for the double-pole partial fraction terms, the following transformations are used:

$$s_{ki} = \frac{1}{T \ln(z_{ki})} \tag{C.17}$$

$$C_1 = \frac{1}{T} \frac{1 - T\, s_{ki} - e^{-s_{ki} T}}{(1 - e^{s_{ki} T})^2} \tag{C.18}$$

$$C_0 = \frac{s_{ki}^2}{(1 - e^{s_{ki} T})^2} \tag{C.19}$$

$$H_{sk} = \frac{a_{ki}}{(s - s_{ki})^2} (C_1\, s + C_0), \tag{C.20}$$

resulting in:

$$H_{s3} = -\frac{e^{-2j\theta} \left[\frac{(1+j\theta-e^{j\theta})}{(-1+e^{-j\theta})^2} \frac{s}{T} - \frac{\theta^2}{T^2} \frac{1}{(1-e^{-j\theta})^2} \right]}{4 \left(s + \frac{j\theta}{T} \right)^2} \tag{C.21}$$

$$H_{s4} = -\frac{e^{2j\theta} \left[-\frac{(-1+j\theta+e^{-j\theta})}{(-1+e^{j\theta})^2} \frac{s}{T} - \frac{\theta^2}{T^2} \frac{1}{(1-e^{j\theta})^2} \right]}{4 \left(s - \frac{j\theta}{T} \right)^2}. \tag{C.22}$$

The addition of equations (C.15), (C.16), (C.21), and (C.22) results in:

$$H_0(s) = \frac{\frac{H_{03}}{T} s^3 + \frac{H_{02}}{T^2} s^2 + \frac{H_{01}}{T^3} s + \frac{H_{00}}{T^4}}{\left[s^2 + \left(\frac{\theta - \delta}{T} \right)^2 \right] \left[s^2 + \left(\frac{\theta + \delta}{T} \right)^2 \right]}, \tag{C.23}$$

where,

$$H_{03} = -\frac{\theta}{2} \frac{\sin\theta}{(1 - \cos\theta)} - \frac{1}{4}$$

$$H_{02} = \frac{\theta^2}{4} \frac{(3 - 4\cos\theta)}{(1 - \cos\theta)} - \frac{\theta}{2} \frac{\sin\theta}{(1 - \cos\theta)}$$

$$H_{01} = -\frac{\theta^3}{2} \frac{\sin\theta}{(1 - \cos\theta)} + \frac{\theta^2}{4}$$

$$H_{00} = \frac{\theta^4}{4} \frac{3 - 4\cos\theta}{(1 - \cos\theta)}$$

and δ is the separation angle between the pole pairs and the center notch frequency. For $\delta = 0$, the two pairs of single poles collapse into a double pole.

Bibliography

[1] Milton Abramowitz and Irene A. Stegun. *Handbook of Mathematical Functions.* Number 0–486–61272–4. Dover Publicatons, 1974.

[2] Sasan H. Ardalan and John J. Paulos. An analysis of nonlinear behavior in delta–sigma modulators. *IEEE Transactions on Circuits and Systems*, CAS–34:593–603, June 1987.

[3] Simona Brigati et al. Modeling sigma–delta modulator non–idealities in SIMULINK®. In *Proceedings of the IEEE International Symposium on Circuits and Systems 1999, ISCAS '99*, pages 384–387, May 1999.

[4] Mark Burns and Gordon W. Roberts. *An Introduction to Mixed–Signal IC Test and Measurement.* Number 0–19–514016–8. Oxford University Press, 2001.

[5] James A. Cherry. *Theory, Practice, and Fundamental Performance Limits of High–Speed Data Conversion using Continuous–Time Delta–Sigma Modulators.* PhD thesis, Carleton University, Ottawa, Canada, 1998.

[6] James A. Cherry and W. Martin Snelgrove. Excess Loop Delay in Continuous–Time Delta–Sigma Modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(4):376–389, April 1999.

[7] J. Alvin Connelly and Pyung Choi. *Macromodeling with SPICE.* Number 0-13-544941-3. Prentice Hall, 1992.

[8] A. E. Cosand, Joseph F. Jensen, H. C. Sun, and C. H. Fields. IF–Sampling Fourth–Order Bandpass $\Delta\Sigma$ Modulator for Digital Receiver Applications. *IEEE Journal of Solid–State Circuits*, 39(10):1633–1639, October 2004.

[9] Cassius C. Cutler. Transmission system employing quantization. U.S. Patent No. 2,927,962, March 1960.

[10] Thomas A. DeMassa and Zack Ciccone. *Digital Integrated Circuits.* Number 0–471–10805–7. John Wiley and Sons, 1996.

[11] Y. Ding and R. Harjani. A High–Efficiency CMOS $+22dBm$ Linear Power Amplifier. *IEEE Journal of Solid–State Circuits*, 40(9):1895–1900, September 2005.

[12] Hans Joakim Dressler. Interpolative Bandpass A/D Conversion – Experimental Results. *IEE Electronics Letters*, 26(20):1652–1653, September 1990.

[13] Ronan Farrell and Orla Feely. Bounding the Integrator Outputs of Second–Order Sigma–Delta Modulators. *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, 45:691–702, June 1998.

[14] Dan Fitzpatrick and Ira Miller. *Analog Behavioral Modeling with the Verilog-A Language.* Number 0-7923-8044-4. Kluwer Academic Publishers, 1998.

[15] Weinan Gao, James A. Cherry, and W. Martin Snelgrove. A 4GHz Fourth–Order SiGe HBT Bandpass $\Delta\Sigma$ Modulator. In *Symposium on VLSI Circuits, 1998. Digest of Technical Papers*, pages 174–175, June 1998.

[16] Weinan Gao and W. Martin Snelgrove. A 950–MHz IF Second Order Integrated LC Bandpass Delta–Sigma Modulator. *IEEE Journal of Solid–State Circuits*, 33(5):723–732, May 1998.

[17] Barrie Gilbert. The Multi–tanh Principle: A Tutorial Overview. *IEEE Journal of Solid–State Circuits*, 33(1):2–17, January 1998.

[18] F. Henkel, U. Langmann, A. Hanke, S. Heinen, and E. Wagner. A 1–MHz–Bandwidth Second–Order Continuous–Time Quadrature Bandpass Sigma–Delta Modulator for Low–IF Radio Receivers. *IEEE Journal of Solid–State Circuits*, 37(12):1628–1635, December 2002.

[19] L. Hernandez and S. Paton. Continuous time sigma–delta modulators with transmission line resonators and improved jitter and excess loop delay performance. In *IEEE International Symposium on Circuits and Systems, ISCAS 2003*, pages 25–28, May 2003.

[20] D. H. Horrocks. A second–order oversampled sigma–delta modulator for bandpass signals. In *Proceedings of the IEEE International Symposium on Circuits and Systems 1991, ISCAS '91*, pages 1653–1656, June 1991.

[21] M. Hotta, K. Maio, N. Yokozawaand T. Watanabe, and S. Ueda. A 150–mW, 8–Bit Video–Frequency A/D Converter. *IEEE Journal of Solid–State Circuits*, 21(2):318–323, April 1986.

[22] M. Iwamoto, A. Jayaraman, G. Hanington, P.F. Chen, A. Bellora, W. Thornton, L.E. Larson, and P.M. Asbeck. Bandpass delta–sigma class–S amplifier. *IEE Electronics Letters*, 36:1010–1012, June 2000.

[23] S.A. Jantzi, R. Schreier, and W.M. Snelgrove. A bandpass $\Delta\Sigma$ A/D convertor for a digital AM receiver. In *Proceedings of the International Conference on Analogue to Digital and Digital to Analogue Conversion*, pages 75–80, September 1991.

[24] S.A. Jantzi, R. Schreier, and W.M. Snelgrove. Bandpass sigma–delta analog–to–digital conversion. *IEEE Transactions on Circuits and Systems*, 38(11):1406–1409, November 1991.

[25] S.A. Jantzi, W.M. Snelgrove, and P.F. Ferguson. A Fourth–Order Bandpass Sigma–Delta Modulator. In *Proceedings of the IEEE Custom Integrated Circuits Conference*, pages 16.5.1–16.5.4, May 1992.

[26] A. Jayaraman, P. Asbeck, S. Beccue, Keh Chung Wang, and K. Nary. Bandpass Delta–Sigma Modulator with 800 MHz Center Frequency. In *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1997*, pages 15–17, October 1997.

[27] David A. Johns and Ken Martin. *Analog Integrated Circuit Design.* Number 0–471–14448–7. John Wiley and Sons, 1997.

[28] Thomas Johnson, Robert Sobot, and Shawn Stapleton. CMOS RF Class D Amplifier with a Fractional Sigma–Delta Bandpass Modulator. *IEEE Transactions on Circuits and Systems–II.* (submitted for publication).

[29] Eliahu Ibrahim Jury. *Theory and Application of the z–transform method.* Number 64–17145. John Wiley and Sons, 1964.

[30] Jaime E. Kardontchik. *Introduction to the Design of Transconductor–Capacitor Filters.* Number 0–7923–9195–0. Kluwer Academic Publishers, 1992.

[31] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck. Digital Generation of RF Signals for Wireless Communications With Band–Pass Delta–Sigma Modulation. In *Microwave Symposium Digest, 2001 IEEE MTT-S International*, volume 3, pages 2127–2130, May 2001.

[32] Benjamin C. Kuo. *Digital Control Systems.* Number 0–03–012884–6. Saunders College Publlishing, 1992.

[33] Hae-Seung Lee and John F. Bulzhacelli. Bandpass Sigma–Delta Modulator Employing High–Q Resonator for Narrowband Noise Suppression. U.S. Patent No. 6,157,329, December 2000.

[34] W. L. Lee. A novel higher order interpolative modulator topology for high resolution oversampling A/D converters. Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, USA, 1987.

[35] Roberto Maurino and Peter Mole. A 200–MHz IF 11–bit Fourth–Order Bandpass $\Delta\Sigma$ ADC in SiGe. *IEEE Journal of Solid–State Circuits*, 35(7):959–967, July 2000.

[36] Steven Norsworthy, Richard Schreier, and Gabor Temes. *Delta–Sigma Data Convertors: Theory, Design and Simulation.* Number 0–7803–1045–4. IEEE Press, 1997.

[37] Alan V. Oppenhiem and Ronald W. Schafer. *Digital–Time Signal Processing.* Number 0–13–754920–2. Prentice Hall, 1999.

[38] Frederick H. Raab. Radio Frequency Pulsewidth Modulation. *IEEE Transactions on Communications*, 21:958–966, August 1973.

[39] Shahriar Rabii and Bruce A. Wooley. *The Design of Low–Voltage, Low–Power Sigma–Delta Modulators.* Number 0–792–38361–3. Kluwer Academic Publishers, 1999.

[40] Gopal Raghavan, Joseph F. Jensen, J. Laskowski, M. Kardos, M. G. Case, M. Sokolich, and S. Thomas III. Architecture, Design, and Test of Continuous–Time Tunable Intermediate–Frequency Bandpass Delta–Sigma Modulators. *IEEE Journal of Solid–State Circuits*, 36(1):5–13, January 2001.

[41] Gopal Raghavan, Joseph F. Jensen, Robert H. Walden, and William P. Possey. A Bandpass $\Sigma\Delta$ Modulator with 92dB SNR and Center Frequency Continuously Programmable from 0 to 70MHz. *IEEE International Solid–State Circuits Conference*, pages 214–215, February 1997.

[42] Lars Risbo. Σ–Δ *Modulators – Stability Analysis and Optimization.* PhD thesis, Technical University of Denmark, Lyngby, Denmark, 1994.

[43] Gordon W. Roberts and Vincent W. Leung. *Design and Analysis of Integrator–Based Log–Domain Filter Circuits.* Number 0–7923–8699–X. Kluwer Academic Publishers, 2000.

[44] Gordon W. Roberts and Albert K. Lu. *Analog Signal Generation for Built–in–Test of Mixed–Signal Integrated Circuits.* Number 0–7923–9564–6. Kluwer Academic Publishers, 1995.

[45] Gordon W. Roberts and Adel S. Sedra. *SPICE.* Number 0–19–510842–6. Oxford University Press, 1997.

[46] Richard Schreier, Jennifer Lloyd, Lawrence Singer, Donald Paterson, Michael Timko, Michael Hensley, Gregory Patterson, Kevin Behel, James Zhou, and William J. Martin. A 50 mW Bandpass $\Sigma\Delta$ ADC With 333 kHz BW and 90dB DR. *IEEE International Solid–State Circuits Conference, ISSCC 2002*, 1:216–217, April 2002.

[47] Richard Schreier and Martin Snelgrove. Bandpass Sigma–Delta Modulaiton. *IEE Electronics Letters*, 25(23):1560–1561, November 89.

[48] Omid Shoaei. *Continuous–Time Delta–Sigma A/D Converters for High Speed Applications.* PhD thesis, Carleton University, Ottawa, Canada, 1995.

[49] Omid Shoaei and W. Martin Snelgrove. Design and Implementation of a Tunable 40MHz–70MHz Gm–C Bandpass $\Delta\Sigma$ Modulator. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 44(7):521–530, July 1997.

[50] Robert Sobot, Shawn Stapleton, and Marek Syrzycki. Tunable Continuous Time Bandpass Sigma–Delta Modulators with Fractional Delays. *IEEE Transactions on Circuits and Systems–I.* (accepted for publication).

[51] Robert Sobot, Shawn Stapleton, and Marek Syrzycki. Behavioral modeling of continuous time $\Delta\Sigma$ modulators. In *Proceedings 2003 IEEE International Workshop on Behavioral Modeling and Simulation, BMAS 2003*, volume 1, pages 88–91, October 2003.

[52] Robert Sobot, Shawn Stapleton, and Marek Syrzycki. Tunable Center Frequency Continuous Time Bandpass $\Delta\Sigma$ Modulators for Wireless Transceivers. In *Proceedings IEEE Vehicular Technology Conference 2004–Fall, VTC2004–Fall*, volume 7, pages 4956–4960, September 2004.

[53] Robert Sobot, Shawn Stapleton, and Marek Syrzycki. A Fractional Delay $\Sigma\Delta$ Upconverter. *IEE Electronics Letters*, November 2005.

[54] Hai Tao and John M. Khoury. A 400–Ms/s Frequency Translating Bandpass Sigma–Delta Modulator. *IEEE Journal of Solid–State Circuits*, 34(12):1741–1752, December 1999.

[55] A.M. Thurston, M.J. Hawksford, and T.H. Pearce. Bandpass Implementation of the Sigma–Delta A–D Conversion Technique. In *International Conference on Analogue to Digital and Digital to Analogue Conversion, 1991.*, pages 81–86, September 1991.

[56] Gerhard Troster, H.J. Dressler, J. Arndt, H.J. Golberg, W. Schardein, K. Schopp, P. Sieber, A. Wedel, and E. Zocher. An Interpolative Bandpass Converter on a $1.2\mu m$ BiCMOS Analog/Digital Array. In *Symposium on VLSI Circuits, 1992. Digest of Technical Papers*, pages 102–103, June 1992.

[57] Jurgen A. E. P. van Engelen, Rudy J. van de Plassche, Eduard Stikvoort, and Ardie G. Venes. A Sixth–Order Continuous Time Bandpass Sigma–Delta Modulator for Digital Radio IF. *IEEE Journal of Solid–State Circuits*, 34(12):1753–1764, December 1999.

[58] M. Vogels, B. De Smedt, and G. Gielen. Modeling and simulation of a Sigma–Delta digital to analog converter using VHDL–AMS. In *Proceedings 2000 IEEE/ACM International Workshop on Behavioral Modeling and Simulation, BMAS 2000*, pages 5–9, 2000.