SoC Prototyping and Validating during DSM CMOS Technology Transfer

by

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Abstract

This report lays out the importance in different technology used from one wafer process foundation to another. Depending on the process technologies they use, processed devices can have varying performance and characteristics. The HSPICE BSIM3 model is used to analyze IV characteristics of N/PMOS transistors based on both FAB1 and FAB2 technology files. Sub-threshold current has also been simulated. Simple five stage inverters as well as ring oscillator with 100nm length and 200nm width transistors are created to simulate and analyze the performance variations. The analysis consists of delay associated with parasitic capacitance parameters from both foundries. Lastly, a simple model, consisting of series of inverters and resistors, is created to simulate effect of power distribution.

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Definitions

CMOS	Chemical Metal Oxide Substrate
DIBL	Drain-Induced Barrier Lowering effect
DSM	Deep Sub-Micron
FAB	Fabrication Foundry
HSPICE	The Golden Standard for Accurate Circuit Simulation
I_D	Drain Current
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
SoC	System On Chip
V_{GS}	Gate to Source Voltage
V_{TH}	Threshold Voltage

Chapter 1. Introduction

1.1 General

This thesis is concentrated on feasibility comparison of the technology between two silicon fabrication foundries, also called FABs. Fabricating technologies of both FABs are implementing processes of 0.18μm single poly two-metal layer with 95%Al/~5%Cu and salicided poly-silicon. Even with same technology levels, each FAB can produce rather different products with the same layout designs. For proprietary protection reasons, these FABs will be identified in this thesis as FAB1 and FAB2. The FAB1 is PMC's original fabrication foundry while FAB2 is fabrication foundry to which the design technology is being transferred to for reduced process costs. Since both foundries have their own budgets for purchasing equipments and developed their own processing steps, they have slightly different 0.18μm process capacities and technologies.

Both foundries are fully capable of fabricating 0.18μm devices, but what are the tradeoffs in IC quality and cost? This question can be answered rather quickly when you start looking at the simulation results of different process technologies being used for wafer fabrication. The different process technologies give each foundry its own capacity and characteristics. However, would each foundry be able to support and process a layout for PMC's designed requirements for a mature 0.18μm technology? This thesis will contain analysis of two fabrication foundries based on the simulation result with their process technology files.

This chapter contains an introduction to what is involved in design technology transfer between foundries. Subsequent chapters elaborate on these topics in further detail. The last section of this chapter contains an outline summary of each chapter.

1.2 Background

Today, a fabless model for semiconductor chipmakers is one of the most successful business methodologies being used in semiconductor companies. The advantage of these fabless companies is that they can concentrate their resources in device design and characterization, while fabrication companies like FAB1 and FAB2 can concentrate on process technology developments.

In order to ensure the fabrication processes are properly qualified to certain standards, characterization of the processed devices is required. This step is necessary to guarantee the function and performance of fabricated devices for different foundries at given technology nodes.

PMC-Sierra (PMC) is one of the companies that utilize the fabless model. After the recent economic downturn, high tech companies have gone through hardship due to the market depression. Therefore, it became imperative for PMC to reduce costs in order to remain competitive in the market. By switching to another fabrication foundry, PMC enjoys a large cost saving in wafer fabrication for a mature process technology like 0.18μm process. However, one must keep in mind such factors as time of delivery, setup cost, and yield from the wafer. If any one factor is compromised, then it is possible that such foundry transfer might not give enough cost savings.

To ensure the characteristics of the devices processed from both foundries were the same, the simulation based on HSPICE (version U-2003.09 from Synopsys Inc. under SUN Solaris 5.8 system) has been conducted. The HSPICE software is using BSIM3 model library files. Also, parasitic technology parameters for both foundries in 0.18μm technology are used. From the seven-metal, single poly process technology, this thesis restricts itself to only a single poly with two-metal layer analysis to conduct the basic simulation and simplify the analysis of the data plus comparisons of the FABs. 0.18μm technology has been developed for

many years and is at mature stage of the development cycle. This is the reason 0.18μm technology is chosen for the transfer.

All the resources and manufacturer's technology files are provided by PMC-Sierra. The details of technology files from FAB1 and FAB2 cannot be revealed due to proprietary nature of the information. PMC-Sierra has signed Non-Disclosure Agreements concerning the details of these files. Hence, the following process details are based on those technology files and full details cannot be revealed.

That being said, for proprietary reasons this report is based solely on results from the simulations. The simulation is based on parasitic parametric values provided from FAB1 and FAB2 technology libraries. The analysis is done based on the simulation which was conducted with basic transistor, inverter, five stage inverters, and five stage ring oscillators with 100nm length and 200nm width for both NMOS and PMOS. Also, other possible effects like cross talk and power grid resistance, which can cause unfavorable performance issues, is reviewed and analyzed. These are the basic and most common test structure that allows unbiased performance comparisons from both FABs.

The impact on either analog or digital circuits will be reviewed and analyzed. Some of the results only affect analog circuits while some others only affect digital circuits. Also, the report will start with smaller and simpler (transistor level) circuits then move on to higher-level general-purpose circuits like power grid resistance effects and cross-talk effects.

1.3 Thesis Outline

In chapter 2 the transistor model simulations are first conducted to compare the I-V characteristics of the transistors. Then the threshold voltage effects of the devices from each FAB are compared.

Chapter 3 presents the device level simulation based on simple inverter, five-stage inverter chain, and five-stage ring oscillator. The analysis is mostly based on the voltage characteristics as well as propagation delay of the input signal. Results from each FAB are analyzed and compared.

Chapter 4 examines a couple of possible issues at the top level. This section includes possible cross talk issues within the device that may affect other signal lines. Also, the power supply grid resistance effect is reviewed to analyze possible power degradation throughout the device.

Chapter 5 presents this project with the conclusion of the analysis.

Chapter 2. Analysis of Transistor Level HSPICE Simulation Results

This chapter provides transistor level simulation results like I-V and transconductance characteristics of 0.18μm N/PMOS transistors. The HSPICE simulation is based on 0.18μm process technology library files obtained from both FAB1 and FAB2. The simulation uses BSIM3 model library files. For convenience, the length of the transistors is set to 180nm for both N and P channel transistors and the width of the transistors is set to 720nm for both N and P channel for I-V Characteristics. This size is used to compare equal size N and P channel transistors. The sub-threshold current simulation is conducted with the length of 180nm for both N and P channel, and the width of 1800nm for P channel and 720nm for N channel transistors. P channel transistor width is greater then N channel transistor to incorporate slower P channel transistor due to slower electron drift velocity. Larger then minimum transistor width is used to increase amount of current drive strength.

2.1 I-V Characteristics

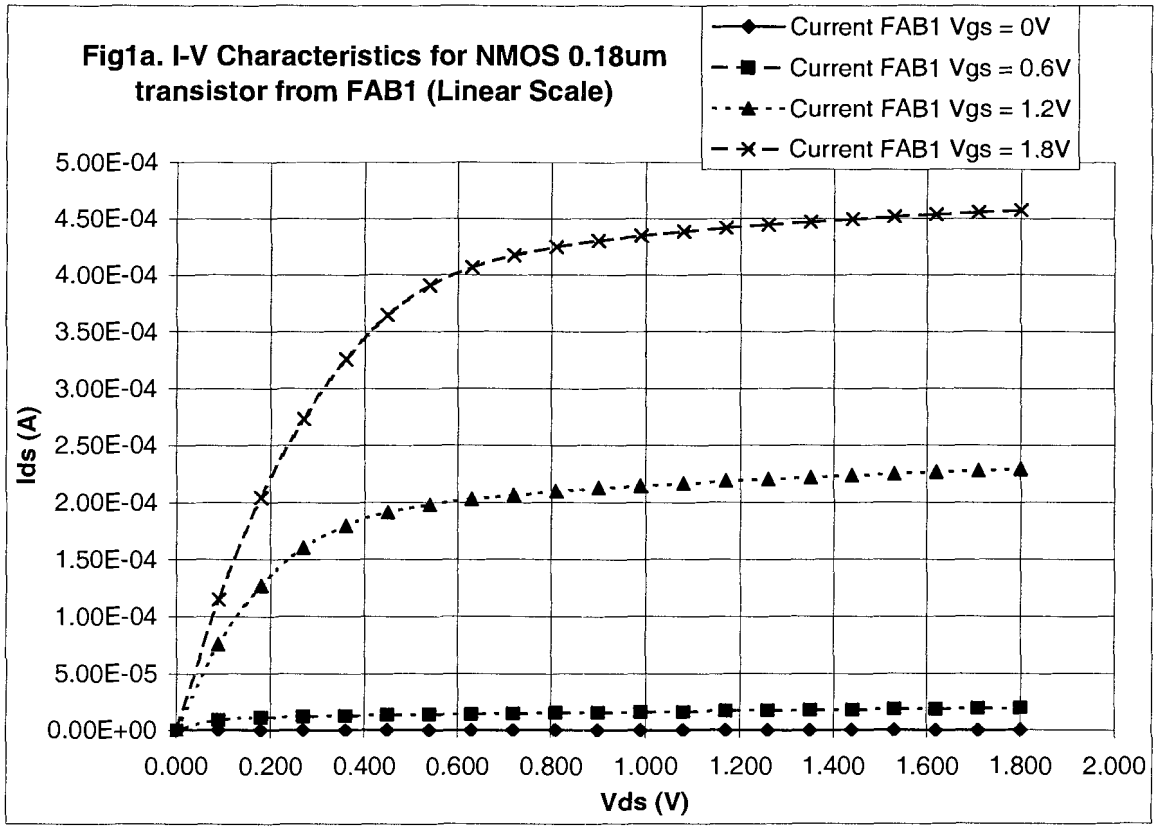
I-V characteristics of FAB1 and FAB2 for the NMOS transistor model with varying gate to source voltage, V_{GS}, are shown in Figure 1. The characteristics for the PMOS transistor model with varying gate to source voltage, V_{GS}, are shown in Figure 2. V_{GS} values used for each curve are V_{GS} = 0V, 0.6V, 1.2V, and 1.8V respectively along the voltage-axis (or x-axis). These characteristics show threshold voltage, V_{TH}, values to be roughly 0mV, 100mV, 350mV, and 650mV respectively.

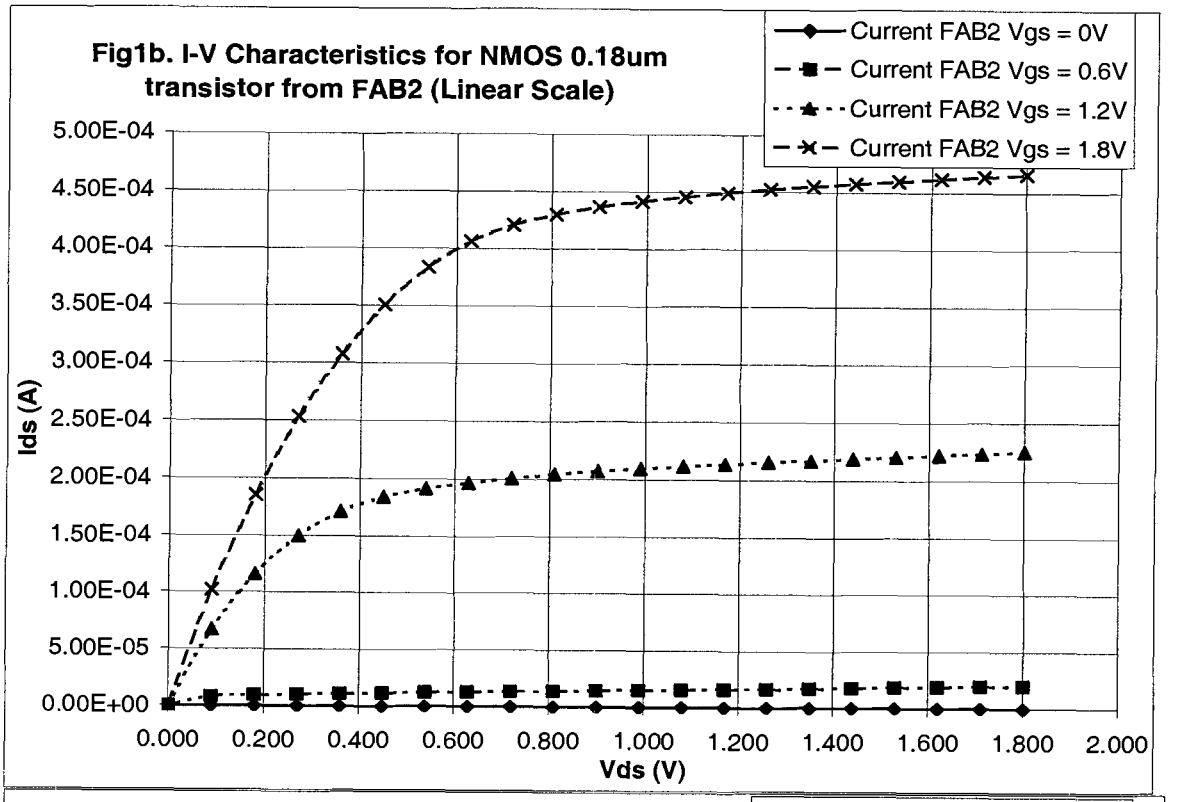
Curves where V_{GS} = 0V, 0.6V, and 1.2V show almost the same V_{TH} characteristic values for both FABs while V_{GS} = 1.8V shows differences in their measurements. FAB1's NMOS transistor shows V_{TH} of ~600mV while FAB2's shows V_{TH} of ~700mV. PMOS transistor, however, shows V_{TH} of ~810mV from FAB1 and

~720mV from FAB2, with FAB2 devices having higher I_{DS} values. Also, these graphs show that FAB1 NMOS transistors reach the saturation region faster than FAB2 NMOS transistors and the other way around for PMOS transistors. This could be the result of channel length modulation[5]. This effect can be derived from the length of the transistor's channel since it is inversely proportional to the length of the transistor. At the same time, the thickness of the poly-silicon would cause a similar effect due to decreased electrical field applied to the channel[1].

The graphs in Figures 1 and 2 also show the difference in slope for the triode region from both FABs between V_{DS} of 0V to ~800mV. At full operating voltage of 1.8V the FAB1 NMOS transistor's triode region slope is greater than that of the FAB2 NMOS transistor. The PMOS transistor, however, shows that the slope of FAB2 is greater then FAB1 for the triode regions. This result indicates potential degraded performance for both analog and digital circuitry.

Figure 1 I-V (I_{DS} vs V_{DS}) Characteristics for minimum geometric 0.18µm NMOS transistors (Linear scale)





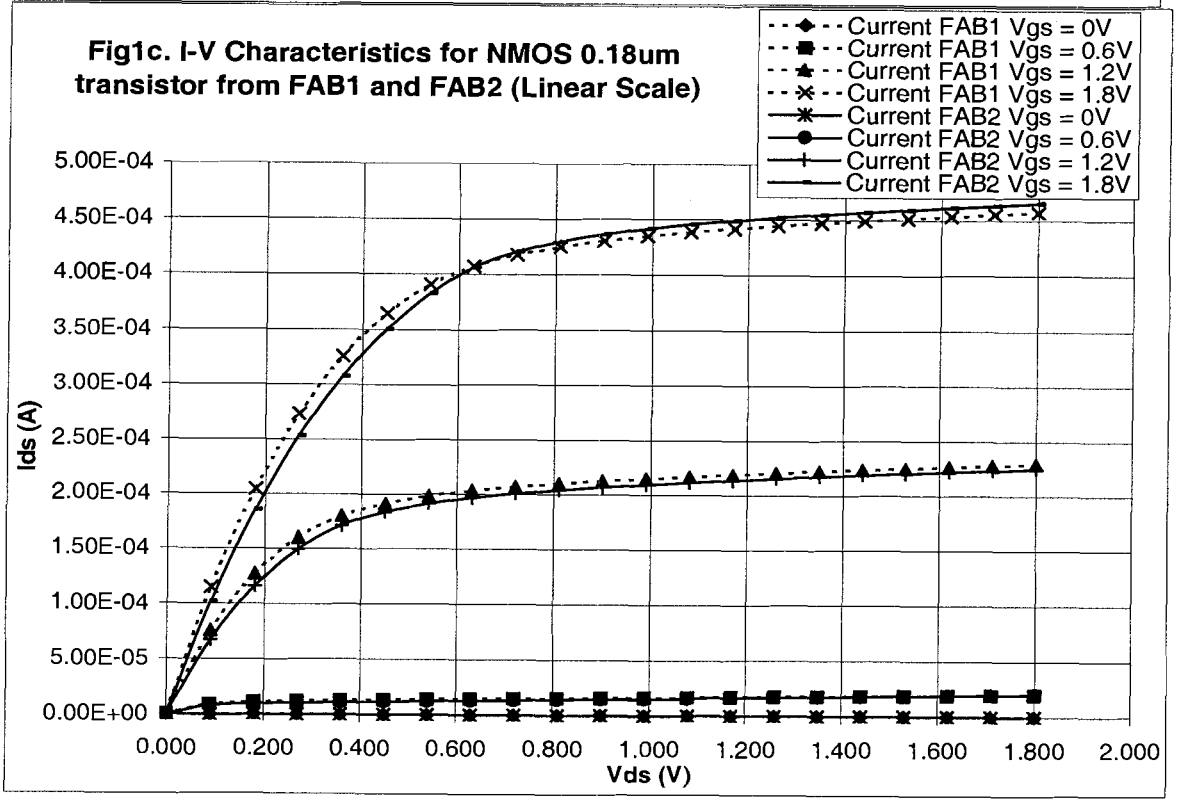
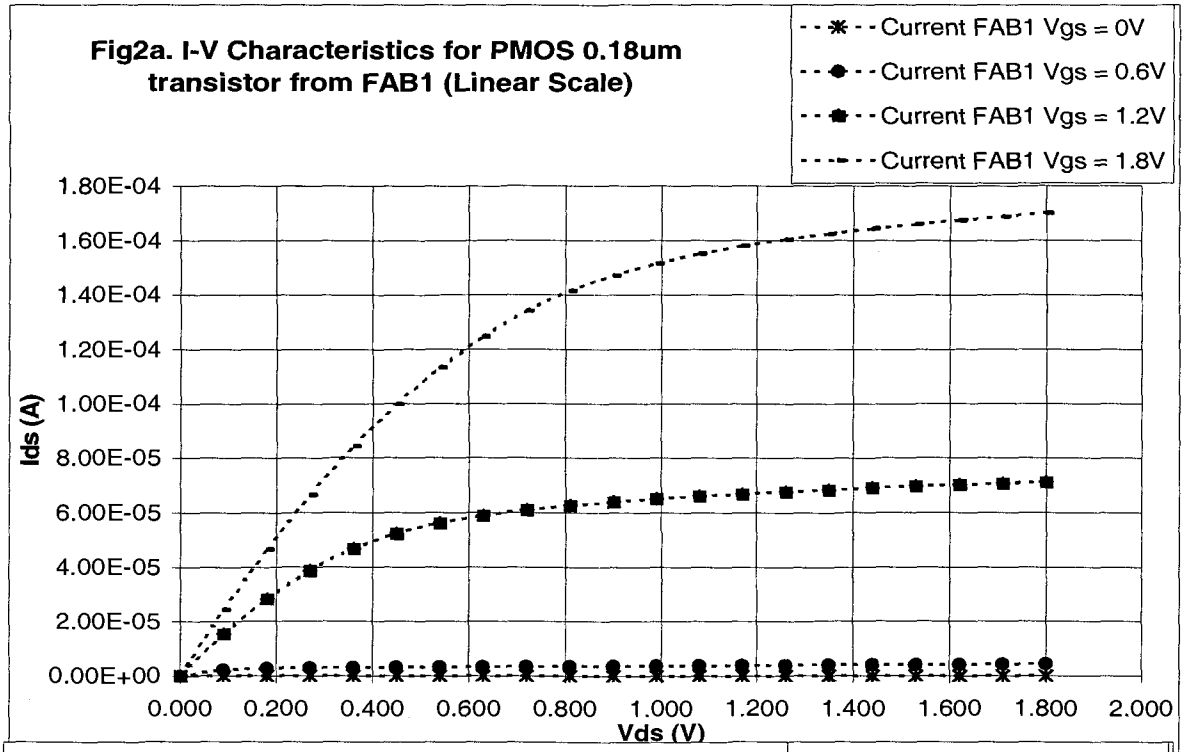
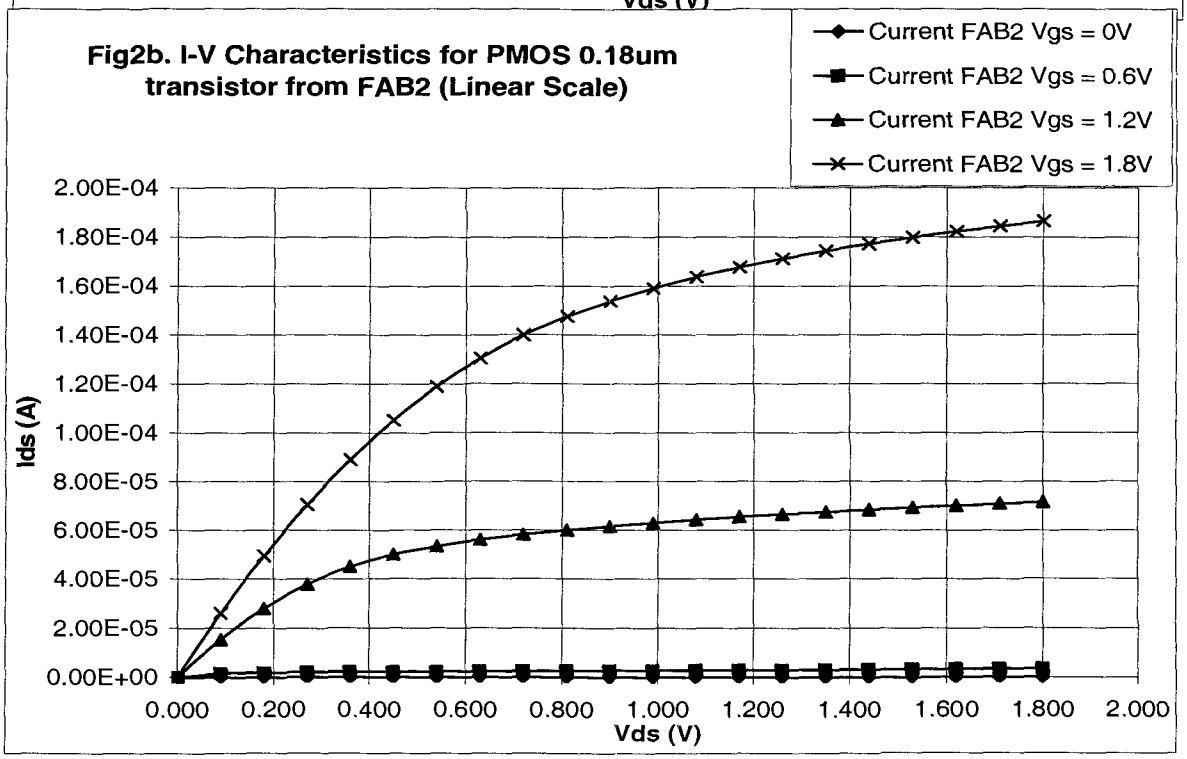


Figure 1 (Continue)

Figure 2 I-V (I_{DS} vs V_{DS}) Characteristics for minimum geometric 0.18µm PMOS transistors (Linear scale)





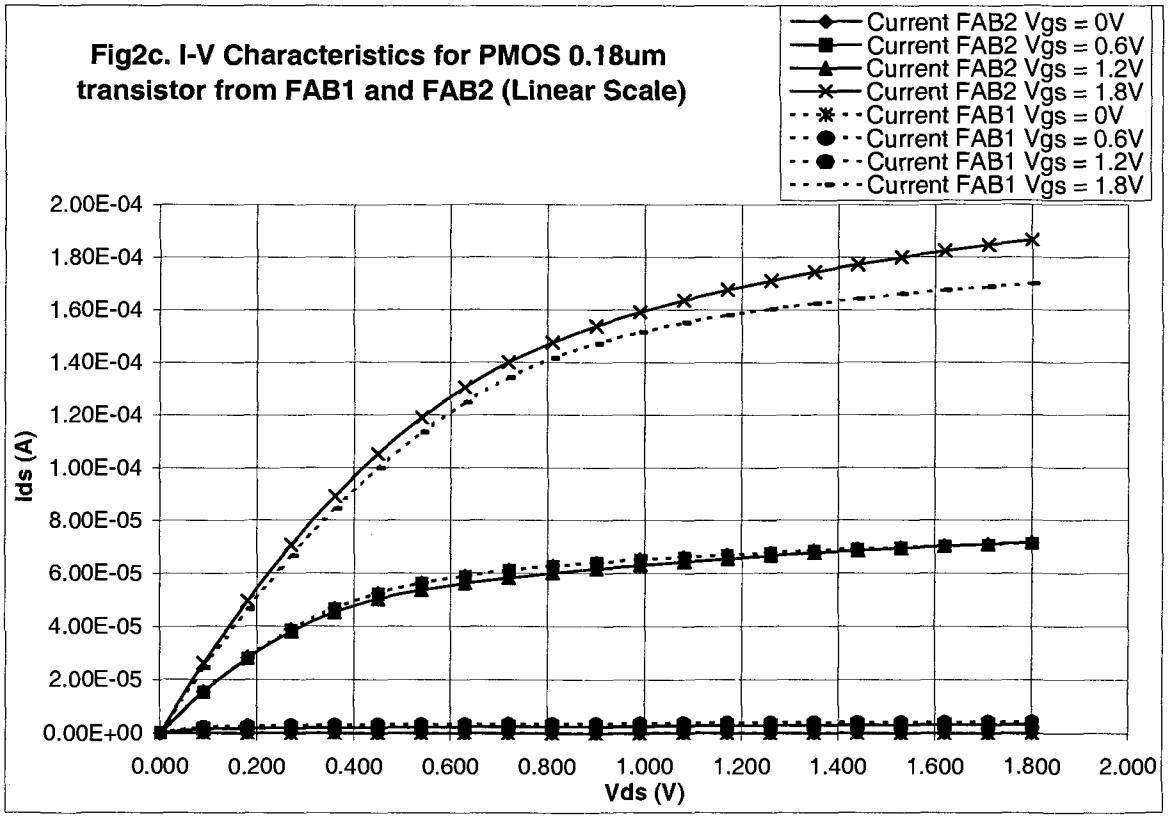


Figure 2 (Continue)

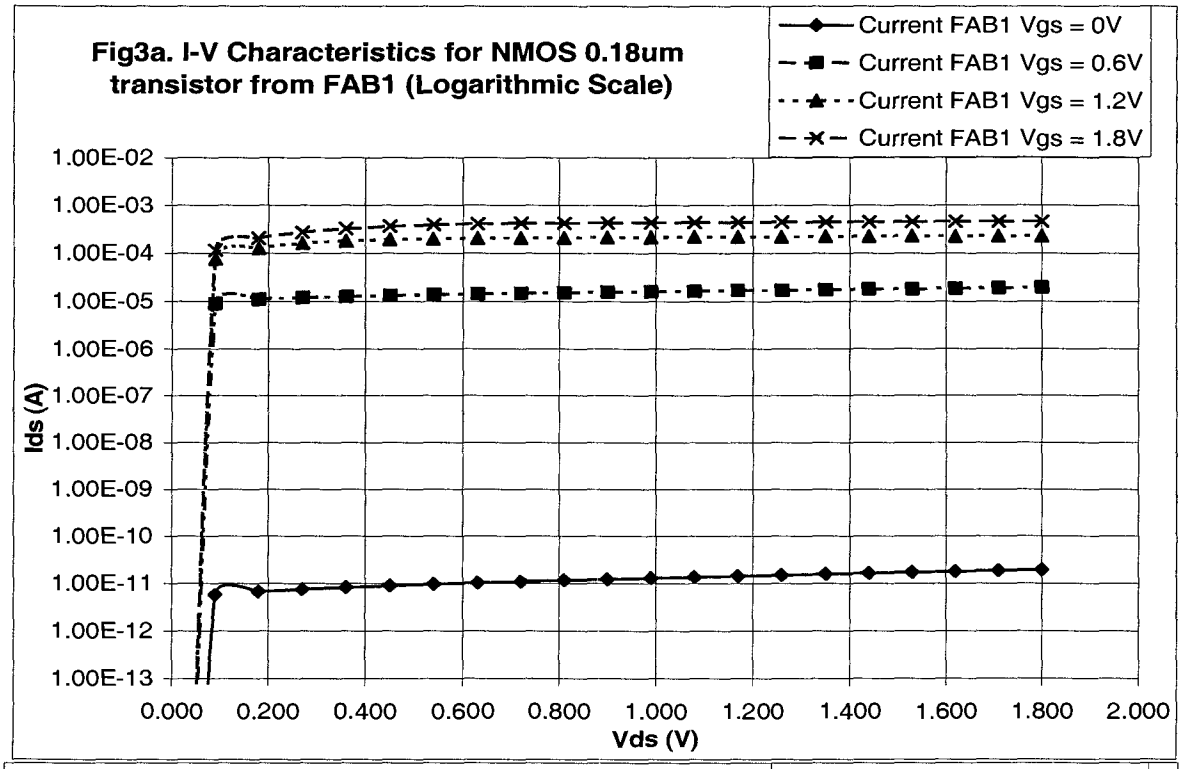
Since the slopes of triode region for the FAB2 devices are smaller for NMOS, the analog circuits will operate slower than the FAB1 devices for N-channel signals. The opposite would happen for PMOS transistors since the slope of FAB2 triode region is greater then FAB1. Also, now we have slightly mismatched N and P channel signals for FAB1 devices and this can cause an increased rise/fall time of the signals. This skew can potentially lower the performance of the high-speed differential signals by generated skew and degraded data-eye. FAB2 devices, however, have closely matched N and P channel transistors. This will help FAB2 devices' analog signal to have better rise and fall time as well as cleaner data-eye.

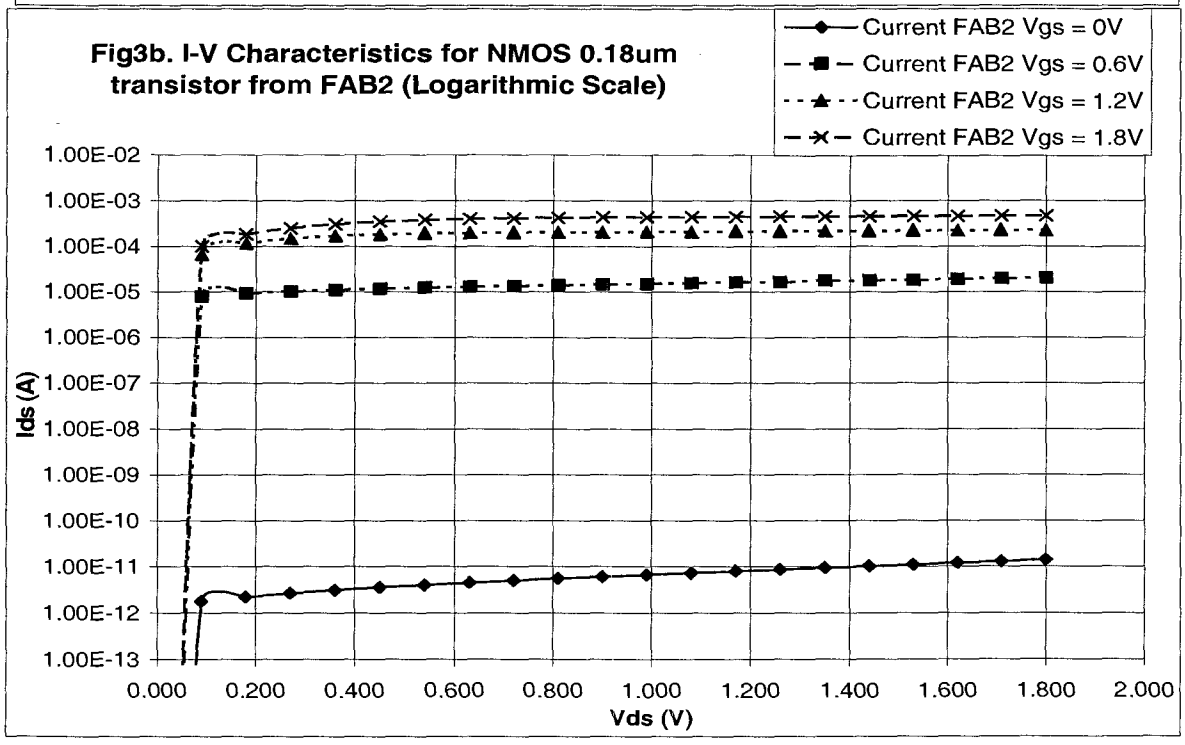
N and P transistor skew from FAB1 can also cause problems for digital circuitry. The bigger N and P skew also means longer "undefined" regions in the digital signal domain[3]. Think about a simple standard inverter for example: The output

voltage will stay "unknown" for an input voltage of 600mV to 810mV for FAB1 devices and 700mV to 720mV for FAB2 devices because between these two values V_{THN} will reach the threshold while V_{THP} will not. There is an undefined region gap of 210mV for FAB1 devices and 20mV for FAB2 devices. Therefore, both N and P channel transistors would stay "on" or "off" at the same time causing the output to be "unknown." As the "unknown" region becomes longer, the circuit downstream will need longer setup and hold time to recognize the data. As a result, the digital circuits will have to operate at lower frequency in order to operate without any errors. Comparing the digital circuits from the two FABs, FAB2 digital circuits will be capable of running at higher frequency due to lesser N and P process skew.

Another implication of this "unknown" stage is that there will be a short from V_{DD} to the ground causing sudden high current draw. Based on this, FAB1 devices will have higher current consumption compared to FAB2 devices for signals with higher transition density. This will be checked in Chapter 3.

Figure 3 I-V (I_{DS} vs V_{DS}) Characteristics for minimum geometric 0.18µm NMOS transistors (Logarithmic scale)





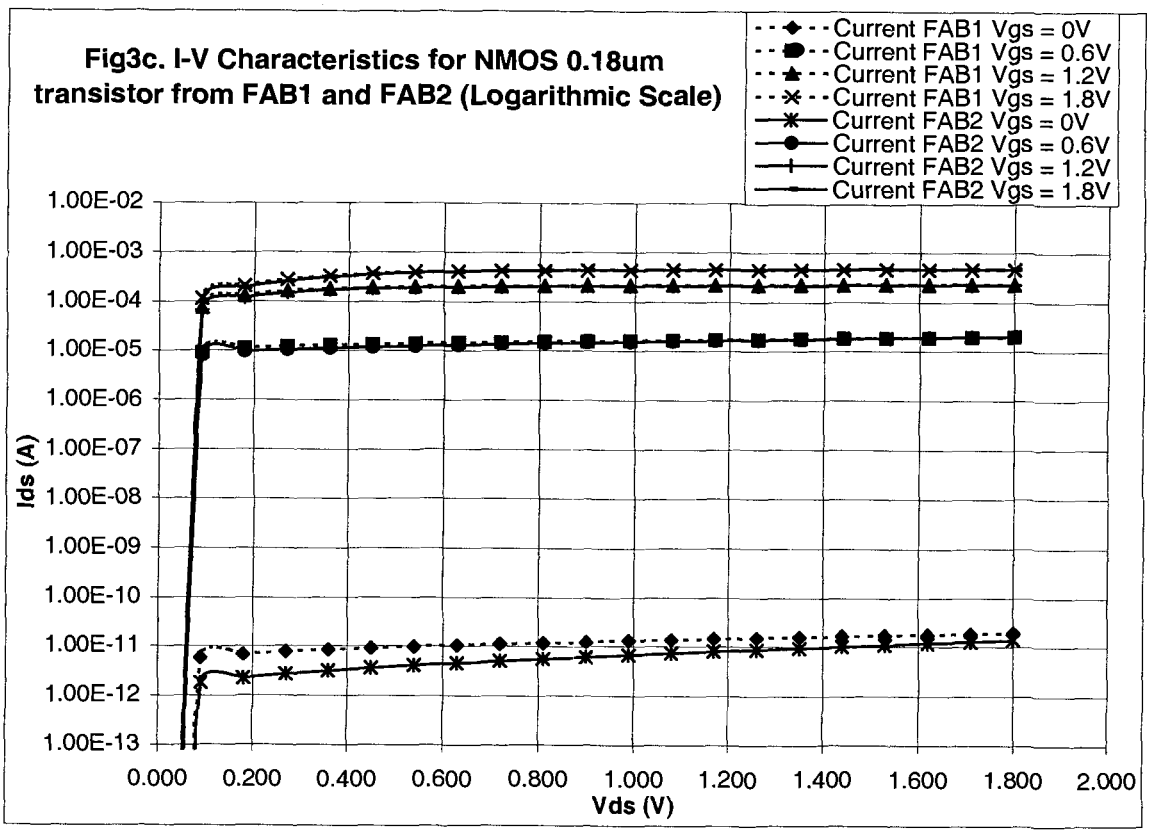
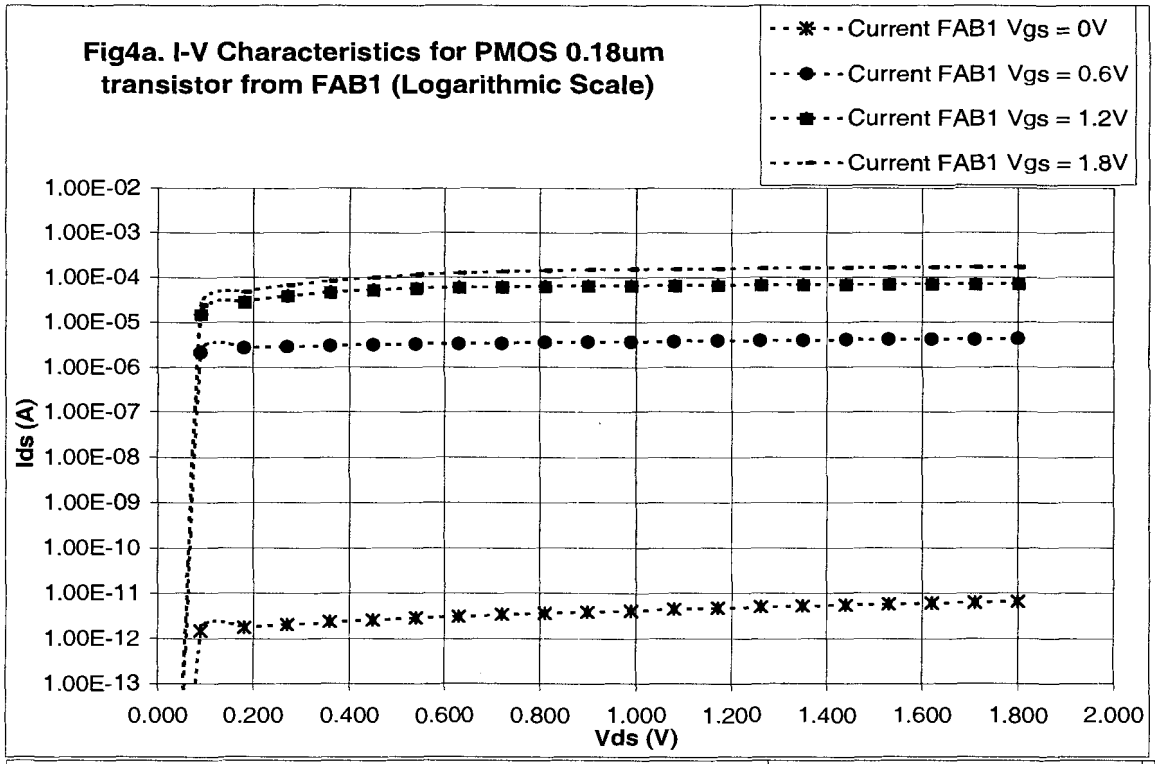
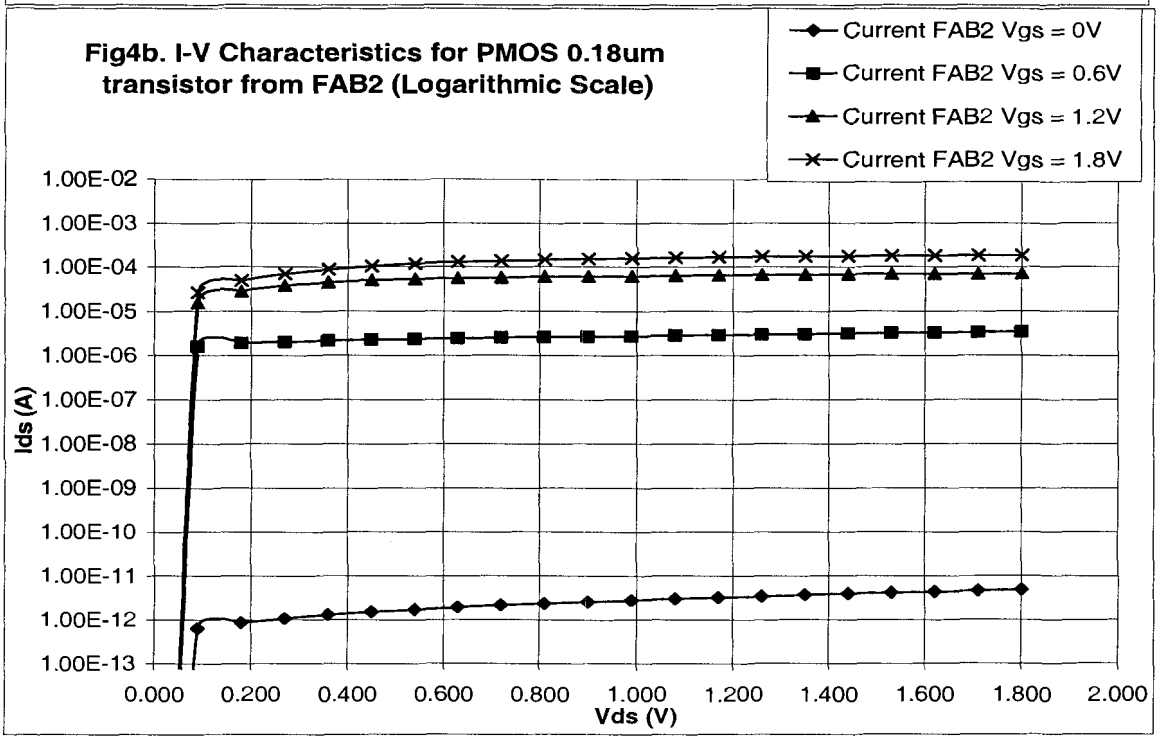


Figure 3 (Continue)

Figure 3 and Figure 4 are the same type of graph as in Figure 1 and Figure 2 but with the I_{DS} axis (y-axis) in a logarithmic scale. These two graphs highlight how saturation regional and triode regional slopes are similar for both FAB1 and FAB2 devices. The current measurements at saturated voltage are ~1pA for lower voltage setting, which is effectively a zero. The higher voltage setting, however, measured to be ~10uA to ~100uA. The current measurements of the devices from both FABs draw about the same amount of current in their transistor operations. Therefore, the power consumption on both FAB's devices would be the same.

Figure 4 I-V (I_{DS} vs V_{DS}) Characteristics for minimum geometric 0.18µm PMOS transistors (Logarithmic scale)





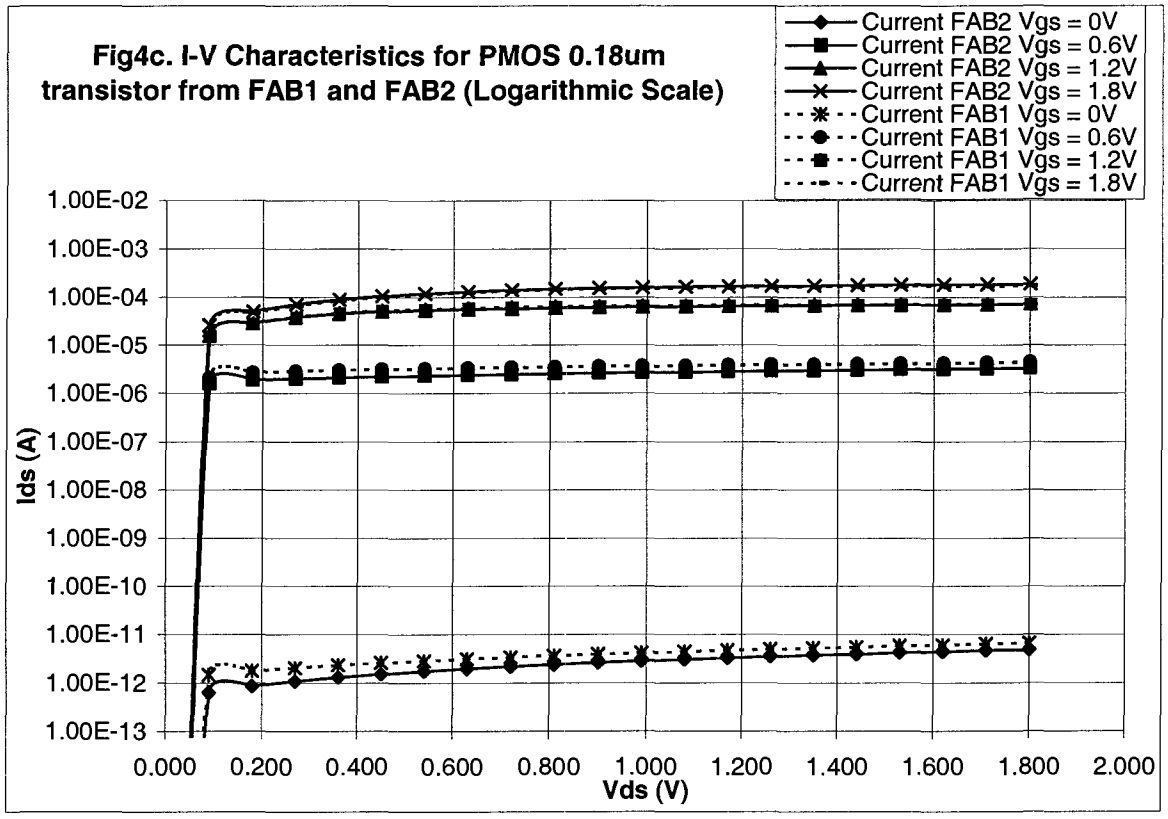
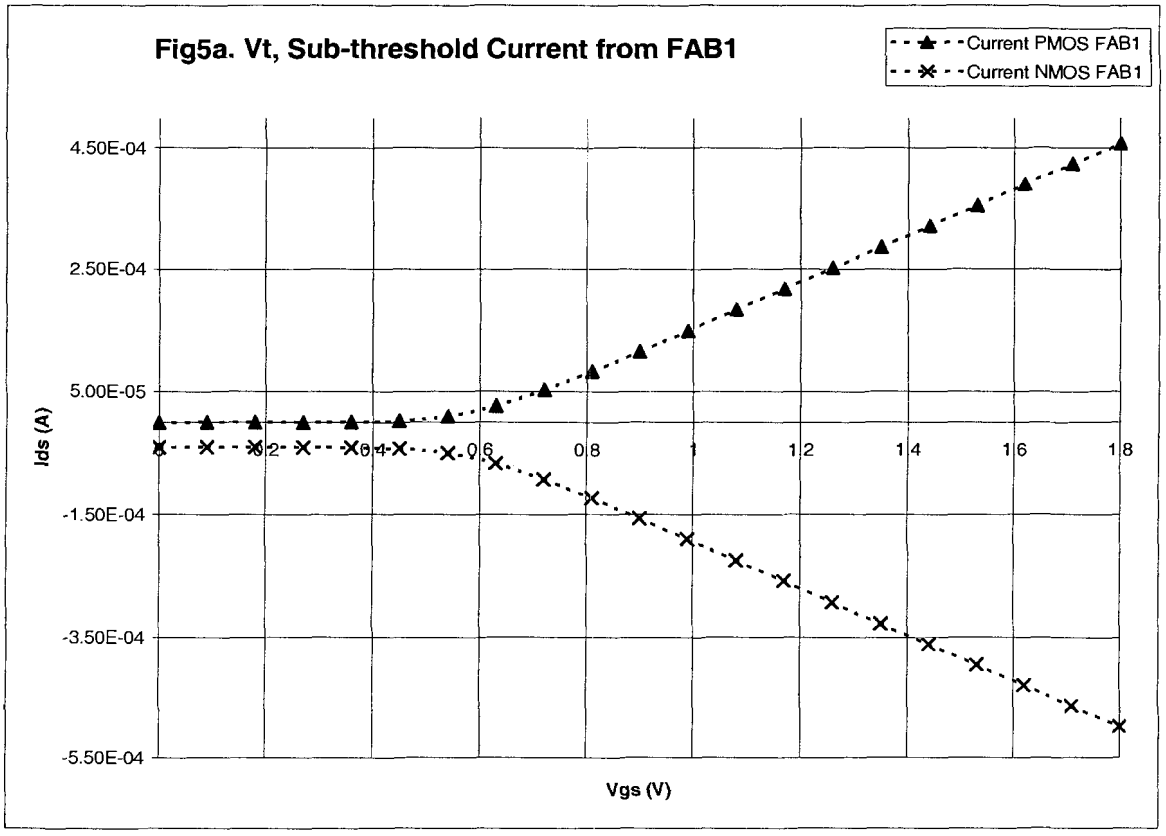


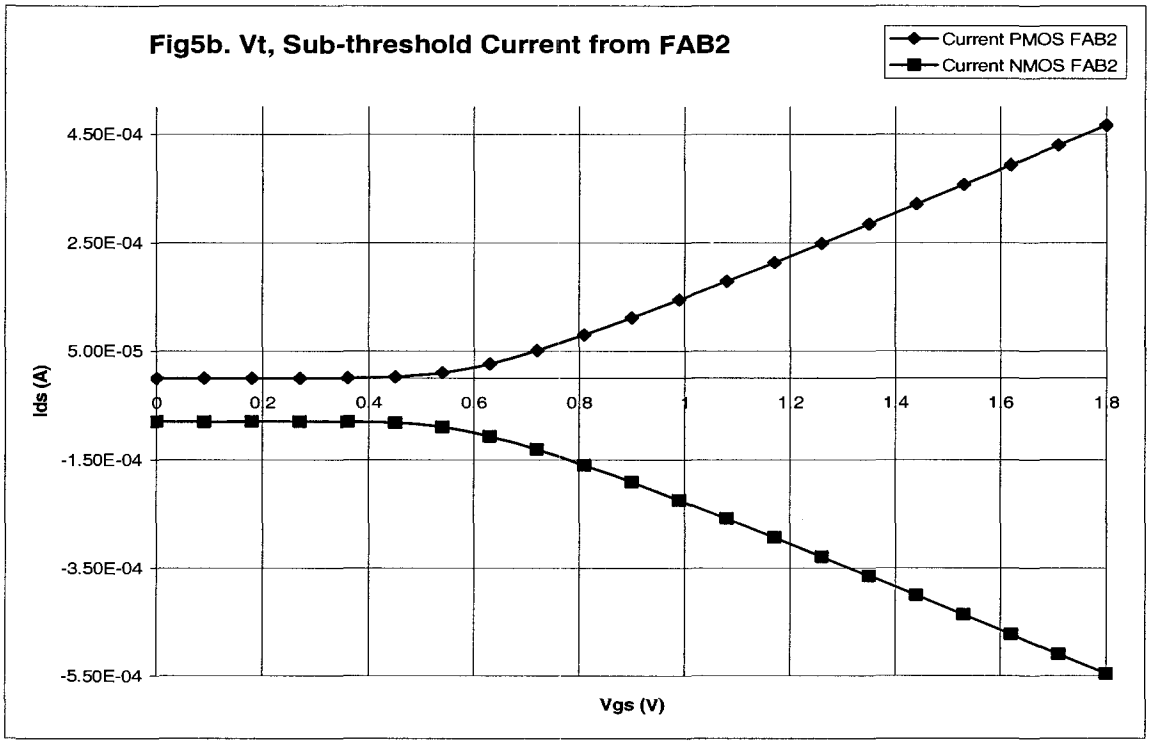
Figure 4 (Continue)

2.2 Transconductance Characteristics

Another important characteristic of a MOS transistor can be obtained by graphing I_{DS} vs V_{GS}, known as the transconductance characteristic[4]. Transconductance for FAB1 and FAB2 transistors' are shown in Figure 5.

Figure 5 Vt, Sub-threshold current (V_{GS} vs I_{DS})





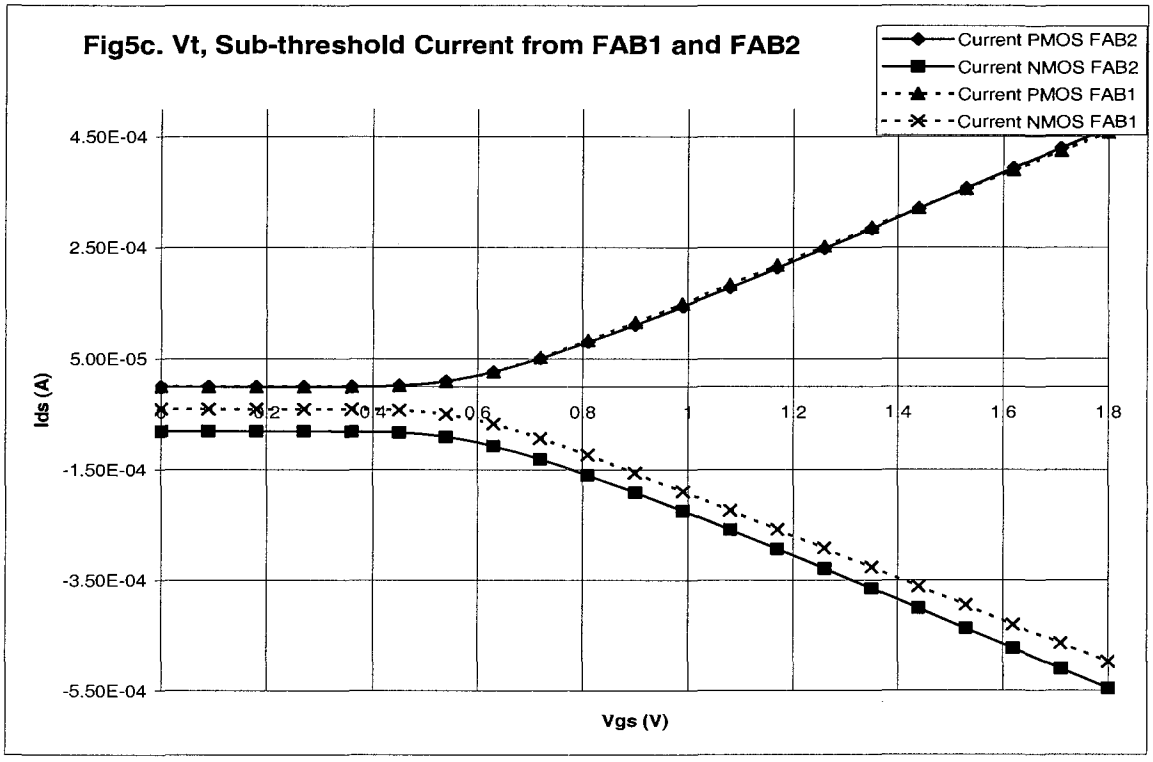


Figure 5 (Continue)

The curve with positive current is the result from PMOS transistors and the curve with negative current is the result from NMOS transistors. As shown in Figure 5, the transconductance characteristics for FAB1 and FAB2 PMOS transistors are similar. However, there seems to be a constant DC offset from FAB1 to FAB2 NMOS transistors.

The DC current shift is ~30μA. This means that NMOS transistors need ~30μA more to reach the threshold voltage. Also, V_{GS} ranges from 0V to 0.6V, where the transistor is in "off" state, FAB2 devices have leakage current of about 60μA while FAB1 devices have leakage current of about 30μA.

The 30μA DC offset current can potentially cause higher power consumption for FAB2 devices due to higher current usage. This can also cause higher drain-induced barrier lowering (DIBL)[5] for FAB2 devices compared to FAB1 devices. At the same time, this means that FAB2 devices will have higher drive strength compared to FAB1 devices.

2.3 Transistor Level Simulation Conclusions

There were a couple of issues found from both FABs. There was skew in the I-V characteristics in FAB1 and FAB2 in the triode regions for N/PMOS transistors. This can lead to a major problem within analog circuitries. The slope difference in the triode region for I-V characteristics can manifest itself by causing higher rise and fall times for signal transitions. It can also increase the amount of jitter embedded in the signals as well as reduced maximum operating frequency.

FAB2 devices in general will perform better than FAB1 devices for both analog and digital circuitries. For NMOS transistors FAB1 processed devices have V_{TH} of 600mV while FAB2 processed devices have V_{TH} of 700mV. For PMOS transistors FAB1 processed devices have V_{TH} of 810mV while FAB2 processed devices have V_{TH} of 720mV. The gap resulting from the V_{TH} difference of NMOS and PMOS transistors will cause "undefined" outputs. Thus, FAB1 devices will have bigger undefined gap compared to FAB2 devices. This gap is due to the N/PMOS process skew and can be devastating for both analog and digital circuits.

Such differential skew presence in the analog signal causes increased rise and fall times. This also implies decreased pulse width of the signal, therefore causing a limitation in the operating frequency. Increased differential skew also decreases the signal integrity by decreased data-eye while at the same time increasing the amount of jitter present in the signal. Having this in mind, it is apparent that because FAB2 devices have lower differential skew compared to FAB1, the FAB2 devices will be able to operate at higher frequency and have better signal integrity than FAB1 devices.

From the digital circuit domain, this N/PMOS skew will lead to a longer "unknown" region, causing higher setup and hold time requirements. Because digital signals only care about the saturation region of the signal, only a solid '1'

or '0' value is important to digital circuitries. Therefore, when there are longer transition gaps from "undefined" region, downstream circuits need longer setup and hold times to be able to latch the correct data. Without longer setup and hold times, the transfer data can be corrupted. Previous assessments from both FAB suggest that FAB2 devices will operate faster and more reliably compared to FAB1 devices, because the FAB2 devices have less N/PMOS skew compared to FAB1 devices.

The transconductance simulation shows that FAB2 NMOS transistors would have higher DC operating current by about 30μA compared to FAB1 NMOS transistors. Although the simulation shows higher current draw for FAB2 devices compared to FAB1 devices, this is not necessarily a "bad" thing. Though there is a potential problem with power consumption of the devices due to higher current draw, it also means that FAB2 devices will have higher drive capabilities. Therefore, both FAB1 and FAB2 devices are desirable depending on the application. For low power requirement applications, FAB1 devices will be more desirable to minimize the power consumption. For applications that require higher performance, FAB2 devices will be more advantageous because the transistors can drive more loads in the output and signal integrity will be better.

Now that the transistor level simulations have been reviewed, let us move onto higher-level simulations.

Chapter 3. Analysis of Gate Level HSPICE Simulation Results

This chapter shows the analysis of multiple transistor device performance from the two different FABs. Voltage transfer, five-stage inverter, and five-stage ring oscillator characteristics were simulated. For convenience, the length of transistors is set to 180nm for both N and P channel transistors and width of the transistors is set to 1440 for P channel and 720nm for N channel for voltage transfer characteristics simulation. This is to offset slower P channel electron drift velocity. Then five-stage inverter and ring oscillator simulations are conducted with the length of 180nm for both N and P channel, and the width of 3600nm for P channel and 1800nm for N channel transistors. The width of transistors has increased since the five-stage invertors needs higher drive strength.

3.1 Voltage Transfer Characteristics

The simple inverter model used in this analysis is shown in Figure 6. Figure 7 simply shows the voltage transfer characteristic for basic inverters with different process parameters provided from FAB1 and FAB2.

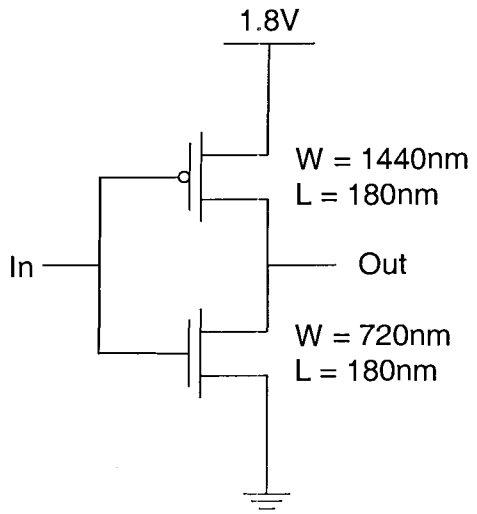
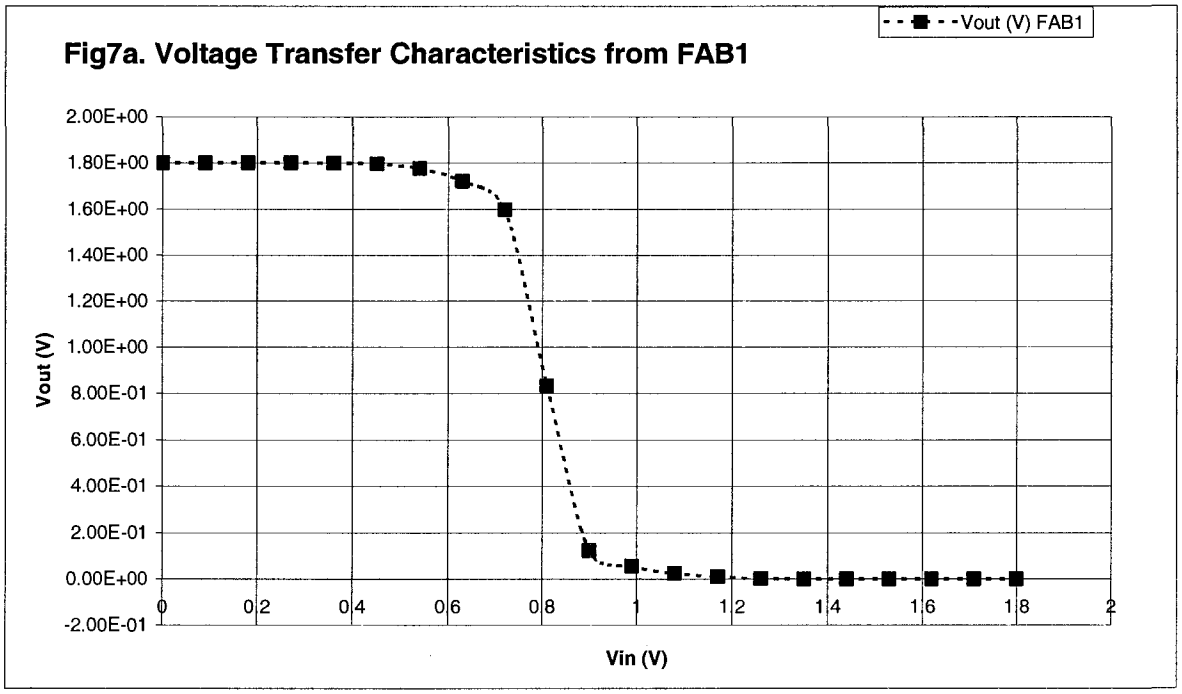
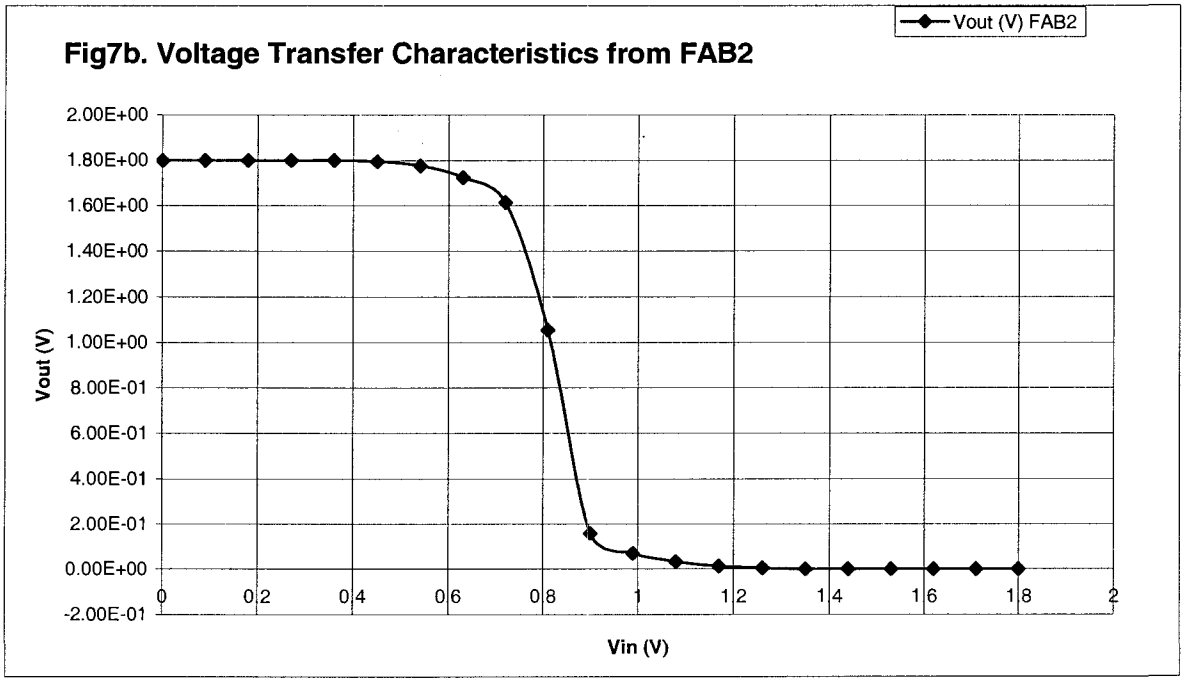


Figure 6 Simple Inverter model used for Voltage transfer characteristics

Figure 7 Voltage transfer characteristics of simple inverter (Vin vs Vout)





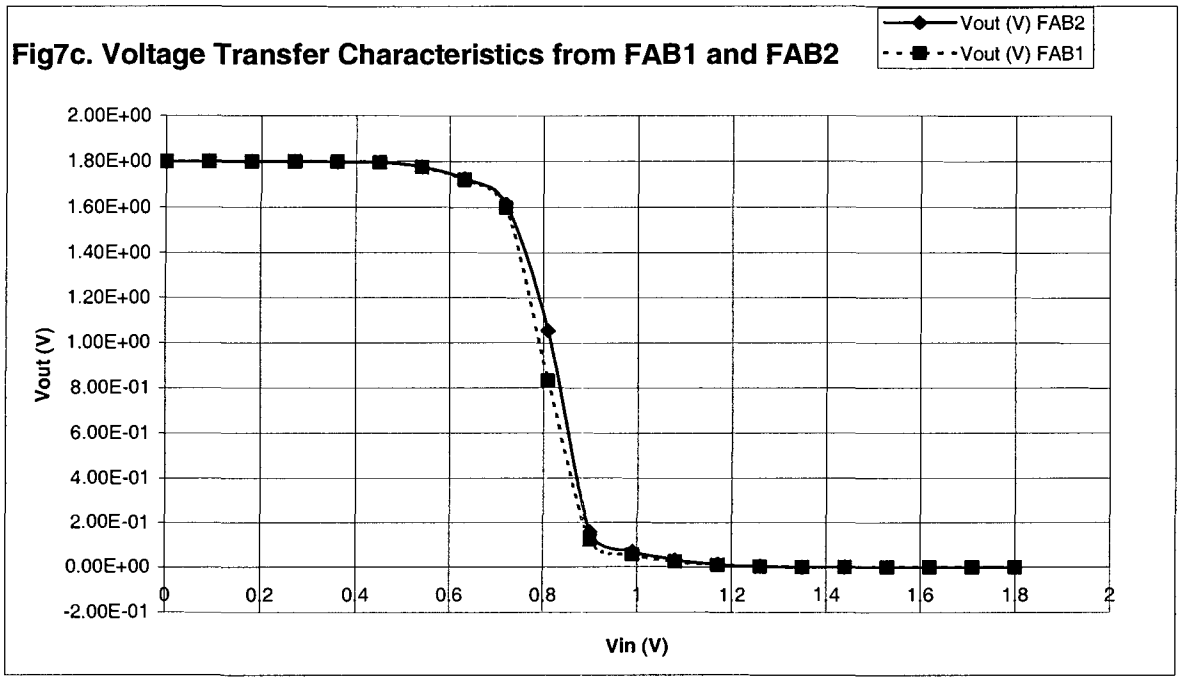


Figure 7 (Continue)

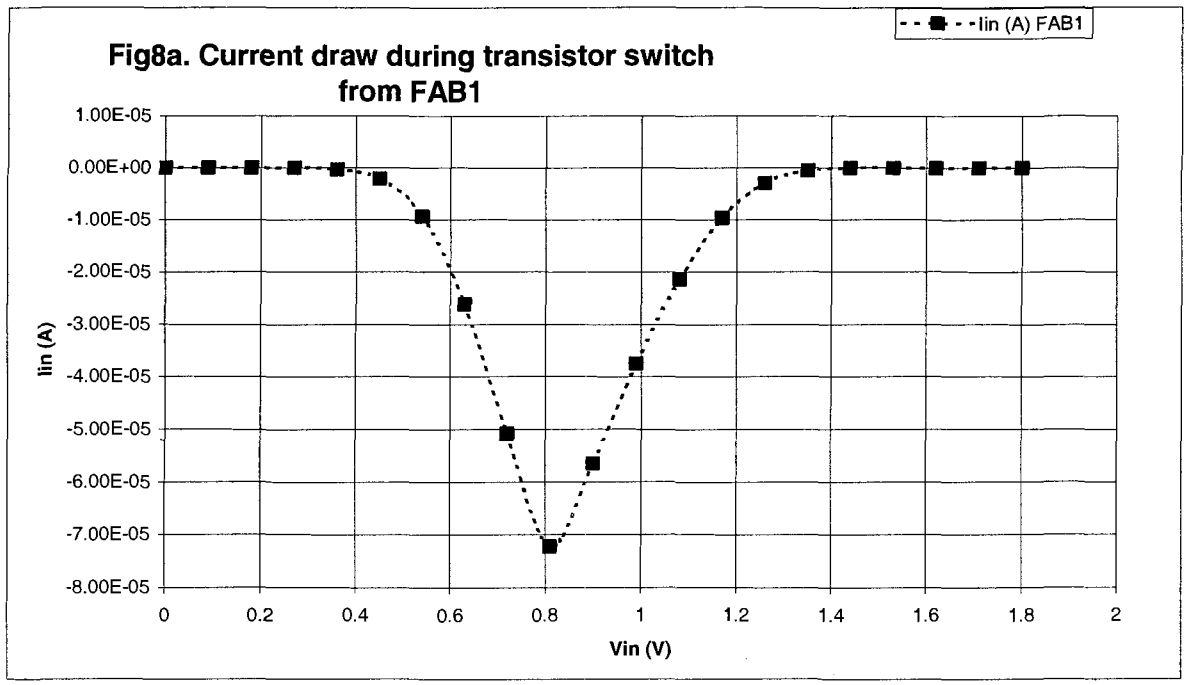
As shown in Figure 7, output voltage characteristics show that FAB1 and FAB2 have almost the same characteristics in the saturation region. However, in the triode region, from Vin of 0.6V to 1.0V, FAB2 is slightly delayed behind FAB1. In the lower voltages, slope is greater for FAB1, while slope of FAB2 device becomes greater beyond ~800mV point. At this point there are about 22mV Vin difference from FAB1 to FAB2.

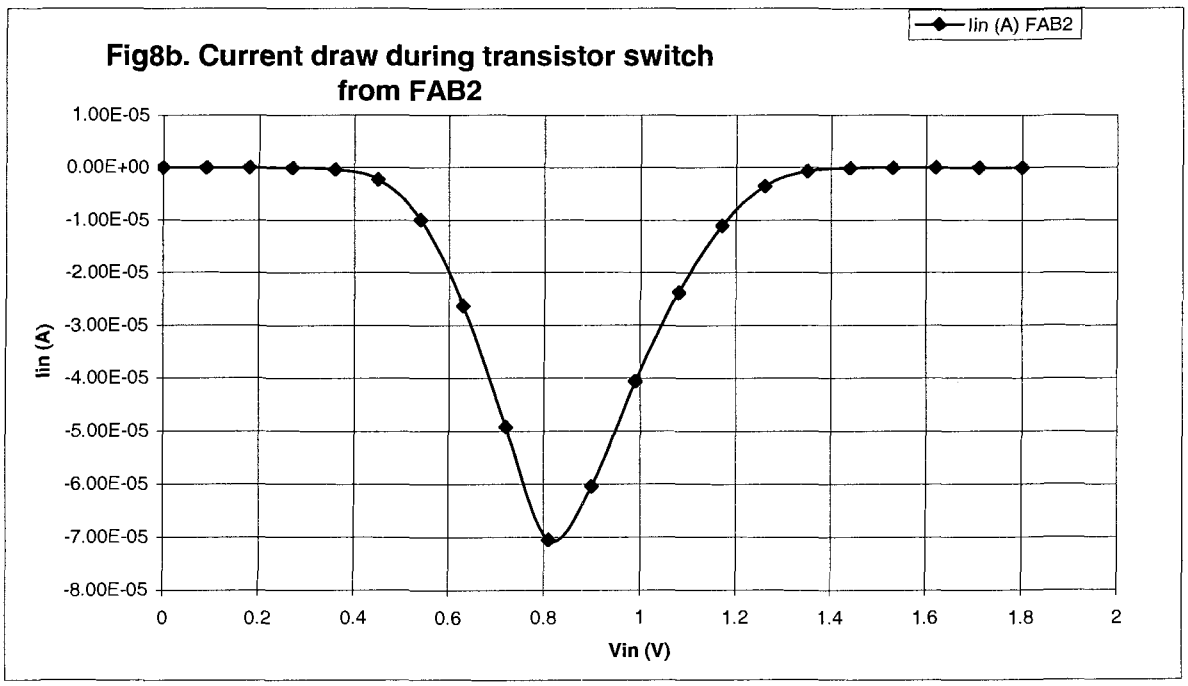
This means that during the transition point, FAB2 devices would switch faster than FAB1 devices for '1' to '0' transition. However, FAB1 devices will switch faster for '0' to '1' transition. This effect can possibly enhance the digital switching speed since digital circuits only respond when the signal reaches VOL/VOH. Overall switching speed for both devices would stay about the same.

A closer analysis of the slope shows that between Vin of 720mV to 810mV, FAB1 devices have a slope of -8.33 while FAB2 devices have a slope of -6.22. Between Vin of 810mV to 900mV, FAB1 devices have a slope of -8.11 while

FAB2 devices have a slope of -10.22. This suggests that FAB1 devices' transition is more linear compared to FAB2 devices' transition slope. From the analog circuit point of view, FAB1 devices would be more desirable since their transient curve is more linear than FAB2 devices.

Figure 8 Current Draw during the inverter switch (Vin vs Iin)





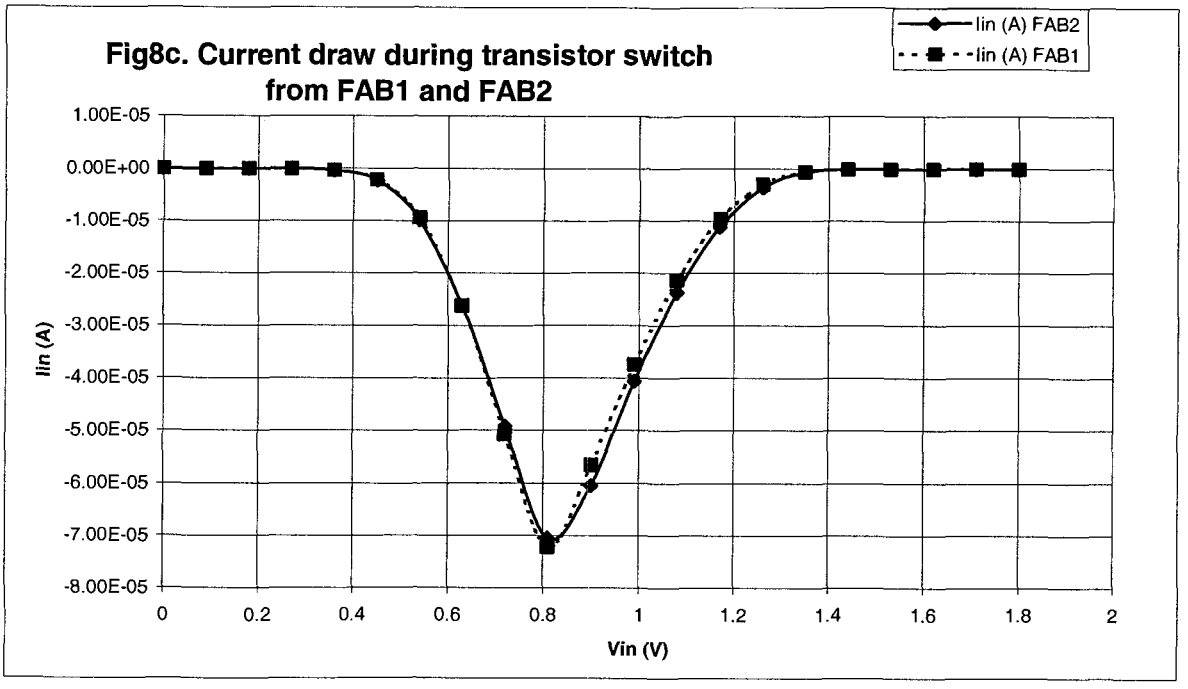


Figure 8 (Continue)

Figure 8 shows the current draw from a Vdd power supply for FAB1 and FAB2 devices. Again there is almost no difference between the two. However, a closer look at the ~800mV Vin point on x-axis shows that total current draw from FAB1 device is -72μA and FAB2 is -70μA. The 2μA difference in instantaneous peak current draw during this operation seems to be driving the difference on the slope of two inverters.

This also means that there will be a difference in power consumption whenever the transistors go thru a transition or switching. Let's consider a system that consists of one million transistors and assume about ten percent of the transistors will be switching at the same time. When these 100,000 transistors are switching at the same time, if the system is built from FAB1, the device will draw instantaneous peak current of 7.2A or instantaneous peak power of 12.96Watts. If the system is built from FAB2, the device will draw instantaneous peak current of 7.0A or instantaneous peak power of 12.6Watts.

The small difference of power consumption difference would cause devices from FAB1 to draw much more compare to its counter part from FAB2 during multi-million transistors switches. Such small differences can manifest to become signal integrity problems considering slower process corners, low V_{DD}, and high temperature environments. Such conditions will slow down the device operation considerably and degrade the device performance.

3.2 Five-Stage Inverter Characteristics

Figure 9 shows the five-stage inverter chain model used in this chapter for an ideal square wave input. Figure 10 shows the output of the five identical inverters with annotated delay and parasitic capacitances for the first input cycle of the simulation. This demonstrates the associated propagation delay through five inverter chains. For the sake of simulation the distances between each inverter are neglected, because of the distance between each inverter will vary for design to design. However, for real device simulations, one has to incorporate the effect of wire resistances as well as capacitances. To the first order approximation, the metal resistance is 50mΩ/square and the metal capacitance is 0.1fF/μm. Point 'a' indicated in Figure 9 is the input 'Vin' as shown in Figure 10, and point 'b' indicates output 'Vout'.

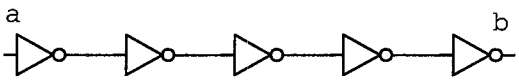
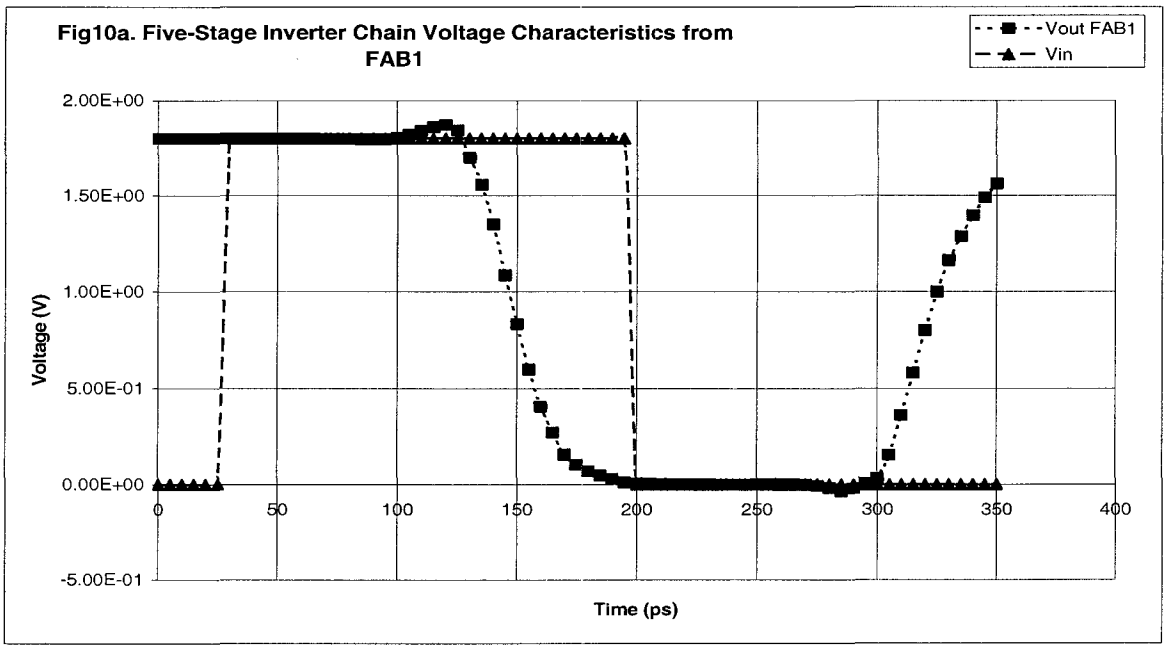
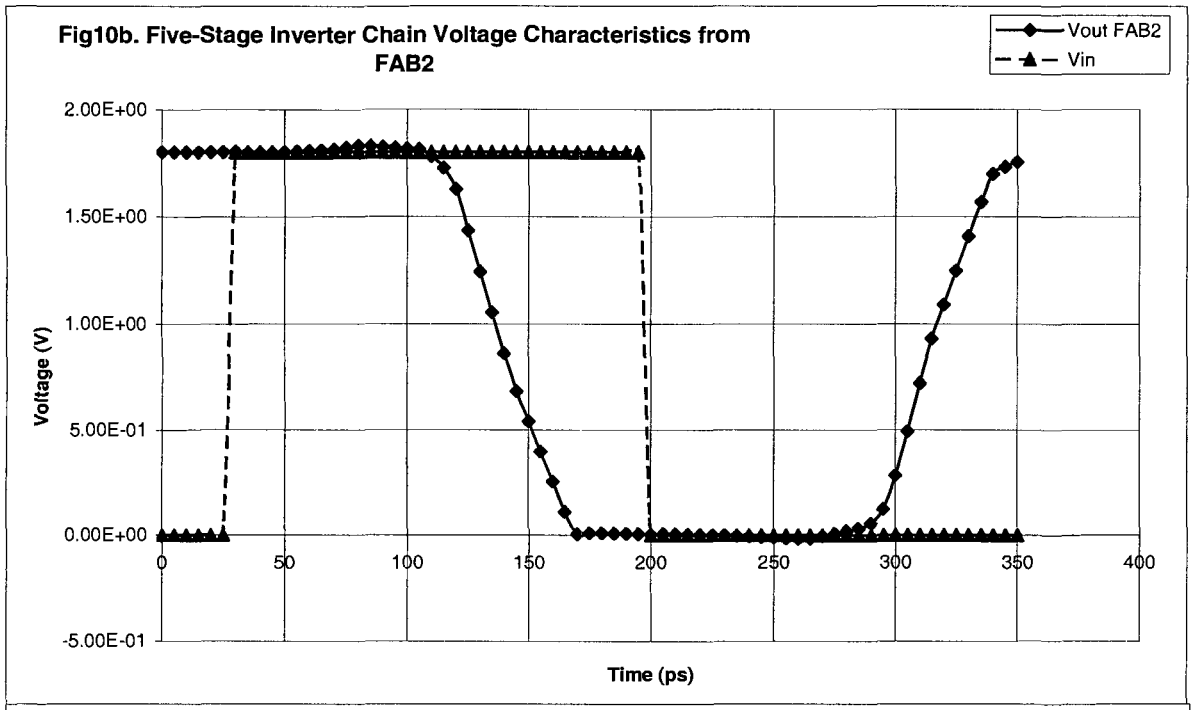


Figure 9 Identical Five Stage Inverter Chain

Figure 10 Five-Stage Inverter Chain Voltage Characteristics (Voltage vs Time)





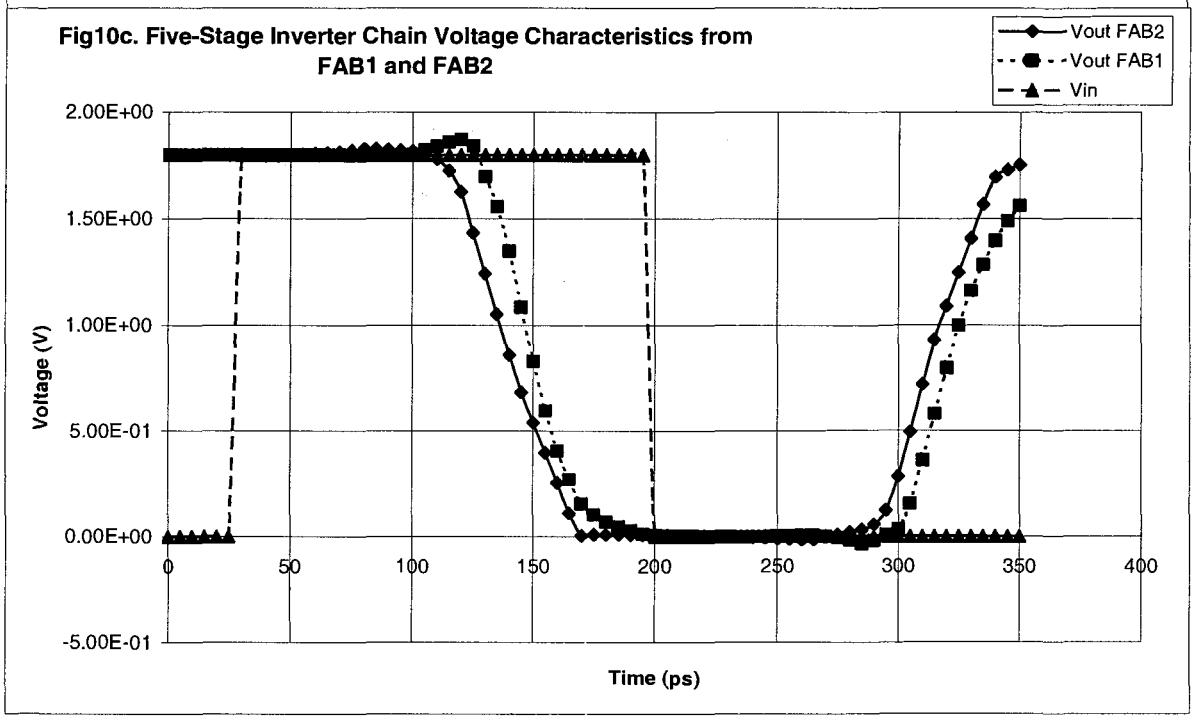


Figure 10 (Continue)

The outputs of this series of inverters are loaded with another of the same type of inverter to keep the loading termination consistent at the output. This graph shows that the propagation delay associated with five-stage inverters are ~130ps for FAB2 devices and ~140ps for FAB1 devices. There is roughly a 10ps or 7.7% propagation delay difference from FAB1 to FAB2 devices when signal is being propagated from point 'a' to 'b.' From this result, FAB1 seems to have higher impedance loading than FAB2, causing the delay to be increased as the signals propagate through the inverters. Each inverter adds ~26ps for FAB2 and ~28ps for FAB1. Thus there is a ~2ps or 7.7% difference in propagation delay from FAB1 to FAB2.

A 2ps difference in delay in signal propagation within digital circuitries may not cause any harm as long as the digital circuits operate at a slower rate by limiting maximum operating frequency. Still, this would cause delayed clock distribution circuitries and increased signal propagation delay.

This can also cause a race condition in the critical path of the data. These effects are impossible to analyze using simulation tools. In order to estimate the possible effects, real device measurements from both FABs are required. With real-data at hand, it is possible to deduce the standard deviation of each delay to see how reliable the system will be.

Although the simulation result shows that FAB2 devices will run at a higher rate compared to FAB1 devices, if FAB2 devices' measurements has a higher variation than FAB1 devices, then FAB1 devices will be more reliable.

In either case, if the circuits are designed properly with this delay in mind, devices fabricated from both FAB1 and FAB2 should not cause much problems. Otherwise, it will be required to re-design in order to eliminate possible critical path problems and make the variation smaller to make the device more reliable.

In analog circuits, however, this delay can pose much bigger problems. The analog signal spends most of the time at the transition point rather than saturation point of the signal. This amount of delay means the analog signals have 2ps less time to rise or fall to either '1' or '0' value. This can ultimately cause smaller signal swing at maximum operating frequency or slower operation.

3.3 Five-Stage Ring Oscillator Characteristics

The five-stage ring oscillator is similar to the five-stage inverter as shown in section 3.2. The five-stage ring oscillator is differentiated from a five-stage inverter because it has a line connecting point 'a' and 'b' in the inverter chain as shown in Figure 11. Since the voltage at point 'a' oscillates like a clock, this type of inverter chain in Figure 11 is called a ring oscillator. The ring oscillators are the common test devices for checking circuit speed. Similar to five-stage inverter model, each gate distance is neglected. Again, in order to simulate the real-life device, the designer needs to incorporate the metal resistance and capacitance. Figure 12 shows the first four cycles of simulation results from the five-stage ring oscillator.

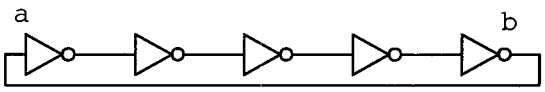
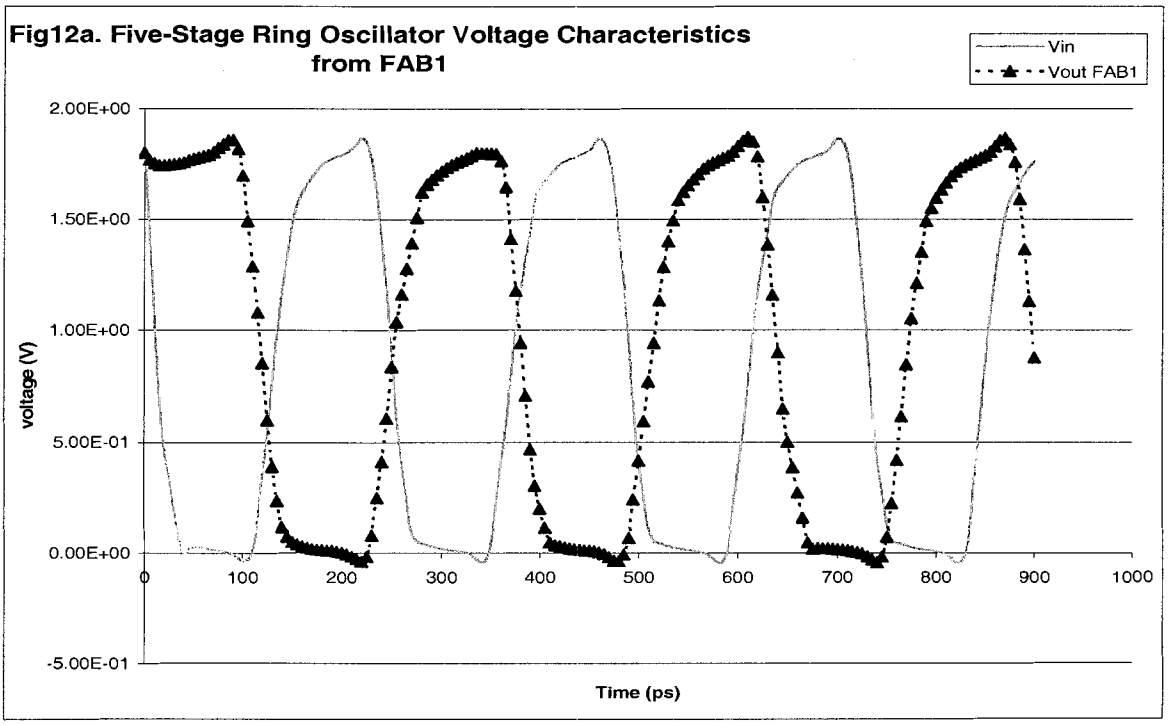
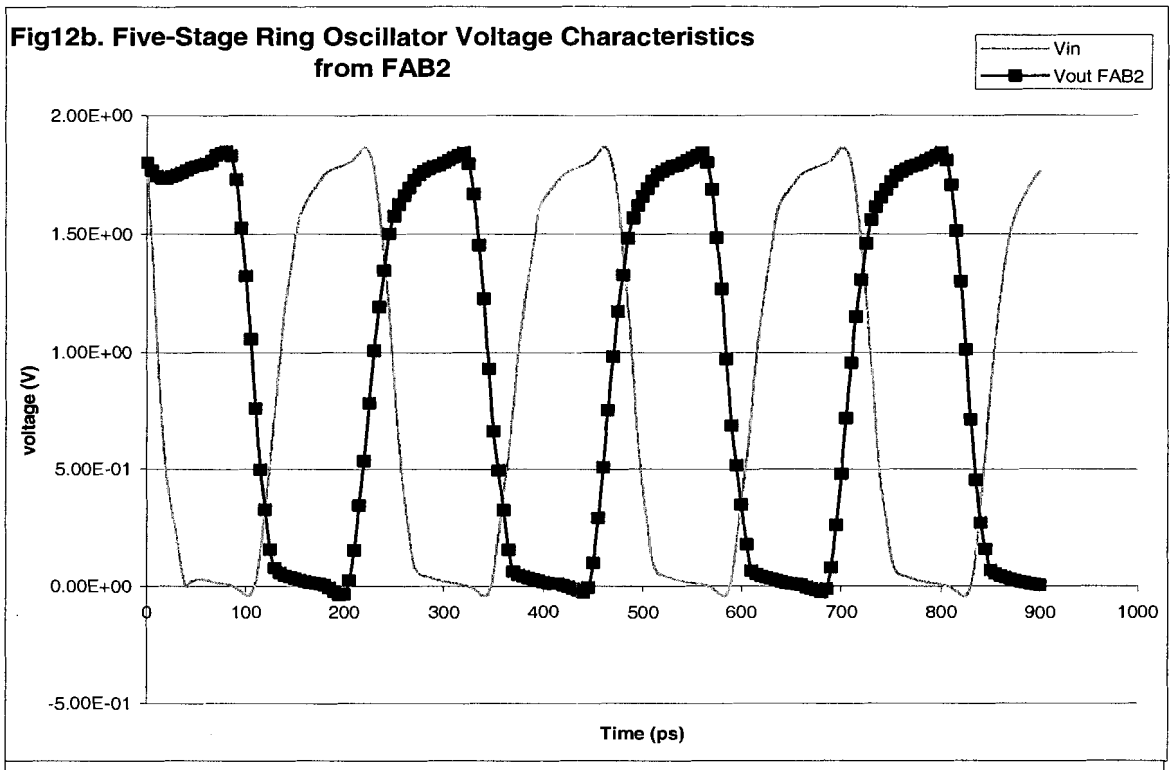


Figure 11 Five-Stage Ring Oscillator

Figure 12 Five-Stage Ring Oscillator Voltage Characteristics (Voltage vs Time)





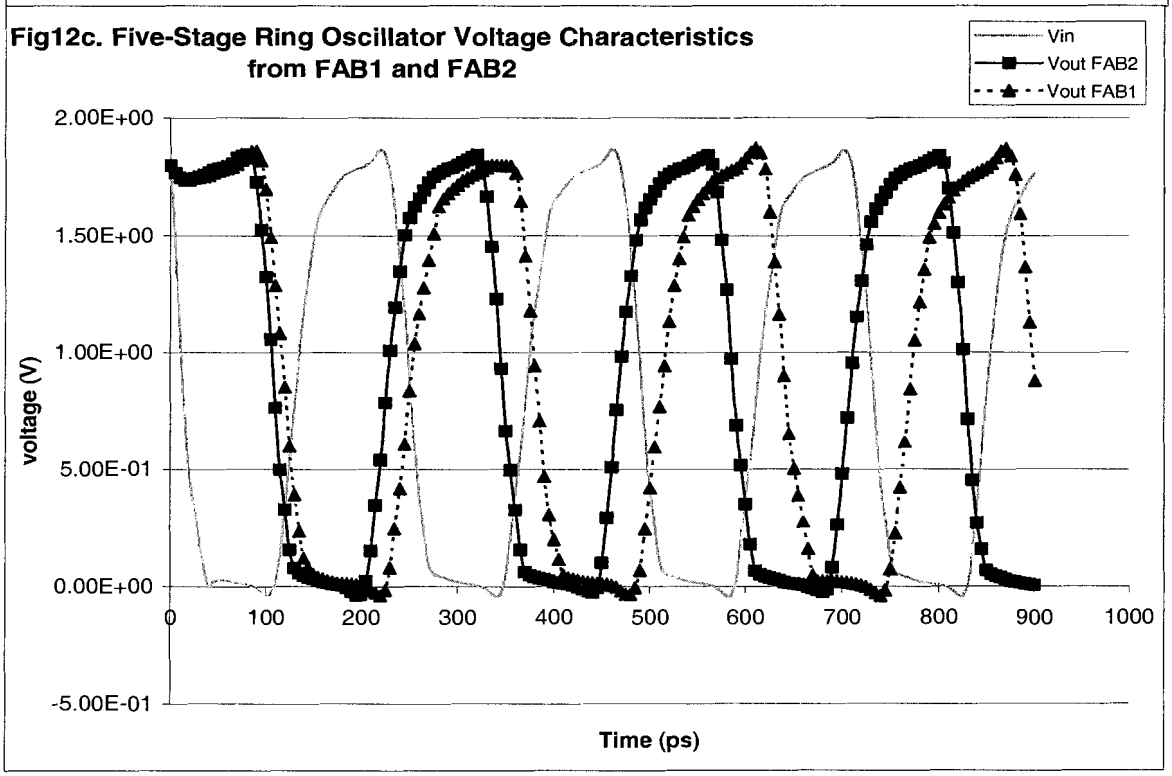


Figure 12 (Continue)

Since there was a propagation delay difference between FAB1 and FAB2 inverter models as shown in section 3.2, it is expected that there is a similar effect on the ring oscillator model. As shown in Figure 12, the different amount of internal loading of each FAB model distinguishes the period of FAB1 and FAB2 oscillating signals.

The FAB1 model reveals the clock pattern with a period of ~260ps while the FAB2 model reflects ~240ps period. Around 20ps or 8.3% difference in their period is observed, as it was shown in section 3.2. This 20ps difference explains the clock frequency offset generated from both oscillators. The FAB1 ring oscillator runs at 3.85GHz while FAB2 oscillator runs at 4.17GHz. This small propagation delay caused by the difference in parasitic loading results in a ~0.32GHz operating frequency difference.

These results show that the maximum frequency clock that can be generated from either FAB1 or FAB2 will be limited by the amount of propagation delay of their clock circuitry. From the simulation, FAB1 devices' propagation delay is less then FAB2 devices.' Thus the clock circuitry built on FAB1 process would have higher operating frequency. With process, voltage, and temperature variation, this can actually cause FAB2 devices to under-perform.

3.4 Gate Level Simulation Results

From the simulation results, there were not any significant differences between FAB1 and FAB2 processed devices except for the propagation delay difference between the two. The FAB1 processed devices have 2ps less propagation on 26ps delay than FAB2 processed devices. Depending on the application, this difference can have huge impact. For lower frequency applications, this should not cause and problems but for higher frequency applications, FAB1 would be preferable.

Chapter 4. Coupling and Power Bus Resistance Effect of HSPICE Simulation Results

This chapter gives a simple analysis of system level performance and its possible outcome with given variable settings. It discusses the cross talk effect by use of coupling capacitor between two live wires and power grid resistance effect by increasing resistance of a power bus connected to a series of inverters. As before, the length of transistors is set to 180nm for both N and P channel transistors and the width is set to 18μm for P channel and 9μm for N channel transistors for aggressor line and 14.4μm for P channel and 7.2μm for N channel transistors for victim line for cross talk effect simulation. To highlight the effect of inter-symbol-interference, the size of the transistors has increased to increase the drive strength. The power grid resistance simulation is conducted with the length of 180nm for both N and P channel, and the width of 1440nm for P channel and 720nm for N channel transistors. The typical transistor size has been used to simulate typical power consumption environment.

4.1 Cross Talk Effect of Coupling Capacitances

This section deals with two adjacent lines with 100fF coupling capacitance between them, which is approximately equivalent to 1μm distance between two adjacent signal wires. The coupling capacitance circuit model shown in Figure 13 has an effect similar to crosstalk. Such crosstalk or inter-symbol interference within the device can cause huge performance reductions due to induced deterministic jitter. This section deals with inter-symbol interference or crosstalk by pseudo-simulation describing two closely located wires with high-speed signals. All the gates and circuit components are set apart by a minimum line length of 0.18μm.

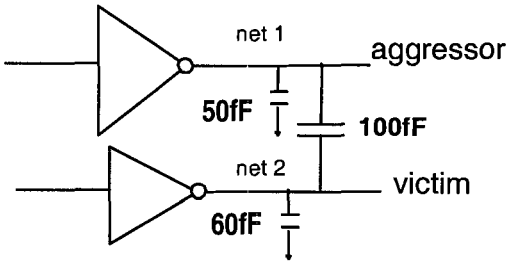
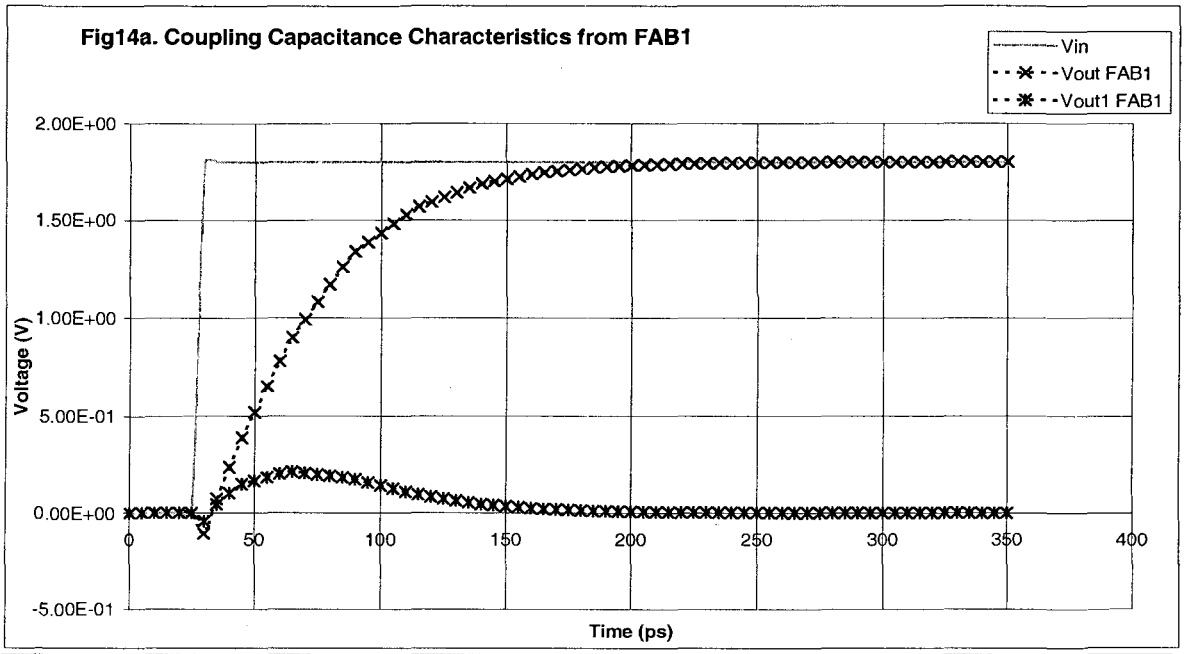
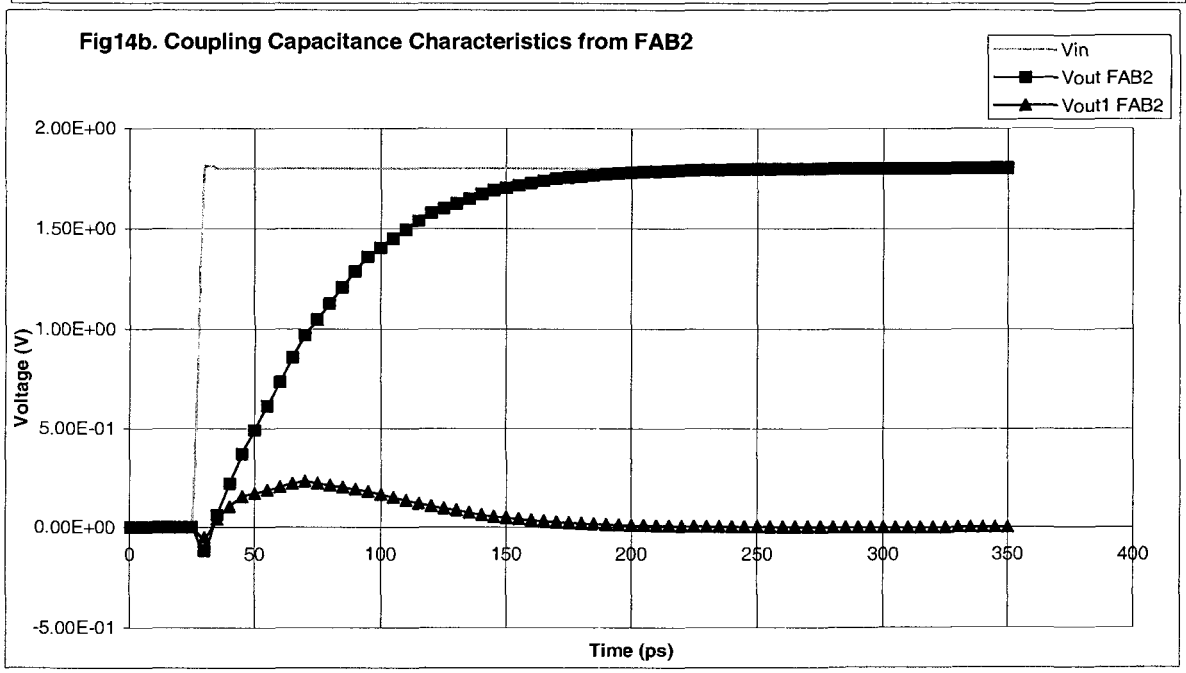


Figure 13 Coupling Capacitance circuit model

Figure 14 Coupling Capacitance Characteristics (Voltage vs Time)





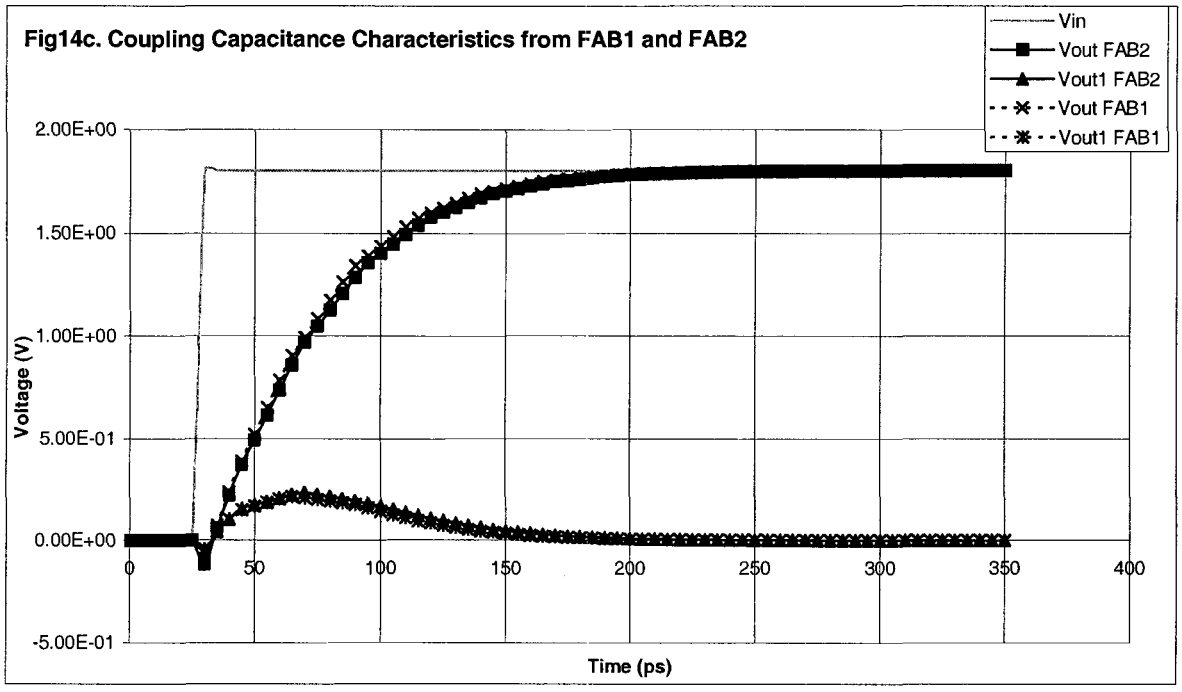


Figure 14 (Continue)

Figure 14 shows the signal in the main, aggressor, line and in the adjacent, victim, line due to the coupling capacitance of 100fF. The coupling capacitance between two wires is an illustration of energy transfer from one wire to the other by the electro-magnetic field generated by the signal. Signals generated from both FAB1 and FAB2 produce a similar trend line. When the input is forced to 1.8V, the aggressor line is slowly increased toward 1.8V while charging up the coupling capacitor, causing the capacitively coupled voltage in the victim line. This victim for FAB1 is increased to a maximum of ~220mV while FAB2 is increased to a maximum of ~240mV. This means that the part of the aggressor signal is being propagated to the victim line. Unwanted signal in the victim line can consequently have a destructive effect on signals that travel through a victim line. Figure 14 reveals that FAB2 devices are more susceptible to internal crosstalk noise from adjacent lines compared to FAB1 devices. This effect can cause higher jitter propagation or crosstalk throughout the device for FAB2.

4.2 Effect of Power Grid Resistance

The issue of power grid resistance arises in any high power circuits. In a poorly designed power grid, part of the circuits cannot receive Vdd close to the full amount. Power grid resistance models simulate the power distribution circuit with varying power dissipation or voltage. As the part of circuit is located further away from the main power line, power grid resistance will increase.

The model used in this analysis consists of 0.4μm wide wire with length of 2μm and 1000μm used as a power bus. The system consists of 32 inverters with the width of 1440nm for P channel and 720nm for N channel transistors, each connected to the power line. To simulate the worst-case condition, all the inverters are switched to high at the same time within a 100ps time period. Same inverter used in section 3.1 is used for this simulation.

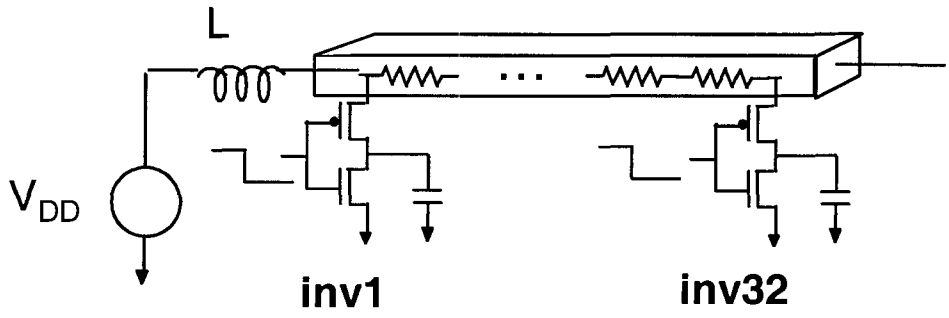
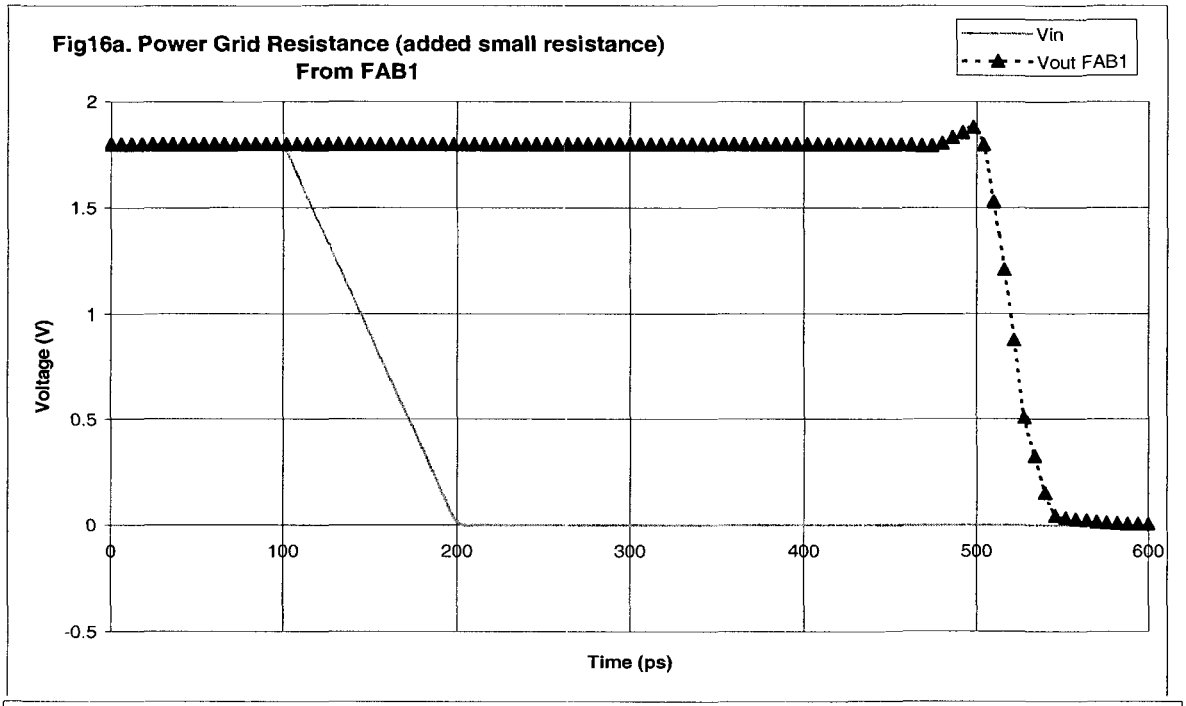
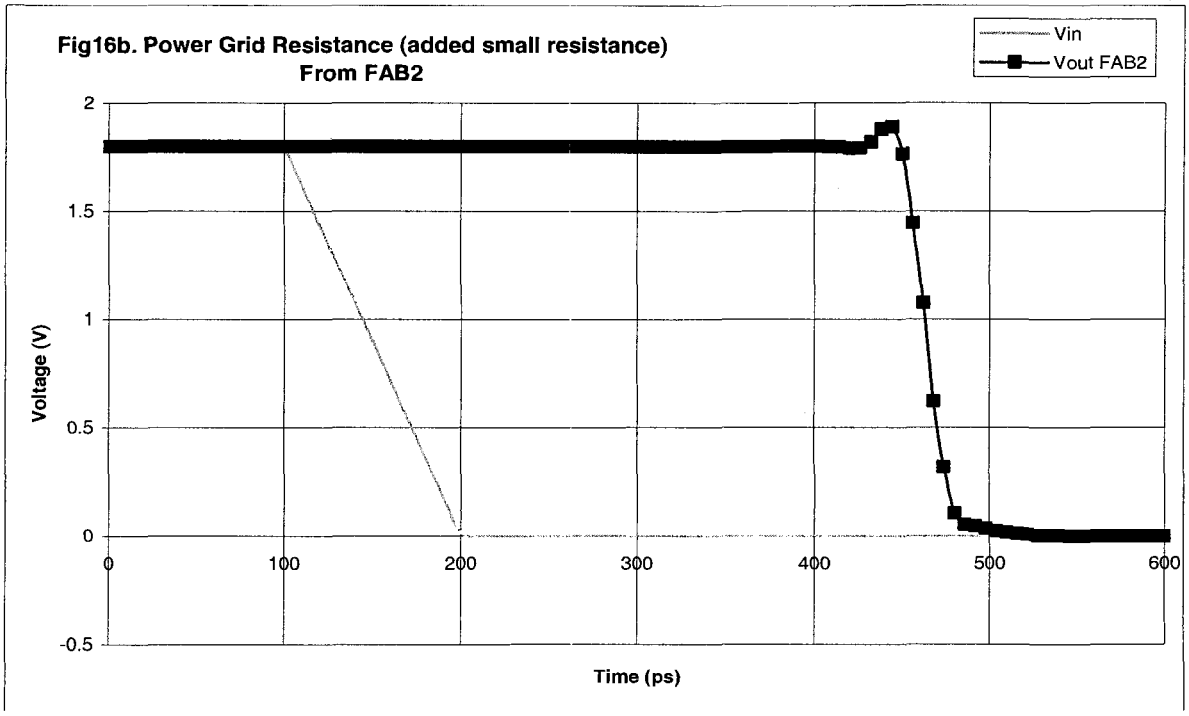


Figure 15 Resistance model in power grid

Figure 16 Added resistance to power grid (Voltage vs Time)





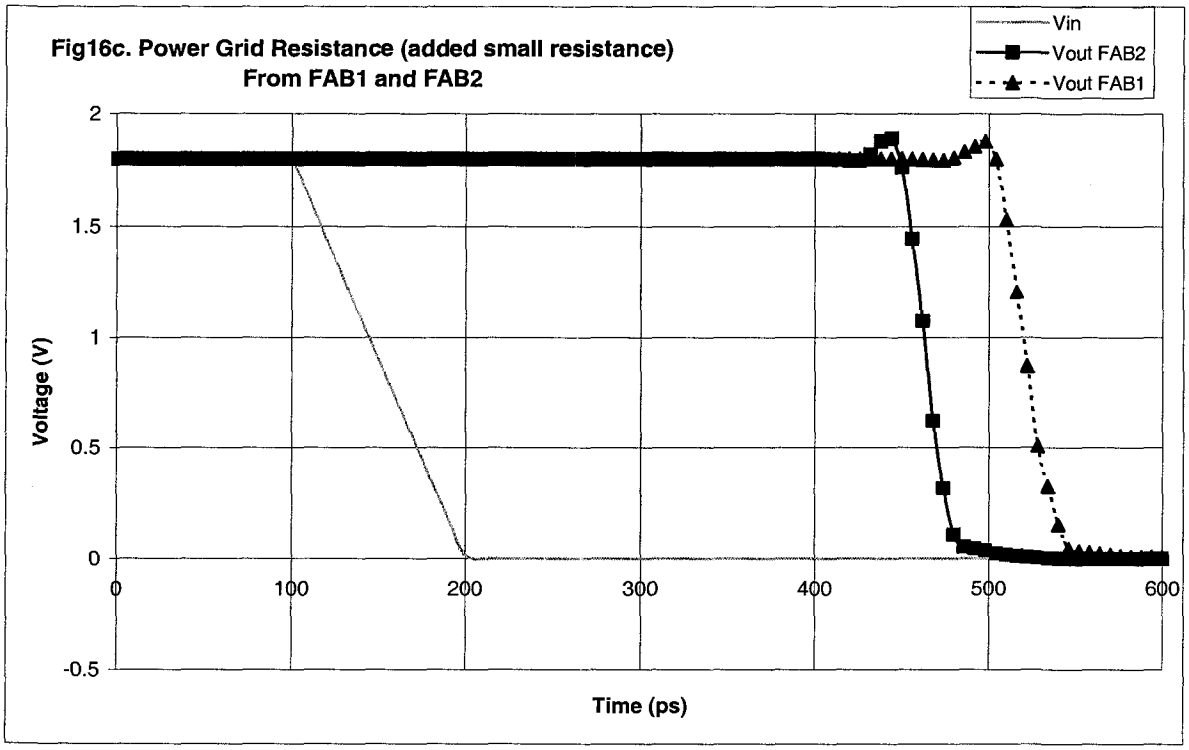


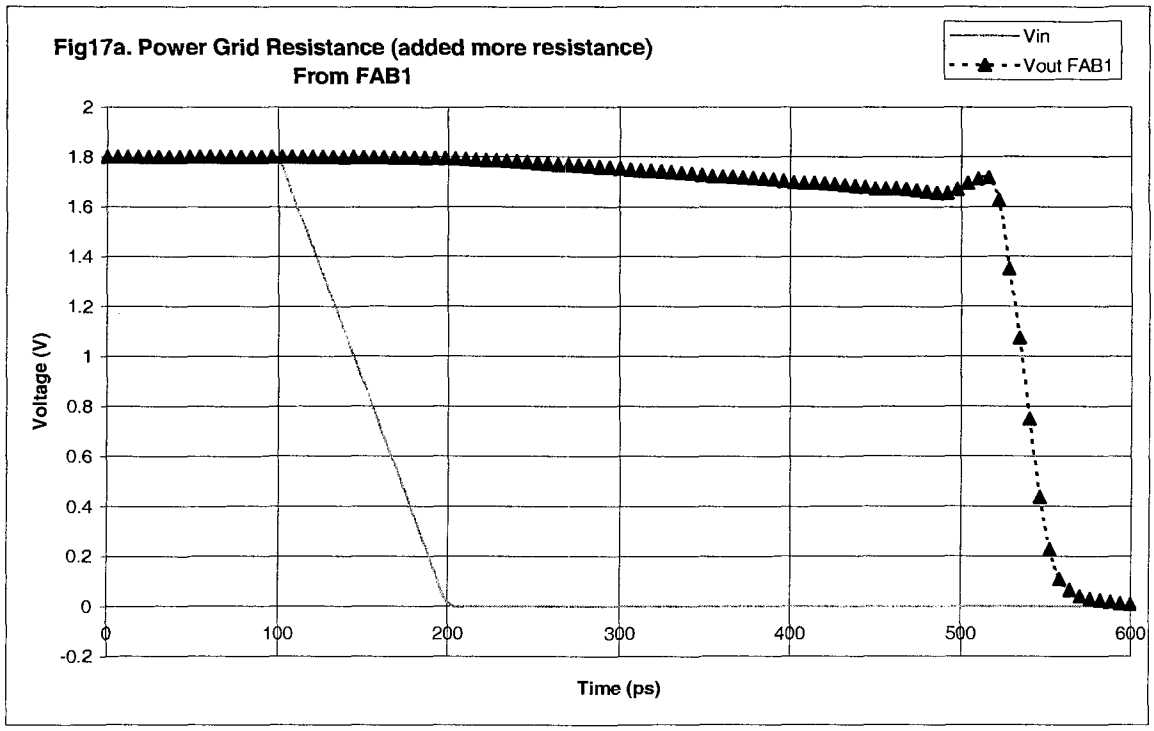
Figure 16 (Continue)

Figure 15 reflects the power grid resistance circuit used for this analysis. Figure 16 shows the effect of the power grid with a small amount of added resistance. The amount of resistance added is determined by varying the length of the wire between each transistor. Figure 16 is the simulation result with total wire length of 2μm. Each transistor is spaced equally apart by 0.0625μm. Since the added resistance is small, the voltage drop at the end of the inverter does not have much effect. There is a little bit of roll off close to ~420ps for FAB2 and ~480ps for FAB1. The voltage drop is less then 10mV, which is negligible.

Reducing the bus length increased the resistance. This illustrates the possible problems with a poorly designed power grid. The result is as shown in Figure 17 with bus length of 1000μm where each transistor is set equally apart by 31.25μm. Now the power dissipation takes a huge effect on inverters located toward the end of the power grid. The voltage dropped by ~140mV for FAB2 devices while FAB1 devices dropped ~130mV. This causes the power supply voltage to drop from 1.8V to 1.66V~1.67V. The voltage drop is more than enough to degrade the

operational performance of the inverter, even without taking the temperature effect into account in the simulation. If the temperature is increased, the voltage drop will increase even further causing possible malfunction of the device.

Figure 17 Increased resistance in power grid (Voltage vs Time)



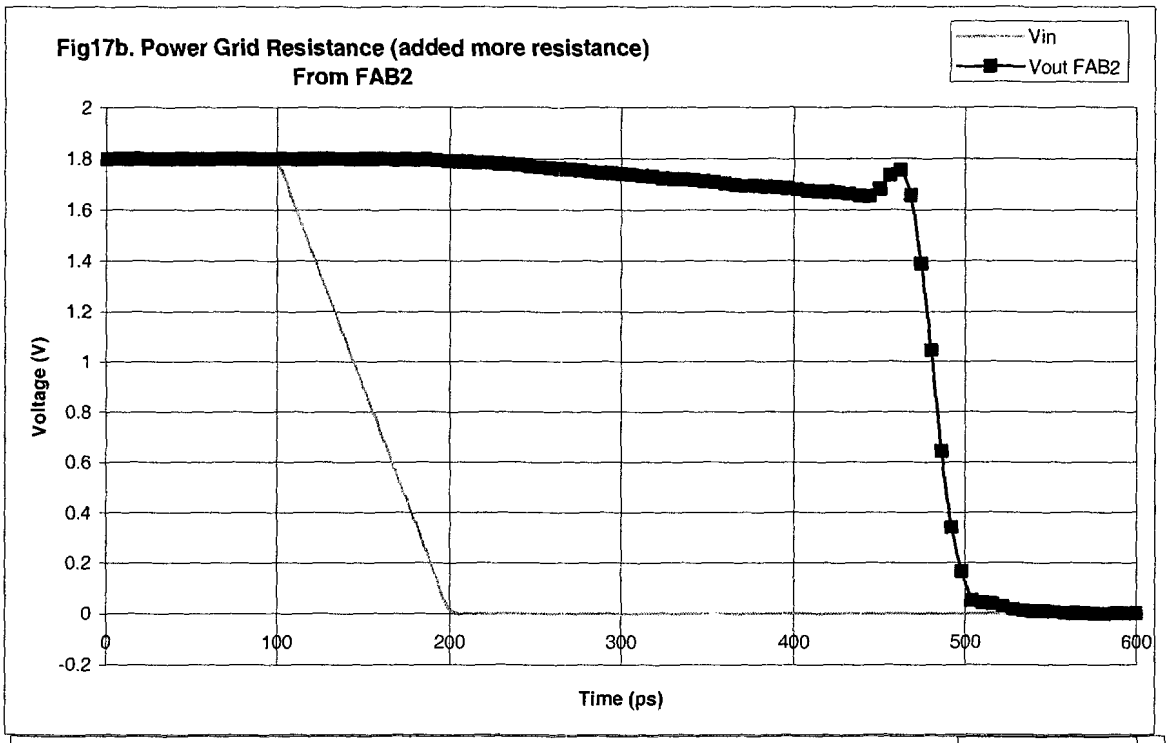


Fig17b. Power Grid Resistance (added more resistance)
From FAB2
Vin
Vout FAB2
Voltage (V)
Time (ps)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
100
200
300
400
500
600

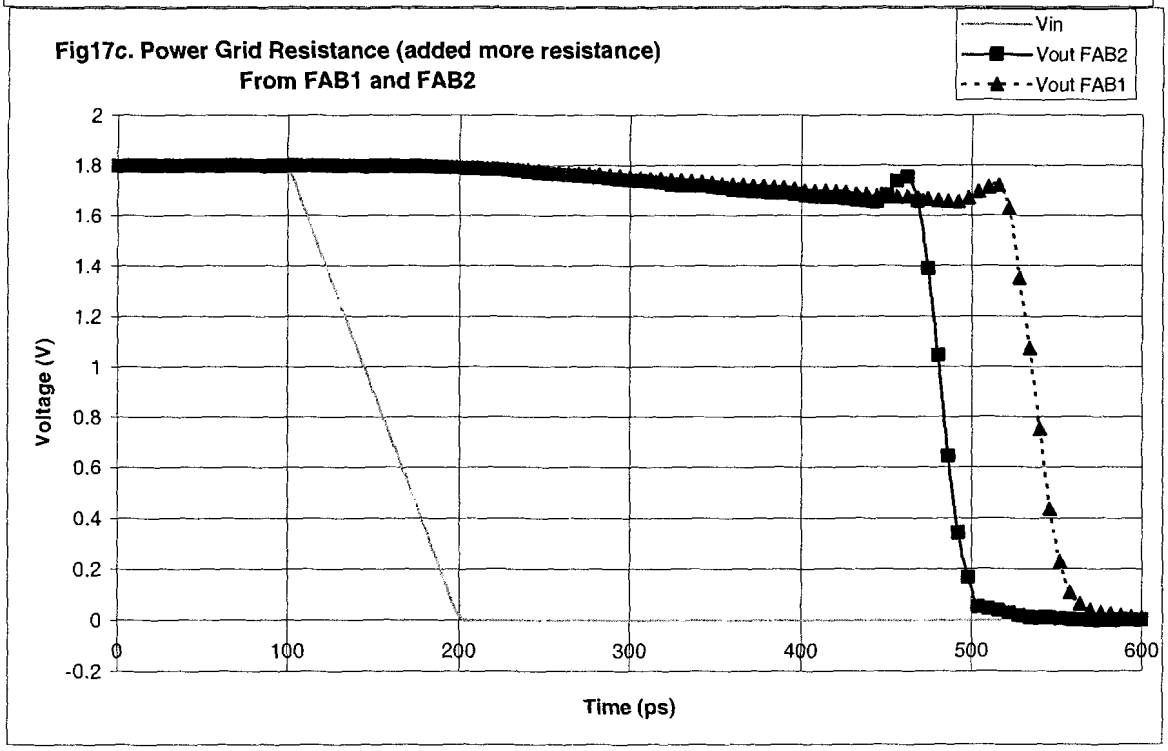


Fig17c. Power Grid Resistance (added more resistance)
From FAB1 and FAB2
Vin
Vout FAB2
Vout FAB1
Voltage (V)
Time (ps)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
0
100
200
300
400
500
600

4.3 Coupling And Power Grid Resistance Results

FAB2 devices are more susceptible to crosstalk noise compared to FAB1 devices as shown in section 4.1. FAB1 devices' interference signal peak in the victim line is at 220mV while FAB2 devices' interference signal peak is at 240mV. This means when the signal is propagating through an aggressor line, the victim line receives 20mV more interference for FAB2 devices. If the victim line also contains its own signal, the crosstalk from the aggressor line will collide with the signal within the victim line, potentially corrupting it. The crosstalk also adds more deterministic jitter within the signal causing higher total jitter within the signal. As observed from the coupling effect of two lines, FAB2 devices will have higher deterministic jitter compared to FAB1 devices.

As for the power grid resistance effect, there was almost no difference for the closely bounded gates of total length of 0.8μm for both FAB1 and FAB2 devices. When the length had been increased to 400μm, however, there was shown quite a difference between two FABs. FAB2 devices' power supply dropped by 140mV while FAB1 devices' power supply dropped by 130mV. This means that the gate, which is located at the end of the power bus, only receives 1.66V for FAB2 devices and 1.67V for FAB1 devices. With possible process parameter corners as well as temperature and power supply variation, 10mV will be enough to cause a device not to function for FAB2 devices while FAB1 device will be still functional.

Chapter 5. Conclusion

The I-V characteristic of FAB1 and FAB2 devices shows that for NMOS transistors, FAB1 devices have higher increasing slope while for PMOS transistors, FAB2 devices have higher increasing slope. Because NMOS transistors will operate faster for FAB1 devices while PMOS transistors will operate faster for FAB2 devices, the combined operating frequency for both FABs will be similar. This, however, also indicates that both FABs devices will have higher signal skew and rise/fall time causing signal integrity problems for very high performance devices. The transconductance simulation shows that FAB2 devices would have higher power consumption for NMOS transistors due to DC offset voltage.

All the simulation in this paper is based on mean process parameters. There is also a factor of variation in process parameter one should consider. Even though the simulation result shows good results, larger variation in the process parameters can actually cause device to under-perform or malfunction in significant factor. However, due to the proprietary reasons, author is not permitted to disclose this information in this paper.

Most of the analysis from the gate level simulation shows that FAB2 devices would operate at a slower speed than the FAB1 devices, while the loading capacitances caused by parasitic load are more for FAB1 than FAB2. When looking at device operation from the top level, the operating frequency of each FAB would not be affected in a great deal either by faster transistor transition or by higher loading effects from FAB1 and FAB2. Incidentally, both effects cancel each other causing the operational frequency of FAB1 and FAB2 to be about the same.

The higher loading capacitance from FAB1 devices cause less crosstalk by decreasing the amount of jitter propagated from wire to wire At the same time it is

increasing the propagation delay of each inverter. FAB2 devices show less loading capacitance by increasing the propagation delay of each inverter. At the same time it is increasing the cross-talk effect causing higher jitter propagation. Therefore, the differences between the two fabrication foundations are small enough that it would not cause a functional problem between two separately fabricated devices.

Although, the cost reduction of the wafer cost is one of the most critical factors in technology transfer, there are couple other factors that must considered. First, one must consider the amount of good die yield from each wafer. When one FAB provide wafer process with lesser cost but with much lower yield, then one might end up with lesser number of good dies with cheaper wafer cost. So at the end, one might not gain much cost reduction or possibly even increase per device cost. Another factor to be considered is the setup cost. If the mask cost is higher on one FAB to the other, cheaper wafer price might not be enough to offset the higher mask cost. Therefore, keeping all the factors in mind before one make a decision about the technology transfer to reduce the cost.

Appendix A HSPICE model source files

All the HSPICE source files are included in this compressed file:
HSPICE_source_code.zip

File descriptions are as follows:

proj1_1:	I-V Characteristics for DSM transistors
proj1_2:	Sub-threshold current
proj1_3:	Voltage transfer characteristics
proj2_2:	Five Stage Inverter Chain
proj2_3:	Five Stage Ring Oscillator
proj3_1:	Coupling Capacitance
proj3_2a:	Added resistance to the power grid
proj3_2b:	Added more resistance to the power grid

Appendix A.1 I-V Characteristic HSPICE Source Code

```
* IV Characteristics for DSM Transistors
*************************************************************************
* Set supply and library
*************************************************************************
.param Sup=1.8      * Must set before calling .lib
.temp  25           * Override temperature by setting it before .lib
.protect            * Don't print the contents of library
                    * Load the library for process corner
* CHANGE THE FOLLOWING LINE IN ALL SPICE FILES FOR PMC-SIERRA
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT
.unprotect          * Resume printing SPICE deck
.opt scale=0.090u     * Set lambda

* Save results of simulation for viewing
.options post

*************************************************************************
* Define power supply
*************************************************************************
.global Vdd   Gnd
Vdd   Vdd   Gnd   'Sup'   * Sup is set above
*************************************************************************
* Top level simulation netlist
*************************************************************************
mp     drainp gatep Vdd Vdd PE2 l=2 w=8 ad=20 pd=4 as=20 ps=4
mn     drainn gaten Gnd Gnd NE2 l=2 w=8 ad=20 pd=4 as=20 ps=4

****new*****
Vdsp Vdd drainp dc
Vgsp Vdd gatep dc
Vdsn drainn 0 dc
Vgsn gaten 0 dc
***********
*.dc    Vdsp  0 'Sup"Sup/20' Vgsp 0 'Sup' 'Sup/3'
.dc     Vdsn  0 'Sup"Sup/20' Vgsn 0 'Sup' 'Sup/3'
.plot dc        I1(mp)
.plot dc        I1(mn)
*************************************************************************
* End of Deck
*************************************************************************
.end
```

Appendix A.2 Sub-threshold current HSPICE Source Code

```
* Vt, Subthreshold current and Temperature
**************************************************************************
* Set supply and library
**************************************************************************
.param Sup=1.8      * Must set before calling .lib
.temp  25           * ADJUST THIS TO CHANGE TEMP
.protect            * Don't print the contents of library
                    * Load the library for process corner
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT
.unprotect          * Resume printing SPICE deck
.opt scale=0.090u       * Set lambda

* Save results of simulation for viewing
.options post

**************************************************************************
* Define power supply
**************************************************************************
.global Vdd   Gnd
Vdd   Vdd   Gnd   'Sup'   * Sup is set above
**************************************************************************
* Top level simulation netlist
**************************************************************************
mp    Gnd   gatep Vdd Vdd PE2 l=2 w=20 ad=20 pd=4 as=20 ps=4
mn    Vdd   gaten Gnd Gnd NE2 l=2 w=8 ad=20 pd=4 as=20 ps=4
****new*****
Vgsp gatep 0 dc
Vgsn gaten 0 dc
************
*.dc    Vgsp 0 'Sup' 'Sup/20'
.dc     Vgsn 0 'Sup' 'Sup/20'
*.plot dc       I1(mp)
.plot dc        I1(mn)
**************************************************************************
* End of Deck
**************************************************************************
.end
```

Appendix A.3 Voltage transfer characteristics HSPICE Source Code

```
* VTC
*********************************************************************
* Set supply and library
*********************************************************************
.param Sup=1.8      * ADJUST THIS TO CHANGE VTC
.temp  25           * Override temperature by setting it before .lib
.protect            * Don't print the contents of library
                    * Load the library for process corner

.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT
.unprotect          * Resume printing SPICE deck
.opt scale=0.090u       * Set lambda

* Save results of simulation for viewing
.options post

*********************************************************************
* Define power supply
*********************************************************************
.global Vdd   Gnd
Vdd   Vdd   Gnd 'Sup'
*********************************************************************
* Top level simulation netlist
*********************************************************************
m1    Out In1 Vdd Vdd            PE2  l=2 w=16 ad=200 as=200 pd=40 ps=40
m2    Out In1 0 0          NE2 l=2 w=8 ad=100 as=100 pd=20 ps=20
*********************************************************************
* Stimulus
*********************************************************************
Vin1    In1     Gnd  DC
*********************************************************************
* Simulation
*********************************************************************
* for Id vs. Vds
.dc Vin1 0 'Sup' 'Sup/20'

*********************************************************************
* Measurements
*********************************************************************
.plot DC V(Out)
.plot DC I(Vdd)
```

```
*************************************************************************
* End of Deck
*************************************************************************
.end
```

Appendix A.4 Five Stage Inverter Chain HSPICE Source Code

```
* Five stage inverter chain
*************************************************************************
* Set supply and library
*************************************************************************
.param Supply=1.8  * Must set before calling .lib
*.temp  25         * Override temperature by setting it before .lib
.protect           * Don't print the contents of library
                   * Load the library for process corner
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT
.unprotect         * Resume printing SPICE deck
.opt scale=0.090u        * Set lambda

* Save results of simulation for viewing
.options post

*************************************************************************
* Define power supply
*************************************************************************
.global Vdd   Gnd
Vdd   Vdd   Gnd 1.8
*************************************************************************
* Top level simulation netlist
*************************************************************************

* 10X inverter
m1    Out In1 Vdd Vdd          PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m2    Out In1 0 0         NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m3    Out1 Out Vdd Vdd   PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m4    Out1 Out 0 0        NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m5    Out2 Out1 Vdd Vdd PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m6    Out2 Out1 0 0            NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m7    Out3 Out2 Vdd Vdd PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m8    Out3 Out2 0 0            NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
```

```
m9     Out4 Out3 Vdd Vdd PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m10    Out4 Out3 0 0          NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m11    Out5 Out4 Vdd Vdd PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m12    Out5 Out4 0 0          NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
*********************************************************************
* Stimulus
*********************************************************************
Vin1     In1      Gnd  PWL (0 0 25ps 0 30ps 1.8 195ps 1.8 200ps 0)
*********************************************************************
* Simulation
*********************************************************************
.tran 5ps 350ps

* You can add other requested simulations here
* or write your own spice deck
*********************************************************************
* Measurements
*********************************************************************
.print tran V(In1) V(Out4)

*********************************************************************
* End of Deck
*********************************************************************
.end
```

Appendix A.5 Five Stage Ring Oscillator HSPICE Source Code

```
* Five stage ring oscillator
*********************************************************************
* Set supply and library
*********************************************************************
.param Supply=1.8  * Must set before calling .lib
*.temp  25         * Override temperature by setting it before .lib
.protect           * Don't print the contents of library
                   * Load the library for process corner
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT
.unprotect         * Resume printing SPICE deck
.opt scale=0.090u       * Set lambda

* Save results of simulation for viewing
.options post
*********************************************************************
* Define power supply
```

```
*********************************************************************
.global Vdd   Gnd
Vdd   Vdd   Gnd 1.8
*********************************************************************
* Top level simulation netlist
*********************************************************************

* 10X inverter
m1    Out In1 Vdd Vdd          PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m2    Out In1 0 0          NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m3    Out1 Out Vdd Vdd   PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m4    Out1 Out 0 0         NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m5    Out2 Out1 Vdd Vdd PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m6    Out2 Out1 0 0              NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m7    Out3 Out2 Vdd Vdd PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m8    Out3 Out2 0 0              NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
* 10X inverter
m9    In1 Out3 Vdd Vdd   PE2  l=2 w=40 ad=200 as=200 pd=40 ps=40
m10   In1 Out3 0 0         NE2  l=2 w=20 ad=100 as=100 pd=20 ps=20
*********************************************************************
* Stimulus
*********************************************************************
.ic V(In1)=1.8V V(out)=0.0V V(out1)=1.8V V(out2)=0.0V V(out3)=1.8V
*********************************************************************
* Simulation
*********************************************************************
.tran 5ps 900ps uic

* You can add other requested simulations here
* or write your own spice deck
*********************************************************************
* Measurements
*********************************************************************
.print tran V(In1) V(Out3)
*********************************************************************
* End of Deck
*********************************************************************
.end
```

Appendix A.6 Coupling Capacitance HSPICE Source Code

```
* Coupling Capacitance
**************************************************************************
* Set supply and library
**************************************************************************
.param Supply=1.8  * Must set before calling .lib
*.temp  25         * Override temperature by setting it before .lib
.protect           * Don't print the contents of library
                   * Load the library for process corner
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT
.unprotect         * Resume printing SPICE deck
.opt scale=0.090u        * Set lambda

* Save results of simulation for viewing
.options post

**************************************************************************
* Define power supply
**************************************************************************
.global Vdd   Gnd
Vdd   Vdd   Gnd 1.8
**************************************************************************
* Top level simulation netlist
**************************************************************************

* 50X inverter
m1    Out In1 Vdd Vdd          PE2   l=2  w=200  ad=1000  as=1000  pd=200
ps=200
m2    Out In1 0 0          NE2   l=2 w=100 ad=500 as=500 pd=100 ps=100
* 1X inverter
*m3   Out1 Vdd Vdd Vdd  PE2   l=2 w=2 ad=200 as=200 pd=40 ps=40
*m4   Out1 Vdd 0 0        NE2   l=2 w=2 ad=100 as=100 pd=20 ps=20
* 40X inverter
m3    Out1 Vdd Vdd Vdd  PE2   l=2 w=160 ad=800 as=800 pd=160 ps=160
m4    Out1 Vdd 0 0        NE2   l=2 w=80 ad=200 as=200 pd=80 ps=80
Cg1   Out 0   50fF   *adjust this to compute Ceff
Cc    Out1 Out   100fF  * adjust this to compute Cg
Cg2   Out1 0 60fF
**************************************************************************
* Stimulus
**************************************************************************
Vin1    In1     Gnd  PWL (0 1.8 25ps 1.8 30ps 0 195ps 0 200ps 0)
**************************************************************************
```

```
* Simulation
**************************************************************************
.tran 5ps 350ps

* You can add other requested simulations here
* or write your own spice deck
**************************************************************************
* Measurements
**************************************************************************
.print tran V(Out) V(Out1)
.plot tran V(Out) V(Out1)
**************************************************************************
* End of Deck
**************************************************************************
.end
```

Appendix A.7 Added resistance to the power grid HSPICE Source Code

```
* Add Resistance in Power Grid
**************************************************************************
.param Supply=1.8                                   * Supply Voltage
.temp  25                                       * Temperature
.protect
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT

.unprotect
.opt scale=0.090u                                   * Value of lambda
.options post                                       * Output Options.

.param        rampTime=100p     * Slope of input
+       period=10n   * Period
+       wireLength=2         * Length of the interconnect between inverters (in µm)
+       wireWidth=0.2        * Width of the interconnect between inverters (in µm)
+       rSquare=42m          * Resistance per unit square
+       cLength=0.2f * Capacitance per micron
+       gridLength=2 * Length of the power line in microns
+       gridWidth=0.4        * Width of the power line in microns
+       gridRSquare=21m   * Resistance per unit square for power grid

.globalVdd    Gnd           * Global Parameters for Subcircuit
Vdd    Vdd    Gnd    'Supply'  * Supply Voltage

Vinu    in1    Gnd     pulse 'Supply'        0                       * Rising Input
+       100p   rampTime     rampTime     'period/2-rampTime'    period
```

```
.subckt      inv    in     out    Vp       * This is an inverter
mp    out    in     Vp     Vp     PE2
+     l=2    w=16
+     ad=0   pd=0
+     as=0   ps=0
mn    out    in     Gnd    Gnd    NE2
+     l=2    w=8
+     ad=0   pd=0
+     as=0   ps=0
.ends

.subckt      signalWire   n1     n2
C1    n1     Gnd    'cLength*wireLength/2'
Rpi   n1     n2     'rSquare*wireLength/wireWidth'
C2    n2     Gnd    'cLength*wireLength/2'
.ends

xinv1  in1   out1   Vp1   inv   M=1
xwire1 out1  in2    signalWire
rgrid1 Vdd   Vp1    'gridRSquare*gridLength/gridWidth'

xinv2  in2   out2   Vp2   inv   M=1
xwire2 out2  in3    signalWire
rgrid2 Vp1   Vp2    'gridRSquare*gridLength/gridWidth'

xinv3  in3   out3   Vp3   inv   M=1
xwire3 out3  in4    signalWire
rgrid3 Vp2   Vp3    'gridRSquare*gridLength/gridWidth'

xinv4  in4   out4   Vp4   inv   M=1
xwire4 out4  in5    signalWire
rgrid4 Vp3   Vp4    'gridRSquare*gridLength/gridWidth'

xinv5  in5   out5   Vp5   inv   M=1
xwire5 out5  in6    signalWire
rgrid5 Vp4   Vp5    'gridRSquare*gridLength/gridWidth'

xinv6  in6   out6   Vp6   inv   M=1
xwire6 out6  in7    signalWire
rgrid6 Vp5   Vp6    'gridRSquare*gridLength/gridWidth'

xinv7  in7   out7   Vp7   inv   M=1
xwire7 out7  in8    signalWire
rgrid7 Vp6   Vp7    'gridRSquare*gridLength/gridWidth'
```

```
xinv8  in8    out8   Vp8    inv    M=1
xwire8 out8   in9    signalWire
rgrid8 Vp7    Vp8    'gridRSquare*gridLength/gridWidth'

xinv9  in9    out9   Vp9    inv    M=1
xwire9 out9   in10   signalWire
rgrid9 Vp8    Vp9    'gridRSquare*gridLength/gridWidth'

xinv10 in10   out10  Vp10   inv    M=1
xwire10 out10 in11   signalWire
rgrid10 Vp9   Vp10   'gridRSquare*gridLength/gridWidth'

xinv11 in11   out11  Vp11   inv    M=1
xwire11 out11 in12   signalWire
rgrid11 Vp10  Vp11   'gridRSquare*gridLength/gridWidth'

xinv12 in12   out12  Vp12   inv    M=1
xwire12 out12 in13   signalWire
rgrid12 Vp11  Vp12   'gridRSquare*gridLength/gridWidth'

xinv13 in13   out13  Vp13   inv    M=1
xwire13 out13 in14   signalWire
rgrid13 Vp12  Vp13   'gridRSquare*gridLength/gridWidth'

xinv14 in14   out14  Vp14   inv    M=1
xwire14 out14 in15   signalWire
rgrid14 Vp13  Vp14   'gridRSquare*gridLength/gridWidth'

xinv15 in15   out15  Vp15   inv    M=1
xwire15 out15 in16   signalWire
rgrid15 Vp14  Vp15   'gridRSquare*gridLength/gridWidth'

xinv16 in16   out16  Vp16   inv    M=1
xwire16 out16 in17   signalWire
rgrid16 Vp15  Vp16   'gridRSquare*gridLength/gridWidth'

xinv17 in17   out17  Vp17   inv    M=1
xwire17 out17 in18   signalWire
rgrid17 Vp16  Vp17   'gridRSquare*gridLength/gridWidth'

xinv18 in18   out18  Vp18   inv    M=1
xwire18 out18 in19   signalWire
rgrid18 Vp17  Vp18   'gridRSquare*gridLength/gridWidth'

xinv19 in19   out19  Vp19   inv    M=1
xwire19 out19 in20   signalWire
```

```
rgrid19 Vp18   Vp19   'gridRSquare*gridLength/gridWidth'

xinv20  in20   out20  Vp20   inv    M=1
xwire20 out20  in21   signalWire
rgrid20 Vp19   Vp20   'gridRSquare*gridLength/gridWidth'

xinv21  in21   out21  Vp21   inv    M=1
xwire21 out21  in22   signalWire
rgrid21 Vp20   Vp21   'gridRSquare*gridLength/gridWidth'

xinv22  in22   out22  Vp22   inv    M=1
xwire22 out22  in23   signalWire
rgrid22 Vp21   Vp22   'gridRSquare*gridLength/gridWidth'

xinv23  in23   out23  Vp23   inv    M=1
xwire23 out23  in24   signalWire
rgrid23 Vp22   Vp23   'gridRSquare*gridLength/gridWidth'

xinv24  in24   out24  Vp24   inv    M=1
xwire24 out24  in25   signalWire
rgrid24 Vp23   Vp24   'gridRSquare*gridLength/gridWidth'

xinv25  in25   out25  Vp25   inv    M=1
xwire25 out25  in26   signalWire
rgrid25 Vp24   Vp25   'gridRSquare*gridLength/gridWidth'

xinv26  in26   out26  Vp26   inv    M=1
xwire26 out26  in27   signalWire
rgrid26 Vp25   Vp26   'gridRSquare*gridLength/gridWidth'

xinv27  in27   out27  Vp27   inv    M=1
xwire27 out27  in28   signalWire
rgrid27 Vp26   Vp27   'gridRSquare*gridLength/gridWidth'

xinv28  in28   out28  Vp28   inv    M=1
xwire28 out28  in29   signalWire
rgrid28 Vp27   Vp28   'gridRSquare*gridLength/gridWidth'

xinv29  in29   out29  Vp29   inv    M=1
xwire29 out29  in30   signalWire
rgrid29 Vp28   Vp29   'gridRSquare*gridLength/gridWidth'

xinv30  in30   out30  Vp30   inv    M=1
xwire30 out30  in31   signalWire
rgrid30 Vp29   Vp30   'gridRSquare*gridLength/gridWidth'
```

```
xinv31  in31   out31  Vp31   inv    M=1
xwire31 out31  in32   signalWire
rgrid31 Vp30   Vp31   'gridRSquare*gridLength/gridWidth'

xinv32  in32   out32  Vp32   inv    M=1
xwire32 out32  in33   signalWire
rgrid32 Vp31   Vp32   'gridRSquare*gridLength/gridWidth'

.tran   6p     600p
.plot   tran V(Vp31)

.end
```

Appendix A.8 Added more resistance to the power grid HSPICE Source Code

```
* More Resistance in Power Grid
*************************************************************************
.param Supply=1.8                                   * Supply Voltage
.temp  25                                         * Temperature
.protect
.lib
'/home/liblib/fab1/techdata/v1_11/models/b3_spdv_v1_11/standalone/hspice/PR
OCESS.L' TT

.unprotect
.opt scale=0.090u                                   * Value of lambda
.options post                                       * Output Options.

.param        rampTime=100p     * Slope of input
+       period=10n   * Period
+       wireLength=2         * Length of the interconnect between inverters (in µm)
+       wireWidth=0.2        * Width of the interconnect between inverters (in µm)
+       rSquare=42m          * Resistance per unit square
+       cLength=0.2f * Capacitance per micron
+       gridLength=1000      * Length of the power line in microns
+       gridWidth=0.4        * Width of the power line in microns
+       gridRSquare=21m   * Resistance per unit square for power grid

.globalVdd    Gnd           * Global Parameters for Subcircuit
Vdd    Vdd    Gnd    'Supply'  * Supply Voltage

Vinu    in1    Gnd     pulse 'Supply'       0                        * Rising Input
+       100p   rampTime     rampTime     'period/2-rampTime'    period
```

```
.subckt      inv    in     out    Vp       * This is an inverter
mp    out    in     Vp     Vp     PE2
+     l=2    w=16
+     ad=0   pd=0
+     as=0   ps=0
mn    out    in     Gnd    Gnd    NE2
+     l=2    w=8
+     ad=0   pd=0
+     as=0   ps=0
.ends

.subckt      signalWire   n1     n2
C1    n1     Gnd    'cLength*wireLength/2'
Rpi   n1     n2     'rSquare*wireLength/wireWidth'
C2    n2     Gnd    'cLength*wireLength/2'
.ends

xinv1  in1   out1   Vp1   inv   M=1
xwire1 out1  in2    signalWire
rgrid1 Vdd   Vp1    'gridRSquare*gridLength/gridWidth'

xinv2  in2   out2   Vp2   inv   M=1
xwire2 out2  in3    signalWire
rgrid2 Vp1   Vp2    'gridRSquare*gridLength/gridWidth'

xinv3  in3   out3   Vp3   inv   M=1
xwire3 out3  in4    signalWire
rgrid3 Vp2   Vp3    'gridRSquare*gridLength/gridWidth'

xinv4  in4   out4   Vp4   inv   M=1
xwire4 out4  in5    signalWire
rgrid4 Vp3   Vp4    'gridRSquare*gridLength/gridWidth'

xinv5  in5   out5   Vp5   inv   M=1
xwire5 out5  in6    signalWire
rgrid5 Vp4   Vp5    'gridRSquare*gridLength/gridWidth'

xinv6  in6   out6   Vp6   inv   M=1
xwire6 out6  in7    signalWire
rgrid6 Vp5   Vp6    'gridRSquare*gridLength/gridWidth'

xinv7  in7   out7   Vp7   inv   M=1
xwire7 out7  in8    signalWire
rgrid7 Vp6   Vp7    'gridRSquare*gridLength/gridWidth'

xinv8  in8   out8   Vp8   inv   M=1
```

```
xwire8 out8   in9    signalWire
rgrid8 Vp7    Vp8    'gridRSquare*gridLength/gridWidth'

xinv9  in9    out9   Vp9    inv    M=1
xwire9 out9   in10   signalWire
rgrid9 Vp8    Vp9    'gridRSquare*gridLength/gridWidth'

xinv10 in10   out10  Vp10   inv    M=1
xwire10 out10 in11   signalWire
rgrid10 Vp9   Vp10   'gridRSquare*gridLength/gridWidth'

xinv11 in11   out11  Vp11   inv    M=1
xwire11 out11 in12   signalWire
rgrid11 Vp10  Vp11   'gridRSquare*gridLength/gridWidth'

xinv12 in12   out12  Vp12   inv    M=1
xwire12 out12 in13   signalWire
rgrid12 Vp11  Vp12   'gridRSquare*gridLength/gridWidth'

xinv13 in13   out13  Vp13   inv    M=1
xwire13 out13 in14   signalWire
rgrid13 Vp12  Vp13   'gridRSquare*gridLength/gridWidth'

xinv14 in14   out14  Vp14   inv    M=1
xwire14 out14 in15   signalWire
rgrid14 Vp13  Vp14   'gridRSquare*gridLength/gridWidth'

xinv15 in15   out15  Vp15   inv    M=1
xwire15 out15 in16   signalWire
rgrid15 Vp14  Vp15   'gridRSquare*gridLength/gridWidth'

xinv16 in16   out16  Vp16   inv    M=1
xwire16 out16 in17   signalWire
rgrid16 Vp15  Vp16   'gridRSquare*gridLength/gridWidth'

xinv17 in17   out17  Vp17   inv    M=1
xwire17 out17 in18   signalWire
rgrid17 Vp16  Vp17   'gridRSquare*gridLength/gridWidth'

xinv18 in18   out18  Vp18   inv    M=1
xwire18 out18 in19   signalWire
rgrid18 Vp17  Vp18   'gridRSquare*gridLength/gridWidth'

xinv19 in19   out19  Vp19   inv    M=1
xwire19 out19 in20   signalWire
rgrid19 Vp18  Vp19   'gridRSquare*gridLength/gridWidth'
```

```
xinv20 in20   out20  Vp20   inv    M=1
xwire20 out20  in21   signalWire
rgrid20 Vp19   Vp20   'gridRSquare*gridLength/gridWidth'

xinv21 in21   out21  Vp21   inv    M=1
xwire21 out21  in22   signalWire
rgrid21 Vp20   Vp21   'gridRSquare*gridLength/gridWidth'

xinv22 in22   out22  Vp22   inv    M=1
xwire22 out22  in23   signalWire
rgrid22 Vp21   Vp22   'gridRSquare*gridLength/gridWidth'

xinv23 in23   out23  Vp23   inv    M=1
xwire23 out23  in24   signalWire
rgrid23 Vp22   Vp23   'gridRSquare*gridLength/gridWidth'

xinv24 in24   out24  Vp24   inv    M=1
xwire24 out24  in25   signalWire
rgrid24 Vp23   Vp24   'gridRSquare*gridLength/gridWidth'

xinv25 in25   out25  Vp25   inv    M=1
xwire25 out25  in26   signalWire
rgrid25 Vp24   Vp25   'gridRSquare*gridLength/gridWidth'

xinv26 in26   out26  Vp26   inv    M=1
xwire26 out26  in27   signalWire
rgrid26 Vp25   Vp26   'gridRSquare*gridLength/gridWidth'

xinv27 in27   out27  Vp27   inv    M=1
xwire27 out27  in28   signalWire
rgrid27 Vp26   Vp27   'gridRSquare*gridLength/gridWidth'

xinv28 in28   out28  Vp28   inv    M=1
xwire28 out28  in29   signalWire
rgrid28 Vp27   Vp28   'gridRSquare*gridLength/gridWidth'

xinv29 in29   out29  Vp29   inv    M=1
xwire29 out29  in30   signalWire
rgrid29 Vp28   Vp29   'gridRSquare*gridLength/gridWidth'

xinv30 in30   out30  Vp30   inv    M=1
xwire30 out30  in31   signalWire
rgrid30 Vp29   Vp30   'gridRSquare*gridLength/gridWidth'

xinv31 in31   out31  Vp31   inv    M=1
```

```
xwire31 out31   in32    signalWire
rgrid31 Vp30    Vp31    'gridRSquare*gridLength/gridWidth'

xinv32  in32    out32   Vp32    inv     M=1
xwire32 out32   in33    signalWire
rgrid32 Vp31    Vp32    'gridRSquare*gridLength/gridWidth'

.tran   6p      600p
.plot   tran V(Vp32)

.end
```

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