DEVELOPING AN EFFICIENT APPROACH TO FABRICATE ELECTRIC CONTACTS ON NANOWIRES

by

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ABSTRACT

Nanostructured materials can have distinctive properties relative to their bulk materials. To determine the electrical properties of nanostructured materials it is important to be able to make electrical connection to these materials. However, the nanoscale dimensions of these materials demand techniques capable of accurate alignment of patterns to the features of the nanostructure. This thesis demonstrates the development of techniques to position metal electrodes onto nanowires to measure the conductivity of these materials. Two lithographic techniques for positioning electrodes on nanowires were newly developed: optical microscope projection photolithography and electron-beam lithography. Our time- and cost-effective optical lithographic approach allows the overlay of electrodes on nanostructures nearly a hundred times faster and a hundred times less costly than previous techniques. Also presented is a new approach to align patterns to single nanowires by electron-beam lithography. Preliminary studies on the electrical characterization of nanowires were also performed using these lithographically defined structures.

Keywords: photolithography, electron-beam lithography, projection lithography, nanofabrication, nanoelectrodes

Subject Terms: microscope projection photolithography, electron-beam lithography, electrical characterization

To my mother, Azam,

You are my inspiration in life.

I love you and to you I dedicate this thesis.

“Things should be made as simple as possible, but not any simpler.”

Albert Einstein

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TABLE OF CONTENTS

Approval ... ii
Abstract ... iii
Dedication ... iv
Quotation ... v
Acknowledgements ... vi
Table of Contents ... ix
List of Figures ... xii
List of Tables ... xx
Glossary of abbreviations and symbols ... xxi
Chapter 1: An Introduction to the Field of this Research ... 1
1.1 Goal of this Thesis ... 1
1.2 Technology Trends towards Nanoscale ... 2
1.3 Semiconducting Nanowires ... 4
1.3.1 Semiconductor Devices ... 6
1.3.2 Semiconducting Materials ... 8
1.3.3 Electronic Band Structure (Band-Gap Energy) ... 9
1.3.4 Semiconducting Selenium ... 11
1.4 Synthesis of Semiconductor Nanowires ... 14
1.4.1 Choice of Bottom-Up Approach for Synthesis of Nanostructures ... 15
1.5 Association of One-Dimensional Nanostructures in Devices ... 16
1.6 Top-Down Fabrication Process for Incorporation of Nanostructures in Devices (An Overview of this Thesis) ... 18
Chapter 2: Microscope Projection Photolithography on Nanowires ... 23
2.1 Lithographic Techniques for Device Fabrication ... 23
2.2 Various Techniques of Resist Exposure ... 31
2.2.1 Exposure of Resists via Contact Photolithographic Techniques ... 32
2.2.2 Exposure of Resists via Proximity Photolithographic Technique ... 33
2.2.3 Exposure of Resists via Projection Photolithographic Techniques ... 34
2.3 Microscope Projection Photolithography ... 37
2.4 Fundamentals of an Optical Microscope ... 39
2.4.1 Physics Behind Microscope Projection Photolithography ... 39
2.4.2 Fundamental Equations for Photolithographic Techniques ... 46

2.5 An Overview of the Fabrication Steps to Overlay Electric Contacts on Selenium Nanowires 51
2.5.1 Growth of an Oxide Layer on Silicon Wafer Substrates 54
2.5.2 Pre-Treatment of Silicon Wafers 55
2.5.3 Spin-Casting a Resist Layer 56
2.5.4 Pre-Exposure Bake of Resist 58
2.5.5 Irradiation of Resist 58
2.5.6 Post-Exposure Bake of Resist 59
2.5.7 Developing of the Resist Coated Substrate After Post-Exposure Bake 59
2.5.8 Hard Bake of Resist 61
2.5.9 Metal Deposition on Resist Covered Silicon Wafers 61
2.5.10 Lift-Off of Metal Layer from Resist-Coated Wafers 63
2.6 Experimental Details & Discussions for Fabrication of Metal Contacts on Selenium Nanowires via Microscope Projection Photolithography 64
2.6.1 Silicon Wafer Substrate Pre-Treatment 65
2.6.2 Deposition of an Ultraviolet Sensitive Photoresist onto Silicon Wafers 68
2.6.3 Irradiation of Photoresist via UV Light Source from an Optical Microscope 71
2.6.4 Developing of Photoresist 90
2.6.5 Metal Deposition on Developed Photoresist Coated Silicon Wafers 95
2.6.6 Lift-Off of Metal-Covered Photoresist 96
2.7 Conclusions and Discussion 98

Chapter 3: Directed Electron-Beam Lithography on Nanowires 100

3.1 Electron-Beam Lithography Technique 100
3.2 Choice of Resist for Electron-Beam Exposure 107
3.3 Variations to Previously Developed Experimental Steps to Overcome Lift-Off Challenges 111
3.4 Experimental Details 115
3.4.1 Deposition of Electron-Beam Resist on Silicon Wafers 115
3.4.2 Exposure of Electron Resist with a Beam of Electrons 116
3.4.3 Developing of Electron Resist 120
3.4.4 Metal Deposition on Developed Electron Resist Coated Silicon Wafers 122
3.4.5 Lift-Off of Metal Covered Electron Resist 122
3.4.6 Challenges of Gold Layer Lift-Off from Resist Covered Selenium Nanowires 124
3.5 Conclusions and Discussion 125

Chapter 4: Conductivity Measurement of Selenium Nanowires 127

4.1 Conductivity of Materials 127
4.1.1 Current-Voltage Characteristics 128
4.2 Electrical Characterization 130
4.2.1 Electrical Measurement Using a Wire Bonder 130
4.2.2 Electrical Measurement Using a Probe Station 131
4.2.3 AFM and SEM Imaging of Selenium Nanowires 135
4.2.4 Assessment of the Set-Up of the Metal Electrodes and Resistivity Calculations 138

4.3 Conclusions and Discussion 146
Chapter 5: Concluding Remarks On Impacts of this Research 147
5.1 Final Conclusions and Implications of this Work 147
5.2 Future Directions of This Work 150
Appendix A: Synthesis of Selenium Nanowires 152
Appendix B: Metal deposition by Thermal Evaporation 156
References 158

LIST OF FIGURES

Figure 1-1: History and future projection for minimum feature sizes in silicon chips, according to the National Technology Roadmap for Semiconductors (*NTRS*).[19, 179-181] 3

Figure 1-2: Gross world product (GWP) and sales volume of the semiconductor industry compared to other industries such as electronics, automobile, and steel from 1980 to 2000 and projected to 2010.[23] 7

Figure 1-3: Conductivity of some insulators, semiconductors and conductors shown on a scale. 8

Figure 1-4: A simplified diagram of relative band-gap energies for electronic insulating, semiconducting and conducting materials..... 10

Figure 1-5: A schematic overview of the fabrication process. 21

Figure 2-1: A general schematic process for lithographic steps (part I). Continuation of this schematic is on the next page. 26

Figure 2-2: Part II and continuation of lithographic steps from Figure 2-1 on the previous page. 27

Figure 2-3: The line spectrum of a mercury lamp (HBO 100/103 mercury short arc lamp purchased from Zeiss). *(Courtesy of Carl Zeiss Company).*[118] 30

Figure 2-4: A schematic depicting '*contact photolithography.'* The patterned photomask is in contact with photoresist. 32

Figure 2-5: A schematic depicting *'proximity photolithography.'* 34

Figure 2-6: A schematic depicting *'projection photolithography.'* 35

Figure 2-7: Schematic of the set-up for microscope projection photolithography used by Palmer and Decker in 1973.[121] 38

Figure 2-8: Schematic of a basic compound optical microscope. 39

Figure 2-9: Conjugate planes within a cross-section of an optical microscope. *(Courtesy of Carl Zeiss Company)* 42

Figure 2-10: Schematic of the optical components of a microscope adjusted for Köhler illumination. In parts b) and c) the conjugate planes for the image-forming and illuminating sets are indicated by crossover points of the ray traces. 45

Figure 2-11: A schematic of longitudinal slice of a microscope objective lens with the cone of light revealing the angular aperture 'α', where image-forming light waves pass through the specimen and enter the objective lens in an inverted cone as illustrated. Focal length '*f*' and diameter of aperture '*D*' are also shown in the figure. 47

Figure 2-12: A bright field optical micrograph of two electrodes overlaid on a nanowire. 51

Figure 2-13: Part I of a schematic representation of the steps involved in overlaying metal contacts on selenium nanowires. See part II in Figure 2-14 on page 53. 52

Figure 2-14: Part II of a schematic representation of the steps involved in overlaying metal contacts on selenium nanowires. 53

Figure 2-15: Schematic illustration of the key components for coating a substrate with resist by a spin-coating process. 56

Figure 2-16: Spin curves provided by MicroChem. Corporation for 2% PMMA in anisole (w/v), depicting different film thickness obtained from spin speed of the resist coated substrate.[158] 57

Figure 2-17: A schematic depiction of the possible developing outcomes on a resist coated substrate. Note that only the figure labelled 'correctly developed' is ideal and other figures are provided for comparison purposes. 60

Figure 2-18: A simplified diagram of a thermal evaporator instrument. 63

Figure 2-19: A cross-sectional schematic of substrates coated with resist before and after the lift-off process. 64

Figure 2-20: A graph of the thermal heating process for oxide growth on silicon wafer substrates. 66

Figure 2-21: A schematic representation of an oxidized silicon wafer with dispersed selenium nanowires deposited onto its surface. 67

Figure 2-22: Diazonaphtoquinone is the photoactive component of SPR-220 resist (manufactured by Rohm and Hass Electronic Materials) that goes through the outlined chemical reactions after UV irradiation. 69

Figure 2-23: Spin speed curves provided by Rohm and Haas. Corporation for the SPR 220 photoresist series. [163] The vertical dashed line points to the spin speed used for the experiments with this resist

and the horizontal line points to the resultant estimated film thickness of ~1.3 μm. 71

Figure 2-24: An image of the filter cube of a Zeiss microscope shown in (a).[157] *(Courtesy of Carl Zeiss Company).* In (b) a three-dimensional view of this filter cube is shown pointing to the locations (1 and 2) at which the photomask was positioned for testing MPP. (c) A two-dimensional view of photomask placement in filter cube..... 72

Figure 2-25: An image of the cross section of a Zeiss microscope (illustrated previously in Figure 2-9 depicting the two sets of conjugates planes), illustrating the relative placement of the filter cube with respect to other optical components in the microscope.[157] *(Courtesy of Carl Zeiss Company)*..... 73

Figure 2-26: An image taken by bright-field optical microscopy demonstrating patterning of an octagon of gold onto selenium nanowires via the MPP technique. The photomask was the projected pattern of ~3 mm diameter field aperture using the 5x objective lens with NA of 0.13..... 75

Figure 2-27: A schematic depicting the two separate exposures performed to produce the pattern shown in Figure 2-28. 76

Figure 2-28: Two separate exposure steps were performed using the 5x objective lens (with NA of 0.13) and the ~3 mm diameter field aperture (overlaid pattern on nanowire) and one slightly larger (overlaid pattern on the previously exposed region). This bright-field optical image was taken after developing the exposed photoresist using the red filter to avoid UV exposure of other parts of resist before the metal deposition step. 77

Figure 2-29: An early design of the mask holder for positioning a projection mask within the light path of an optical microscope. 78

Figure 2-30: A schematic representation of the Zeiss microscope and two versions of the mask holder shown in “b” and “c”. Part labelled as “b” is a depiction of an early design of the mask holder, and part labelled as “c” is a newer version, which is detailed in Figure 2-31 and Figure 2-32.[118] *(Courtesy of Carl Zeiss Company)* 79

Figure 2-31: A schematic of the (a) front and (b) back of the latest version of the mask holder, as well as the (c) position of the photomask. The blue arrow in (a) indicates rotation of wheel which in turn moves the belt that rotates the screw at the end of which is mounted the photomask as shown in (b). As shown, the photomask moves towards the image-forming conjugate plane of Köhler diaphragm by rotation of the wheel. 79

Figure 2-32: Pictures of the front and back of the mask holder (top) and side view of the holder to show the ‘in’ and ‘out’ positions of the photomask achieved by rotating the wheel. 80

Figure 2-33: Detailed view of “A” from Figure 2-30. Slot labelled ‘B’ is the position where the mask holder is mounted within the light path of the optical microscope. The width of this passage is 8 mm, as indicated by the red line. 81

Figure 2-34: The mask holder needs to be positioned in the rail “B” installed in the small passage on the left of component labelled “C”. Component “D”, identical to “C”, is shown to provide a clearer image of similar components inside the microscope. 81

Figure 2-35: Overlay of a photomask on resist coated nanowires on a substrate using a given objective lens. 82

Figure 2-36: Two patterns used in MPP, which are discussed in more detail towards the end of this section: a) This pattern was used to optimize the focus of the mask; b) this pattern was used to compare the size reduction and resolution of different objective lenses. 83

Figure 2-37: An image of a photomask before and after prolonged (~30 min) exposure of UV radiation. The image on the right shows a deformed mask due to excess heating by the UV lamp. Note that after roughly ten exposures (~15-30 s/exposure) this deformation is not seen. The insets show higher magnification images of the center of the photomask before and after exposure. 84

Figure 2-38: A schematic of the fabrication process to make gold masks on round glass slides. A cleaned glass slide is used for Cr/Au deposition followed by spin casting of photoresist. After the contact photolithography step the substrate is developed in a developing solution to uncover the underlying gold layer. The exposed gold layer is etched using a Cr/Au etchant to create a transparent region and to produce the gold masks. 86

Figure 2-39: Images of two gold-coated, glass MPP photomasks acquired by bright-field optical microscopy depicting the etched and un-etched regions of gold film on the glass slide forming a pattern to allow selective UV exposure. 87

Figure 2-40: Progressive focusing of the photomask within the mask holder as the wheel is turned to approach the conjugate plane. The improvement in the focus can be seen from (a) through (f) as the mask moves closer to the conjugate image plane. Comparison of image (f) with that in Figure 2-36 is indicative that the conjugate image plane has not yet been reached. The lateral distance within the ray tube of the optical microscope that the photomask has moved from (a) to (f) is 6.5 mm. Note that there

is no scale bar for these images since regardless of the magnification of the lens used, the focusing of the photomask pattern will not change. 88

Figure 2-41: Images acquired by bright-field optical microscopy using a 5x objective lens with NA of 0.13. (a) An under-exposed (b) properly exposed patterns taken after developing using a projection of the pattern shown in Figure 2-36-b. 90

Figure 2-42: An image acquired by bright-field optical microscopy of the projected pattern using a photomask with the pattern shown in Figure 2-36-a using a 10x objective lens with NA of 0.25, after the developing process. 91

Figure 2-43: Images acquired by bright-field optical microscopy of the projected pattern using the photomask pattern shown in Figure 2-36-b with a 5x objective lens with NA of 0.13 (shown in a) and a 10x objective lens with NA of 0.25 (shown in b), after developing process. The insets depict the drawing of the anticipated patterns. The out of focus projection is due to the limitation of the mask holder in reaching the exact location of the image-forming conjugate plane of Köhler diaphragm. It is worth noting that the projected pattern using the 10x objective lens is roughly half the size of that using the 5x objective lens. 92

Figure 2-44: Bright-field optical images of the projected pattern (using 5x objective lens with NA of 0.13 for projection) and gold photomasks with pattern shown in Figure 2-39 (a) and (b), respectively, after developing process. The insets depict the drawing of the anticipated patterns. It is important to note that the unfocused projection is far more exaggerated in part (b) of this figure, as the smallest feature in the photomask pattern was much smaller than that of the pattern in (a). 93

Figure 2-45: Bright-field optical images of the projected pattern testing the smallest size that could be achieved using a 10x objective lens with NA of 0.25 in (a) and a 20x objective lens with NA of 0.50 in (b) given the limitation of the current mask holder. 94

Figure 2-46: Metal deposition on a developed silicon wafer substrate. 95

Figure 2-47: Lift-off step after metal deposition on the developed silicon wafer substrate. 96

Figure 2-48: Optical images of the projected pattern testing the smallest size that could be achieved given the limitation of the current photomask using a 20x objective lens with NA of 0.50. 97

Figure 3-1: A schematic depiction of the key components of an electron-beam lithography tool. 101

Figure 3-2: An illustration depicting the two modes of exposure in EBL: Raster scanning in (a) and vector scanning in (b). The arrows on the surface illustrate the direction of the travel of the electron-beam. Note that the gray colour of the arrows indicate the beam is off, whereas the black colour indicate the beam is on. 104

Figure 3-3: A schematic depiction of individual write fields of a pattern on a substrate and the e-beam deflection system for the EBL tool. Each cone depicts the area covered by deflection of the e-beam associated with one write field. 105

Figure 3-4: An illustration depicting the electron-beam trajectory and the resist area affected due to the forward and backscattering of electrons. 107

Figure 3-5: Two recognized mechanisms for PMMA degradation. 109

Figure 3-6: An SEM image depicting the selenium nanowires exposed with electron-beam in (a), taken after the overlay of the gold electrode. SEM image shown in (b) depicts an unexposed region selenium nanowires. 110

Figure 3-7: A schematic of substrates with single and bi-layer resist after the developing step, in which the undercutting profile can be seen for the bi-layer resist covered substrate. 113

Figure 3-8: A cross-sectional schematic of substrates with single and bi-layer resist after metal deposition step. This schematic is the continuation step from Figure 3-7. 114

Figure 3-9: A cross-sectional schematic of substrates with single and bi-layer resist after the lift-off step. This schematic is the subsequent step to that depicted in Figure 3-8. 115

Figure 3-10: A bright-field optical image of a substrate after the developing process. This image depicts the misalignment between write fields of an exposed pattern. 117

Figure 3-11: Bright-field optical images of e-beam exposed substrates depicting exposed viewing field in (a), misalignment of the pattern to a selenium nanowire in (b) and a partially over exposed viewing field in (c). 119

Figure 3-12: Bright-field optical images of developed patterns from electron-beam lithography exposures. Image in (a) depicts a successful overlay of a pattern on a selenium nanowire and that in (b) depicts the undercutting profile for a developed bi-layer resist stack. The inset in (b) depicts a side view illustration of the undercutting. 120

Figure 3-13: Bright-field optical microscopy images of pattern exposure on selenium nanowires via a direct electron-beam writing technique. These images were taken after developing the PMMA resist.

Note that in (a) the patterned lines surrounding the electrode pattern are positioned to create more breaks in the gold layer and assist with the lift-off process. Notice that in image (c) the ends of the nanowire, where the resists has been developed, can be seen with more contrast compared to the part of the nanowire under the resist. The inset in (c) indicates the positions of the nanowires under the resist with dotted lines. 121

Figure 3-14: Bright-field optical images taken after the lift-off step. a) This image depicts an unsuccessful lift-off of the gold layer from the unpatterned areas in a single-layer resist coated substrate. b) This micrograph depicts the successful lift-off process in a bi-layer resist substrate. Note that the patterned region of gold not on the nanowire is placed near the nanowire to help break-up the gold layer and help the lift-off..... 123

Figure 3-15: An image acquired by dark-field optical microscopy depicting a torn nanowire after rinsing the substrate with water following to the lift-off step. 125

Figure 4-1: The current-voltage curve of a simple resistor. 129

Figure 4-2: An image of a substrate wire bonded to a DIP (dual in line) IC package. 131

Figure 4-3: An image of the probe station and the electronic analyzer. 132

Figure 4-4: Bright-field optical images of the tungsten probes of the probe station on the gold electrodes. 133

Figure 4-5: The current-voltage curve of selenium nanowires. 134

Figure 4-6: SEM images of selenium nanowires between the gold electrodes. These images depict the non-uniform number of nanowires bundled together at different points between the two electrodes. 135

Figure 4-7: An image acquired by atomic force microscopy (tapping mode). Height profile measurements of the nanowire bundle were performed along the lines labelled a, b and c. 136

Figure 4-8: Height profile measurement of the selenium nanowire bundle across lines a, b and c as shown in Figure 4-7. The highest point of the bundle is 175, 155 and 130 nm along lines a, b and c, respectively..... 137

Figure 4-9: A bright-field optical image of the gold wire in between the two gold electrodes. Points ‘a’ and ‘d’ represent the approximate position of the tungsten probes of the probe station during the subsequent measurements. Points ‘b’ and ‘c’ represent the two ends of the gold wire. 138

Figure 4-10: The current-voltage curve of a gold wire obtained using the probe station and the analysis system as shown in Figure 4-9. 139

Figure 4-11: A schematic depicting the 5 resistors in series used for calculation of the contact resistance between the tungsten probe and the gold film. 140

Figure 4-12: A current-voltage curve for selenium nanowires. The blue data points are the original data obtained from this measurement and the red line is a fit to this data, from which the other plots in this section are derived. The equation of this line is: $f(x)= 0.0044 x^5 - 0.0670 x^4 + 0.4103 x^3 - 1.2793 x^2 + 2.5189 x + 0.2539.$ 142

Figure 4-13: The resistance-voltage curve obtained from the reciprocal of the derivative of the fit to the *I-V* curve plotted in Figure 4-12. 143

Figure A-1: A schematic depiction of the synthetic process for selenium nanowires. 153

Figure A-2: Pictures depicting the set-up for synthesis of selenium nanowires. Image in (a) was taken during the reduction of selenious acid with excess hydrazine at ice-water temperatures and picture in (b) is of the isolation and purification procedure for a-Se colloids. 154

Figure A-3: A bright-field optical image of aggregated selenium nanowires shown in (a). Scanning electron microscopy images of selenium nanowires dispersed in isopropanol, chloroform, hexanes, hexadecane-thiol prior to drying is shown in (b), (c), (d) and (e), respectively..... 155

Figure B-1: A picture of Kurt J. Lesker thermal evaporator used in the 4D LABS cleanroom facility..... 157

LIST OF TABLES

Table 2-1: Common nomenclature from the mercury emission spectrum. 31

Table 2-2: Conjugate focal planes as labelled in Figure 2-9. 42

Table 3-1: Relative influence of developer concentration in isopropanol on sensitivity and resolution.[125] 111

GLOSSARY OF ABBREVIATIONS AND SYMBOLS

AFM	atomic force microscopy
a-Se	amorphous selenium
I-V curve	current-voltage curve
DI	de-ionized
DNQ	diazonaphthoquinone
DUV	deep ultraviolet
σ	depth of focus
EBL	electron-beam lithography
eV	electron volts
HMDS	hexamethyldisilazane
IC	integrated circuits
CVD	chemical vapour deposition
σ	conductivity
LED	light emitting diodes
MΩ	mega Ohm
MOSFET	metal oxide semiconductor field effect transistor
μCP	microcontact printing
MPP	microscope projection photolithography

nm	nanometer
NIL	nanoimprint lithography
nw	nanowire
NA	numerical aperture
1D	one-dimensional
PVD	physical vapour deposition
PMMA	poly methylmethacrylate
SEM	scanning electron microscopy
TEM	transmission electron microscopy
t-Se	trigonal selenium
UV-Vis	ultraviolet-visible spectroscopy
VLS	vapor-liquid-solid
VS	vapor-solid
WF	write field
XRD	X-ray diffraction

CHAPTER 1: AN INTRODUCTION TO THE FIELD OF THIS RESEARCH

1.1 Goal of this Thesis

The continued miniaturization of electronics has motivated significant efforts towards the development of new functional materials and devices based on nanoscale building blocks.[1-8] A large number of studies have explored nanowires as new building blocks for use in devices such as sensors, [9-12] electrodes, [13-16] and photonic materials.[17,18] While these nanostructures have a number of unique applications, it is often expensive and time consuming to electrically characterize them or incorporate them into functional devices. The existence of an approach by which electrical characterization of nanomaterials can be done on the bench top requiring less fabrication time, less expensive instrumentation, no need for cleanroom facilities and no need for prior alignment of the mask with the nanostructures can be very practical and in high demand for research purposes. The major challenge is to control the position of electrodes with respect to nanostructured materials easily, inexpensively and accurately.

This chapter provides a short summary of the technological trends in the field of integrated device fabrication and introduces the field of nanomaterials; specifically semiconducting nanowires, the two main approaches of synthesis and their assembly. The goal of this thesis is to illustrate the development of two lithographic methods to

fabricate electric contacts on selenium nanowires in order to facilitate their conductivity and photoconductivity characterization as a function of wavelength as their composition is modified by addition of various dopants. To measure the changes in electrical properties of these one-dimensional nanostructured materials, electrodes need to be placed onto the two ends of nanowires. The small dimensions of these materials demand techniques capable of accurate alignment and positioning of electrodes. The processes developed using both techniques require fewer steps for positioning electrodes onto nanowires than previously demonstrated in the literature. Given the generality of the fabrication process, it can be applied to various one-dimensional nanostructures of nanowires or nanotubes.

1.2 Technology Trends towards Nanoscale

Since the beginning of the microelectronics era, the smallest achievable line width (or the minimum feature length) of an integrated circuit has been reduced at a rate of about 13% per year.[19] The graph in Figure 1-1 illustrates the evolution in size for the minimum features within silicon chip from the past to the projected near future as per National Technology Roadmap for Semiconductors.[25, 26] One benefit from device miniaturization has been the reduced unit cost per circuit function. For example, the cost per bit of memory chips has halved every 2 years for successive generations of dynamic random access memory (DRAM) circuits.[21,22] As device dimensions decrease, the intrinsic switching time also decreases. Device speed has improved by four orders of magnitude since 1959.[23] In the future, digital ICs will be able to perform data processing and numerical computation at terabit-per-second rates.[24] As devices become smaller, they consume less power. Therefore, device miniaturization also reduces the energy

used for each switching operation. Hence, production of nanoscale materials and their incorporation into devices is of high importance for future technologies.

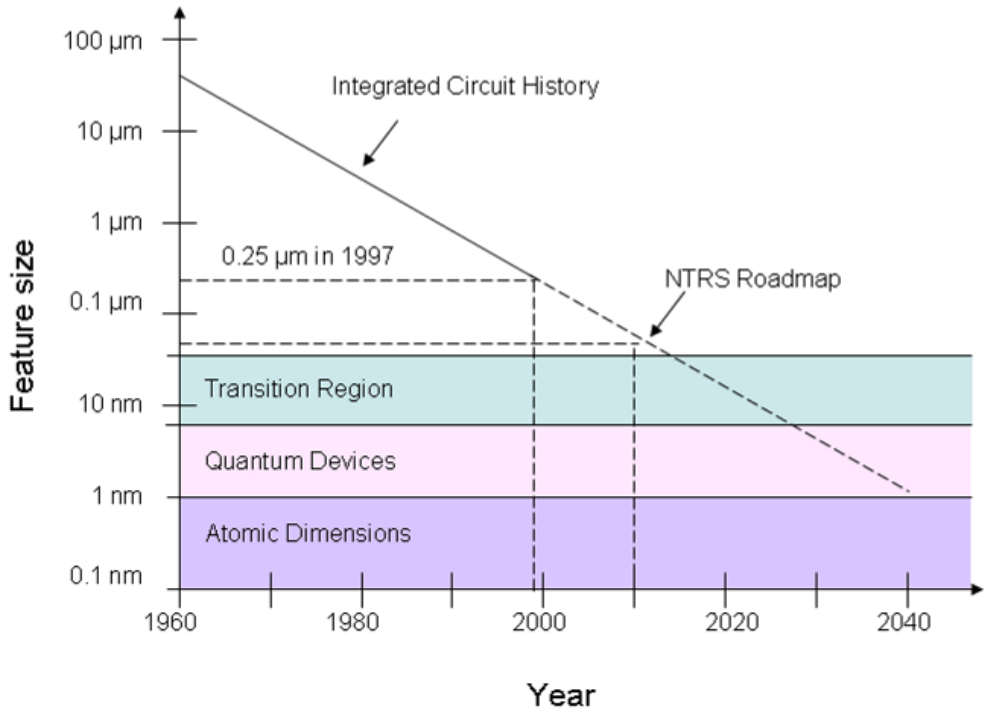


Figure 1-1: History and future projection for minimum feature sizes in silicon chips, according to the National Technology Roadmap for Semiconductors (*NTRS*).[19, 179-181]

The realm of nanoscale in the popular sense means 'small.' The feature sizes of nanomaterials and objects are in nanometers, where one nanometer equals 1 x 10^{-9} meter. Structures with dimensions up to 100 nm are considered nanostructures. It is now widely recognized that, aside from the benefit of device miniaturization, nanoscaled materials can exhibit properties that are not observed in bulk materials.[27] Over the last decade, the interest in nanosized materials and their applications in novel electronic devices have increased tremendously due to their unique properties and performance in devices.[28] The attractive and often unique properties of these structures and devices opened new and sometimes unexpected fields of applications. Today, widespread

applications include the detection of explosives, drugs, fissionable materials,[29-32] bio- and infrared-sensors,[30-32] spintronic devices,[33-35] data storage media,[36] magnetic read heads for computer hard disks,[37,38] microwave electronic devices,[39] and many more.

In the continuous search for nanosized structures with distinctive and advantageous physical properties, anisotropic nanostructures such as nanowires, nanotubes and nanorods have been investigated comprehensively over the last couple of decades. The advances in nanowire synthesis has led to an increasing number of research groups demonstrating that nanowires are suitable for investigating novel nanoscale physics.[28] These structures can be used as piezoelectric or optical switching devices, or to transport heat and/or electricity.[40] Consequently, it is crucial to achieve not only the controlled preparation of nanoscale elements, but more importantly, to characterize them for research and development purposes. A major class of the materials and structures being investigated is semiconductor nanowires.

1.3 Semiconducting Nanowires

It is widely agreed that new materials, structures and device concepts are needed to maintain the trend of transistor scaling.[41] One-dimensional (1D) nanostructures represent the smallest structure that can efficiently transport electrical carriers and can play an important role as both interconnects (connecting wires) as well as functional device elements in integrated devices. Perhaps the most prominent materials and structures being considered are semiconductor nanowires, which are single crystals with diameters of a few nanometers to tens of nanometers and lengths of at least a few micrometers.[42] Semiconductor nanowires represent a unique system to explore the occurrences at the nanoscale and are expected to play a critical role in the

future of electronics and optoelectronics.[43] Recently, there has been wide interest in the synthesis of semiconducting nanowires, as these structures may play a significant role in the next generation of nanoscale devices.[44] Using semiconducting nanowires as building blocks, a number of high-performance electronic devices have been fabricated.[45,46] These structures have functioned both as components within a device and as interconnecting wires.

Semiconductor nanowires have attracted considerable attention because of their unique electrical properties and miniaturized dimensions.[47-49] It is known that electron scattering in one dimension is much reduced, hence offering the possibility of ballistic transport in nanowires.[50] In general, in terms of their performance, nanowire-based electronic devices often rival devices made from bulk and epitaxial single-crystal semiconductors. Important properties of nanowires include their asymmetric shape, dimensionality-dependent optical/electrical properties, intrinsic anisotropies, prospects for ballistic transport[51,52] as well as potentially unique 1D physics.[53] Semiconductor nanowires can have an on-off current ratio that varies by many orders of magnitude for small changes in gate voltage.[44] These nanowires make excellent candidates for sensors,[54] transistors,[55,14] digital logic,[56] waveguides,[57,39] photovoltaics,[58,59] photodetectors,[60,61] and lasers, [62,18] and there are many literature reviews covering these various applications of nanowires.[15,63-65] Semiconductor nanowires are looked upon as a potential solution to some of the challenges in the effort to shrink devices into the nanometer regime.[44]

1.3.1 Semiconductor Devices

A huge range of transistor designs have been introduced from the late 1940s through today, and, as a result, a great number of innovations in semiconductor materials processing and much understanding have been achieved.[23] There have been many differences in device design over this period, but from a materials science point of view the most outstanding differences between the first point contact transistor – the first type of solid-state electronic transistor ever constructed – and the majority of electronics in use today are the choice of semiconductor, the material purity, crystalline quality and dimensions of key components that have an effect on operating speed and efficiency of these devices.[28] Many of the key electronic materials for technologies of today derive from the developments in the very early years of the semiconductor industry.

Semiconductor devices are the foundation of the electronics industry, with global sales of over one trillion dollars since 1998.[23] Figure 1-2 shows the sales volume of the semiconductor device-based electronics industry in the past 20 years and projected sales to the year 2010. The figure also shows gross world production (GWP) and the sales volumes of automobiles and steel. If the current trends continue, the sales volume of the electronics industry will reach three trillion dollars and will constitute about 10% of gross world product by 2010. The semiconductor industry, a subset of electronics industry, will grow at an even higher rate, exceeding the steel industry in the early twenty-first century and constituting about 25% of the electronics industry in 2010.

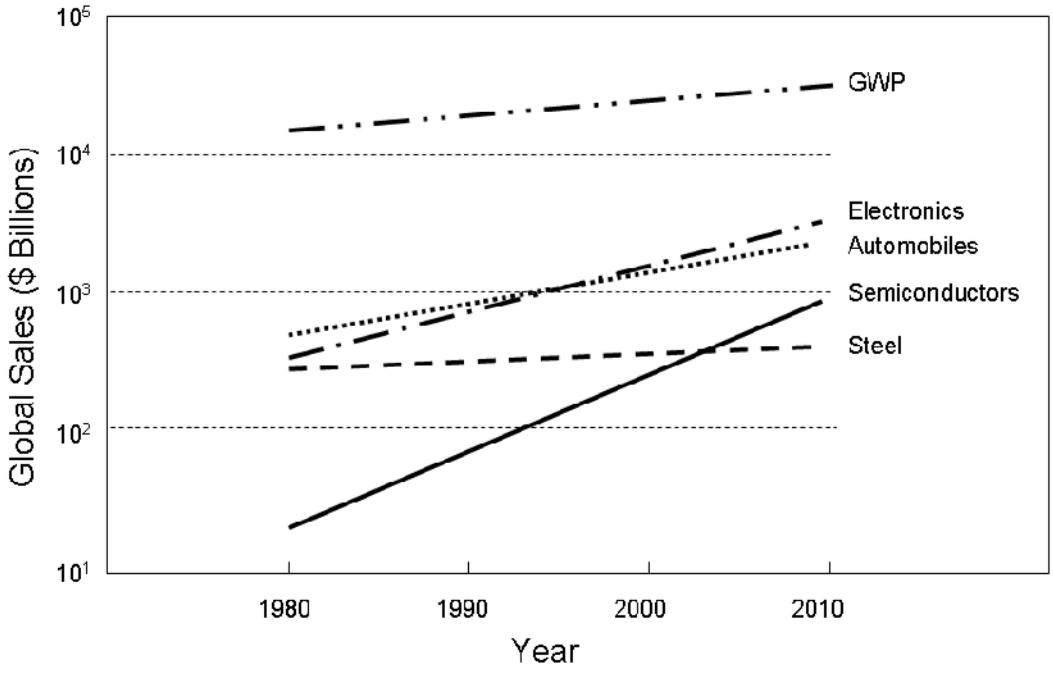


Figure 1-2: Gross world product (GWP) and sales volume of the semiconductor industry compared to other industries such as electronics, automobile, and steel from 1980 to 2000 and projected to 2010.[23]

The multi-trillion dollar electronics industry is fundamentally dependent on the manufacture of semiconductor integrated circuits (ICs). The solid-state computing, telecommunications, aerospace, automotive, and consumer electronics industries all rely heavily on these devices. Thus, due to increasing demand of these industries for production of modern electronics, it is essential to develop new semiconductors with fine tuned properties for which developing inexpensive and simple techniques for probing their properties becomes crucial.

1.3.2 Semiconducting Materials

One of the principal characteristics of materials, in general, is their ability (or lack of ability) to conduct electrical current. Indeed, materials can be classified by this property and are divided into conductors, semiconductors, and nonconductors (commonly referred to as insulators). The conductivity, σ, of different materials at room temperature spans more than 25 orders of magnitude, as depicted in Figure 1-3, where the unit of conductivity is $\Omega^{-1}cm^{-1}$. Moreover, if one considers the low–temperature conductivity of superconductors (estimated values of ~10^{20} $\Omega^{-1}cm^{-1}$), conductivity of different materials covers 40 orders of magnitude.[66-69] This range is comparable to the ratio between the diameter of the universe (about 10^{26} m) and the radius of an electron (10^{-14} m).

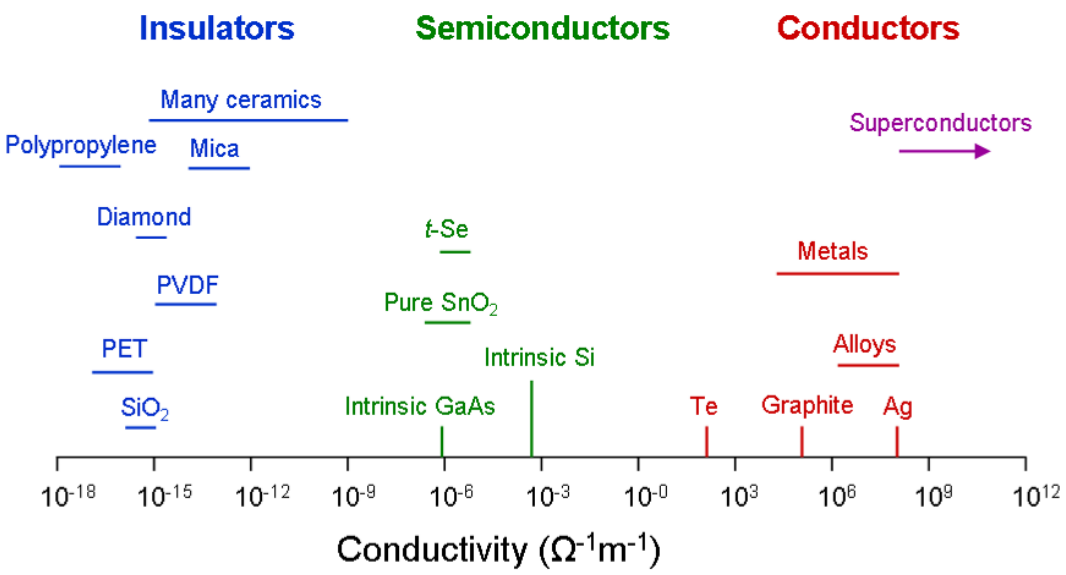


Figure 1-3: Conductivity of some insulators, semiconductors and conductors shown on a scale.

The best-known semiconductor is undoubtedly silicon. However, there are many other semiconductors besides silicon. In fact, many minerals found in nature such as zinc-blende (ZnS), cuprite (Cu_2O) and galena (PbS), to name just a few, are semiconductors. Including the semiconductors synthesized in laboratories, the family of semiconductors forms one of the most versatile classes of materials for their tunable electronic properties.[68] Semiconductors occur in many different chemical compositions with a large variety of crystal structures. They can be elemental semiconductors, such as silicon (Si), and selenium (Se), or binary compounds, such as gallium arsenide (GaAs). Many organic compounds such as polyacetylene $(CH)_n$ are semiconductors.

The unique properties of semiconductor materials have enabled the development of a wide variety of ingenious devices that have made significant improvements in our world. To date, there are about 60 major devices, with over 100 variations.[70] Some major semiconductor devices are light-emitting diodes (LEDs), p-n junctions, solar cells, lasers, and metal-oxide semiconductor field-effect transistors (MOSFET).

1.3.3 Electronic Band Structure (Band-Gap Energy)

In the field of solid-state physics, a semiconductor is usually defined rather loosely as a material with electrical resistivity lying in the range of 10^{-2}-10^{9} $\Omega^{-1}cm^{-1}$.[168] Alternatively, semiconductors can be defined and distinguished based on the behaviour of their valence electrons. In particular this definition is dependent on the structure of band gap in these materials. The microscopic behaviour of electrons in a solid is most conveniently specified in terms of the electronic band-gap energies. In a single atom, the electrons occupy atomic orbitals that form a distinct set of energy levels. The atomic orbitals of a molecule with several atoms produce a number of molecular orbitals

proportional to the number of atoms. As for a solid, where a large number of atoms on the order of 10^{20} or more are brought together, the number of orbitals becomes exceedingly large and the difference in energy between them becomes very small, so the levels may be considered to form *'continuous bands of energy'* rather than the discrete energy levels of the atoms in isolation.[169] However, for some materials an interval of energy contains no orbitals, no matter how many atoms are gathered, forming *band-gaps*. The difference between conductors, insulators and semiconductors can be visualized by plotting the available energy states for electrons that form a band in the materials instead of the discrete energies as in the case of individual atoms or molecules and can be seen in Figure 1-4.

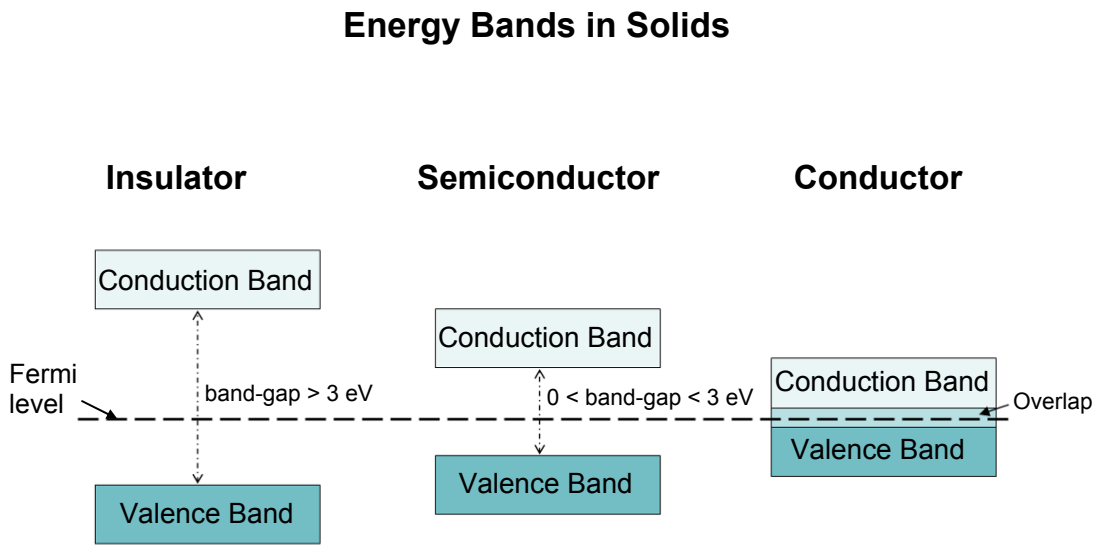


Figure 1-4: A simplified diagram of relative band-gap energies for electronic insulating, semiconducting and conducting materials.

Whether or not electrons are present in the conduction band is essential for the conduction process. In insulators the electrons in the valence band are separated by an

energy gap larger than 3 eV from the conduction band; in conductors the valence band overlaps the conduction band; and in semiconductors there is a small gap between zero and about 3 eV between the valence and conduction bands.[169] Electrons in semiconductors, due to presence of a small gap, can bridge the band-gap to reach the conduction band via thermal or other forms of excitations. In fact, the conduction in semiconductors can be structurally tuned by addition of a small percentage of impurities (commonly known as dopants) in the crystal lattice of the semiconductor material. Doping is the process of intentionally introducing impurities into an extremely pure semiconductor to change its electronic properties. Addition of dopants results in a material having charge carriers that are predominantly negative (n-type) or positive (p-type) depending on the dopant species. The addition of a dopant to a semiconductor shifts the Fermi level within the material (see Figure 1-4).

In applied research, the focus for particular fields is often driven and guided by the needs of industry. The need for efficient LEDs and lasers operating over the whole of the visible spectrum as well as fiber-optic windows at specific wavelengths has required the research focus to be concentrated on new direct-gap semiconductors to act as the active materials.[66, 67] Since the emission wavelength of a semiconductor corresponds to its band-gap energy, research focuses on engineering new materials that have their band-gaps at custom-designed energies. This field is called '*band-gap engineering*'. Advances in band-gap engineering rely heavily on developments in the science of crystal growth and is one of the foundations of current semiconductor technology.

1.3.4 Semiconducting Selenium

The element selenium had a historic role in the field of semiconductors and discovery of photoconductivity. The chemist Berzelius discovered selenium in 1817.[71]

Over half a century later, in 1873, an English electrical engineer named Willoughby Smith detected the photoconductivity of trigonal selenium (*t*-Se), which is one allotropic form of the selenium crystalline structure.[71,72] Smith, in search of a high resistance material for a project, selected selenium rods, the dimension of which are not mentioned in literature. In Smith's experiments, the original trials using selenium performed desirably; however, in actual use the device gave inconsistent results. After more investigations, Smith discovered that the conductivity of the selenium rods increased significantly when exposed to high intensity light. In 1873, he published his discovery in an article describing the effect of light on selenium during the passage of an electric current.[72] After the discovery of this property, a significant number of investigations were carried out and new technical applications resulted in production of the first photocells using trigonal selenium, *t*-Se. In fact, at the time "selenium-cell" and "photoconductive device" were synonymous.[73]

In spite of the technical importance and the great number of investigations that took place until the 1950s, the understanding of the electronic properties of trigonal selenium was poor and far behind other photoconducting elements and compounds. This lack of progress in that period is largely attributed to the unavailability of good quality single crystals.[74] In 1945 the first real advances in the knowledge of semiconductors occurred. After the invention of the transistor in 1948, the semiconductors, germanium and silicon, and a little later the III-V compounds were of such scientific and technical interest that the importance of selenium diminished considerably. Recently considerable progress has been made in the growth of crystals of trigonal selenium.[75]

Selenium is an important semiconductor that exhibits a unique combination of many interesting and useful properties. This element shows a variety of interesting

properties, such as high photoconductivity (~0.8 $\Omega^{-1}cm^{-1}$),[75] nonlinear optical properties,[76,77] thermoelectric and high piezoelectric response,[78-80] and can be chemically converted to other functional materials such as CdSe, ZnSe, Ag_2Se, Bi_2Se_3, GaSe and HgSe.[81,82] Selenium has potential to be used as a photosensor material and has commercial applications in solar cells, photovoltaic cells, rectifiers, photographic exposure meters, and xerography.[71,76,83,79] Like other photonic semiconductors,[84-87] nanostructures of selenium are expected to enhance performance and offer new or improved photonic applications as a result of their size confinement.

There are limited reports on the physical properties of selenium nanostructures, especially as an electrical or photonic device. The electrical conductivities of *t*-Se at room temperature have been reported in the range of 10^{-6} -10^{-5} $\Omega^{-1}cm^{-1}$, and the photoconductivities range up to 10^5 $\Omega^{-1}cm^{-1}$.[88] The optical properties of *t*-Se are of interest when illuminated with visible light, as optical data could be used to probe the electronic structures and its dependence on nanowire dimension and composition. The band-gap energy of *t*-Se has been computed using a number of approximation methods.[89-91] Similar to many other semiconductor systems, the band-gap of t-Se nanowires can be tuned by changing the dimension of diameter in nanowires, which can be done through monitoring experimental conditions such as temperature during the synthesis.[75] It is generally accepted that *t*-Se is a p-type extrinsic semiconductor, with an indirect band-gap of ~1.6 eV.[75,92-94] According to calculated electronic band structures for trigonal selenium, the lowest energy excitations from the valence band correspond to three transition energies of ~2.1, 2.6, and 3.2 eV. A transition energy of 2.1 eV is attributed to interchain interactions, whereas transition energies of 2.6 and 3.2 eV are attributed to arise from interactions along covalent bonds within the selenium chain.[75]

The properties of selenium nanowires could be better enhanced for device usage by tuning their band-gap and conductivity via changing their diameter size and/or composition or implementing different device set-up such as providing different intensities of various wavelengths from the electromagnetic spectrum at desired temperatures. As such, there are many conductivity measurements that need to be done to tune the properties of these nanostructures for specific device purposes. The fabrication processes developed and discussed in this thesis are a means to provide an easier, faster and less costly experimental process for positioning electric contacts on these nanostructures with little or no damage done to the nanowires during that process to perform the desired conductivity measurements.

1.4 Synthesis of Semiconductor Nanowires

Semiconducting nanowires with diameters ranging from 1 to 400 nm and lengths of up to hundreds of micrometers are perhaps the most versatile building blocks (aside from molecules) for optical and optoelectronic circuits at the nanoscale.[15,27] The integrated circuit technology of today is based on a top-down approach where elements such as transistors and interconnects are formed by lithographic techniques.[95] The cost and size of the basic transistor switching element still continues to halve every two years as predicted by Moore in 1965.[96] It is expected that the current transistor size of 32 nm will shrink to 22 nm in 2011 just by incremental enhancements of the current technology.[97] A bottom-up approach of circuit assembly using building blocks can be useful and complementary to the already existing synthetic approaches.

1.4.1 Choice of Bottom-Up Approach for Synthesis of Nanostructures

One-dimensional semiconducting nanowires have unique electronic properties such as quantum-confinement effects and low leakage currents, which make them attractive as building blocks for functional nanosystems and the next generation electronics. Semiconductor nanowires have been synthesized via either 'top-down' or 'bottom-up' approaches. Top-down approaches to making nanostructures require lithographic techniques for fabrication (further discussion on lithographic techniques is found in Section 1.6). Bottom-up approaches, on the other hand, uses interactions between molecules or colloidal particles to assemble discrete nanoscale structures.[170] These methods offer unique opportunities and alternatives for the design and fabrication of single- and multi- nanowire device structures on a range of substrates without the need for lithographic procedures.[44] A bottom-up approach, in which functional systems are assembled from chemically synthesized and well-defined nanoscale building blocks, has the potential to go beyond the limits of top-down technology by defining key nanometer-scale dimensions through synthesis. For instance, the critical size of a nanowire is defined during the growth in the chemical synthesis process and can be controlled with atomic-scale resolution. Using this approach to the fabrication of nanostructures, that has attracted much attention, new synthetic routes are developed to have precise control of structure parameters, such as diameter, length, size uniformity, growth direction, chemical composition, and dopant level to produce nanowires. This ability to tune certain parameters may enable the integration of these structures in a wide range of devices.[13,95,99-102] The bottom-up approach for fabrication of nanostructures is attractive for its ease of scaling to large quantities (e.g., gram scale), which would be a necessary step for applications utilizing nanowires in nanowire-based electronics.

To date, great efforts and progress have been made in the field of semiconducting materials and nanowires. There are, however, still many more nanowires of various sizes and compositions that have not been investigated and could be more controllably synthesized by solution-phase techniques. While the synthesized materials produced from the bottom-up approach have a number of advantages, it is usually a challenge to incorporate these materials into functional devices such as integrated circuits, sensors and photonic devices. The challenge is, in fact, having to make contacts between these nanostructures and other components in a device.

1.5 Association of One-Dimensional Nanostructures in Devices

The future success of one-dimensional nanostructures in research and technology is dependent on the success and ease of associating these materials with desired components in a device.[28,65] In order to make contacts with these nanostructures and other device components, there needs to be a selection of fast and inexpensive techniques. The approaches taken in today's research, as will be briefly described with examples below, mainly require knowledge of the exact position of the nanowires on the substrate. This requirement holds true whether the position of the nanowire was designated prior to or subsequent to nanowire deposition for alignment and fabrication of electrical contacts on nanowires.

A popular assembly strategy utilizes the self-assembly of nanostructured components. Self-assembly describes the process that occurs when intermolecular interactions within an initially disordered system favors the spontaneous generation of an organized pattern or structure. This assembly is a consequence of specific, local interactions among the components and substrate surface, without the need for external

direction. These interactions can be of various nature such as van der Waals, hydrophobic/hydrophilic, electrostatic, or covalent.[28] Self-assembly of nanowires is compatible with a variety of materials and can be applied to a mixture of one-dimensional components. In this fabrication strategy, surface chemistry is used to direct the assembly of one-dimensional nanostructures onto lithographically patterned substrates. By modifying the surfaces of the nanowires and the substrate with self-assembled monolayers (SAMs), it is possible to control the attractive and repulsive interactions that result in where and how nanowires attach to the substrate and to each other. For instance, Mallouk and colleagues have demonstrated the selective adhesion of gold nanowires to properly functionalized gold surfaces.[142] In this work, the authors controlled the micron-scale location of groups of nanowires, but not their density or orientation.

Fabricating simple networks for positioning nanowires can be done using fluidic assembly. For instance, using surface modification of the electric contact pads and fluidic directed assembly a parallel orientation among nanowires can be created to yield nanowires connected to both electrodes.[104] However, this technique is not ideal for the precision and complexity needed for the high pattern density of many applications. Other methods to align nanowires use an electric [105] or magnetic [106] field, which may also prove to be impractical for the construction of dense and complex architectures.

Another method generally used for the assembly of nanowires is guiding nanowires into desired locations via directed assembly. In this approach, some form of lithography, such as electron-beam lithography (EBL), nanoimprint lithography (NIL) [107] or microcontact printing (μCP) [108], is used to pattern the surface such that it will affect the subsequent assembly of nanostructured materials or the subsequent growth of these nanosized structures on the substrate. For instance, Van Haesendonck and colleagues

have shown a deposition technique for either individual or small numbers of nanotubes based on electron-beam lithography.[109] In their technique, openings are created in a polymer layer using electron-beam lithography, and subsequently nanotubes are deposited from solution onto the substrate. It is possible to have one or a few nanotubes in one opening. Using alignment markers in the process of electron-beam lithography (as will be further described in Section 3.1), one can deposit nanotubes on top of gold to create interconnects. Another example for depositing nanowires in the desired location is shown by positioning them using a process that is referred to as a 'pre-alignment process.' In this approach, the alignment has been pre-determined by positioning of catalyst so that the nanowires are grown and automatically aligned to the contacts. Koley *et al.* [110] patterned alignment marks on an oxide layer followed by metal deposition. They then made catalyst patterns using electron-beam lithography at the desired locations where electrode contacts would be positioned. However, nanowires synthesized by a solution-phase method that requires multistep processing can not be assembled using this approach.

As exemplified in this section, the incorporation and alignment of nanostructures with other device components has been a challenging issue for nanostructure-based electronic devices for future technological applications. Progress in the field of directed assembly for incorporation of these nanomaterials, although impressive in proving several design concepts, still faces limitations and challenges.

1.6 Top-Down Fabrication Process for Incorporation of Nanostructures in Devices (An Overview of this Thesis)

One-dimensional nanostructures, specifically semiconductor nanowires, have unique properties and represent the smallest structure that can efficiently transport

electrical carriers and could function as building blocks for nanoscale electronics. These structures could play an important role in the future as both interconnects and functional device elements within integrated devices. Fabrication of modern microelectronics devices such as capacitors, transistors, or simple interconnects of wires relies on having techniques to provide better measurement of electrical properties of such components and also to incorporate them with other existing components within a device.

Characterization techniques such as scanning and transmission electron microscopy (SEM and TEM), atomic force microscopy (AFM), X-ray diffraction (XRD), ultraviolet-visible (UV-Vis) spectroscopy and many other spectroscopic techniques provide valuable information regarding topography, crystallinity, optical properties and composition of nanostructures. However, electrical characterization is essential for the design and integration of these structures for future nanoscale electronics. It is, therefore, crucial for the research community to continually characterize the electrical properties of these nanostructures, with varying composition and geometries (e.g., nanotubes and nanobelts), to be able to synthetically tune their properties and also to incorporate and connect them with other device components without the need for time-consuming, complex and costly fabrication processes and facilities. One of the efforts of current leading edge chemistry and materials science is to hybridize top-down and bottom-up techniques for the architecture of nano-electronic devices. This thesis presents the fabrication of electric contacts using top-down lithographic techniques on selenium semiconducting nanowires randomly distributed on a surface. These nanowires were synthesized using bottom-up techniques, avoiding some of the challenges mentioned above.

Fabrication processes that are investigated in this thesis use patterning in a series of steps that result in the removal of selected portions of the added surface layers,

such as a resist layer. As will be discussed further in Section 2.1, after partial removal of resist layer, a pattern is left on the wafer surface. The depicted patterning process in Figure 1-5 is known by some common names such as: photomasking, masking, photolithography or, more generally, lithography. During the fabrication process, to briefly overview as shown in Figure 1-5, different layers of the system are formed on the substrate surface by various deposition techniques such as spin coating, physical vapour deposition (PVD), chemical vapour deposition (CVD), evaporation, and sputtering (further discussed in Sections 2.5.3 and 2.5.9). These parts are created one layer at a time by the combination of putting a layer on the surface and removing portions of it, with a patterning process, to leave a specific shape or pattern of materials on the wafer surface. The goals of the patterning operation is not only to create the desired shapes in the exact dimension (feature size) required by the circuit design, but also to precisely locate them on the wafer surface and in relation to the other existing parts. Further discussion on the details of these processes are provided in Section 2.5.

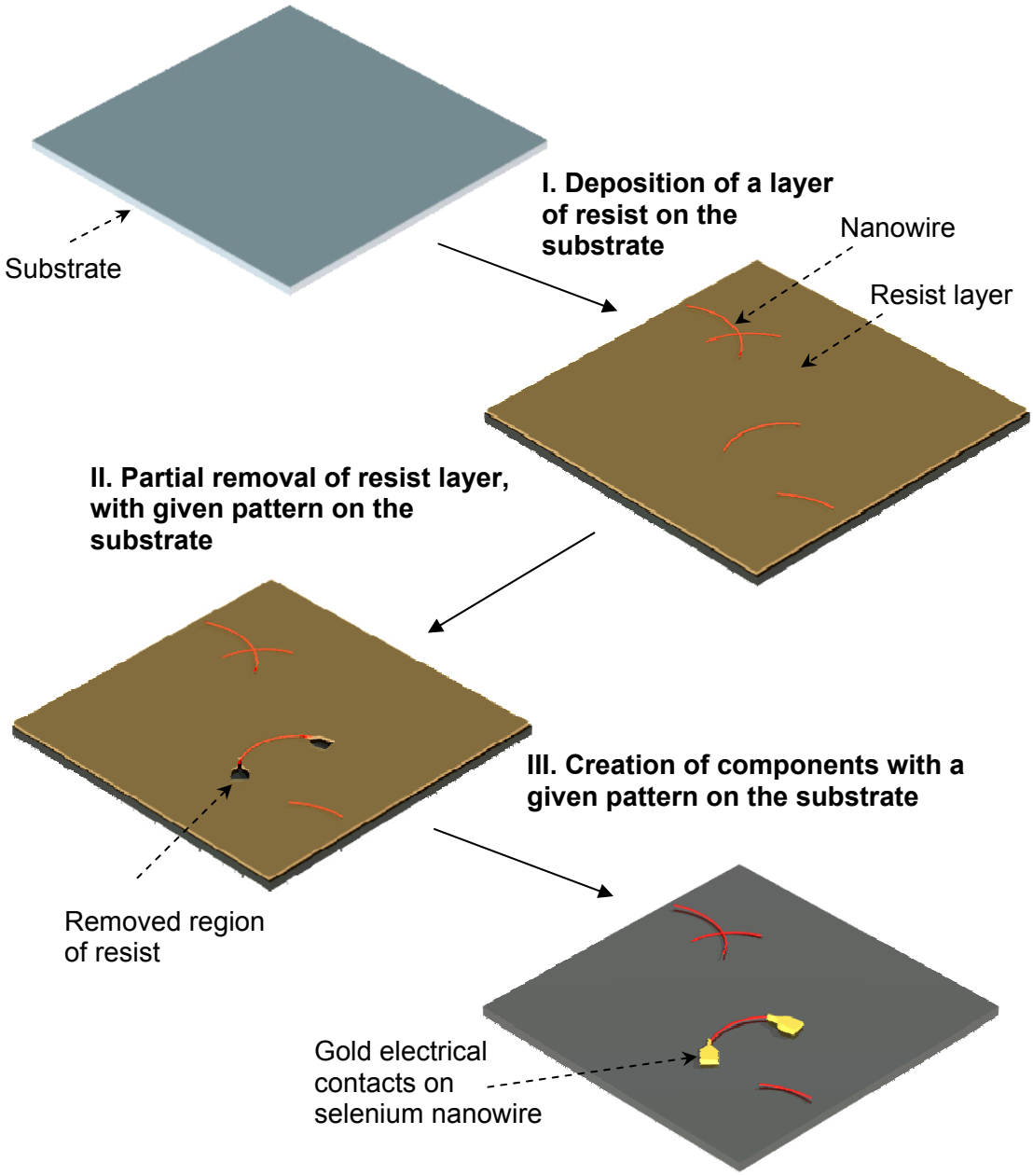


Figure 1-5: A schematic overview of the fabrication process.

The number of applications for nanostructured materials synthesized in the laboratory could be significantly expanded by designing techniques to incorporate them in desired devices. Also these structures would have limited value if their conductive properties are not known. This thesis addresses two concepts: the challenge of positioning electrodes on one-dimensional nanostructures and the need to know the electric properties for application purposes. The research demonstrated in this thesis focuses on developing a time- and cost-effective technique requiring fewer processing steps than previously demonstrated in the literature for providing electric contact between nanomaterials and other existing components on a substrate. To do so, two lithographic techniques, optical projection photolithography and electron-beam lithography, were used. The use of optical projection photolithography involved modification of an optical microscope. The developed process for fabrication was applied using both optical projection photolithography as well as electron-beam lithography techniques. Via the two techniques, metal contacts were positioned on selenium nanowires. Also, conductivity measurements on the fabricated systems were performed. Using the techniques introduced in this thesis, characterization and tuning of one-dimensional nanostructures, specifically conductivity and photoconductivity as a function of the wavelength of irradiated light, can be performed. As a result of such investigations, the properties of these nanostructures can be tuned for specific applications and in a much more time and cost effective manner than currently used techniques without the requirement of expensive instruments and facilities such as cleanroom environments (see Chapter 3 for further details).

CHAPTER 2: MICROSCOPE PROJECTION PHOTOLITHOGRAPHY ON NANOWIRES

At present, research in the field of nanofabrication requires the development of new tools and methods for high-speed throughput and cost-effective fabrication. These developments would be immensely valuable to the research community. This need is in part due to the range of materials and structures readily available through materials synthesis. In the current state-of-the-art, there exists no approach, or set of tools, that can simultaneously meet all criteria for cost and speed of device fabrication and testing. This chapter introduces some of the lithographic technologies that are applied for the processing in device fabrication. It also integrates existing techniques into a method for fabricating electric contacts on nanowires in a time- and cost-effective manner.

2.1 Lithographic Techniques for Device Fabrication

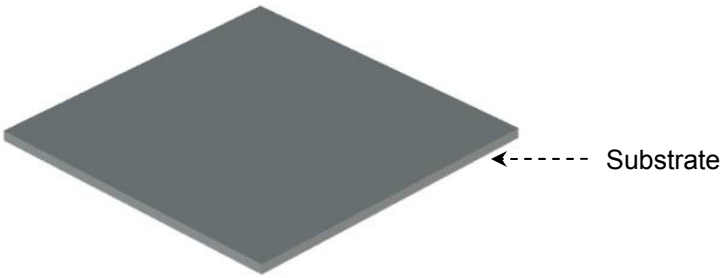
Lithography is a key technology for the semiconductor industry. It is the most expensive and yet critical process in mainstream micro- and nano-electronic fabrication. Lithography is, in fact, a significant economic factor, currently representing over 35% of integrated circuit (IC) manufacturing costs.[23] Lithography has enabled the formation of many solid-state devices on substrates without the traditional assembly of individual devices. The continued and astonishing growth of the electronics industry (as seen in

Figure 1-2) and other related fields, including the semiconductor industry, has been the direct result of improved lithographic technologies.

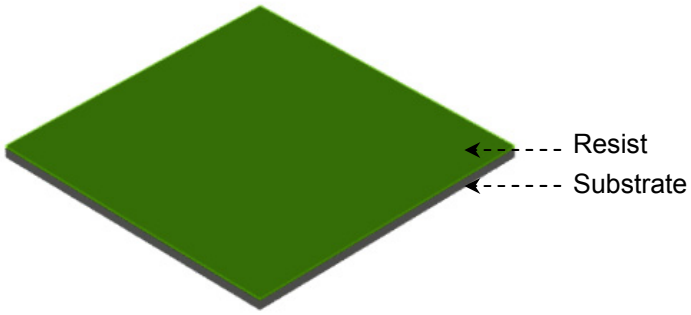
Alois Senefelder invented the lithographic process in 1796.[112] The term lithography, originally known as stone-printing, referred to the process of printing text or artwork using a nonpolar ink applied to a master stone plate (usually limestone) and transferring that onto paper or other materials.[113] To begin with, an image was drawn on the surface of a stone plate with an oil-based pigmented medium. An acidified solution was then applied to the plate that penetrated into the pores of the stone where the stone was not protected by the oil. The stone was kept wet with water prior to loading of a hydrophobic ink, so that only the hydrophobic parts of the stone would load with the ink. The stone and paper was then run through a press, which applied pressure to transfer the ink from the stone to the paper.

It was not until 1957 that the ancient lithography process was developed and applied by Jules Andrus and Walter Bond at Bell Labs for the fabrication of semiconductor devices.[114] Andrus and Bond began adapting and developing existing lithographic techniques for making patterns on printed-circuit boards to produce more elaborate designs on silicon wafers. In their technique a photosensitive coating or "resist" was applied on the silicon wafer and after exposing the desired pattern on this coating through an optical mask, precise areas were defined in the layer by chemical etching where unexposed resist had been washed away. (See Figures 2-1 and 2-2). Impurities were then diffused through these openings into the underlying silicon to establish the zones of n-type and p-type silicon needed in semiconductor devices. N-type silicon is obtained by addition of donor type impurities to produce an excess of free electrons (e.g., P, As, and Sb) and p-type silicon by addition of acceptor type impurities to produce an excess hole density (e.g., B, Al, and Ga).[76]

Today, in the modern practice, lithography is more generally applied to a number of methods that reproduce a predetermined pattern on various surfaces. Lithography is the creation of three-dimensional (3D) structures in a material. A general scheme for the lithographic process is depicted in Figures 2-1 and 2-2. First, a “resist” — a material sensitive to photons or electrons — is deposited on a substrate (Figure 2-1, step I). Certain areas of the resist are exposed to a collimated beam of photons or electrons that are chosen to appropriately interact with the resist material (Figure 2-1, step II). The exposure of the resist alters the physical and/or chemical properties of the exposed regions, making them more susceptible to a subsequent chemical treatment called “development”. In the developing step, an appropriate solvent dissolves either the exposed or unexposed regions of resist layer, depending on the resist type. After development, the substrate contains only certain regions where it is still covered by resist (Figure 2-2, step III). The substrate is then etched or additional material is deposited over the entire surface (only this case is shown in Figure 2-2, step IV). Finally, the resist is stripped away, leaving the desired positive or negative pattern of metal on the substrate (Figure 2-2, step V).



I. Apply resist film (either positive or negative tone resist)



II. Expose certain areas of substrate (via a collimated beam of either photons or electrons)

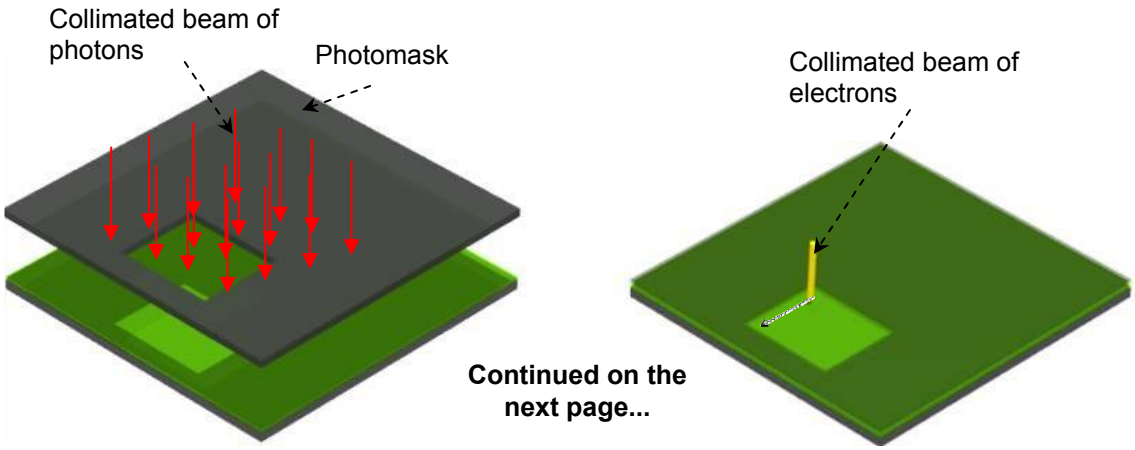


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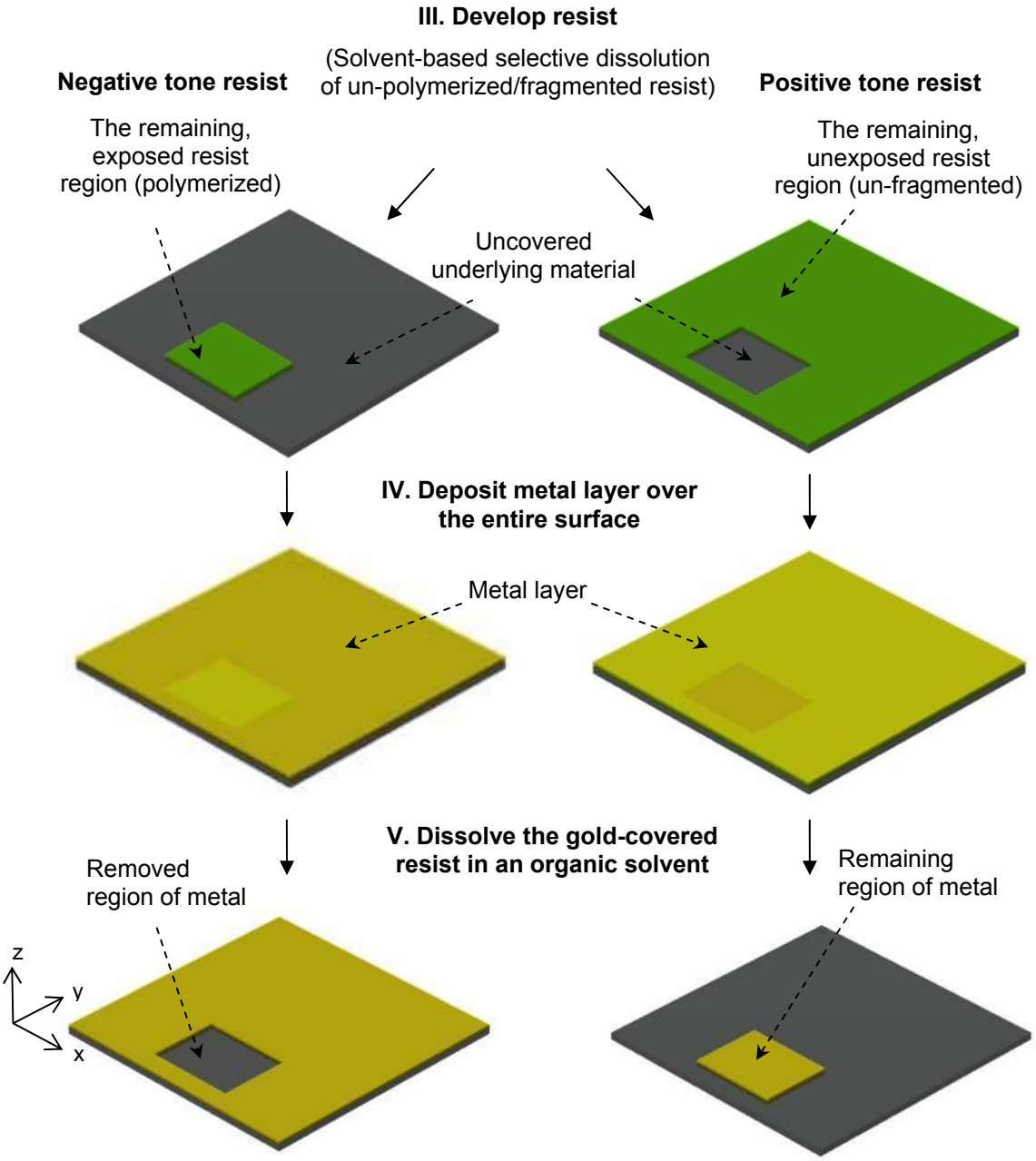
Figure 2-1: A general schematic process for lithographic steps (part I). Continuation of this schematic is on the next page.



Note: The limiting dimensions in x and y axes depend upon the choice of lithographic technique.

Figure 2-2: Part II and continuation of lithographic steps from Figure 2-1 on the previous page.

In the lithography process, the thickness (dimension in the z axes, as shown in Figure 2-2) of the produced structure, though only through immense historic development, can be precisely controlled through well-defined spin casting processes or by PVD/CVD processes, as described further in Section 2.5.3. The resolution of the other two dimensions (x and y axes, as shown in Figure 2-2) depends on the technique used to expose and irradiate the substrate.

There are many lithographic techniques for the controlled fabrication of miniaturized structures on substrates, such as optical lithography (commonly known as photolithography), X-ray lithography, electron-beam lithography, ion-beam lithography, and other emerging lithography techniques.[115,124] Among the mentioned lithographic methods, the more commonly used are photolithography and electron-beam lithography.[22] Photolithography employs photons in the optical regime (193 nm with use of ArF lasers to ~400 nm with use of Hg lamps) and electron-beam lithography uses a collimated beam of electrons for the controlled exposure of the resist-coated substrate. For photolithography, the limit of the smallest feature that can be produced depends linearly on the wavelength of light. The wave nature of light dictates the diffraction limits of patterning resolution, whereas in electron-beam lithography, the wavelength of electrons is so small that the process is no longer diffraction limited. State-of-the-art deep UV (DUV) photolithography techniques use light with a wavelength of 193 nm to provide a minimum feature size of ~50 nm.[116] However, some applications require higher resolution. Thus, the second common lithography method, electron-beam lithography, is employed. In this thesis, both ultraviolet and electron-beam lithographic techniques have been utilized and will be discussed, as they are applicable to the formation of lithographically defined electric contacts to nanowires.

Upon irradiation of a resist with either electrons or photons, the solubility of the resist film is modified due to a change in the chemical properties of the resist, such that by immersion in a “developing” solvent the exposed and unexposed regions have differentiated rates of dissolution in this solvent. The change in chemistry of the resist can either increase or decrease the solubility in the exposed regions. Hence, there are two categories of resists: positive resist (also known as positive tone resist) and negative resist (or negative tone resist).

A positive resist, when selectively exposed to radiation, changes in chemical structure so that it becomes more soluble in the developer solvent. The exposed resist is then washed away by the developer solution, uncovering the underlying material, as seen in Figure 2-2. The pattern produced using a positive resist is therefore a positive image (or identical copy) of the photomask (see Figure 2-1) used during exposure. A negative resist behaves in an opposite manner to that of a positive resist. Exposure of a negative resist to either electrons or photons causes polymerization and, as a result, the polymer becomes more difficult to dissolve. Therefore, the negative resist remains on the surface wherever it is exposed to irridiation, and the developer solution removes only the unexposed portions, as seen in Figure 2-2. Patterns produced using a negative resist contain the negative image (or reverse copy) of the mask used during exposure. Figure 2-2 shows schematically the difference in patterns generated with the use of positive and negative resists.

The sensitivity of a resist relates to the amount of energy required to cause the selective polymerization or photosolubilization to occur within the resist material. Furthermore, sensitivity relates to the energy associated with specific wavelength of the irradiating source. In nature, all electromagnetic energies (or radiation) are differentiated from each other by their wavelength, with the shorter-wavelength radiation

corresponding to higher energies. The choice of lithographic wavelength is primarily determined by the availability of radiation sources with a sufficient flux of photons. A common light source used in lithographic exposure systems is the mercury arc lamp.[117] This source produces intense radiation at a number of wavelengths such as 436, 405, and 365 nm (commonly known as the g-line, h-line and i-line, respectively). The spectrum of a mercury lamp is shown in Figure 2-3. The mercury arc lamp is a good choice of radiation source when the required minimum feature size is greater than about 300 nm.[117]

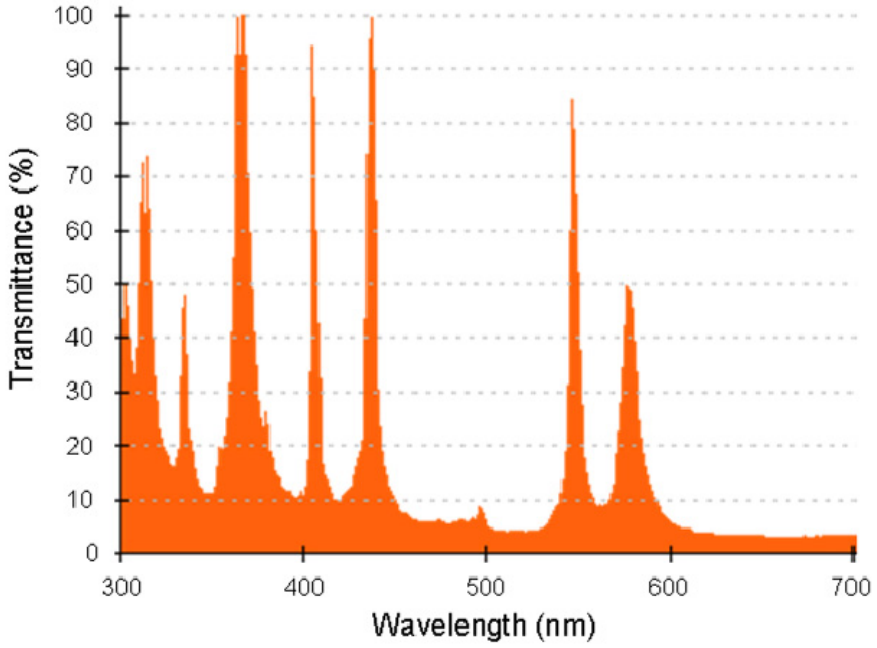


Figure 2-3: The line spectrum of a mercury lamp (HBO 100/103 mercury short arc lamp purchased from Zeiss). *(Courtesy of Carl Zeiss Company).*[118]

Table 2-1: Common nomenclature from the mercury emission spectrum.

Wavelength, λ (nm)	Common nomenclature
365	i-line
405	h-line
436	g-line

Common positive and negative photoresists respond to energies in the ultraviolet and deep ultraviolet (DUV) portions of the electromagnetic spectrum. Some resists are designed to respond to particular wavelengths (e.g., g-, h-, i-lines as seen in Table 2-1) within the UV spectrum, and some are designed to work with X-rays or electron-beams. Resist sensitivity, as a parameter, is measured as the amount of energy required to initiate the central reaction for polymerization or fragmentation of resist material. The units for resist sensitivity to irradiation are milli-Joules per square centimetre (mJ/cm^2). In this thesis, the positive photoresist used in photolithography was sensitive to the i-line of the mercury lamp and intensity of the lamp was optimized as described further in Section 2.6.3.

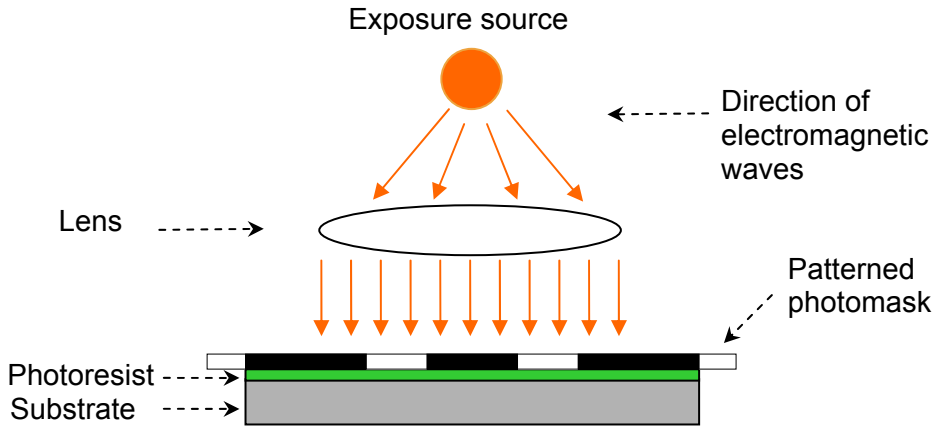
2.2 Various Techniques of Resist Exposure

The lithographic methods using light to project a pattern onto a photosensitive material are referred to as optical lithography or photolithography techniques. Photolithography methods have been key processes for the semiconductor industry, as they have enabled the miniaturization of components within semiconductor devices used

for integrated circuit (IC) manufacturing.[22] Photolithography techniques require a photomask to transfer only part of the radiation to photoresist leading to a desired pattern on a resist coated substrate. The photomask is a transparency mask allowing passage of light through certain regions based on the pattern of interest. Depending on the positioning of the mask, three techniques have been developed: 1) contact lithography; 2) proximity lithography; and 3) projection lithography. These techniques will be discussed in detail below to provide an insight into the advantage that projection lithography offers with use of an optical microscope (see Section 2.3) over the other techniques.

2.2.1 Exposure of Resists via Contact Photolithographic Techniques

Contact photolithography is an early method used for producing patterns on substrates.[119] In this technique, light is exposed to a photomask that is positioned on the top of the photoresist-covered wafer and pressed against it, creating exposed and unexposed areas. A schematic of this set-up is shown in Figure 2-4.



Note: the photomask and the photoresist are in contact.

Figure 2-4: A schematic depicting '*contact photolithography.*' The patterned photomask is in contact with photoresist.

Contact printing results in defects such as scratches and pinholes in the photomasks as well as in the photoresist necessitating the regular disposal of photomasks. Mask defects accumulated during successive mask uses are the main limitation of contact printing. The pressure during contact printing damages both the mask and substrate. The accrued damage and particles of resist adhering to the mask are brought into contact with other substrates in subsequent exposures, causing a rapid build-up of defects. Depending on the scale of integration and durability of the mask surface, only a limited number of uses can be tolerated by the mask. As chip areas increase and features shrink, the need for lower defect densities and higher dimensional integrity to maintain yield has encouraged the development of alternate exposure methods, particularly proximity and projection printing.

2.2.2 Exposure of Resists via Proximity Photolithographic Technique

In proximity photolithography, the mask is slightly separated from the substrate to avoid contact and eliminate most defects that result from the contact process. As seen in Figure 2-5, masks used in this technique are usually 10 to 50 μm away from the wafer and as a result have longer useful life times than those used in contact photolithography.

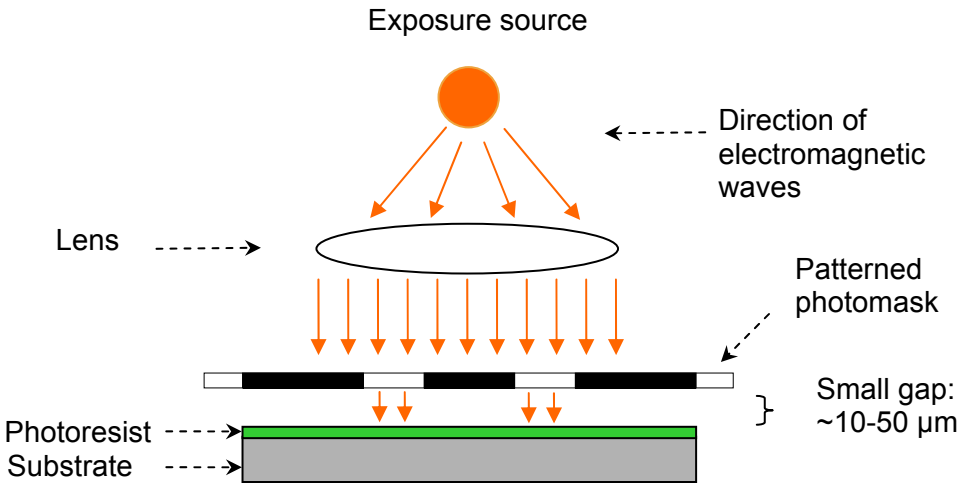


Figure 2-5: A schematic depicting *'proximity photolithography.'*

The resolution achieved by this technique is less and the distortion of individual features on photoresist is increased relative to that of contact photolithography. This result is due to diffraction of the transmitted light, which increases with increasing spacing between the mask and the photoresist film.[119,120] The lower resolution is a result of Fresnel diffraction[124] (also known as near-field diffraction) of the projected light that is caused by the small gap between the mask and the wafer. To obtain a high resolution similar to contact photolithography without the defects and distortion of proximity photolithography, projection photolithography was developed as will be discussed below.

2.2.3 Exposure of Resists via Projection Photolithographic Techniques

The method by which the image of a photomask is projected directly onto the photoresist-covered substrate using high-resolution lenses is called projection

photolithography. This method avoids contact between the mask and the wafer. This technique, in fact, employs a large gap (>> 50 μm) between the mask and the wafer. In this system, the mask life is potentially unlimited except for damage due to handling of the mask. Projection photolithography was developed to obtain the higher resolution of contact photolithography while minimizing the accumulation or transfer of defects to subsequently patterned substrates.

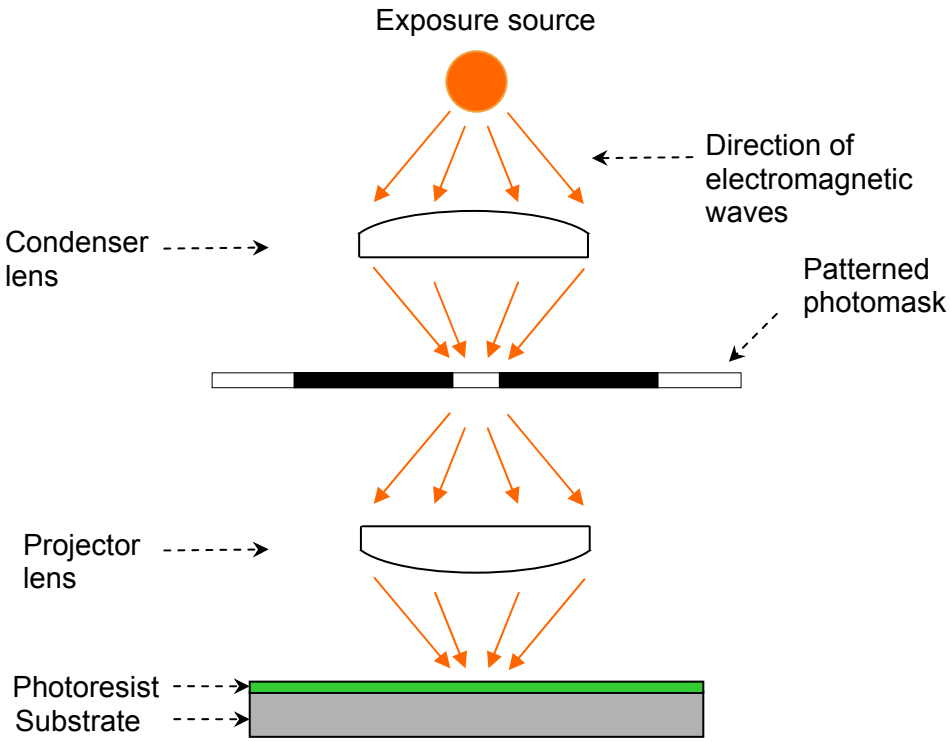


Figure 2-6: A schematic depicting *'projection photolithography.'*

Figure 2-6 shows a simple illustration of a projection photolithography system. The mask is held between the condenser and a second set of lenses called the projector or objective lens. The purpose of the projector is to focus the light transmitted through the mask onto the wafer. As there are optical components between the mask and the substrate, the projection system offers many advantages. These advantages include the

ability to change the reproduction ratio to produce images smaller than the original mask. In this system, Fresnel diffraction, a limitation in proximity printing, is no longer an issue. Instead, Fraunhofer diffraction [124] (also known as far-field diffraction) is in effect. Due to this diffraction, light which passes through a small pattern (narrow slit) does not produce a sharp, geometrical shadow identical to the shape of the pattern of photomask, but a distributed pattern of light intensity produced by diffraction. Aside from Fraunhofer diffraction, another drawback to this exposure technique is the compromise between resolution and depth of focus that will be discussed further in Section 2.4.2 of this thesis.

The resolution of a projection system can be limited by imperfections in the optical train. These imperfections may take the form of lens irregularities such as aberrations, or the separation between the mask and the objective lens may be incorrect. In most systems used nowadays the optics are, however, sufficiently well made that the resolution is limited by the ability of the optical train to efficiently collect and reimage the light.

In this thesis, it is demonstrated that through modification of an optical microscope, in which the optical components act as a projection system, the pattern on a photomask can be reduced in size by the objective lens and projected on photoresist coated substrates. This technique can extend the lithographic fabrication mainly performed in cleanroom facilities with use of expensive instrumentation to laboratories equipped with a bench top optical microscope. The two goals of this thesis are to utilize this technique for monitoring changes in properties of one-dimensional nanowires by measurements of conductivity and photoconductivity, as well as to connect and incorporate these nanostructures into an integrated electronic device.

2.3 Microscope Projection Photolithography

For production level processing, photolithography techniques require high quality, expensive equipment (~$750,000 to $4,000,000) such as mask writers and photolithography aligners, photomasks (~$500 to $2000) and access to dust free cleanroom environments. Such requirements are necessary since in contact printing, if dust particles are present, the pressure applied damages both the photomask and the photoresist. Access to this level of cleanliness and sophistication is necessary for microelectronic device manufacturing. For exploratory research one could, however, avoid using such expensive and sophisticated instrumentation and cleanroom facilities.

An approach to facilitate the need for exploring research on nanowires is provided by the technique described herein. This new approach requires a standard reflecting optical microscope (~$10,000 to $100,000) and comparatively lower cost projection photolithography masks (~$10 to $100), which is ideal for academic laboratories. This technique that was developed and optimized in the 1970s and 1980s by Palmer and Decker is called microscope projection photolithography (MPP).[121] Palmer and Decker were able to produce submicron patterns in photoresist by using a Zeiss RA optical microscope equipped with a II-B vertical illuminator. Using original masks with 20 μm features, positioned at the field diaphragm, they projected a reduced image of the mask though the objective lens and projected onto a photoresist layer. A schematic of their set-up is illustrated in Figure 2-7. More recently, this technique was applied by Love *et al.* [122] to produce rapid prototyping of photoresist patterns. These patterns were used as masters for replication into elastomers for use in soft lithography procedures.

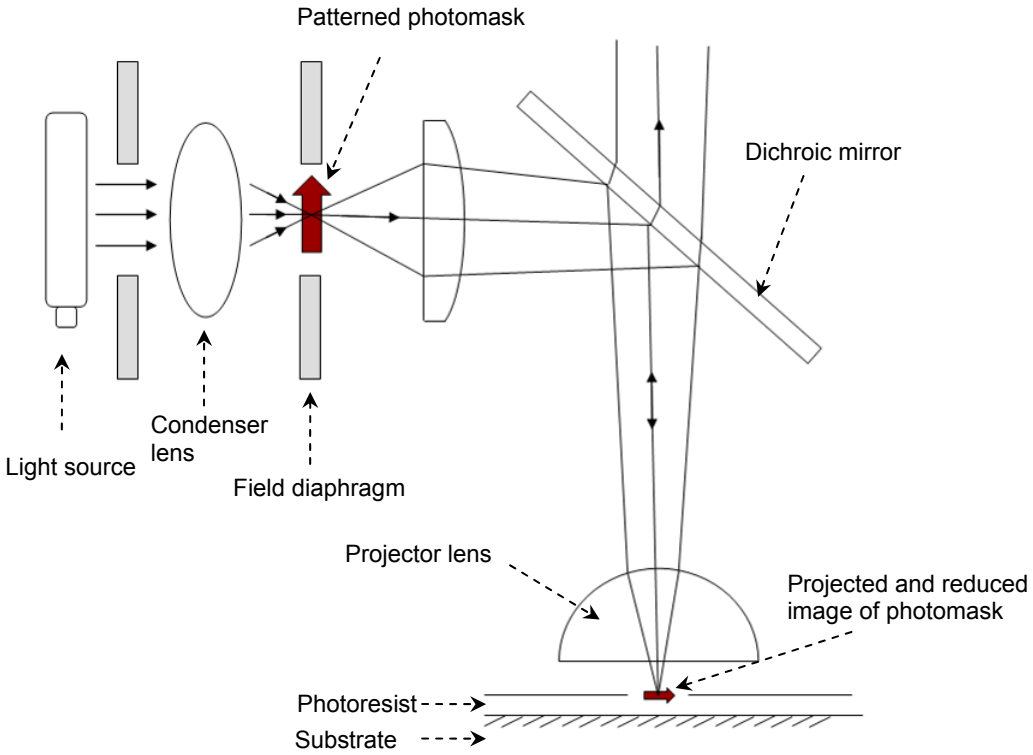


Figure 2-7: Schematic of the set-up for microscope projection photolithography used by Palmer and Decker in 1973.[121]

The goal of the research presented in this thesis is to make use of this projection lithography technique in order to create metal contacts overlaid on nanowires for electrical characterization purposes. Hence, it is essential to discuss some of the fundamental concepts in an optical microscope to understand the modifications performed to a Zeiss optical microscope (more details in 2.6.3) to make use of this technique. In the following discussion a device has been designed for use in a Zeiss

optical microscope, however, this design can be adapted for other microscopes or could be implemented using optical components laid out on an optical table.

2.4 Fundamentals of an Optical Microscope

2.4.1 Physics Behind Microscope Projection Photolithography

Microscopes are instruments designed to produce magnified visual or photographic images of objects too small to be seen with the naked eye. Modern compound microscopes are equipped with a two-stage magnifying design built around separate lens systems, the objective lens and the eyepiece, mounted at opposite ends of a tube, known as the body tube.

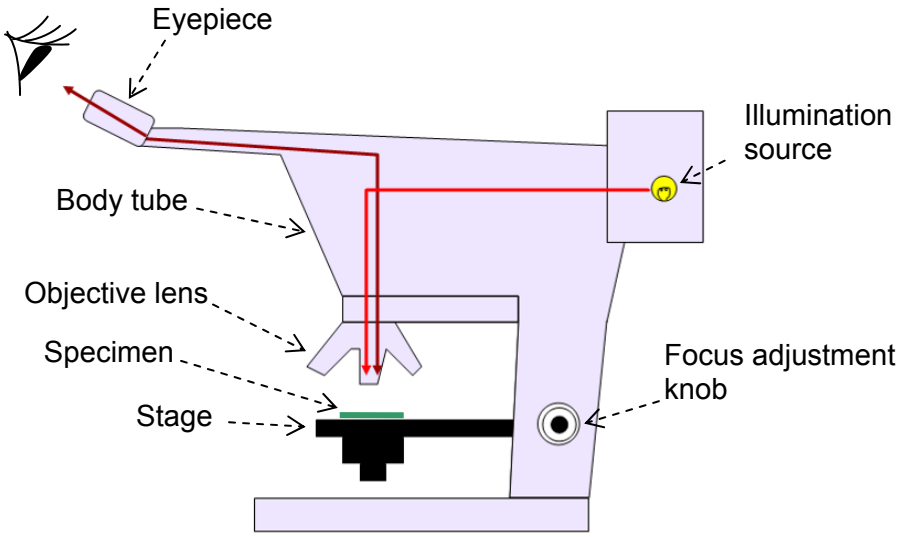


Figure 2-8: Schematic of a basic compound optical microscope.

The objective lens is composed of several lens elements that together form a magnified image (the intermediate image) of the specimen being examined. The

intermediate image is further magnified by the eyepiece. The microscopist is able to observe an enlarged image of the specimen by peering through the eyepieces. The total magnification of a microscope is determined by multiplying the individual magnifications of the objective lens and eyepiece lens. This section discusses the basic concepts associated with an optical microscope and how it could be used to project a pattern onto a photoresist coated substrate for the purposes of microfabrication.

A uniform illumination of high intensity is one of the most critical factors in determining the overall performance of the optical microscope. The full aperture and field of the instrument is usually obtained by adjusting the illumination system following the principles first introduced by August Köhler in the late nineteenth century.[167] This method, commonly referred to as Köhler illumination, creates an evenly illuminated field of view while illuminating the specimen with a very wide cone of light. Via this method of illumination two conjugate image planes are formed: one contains an image of the specimen and the other the filament from the light. The requirements for having two separate sets of conjugate focal planes, field planes and aperture planes, in precise physical locations within the microscope can be obtained once the conditions of Köhler illumination have been met. The details of adjusting a given microscope to satisfy the Köhler illumination conditions depend to some extent upon how the individual manufacturer meets the requirements. Through the rest of this section the advantage of having the separate conjugate planes, obtained via Köhler illumination, is elaborated upon. In this chapter, it is also shown how this set-up can be used for projection photolithography through modifying an optical microscope.

As mentioned before, along the optical pathway of an optical microscope that has been properly focused and aligned, there exist two sets of principle conjugate focal planes. One set consists of four field (or object) planes and is referred to as the field or

‘image-forming conjugate set’. The other set consists of four aperture planes and is referred to as the ‘illumination conjugate set’. Each plane within a set is referred to as the conjugate to the others in that set because they are each simultaneously in focus. Images of each of these planes can be viewed superimposed upon one another when observing specimens through the microscope. In other words, observing the specimen through the eyepiece, one should also be able to simultaneously view the conjugate set of field planes if the specimen is in focus.[123]

Table 2-2 lists the elements that compose each set of conjugate planes, as well as alternate names often found in the literature.[166] Also in Figure 2-9 a cutaway diagram of a Zeiss microscope is depicted, which labels the location of the two sets of conjugate planes in the optical pathways for both transmitted and incident illumination modes. Conjugate planes of the image plane are labelled with blue dotted lines, while those in the aperture plane are labelled in red.

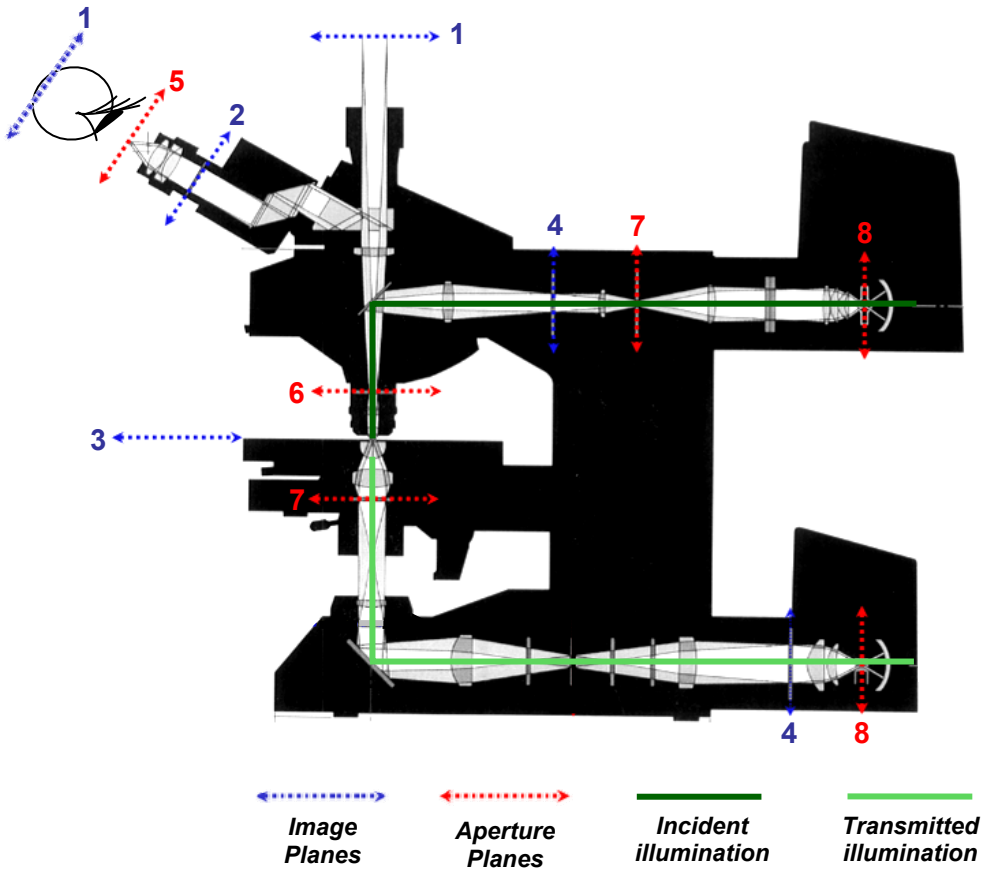


Figure 2-9: Conjugate planes within a cross-section of an optical microscope. *(Courtesy of Carl Zeiss Company)*

Table 2-2: Conjugate focal planes as labelled in Figure 2-9.

Field or image-forming conjugate plane set (blue dotted lines in Figure 2-9)	Aperture or Illuminating conjugate plane set (red dotted lines in Figure 2-9)
(1) Retina of the eye; camera image plane	(5) Eye point; microscope exit pupil; eye iris diaphragm
(2) Intermediate image plane	(6) Objective back focal plane
(3) Specimen plane	(7) Condenser aperture diaphragm
(4) Field diaphragm; Köhler diaphragm	(8) Light source

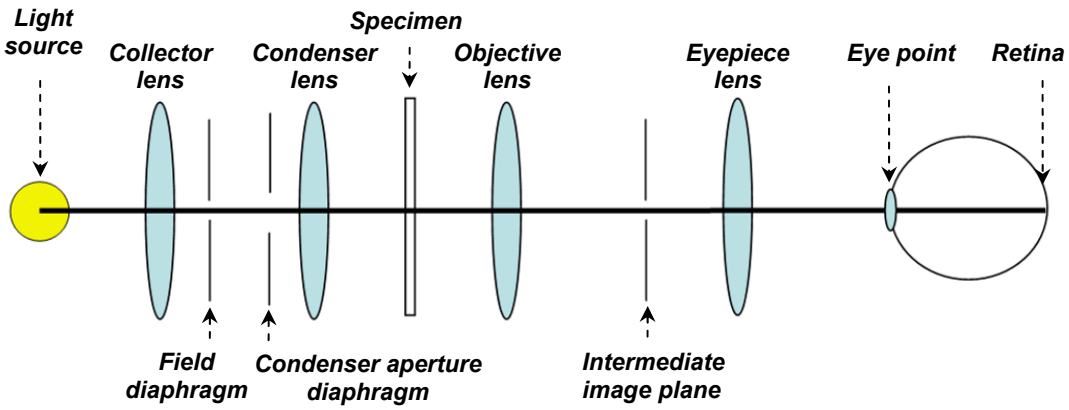
Planes belonging to the pair of conjugate sets alternate in the order in which they appear through the optical train from the light source filament to the final microscope image produced on the retina or the image plane of an electronic sensor. An understanding of the relationships between these conjugate plane sets, and their location within the microscope, is essential in understanding image formation and carrying out the correct adjustment of illumination. Also, the location of principal conjugate planes is often a key factor in the proper placement of optical components, such as phase plates, polarizers, or filters.

The basic requirements of Köhler illumination are simple. A collector lens on the lamp housing is required to focus light emitted from the various points on the lamp filament at the front aperture of the condenser while completely filling the aperture. Simultaneously, the condenser must be focused to bring the two sets of conjugate focal planes (when the specimen is also in focus) into specific locations along the optical axis of the microscope. Even though, the filament will not be in focus on the specimen plane, meeting the Köhler illumination will result in a bright, evenly illuminated specimen plane, even with an uneven light source such as a tungsten or halogen lamp filament. With the specimen and condenser in focus, the focal conjugates will be in the correct position so that resolution and contrast can be optimized by adjusting the field and condenser aperture diaphragms.

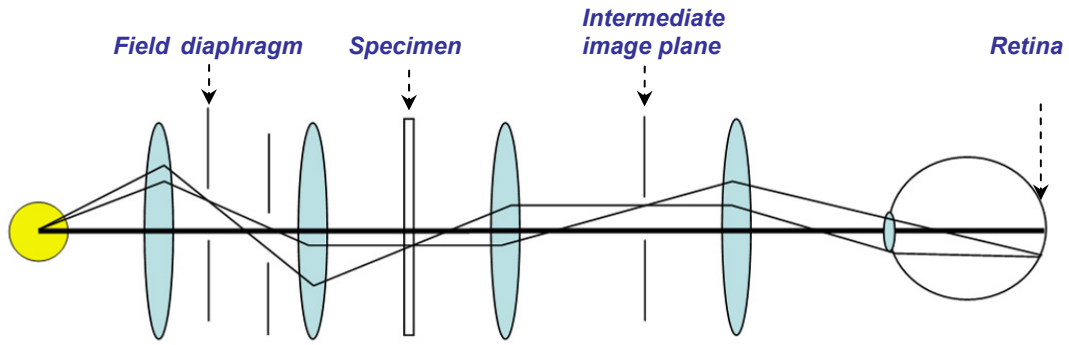
In Figure 2-10, the optical components of a simple set-up of an optical microscope, adjusted for Köhler illumination, is presented. In addition, each set of conjugate planes is shown using crossover points of the ray traces. This figure presents the reciprocal nature of the two sets of conjugate planes that occur in the microscope. The optical relationship between the sets of conjugate plane is based upon the fact that, in the illuminating light path, the spherical wave fronts converge and are brought into

focus onto the aperture planes. On the other hand, in the image forming light path, the spherical waves converge into focused rays in the field planes. Light rays that are focused in one set of conjugate planes are nearly parallel when passing through the other set of conjugate planes.[165] The reciprocal relationship between the two sets of conjugate planes determines how the two ray paths fundamentally interact in forming an image within the microscope. This relationship between the two sets also presents practical correlations for optimization of the microscope.

(a) Optical components of a microscope adjusted for Köhler illumination



(b) Conjugate planes for image-forming rays in Köhler illumination



(c) Conjugate planes for illuminating rays in Köhler illumination

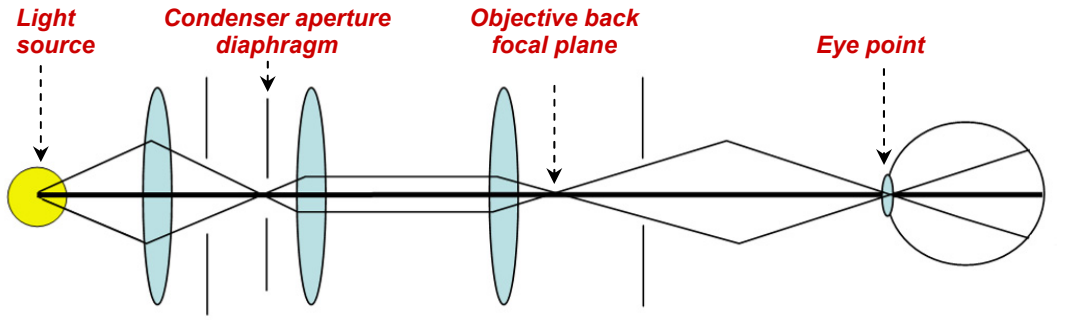


Figure 2-10: Schematic of the optical components of a microscope adjusted for Köhler illumination. In parts b) and c) the conjugate planes for the image-forming and illuminating sets are indicated by crossover points of the ray traces.

2.4.2 Fundamental Equations for Photolithographic Techniques

Various factors in optical lithography can be tuned to decrease the minimum feature size of the pattern produced on substrates. Some of these tunable factors will be discussed in this section. The fundamental equations governing resolution for all photolithography techniques and the important factors involved for the choice of optical components in projection photolithography in the context of patterning electrical contacts on nanowires also will be discussed.

The German physicist Ernst Abbe (1840-1905) defined a quantitative value for the angular aperture of a lens called the numerical aperture[166,167] (usually abbreviated as *NA*), such that

$$NA = n \sin \alpha \qquad \textbf{Equation 2-1}$$

Where *n* is the refractive index of the medium between the object and the lens, and α is half the angular aperture (intake angle of the lens) as seen in Figure 2-11. Half the angular aperture can be determined [166] using:

$$\alpha = 2 \arctan(\frac{D/2}{f}) \qquad \textbf{Equation 2-2}$$

where '*f*' is the focal length of objective lens and '*D*' is the diameter of aperture used.

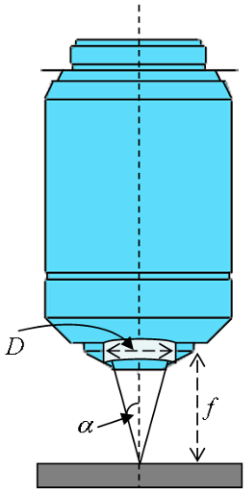


Figure 2-11: A schematic of longitudinal slice of a microscope objective lens with the cone of light revealing the angular aperture 'α', where image-forming light waves pass through the specimen and enter the objective lens in an inverted cone as illustrated. Focal length '*f*' and diameter of aperture '*D*' are also shown in the figure.

The numerical aperture (*NA*) of a microscope objective lens is a measure of its ability to gather light and resolve fine specimen detail at a fixed object distance. Mathematically it is possible to calculate the resolution (smallest feature that can be seen), the light intensity and the depth of the field for a specific lens. The *NA* of a lens is an extremely important notion in optical microscopy. In fact, it is so important that all modern microscope objective lenses have this information indicated on the barrel of each lens.[167] The *NA* marked on a lens is the maximum possible value with that particular lens. The importance of identifying an objective lens with a particular *NA* will be discussed further in the next section.

Factors Affecting the Resolution Limits for Photolithography

The resolution of an optical element is defined as the minimum distance between two points for them to be resolvable in the microscope and is given by the Raleigh criterion [166] and based on the following equation:

$$resolution = k_1 \frac{\lambda}{NA} \qquad \textbf{Equation 2-3}$$

In Equation 2-3, k_1 is a constant that depends on the thickness and index of refraction of the photoresist (generally k_1~0.6);[166] λ is the wavelength of the radiation used to expose the resist. For the minimum resolved distance to be kept small, the wavelength should be as small as possible. For use of the light microscope this might not have tremendous practical importance, but it suggests the desire to improve resolution working with short wavelength light that has led in turn to use of blue light, ultraviolet, X-rays and electrons as sources of illumination. To minimize resolution in photolithography, however, fewer choices of the wavelength of light used may be possible since λ is dependant on the sensitivity of photoresist. The electron-beam lithography has a high resolving power only because of the very low wavelengths associated with the electron-beam (~0.2 to 0.5 Å).

The numerical aperture of the focusing optical elements is typically ~0.5. The numerical aperture of the lens system is an important factor in determining the image quality of a specimen. From the formula in Equation 2-3, it is seen that the *NA* should be as large as possible to minimize the resolution. Choice of numerical aperture of the objective lens is very much in hands of the experimentalist and not dependant on choice of photoresist.

The refractive index of the medium, *n*, in between the lens and the specimen is another important factor. Given Equation 2-1, another logical approach that can be taken to increase *NA* is to increase refractive index between the sample and the lens. The gap for most lens systems is occupied by air, which has a low refractive index value. Successful common practice to achieve a high lens numerical aperture makes use of so-called immersion lenses with high refractive index liquids such as water (~1.3) or oil (~1.5).[175]

Increasing the numerical aperture increases the resolution linearly, but this approach to improving resolution has limitations as well. As shown in Equation 2-4, the depth of focus of a lens, σ, is inversely proportional to the square of the *NA*, so improving the resolution by increasing the *NA* reduces the depth of focus of the system. The depth of focus also known as depth of field, can be described as the distance along the optical train that the object can be moved and still keep the image in focus.[165] For a projection system, σ is given by:

$$\sigma = \frac{\lambda}{NA^2} \qquad \textbf{Equation 2-4}$$

The depth of field is an opposing factor to lowering the resolution since it increases the practicality of the experiment by extending the range over which the sample can be positioned. For a particular focus setting for the microscope, points in the specimen above and below the true focus will also appear acceptably sharp to the observer; they appear to be 'in focus'. It is this distance (depth) between the uppermost and lowermost acceptable sharp points that is referred to as the depth of focus, which varies from a distance of ~0.5 μm for a 1.3 *NA* lens, to ~10 μm for a 0.25 *NA* lens.[165] It

is important to note that the phrase ‘depth of focus’ has a different meaning and is associated with the image plane; depth of field relates to the specimen. Since the depth of field is dependent on a function related to the *NA*, as seen in Equation 2-4, reducing the effective *NA* of the optical system will increase the depth of field. Poor depth of focus is not ideal as small height differences in the photoresist (which may come from a tilt caused by dust or debris under the wafer) as it may cause some positions on the wafer to be out of focus. Thus, proper design of aligners used in projection photolithography must consider a compromise between resolution and depth of focus. Finally, the image resolution is also a function of the spatial coherence of the light source. Optical imaging systems for projection photolithography are classified as either coherent or incoherent, depending on the type of illumination employed.

As will be discussed in Section 2.5, a pattern is required for exposure of resist covering nanostructures in order to position electric contacts on these nanostructures. The pattern that ultimately will contain features of the electrical contacts on nanowires needs to be comparable in size to the nanostructure. Hence, it is crucial to have an optimum resolution using the factors mentioned in this section. A general and basic process for the steps that were taken to produce electric contacts on nanowires will also be discussed. In following general steps for the fabrication process, the exposure source will be either the photons, using the microscope projection photolithography technique, or electrons, using electron-beam lithography. Both techniques were used in this research project and are discussed further in the rest of this chapter and Chapter 3 of this thesis, respectively.

2.5 An Overview of the Fabrication Steps to Overlay Electric Contacts on Selenium Nanowires

The lithographic process is a set of steps used to selectively remove or deposit materials in a designed layout. The general sequence of processing steps for a typical lithography process includes: substrate preparation, resist spin coating, pre-exposure baking, irradiation with photons or electrons, post-exposure baking, developing with a solvent, post baking, metal deposition and lift-off. Figure 2-12 is an optical micrograph of two metal electrodes overlaid on a nanowire. This result of aligning electric contacts to nanowires is achieved through a series of lithographic processes.

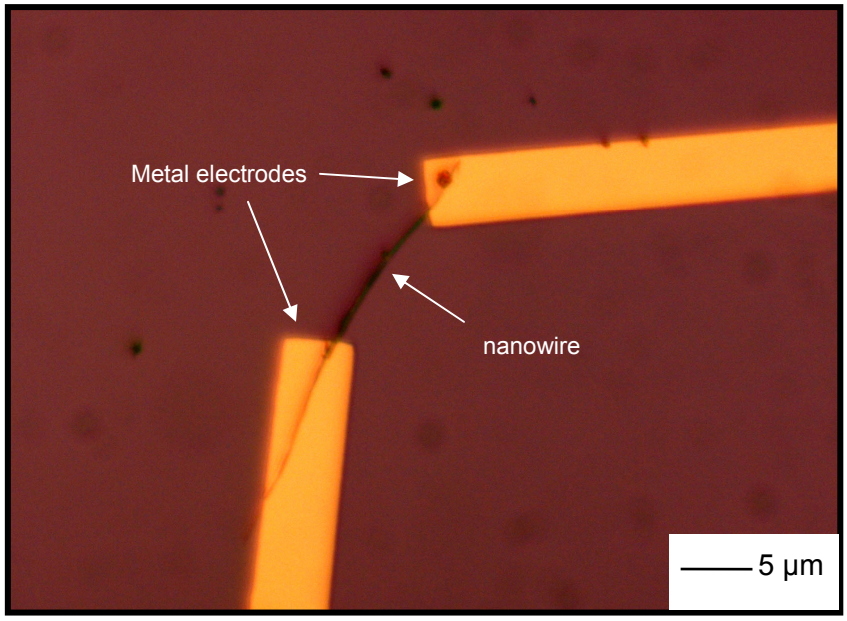


Figure 2-12: A bright field optical micrograph of two electrodes overlaid on a nanowire.

How would one fabricate metal electrodes on nanowires? The process used is shown schematically in Figure 2-13 and Figure 2-14 and will be discussed with more detail in the following section.

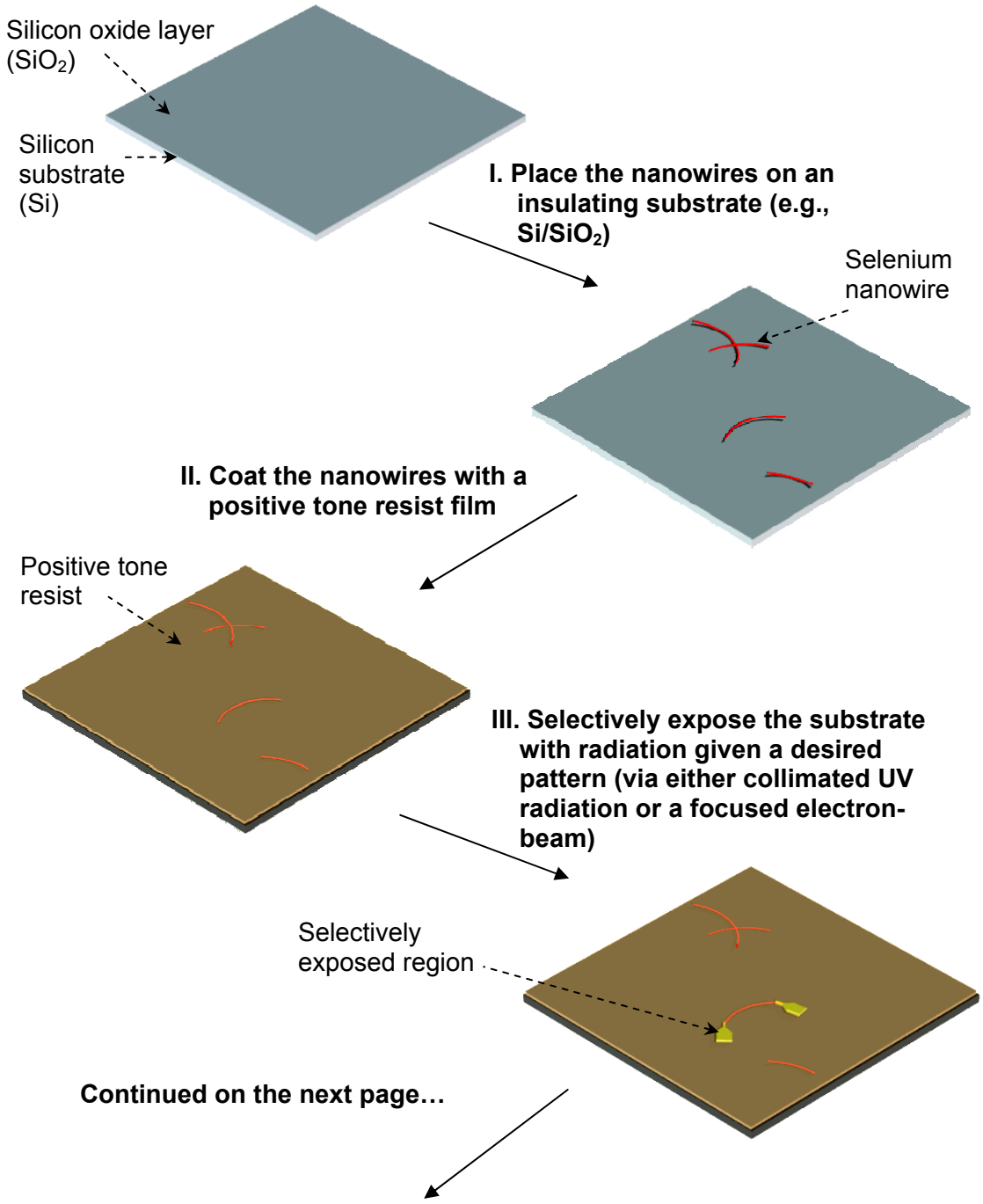


Figure 2-13: Part I of a schematic representation of the steps involved in overlaying metal contacts on selenium nanowires. See part II in Figure 2-14 on page 53.

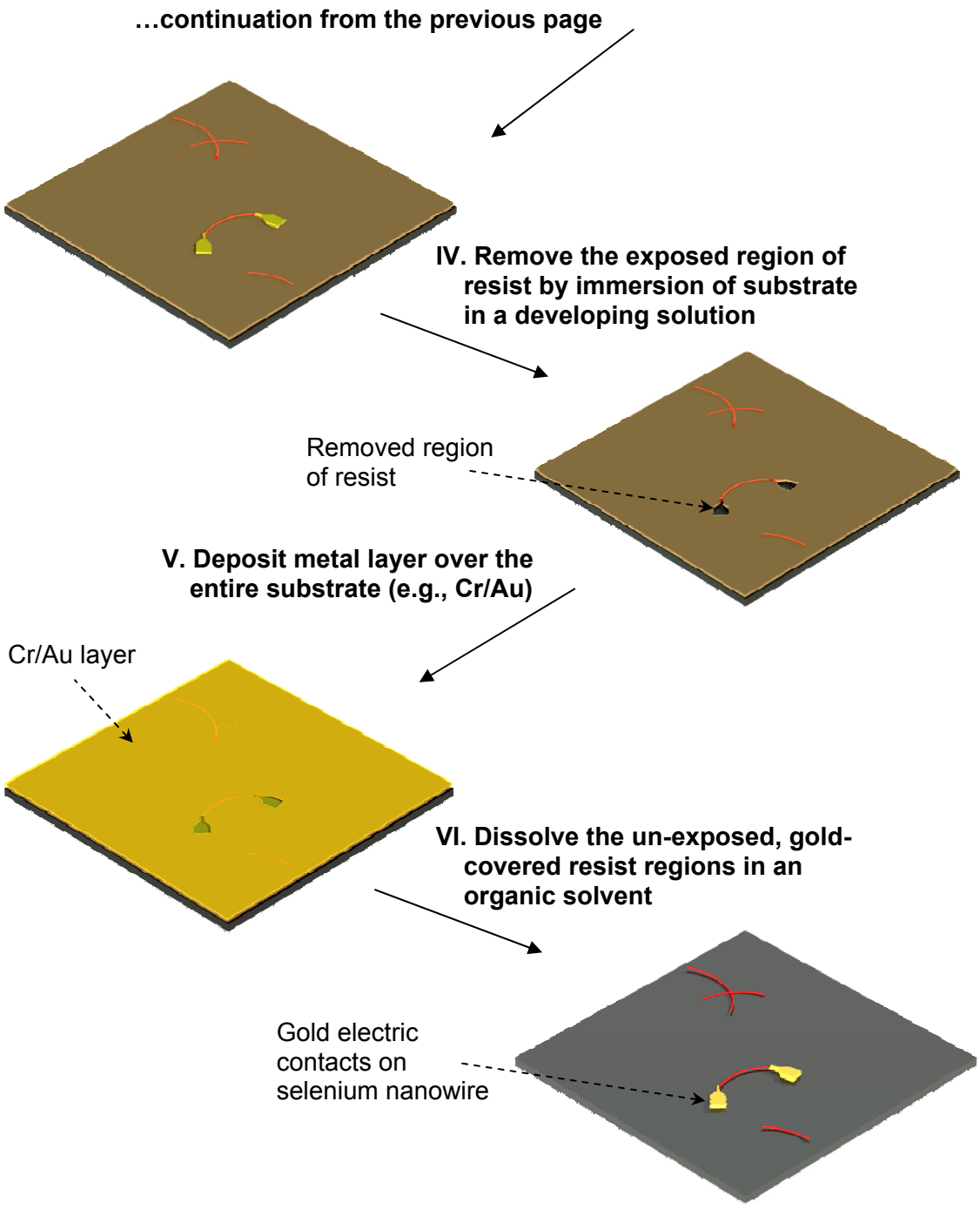


Figure 2-14: Part II of a schematic representation of the steps involved in overlaying metal contacts on selenium nanowires.

2.5.1 Growth of an Oxide Layer on Silicon Wafer Substrates

The ultimate goal of the fabrication process used in this thesis is to prepare a substrate on which to measure nanowire conductivity. It is, therefore, important to position these nanostructures on an insulating surface. The growth of a thick silicon oxide (SiO_2) layer on a silicon wafer requires exposure of the wafer to O_2 gas at high temperatures. This silicon dioxide film is a high-quality electrical insulator. In fact, the primary reason for silicon becoming the dominant material in fabrication of integrated circuits is the property of silicon that it can act as a barrier to diffusion or impurity implantation. The polished silicon wafer surface is generally a metallic gray colour. Once SiO_2 is formed on the wafer, the surface will have a colour that depends on oxide thickness. A layer of silicon oxide can be prepared by a number of methods including thermal oxidation, chemical vapour deposition, and sputtering.

The most common approach to obtain a thin film of silicon oxide on a silicon wafer is through thermal oxidation, which can be easily achieved by heating the wafer to a high temperature, typically 900-1200 ºC.[133] There are two methods to grow SiO_2: i) dry oxidation using dry oxygen; and ii) wet oxidation using water vapour. Dry oxidation is usually used to form thin oxides in a device structure because of its good Si-SiO_2 interface characteristics. On the other hand, wet oxidation is used to produce thicker layers of SiO_2 because of its higher growth rate and is generally used to create an electrically insulating layer. Chemical vapour deposition techniques can also form thin films covering the surface of a substrate by thermal decomposition or reaction of gaseous compounds.[131] The material of interest is deposited directly from the gas phase onto the surface of the substrate. Sputtering is achieved by bombarding a target (e.g., SiO_2) with energetic ions, typically Ar^+, whereby atoms at the surface of the target are knocked loose and ejected towards the silicon substrate, where deposition occurs.

Thermal oxidation is one of the more commonly used techniques recognized for producing high-quality oxide layers in terms of density, uniformity and dielectric strength than any other method. Among the two thermal oxidation techniques, dry thermal oxidation produces a relatively higher quality oxide in terms of density, as the oxide growth is a slower process. In experiments performed in this thesis, the wet-oxidation technique was used as multiple wafers could be placed in the chamber of the instrument, requiring less processing time.

2.5.2 Pre-Treatment of Silicon Wafers

Substrate preparation is intended to improve the adhesion of resist material to the substrate and provide for a particulate- and contaminant-free resist film. This pre-treatment is accomplished by one or more of the following processes: i) substrate cleaning to remove contamination (as particulates result in defects in final resist pattern); ii) dehydration bake to remove water; and iii) addition of an adhesion promoter.

One very important solvent used in wafer cleaning before and throughout the fabrication processes is de-ionized (DI) water. De-ionized water is filtered and highly purified to remove a variety of impurities and residues that include all traces of ions and particulates. Standard DI water systems achieve a resistivity of around 18.0 MΩ. After the rinsing of the wafer surface with DI water to remove all the residues and particles, the wafer has to be thoroughly dried so that the resist can adhere well to the surface. The wafer must, therefore, be placed in an oven or on a hotplate to completely dry. Another process that could be used to improve resist adhesion is to coat a thin layer of HMDS (hexamethyldisilazane) onto the silicon surface. Without good adhesion, resist patterns may peel off from the substrate after subsequent processing stages.

2.5.3 Spin-Casting a Resist Layer

The next step after pre-treatment of a silicon wafer is to deposit a solution of *t*-Se nanowires dispersed in a resist solvent mixture onto the silicon wafer. Resists can be applied to the surface of the wafer by several methods, including spin coating, spray coating, and dip coating.[124] The most commonly used method for coating resist onto wafers is spin coating. During spin-coating, shown in Figure 2-15, excess amount of resist is dispensed onto a wafer substrate and the wafer accelerated to a certain spin speed to form a thin film of the desired thickness. Spin coating processes use the dynamics of centrifugal force to disperse resist material over the entire wafer surface. Centrifugal force arises in connection with rotation and is experienced as an outward force away from the center of rotation. By high-speed spinning of the vacuum chuck, the photoresist uniformly spreads over the entire surface to result in a resist of uniform thickness.

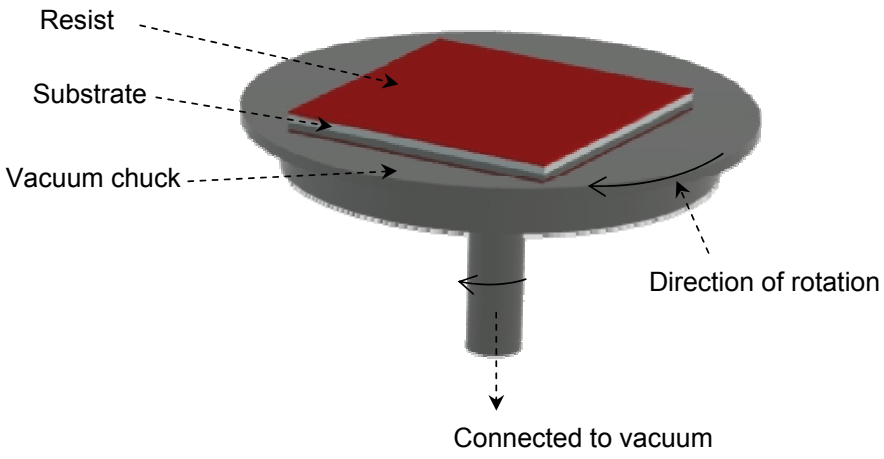


Figure 2-15: Schematic illustration of the key components for coating a substrate with resist by a spin-coating process.

As a solution of resist is spin cast, the film thickness decreases uniformly, at a rate dependant on the spin speed, resist viscosity, solvent evaporation rate, and initial film thickness.[124] Improperly cleaning the wafer in the previous step may leave particles that would result in pinholes or streaks (radial patterns within the resist) and a non-ideal resist film. Striations may also occur due to non-uniform drying of solvent during spin coating.

Resist thickness is set primarily by resist viscosity, and secondarily by spinner rotational speed. The lower the viscosity (that is related to the concentration of polymer) and the higher the angular speed of spinning, the thinner the film can be made. There are usually spin curves reported for available concentrations of a resist that provides a general guideline for the thickness of the resist depending on the speed of spinning. For instance a spin curve for 2% 950 k average molecular weight PMMA (poly methylmethacrylate) in anisole (w/v) is shown in Figure 2-16. The estimated thickness of PMMA resist spun on a substrate (discussed in Section 3.4.1) is based on the following curve. A more exact value on the thickness can be measured using a profilometer or scanning probe microscope.

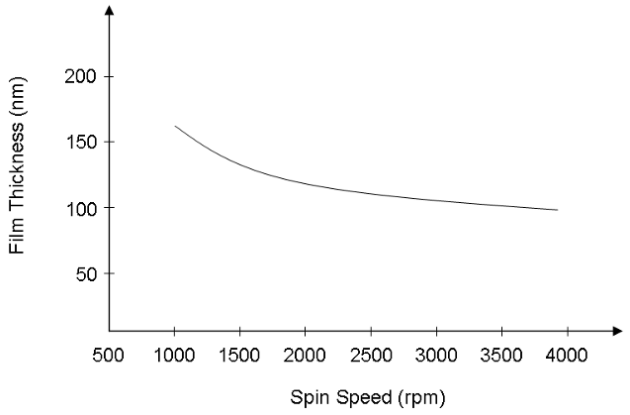


Figure 2-16: Spin curves provided by MicroChem. Corporation for 2% PMMA in anisole (w/v), depicting different film thickness obtained from spin speed of the resist coated substrate.[158]

2.5.4 Pre-Exposure Bake of Resist

After coating resist, the wafer should be thermally baked before the exposure process. The purpose of this pre-exposure bake is to drive out most of the solvent in the photoresist layer to improve adhesion of resist to the substrate. Prior to coating, the solution of resist is composed of 65 to 85% solvent. Once spin cast, the solvent content is reduced to 20 to 40% and the film is considered to have a 'solid' state.[117] Note that there are variations on reported values of the remaining percentage solvent content depending on resist viscosity and the amount of solvent evaporation due to air flows in the spin coating instruments. There are, therefore, discrepancies in values reported in literature, such as 10 to 20%.[124] If the resist-coated substrate was exposed and processed at this point, a number of undesirable consequences would result. At this solvent level, the film is highly susceptible to particulate contamination, which can be transferred through handling to subsequent steps. Other consequences of soft-baking include a reduction of porosity within the resist and polymer relaxation, which have been suggested to be important phenomena that affect resist process performance.[106] Pre-exposure-bake is more commonly known as "pre-bake" or "soft-bake". The recommended temperature and baking time is specified by each photoresist manufacturer's data sheet.

2.5.5 Irradiation of Resist

After soft-baking, the resist is ready for exposure. Exposure of resist involves the absorption of radiation and subsequent photochemical change, resulting in a modification of dissolution properties of the resist. Depending on the resist used, whether for the MPP or EBL technique, ultraviolet (UV) light or a beam of focused electrons, respectively, is utilized for the exposure process. The substrate, specifically

silicon wafers coated with nanowires embedded in a resist, must be aligned and positioned properly for exposure. The alignment involves finding the desired nanowires and making sure that the pattern of interest is exposed in an accurate location with respect to the designated nanostructure, the details of this are provided in Sections 2.6.3 and 3.4.2. In this step, the appropriate exposure dose of electrons or photons has to be optimized, the conditions of which are sample specific relying on factors such as choice of resist and film thickness.

2.5.6 Post-Exposure Bake of Resist

A post-exposure bake step is mainly performed to eliminate more of the solvent in the resist and improve adhesion of resist to the substrate. Depending on the resist type, whether it is photons or electrons sensitive, a post-exposure bake may need to be carried out.

2.5.7 Developing of the Resist Coated Substrate After Post-Exposure Bake

Once the resist coated substrate has been exposed, the resist must be developed with an appropriate solvent. The development stage is undoubtedly one of the most critical steps in the processing.[161] The basic principle behind the operation of a resist is to enhance a change in solubility of the exposed and unexposed portion of resist in a developer solution following irradiation. Depending on the type of resist, positive or negative tone, different results are obtained. Irradiation induces a chemical change in the resist material which allows pattern formation in the resist material. For a positive resist, for instance, the irradiation of the polymer causes chemical bonds to be broken to

form fragments of smaller molecular weight. Therefore, areas that have been irradiated and have smaller molecular weight fragments than the native, unexposed resist can be dissolved in a developer solution that solvates the low-molecular-weight material. For a negative resist, the radiation induces cross-linking. This cross-linking creates a complex three dimensional structure with a molecular weight higher than that of the non-irradiated resist. The non-irradiated resist can be selectively removed by dissolution in a developer solution that does not solvate the higher-molecular-weight polymer.[161]

The longer the developing time, the more dissolution takes place for the resist coated wafer. Substrate developing time must be experimentally optimized to obtain ideal removal of resist during this process. Figure 2-17 illustrates the effects of developing time on a single-layer resist coated substrate and points out the ideal result.

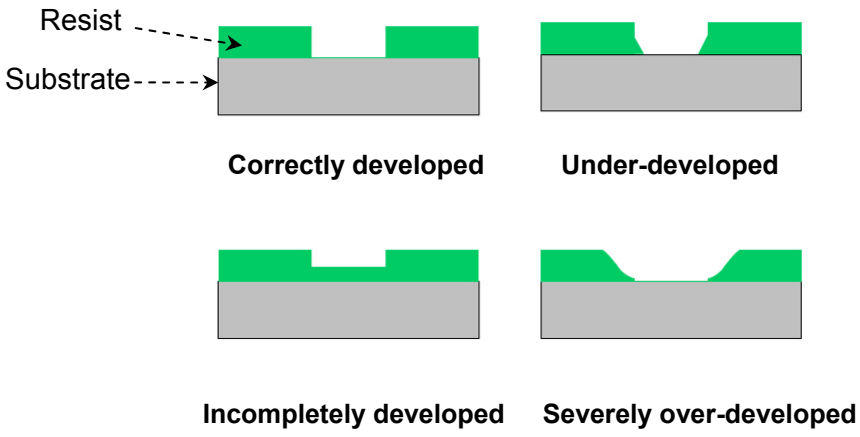


Figure 2-17: A schematic depiction of the possible developing outcomes on a resist coated substrate. Note that only the figure labelled 'correctly developed' is ideal and other figures are provided for comparison purposes.

Following this developing step, the underlying nanowire is uncovered for the fabrication of a metal contact.

2.5.8 Hard Bake of Resist

Hard bake is the last heat treatment operation in the fabrication process. Its purpose is essentially the same as the soft-bake step, that is, to evaporate the solvent left in the resist in order to harden it. The reason to do the 'hard bake' step is mainly to enhance the adhesion of the patterned resist to the silicon wafer by high-temperature baking of the developed wafer in an oven or on a hotplate. A downside to the hard-bake step is that it could make resist more difficult to remove during the lift-off process, as will be discussed in Section 2.5.10.

2.5.9 Metal Deposition on Resist Covered Silicon Wafers

In order to form metal contacts and interconnections between nanostructures and other device components, a necessary step is metal deposition, commonly referred to as the metallization. Metal films can be formed via various techniques of physical and chemical deposition. Two commonly used physical deposition techniques are sputtering and thermal evaporation processes. Since a thermal metal evaporator was utilized for metalizing the substrate, only this technique will be discussed in further detail herein.

Thermal evaporation is one of the most commonly used metal deposition techniques.[124] It operates by heating a metal to sufficiently high temperatures to vapourize it, after which the metal vapours re-condense onto a cooler substrate to form a thin film. The heating of metal is carried out under vacuum by passing a large current through a filament (usually in the shape of a basket, boat or crucible) which has a

predetermined electrical resistance. The metal to be deposited on the substrate is placed in the filament and the substrate is assembled on the top as seen in Figure 2-18. The choice of this filament material is dictated by the evaporation temperature and its inertness with the metal vapour. This technique is also known as 'indirect' thermal evaporation since a supporting material is used to hold the metal source.

Once the metal is evaporated, the vapour atoms undergo collisions with the surrounding gas molecules inside the evaporation chamber. As a result a fraction of vapour atoms is scattered within a given distance from the filament during their transfer to the substrate through the ambient gas. The mean free path for metal atoms at 25 °C is ~45 and 4500 cm at pressures of 1×10^{-4} and 1×10^{-6} Torr, respectively.[133] Therefore, pressures lower than 1×10^{-5} Torr are desirable to ensure a straight line path for the majority of evaporated metal atoms. Such a good vacuum is also a crucial factor for producing contamination free metal films. A thermal evaporator tool can monitor the thickness of the deposited materials by the use of a quartz crystal monitor. Common metals used for evaporation include silver, gold, aluminum, nickel, and chromium. Obviously, only materials with a much higher vapour pressure than the heated filament can be deposited without contamination of the filament metal in the film.

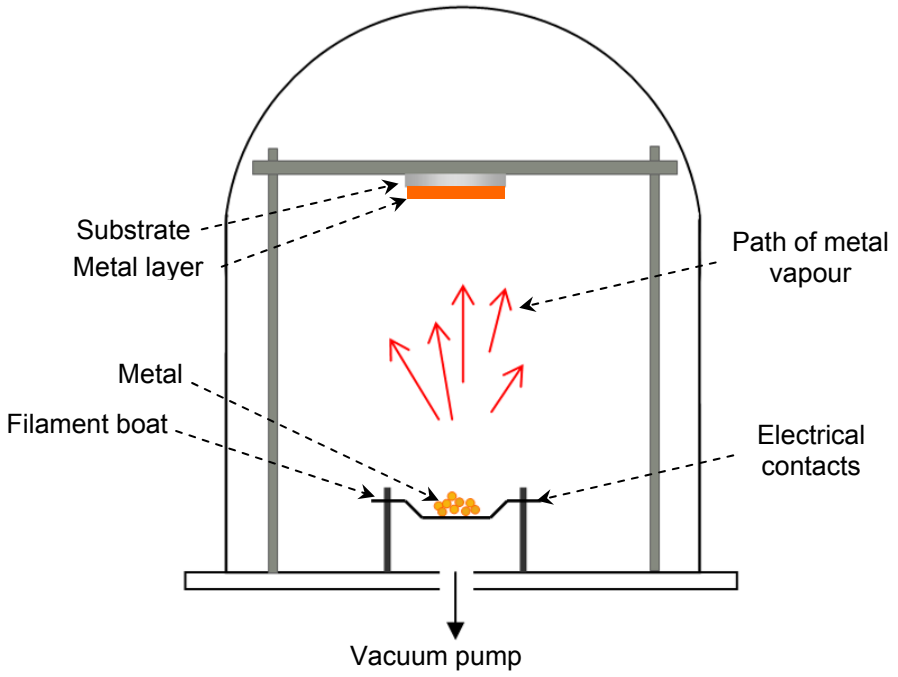


Figure 2-18: A simplified diagram of a thermal evaporator instrument.

2.5.10 Lift-Off of Metal Layer from Resist-Coated Wafers

Once the substrate is metal coated, to form the pattern of interest, the substrate is placed in a solvent to dissolve the remaining resist and along with that the metal layer coated on top of this resist will lift-off. This lift-off step allows the patterning of metal without the use of metal etchants – in which protecting layers are used on the substrate in a given pattern to remove unprotected parts. In the lift-off process, it is often recommended to use heat and/or sonication techniques to assist in the removal of metal layers on the resist (see Figure 2-19). Sonication techniques use ultrasonic waves which help to disconnect and break the fragile connection of the metal coating the resist to the

metal covering the exposed substrate. On the other hand, heating the substrate in the solvent helps to promote the dissolution of the remaining resist.

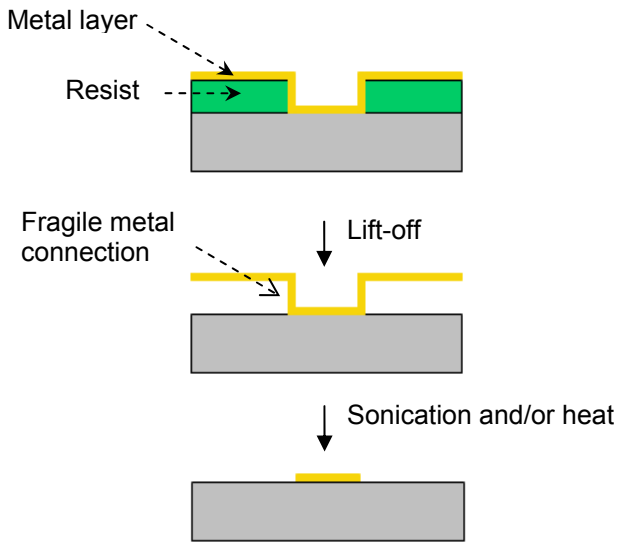


Figure 2-19: A cross-sectional schematic of substrates coated with resist before and after the lift-off process.

2.6 Experimental Details & Discussions for Fabrication of Metal Contacts on Selenium Nanowires via Microscope Projection Photolithography

As discussed in Section 2.5, a number of steps need to be followed for the overlay of metal contacts on nanowires. The details of this procedure with use of microscope projection photolithography are described below.

2.6.1 Silicon Wafer Substrate Pre-Treatment

The fabrication process used silicon wafers as the substrate. These silicon wafers were purchased from Silicon Sense, Inc. (3-inch diameter, N/Phos, <100>, 1-10 Ohm-cm, 381± 50 microns thick, SEMI std. flats, one side polished, test grade). As mentioned earlier (in Section 2.5), an oxide layer needs to be deposited onto the top surface of the silicon wafer to provide an insulating layer for the later electrical characterization of selenium nanowires.

Growth of an Oxide Layer on Silicon Wafers

The silicon wafers were placed in a ceramic container covered with a lid and placed in a furnace (Barnstead Thermolyne Furnace 4800) for the growth of a thermal oxide layer. The temperature of the oven was slowly raised (1 °C/min – 2 °C/min) to a temperature of 1050 °C (the maximum temperature of this furnace) and kept at that temperature for 5 h before slowly cooling back down to room temperature, as shown in Figure 2-20. The small plateaus shown in the graph represent the 5 min wait time at 120 and 600 °C. These plateaus were used to slow down the rate at which the temperature of the silicon substrate was increasing and ensure substrate would not break due to a quick raise in temperature.

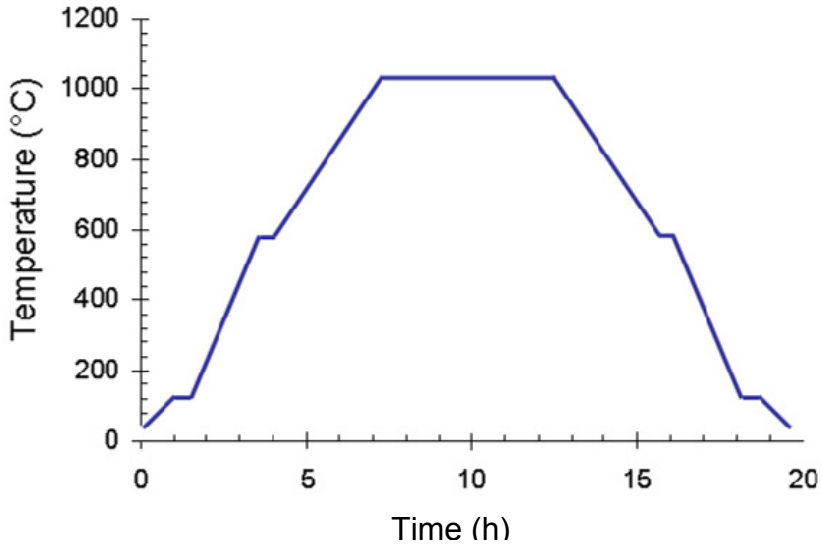


Figure 2-20: A graph of the thermal heating process for oxide growth on silicon wafer substrates.

A number of attempts were made that resulted in wafers with non-uniform oxide layers. These non-uniformities were most likely due to uneven heating within the furnace due to an opening in the chamber for ventilation. This non-uniformity was deduced from the variation in colour across the surface of the wafer.[164] Hence, a wet thermal oxidation approach was pursued in the Engineering Department at SFU and a fairly uniform silicon oxide layer was grown on the silicon substrates.

To measure the thickness of the silicon oxide, we used a Jobin-Yvon UVISEL NIR variable angle spectroscopic ellipsometer with a 75 Watts Xenon lamp light source. Multiple spots of ~1 mm^2 were studied with an operating wavelength of 450 nm and at a 70^o angle of incidence. The model used for fitting was "Si/SiO_2 bilayer model" and using Cauchy fitting in DeltaPsi2 software the thickness of the oxide was estimated at various points on the substrate. The average thickness value from these measurements indicated an oxide layer of ~277 ± 10 nm.

These wafers were cleaved into smaller (~1 cm x 1 cm) chips for use as substrates. Selenium nanowires (see the synthesis of *t*-Se nanowires in Appendix A) were then deposited onto the surface of the silicon chips via spin casting from a solution of nanowires suspended in isopropanol. Figure 2-21 is a schematic representation of nanowires randomly placed on the silicon substrate. It is important to note that significant efforts were put into dispersion of these nanowires as they aggregated in solution after synthesis. Aggregated nanowires are not ideal for spin casting, resist coating and more importantly for electrical measurements (see Chapter 4). Images of the aggregated and bundled *t*-Se nanowires can be found in Appendix A.

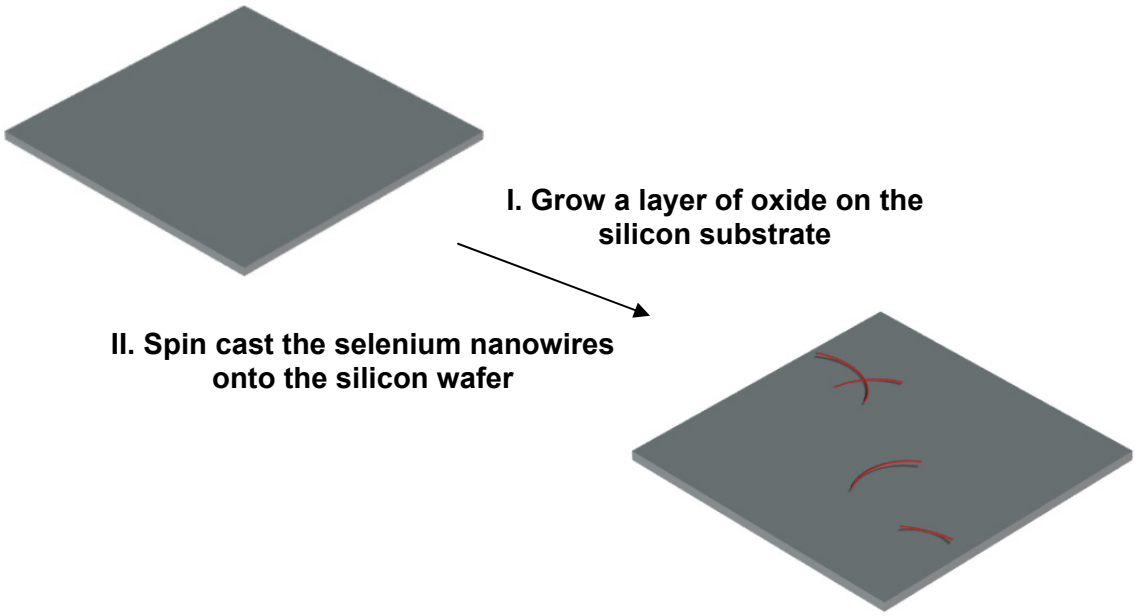


Figure 2-21: A schematic representation of an oxidized silicon wafer with dispersed selenium nanowires deposited onto its surface.

2.6.2 Deposition of an Ultraviolet Sensitive Photoresist onto Silicon Wafers

Choosing a Photoresist Sensitive to Ultraviolet Light

The lithographic properties of photoresists are determined by several factors. One key factor is to have the light sensitive component of the resist to absorb in the region of wavelengths of the source of light employed. Another factor is the necessity to have a change in the chemical properties of the resist upon exposure to this light source to distinguish between the exposed and non-exposed areas. One very common positive photoresist, sensitive to the i-line of the mercury lamp, is based on a mixture of a derivative of diazonaphthoquinone (DNQ) and a novolac resin (a phenol formaldehyde resin). The photoactive component of the resist is DNQ and can contain different substituents in position R shown in the Figure 2-22. The choice of the substituent R can have an effect on both the solubility and the absorption characteristics of the resist. Upon irradiation, the DNQ undergoes a number of reactions including a Wolff rearrangement followed by hydrolysis to generate a base-soluble indene carboxylic acid.[126,127] This acid, unlike the starting diazonaphthoquinone, is readily soluble in aqueous alkaline solutions due to the formation of an ionized salt of the acid. Hence, the developing solution that is used to treat the substrate after exposure is a basic solvent (usually tetra-methyl ammonium hydroxide in water) to remove the exposed regions of the film.

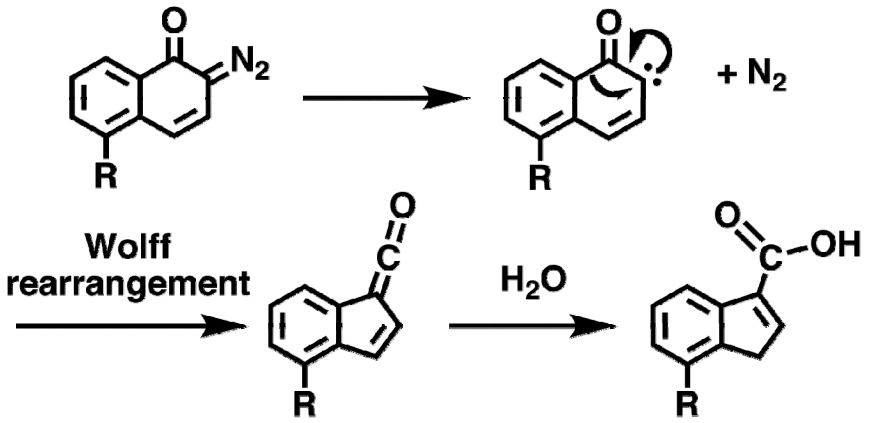


Figure 2-22: Diazonaphtoquinone is the photoactive component of SPR-220 resist (manufactured by Rohm and Hass Electronic Materials) that goes through the outlined chemical reactions after UV irradiation.

The argument mentioned above assumes that the major contribution to the change in dissolution rate in the DNQ systems is the change in solubility associated with conversion of the DNQ into the corresponding indene-carboxylic acid. However, there are conflicting reports on this matter. Kanazawa *et al.* compared the dissolution rate of DNQ systems, in which the diazonaphtoquinone was photolytically converted to the corresponding acid, to that of resists formulated from novolac and the pure acid photoproduct.[128] The result was much higher dissolution rates for films in which the acid was photogenerated, leading to the conclusion that nitrogen produced as a byproduct of the photolysis of the DNQ, is a major contributor to photogenerated changes in dissolution rate in these systems. Presumably, the nitrogen gas evolved upon photolysis causes an increase in porosity within the resist that is known to have a profound effect on the dissolution rate of the films.[129] Further investigations are required to resolve this controversy.

Experimental Parameters Followed for Spin Casting the Photoresist

Before spin casting the wafer with resist, the wafers were baked on the hotplate at 115 ºC for 120 s to remove water from the surface. Air-based plasma was attempted to increase adhesion of the resist to substrate. Since this process did not help the resist adhesion, the substrate was coated with a pre-treatment chemical known as 80/20 primer. The 80/20 primer, purchased from MicroChem (Newton, MA), is based on a combination of 80% propylene glycol monomethyl ether acetate *(*PM Acetate) and 20% hexamethyldisilazane *(*HMDS). The primer was drop cast onto a silicon chip, which was subsequently spun cast at 3000 rpm for 30 s and baked (pre-bake step) on a hotplate at 115 ºC for 30 s. Before deposition of the resist layer, the chip was placed on a cold metallic surface to transfer the heat out of the silicon.

Photoresist SPR 220-7 (manufactured by Rohm and Haas Electronic Materials-Batch #: 0002206107) was diluted from 7% (w/v) to 1.5% using ethyl lactate, which is one of the main solvents for the SPR 220 series photoresists. Separately, the selenium nanowires were mixed into the ethyl lactate prior to the dilution of the photoresist. The SPR 220-1.5, prepared from this dilution process, was drop cast onto the silicon chip, spin cast at 4000 rpm for 60 s, and subsequently baked (pre-bake step as described in Section 2.5.4) on a hotplate at 115 ºC for 90 s. From Figure 2-23, the expected thickness of the resist spin cast at 4000 rpm is ~1.3 μm.

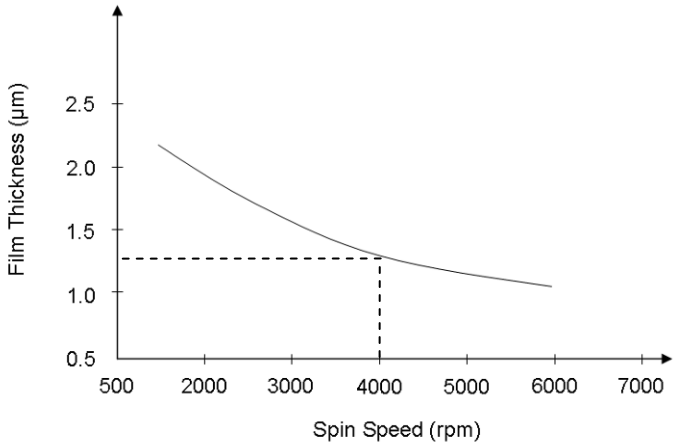


Figure 2-23: Spin speed curves provided by Rohm and Haas. Corporation for the SPR 220 photoresist series. [163] The vertical dashed line points to the spin speed used for the experiments with this resist and the horizontal line points to the resultant estimated film thickness of ~1.3 µm.

2.6.3 Irradiation of Photoresist via UV Light Source from an Optical Microscope

Placement of the Photomask in an Image-Forming Conjugate Plane

Microscope projection photolithography was pursued using, a Zeiss optical microscope (Axio Imager.M1m – model: 75160003). To use this technique for photolithography patterning, a photomask with the desired pattern must be placed in the light path of the microscope at the precise location of one of the image-forming conjugate planes as discussed in Section 2.4.1. Placement of the photomask in this location ensures the projection of a properly focused pattern onto the substrate. As no ray diagram of this microscope was available from Zeiss, due to proprietary concerns, a number of locations in the microscope were investigated as plausible image-forming conjugate planes for the placement of the photomask. Among the four image-forming conjugate sets (camera image plane, intermediate image plane, specimen plane, Köhler

diaphragm), the probable location of the intermediate image plane and field diaphragm were investigated for placement of the photomask. The photomasks were prepared as described in “Generating a MPP Photomask” of Section 2.6.3.

One of the first positions investigated for photomask placement was the filter cube of the optical microscope, an image of which can be seen in Figure 2-24. The location of filter cube with respect to the objective lenses and the light source of the microscope is illustrated in Figure 2-25. It is important to note that the microscope cross section shown in Figure 2-25 is not of the same model used in our experiments, and it only serves to depict the relative position of the filter cube in the optical microscope.

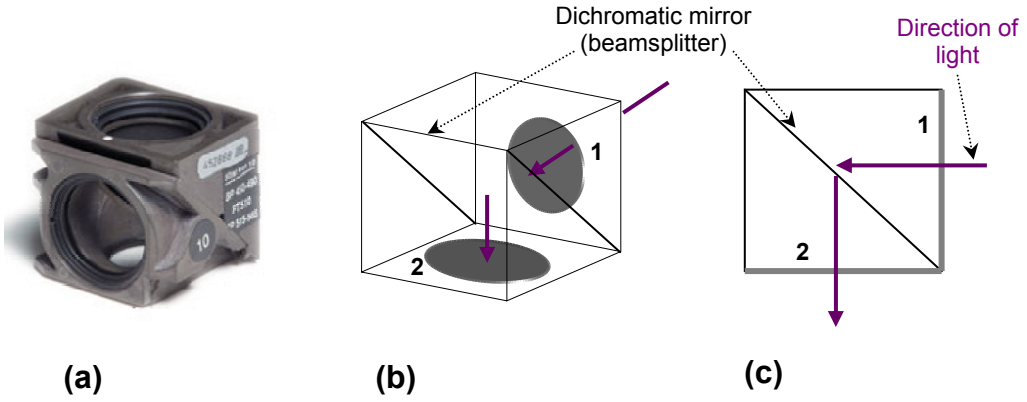


Figure 2-24: An image of the filter cube of a Zeiss microscope shown in (a).[157] *(Courtesy of Carl Zeiss Company).* **In (b) a three-dimensional view of this filter cube is shown pointing to the locations (1 and 2) at which the photomask was positioned for testing MPP. (c) A two-dimensional view of photomask placement in filter cube.**

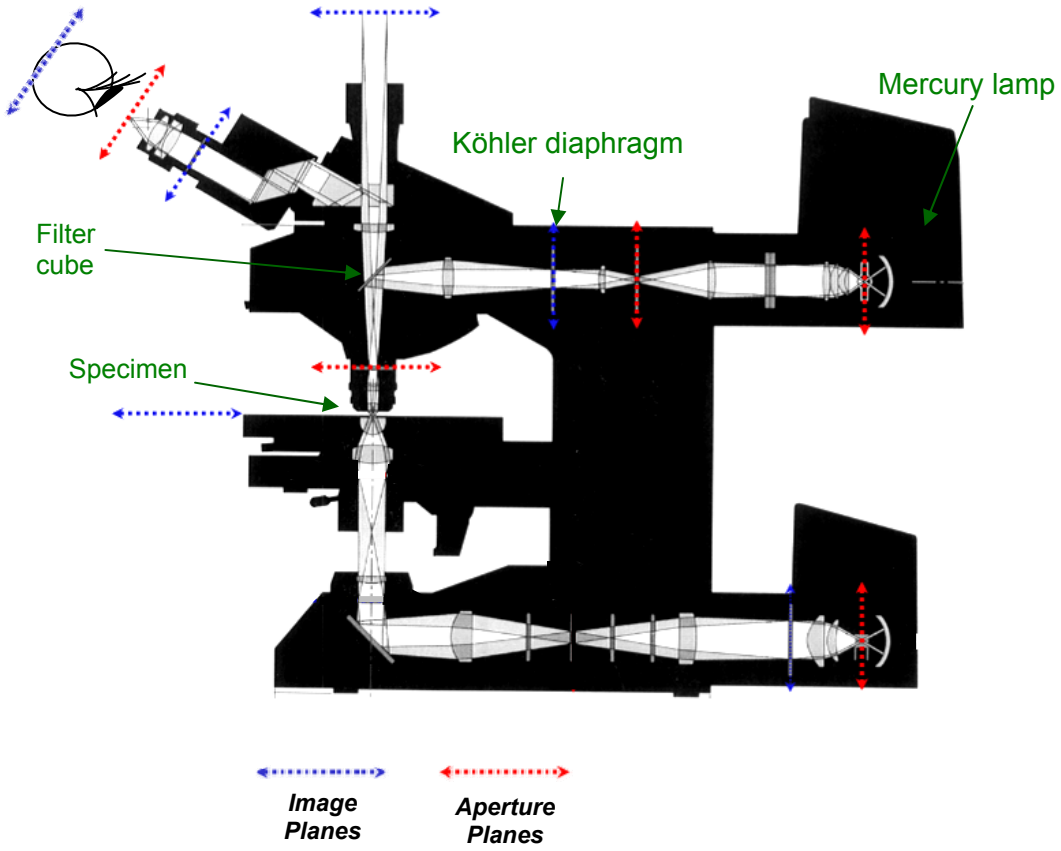


Figure 2-25: An image of the cross section of a Zeiss microscope (illustrated previously in Figure 2-9 depicting the two sets of conjugates planes), illustrating the relative placement of the filter cube with respect to other optical components in the microscope.[157] *(Courtesy of Carl Zeiss Company)*

As the photomask pattern was not in focus simultaneously to when the selenium nanowires on the silicon substrate were in focus, the filter cube location for the photomask was not investigated further. Another concern with this approach was the continual placement and removal of the photomask during an experiment. During this process one would locate nanowires on the substrate (while the pattern was removed) and expose the resist (with the pattern in place). This procedure would introduce a high chance of generating dust particle inside the optical components of the microscope.

Placement of the Photomask at the Köhler Diaphragm (Part I)

Aside from the intermediate image plane, another location in which the pattern could be placed at is the Köhler diaphragm (commonly referred to as field diaphragm). At the location of field diaphragm in the Zeiss microscope, there is a field aperture that can be fully opened or partially closed (forming an octagonal shape as the aperture is closed). Early exposure experiments were done utilizing this aperture as the projected pattern for selective exposure of an octagon pattern onto the resist containing nanowires on the wafer substrate. The objective lens reduces the size of the octagonal pattern of the aperture. The size reduction of this pattern was close to the power of the reduction lens (~90% reduction). The size scaling was not equivalent to the magnification of the lens most likely due to influence of other optical components in the light pathway. An example of this pattern projection is shown in

Figure 2-26 that demonstrates an octagonal pattern overlaid on a selenium nanowire using a 20x objective lens. To locate a nanowire, the stage is moved to position the substrate being viewed through the eyepiece. Note that a filter is placed in the light pathway to block 365 nm of light that the SPR-220 resist is sensitive to and avoid the exposure of the resist. Once the nanowire is located the photomask is placed in the light pathway and subsequently the filter is removed to expose the resist for a measured amount of time. Further details on the exposure can be found towards the end of this section. It is important to note that this exposure used the smallest aperture size of ~3 mm. Exact size of the aperture is unknown as the diaphragm is mounted inside the microscope, making it inaccessible.

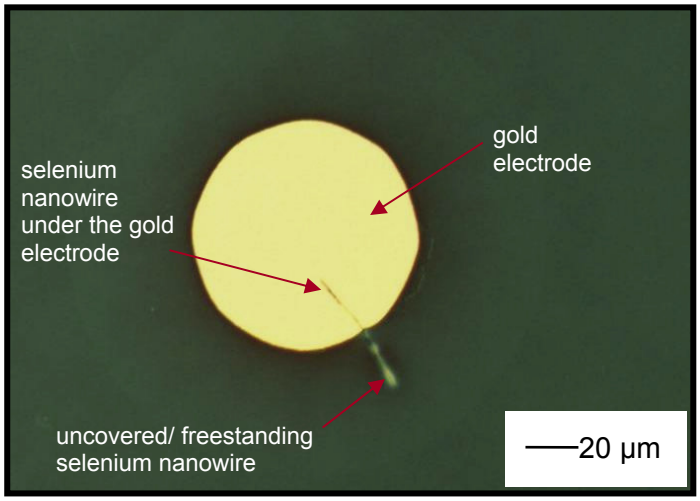


Figure 2-26: An image taken by bright-field optical microscopy demonstrating patterning of an octagon of gold onto selenium nanowires via the MPP technique. The photomask was the projected pattern of ~3 mm diameter field aperture using the 5x objective lens with NA of 0.13.

The shape and dimension of the exposed pattern needs to be such that electrical probes (using a probe station, see Section 4.2) can be placed on the metal contact pads or alternatively metal wires can be bonded to them (using a wire bonder, see Section 4.2). These electrical connections are necessary for performing electrical measurements with ease and without damaging the nanowires. Hence, a more elongated pattern is desired so that it has a minimum feature size more comparable with the nanowire, with the opposite end of a sufficient size to be compatible with probes of either a probe station or a wire bonder for making the electrical connection. The ultimate goal is to develop simple techniques for the characterization of the electrical properties of selenium nanowires.

We developed an alternate MPP process in order to achieve the desired pattern and thus electric contact with the nanowires. Using the field aperture, the MPP process was performed in two steps (referred to as double exposure in this thesis). The result is the smallest possible aperture projection was overlaid on the nanowire with a slightly larger second aperture setting overlapping the first exposed region (Figure 2-27). The placement for projection of the second exposure step was experimentally optimized to ensure sufficient overlap of the two exposed patterns on the resist, as there is no physically visible feature to assist in overlapping the second with the first exposed region. The halo region at the junction of the two octagonal patterns (Figure 2-28) is most likely due to overexposure of these regions from scattered UV light.

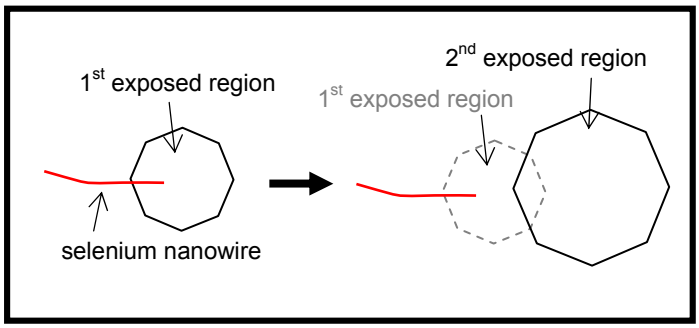


Figure 2-27: A schematic depicting the two separate exposures performed to produce the pattern shown in Figure 2-28.

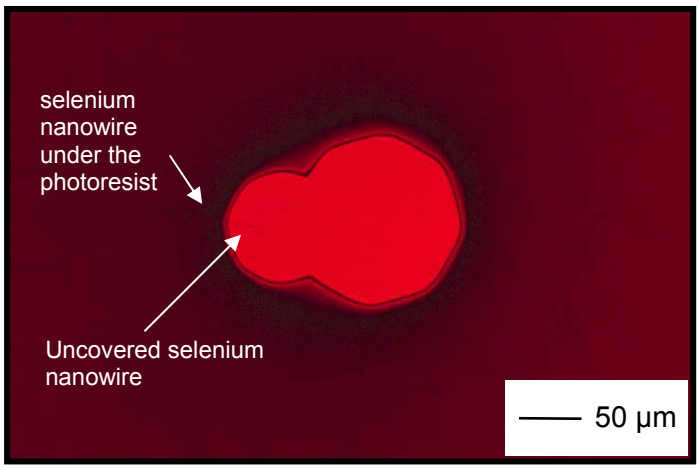


Figure 2-28: Two separate exposure steps were performed using the 5x objective lens (with NA of 0.13) and the ~3 mm diameter field aperture (overlaid pattern on nanowire) and one slightly larger (overlaid pattern on the previously exposed region). This bright-field optical image was taken after developing the exposed photoresist using the red filter to avoid UV exposure of other parts of resist before the metal deposition step.

Placement of the Photomask at the Köhler Diaphragm (Part II): Modification of the Optical Microscope and Design of a Projection Mask Holder

The double exposure of resist using the field aperture is not accurate and, therefore, a far from ideal approach to MPP patterning. To improve upon this demonstration a mask holder was designed to be inserted in the light path at the location of the image-forming conjugate plane of the Köhler diaphragm. An image of an early design of the mask holder can be seen in Figure 2-29. This mask holder can hold a photomask (see 'generating a MPP photomask' in the next subsection) containing a desired pattern. Various designs can be generated for the photomasks so that the shape and size of such patterns is more compatible with the nanowires for overlaying metal contacts. Through numerous experiments (see 'Focusing Tests Using the Mask Holder' in Section 2.6.3), the simple early design of the mask holder evolved into an improved

design. As seen in Figure 2-30 and Figure 2-31, the modified mask holder was inserted into the microscope at the position labelled ‘A’. Pictures of an advanced version of the mask holder and its position within the light path of the microscope are shown in Figure 2-32, Figure 2-33 and Figure 2-34.

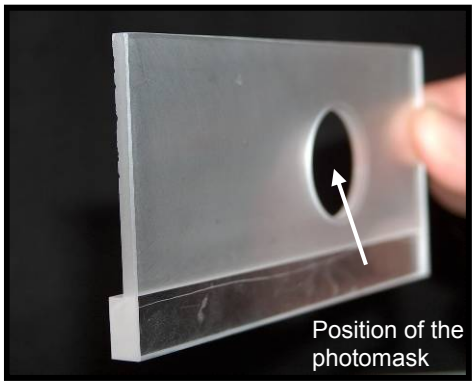


Figure 2-29: An early design of the mask holder for positioning a projection mask within the light path of an optical microscope.

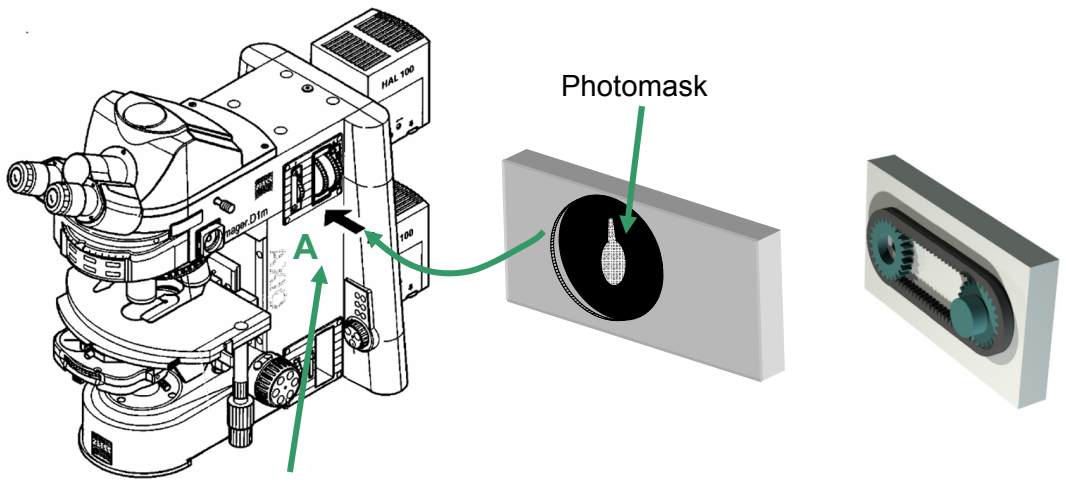


Figure 2-30: A schematic representation of the Zeiss microscope and two versions of the mask holder shown in "b" and "c". Part labelled as "b" is a depiction of an early design of the mask holder, and part labelled as "c" is a newer version, which is detailed in Figure 2-31 and Figure 2-32.[118] *(Courtesy of Carl Zeiss Company)*

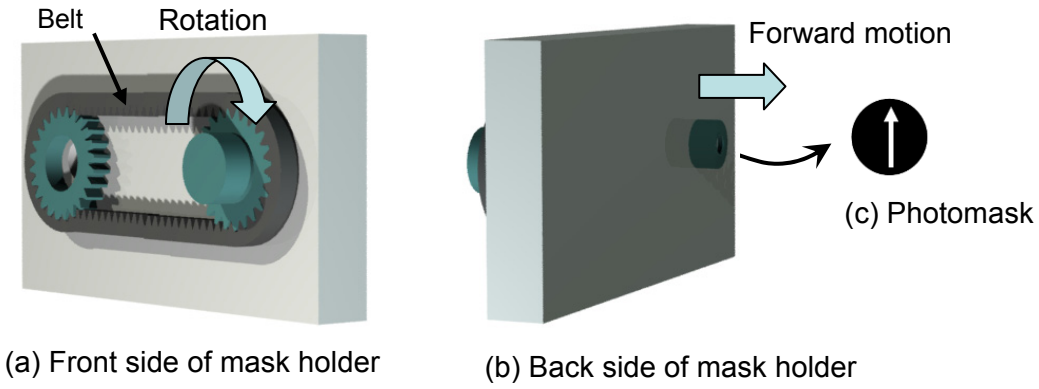


Figure 2-31: A schematic of the (a) front and (b) back of the latest version of the mask holder, as well as the (c) position of the photomask. The blue arrow in (a) indicates rotation of wheel which in turn moves the belt that rotates the screw at the end of which is mounted the photomask as shown in (b). As shown, the photomask moves towards the image-forming conjugate plane of Köhler diaphragm by rotation of the wheel.

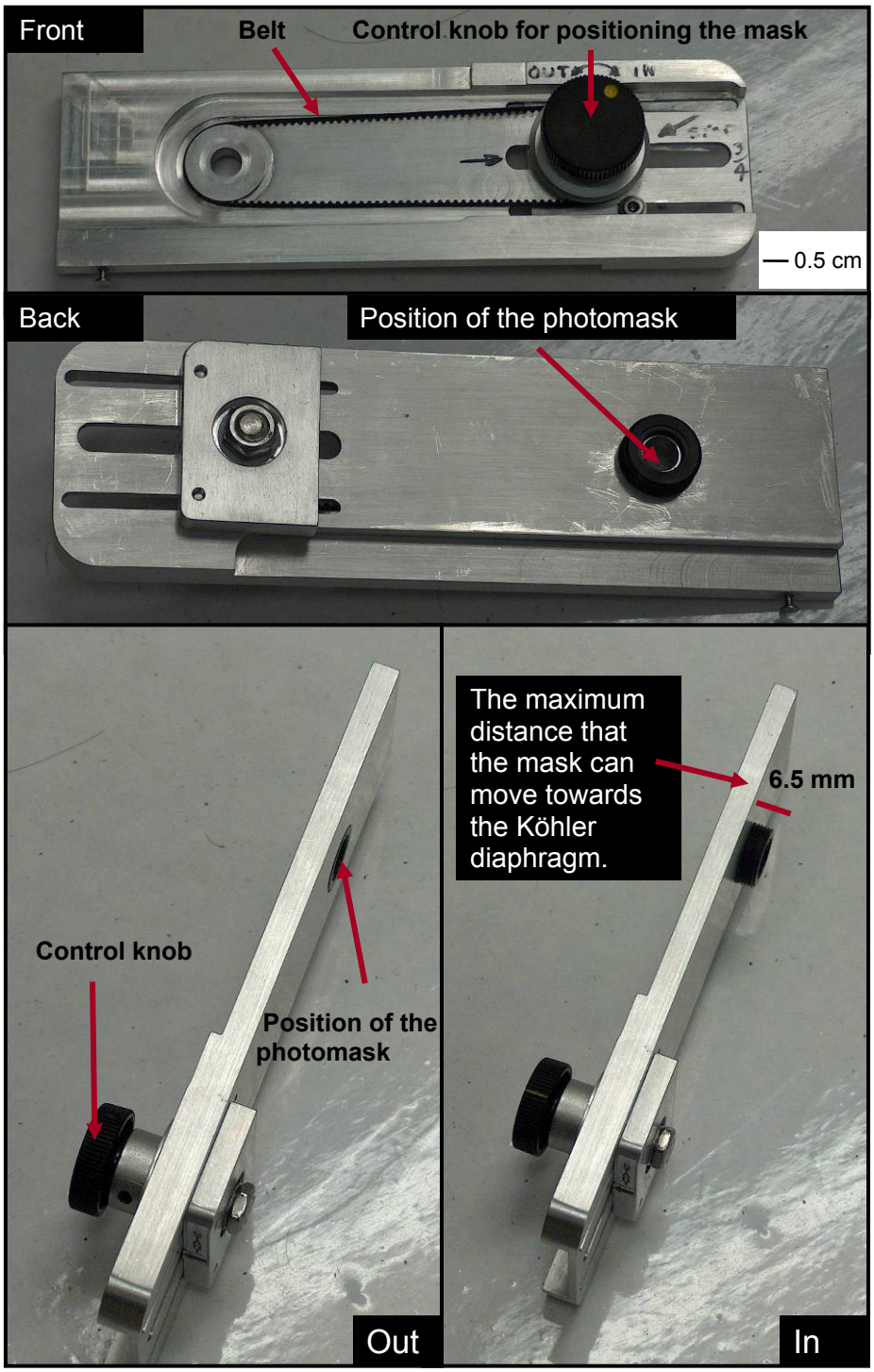


Figure 2-32: Pictures of the front and back of the mask holder (top) and side view of the holder to show the 'in' and 'out' positions of the photomask achieved by rotating the wheel.

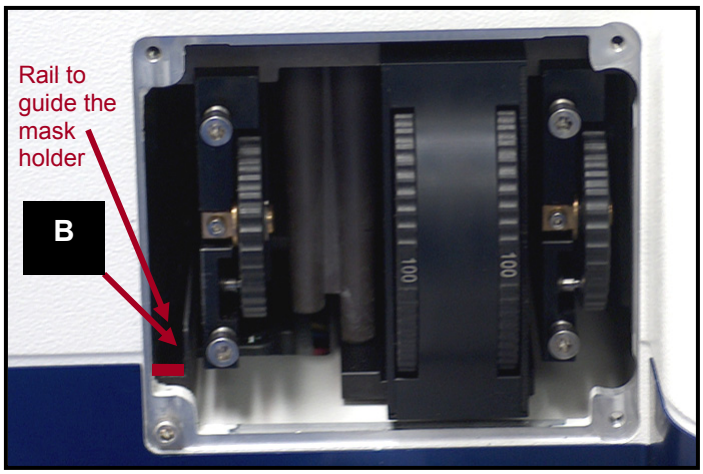


Figure 2-33: Detailed view of "A" from Figure 2-30. Slot labelled 'B' is the position where the mask holder is mounted within the light path of the optical microscope. The width of this passage is 8 mm, as indicated by the red line.

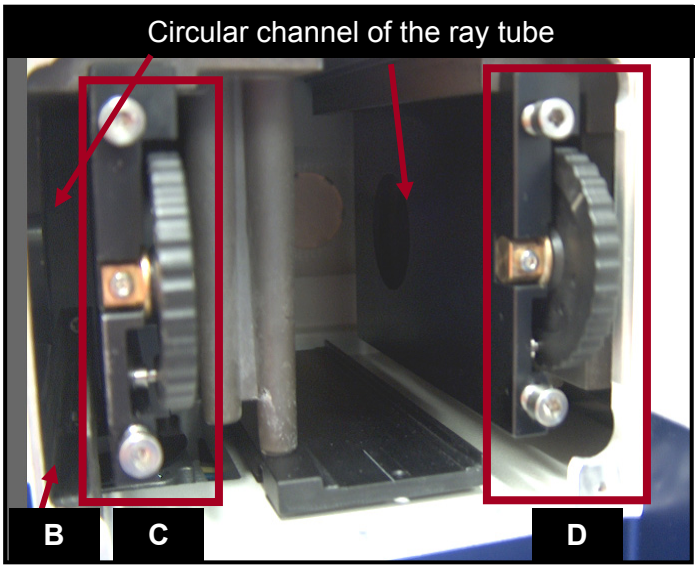


Figure 2-34: The mask holder needs to be positioned in the rail "B" installed in the small passage on the left of component labelled "C". Component "D", identical to "C", is shown to provide a clearer image of similar components inside the microscope.

A rail was place within the microscope (Figure 2-33) to guide in the mask holder smoothly and to assure that the motorized z-drive for the stage is not damaged. This rail is also to guide the travel of the mask holder in and out of the microscope. Once the mask-holder is inserted into the microscope, the control knob of the mask holder (shown in Figure 2-32) can be rotated to move the photomask 'in' and towards the Köhler diaphragm inside the ray tube (see Figure 2-34). By the reverse process, the mask can be taken out of the microscope and switched with a different one. To overlay a pattern onto the selenium nanowires there are a few important factors to pay attention to. These factors include the location of the mask holder and the substrate, as well as the magnification of the objective lens used as shown in Figure 2-35.

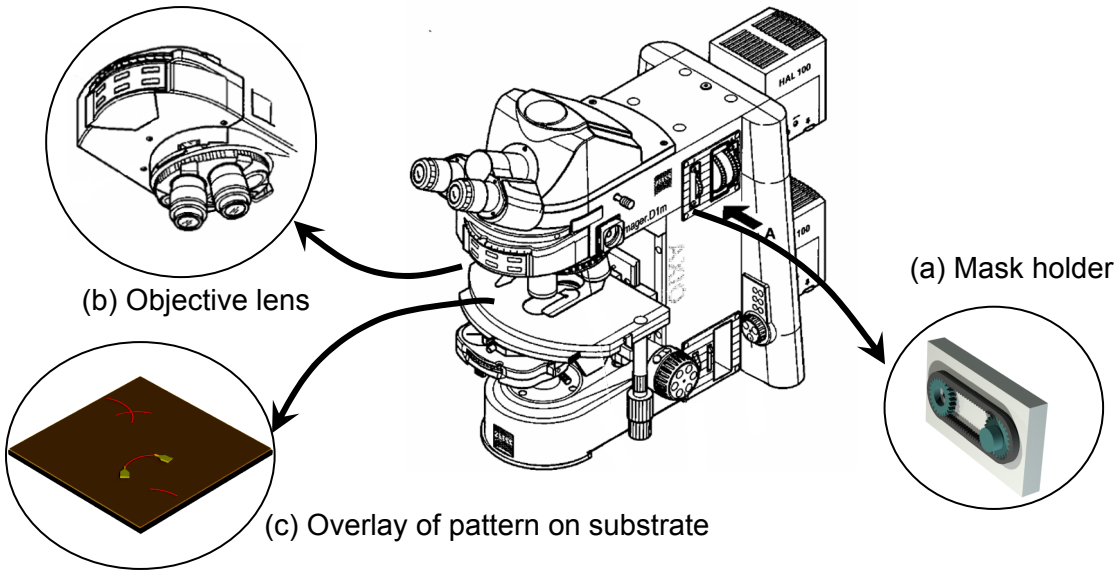


Figure 2-35: Overlay of a photomask on resist coated nanowires on a substrate using a given objective lens.

Generating a MPP Photomask

Patterns on photomasks were generated using Clewin, a vector-based drawing program. These patterns were printed by high-resolution printers at CAD/Art Services Incorporated (Bandon, OR).[177] The patterns were printed on 0.007-inch thick mylar with a resolution of 10,000 dots per inch to produce features as small as 25 μm. Examples of the diverse patterns that can be designed are shown in Figure 2-36.

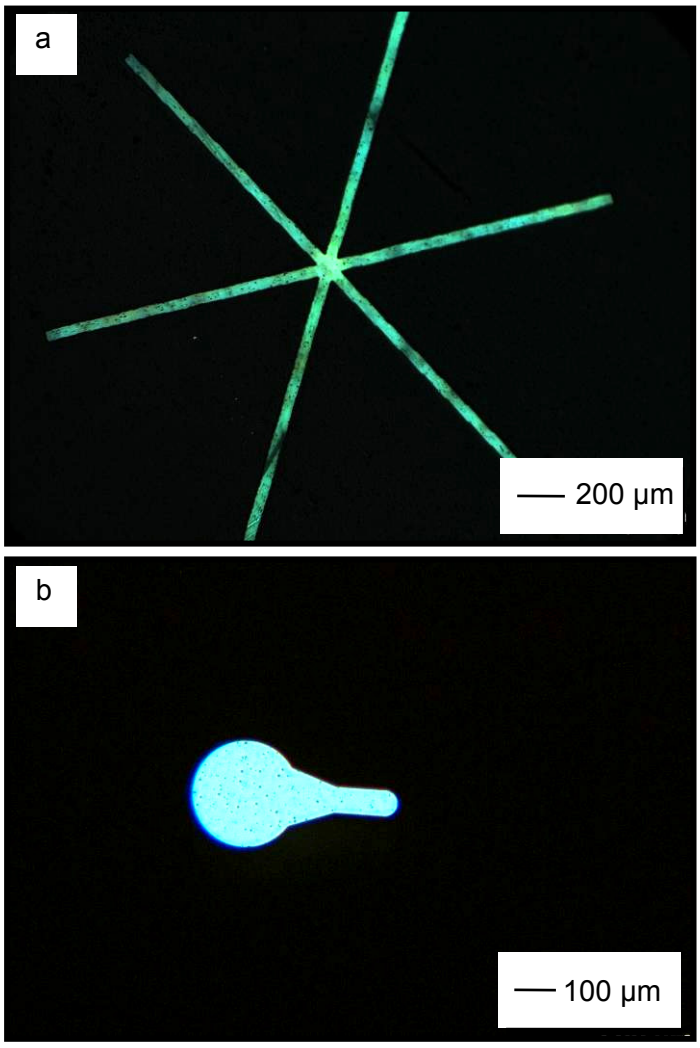


Figure 2-36: Two patterns used in MPP, which are discussed in more detail towards the end of this section: a) This pattern was used to optimize the focus of the mask; b) this pattern was used to compare the size reduction and resolution of different objective lenses.

Wu *et al.* generated patterns down to 8 μm.[178] In this work, however, a larger scale was chosen for demonstration purposes.

Generating a Photomask Made from Glass Slides

During the MPP experiments, a number of photomasks were used to test the focus of the resulting pattern as a function of objective lens magnification and numerical aperture and the movement of photomask along the ray tube. During these experiments it was noted that the photomasks would deform after prolonged exposure to the source (Figure 2-37). The most likely reason for this distortion is the heat from the UV lamp. In order to overcome the deformation of the photomask, patterns were generated on round glass slides by the process described below. These glass slides are more robust than the mylar sheets used in Figure 2-36.

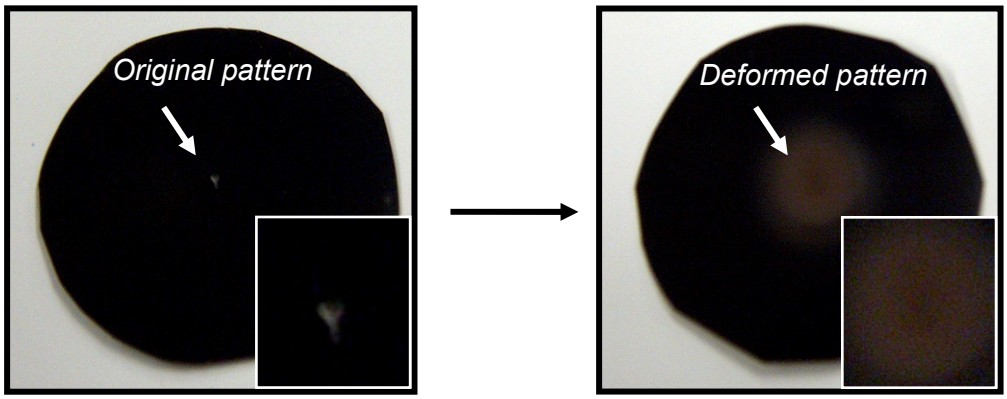


Figure 2-37: An image of a photomask before and after prolonged (~30 min) exposure of UV radiation. The image on the right shows a deformed mask due to excess heating by the UV lamp. Note that after roughly ten exposures (~15-30 s/exposure) this deformation is not seen. The insets show higher magnification images of the center of the photomask before and after exposure.

The glass slides (cover slips purchased from VWR International, 25 mm circle No. 2 – Part #: 48382085), must be cleaned prior to use as substrates to form the MPP masks. First, these glass substrates were washed with soap and water, washed with acetone, rinsed with water and dried under a stream of nitrogen gas. A piranha solution, a 7:2 (v/v) mixture of sulfuric acid (purchased from J. T. Baker, Lot#: B41043) and 30% hydrogen peroxide (purchased from Caledon laboratory chemicals, Lot#: 4060-1) respectively, was prepared for immersion of the glass substrates. The pre-cleaned and dried glass slides were soaked in the piranha solution for 20 min. (***Caution:*** *This mixture reacts violently with organic material and should be handled with care.)* Afterwards, the substrates were rinsed with 18 MΩ water and dried under a stream of pressurized filtered nitrogen gas. These steps are designed to remove organic molecules from the surface of the glass slides.

A procedure to make MPP masks mounted on glass slides is outlined in Figure 2-38. First, a layer of metal was deposited onto the clean glass substrates to create a blank photomask. The first metal deposited was 5 nm of chromium, as an adhesion layer, upon which was deposited 150 nm of gold. Refer to Appendix B for a procedure for metal deposition. A layer of SPR 220-1.5 photoresist was spin cast onto the gold covered substrate using the procedure as described in Section 2.6.2. The next step was to expose the photoresist by using the polyester mylar patterns in contact with the resist. In this step, collimated UV light (wavelength of 365 nm) was used to expose the photoresist. The underlying gold layer is exposed after a developing step (described in Section 2.6.4) to remove the exposed regions of photoresist. To create a MPP mask, the substrate is then placed in a Cr/Au etchant to remove the exposed gold and chromium and create a region of exposed glass substrate.

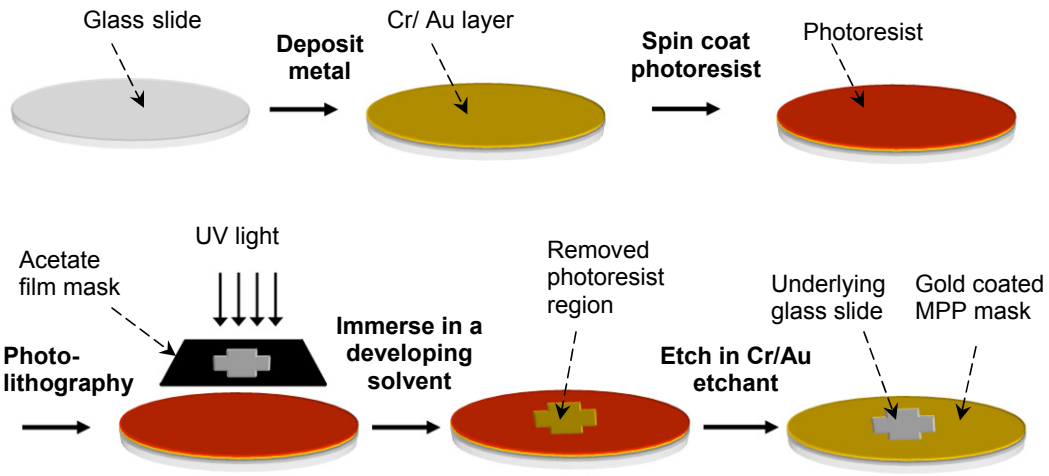


Figure 2-38: A schematic of the fabrication process to make gold masks on round glass slides. A cleaned glass slide is used for Cr/Au deposition followed by spin casting of photoresist. After the contact photolithography step the substrate is developed in a developing solution to uncover the underlying gold layer. The exposed gold layer is etched using a Cr/Au etchant to create a transparent region and to produce the gold masks.

In Figure 2-39, optical images of two gold masks on glass slides depict some of the patterns produced using the described fabrication steps.

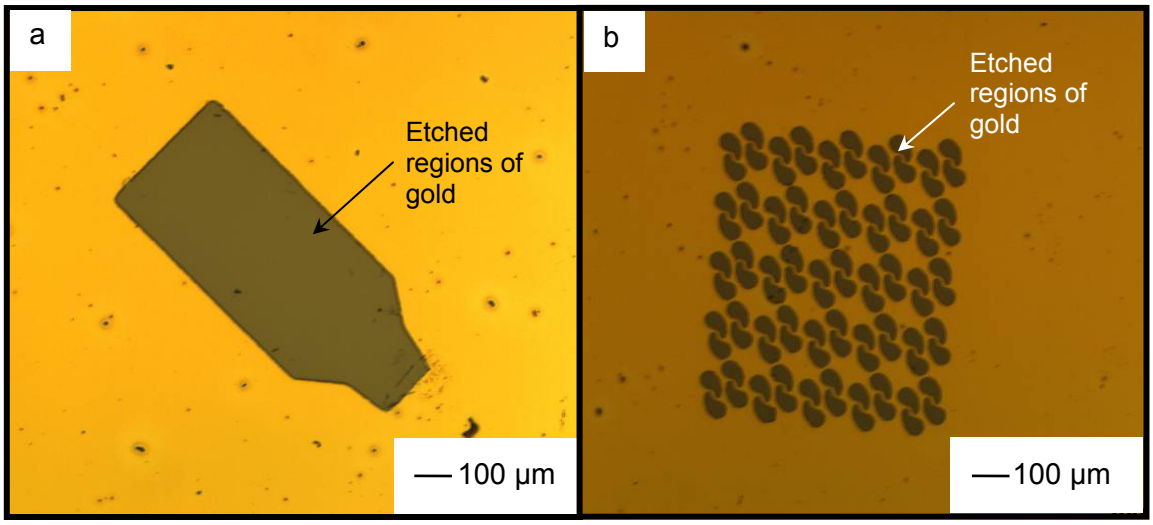


Figure 2-39: Images of two gold-coated, glass MPP photomasks acquired by bright-field optical microscopy depicting the etched and un-etched regions of gold film on the glass slide forming a pattern to allow selective UV exposure.

Focusing Tests Using the Mask Holder

As described previously for MPP of a pattern onto the sample, both the substrate and photomask need to be simultaneously in focus. A number of modifications were done to the mask holder to achieve this requirement. The images shown in Figure 2-40 (from a→f) represent the difference in focus of the pattern and substrate as the pattern is moving towards the field diaphragm by the rotation of the wheel. These images were taken using a projected star pattern depicted in Figure 2-36-a. Due to space limitations within the microscope, the latest modification of the mask holder designed was only capable of reaching 6.5 mm towards the field diaphragm instead of the 8 mm required to properly position the photomask. The distance of 8 mm that the photomask needs to reach was measured from component D as labelled in Figure 2-34. A number of other designs for the mask holder were taken in consideration as well, with use of telescopic or conical spring components, which will not be discussed in this thesis.

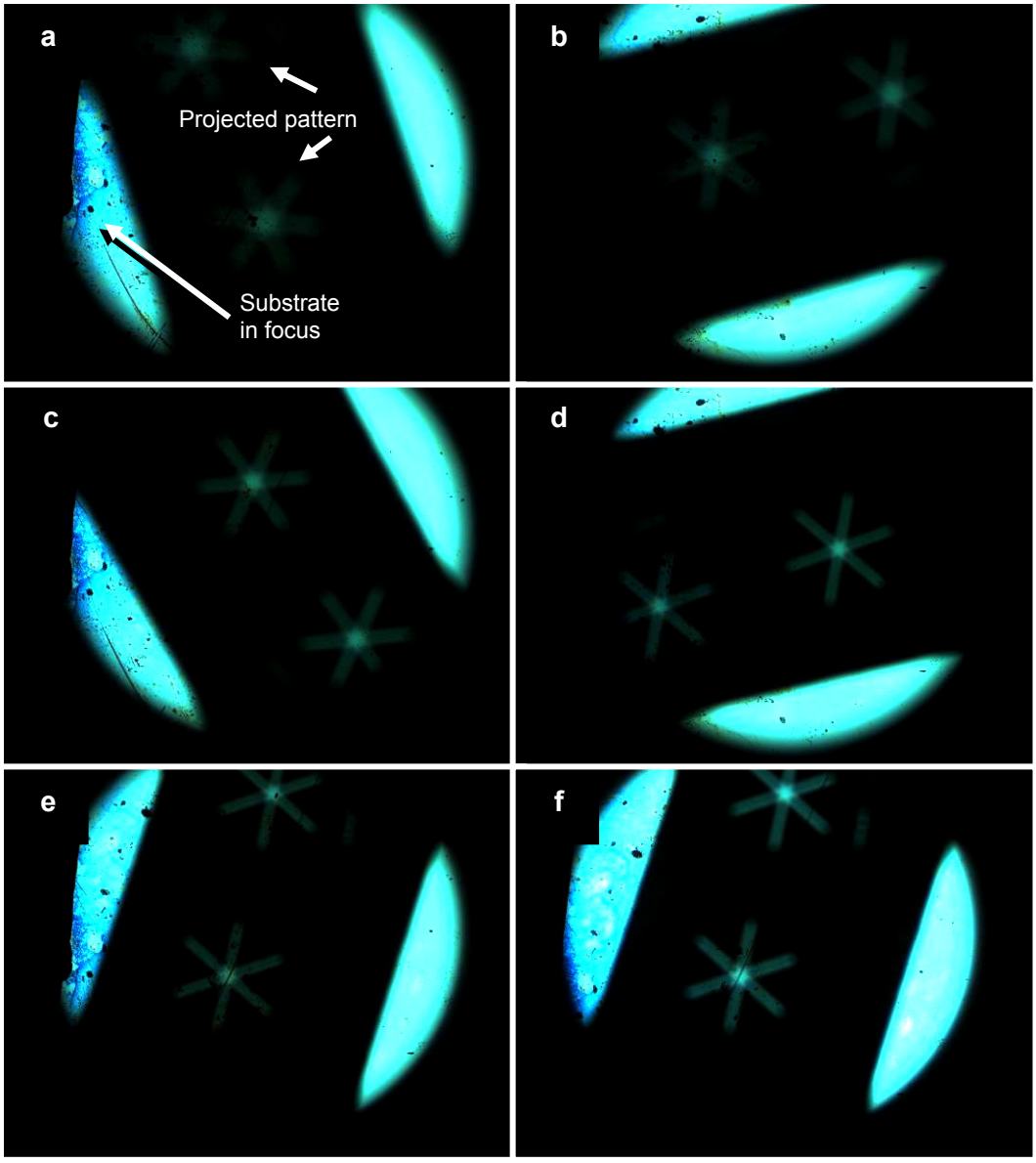


Figure 2-40: Progressive focusing of the photomask within the mask holder as the wheel is turned to approach the conjugate plane. The improvement in the focus can be seen from (a) through (f) as the mask moves closer to the conjugate image plane. Comparison of image (f) with that in Figure 2-36 is indicative that the conjugate image plane has not yet been reached. The lateral distance within the ray tube of the optical microscope that the photomask has moved from (a) to (f) is 6.5 mm. Note that there is no scale bar for these images since regardless of the magnification of the lens used, the focusing of the photomask pattern will not change.

Exposure Parameters Using MPP

The MPP exposures were performed using a mercury arc lamp. This choice of exposure source was based on the sensitivity of SPR 220 photoresist series to the i-line region (365 nm) of electromagnetic spectrum. The intensity of mercury lamp was adjusted and measured with a laser power meter (model #: TPM-300, Gentec company) with a photosensitive plate of ~0.3 cm^2. A number of neutral density filters were initially used to tune the intensity of lamp, but as they proved to not be necessary, they were not used further in the experiments. As indicated by the manufacturer of SRR-220, for a thickness of 1.2 μm, the required i-line exposure is 160 mJ/cm^2. Based on the relationship in Equation 2-5, the time required for exposure was calculated and further optimized in a number of experiments. Patterns on photomasks, as previously mentioned, were generated using the Clewin drawing program and then printed by CAD/Art Services Incorporated.

$$\text{Exposure time} = \frac{0.3\ cm^2 \times 160\ mJ/cm^2}{\text{Intensity of mercury lamp (mJ/s)}} \qquad \textbf{Equation 2-5}$$

The mercury lamp intensity was adjusted to 8 mJ/s, which required at least 6 s of exposure per pattern. Optical images in Figure 2-41 depict projected patterns taken after the developing step of an underexposed and a properly exposed sample with exposure of 6 s and 15 s, respectively. Possible reasons for the need to increase the exposure time from 6 to 15 s could be the fact that mylar of the photomask absorbs some UV light and the power meter may not be measuring the intensity of the mercury lamp as accurately as required for this experiment.

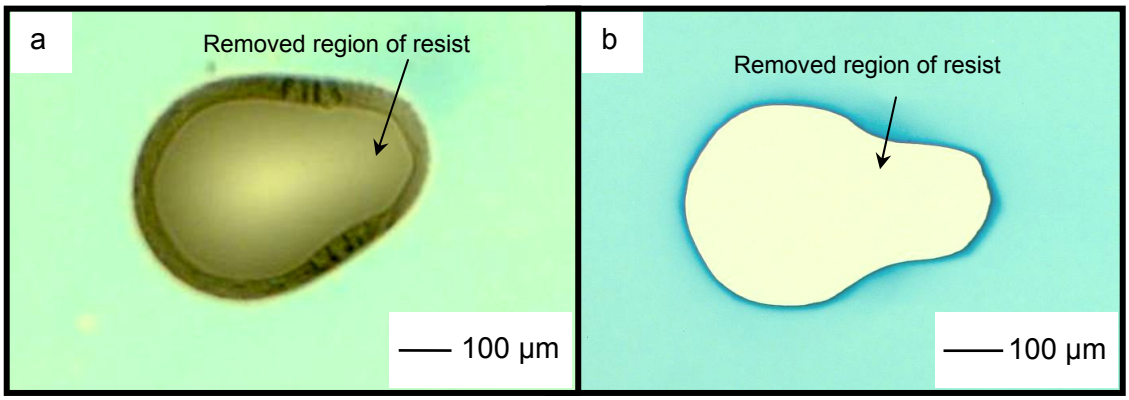


Figure 2-41: Images acquired by bright-field optical microscopy using a 5x objective lens with NA of 0.13. (a) An under-exposed (b) properly exposed patterns taken after developing using a projection of the pattern shown in Figure 2-36-b.

2.6.4 Developing of Photoresist

After exposure, the substrates were baked at 115 ºC for 90 s. The substrate, after cooling, was developed in MFP-319 solvent (manufactured by Rohm and Hass Electronic Materials – Batch #: 0002177628) for 45 s. The developing time of the substrate was optimized by immersion of the substrate in the developing solvent for 30 to 90 s. The shorter developing time resulted in under-developed samples and the longer developing time resulted in severely over-developed substrates as depicted in Figure 2-17 from Section 2.5.7. The developing process was terminated by thoroughly rinsing the substrate with de-ionized water for 2 min and then dried under a stream of pressurized, filtered air.

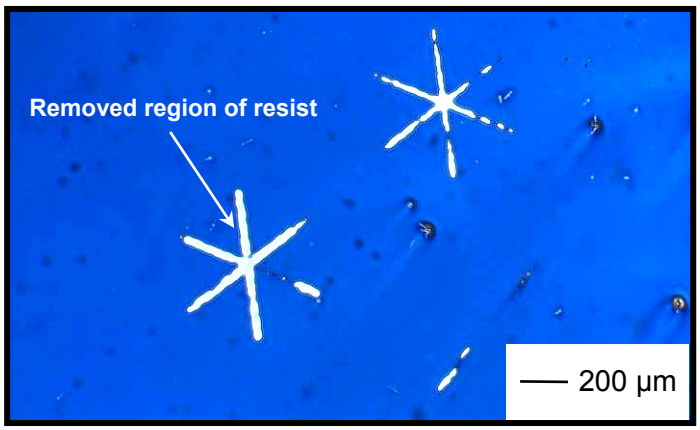


Figure 2-42: An image acquired by bright-field optical microscopy of the projected pattern using a photomask with the pattern shown in Figure 2-36-a using a 10x objective lens with NA of 0.25, after the developing process.

Figures on the next couple of pages illustrate a number of selected images taken after the developing step using various objective lenses and photomask patterns as indicated by their captions. As the photomask could not reach the image-forming conjugate plane of the Köhler diaphragm due to a limitation of the mask holder design and limited space to work with in the optical microscope the images shown are not focused projections of the photomask patterns.

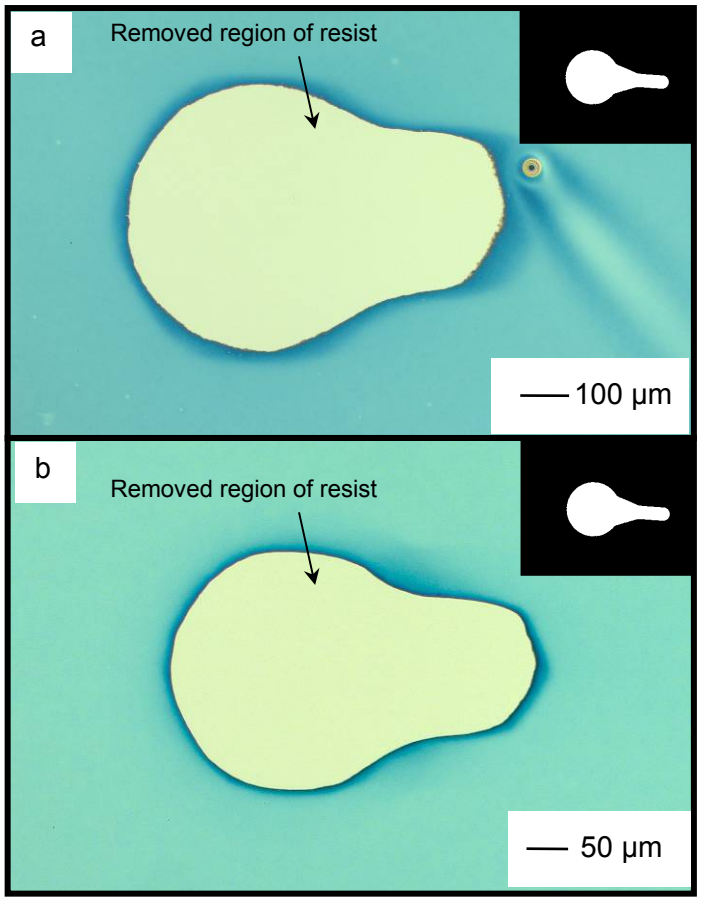


Figure 2-43: Images acquired by bright-field optical microscopy of the projected pattern using the photomask pattern shown in Figure 2-36-b with a 5x objective lens with NA of 0.13 (shown in a) and a 10x objective lens with NA of 0.25 (shown in b), after developing process. The insets depict the drawing of the anticipated patterns. The out of focus projection is due to the limitation of the mask holder in reaching the exact location of the image-forming conjugate plane of Köhler diaphragm. It is worth noting that the projected pattern using the 10x objective lens is roughly half the size of that using the 5x objective lens.

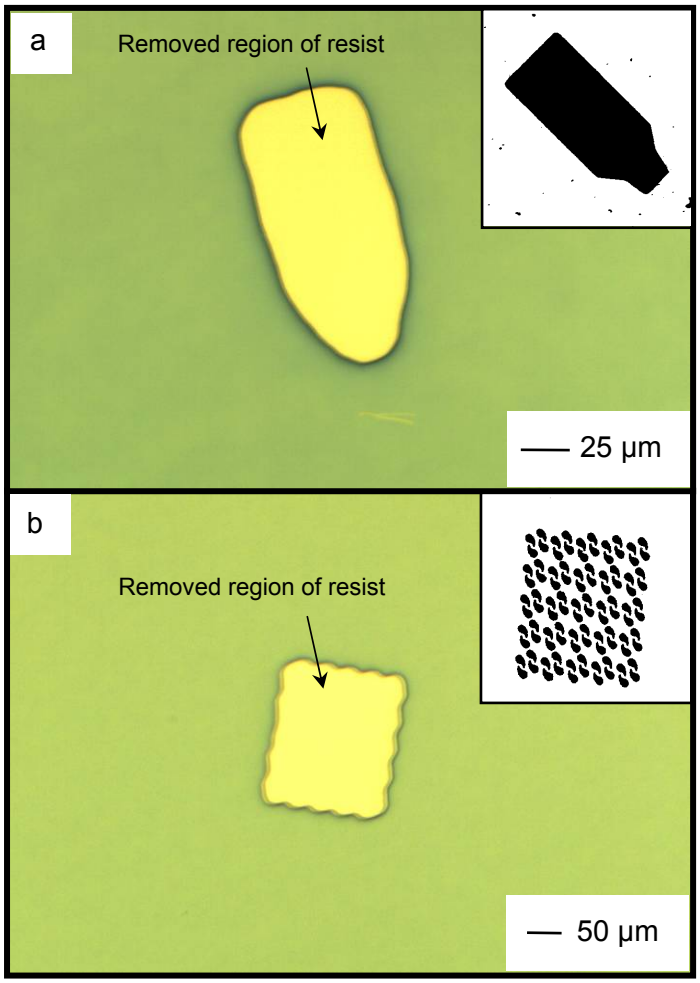


Figure 2-44: Bright-field optical images of the projected pattern (using 5x objective lens with NA of 0.13 for projection) and gold photomasks with pattern shown in Figure 2-39 (a) and (b), respectively, after developing process. The insets depict the drawing of the anticipated patterns. It is important to note that the unfocused projection is far more exaggerated in part (b) of this figure, as the smallest feature in the photomask pattern was much smaller than that of the pattern in (a).

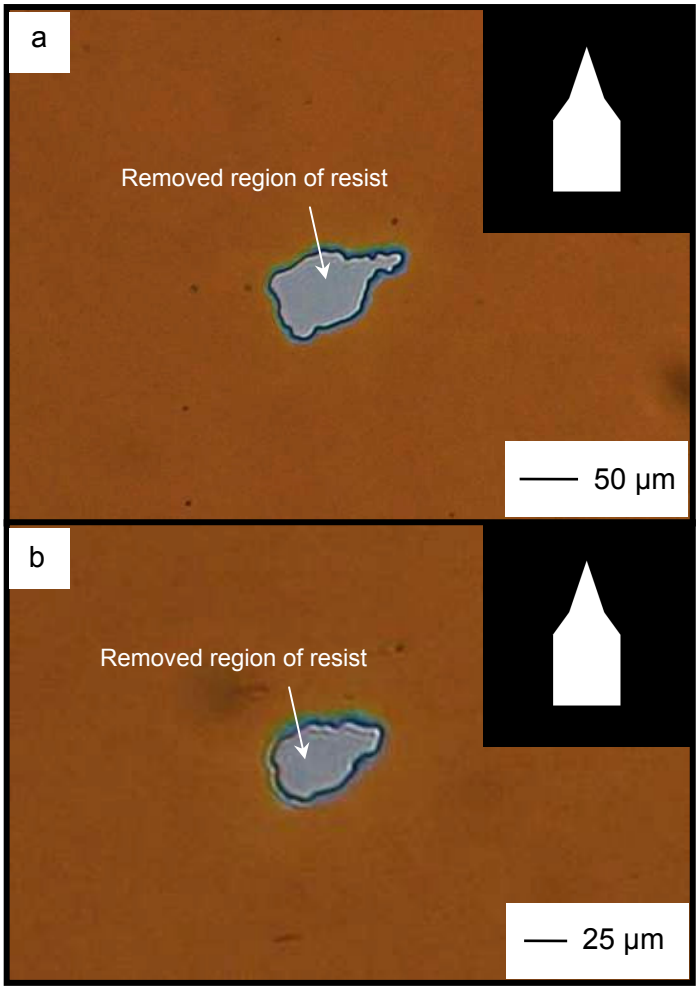


Figure 2-45: Bright-field optical images of the projected pattern testing the smallest size that could be achieved using a 10x objective lens with NA of 0.25 in (a) and a 20x objective lens with NA of 0.50 in (b) given the limitation of the current mask holder.

2.6.5 Metal Deposition on Developed Photoresist Coated Silicon Wafers

In order to form electric contacts on selenium nanowires, metal needs to be deposited on developed substrate. The developed substrate was positioned and fixed on the holder of the Lesker thermal evaporator. More details on the operation of this instrument can be found in Appendix B. The first metal layer deposited was 5 nm of chromium (99.95.% purity, purchased from Kurt J. Lesker Company), to act as an adhesion layer, followed by 100 nm of gold (99.999 % purity, purchased from Kurt J. Lesker Company).

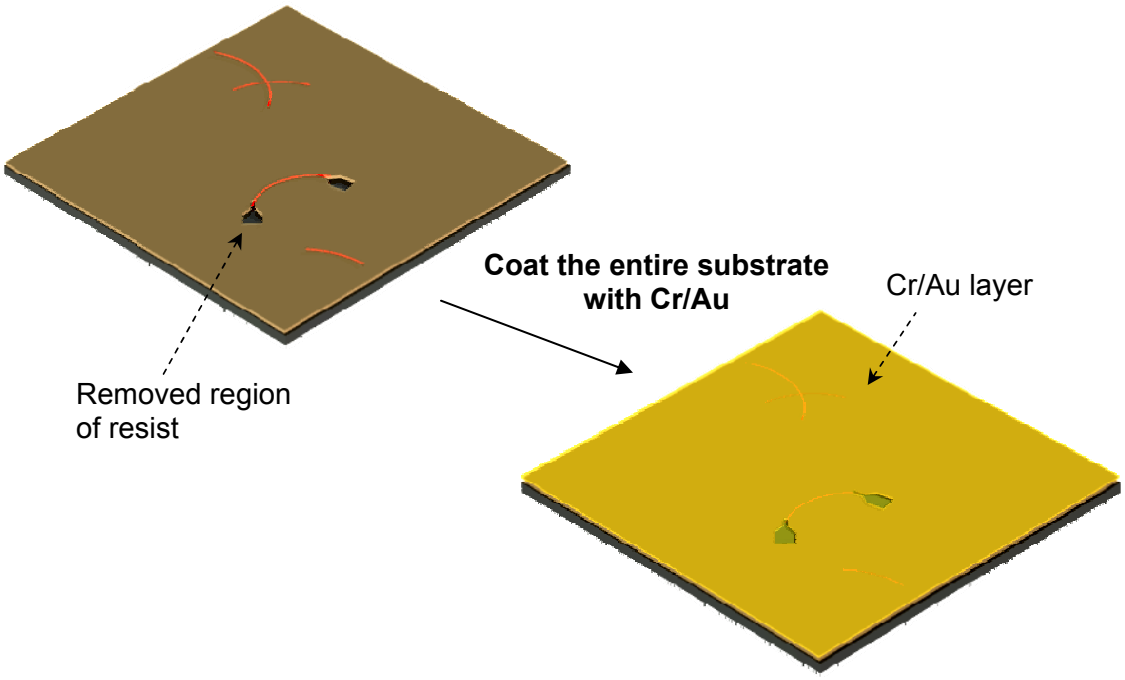


Figure 2-46: Metal deposition on a developed silicon wafer substrate.

2.6.6 Lift-Off of Metal-Covered Photoresist

After metal deposition, the substrate was immersed in a solvent to remove the left over resist under the gold layer by penetration of the solvent through the side walls of the exposed and removed resist. Ideally, the results would match the depiction in the schematic shown in Figure 2-47.

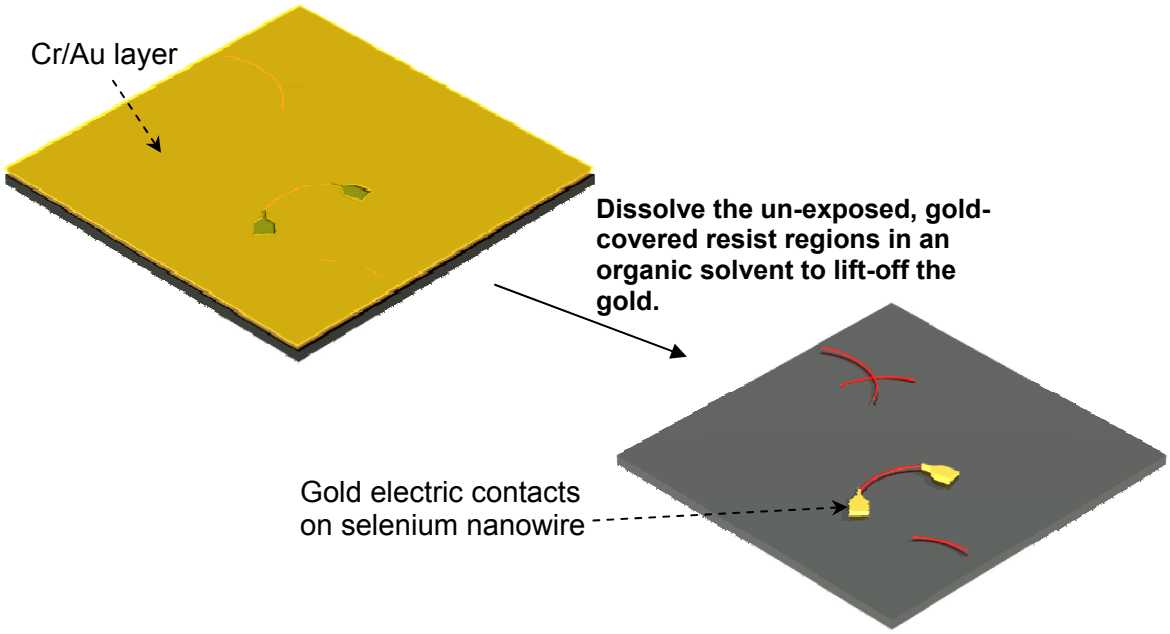


Figure 2-47: Lift-off step after metal deposition on the developed silicon wafer substrate.

In this experiment acetone, heated to ~50 ºC, was used as the solvent for removal of SPR 220. As mentioned before, it is often recommended by the manufacturer of the resist companies to use heat and/or sonication techniques to promote fracture of the metal layer. Given that the goal of this project is to overlay metal contacts on selenium nanowires and having knowledge of the fact that selenium nanowires break due to sonication, sonicating the substrate is not a viable step to be taken for removal of the gold layer. Figure 2-48-a depicts the optical image of a non-sonicated sample that

was left in 50 ºC overnight. Note that in this figure the metal that was deposited on the photoresist is detached from the surface (slightly wrinkled regions), but remain connected to the pattern of gold that is supposed to remain on the surface. Alternatively, Figure 2-48-b represents a sonicated sample in which all the unwanted metal layer has been removed from the surface along with the nanowire.

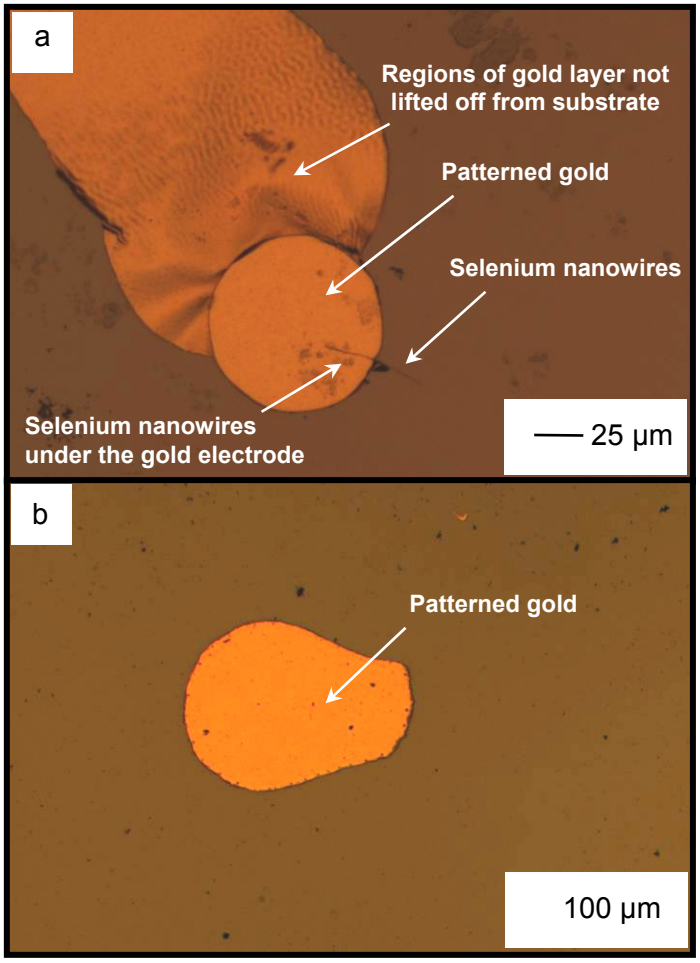


Figure 2-48: Optical images of the projected pattern testing the smallest size that could be achieved given the limitation of the current photomask using a 20x objective lens with NA of 0.50.

Since positioning the photomask at the exact location of the conjugate plane using the mask holder was not successful, overlay of metal contacts on selenium nanowires were done using electron-beam lithography techniques and will be described in the next chapter. The effort put towards overcoming the challenge of gold layer lift-off without the breakage of selenium nanowires will also be addressed in Chapter 3.

2.7 Conclusions and Discussion

The experiments performed using the microscope projection photolithography technique focused on a number of factors necessary to produce projected patterns with the desired focus and resolution including: i) the position of photomask; ii) the position of the substrate; iii) focal length of objective lens; and iv) alignment of the UV lamp. With the use of a mask holder similar to the one presented in this thesis, one could potentially position a photomask precisely at the image conjugate plane of the Köhler diaphragm. However, due to machining limitations, the latest version of the mask holder design was only capable of reaching 6.5 mm instead of the 8 mm required to position the photomask at the desired position. A number of other designs were taken into consideration as well, such as the use of telescopic or conical spring components, which were not discussed in this thesis.

Data showing the result of exposure with the photomask not precisely located at the conjugate image plane were provided in this chapter. In addition, the resist covered substrate needs to be positioned precisely at the specimen plane. To produce a distinct, well-aligned pattern requires the precise positioning of both photomask and the substrate. Making use of objective lenses with a higher depth of focus provides more leniency for the experimentalist in terms of substrate positioning. However, the depth of

focus of a lens is inversely proportional to the square of the *NA* and *NA* is directly proportional to resolution. The *NA* choice of an objective lens is a balance between needs for higher resolution and large depth of field.

There are a number of advantages using the MPP technique for pattern projection. One advantage with this set-up is that, due to the simultaneous viewing of mask and substrate, the alignment and overlay of the pattern onto a nanowire can be done at the time of exposure. Wafer mask aligners, used in lithography, lack the optical resolution to align to nanowires and certainly cannot be used to apply contacts to individually chosen single nanowires which are randomly arranged. Hence, using MPP, unlike all other lithography techniques, there is no requirement for prior alignment of the substrate and a mask, which ultimately means fewer steps in the required processing. Also, there is no need for a substrate-specific mask as the substrate with randomly orientated nanowires can be moved on the stage. Another advantage of this system is that a filter can be placed in the path of light to prevent substrate exposure as the experimentalist is searching for a given nanowire on which to overlay the pattern.

CHAPTER 3: DIRECTED ELECTRON-BEAM LITHOGRAPHY ON NANOWIRES

Research on high resolution lithography has been an active pursuit for the past couple of decades. Most of the effort has been put to develop machines and processes focusing on developing the lithographic and processing tools necessary in order to fabricate high resolution devices.[156] However, the ultimate purpose of this research is to develop various forms of micro- or nano- sized devices with high resolution nanoscopic components. A commonly used method of top-down fabrication of patterns is directed electron-beam lithography. This technique works very well and is highly developed, but it has many advantages and disadvantages that will be discussed in this chapter.

3.1 Electron-Beam Lithography Technique

Electron-beam lithography (EBL) is a specialized lithographic technique for creating nanoscale patterns required by the modern electronics industry for integrated circuits. This technique is derived from early scanning electron microscopes. The name of this technique refers to a lithographic process that, in contrast to optical lithography that uses light, uses a focused beam of electrons to expose the desired pattern on a resist coated wafer. Lithography using beams of electrons to expose the resist was one of the earliest processes used for integrated circuit fabrication, dating back to 1957.[130]

Electron-beam lithography systems continue to play two very important roles, which most likely will not diminish in importance for the foreseeable future.[124] First, they are used to generate lithographic masks that are used in optical exposure systems (as well as X-ray systems), and second, they are used in the low-volume manufacture of ultra-small electronic components and features for very high performance devices.[124]

A typical EBL system consists of the following parts: 1) an electron gun or electron source that supplies the electrons; 2) an electron column that controls the position and focuses the electrons into a beam; 3) a mechanical sample stage that positions the wafer under the electron-beam; 4) a vacuum pump to generate vacuum in the chamber; and 5) a computer system that controls these and other components of the equipment. Figure 3-1 illustrates a simplified diagram of an electron-beam lithography instrument.

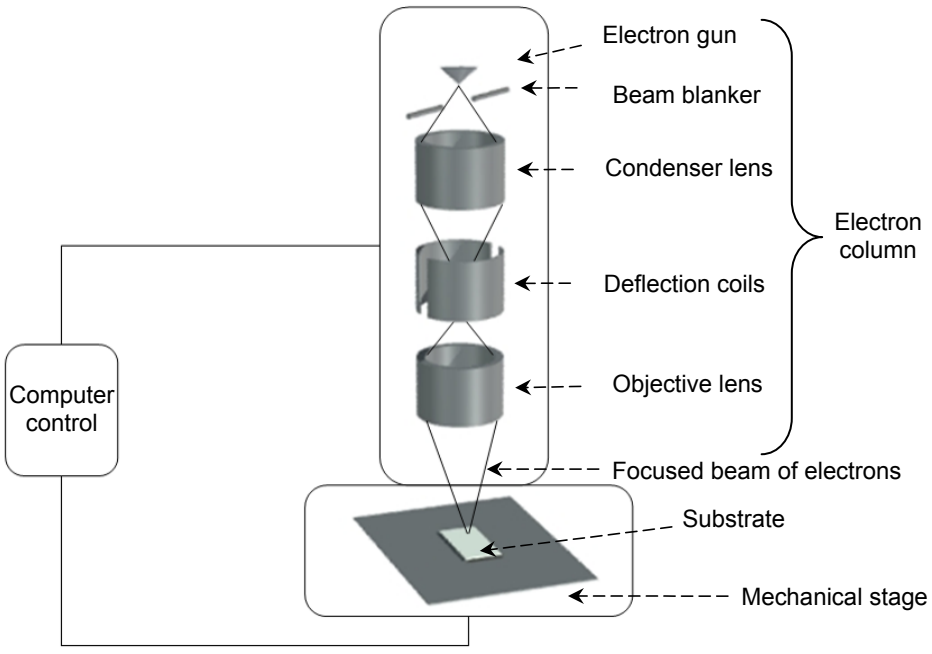


Figure 3-1: A schematic depiction of the key components of an electron-beam lithography tool.

The exposure process must take place in a vacuum to prevent air molecules from interfering with the electron-beam. The column is the controlling system for the electron-beam (see Figure 3-1). It consists of magnetic coils and electrostatic elements that deflect the e-beam and a beam blanker that controls exposure of the electron-beam to the substrate.[132] The beam also passes through electrostatic plates that direct (steer) the beam in the x-y direction on the substrate.

The mechanical sample stage that positions the wafer under the electron-beam is equipped with a high precision laser-interferometric positioning system (resolution 5 nm) and a combination of servo-motors and piezo-electric actuators. This stage is called the ‘XY coordinate system’ to which the coordinate system of the designed pattern will be aligned. The coordinates in the design are called the ‘UV coordinate system’, where the U-axis of the design corresponds to X and the V-axis corresponds to Y in the XY coordinate system. The pattern can be made out of several ‘layers’ in the software, which can be selectively ‘written’ or exposed with electrons on the wafer. In fact, the very accurate alignment of the XY and UV coordinate systems is often used for overlaying patterns to pre-existing alignment marks (which could be previously deposited or fabricated structures) on the wafer.

The blanking and steering functions are controlled by a computer that has in its memory the wafer pattern taken directly from the design stage. The beam is directed to specific positions on the surface by the deflection subsystem and the beam is turned on where the resist is to be exposed. Substrates are mounted on the x-y stage and are moved under the beam to achieve full exposure of the desired pattern. It is for this process of alignment and exposure that this technique is called ‘direct writing’. An electron-beam lithography system follows the pattern that has been made by the user in a compatible program and simply 'draws' the pattern over the resist wafer using the

focused electron-beam as its drawing pen to expose the wafer one point at a time. Thus, such systems produce the resist pattern in a 'serial' manner, making it slow compared to optical systems that can simultaneously expose an entire wafer. Given that a small-diameter, focused beam of electrons that is scanned over a surface, an EBL system avoids the need for masks to achieve high resolution lithography (unlike optical lithography, which uses photomasks to project the patterns).

The pattern exposure in the resist is done by either raster or vector scanning as seen in Figure 3-2.[133] Raster scanning is the movement of the electron-beam side-to-side and down the wafer. The computer directs the movement and activates the beam blanker in the regions where the resist is to be exposed. One drawback to raster scanning is the time required for the beam to scan, since it must travel over the entire surface. In vector scanning, the beam is moved directly to the regions that have to be exposed. At each location, a small square or rectangular shaped area is exposed. These areas are stitched together as the stage moves under the beam in order to build-up the desired shape for the overall exposed area.

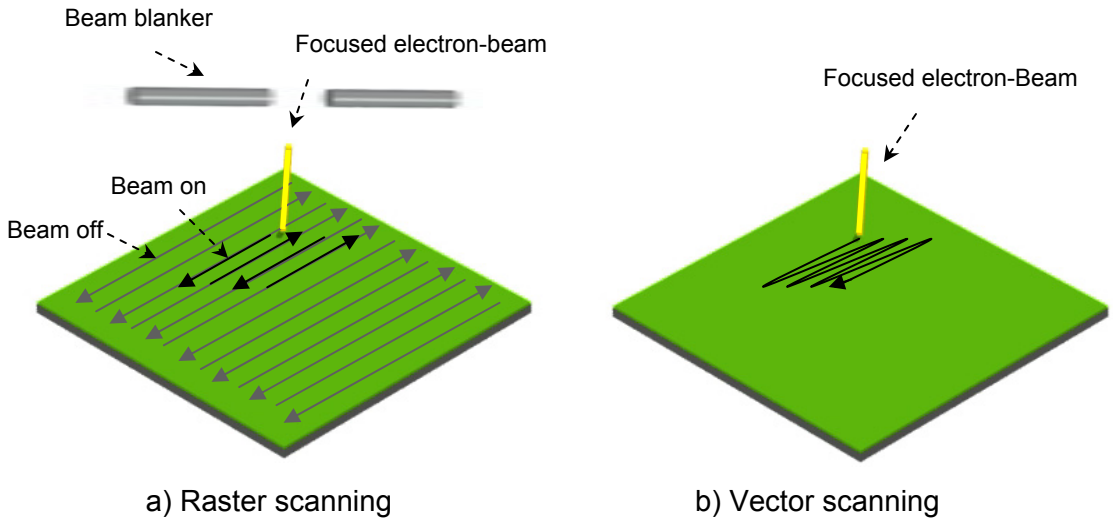


Figure 3-2: An illustration depicting the two modes of exposure in EBL: Raster scanning in (a) and vector scanning in (b). The arrows on the surface illustrate the direction of the travel of the electron-beam. Note that the gray colour of the arrows indicate the beam is off, whereas the black colour indicate the beam is on.

For each magnification used during exposure of the design there is a certain area that can be covered by the e-beam with good precision. This area is referred to as the 'write field' (WF). The deflection of the electron-beam always has some errors, which must be compensated for, by aligning the write-fields with respect to each other and the substrate. In Figure 3-3, the deflection is represented for the e-beam. Since electrons have a much smaller wavelength than that for the light used in photolithography, EBL has a much higher intrinsic resolution. Electron-beam lithography offers higher patterning resolution than optical lithography, because of the shorter wavelengths of electrons (0.2-0.5 angstroms).

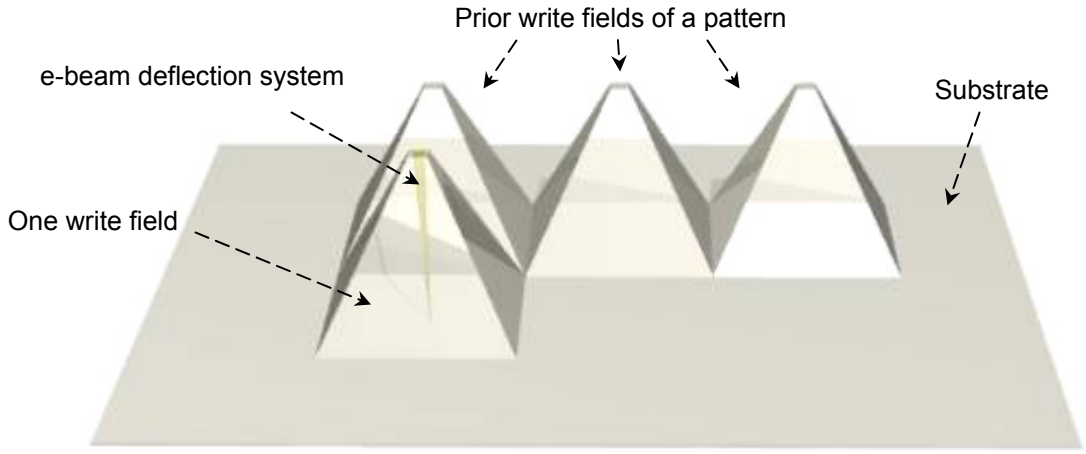


Figure 3-3: A schematic depiction of individual write fields of a pattern on a substrate and the e-beam deflection system for the EBL tool. Each cone depicts the area covered by deflection of the e-beam associated with one write field.

While optical lithography requires photomasks to project patterns, the electron-beam can be directly focused onto a substrate and controlled so it only exposes specific areas, without needing a mask to block unwanted exposure of other areas.[134] Alignment and overlay parameters are very good with electron-beam systems, because few distortions are introduced from electron scattering. The resolution is also good, with current machines capable of <20 nm critical feature sizes.[135] Nevertheless, the resolution of an electron lithography system is still limited by factors such as backscattering of electrons at the substrate's surface, the sensitivity of resists, and various aberrations in its electron optics.[21,132] Patterning of features with less than 20 nm line-widths can be achieved in a resist such as PMMA.[22] Depending on the design, e-beam energy varies in the range of 0.1-200 keV with a spot size down to a few nanometers.[136] The beam current and the scan field size are determined according to

the experimental requirements. These experimental parameters are noted in Section 3.4.2.

The resolution of e-beam lithography also depends on the beam size and several factors related to the electron-solid-interactions.[132,139] In fact, for e-beam lithography, the resolution is mainly determined by the scattering of primary and secondary electrons in the resist film and the underlying substrate. In a resist, electrons undergo forward scattering and some back-scattering events that come from the substrate. The forward scattering tends to broaden the initial beam diameter, whereas the back-scattering can spread the electrons over a large volume (see Figure 3-4). These scattering events cause a broadening of patterns and are commonly referred to as proximity effects.[136] During this process, the electrons slow down continuously, providing a cascade of low-energy electrons (secondary electrons) that expose a much larger area of the resist than the area of the incoming electron-beam.[134] The secondary electrons induce a reaction within the resist that can induce polymerization, polymer cross-linking or chain scission as well as more complex processes such as chemical amplification involving acid-base reactions.[140]

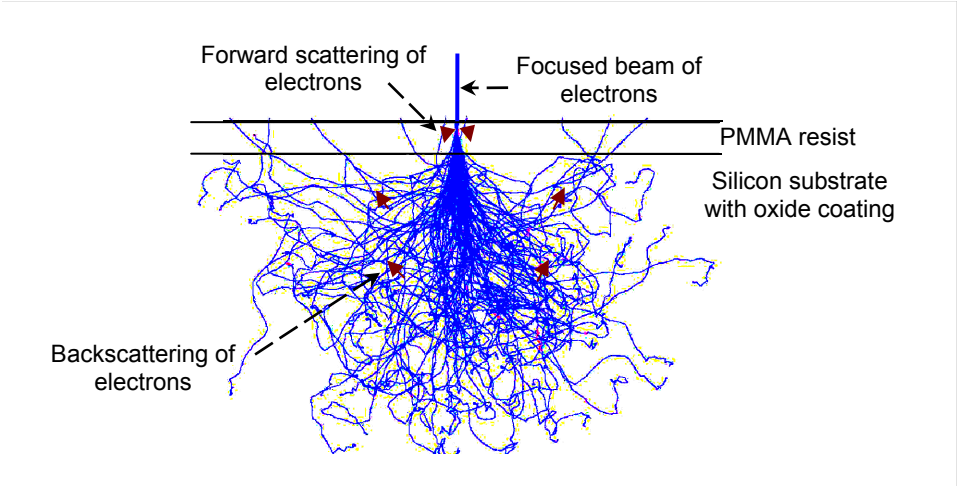


Figure 3-4: An illustration depicting the electron-beam trajectory and the resist area affected due to the forward and backscattering of electrons.

The proximity effects due to scattered electrons in these systems can be corrected by varying the dose of electrons. In principle, low energy electrons (~1 keV) yield very limited proximity effects because of their short penetration depths and therefore require thin resist layers.[132]

3.2 Choice of Resist for Electron-Beam Exposure

Electron resists are polymers that behave similar to photoresists in which irradiation can induce a chemical change. This change allows the resist to be patterned. For a positive electron resist, the interaction of electrons with the polymer causes chemical bonds to be broken to form fragments of smaller molecular weight. Therefore, areas that have been irradiated and have smaller molecular weight fragments have a higher dissolution rate in a developer solution. Common positive electron resists include

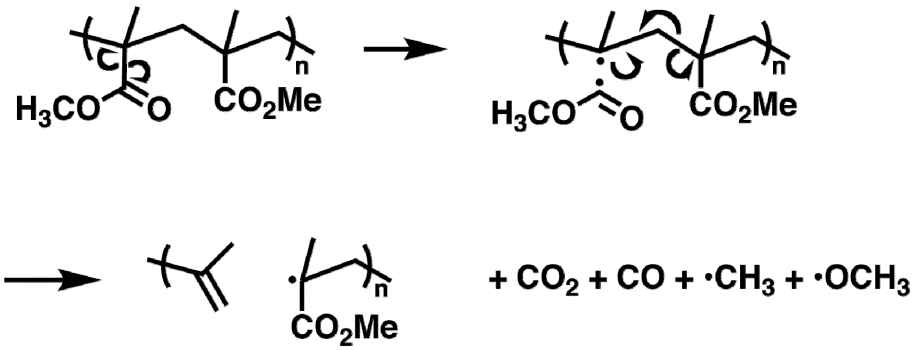
poly(methyl methacrylate) (PMMA) and poly(butane-1 sulfone) (PBS).[23] Poly(methyl methacrylate) is the first polymer discovered to be used as an e-beam resist,[141] and is one of the most commonly used positive resists, and a resist with one of the highest resolutions available.[142] The PMMA resist solution is typically composed of 1-10% solids dissolved in either anisole or a similar solvent. Ready-to-use PMMA resist can be purchased from manufacturers such as MicroChem (see further details in Section 3.4.1). The solid content of PMMA in the mixed solvent directly influences both the viscosity of the resist and the thickness of a spun cast film. For example, spin coating PMMA resist with 4% solids at 2500 rpm will produce a film thickness of 0.5 μm, as opposed to a 2 μm thickness for 9% PMMA that are spin cast under identical conditions.

Generally, the most important resist criteria are resolution, contrast and sensitivity for the exposure source (electrons or photons) and energy.[142] Poly(methyl methacrylate) is distinct, relative to other resists, for having high resolution, high contrast and low sensitivity.[125] Resist sensitivity to developing solvent (developing efficiency) depends on the relative molecular mass, whereby the higher the relative molecular mass the lower the sensitivity. This relation is due to a decrease in solubility of PMMA in developer when the relative molecular mass increases. Commercial PMMA resists have various relative molecular mass; however, relative molecular mass of 495 k and 950 k g/mol PMMA are commonly used for electron-beam lithography. The sensitivity of PMMA is also based on electron acceleration voltage and the dose factor chosen, both of which ultimately account for the exposure dose (units for exposure dose are $\mu C/cm^2$) of a given sample and must be optimized for each sample.

In PMMA resist that has been exposed to electrons, both cross-linking and fragmentation of the polymeric chains occur. However, the rate of chain scission is much larger than that of cross-linking. While there are certain contradictions in terms of what

species are formed after exposure, based on EPR measurements of irradiated PMMA,[127] most agree that the fragmentation of PMMA occurs by the first mechanism shown in Figure 3-5.[127,143-145] Both recognized mechanisms of PMMA degradation are shown in Figure 3-5.[146, 147]

Mechanism 1:



Mechanism 2:

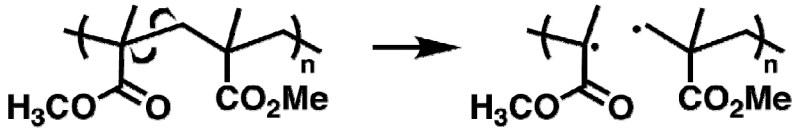


Figure 3-5: Two recognized mechanisms for PMMA degradation.

As shown in Figure 3-5, both proposed mechanisms indicate production of radical fragments. The unstable radical species are likely to interact with the selenium nanowires embedded in the resist material. Such an interaction may introduce electrochemical changes or damage to the *t*-Se nanowires. Regions of selenium nanowires exposed to the e-beam, under the gold electrode, can be compared with the unexposed regions of the nanostructure. A high-energy focused beam of electrons can

be damaging to materials. In fact, many studies make use of the high energy of electrons to induce a reaction.[174] As well, our prior SEM imaging of V_2O_5 nanowires (not discussed in this thesis) was difficult, as this material melted and deformed within seconds of exposure to a high-energy beam of electrons.

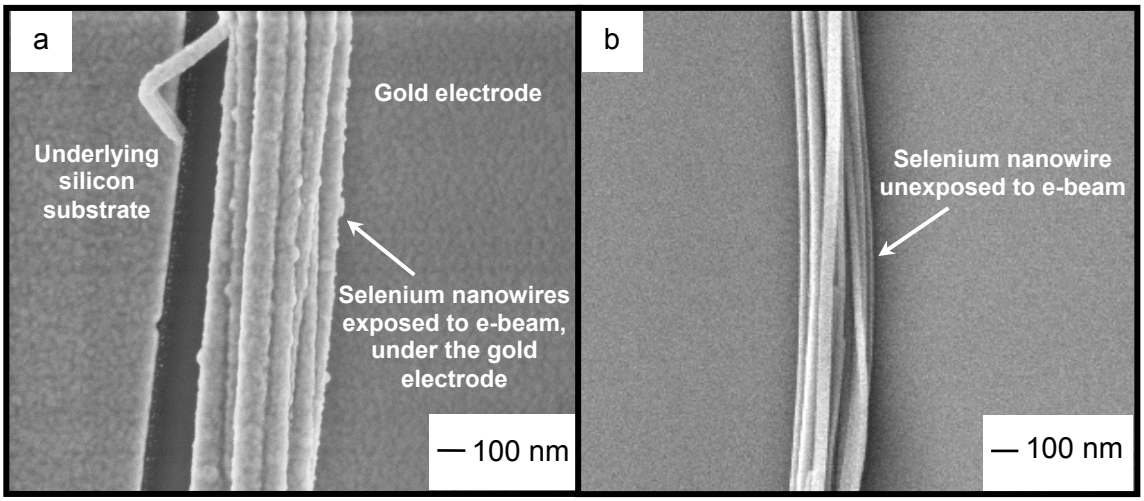


Figure 3-6: An SEM image depicting the selenium nanowires exposed with electron-beam in (a), taken after the overlay of the gold electrode. SEM image shown in (b) depicts an unexposed region selenium nanowires.

Regardless of what species are formed during degradation, interaction of the electron-beam with PMMA causes local chain scission resulting in formation of lower molecular weight monomers and oligomers. The fracturing of PMMA will enhance the solubility of this material in a developer that consists of methyl isobutyl ketone (MIBK) and 2-propanol (IPA).[146]

The sensitivity of PMMA also depends on the concentration of developer. Standard developer is a mixture of MIBK and IPA with concentration ratio of MIBK:IPA of 1:3. Increasing the MIBK concentration can enhance the PMMA sensitivity, but at the

expense of resolution. The relative effect of developer concentration versus sensitivity and resolution of features is shown in Table 3-1.

Table 3-1: Relative influence of developer concentration in isopropanol on sensitivity and resolution.[125]

Developer Concentration (MIBK: IPA, v/v)	Efficiency of the developing process (sensitivity of resist)	Resolution
1:3	Low	Extremely high
1:2	Medium	Very high
1:1	High	High
Pure MIBK	Very high	Low

3.3 Variations to Previously Developed Experimental Steps to Overcome Lift-Off Challenges

Multiple-layer Resist Coating

The positioning of metal contacts onto selenium nanowires faced challenges in lift-off of the gold layer, as described in the previous chapter. An approach was, therefore, developed to address this concern, which is referred to as multiple-layer resist coating (or multiple-resist approach in this thesis). The resists within each layer of the multiple-layer resist stack are chosen based on their different response to the exposure and developer. In this thesis, a bi-layer stack of resists was used such that the bottom layer resist was more sensitive than the top layer to the source of irradiation. Hence

more area of the bottom resist is affected by the exposure compared to that of the top layer. The advantage and outcome of multi-layer resist coating compared with single-layer resist are discussed in the following sections.

Development of Multiple-Layer Resists

The developing results are slightly different in a multiple-layer resist stack compared to that of a single-layer. In this set-up, since the bottom layer is chosen such that it is more sensitive to irradiation, more of the bottom layer will dissolve in the developer compared to the top layer for a given developing time. This result is depicted in Figure 3-7, which is referred to as an undercutting profile. The advantage of having an undercut profile will be explained further in the lift-off step later in this section.

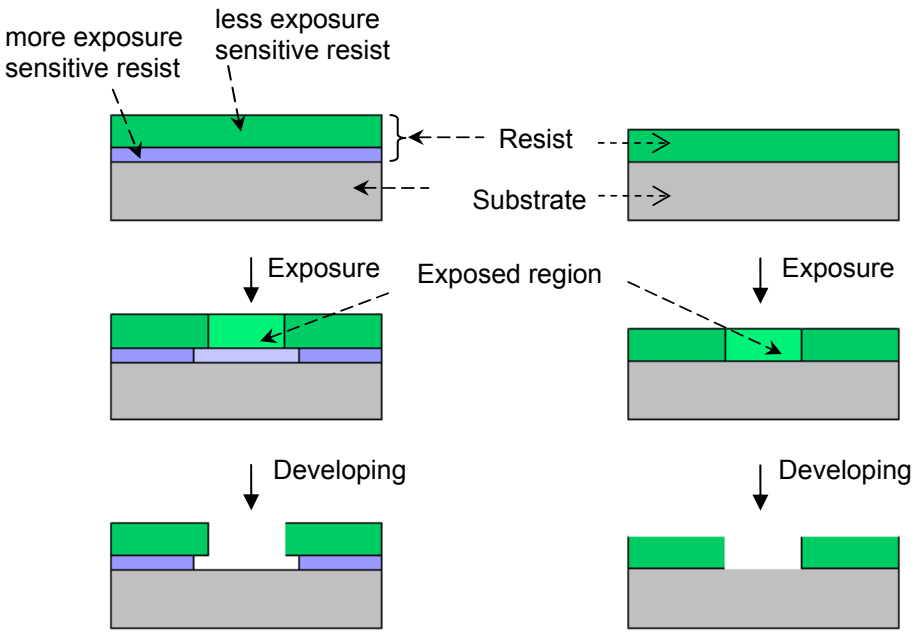


Figure 3-7: A schematic of substrates with single and bi-layer resist after the developing step, in which the undercutting profile can be seen for the bi-layer resist covered substrate.

The developing time in a bi-layer stack is very critical since a short developing time will result in the width of the undercut layer being small, which would not have the effect that is desired. Similarly a longer developing time is not desired either, as it could lead to the top layer collapsing onto the underlying surface due to lack of support. The collapse of the top layer could also occur in the metal deposition step (see Section 2.5.9) on the substrate.

Metal Deposition on Multiple-Layer Resist Stack

Metallization on single and bi-layer resist substrate is shown in a schematic in Figure 3-8. As depicted in the figure, metal layer deposited on the surface of a single layer substrate is connected all throughout. However, a bi-layer resist coated substrate

due to the presence of the undercutting profile created in a previous step of development, the connection is broken in the metal film. The importance and advantage of this discontinuity will be explained in lift-off process.

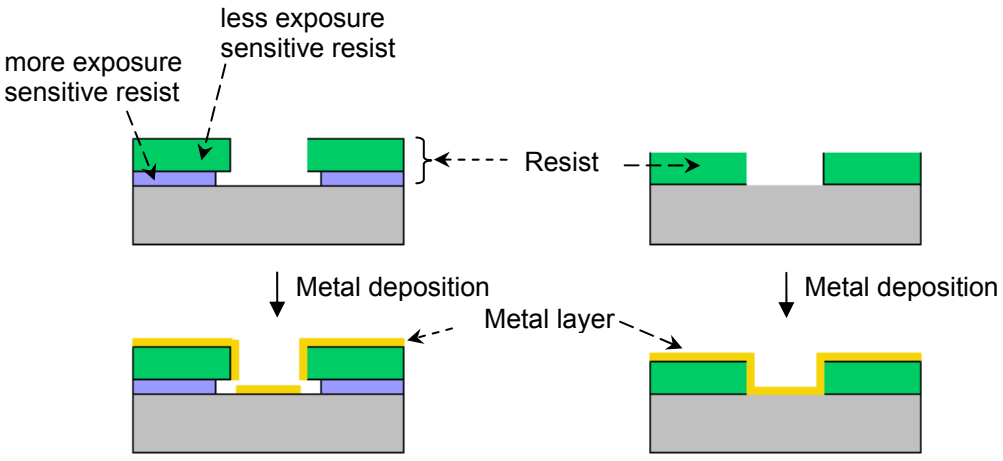


Figure 3-8: A cross-sectional schematic of substrates with single and bi-layer resist after metal deposition step. This schematic is the continuation step from Figure 3-7.

Lift-Off of Metal-Covered Resist

Performing sonication and heating may not be an issue for certain materials and structures, but as discussed earlier heat and sonication assisted lift-off is detrimental to selenium nanowires. Since the goal of this research is to place electric contacts on selenium nanowires, the bi-layer system was utilized. As depicted in Figure 3-9, the undercutting profile that was created using a bi-layer resist stack in the developing process provides a gap for the solvent to wash away the metal coated resist that remains.

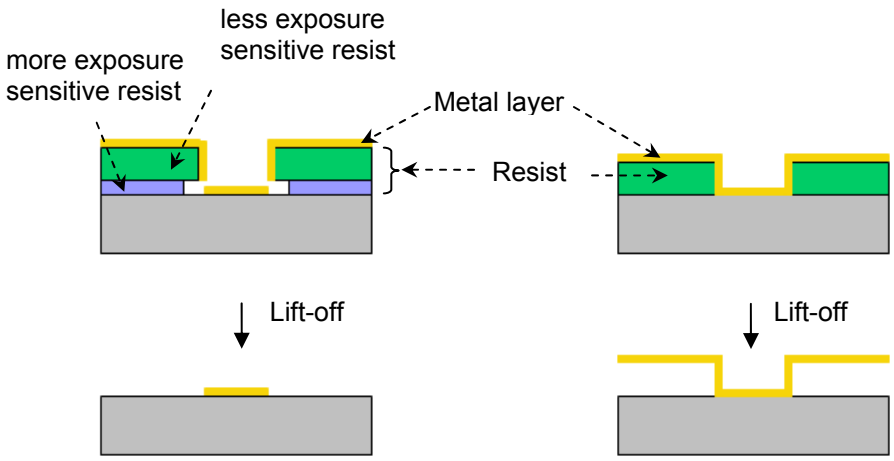


Figure 3-9: A cross-sectional schematic of substrates with single and bi-layer resist after the lift-off step. This schematic is the subsequent step to that depicted in Figure 3-8.

3.4 Experimental Details

Silicon wafers as previously described in 'Silicon Wafer Substrate Pre-Treatment' in Section 2.6.1 were used for the following experiments of metal contact overlay on selenium nanowires (see Appendix A). Wafers were cleaved into smaller (~1 cm x 1 cm) chips to be used as substrates.

3.4.1 Deposition of Electron-Beam Resist on Silicon Wafers

Before spin casting the wafer with resist, the wafers were baked on the hotplate at 180 ºC for 120 s to remove water molecules adsorbed on the surface. A silicon chip was centered on the chuck holder of the spin coater and several drops of methyl methacrylate (8.5 MMA purchased from MicroChem- Lot #: 05050318) were then dispensed to fully cover the surface. The wafer was then spun by ramping up at a rate of

~1000 rpm/s to reach a spin speed of 4000 rpm, which was held for 40 s. The silicon chip was then baked (pre-bake step) on a hotplate at 180 ºC for 60 s. Note that during the entire process, after every bake step, the chip was placed on a cold metallic surface to transfer out the heat. A volume ratio of anisole solvent (anhydrous anisole, 99.7% purchased from Sigma Aldrich- Batch #: 01946LD) was added directly to 7% PMMA (950 PMMA A7, purchased from MicroChem – Lot #: 04120897), to make a ~1% PMMA solution. This dilute solution of resist was spin cast on the substrate at 4000 rpm for 40 s and baked on a hotplate at 180 ºC for 60 s. In ~2 mL anisole solvent, roughly 2 drops of the concentrated selenium nanowires were added to produce a mixture that contained visually non-aggregated selenium nanowires in anisole. The next resist layer consisted of selenium nanowires in anisole used to dilute the 7% PMMA to make a resist of ~2% PMMA containing selenium nanowires. This mixture was spun at 4000 rpm for 40 s and post-baked on a hotplate at 180 ºC for 60 s. Lastly, a 4% PMMA in anisole was spin cast and baked using the same parameters used above.

3.4.2 Exposure of Electron Resist with a Beam of Electrons

The electron-beam exposure was performed using a Raith e-LiNE writer. In the experiments, an electron-beam with an accelerating potential of 10 kV was used with an aperture opening of 30 μm, which resulted in a nominal beam size of 2-4 nm. Patterns were generated using a GDSII drawing program that is incorporated in the Raith control software. The computer controller for pattern generation controls the beam exposure, following the designed pattern and parameters such as beam step size, dose factor and area dose (combination of the last two factors results in the amount of electrons a given area of sample is exposed to). Important parameters to note that were used for this experiment for exposure are: area dose of 110 $\mu As/cm^2$, a dose factor of 2, a beam

speed of ~10 mm/s and a write field of 100 μm x 100 μm. It is important to note that there is an equation provided by Raith for calculating the total charge of incident electrons, which is:

$$\text{Total charge of incident electrons} = \frac{\text{Beam current x exposure time}}{\text{Step size x 2}} = \text{dose x exposed area} \qquad \textbf{Equation 3-1}$$

However, optimizing the parameters is always done experimentally. Also, to focus the electron-beam and optimize the astigmatism, 112 nm diameter polystyrene particles and 18 nm diameter gold nanoparticles were placed at the corners of the silicon chip on top of the resist.

There are some challenges using electron-beam lithography. For instance Figure 3-10 depicts an exposed pattern with some misalignment between the write fields.

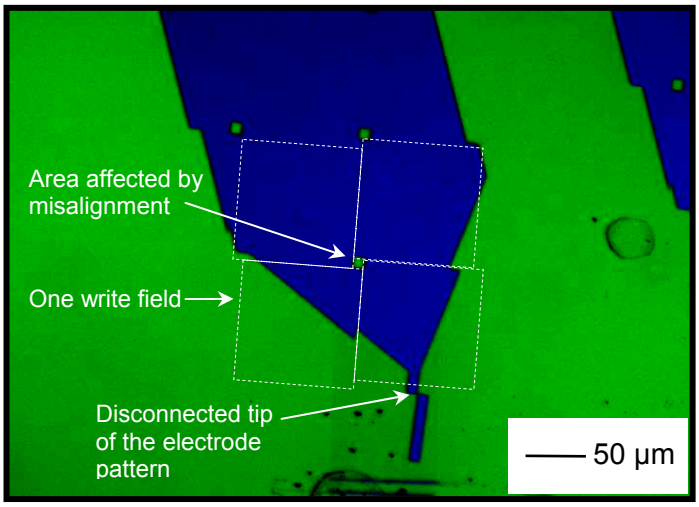


Figure 3-10: A bright-field optical image of a substrate after the developing process. This image depicts the misalignment between write fields of an exposed pattern.

The write fields outlined with red squares need to be aligned right next to each other, as previously shown in Figure 3-3, to avoid any pattern misalignment. A parameter modified to avoid this problem was the dwell time of the e-beam which was increased from 1 ms to 5 ms in between the write fields.

Unlike the microscope projection photolithography technique, in this technique any region of the sample that is viewed with the electron-beam (SEM imaging mode) would be exposed to the electron-beam. Depending on the amount of exposure that the sample receives, the results may or may not be desirable. During the time that sample is viewed via SEM imaging mode, the coordinates of the nanowires upon which we desire to overlay a pattern is recorded and registered in the computer controller to allow the exposure of desired patterns at specific locations. Figure 3-11 shows initial attempts of exposure using a focused electron-beam. As it is illustrated in Figure 3-11-a, the viewing field fully exposed an area around the nanowire. Figure 3-11-b depicts faster attempts (dependent on the magnification used for viewing, these times are ~3-5 s) resulted in a pattern close to, but not on the nanowire (nw). Figure 3-11-c shows that a partial exposure of the viewing field that has occurred.

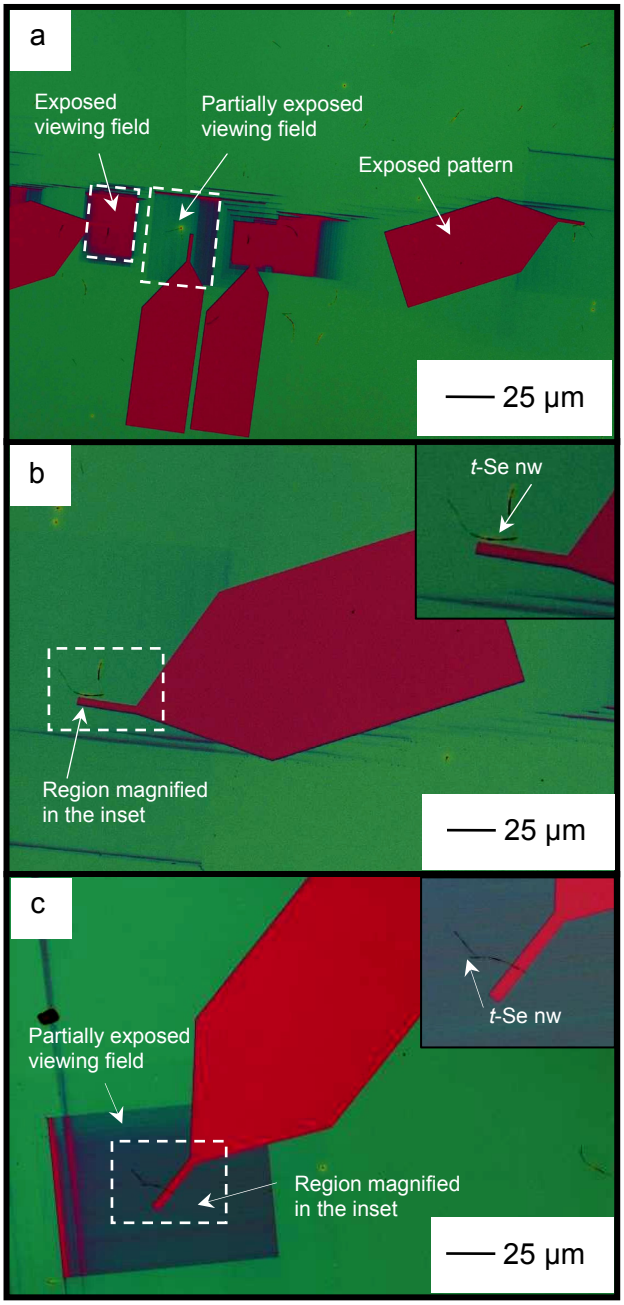


Figure 3-11: Bright-field optical images of e-beam exposed substrates depicting exposed viewing field in (a), misalignment of the pattern to a selenium nanowire in (b) and a partially over exposed viewing field in (c).

3.4.3 Developing of Electron Resist

After exposure, the substrates were baked at 90 ºC for 30 s. The substrates were then treated and developed in a solution of MIBK/IPA (1:3, v/v) for 30 s, after which the developing was stopped by immersion of the substrate in an isopropanol solution. This substrate was then thoroughly rinsed with DI water for 2 min and then dried under a stream of pressurized, filtered air. Figure 3-12 and Figure 3-13 depict successful overlaying of patterns on nanowires.

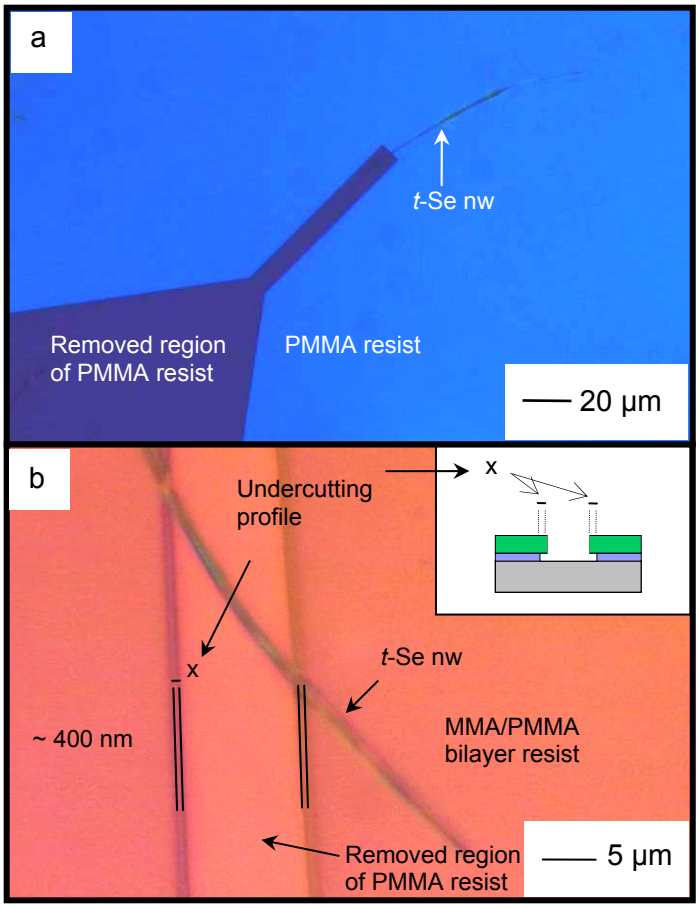


Figure 3-12: Bright-field optical images of developed patterns from electron-beam lithography exposures. Image in (a) depicts a successful overlay of a pattern on a selenium nanowire and that in (b) depicts the undercutting profile for a developed bi-layer resist stack. The inset in (b) depicts a side view illustration of the undercutting.

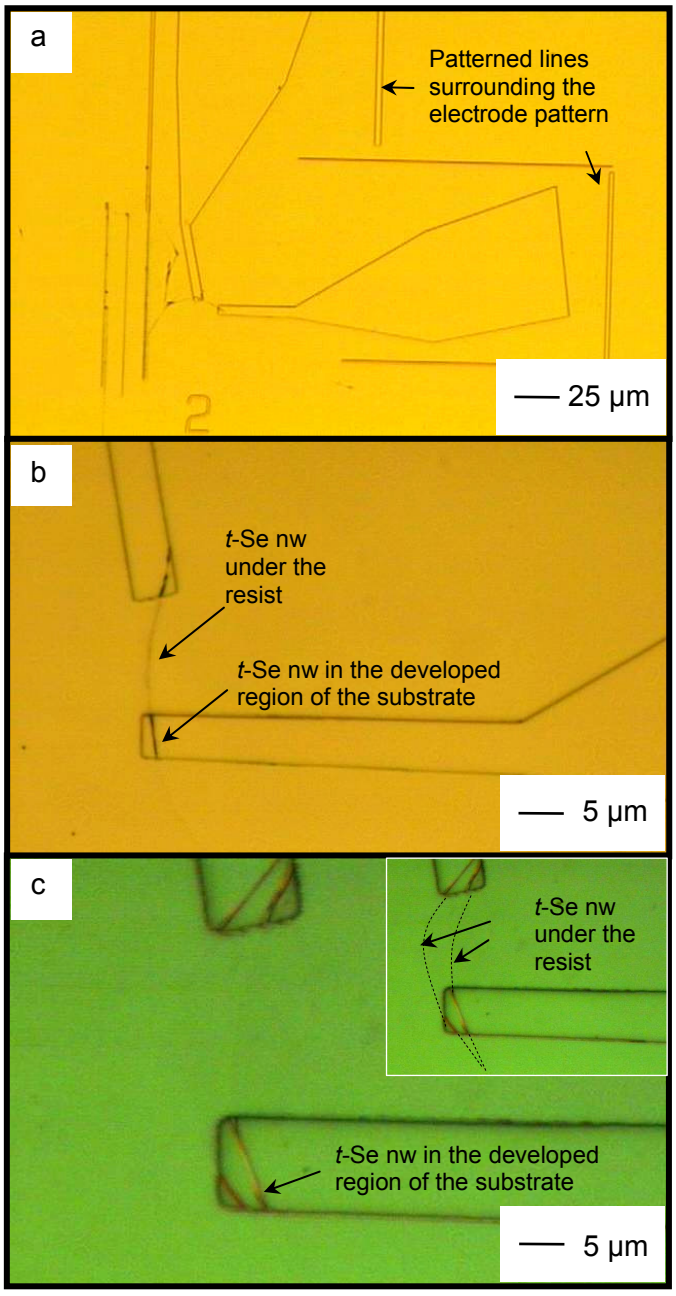


Figure 3-13: Bright-field optical microscopy images of pattern exposure on selenium nanowires via a direct electron-beam writing technique. These images were taken after developing the PMMA resist. Note that in (a) the patterned lines surrounding the electrode pattern are positioned to create more breaks in the gold layer and assist with the lift-off process. Notice that in image (c) the ends of the nanowire, where the resists has been developed, can be seen with more contrast compared to the part of the nanowire under the resist. The inset in (c) indicates the positions of the nanowires under the resist with dotted lines.

As seen in Figure 3-13a there are a number of line patterns surrounding the electrode pattern. These line patterns are placed to create more regions with an undercutting profile after developing process, which helps break the gold layer film into smaller pieces and make the lift-off process less challenging (see Figure 3-14).

3.4.4 Metal Deposition on Developed Electron Resist Coated Silicon Wafers

The substrate was positioned and fixed on the holder of a Lesker thermal evaporator (more details of operation are located in Appendix B). A film of 5 nm Cr and 50 nm Au was deposited onto the wafers. Specifications for metal deposition were mentioned in 'Metal Deposition on Developed Photoresist Coated Silicon Wafers' in Section 2.6.5.

3.4.5 Lift-Off of Metal Covered Electron Resist

After metallization, the substrates were placed in an acetone solution warmed to ~50 ºC. In roughly 1 h, gold layer wrinkled as the solvent diffused under the gold layer to wash away the remaining resist. This part of metal layer can be washed away with a gentle solvent flow from acetone wash bottles. High-pressure flow of solvents or the use of solvents with high surface tension such as water, can wash away the wrinkled layer of gold; however, these solvents can also break the selenium nanowires. It is best to keep the substrate in the warm acetone overnight (~12 h) to allow the gold layer to lift-off with only gentle agitation of the solvent and to avoid breaking the selenium nanowires as

shown in Figure 3-15. Optical images of substrates with gold electrode overlaying the *t*-Se nanowires after the lift-off process are depicted in Figure 3-14.

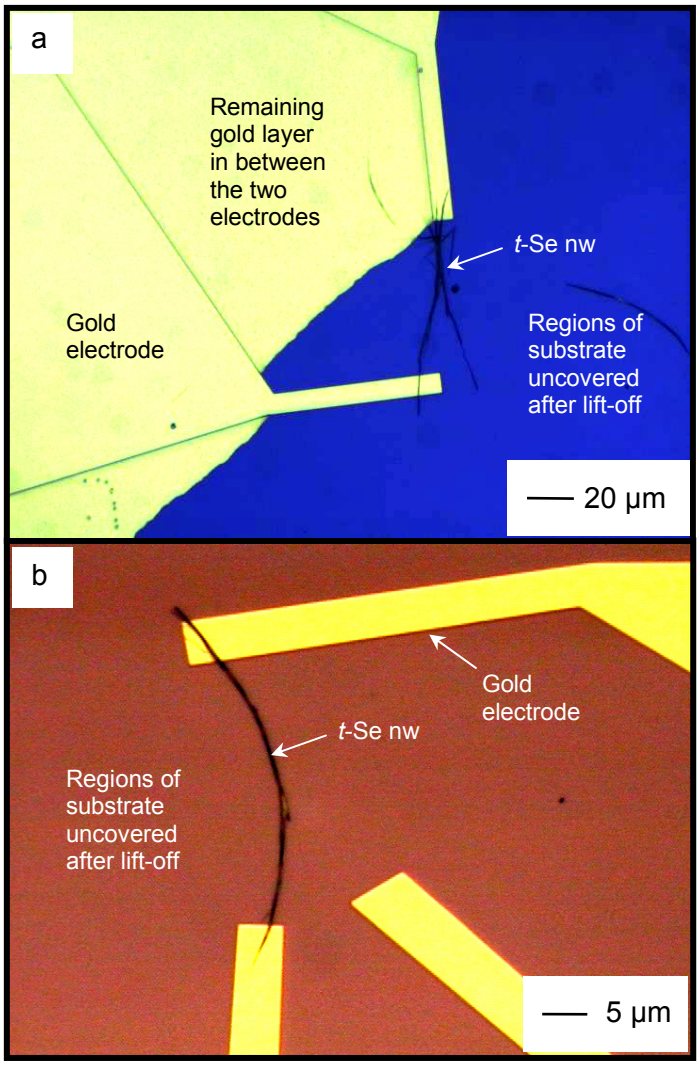


Figure 3-14: Bright-field optical images taken after the lift-off step. a) This image depicts an unsuccessful lift-off of the gold layer from the unpatterned areas in a single-layer resist coated substrate. b) This micrograph depicts the successful lift-off process in a bi-layer resist substrate. Note that the patterned region of gold not on the nanowire is placed near the nanowire to help break-up the gold layer and help the lift-off.

3.4.6 Challenges of Gold Layer Lift-Off from Resist Covered Selenium Nanowires

Solvent Incompatibility with Selenium Nanowires

A number of resists were considered for the bottom, more sensitive layer of the resist bilayer. Prior to experiments using MMA, LOR-3B (purchased from MicroChem- Lot # 08090642) was deposited in place of MMA. In these experiments, the fabrication process followed was the same as procedure using MMA that was mentioned above. LOR 3B resists requires solvents such as Shipley's MFP-319 or Microposit remover-1165 in the lift-off process. The primary component of Microposit remover-1165 is 1-methyl-2-pyrrolidinone and for MFP-319 is tetramethylammonium hydroxide. Both of these reagents were found to etch (or otherwise dissolve) selenium nanowires at the temperature of ~100 ºC that is required for the lift-off process. Lower temperatures of ~40 ºC were also experimentally tested for these developers with unsuccessful results in the lift-off step. While the solvent for the lift-off step was not chemically compatible with selenium nanowires (e.g., it etches or otherwise damages the selenium), the procedure can be applicable to nanowires and nanorods of other compositions.

Challenge of Maintaining Selenium Nanowires During the Lift-Off Process

As selenium nanowires are very soft and break easily, solvent exchange was performed after the lift-off process before taking the substrate out of the solvent. In the process of solvent exchange a solvent with lower surface tension was introduced in the container storing the substrate prior to taking the substrate out as explained in Section 3.4.5. Among solvents with relatively low surface tension, n-hexane (with a surface tension of 18.3 dyne/cm at 20 °C) was used. Substrates taken out of the pure hexane

solvent did not have torn nanowires between the electrodes. Figure 3-15 is a depiction of torn nanowires between the two electrodes after the substrate was rinsed with water.

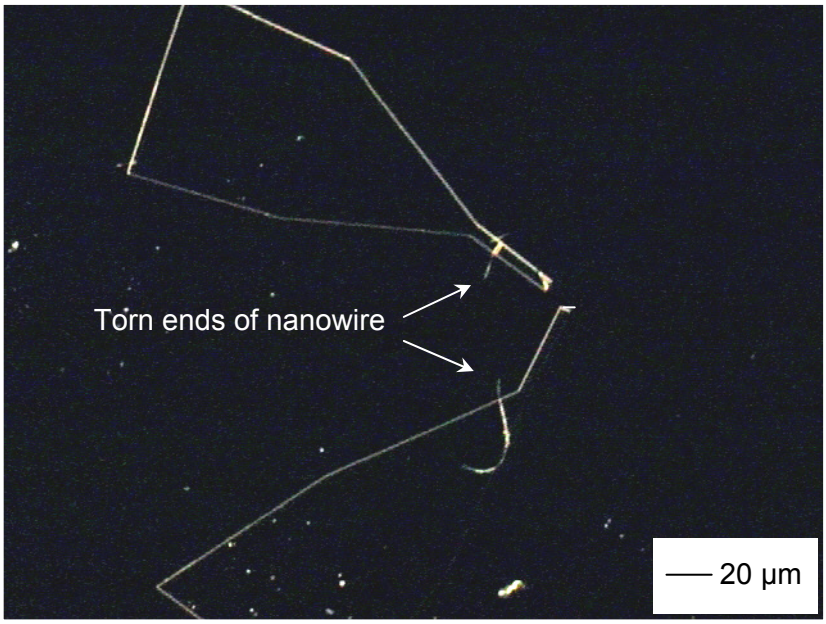


Figure 3-15: An image acquired by dark-field optical microscopy depicting a torn nanowire after rinsing the substrate with water following to the lift-off step.

3.5 Conclusions and Discussion

In the experiments performed using electron-beam lithography, a process was developed to overlay metal contacts on selenium nanowires. Electron-beam lithography offers higher patterning resolution than optical lithography since it employs high energy electrons that possess shorter wavelengths. The short wavelength of these high-energy electron-beams gives e-beam writing a much higher resolution capable of producing patterns with nanometre scale features. Regardless of the successful results obtained from this technique, there were a number of limitations to using this approach for patterning. Use of the EBL approach is much more costly compared to MPP as it requires an electron-beam writer with access to cleanroom facilities. This technique has

limited throughput of samples due to the serial exposure of patterns. Patterns of electrodes exposed by the EBL technique shown in this thesis took ~20 min for every electrode (~40 min for a set required for the *t*-Se nanowire measurements). Hence, the exposure time is dependent on the size of the pattern. Another limitation of this technique, using the processes developed in this thesis, is the requirement for rapid alignment of patterns with nanostructures on the substrate as the whole area in the field of view is in danger of being over-exposed. It is important to point out that the high energy electrons could also damage the section of the nanowire upon which the pattern is overlaid. Hence, the conductivity measurement obtained from nanowires obtained from this technique may not be accurate.

CHAPTER 4: CONDUCTIVITY MEASUREMENT OF SELENIUM NANOWIRES

4.1 Conductivity of Materials

Materials have different uses in the arts, engineering and sciences depending on their properties. One of the main criterion in selecting materials for engineering devices is their fundamental properties such as thermal, magnetic,[37,38] electrical[40] and optical[15,27,40] properties. These physical properties describe the way by which materials respond to external factors such as mechanical stresses, heat, magnetic fields, electrical fields and electromagnetic radiation. With the current advancement of nano-science and general trend on miniaturization of devices, it is important for the scientific community to develop and incorporate nanomaterials for technologically applicable and important devices such as sensors,[9-12,54] transistors,[14,55] photodetectors,[60,61] photovoltaics[17,18,58,59] and other electronic devices.[13-16] It is, therefore, necessary to have fabrication techniques and processes by which these structures can be incorporated and connected with other device set-ups so that their conductivity properties can be measured without damaging the nanostructures. These techniques need to make fabrication in a fast and cost-effective approach. Electrical properties of these nanostructures could be tuned fast and at low cost as a result of continual synthetic modification of the nanostructure.

The techniques and processing developed in Chapters 2 and 3 of this thesis provide a practical process for incorporation and metal contact fabrication to 1D

nanostructures. In this thesis, gold metal electrodes were fabricated on selenium nanowires. The conductivity properties of selenium nanowires were not studied in-depth in this thesis. However, to assure that the developed procedures can be used for further electrical measurements, some conductivity measurements were performed, the details of which will be briefly explained in the rest of this chapter.

4.1.1 Current-Voltage Characteristics

The development of electronic materials in solid-state devices primarily occurred in the second half of the twentieth century, but the first unexpected observations of semiconducting materials behaviour took place somewhat earlier than this period. In 1833, Faraday found that silver sulphide exhibited a decrease in electrical resistivity with increasing temperature.[148] Today, almost two centuries later, scientists are still investigating electrical conduction properties of materials and their response to external factors such as mechanical stresses, heat, magnetic fields, electrical fields and electromagnetic radiation.

The conductivity characteristics of a material are measured using the relationship between the voltage applied across the terminals of a material and the unidirectional flow of charge through it and is considered the current-voltage characteristic of the material, represented by *I-V* curves. The simplest *I-V* curves involve a resistor, which according to Ohm's law exhibits a linear relationship between the applied voltage and the resulting electrical current.

The resistance of a material is defined as

$$R = \frac{V}{I} \qquad \textbf{Equation 4-1}$$

where R is the resistance (measured in ohms, Ω), I is the current (measured in amperes, A) and V is the voltage or the electrical potential difference across the material (measured in volts, V). In general, R can be a complicated function of both the current and temperature. However, when R is a constant, the equation can also be written as

$$I = \left(\frac{1}{R}\right) \times V \qquad \textbf{Equation 4-2}$$

Hence, the reciprocal of the slope of the *I*-*V* plot equals the resistance, *R*.

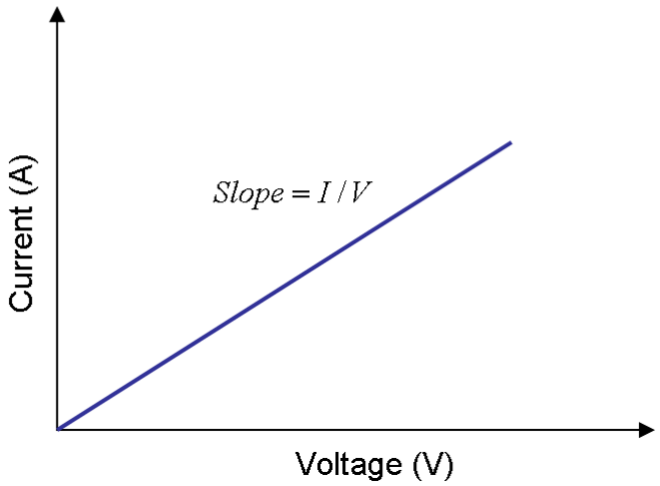


Figure 4-1: The current-voltage curve of a simple resistor.

The resistivity of materials depends on a number of factors, including externally controlled factors (e.g., temperature, irradiation with electromagnetic light) and factors such as dopants within the material or the dimensions of the material. For example, an increased conductance with increasing temperature has been previously observed in *t*-Se crystals.[71]

In fact, resistance may be defined as a function of the intrinsic electrical resistivity (ρ), cross-sectional area (A) and length (l) of 1D nanostructures, as seen in Equation 4-3.

$$R = \rho \frac{l}{A} \qquad \textbf{Equation 4-3}$$

Conductivity of a material is the reciprocal of its electrical resistivity, as shown in Equation 4-4, with units: $\Omega^{-1}cm^{-1}$.

$$\sigma = \frac{l}{\rho} \qquad \textbf{Equation 4-4}$$

Due to the complex relationship of resistance with some of the mentioned factors, *I*-*V* measurement of some materials may produce a non-linear curve, as will be discussed in the case of *t*-Se nanowires.

4.2 Electrical Characterization

4.2.1 Electrical Measurement Using a Wire Bonder

One of the methods of making interconnections between integrated circuits and a circuit board in semiconductor device fabrication is with the use of a wire bonder. For the electrical characterization of selenium nanowires, originally a wire bonder was repaired for our use. However, due to a number of factors such as non-reproducibility of bonding this method was not pursued further. Figure 4-2 shows an image of the wire bonding done on a substrate assembled in an integrated circuit (IC) package.

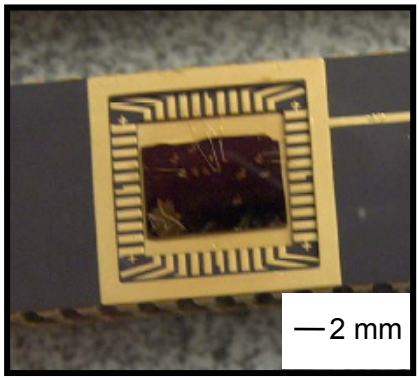


Figure 4-2: An image of a substrate wire bonded to a DIP (dual in line) IC package.

Electrical characterization using a wire bonder may be pursued in the future with a recently purchased wire bonder. Our alternative solution at the time was to use a probe station.

4.2.2 Electrical Measurement Using a Probe Station

The electrical measurement of selenium nanowires –with metal contacts of Cr/Au (5 nm/50 nm, respectively) placed at either end of the nanowires– were obtained using a probe station (model: Cascade 150) and analysis system (model: Semiconductor/ parameter analyzer: Agilent B1500) as seen in Figure 4-3.

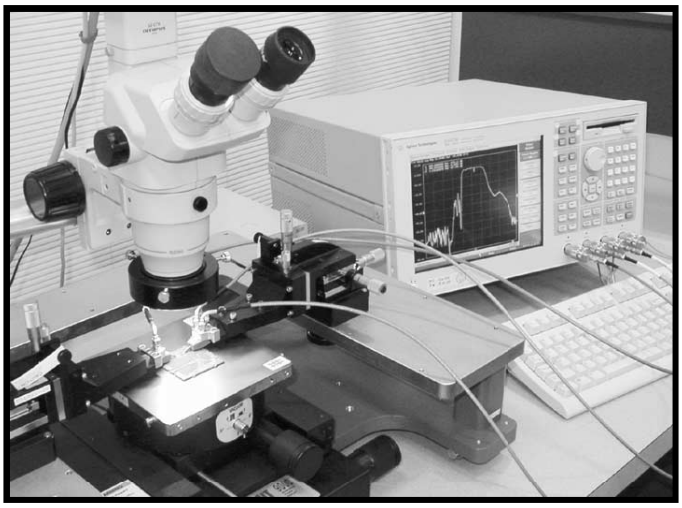


Figure 4-3: An image of the probe station and the electronic analyzer.

The substrate containing the nanowires was placed on the probe station stage and held fixed in position by a vacuum chuck. The probes (that are essentially long flexible metallic arms) can move very accurately using knobs provided for coarse and fine movement to ensure the accurate positioning of the flexible electronic probes onto the electrical contacts at the two ends of a selenium nanowire. By looking through the eyepiece of the microscope and with fine movement of the stage, a set of contact pads can be selected.

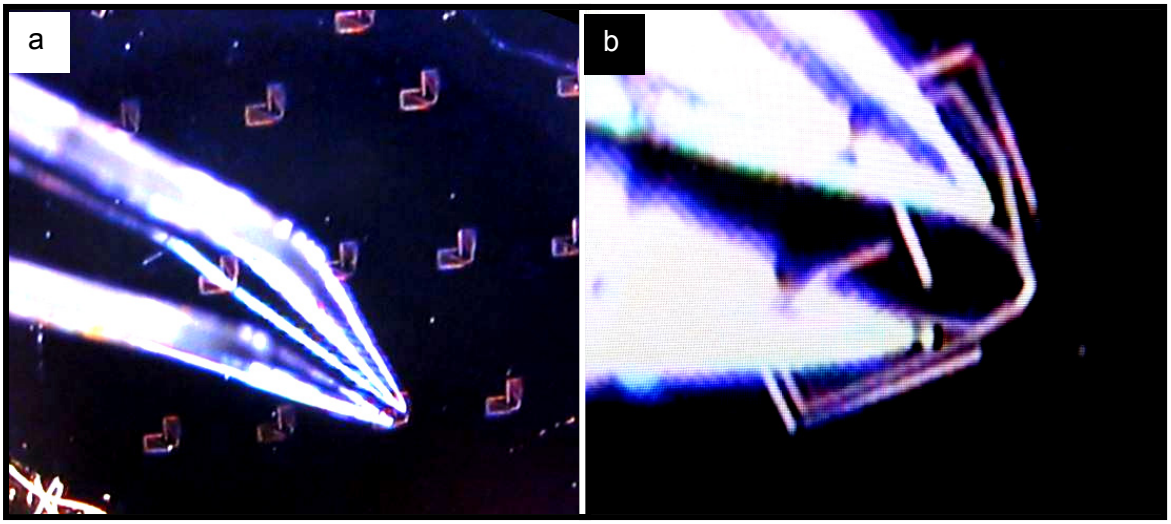


Figure 4-4: Bright-field optical images of the tungsten probes of the probe station on the gold electrodes.

In the software-based workspace of the Agilent analyzer, under 'diode test' the set-up of a 'junction *I-V*' was chosen. This set-up allows the instrument to measure the current as it sweeps the voltage across the structure. The software uses the current and voltage values to produce an *I-V* curve for the structure. A voltage sweep from 0 V to +5 V (with 50 mV steps) was applied across the contacts. Figure 4-5 is a representative voltage-current curve for selenium nanowires at room temperature. The following data, discussion, and explanation are merely an attempt to understand the preliminary results obtained from our experiments.

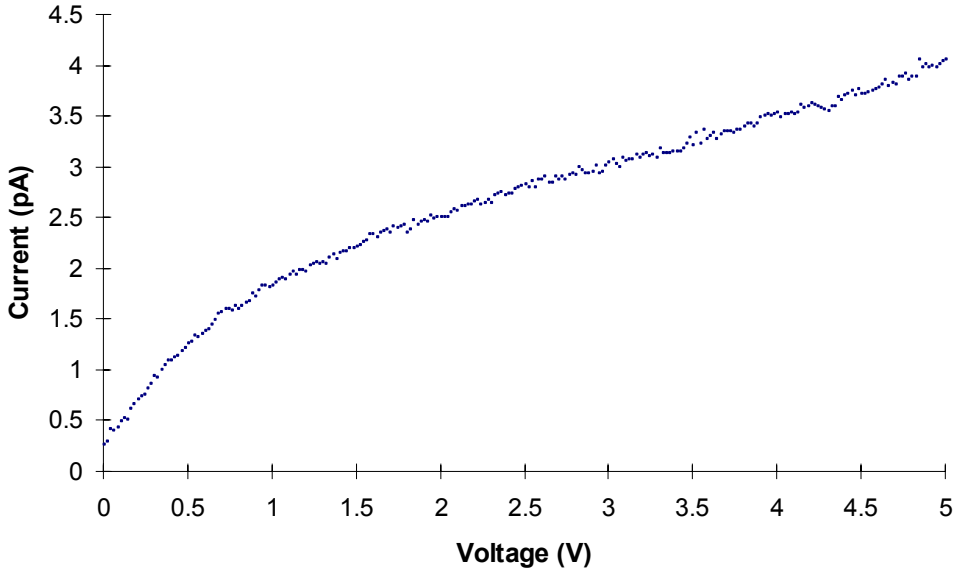


Figure 4-5: The current-voltage curve of selenium nanowires.

At least 10 conductivity measurements (i.e., complete I-V measurements) were obtained for each of the five sets of electrodes tested. The trend lines demonstrate the general agreement between these measurements. Experiments were also done to measure the *I-V* curves for two electrodes without the presence of any nanowire on the same silicon substrate. The later set-up was used to test for the presence of leakage current through the substrate. In this set-up, the two electrodes were placed at a similar distance apart as the electrodes that were overlaid onto the nanowires. This background measurement produced a horizontal trace with a peak-to-peak current of -0.15 fA to +0.15 fA. The offset from zero for the initial current through the selenium nanowires, as observed in Figure 4-5, could be attributed to a photocurrent from indirect lighting during these measurements. Although conductivity measurements were obtained for the selenium nanowires a question remains for how many nanowires were included within the measured devices. The next section addresses this question.

4.2.3 AFM and SEM Imaging of Selenium Nanowires

Scanning electron microscopy analysis indicates that the gold electrodes are overlaid onto a bundle of selenium nanowires. In Figure 4-6-a, the bundle of selenium nanowires seems uniform in terms of the number of nanowires between the two electrodes. However, at higher magnifications the SEM analysis (Figure 4-6-b to Figure 4-6-d) taken at various points between the two electrodes indicates otherwise. The number of nanowires in the bundle between the two electrodes is not uniform along the length of this bundle.

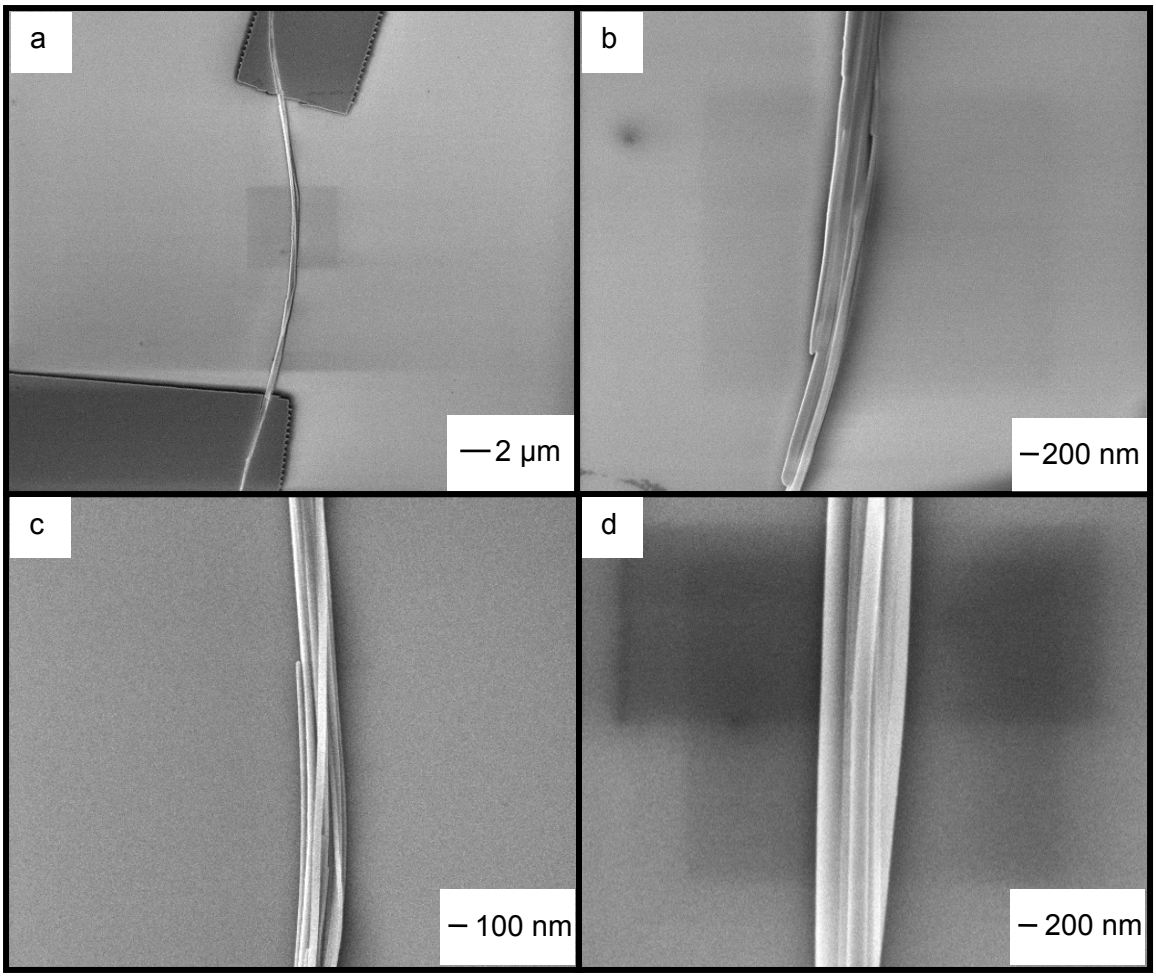


Figure 4-6: SEM images of selenium nanowires between the gold electrodes. These images depict the non-uniform number of nanowires bundled together at different points between the two electrodes.

From SEM images shown in Figure 4-6, it is difficult to get an approximate number of selenium nanowires in a bundle. In order to have a more clear perspective on the interpretation of the conductivity measurements for these nanowires it would be useful to know an approximate number of nanowires in the bundle. Atomic force microscopy (AFM) measurements were used to obtain a height profile for the bundle of selenium nanowires. The AFM images in were acquired using an MFP3D AFM (Asylum Research) equipped with a silicon cantilever (VistaProbes, model #: AC 240TS). The following AFM image (Figure 4-7) was acquired by tapping mode since this mode is less damaging to the bundle of selenium nanowires than contact mode imaging. As seen in Figure 4-7, the lateral spatial resolution of an AFM is limited by both the diameter of the AFM tip (typically >10nm) and the shape of the probe relative to the shape of the nanowire bundle. Height measurements are, however, accurate down to the sub-nanometer scale. Therefore, height profiles were taken at various locations along the structure to determine the approximate number of nanowires in the bundle.

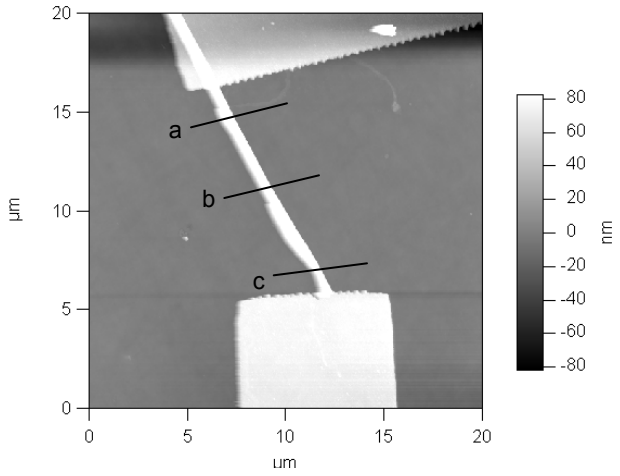


Figure 4-7: An image acquired by atomic force microscopy (tapping mode). Height profile measurements of the nanowire bundle were performed along the lines labelled a, b and c.

The height profiles taken at various positions along the selenium nanowire bundle are plotted in Figure 4-8. The peak height measured at three points along the bundle were 175, 155 and 130 nm, which correspond to measurements taken at positions a, b and c in Figure 4-7, respectively.

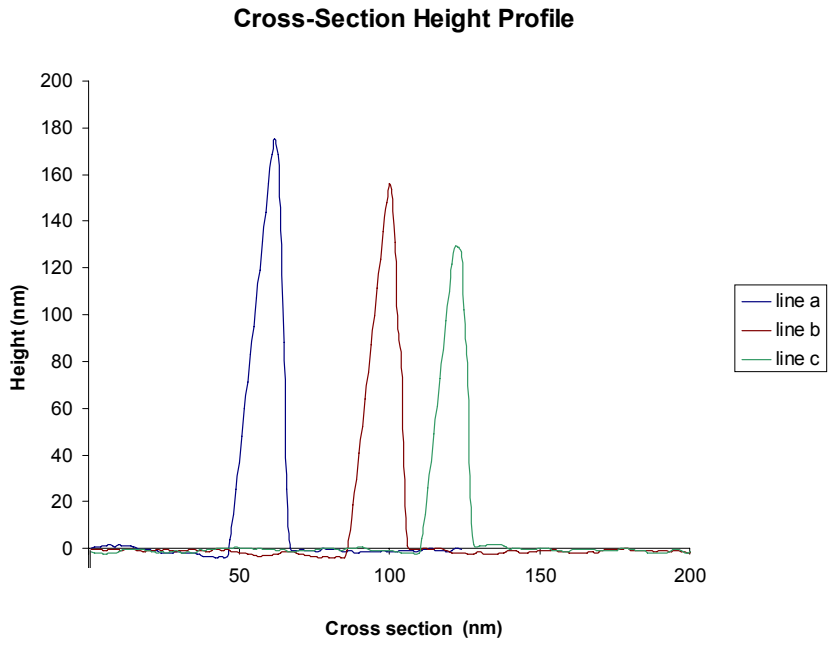


Figure 4-8: Height profile measurement of the selenium nanowire bundle across lines a, b and c as shown in Figure 4-7. The highest point of the bundle is 175, 155 and 130 nm along lines a, b and c, respectively.

From the SEM images and the AFM height profile data, it is estimated that the minimum number of nanowires per bundle is 5; however, we approximate between 5 to 15 nanowires could be bundled together for the samples studied in this thesis.

4.2.4 Assessment of the Set-Up of the Metal Electrodes and Resistivity Calculations

Calculation and Comparison of Electrical Resistivity of Fabricated Gold Wire vs. Bulk Gold

The selenium nanowires in the set-up were replaced with a micro-fabricated gold wire to assess the reliability of the electrical measurements from the nanowire bundles. A micron-scale gold wire (height: 85 nm; width: 0.5 μm, length: 30 μm) between the electrodes was fabricated by generating a pattern in the Raith EBL tool. The pattern of electrode and wire was exposed in a serial manner onto a resist coated substrate (details of which are as previously discussed in Section 3.4.2). An optical image of this test structure can be seen in Figure 4-9.

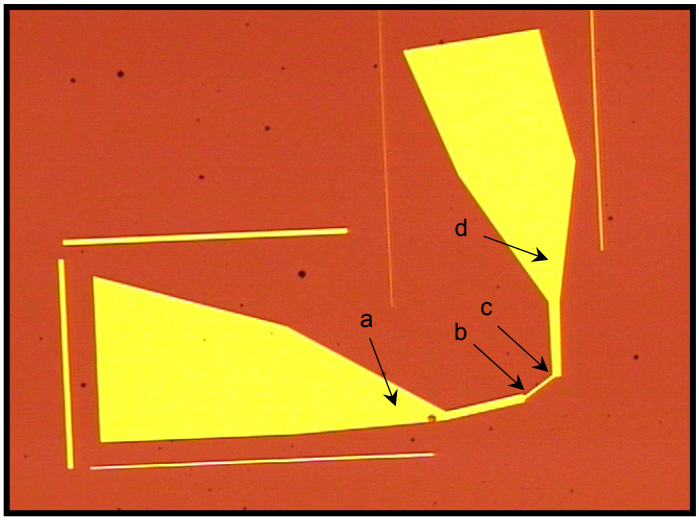


Figure 4-9: A bright-field optical image of the gold wire in between the two gold electrodes. Points 'a' and 'd' represent the approximate position of the tungsten probes of the probe station during the subsequent measurements. Points 'b' and 'c' represent the two ends of the gold wire.

In Figure 4-9, points labelled ‘b’ and ‘c’ represent the two ends of the fabricated gold structure and points labelled ‘a’ and ‘d’ are the approximate positions of the probes on the electrodes. The *I*-*V* curve produced from the measurement can be seen in Figure 4-10. Note that the maximum value of current that could be measured by the probe station for our set-up was 50 mA. As a result, the current values obtained at 1.5 V and higher are saturated as seen with the horizontal trace at 50 mA.

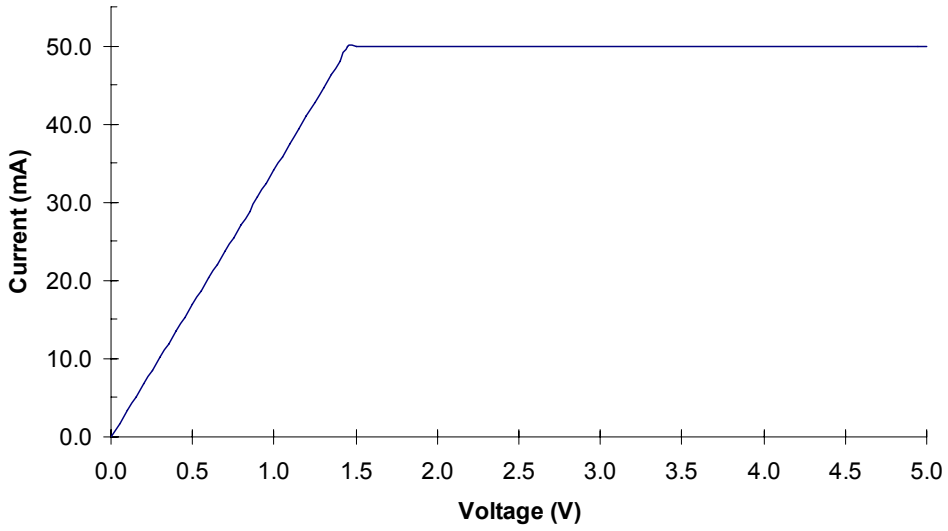


Figure 4-10: The current-voltage curve of a gold wire obtained using the probe station and the analysis system as shown in Figure 4-9.

For analysis, the electrical resistivity of the gold wire was calculated based on the value of resistance obtained from the *I*-*V* curve of the set-up shown in Figure 4-9. The calculated value of resistivity was then compared with that of bulk gold. Based on Equation 4-3, the resistivity of the fabricated gold wire, $\rho_{\textit{gold wire}}$, was calculated with the following set of data:

R : 30.02 Ω (calculated from the graph, $R = \frac{V}{I}$)

l: 30 μm (distance of the gold wire)

$A \sim 2.55 \times 10^{-13}$ m^2

The calculated value of $\rho_{gold\ wire}$ is 2.55×10^{-7} Ωm. The electrical resistivity of bulk gold ($\rho_{bulk\ gold}$) reported in the literature is 2.44×10^{-8} Ωm.[171] The calculated resistivity of the gold wire is very close to the value for the resistivity of bulk gold, confirming that the set-up is most likely producing reliable results. To ensure that the contact resistance of the tungsten probe with the gold film, R_{W-Au}, is not influencing our results, a model of 5 resistors in series was used as depicted in Figure 4-11. For this model the sheet resistivity of gold was used which was calculated based on the thickness of the thin film and the value of bulk gold resistivity.[172]

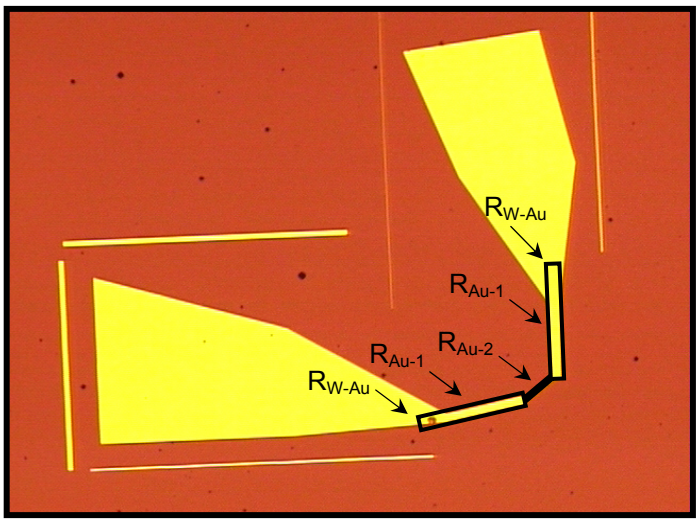


Figure 4-11: A schematic depicting the 5 resistors in series used for calculation of the contact resistance between the tungsten probe and the gold film.

The total resistance in the system, R_{Total}, is obtained from the addition of resistance between the tungsten probes and the gold electrodes at the two ends ($R_{W\text{-}Au}$); the resistance from the rectangular shaped part of the gold electrodes ($R_{Au\text{-}1}$) and the electrical resistance of the gold wire ($R_{Au\text{-}2}$) in between the gold electrodes (as labelled in Figure 4-11).

$$R_{Total} = 2R_{W-Au} + 2R_{Au-1} + R_{Au-2} \qquad \textbf{Equation 4-5}$$

The electrical resistance in Au-1 and Au-2 is further expanded using Equation 4-3.

$$R_{Total} = 2R_{W-Au} + 2\frac{\rho_{Au-1} \times l_{Au-1}}{h_{Au-1} \times w_{Au-1}} + \frac{\rho_{Au-2} \times l_{Au-2}}{h_{Au-2} \times w_{Au-2}}$$

Based on the value of bulk gold resistivity reported in literature (as mentioned earlier in the text) as well the experimental values obtained for the height of the gold layer, the following values can be substituted into the above equation.

$$\rho_{Au} = \rho_{Au-1} = \rho_{Au-1} = 2.44 \times 10^{-8} \Omega m$$
$$h_{Au} = h_{Au-1} = h_{Au-2} = 85 \times 10^{-9} m$$

Dimension of Au-1 block:

$$l = 120 \times 10^{-6} m;\ w = 5 \times 10^{-6} m$$

Dimension of Au-2 block:

$$l = 30 \times 10^{-6} m;\ w = 5 \times 10^{-7} m$$

From the equations above, the calculated resistance between the tungsten probe and the gold electrode is:

$$R_{W-Au} = 3.8\Omega$$

The value of the calculated contact resistance may be of importance for consideration in the measurement of the resistance of selenium nanowire bundle.

Calculation and Comparison of Electrical Resistivity of Selenium Nanowire Bundles vs. Bulk Selenium

The electrical resistivity of a bundle of selenium nanowires was estimated based on the data from the *I-V* curve shown in Figure 4-5 and the results from the SEM and AFM analysis of the nanowire bundles. A trend line for the data from *I-V* curve of Figure 4-5 is shown as an overlapping red line in Figure 4-12.

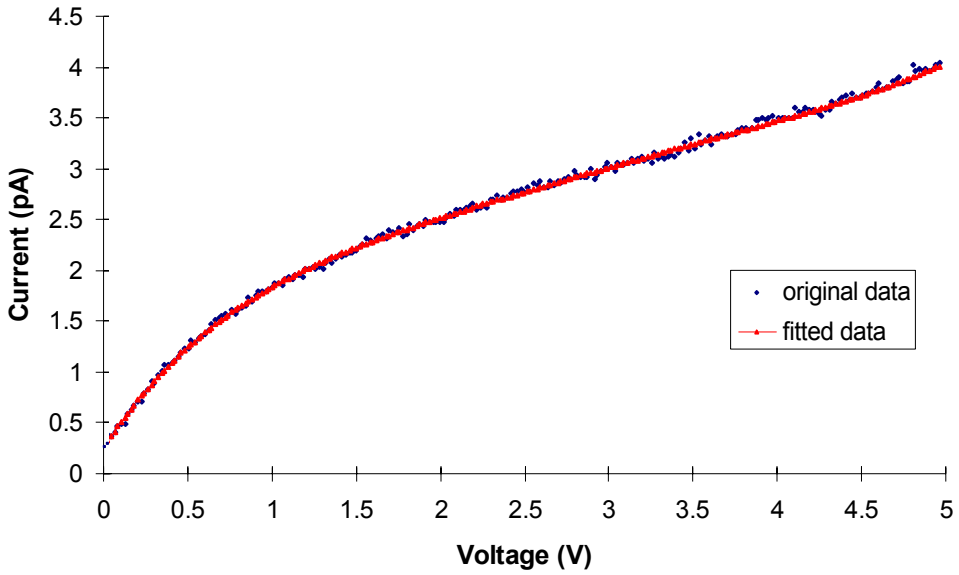


Figure 4-12: A current-voltage curve for selenium nanowires. The blue data points are the original data obtained from this measurement and the red line is a fit to this data, from which the other plots in this section are derived. The equation of this line is: $f(x)= 0.0044\ x^5 - 0.0670\ x^4 + 0.4103\ x^3 - 1.2793\ x^2 + 2.5189\ x + 0.2539$.

The derivative of the *I-V* curve was obtained from the equation of the fitted line. This derivative graph was used to plot the resistance versus voltage. From this plot, shown in Figure 4-13, the range of values of the resistance of the selenium nanowires can be obtained as a function of the applied voltage. More importantly, the resistance-voltage plot indicates the electrical conduction behaviour of these nanowires in the voltage range of 0 to 5 V that is more convoluted than that observed for bulk trigonal selenium.

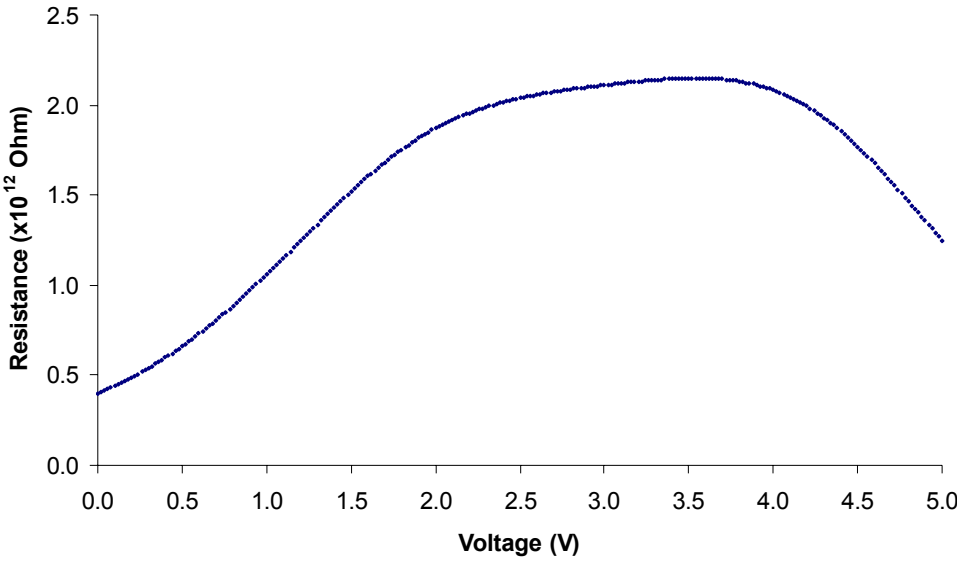


Figure 4-13: The resistance-voltage curve obtained from the reciprocal of the derivative of the fit to the *I-V* curve plotted in Figure 4-12.

To calculate the resistivity of the selenium nanowire bundle, the range of resistance was taken from the plot in Figure 4-13 and the length and smallest cross sectional area of the nanowire bundle was obtained from the results of AFM and SEM

imaging. The values required for the calculation (based on Equations 4-3 and 4-4) and the range of resistivity of these nanowires are as follows:

R : 4.7 $\times 10^{11}\,\Omega$ – 2.2 $\times 10^{12}\,\Omega$ (range obtained from Figure 4-13)

l ~ 30 μm (approximate distance of selenium nanowire bundle)

A ~ 2.04 $\times$ 10^{-14} m^2 (smallest cross sectional area: h : 130 nm; w : 160 nm)

$\therefore \rho_{\text{t-Se nw bundle}} = 10^2 - 10^3\ \Omega m$

Values obtained from the literature [173] indicate the following result:

$\sigma_{\text{bulk t-Se}} = 10^{-6}$–$10^{-5}\,\Omega^{-1}cm^{-1}$

$\therefore \rho_{\text{bulk t-Se}} = 10^3$–$10^4\,\Omega m$

As calculated in previous section (see page 142), the contact resistance (R_{W-Au}) of 3.8 Ω is very negligible compared to resistance of the nanowire bundle, which is in the range of 10^{11}-10^{12} Ω. Comparison of the electrical resistivity of the *t*-Se nanowire bundle with that of bulk *t*-Se is moderately different ($\rho_{\text{t-Se nw bundle}}$:$10^2 - 10^3$ Ωm vs. $\rho_{\text{bulk t-Se}}$:10^3–10^4 Ωm). The electrical resistivity in 1D nanostructures is expected increase relative to bulk materials due to an increased probability of electron scattering within the material. The photoconductive properties of selenium nanowires and the bulk has been studied in the past.[75] In our experiments, the considerably lower resistivity in *t*-Se nanowires could be partially due to the indirect lighting of the surrounding environment. Due to the location of the probe station at the time of the experiment, a completely dark room was not possible; however, attempts were made to block the light from the substrate at the time of measurement. It has, in fact, been reported in the literature that

the photoconductivity of selenium nanowires could be as high as $10^5\ \Omega^{-1}cm^{-1}$ ($\rho_{t\text{-}Se\ nw}$: $10^{-5}\ \Omega m$). [75]

There are many models for explaining the charge transport in semiconductors.[71] The conduction mechanism, for instance, in bulk selenium has been interpreted via a barrier model.[71] Based on this model, the carrier concentration in a selenium crystal is not uniform. A selenium crystal is composed of a non-uniform network of depleted layers that contains regions with a few carriers as well as non-depleted regions with more carriers.[71] At relatively low voltages (< 0.6 V) the conductivity is limited by the carrier concentration in the depleted layers. At relatively high voltages the conductivity increases because the applied potential is above a threshold to assist with injecting carriers from the non-depleted regions to the depleted layers.

The electron conduction in selenium nanowire bundles may involve a more complicated transport mechanism due to its confined dimensions. Our experimental observations based on preliminary results for electron conduction in selenium nanowires differ from that reported for bulk selenium crystals. These preliminary results suggest that a different mechanism, or one that is more convoluted, may exist for electron transport within the nanowires. The observed trend may be explained by a limited injection of the charge carriers. In a selenium nanowire, the number of carriers is much more limited than in a bulk crystal. It could be that in our measurements the carriers for charge transport approached a saturated concentration in the voltage range from 2 to 4 V. There were, therefore, not enough carriers for the current to increase proportionally with the increase in voltage. Another mechanism that may account for the trend observed from 0 to 4 V for conductivity of the selenium nanowire is a limited transport due to charge hoping[71] between nanowires through a path of least resistance rather than conductivity through a single nanowire. Injection is limited by charge hopping where

interfacial dipoles play a crucial role because they may alter the effective injection barrier. [71] At voltages higher than 4 V, the organic molecules between the nanowires within the bundle may be rearranging such that the tunnelling of the carriers can take place at a lower resistance. Neither these organic molecules or the selenium are irreversibly modified at voltages of up to 5 V, as roughly 10 cycles of the conductivity measurements were performed on the same selenium nanowire bundle without a noticeable change in the observed *I-V* curve. The mechanism of electron transport within these selenium nanowire bundles remains unclear, and remains the focus of future detailed analyses.

4.3 Conclusions and Discussion

We successfully obtained electrical measurements on selenium nanowires. To test the reliability of the electrodes and the set-up, we performed electrical measurements on gold structures that we fabricated on identical substrates. The results for gold nanostructures and bulk gold were comparable, suggesting that the obtained electrical measurements are most likely reliable. The resistivity values for selenium nanowires on the other hand are not conclusive, as the measurement was performed on a bundle and not one single nanowire. Selenium nanowires, regardless of numerous efforts as mentioned in Appendix A, formed bundles of an inconsistent number of nanowires, ranging from 5 to 20 for those with patterned electric contacts. Due to an inconsistent number of selenium nanowires within a bundle, further studies into the dispersion of these nanostructures is required.

CHAPTER 5: CONCLUDING REMARKS ON IMPACTS OF THIS RESEARCH

5.1 Final Conclusions and Implications of this Work

The continued miniaturization of electronics through the top-down approach is expected to reach fundamental physical limits. Therefore, significant efforts have been invested into the development of new functional materials and devices based on nanoscale building blocks via bottom-up approaches.[1-8] Semiconducting nanowires that can be electronically modified by addition of dopants to continually improve their electronic properties have been of particular interest. Hence, there is a need for an approach to overlay metal contacts on synthesized nanostructures without causing damage to them in a time and cost effective manner. As described in this thesis, using microscope projection photolithography techniques, such processing can be done on the bench top without requiring clean room facilities. This technique also minimizes the time spent, as there would be no need for prior alignment of the mask with the nanostructures on the substrate and a photomask can be reused for multiple samples. Also, use of UV light provides photons with much less energy compared with high-energy electrons from an electron-beam lithography tool. As mentioned previously, a lower energy method of patterning photoresist-coated nanostructures is preferred as electron-beam can damage nanostructures as shown in the literature. This technique has the capability to help improve the throughput for electrical investigations on 1D nanostructure. In fact, using the techniques and processes described in this thesis one can overlay electrodes on

nanostructures nearly a hundred times faster and a hundred times less costly than previously obtainable.

Recently, in the research community, major efforts have been put towards the synthetic control of one-dimensional building blocks and characterization of their properties. This tremendous increase in interest towards such materials is due to the unique properties and the potential applications that such materials present. Progress on the syntheses of nanowires of various materials has provided new components with optimized properties for incorporation into electronic and biochemical device fabrication.[149,150] A critical step towards more versatile devices using nanowires is the systematic control of their electronic properties through continual modification of such materials (e.g., via doping impurities). In fact, the extreme changes of electronic properties of carbon nanotubes [151,152] and semiconductor nanowires [153-155] by atomic or molecular doping were demonstrated recently. A systematic, general approach that is time and cost effective can be of high importance for the research community to overlay metal contacts on such nanostructures for their electrical characterization measurements in order to tune the electronic properties as these materials can be key components for future technological progress.

In this thesis, to measure the electrical properties of these nanostructures or to be able to simply incorporate them within electronic devices, two approaches were selected for positioning metal contacts on nanowires: i) microscope projection photolithography; and ii) electron-beam lithography. The fabrication process, which was developed for use with both techniques, required a fewer number of steps than previously demonstrated in the literature. This processing does not require aligning or assembling of nanostructures to features on the substrate, and there is no need for

substrate-specific pattern generation, whether it is printing a photomask or designing a pattern with software for EBL.

For the microscope projection photolithography technique, modifications were made to an optical microscope in order to place a photomask in the conjugate plane of field diaphragm for patterning purposes; however, more modifications are still required, as the final stages of the designed mask-holder could not position the photomask exactly at the required position. The limitation of the current mask holder design only allows pattern formation with lower resolution that may not be ideal for overlaying metal contacts on nanowires. In addition, an electron-beam lithography technique was utilized, following the developed fabrication process, to overlay patterns on nanostructures. Using this technique, gold metal contacts were successfully positioned on selenium nanowires. Finally, the conductivity of selenium nanowires was measured using a probe station.

Each of the techniques mentioned, MPP and EBL, has its own advantages and disadvantages; however, a number of advantages of MPP make it a much more practical technique for research laboratories. Microscope projection photolithography provides a much lower fabrication cost compared to electron-beam lithography as it requires a simple optical microscope, as opposed to an electron-beam writer with access to clean room facilities. MPP technique is a much faster approach to the fabrication of patterns as the exposure time is independent of the pattern size. This technique also allows examination of resist-covered nanostructures without exposure of resist if an optical filter is placed in the light path to prevent unwanted exposure of the resist to ultraviolet light. As for EBL, its limited throughput of samples makes this technique a major obstacle for production purposes in the microfabrication industry.[156] The limited throughput of this technique is due to serial exposure of the electron-beam and hence

the dependency of exposure time with pattern size. Another disadvantage of this technique, using the developed fabrication process, is that examining the sample for simultaneous alignment of the pattern with the nanostructure has to be done very rapidly (dependent on the magnification used for viewing ~3-5 s) as failure to do so will expose the entire area of resist visible in the field of view. However, this technique is capable of forming patterns of much smaller dimensions compared to the MPP technique. Overall, given the advantages and disadvantages of each technique, either technique could be employed with the developed fabrication process to incorporate and/or characterize nanostructures more rapidly than previously achieved in prior studies.

5.2 Future Directions of This Work

A number of one-dimensional materials could be used with this technique in order to gain better insight and tune their electronic properties. An excellent choice of materials is semiconducting nanowires, in particular selenium nanowires, due to their unique combination of useful properties. It is believed that photoconductivity properties of *t*-Se nanowires make these structures ideal candidates to be used for applications such as phototransistors, sensors, or tunable electronic interconnects.[75]

Photoconductivity of selenium nanowires can be measured as a function of wavelength. In such experiments, varying illumination intensities of irradiated light can be tested as well. UV-vis absorption spectra can help identify major electronic transitions for these structures. Similar to many other semiconductor systems, the bandgap of *t*-Se nanowires can be tuned with changing the dimension of the diameter. The diameter and length of selenium nanowires can be controlled by monitoring experimental conditions such as temperature during the synthesis.[75] Conductivity and photoconductivity

measurements can be performed on *t*-Se nanowires with varying diameter size, with or without surface modification or the presence of varying levels of dopants (positive or negative type). These measurements can be taken as a function of temperature and/or length of the nanowires. In order to measure conductivity as a function of length one can use conductive atomic force microscopy (cAFM) techniques. Using these techniques, an electrode can be attached to one end of the structure and the conductive tip of an atomic force microscope is scanned along the nanowire. It would be ideal to investigate the conductivity and photoconductivity of a single selenium nanowire rather than a bundle of nanowires to better understand some of the fundamental properties of these nanowires. Further investigation on the influence of various surfactants used to disperse the bundled nanowires may be of importance as well. Another experiment that would be important to carry out is the optimization of the electrical contacts on selenium nanowires. Various metals need to be investigated as the electrode material. In this thesis, measurements were made for the conductivity of selenium nanowire bundles using gold electrodes. However, a number of other metals could be chosen (e.g., Ag or Al) based on their work function and their relation with Fermi energy level of the selenium nanowire. The choice of metal as electrical contact is crucial as the metal electrode could be the source of the non-ohmic behaviour observed in the experimental section of this thesis. These measurements could also be performed on overlapping nanowires to test the possible current leakage between nanowires. The properties of selenium nanowires could be better enhanced for electronic applications by tuning their conductivity and photoconductivity by implementing the different strategies mentioned above. The ultimate goal of this research is to open up research avenues into nanowire-based circuits.

APPENDIX A: SYNTHESIS OF SELENIUM NANOWIRES

The synthesis of the selenium nanowires used for this work was based on the procedure outlined in a previous publication.[75] Below is a brief description on their synthesis and a number of images showing the partially dispersed selenium nanowires in various solvents. Final modifications for dispersion of selenium nanowires in ethanol were done by addition of surfactants through the work of Michael Wang, details of which will be published elsewhere.

The first step of this synthesis involved the formation of amorphous selenium (*a*-Se) colloids in an aqueous solution via the reduction of selenious acid with excess hydrazine. These *a*-Se colloids were then rinsed with 0 °C DI water. The next step was to suspend the selenium colloids in an isopropanol solution after which the selenium colloids were sonicated to induce growth via providing the energy to change the *a*-Se to the more stable *t*-Se form. The *t*-Se seeds start the growth process to form nanowires. As the produced nanowires are in an aggregated form, surfactants were then added for the dispersion of these nanostructures. A schematic depiction of these steps are presented in Figure A-1. It is important to note that in this synthesis, there are a number of important factors that affect the final product, some of which are: 1) choice of the concentration of each of the reagents; 2) the speed and order of mixing the two reagents; 3) the temperature at which the reaction takes place; 4) solvent choice for *a*-Se colloid dispersion; and 5) sonication time and power.

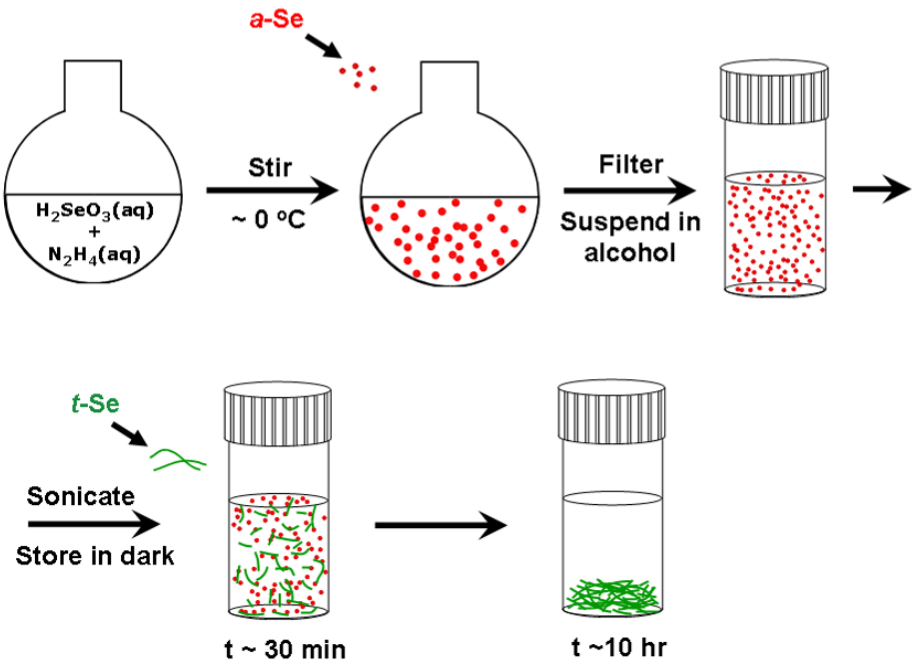


Figure A-1: A schematic depiction of the synthetic process for selenium nanowires.

Some of the optimized parameters used in synthesis of the selenium nanowires are as follows: 2.73 g of H_2SeO_3 (98% pure) was dissolved in 100 mL of water and 3 mL of hydrazine hydrate (50% hydrazine in water) was added drop-wise at ice-water temperatures as shown in Figure A-2-a. The mixture was vacuum filtered using a filter paper 15 min after addition of the last drop of hydrazine. The *a*-Se colloids formed were washed with ~300 mL of 0 °C DI water poured over the selenium colloids, and left to dry in a dessicator kept in dark overnight. The a-Se colloids were suspended in ethanol before sonication for 20 s at room temperature. After 12 h the formation of nanowires was completed.

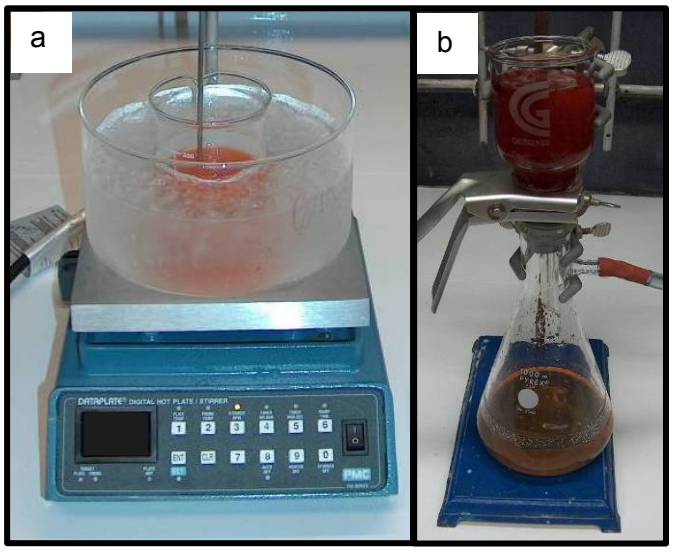


Figure A-2: Pictures depicting the set-up for synthesis of selenium nanowires. Image in (a) was taken during the reduction of selenious acid with excess hydrazine at ice-water temperatures and picture in (b) is of the isolation and purification procedure for a-Se colloids.

As seen in Figure A-3-a, the as synthesized selenium nanowires are aggregated and not ideal for patterning metal contacts for electrical measurements. Images shown from b→e of Figure A-3 show their partial dispersion in various solvents. It is crucial to disperse these nanowires further to make electronic measurements from individual nanowires. The dispersion of these nanowires will be pursued further in the future.

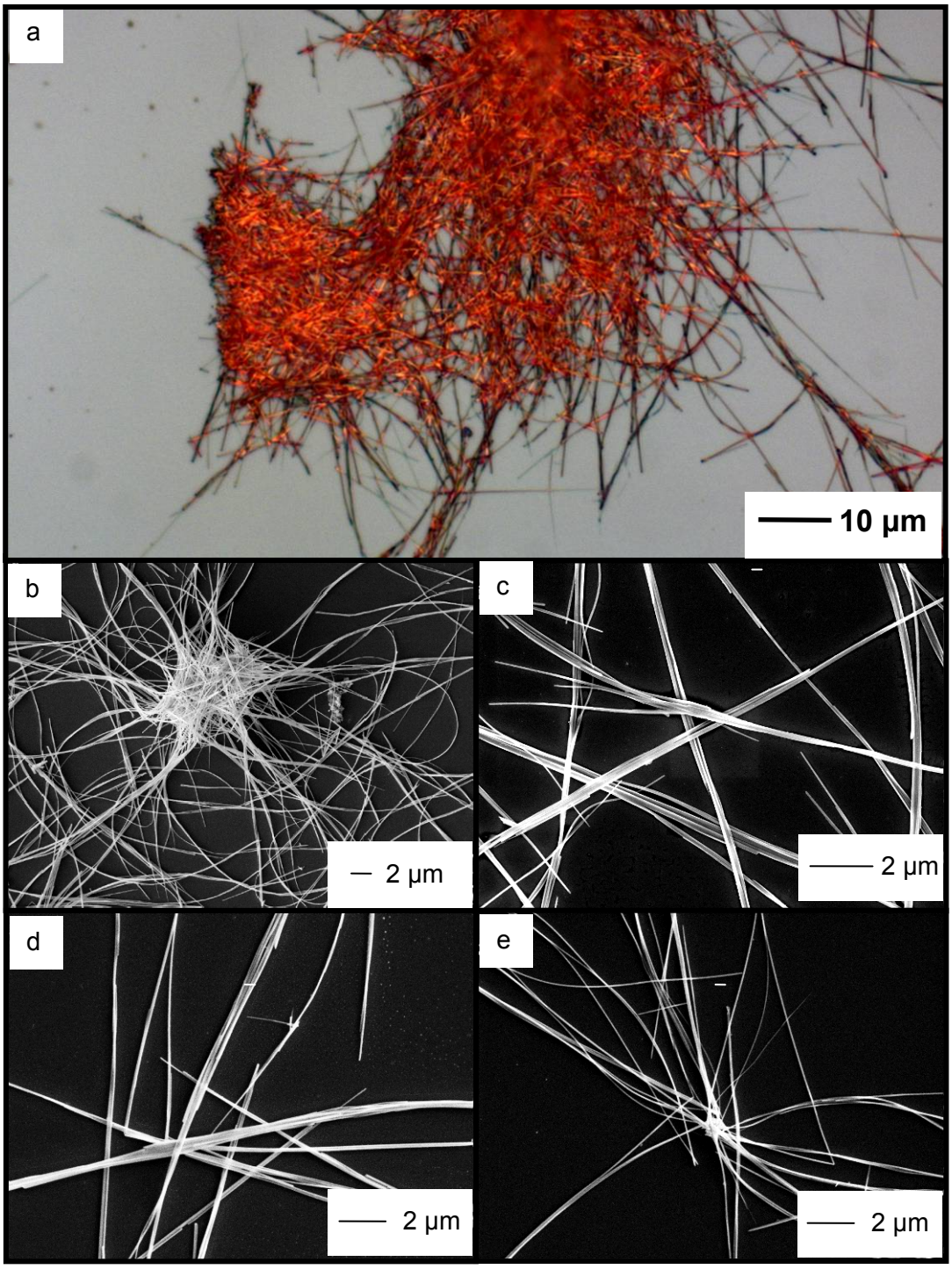


Figure A-3: A bright-field optical image of aggregated selenium nanowires shown in (a). Scanning electron microscopy images of selenium nanowires dispersed in isopropanol, chloroform, hexanes, hexadecane-thiol prior to drying is shown in (b), (c), (d) and (e), respectively.

APPENDIX B: METAL DEPOSITION BY THERMAL EVAPORATION

For the metal deposition Kurt J. Lesker Thermal Evaporator (customer installed) was used as seen in Figure B-1. As the substrate is held facing down, towards the source, as seen in Figure 2-18 the substrate needs to be fixed in position on the sample holder not to fall off. Since various kinds of tape do not hold the silicon chip at high temperatures under vacuum, vacuum grease was put at the back surface of silicon chips to stick the sample to the holder. Once the sample was in place, the chamber was put under vacuum to ~1 x 10^{-7} Torr.

Chromium is the first metal to be deposited as it acts as an adhesive layer between silicon oxide and gold. It is generally suggested to deposit ~5 nm of chromium as an adhesive layer. When using the Lesker evaporator the current output should slowly increase to reach a maximum of 15% to achieve a deposition rate of roughly 0.5 Å/s of chromium given the kind of crucible that is used to hold the chromium metal. After chromium deposition, the source target is switched to gold and slowly the current output is increased to 35% to achieve a deposition rate of roughly 0.5 Å/s. The thickness of the gold deposited varied between different experiments as noted in the main text.

Figure B-1: A picture of Kurt J. Lesker thermal evaporator used in the 4D LABS cleanroom facility.

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(67) In semiconductor physics, the band gap of a semiconductor is always one of the two following types: i) a direct band gap; or ii) an indirect band gap. For materials with a direct band gap, a photon excites an electron from the valence band to the conduction band. This electron will subsequently shift from the lowest-energy state in the conduction band to the highest-energy state in the valence band without a change in momentum. For materials with an indirect band gap, almost all of the energy for electron excitation comes from incident photons, while almost all of the momentum comes from a phonon through a relaxation process within the conduction band. Upon relaxation the electron cannot directly transition from the lowest-energy state in the conduction band into the highest-energy state in the valence band without a change in momentum.

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