March 28, 2023 Letter of Transmittal

Dr. Mike Hegedus School of Engineering Science, Simon Fraser University, Burnaby, B.C. V5A 1S6



#### **RE: ENSC 405W Project Proposal for SyncLock DLA**

Dear Dr. Hegedus,

Please find attached a copy of a project proposal prepared by SyncLock for ENSC 405W/440. It outlines the high-level overview of a digital lock-in amplifier (DLA) that we will develop. This device will be characterized by high portability, low power consumption, and flexible signal parameter setting.

This document will outline the background and scope of the project, its risks and benefits, and an analysis of its market and its competitiveness with other similar products. This proposal also details the cost of the project, the source of funding, and the plan for each phase of the project. Finally, it will provide a brief introduction to our team.

SyncLock consists of six senior engineering students with a diverse range of specializations: Ese Dan-Aighewi, Minghui Liang, Brayden McKeen, Lucien Somorai, Yupeng Zhao, and Haoran Zhou.

Thank you for taking the time to review our final proposal document for digital lock-in amplifiers. Should any questions or concerns arise, please do not hesitate to contact our Chief Communication Officer, Ese Dan-Aighewi, by email (adanaigh@sfu.ca).

Sincerely,

Ese Dan-Aighewi Chief Communication Officer SyncLock



# **Digital Lock-In Amplifier**

### Final Proposal Document

SyncLock (Company #8)

Simon Fraser University ENSC 405W - Capstone A

March 30, 2023

### **Sponsor:**

Intelligent Sensing Laboratory **Supervisors:** Dr. Behraad Bahreyni, PEng Dr. Fatemeh Es.haghi

### Members:

Ese Dan-Aighewi Minghui Liang Brayden McKeen Lucien Somorai Yupeng Zhao Haoran Zhou

## **Executive summary**

A lock-in amplifier is a very widely used instrument in the field of scientific research and development laboratories, which is used to detect small signals. With the development of digital technology, signal processing in lock-in amplifiers can be performed using digital signal processing systems, which are called digital lock-in amplifiers. Our goal is to create a digital lock-in amplifier with high portability, low power consumption, and flexible parameter settings.

The digital lock-in amplifier is mainly composed of the following five parts: a pre-amp, an analog-to-digital converter (ADC), a direct digital synthesizer (DDS), a microprocessor, and a digital-to-analog converter (DAC). The input signal first enters the preamp to adjust the amplitude of the input signal and then enters the ADC unit to convert the input signal into a digital signal. The "lock-in" processing of the digital signal is in the microprocessor. Finally, the processed digital signal enters the DAC to convert the signal into an analog signal again. The DDS mainly provides a reference signal to the microprocessor as one of the steps in the "lock-in" processes in the microprocessor. All these parts in the prototype will be combined together in a PCB.

The market for lock-in amplifiers is relatively small and highly specialized and estimated to be around \$25.4 million in 2022, projected to reach \$32.2 million by 2030, with the digital segment projected to be around \$20.9 million by 2030. While several top companies manufacture lock-in amplifiers, there is a market vacancy for highly portable digital lock-in amplifiers. SyncLock's product is uniquely suited for both field and lab use due to its small size, low power consumption, and lower cost than other devices.

We expect to complete the proof of concept by April 13th. The estimated total development cost will not exceed \$560, including proof of concept and prototype development. We plan to start the development of the prototype of the device on April 27<sup>th</sup> and continue until the end of the next semester to complete the prototype development. It will bring better convenience to scientific research and engineering applications.

# **Table of Contents**

Executive summary	
Table of Contentsii	i
List of Figures	i
List of Tablesiii	i
Glossaryiii	i
1. Introduction 1	L
2. Project Overview 1	
2.1 Background1	L
2.2 Scope	;
3. Product Justification	;
3.1 Risks	;
3.1.1 Electric shock	;
3.1.2 Hardware Issues	ł
3.1.3 Software Issues4	ł
3.1.4 Use Cases	ł
3.1.5 Device heating	ł
3.2 Benefits 4	ł
3.2.1 Portable	ł
3.2.2 Data Storage	;
3.2.3 Cost	;
3.2.4 Safe	;
3.2.5 Reliable	;
3.3 Market	;
3.4 Competition	5
4. Finances	3
4.1 Costs	3
4.2 Funding	)
4.2.1 The Engineering Science Student Endowment Fund (ESSEF):	
4.2.2 Wighton Engineering Development Fund	)
4.2.3 The Intelligent Sensing Laboratory	)
4.2.4 Personal Funding10	)
5. Project Planning	)
5.1 Proof of Concept Development:	L
5.2 Prototype Development:	
6. Company Overview12	2
7. Conclusion	
8. References	Ĵ

# **List of Figures**

Figure 2.1a: Principle of signal "lock-in"	2
Figure 2.1b: Digitalization of signal "lock-in"	2
Figure 5.1a: First half of the Gantt chart showing the project tasks	
Figure 5.1b: Second half of the Gantt chart showing the project tasks	

## **List of Tables**

6
7
8
8

# Glossary

Term	Definition	
ADC	Analog-to-Digital Converter	
DAC	Digital-to-Analog Converter	
DC	Direct Current. A signal which exhibits either positive or negative values	
DDS	Direct Digital Synthesis, to generate reference signal	
DLA	Digital Lock-In Amplifier	
DSP	Digital Signal Processing	
PCB	Printed Circuit Board	
Preamp	Preamplifier, amplifies input signal for processing by ADC	
Raspberry Pi	Single board mini computer, running on Linux	

## **1. Introduction**

A digital lock-in amplifier (DLA) is an amplifier that uses a digital signal processing (DSP) system to extract signals with known carriers from extremely noisy environments. It is a very widely used instrument in the field of scientific research and development laboratories. Lock-in amplifiers were invented in the 1930s and commercialized in the mid-20th century as electrical instruments capable of extracting signal amplitudes and phases in extremely noisy environments [1]. It brought a great breakthrough in the technology responsible for detecting weak signals. Today, with the development of digital technology, signals can be processed using digital signal processing algorithms, which greatly compensates for the shortcomings of analog multipliers in traditional lock-in amplifiers that are prone to harmonic distortion and thermal shifts [2].

The SyncLock team accepted an offer from Dr. Behreyni and his Intelligent Sensing Laboratory (ISL) to create a small digital lock-in amplifier with high portability, low power consumption, and flexible signal parameter settings. It has the functionality of a normal digital lock-in amplifier; the input analog signal will be converted by an onboard ADC to a digital signal. The digital signal will then be "locked in" in the DSP, and the output digital signal will be converted by the DAC into an analog signal. All its parts will be combined together on a PCB board, and it will be similar in size to a cell phone. It can not only work with a computer but also work independently for two to three days with the parameters preset on the computer and store the data in the SD card.

The purpose of this proposal is to provide a high-level overview of our product and prototype, outlined below in the project overview section. Following that, the risks and benefits of the product, the analysis of the product's market, its competitiveness, its cost, and a timeline for each phase of the product will be discussed.

## 2. Project Overview

### 2.1 Background

The core concept of a lock-in amplifier is "lock-in". The principle of "lock-in" is shown in figure 1 below. The input signal contains the target signal and other unwanted noises. The reference signal is a cosine with a frequency matching that of the target signal. Two mixers multiply the input signal with the reference signal or phase-shifted reference signal. The mixing operation will create two different components:  $f_s - f_r$  and  $f_s + f_r$ .  $f_s$  is the input signal frequency and  $f_r$ 



is the reference signal frequency. Finally, low pass filters are used to remove the  $f_s + f_r$  component and the  $f_s - f_r$  component remains untouched. The two lowpass filters output the in-phase and the quadrature components of the target signal, represented as X and Y in the figure respectively. Based on X and Y, amplitude (R) and phase ( $\theta$ ) can also be calculated.

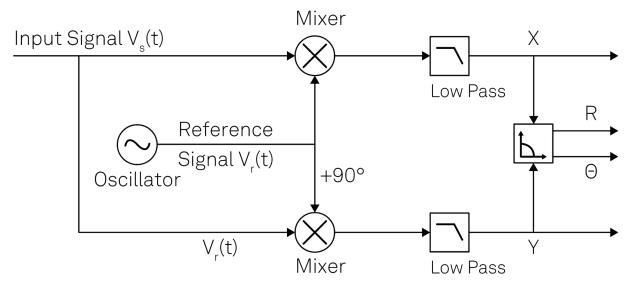


Figure 2.1a, Principle of signal "lock-in" [1]

In our DLA, the "lock-in" principle is applied in the digital domain. As shown in figure 2, the analog input signal is first converted into a digital signal by an analog-to-digital converter (ADC). Then, mixing and filtering operations are performed digitally as described above. Bringing the signal processing into the digital domain reduces the design complexity and makes the device more configurable.

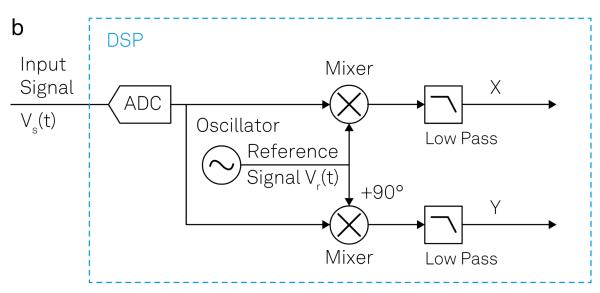


Figure 2.1b, Digitalization of signal "lock-in" [1]

### 2.2 Scope

In this section, we will introduce the project scope from three perspectives: goal, tasks, and deliverables.

The main goal of this project is to create a DLA device that satisfies the requirements of our clients: Dr. Behraad Bahreyni and his research team. Moreover, this device can also fill the absence of portable, long battery life and configurable lock-in amplifiers in the market.

The project tasks consist of parts selection, assembly, UI design, and testing. In the part selection, our company will select appropriate electrical components from the market by considering their performance, cost, and delivery time. In the assembly phase, the purchased components are connected and assembled together. We need to make all components communicate with each other with no error at a hardware level. UI allows users to control our device, our computer engineers will create a user-friendly interface and integrate the interface with the electrical components. In the end, we need to perform various tests to make sure the device works as expected and make sure our clients can operate it as well.

The project has two deliverables, the first one is showing the proof-of-concept in April 2023, and the second one is showing the prototype in August 2023. In the proof-of-concept stage, the company will use less strict requirements to show the concepts of extracting signals from noisy environments and amplifying the extracted signal according to the user settings. In the prototype stage, we will follow all requirements strictly and also mount all electrical components to a PCB to create a more formal device.

# **3. Product Justification**

### 3.1 Risks

There are numerous risks that we are aware of with this product which include societal and business risks. However, we do not see any significant safety hazards that are a threat to the user or the team when using the product. Therefore, most of the risks outlined below are worst-case scenarios pertaining to our user market and the product itself.

### 3.1.1 Electric shock

Since we are designing and working with electronics, there is the risk that electric shock might occur from environmental features. Since this device will be taken to the field, rain might be a cause of this risk and needs to be addressed. We can alleviate this risk by making sure our casing



for the device is waterproof and has been thoroughly tested in all conditions. This will prevent electric shock from occurring, allowing the user to operate the device safely.

#### 3.1.2 Hardware Issues

The device will have a total of 6 different hardware components within the PCB allowing for the risk of error. Preventing this will be challenging as we would need to thoroughly test each component individually and then do the same thing by combining everything together. Even though we will go through this process, issue-free hardware cannot be guaranteed.

### 3.1.3 Software Issues

The device will have a user interface allowing the user to control different parameters. Numerous errors might occur between the interaction with the hardware and software of the device. We will do thorough testing here as well hoping no issue will be presented by the device.

### 3.1.4 Use Cases

The device will primarily be used by Dr. Behraad Bahreyni. Keeping this in mind, this product was solely designed to meet his requirements of how he wanted the product to work. Therefore, this product might not suit everyone's requirements concerning input channels, output channels, and adjusting parameters for the reference signal.

### 3.1.5 Device heating

Again, since we are working with electronics, there is the risk of electric shorts which might make the product very hot to touch, burning the users' hands. On top of that, a fire might break out depending on how hot the device gets. This will be prevented as we try to keep the power requirements to a minimum.

### **3.2 Benefits**

This device will provide benefits that will out way the potential risks. Moreover, the device is useful, which means both our team and the users will reap the benefits.

### 3.2.1 Portable

Compared to existing lock-in amplifiers, this device will be much smaller and more portable to carry around. It will be similar to the size of a phone and can be taken to a field as there is a case that surrounds the PCB. If needing to work at a lab, this device is not as bulky as it takes up limited space when running simulations.



### 3.2.2 Data Storage

The device will allow users to store their data via an SD card where they can analyze and process the data later. Existing lock-in amplifiers do not have this functionality making our product unique and useful.

### 3.2.3 Cost

Our device will cost much less than other lock-in amplifiers making it more affordable for lab users and researchers. This allows them to purchase multiple devices if they need to collect data in multiple settings.

### 3.2.4 Safe

The team has kept safety as our biggest priority when designing the device and can assure that the product is safe for all users. Additionally, no protective equipment will be needed when handling the device.

### 3.2.5 Reliable

With regard to testing, the team has spent hours testing the product within the team and will test extensively with real-world users. This product will be guaranteed to work without errors providing the data the users need.

### 3.3 Market

Lock-in amplifiers are widely used in scientific research and engineering applications that require the detection of weak signals buried in background noise [1]. They are commonly classified based on their operating frequency range and the adopted signal processing technique [1, 3]. The solution offered by SyncLock is a digital lock-in amplifier that targets signal frequency in the low radio-frequency range, which ranges from a few kilohertz to hundreds of kilohertz. It features flexibility on signal parameter adjustment, and it is portable such that users can carry it to fields for signal measurement.

The market for lock-in amplifiers is relatively small but highly specialized. Several top companies that design and manufacture lock-in amplifiers include Zurich Instruments, Stanford Research Systems, Liquid Instruments, and others. In the year 2022, the global market for lock-in amplifiers was estimated at US\$25.4 Million. It is projected to reach US\$32.2 Million by 2030. Among the entire lock-in amplifier market, the digital segment is projected to reach US\$20.9 Million by the end of the analysis period from 2022 to 2030 [4].



It is difficult to estimate the market share of digital lock-in amplifiers as no publicly available data on the lock-in amplifier market based on its classification has been found. However, as digital lock-in amplifiers offer higher measurement precision and better signal-to-noise ratios relative to traditional analog lock-in amplifiers, the market trend is expected to shift focus toward the digital side.

The market for lock-in amplifiers is primarily driven by the demand for scientific research from the technology and engineering sectors [1]. Studies involving detecting and analyzing the emitted small signals to gain better insight into the system's behavior exhibit the most demand for lock-in amplifiers. Its market is expected to grow in the coming years as the demand for signal detection increases across various fields of study.

The primary client of SyncLock is the Intelligent Sensing Laboratory (ISL) based in Simon Fraser University's (SFU) Surrey campus. ISL's research is focused on developing algorithms and systems for sensing applications. While the client has lock-in amplifiers capable of measuring signals up to 600 MHz at their disposal, they still find a need for small, portable digital lock-in amplifiers with low power consumption and flexibility in signal parameter settings.

### **3.4 Competition**

Apart from offering higher measurement precision and greater flexibility than their analog counterpart, digital lock-in amplifiers are also more user-friendly. They typically come with software that allows users to easily control signal parameters and perform further data analysis. Altering the reference signal parameters and the lowpass filter characteristics is easier when the signal processing is implemented digitally.

Some of the common digital lock-in amplifier products currently on the market include the MFLI, UHFLI, and UF2LI models manufactured by Zurich Instruments, as well as SR810 and SR830 manufactured by Stanford Research Systems [5, 6]. These amplifiers are heavy, large, and designed specifically for use in laboratory settings. The following table lists the weight, dimensions, required power supply, and power consumption for these models. This leaves a market vacancy for digital lock-in amplifiers with high portability, which SyncLock aims to fill in. The first row of the table lists SyncLock's general specifications for comparison.

Model	Weight (kg)	Dimension (cm)	Power Supply (V)	Power Consumption (W)
DLA (SyncLock)	<0.2	16 x 9 x 3	9 V (DC)	<1



MFLI (Zurich)	3.8	28.3 x 23.2 x	12 V, 2 A (DC)	40
		10.2	100 - 240 V	
			(AC)	
UHFLI (Zurich)	6.4	45 x 35 x 10	100 – 240 V	NA
			(AC)	
HF2LI (Zurich)	6.2	45 x 35 x 10	100 – 240 V	NA
			(AC)	
SR810 (SRS)	10.4	50 x 43 x 13	100 - 240  V	40
			(AC)	

Table 3.4a: Comparison of dimension and power specifications.

SyncLock's digital lock-in amplifier has a smaller size, lower power consumption, and lower cost than any other device currently offered, making it portable and uniquely suited for both field and lab use. This is made possible by sacrificing bandwidth. The following table lists some of the specifications for comparison [5, 6].

Model	Number of Input	Frequency	SNR	Cost
	Channel	Range		
DLA	2	Up to 200 kHz	Around 100 dB	\$800
(SyncLock)				
MFLI (Zurich)	2	DC to 500 kHz,	Up to 135 dB,	\$6470
		can be upgraded	decrease with	
		to 5 MHz	increasing	
			frequency	
UHFLI (Zurich)	2	DC to 600 MHz	Up to 147 dB,	Starting at
			decrease with	\$45000
			increasing	
			frequency	
SR810 (SRS)	1	1 mHz to 102.4	>100 dB	\$4250
		kHz		

Table 3.4b: Comparison of signal inputs specifications and costs.



# 4. Finances

### 4.1 Costs

The cost of each component and the total cost of the proof-of-concept and prototype are outlined in the tables below.

Component	Quantity	Cost (CAD)	
Raspberry Pi	1	Provided by Intelligent Sensing Laboratory	
AdaFruit ADS1115 ADC	1	\$20.63	
Atmel MCP3008 ADC	1	\$4.50	
Atmel MCP4812 DAC	1	\$4.40	
Pre-Amp	1	\$5.00	
Jumper cables Bulk \$15.00			
Total + Tax (12%) + Shipping (\$10.00) = \$65.47			

Table 4.1a: Estimates of Proof- Of Concept Costs

Component	Quantity	Cost (CAD)
Microcontroller	1	\$30.00
SD Card Controller	1	\$6.00
SD Card	1	\$10.00
USB module	1	\$30.00
РСВ	1	\$100.00
Testing Probes	4	\$15.00
Casing	1	\$50.00
Lithium Batteries	1	\$15.00
DDS	1	\$30.00

LEDs	2	\$1.00	
Amplifiers, Resistors, Capacitors	Bulk	\$30.00	
LTC2353HLX ADC	1	\$80.00	
DAC8830 DAC	1	\$20.00	
Total + Tax (12%) + Shipping (\$20.00) = \$487.00			

Table 4.1b: Estimates of Prototype Costs

The combined cost of the entire project is \$552.50

### 4.2 Funding

After performing a cost analysis to develop the product, the SyncLock team has decided to consider various sources of funding to cover these costs. The funds shall be used to design and build the proof-of-concept and prototype of the DLA and will all be spent on purchasing the required components.

### 4.2.1 The Engineering Science Student Endowment Fund (ESSEF):

The Engineering Science Student Endowment Fund is provided each semester by the Engineering Science Student Society to provide money and equipment for projects. The DLA falls into Category C – "Class" since our project is primarily intended for use in the Intelligent Sensing Laboratory at SFU Surrey. The team meets the GPA and credit requirements for eligibility and will apply for the fund at the start of the Summer 2023 semester.

### 4.2.2 Wighton Engineering Development Fund

This is a competitive fund managed by Dr. Andrew H. Rawicz, to provide money for practical projects. The team shall submit a proposal outlining the project description and market, as well as the qualifications of all members of the team.

#### 4.2.3 The Intelligent Sensing Laboratory

Dr. Behraad Bahreyni from the Intelligent Sensing Laboratory has provided Raspberry Pi for the development of the proof-of-concept and has offered to cover a few expenses needed for the prototype stage of the DLA. The receipts from purchasing components shall be sent to him for consideration.



### 4.2.4 Personal Funding

In the case that the above funding sources are unavailable, the team is ready to foot the cost of development. Each member shall contribute \$92.00 to make up \$552.00 in total.

## 5. Project Planning

The figure below shows a timeline of the tasks completed for the DLA project, in the form of a Gantt chart. The horizontal bars on the chart show the duration of each component, from start to finish.

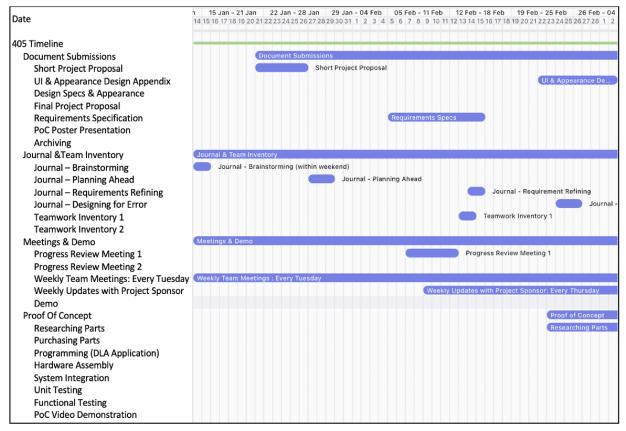


Figure 5.1a: First half of the Gantt chart showing the project tasks

Project planning was a bit off schedule since the initial project ideas could not be finalized on time before the first progress review meeting. However, the Digital Lock-in Amplifier was chosen after discussing with the project sponsor, Dr. Behraad Bahreyni, from Intelligent Sensing Laboratory. Planning started after February 9<sup>th</sup>, and several meetings were scheduled to discuss the project requirements and expectations.



Figure 5.1b: Second half of the Gantt chart showing the project tasks

### **5.1 Proof of Concept Development:**

Development of the proof of concept was slated to begin on February 28<sup>th</sup>, however, there were more meetings scheduled with the project sponsors to finalize what parts and components will be used to ensure that all the important requirements necessary to build the DLA are met. The parts were purchased on March 9<sup>th</sup> instead and development began on March 15<sup>th</sup>. The development process was a bit slow at the start due to the lengthy design documents, but it picked up right after that was complete.

Software and hardware development will be done in parallel, along with unit testing on all the individual components of the DLA proof of concept. System integration will occur before the final testing of the device in preparation for the poster presentation and final demo on April 13<sup>th</sup>.

### **5.2 Prototype Development:**

Plans and projections for the DLA prototype will begin on April 27<sup>th</sup> and will continue into the next semester during ENSC440 (Capstone B).



### 6. Company Overview



"We here at SyncLock strive to make nano sensing technologies portable, affordable, and flexible"



# Ese Dan-Aighewi - CCO

I am currently a 5th-year Computer Engineering student with an interest in digital logic design and hardware programming. I also enjoy user interface and experience design, as well as software development. Along with my technical skills, I have also amassed a wide range of soft and transferable skills from previous co-op opportunities and team projects.

-Ese Dan-Aighewi

#### **Experience and Expertise**

Firmware User Interface

Roles

- > Software Development
- > UI/UX Design
- > Soldering

> Hardware Programming & Design



# Lucien Somorai - CTO

I am a Computer Engineering Student interested in software development, machine learning, and AI. I also enjoy designing and programming hardware. *-Lucien Somorai* 

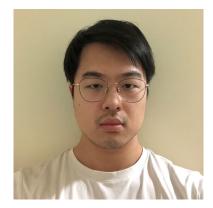


#### **Experience and Expertise**

Roles

- > Hardware Design & Programming
- > Software Development

Firmware User Interface



#### Roles

Firmware User Interface

# Haoran Zhou - CFO

A computer engineering student interested in embedded devices and neural networks.

-Haoran Zhou

### **Experience and Expertise**

Software Programming in C/C++ and Python
 Experience in HLS, CUDA and neural networks



# Yupeng Zhao - CEO

I am in Engineering Physics and this is my 6th year of study. The previous course experience around analyzing waves and harmonics laid the foundations for the signal processing involved in building a lock-in amplifier. In SyncLock, I primarily focus on firmware programming. -Yupeng Zhao



#### **Experience and Expertise**

- > Operating electronic laboratory equipments
- Programming in C++ and Python
- > Electronic Circuit Design

Firmware Schematic PCB

Roles



# Minghui Liang - CIO

I am currently a 5th-year Electrical Engineering student interested in circuits, robotics, and image processing. -Minghui Liang

#### Roles

Schematic PCB

#### **Experience and Expertise**

Circuit Design, Testing, and 
 Debugging

> Soldering

- PCB Design and Assembly Software Programming in
- C++ and Python



# **Brayden McKeen - COO**

I am currently in my 7th year at SFU studying electrical engineering. My extra years of study have been mostly spent in various co-ops providing me with a wealth of experience in designing and manufacturing circuits and custom PCBs. I am particularly interested in automotive systems and technologies, especially from an electrical and mechanical point of view. *-Brayden McKeen* 



Roles

- > Schematic and PCB Design >
- Circuit Design, Simulation, 
  Prototyping, Testing, and Debugging
- PCB Assembly and Rework Mechanical Design and Fabrication

**Experience and Expertise** 

Schematic PCB Mechanical

### 7. Conclusion

The SyncLock team is developing a digital lock-in amplifier for use in research and development in the fields of science and engineering. More specifically, this device is being designed for Dr. Behreyni and his Intelligent Sensing Laboratory.

Current and potential funding streams include the Engineering Science Student Endowment Fund, the Wighton Engineering Development Fund, funding from the Intelligent Sensing Laboratory, as well as internal funding from within SyncLock.

SyncLock's DLA benefits over similar analog systems by providing beneficial noise reduction characteristics, as well as providing the ability to configure system parameters such as target frequency. Current analog solutions require complete redesigns each time a new target frequency needs to be detected. SyncLock's DLA also benefits over other competitors' digital lock-in amplifiers by offering a portable package far better suited for field use, as well as significantly better power consumption and cost.



## 8. References

[1]"Principles of Lock-in Detection | Zurich Instruments," www.zhinst.com, Dec. 20, 2019. https://www.zhinst.com/americas/en/resources/principles-of-lock-in-detection [accessed Mar. 26, 2023].

[2] Javier Gaspar, Suei Feng Chen, Alejandro Gordillo, Mateo Hepp, Pablo Ferreyra, Carlos Marqués, Digital lock-in amplifier: study, design, and development with a digital signal processor, Microprocessors and Microsystems, Volume 28, Issue 4, 2004, Pages 157-162, ISSN 0141-9331, https://doi.org/10.1016/j.micpro.2003.12.002. [accessed Mar. 28, 2023].

[3] "About Lock-In Amplifiers," Stanford Research Systems, [Online]. Available: https://www.thinksrs.com/downloads/pdfs/applicationnotes/AboutLIAs.pdf. [Accessed: Feb. 13, 2023].

[4] "Lock-in Amplifiers World Market Report," StrategyR Global Industry Analysts, [Online]. Available: https://www.strategyr.com/market-report-lock-in-amplifiers-forecasts-global-industry-analysts-inc.asp. [Accessed: Mar. 26, 2023].

[5] "Lock-in Amplifiers," Zurich Instruments, 2023. [Online]. Available: https://www.zhinst.com/americas/en/lock-in-amplifiers. [Accessed: Mar. 27, 2023].

[6] "Lock-in Amplifiers SR810 & SR830," Stanford Research Systems, [Online]. Available: https://www.thinksrs.com/products/sr810830.htm. [Accessed: Mar. 27, 2023].

