Fault-Tolerant Topology and Operation of Multi-Port Interlink Modular Multilevel Converter Based Solid-State Transformer in Future Distribution Systems

by

Jiajie Zang

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Name:	**Jiajie Zang**
Degree:	**Doctor of Philosophy**
Title:	**Fault-Tolerant Topology and Operation of Multi-Port Interlink Modular Multilevel Converter Based Solid-State Transformer in Future Distribution Systems**
Committee:	**Chair: Woo Soo Kim** Associate Professor, Mechatronic Systems Engineering
	Jiacheng (Jason) Wang Supervisor Associate Professor, Mechatronic Systems Engineering
	Mehrdad Moallem Committee Member Professor, Mechatronic Systems Engineering
	Amr Marzouk Committee Member Senior Lecturer, Mechatronic Systems Engineering
	Mariana Resener Examiner Assistant Professor, Sustainable Energy Engineering
	Mehdi Narimani External Examiner Associate Professor, Department of Electrical and Computer Engineering McMaster University

Abstract

Conventional radial AC distribution systems cannot effectively accommodate the rapidly increasing renewable energy sources (RESs) and new loads such as fast charging stations of electric vehicles. To address the pressing challenges, active distribution grids and DC systems have attracted significant interests with their many potential benefits. Considering that AC and DC systems will coexist in future distribution grids wherever suitable, hybrid AC/DC distribution is regarded as a promising and practical solution for future distribution systems. The focus of this work, multiport interlink modular multilevel converter-based solid-state transformers (iMMC-SSTs), is expected to play a key enabling role in hybrid distribution systems to integrate different grid entities, including both AC and DC networks at both medium and low voltage levels. The iMMC-SST features capabilities such as bidirectional power transfer, fault isolation and restoration, system reconfiguration, and voltage regulation.

However, power electronics-based SSTs are more vulnerable under abnormal conditions, which hinders their adoption in practical systems. The high number of circuit elements are potential fault sources in the iMMC-SST. The possible faults of the SST and the connected feeders can destroy balance of the system and even result in second faults. A comprehensive protection scheme for the iMMC-SST is indispensable to ensure the device's safety and improve the system’s reliability and robustness. Based on the fault location, abnormal conditions are in general divided into external and internal types. In this work, grounding scheme for the SST is designed and investigated to address typical external fault conditions such as the single line-to-ground (SLG) short-circuit fault and single pole-to-ground (SPG) short-circuit fault.

For internal abnormal conditions, power switch faults are of major concerns of the iMMC-SST since a switch failure will lead to arm voltage imbalance, circulating current increase, and second faults. The submodule (SM) switch open-circuit (OC) fault analysis is presented considering different operation modes of the iMMC-SST in Chapter 4. Unlike traditional MMC applications, the iMMC-SST has different fault characteristics, and the previous fault diagnosis and fault-tolerant schemes developed for other applications are not applicable here. Based on detailed analysis of the fault behaviors, a fault-tolerant scheme based on the global redundant module and unbalanced control is proposed in Chapter 5. Similarly, the dual active bridge (DAB) switch OC fault is studied in detail, and a DC current injection fault-tolerant method is proposed to address the overcurrent and transformer saturation issues in Chapter 6.

The proposed solutions and their analysis are verified with MATLAB simulations and experiments with scaled-down laboratory prototypes.

Keywords: interlink modular multilevel converter solid-state transformer; grounding scheme design; submodule; dual active bridge; open-circuit fault analysis; fault-tolerant scheme

Dedicated to my dear wife Xianyu, lovely son Jincheng, my dear parents, and parents-in-law for believing in me and providing constant support and encouragement

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List of Acronyms

BIL	Basic Insulation Level
CDSM	Clamp Double Submodule
CHB	Cascaded H-Bridge
CHBSM	Cascaded H-Bridge Submodule
CM	Common-Mode
DAB	Dual Active Bridge
DER	Distributed Energy Resource
DG	Distributed Generation
DM	Differential-Mode
DPS	Double Phase Shift
EI	Energy Internet
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPS	Extended Phase Shift
ESS	Energy Storage System
EV	Electric Vehicle
FBSM	Full-Bridge Submodule
HBSM	Half-Bridge Submodule
HFT	High-Frequency Transformer
IGBT	Insulated gate bipolar transistor
iMMC-SST	Interlink Modular Multilevel Converter Solid-State Transformer
LFT	Line-Frequency Transformer
LVAC	Low-Voltage AC
LVDC	Low-Voltage DC
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MVAC	Medium-Voltage AC
MVDC	Medium-Voltage DC
NGR	Neutral Ground Resistor

NPCSM	Neutral Point Clamped Submodule
NPPSM	Neutral-Point Piloted Submodule
OC	Open Circuit
PM	Power Module
RES	Renewable Energy Source
RPM	Redundant Power Module
RSM	Redundant Submodule
SC	Short Circuit
SM	Submodule
SPS	Single Phase Shift
SST	Solid-State Transformer
TOV	Transient Overvoltage
TPS	Triple Phase Shift

Chapter 1.

Introduction

1.1. Motivation of the Research

Traditional AC distribution grids are designed to be radial and unidirectional and cannot effectively address the many challenges brought by the rapid increase of grid-tied renewable energy resources (RESs) and electric vehicles (EVs) [1]. In the past decade, significant efforts have been made on developing new architectures of distribution grids and studying their characteristics and performances. Among other solutions that have been proposed, one direction that has attracted many interests is the possible adoption of DC and hybrid DC/AC systems in medium-voltage (MV) and low-voltage (LV) distribution systems. This is partly owing to the experiences accumulated from the recent successful deployments of converter-based high-voltage DC (HVDC) technologies at the transmission level and, also is in light of the considerable theoretical benefits that DC grids can bring to the next-generation distribution systems. It is reported that RES such as wind farms [2], [3] and photovoltaic power plants [4], [5] can achieve higher efficiency in DC grids than AC systems. Besides, DC grids also feature high power density, high controllability, and no reactive power [6]. Assuming the co-existence of AC and DC grids at the distribution level, the concept of hybrid AC/DC distribution system has emerged and received consideration as a promising and practical structure for future implementations. Figure 1.1 shows an illustrative diagram of such a hybrid distribution grid example.

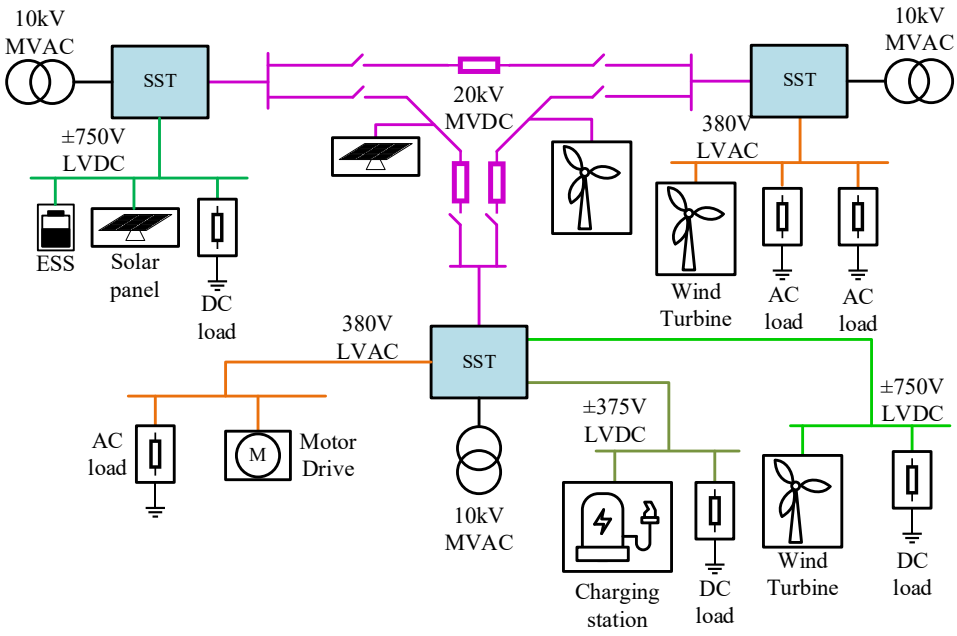

Figure 1.1 Configuration of a hybrid distribution network example

As shown in Figure 1.1, power electronics based solid-state transformers (SSTs) will serve as the key enablers in such hybrid systems by interconnecting the various distribution grids with different voltage levels and forms. In AC systems, SSTs are proposed to replace the traditional bulky line-frequency transformers (LFTs) for voltage leveling and isolation. They can be designed to offer DC ports to flexibly interface DC systems and components. With their inherent control freedoms, they can provide additional ancillary functions such as voltage regulation, power flow control, reactive power compensation, and system restoration and reconfiguration [7]. Many SST topologies have been proposed and investigated over the past decade. When it comes to the MV grid level, SSTs with modular multilevel structures are favorable candidates due to their excellent scalability and modularity, as well as their ability to interconnect different types of grids. In this regard, two prominent modular multilevel SST topologies emerged in the past decade, i.e., the cascaded H-bridge SSTs (CHB-SSTs) and the modular multilevel converter SSTs (MMC-SSTs) [8]. Both topologies offer ports for medium-voltage AC (MVAC), low-voltage DC (LVDC), and low-voltage AC (LVAC). Unlike the CHB-SST, the MMC-SST can provide an additional MVDC port, making it more suitable and competitive for applications that require interfacing with an MVDC grid. The MVDC distribution system makes better use of the line capacity with lower cost than its AC counterparts [9], [10]. Besides, the large-scale RESs generate less loss when connecting with MVDC grids because of the fewer power conversion stages. In this

work, hybrid distribution systems with MVDC buses are considered, which favors the MMC-SSTs as a key device for grid interconnection.

This thesis focuses on the recently emerged interlink MMC-SST (iMMC-SST) which has high scalability, modularity, and capability for decoupled power transfer by each port. The iMMC-SST is formed by directly coupling MMC submodules (SMs) and dual active bridge (DAB) modules, as shown in Figure 1.2. The MMC structure provides the MVAC and MVDC ports, and the outputs of the DAB modules are parallel connected to form the LVDC port. An independent LV converter is applied to create the LVAC port.

However, the iMMC-SST is more vulnerable to abnormal conditions than a traditional LFT. The large number of circuit elements are potential fault sources in an iMMC-SST. These faults may deteriorate the balance of the iMMC-SST and even result in second faults if abnormal conditions are not cleared quickly. Additionally, the interconnection of different distribution systems complicates the system's configuration, enabling a fault in one of the feeders to propagate to healthy parts of the MMC-SST. The faults that occur in (or out of) the iMMC-SSTs lead to subsequent overcurrent and overvoltage problems and threaten the safety of the device and the adjacent feeders. The relatively low reliability of iMMC-SSTs hinders their utilization in practical distribution systems. Therefore, a comprehensive protection scheme is indispensable to improve the reliability and robustness of these SSTs.

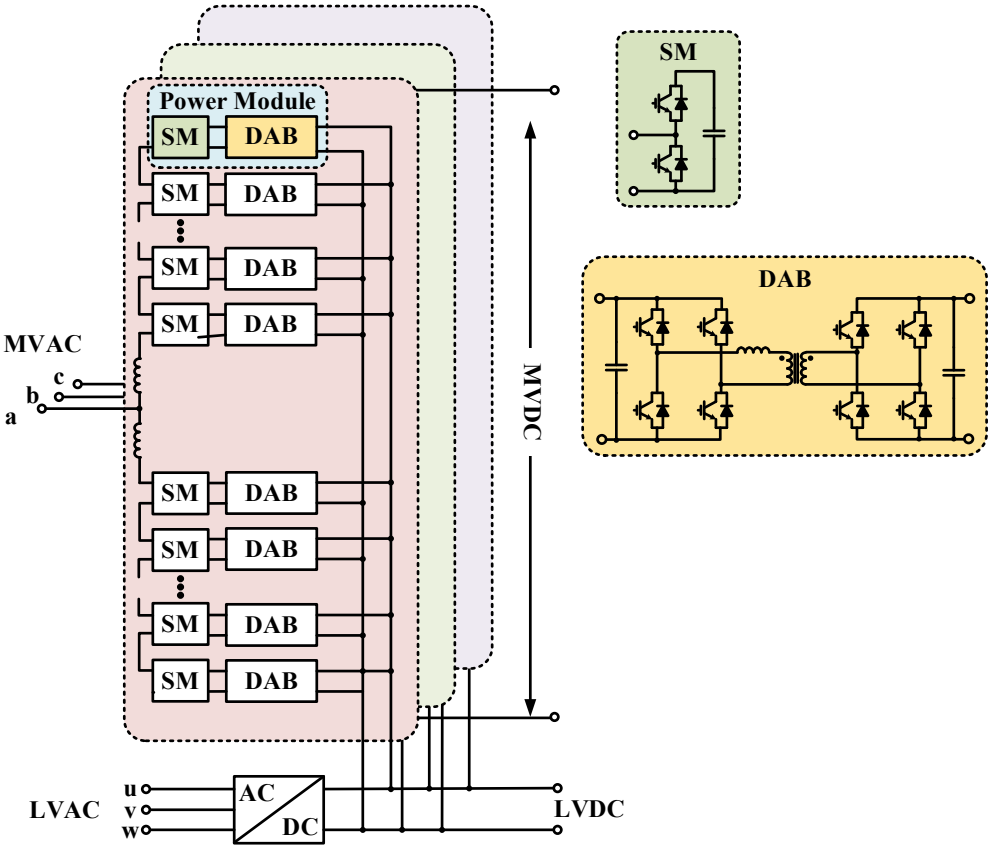

Figure 1.2 Topology of the iMMC-SST [8]

1.2. Overview of Solid-State Transformers

Various grid-participating / grid-forming power electronic devices [11], e.g., soft open points [12], hybrid transformers [13], and loop balance controllers [14], [15], have been recently proposed to act as critical nodes in hybrid distribution networks. Here, they are all considered as SST-type devices in general and share the following common features:

- They serve as multiport nodes to interconnect distribution systems with the same or different voltage forms and levels [11].
- They function as interfaces for distributed generation sites and energy storage systems [11], [12].
- They provide power flow and voltage control, electrical isolation, and power quality enhancement [7], [16], [17].

- They enable fault detection, isolation, postfault reconfiguration and restoration [11], [12], [14], [15], [18].

- They help with flexible power dispatch and optimization when multiple SSTs work in coordination [19], [20].

1.2.1. Solid-State Transformer Topologies

SSTs with different topologies are suitable for different applications. As shown in Figure 1.3, SSTs are generally categorized as single-stage, two-stage, and three-stage according to their number of power conversion stages [15], [20], [21]. Among the SSTs, the three-stage type is prominent in future hybrid distribution systems because, relative to single-stage and two-stage SSTs, they offer more ports to interconnect AC and DC grids with different voltage levels.

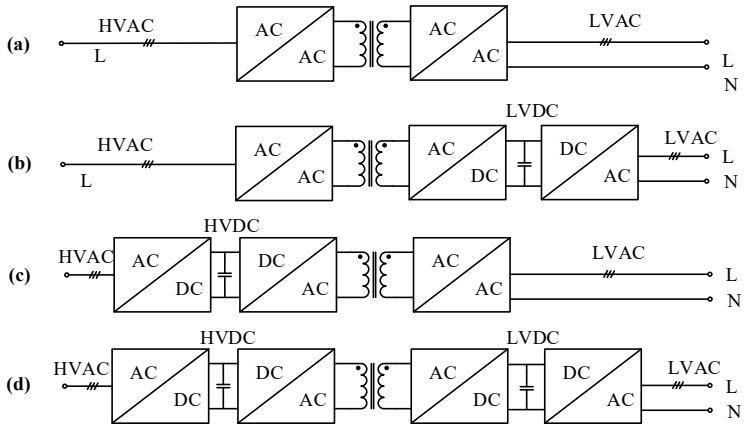

Figure 1.3 SST topology configurations: (a) Single-stage; (b) Two-stage type I; (c) Two-stage type II; (d) Three-stage [21]**.**

Because of the limited voltage and current ratings of insulated gate bipolar transistors (IGBTs), three-stage modular multilevel SSTs are developed to interconnect multiple MV distribution systems. To date, a few research groups have proposed several three-stage modular multilevel SST topologies. In [22], a 6.5 kV-IGBT 3.6 kHz CHB-SST prototype was offered by future renewable electric energy delivery and management (FREEDM) system center to serve as an active grid interface in an intelligent grid architecture. As shown in Figure 1.4, the device can provide MVAC, LVDC, and LVAC ports.

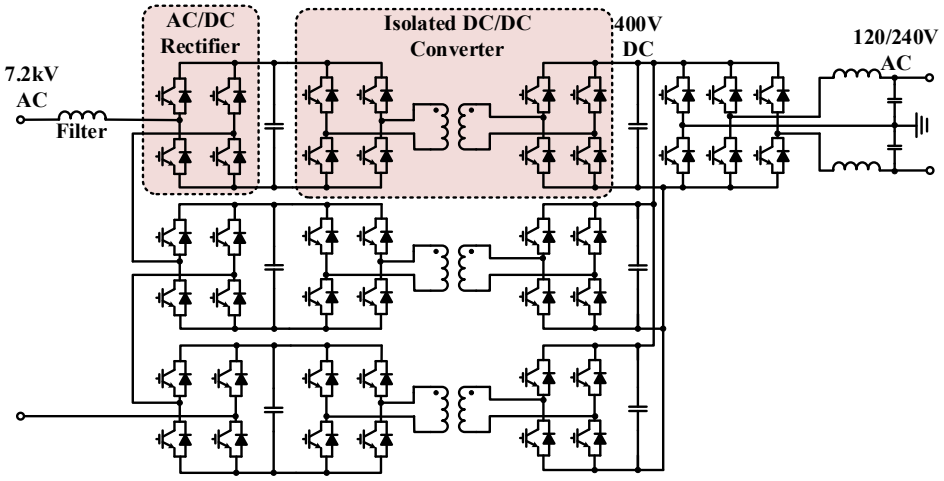

Figure 1.4 Multiport CHB-SST from FREEDM [22]

Another CHB-SST, illustrated in Figure 1.5, is the intelligent universal transformer (IUT) [23] introduced by the electric power research institute (EPRI) as a 25 kVA/50 kHz prototype with three ports. However, due to diode-based rectifiers, this SST cannot provide bidirectional power transfer capability.

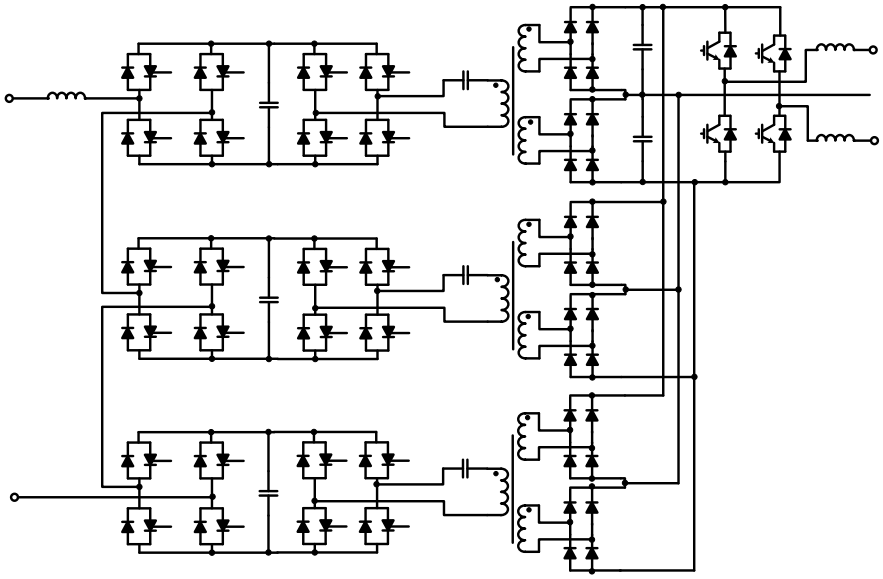

Figure 1.5 IUT from EPRI [23]

In [24], Huber *et al.* from ETH presented a CHB-SST consisting of neutral point clamped type SMs (NPCSMs). As depicted in Figure 1.6, each SM can sustain a higher voltage such that fewer transformers are used in this device. Although using multilevel submodules reduces the number of HFTs, the control complexity increases.

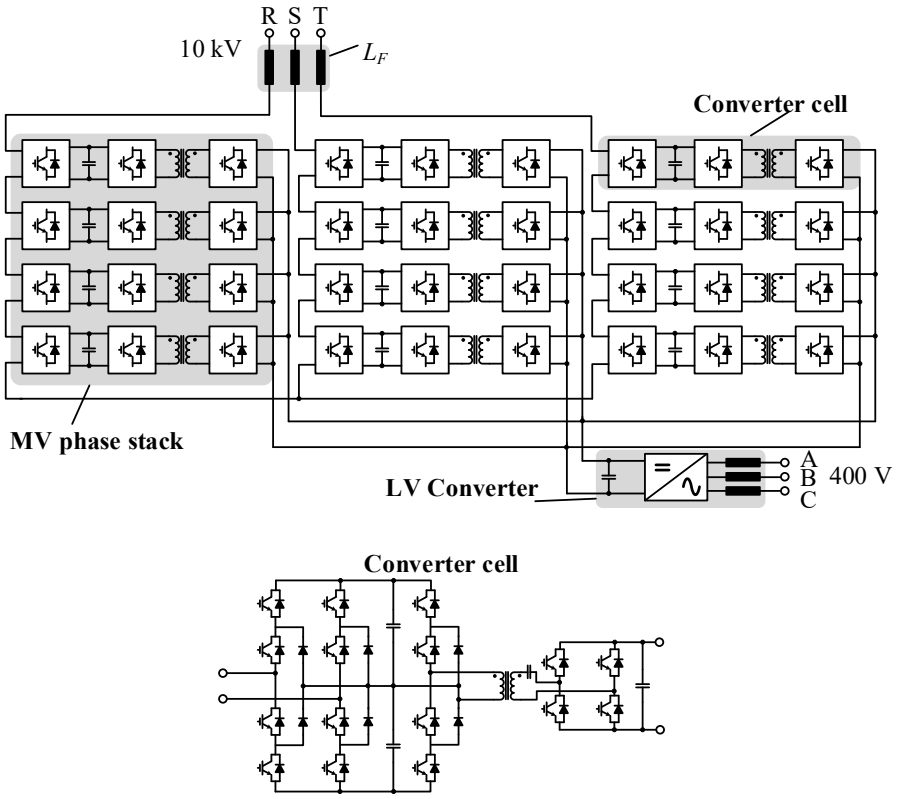

Figure 1.6 CHB-SST from ETH [24]

Figure 1.7 shows the universal and flexible power management (UNIFLEX-PM) structure formed by a CHB-SST [25]. In the second conversion stage, DC links with different voltage levels can be provided via multiple parallel-connected building blocks such that different DC grids can be interconnected directly. Unlike the first two CHB-SSTs, different LVAC ports can be provided by the UNIFLEX-PM.

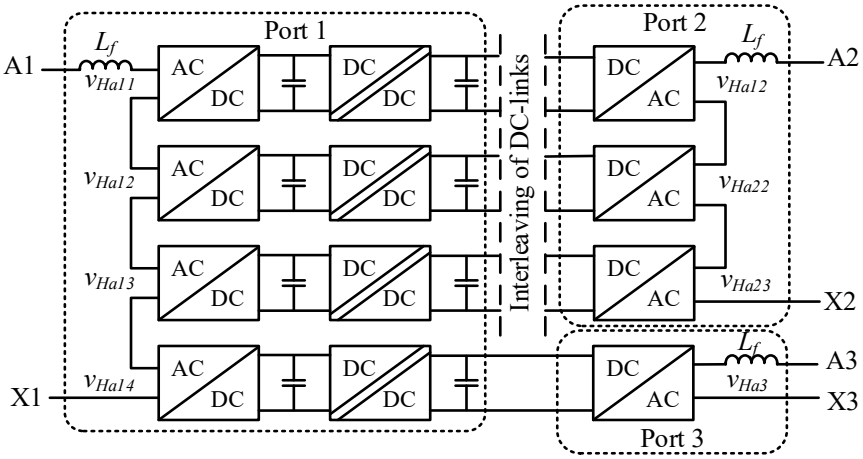

Figure 1.7 UNIFLEX-PM [25]

Notably, MVDC distribution networks are critical parts of hybrid distribution systems. Therefore, the mentioned CHB-SSTs are not suitable for use in hybrid distribution systems. To provide MVDC ports, an MMC-SST was proposed by the Institute of Electrical Engineering of the Chinese Academy of Sciences (IEECAS) [26]. According to Figure 1.8, this type of MMC-SST integrates two independent converter topologies: MMC structure and DAB modules. Although the MVDC port is provided, the power exchange between the MV- and LV-sides should flow through the MVDC bus where the reliability of the LVDC port power supply cannot be guaranteed, especially under MVDC fault conditions. Nevertheless, this device requires large capacitors in the MVDC bus, leading to a high initial cost and large size.

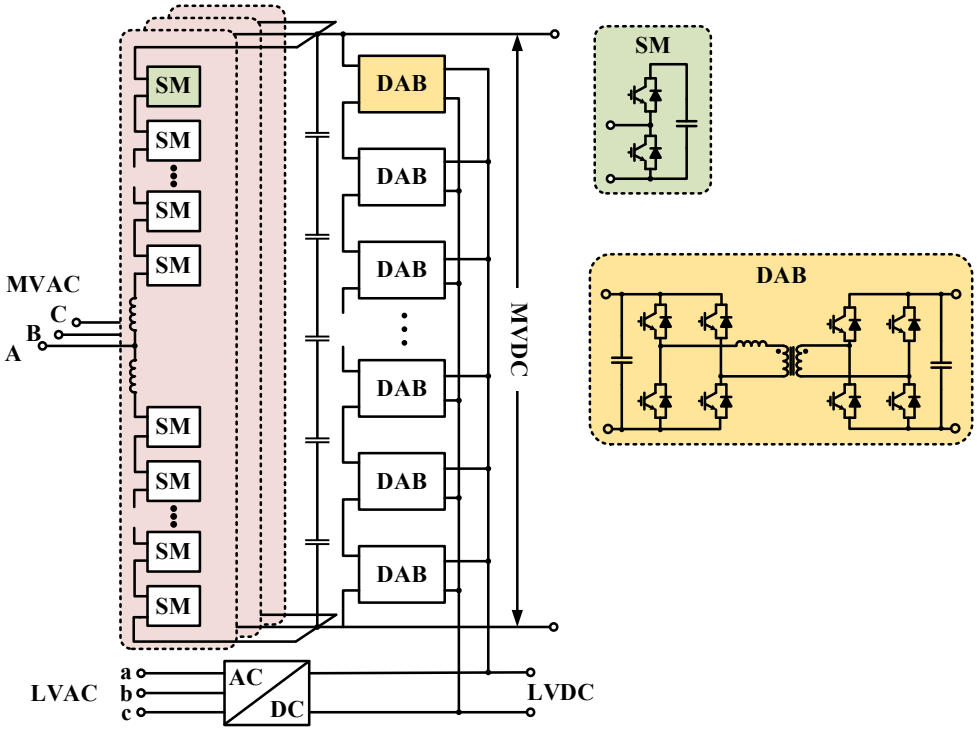

Figure 1.8 MMC-SST from IEECAS [26]

Unlike the MMC-SST shown in Figure 1.8, the iMMC-SST MVDC capacitor ports are removed to reduce the cost and size of the system. Since the power exchange between different ports is decoupled, faulty feeders can be disconnected from the SST without affecting the power supply of the healthy feeders. Moreover, the SM and the DAB converter are integrated with a common capacitor where the modularity is better than the topology from IEECAS. Because of its modularity and scalability, this device can conduct potential optimization and control strategies to enhance the performance,

reliability, and robustness of the hybrid distribution system. Thus, the iMMC-SST is selected as the main research platform for the work presented in this thesis.

1.2.2. Challenges of iMMC-SSTs in Hybrid Distribution Networks

Although SSTs are favored over traditional devices in terms of weight, volume and controllability [27], several issues, including low reliability, lack of robustness, and relatively lower efficiency, still hinder their adoption in distribution networks. Since the SSTs are subject to interferences generated from both the grid and the device itself, abnormal conditions that have impact on them are in general categorized as the internal and external types. The internal conditions correspond to faults inside the SST device, such as the malfunction of circuit elements and the control failure of the SST. The external counterparts represent cases that occur in the connected feeders, e.g., MV and LV short-circuit (SC) faults, lightning surges, switching transients, and nonideal loads [13], [28].

From the perspective of external abnormal conditions, a conventional 10 kV LFT can sustain a 20 kV dielectric for 1 min during a short circuit fault, and the oil insulated LFT has overload capabilities of 25× for 2 s, 11× for 10 s, and 3× for 300 s. Additionally, traditional LFTs can achieve galvanic isolation such that faults do not propagate to other ports. Unlike LFTs, SSTs have an overload capability of 1.5× for some min and 4× for some ms [27], [28]. Hence, compared with traditional devices, SSTs are more vulnerable and sensitive to abnormal external conditions due to the limitations of the IGBT's voltage and current ratings. Moreover, except for the common issues of SSTs, the protection of iMMC-SSTs used in hybrid distribution systems is more complicated because of the integration of different grids. The external faults on any adjacent feeders can be transferred to other ports through the iMMC-SST if a proper protection scheme is not in place.

However, internal faults of the iMMC-SST, like circuit component failure and malfunction of gate drivers, may disrupt the balance of the system and cause an increase in circulating current and fault propagation in adjacent feeders. In addition, more severe secondary faults may occur when internal faults are not detected and cleared quickly. Internal and external faults can bidirectionally propagate due to a lack of galvanic isolation between MV- or LV-level AC and DC ports. Therefore, since less

research has been conducted on SST protection and the existing SST protection has not been thoroughly investigated [30], [31], a comprehensive iMMC-SST protection scheme is indispensable for maintaining the power supply and protecting the entire system.

According to [28], the quality of a protection scheme can be evaluated with the following criteria: selectivity, sensitivity, security, safety, speed, reliability, losses, and cost. In terms of selectivity, an SST protection scheme should cooperate with the counterparts implemented in distribution networks to maintain consistency with minimum interference to customers of the systems. Additionally, protection devices should be capable of identifying all abnormal conditions, even those with small magnitudes, in consideration of sensitivity. Moreover, system security is ensured by preventing the false tripping of protection devices. Nevertheless, the trade-off is inevitable to loosen the protection scheme's sensitivity and security level when the fault-tolerant (fault-tolerant) operation is expected. Otherwise, the protection schemes will shut down the iMMC-SST instead of maintaining its operation under fault conditions. Safety is another essential concern in SST protection scheme design, i.e., safeguarding both personnel and devices from hazards during faults, inspection, and maintenance. Moreover, a protection scheme should identify abnormal conditions as rapidly as possible to protect customers and entire systems with less influence.

1.2.3. Protection Schemes for iMMC-SSTs

Thorough protection of SSTs is generally realized along with protection devices [17], [28], [29] and corresponding fault-tolerant control strategies [30]–[33]. Multiple protection devices are adopted in SST applications, as shown in Figure 1.9. Metal oxide surge arrestors are arranged at MV and LV ports of the iMMC-SST to address overvoltage conditions caused by abnormal external conditions [28]. Overcurrent in adjacent distribution networks is often solved by fuses/breakers associated with corresponding fault-tolerant operation combinations [34], [35]. In contrast to overcurrent issues encountered with traditional grid systems, hybrid distribution networks implemented with iMMC-SSTs can achieve fault-tolerant operation and maintain power supplies to consumers instead of shutting down the entire system. Thus, the selection of overcurrent protection devices should consider the detailed design of the iMMC-SST to keep the consistency of overcurrent protection. Besides, disconnectors are placed at each port for severe fault conditions and maintenance to realize isolation [36].

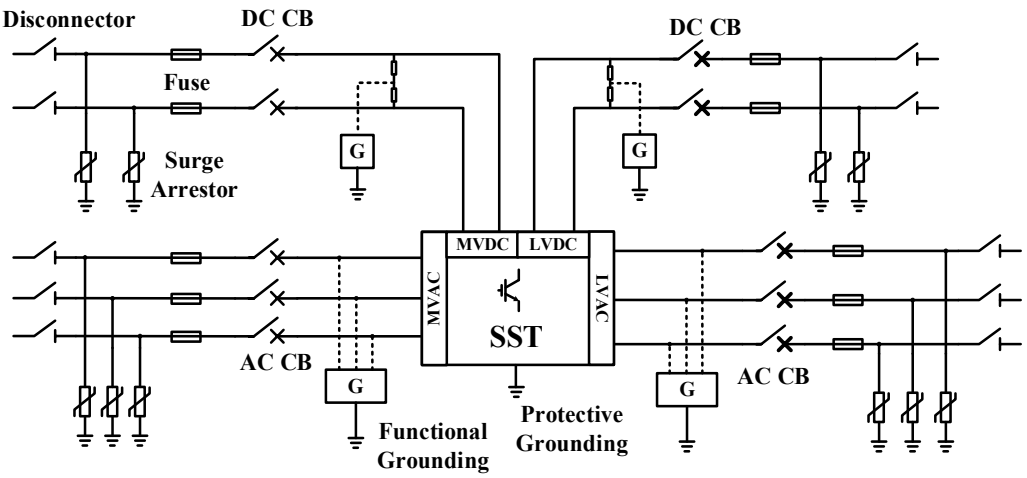

Figure 1.9 Protection devices used in iMMC-SSTs

The grounding scheme is critical in protecting SSTs in various scenarios. On one hand, the common-mode (CM) interference can be efficiently suppressed by grounding schemes and cooperation with specific control strategies under normal conditions [37]. On the other hand, the overvoltage and overcurrent caused by the faults can be affected by various grounding schemes in different degree. Typical grounding schemes limit the amplitudes of the relevant voltages and currents, enabling the development of potential fault-tolerant strategies. Furthermore, the choice of a grounding scheme affects the selection of other protection devices in terms of their sensitivity and selectivity. Therefore, Chapter 3 will discuss iMMC-SST grounding scheme design via careful considerations.

In the [38], three practical solutions for avoiding internal failure of SSTs are summarized, including oversized components, redundancy of converters, and a fault-tolerant approach, as shown in Figure 1.10. Component overdesign is a simple and inexpensive solution to address the overstressing issue. However, it is uneconomical in the selection of semiconductors, considering price and losses. The redundancy scheme is another solution to cope with the internal faults without affecting the operation of systems. This method can achieve higher reliability and robustness, and maintains the system service continuity in modular SST applications under circuit element faults [10], [39]–[42]. Nevertheless, the redundancy scheme also raises the number of circuit elements and, in turn, increases the cost and volume. Unlike the previous two methods, fault-tolerant control strategies are proposed to address the abnormal internal conditions of SSTs without using additional components [43]–[45]. But performance degradation is

inevitable in SSTs when fault-tolerant control strategies are used due to the asymmetrical topologies caused by faults [45], [46].

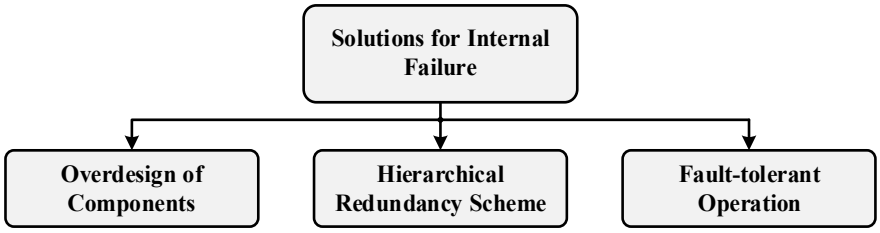

Figure 1.10 Typical methods for solving internal failure on SST

1.3. State-of-the-Art Solutions for Typical Fault Conditions

The protection scheme is provided to deal with several typical fault conditions, like single-phase-to-ground SC (SLG-SC) faults, single-pole-to-ground SC (SPG-SC) faults, and open-circuit (OC) faults that occur in the IGBTs of an iMMC-SST, which are investigated to design the corresponding grounding scheme and fault-tolerant strategies. SLG and SPG SC faults are the most common faults occurring in connected distribution systems[47], [48]. Moreover, secondary faults may occur if these faults are not solved immediately. While inside the iMMC-SST, the large number of IGBTs can be regarded as potential fault sources that will deteriorate the system's normal operation and may result in cascading failures of the device.

Grounding schemes should be designed for the system by considering the impact caused by the introduction of SSTs under different operation modes. To date, very little research has been carried out on grounding scheme design for emerging SSTs used at the distribution level. Several grounding schemes have been used and evaluated in SST applications. Resistance and solid grounding schemes were applied and assessed in MV- and LV- AC ports of the CHB-SST [28]. A flexible arc-suppression device based on a three-phase CHB converter with auxiliary sources and model predictive control was developed to suppress fault currents caused by line-to-ground SC faults [49]. A flexible grounding method for neutral points is presented in the literature [50] for solving arc suppression issues in traditional distribution networks during single-phase ground faults. In [29], the MV side of the hybrid transformer was delta-connected, and the LV side was grounded with a neutral inductor. However, a traditional bulky and expensive LFT was required to provide the natural neutral point for specific grounding

scheme implementation [29], [50]. Due to the different topologies of SSTs shown in the literature [28], the grounding schemes for SSTs cannot be directly used in iMMC-SSTs since there is no natural neutral point. Although the arc-suppression method is effective in [49], the modularity cannot be achieved, and the control complexity is increased, which is undesirable in iMMC-SSTs. In summary, all the abovementioned grounding schemes considered only fault conditions on the grid side, which is insufficient to deal with common-mode (CM) interference generated under normal conditions in hybrid distribution networks. Therefore, a specific grounding scheme design is proposed in this thesis for iMMC-SSTs.

According to [38], [51], power devices are the most fragile components in utility power industry applications. Additionally, SC and OC faults accounted for approximately 50% of all the abnormal conditions related to semiconductors. The gate driver detects modules with SC faults and directly shuts them down based on fault characteristics. When an IGBT OC fault occurs, the faulty unit can still operate for a short period because the overvoltage and overcurrent issues under this condition are not as severe as those of an SC fault, which makes it possible to develop potential fault-tolerant strategies.

On the MMC side, IGBT OC fault-tolerant operation is mainly realized by using redundant SMs that are evenly implemented in all the arms. After a fault is identified, the faulty SMs are bypassed and replaced by healthy redundant SMs [43], [46], [52]–[54]. However, the traditional redundancy scheme used in MMC applications needs more SMs, increasing the initial cost and volume. Moreover, due to the unique topology of the iMMC-SST, this approach is not cost-effective since bypassing the faulty unit results in a lower equipment usage ratio. To enhance the availability of the device, two fault-tolerant schemes for solving an SM IGBT OC fault are developed in this work with lower cost and volume than previous schemes.

A fault-tolerant approach based on a redundancy scheme was adopted on the DAB side [30]. However, the healthy circuit elements of the faulty unit cannot be fully used when the faulty element is bypassed. Zhao, et al. proposed another DAB fault-tolerant scheme in [45] to improve equipment utilization and reliability by using the healthy components of the faulty module. Nevertheless, the analysis demonstrated in [45] is based on the ideal circuit condition, while in an actual situation, a DC bias current

appears on the faulty side of the DAB and generates unbalanced magnetic fluxes in the HFT, leading to transformer magnetic saturation. Hence, a fault-tolerant control strategy based on DC current injection is developed in this program to overcome the DAB IGBT OC fault without causing transformer saturation. On this basis, the systems' reliability and robustness can be improved with lower cost and volume, and therefore, the competitiveness of iMMC-SSTs in hybrid distribution networks can be improved significantly.

1.4. Objectives and Contributions of this Work

The objective of this work is to develop a comprehensive protection scheme for improving the reliability and safety of an iMMC-SST and its connected distribution systems. The iMMC-SST can be flexibly reconfigured under different abnormal conditions with minimum service degradation, enabling practical use in the distribution systems.

The contributions of this work include:

- The iMMC-SST basic operating principle under normal conditions is investigated. In addition, the general control strategy of the iMMC-SST is proposed according to a steady-state analysis. On this basis, fault analysis and fault-tolerant schemes are presented in the following sections. (Chapter 2)

- Based on SLG-SC and SPG-SC fault analyses, a grounding scheme is designed for an iMMC-SST while considering system safety and coordination of potential fault-tolerant strategies (Chapter 3)

- A comprehensive SM IGBT OC fault analysis considering different operation modes is proposed for future fault diagnoses and fault-tolerant operation schemes. (Chapter 4)

- An SM IGBT OC fault-tolerant operation scheme is proposed using a global redundancy scheme to provide minimum performance degradation with fewer redundant SMs. Moreover, the system's initial cost and size can be further reduced. (Chapter 5)

- A fault-tolerant control strategy based on DC current injection is proposed, which maintains the operation of the iMMC-SST under IGBT OC faults without causing transformer magnetic saturation and overcurrent issues. (Chapter 6)

In Chapter 7, the general outcomes and achievements of this research are summarized based on the theoretical analysis, simulation, and experimental results. This chapter also presents several new ideas that were not realized during this research. These are described in the future works section.

Chapter 2.

Basics of the iMMC-SST

2.1. iMMC-SST Structure and Mathematical Model

2.1.1. iMMC-SST Topology

As shown in Figure 1.2, the topology of an iMMC-SST is composed of an MMC structure, several DAB converters, and an LV AC/DC converter. MMC topology has been adopted in several power applications due to its scalability and modularity, including flexible AC transmission (FACT) devices [55], [56], high- and medium-voltage drives [57], [58], and power quality management devices [59]. The DAB DC/DC converter has been widely studied because of its features of auto-adjusted bidirectional power flow, wide voltage gain range, and zero voltage switching (ZVS)-on capability [60]–[63], and has been adopted in various applications [11], [64], [65]. The LVAC and LVDC ports are interconnected by an LV AC/DC converter, which can be regarded as an isolated block in the system and will not be discussed in detail.

In addition, based on the demands of specific applications, different features can be satisfied via various SM topologies, such as DC-side fault current blocking, smaller capacitor voltage ripple and circulating currents, and high efficiency [42], [66]–[68]. The most commonly used SM topologies are depicted in Figure 2.1, including half-bridge SM (HBSM), full-bridge SM (FBSM), neutral-point piloted SM (NPPSM), clamp double SM (CDSM), cascaded HBSM (CHBSM), neutral-point-clamped SM (NPCSM), flying-capacitor SM (FCSM), and cascaded FBSM (CFBSM) topologies.

All these SM topologies can be classified as 1) basic SM topologies, e.g., HBSM and FBSM; 2) multilevel SM topologies, e.g., NPPSM, NPCSM, and FCSM; 3) cascaded SM topologies, e.g., CHBSM and CFBSM; and 4) clamping SM topologies, e.g., CDSM. Compared with the basic SM topologies, although extra functions can be realized by the other topology variants, the design and controllability are more complicated, which hinders their practical adoption. Therefore, the HBSM will be considered the main SM topology in this research.

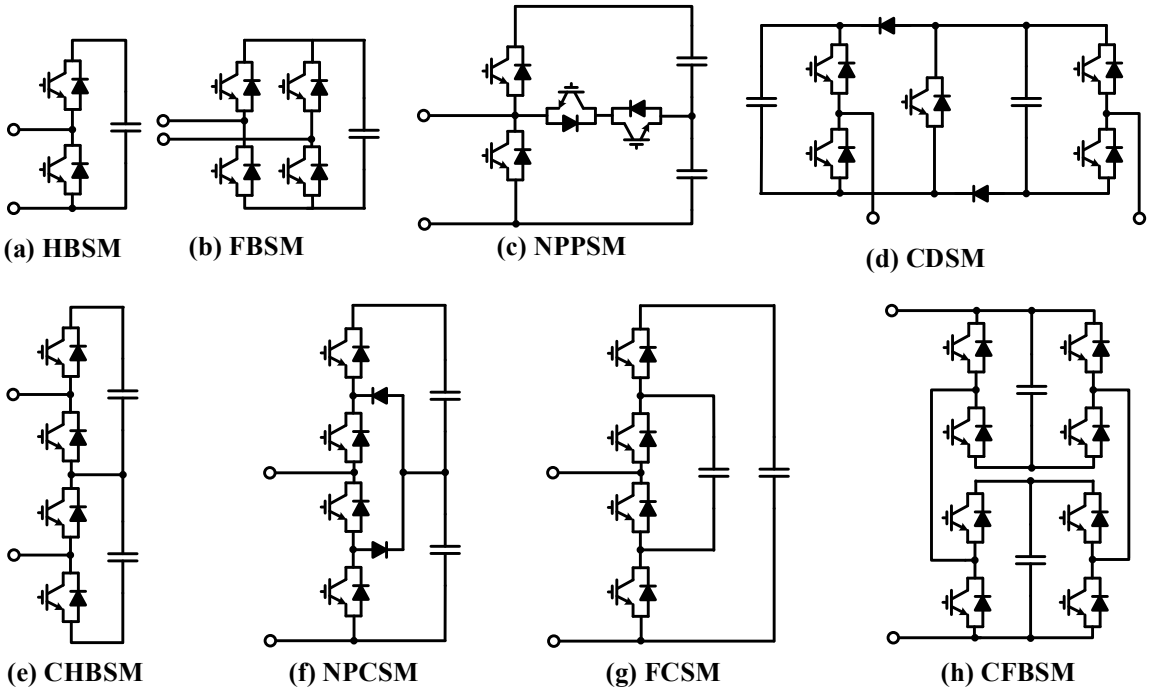

Figure 2.1 SM Topologies

The combination of the SM and the series-connected DAB converter is defined as the power module (PM) of the iMMC-SST. Several potential DAB topologies are used to match the SM capacitor voltage. For example, when an HBSM or FBSM is adopted, a traditional H-bridge topology is preferred as the interface. If a CHBSM or NPCSM is applied, an NPC active bridge is used in the DAB front-end, which reduces the number of HFTs compared with cases with an HBSM or FBSM. Owing to the flexibility of the iMMC-SST, multiple PM variants can be used to meet different demands of detailed applications.

2.2. iMMC-SST Mathematical Model

2.2.1. MMC System Level Model

Without considering the arm inductors, the MMC structure has the following characteristics: 1) the MVDC voltage is maintained by a constant number of inserted SMs in each phase; 2) the MVAC voltage and level can be regulated by varying the SMs inserted in both the upper and lower arms in each phase; and 3) the MMC arm currents contain both AC and DC components such that power can be exchanged between MVAC and MVDC networks.

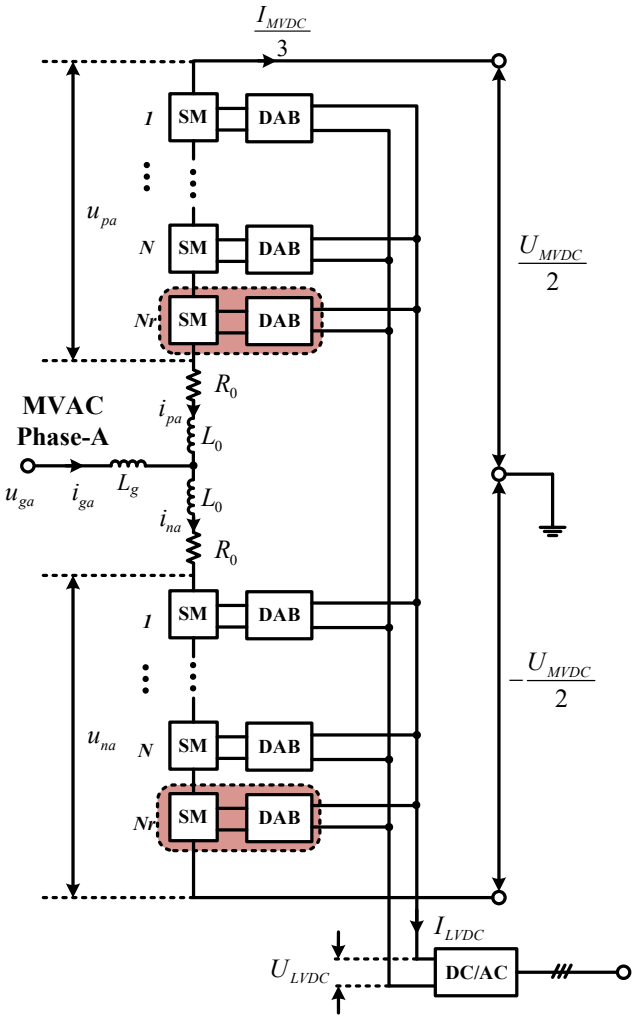

Figure 2.2 Single-phase iMMC-SST topology

As shown in Figure 2.2, a single-phase iMMC-SST has *N* regular SMs and one redundant SM in each arm. The mathematical model of the MMC structure is based on the most widely accepted model in the literature [68], [69]. According to Kirchhoff's Voltage Law (KVL), the MMC structure Phase-a has the following relationship:

$$-\frac{U_{\mathrm{MVDC}}}{2}+u_{pa}+L_0\frac{di_{pa}}{dt}+R_0 i_{pa}+u_{ga}=0 \tag{2.1}$$

$$\frac{U_{\mathrm{MVDC}}}{2}-u_{na}-L_0\frac{di_{na}}{dt}-R_0 i_{na}+u_{ga}=0 \tag{2.2}$$

Here, U_{MVDC} is the MVDC bus voltage; u_{ga} and I_{ga} are the MVAC grid voltage and current, respectively; I_{MVDC} is the MVDC current; u_{pa} and u_{na} represent the upper and

lower arm voltages; i_{pa} and i_{na} denote the upper and lower arm currents; L_0 and R_0 are the arm inductor and resistor, respectively; and L_g is the MVAC grid-side inductor.

For further simplification, three variables are defined:

$$u_{diffa} = \frac{1}{2}\left(u_{na} - u_{pa}\right) \tag{2.3}$$

$$u_{coma} = \frac{1}{2}\left(u_{pa} + u_{na}\right) \tag{2.4}$$

$$i_{ca} = \frac{1}{2}\left(i_{pa} + i_{na}\right) = I_{ca}^{DC} + i_{ca}^{AC} \tag{2.5}$$

where u_{diffa} is the differential-mode (DM) voltage of the upper and lower arms in Phase-a; u_{coma} is the CM voltage of the upper and lower arms in Phase-a; and i_{ca} is the circulating current of Phase-a, which is formed by both AC and DC components. Under normal conditions, the circulating current is evenly distributed to the three phases according to the following relationships:

$$i_{ca}^{AC} + i_{cb}^{AC} + i_{cc}^{AC} = 0 \tag{2.6}$$

$$I_{ca}^{DC} = I_{cb}^{DC} = I_{cc}^{DC} = -\frac{I_{\mathrm{MVDC}}}{3} \tag{2.7}$$

Subtracting and summing (2.1) from (2.2) while considering the newly defined variables, two new equations can be derived:

$$\frac{L_0}{2}\frac{di_{ga}}{dt} + \frac{R_0}{2} i_{ga} = -u_{ga} + u_{diffa} \tag{2.8}$$

$$L_0 \frac{di_{ca}}{dt} + R_0 i_{ca} = \frac{U_{dc}}{2} - u_{coma} \tag{2.9}$$

Thus, the MVAC current and circulating current can be regulated by adjusting u_{diffa} and u_{coma} when the MVAC and MVDC voltages are maintained.

2.2.2. Power Module Level Model

In the iMMC-SST, the DAB converters are series-connected with SM capacitors, as shown in Figure 2.3. The DAB converter contains two H-bridges, a high-frequency transformer (HFT), and an auxiliary inductor. T_1-T_4 and D_1-D_4 are the IGBTs and the free-wheeling diodes (FWDs) of the primary side, respectively. T_5-T_8 and D_5-D_8 are the corresponding counterparts of the bridge H2. L_s is the sum of the leakage inductance of the HFT and the auxiliary inductance; i_1 and i_2, u_{AB} and u_{ab} are the primary- and secondary-side AC currents and voltages of the HFT, respectively; i_{dij} and i_{oij} are the input and output currents of the DAB of Phase-*j* Arm-*i*; u_{cpa} and i_{cpa} are the SM capacitor voltage and current; and i_{ipa} is the input current of the SM.

Since the SMs in the same arm share common dynamic behavior under normal operation, the upper- and lower-arm SM input voltages are:

$$\begin{aligned} u_{opa} &= S_{pa} \cdot u_{cpa} \\ u_{ona} &= S_{na} \cdot u_{cna} \end{aligned} \tag{2.10}$$

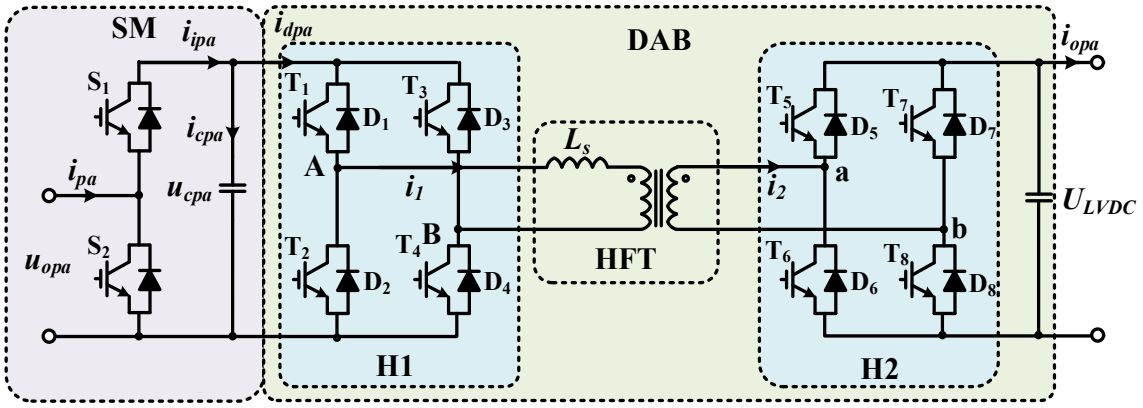

Figure 2.3 Typical power module topology of iMMC-SST

According to (2.8) and (2.9), the switching functions of the upper and lower arm SMs under normal operation can be rewritten as:

$$\begin{aligned} s_{pa} &= \frac{0.5U_{\mathrm{MVDC}} - e_a + u_{cira}}{Nu_{cpa}} \approx \frac{1}{2} - \frac{e_a}{U_{\mathrm{MVDC}}} + \frac{u_{cira}}{U_{\mathrm{MVDC}}} \\ s_{na} &= \frac{0.5U_{\mathrm{MVDC}} + e_a + u_{cira}}{Nu_{cna}} \approx \frac{1}{2} + \frac{e_a}{U_{\mathrm{MVDC}}} + \frac{u_{cira}}{U_{\mathrm{MVDC}}} \end{aligned} \tag{2.11}$$

where e_a is the equivalent MVAC output voltage of Phase-a and u_{cira} is the voltage stress generated by the circulating current.

Correspondingly, the input currents of the upper and lower arm SMs are:

$$\begin{aligned} i_{ipa} &= S_{pa} \cdot i_{pa} = i_{cpa} + i_{dpa} \\ i_{ina} &= S_{na} \cdot i_{na} = i_{cna} + i_{dna} \end{aligned} \tag{2.12}$$

In (2.12), the upper and lower SM capacitors have the following dynamic equations:

$$\begin{aligned} C\frac{du_{cpa}}{dt} &= i_{cpa} \\ C\frac{du_{cna}}{dt} &= i_{cna} \end{aligned} \tag{2.13}$$

Phase-shift modulations have been the most attractive modulation techniques for DAB converters. According to the control degree of freedom, the modulation schemes can be divided into single-phase-shift (SPS), extended-phase-shift (EPS), dual-phase-shift (DPS), triple-phase-shift (TPS), and variable-frequency modulation methods [62], [63]. By adding controllable variables, better system efficiency can be achieved at the cost of higher complexity. In this thesis, the SPS is adopted in the iMMC-SST due to its simplicity, where the transmission power of each DAB converter on the upper and lower arms can be expressed as:

$$P_{dpa} = \frac{u_{cpa} \cdot n \cdot U_{\mathrm{LVDC}}}{2\pi^2 f_d L_s} \phi_d \left[\pi - \left| \phi_d \right| \right] \tag{2.14}$$

$$P_{dna} = \frac{u_{cna} \cdot n \cdot U_{\mathrm{LVDC}}}{2\pi^2 f_d L_s} \phi_d \left[\pi - \left| \phi_d \right| \right] \tag{2.15}$$

All the DAB modules share the same phase shift angle to maintain the power balance. Thus, the input and output currents of the DAB converters can be derived according to (2.14) and (2.15),

$$i_{dpa} = i_{dna} = \frac{n \cdot \phi_d \left[\pi - \left| \phi_d \right| \right]}{2\pi^2 f_d L_s} \cdot U_{\mathrm{LVDC}} = g_{di} \cdot U_{\mathrm{LVDC}} \tag{2.16}$$

$$i_{opa} = \frac{n \cdot \phi_d [\pi - |\phi_d|]}{2\pi^2 f_d L_s} \cdot u_{cpa} = g_{do} \cdot u_{cpa}$$
$$i_{ona} = g_{do} \cdot u_{cna} \tag{2.17}$$

According to (2.17), the corresponding fluctuation is excited in the LVDC port due to the vibration of the SM capacitor voltages. For simplification, the phase shift ratio (*D*) is defined, which has the following relationship with the phase shift angle ϕ_d,

$$D = \frac{\phi_d}{\pi} \tag{2.18}$$

The relationship between the DAB output current and the LVDC bus capacitor C_L can be written as:

$$C_L \frac{dU_{\text{LVDC}}}{dt} = N(i_{opa} + ... + i_{onc}) - I_{\text{LVDC}} \tag{2.19}$$

Assuming the loads on the MVDC and LVDC buses are R_d and R_L, the following equations can be obtained:

$$U_{\text{MVDC}} = R_d I_{\text{MVDC}} = R_d \cdot \sum_{j=a,b,c} i_{cj} \tag{2.20}$$

$$C_L \frac{dU_{\text{LVDC}}}{dt} = N\left(\sum_{\substack{i=p,n \\ j=a,b,c}} i_{oij}\right) - \frac{U_{\text{LVDC}}}{R_L} \tag{2.21}$$

In (2.20) and (2.21), i_{cj} is the Phase-j circulating current, and i_{oij} is the DAB output current of Phase-*j* Arm-*i*. The state equation of the LVDC capacitor voltage can be expressed according to (2.21):

$$\frac{dU_{\text{MVDC}}}{dt} = N\frac{g_d}{C_L}\sum_{\substack{i=p,n \\ j=a,b,c}} u_{cij} - \frac{U_{\text{LVDC}}}{C_L R_L} \tag{2.22}$$

Here, C_L is the output capacitor of the DAB module. (2.11) can be simplified as shown in the following two equations without considering the circulating components:

$$\begin{cases} S_{pa} = \dfrac{1}{2} - \dfrac{e_a}{U_{\mathrm{MVDC}}} \\ S_{na} = \dfrac{1}{2} + \dfrac{e_a}{U_{\mathrm{MVDC}}} \end{cases} \tag{2.23}$$

Under steady-state conditions, the SM capacitor voltages contain both DC (U_c) and fluctuation (Δu_{cpa}, Δu_{cna}) components,

$$\begin{cases} u_{cpa} = U_c + \Delta u_{cpa} \\ u_{cna} = U_c + \Delta u_{cna} \end{cases} \tag{2.24}$$

During normal operation, the U_{MVDC} is sustained by the SMs,

$$NU_c = U_{\mathrm{MVDC}} \tag{2.25}$$

assuming the grid-side voltage, current, and virtual electromotive force are expressed by the following equations:

$$\begin{aligned} u_{ga} &= U_{gm} \sin(\omega t) \\ i_{ga} &= I_{gm} \sin(\omega t - \varphi) \\ e_a &= E_m \sin(\omega t - \delta) \end{aligned} \tag{2.26}$$

Here, U_{gm}, I_{gm}, and E_m are the amplitudes of the relevant parameters; φ is the phase difference between the grid-side voltage and current; and δ is the phase shift between the grid-side voltage and the virtual electromotive force of Phase-a.

The transmission power equation among MVAC, MVDC, and LVDC ports is:

$$\frac{3}{2} E_m I_{gm} \cos(\delta - \varphi) = U_{\mathrm{MVDC}} I_{\mathrm{MVDC}} + U_{\mathrm{LVDC}} I_{\mathrm{LVDC}} \tag{2.27}$$

The voltage modulation index is defined as:

$$M = \frac{2E_m}{U_{\mathrm{MVDC}}} \tag{2.28}$$

The arm currents of Phase-a can be expressed as:

$$i_{pa} = -\frac{1}{3} I_{\mathrm{MVDC}} - \frac{1}{2} I_{gm} \sin\left(\omega t - \varphi\right) \tag{2.29}$$

$$i_{na} = -\frac{1}{3} I_{\mathrm{MVDC}} + \frac{1}{2} I_{gm} \sin\left(\omega t - \varphi\right) \tag{2.30}$$

Without considering the SM capacitor voltage fluctuation, the arm voltages of Phase-a can be expressed as:

$$u_{pa} = N \cdot S_{pa} \cdot U_c = \frac{1}{2} U_{\mathrm{MVDC}} - \frac{1}{2} M U_{\mathrm{MVDC}} \sin\left(\omega t - \delta\right) \tag{2.31}$$

$$u_{na} = N \cdot S_{na} \cdot U_c = \frac{1}{2} U_{\mathrm{MVDC}} + \frac{1}{2} M U_{\mathrm{MVDC}} \sin\left(\omega t - \delta\right) \tag{2.32}$$

The corresponding instantaneous power of the upper and lower arms are:

$$\begin{aligned} P_{pa} = & \underbrace{\frac{1}{6} U_{\mathrm{LVDC}} I_{\mathrm{LVDC}}}_{DC} \\ & \underbrace{-\frac{1}{4} U_{\mathrm{MVDC}} I_{gm} \sin\left(\omega t - \varphi\right) + \frac{1}{6} M U_{\mathrm{MVDC}} I_{\mathrm{MVDC}} \sin\left(\omega t - \delta\right)}_{1st} \\ & \underbrace{-\frac{1}{8} M U_{\mathrm{MVDC}} I_{gm} \cos\left(2\omega t - \delta - \varphi\right)}_{2nd} \\ P_{na} = & \underbrace{\frac{1}{6} U_{\mathrm{LVDC}} I_{\mathrm{LVDC}}}_{DC} \\ & \underbrace{+\frac{1}{4} U_{\mathrm{MVDC}} I_{gm} \sin\left(\omega t - \varphi\right) - \frac{1}{6} M U_{\mathrm{MVDC}} I_{\mathrm{MVDC}} \sin\left(\omega t - \delta\right)}_{1st} \\ & \underbrace{-\frac{1}{8} M U_{\mathrm{MVDC}} I_{gm} \cos\left(2\omega t - \delta - \varphi\right)}_{2nd} \end{aligned} \tag{2.33}$$

According to (2.33), unlike the traditional MMC structure, the arm instantaneous power contains DC, 1st order, and 2nd order components. The DC components are absorbed by the DAB converters and transferred to the LVDC bus. Moreover, based on (2.17) and (2.24), the actual DAB transmission power also has an AC component. Hence, combining (2.17), (2.24), and (2.33), the power absorbed by the DAB converters in the upper and lower arms of Phase-a can be expressed as:

$$
\begin{aligned}
P_{DAB}^{\sum pa} &= N \cdot u_{cpa} \cdot i_{ipa} = \frac{1}{6} U_{\mathrm{LVDC}} I_{\mathrm{LVDC}} + N \Delta u_{cpa} i_{ipa} \\
P_{DAB}^{\sum na} &= N \cdot u_{cpa} \cdot i_{ipa} = \frac{1}{6} U_{\mathrm{LVDC}} I_{\mathrm{LVDC}} + N \Delta u_{cna} i_{ina}
\end{aligned}
\tag{2.34}
$$

Combining (2.33) and (2.34), the fluctuating power transferred by the DAB converters is self-cancelled when the three phases of the MMC side are well controlled and balanced.

The power delivered to the LVDC bus in each arm can be simplified,

$$
P_{DAB}^{pa} = P_{DAB}^{na} = \frac{1}{6} U_{\mathrm{LVDC}} I_{\mathrm{LVDC}} \tag{2.35}
$$

Furthermore, (2.12) can be rewritten as,

$$
\begin{aligned}
i_{ipa} = & \\
& \frac{U_{\mathrm{LVDC}}}{6U_{\mathrm{MVDC}}} I_{\mathrm{LVDC}} - \frac{1}{4} I_{gm} \sin(\omega t - \varphi) + \frac{1}{6} M I_{\mathrm{MVDC}} \sin(\omega t - \delta) - \frac{1}{8} M I_{gm} \cos(2\omega t - \delta - \varphi) \\
i_{ina} = & \\
& \frac{U_{\mathrm{LVDC}}}{6U_{\mathrm{MVDC}}} I_{\mathrm{LVDC}} + \frac{1}{4} I_{gm} \sin(\omega t - \varphi) - \frac{1}{6} M I_{\mathrm{MVDC}} \sin(\omega t - \delta) - \frac{1}{8} M I_{gm} \cos(2\omega t - \delta - \varphi)
\end{aligned}
\tag{2.36}
$$

Combining (2.13) and (2.36), the detailed SM capacitor voltage considering the fluctuation can be derived:

$$
\begin{aligned}
u_{cpa} = & \\
& U_c + \frac{1}{4\omega C} I_{gm} \cos(\omega t - \varphi) - \frac{1}{6\omega C} M I_{\mathrm{MVDC}} \cos(\omega t - \delta) - \frac{1}{16\omega C} M I_{gm} \sin(2\omega t - \delta - \varphi) \\
u_{cna} = & \\
& U_c - \frac{1}{4\omega C} I_{gm} \cos(\omega t - \varphi) + \frac{1}{6\omega C} M I_{\mathrm{MVDC}} \cos(\omega t - \delta) - \frac{1}{16\omega C} M I_{gm} \sin(2\omega t - \delta - \varphi)
\end{aligned}
\tag{2.37}
$$

The arm voltages of Phase-a can be expressed as,

$$
\begin{aligned}
u_{pa} &= \sum u_{cpa} = N \cdot s_{pa} \cdot u_{cpa} \\
u_{na} &= \sum u_{cna} = N \cdot s_{na} \cdot u_{cna}
\end{aligned}
\tag{2.38}
$$

From (2.9), since the circulating current is affected by the sum of the arm voltages, the SM capacitor voltage fluctuation excites extra circulating current components. Combining (2.9), (2.37), and (2.38), the detailed circulating current of Phase-a can be expressed as:

$$i_{ca} = -\frac{1}{3} I_{\mathrm{MVDC}} - \frac{3NMI_{gm}}{64\omega^2 LC}\cos\left(2\omega t - \delta - \varphi\right) - \frac{NM^2 I_{\mathrm{MVDC}}}{48\omega^2 LC}\cos\left(2\omega t - 2\delta\right) \tag{2.39}$$

The iMMC-SST has almost the same behavior as traditional MMC applications when there is no circulating current suppression control. In (2.39), i_{ca} consists of DC and second-order components. The second-order components flow only in the three phases under balanced conditions.

Hence, the self-balance of the LVDC bus current can be obtained according to the symmetry of the transmission power and the SM capacitor voltage fluctuation of the three phases,

$$\sum_{\substack{i=p,n \\ j=a,b,c}} i_{oij} = I_{\mathrm{LVDC}} \tag{2.40}$$

2.3. iMMC-SST Control Strategy

Based on the analysis shown in Section 2.2, the control between the MMC side and the DAB converters can be decoupled by SM capacitors. To maintain the balance and power transfer capability, the overall control diagram of the iMMC-SST includes several parts, e.g., the MVDC voltage/MVAC current control block, the SM capacitor voltage balance control block, the circulating current suppression control block, and the LVDC voltage control block, as illustrated in Figure 2.4.

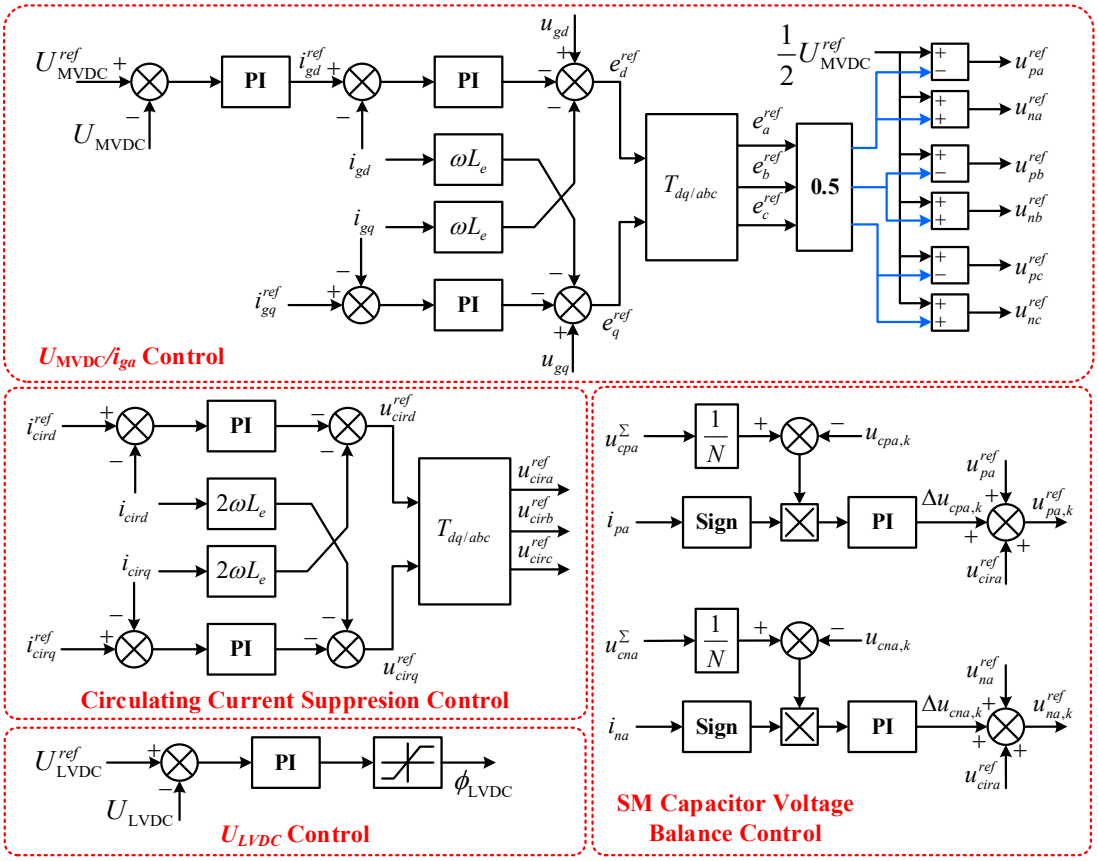

Figure 2.4 Overall control diagram of iMMC-SST

2.3.1. MVDC Voltage Control

According to (2.9), the stability of the MVDC bus voltage is essential to the normal operation of the iMMC-SST. In contrast to the MMC-SST shown in Figure 1.8, no MVDC capacitors are used in the iMMC-SST, and the MVDC bus voltage is determined by the energy stored in the SM capacitors of all three phases. According to (2.12) and (2.13), the state equations of the Phase-*j* upper and lower arm SM capacitor voltage can be expressed as:

$$\begin{cases} \dfrac{du_{cpj}}{dt} = \dfrac{S_{pj}}{C} i_{cj} - \dfrac{S_{pj}}{2C} i_{gj} - \dfrac{g_d}{C} U_{\mathrm{LVDC}} \\ \dfrac{du_{cnj}}{dt} = \dfrac{S_{nj}}{C} i_{cj} + \dfrac{S_{nj}}{2C} i_{gj} - \dfrac{g_d}{C} U_{\mathrm{LVDC}} \end{cases} \tag{2.41}$$

By summing (2.41) all three phases, we obtain:

$$\frac{d\left(\sum_{j=a,b,c}^{i=p,n} u_{cij}\right)}{dt} = \frac{N}{C}\sum_{j=a,b,c}\left(S_{pj}+S_{nj}\right)i_{cj} + \frac{N}{2C}\sum_{j=a,b,c}\left(S_{nj}-S_{pj}\right)i_{gj} - \frac{6N}{C}g_d U_{\mathrm{LVDC}} \quad (2.42)$$

Under balanced conditions, the three-phase AC components of the SM capacitor voltages are symmetrical. Then, (2.42) can be simplified by substituting (2.11):

$$\frac{dU_{\mathrm{MVDC}}}{dt} = \frac{N}{6C}\frac{U_{\mathrm{MVDC}}}{R_d} + \frac{N}{3CU_{\mathrm{MVDC}}}\left(\sum_{j=a,b,c} u_{cj}^{ref} i_{cj}\right) + \frac{N}{12C}\left(\sum_{j=a,b,c} e_j^{ref} i_{gj}\right) - \frac{N}{C}g_d U_{\mathrm{LVDC}} \quad (2.43)$$

When ignoring the arm resistance of the MMC side, u_{cj}^{ref} is orthogonal to the circulating current of phase j (i_{cj}). Moreover, u_{cj}^{ref} is much smaller than the MVDC bus voltage. Thus, the second item on the right-hand side can generate only reactive power, which affects the fluctuation of the MVDC voltage, and it cannot be used to regulate the amplitude of U_{MVDC}. Therefore, (2.43) can be further simplified as:

$$\frac{dU_{\mathrm{MVDC}}}{dt} \approx \frac{N}{6C}\frac{U_{\mathrm{MVDC}}}{R_d} + \frac{N}{12C}\left(\sum_{j=a,b,c} e_j^{ref} i_{gj}\right) - \frac{N}{C}g_d U_{\mathrm{LVDC}} \quad (2.44)$$

According to the Park transformation matrix,

$$T_{abc-dq} = \sqrt{\frac{2}{3}}\begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2}{3}\pi\right) & \sin\left(\omega t + \frac{2}{3}\pi\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2}{3}\pi\right) & \cos\left(\omega t + \frac{2}{3}\pi\right) \end{bmatrix} \quad (2.45)$$

By combining (2.44) and (2.45), the three-phase components are converted into a *dq*-reference frame,

$$\frac{dU_{\mathrm{MVDC}}}{dt} \approx \frac{N}{6C}\frac{U_{\mathrm{MVDC}}}{R_d} + \frac{N}{8C}\left(e_d^{ref} i_d + e_q^{ref} i_q\right) - \frac{N}{C}g_d U_{\mathrm{LVDC}} \quad (2.46)$$

In (2.46), the U_{MVDC} is well controlled by the DAB modules and therefore is used to regulate the U_{MVDC}. In this work, the MVAC voltage reference is aligned to the d-axis and u_{gq}=0. Since the arm and phase inductances are relatively small, $e_d^{ref} \gg e_q^{ref} \approx 0$ can be obtained when the phase shift between u_{gj} and e_j is maintained within a small value. On this basis, the stability of U_{MVDC} can be maintained by adjusting i_{gd}^{ref}. The control diagram is shown in Figure 2.5, where U_{MVDC}^{ref} is the reference value of the MVDC bus.

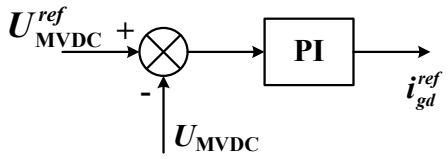

Figure 2.5 Control of the MVDC bus voltage

2.3.2. MVAC Current Control

The power exchange of the MVAC port is realized mainly by controlling the MVAC currents. The Park transformation is also adopted for the simplification of the current control design. By combining (2.3) and (2.8), the MVAC grid-side current state equations can be expressed as:

$$\frac{L+2L_g}{2}\frac{di_{gj}}{dt}=u_{gj}-\left(S_{nj}u_{cnj}-S_{pj}u_{cpj}\right),\left(j=a,b,c\right) \tag{2.47}$$

By substituting (2.11) in (2.47), the following equation can be obtained while ignoring the SM capacitor voltage fluctuation,

$$\left(\frac{L+2L_g}{2}\right)\frac{di_{gj}}{dt}=u_{gj}-e_j^{ref},\ \left(j=a,b,c\right) \tag{2.48}$$

Through the Park transformation, the MVAC grid-side current state equations in the *dq*-reference frame are:

$$\left(\frac{L+2L_g}{2}\right)\frac{d}{dt}\begin{bmatrix}i_{gd}\\ i_{gq}\end{bmatrix}=\begin{bmatrix}u_{gd}\\ u_{gq}\end{bmatrix}-\begin{bmatrix}e_d^{ref}\\ e_q^{ref}\end{bmatrix}+\begin{bmatrix}0 & \omega\left(\frac{L+2L_g}{2}\right)\\ -\omega\left(\frac{L+2L_g}{2}\right) & 0\end{bmatrix}\begin{bmatrix}i_{gd}\\ i_{gq}\end{bmatrix} \tag{2.49}$$

In (2.49), i_{gd} and i_{gq} are the components in the *dq*-reference frame of the MVAC grid side current; u_{gd} and u_{gq} are the MVAC grid side voltage components in the *dq*-axis. Thus, the MVAC currents can be controlled by regulating e_d^{ref} and e_q^{ref}. In addition, i_{gd} and i_{gq} are coupled with the sum of the arm and grid side inductances. Similar to the control scheme used in conventional converters, i_{gd} and i_{gq} should be decoupled. Using the Park transformation, the sinusoidal MVAC currents are converted into DC components such

that PI controllers are applied. The MVAC current decoupled control diagram is depicted in Figure 2.6.

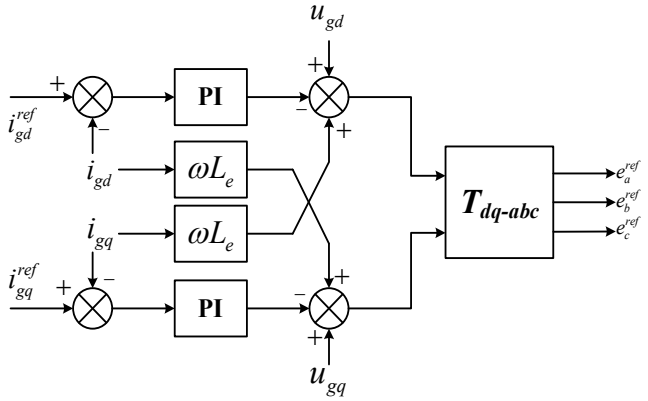

Figure 2.6 MVAC current control diagram

In Figure 2.6, i_{gd}^{ref} and i_{gq}^{ref} are the MVAC current references in the *dq*-axis; L_e (=0.5L+L_g) is the MVAC equivalent inductance; and $T_{dq\text{-}abc}$ is the *dq-abc* transformation matrix, as shown in (2.50).

$$T_{dc-abc}=\sqrt{\frac{2}{3}}\begin{bmatrix}\sin(\omega t) & \cos(\omega t)\\ \sin\left(\omega t-\frac{2}{3}\pi\right) & \cos\left(\omega t-\frac{2}{3}\pi\right)\\ \sin\left(\omega t+\frac{2}{3}\pi\right) & \cos\left(\omega t+\frac{2}{3}\pi\right)\end{bmatrix} \tag{2.50}$$

2.3.3. MMC-side Circulating Current Suppression Control

Similar to traditional MMC applications, 2nd-order harmonics also exist in the arm currents of the iMMC-SST, which increases the system's current stress and reactive power. Additionally, the SM capacitor voltage is coupled with the circulating current, which results in high-order harmonics and threatens the normal operation of the iMMC-SST. Hence, circulating current suppression control (CCSC) is indispensable for the system, and (2.39) can be simply expressed as:

$$i_{ca}=-\frac{1}{3}I_{\mathrm{MVDC}}-I_c\sin(2\omega t-\varphi_c) \tag{2.51}$$

Here, I_c is the amplitude of the 2nd-order circulating current and φ_c is the circulating current phase angle of Phase-a. Likewise, the counterparts of Phase-b and -c are:

$$i_{cb} = -\frac{1}{3} I_{\mathrm{MVDC}} - I_c \sin\left[2\left(\omega t - \frac{2}{3}\pi \right) - \varphi_c \right] \tag{2.52}$$

$$i_{cc} = -\frac{1}{3} I_{\mathrm{MVDC}} - I_c \sin\left[2\left(\omega t + \frac{2}{3}\pi \right) - \varphi_c \right] \tag{2.53}$$

Therefore, the three-phase circulating currents are in a negative sequence. By combining (2.9) and (2.11), the circulating current state equation can be expressed by the following equation while neglecting the SM capacitor voltage fluctuation,

$$\frac{di_{cj}}{dt} = -\frac{1}{L} u_{cj}^{ref}, \left(j = a, b, c \right) \tag{2.54}$$

Based on the Park transformation, the negative sequence *abc-dq* conversion matrix is:

$$T_{abc-dq}^{2nd} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(2\omega t) & \cos\left(2\omega t - \frac{2}{3}\pi \right) & \cos\left(2\omega t + \frac{2}{3}\pi \right) \\ -\sin(2\omega t) & -\sin\left(2\omega t - \frac{2}{3}\pi \right) & -\sin\left(2\omega t + \frac{2}{3}\pi \right) \end{bmatrix} \tag{2.55}$$

The circulating currents in the *dq*-axis can be expressed as:

$$L\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega L \\ 2\omega L & 0 \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = -\begin{bmatrix} u_{cd}^{ref} \\ u_{cq}^{ref} \end{bmatrix} \tag{2.56}$$

On this basis, the CCSC can be achieved by regulating u_{cd}^{ref} and u_{cq}^{ref}. Similar to the MVAC grid side current control design, the corresponding CCSC diagram is illustrated in Figure 2.7. In this figure, i_{cd}^{ref} and i_{cq}^{ref} are the circulating current reference values in the *dq*-axis. T_{dq-abc}^{2nd} is the 2nd-order negative sequence *dq-abc* transformation matrix,

$$T_{dq-abc}^{2nd}=\sqrt{\frac{2}{3}}\begin{bmatrix}\cos(2\omega t) & -\sin(2\omega t)\\ \cos\left(2\omega t-\frac{2}{3}\pi\right) & -\sin\left(2\omega t-\frac{2}{3}\pi\right)\\ \cos\left(2\omega t+\frac{2}{3}\pi\right) & -\sin\left(2\omega t+\frac{2}{3}\pi\right)\end{bmatrix} \tag{2.57}$$

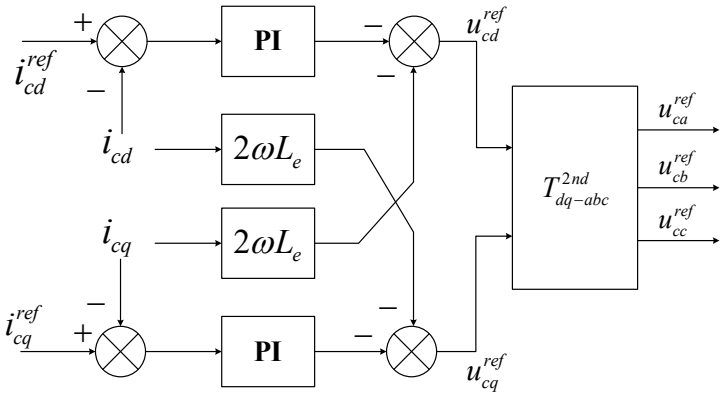

Figure 2.7 Circulating current suppression control diagram

2.3.4. MMC-side SM Capacitor Voltage Balance Control

In the above analysis of the iMMC-SST normal operation, the SM capacitor voltages are assumed to be equally controlled. In practice, a small energy difference occurs among the SMs within a switching cycle for several reasons, such as gating signal asynchronization, control delay, and device losses. The accumulation of energy difference leads to a voltage difference between the SM capacitor voltages that further deteriorates the normal operation of the iMMC-SST. The SM capacitor voltage balance control diagram is depicted in Figure 2.8. u_{cpa}^{Σ} and u_{cna}^{Σ} are the sum of the SM capacitor voltages of the upper and lower arms of Phase-a; $u_{cpa,k}$ and $u_{cna,k}$ are the k^{th} SM's capacitor voltages of the upper and lower arms of Phase-a; $\Delta u_{cpa,k}$ and $\Delta u_{cna,k}$ are the compensated components for the k^{th} SM capacitor voltage balance.

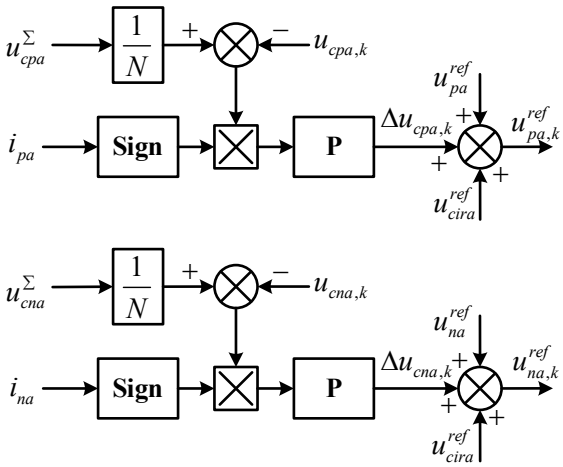

Figure 2.8 SM capacitor voltage balance control diagram

The instantaneous power exchanged by the SMs is determined by the SM output voltage u_{opa} and the arm currents. When the SM capacitor is in charging mode, the modulation index of the SM with the higher voltage should be reduced and that with the lower voltage should be increased; when the SM capacitor is in discharging mode, the modulation index of the SM with the higher voltage should be increased and that with the lower voltage should be reduced such that the SM capacitor voltage balance is controlled.

When $u_{cpa,k}$ (or $u_{cna,k}$) is larger than the arm SM capacitor voltage average values u_{cpa}^{Σ}/N (or u_{cna}^{Σ}/N), the energy of the k^{th} SM capacitor is smaller than the others. Hence, when $i_{pa}>0$ (or $i_{na}>0$), the product of the k^{th} SM capacitor voltage difference and the arm current is negative; a negative $\Delta u_{cpa,k}$ (or $\Delta u_{cna,k}$) can be obtained via the P controllers such that the power, i.e., the product of $\Delta u_{cpa,k}$ (or $\Delta u_{cna,k}$) and the arm currents is negative to compensate for the voltage difference. When $i_{pa}<0$ (or $i_{na}<0$), the product of the k^{th} SM capacitor voltage difference and the arm current is positive, and $\Delta u_{cpa,k}$ (or $\Delta u_{cna,k}$) can be obtained via the P controller to generate a negative compensated power to reduce the voltage difference of the k^{th} SM. Therefore, the energy of the k^{th} SM can be reduced to realize the SM capacitor voltage balance for both arm current directions. The same characteristics can be obtained when $u_{cpa,k}$ (or $u_{cna,k}$) is smaller than the arm SM capacitor voltage average values u_{cpa}^{Σ}/N (or u_{cna}^{Σ}/N), which will not be further discussed. Hereby, the SM capacitor voltage balance can be maintained by regulating $\Delta u_{cpa,k}$ and $\Delta u_{cna,k}$.

2.3.5. LVDC Bus Voltage Control

Equation (2.22) can be simplified in the three-phase balanced mode since the SM capacitor voltage fluctuation is self-cancelled when all the DAB modules adopt the same phase shift angle,

$$\frac{dU_{\mathrm{LVDC}}}{dt}=\frac{6U_{\mathrm{MVDC}}}{C_L}\cdot\frac{n}{2\pi^2 f_d L_s}\phi_d\left(\pi-\left|\phi_d\right|\right)-\frac{U_{\mathrm{LVDC}}}{C_L R_L},\ \phi_d\in\left[-\frac{\pi}{2},\frac{\pi}{2}\right] \tag{2.58}$$

Based on (2.58), the common phase shift angle can be used to control the stability of the LVDC bus voltage. Within the range $\left[-\frac{\pi}{2},\frac{\pi}{2}\right]$, the phase shift angle and $\frac{dU_{\mathrm{MVDC}}}{dt}$ have a monotonic relationship where the PI controller can be adopted. The LVDC bus voltage control diagram is shown in Figure 2.9.

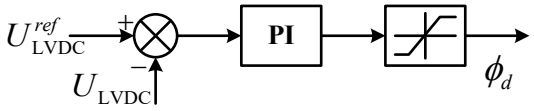

Figure 2.9 LVDC bus voltage control diagram

2.4. Operation Modes of the iMMC-SST

The multiport feature of the iMMC-SST complicates the system operation modes where power can be flexibly transferred among all three ports. Compared with traditional MMC applications, the iMMC-SST can achieve twelve operation modes, as shown in Table 2.1.

Table 2.1 iMMC-SST Operation Modes

Mode	Power direction			Description
	MVAC	*MVDC*	*LVDC*	
1	<0	>0	>0	1 source, 2 loads
2	<0	-	>0	1 source, 1 load
3	<0	>0	-	1 source, 1 load
4	>0	<0	>0	1 source, 2 loads
5	>0	<0	-	1 source, 1 load
6	-	<0	>0	1 source, 1 load
7	>0	>0	<0	1 source, 2 loads
8	>0	-	<0	1 source, 1 load
9	-	>0	<0	1 source, 1 load
10	<0	<0	>0	2 sources, 1 load
11	<0	>0	<0	2 sources, 1 load
12	>0	<0	<0	2 sources, 1 load

Modes 3 and 5 are similar to those of conventional MMC applications, which will not be further discussed in this thesis. When the power is exchanged between the MV side and the LVDC port, the current paths under different switching modes are illustrated in Figure 2.10. Because the SMs of the upper and lower arms share the same characteristics, only scenarios with upper arm SMs are considered. The power exchanged between the MV and LV ports is realized via state (1, 0) with a positive arm current direction and state (0, 1) with a negative arm current direction, as illustrated in Figure 2.10(a) and (c).

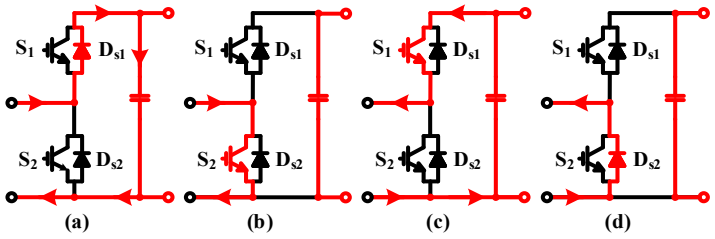

Figure 2.10 Current path of the SM under different switching states. (a) i_{pa}>0 & (1, 0); (b) i_{pa}>0 & (0, 1); (c) i_{pa}<0 & (1, 0); (d) i_{pa}<0 & (0, 1).

The twelve operation modes listed in Table 2.1 can be categorized into four types according to the arm current polarity, as indicated in (2.27), to simplify the fault analysis in the following sections. The four types of operation are illustrated in Figure 2.11. In this figure, a positive DC component of the arm currents implies that the MVDC port transfers power to the other ports, while a negative value means that the MVDC port absorbs

power from the other ports; the shaded areas represent i_{iap} during the period when the SM is inserted in the arm.

Among all operation types, Type I includes Mode 6 with the full range of I_{MVDC} and Modes 4, 10, and 12 with $I_{MVDC} \leq -3I_m$; Type II includes Modes 4, 10 and 12 with $-3I_m < I_{MVDC} \leq 0$; Type III includes Modes 1, 7, and 11 with $0 < I_{MVDC} < 3I_m$; and Type IV includes Mode 9 with the full range of I_{MVDC}, and Modes 1, 7, and 11 with $3I_m \leq I_{MVDC}$.

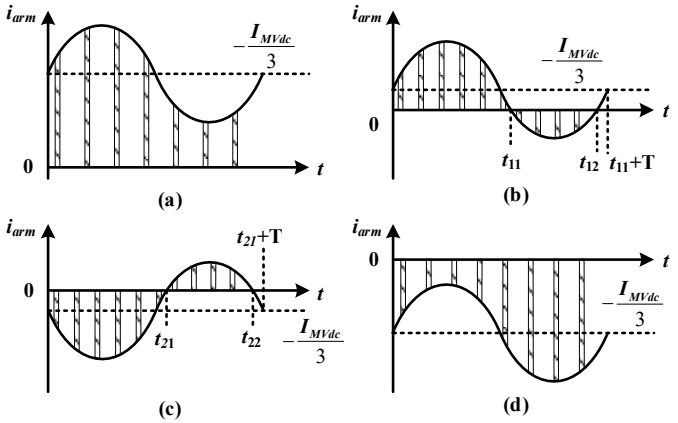

Figure 2.11. Recategorized operation modes. (a) Type I; (b) Type II; (c) Type III; and (d) Type IV.

Chapter 3.

Grounding Scheme Design for iMMC-SST

The grounding schemes play a critical role in the protection scheme under different conditions [28], [70]. A suitable grounding scheme can effectively suppress the CM interference introduced by the SSTs and their adjacent grid systems under normal operation. On the other hand, the overvoltage and overcurrent issues caused by the external faults can be mitigated by the grounding schemes in different manners. For instance, the impedance of the grounding scheme can adjust the amplitudes of the voltage and the currents caused by the faults such that certain fault detection and fault-tolerant schemes can be achieved in the iMMC-SST. Moreover, the grounding scheme design also influences the selection of other protection devices in terms of sensitivity and selectivity.

Different grounding scheme objectives are required in the iMMC-SST MV and LV ports. For MV distribution systems, ensuring power quality is of primary concern, whereas personnel safety should be considered first for LV distribution networks. So far, only a few grounding schemes have been discussed and evaluated specifically for SST applications. In [28], resistance grounding and solid grounding are adopted in the MVAC and LVAC ports of the CHB-SST. It proves that the MV side grounding can significantly affect the post-fault overcurrent and overvoltage by varying the grounding impedance, and the design of the LV-side grounding scheme should cooperate with the downstream protection devices to guarantee the safety of the SST.

However, protection of the SST DC port is not discussed, where fault at this port would also affect the whole system. In [71], the evaluation of grounding design with different schemes for the iMMC-SST was presented based on the short-circuit faults on both AC and DC ports. It indicates that more consideration should be taken in the system reliability of the MV-side grounding while personnel safety is the most important factor in the LV-side grounding. The cooperation with the protection devices, however, was not discussed in [71]. Most of the grounding designs for grid-scale power electronics apparatus are originated from the existing grounding schemes used in conventional distribution systems, e.g., resistance grounding and reactance grounding. However,

considering their unique characteristics and different application scenarios from traditional equipment, no general guidelines of the grounding scheme design for SSTs exist in the literature. When more new devices are implemented in the hybrid distribution systems, interferences originated under both normal and fault conditions could be propagated to the adjacent systems. The mutual influence of the grounding schemes implemented on both the AC and DC ports is not clear in the iMMC-SST. Moreover, the coordination analysis between the grounding schemes and new protection devices is also missing in the literature.

Major factors that should be considered in the grounding scheme design for a typical SST include,

- Structure and configuration of the connected grids;
- Grounding and protection schemes used in the adjacent distribution systems;
- Voltage types and levels of the SST ports;
- SST topology;
- Mutual influence between different SST ports;
- Protection device selection.

3.1. General Considerations of the Grounding Scheme Design for an SST

Several major factors should be considered in the detailed grounding scheme design for distribution-level SSTs, including 1) the types and configurations of the connected distribution systems, 2) the existence of isolation transformers at the SST ports, and 3) the topologies of the SSTs. As a generic representation, Figure 3.1 illustrates a simplified iMMC-SST with multiple ports of different voltage forms and levels, i.e., MVAC, MVDC, LVAC, and LVDC. Factors that need to be considered in the grounding design for each port are also given in the figure.

As shown in Figure 3.1, grounding design at any one port of the SST should first consider the local distribution system configuration. The AC ports are usually connected

with three-phase three-wire or three-phase four-wire distribution networks, where the systems should be grounded to the earth or neutral line, respectively. As shown in Figure 3.2, typical arrangements for systems tied to the DC ports include the asymmetrical monopolar, symmetrical monopolar, and symmetrical bipolar configurations [24], [25]. Each of these structures has its typical grounding design and implementations. Due to these possible combinations, the design and location choice of the grounding schemes around an SST is largely dependent on the type and configuration of the distribution networks the SST is interfaced with.

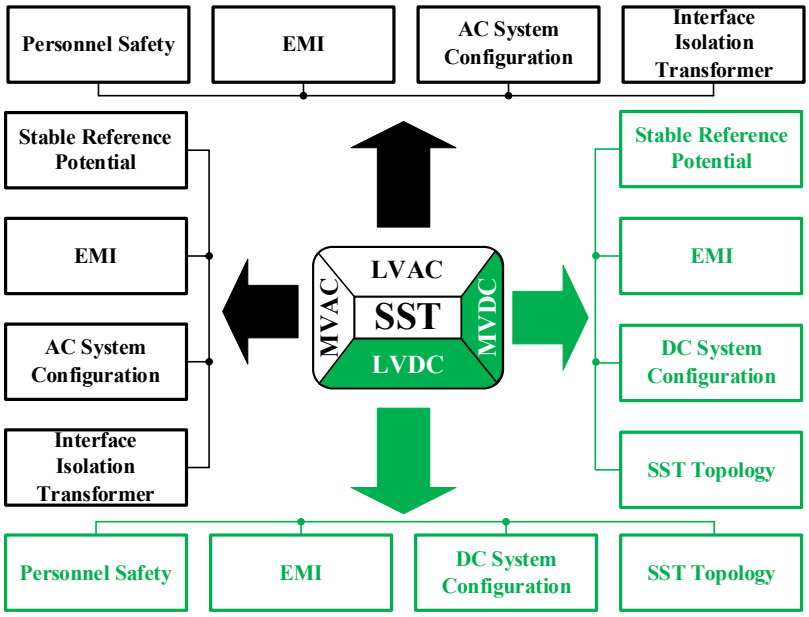

Figure 3.1 Factors to be considered in the grounding design for SSTs

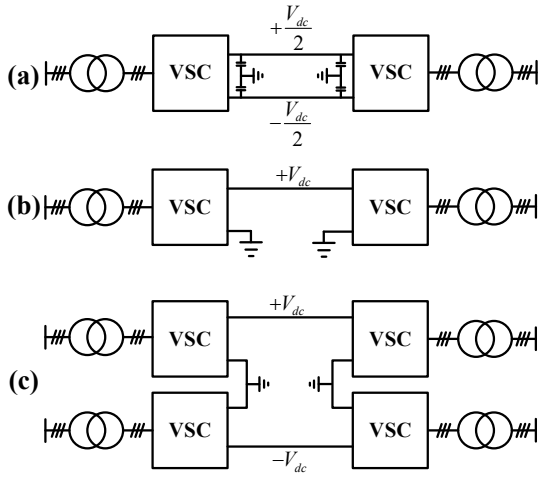

Figure 3.2 DC distribution system configurations (a) symmetrical monopolar; (b) asymmetrical monopolar; (c) symmetrical bipolar

The selection of the SST grounding scheme also depends on whether line-frequency interface isolation transformers are present at their AC ports. If an interface isolation transformer exists, it provides a convenient location for implementing grounding and helps mitigate mutual influences such as electromagnetic interference (EMI) and fault propagation from both the grid- and the converter-side of it. Different AC-side fault characteristics with or without interface isolation transformers were investigated for a modular multilevel converter (MMC) based HVDC system [72]. It was revealed that the transformer could be readily used to implement the grounding for the MMC and effectively contain potential fault propagation. Characteristics of faults happening at different locations on the DC side of an SST under different grounding designs are analyzed and compared in [73] for an MVDC distribution system, based on which several suitable schemes for the SST were provided. It indicated that transformers with Δ/Yn configuration are preferred due to their low CM voltage under SLG faults and their fault restoration capability under SPG faults.

Additionally, the winding configuration of the transformer also affects the location choice of the grounding scheme. As shown in Figure 3.3, an isolation transformer can have several different winding configurations such as Yg/Yg, Y/Δ, Yg/Δ, Δ/Δ, and Δ/Yg in both MV [74] and LV distribution networks [75]. All the wye-connected configurations can provide a neutral point to implement the grounding schemes directly. However, extra grounding transformers (zig-zag transformers or Y/Δ transformers) or star-connected reactance are required to provide an artificial neutral point for delta-connected windings. Moreover, the zig-zag transformer has several advantages over the Y/Δ transformers, which is favorable in the SST applications: low installation area, low loss, and low reactive power consumption, as indicated in [76].

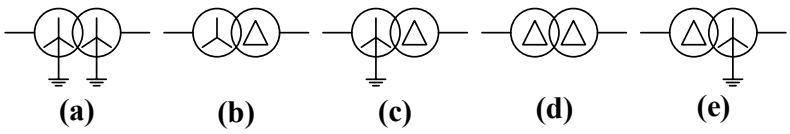

Figure 3.3 Interface isolation transformer (a) Yg/Yg; (b) Y/Δ; (c) Yg/Δ; (d) Δ/Δ; (e) Δ/Yg

It should be noted that the detailed grounding arrangements are related to the requirements on system fault isolation and protection. Since the iMMC-SST is the interface device between the AC and DC distribution systems, fault incidents should be

limited to protect the device and the other connected feeders. All the factors mentioned above should be considered to design an optimal grounding scheme for the device. Moreover, trade-offs may have to be made to meet the grounding requirements of a specific system.

3.2. Fault Propagation Analysis of the iMMC-SST in the Proposed Hybrid Distribution System

Compared with the traditional AC distribution system, integrating different grid systems enabled by the iMMC-SST also introduces mutual interference among the connected feeders. Fault propagation within the system is inevitable if the protection devices and schemes are not employed. So far, most of the fault analysis and grounding scheme design for the MMC-based applications are conducted to only address the faults happening in a single type of distribution system, either AC [76], [77] or DC [78], [79]. Currently, interfacing line-frequency transformers [76], [80], star point reactors [76], and grounding transformers [77] are often applied at the AC ports to offer a neutral point for the grounding implementation. On the DC side of the iMMC-SST, possible grounding can be arranged at the artificial neutral point formed by split capacitors [74], [79], or resistors [81]. As shown in the previous sections, potential grounding schemes can be applied to the AC and DC ports of the iMMC-SST based on the detailed requirements of the connected distribution networks. Fault propagation has not been analyzed for the multi-port SST system in the previous literature. However, it is essential for the proper grounding and protection design around the SST and its reliable operation. Among all the abnormal conditions, the single line-to-ground (SLG) short-circuit fault and the single pole-to-ground (SPG) short-circuit fault are two of the typical abnormal conditions that happened on the adjacent feeders, and they will be used to evaluate the influence of the grounding scheme design for the iMMC-SST.

It is assumed that no grounding scheme has been implemented for the iMMC-SST, and the fault occurred on Phase-a of the MVAC port. The MVAC and MVDC grids are assumed to be not grounded with three-phase three-line and symmetrical monopolar configurations. There are mainly two types of grounding schemes used in the MVDC distribution systems [10]: high-resistance and low-resistance grounding. And the LVDC system grounding options include 1) solid grounding, 2) low-resistance grounding, 3) high-resistance grounding, and 4) ungrounded [82]. So far, the MVDC and the LVDC

grids are new concept distribution systems, and most of the existing distribution systems are formed by the AC grids. Hence, the grounding schemes for the connected DC distribution systems are assumed to be ungrounded (Isolated Terra (IT) type grounding scheme). While the grounding schemes for the AC distribution systems with different voltage levels are quite different from each other according to the local grid codes and regulations. Due to the wide adoption of the ungrounded scheme in the MVAC grid around the world, this scheme will be considered in the fault analysis as well [83].

3.2.1. SLG Fault Analysis without the iMMC-SST Grounding Design

In the iMMC-SST, the MV ports (or the LV ports) are interconnected through the MMC structure without electrical isolation. Hence, the system encountered with SLG fault will induce fault propagation between different ports with the same voltage level. According to the analysis presented in [72], the zero-sequence and negative-sequence currents caused by the SLG fault will flow into the MVAC and MVDC grids via the existing grounding points. Moreover, different from the conventional MMC applications, the iMMC-SST contains more ports such that the fault that happened on any one port will affect the performance of the other ports.

The current will not be affected on the MV side of the iMMC-SST since no grounding points can be used to form the close-loop fault circuit when the SLG fault occurs at the MVAC port. However, the MVAC and MVDC overvoltage issue caused by the faults threatens the insulation capability of the iMMC-SST and the connected distribution systems. The faulty phase voltage dropped to zero, and the other two healthy phase voltages increased to the line voltage level. Besides, a fundamental frequency CM voltage is also introduced in the MVDC pole-to-ground voltages.

Additionally, the current and voltage on the LV side of the iMMC-SST will not be affected due to the HFTs used in the DAB modules. Thus, grounding schemes should be designed on the MV ports of the iMMC-SST to maintain consistency with the connected distribution systems' grounding and protection schemes and protect the device itself. The same results can be obtained when the fault happened in the LVAC grid, which will not be further discussed.

3.2.2. SPG Fault Analysis without the iMMC-SST Grounding Design

With the same grid configuration, the MVDC SPG fault will also propagate to the MVAC port of the iMMC-SST and the adjacent feeders when no specific grounding scheme is designed for the device. Though no closed-loop fault circuit is created, a DC CM voltage caused by the fault is introduced in the MV-side neutral point of the iMMC-SST, leading to shifted phase-to-ground and pole-to-ground voltages. Due to the neutral point shift, the MVAC line voltages are not affected while the phase voltage increases challenge the insulation of the connected feeders and the voltage ratings of the circuit elements in the iMMC-SST. Due to the galvanic isolation achieved by the HFTs, the LV side ports are not influenced. Besides, the same results can be obtained in the LV ports fault conditions when the distribution systems apply the same grounding schemes and configurations, which will not be further discussed in this thesis.

3.3. Grounding Scheme Design

As discussed in section 3.1, the grounding scheme design for the SSTs needs to follow several criteria to guarantee personnel and device safety with considering the local grids' regulations. The device safety and the operation performance are the major concerns in the MV-level grid, and personnel safety should be firstly considered in the LV-level system due to the difference in the accessibility to the distribution system for human beings. Because the SSTs connected to the distribution systems are more vulnerable than the conventional distribution devices, it would be beneficial to suppress the large voltage and current to a suitable level to identify the fault and guarantee the entire systems' and personnel safety. The grounding schemes designed for specific ports of the iMMC-SST should maintain consistency with the existing grounding schemes of the connected distribution networks. Otherwise, conflict may occur between the grounding schemes of the iMMC-SST and the existing grounding schemes used in the connected grids.

3.3.1. Artificial Neutral Points Creation and the Neutral Grounding Resistor Selection

- MV side of the iMMC-SST

No natural neutral points can be provided by all ports of the iMMC-SST. Hence, auxiliary grounding devices must implement certain grounding schemes, such as the isolation transformer, zig-zag transformer, star-connected reactor at the AC ports, and split capacitors and split resistors at the DC ports.

Since the MVDC capacitor of the iMMC-SST is evenly distributed in the SMs, more initial cost and losses will be generated when the split resistors create the artificial neutral point at the MVDC port. Therefore, the grounding scheme of the MV side of the iMMC-SST will be implemented at the artificial neutral point provided by the zig-zig transformer based on the analysis presented in section 3.1. Due to the interconnection of the AC and DC distribution networks enabled by the iMMC-SST, the capacitive current of the MV side rises so that the pre-designed conventional resonant grounding scheme is not capable of dealing with the increasing fault current. Moreover, the resonant grounding scheme implementation is hard to adjust when more iMMC-SSTs are integrated into the MV distribution systems. Hence, because of its easy installation and upgrade, the high-resistance grounding scheme is adopted in the MV side of the iMMC-SST to maintain the consistency of both grounding and protection schemes with those used in the connected distribution systems.

When the high-resistance grounding scheme is adopted, the short-term kVA rating of the zig-zag transformer (S_d) is decided by the MVAC Phase voltage (U_{gj}) and the fault current flowing through the neutral point (I_g), as shown in (3.1).

$$S_d = U_{gj} I_g \tag{3.1}$$

And I_g can be obtained as follows

$$I_g = U_{gj} / R_g \tag{3.2}$$

R_g is the grounding resistance implemented at the artificial neutral point, which is determined by the faulty capacitive current and the regulation of the local MV grid systems. According to the IEEE-C62.92.3 standard [84], the capacity rating S_e of the zig-zag transformer can be calculated via the short-time overload factor k_{over}, as given in the (3.3).

$$S_e = S_d / k \tag{3.3}$$

Where k_{over} equals 10.5 with 10s duration of the overload.

Under the SLG fault, the closed-loop fault circuit is formed by the grounding and fault points via two paths, including the MVAC grid-side path and the path with the MMC structure, as shown in Figure 3.4. Since the MV-side grounding scheme keeps consistent with that of the grid system, the same fault voltage behaviors can be obtained where a sinusoidal faulty CM voltage is added to all three phases. The fault phase voltage drops to zero, and the healthy phase voltages rise to the line voltage level. The neutral voltage shift also results in the vibration with the fundamental frequency of the pole-to-ground voltages. Therefore, the arm voltages of the faulty and healthy phases can be expressed in (3.4) and (3.5), respectively.

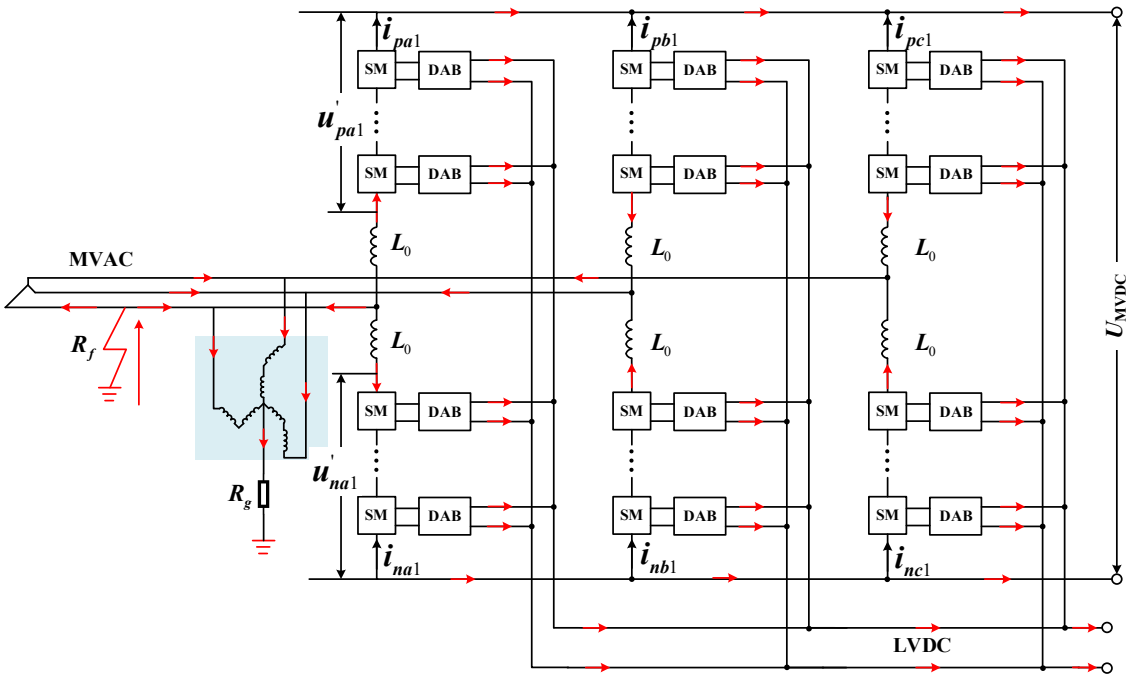

Figure 3.4 SLG fault circuit of the iMMC-SST

$$\begin{cases} u'_{pa1} = \dfrac{U_{\text{MVDC}}}{2} - (R_0 i_{pa1} + L_0 \dfrac{di_{pa1}}{dt}) \\ u'_{na1} = \dfrac{U_{\text{MVDC}}}{2} - (R_0 i_{na1} + L_0 \dfrac{di_{na1}}{dt}) \end{cases} \tag{3.4}$$

$$\begin{cases} u_{pj1}^{'} = \dfrac{U_{\mathrm{MVDC}}}{2} - u_{j1} - (R_0 i_{pj1} + L_0 \dfrac{di_{pj1}}{dt}) + u_{cmf} \\ u_{nj1}^{'} = \dfrac{U_{\mathrm{MVDC}}}{2} + u_{j1} - (R_0 i_{nj1} + L_0 \dfrac{di_{nj1}}{dt}) + u_{cmf} \end{cases}, \ (j = b, c) \tag{3.5}$$

where $u_{pa1}^{'}$ and $u_{na1}^{'}$ are the post-fault arm voltages of Phase-a; $u_{pj1}^{'}$ and $u_{nj1}^{'}$ are the post-fault arm voltages of the healthy phases. In the faulty path through the MMC structure, the faulty currents will be unevenly introduced to all arm currents resulting in a power transfer imbalance in the power modules. Moreover, the imbalance also induces voltage and current fluctuation in the LVDC voltage and current. From (3.4) it can be seen that the fundamental voltage component is canceled by the faulty CM voltage resulting in a decline of the corresponding arm current. Besides, the DC components of the arm currents decay as well since energy can no longer be transferred in this phase. On the contrary, the fundamental and DC components of the arm currents in the healthy phases increase, as given in (3.5).

The impedance of the faulty close-loop determines the amplitude of the faulty zero-sequence current under steady-state. The steady-state SLG fault current can be calculated as,

$$I_{SLGf\,(steady)} = \frac{u_{gm}}{Z_g + R_{f-\mathrm{AC}}} \sin(\omega_0 t + \pi) \tag{3.6}$$

According to (3.6), the grounding impedance can effectively limit the zero-sequence fault current, where Z_g is the total grounding impedance, and $R_{f\text{-AC}}$ is the resistance of the fault point. Moreover, the grounding impedance selection is also determined by the connected distribution systems. To ensure consistency with the existing protection schemes used in the connected grids, the grounding design for the MMC-SST should choose schemes from the same category, being either the large fault current type or small fault current type. In the demonstrated case, high impedance grounding is preferred to meet the demands of the ungrounded MVAC and MVDC grids. Furthermore, the MVDC bus voltage can still be properly controlled under fault scenarios such that fault-tolerant operation can be realized.

Assuming the SPG fault occurred on the MVDC positive pole, the faulty circuit is created by the upper arms of the MMC structure and the grounding points, as shown in Figure 3.5.

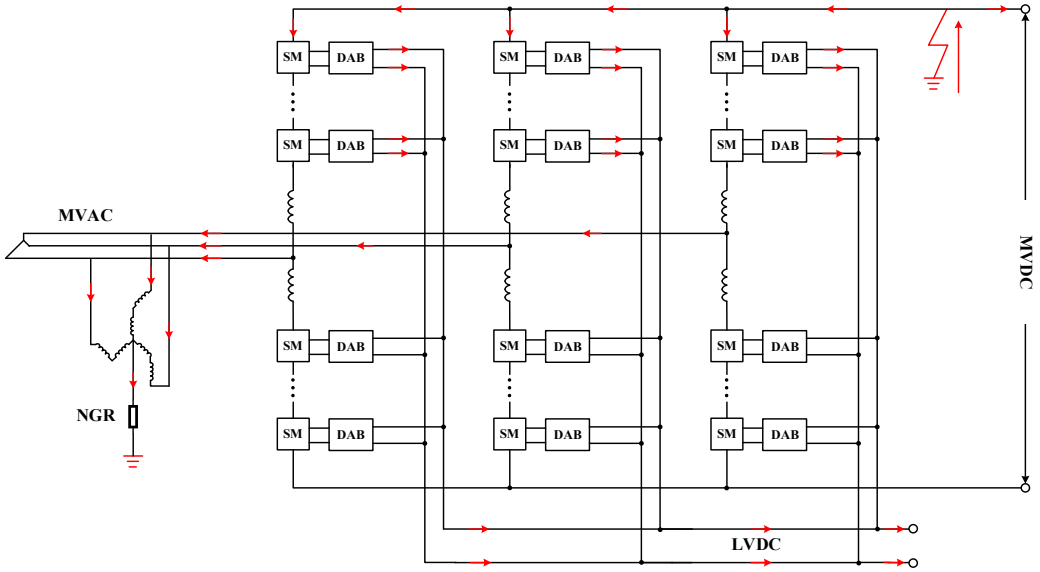

Figure 3.5 SPG fault circuit of the iMMC-SST

Figure 3.6 illustrates the single-phase equivalent circuit. The SM DC capacitor is discharged, in which $C_a=C_{SM}/N_1$ is the equivalent capacitance of a converter arm; N_1 is the number of inserted SMs in the arm when the fault occurs; L_0 is the arm inductance; L_g and R_g are the inductance and resistance of the grounding scheme, respectively; $R_{f\text{-}DC}$ is the equivalent resistance of the fault point, and R_{loss} represents the total resistance of the fault circuit.

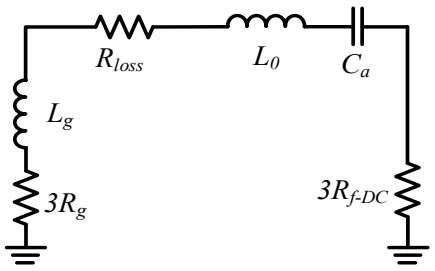

Figure 3.6 Simplified SPG fault circuit

During the transient state of a fault, the iMMC-SST is still under its normal condition operations. The fault current in the shown loop is mainly composed of the discharging current of the SM capacitors connected to the faulty pole. According to

Figure 3.6, the equivalent circuit under the transient state is a second-order capacitor discharging circuit with known initial conditions [85]. Based on KVL, we have:

$$(L_0 + L_g)C_a \frac{d^2u_c(t)}{dt} + (3R_g + 3R_{f-DC} + R_{loss})C_a \frac{du_c(t)}{dt} + u_c(t) = 0 \tag{3.7}$$

The corresponding equivalent SM capacitor discharging current can be expressed as:

$$i_c'(t) = -C_a \frac{du_c(t)}{dt} \tag{3.8}$$

The solution of (3.7) can be expressed as:

$$u_c = A_1 e^{p_1 t} + A_2 e^{p_2 t} \tag{3.9}$$

$$\begin{aligned} p_{1,2} &= -\frac{(3R_g + 3R_{f-DC} + R_{loss})}{2(L_a + L_g)} \pm \sqrt{\left(\frac{3R_g + 3R_{f-DC} + R_{loss}}{2L_a + 2L_g}\right)^2 - \frac{1}{(L_a + L_g)C_a}} \\ &= -\alpha \pm \sqrt{\alpha^2 - \omega^2} \end{aligned} \tag{3.10}$$

Here, A_1 and A_2 are determined by the initial conditions of the capacitor voltage and current. As high resistance grounding is adopted and $(3R_g+3R_{f\text{-}DC}+R_{loss})/2(L_0+L_g)>1/(L_g+L_0)C_a$, the fault circuit is under overdamped condition. The capacitor current can be rewritten as:

$$i_{cap}'(t) = \frac{0.5U_{\mathrm{MVDC}}}{\omega L} e^{-\delta t} \sin(\omega t) \tag{3.11}$$

where $\delta=(3R_g+3R_{f\text{-}DC}+R_{loss})/2(L_0+L_g)$, and $\omega^2=1/(L_0+L_g)C_a-\delta^2$. In this condition, assuming the MMC structure still works under normal control, the steady-state fault current at the grounding point is

$$I_{SPGf(steady)} = 0.5U_{\mathrm{MVDC}} / (R_g + R_{f-DC}) \tag{3.12}$$

According to (3.11) and (3.12), the fault current amplitude is determined by the grounding resistance R_g and the resistance at the fault point $R_{f\text{-}DC}$. Therefore, the fault current can be limited by varying the value of R_g to protect the MMC-SST. The potential fault-tolerant operation can be achieved with this grounding scheme. Besides,

coordination with the existing relay protection can be achieved to keep the consistency of the system relay protection.

However, before the SPG fault is cleared, fault ride-through operation is only suitable for cases with relatively small fault current to prevent possible equipment damage and magnetic saturation of the zig-zag transformer. Here, the fault currents under both the SLG and SPG conditions in both transient and steady states can be effectively suppressed by the neutral ground resistor (NGR, R_g) to a certain value to meet the requirement of the connected distribution systems.

Small grounding fault current designs are normally adopted in ungrounded MV systems, where the current amplitude is generally limited to below 10A in 10kV–66kV MV networks. The value of the NGR is determined with considerations of both MVAC and MVDC fault conditions. In SLG faults, the faulty voltage's peak value equals the phase voltage (5.77kV). For SPG faults, the maximum fault voltage is half of the MVDC bus voltage (10kV). The corresponding line impedance is ignored in the calculation. Thus, the NGR can be calculated as,

$$\text{MVAC: } R_g \approx \frac{\Delta U}{I_{\max}} = \frac{U_{com\_SLG}}{I_{\max}} = \frac{10\,\text{kV}}{\sqrt{3}} \cdot \frac{1}{10\,\text{A}} \approx 577\,\Omega \tag{3.13}$$

$$\text{MVDC: } R_g \approx \frac{\Delta U}{I_{\max}} = \frac{U_{com\_SPG}}{I_{\max}} = \frac{10\,\text{kV}}{10\,\text{A}} = 1\,\text{k}\Omega \tag{3.14}$$

The NGR with 1kΩ is selected to be implemented on the MVAC port of the iMMC-SST. And the corresponding capacity of the zig-zag transformer can be calculated according to (3.1) - (3.3) where S_e equals 3.175 kVA.

- LV side of the iMMC-SST

Similarly, the grounding schemes on the LV side of the iMMC-SST should keep consistent with the existing protection and grounding schemes used in the LV grids. Instead of using the zig-zag transformer on the LVAC port, the artificial grounding points can also be created on the LVDC port via split resistors or capacitors. Based on the assumption, the LVAC and LVDC distribution systems are also ungrounded (IT type).

Under this scenario, the high-resistance grounding scheme is also adopted on the LV side of the iMMC-SST.

The fault analysis under different states can be applied to the LV side of the iMMC-SST as well. Though the objectives of the grounding scheme design for the LV side of the SST are different from those of the MV side, high-resistance grounding is also preferred in LV ports of the iMMC-SST with IT-type LV distribution systems to maintain the consistency of the protection and grounding schemes with those implemented in the LV grids. To save cost and volume on the LV side, the NGR is placed at the neutral point of the LVDC port formed by the split capacitors instead of using the artificial neutral point created by the bulky grounding transformers, as shown in Figure 3.7.

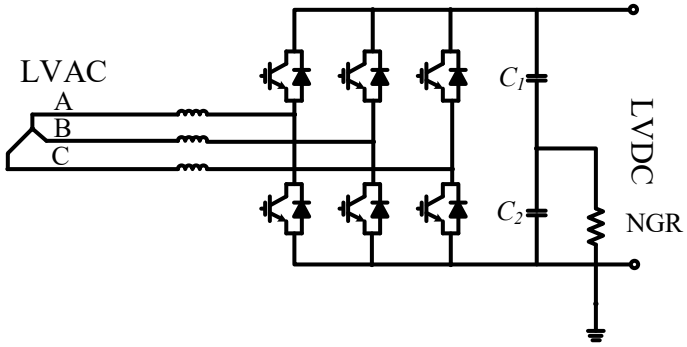

Figure 3.7 LV-side grounding scheme of the iMMC-SST

The fault current amplitude should be limited below 10A to keep the consistency of the protection and grounding scheme used in the LV distribution systems. The NGR used in the LV distribution system equals 40Ω.

3.3.2. Simulation Results

The grounding schemes designed for the iMMC-SST are tested in a MATLAB/Simulink model. The parameters of the iMMC-SST system for simulation are summarized in Table 3.1. Since the LV side converter is independent of the iMMC-SST, the converter is ignored in the simulation. Hence, only three types of fault conditions are considered. In the simulation, the high-resistance grounding scheme is implemented at both MVAC and LVDC ports of the iMMC-SST.

Table 3.1 iMMC-SST Parameters for the Simulation

Symbol	Description	Value	Symbol	Description	Value
P	Rated power	2 MVA	V_{SM_cap}	Submodule capacitor	650 μF
f_0	Fundamental frequency	50 Hz	L_0	MMC Arm inductor	16 mH
V_{MVAC}	MVAC voltage (line-to-line)	10 kV	N	HFT turns ratio	1666:800
V_{MVDC}	MVDC voltage	20 kV	f_d	Switching frequency of the DABs	6 kHz
V_{LVAC}	LVAC voltage (line-to-line)	380 V	$f_{SW\text{-}MMC}$	Switching frequency of the MMC	1 kHz
V_{LVDC}	LVDC voltage	800 V	$f_{SW\text{-}LVcon}$	Switching frequency of the converter	2 kHz
N_{arm}	Submodule number per arm	6	L_s	Leakage inductance of the DABs	1 mH

- Results of the MV-Side Faults

On the MV side, to show the feasibility of the high-resistance grounding scheme, the selected 1 kΩ NGR is compared with the solidly grounded system under both MV SLG and SPG fault conditions. The results of the MV side under SLG fault with the solid grounding and 1 kΩ NGRs are given in Figure 3.8 and Figure 3.9, respectively, including the MVAC phase voltages, MVDC bus and pole voltages, arm currents, SM capacitor voltages, fault circuit currents, and LVDC side voltages and currents. In these two sets of waveforms, an SLG fault occurs at 0.45s in the Phase-a of the MVAC system. In Figure 3.8(a), the faulty MVAC phase voltage drops to zero and the healthy phase voltage increase to the line voltage level because the fault current amplitude suppressed by the large NGR will not affect the operation of the iMMC-SST. Similarly, the shifted neutral point also causes the fluctuation of the pole voltages, as depicted in Figure 3.8(b). In Figure 3.8(c) and (d), the fault does not influence the arm currents and SM capacitor voltages which implies the system is not affected. In Figure 3.8(e), the fault currents indicate that their amplitudes are effectively limited below 10A by the NGR. On the LVDC side, the voltages and currents keep the same as those under normal conditions.

On the other hand, different fault characteristics can be obtained when the solid grounding scheme is applied at the MVAC port. The large fault current depicted in Figure 3.9(e) will be transferred to the MMC part and will deteriorate the system performance, as shown in Figure 3.9(c) and (d). The arm currents are distorted, leading to the three-

phase current imbalance. Moreover, the SM capacitor voltage balance is interrupted. Besides, except for the MVDC pole voltages, a fundamental frequency component is introduced in the MVDC bus voltage, as illustrated in Figure 3.9(b). However, in Figure 3.9(f), the LVDC side voltages and currents are not affected due to the galvanic isolation realized by the HFTs.

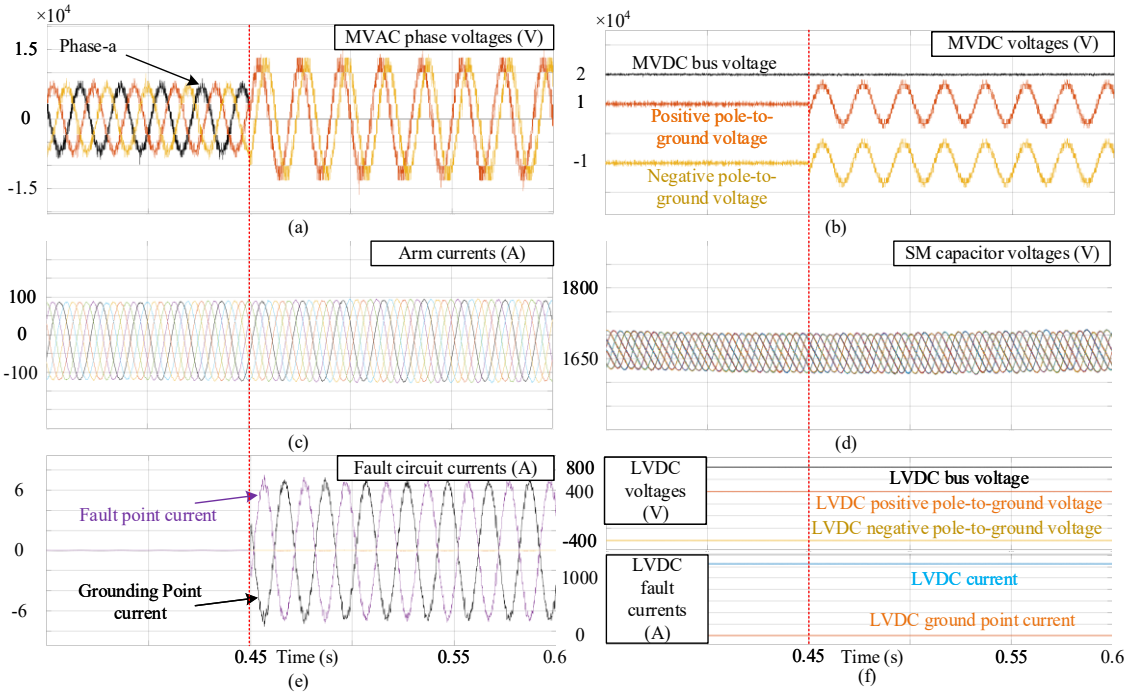

Figure 3.8 MV SLG fault simulation results with 1 kΩ NGR.

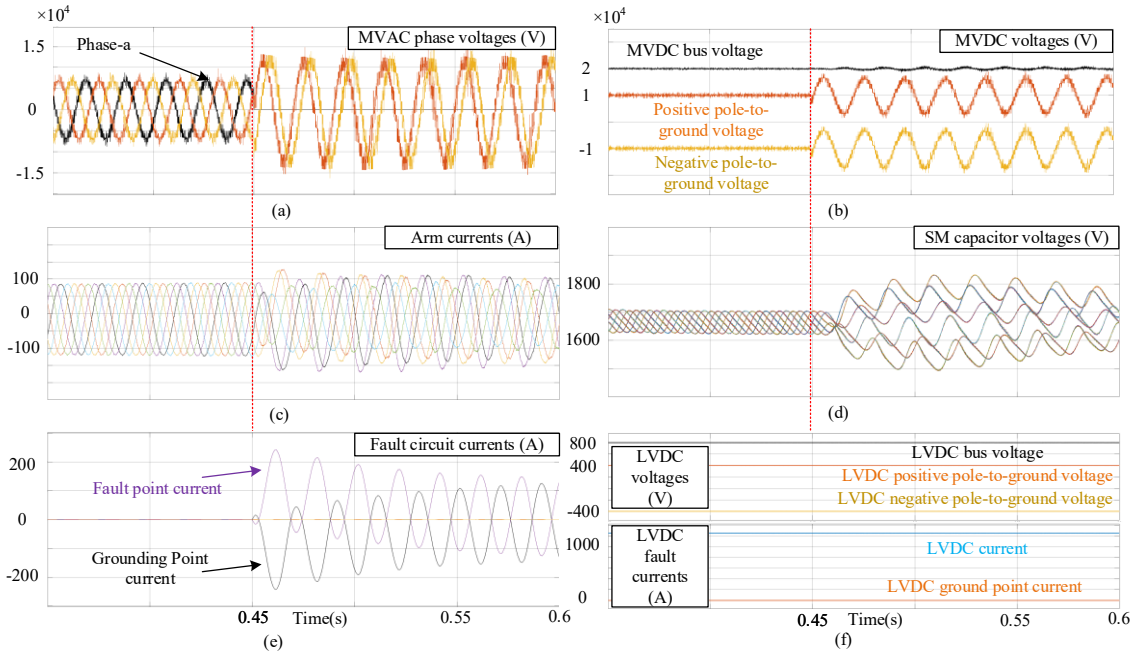

Figure 3.9 MV SLG fault simulation results with the solid grounding.

The SPG fault simulation results with different grounding schemes are presented in Figure 3.10 and Figure 3.11. As shown in Figure 3.10(a) and (b), a CM DC bias voltage is injected in the neutral point of the MV side of the iMMC-SST. The MVDC bus voltage is not affected when 1 kΩ NGR is applied. The faulty MVDC pole voltage drops to zero, and the healthy one is doubled. The arm currents and the SM capacitor voltages are distorted such that the normal operation cannot be maintained. In Figure 3.10(e), the fault current is also restricted below 10 A by the NGR. On the LV side of the iMMC-SST, the DC voltages and currents are not affected due to the galvanic isolation of the HFTs.

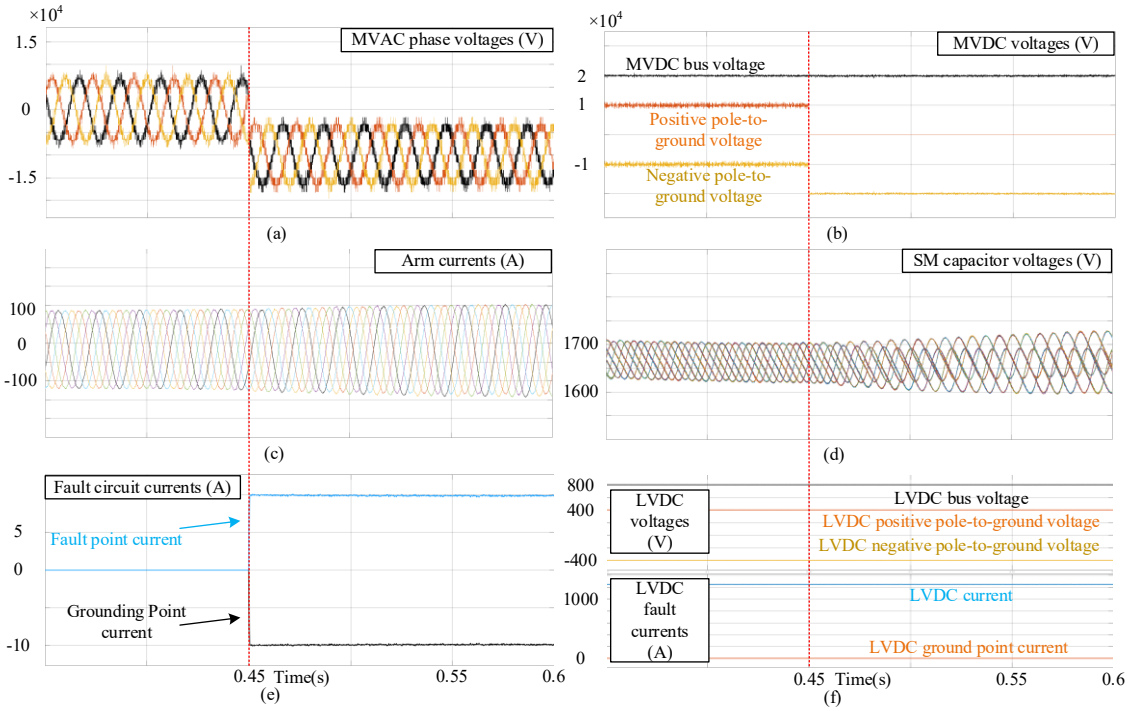

Figure 3.10 MV SPG fault simulation results with 1 kΩ NGR.

However, when the solid grounding scheme is adopted, the iMMC-SST cannot maintain its normal operation under SPG fault conditions. Under this condition, the fault current amplitude reaches around 1300 A, as illustrated in Figure 3.11(e). Due to the neutral point shift caused by the SPG fault, the three MVAC phase voltages cannot be kept, as depicted in Figure 3.11(a). In Figure 3.11(b), since the fault current flows through the MMC part, deteriorating its control, the MVDC voltages cannot be guaranteed as well. Moreover, Figure 3.11(c) and (d) show that the arm currents and SM capacitor voltages are also out of control owing to the overcurrent issue. Unlike the previous fault conditions, the LVDC-side voltages and currents are affected by the MV-side SPG fault conditions. In Figure 3.11(f), because of the unbalanced power transferred by the DAB modules on each phase, neither the LVDC voltages nor currents can be maintained.

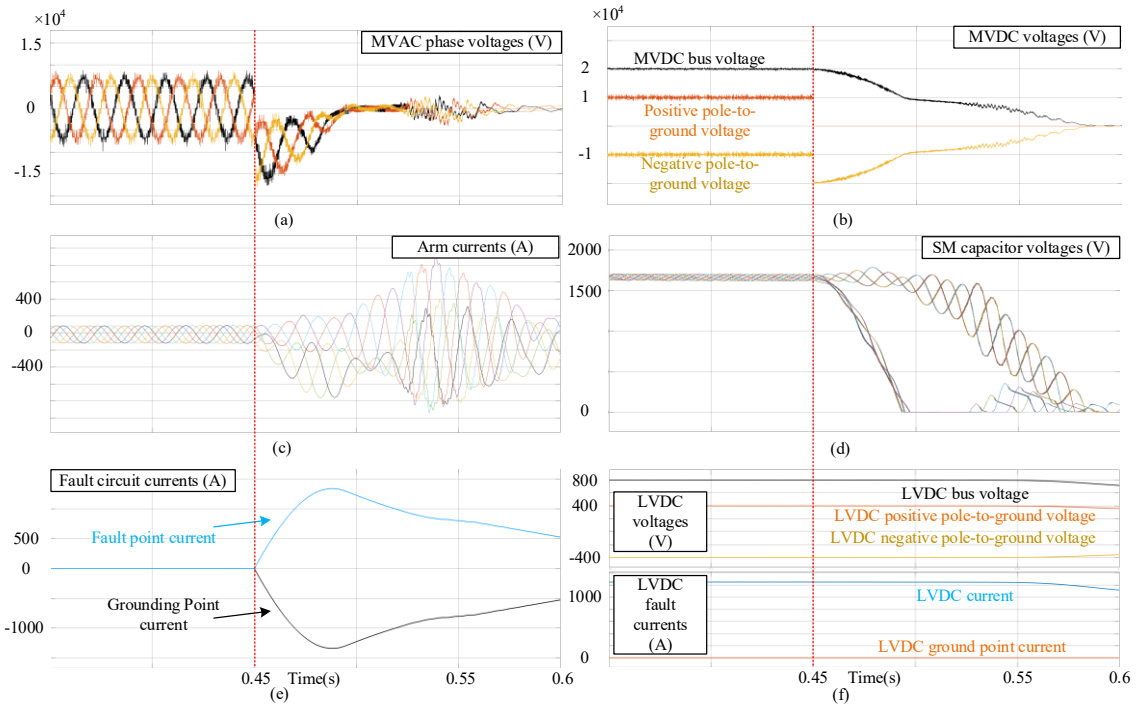

Figure 3.11 MV SPG fault simulation results with the solid grounding.

- Results of the LVDC-Side Fault

Because the LV-side converter is independent of the iMMC-SST control, it is omitted in the simulation test. Thus, only SPG fault conditions are considered in the LV-side of the iMMC-SST. Like the MV-side, a comparison between the high-resistance grounding and the solid grounding scheme is demonstrated. As shown in Figure 3.12, the MV side is not affected due to the galvanic isolation. The faulty LVDC pole voltage drops to zero on the LV side, and the healthy one is doubled, as illustrated in Figure 3.12(e). The LVDC bus voltage control is maintained the same as that under normal operation.

The MVDC and the LVDC voltages show the same fault characteristics as those with the high-resistance grounding scheme when the solid grounding scheme is applied at the midpoint of the MVDC bus. The MVAC phase voltage is also not affected under this condition. However, in contrast to the results using a high-resistance grounding scheme, the simulation results reveal different fault characteristics with the solid grounding scheme at the LVDC port, as depicted in Figure 3.13. With the solid grounding scheme, a large fault current spike (more than 150 kA) appears in the grounding point and the fault point because of the LVDC capacitor discharging and the

low grounding impedance of the fault circuit. The instantaneous capacitor is discharged, leading to the sudden change of the power transferred by the DAB modules of the MMC part, and the SM capacitor voltage drop is shown in Figure 3.13(d). Additionally, the arm currents shown in Figure 3.13(c) increase and gradually regulate their normal values.

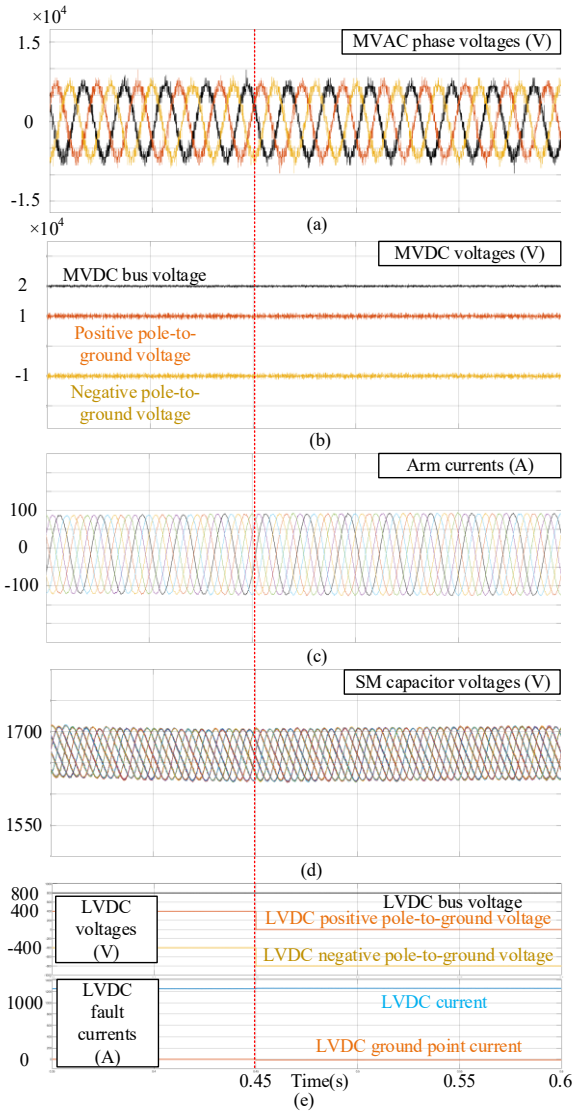

Figure 3.12 LV SPG fault simulation results with 40 Ω NGR.

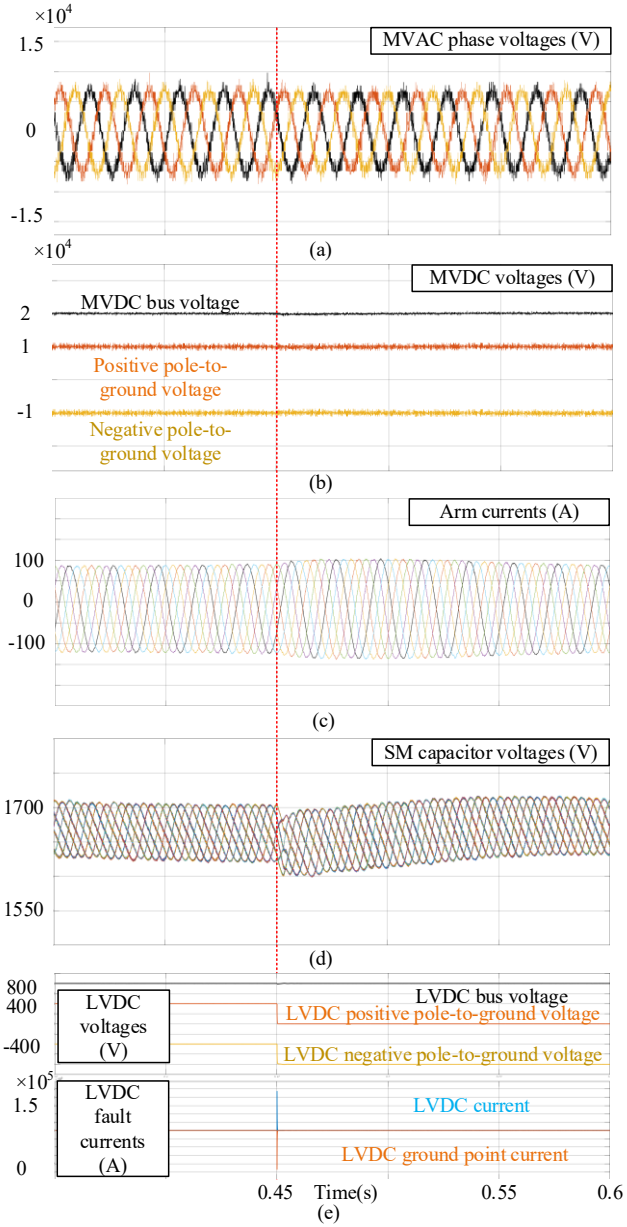

Figure 3.13 LV SPG fault simulation results with solid grounding scheme.

The simulation results show the agreement with the analysis presented in the previous section. By adopting the high-resistance grounding scheme on both the MV and LV sides of the iMMC-SST, the fault current can be significantly limited without destroying the device. Furthermore, the designed grounding scheme maintains consistency with the existing grounding schemes used in the connected distribution systems to prevent the spurious triggering of the protection schemes and devices.

3.3.3. Conclusion

To save cost and volume, line-frequency transformers traditionally used at the AC ports can be eliminated. However, this makes the system more vulnerable to potential fault propagation issues and overvoltage and overcurrent problems, which affect the normal operation of the SST and deteriorate the service of the connected distribution networks. In this chapter, the models of both SLG and SPG faults are analyzed in detail for the iMMC-SST system to investigate the fault behaviors. The analysis reveals that the faulty CM voltages cause the fault currents. Due to the HFTs used in the DABs, the proposed iMMC-SST system is galvanically isolated and divided into two parts to arrange the grounding scheme. The amplitudes of the main fault current components are determined by the impedance of the fault circuit loop. In both SLG and SPG conditions, the fault current always flows through the iMMC-SST. In the case study, the grounding scheme design impedance should depend on the existing grid-side grounding and relay protections so that consistency can be maintained.

A zig-zag transformer is selected to form an artificial neutral point to implement the grounding scheme on the MV side. Comparing with other grounding devices such as the star-connected reactor and traditional interfacing transformer, the zig-zag transformer has the advantages of low volume and capacity, low loss, and small zero-sequence impedance. Moreover, high resistance grounding with 1 kΩ NGR is applied to restrict the transient- and steady-state fault current to protect the system and meet the relay protection requirement of the corresponding distribution systems. In the LV side of the iMMC-SST, the solid grounding scheme is implemented at the natural neutral point of the LVDC port to avoid overcurrent caused by the fault conditions. Besides, the controllable fault current can be used to achieve fast fault detection and isolation to guarantee personnel and device safety.

The performance and parameter design of the grounding scheme is evaluated in MATLAB/Simulink under both SLG and SPG fault conditions. The simulation results verify the effectiveness of the grounding scheme designed for the proposed iMMC-SST system in containing the fault behaviors to meet different requirements of the connected distribution systems. The MV side system can ride through the fault condition in a certain period with a degraded service. For the LV side, the current spike yielded by the DC

capacitors can be significantly limited to protect the system's safety with the help of the designated NGR.

3.4. Inclusion of Relay Protections in the Grounding Scheme Design

Protection schemes in AC or DC distribution systems are generally evaluated based on four basic metrics: speed, selectivity, sensitivity, and reliability [86]. In most scenarios, protection for the distribution system and the connected electrical equipment is always done by coordinating the grounding schemes and the relay protections implemented on the adjacent feeders.

However, conventional relay protection methods and devices may not function properly when SSTs are introduced to the distribution systems because of the changed fault characteristics [28]. Conventional relay protections are usually separately designed for AC or DC distribution systems. Due to the integration of the AC and DC grids and the mutual influence, relay protection devices will encounter more complicated abnormal conditions such as fault propagation in future distribution systems [87], [88]. The characteristics of SLG/SPG faults will be transferred to the healthy DC/AC feeders and affect the performance of the corresponding relay protections.

In terms of relay protection methods, conventional relay protection devices may be tripped spuriously if directional protection is adopted when an AC side fault propagates to the DC side via the SST. This is mainly because of the possible reverse power transfer transients. Another case is that conventional relays with current sensitivity and selectivity levels will not suffice when differential protection is used. Furthermore, if distance protection is applied, the protection scope will decrease due to the system impedance. The large harmonic currents introduced by the transient fault propagation could cause mis-triggering of the DC relay protection devices and commutation failure if AC fault occurs.

Additionally, since the power electronic elements in the SSTs are more vulnerable and sensitive, conventional relay protection devices cannot properly deal with the abnormal conditions [89]. Relay protection devices with higher sensitivity and selectivity are therefore necessary. The traditional protection methods [90]–[93] should

also be modified and upgraded with these new protection devices, sensors with a high sampling rate, and fast communications systems [94], [95]. For example, the traditional differential protection used in the line-frequency transformer cannot be used to protect the SSTs because of the altered fault characteristics of future distribution networks. At present, solid-state relays, such as solid-state circuit breakers (SSCB) [96]–[99], and advanced current limiters [97], [100], [101] shown in Figure 3.14, are becoming more attractive due to their fast switching speed, high reliability, capability in suppressing fault current and arc-flash, and compact size [88]. These devices also come with inherent disadvantages such as high conduction loss, short device lifespan, and high cost, hindering widespread use. It is worth noting that some of the MMC-based SSTs have intrinsic DC blocking capability owing to their specific submodule structures [102]. In MMCs with full-bridge submodules, clamp-double submodules, and three-level cross-connected submodules, the protection device such as DC circuit breakers, can be saved to further reduce the volume and investment of the system at the cost of the increased use of the power electronic elements [103]. The coordination of the relay protection and grounding scheme design of the SSTs used in the future distribution system should be comprehensively considered to improve the reliability and robustness.

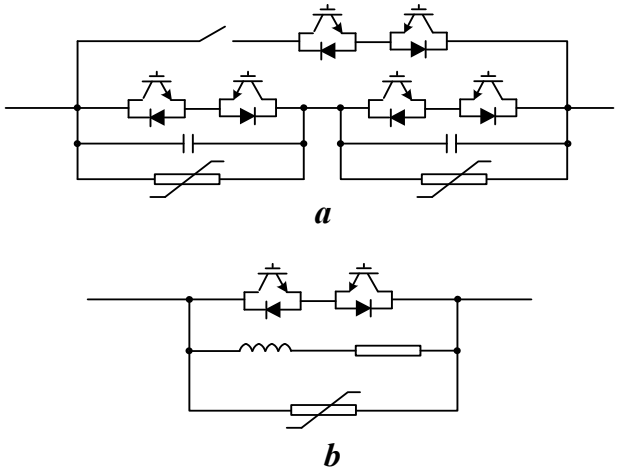

Figure 3.14 Typical relay protection devices (a) hybrid solid-state circuit breaker; (b) solid-state current limiter

Chapter 4.

Residual Power Transfer Capability of the iMMC-SST with SM IGBT Open-Circuit Fault

Due to the flexible power transfer feature, iMMC-SST is becoming more attractive in the hybrid distribution system to integrate different grids [104], [105]. A large number of IGBT devices used in the iMMC-SST can be regarded as the potential fault sources, which include the OC and SC faults [51], [106]. The SC fault is generally associated with overcurrent, which can be solved by the system's built-in protection schemes. On this basis, the corresponding fault analysis, fault diagnosis, and fault-tolerant schemes for the SC fault will not be further discussed in this chapter. The power switch OC fault will exhibit different behaviors when different power switching elements are adopted. Only the scenarios with IGBTs with anti-parallel connected diodes is considered in this thesis since the undamaged diodes can still carry current. Thus, contrary to the SC fault, the OC fault is hard to identify due to the less-severe fault characteristics, making it possible to realize certain fault-tolerant schemes [45], [76]. The fault detection and fault-tolerant approaches of the MMC-side SM IGBT OC fault have been studied in the past decade. The fault diagnosis must be completed before any fault-tolerant operation [107]. Several fault diagnosis methods have been presented for the traditional MMC applications relying on the magnitude changes of the SM capacitor voltages and the MMC arm currents [108]–[111]. These works only considered the inverter mode MMC operation. Under rectifier mode, with the capacitor voltage of the faulty SM kept the same as the other SMs, a fault diagnosis method based on accumulations of the errors between individual capacitor voltage increment and maximum capacitor voltage increment in each fundamental period is developed in [112].

However, these methods cannot be applied to the iMMC-SST directly. Its multiport topology extends the operating range of the iMMC-SST, and more operation modes need to be considered for it [8]. The SM IGBT OC fault behaviors are quite different from the traditional MMC applications [113]. In an iMMC-SST, the faulty SM capacitor voltage may be balanced when the system operates under some faulty modes. Therefore, most of the abovementioned fault diagnosis methods relying on capacitor voltage changes cannot correctly identify and locate the fault conditions. Additionally,

based on the unique SM IGBT OC fault characteristics of the iMMC-SST, the faulty SM can still transfer power with different levels by applying suitable fault-tolerant operation.

This section comprehensively analyzes the SM IGBT OC faults with considering the iMMC-SST's different operation modes. In addition, fault behaviors such as fault propagation in the SST and its residual power transfer capability are investigated. This analysis offers the ground for developing fault diagnosis and fault-tolerant schemes for the iMMC-SST to improve the system reliability with less initial cost and size.

4.1. Comparison with the conventional MMC Applications

The SM IGBT OC fault behaviors are different from the conventional MMC applications due to the iMMC-SST's complex operation modes and the unique power module topology. The iMMC-SST twelve operation modes are summarized in Table 2.1 in terms of the power direction of each port. Different from the analysis in [112], the iMMC-SST operation cannot be defined as the inverter or rectifier modes. According to (2.27), the power portion transferred by each port can be flexibly dispatched among the ports to achieve specific operation modes, leading to an erratic SM capacitor voltage behavior. For example, when the system operates under Mode 7, the power supplied from the LVDC port can be flexibly distributed to the MV ports. Besides, the system can operate in Modes 2 or 6, where the LVDC loads are supplied by either the MVAC or MVDC ports. Thus, the range of the DC component under these modes is [$-U_{LVDC}I_{LVDC}/3U_{MVDC}$, 0].

Besides, extra current paths can be created by the DAB side of the power module. Under SM IGBT OC faults, the increasing charge of the SM capacitor can be released by the DAB module so that the SM voltage will not increase as fast as that of the traditional MMC applications. Hence, the previously SM capacitor voltage increment-based fault diagnosis schemes for the traditional MMC applications are not suitable for the iMMC-SST. However, the faults lead to a rapid increase in the input current of the DAB module. Therefore, the new fault characteristics can also indicate the SM IGBT OC fault via the DAB side. Additionally, the potential unidirectionally fault-tolerant operation can be developed to maintain the power transfer capability of the faulty unit.

4.2. iMMC-SST SM IGBT OC fault Analysis

4.2.1. Impact on the Faulty SM

As shown in Figure 4.1 and Figure 4.2, two possible IGBT OC fault conditions may happen in a HBSM. In Figure 4.1(c), under the S_1 fault, the SM capacitor-discharge period is replaced by a bypassing period during which the SM may not maintain its balanced condition due to the increase of its capacitor voltage. When a fault occurs in S_2, the bypassing process is replaced by a charging period where the SM would be charged with extra time, and the capacitor voltage will therefore increase as well (Figure 4.2(b)). As shown in Figure 2.11(b) and (c), when S_1 fails, the shaded area with negative arm currents will disappear so that the SM capacitor voltage cannot be discharged. Likewise, the SM bypass periods (white area) with positive arm current will be changed under S_2 failure leading to extra insertion periods of the faulty SM. Because the SM faults share the same features, the analysis of the lower arm faults is similar.

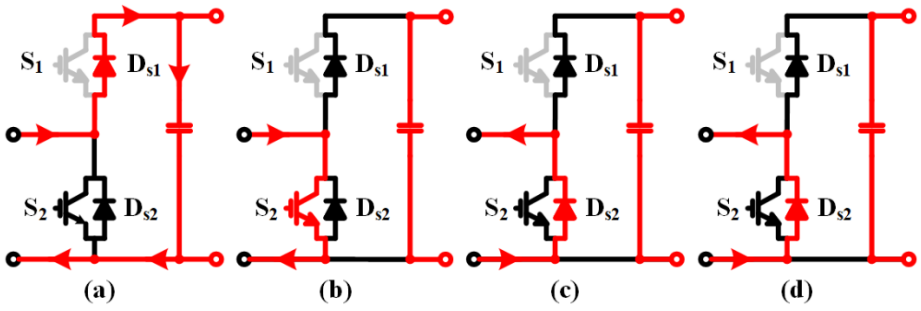

Figure 4.1 **S_1 fault condition (a) (1, 0) & i_{ap}>0; (b) (0, 1) & i_{ap}>0; (c) (1, 0) & i_{ap}<0; (d) (0, 1) & i_{ap}<0.**

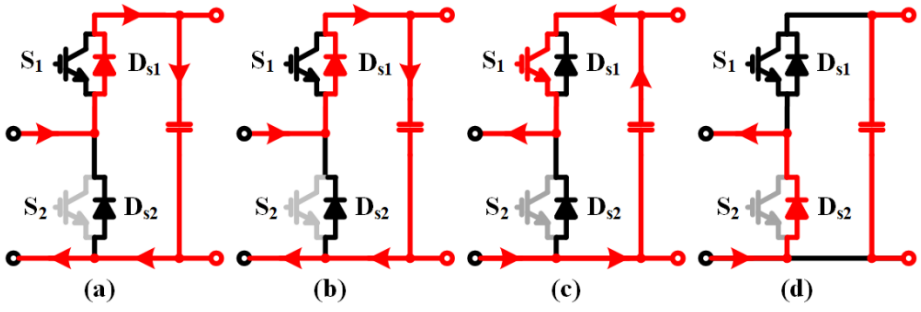

Figure 4.2 **S_2 fault condition (a) (1, 0) & i_{ap}>0; (b) (0, 1) & i_{ap}>0; (c) (1, 0) & i_{ap}<0; (d) (0, 1) & i_{ap}<0.**

According to (2.27), the DC component of the arm currents may vary under the same operation mode, and as a result, the SM may exhibit different post-fault behaviors depending on the actual arm currents. The detailed fault behaviors under different cases are summarized in Table 4.1.

Table 4.1 Fault Behaviors under Different iMMC-SST Operation Modes

Mode	i_{ap}	Switching State Under S_1 Fault		Switching State Under S_2 Fault	
		(1, 0)	(0, 1)	(1, 0)	(0, 1)
Type I	>0	No (*N*)	No (*N*)	No (*N*)	Charge (*N*+1)
Type II	>0	No (*N*)	No (*N*)	No (*N*)	Charge (*N*+1)
	<0	Bypass (*N*-1)	No (*N*)	No (*N*)	No (*N*)
Type III	>0	No (*N*)	No (*N*)	No (*N*)	Charge (*N*)
	<0	Bypass (*N*-1)	No (*N*)	No (*N*)	No (*N*)
Type IV	<0	Bypass (*N*-1)	No (*N*)	No (*N*)	No (*N*)

Type I: When the system operates in the Type I mode, because the arm currents always flow in the positive direction, the SMs of the MMC always switch between the operation states of (a) and (b) in Figure 2.10. Since S_1 does not carry current in these states, as shown in Figure 2.11(a), if an S_1 fault happens, the SM will not be affected by the failed S_1, and the faulty power module can continue to be used without fault-tolerant operation. However, if S_2 fails, this SM will always be inserted in the faulty arm (*N*+1 SMs are inserted), and its capacitor will keep charging under both switching states. The extra SM inserted and its increasing capacitor voltage of the faulty arm result in arm voltage and SM voltage imbalance, which may deteriorate the entire system's operation.

Type II: As shown in Figure 2.11(b), the arm currents polarity will change under the Type II operation mode. The discharge process of the faulty SM is replaced by the bypassing period under S_1 fault with i_{pa}<0. With the DAB still under normal mode operation and not providing extra discharging support, the SM capacitor cannot be properly discharged in this condition, increasing its voltage, u_{cpa}. The charge transferred to the faulty SM capacitor and the capacitor voltage increment during i_{pa}>0 are given in (5.1).

$$
\begin{aligned}
Q_{\mathrm{II\_1\_S1}} &= \int_0^{t_{11}} i_{ap}\,dt + \int_{t_{12}}^{t_{11}+T} i_{ap}\,dt \\
&= \frac{I_{gm}}{\omega}\sqrt{1-\left(-2I_{\mathrm{MVDC}}/3I_{gm}\right)^2} + \frac{2I_{\mathrm{MVDC}}}{3\omega}\arccos\left(2I_{\mathrm{MVDC}}/3I_{gm}\right) \\
\Delta u_{\mathrm{II\_1\_S1}} &= \frac{Q_{\mathrm{II\_1\_S1}}}{C}
\end{aligned}
\tag{5.1}
$$

For i_{pa}<0, as can be seen from Figure 2.11(b), the charge transferred away from the capacitor ($Q_{II\_2\_S1}$), and the voltage decrement ($\Delta u_{II\_2\_S1}$) is equal to zero. Thus, the faulty SM capacitor voltage cannot be kept because $\Delta u_{II\_1\_S1} > \Delta u_{II\_2\_S1}$. As such, the fault will further result in the increases of i_{dpa} and the power of the faulty power module. Furthermore, the SM capacitor voltage balance control will make the faulty SM operate in the (1, 0) state due to the voltage increase, resulting in an arm voltage imbalance where only N-1 SMs are inserted in the faulty arm.

If S_2 failed, the SM would always be inserted when i_{pa}>0, causing the capacitor to be charged. In addition, the fault will induce arm voltage imbalance, where N+1 SMs will join the operation of the faulty arm. The charge transferred to the faulty SM capacitor and the capacitor voltage increment during the positive period are expressed in (5.2).

$$
\begin{aligned}
Q_{\mathrm{II\_1\_S2}} &= \int_0^{t_{11}} i_{pa}\,dt + \int_{t_{12}}^{t_{11}+T} i_{pa}\,dt \\
&= \frac{I_{gm}}{\omega}\sqrt{1-\left(-2I_{\mathrm{MVDC}}/3I_{gm}\right)^2} + \frac{2I_{\mathrm{MVDC}}}{3\omega}\arccos\left(2I_{\mathrm{MVDC}}/3I_{gm}\right) \\
\Delta u_{\mathrm{II\_1\_S2}} &= \frac{Q_{\mathrm{II\_1\_S2}}}{C}
\end{aligned}
\tag{5.2}
$$

However, the SM behavior will not change when i_{ipa} flows in the negative direction. The charge transferred away from the capacitor, and the voltage decrement are given in (5.3) under this case.

$$
\begin{aligned}
Q_{\mathrm{II\_2\_S2\_max}} &= \int_{t_{11}}^{t_{12}} \left|i_{pa}\right| dt \\
&= \frac{I_{gm}}{\omega}\sqrt{1-\left(-2I_{\mathrm{MVDC}}/3I_{gm}\right)^2} - \frac{2I_{\mathrm{MVDC}}}{3\omega}\arccos\left(2I_{\mathrm{MVDC}}/3I_{gm}\right) \\
\Delta u_{\mathrm{II\_2\_S2\_max}} &= \frac{Q_{\mathrm{II\_2\_S2\_max}}}{C}
\end{aligned}
\tag{5.3}
$$

Under this condition, it can be easily obtained that

$$
\Delta u_{\mathrm{II\_1\_S2}} > \Delta u_{\mathrm{II\_2\_S2\_max}} \tag{5.4}
$$

Therefore, the faulty SM capacitor voltage balance cannot be maintained where i_{dpa} and u_{cpa} will gradually increase.

Type III: As shown in Figure 2.11(c), the SM will show similar fault behaviors as those under the Type II mode with S_1 fault. In this mode, the SM discharging process under state (1, 0) is replaced by a bypassing process during i_{pa}<0 periods. Therefore, the capacitor voltage increment during the positive period ($\Delta u_{III\_1\_S1}$) is greater than the voltage decrement ($\Delta u_{III\_2\_S1}$) with i_{pa}<0. So, the SM capacitor voltage balance cannot be maintained and will result in further arm voltage imbalance since only *N*-1 SMs can participate in the operation of the faulty arm.

When the SM encounters an S_2 fault, the two switching states with negative arm current (i_{pa}<0) will not be influenced. On the other hand, the bypassing process is forced to be changed to a charging process with a positive current direction. However, it should be noted that the capacitor voltage will maintain balance under this condition because the SM balance control will insert the faulty unit to release the extra charge generated by the fault. The charge transferred to the faulty SM capacitor and the capacitor voltage increment during the positive period are given in (5.5).

$$\begin{aligned} Q_{\text{III\_1\_S2}} &= \int_{t_{21}}^{t_{22}} i_{pa}\,dt \\ &= \frac{I_{gm}}{\omega}\sqrt{1-\left(-2I_{\text{MVDC}}/3I_{gm}\right)^2} + \frac{2I_{\text{MVDC}}}{3\omega}\arccos\left(2I_{\text{MVDC}}/3I_{gm}\right) \\ \Delta u_{\text{III\_1\_S2}} &= \frac{Q_{\text{III\_1\_S2}}}{C} \end{aligned} \tag{5.5}$$

With i_{pa}>0, the charge transferred away from the capacitor, and the voltage decrement are demonstrated in (5.6).

$$\begin{aligned} Q_{\text{III\_2\_S2\_max}} &= \int_0^{t_{21}} \left|i_{pa}\right| dt + \int_{t_{22}}^{t_{22}+T} \left|i_{pa}\right| dt \\ &= \frac{I_{gm}}{\omega}\sqrt{1-\left(-2I_{\text{MVDC}}/3I_{gm}\right)^2} - \frac{2I_{\text{MVDC}}}{3\omega}\arccos\left(2I_{\text{MVDC}}/3I_{gm}\right) \\ \Delta u_{\text{III\_2\_S2\_max}} &= \frac{Q_{\text{III\_2\_S2\_max}}}{C} \end{aligned} \tag{5.6}$$

During these operation modes, it can be derived that

$$\Delta u_{\text{III\_1\_S2}} < \Delta u_{\text{III\_2\_S2\_max}} \tag{7}$$

Therefore, the charge of the SM capacitor can be kept in the balanced mode such that the SM capacitor voltage balance will not be affected. Besides, the arm voltage balance is not deteriorated (*N* SMs participate in the normal operation of the iMMC-SST). But it should be noted that the insertion period of the faulty SM will be longer than the

healthy SMs to release the extra charge. Thus, though the SM capacitor voltage balance is maintained, the arm voltage balance control is slightly affected, leading to the circulating current increase and distortion in the MVAC phase current and the MVDC pole current. Moreover, the S_2 fault can still be identified via the increment of u_{cpa} during the positive arm current period [112].

Type IV: Due to the arm currents always flowing in the negative direction in a Type IV mode, during S_1 fault, the faulty SM cannot be inserted during (1, 0) state such that the power cannot be transferred from the LVDC port to the MV ports. Hence, the faulty SM is not capable of achieving any fault-tolerant operations. As shown in Figure 2.11(d), unlike the S_1 fault, the faulty SM will not be affected during the S_2 fault, and therefore it can retain the full power transfer capability without using fault-tolerant schemes. However, the S_2 fault cannot be detected in this scenario because both the arm currents and the SM capacitor voltages retain the same behaviors as normal conditions.

4.2.2. Impact on the iMMC-SST

According to (2.8) and (2.9), the MV-side power and the circulating current are affected by the CM voltage u_{coma} (=u_{pa}+u_{na}) and the DM voltage u_{diffa} (=0.5(u_{na}-u_{pa})), respectively. And they can be rewritten as the following equations based on (2.31) and (2.32).

$$u_{coma\_norm} = \frac{N}{48\omega C}\left[\begin{array}{l}\underbrace{48\omega C U_c + 6MI_{gm}\sin(\delta-\varphi)}_{DC} \\ \underbrace{-9MI_{gm}\sin(2\omega t-\delta-\varphi)+4M^2 I_{\mathrm{MVDC}}\sin(2\omega t-2\delta)}_{2nd}\end{array}\right] \tag{5.8}$$

$$u_{diffa\_norm} = -\frac{N}{192\omega C}\left[\begin{array}{l}\underbrace{\left(24+3M^2\right)I_{gm}\cos(\omega t-\varphi)}_{1st} \\ \underbrace{-16MI_{\mathrm{MVDC}}\cos(\omega t+\delta)-96M\omega C U_c\sin(\omega t-\delta)}_{1st} \\ \underbrace{-3M^2 I_{gm}\cos(3\omega t-2\delta-\varphi)}_{3rd}\end{array}\right] \tag{5.9}$$

According to Table 4.1, those influenced modes are always associated with one more or one less SM inserted in the faulty arm, which causes the arm voltage imbalance

and the circulating current increase. When the fault occurred on S_1 with the state (1, 0), the faulty SM will be bypassed, and the number of the inserted SMs in the faulty arm equals (*N*-1) under Type II, III and IV with negative arm current. For the other operation modes, the number of inserted SMs on the faulty arm will always keep *N*. Hence, assuming the switching functions are not changed after the fault happened, the CM and DM voltages with S_1 fault scenarios can be rewritten as

$$u_{coma\_S1\_ft} = -\frac{1}{96\omega C}\left[\begin{array}{l}\underbrace{\left(48\omega CU_c - 96\omega CNU_c\right) + \left(6MI_{gm} - 12MNI_{gm}\right)\sin\left(\delta-\varphi\right)}_{DC} \\ \underbrace{+\left(12I_{gm} + \frac{3}{2}M^2 I_{gm}\right)\cos\left(\omega t-\varphi\right)}_{1st} \\ \underbrace{-8MI_{\mathrm{MVDC}}\cos\left(\omega t-\delta\right) - 48M\omega CU_c\sin\left(\omega t-\delta\right)}_{1st} \\ \underbrace{+\left(18MNI_{gm} - 9mI_{gm}\right)\sin\left(2\omega t-\delta-\varphi\right)}_{2nd} \\ \underbrace{+\left(4M^2 I_{\mathrm{MVDC}} - 8m^2 NI_{\mathrm{MVDC}}\right)\sin\left(2\omega t-2\delta\right)}_{2nd} \\ \underbrace{-\frac{3}{2}M^2 I_{gm}\cos\left(3\omega t-2\delta-\varphi\right)}_{3rd}\end{array}\right] \tag{5.10}$$

$$u_{diffa\_S1\_ft} = \frac{1}{192\omega C}\left[\begin{array}{l}\underbrace{6MI_{gm}\sin\left(\delta-\varphi\right) + 48\omega CU_c + \left(12I_{gm} - 24NI_{gm}\right)\cos\left(\omega t-\varphi\right)}_{DC} \\ \underbrace{+\left(\frac{3}{2}M^2 I_{gm} - 3M^2 NI_{gm}\right)\cos\left(\omega t-\varphi\right)}_{1st} \\ \underbrace{+\left(16MNI_{\mathrm{MVDC}} - 8MI_{\mathrm{MVDC}}\right)\cos\left(\omega t-\delta\right)}_{1st} \\ \underbrace{+\left(96M\omega CNU_c - 48M\omega CU_c\right)\sin\left(\omega t-\delta\right)}_{1st} \\ \underbrace{+9MI_{gm}\sin\left(2\omega t-\delta-\varphi\right) + 4M^2 I_{\mathrm{MVDC}}\sin\left(2\omega t-2\delta\right)}_{2nd} \\ \underbrace{+\left(3M^2 NI_{gm} - \frac{3}{2}M^2 I_{gm}\right)\cos\left(3\omega t-2\delta-\varphi\right)}_{3rd}\end{array}\right] \tag{5.11}$$

In contrast to the normal condition, the components of the CM and DM voltages are increased, leading to the circulating current increment and the voltage and current distortion of all the ports of the iMMC-SST.

Likewise, the faulty SM will be inserted when S_2 fails with the state (0, 1) under Type I, II, and III with positive arm current direction. Under these scenarios, the number of the inserted SM of the faulty arm is *N*+1. The corresponding CM and DM voltages with the S_2 fault scenarios can be expressed as

$$u_{coma\_S2\_ft} = -\frac{1}{96\omega C}\left[\begin{array}{l}\underbrace{\left(48\omega CU_c + 96\omega CNU_c\right) + \left(6MI_{gm} + 12MNI_{gm}\right)\sin\left(\delta-\varphi\right)}_{DC} \\ \underbrace{+\left(12I_{gm} + \frac{3}{2}M^2 I_{gm}\right)\cos\left(\omega t-\varphi\right)}_{1st} \\ \underbrace{-8mI_{\mathrm{MVDC}}\cos\left(\omega t-\delta\right) - 48M\omega CU_c\sin\left(\omega t-\delta\right)}_{1st} \\ \underbrace{-\left(18MNI_{gm} + 9MI_{gm}\right)\sin\left(2\omega t-\delta-\varphi\right)}_{2nd} \\ \underbrace{+\left(4M^2 I_{\mathrm{MVDC}} + 8M^2 NI_{\mathrm{MVDC}}\right)\sin\left(2\omega t-2\delta\right)}_{2nd} \\ \underbrace{-\frac{3}{2}M^2 I_{gm}\cos\left(3\omega t-2\delta-\varphi\right)}_{3rd}\end{array}\right] \tag{5.12}$$

$$u_{diffa\_S2\_ft} = -\frac{1}{192\omega C}\left[\begin{array}{l}\underbrace{6MI_{gm}\sin\left(\delta-\varphi\right) + 48\omega CU_c}_{DC} \\ \underbrace{+\left(12I_{gm} - 24NI_{gm}\right)\cos\left(\omega t-\varphi\right)}_{1st} \\ \underbrace{+\left(\frac{3}{2}M^2 I_{gm} + 3M^2 NI_{gm}\right)\cos\left(\omega t-\varphi\right)}_{1st} \\ \underbrace{-\left(16MNI_{\mathrm{MVDC}} + 8MI_{\mathrm{MVDC}}\right)\cos\left(\omega t-\delta\right)}_{1st} \\ \underbrace{-\left(96M\omega CNU_c + 48M\omega CU_c\right)\sin\left(\omega t-\delta\right)}_{1st} \\ \underbrace{+9MI_{gm}\sin\left(2\omega t-\delta-\varphi\right) + 4M^2 I_{\mathrm{MVDC}}\sin\left(2\omega t-2\delta\right)}_{2nd} \\ \underbrace{-\left(3M^2 NI_{gm} + \frac{3}{2}M^2 I_{gm}\right)\cos\left(3\omega t-2\delta-\varphi\right)}_{3rd}\end{array}\right] \tag{5.13}$$

4.2.3. Residual Power Transfer Capability Consideration

For the systems operating under Type I with S_1 fault and Type IV modes with the S_2 fault, the balanced SM capacitor voltages and arm voltages enable the faulty SM to achieve full power transfer capability. When the system runs under Type III with the S2 fault, the faulty SM can transfer the extra charge away such that the SM capacitor voltage balance will not be influenced. Therefore, the faulty SM can also realize full power transfer capability under this condition. Under these scenarios, the control of the DAB module that is series-connected to the faulty SM does not need to be adjusted to keep its power transfer capability owing to the balanced SM capacitor voltages. While for the other operation modes, the iMMC-SST cannot guarantee its balanced operation if the system control strategy is not changed.

Generally, the system will bypass the faulty SM and activate different fault-tolerant schemes. However, although the system may not be affected under the above-described operation modes, the faulty SM cannot maintain its bidirectional power transfer capability when the iMMC-SST switches to the other working conditions. Moreover, the previously proposed fault-tolerant strategies in the literature based on advanced control can only ensure the faulty SM with unidirectional power transfer capability. They are not suitable for this device if bidirectional power transfer is desired to be maintained.

4.3. Simulation results

Simulations of a five-level iMMC-SST are conducted to verify the fault analysis with different operation modes and fault conditions. The simulation system parameters are listed in Table 4.2. The power transferred under the four operation modes is provided in Table 4.3. The simulation waveforms, including the arm currents, the circulating currents, the first SM capacitor voltages of each phase, the faulty SM input current, and the faulty SM capacitor current, with different fault conditions and operation modes, are illustrated in Figure 4.3-4.10.

Table 4.2 Parameters of the iMMC-SST for Simulation

Parameters	Values	Parameters	Values
MVAC voltage	10 kV	Arm inductance	8 mH
MVDC voltage	20 kV	SM capacitance	650 uF
LVDC voltage	800 V	MMC switching frequency	1 kHz
SM number per arm	12	DAB switching frequency	6 kHz
Transformer turns ratio	1666:800	DAB inductance	1 mH

Table 4.3 Specific Operation Modes for Simulation

Modes	Power
Type I	MVAC: -200 kVA, MVDC: -800 kVA, LVDC: 1 MVA
Type II	MVAC: -600 kVA, MVDC: -400 kVA, LVDC: 1 MVA
Type III	MVAC: -960 kVA, MVDC: 1 MVA, LVDC: -40 kVA
Type IV	MVAC: -200 kVA, MVDC: 1 MVA, LVDC: -800 kVA

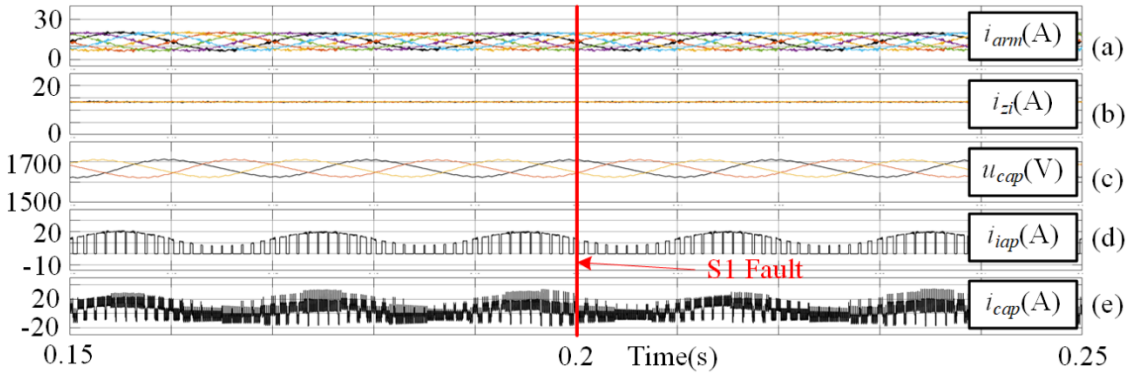

Figure 4.3 **Type I with S_1 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

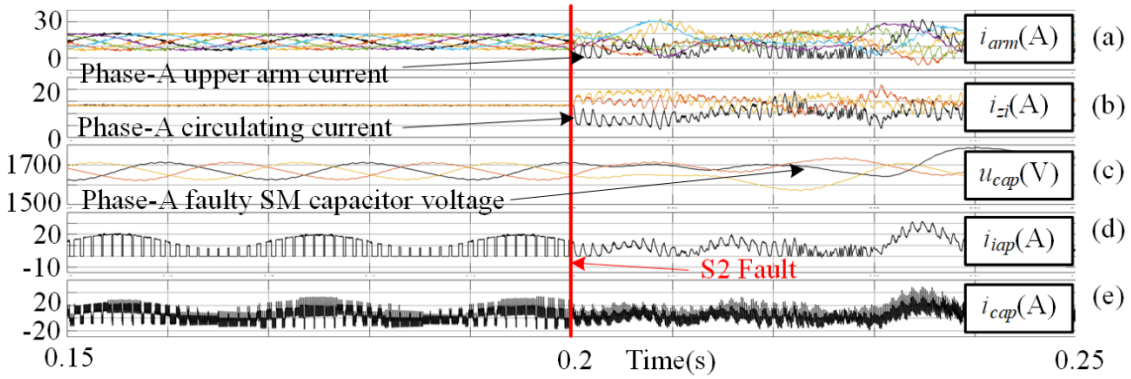

Figure 4.4 **Type I with S_2 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

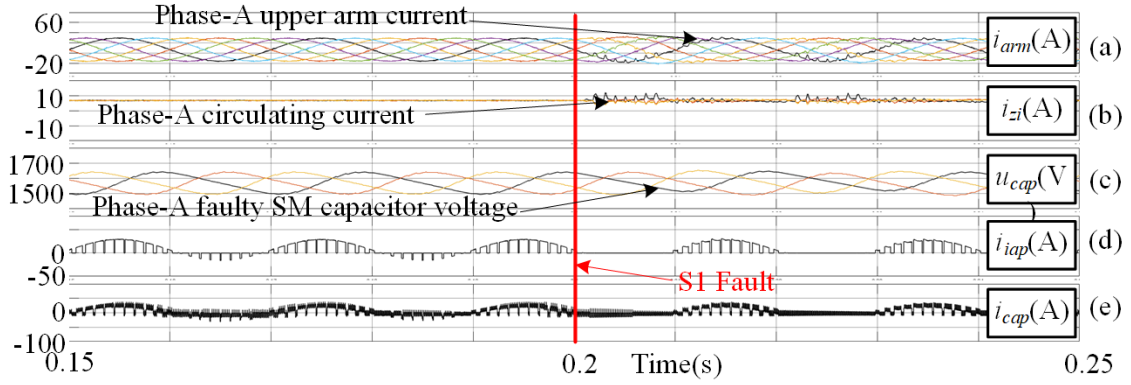

Figure 4.5 **Type II with S_1 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

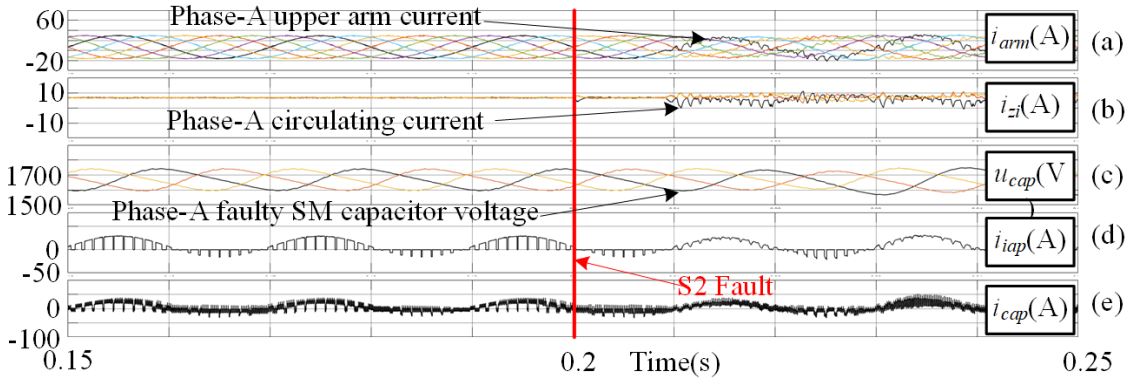

Figure 4.6 **Type II with S_2 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

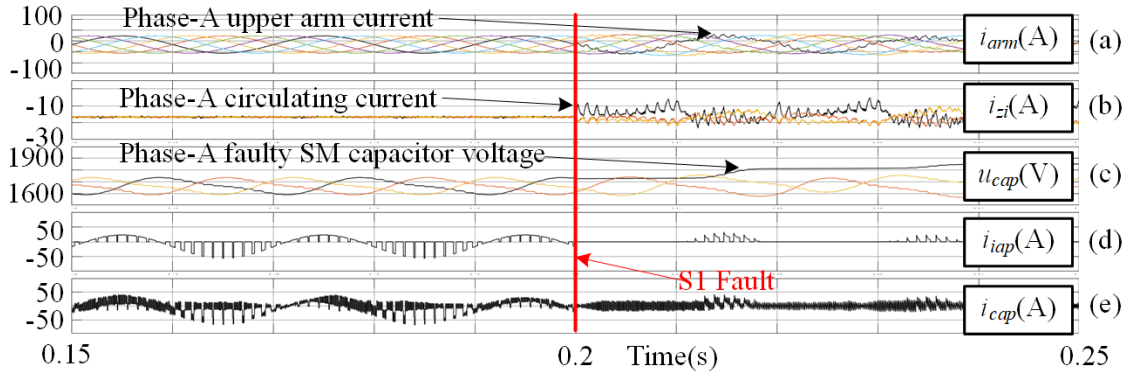

Figure 4.7 **Type III with S_1 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

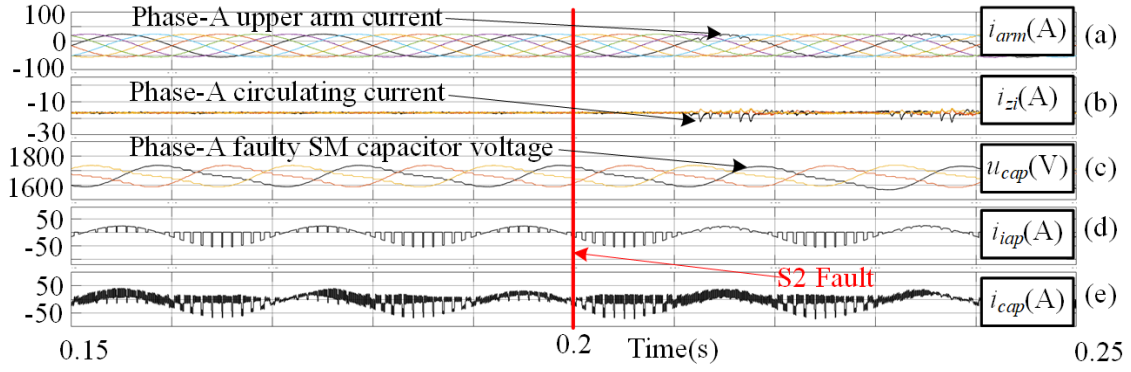

Figure 4.8 **Type III with S_2 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

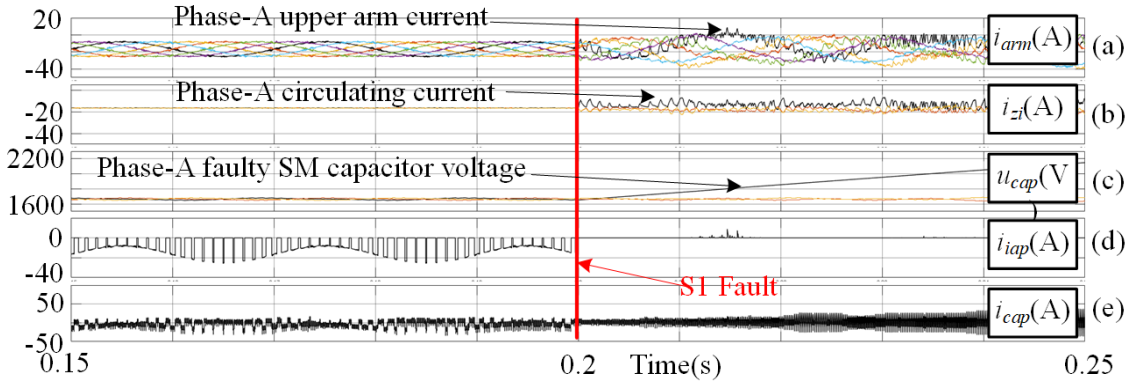

Figure 4.9 **Type IV with S_1 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

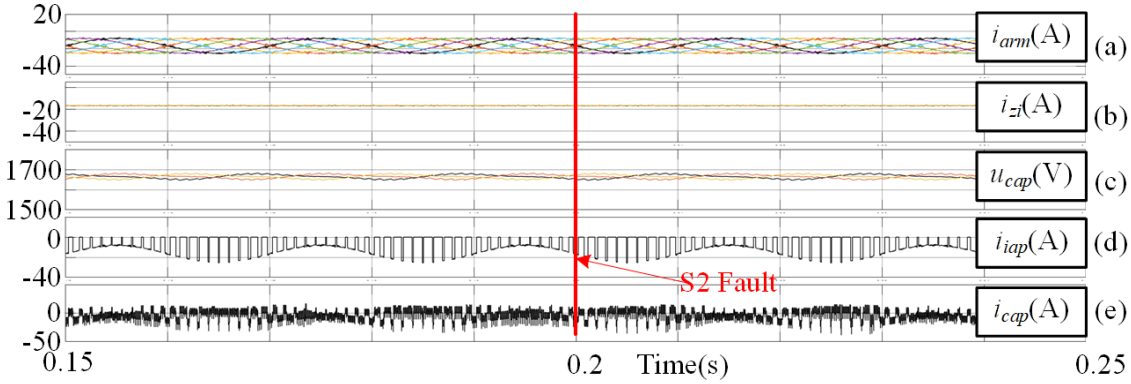

Figure 4.10 **Type IV with S_2 fault. (a) arm currents; (b) circulating currents; (c) 3-ph SM capacitor voltages; (d) faulty SM input current; (e) faulty SM capacitor current.**

In all the simulated scenarios, the SM IGBT OC faults are activated at 0.2 s. Compared with the other operation modes, i_{ipa} in Type I and Type IV modes only flow in one direction, as shown in Figures 4.3, 4.4, 4.9, and 4.10. Besides, since the power is mainly exchanged between the MVDC and LVDC ports, the SM capacitor voltage fluctuation is much smaller than the other modes. In Figures 4.3 and 4.10, the faults will not affect the system's balance condition where full power transfer capability of the faulty SM can be achieved. The balance of the iMMC-SST is also not affected under Type III mode with S_2 fault, as shown in Figure 4.8. The extra charge of the faulty SM is released by increasing the SM discharging periods. Therefore, though the SM output voltage is slightly changed with increasing circulating currents, the transmission power of this faulty unit is kept the same as that under normal conditions. On the other hand, the faulty SM

capacitor voltage will gradually increase due to the missing discharging periods or the extra charging periods leading to SM capacitor voltage imbalance and arm voltage imbalance, as illustrated in Figures 4.4, 4.5, 4.6, 4.7, and 4.9.

4.4. Conclusion

In this chapter, the SM IGBT OC fault characteristics of a multiport iMMC-SST are studied in detail. In contrast to the fault conditions in conventional MMC applications, the iMMC-SST exhibits different fault characteristics due to its complex operation modes. The simulation results agree with the theoretical analysis and prove that the SM switch OC fault poses challenges to system operation and may propagate to the connected distribution systems. The faulty SM can still maintain the full power transfer capability under specific operation modes, including the conditions of the Type I mode with S_1 fault, Type IV mode with S_2 fault, and Type III mode with S_2 fault. Based on the analysis, it is obvious that the conventional fault-diagnosis schemes fall short in capability to identify and locate the SM IGBT OC faults under the cases with balanced SM capacitor voltages unless the system operation mode is changed.

Additionally, the previous fault-tolerant methods without using redundant modules are not applicable in the iMMC-SST. The iMMC-SST can only operate under specific operation modes under SM OC faults with balanced SM capacitor voltages. The presented analysis lays the ground for developing suitable fault-tolerant schemes for the iMMC-SST under SM IGBT OC faults.

Chapter 5.

Global Redundancy Scheme for iMMC-SST

As analyzed in Chapter 4, the healthy circuit components of the faulty module can still operate for a certain period under SM IGBT OC faults. Since the voltage and current will not exceed the protection thresholds, it is possible to develop fault-tolerant schemes to maintain the continuity of the power supply of the connected feeders.

Hardware-based and software-based methods were proposed in the previous articles to address the SM OC fault [114], as shown in Figure 5.1. Redundant SMs (RSMs) are employed in the hardware-based methods to solve the problem by replacing the faulty units. These methods can be further classified into two subtypes in terms of the capacitor charging state of the RSMs, such as the cold-reserved mode [52], [115], [116] and the hot-reserved mode [43], [53], [54], [109], [117]–[122]. The RSMs with the cold-reserved mode are not pre-charged and will not participate in the regular operation of the MMC applications, such that less conduction loss will be generated. However, the RSMs cannot be fully used during regular operation leading to a lower equipment usage ratio and longer response time for charging the capacitors.

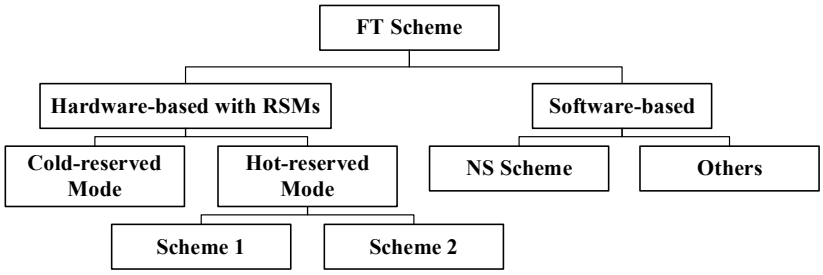

Figure 5.1 Classification of the fault-tolerant schemes for SM OC fault in MMC applications

The fault-tolerant strategies with hot-reserved mode RSMs can be divided into two sub-schemes based on the detailed SM operations after the fault detection. The RSMs in [43], [114], [118], [119] are treated as the regular SMs which participated in the normal operation of the MMC applications such that the SM capacitor voltages can be mitigated with lower switching losses. Nevertheless, this method is associated with arm voltage mismatch and poor harmonic profile. The hot-reserved RSMs are not fully

utilized under normal conditions in [122]. Additionally, the same number of healthy SMs in the other arm must be bypassed, leading to a lower equipment usage ratio. In [54], the RSMs operated the same as the regular SMs and were inserted in the arm periodically under normal conditions. After the fault diagnosis (FD) scheme detects the fault conditions, only the faulty units will be bypassed without causing arm voltage mismatches and worse harmonics. Though the method proposed in [46] shares features of the RSMs based schemes and the neutral shift (NS) schemes, a heavy computational burden is inevitable. Overall, all these RSM-based schemes will increase the size of the MMCs with relatively higher conduction losses.

On the other hand, software-based fault-tolerant schemes were provided without using extra hardware components, separated into two subgroups. The first subgroup relying on the neutral shift technique concerns more about the balance of the three-phase line voltages [122]–[125]. The line-voltage balance is maintained via adding a zero-sequence voltage to each phase-voltage in [123]. In [122], the AC neutral point location is shifted accordingly to obtain the maximum balanced line voltage amplitude. Kucka et al. demonstrated a method by moving the neutral points on the AC and DC sides [125]. An extended method was proposed in [124], where the optimum DC component and the best neutral point position are used to achieve the maximum line-voltage amplitude. Full performance can be restored in [114] by using the residual healthy SMs to share the faulty SM voltage associated with the NS technique. However, the amplitude of the line voltages has to be curtailed due to the limited SM number in each arm with a relatively heavier computational burden.

Another subgroup aims to compensate for the missed capacity by using the rest healthy SMs [107], [121], [126]. Full performance can be restored when these fault-tolerant schemes are activated at the cost of the higher capacitor voltages of the healthy SMs. Abdelsalam *et al.* [121] and Yang *et al.* [107] modify the modulation scheme and the capacitor references for the rest healthy SMs of the faulty phase. In [126], the fault-tolerant is enabled by applying an asymmetrical space vector modulation technique. In comparison, these fault-tolerant schemes result in a higher circulating current, which should be surpassed to maintain the MMC performance.

It should be noted that the distribution networks used iMMC-SSTs contain fewer SMs in each arm due to the limited voltage level comparing with the existing MMC-

HVDC applications. The cost and size of the RSMs cannot be ignored in the iMMC-SST when conventional redundancy is employed. Besides, since all the SMs used in the iMMC-SST are series-connected with dual active bridge (DAB) modules [8], more circuit elements are required with the traditional arrangement and will further raise the total system cost size and losses. On this basis, an extended SM OC fault-tolerant strategy is proposed for the iMMC-SST by using the global redundant PM and asymmetrical control. And the proposed scheme can improve system reliability and robustness with minimum cost, size, and losses.

In this method, the upper and lower arms share a common redundant PM (RPM) in each phase through several bidirectional switches. Due to the directly coupled PM topology, the RPM of each phase can be reversely charged via the LVDC bus to achieve hot-reserved mode. The RPM will be inserted when one SM OC fault is identified. When more SM failed in the same phase, the asymmetrical control strategy would be activated by adequately modifying the arm modulation waveforms and the SM capacitor voltages of the faulty arm to achieve minimum performance degradation.

5.1. Fault-Tolerant Scheme Based on Global Redundancy and Asymmetrical Control

Based on the fault analysis presented in Chapter 4, a fault-tolerant scheme relying on the global redundant PM and the asymmetrical control is proposed to further improve the iMMC-SST reliability and robustness with less cost and smaller size used in the distribution networks than traditional redundancy schemes, as shown in Figure 5.2 (a). Two fault conditions are considered with two SM topologies (HBSM and 3-level SM) in the fault-tolerant scheme, including a) N_f=1 and b) N_f≥2. From [121], a threshold N_{th} (where N_f/N=0.25) is predefined based on the SM capacitor voltage design margin to prevent the system cascaded failure. Here N_f is the number of the faulty SMs of one arm. The flowchart of the whole fault-tolerant scheme is depicted in Figure 5.3.

The SM capacitor voltages of the six arms are sampled and updated to obtain the real-time status of the SMs. Proper FD schemes [127], [128] are used to identify the faulty units as fast as possible. If N_f>N_{th}, all the defective units will be bypassed, and the entire system will be shut down to avoid potential system damage. When only one SM fails on the MMC side, the RPM will be utilized to remove the faulty unit; if $2 \le N_f \le N_{th}$, the

asymmetrical control will be activated since the RPM is occupied with compensating the arm voltage mismatch.

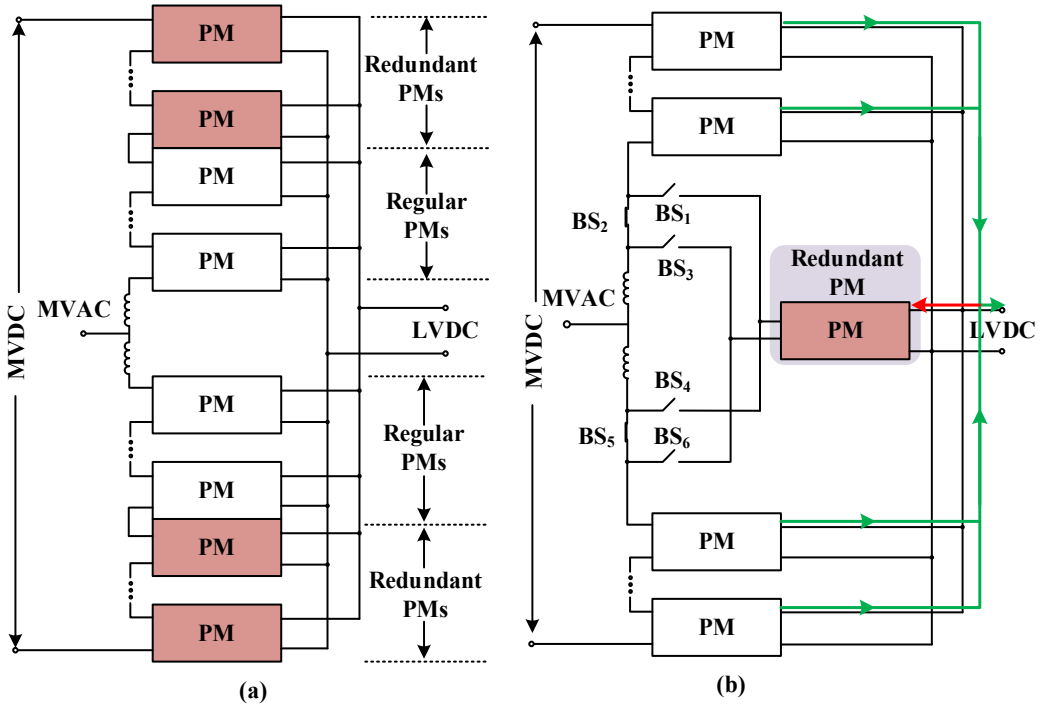

Figure 5.2 Redundancy schemes (a) traditional arrangement; (b) global arrangement.

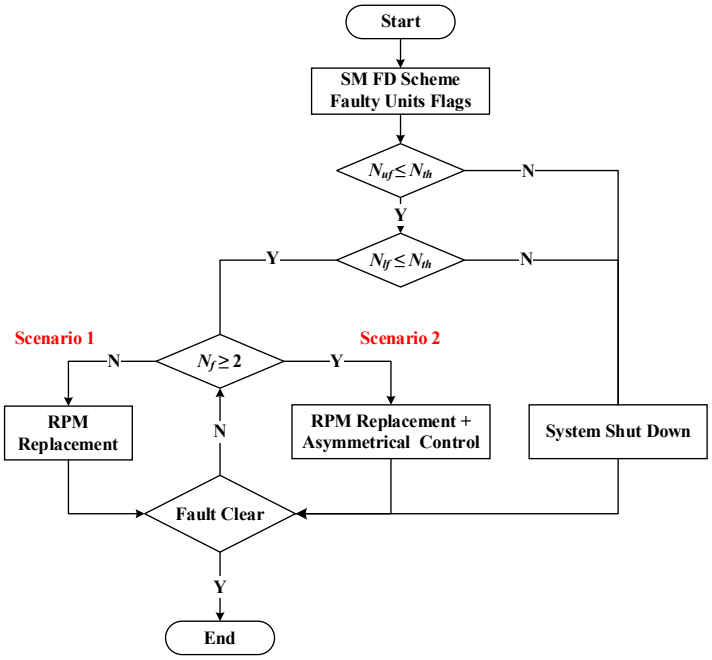

Figure 5.3 Flowchart of the proposed fault-tolerant scheme.

The RPM has the same topology as the regular SMs in this work. Its SM's input is shared by the upper and lower arms of the same phase through six bidirectional switches (BS_1-BS_6), formed by anti-series connected switches (or anti-parallel connected reverse blocking type switches). Due to the redundant PM's DAB module output being parallel connected to the LVDC bus, the redundant PMs can be reversely pre-charged to quickly and smoothly replace the faulty unit after the FD procedure.

The precharge control diagram of the redundant PM is illustrated in Figure 5.4. The redundant PM is bypassed from both arms by opening BS_1, BS_3, and BS_4, BS_6. The SM capacitor is reversely charged via the DAB module. A PI controller is adopted to generate the corresponding phase shift ratio $D_{RPM\text{-}PC}$ to charge the u_{cpa} of the redundant PM where the power consumption can be ignored.

Assuming the conventional fault detection schemes are adopted, it will take a few microseconds to several milliseconds [108], [129]–[131] to finish the fault detection and localization. After the fault is identified, if only one SM failed (N_f=1), the redundant PM will be immediately inserted to remove the faulty unit. Meanwhile, the redundant PM will adopt the phase shift ratio (shown in Figure 2.9) to control the LVDC bus voltage.

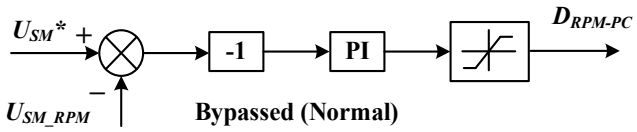

Figure 5.4 Redundant PM precharge control diagram

When more than one SM failed (N_f>1), since the redundant PM has been used for the faulty unit removal, the asymmetrical control will be activated to maintain the defective phase's arm voltage balance. Using the Double Fourier Series expansion, (2.31) and (2.32) can be denoted as

$$u_{pj} = \frac{U_{\mathrm{MVDC}}}{2} - \frac{MU_{\mathrm{MVDC}}}{2}\cos(\omega_0 t + \varphi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2U_{\mathrm{MVDC}}}{m\pi N_{pj}} J_n\left(\frac{MN_{pj}m\pi}{2}\right)\sin\left[\frac{(N_{pj}m+n)\pi}{2}\right]\cos\left[N_{pj}m\omega_c t + n(\omega_0 t + \varphi + \pi)\right] \tag{6.1}$$

$$u_{nj} = \frac{U_{\mathrm{MVDC}}}{2} + \frac{MU_{\mathrm{MVDC}}}{2}\cos(\omega_0 t + \varphi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2U_{\mathrm{MVDC}}}{m\pi N_{nj}} J_n\left(\frac{MN_{nj}m\pi}{2}\right)\sin\left[\frac{(N_{nj}m+n)\pi}{2}\right]\cos\left[N_{nj}m\omega_c t + n(\omega_0 t+\varphi)\right] \quad (6.2)$$

Where m and n are the harmonic order of the carrier wave and the reference wave, $J_n(x)$ is the Bessel coefficient of order n and argument x; $\omega_c(=2\pi f_c)$ is the angular frequency of the carrier wave. The third item on the right-hand side of (6.1) and (6.2) can be canceled out by each other in the MVAC phase voltages under normal conditions. According to the analysis demonstrated in Chapter 4, additional harmonics will appear in the MV-side ports when N_{pj} is not equal to N_{nj}. Hence, the modulation and the carrier waveforms will be adjusted in the asymmetrical control to compensate for the arm voltage mismatch after the redundant PM is used.

Only the modulation and carrier waveforms of the faulty arm need to be modified on the MMC side. The new modulation waveform can be expressed as

$$u'_{pj}(i) = \frac{U_{\mathrm{MVDC}}}{2N_{pj\_asy}}\left[1 - M\cos(\omega_0 t + \varphi)\right] \quad (6.3)$$

N_{pj_asy} (=N_{pj}-N_{pf}) is the rest of the healthy PMs in the faulty arm; N_{pf} is the faulty SMs in the upper arm. The carrier frequency is adjusted to f_c'=(N_{pj}/N_{pj_asy})f_c, and the phase shift of the faulty arm is changed to (2π/ N_{pj_asy}); the SM capacitor voltage of the defective arm increases from (U_{MVDC}/N_{pj}) to (U_{MVDC}/N_{pj_asy}). Thus, the modified modulation scheme can be denoted as

$$u'_{pj} = \frac{U_{\mathrm{MVDC}}}{2} - \frac{MU_{\mathrm{MVDC}}}{2}\cos(\omega_0 t + \varphi) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2U_{\mathrm{MVDC}}}{m\pi N_{pj\_asy}} \underbrace{J_n\left(\frac{MN_{pj\_asy}m\pi}{2}\right)\sin\left[\frac{(N_{pj\_asy}m+n)\pi}{2}\right]}_{amplitude} \underbrace{\cos\left[N_{pj\_asy}m\omega'_c t + n(\omega_0 t+\varphi+\pi)\right]}_{harmonic} \quad (6.4)$$

From (6.4), it is obvious that the first two items on the right-hand side can be maintained the same as those under normal conditions. The third item on the right-hand is different from the counterparts of (6.1) due to the alternation of N and f_c of the faulty arm, and the harmonics with switching frequency f_c' and the side-bands cannot be eliminated. These harmonics will be coupled with the arm inductors and the SM

switching functions and excite extra current components. As the SM number in each arm increases, the influence induced by the harmonics can be ignored. However, the SM capacitors should be carefully selected in the worst scenario where $N_f > N_{th}$ when adopting the asymmetrical control strategy. The novel capacitor value can be determined by considering the maximum energy variation and the increased capacitor voltage level [121]:

$$C_{SM} > \frac{2\Delta e_{p\max}}{N_{eff} V_c^2 \left(1 + k_{ripple\max}\right)^2} \tag{6.5}$$

V_c is the rated capacitor voltage, $k_{ripplemax}$ is the maximum allowable ripple percentage, and Δe_{pmax} is the maximum energy variation.

5.2. Comparison with the Conventional Redundancy Scheme

Based on the redundant modules' operation status, the systems with hot-reserved mode can be re-defined: 1) type I; and 2) type II. Redundant modules will not participate in the normal operation with type I hot-reserved mode. By contrast, the Type II hot-reserved mode will fully utilize the redundant modules under the normal state to enhance the equipment usage ratio. In this section, the performance of the global redundancy schemes is thoroughly compared with the conventional method from different perspectives in a typical case study of the iMMC-SST applications with 12 modules per arm, including the equipment usage ratio, the number of the circuit elements, the fault response speed, the conductions losses, the power factor, and the initial cost, as shown in Table 5.1. In this case, each arm contains one redundant module with traditional redundancy schemes.

Table 5.1 Comparison of the Redundancy Schemes

	Cold-Reserved Schemes [52], [115], [116]	**Type I Hot-Reserved Schemes** [53], [109], [117]	**Type II Hot-Reserved Schemes** [43], [54], [118]–[122]	**Proposed fault-tolerant Scheme**
Equipment Usage Ratio	**Low**, 92.3%	**Low**, 92.3%	**High**, 100%	**Medium**, 96%
# of Circuit Elements (per phase)	26 HBSMs + 26 DABs (2 redundant modules)			25 HBSMs + 25 DABs, 6 MV-level bidirectional switches
Response Speed	**Slow**, the capacitors in the redundant modules need to be charged	**Fast**, all the capacitors are pre-charged.	**Fast**, all the capacitors are pre-charged.	**Fast**, all the capacitors are pre-charged.
Conduction Loss	**Low,** all the redundant modules will not operate under regular operation.	**High,** all the redundant modules are charged without participating in the normal operation	**High,** all the redundant modules are charged and participating in the normal operation.	**Medium,** the shared redundant modules are charged without participating in the normal operation
Power Factor	**Low**, no inductors and capacitors of the redundant modules need to be charged	**High**, the inductors and capacitors of the redundant modules will result in more reactive power	**High**, the inductors and capacitors of the redundant modules will result in more reactive power	**Medium**, the inductors and capacitors of the shared global redundant modules will result in less reactive power
Cost	**High,** redundant modules are evenly implemented in each arm.			**Low,** the redundant module is shared by two arms via several bidirectional switches.
Description	The redundant modules are not fully used; no voltage mismatch occurs under fault-tolerant operation.	The redundant modules are not entirely used under normal conditions; no voltage mismatch occurs under fault-tolerant operation.	The redundant modules are fully used under normal conditions; the healthy modules need to sustain higher voltage stress under fault condition, and one or more healthy modules must be bypassed to maintain the arm voltage balanced; voltage mismatch may occur when the redundant modules are used up leading to worse harmonic profiles.	The redundant module is not fully used under normal conditions; no other healthy modules need to be bypassed.

According to Table 5.1, the number of the circuit elements is significantly reduced by using the proposed fault-tolerant scheme compared with the traditional redundancy arrangement in the typical case. The proposed fault-tolerant approach's equipment usage ratio is higher than the first two types of redundancy schemes. Though this ratio is

lower than type II hot-reserved schemes, a higher power factor and efficiency can be obtained. Among all the redundancy schemes, the quasi-balanced operation mode can be maintained in the faulty phase without bypassing extra regular PMs in the healthy arm. The normal operation of the rest two phases can be maintained. Moreover, the power transmission capability of the iMMC-SST can be maintained to the maximum extent.

Overall, the proposed fault-tolerant scheme has the following benefits: 1) high equipment usage ratio; 2) less conduction loss; 3) high power transmission capability under fault conditions; and 4) lowest initial investment and smallest size. This method can be extended to all three phases with only redundant SM. However, the proposed fault-tolerant scheme with RPM shared between arms is more prominent than the RPM shared between three phases due to the less complicated circuit and control system.

5.3. Simulation and Experiment Results

- MATLAB/Simulink Simulation

The iMMC-SST with HBSM and 3LSM are modelled and simulated with the proposed fault-tolerant scheme in MATLAB/Simulink to evaluate the proposed fault-tolerant scheme's feasibility and effectiveness. The simulation parameters of the HBSM case are listed in Table 5.2.

Table 5.2 Parameters of the iMMC-SST for Simulation Test

Specifications	Value	Specifications	Value
System Power	2 MVA	SM Cap. Volt. u_{cpa}	1.66 kV
MVDC U_{MVDC}	20 kV	Arm Induct. L_0	8 mH
MVAC $u_{line\text{-}to\text{-}line}$	10 kV	Arm Resist. R_0	0.2 Ω
LVDC U_{LVDC}	800 V	SM Capacit. C_{SM}	650 μF
Modules # N/arm	12	HFT Turn Ratio k	25:12
MMC f_{sw}	1.5 kHz	DAB f_d	5 kHz

The simulation results with HBSM and 3LSM are depicted in Figure 5.5 and Figure 5.6, respectively. The iMMC-SST systems with both SM topologies are initially operated under normal conditions before 0.2 s. At 0.2 s, one of the regular SMs failed in the upper arm of Phase-a of the MMC structure that triggered the fault identification scheme, which takes 2 ms. Because N_f <2, the bidirectional switches in the faulty arm

will be toggled to plugin the hot-reserved global redundant SM for the defective unit replacement. At 0.35 s, another SM failed in the same phase, and the first scenario occupies the global redundant module. The asymmetrical control scheme is activated to compensate for the voltage mismatch without affecting other healthy arms' regular operations. The carrier switching frequency of the faulty arm is adjusted to 1.64 kHz with HBSM (or 1.8 kHz with 3LSM); the phase shifts of the carriers are altered to 2π/11 with HBSM (or 2π/10) with 3LSM, and the corresponding u_{cpa} are increased to 1.82 kV and 2 kV in Figure 5.5 (d) and Figure 5.6 (d), respectively.

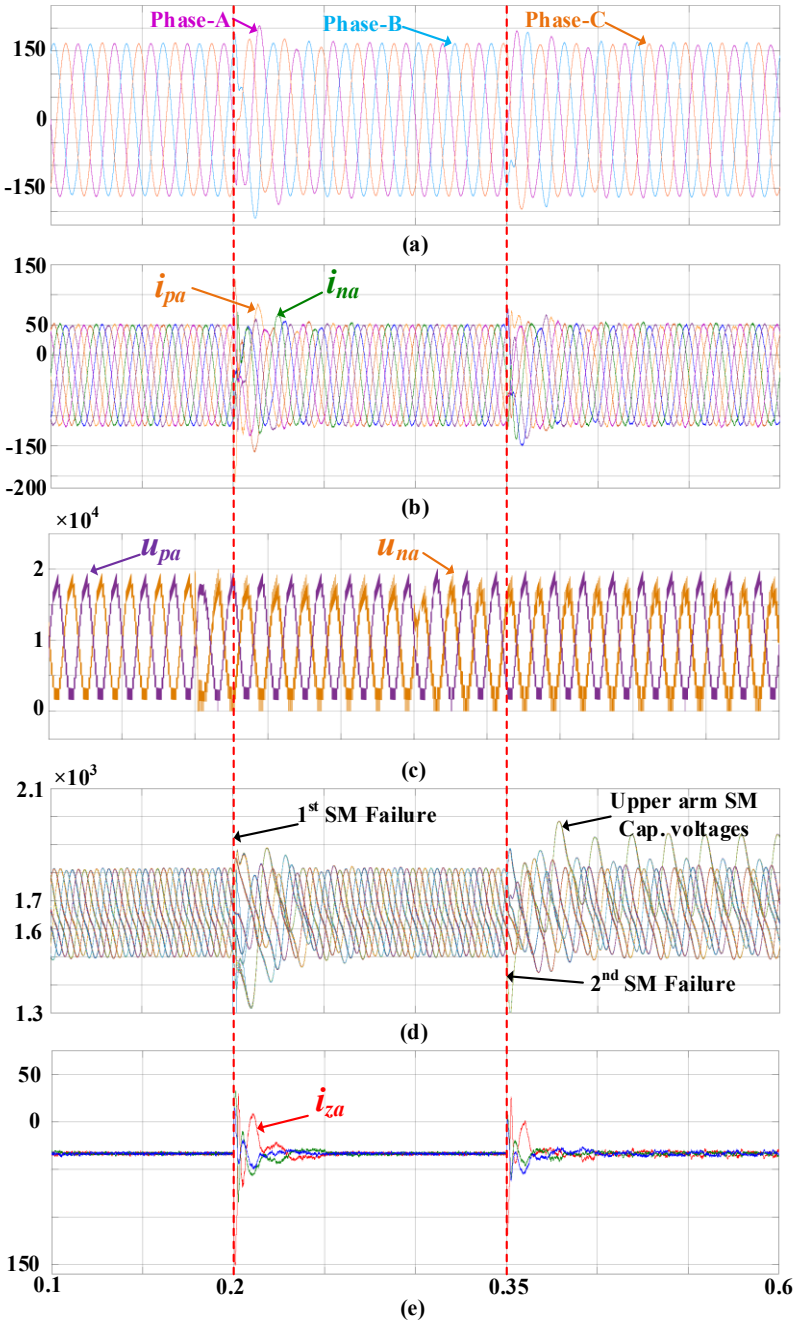

Figure 5.5 **Simulation results with HBSM: (a) MVAC output currents; (b) arm currents; (c) arm voltages; (d) SM capacitor voltages; (f) circulating currents.**

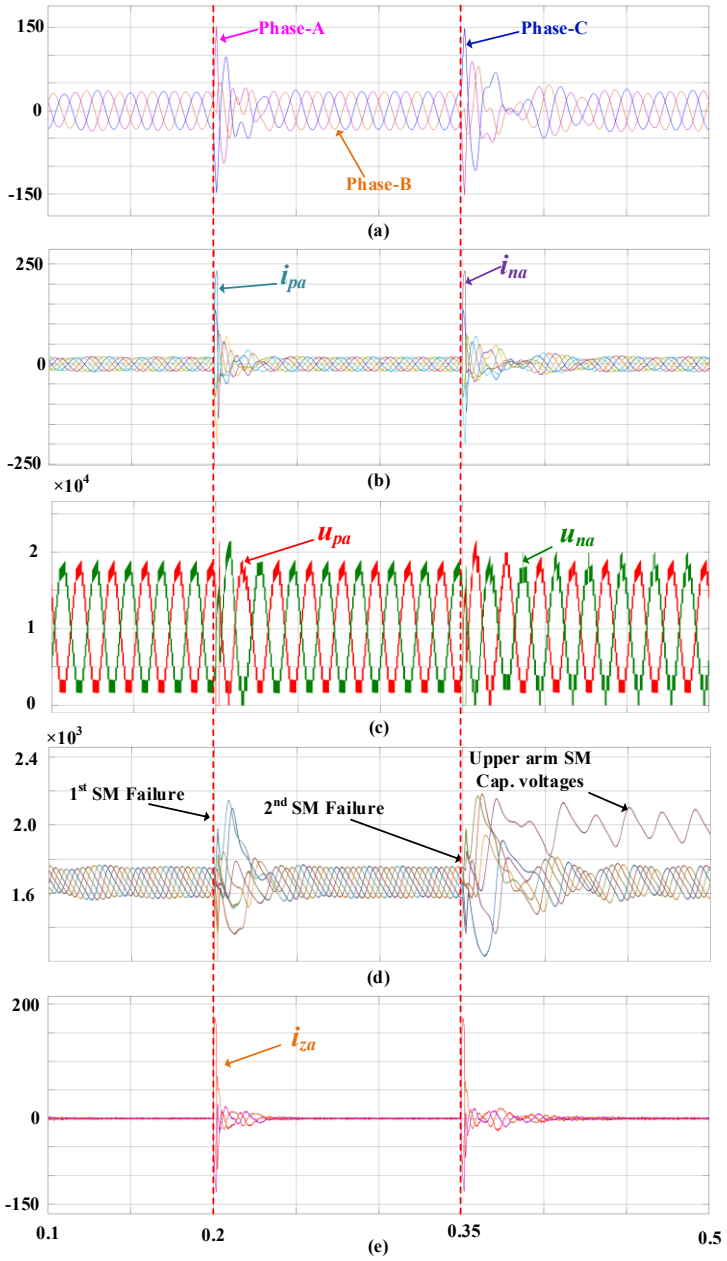

Figure 5.6 **Simulation results with 3LSM: (a) MVAC output currents; (b) arm currents; (c) arm voltages; (d) SM capacitor voltages; (f) circulating currents.**

- HIL Experiment

The proposed SM IGBT fault-tolerant strategy is further validated by experimental tests using a hardware-in-the-loop (HIL) system consisting of a real-time model simulator and a rapid control prototyping (RCP) system, as shown in Figure 5.7. Due to the limited I/O ports of the test platform, the model of a single-phase iMMC-SST is developed in the

simulation software StarSim and operates on the real-time HIL system based on one NI PXI FPGA 7868R with the time step 1 μs. Two NI PXI FPGA 7846R boards served as the RCP and were used to realize the corresponding control system. The analog and digital signals communicate between the HIL and RCP systems via the interface boards. The single-phase iMMC-SST model built in the HIL system contains four SMs in each arm. The sampling period of the controller and the switching frequency are 100 μs and 3 kHz, respectively. Two scenarios are designed to show the feasibility of the proposed fault-tolerant strategy, as shown in Figure 5.8.

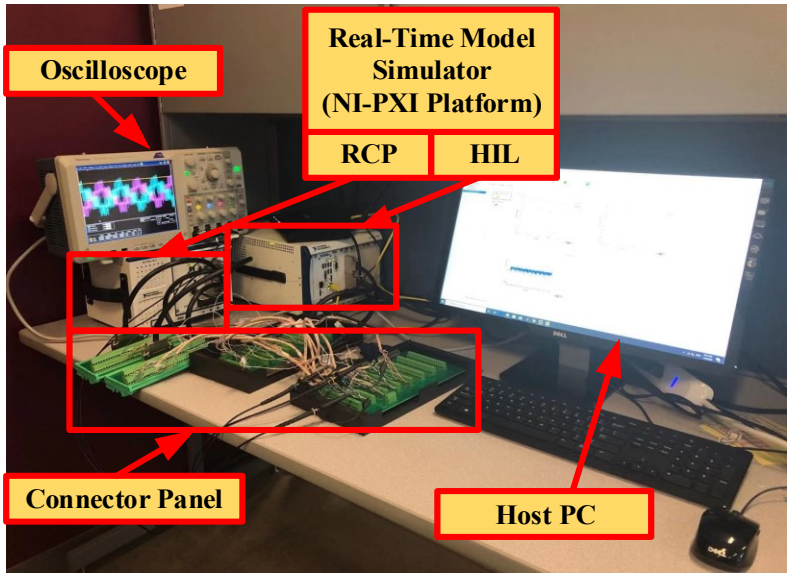

Figure 5.7 Real-time experimental platform setup.

Case 1: Single SM switch Fault in the Upper Arm

In this case, one of the SM in the upper arm encountered IGBT failure and was bypassed at t_1. Since N_f<2, the hot-reserved global redundant module was activated and inserted in the upper arm to replace the faulty unit in 2 ms. During the transient period ΔT_1, the increase of the MVAC grid-side current is less than 2× of the original current amplitude under normal conditions, as shown in Figure 5.8(b). The SM capacitor voltages u_{p2} from the upper arm and u_{n2} from the lower arm were maintained after t_1, as shown in Figure 5.8(c) and (d). According to Figure 5.8(e) and (f), it is evident that the upper and lower arm voltages can be restored from the fault condition back to regular operation within two cycles.

Case 2: One More SM IGBT Fault in the Same Phase (Lower arm)

In this case, one more SM IGBT fault occurred in the lower arm, and this SM was bypassed at t_2. Because the global redundant SM was occupied in the upper arm, the asymmetrical control was activated 2 ms after t_2 by adjusting the lower arm's modulation waveform and carrier waveforms. The rest SMs shared the MVDC voltage evenly, where the value increased from 5 kV to 6.67 kV, as shown in Figure 5.8 (d). The SM capacitor voltages in the upper arm were not changed, as shown in Figure 5.8 (c). During the transient period ΔT_2, the MVAC current dropped to zero and was restored to normal condition within two cycles, as given in Figure 5.8 (b). In Figure 5.8 (e), the upper arm voltage was controlled to regular status with five voltage levels. Nonetheless, the lower arm voltage shifted from five to four voltage levels using the proposed unbalanced control, and the system returned to the new steady state within two cycles, as shown in Figure 5.8 (f).

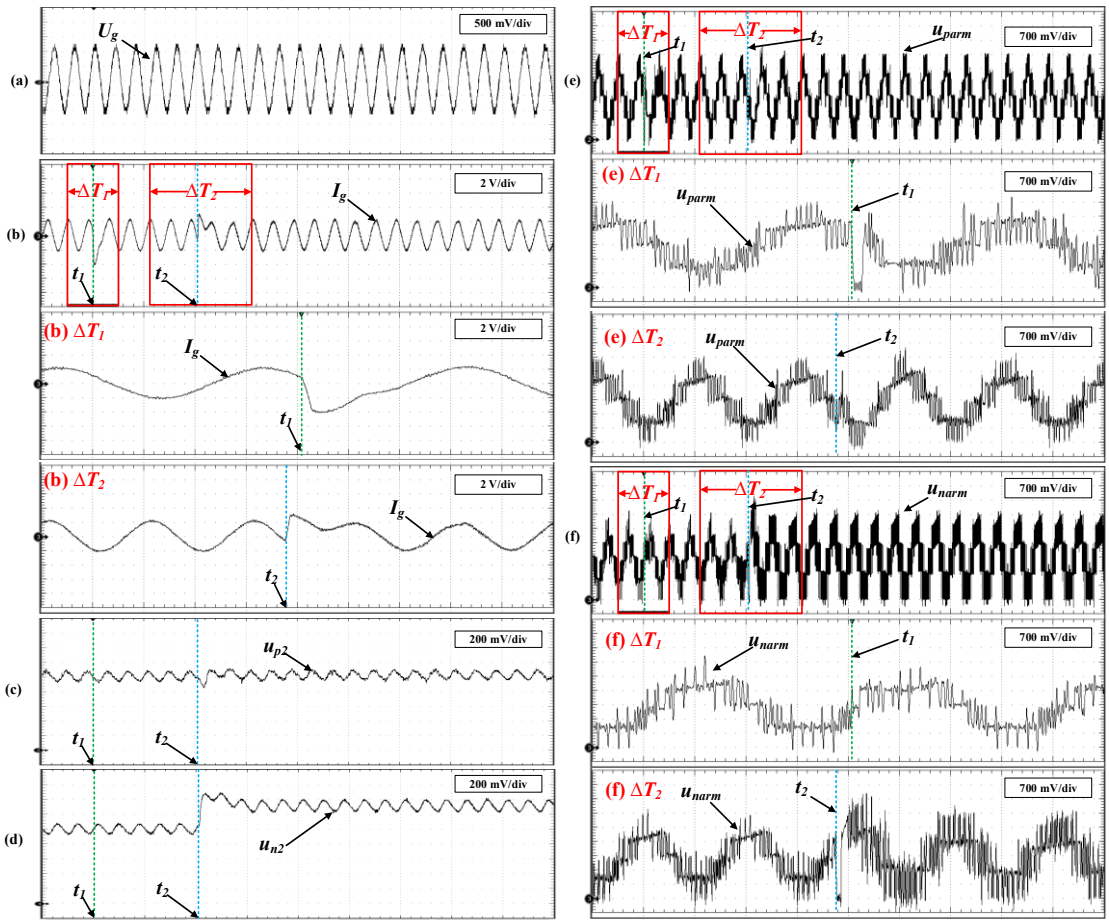

Figure 5.8 Experimental results (a) MVAC grid-side voltage; (b) MVAC grid-side current; (c) SM capacitor voltages u_{p2} of the upper arm; (d) SM capacitor voltages u_{n2} of the lower arm; (e) upper arm voltage; (f) lower arm voltage.

5.4. Conclusion

This fault-tolerant scheme is designed for the iMMC-SST based on the global redundant PM and the asymmetrical control. Additionally, the robustness and reliability can be improved with fewer redundant PMs and minimum. In this chapter, the SM switch OC fault behaviors with different SM topologies are analyzed. Based on the fault behaviors, the fault-tolerant scheme is presented to deal with the two switch OC fault cases: a) when N_f=1, the redundant PM will replace the only faulty unit to address arm voltage mismatch issue; b) when N_f>1, the asymmetrical control complements the arm voltage mismatch by reconfiguring the carrier and modulation waveforms of the faulty arm. The rest healthy arms maintain regular operation with a minimum output degradation. Overall, the proposed fault-tolerant scheme has the following merits: 1) less

cost and smaller size of the iMMC-SST; 2) the regular operation of the healthy arms is not influenced; 3) less conduction loss; 4) and higher power transmission capability. The control system maintained all ports' voltages and currents in balanced mode throughout the fault-tolerant period with relatively small distortions. The evaluation of both simulation and the HIL platform has shown the effectiveness of the proposed fault-tolerant scheme.

Chapter 6.

DAB Switch Open-Circuit Fault-Tolerant Strategy

Reliability and robustness are two main concerns for modular applications with a large number of semiconductors which can be potential fault sources [106]. According to [51], the SC and the OC faults resulting from the power switches or driver circuits account for 46% of all fault conditions in power electronic converters. The destructive switch SC fault is generally solved by the system's built-in protection schemes [38], [132], [133] and will not be further discussed in this chapter. The iMMC-SST is separated into two parts to clarify the fault location: the MMC and the DAB sides. The behavior of the SM switch OC fault conditions has been analyzed in Chapter 4 and Chapter 5. However, less research has been conducted in the DAB switch OC fault analysis in modular multilevel applications. Accordingly, multiple SM switch OC fault diagnosis methods [108], [134] and fault-tolerant schemes [46], [107], [135] have been proposed and therefore will not be discussed in this chapter. However, when the switch OC fault happened in the DAB modules, the traditional fault-tolerant schemes relying on the redundant modules were not cost-effective in the iMMC-SST due to its unique PM topology.

Similar to the SM switch OC fault, two steps are required in implementing a DAB switch OC fault-tolerant strategy for the iMMC-SST, including 1) the detection and localization of the fault and 2) the carrying out of the fault-tolerant operation [136]. Several diagnosis and localization strategies have been introduced in [137], [138], proving that the fault can be identified within 2-5 switching cycles post-fault. In the second step, fault-tolerant operation [64], [139] can be achieved by adopting one or the combination of the following approaches, i.e., overdesign of components, redundancy of converters, and fault-tolerant control strategies. Component overdesign is one of the most practical ways to tackle unknown failures with increased cost and reduced efficiency, which is unsuitable for iMMC-SST. With converter redundancy, the DABs with IGBT OC fault can be replaced by the redundant module [30], [140], but the power transfer capability of the faulty unit can no longer be utilized, leading to a lower equipment usage ratio. For control-based approaches, the fault-tolerant schemes presented in [141]–[144] are realized by adjusting the switching signals to maintain the

power transfer capability of the isolated DC-DC converters. In these articles, the H-bridge on the secondary side is formed by four uncontrolled diodes, and the power can only be transferred in one direction. Another fault-tolerant scheme using extra phase shift angles is demonstrated in [45], [145] to address the switch OC faults on both sides of the DAB. However, it relies on the freewheeling diodes (FWDs) and is designed to address only the rectifier-side fault conditions, and as such, it cannot allow reverse power transmission of the DAB after the fault. In [146], a fault-tolerant strategy for a 3-phase DAB converter is proposed by freezing the half-bridge structure and working as a single-phase DAB converter. Nevertheless, the FWDs of the faulty unit can still self-commutate, leading to higher current stress and lower efficiency. An improved open-phase fault-tolerant method is developed in [147] by removing the interaction with the FWDs of the faulty leg such that the efficiency and power transfer capability of the 3-phase DAB converter can be improved.

It should be noted that all the control-based approaches are proposed and investigated in the DAB applications with ideal transformers. Detailed magnetic analysis of the non-ideal high-frequency transformer (HFT) under switch OC fault conditions was not discussed in the single-phase DAB converter-based applications. In a practical scenario, unbalanced magnetic flux caused by the faults will appear in the system with a non-ideal HFT model and cause transformer saturation [148], resulting in undesirable overheating of circuit elements and even destroying the faulty DAB module. Furthermore, the fault propagation will deteriorate the operation of the iMMC-SST and the performance of the adjacent distribution systems.

In this part, we focused on the fault analysis by considering the overcurrent and HFT saturation issues under switch OC faults and proposed a fault-tolerant approach based on DC current injection and phase shift ratio adjustment. The fault-tolerant scheme has the following advantages,

- by injecting the DC current, the magnetic flux imbalance can be solved to prevent the HFT saturation;
- by adjusting the phase shift ratio, possible maximum power transfer capability can still be guaranteed via the faulty DAB module;

- bidirectional power transfer capability of the faulty DAB module can be maintained;

- the fault-tolerant scheme is easy-to-implemented with minimum performance degradation of the faulty DAB module and the iMMC-SST system without using the redundancy scheme.

Overall, the reliability and robustness of the iMMC-SST can be guaranteed and improved by the proposed fault-tolerant method with less cost and smaller size. Moreover, the proposed fault-tolerant scheme can be applied to the other topologies based on the DAB module, such as the MMC-based SST [149] and the DC transformer [150], to enhance the system reliability.

6.1. DAB IGBT Open-Circuit Fault Analysis

Several causes, including bond wire lift-off and failure of the driver circuit, may potentially lead to the IGBT OC fault. Due to the asymmetrical current commutation, the faults will excite a DC bias current component in the faulty H-bridge. Once the DC component flows into the HFT winding, the induced DC magnetic flux and the existing AC magnetic flux will superimpose, and the operating point of the magnetic core exceeds the saturation point, leading to one half cycle magnetic flux increase and the other decrease. The exciting current will also be distorted, where peaks will appear in the half-cycle with increased magnetic flux. This chapter assumes that all the FWDs can continue to provide current paths under switch OC fault such that the DAB module will not be shut down immediately. It provides the possibility to realize fault-tolerant operation in the faulty DAB module without using conventional redundancy schemes.

Assuming the power is transferred from the H1 to the H2 bridge (positive direction), the H1 and the H2 bridges are defined as the inverter and rectifier sides of the DAB module. When power is reversely transferred (negative direction), H1 and H2 will be redefined as the rectifier and inverter sides, respectively. Owing to the DAB symmetrical topology and identical fault characteristics, only T_1 (inverter-side) and T_5 (rectifier-side) faults are analyzed in this section. Due to the SM capacitor voltage fluctuation, k varies between 0.9 to 1.1, which should be considered. The analysis of both faults is conducted with k<1. Both faults can be divided into transient state and

steady state [45]. The transient state analysis can be found in [45], [137], which will not be further discussed in this part.

Each switch in the DAB contains an active device T and an antiparallel diode D. As shown in Figure 6.1. The winding current i_2 rapidly increases to around 150A due to the magnetic saturation of the transformer. This overcurrent may even destroy the circuit elements of the system and harm the operation of the iMMC-SST.

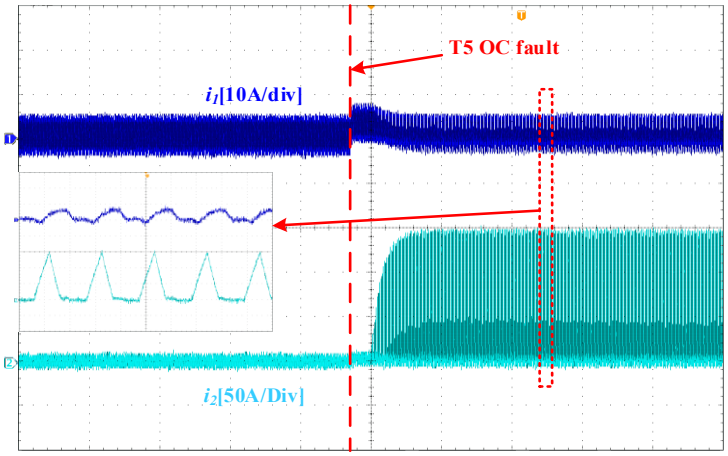

Figure 6.1 Experiment transformer current waveforms of the faulty DAB in the iMMC-SST.

The detailed steady-state waveforms of the faulty DAB module under T_1 and T_5 faults are illustrated in Figure 6.2 and Figure 6.3, respectively. In contrast to the analysis in [45], the bias currents on the healthy H bridges are consumed by the HFT parasitic resistance R_2 under T_1 fault and R_1 under T_5 fault during steady state, respectively. Under both faults, the steady states contain eight switching states. The corresponding current path and the voltage over L_s (U_{Ls}) with different switching states are summarized in Table II. Residual currents always exist because of k<1 and the asymmetrical topology of the faulty H bridges. As shown in E3 and E4 of Figure 6.2, residual i_1 with positive polarity flows through D_2, and the relevant slopes of freewheeling periods are changed to $-U_{LVDC}/L_s$ and U_{LVDC}/L_s, respectively. The same conclusion can be found in the T_5 fault condition as well as in E7 and E8. The other switching states of the faulty side currents are the same as the analysis in [45], where further analysis will be given in this chapter. From Figure 6.2 and Figure 6.3, $i_1(t_6)$ equals zero under the T_1 fault, and $i_2(t_6)$ equals zero under the T_5 fault. Hence, the current magnitudes at different moments can be calculated.

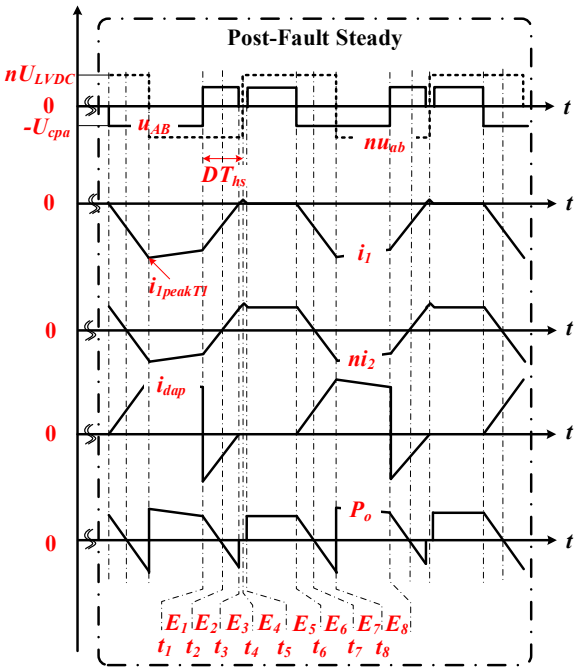

Figure 6.2 Waveforms of DAB with T_1 (T_4) OC fault

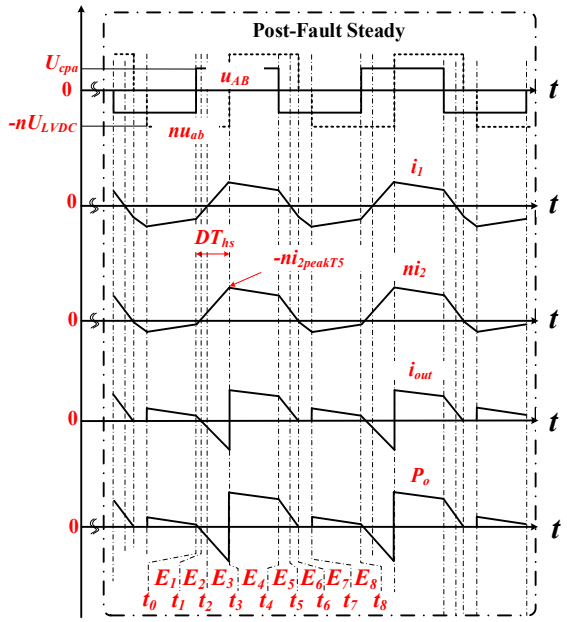

Figure 6.3 Waveforms of DAB with T_5 (T_8) OC fault

Under T_1 fault, the peak current of i_1 (or i_{dpa}) is

$$i_{1peakT_1} = i_{dpapeakT_1} = -\frac{nU_{\mathrm{LVDC}}}{2f_d L_s}(2D-1+k) \tag{6.6}$$

Under T_5 fault, the peak current of i_2 (or i_{out}) is

$$i_{2peakT_5} = i_{outpeakT_5} = \frac{u_{cpa}}{2f_d L_s}(k+1)D \tag{6.7}$$

From (6.6) and (6.7), the peak current values under faults are approximately doubled than those under normal conditions. When $0 \le |D| \le 0.25$, the actual HFT currents will not exceed the rated current values; when $0.25 \le |D| \le 0.5$, the peak currents of the faulty H bridge will exceed the rated current values of the circuit elements and threaten their safety. The DC bias currents of both faults can be derived via calculating the average values of i_1 and i_2.

$$I_{1biasT_1} = -\frac{nU_{\mathrm{LVDC}}}{4f_d L_s}(2D-1+k) \tag{6.8}$$

$$I_{2biasT_5} = \frac{u_{cpa}}{4f_d L_s}(k+1)D \tag{6.9}$$

Similar fault characteristics can also be obtained when $k>1$, which this chapter will not further discuss. When $k=1$, i_1 will completely flow in the negative direction where E3 and E4 will not exist under T_1 fault; under T_5 fault, E7 and E8 will not exist. In addition, the power transfer capability of the faulty DAB module will not be influenced without considering the overcurrent issue [45]. Under T_1 fault, the new HFT currents of both sides are

$$\begin{cases} i_1 = i_{1AC} + I_{1biasT_1} \\ i_2 = i_{2AC} \end{cases} \tag{6.10}$$

According to (6.10), the magnetic fluxes of the HFT under T_1 fault can be expressed as

$$\begin{cases} \Phi_{1T_1} = \underbrace{\frac{L_1}{N_1} i_{1AC} - \frac{L_1}{N_1} I_{1biasT_1}}_{\Phi'_{11}} \underbrace{+ \frac{L_M}{N_2} i_{1AC} - \frac{L_M}{N_1} i_{2AC} - \frac{L_M}{N_2} I_{1biasT_1}}_{\Phi'_{12}} \\ \Phi_{2T_1} = \underbrace{\frac{L_2}{N_2} i_{2AC}}_{\Phi'_{22}} \underbrace{- \frac{L_M}{N_2} i_{1AC} + \frac{L_M}{N_1} i_{2AC} + \frac{L_M}{N_2} I_{1biasT_1}}_{\Phi'_{21}} \end{cases} \tag{6.11}$$

From (6.11), the primary side leakage flux Φ'_{11} increases, resulting in HFT magnetic flux imbalance. Potential transformer saturation will happen and even destroy the DAB module and deteriorate the iMMC-SST. In the T_5 fault, the HFT currents are changed as follows

$$\begin{cases} i_1 = i_{1AC} \\ i_2 = i_{2AC} + I_{2biasT_5} \end{cases} \tag{6.12}$$

Based on (6.12), the magnetic fluxes of the HFT under T_5 fault can be denoted as

$$\begin{cases} \Phi_{1T_5} = \underbrace{\frac{L_1}{N_1} i_{1AC}}_{\Phi''_{11}} + \underbrace{\frac{L_M}{N_2} i_{1AC} - \frac{L_M}{N_1} i_{2AC} - \frac{L_M}{N_1} I_{2biasT_5}}_{\Phi''_{12}} \\ \Phi_{2T_5} = \underbrace{\frac{L_2}{N_2} i_{2AC} + \frac{L_2}{N_2} I_{2biasT_5}}_{\Phi''_{22}} \underbrace{- \frac{L_M}{N_2} i_{1AC} + \frac{L_M}{N_1} i_{2AC} + \frac{L_M}{N_1} I_{2biasT_5}}_{\Phi''_{21}} \end{cases} \tag{6.13}$$

The secondary side leakage flux Φ''_{22} increases and leads to the same results as the T_1 fault. Due to the overcurrent and HFT saturation issues in the fault conditions, a fault-tolerant scheme is indispensable for the safety and operation of the faulty DAB module and the iMMC-SST system.

6.2. Proposed Fault-Tolerant Scheme

The OC fault behaviors will vary according to the adopted different power switches. Two scenarios should be considered: 1. When IGBT (or MOSFET with additional diode) is applied, the current can still flow through diodes with defective gate drivers or destroyed switches; 2. If the MOSFET is used without extra diodes, the OC fault will destroy the whole switch module so that the current cannot flow through the intrinsic body diode. This section aims to deal with the first scenario, which assumes that all the free-wheeling diodes continue to provide current paths under power switch OC fault such that the DAB module will not be shut down immediately. It gives the possibility to realize fault-tolerant operation in the faulty DAB module without using conventional redundancy schemes.

The fault diagnosis methods of the DAB converter have been well studied in [137], [138] and show that the fault conditions can be identified and located within three

switching cycles, which will not be discussed further in this part. When the fault conditions are detected, potential overcurrent and the HFT saturation issues need to be solved according to the fault analysis in Section 6.2. The control diagram of the fault-tolerant scheme is depicted in Figure 6.4.

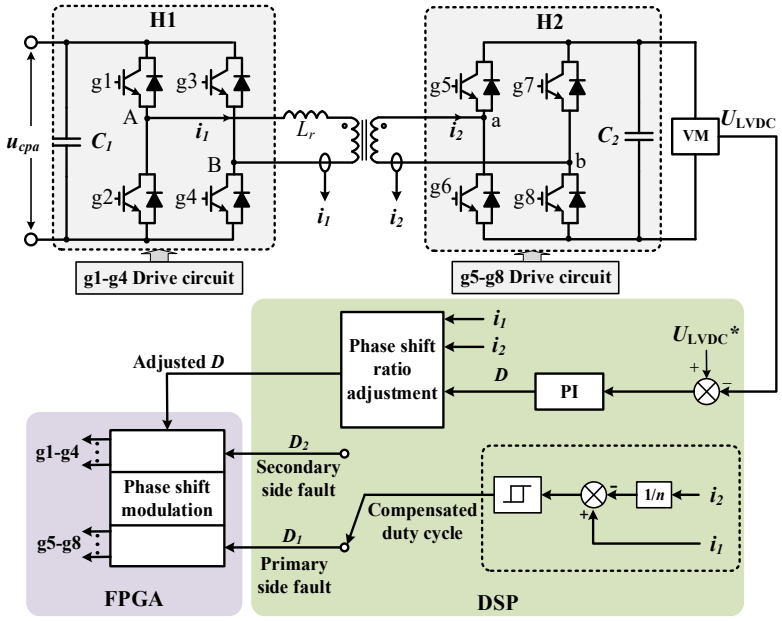

Figure 6.4 Control diagram of the fault-tolerant scheme

In this figure, i_1, i_2, and D are sampled and updated for the fault diagnosis process and fault-tolerant scheme. When D ranges between 0 and 0.25, the peak current under the faults will not surpass the rated current values; while overcurrent issue will occur when D is located between 0.25 and 0.5, D is reduced to 0.25 to achieve the residual maximum transmission power of the faulty DAB module under the fault conditions happened on either H1 bridge or H2 bridge.

According to (6.8) and (6.9), the corresponding new bias currents under both faults can be derived.

$$I'_{1biasT_1} = -\frac{nU_{\mathrm{LVDC}}}{4f_d L_s}\left(2D'-1+k\right) \tag{6.14}$$

$$I'_{2biasT_5} = \frac{u_{cpa}}{4f_d L_s}\left(k+1\right)D'' \tag{6.15}$$

In T_1 and T_5 faults, to eliminate the increased magnetic fluxes caused by the DC bias currents, the compensated DC currents I_{dc2} in T_1 fault and I_{dc1} in T_5 fault are generated based on $I'_{1biasT1}$ and $I'_{2biasT5}$. The new HFT magnetic fluxes under T_1 fault with DC current injection can be expressed as

$$\begin{cases} \Phi_{1T_1comp} = \underbrace{\frac{L_1}{N_1} i_{1ac} + \frac{L_1 I'_{1biasT_1}}{N_1}}_{\Phi_{11compT_1}} \underbrace{+ \frac{nL_M I'_{1biasT_1}}{N_1} - \frac{L_M I_{dc2}}{N_1} + \frac{L_M}{N_2} i_{1ac} - \frac{L_M}{N_1} i_{2ac}}_{\Phi_{12compT_1}} \\ \Phi_{2T_1comp} = \underbrace{\frac{L_2}{N_2} i_{2ac} + \frac{L_2 I_{dc2}}{N_2}}_{\Phi_{22compT_1}} \underbrace{- \frac{L_M I'_{1biasT_1}}{N_2} + \frac{(L_M / n) I_{dc2}}{N_2} - \frac{L_M}{N_2} i_{1ac} + \frac{L_M}{N_1} i_{2ac}}_{\Phi_{21compT_1}} \end{cases} \tag{6.16}$$

where I_{dc2} has the following relationship with $I'_{1biasT1}$,

$$I_{dc2} = nI'_{1biasT_1} = \frac{V_{dc2}}{R_2} = \frac{U_{\mathrm{LVDC}} D_2}{R_2} \tag{6.17}$$

Likewise, the fluxes under T_5 fault with DC current injection can be derived as

$$\begin{cases} \Phi_{1T_5comp} = \underbrace{\frac{L_1}{N_1} i_{1ac} + \frac{L_1 I_{dc1}}{N_1}}_{\Phi_{11compT_5}} \underbrace{+ \frac{nL_M I_{dc1}}{N_1} - \frac{L_M I'_{2biasT_5}}{N_1} + \frac{L_M}{N_2} i_{1ac} - \frac{L_M}{N_1} i_{2ac}}_{\Phi_{12compT_5}} \\ \Phi_{2T_5comp} = \underbrace{\frac{L_2}{N_2} i_{2ac} + \frac{L_2 I'_{2biasT_5}}{N_2}}_{\Phi_{22compT_5}} \underbrace{- \frac{L_M I_{dc1}}{N_2} + \frac{(L_M / n) I'_{2biasT_5}}{N_2} - \frac{L_M}{N_2} i_{1ac} + \frac{L_M}{N_1} i_{2ac}}_{\Phi_{21compT_5}} \end{cases} \tag{6.18}$$

where I_{dc1} has the following relationship with $I'_{2biasT5}$,

$$I_{dc1} = \frac{1}{n} I'_{2biasT_5} = \frac{V_{dc1}}{R_1} = \frac{U_{cpa} D_1}{R_1} \tag{6.19}$$

In the iMMC-SST, k keeps changing due to the fluctuation of u_{cpa}. Hence, a hysteresis controller is adopted to regulate the DC compensated currents for both fault conditions, as shown in Figure 6.4.

The waveforms of the faulty DAB module under T_1 and T_5 faults with the fault-tolerant scheme are shown in Figure 6.5 and Figure 6.6, respectively. The compensated currents (I_{dc2} and I_{dc1}) have the same polarity as the DC bias currents ($I'_{1biasT1}$ and $I'_{2biasT5}$).

Two zero-voltage short periods with $0.5D_2T_{hs}$ are added in the negative cycle of u_{ab} to generate the desirable I_{dc2} under the T_1 fault. Likewise, two $0.5D_1T_{hs}$ periods are added in the positive half cycle of u_{AB} to generate I_{dc1} under T_5 fault.

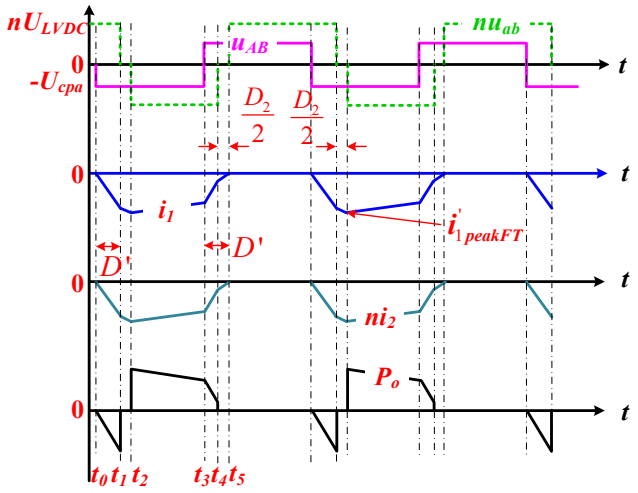

Figure 6.5 Waveforms of the fault-tolerant operation with T_1(T_4) OC fault

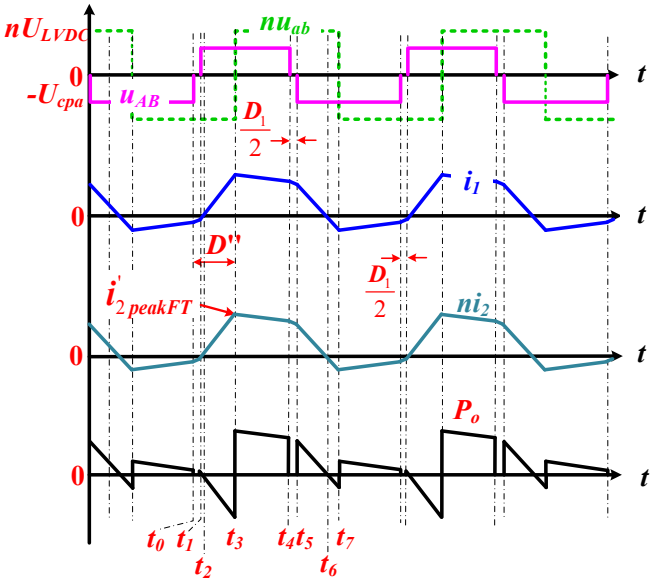

Figure 6.6 Waveforms of the fault-tolerant operation with T_5(T_8) OC fault

In Figure 6.5, since $i_1(t_0)=i_1(t_5)=0$, its peak value with a fault-tolerant scheme can be derived with the same derivation as (6.6).

$$i'_{1peakT_1FT} = -\frac{nU_{\mathrm{LVDC}}}{2f_dL_s}\left(kD + D + \frac{kD_2}{2}\right) \tag{6.20}$$

The new bias current after the fault-tolerant activation can be obtained via calculating the average value of i_1, as shown in (6.21).

$$I''_{1biasT_1} = -\frac{nU_{\mathrm{LVDC}}}{8f_dL_s}\left(2D+2kD+\frac{kD_2^2}{2}-\frac{DD_2}{2}-\frac{kDD_2}{2}\right) \tag{6.21}$$

Similarly, because $i_2(t_2)=i_2(t_6)=0$ in Figure 6.6, its peak value and new bias current are expressed as

$$i'_{2peakT_5FT} = \frac{U_{cpa}}{2f_dL_s}\left(D-\frac{D_1}{2}\right) \tag{6.22}$$

$$I''_{2biasT_5} = \frac{u_{cpa}}{32f_dL_s(k+1)}\begin{pmatrix}16D-8D_1-4kD_1+16kD-12k^2D_1-3kD_1^2+D_1^2+8k^2\\+8k^2D_1^2+4DD_1-16kDD_1-4k^2DD_1-8\end{pmatrix} \tag{6.23}$$

According to (6.17) and (6.19), owing to the small parasitic resistance, the value of D_2 and D_1 are much smaller than D' and D'', such that the influence on u_{AB} and u_{ab} can be ignored.

By using the proposed fault-tolerant scheme and ignoring power consumed by the parasitic components, the transmission power of the faulty DAB module under T_1 fault can be derived via integrating the product of u_{AB} and i_1 in one switching cycle.

$$P_{T_1FT} = \frac{nu_{cpa}U_{\mathrm{LVDC}}}{8f_dL_s}\left(2D+2kD-2kD^2-2D^2-\frac{3}{2}DD_2-\frac{3}{2}kDD_2\right) \tag{6.24}$$

Its maximum possible value can be achieved when k=1 and D=0.25.

$$P_{T_1FT\max} = \frac{nu_{cpa}U_{\mathrm{LVDC}}}{8f_dL_s}\left(\frac{3}{4}-\frac{3}{4}D_2\right) \le 0.75P_{norm} \tag{6.25}$$

where P_{norm} is rated power transferred by a DAB module under normal conditions. Under the T_5 fault, the transmission power with the fault-tolerant scheme can be calculated similarly to the T_1 fault.

$$P_{T_5FT}=\frac{nu_{cpa}U_{\mathrm{LVDC}}}{32f_dL_s\left(k+1\right)}\begin{pmatrix}12k^2D_1^2-kD_1^2-D_1^2\\+4k^2DD_1-8kDD_1+4DD_1\\-16k^2D_1-4kD_1-4D_1\\-8k^2D^2-16kD^2-8D^2\\+16kD+16D+8k^2-8\end{pmatrix} \tag{6.26}$$

Its maximum value can also be obtained with k=1 and D=0.25.

$$P_{T_1FT\max}=\frac{nu_{cpa}U_{\mathrm{LVDC}}}{8f_dL_s}\left(\frac{3}{4}+\frac{3}{4}D_1^2-3D_1\right)\le 0.75P_{norm} \tag{6.27}$$

The fault DAB module can maintain at least 75% rated transmission power under both fault conditions. λ_{LVDC} is the ratio between the actual and the rated MV-LV power transfer capability of the iMMC-SST. According to (24) and (26), λ_{LVDC} has the following relationship.

$$\frac{\left[\left(6N-1\right)+0.75\right]P_{norm}}{6NP_{norm}}\le\lambda_{\mathrm{LVDC}}\le 1 \tag{6.28}$$

As a result, the iMMC-SST's residual MV-LV power transfer capability increases with the SM number of each arm. However, it should be noted that the DC voltages of the healthy H-bridges will be slightly affected by the proposed fault-tolerant scheme. When the switch OC fault occurs on the H2 bridge, the compensated duty cycle is added to the gating signals of the H1-bridge, influencing the u_{cpa} and resulting in the arm voltage mismatch. This disturbance can be effectively suppressed by additional neutral point shift control [123] of the MMC part, which will not be further discussed in this chapter.

Therefore, the proposed fault-tolerant method enables the possible maximum power transfer capability between the MV and LV ports under DAB module IGBT OC fault without using a redundancy scheme such that the iMMC-SST system cost and volume can be significantly reduced with higher reliability and robustness.

6.3. Simulation and Experiment Verifications

In this section, the full-scale 13-level MATLAB/Simulink model and a scaled-down 5 level experimental platform are built to verify the effectiveness of the proposed fault-tolerant scheme in the iMMC-SST system.

A. Simulation Results

A 2 MVA full-scale iMMC-SST MATLAB/Simulink model is built with twelve power modules in each arm. The parameters of the simulation model are listed in Table 6.1. Four operation modes are considered in the simulation verification, including the primary and secondary faults of one of the DAB modules of the iMMC-SST under positive (MV ports → LVDC port) and negative (LVDC port → MV ports) power transfer conditions.

Table 6.1 System Parameters for Simulation

Description	Value	Description	Value
Number of PMs per arm	12	SM DC voltage	1666 V
Rated MVAC power	2 MVA	MMC switching frequency	1 kHz
MVAC voltage	10 kV	DAB switching frequency	6 kHz
MVDC voltage	20 V	Transformer turns ratio	1666:800
LVDC voltage	800 V	DAB inductance	3.5 mH
Line frequency	50 Hz	Rated MVDC power	1 MVA
SM capacitor	1.3 mF	Rated LVDC power	1 MVA

Condition 1 (T_1 fault with positive power transmission) and Condition 2 (T_5 fault with positive power transmission): the MVAC is connected to a 10 kV grid to transfer 1 MVA power to the MVDC and LVDC ports, respectively. Under normal operation with positive power flow, the three phases of the iMMC-SST are maintained in balanced mode with these two cases. The corresponding simulation results are depicted in Figure 6.7. The HFT currents (i_1 and i_2) are in phase and maintain balance mode. The primary-side voltage u_{AB} is ahead of the voltage $u_{ab,}$ indicating that the power is transferred from the MMC side to the LVDC port.

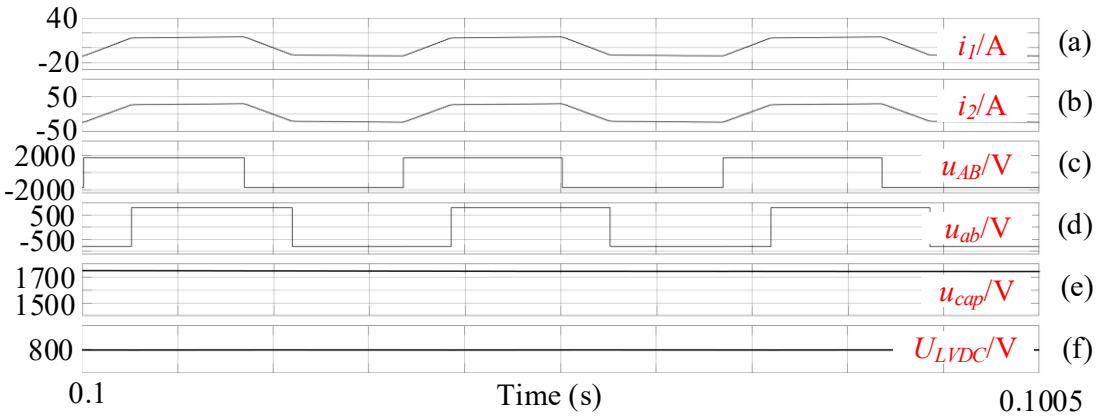

Figure 6.7 **Simulation results under the normal condition with positive power flow (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.**

As shown in Figure 6.8, the T_1 fault occurs at 0.15 s, and the fault-tolerant scheme is activated 100 ms after the fault. After the proposed fault-tolerant scheme activation, a duty cycle is generated and injected into the healthy-side voltage to generate the compensated DC current that occurred in the faulty side of the DAB, as illustrated in Figure 6.9(d). By using the fault-tolerant scheme, the overcurrent and HFT saturation issues are prevented. As shown in s 6.8 (e) and (f), the SM capacitor and LVDC bus voltage are not affected.

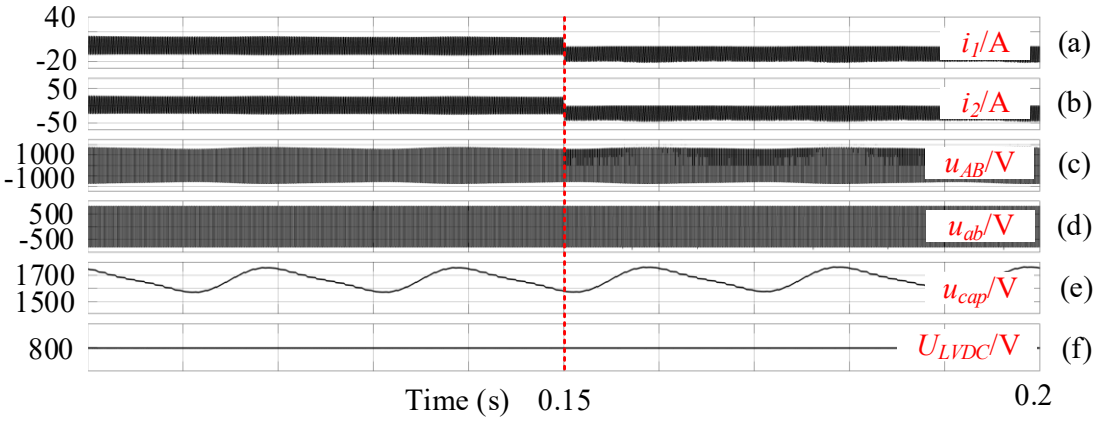

Figure 6.8 **Total Simulation results under T_1 OC fault with positive power flow (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.**

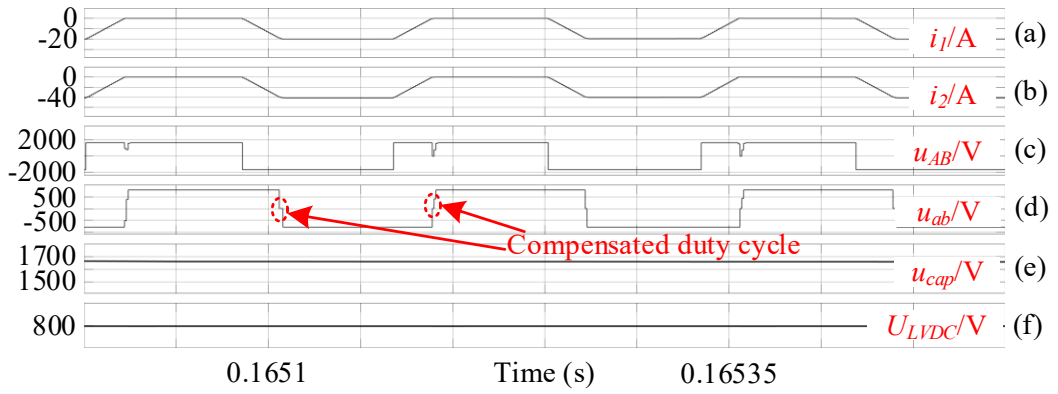

Figure 6.9 Simulation results under T_1 OC fault with positive power flow after fault-tolerant activation (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.

The simulation results of Condition 2 are illustrated in Figure 6.10 and Figure 6.11， respectively. Likewise, the fault happens at 0.15 s, and the fault-tolerant scheme starts 100 ms after the fault. As shown in Figure 6.10, the overcurrent and HFT saturation issues of the faulty DAB module are solved without significant influence on the system operation. In Figure 6.10(e) and (f), the SM capacitor voltage is kept balanced, and the LVDC bus voltage is not affected. The detailed simulation results with fault-tolerant activation are shown in Figure 6.11. By injecting the DC current on the healthy side of the DAB module, the unbalanced magnetic flux can be compensated. As illustrated in Figure 6.11(a) and (b), i_1 and i_2 are all flowing in the positive direction. In Figure 6.11(c), the compensated DC current is injected via adding extra zero-voltage periods in u_{AB}.

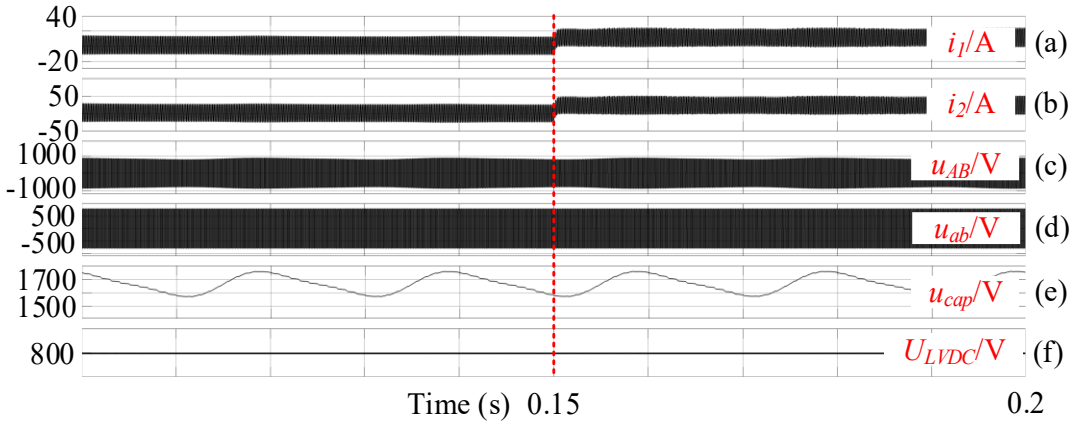

Figure 6.10 Total Simulation results under T_5 OC fault with positive power flow (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.

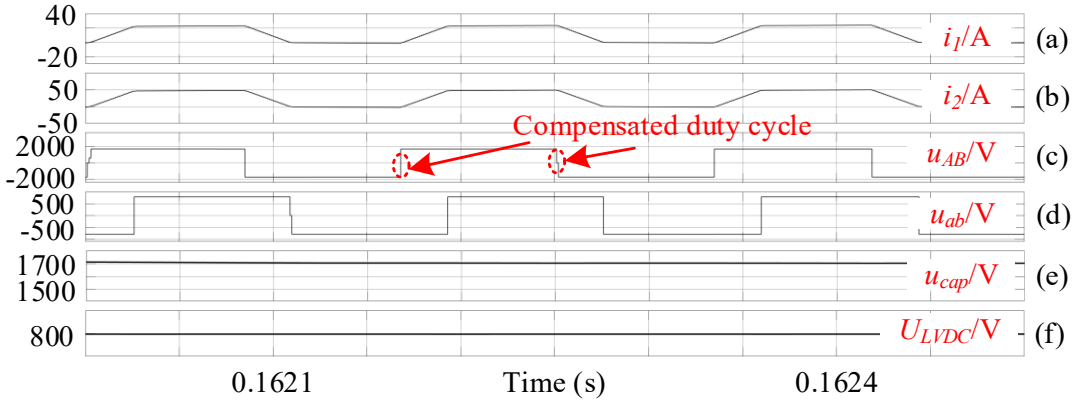

Figure 6.11 Simulation results under T_5 OC fault with positive power flow after fault-tolerant activation (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.

Condition 3 (T_1 fault with negative power transmission) and Condition 4 (T_5 fault with negative power transmission): the MVAC is connected to a 10 kV grid; the MVDC port is connected to a purely resistive load (400 ohm), and the LVDC port is connected to 500 kVA power source. Hence, the power transferred to the MVDC port is evenly supplied by the MVAC port and the LVDC port. Owing to the same fault characteristics as Condition 2, the simulation results of Condition 4 will not be further discussed in this

section. The simulation results under normal operation are displayed in Figure 6.12. The HFT currents (i_1 and i_2) are in phase and maintain balance mode. The primary-side voltage u_{AB} is lagging the secondary-side of the voltage $u_{ab,}$ indicating that the power is transferred from the LVDC port to the MMC side.

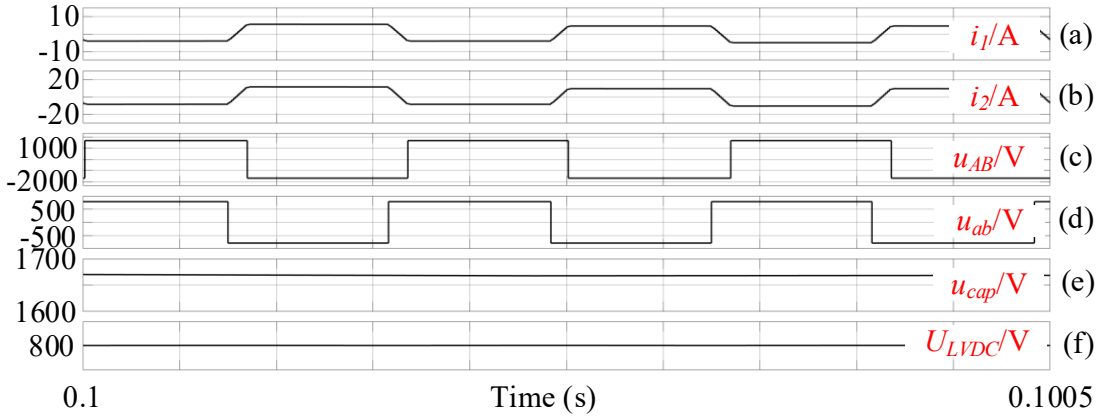

Figure 6.12 Simulation results under normal condition with negative power flow (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.

Likewise, the fault occurs at 0.15 s, and the proposed fault-tolerant scheme is activated 100 ms after the fault, as shown in Figure 6.13. In Figure 6.13(a) and (b), the primary- and secondary-side currents i_1 and i_2 are flowing in the negative direction during fault-tolerant activation. And the SM capacitor voltage connected to the faulty unit and the LVDC bus voltage is not affected, as shown in Figure 6.13(e) and (f).

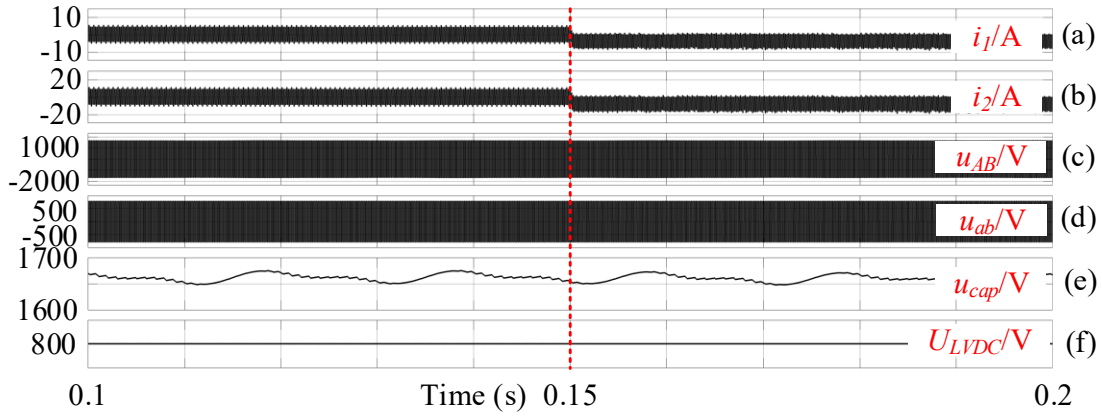

Figure 6.13 Total Simulation results under T_1 OC fault with negative power flow (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.

The detailed simulation results fault-tolerant activation is shown in Figure 6.14. The compensated DC current is injected into the i_2 to deal with the unbalanced magnetic flux. By doing so, the overcurrent and HFT saturation issues are prevented.

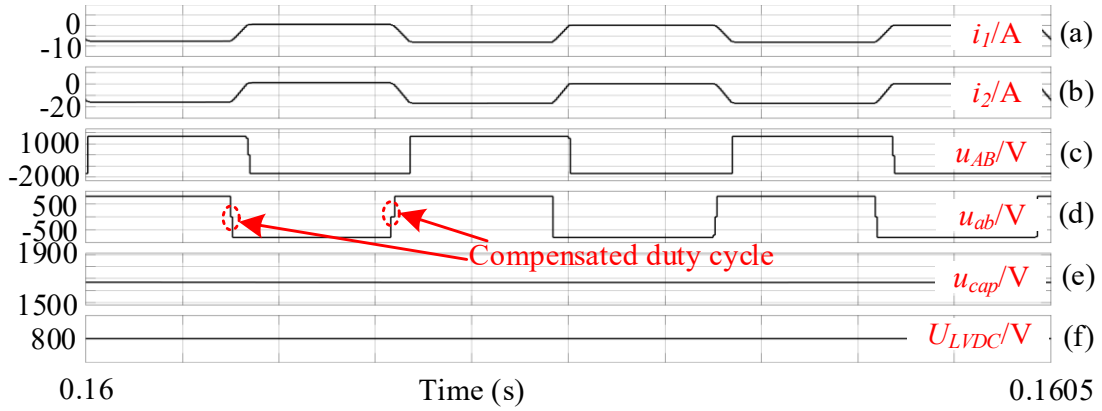

Figure 6.14 Simulation results under T_1 OC fault with negative power flow after fault-tolerant activation (a) the primary-side current of the faulty DAB; (b) the secondary-side current of the faulty DAB; (c) the primary-side voltage of the faulty DAB; (d) the secondary-side current of the faulty DAB; (e) the SM capacitor voltage; (f) the LVDC bus voltage.

B. Experimental Results

A 4.8 kVA scaled-down iMMC-SST experimental platform is constructed to verify the effectiveness of the proposed fault-tolerant strategy. The parameters of the

experimental platform are listed in Table 6.2. Figure 6.15 shows the picture of the 5-level iMMC-SST prototype containing twelve power modules.

Table 6.2 System Parameters for Experiment

Description	Value	Description	Value
Number of PMs per arm	4	SM DC voltage	40 V
Rated power	4.8 kVA	MMC switching frequency	1 kHz
MVAC voltage	80 V	DAB switching frequency	6 kHz
MVDC voltage	160 V	Transformer turns ratio	1:1
LVDC voltage	40 V	DAB inductance	340 μH
Line frequency	50 Hz	Positive power flow	1.8 kVA
SM capacitor	10 mF	Negative power flow	1.2 kVA

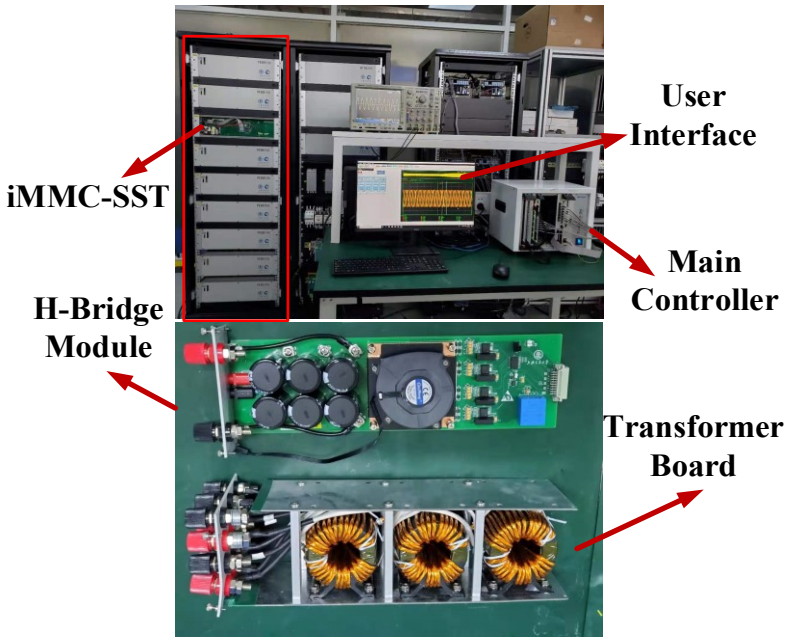

Figure 6.15 Experimental Platform

Under normal conditions with positive power flow, the three phases of the iMMC-SST are well-regulated in balanced mode, and the submodule capacitor modes are considered and tested in the experiment with different power directions, i.e., 1) $0.25<|D|<0.5$ and 2) $0<|D|<0.25$. The experimental results assume that the faults are detected and localized. Once the iMMC-SST achieved the normal steady state, T_1 (or T_5) was forced to be switched off to emulate the open-circuit faults. The fault-tolerant scheme was activated 0.15 ms after the faults.

The T_1 OC fault condition waveforms with positive power flow are illustrated in Figure 6.16. Under this condition, each DAB module needs to transfer 75 W where D equals 0.26 (>0.25). After the fault-tolerant control is activated, the phase shift ratio of the faulty DAB module is limited to 0.25 to prevent the potential overcurrent issue. Figure 6.16(a) depicts the waveforms with the entire process of the faulty DAB module, which shows the DAB reached another steady state (i_{1max}=i_{2max}≈8 A) when the fault-tolerant scheme was enabled. Additionally, the u_{cpa} of the faulty DAB module is slightly increased by the clustered voltage control to maintain the three-phase energy balance due to the reduced D, as shown in Figure 6.16(b). Figure 6.16(c) shows that u_{AB} is in the leading phase indicating the power flows from the MVAC port to the LVDC port. Different from Figure 6.1, the overcurrent and transformer saturation issues were effectively solved by injecting a DC bias current to the H2 bridge, as shown in Figure 6.16(d). As shown in Figure 6.17, except for the compensated duty cycle is injected in the H1 bridge, the waveforms under the T_5 OC fault revealed almost the same features as the T_1 fault scenario.

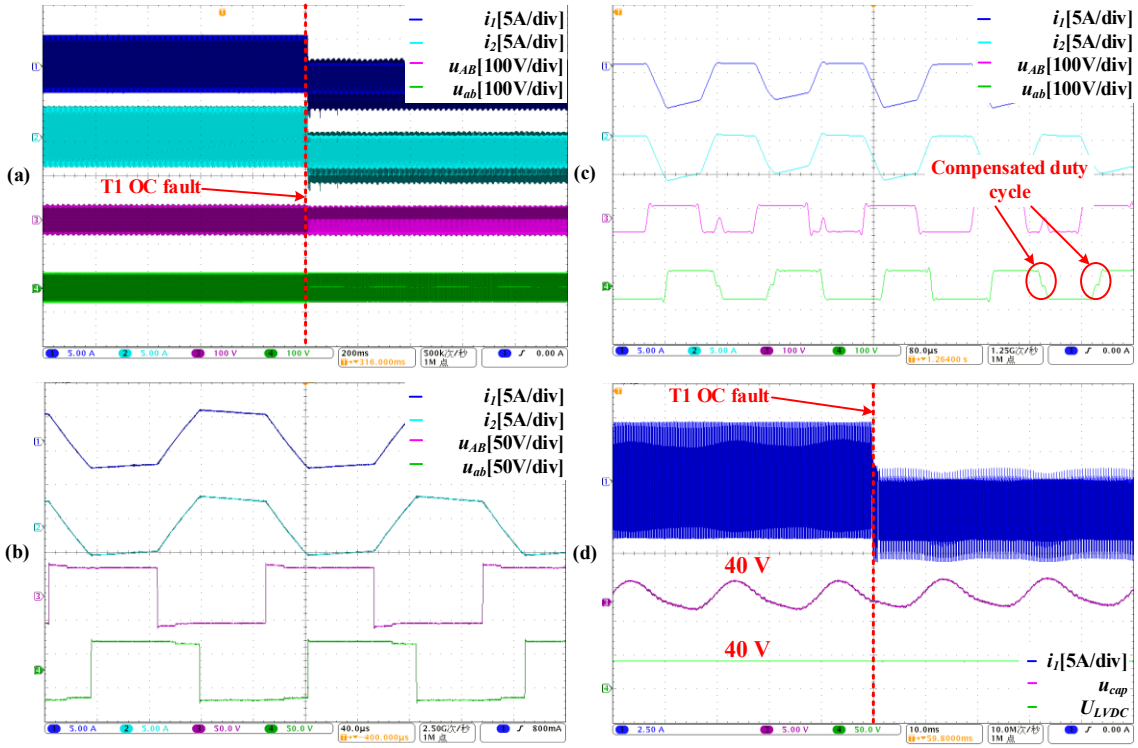

Figure 6.16 Waveforms under T_1 OC fault with positive power flow (a) the faulty DAB module waveforms in the whole process; (b) the input and output DC voltages of the faulty DAB module; (c) the faulty DAB module waveforms under normal condition; (d) the faulty DAB module waveforms with activation of the fault-tolerant scheme.

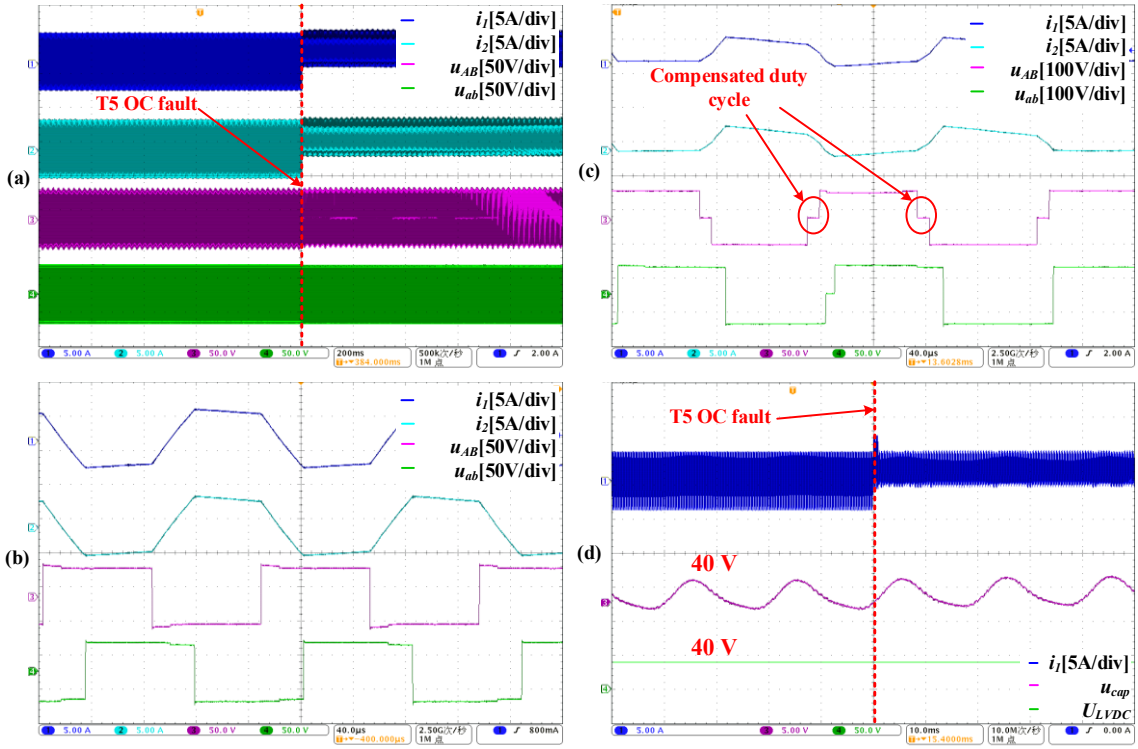

Figure 6.17 **Waveforms under T_5 OC fault with positive power flow (a) the faulty DAB module waveforms in the whole process; (b) the input and output DC voltages of the faulty DAB module; (c) the faulty DAB module waveforms under normal condition; (d) the faulty DAB module waveforms with activation of the fault-tolerant scheme.**

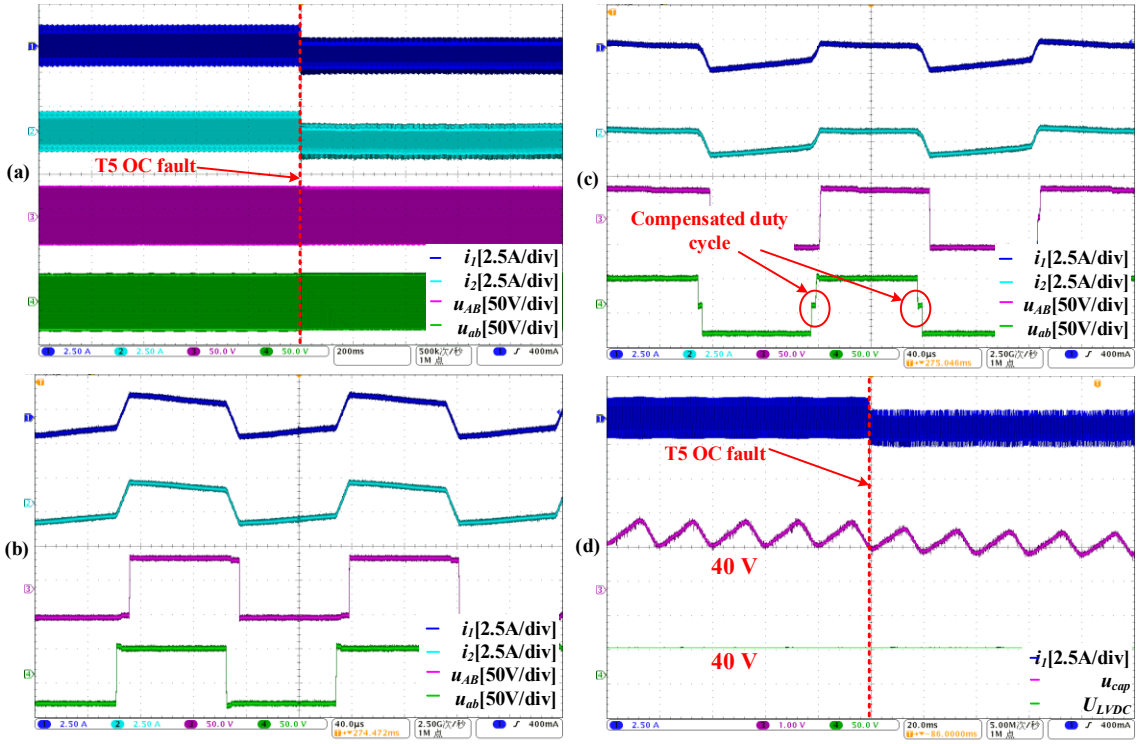

Figure 6.18 Waveforms under T_5 OC fault with negative power flow (a) the faulty DAB module waveforms in the whole process; (b) the input and output DC voltages of the faulty DAB module; (c) the faulty DAB module waveforms under normal condition; (d) the faulty DAB module waveforms with activation of the fault-tolerant scheme.

When the power transfer direction is reversed with T_5 OC fault, the phase shift ratio for each DAB module is -0.15 (ranges between [-0.25, 0]), where u_{ab} is phase-leading. Figure 6.18(a) shows that the faulty DAB module reached another steady state when the fault-tolerant scheme was employed. In Figure 6.18(b), the u_{cpa} of the defective DAB module is marginally increased by the compensated duty cycle injection, which will not affect the operation of the MMC SST. Under this condition, only D_1T_{hs} is injected into the healthy H-bridge of the faulty DAB module, as shown in Figure 6.18(d).

The overcurrent and the transformer saturation issues are eliminated by the proposed fault-tolerant scheme such that the faulty DAB module can remain operational for power transmission under switch OC fault conditions. The experimental verifications under different modes and scenarios show good agreement with the theoretical analysis and prove the correctness and effectiveness of the proposed scheme.

6.4. Conclusion

Based on the detailed fault analysis for power switch OC faults in the DAB modules of the MMC SST, a fault-tolerant control scheme using DC current injection and the phase shift ratio adjustment is proposed in this chapter to address the previously overlooked DAB transformer saturation issue properly. When faults happen on either side of the DAB module, a DC bias current component will appear on the DAB module's faulty side and lead to magnetic flux imbalance and saturation of the DAB transformer. These fault characteristics will further result in PM damage and even deteriorate the operation of the iMMC-SST and its connected grids. The DAB module can achieve 75% bidirectional power transfer under DAB switch OC fault conditions when applying the fault-tolerant scheme. The overcurrent and the transformer saturation issues are eliminated to ensure system safety. The system reliability can be improved with the proposed scheme without using redundant modules. Experimental results validate the effectiveness and performance of the proposed control strategy.

It should be noted that the proposed strategy can also be applied to other non-resonant DAB module-based applications. It is also possible to use the method with the other phase shift modulation schemes for DAB, including extended phase-shift (EPS), dual phase-shift (DPS), and triple phase-shift (TPS) schemes, where the efficacy will require further investigation.

Chapter 7.

Summary, Conclusion, and Future Work

7.1. Summary and conclusion

In this thesis, a detailed analysis of external and internal abnormal conditions of the iMMC-SST used for the future hybrid distribution systems is presented, and the corresponding fault-tolerant schemes are proposed and studied in this thesis. The key contributions of the present dissertation can be summarized as follows:

1. The comprehensive considerations for the iMMC-SST grounding scheme design associated with the corresponding protection schemes were demonstrated according to the requirements of the connected distribution systems and the iMMC-SST. Then a grounding scheme specially designed for the iMMC-SST was proposed to verify the fault behaviors. The simulation results indicate that the external fault can propagate to the other distribution systems via the iMMC-SST, and the magnitude of the fault current and voltage can be effectively controlled via the grounding impedance so that the requirements of different grounding schemes can be satisfied.

2. The DAB IGBT OC fault in the iMMC-SST was analyzed in terms of the HFT magnetic flux. To overcome the overcurrent and magnetic flux imbalance, a DC bias current injection-based fault-tolerant scheme was proposed. The simulation and experimental results show that the overcurrent and HFT saturation problems are eliminated with at least three-quarters of the faulty unit's power transfer capability under normal conditions.

3. The SM IGBT OC fault analysis was conducted considering the detailed operation modes of the iMMC-SST. The simulation results show the agreement with the fault analysis. Unlike the conventional MMC applications, the fault characteristics and behaviors were demonstrated in detail, which revealed that the existing fault diagnosis and control-based fault-tolerant were not applicable for the iMMC-SST. Some of the fault conditions will not be influenced, implying that the faults are

undetectable, and the system can operate without activating the corresponding fault-tolerant schemes.

4. The global redundant scheme was proposed to address the iMMC-SST SM IGBT OC fault with less initial cost and volume. The proposed fault-tolerant scheme combines the redundant modules and the arm unbalanced control strategy such that different SM IGBT OC fault conditions can be solved with minimum performance degradation.

7.2. Suggestions for future work

Based on the experience gained and the results obtained in this research, the following suggestions may be considered for future work to improve the system's reliability and robustness further.

7.2.1. Comprehensive Fault-Tolerant Scheme for the iMMC-SST SM IGBT OC fault

The proposed SM IGBT OC fault-tolerant scheme mainly considered the fault conditions under specific operation modes of the iMMC-SST. Since the bidirectional power transfer can be achieved via the iMMC-SST, the fault may show different fault behaviors which invalidate the fault-tolerant scheme when the device changes its operation modes. Hence, a comprehensive fault-tolerant scheme should be made to solve the iMMC-SST SM IGBT OC fault under different operation modes for future work.

7.2.2. iMMC-SST SM IGBT OC fault diagnosis

According to the presented iMMC-SST SM IGBT OC fault analysis, the faulty SM showed different fault characteristics making the existing fault detection methods based on the SM capacitor voltage increase unable to identify the abnormal conditions under different operation modes. Besides, because the DAB module can also show some of the fault features, it is possible to use it to detect the fault conditions. Thus, improving the fault diagnosis methods to a more sensitive and accurate scheme is attractive in future work.

7.2.3. iMMC-SST DAB IGBT OC fault-tolerant strategy based on novel DAB topologies

Similar to the SM variants in the MMC applications, higher reliability and better fault-tolerant scheme can be achieved via different DAB topology variants. In this case, more potential fault-tolerant operation schemes can be proposed with less system performance degradation and initial cost on the redundant modules.

7.2.4. iMMC-SST MVDC Single Pole-to-Ground Fault Ride-Though Strategy

Except for the MVAC SLG fault condition, the SPG fault happened in the MVDC distribution system is another most seen external fault which should be seriously addressed. Owing to the multi-port feature of the iMMC-SST, the system is equipped with grid reconfiguration and restoration capability where the device should maintain the power supply to other healthy ports and poles with minimum influence of the fault propagation. So, an advanced control strategy should be proposed associated with the corresponding protection schemes to improve system reliability and robustness.

7.2.5. Energy Optimization of the DAB Modules with Fault-Tolerant Scheme

When the proposed DAB IGBT OC fault-tolerant scheme is activated, the faulty unit's power transfer capability is slightly changed compared with the other healthy DAB modules. This will lead to unbalanced power dispatch and increase the system power losses, especially under light load conditions. Therefore, further research on the control strategy for energy optimization should be carried out to cope with this issue.

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