Versatile Innovations
School of Engineering Science
Simon Fraser University
V5A 1S6
Versatile-innovations@sfu.ca

March 14, 1999

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, BC
V5A 1S6

RE: ENSC 370 Project – **Physiological Signal Data Logger Design Specifications**

Dear Dr. Rawicz,

The attached document, *Physiological Signal Data Logger Design Specifications*, outlines the design specifications for our 16-channel signal data logger for physiological system that is to be used by the Living Lab, a joint venture between SFU and BCIT. This project will provide researchers at the Living Lab a lightweight portable data logger that is capable of monitoring and recording 16 different input physiological signals captured by already available biomedical sensors and electrodes.

This selected electronic components and the specific design specifications of our system are listed in this document. The signal data logger has three modes of operation: Configuration, Logging, and Uploading. There is also a software control program running on a Windows 9x personal computer to program the signal data logger.

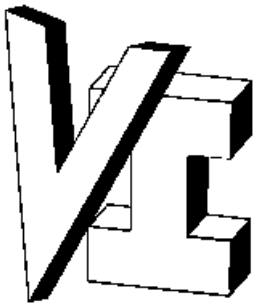
Versatile Innovations consists of four innovative and enthusiastic third-year engineering students – Fiona Chan, Karen Chan, Andy Jien, and Sean Shieh. If you have any questions or concerns, please feel free to contact me at 420-0782 or yjien@sfu.ca.

Sincerely,
Andy Jien, Chairperson

Versatile Innovations

Enclosure: *ENSC 370 Physiological Signal Data Logger Design Specifications*

VERSATILE INNOVATIONS



Design Specifications
for a
Physiological Signal Data Logger

Submitted by: Versatile Innovations
Fiona Chan, Karen Chan, Andy Jien, Sean Shieh

Contact: Andy Jien
School of Engineering Science
Simon Fraser University
versatile-innovations@sfu.ca

Submitted to: Andrew Rawicz
School of Engineering Science
Simon Fraser University

Ivan Li
Project Leader
Health Applied Research and Development
Technology Centre

Steve Whitmore
School of Engineering Science
Simon Fraser University

Date: March 16, 1999

Abstract

Versatile Innovations' 16-channel physiological signal data logger is a research development tool that allows monitoring and recording of electrical activities of the heart, muscle and brain, the arterial oxygen saturation level in the blood stream, and body temperature. It also records data collected from force, acceleration, and pressure sensors to monitor physical activities.

Surface electrodes and sensors are attached to the body of a subject to acquire the input signals of interest, and signals are pre-amplified before the signals are fed into the signal data logger. The signals are then passed through a series of Butterworth filters to make them suitable to be processed by an analog-to-digital converter (ADC) which samples the continuous signal inputs. The resulting digital data are then put into a digital signal processor (DSP) for noise reduction and data compression by a number of DSP algorithms. Lastly, the digitally processed data are stored in random access memory (RAM) in the logger and are uploaded to a computer through RS-232 upon user's request.

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Introduction

Data is the key to any scientific research. Today, many data-recording devices for obtaining raw data are available in the market. Versatile Innovations' portable 16-channel signal data logger will provide researchers at the Living Laboratory with an effective way to collect data in order to conduct research activities that improve the "fit" between people and their daily environment. The physiological data logger

The purpose of this document is to describe the design specification of the 16-channel physiological signal data logger. The design specification of each part of the system and the selected components are discussed.

System Overview

The signal data logger will sample the physiological data from the test subject and store the data in the memory module inside. The data can then be later uploaded to a Microsoft Access database in a PC for analytical uses. Naturally, we can divide the system into two parts, the signal data logger and the control program that resides on the PC. Phase one of this project concentrates on the hardware and firmware design of the logger. The majority of the controlling software will be developed in phase two, which will commence in May 1999. This document will only outline the basic design of the control software on PC.

Figure 1 shows the overall structure of our signal data logger.

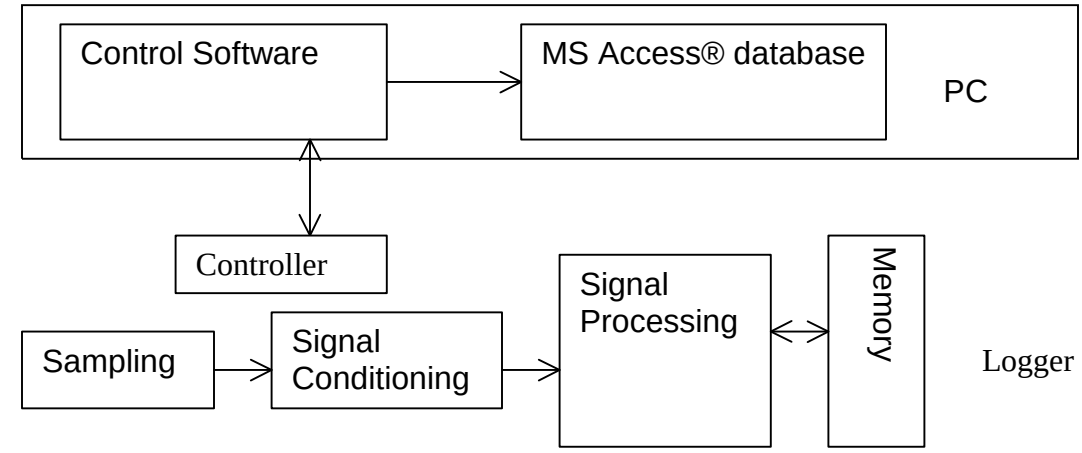

Figure 1: Signal data logger structure

Logger Design

To build a logger that performs to the requirement, we have designed a computer architecture with the components necessary for the project. Figure 2 is a block diagram of a simplified version for the logger. Along with the software on the personal computer, the Physiological Data Logger System is complete.

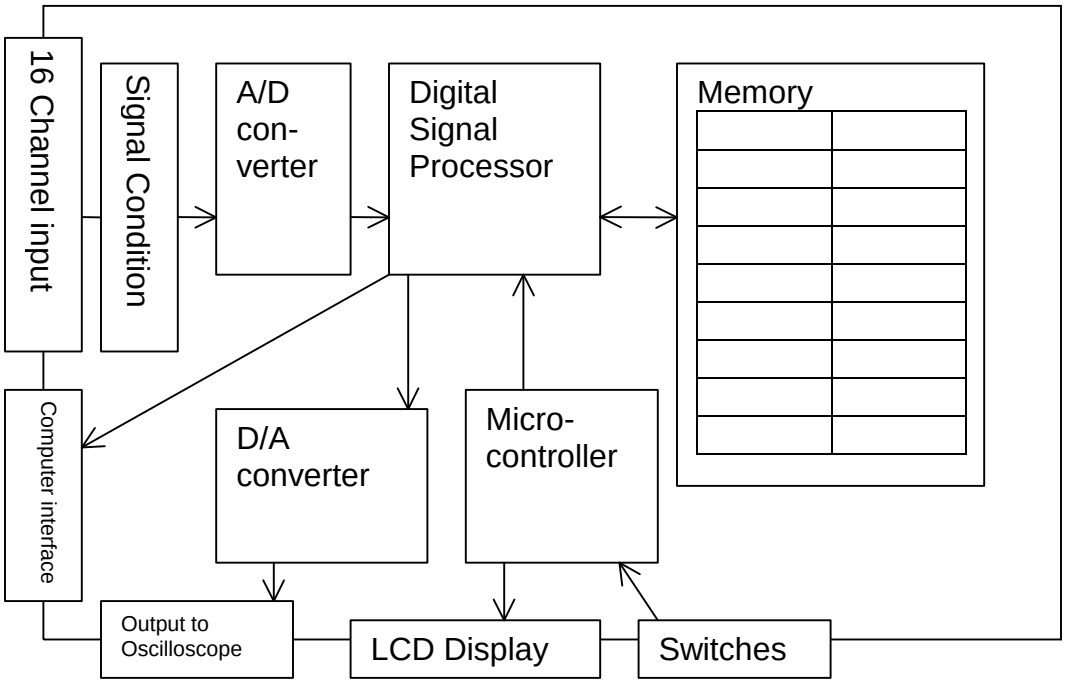

Figure 2: Logger design

Microcontroller Unit

Several microcontrollers are considered for our signal data logger, including the TM320C40 family, the PIC15, PIC16, PIC17, 68HC11, 68HC12, and 68HC16. A major consideration is that the microcontroller must be powerful and yet low in power consumption. Our design is to use two microcontrollers, one to handle the signal conditioning and the other dedicated to the user I/O and interrupts. The 68HC11K4 microcontroller is selected to handle the user I/O and interrupts for its performance, expandability, and low power consumption.

Digital Signal Processor

In the project, we are dealing with data collected from analog sources and stored digitally. In the process, we need to manipulate our data for purposes such as filtering and compressing. We will be performing digital signal processing (DSP) on the data collected. A digital signal processor is very suitable for this application. The DSP chip we've chosen for this application is among Texas Instruments (TI) TM320C4000 family. The processor is among the high end products in the market. However, with the investment in the DSP chip, we can use a basic microcontroller in our system. The justification for the selection will be apparent when the other parts of the system is discussed. The detailed information of this family of DSP chips is available at TI's homepage on the World Wide Web: http://www.ti.com. Here are the two most important features that affected our decision:

Table 1: Characteristics of TM320C4000

Speed	up to 60 MHz
Memory Addressing Capability	up to 4 GigaByte

Memory Storage

Memory Module

The signal data logger is to be sampled at a maximum combined frequency of 80kHz when all 16 channels are utilized. Since a typical sampling session lasts for an hour, the maximum storage space required for our signal data logger is calculated as follows:

$$\begin{aligned}\text{storage size} &= 80\times10^{3}\ {}^{sample}\!/_{s} \times 12\ {}^{bits}\!/_{sample} \times 3600\ {}^{s}\!/_{hr} \times {}^{hr}\!/_{hr} \\ &= 3456000000 bits \\ &\approx 412 MBytes\end{aligned}$$

Since we need a very large storage space, we decide to use DRAM SIMM modules due to its high capacity and low cost comparing to other forms of memory storage devices. This large memory storage space also means that we need an address bus that is at least 29 bits wide. This is another reason why we are using the Texas Instrument TM320C40 DSP microprocessor, since it has a 32-bit wide address bus.

Memory Access

Texas Instruments' TM320C40 family DSPs' have direct memory access controllers built in. The DSP itself can manage up to four gigabyte of memory. Some portion of the address will be used for memory mapped I/O. For example, the parallel port to the PC, LCD display, and the digital-analog converter will be mapped to their individual address thus facilitates easy input and output to the environment.

I/O Specification

LED Indicators

The Power LED (red in color) will indicate whether the signal data logger is turned on or not. It will also serve as the battery low indication. When the battery is low, the Power LED will blink to indicate low battery power.

For the first phase of the project, the Memory Full indicator and the Operation Mode indicator will also be implemented using LED's. However, these two indicators will be implemented using the LCD module in the second phase of the project. Three additional LED's will be used for the Operation Mode indicator, one for each mode. The LED indication for the Logging Mode will blink when the memory is full to serve as the Memory Full indicator.

LCD

The signal data logger will have a 20 by 4 LCD display to give a visual feedback to the user on the operation of the logger, such as the type of signal each channel is sampling and a memory full warning. The controller on the LCD module will communicate directly with the 68HC11K4 microcontroller to display the information on the LCD. Figure 3 shows the diagram for a LCD display.

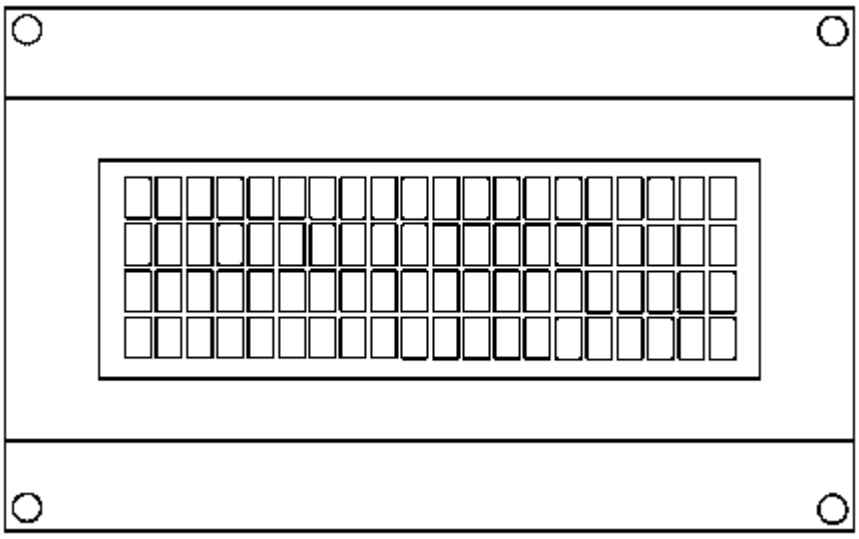

Figure 3: LCD display

Switches

Membrane switches will be used on the signal data logger to control some basic operations, such as turning the logger on and off, and pausing the operations. Membrane switches are chosen because they are waterproof. However, simple push switches will be used in place of membrane switches in the current stage. There are three switches: a ON/OFF switch to turn the signal data logger on and off; a PAUSE/RESUME switch to pause the sampling session and resume it; and a RESET switch to clear the data stored in the memory. The 68HC11K4 processor will treat the signals from the switches as interrupts and perform interrupt handling routines accordingly.

Software Design

The software components for this system can be categorized into two parts. They are the software component that reside on the personal computer and the components that are stored in the data logger. The components on the personal computer will be referred to as Logger Manager in the specification. The components on the logger itself will be called the firmware (**Firmware**).

Logger Manager

Logger Manager will be the main user interface in Configuration Mode and Upload Mode. The objective of the software is to provide the users with easy access to all the advance functions of the system such as user selectable gain, sampling rate and filtering scheme. Moreover, Logger Manager will also contain features that can hide the above advanced functions from inexperienced users and make the data logger system easy to manage. The features will be implemented by the introduction of profiles and wizards.

Firmware

The firmware is the heart of the system in Logging Mode. Components include software to operate the selectable features, software to manage the data on board, and one that interact with users through the LCD display and the switches.

Design Hierarchy

To design the above the Logger Manager and the firmware, we will need tool sets that allows us to work with the basic features of the personal computer and the hardware of our logger. In this documentation, the tools will be refereed as routines and the tool sets will be called the libraries. To further reduce the redundancy in the source code for the software, appropriate application programming interfaces (API's) will be developed using the tools. Figure 4 shows the dependence between the software components.

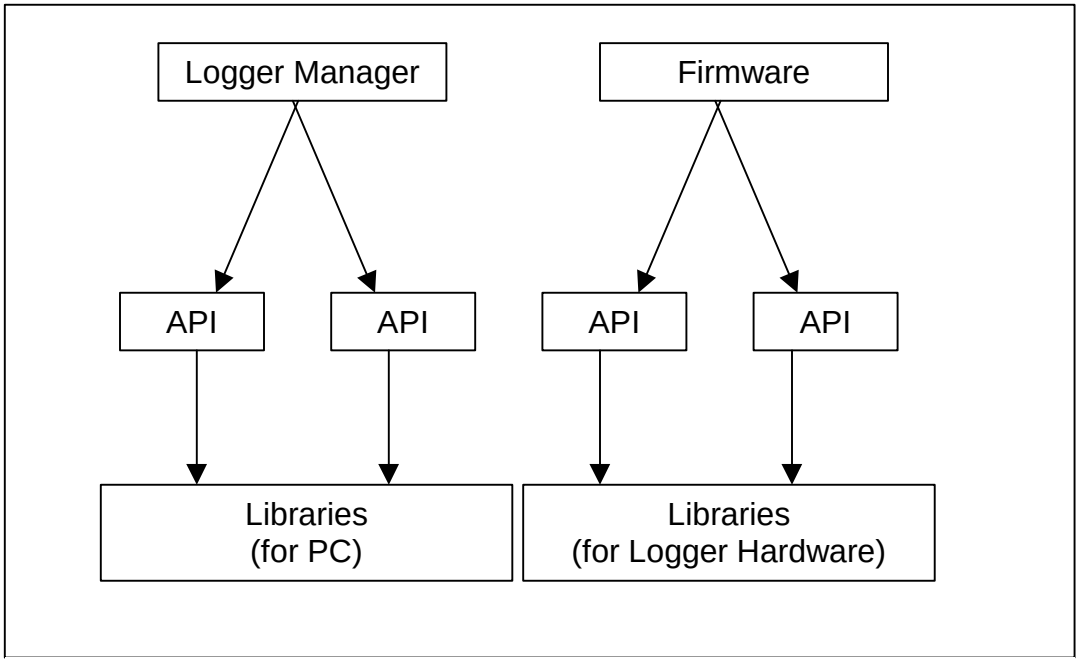

Figure 4: Software component

Development Platform

To implement the software components, Versatile Innovation has chosen C/C++ to be the computer programming language to develop the software in. The justification for the decision is mainly the flexibility and the popularity of these two languages. Moreover, a wide array of development tools can be found for C/C++ both for PC's and the hardware on the logger. The development tools can greatly raise the productivity when the software is being developed.

Graphical User Interface

The graphical user interface will be developed using Microsoft's Visual C++® development tool. Visual C++ allows easy implementation of a GUI while utilizing the power and flexibility of C++. The interface will be implemented based on the concept of profiles and wizards.

Logger/Computer Interface

In the system, the data logger will interface with a personal computer via parallel interface. In the functional specification, the interface was specified to be RS-232 as required by the client. However, after evaluating the performance of the proposed solution with RS-232, we have noticed that RS-232 is not sufficient to meet the requirement. After discussing the alternatives with the Living Lab, we have modified the computer interface from serial to parallel, which can improve the performance by a factor of ten in Upload Mode.

A bi-directional parallel port is needed on the host PC. Through the parallel interface on the logger, communication between the host and the logger can be established. In Configuration Mode, information mainly flows from the PC to the logger and reversed in Upload Mode.

Configuration Mode

In Configuration Mode, the logger receives command from the users via a personal computer. Figure 5 summarizes the Configuration Mode of signal data logger.

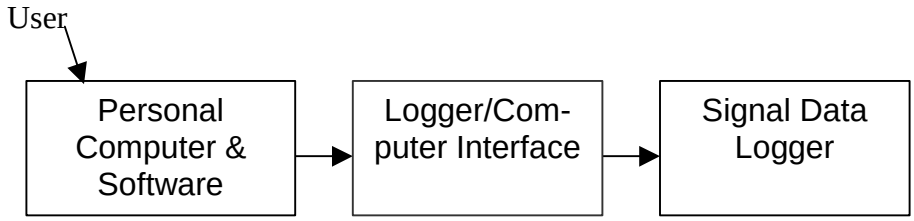

Figure 5: Configuration mode

Logging Mode

In Logging Mode, signals from the electrodes or sensors are being recorded. The Logging Mode has two functions: signal conditioning and data acquisition. Figure 6 shows the block diagram for this mode.

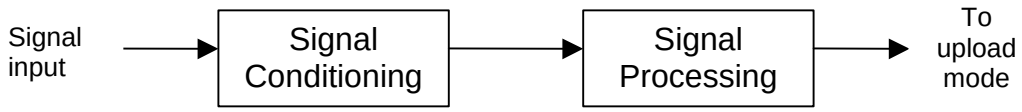

Figure 6: Logging mode

Signal inputs

The 16-channel physiological signal data logger takes in 16 different channels of signal inputs. As requested by the Living Laboratory, 8 of these channels are dedicated to EMG signal inputs acquired from surface electrodes. The other 8 channels are dedicated to signal inputs acquired from EEG and ECG surface electrodes, force and pressure sensors, accelerometer, pulse oximeter and thermistor.

A large selection of sensors and surface electrodes are available commercially. In order to suit the specific needs of each customer, the signal data logger does not impose any restriction on the choice of sensors or electrodes. To ensure the sampling quality of the input signals, preamplification is expected before the actual inputs to the signal data logger.

Signal Conditioning

In the signal conditioning stage, the input signals from the electrodes and sensors are taken differentially with respect to the ground level and amplified according to the user-specified gain. And to ensure no anti-aliasing when the analog signals are converted to digital data, the input signals must pass through an anti-aliasing filter.

Figure 7 shows the functional block diagram of the signal conditioning stage. The detailed schematic for the entire stage is provided in the appendix.

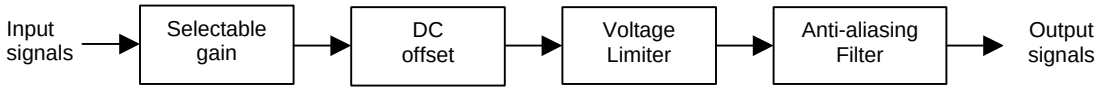

Figure 7: Functional block diagram of the signal conditioning stage

Selectable gain

The signal data logger allows user to set the gain of each input signal. The logger offers a user selectable gain of 1, 2, 4, 8 and 10. The desired gain is accomplished by the inverting amplifier shown in Figure 8.

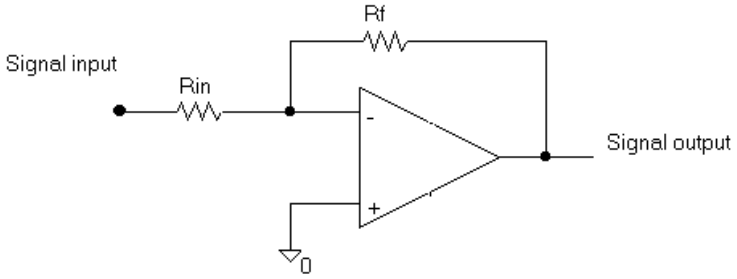

Figure 8: Inverting amplifier for selectable gain of the input signals

The gain of the inverting amplifier is:

$$Gain = -\frac{R_f}{R_{in}}$$

R_f is a digitally controlled potentiometer while R_{in} is a standard resistor with relatively constant resistance. To set the gain of the amplifier, user selects the desired resistance through a software application, which in term instructs a microcontroller when to send a suitable length of train of pulses to set R_f to bring forth the desirable gain.

Note that the gain is negative and thus the waveform is upside down after the user selectable gain. This can be resolved by complementing the sign bit using the digital signal processor in the signal processing stage.

DC offset

An analog-to-digital converter, A/D converter, is used in the signal processing stage. This A/D converter only allows an input voltage above 0V. To accommodate this, a DC offset of the signals is necessary.

Voltage Limiter

The A/D converter used in the signal processing stage has a limit on the input voltage range: 0V to 5V. This way, the maximum peak-to peak voltage of the input signals after preamplification and selectable gain is 5 V.

To ensure the voltage range, a voltage limiter is used to limit the input signal of the A/D converter to 0V to 5V. Figure 9 shows the voltage limiter circuit.

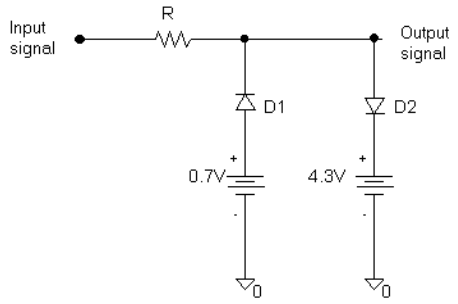

Figure 9: Voltage limiter circuit

To get voltage sources of 0.7V and 4.3V, a voltage divider is used, and this is shown in Figure 10.

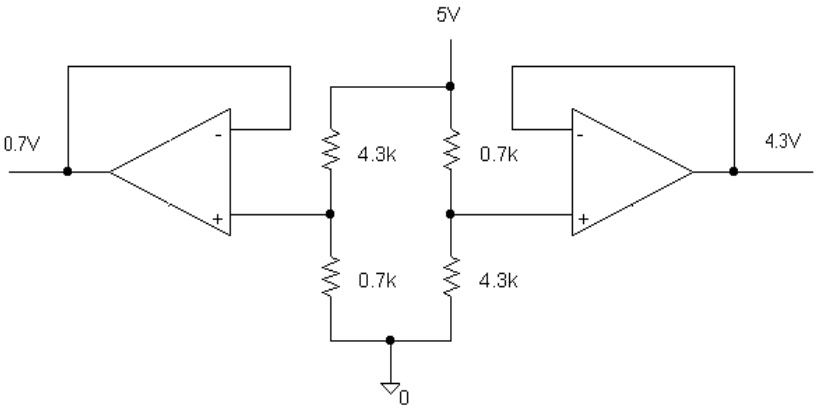

Figure 10: Voltage divider circuit

Anti-aliasing Filter

An analog electronic filter is used to remove frequency above one-half of the sampling rate that would alias during the sampling. To accomplish the objective and to ensure close resemble of the original waveform, a 4th order Butterworth low-pass filter is to be used. Figure 11[3] shows a 2nd order Butterworth low-pass filter.

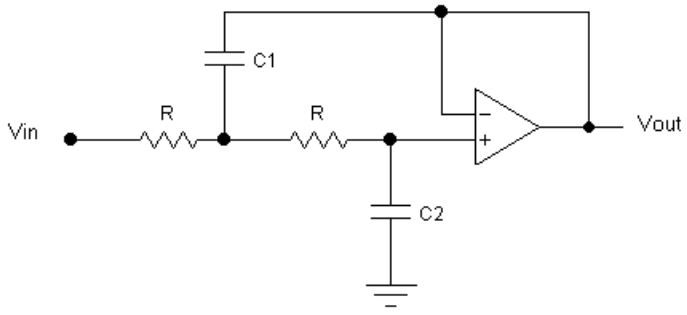

Figure 11: 2nd order Butterworth filter

The removal of high frequencies with close resemble of the original waveform requirement is achieved with this filter since a Butterworth is optimized to provide the sharpest roll-off possible from passband to stopband without allowing ripple in the passband. Moreover, the filter to be used will be of fourth-order, and this is generated by cascading two 2nd order Butterworth filters. Using higher order will further increase the rate of attenuation.

In our signal data logger, LMF40 High Performance 4th-Order Switched-Capacitor Butterworth Low-Pass Filter will be used. A switched-capacitor technique was chosen because it allows elimination of external component requirements and a clock-tunable cutoff frequency.

Signal Processing

In the signal processing stage, analog signals are digitized, and the digitized signals are processed and compressed digitally. To minimize storage space, digital compression will be done. Figure 12 shows the functional block diagram of the signal processing stage.

Figure 12: Functional block diagram of the signal processing stage

Analog-Digital Conversion

An A/D converter is used to digitize the analog input signals. The A/D converter that is used in the logger is ADC12048 12-bit plus sign 216kHz 8-channel sampling A/D converter from National Semiconductor. It has 8-channel multiplexing input and 12-bit parallel output. Some of the features include programmable acquisition time, which is useful for the application of our user selectable sampling rate of the signal. The multiplexer before the actual conversion within the converter allows us to include an anti-aliasing filter, as discussed in the signal conditioning stage, after the multiplexer and before the sampling of the signal. This way, the number of anti-aliasing filters in the design can be reduced.

Since the signal data logger has 16-channel input, two ADC12048 is needed. The output of these two A/D converters will be processed by DSP for filtering and compression of the signals.

Digital Filtering

Since the frequency range under interest for different types of input signals are different, filtering of the signals is necessary. Digital Signal Processing, DSP, is fast, flexible, and it supports parallel processing, thus a digital signal processor will be used to accomplish signal filtering. Digital filter will use appropriate band-pass range for different signals, and the digital signal processor will run the digital filter scheme/algorithm.

A digital finite impulse response (FIR) filter is chosen as the basic filtering scheme. A FIR filter has the advantage of flexibility in shaping its frequency response and is convenient to implement.[2] Although the computational complexity of a FIR filter is high, provided we use a DSP processor which has a fast instruction operation rate compared to our signal acquisition rate, the disadvantages of FIR filter can be overshadowed by its advantages.

The general filtering scheme is to calculate the impulse response of a FIR filter, and then apply a window to the filter to attenuate the Gibbs oscillations[1]. The design procedure for windowed FIR filter is listed as follows:

1. The amplitude response for a band-pass filter is

$$A_d(q) = \begin{cases} 1, & q_1 \le |q| \le q_2, \\ 0, & otherwise, \end{cases}$$

where q_1 and q_2 are band-edge frequencies in radians.

2. The ideal frequency response is

$$H_d^f(q) = A_d(q) \cdot e^{j(m0.5p - 0.5qN)},$$

where m=0 for a band-pass filter and N is the order of the filter. The order N of the filter will be calculated based on the transition bandwidth, and the calculation of N will be provided in step 6. Using $A_d(q)$ form step 1, $H^f_d(q)$ becomes

$$H_d^f(q) = \begin{cases} e^{-j0.5qN}, & q_1 \le |q| \le q_2, \\ 0, & otherwise. \end{cases}$$

3. Compute the impulse response of the ideal filter by the inverse Fourier transform formula

$$h_d[n] = \frac{1}{2p} \int_{-p}^{p} H_d^f(q) \cdot e^{jqn} dq \ .$$

in the case of a band-pass filter, $h_d[n]$ becomes

$$h_d[n] = \frac{q_2}{p} \text{sinc}\left[\frac{q_2(n-0.5N)}{p}\right] - \frac{q_1}{p} \text{sinc}\left[\frac{q_1(n-0.5N)}{p}\right]$$

4. Compute the coefficients of the filter by

$$h[n] \begin{cases} w[n]h_d[n], & 0 \le n \le N, \\ 0, & otherwise. \end{cases}$$

where $w[n]$ is the window function, and it is defined in step 5.

[1] Gibbs oscillations are oscillations occur at the pass-band and stop-band of an amplitude response of an impulse response truncation FIR filter.

5. Blackman window is chosen as the window being employ in step 4. Blackman window has pass-band ripple of 0.0017dB and stop-band attenuation of 53dB, which gives very good attenuation for the Gibbs oscillations. The Blachman window is

$$w_b[n] = 0.42 - 0.5\cos\left(\frac{2pn}{N-1}\right) + 0.08\cos\left(\frac{4pn}{N-1}\right), \quad 0 \le n \le N-1.$$

6. The order of the filter, *N*, is calculated by equating the transition bandwidth of the Blackman window, which is $12\pi/(N+1)$, with that of the band-pass filter. The equation looks like

$$\frac{12p}{N+1} = \text{transition bandwidth of the band-pass filter.}$$

The DSP suitable for our application should be capable of performing the complicated filtering algorithm mentioned above. Since the amount of data acquired by the logger will be very large, a compression algorithm (discussed in the next section) will also be apply to the data to save storage space. Moreover, the output from the DSP will go to the memory in the logger, the DSP should be able to handle the addressing of the data to the memory. The DSP that will be used in the logger is TM320C40 family from Texas Instruments. TM320C40 is capable to address 4GB of memory, and run 40 million instructions pre second.

Data Compression

The signal data logger is required to hold 3600 second worth of data, a large amount of data will result. In order to minimize storage space, data compression done by DSP is necessary. The compression algorithm will use discrete cosine transform to process the signal. In signals like ECG, this algorithm gives a best compression ratio of almost 27. On other signals, this algorithm provides a ratio of at least 2.

Output to Oscilloscope

The system allows the logger to display a processed signal out to an oscilloscope for viewing. To reconstruct the signal from digital data, we will convert the data into analog signal and pass the signal through a reconstruction filter.

For digital-analog converter, we choose AD7392 from Analogue Devices. For our application, we will configure the converter with one op-amp as shown in Figure 13 [1]. Figure 13 shows a circuit configuration that will enable the AD7392 to operate in bipolar mode and provide a voltage range from –5V to 5V.

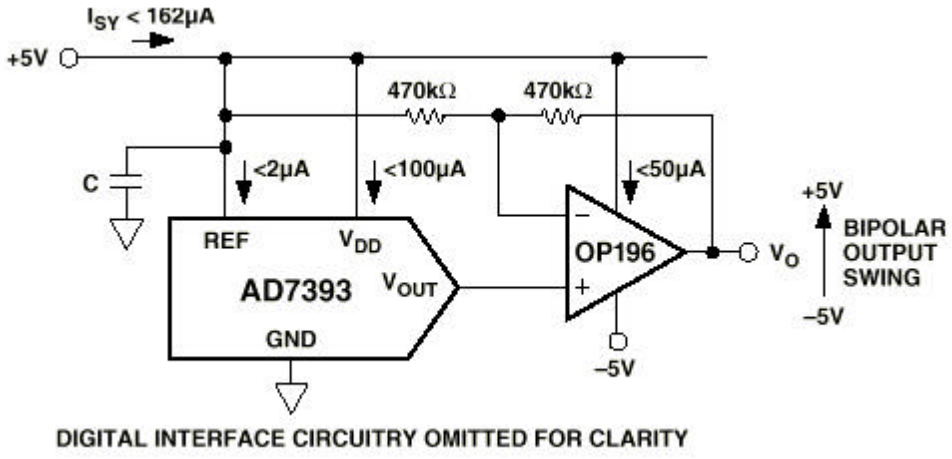

Figure 13: Output to oscilloscope

With this configuration, the input data will be converted to a value of

$$\frac{(D-2048)}{2048}$$, where D is between 0 and 4096.

After conversion, the signal has to pass through a reconstruction filter to be restored to the original sampled signal. The reconstruction filter is identical to the components used for anti-aliasing filter. However, the cut off frequency is dependent on the individual sampling rate of the particular channel being displayed. The filter selected for this task is a 4^{th} order Butterworth filter (LMF40 from National Semiconductor). The clock input to the LMF40 circuit determines the cut-off frequency of this filter. A variable frequency divider will be able to produce the clock signal that will produce the desired filtering effect. After the proper filtering, the signal is output to a connector for easy connection to an oscilloscope. Figure 14 is a block diagram representing the reconstruction process.

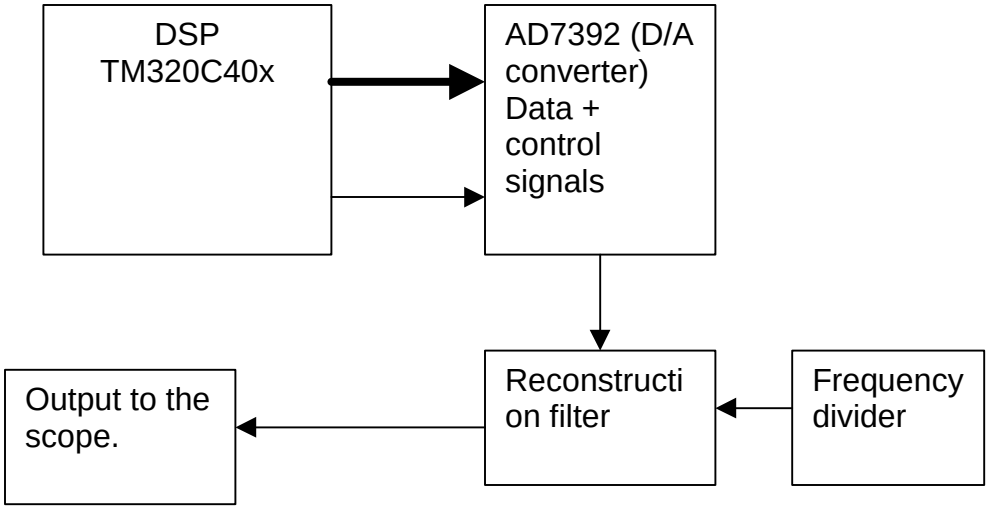

Figure 14: Reconstruction process

Upload Mode

In Upload Mode, the system will transfer the information on the logger to the personal computer running Logger Manager. On the logger, the information is accessed by the DSP and transferred to the PC via the Logger/Computer Interface. On the PC, Logger Manager will be responsible for storing the data on to some storage device. Figure 15 shows the major blocks in Upload Mode. (The managing software on both sides has been made transparent.)

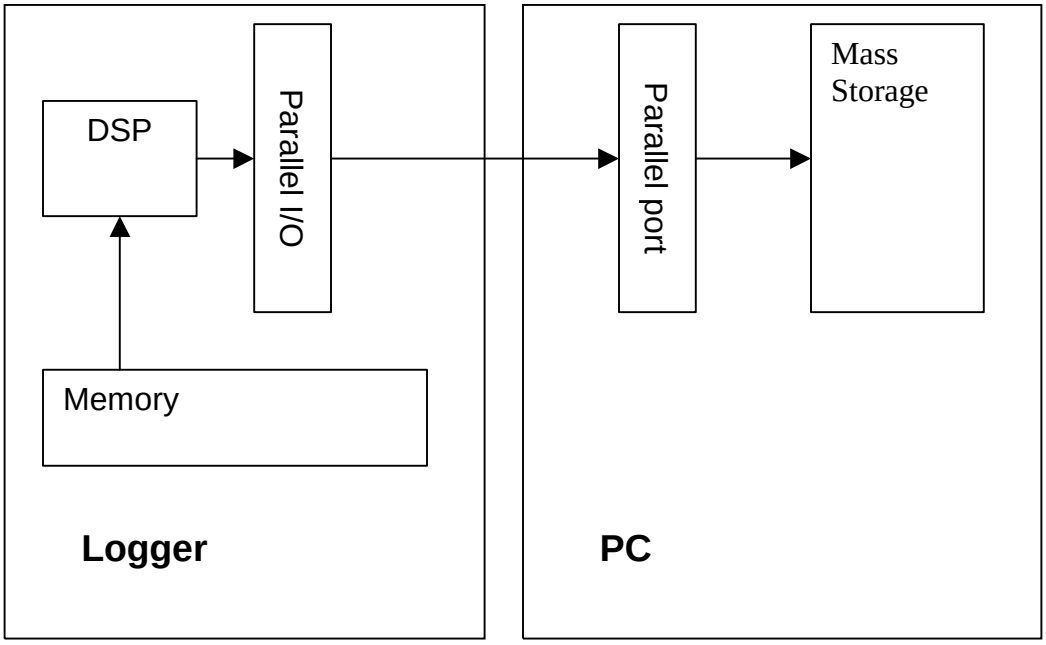

Figure 15 Basic blocks in Upload Mode

Computer Software

Our current plan is to store the data into a Microsoft Access® database via Microsoft's Data Accessing Object (DAO). Data will be grouped by channels and stored along with the sampling frequency.

Power Requirement

The power will be supplied by a ±5V, 100mA max power supply at the current stage. A lithium-ion rechargeable battery will be used to power the system in the second phase of the project.

Physical Specification

The signal data logger will be enclosed in a plastic box to prevent damage to the internal circuitry. There will be 16 connectors to connect the electrodes, one parallel port, and a scope output. The design for the enclosure is not available at the current stage of the project.

Test Case

We will test the system against the following requirements for the first phase of the project. In the first phase, the LCD display is not included in the design. The status indicator will be implemented with light emitting diodes. Therefore, LCD will not be tested in this phase.

- Configuration and Sampling:
  Invoke Logger Manager and configure the logger to different setups.
  Observe the output from the oscilloscope to verify the following components: sampling, anti-aliasing filter, analog-digital conversion, digital-analog conversion, reconstruction filter, filtering schemes, and programmable gain.
- Power Indicator:
  Turn on the power and observe the power indicator LED.
  When the battery is low, observe if the power indicator blinks.
- Memory Full Indicator:
  The LED indicators will turn on and blink accordingly.
- Upload:
  Configure the logger to be at unity gain at a preset frequency without a filtering scheme. Sample a waveform from the function generator and upload the result to the PC.
- Switches:
  The logger should react to the Pause/Resume switch in Logging Mode. If the logger is recording signals when Pause command is given to the logger, the logger should stop recording. If the logger is paused when the resume command is issued, it should resume its logging process.
  When the reset button is pressed, the logger should abandon previous logged data and end the current process. Moreover, it should restart the session with the same configuration.
  When the On/Off switch should turn the logger on and off.

Reference

[1] Analog Devices, *Data Sheet for AD7392*, 1994.

[2] Boaz Porat *A Course in Digital Signal Processing*, John Wiley & Sons, Inc, Canada: 1997.

[3] Joseph D. Bronzino *The Biomedical Engineering Handbook*, IEEE Press: 1995.

Appendix

A1. Part List

Item	Manufacturer	Part Number	Quantity
Microcontroller	Motorola	MC68HC11K4	1
DSP chip	Texas Instruments	TM320C40GW60	1
Switches	Customized	Push switches	3
LED, Red		Red LED	1
LED, Blue		Blue LED	1
LED, Green		Green LED	1
LED, Yellow		Yellow LED	1
Memory, 64MB		DRAM-SIMM module	6
Memory, 16MB		DRAM SIMM module	2
Digitally Controlled Potentiometer	Xicor	X9315	16
Operational Amplifier	National Semiconductor	TL084	25
Resistor, 0.25W, 1%		Numerous values	22
Filter	National Semiconductor	LMF40, 4^{th} order butterworth filter	3
A/D converter	National Semiconductor	ADC12048CIV	2
D/A converter	Analog Devices	AD7392	1
Diode	National Semiconductor	Numerous types	32

A2. Schematic of the Signal Conditioning Stage