

Digital Audio Evolution

Simon Fraser University
Burnaby, BC
V5A 1S6
Email: ensc-340@sfu.ca

November 9th, 1999

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, BC
V5A 1S6

Re: ENSC 340 Design Specification: The iDAC (Digital Audio Cassette)

Dear Dr. Rawicz:

The attached document, *ENSC 340 Design Specification: The iDAC (Digital Audio Cassette)*, details the design specifications for our project for ENSC 340 (Engineering Science Project Course).

The purpose of the design specification is to detail how we intend to solve the problem we described in the functional specification document. Within the attached document parts selections are detailed with relevant evaluation materials.

Digital Audio Evolution consists of four motivated, innovative, and talented third-year engineering students—Paul Gurney, President and CEO; Bill England, VP Finance; Scott Wakelin, VP Engineering; and Michael Hutchison, VP Production. The company can be contacted by phone at 294-0095 or by e-mail at ensc-340@sfu.ca should you have any questions.

Sincerely,

Paul Gurney, President and CEO
Digital Audio Evolution

Enclosure: *ENSC 340 Design Specification: The iDAC (Digital Audio Cassette)*

Digital Audio Evolution

ENSC 340 Design Specification: The iDAC (Digital Audio Cassette).

Submitted By	Digital Audio Evolution Paul Gurney, Bill England, Scott Wakelin, Michael Hutchison
Contact	Paul Gurney School of Engineering Science Simon Fraser University ptgurney@sfu.ca
Submitted To	Andrew Rawicz School of Engineering Science Simon Fraser University Steve Whitmore School of Engineering Science Simon Fraser University
Date	November 8 th , 1999

Executive Summary

This document presents a high level design for the iDAC device. Included in the sections for each major system component are discussions relating the requirements to be met (as set forth in the requirements specification), and how the various design options compared to those goals.

The iDAC system will consist of the following major components:

1. Data Storage Unit
2. Host Computer
3. System Controller
4. MPEG Decoder
5. Digital to Analog Converter
6. Amplifier Network
7. Transducer
8. Software (running on the Host Computer)

Parts that have been selected after careful consideration are as follows:

Data Storage Unit	SanDisk SDMB16
System Controller	PIC 16F84
MPEG Decoder	MAS3507D
Digital to Analog Converter	Crystal 4340
Amplifier Network	Standard Op-amp Circuitry
Transducer	Standard Stereo Tape Transducer

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Revision History

Revision	Date	Description	Name
0.1	November.3.1999	Initial Version.	Michael Hutchison
0.2	November.7.1999	Added executive summary, amplifier and filtering network design sections. Minor revisions.	Scott Wakelin
0.3	November.9.1999	Integration of teams work and cleanup.	Michael Hutchison
1.0	November.9.1999	Final overview	Paul Gurney

Acronyms

AAC	Advanced Audio Coding
ADPCM	Advanced Differential Pulse Code Modulation
DAC	Digital to Analogue Converter
MP3	MPEG Layer 3
MPEG	Moving Pictures Experts Group
MTBF	Mean Time Between Failures
PC	Personal Computer
PCA	Printed Circuit Assembly
CPLD	Complex Programmable Gate Array
USB	Universal Serial Bus
Kbps	Kilobits per second (data transfer rate)
Mbps	Megabits per second (data transfer rate)
RAM	Random Access Memory

1. Introduction

The iDAC is a digital device capable of storing MPEG2 data for playback. The device resides in a standard tape cassette form factor and can store approximately 30 minutes of compressed music. Users treat the iDAC like a standard tape cassette, inserting it into a standard tape player for playback. The unit will use Flash RAM to store the data, an integrated MPEG2 decoder and a microprocessor to interface between the RAM and decoder device, as well as to the host computer.

1.1. Scope

This document describes the design specifications for the iDAC device.

This document will drive the implementation of the iDAC device.

1.2. Intended Audience

Design Engineers will use this document to implement the iDAC device.

The Project Manager will use this document to assign resources to design implementation, and to forecast time schedules.

1.3. Reference Specification

1.3.1. Applicable Documents

- [1] *Engineering Science Communications Handbook 6th Edition*, S. Stevenson, S. Whitmore, 1996.

1.3.2. Reference Documents

- [2] *ENSC340 Functional Specifications: The iDAC (Digital Audio Cassette)*, M. Hutchison, S. Wakelin, P. Gurney, W.England, October 18th, 1999.
- [3] *ENSC340 Proposal: The iDAC (Digital Audio Cassette)*, M. Hutchison, S. Wakelin, P. Gurney, W. England, September 20th, 1999.
- [4] *ISO/IEC 13818-1: Information Technology – Generic Coding of Moving Pictures and Associated Audio – Part 1: Systems*, International Standards Organisation, N0801, November 13th, 1994.
- [5] *Multimediacard Product Manual*, SanDisk Corporation, 80-13-00089, 4/99.
- [6] *LTC1348 Data Sheet*, Linear Technology Inc., 01/97.

2. System Overview

The iDAC receives input from the host computer and the tape speed sensors. Output is created through a transducer. Figure 1 shows a high-level block diagram of the unit, illustrating the data flow within the device.

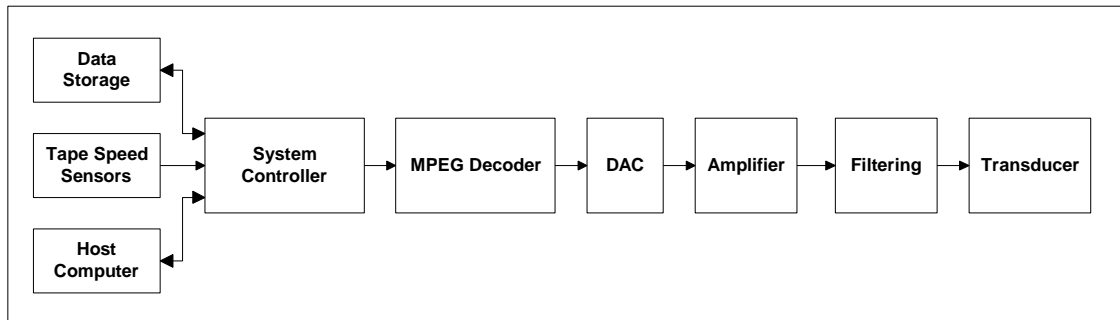


Figure 1 Functional System Block Diagram

MPEG-2 Layer 3 data is received from the host computer and stored in 16 megabytes of onboard data storage through the system controller interface.

The system controller monitors the speed of the tape reels, and initiates data transfer from the data storage to the MPEG Decoder when it senses a valid playback mode.

Output from the MPEG Decoder, in the form of a serial bit stream, is fed to the digital to analogue converter (DAC). The analogue output of the DAC is fed to an amplifier for amplification for the output transducer. Filtering is required for the amplifier output to remove artifacts remaining from the digital domain.

The filtering stage output is then fed to the transducer for output to the tape read head in the tape player.

3. Host Computer Interface Implementation

Detailed in the *Functional Specifications* [2] are the requirements affecting the host computer interface. They are included here in Table 1 for your reference.

Table 1 Functional Requirements Affecting Host Computer Interface

Requirement	Detail
R1.12	The unit shall operate from internal power for eight hours before recharging is required.
R1.15	The host interface software shall run on any standard Windows 95 or 98 computers.
R1.16	The host interface software shall run on any standard Windows NT computer.
R1.22	The self-test shall identify sub-systems at fault and relay that information to the user.
R1.36	The connection interface shall be capable of transferring data at 1Mbps.
R1.37	The connection interface shall use no more than three wires.
R1.38	The connection interface shall consist of a single cable.
R1.39	The connection interface shall be a standard interface available on all consumer computers made in the past 2 years.

The following communications interfaces have been investigated

- Universal Serial Bus (USB), using Philips PDIUSB11
- RS-232, using Linear Technologies LTC1348

Table 2 details the characteristics of each interface.

Table 2 Host Computer Interface Characteristics

Characteristic	USB Interface	RS-232 Interface
Transfer Speed	2.5Mbps	250Kbps
Package Area	112mm ²	77 mm ²
Power Consumption	33mW	1.98mW
Component Count	7	5
Package Pins	16	28
Routed Pins	15	12
Interface Pins to Host Computer	4	3
Interface Pins to system controller	5	2
System controller Interface Type	I ² C (Complex)	Serial TTL (Simple)

Below Table 3 includes a detailed breakdown of how each interface compares with the requirements it must meet. The possible ratings are ‘G’ for good, ‘A’ for acceptable, and ‘U’ for unacceptable.

Table 3 Host Interfaces as Compared to Requirements

Requirement	USB Interface	RS-232 Interface	Comment
R1.12	A	G	The RS-232 Interface uses much less power than the USB interface.
R1.15	G	G	Both interfaces will operate on Windows 95 and 98 machines.
R1.16	U	G	USB will not operate under Windows NT, while RS-232 will.
R1.22	A	G	USB requires a large amount of micro-controller interaction to function, making it possibly difficult to inform the user of malfunctions; while the RS-232 interface is transparent to the micro-controller.
R1.36	G	U	USB operates at 2.5Mbps, while current RS-232 interfaces operate at 250Kbps.
R1.37	U	G	The USB interface requires 4 pins, while the RS-232 interface requires only 3.
R1.38	G	G	Both interfaces require only a single cable.
R1.39	U	G	USB has not been available on all consumer computers made in the past 2 years, while RS-232 has been.

It is clear from the analysis that the RS-232 interface best suits the requirements set forth. R1.36 has been modified so that it requires the interface to operate at speeds not in excess of 250Kbps.

The RS-232 interface requires less board space, has lower power consumption, has less routed pins, requires less external components and is a simpler interface to implement. With the modification of R1.36 RS-232 meets all functional requirements, and will be implemented as the interface of choice.

The schematic detail of the LTC1348 is shown below in Figure 2.

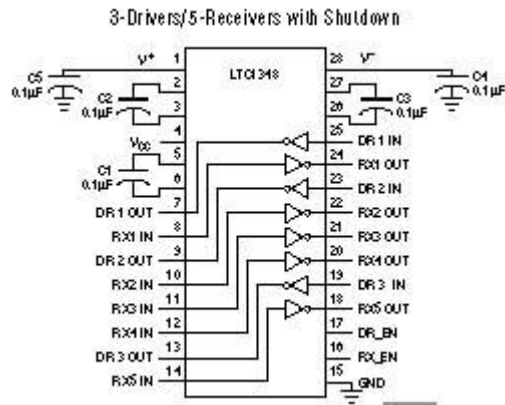


Figure 2 LTC1348 Schematic Detail

4. Tape Speed Sensor Implementation

Detailed in the *Functional Specifications* [2], are the requirements affecting the tape speed sensor implementation. They are included here in Table 4 for your reference.

Table 4 Functional Requirements Affecting Tape Speed Sensor Implementation

Requirement	Detail
R1.3	The unit shall contain two standard tape reel gears.
R1.6	The unit shall detect the speed of the tape reels and select the appropriate mode of operation based on that speed...
R1.23	The unit shall have a playback mode.
R1.24	The unit shall have a stop mode.
R1.26	The unit shall have a fast-forward mode.
R1.27	The unit shall have a rewind mode.
R1.28	The unit shall have a pause mode.

When the user presses the “play” button, the playback head and tape guide mechanism are pushed into the bottom of the tape. This action can activate a switch that will power the device. That is, no power will be consumed unless the iDAC is being played.

An optical sensor can be used to detect whether the tape gears are moving forward or backwards and at what speed.

In the initial proof-of-concept device, this functionality will not be implemented. It will instead be simulated by using dip-switches that will be directly tied to the system controller input pins.

5. Data Storage Implementation

Detailed in the *Functional Specifications* [2], are the requirements affecting the Data Storage implementation. They are included here in Table 5 for your reference.

Table 5 Functional Requirements affecting Data Storage Implementation

Requirement	Detail
R1.4	The unit shall perform self-tests as requested by the host computer including: full read/write test of memory...
R1.12	The unit shall operate from internal power for eight hours before recharging is required.
R1.18	The unit shall retain its data for 30 years.
R1.19	The unit shall allow up to 50,000 erase/write cycles. This allows the data to be changed 4 times a day for 30 years.
R1.20	The unit shall meet a MTBF of 5,000 hours.
R1.40	The unit shall support all standard sample rates from 1kHz to 44.1kHz.

The following Data Storage implementations have been investigated

- SanDisk SDMB16 Multimedia Card
- Intel 28F128J3A Flash RAM

Table 6 details the characteristics of each data storage device

Table 6 Data Storage Characteristics

Characteristic	SanDisk	Flash RAM
Storage Capacity	16 Megabytes	16 Megabytes
Access Time	50nS	25nS
Power Consumption (Read)	108.9mW	132.0mW
Power Consumption (Write)	115.5mW	115.5mW
Power Consumption (Idle)	.165mW	.164mW
Erase/Write Cycles	300,000 cycles	12,800,000 cycles
MTBF	>1,000,000 hours	Not available
Package Area	768mm ²	130mm ²
Package Pins	7	64
Routed Pins	7	64
Interface Pins to system controller	4	51
System controller interface type	SPI Bus	Address and Data Bus

Below Table 7 includes a detailed breakdown of how each implementation compares with the requirements it must meet. The possible ratings are ‘G’ for good, ‘A’ for acceptable, and ‘U’ for unacceptable.

Table 7 Data Storage Methods as Compared to Functional Requirements

Requirement	SanDisk	Flash RAM	Comment
R1.4	A	A	Units do not have BIST, but will allow full read/write testing.
R1.12	A	A	Both units have relatively low power requirements.
R1.18	Not rated.	Not rated.	Neither unit provides data integrity information. An inquiry is in progress.
R1.19	G	G	Both units support >50,000 cycles.
R1.20	G	Not rated.	SanDisk MTBF exceeds 5,000 hours, Flash RAM is not published. An inquiry is in progress.
R1.40	G	G	Both units have access times that will satisfy 44.1kHz data throughput.

The investigation of these two technologies lead to the conclusion that either unit would perform the required functions. The SanDisk unit requires significant PCB area as compared to the Flash RAM device (768mm² vs. 130mm²); however the Flash RAM device requires the routing of 64 pins vs. 7 pins for the SanDisk device.

It is estimated that the additional 57 traces for the Intel Flash device would require the use of a larger system controller than would be required with the SanDisk device. The additional traces are expected to take up approximately 1040 additional mm² of board space using the following calculation (based on a standard low density PCB layout).

$$\text{Trace Area Requirement} = 2 \text{ mm/trace} * 10 \text{ mm trace length} * 52 \text{ traces} = 1040 \text{ mm}^2$$

The total required area for the Flash RAM is then 1170mm² which is in excess of the 768mm² required for the SanDisk. This factor combined with the fact that the interface for the SanDisk device is far less complicated than that required for the Flash RAM clearly indicates that selection of the SanDisk device is favorable.

The design will use the SanDisk SMB16 multimedia card. The schematic detail of the SMB16 is shown below in Table 8 and Figure 3.

Table 8 SanDisk Pin Assignments (SPI Mode)

Pin #	Name	Type*	SPI Description
1	CS	I	Chip Select (Active low)
2	DataIn	I	Host to Card Commands and Data
3	VSS1	S	Supply Voltage Ground
4	VDD	S	Supply Voltage
5	CLK	I	Clock
6	VSS2	S	Supply Voltage Ground
7	DataOut	O	Card to Host Data and Status

*Note: S=power supply; I=input; O=output.

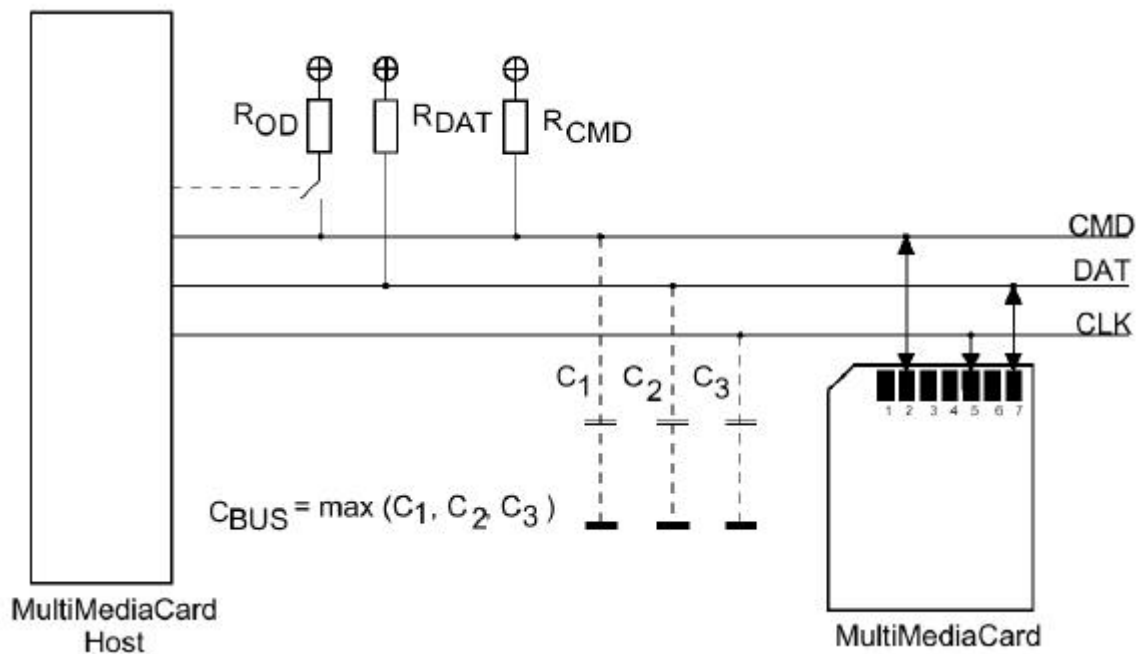


Figure 3 SanDisk Schematic Detail

6. System Controller Implementation

The major factors affecting the implementation of the system controller are the selection of the data storage device and the selection of the host PC communications interface. In addition, board layout area and power consumption issues are very important.

The following system controller implementations have been investigated

- Motorola HC11 Micro-Processor
- PIC 16F84 Micro-Processor
- Philips 80C32 Micro-processor (or equivalent)
- Altera 7128 Complex Programmable Logic Device (CDPL)

Early in the investigation, it became clear that the Motorola HC11 microprocessor would be an inadequate selection due to its 2MHz clock operation, which is not fast enough to facilitate the SanDisk memory interface.

Table 9 details the characteristics of the three remaining options.

Table 9 System-controller implementation characteristics

Characteristic	PIC	80C32	7128 (84 pin)
Maximum I/O Speed	20MHz	33MHz	147.1MHz (1.75W)
Power Consumption	55mW (20MHz)	101.64mW (33 MHz)	500mW (30MHz)
Package Area	55.05mm ²	166.41mm ²	345mm ²
Package Pins	18	44	84
Routed Pins	18	44	24 + <#I/O>*
User I/O Pins	13	32	68
Integrated Interfaces	None.	RS-232	None.
Development Support	EEPROM	EPROM	EEPROM
Programmability	Out of circuit	In circuit, RS-232	In circuit, JTAG

*<#I/O> refers to the number of routed I/O pins.

It is clear from the comparison above that the PIC processor uses the least amount of power and occupies the smallest amount of board space, while still offering enough user I/O pins for development.

The drawback to the PIC device is the out of circuit programmability of it; however use of a socketed 18 pin DIP for development will make this process reasonably painless.

Schematic detail of the PIC microprocessor is shown below in Figure 4.

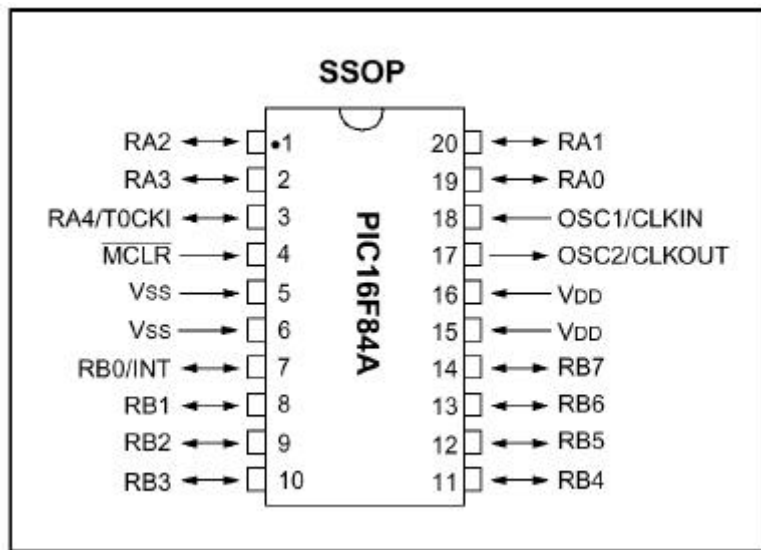


Figure 4 PIC Schematic Detail

7. MPEG Decoder Implementation

Detailed in the *Functional Specifications* [2], are the requirements affecting the MPEG decoder implementation. They are included here in Table 5 for your reference. Additional requirements are a low power device in a small package, and lead time to obtain the required parts.

Table 10 Functional Requirements affecting Data Storage Implementation

Requirement	Detail
R1.40	The unit shall support all standard sample rates from 11kHz to 44.1kHz.
R1.41	The unit shall be able to decode ADPCM data.
R1.42	The unit shall be able to decode MPEG1 Layer 1, and Layer 2 data.
R1.43	The unit shall be able to decode MPEG2 Layer 1, and Layer 2 data.

The following MPEG decoder implementations have been investigated

- Micronas Intermetall 3507D
- ST Microelectronics STA013

Table 6 details the characteristics of each MPEG decoder. Both devices support all required decoding modes and sample rates.

Table 11 Data Storage Characteristics

Characteristic	Micronas	ST Micro
Power Consumption	165mW	85mW
Package Area	131mm ²	131mm ²
Package Pins	44	44
Routed Pins	44	28

The power consumption and routed pin requirements of the ST Micro device are much lower than the Micronas device.

After further investigation it was realized that obtaining the ST Micro device was a nearly impossible task whilst the Micronas device is readily available.

Due to the relative availability of development information and support for the Micronas device it has been decided to use the 3507D. Schematic detail information is shown below in Figure 5.

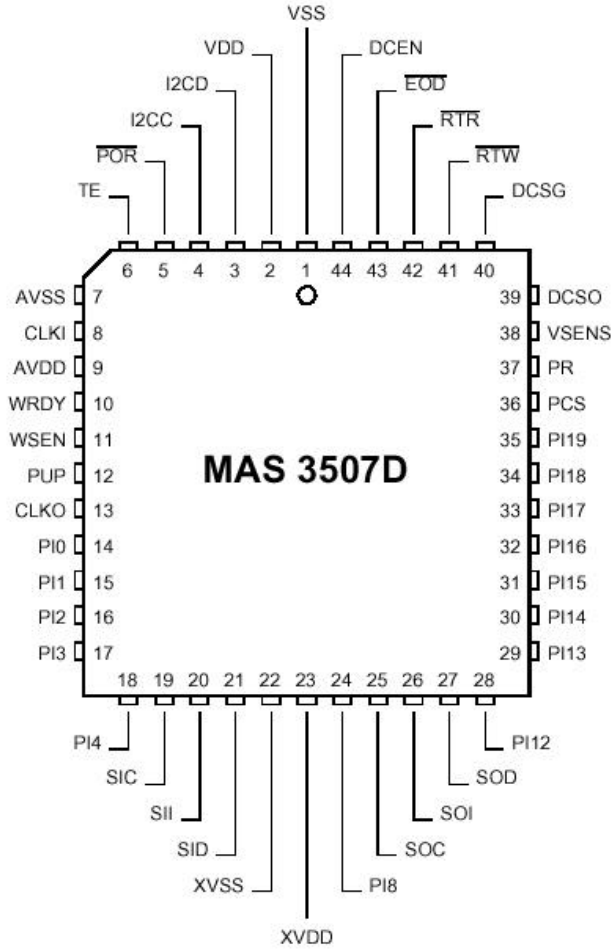


Figure 5 Micronas 3507D Schematic Detail

8. Digital to Analogue Converter Implementation

Detailed in the *Functional Specifications* [2] are the requirements affecting the Digital to Analogue Converter (DAC) Implementation. They are included in Table 12 for your reference.

Table 12 Functional Requirements Affecting DAC Implementation

Requirement	Detail
R1.1	The unit shall have a bandwidth of at least 12kHz.
R1.2	The unit shall receive a ranking of at least 3.5 on the standardized 5-point perceptual quality scale. (A tape cassette has a ranking of 2).
R1.40	The unit shall support all standard sample rates from 11kHz to 44.1kHz.

The following DAC devices have been investigated

- Crystal 4340
- Micronas Intermetall 3550A

Table 13 details the characteristics of each DAC.

Table 13 DAC Characteristics

Characteristic	Crystal	Micronas
Range for Sample Rates	2kHz to 100kHz	8kHz to 50kHz
Power Consumption	30mW	32mW
Component Count	20	20
Package Area	62mm ²	72mm ²
Package Height	1.75mm	N/A
Package Pins	16	16
Routed Pins	16	16
Decoder Interface	I ² C and I ² S	I ² C and I ² S
Output Type	Left, Right, and Ground	Left, and Right

Table 14 includes a detailed breakdown of how each implementation compares with the requirements it must meet. The possible ratings are 'G' for good, 'A' for acceptable, and 'U' for unacceptable.

Table 14 DACs and Compared to Functional Requirements

Requirement	Crystal	Micronas
R1.1	G	G
R1.2	A	A
R1.40	G	G

The investigations of these two technologies lead to the conclusion that either unit would perform the required functions. However, the Crystal DAC has the following advantages: (1) slightly smaller package size, (2) lower power consumption, and (3) Cirrus Logic is a world leader in high-quality Audio DACs. Consequently, the Crystal CS4340 DAC will be used.

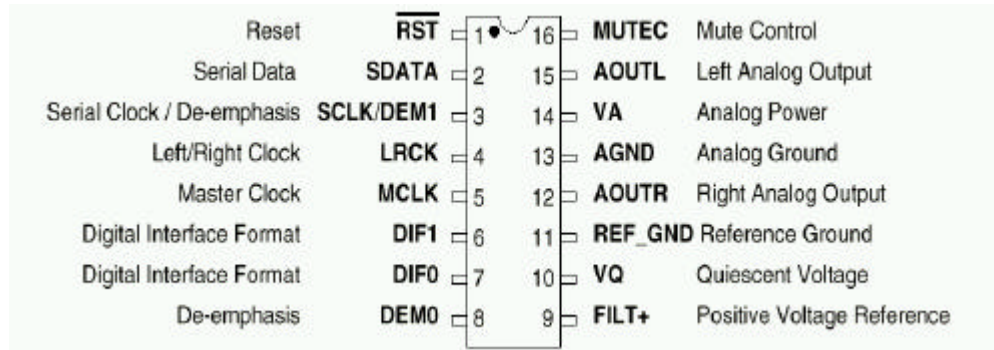


Figure 6 CS4340 Pin Description

9. Amplifier Implementation

A review of the data sheet for the Crystal CS4230 DAC reveals that it provides a full scale output voltage equivalent to $0.7 V_A$ (typical), where V_A is the analog supply voltage. In this design, V_A is equal to 3.3V, yielding a typical full scale output voltage of $2.31 V_{p-p}$. This value is more than sufficient to drive the output transducer.

However, it is still desirable to provide a buffer between the high impedance source of the DAC, and the low impedance load presented by the transducer. An ideal amplifier for this situation is the voltage follower, which provides a gain of 1.

The following figure details the design of the amplifier stage.

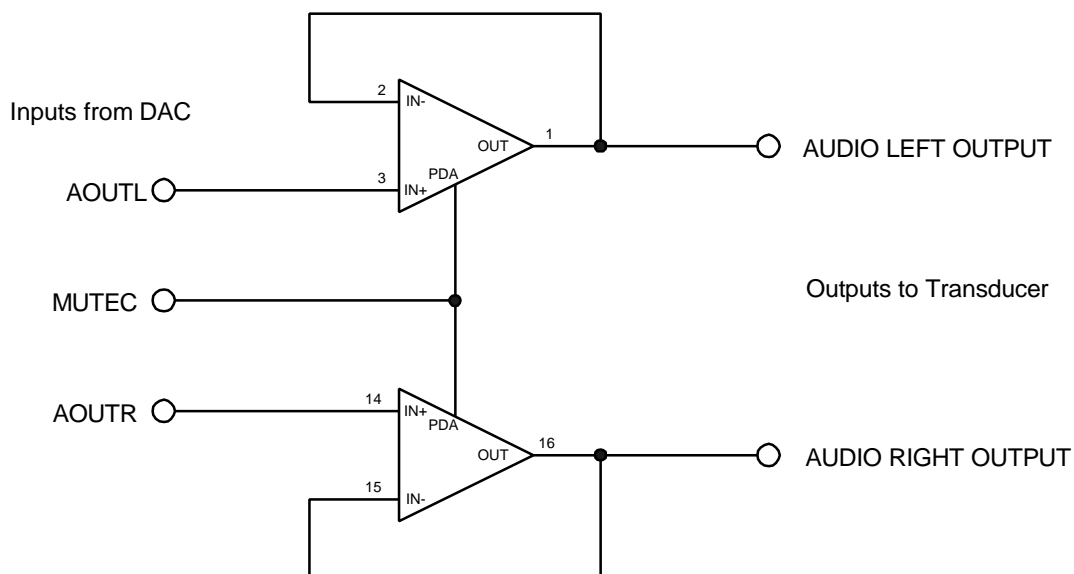


Figure 7 Amplifier Network with Muting.

The above circuit includes a mechanism for disabling the amplifiers. The amplifiers are disabled when the DAC outputs a logic high on its MUTE output.

A suitable op-amp for this arrangement is the National Semiconductor LMC6684. The LMC6684 contains 4 op-amps in a surface mount package, and is capable of operating from a single 3.3V supply. In addition, the LMC6684 contains 2 power down inputs (PDA and PDB) which each control two amplifiers. This allows audio muting to occur under the control of the DAC.

10. Filtering Implementation

At this stage, only passive filtering networks are required for this design. This is because the CS4340 DAC features integrated analog filters, providing a pass band from 10 Hz – 20 kHz. Each audio output circuit from the DAC will feature a high pass filter, followed by a low pass filter as shown in the diagram below. In this figure,

$$C = \frac{R_{LOAD} + 560}{4\pi R_{Load} F_S 560}$$

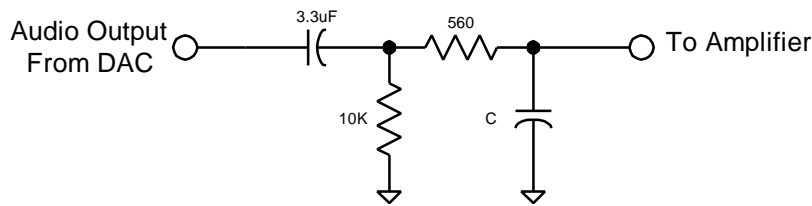


Figure 8 DAC Output Filtering Network.

The above figure shows the configuration for one audio output of the DAC. The same circuit will be repeated for the other audio output as required.

10. Transducer Implementation

A standard stereo magnetic tape record head will be used to convert the filtered audio signal into the required magnetic flux. The head has two distinct areas as shown in Figure 9: the topmost area drives the left stereo signal, and the lower area drives the rightmost stereo signal. These areas must be coupled closely to the corresponding areas on the playback head in the car stereo or walkman.

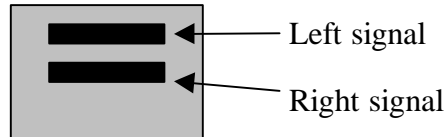


Figure 9: Record Head signal areas

The magnetic flux signal strength drops off as the inverse square of the distance, so it is important to closely couple the record head with the play back head. Figure 10 shows mechanisms which will help ensure correct coupling. Plastic tape bars can be attached to the record head. These bars will interact with the tape guide mechanism on the player to ensure that the record head is placed correctly. The record head is attached to the cassette with a spring load which allows it to move forward and backward. This will allow the play head to be placed in direct contact with the record head.

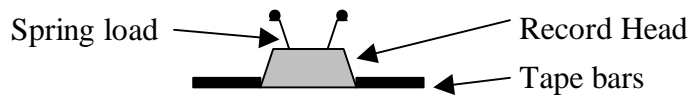


Figure 10: Mechanism to couple record head

The standard stereo head used in tape recorders has a 4-contact interface, described in Table 15

Table 15 Tape Head Contact Interface Pinout

Contact	Description
1	Ground
2	NC
3	Left channel
4	Right channel

The two output channels and the common ground from the filter will be connected to the appropriate contact on the record head.

Table 16 shows the requirements relating to the transducer.

Table 16 Functional Requirements affecting transducer response

Requirement	Detail
R1.13	The unit shall have a bandwidth of at least 12kHz

Table 17 shows some parameters relating to a standard stereo record head (Apollo Electronics - AP4211T):

Table 17 Stereo Record Head Characteristics

Parameter	Value
Width	10.4 mm
Height	7 mm
Length	7.7 mm
Frequency response (3dB)	10KHz
Impedance	220 ohms

The bandwidth is slightly less than that given in the functional specification. However, it may be possible to work around this problem by increasing the treble response of the MPEG decoder.

The width, height and length will all fit in a standard cassette form factor.

The impedance of 220 ohms implies that the maximum current drawn will be $3/220$ which is about 15mA.

11. User Interface Design

The user interface running on the local computer will allow users to select files to transfer to the iDAC through a graphical interface similar to that shown below in **Error!**
Reference source not found..

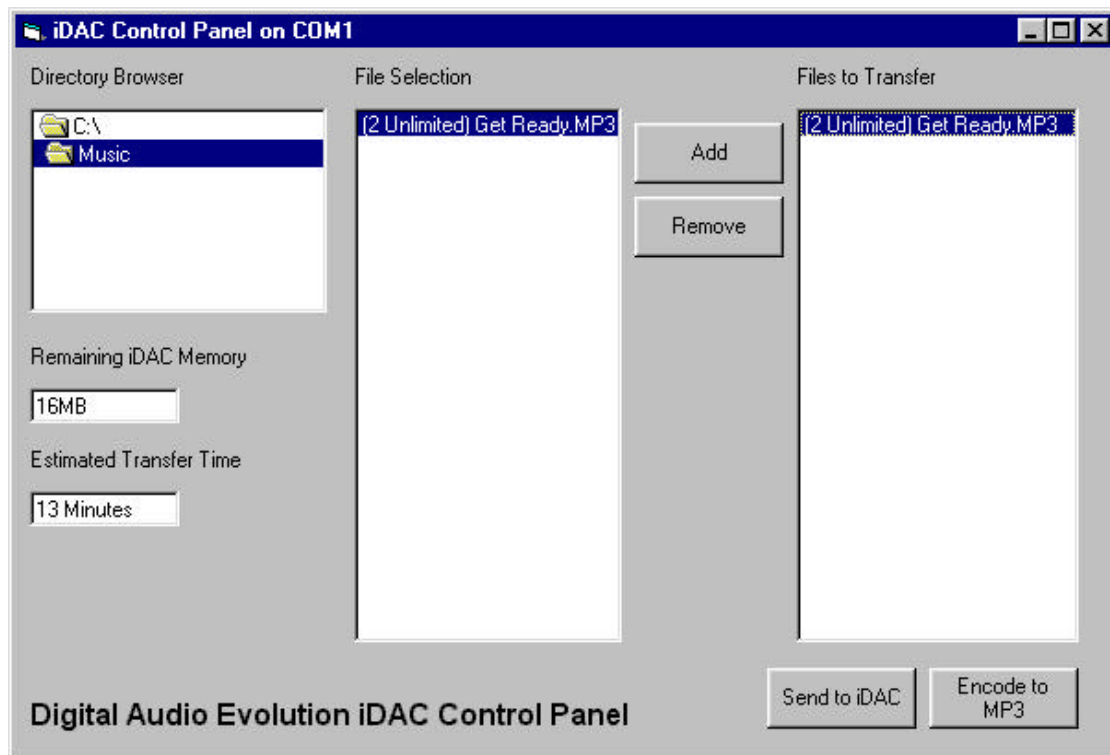


Figure 11: iDAC Control Panel

The user interface allows the user to easily navigate through their hard drive using the directory browser and then select files to transfer in the file selection menu. The user clicks the "Add" button to add selected files to the transfer list, or "Remove" to remove files from the transfer list.

The user then clicks either the "Send to iDAC" button to send files to the iDAC, or "Encode to MP3" to encode the listed files into MP3 format.

Convenient dialogue boxes are located in the left portion to indicate remaining memory and estimated transfer times.

12. Test Plan

As indicated in the *Functional Specifications* [2] (1.4 Objectives, p. 1) the iDAC development has two phases: (1) the proof of concept design, and (2) future development. Accordingly separate test plans exist for both the proof of concept device and the future development, the test plan for the proof of concept device is included below.

The *Functional Specifications* [2] outline the verifiable requirements of the iDAC. The test plan contains these verifiable requirements and the methods by which the *Validation and Test Team* shall ascertain whether the requirements are met.

12.1. Proof of Concept Test Cases

12.1.1. The unit shall connect to the host computer using a 100 mil spaced, single row, three-pin header.

By inspection the Validation and Test Team shall verify that the iDAC and the host computer connect via the said method.

12.1.2. The host interface program shall be able to run concurrently with other host computer tasks.

In testing the host interface program the Validation and Testing Team shall:

- Prior to running the host interface program open any number of standard Windows 95/98 applications, and thereafter launch the host interface program.
- While running the host interface program open any number of standard Windows 95/98 applications, and thereafter run the host interface program.
- Simultaneously download from the Internet while running the host interface program.
- Compile software while running the host interface program.
- Any combination of the above.

12.1.3. The unit shall recover gracefully from unexpected events, such as being ejected while playing.

The Validation and Test Team shall test the ability of the unit to recover from unexpected events while interfacing with the host computer by:

- Cycling the power on the host computer before and during a download to the unit.
- Disconnecting wire interface between the unit and the host computer during a download.

The Validation and Test Team shall test the ability of the unit to recover from unexpected events while on modes other than downloading by:

- Initiating a temporary loss of power.
- Creating an inconsistent power supply.

12.1.4. The unit shall continue to operate correctly in the presence of vibrations of up to 9Gs.

The proof of concept unit shall not be subjected to vibration testing as it is inconsequential in proving the validity of the concept, and could potentially damage the prototype. Therefore, vibration testing will be placed in the test plans of future unit revisions.

12.1.5. The unit shall not be harmed by shocks of up to 100Gs

The proof of concept unit shall not be subjected to shock testing as it is inconsequential proving the validity of the concept, and could potentially damage the prototype. Therefore, shock testing will be placed in the test plans of future unit revisions.

12.1.6. The unit shall have a bandwidth of at least 12kHz.

The Validation and Test team shall download a sample file to the unit that contains a range of frequencies with a bandwidth of at least 12kHz. The team shall then play this file back and verify the units bandwidth with a Spectrum Analyzer.

12.1.7. The unit shall receive a ranking of at least 3.5 on the standardised 5-point perceptual quality scale.

The Validation and Test Team shall endeavor to carry out the perceptual quality scale test (5-point) on the unit as specified by industry standards.

12.1.8. The host interface software shall run on any standard Windows 95 or 98 computers.

The Validation and Testing Team shall operate the host interface software on a variety of host computer hardware configurations operating under Windows 95 and Windows 98. The following hardware configuration variables are to be considered:

- Different amounts of RAM: from 16MB to 128MB.
- Different processor speeds ranging from a Pentium-I 90MHz to a Pentium-III 550MHz.
- Windows 95/98 configurations (standard, full, custom, etc.)

12.1.9. The unit shall retain its data for 30 years and allow up to 50,000 erase/write cycles.

The SanDisk RAM specifications detail the RAM life expectancy as in excess of 30 years with more than 50,000 erase/write cycles. The Test and Validation team shall confirm this information with SanDisk.

12.1.10. The unit shall have a record mode (induced by the host computer user interface) and a playback mode.

The Validation and Test Team shall test the record mode of the unit by following instructions accompanying the host computer user interface indicating the recording method. After completing the instructions accompanying the host computer user interface the Team shall proceed to play the data recorded according to operating instructions accompanying the iDAC (as specified in the following Requirement).

Upon proper audio playback, the Team will have verified the ability of the unit to Record and Playback.

12.1.11. The unit shall have a stop mode.

The Validation and Test Team will audibly verify the stop mode by pressing the stop button while the unit is playing.

12.1.12. The host computer interface shall not allow transfer of data (songs) from the iDAC to a host computer.

The team will download a song to the iDAC and then proceed to play it out of the iDAC.

12.1.13. The unit shall support all standard sample rates from 11kHz to 44.1kHz.

The Validation and Test Team shall undertake to:

- Record files of all standard sample rates from 11kHz to 44.1kHz onto the unit.
- Play all standard sample rates from 11kHz to 44.1kHz from the unit.

12.1.14. The unit shall be able to decode ADPCM, MPEG1 Layer 1, and Layer 2, MPEG2 Layer 1, and Layer 2 data.

The Validation and Test Team shall undertake to:

- Transfer ADPCM, MPEG1 Layer 1, and Layer 2, MPEG2 Layer 1, and Layer 2 files onto the unit.
- Play ADPCM, MPEG1 Layer 1, and Layer 2, MPEG2 Layer 1, and Layer 2 files from the unit.

12.1.15. The unit shall be able to transfer ADPCM, MPEG1 Layer 1, and Layer 2, MPEG2 Layer 1, and Layer 2 data to the attached iDAC device.

The Validation and Test Team shall undertake to:

- Transfer ADPCM, MPEG1 Layer 1, and Layer 2, MPEG2 Layer 1, and Layer 2 files onto the unit.
- Play ADPCM, MPEG1 Layer 1, and Layer 2, MPEG2 Layer 1, and Layer 2 files from the unit.

13. Conclusion

This paper has detailed the design specifications for the iDAC project. The proof of concept device will be completed for December of 1999, using the implementation outlined in the above specifications, with the exception that form factor will not be attained.

The proof of concept device serves only to demonstrate that with the components chosen in this document, it is *possible* to create a digital audio cassette (the iDAC). The proof of concept device will not, however, fit in a cassette tape, or meet all power requirements as outlined. Future development of the device will bring the device within the physical parameters of the cassette, and will lower the power requirements as required in the *Functional Specifications*.

Notes: