RimaTech ltd.™

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October 16th, 2000

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, BC
V5A 1S6

Re: ENSC 340 Project Multi-Display Video Adaptor Design Specifications

Dear Dr. Rawicz,

The enclosed document, Multi-Display Video Adaptor (MVA) Design Specifications, outlines the system design specifications for our device. Our project is to design a Multi-Display Video Adapter that is compatible with any computer system, can be attached to any computer externally, and is able to display an image on four monitors, each displaying a quarter of the image. Due to high cost of the front-end prototyping and the limited available lab equipment, our prototype will generate images by itself and will support the Quad output display.

This document outlines the framework on which we will base our design. It describes in detail the desired behavior and an overview of the design of the MVA and its subsystems.

If you have any question or concerns about this report, feel free to contact me by phone at 421-6542 or by e-mail at skhalili@sfu.ca.

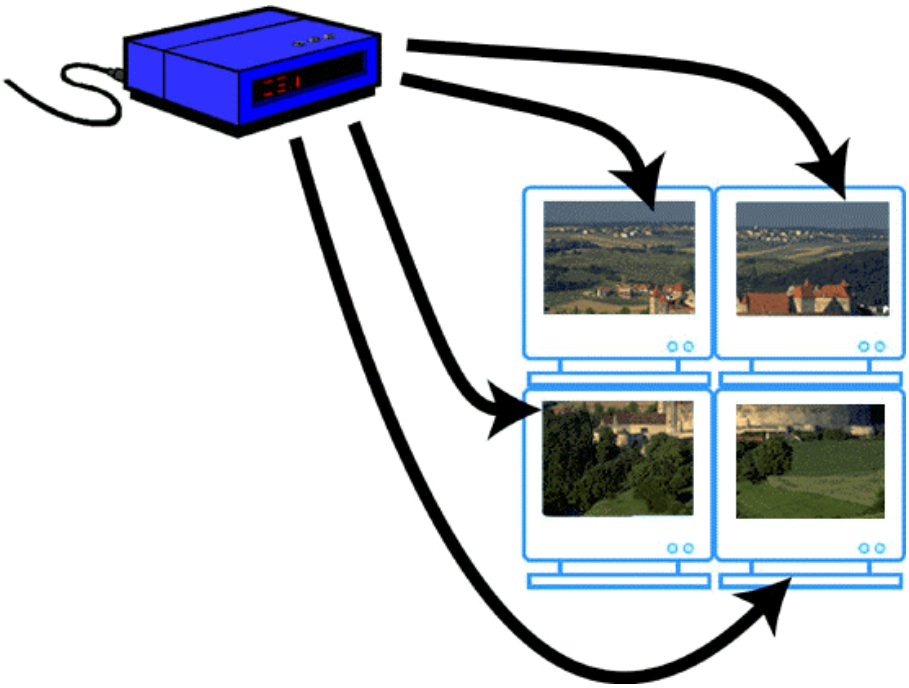
Sincerely,
Sahar Khalili, President and CEO

Rima Tech Inc.

Enclosure: ENSC 340 Multi-Display Video Adaptor Design Specifications

RimaTech ltd.

Design Specification for a Multi-display Video Adapter



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Submitted to:
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Steve Whitmore
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Date:
November 6, 2000

Abstract

This document is an overview of the system design of the Multi-display Video Adapter. The system prototype will have its own image generator, and will support animation. The output of the system is quad monitor display. The intelligent controlling circuit will support interpolation to produce high-resolution images, and provide animation in its further development. We will have sufficient testing and additional features to support the concept of External Multi display adaptors.

The built-in logic will be able to handle displays without causing image skewing, overlap, or distortion. Our output is a standard VGA/SVGA output, and can be easily converted to standard TV Signals for further development of our product.

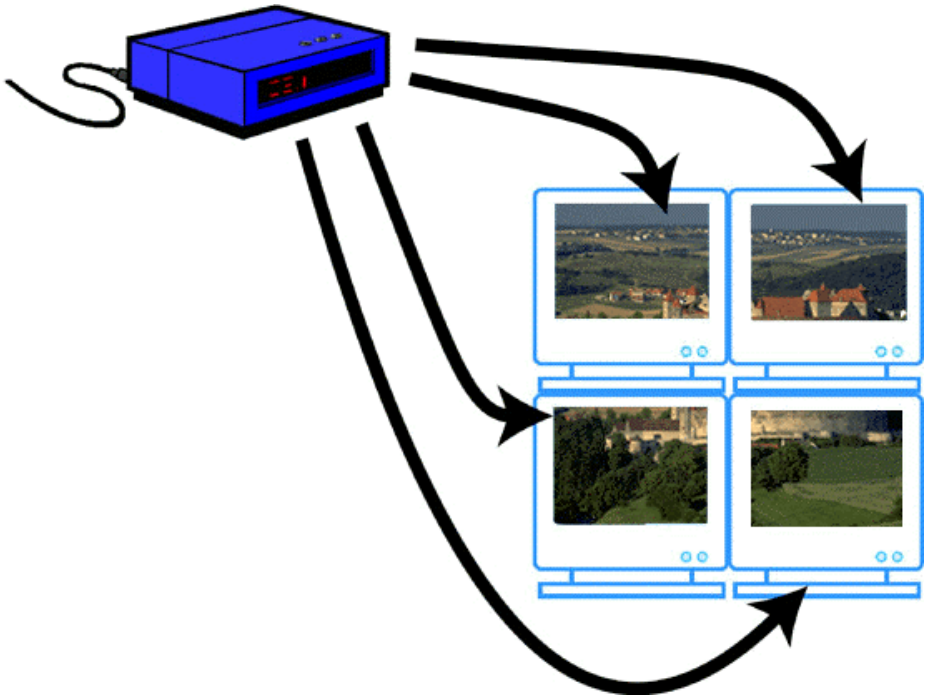

Figure 1 Overview diagram of the system

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Introduction

Today, human interactions and communication are greatly dependent on high-tech communication through computers. The information is usually conveyed to the computer users through the displayed images. In some circumstances, however, the displayed image size is not sufficient and needs to be enlarged. Examples for such cases are company presentations, medical images displayed during surgeries or illness diagnosis, advertisements, and entertainment. This brings a need towards larger screens with higher resolutions and less complicated setups and control systems.

The Multi-display Video Adapter or the MVA is a device that not only will answer this need, but also will provide the user with a user-friendly device. The MVA will get the SVGA output of the computer and will display each quarter of the image on a different screen after doing the appropriate signal conversions and signal processing. The external interface and the compatibility of the device with any type of computer system provide a user-friendly product with the most effective control system.

In this document, the design specifications of each unit of the MVA are described starting with an overall view of the design. The audience of this report is Dr. Andrew Rawicz, Mr. Steve Whitmore, Mr. Jason Roth, Mr. James Balfour, RimaTech Engineers, and selected external companies and professionals.

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System Overview

The MVA system will obtain the SVGA output of the computer as input, and generate four different SVGA outputs for the four monitors. A detailed diagram of the system overview of the MVA is illustrated in Figure 2. It describes how the system will acquire the signal from the computer, process the acquired signal, and generate the appropriate output of the four monitors.

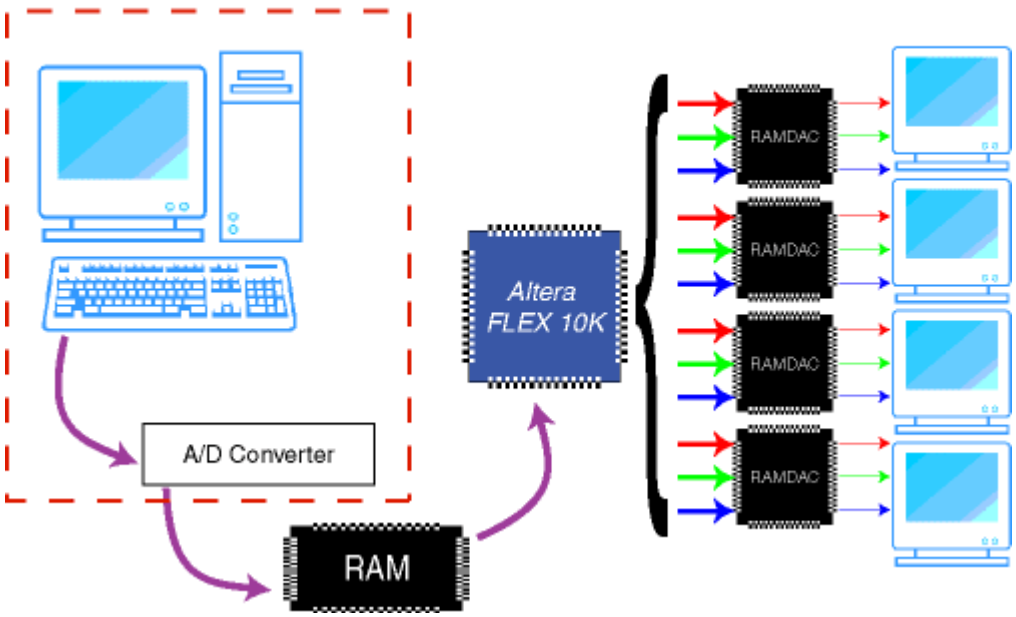

Figure 2 - System Overview

The first step of the design is to obtain the SVGA signal from the computer. Since the signal is of the analog format, it has to be first converted to digital signal for easier signal processing. The signal is then stored into a RAM to be ready for being processed by the Altera FLEX10K. In order to not loose any information and have no flicker in the final image, the A/D converters and the FLEX10K have to be operating at a very high frequency (A/D converters at 40MHZ & FLEX10K at 160MHZ). Since the facilities at SFU Engineering Labs are not fast enough for these high frequencies, the first part of the design (the red-dashed section) was replaced by an image in the memory-chip. This chip contains digitized pictures being downloaded from previously created files.

The FLEX10K then processes the signal and sends the developed signal for each part of the image to the appropriate monitor by first storing it into memory chips and then converting it back to the analog format. Before sending the new analog signals to the monitors the voltage levels of the signals have to be brought into the acceptable voltage range by the monitor.

The detailed schematics can be found in the appendix.

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Front-End: Generating Circuit

In the design of the front end of our system, we wanted to obtain the signal from the SVGA output of the computer. Therefore, we had to have an analog to digital converter to digitize the acquired signal before saving it in to the memory chips and processing it. According to sampling theory, the sampling frequency had to be twice the data rate we needed. For displaying an 800*600 resolution image the output data rate had to be 40MHz, thus the sampling frequency had to be 80MHz. Also for displaying on four monitors the memory had to be read at 4*40MHz=160MHz frequency. We found out that working with high frequency signals is almost impossible with the available equipment in the lab. And building precision high-speed circuitry is extremely expensive.

Therefore, we decided to reduce the frequency of the signal and concentrate more on displaying the image on four monitors rather than digitizing the SVGA signal from the computer. There are two modifications that we had to make to the design:

1) We changed the output from an SVGA signal to VGA signal, this way the output frequency will be reduced to 25MHz. According top the VGA spec, our device has to handle 640 x 480 resolution.
2) Instead of reading the image from the computer, we decided to read a constant image, which is stored in our prototype. This change is also made for reducing the frequency from 80MHz (for writing to the memory) and 160MHz (for reading from the memory) to 25MHz (the reading frequency of the memory).

With these two modifications, we can build a prototype that can illustrate the final output of the product. At this stage it is very important for us, to prove our concept to our potential customer and partners. This prototype can later be expanded with support of external companies to build the ideal high frequency model.

The following figure shows how the image is stored and read.

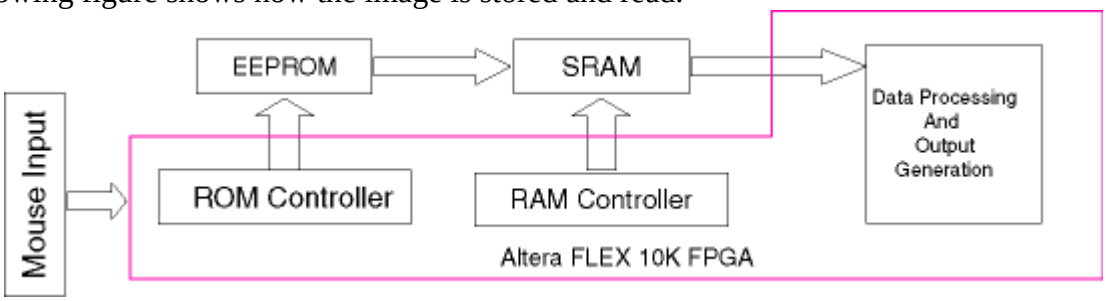

Figure 3 - Front-end Logic Block Diagram

The logic of the circuit is written in VHDL and runs on an ALTERA FLEX 10K20E FPGA Chip. During the startup the ROM Controller logic circuit downloads the image, which has been stored in the EEPROM to the SRAM. The reason we are not reading the image from the EEPROM for processing is

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that we need to read the data in less than 40ns, which is less that the EEPROM's access time. So we have to load the image data to the SRAM, which has a much higher access time. We can then process it from the SRAM using the RAM Controller logic inside the FPGA. To provide some animation, the image is moved on the screen using a mouse connected to the EVB (explained in more detail in the next section).

The following figures explain the controllers' logic.

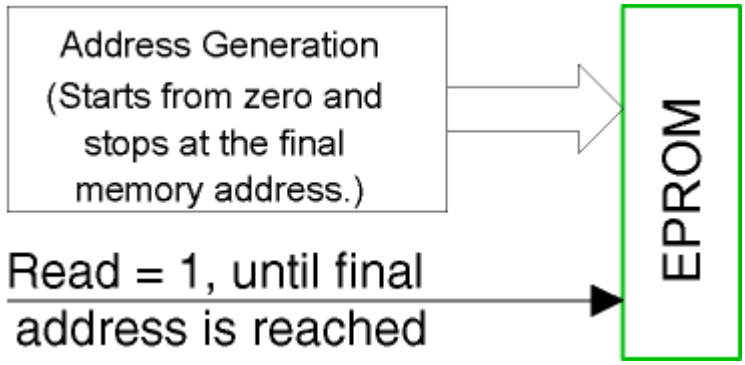

Figure 4 - EEPROM Controller Logic

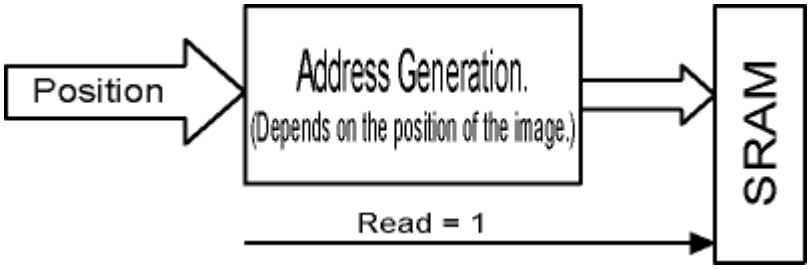

Figure 5 - SRAM Controller Logic

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Control system

In order to show that our prototype is capable of displaying the image on four monitors and enlarging the image, we added some controllers to the prototype. The controlling of the system is done by a Mouse, which is connected to our system. The input signals from the mouse will move the image throughout the four screens, enlarge the image on the screen, and switch between the images stored into the RAM. This way we are able to prove that our image dividing and processing techniques work.

Movements of the mouse indicate the position of the image on the four screens. The left button enlarges the image when pressed once, and reduces the size to its original if pressed again. The right button switches between the images in the memory. We had to write a mouse driver to be able to communicate with the mouse. The code was done in VHDL and is part of the downloaded program to the FPGA chip.

The mouse driver would first initialize a communication string to the mouse, get the real time information from the mouse, adjust the information, and then send it to the main block for use. Two of the adjustments were debouncing[1] the mouse buttons and changing the limits of the page whenever the left button was pressed.

[1] When we press a button the output signal does not stay high. It is as if we are pressing the button 10 times per second. We had to fix this problem so that the program would see only one 'click'. This procedure is called debouncing.

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Signal Processing

As we explained earlier, the input of our prototype system is an internally generated image. Our signal-processing unit splits the image and sends the image signal to the four monitors.

The signal-processing unit has different functionalities as listed below:

Enlarging and reducing the image size
As the images are shown on different monitors, the user can enlarge or reduce the size of the image with a click of the mouse (left click). If we only split the image and show it on the monitors the resolution would become 320*240. As one can imagine this resolution is not satisfactory. For having 640*480 resolution the signal processing block will be doing some data averaging of neighboring pixels in order to fill in the gaps, which are caused by splitting the image into four.

Swapping images
Our signal-processing unit is also capable of swapping two images. The user can change the displayed image with a different one using the right click of the mouse. This functionality of the signal-processing unit allows further development of our system to produce an animation graphics, which is basically, an image that is being swapped on the screen.

Figure 6 - Generating Animation

Synchronizing the images
An important functionality of the signal-processing unit is synchronizing the images on the four monitors. This means that the system ensures the images are displayed and changed simultaneously and the memory addressing is taken care of to show the correct part of the image.

In short, the signal-processing block does the following:

- Reads data from memory. (The user can map the signals to be read from different files to perform swapping.)
- Interpolates the data during the enlarge process and generates full 640*480 resolution data lines.
- Sends the produced full data signals into four monitors.

All these functions are implemented digitally in VHDL.

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Back-End

The back end of our system takes control of converting high-speed digital signals to SVGA standard analog voltage levels. We support both 3 bit and 24 bit digital formats. These two systems have different circuitry. The following is the overview of each design.

3-bit D/A

The 3-bit convector consists of a single line digital to analog converter, a voltage regulating circuit, and a protection mechanism. The following figure displays the subdivision of the 3-bit Converter.

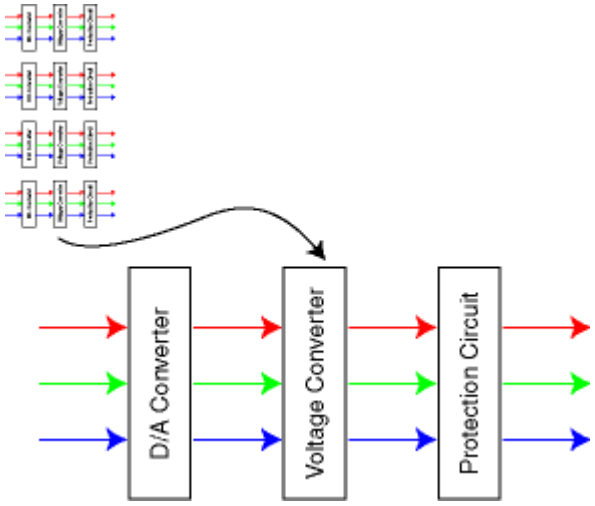

Figure 7 - 3-bit Output Block Diagram

The protection mechanism ensures that we do not use too much power, and protects our sensitive internal circuitry. It also ensures that we do not give too much voltage to the output, and protects the monitors from a short circuit.

We have to take the line impedance and the monitor impedance into account to make sure that we would not get any reflection from these blocks. Therefore, we have to match the output impedance to the standard 75-ohm impedance to ground (SVGA standard).

24-bit D/A

The 24-bit converter supports systems up to 24-bit (maximum SVGA standard). We use a 40 MHz RAMDAC that complies with SVGA standards. The input to this block is a 24-line bus. The RAMDAC has built-in circuitry that handles the digital signals, and generates appropriate analog output. We will use the Altera FPGA for controlling and programming the RAMDAC.

The following figure shows the block design if the RAMDAC is used.

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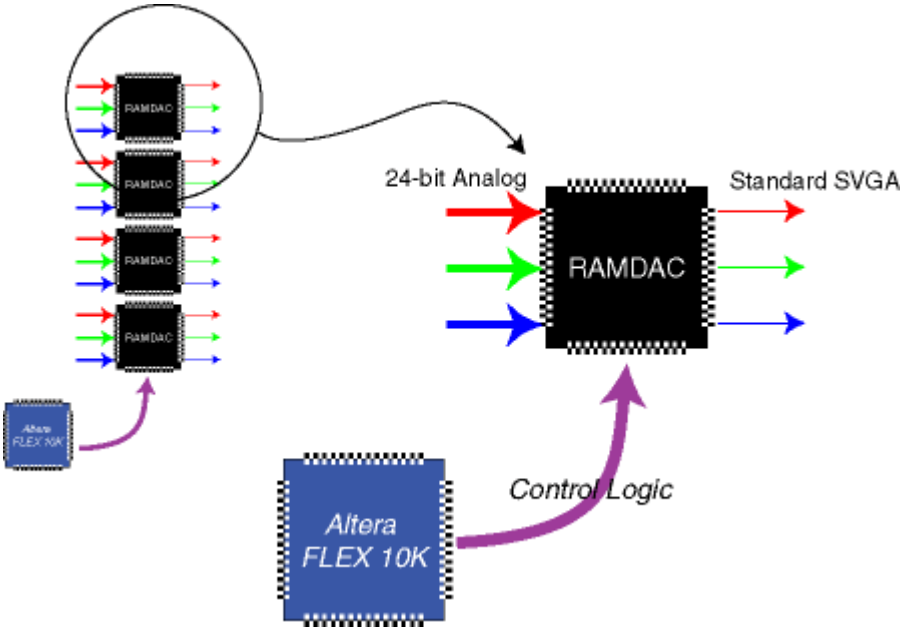

Figure 8 - 24-bit Output Block Diagram

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Enclosure

The Enclosure will be a lightweight plastic box. It will keep the internal circuitry safe from electrostatic shock.
All the input and outputs will be easily accessible and clearly marked.
Some additional weights may be added to the box to keep it on the ground, because all the cables attached to the system can easily lift a lightweight box.

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Testing

VGA Signal Testing

The following is the test procedure for the VGA signal testing:

1. The three RGB pins on each VGA connector are probed individually on the scope to see whether the signals meet the VGA spec. (i.e. the amplitude should be 0.6 - 1 Vpp)

2. Each VGA connector outputs a VSYNC and an HSYNC signal. The two mentioned signals are used for synchronization of each line and frame on the monitor respectively. Therefore, it is crucial for both the HSYNC and the VSYNC signals to have the same frequency and display no phase shift among the four monitor outputs.

Overall Testing

The following test plan describes the tests that our device will undergo in order to meet the main specifications. These tests are performed after the outputs of the device are connected to four monitors.

• *Image Enlargement (interpolation)* : When the mouse is left clicked, our image on the screen should double in size and when the it is left clicked again, the image should get back to its original size. We have implemented an averaging interpolation algorithm for enlarging the image size. Therefore, the quality of the image should remain as the quality of the original image size.

• *Image Swapping*: When the mouse is right clicked, our image on the screen should swap with another image. No flickering should be observed on the screen when the pictures are being swapped.

• *Boundary Checking*: If an image is positioned between the monitor's boundaries, no distortion on the image should be observed. The test is performed by moving the mouse (i.e. the image) and placing the image between the boundaries of the four monitors.

• *Flickering Image*: The images should be tested on the level of flicker that appears on them and how noticeable it is.

• *Image Overlap*: After the outputs of the device are connected to the monitors, the monitors should be put together to make sure that no overlapping is done on the images and no part of the images is missing or repeating.

• *Shifted Image*: The images on all four screens should be tested on not being shifted to another monitor (shifted to the left, right, top, or bottom).

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• *Image Resolution*: The image on each monitor should have the same resolution as the image on the other three monitors.

Figure 4- Normal Quad Output

Figure 5- Low resolution or Noisy output

• *Skew Image*: The images on all four monitors should be tested on being straight. No part of the image should be skew. They should also be tested on not being stretched out or shortened.

Figure 8- Normal Quad Output

Figure 9- Skewed Output

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http://www.idt.com/products/pages/SRAM.html
http://www.techservinc.com/links.html#Organizations

* Note: The complete list of reverences for the project is available online at: http://rimatech.cjb.net

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Appendix

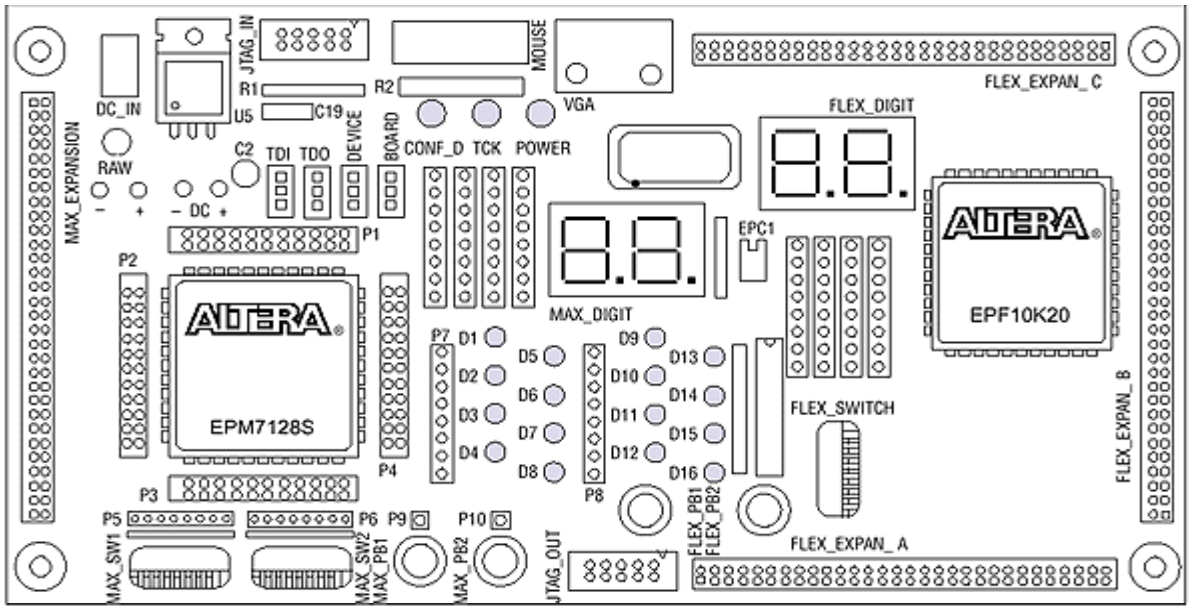

Figure 9 - Altera FLEX 10K EVB

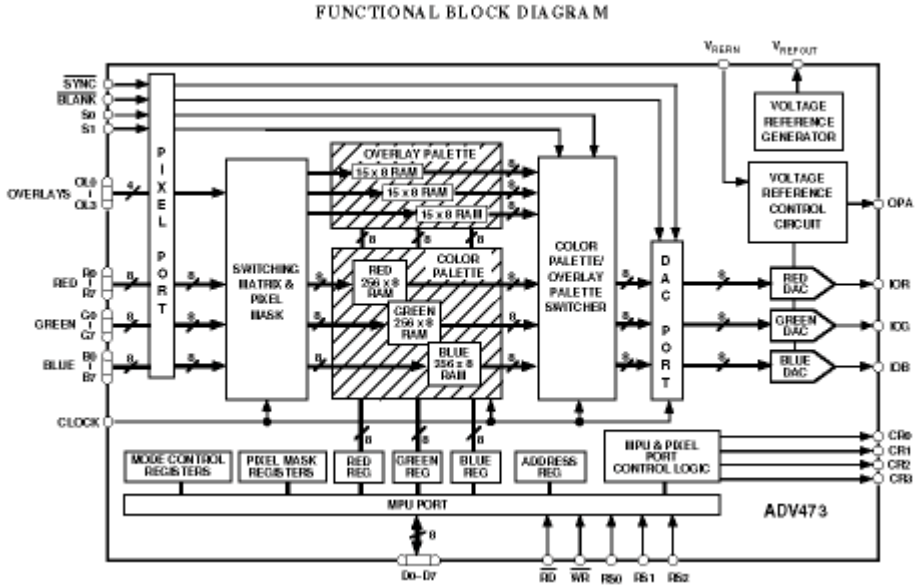

Figure 10 - ADV473 - RAMDAC

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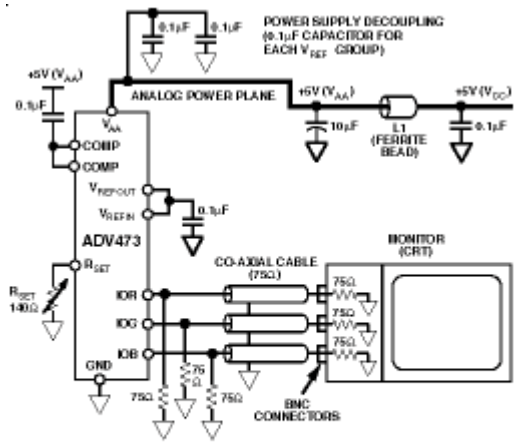

COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1µF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10µF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	

Figure 11 - RAMDAC Implementation

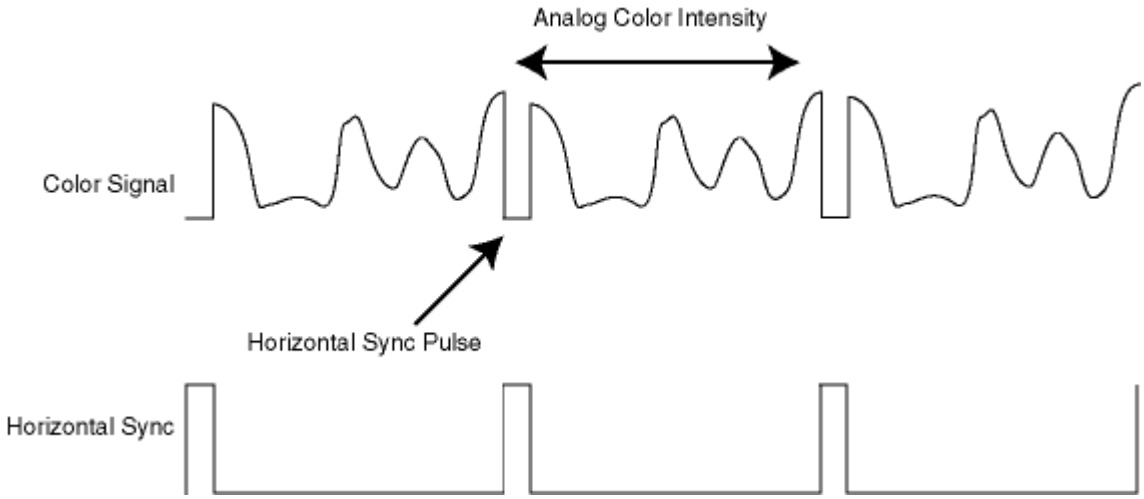

Figure 12 - SVGA Color and H-sync Signals

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Figure 13 - SVGA H-sync and V-sync Signals

Table 1 VGA/SVGA/XGA Connector Pin-Out

PIN#	**SIGNAL**	**DESCRIPTION**	
1	Red	(Analog)	
2	Green	(Analog)	
3	Blue	(Analog)	
4	Monitor	ID	Bit2
5	Ground	(Digital)	
6	Ground	(Red)	
7	Ground	(Green)	
8	Ground	(Blue)	
9	Not Used		
10	Ground	(Sync)	
11	Monitor	ID	Bit0
12	Monitor	ID	Bit1
13	Horizontal Sync		
14	Vertical Sync		
15	Not Used		