



DC Integration *Innovations*

School of Engineering Science
Simon Fraser University, Burnaby, BC, V5A 1S6

January 14, 2002

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, BC
V5A 1S6

Re: ENSC 340 Process Report

Dear Dr. Rawicz:

DC Integration Innovations has the goal of developing a more efficient, expandable, and maintainable solution for DC signal wiring. We will replace complicated and expensive wiring networks with a unified bus that uses a time division multiplexing strategy to carry a large number of DC signals.

We completed our prototype in December 2001 and presented a demo to you and other interested faculty members. We are now following up on that with a process report of how we were able to achieve our goals. Also included are future plans for our product and personal statements from all team members.

DC Integration Innovations is comprised of Ian Chan, Gary Lau, Erik Haberber, and Aydin Kilic. Each of these members brings their own unique skills to form a motivated and well-rounded team.

Please feel free to contact us if you have any comments or questions about our process report. We can be reached at dc-i2@sfu.ca

Sincerely,

A handwritten signature in blue ink, appearing to read 'Erik Haberber', is written over a light blue grid background.

Erik Haberber, CTO
DC Integration Innovations



DC Integration *Innovations*

DC Multiplexed Wiring System Process Report

DC Integration Innovations

Team Members Ian Chan
Gary Lau
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Contact Ian Chan
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Submitted To: Dr. Andrew Rawicz
Steve Whitmore
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Submitted: January 14, 2002



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1 Introduction

Through our diligence, efforts, and innovations, we have successfully completed the second generation of the DC-1I System. As we have demonstrated, the system is fully functional, with the hardware designs implemented at the prototype board level. This document serves to examine and describe the process that evolved the DC-1I system from a concept to its present state. Furthermore, this report contains an overview of the personal experiences of each team member, and also plans for the future development of the system.

2 System Overview

The *Direct Current – Integrated in One (DC-1i)* is a time division multiplexed wiring system that replaces the complication of a traditional wiring system with a unified bus architecture. This new multiplexed wiring approach replaces thousands of individual wires with a single data bus. A block diagram of the **DC-1i** system is shown below in Figure 1.

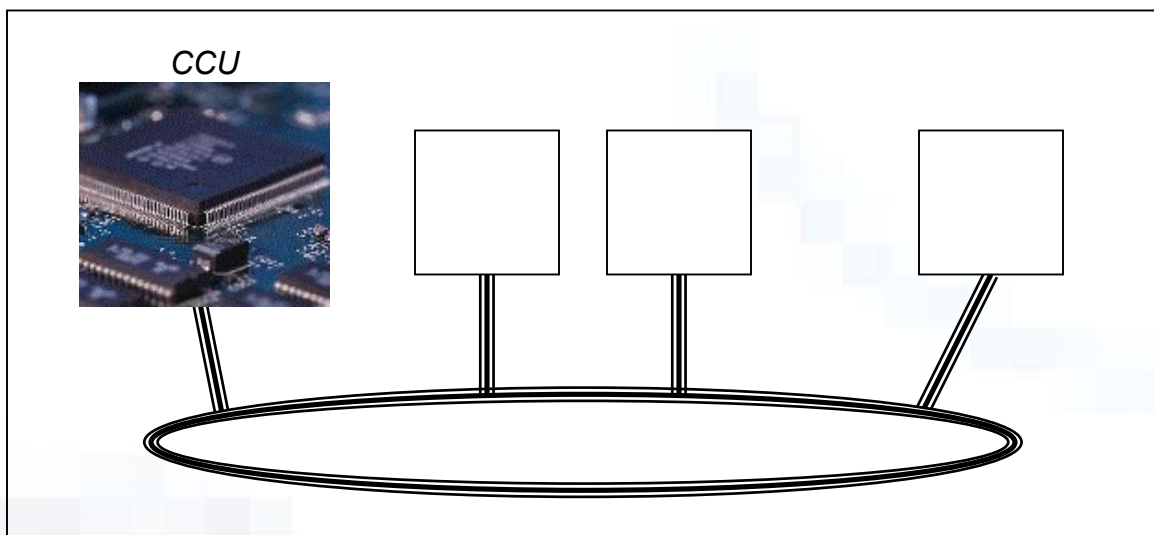


Figure 1: DC1i System Overview

2.1 Functional Blocks

The **DC-1i** system consists of a Central Control Unit (CCU) that controls the use of the unified bus. Different points on the bus provide input and output to various



devices in the system, and each of these points is referred to as an Input/Output Node (ION). An additional module, called the System Diagnostic Unit (SDU), can be connected to the unified bus and used to diagnose problems in the system or in the external circuitry.

2.1.1 Central Control Unit (CCU)

The CCU is responsible for the arbitration of the bus. This unit determines the address of the transmitting and receiving channels and connects input nodes with output nodes. It alone is responsible for the timing of the bus transactions.

2.1.2 Input / Output Node (ION)

The IONs are points on the bus where the **DC-1i** system interfaces with the external world. At these nodes, data can get on and off the bus and transfer to or from external circuitry, such as switches, sensors, or actuators. Each node may contain multiple input or output channels. Under the supervision of the CCU, data is transferred from a single input channel to multiple output channels via the bus.

2.1.3 System Diagnostic Unit (SDU)

The SDU is an external module that can be inserted at any point on the bus. Once attached, the SDU gathers data on every channel that is being transmitted on the bus. The SDU relays the data on all channels to a PC or laptop via a parallel port interface. This data is then interpreted and any problems with the **DC-1i** system are diagnosed. This unit can also, and more commonly, be connected for diagnosing problems that are not related to the **DC-1i** system, but instead are problems with the external circuitry. The SDU will give service personnel a detailed view of what data is being transmitted on the bus, and thereby allow them to pinpoint any malfunctions in the external circuitry.

3 Current Status of DC-1i

In the several months of development for the **DC-1i** product we were able to construct a fully operational platform that was programmed to handle a maximum of 64 channels on the bus at any given time. An onboard power supply was also constructed which allowed the entire system to operate independently from an automotive battery. In our demo we only used a fraction of the potential bandwidth of our system as we only used 16 of the 64 channels. At the product's current state it could easily be upgraded to handle 256 channels by a few minor changes to the code. Development of the **DC-1i** system went relatively smoothly as we designed our system to be as simple as possible in order to increase reliability and reduce complexity.



Our entire system consisted of the CCU, a 16-channel FPGA node, an 8-channel flexible node, a 4-channel hardwired input node and a 4-channel hardwired output node. We constructed a demonstration setup that consisted of a mock dashboard (affectionately referred to as the “*Ghetto Dashboard*”) that housed the controls typically found on an automobile’s dash, such as a horn, light controls, temperature controls, fan controls and gauges. The demonstration setup also consisted of a control board that represented the engine compartment of an automobile, on the control board was a fan, incandescent light bulb, horn and various dials and switches to control the displays on the dashboard. We also modified a small model car with LEDs to represent the headlights, brake lights and turn signals of an automobile. Finally, we wired up these different components with our nodes and a single unified bus in a closed loop to demonstrate the transmission of data by our system. We demonstrated the diagnostic capabilities of the SDU by inserting the SDU at any point in our system and then displaying on the PC the data contained on each channel. The “*Ghetto Dashboard*” allowed us to demonstrate the features and potential of the **DC-1i** product.

3.1 Central Control Unit (CCU)

The Central Control Unit is fully operational and also houses the onboard power supply that provides power to the entire system. The CCU consists of only a microcontroller, a crystal oscillator and two line drivers. This simple hardware implementation allowed us to also simplify the controlling firmware and reduce the complexity of the system as a whole. At its current state the CCU can be easily upgraded by modifications to the firmware, for example more features can be built into the system simply by adding the feature to the code.

3.2 Input / Output Nodes (IONs)

The basic design of the Input / Output Nodes are very simple in nature and thus we were able to construct several different variations of the IONs to demonstrate the flexibility of the node design, and to illustrate the possible size and cost reductions. In our development, the following IONs were constructed:

- 8 Channel Flexible Node
 - selectable channels (DIP switches)
 - selectable input/output modes (jumpers)
- 16 Channel FPGA Node
 - fixed channels (in FPGA code)
 - selectable input/output modes (jumpers)
 - reduce size and components
- 4 Channel Hardwired Input Node
 - fixed input channels (hardwired)
 - input mode only
 - reduce size and components



- 4 Channel Hardwired Output Node
 - fixed output channels (hardwired)
 - output mode only
 - reduce size and components

Another feature of our ION design is that mass-producing large quantities of these nodes is very quick and inexpensive. Efficiency can be further improved by incorporating all the hardware in a node onto a single Application Specific Integrated Circuit (ASIC). This would reduce size and production costs, and at the same time increase reliability. See Future Plans for more details.

3.3 System Diagnostic Unit (SDU)

The System Diagnostic Unit is fully operational and includes most of the features that we had envisioned in our initial concept. The SDU captures all the channel data from the bus and transfers this information to the PC via the parallel port. For our demo we presented a few of the possible applications that can be used to process this data. We demonstrated that data can be updated in real-time from the parallel port and displayed on the PC for diagnosis. Basically, we have proven the concept that any data on any channel is visible to the PC. This opens the door to a wide range of applications that can be developed on the PC to interpret and analyze the data.

We were also inspired to add some additional features to the SDU. Specifically, we implemented an LED node detection scheme that allows service personnel to instantly pinpoint the location of any breaks in the DC-1I bus. It lights up a string of LEDs (one at each node) along from either the left or right so that the bus continuity can be visually verified. This feature is a great highlight of our product in terms of reliability and maintainability.

4 Deviation of DC-1*i* from Initial Design

4.1 Overall System

For the most part no major changes were made to the overall system design. We did not demonstrate the full bandwidth of the **DC-1*i*** system but this was because we just did not have enough information to send over all the channels. Our mock dashboard demonstrated transmission of 16 channels and provided a proof of concept for our system.

4.2 Bus Protocol

The DC-1I bus protocol was modified in one respect: the Data Ready (DRDY) line was eliminated. This was done for a number of reasons, including the following:



- After gaining a deeper understanding of the sample and hold circuit that we implemented, we realized that a somewhat ambiguous value at the beginning of the sample period would not be a huge problem since it would be removed by the end of the sample period. Also, since there would be no source driving this value, it would not significantly impact on the charge on the hold capacitor.
- In order to generate the delay associated with DRDY, we would have to add a timer to each channel on each node. This would drastically increase our hardware costs. The analog switches used had a turn-on delay of 200 ns, which we decided would be sufficient.
- Eliminating the DRDY line allowed us to eliminate one conductor from our bus, making the wiring and connectors simpler.

4.3 CCU

From a hardware standpoint, the CCU was built exactly as detailed in the functional specification. The power supply, PIC microprocessor, and line drivers all operated satisfactorily.

The firmware of the CCU was modified somewhat from the original plan, mainly to accommodate the removal of the DRDY signal. As well, some fine-tuning was done to the timing of the output signals to clean up some cross-talk problems that we encountered when running multiple channels.

4.4 IONs

There were no major deviations from the initial design of the IONs. The ION design was kept as simple as possible while maintaining a certain level of flexibility.

4.4.1 Configuring Input / Output Nodes

The only significant change was to incorporate input / output selection to the design of the IONs. The initial ION design distinguished between an input channel and an output channel, but we later decided that it would be worthwhile to be able to select whether the channel is an input or an output. With a little bit more hardware and a jumper we were able to incorporate this in our 8 channel flexible node and our 16-channel FPGA node. When our requirements became more solid, however, we found that it would be more beneficial to hardwire the address and fix the input or output mode. We therefore created the 4-channel hardwired input and 4-channel hardwired output nodes.



4.4.2 FPGA Input / Output Node

When constructing the first ION (8 channel flexible node) we observed that the amount of components necessary just to accommodate 8 channels took up substantial space on the board. We then realized that we could achieve many more channels with fewer components if we replaced the comparators and DIP switches with a single FPGA that would do all the comparing necessary. Thus we began the construction of the 16-channel FPGA node that served as a proof of concept that the size of each node can be reduced significantly if we move away from discrete components and migrate towards a more integrated approach. The FPGA node showed that we could fit 16 channels in the same area that previously only contained 8 channels. Further efficiencies can be achieved by combining more logic components into an ASIC form.

4.5 SDU

The SDU was drastically modified from its original design. At first, we planned to have the SDU operating in real time with respect to the bus timings. (sampling the value of each channel every time it was updated) However, we realized that this would require an extremely fast analog to digital converter, faster than any which were commercially available. Therefore, this goal would not be possible.

As a plan B, we decided to make the SDU a slave device to the host PC. Instead of the SDU continuously scanning the bus and storing the values of all the channels in its memory, we made it respond to specific requests from the PC. The PC would make a request to the SDU with a channel number, and then the SDU would configure an onboard hardware node to obtain the value of that channel. Once this was completed, the SDU would convert that value into digital form and send it back to the PC.

By making this change in architecture, we were able to get the SDU fully functional in the time allowed and still meet all the performance requirements. It turned out that the limiting factor in terms of latency was the PC itself, and so our slower bus-monitoring rate had no impact whatsoever. Our GUI was able to obtain all of the data that it needed from the SDU.

5 Future Plans

While we are very pleased at our completion of a working prototype, there is still a lot of development to be done before our product is ready for market. Specifically, we would like the chance to make the following improvements:



- We had a problem with cross-talk between the channels, which we were able to improve greatly through fine-tuning the bus timings. However, we believe that we can completely eliminate this through additional measures such as isolating the digital and analog grounds used in our system.
- In order for our product to present a competitive alternative to conventional wiring systems, we will have to ensure that we have the lowest possible cost. While our costs are already low, we intend to reduce them further by integrating the functionality of the ION onto fewer chips.
- To ease deployment in automotive applications, the nodes will have to be made smaller. As we have shown with the FPGA node, moving to a more integrated format allows us to dramatically reduce the size. We hope to continue this trend by moving to an ASIC chip and a PCB.
- Our current SDU design is a proof of concept, showing that a PC can easily read any data on the bus. We would like to build additional features onto this platform. Some possibilities are: TCP/IP for remote debugging, and automated test sequences for ignition timing, ABS operation, etc.

We feel that we have developed a product that may have real market potential. We are therefore currently investigating the possibility of obtaining a patent for our technology. In fact, we have formed an alliance with a team of three commerce students at Queen's University who are using our idea for a project course in which they will make a business plan and continue patent research.

6 Budget Constraints

The estimated budget that was initially presented in our project proposal is shown below in column two of Table 1. Also shown in Table 1, in the third column, is the actual cost that was incurred over the course of our product development.

Table 1 - Estimated Budget vs. Actual Budget

Required Materials	Estimated Cost	Actual Cost
Control Logic (Microprocessors and FPGA)	\$200	\$100
Wiring & Connectors	\$90	\$50
Packaging	\$120	\$60
Test Equipment	\$150	\$100
Miscellaneous Electrical Parts	\$100	\$360
TOTAL	\$660	\$670



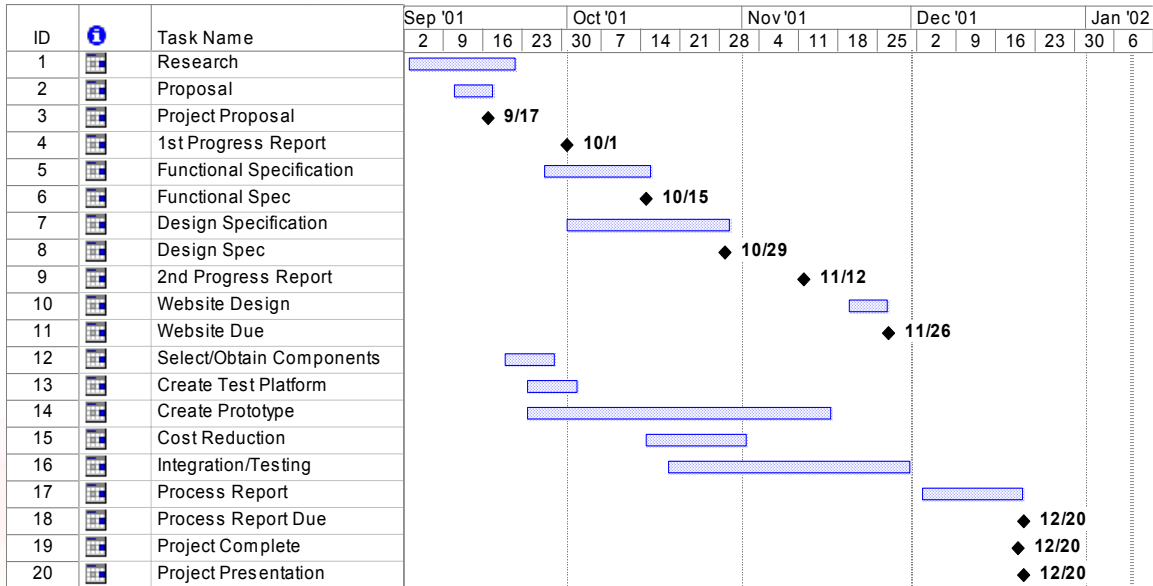
As can be seen from the above table our product development costs were right on our projected budget. Table 1 shows that we overestimated the costs for almost all our required materials except for one category, we did not anticipate that we would require so many miscellaneous electrical parts and that drove our costs up. In the end, our actual costs were approximately \$10 more than our initial budget estimations. Table 2 shows a detailed list of our expenditures for the development of the product.

Table 2 - Expenditures

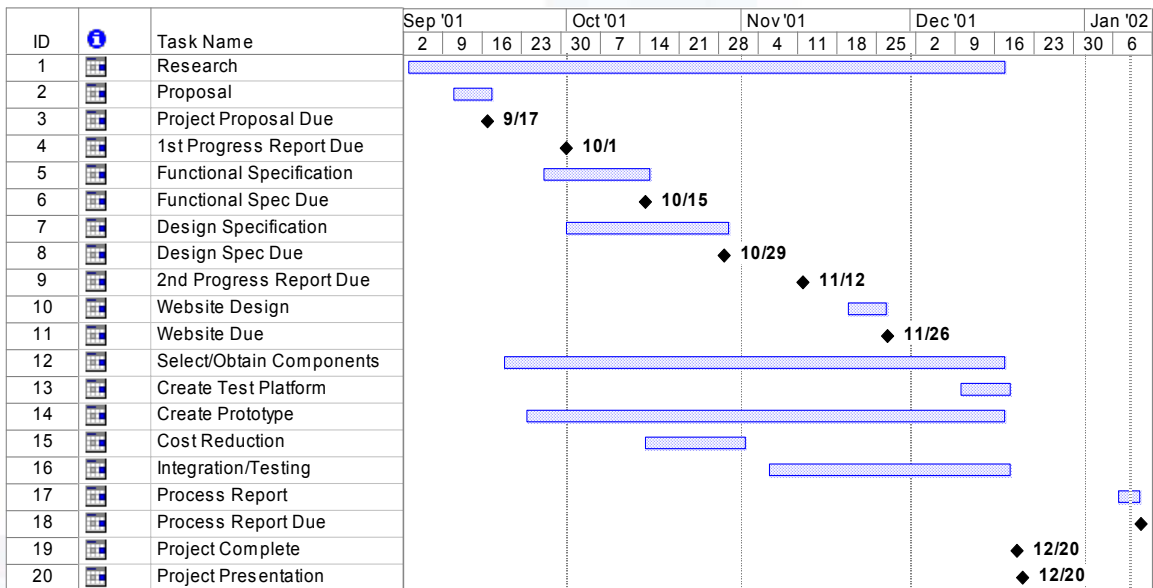
Date	Company	Amount
10/01/2001	DKC DIGI KEY CORP	\$106.64
10/02/2001	ACTIVE VANCOUVER	\$24.61
11/13/2001	ACTIVE VANCOUVER	\$38.65
11/13/2001	R.P. ELECTRONICS	\$9.12
11/13/2001	R.P. ELECTRONICS	\$42.33
11/13/2001	DKC DIGI KEY CORP	\$147.30
11/27/2001	R.P. ELECTRONICS	\$57.56
12/17/2001	INTEK ELECTRONICS	\$12.57
12/17/2001	ACTIVE VANCOUVER	\$13.06
12/17/2001	R.P. ELECTRONICS	\$24.90
12/18/2001	THE HOME DEPOT	\$7.76
12/18/2001	WAL-MART	\$19.02
12/19/2001	DKC DIGI KEY CORP	\$114.74
12/19/2001	PLASTICSMITH	\$54.16
	TOTAL	\$672.42

7 Time Constraints

The following Gantt chart, reproduced from our project proposal, illustrates our original estimate of the time to complete various tasks of the project.



However, things did not go as planned. The following Gantt chart illustrates the actual time required to complete various tasks of the project.



Our initial research and prototyping was greatly under-estimated. New issues and problems were created by the prototyping stage, which created the need for research to find solutions. As a result of the elongated prototyping and research stage, other planned tasks were set off schedule.





Waiting for parts during the last stages of the project also caused a lot of delays for project completion.

Other factors that caused slippages from the original schedule were course load outside of ENSC340, laziness, and exams.

8 Personal and Technical Experiences

Ian Chan

Enrolment in ENSC 340 has been an extremely valuable experience for me; the course has expanded my ability of applying theory in real world situations as well as challenged my ability to overcome hardware design issues. Throughout the course of this project I have stressed the design for simplicity principle, which advocates that a simple design is a good design, this has proven to be true because a simple design increases reliability by allowing fewer points for failure.

I have found ENSC 340 to be one of the most valuable and fulfilling courses to date because it is one of the few courses that really allows our imaginations to dictate our achievements. Thus, I was an enthusiastic contributor to the initial conception of the project idea; I was also actively involved in the design of the bus protocol, which is the very basis of the system.

Many of my technical responsibilities were on the hardware intensive portions of the project. Design of the Input / Output Nodes was a challenge because it was necessary for the design to be simple yet flexible. Creation of the FPGA node was also a unique challenge as it allowed me to expand on my Very High Level Hardware Description Language (VHDL) coding skills and gain more familiarity with Field Programmable Gate Arrays (FPGA). I also improved my soldering and hardware troubleshooting skills, as I was responsible for the construction of the CCU and the FPGA node hardware. Valuable experience was also gained in system level testing and performance evaluation, since we tested the individual components of the system as well as the entire system as a whole. My responsibilities also included the design and construction of the demonstration setup (mock dashboard and control board).

Throughout the course of this project I have found that time budgeting is a very critical aspect to completion of a large project. One should always be prepared to spend more time than anticipated on any given task because (as we found out) things do go wrong and when they do it is important to have allowed enough time to correct them. Another important lesson we learned is to always plan ahead, that way one can contemplate the different options and choose the best possible solution to any problem.



Finally, one of the most important things I take away from this course is dealing with team dynamics. In a large project such as ENSC 340 or perhaps a project encountered in industry, the entire team must set goals to achieve as a collective. In addition, members of the team must take initiative to set their own long and short term goals to benefit the project. I also learned that communication is vital to the success of the project, as all parties must coordinate their individual tasks in order to meet the milestones of the entire project. In a team, every person has different skills, different thoughts and different points of view. This semester, I have learned that it is the coordination of all these factors that makes a project a success.

Erik Haberberger

I had been looking forward to this course ever since completing my project for ENSC 151. I really enjoy the chance to work on the design side of a project, as opposed to filling in the blanks on an assigned project. Our project was a good challenge because it contained a wide variety of tasks, including all of hardware, software and firmware.

My main responsibilities in the project were firmware and system interface. I worked mainly on the following tasks:

- Firmware for CCU
- Firmware for SDU
- Construction of SDU
- SDU/PC Interface Protocol
- DC-1i Bus Protocol
- Architecture of data transmission path
- Editing Documents

I believe that we all learned a great deal as we worked through this project. Although we came into 340 with knowledge of circuits from 220, 225, 320 and 325, we had never actually implemented them other than in labs that told us the exact circuit to build. It was neat to design something based on a theory and have it actually work in practice. I gained a lot of confidence in my abilities as the things that we built actually worked!

One thing that we could have done better is project scheduling. Because we started our brainstorming in the summer, we fell into a bit of a trap thinking that we were ahead of the schedule. For a few weeks in October, we got into a routine where we would meet to work on the project but merely set it up and then proceed to shoot the breeze for a few hours. We started to turn on the pressure in November, but then exams forced us to leave a good chunk of work for a 5-



day marathon immediately before the demo date! As we came down to the wire, however, we became very disciplined and methodical – we made deadlines and statements such as, “If the SDU FW isn’t finished by noon on Tuesday, we’re postponing the demo”.

Our group worked well together. After the initial architecture of the project was formed, group members with various skills took the initiative to work on the areas where they had proficiency. However, we communicated well enough with each other that the integration of efforts was quite painless. It was also interesting to note the roles played by different people. While myself and another optimist were coming up with lists of possible features, a “Devil’s advocate” stepped forward to remind us that we had to actually deliver what we promised. In this way we formed a project that was challenging and yet possible.

In all, I was very glad to have the opportunity to take this course. In a sense, the course allowed us to do what we had always wanted to do, but never had the time for because courses are a higher priority than personal interest projects.

Aydin Kilic

Technically, I contributed to the design of and construction of various hardware circuits. This exercised my knowledge of electronics, and my ability to implement circuits. Furthermore, I researched various technical issues both related and unrelated to our final product. Before we had decided on our 340 project, we had many interesting ideas, and I spent a lot of time looking into what methods we might use to implement our ideas, and what resources were available to do so. I enjoyed this particularly, since it gave me the chance to ‘see what’s out there today’ in our world of technology.

I felt that one of the most important lessons I learned was to realize the necessity of timely tasks. If one has spent several hours trying to achieve a certain goal, one should take the time to consider certain factors. First, is there a more efficient, less time consuming manner to get the job done? If not, is it possible that the goal might be achieved through another component of the system (i.e. can any existing components be adjusted to effectively do the same thing)? And finally, is the task entirely necessary for the trouble that it worth? This final consideration is especially important when the deadlines are fast approaching.

Working on this project has been an eclectic experience. Through the many stresses and joys, we have ultimately succeeded. We not only applied our existing knowledge of engineering and technology, but also learned new technical and practical skills. Beyond this, we also had to integrate the various components of our system. This practice required a significantly greater amount



of work than we had initially thought. Therefore, through this 'extra' work, I gained insight into what it really takes to put an entire project together. I believe that this is what makes ENSC 340 such an educational course. I also believe that this experience is distinctly unique from co-op, in that we were in control of all the design decisions (whereas on co-op terms, we usually do not contribute to the ground-up design). Through all this, I feel that we have all become better engineers.

Gary Lau

Technical Experience

Our project consisted of many hardware devices. The following are devices that I constructed:

- 8 Channel Selectable Input/Output Node (ION)
- 4 Channel Hardwired Input Node
- 4 Channel Hardwired Output Node
- LED Test Car

I also helped in the construction/development of:

- Initial layout and design of the System Diagnostic Unit
- Test setup

I developed and implemented the Graphical User Interface for the SDU and helped define the communication standard for communication between the SDU and PC. I was also responsible for the DC Integration Innovations website.

Technically, the project was very interesting. At first, all hardware components worked to original design expectations. However, during system integration a lot of interesting and unpredicted things happened. The most important technical lesson learned is that hardware doesn't always work the way you predict in a larger system consisting of other hardware and other variables.

Personal Experience

ENSC340/305 has taught me a lot about personal relations and experience of group members in my team. The workload was quite high as we had some internal issues.

A lot of stress was put upon others and me the four days before our presentation, when we really had to rush to get stuff done. There were a few events during these four days that could have delayed our presentation until next semester, but we managed to work through them quite well. In fact, another group helped us



out with a PNP transistor we needed to complete the SDU after killing four PIC microprocessors. To help complete this project in time I became the devil's advocate, making sure that things are done at certain times and questioning choices just to make sure we had not overlooked anything.

Trust in peers is very important and the lost of this trust is very damaging.

Overall, I would say that I had an enjoyable time. Reward is only truly received with effort and hard work.

9 Acknowledgements

DC Integration Innovations is very grateful to the following. Their help was tremendously appreciated in designing and building our prototype.

Andrew Rawicz – Our inspirational leader, Dr. Rawicz provided us with the knowledge of how to successfully create and develop a project. This included all the organizational, technical, and practical aspects of the process. Through his course, we have gained a vast multitude of engineering experience and education.

Steve Whitmore – Mr. Whitmore, our communications guru, guided DC-i² Systems in creating concise, informative documentation throughout the entire process of development. Through his attentive revisions and suggestions, we were able to greatly improve the quality of our literature.

Jacques Vaisey – Dr. Vaisey, who specializes in DSP, helped us to realize the particular frequency considerations from which interference issues arise. With this knowledge, we managed to avoid having a faulty system prone to electromagnetic interference (thereby making our product highly dependable).

Patrick Leung – Mr. Leung's proficiency and experience with microcontrollers and FPGA proved to be very helpful as we moved forward in utilizing these components in our design. This included assistance regarding microprocessing requirements. He also provided us with a free FPGA (thanks Patrick!).

Fred Heep – With several years of experience in the field, Mr. Heep provided us with invaluable insight into issues for consideration while selecting and sourcing



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our components. Also, he provided us with many useful tips and suggestions, including everything from programming our PIC to selecting diodes.



DC Integration Innovations