

School of Engineering Science Simon Fraser University, Burnaby, BC, V5A 1S6

October 15, 2001

Dr. Andrew Rawicz School of Engineering Science Simon Fraser University Burnaby, BC V5A 1S6

Re: ENSC 340 Functional Specification for a Multiplexed Wiring System

Dear Dr. Rawicz:

DC Integration Innovations has the goal of developing a more efficient, expandable, and maintainable solution for DC signal wiring. We will replace complicated and expensive wiring networks with a unified bus that uses a time division multiplexing strategy to carry a large number of DC signals.

Our attached functional specification outlines the parameters that the finished product will fulfill. The document lists the specifications that will be completed by the end of this course, as well as some additional features that are intended for future work beyond December 2001.

DC Integration Innovations is comprised of Ian Chan, Gary Lau, Erik Haberger, and Aydin Kilic. Each of these members brings their own unique skills to form a motivated and well-rounded team.

Please feel free to contact us if you have any comments or questions about our functional specification. We can be reached at <u>dc-i2@sfu.ca</u>

Sincerely,

Erik Haberger, CTO DC Integration Innovations





DC Multiplexed Wiring System Functional Specification

DC Integration Innovations

Team Members

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Contact

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Submitted To:

ted To: Dr. Andrew Rawicz Steve Whitmore School of Engineering Science Simon Fraser University

Submitted: October 15, 2001



Executive Summary

With the ever-increasing complexity of electronic systems today, interconnections between various functional blocks becomes more and more of a challenge and this increased complexity also brings increased costs. DC Integration Innovations proposes a solution to this growing problem with the introduction of the *Direct Current – Integrated in One* (**DC-1***i*) multiplexed wiring system. The **DC-1***i* replaces the thousands of wires in a traditional wiring system with a single unified bus that provides an interconnection between all the nodes in the system.

Development of the **DC-1***i* system will be performed in three phases. The first phase will involve the creation of a simple working prototype that will provide a basic two point input/output test platform. The resulting first prototype (ENG0) will incorporate the following features:

- Single input node and single output node
- CCU arbitrating bus transfers

The second phase of development will provide a more stable platform for development. This second prototype (ENG1) will have the added features:

- Multiple input and output nodes
- Power saving modes for low power operation
- Short circuit protection circuitry
- On board power supplies

The final phase of development will lead to the creation of a production quality platform (ENG2). Added features not found on its predecessors include:

- In Circuit Serial Programming (ICSP) of microcontroller
- System Diagnostic Unit (SDU)

The first and second phase of development will be completed by December 2001.

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1 Introduction

The DC-1i system unifies wiring configurations involving many wires, as is common in such intricate electrical systems as those for automobiles. This is accomplished through the implementation of several Input/Output Nodes (IONS) along a unified bus controlled by a Central Control Unit (CCU). The DC-1i system is intended to be an efficient alternative to the costly and complex traditional wiring systems that exist in automobiles today. This efficiency stems from the simplicity of the design, which provides for faster, cheaper, and easier implementation and diagnosis of the system.

1.1 Scope

This document will describe the functional requirements that must be met by the DC-1i system. Each stage of development will be subject to different requirements (though these requirements are by no means mutually exclusive in different stages). It is expected that, as the product evolves and progresses through development, additional requirements will be appended. These will likely arise through conformance to certification regulations and compatibility issues, as well as unforeseen issues that arise during development of the prototype.

1.2 Glossary

- **CCU** Central Control Unit
- ION Input/Output Node
- **SDU** System Diagnostic Unit
- **ICSP** In Circuit Serial Programming

1.3 Reference Documents

- [1] DC Multiplexed Wiring System Project Proposal. DC Integration Innovations.
- [2] DC1*i* Bus Protocol. DC Integration Innovations.
- [3] Standard TTL Logic Levels. Twisted Pair web resource.
- [4] Interfacing the Standard Parallel Port. C. Peacock.

1.4 Audience

 Investors and vulture capitalists will use this document as a reference and a definitive source of information regarding the functionality and economic viability of the DC-1i system.

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- Designated design engineers will both reference and update this document as future versions of the DC-1i system are developed.
- Other design engineers will reference this document when developing auxiliary or complementary products for the DC-1i system.
- Executive staff and management will use this document as a reference and checklist throughout product development. This will help ensure that all of the original design goals are incorporated in the final product. Also, they may update this document is a management decision is made to modify existing requirements or to add further requirements
- Marketing staff will reference this document as needed to prepare marketing materials. In addition, this document may be forwarded to companies (such as automobile manufacturers) who may be interested in implementing our system an d would like details on what kind of performance they can expect form the DC-1i.

1.5 Requirement Notation

Throughout this document we will designate each functional requirement with a unique requirement number, as follows:

[XX#] Functional requirement

The XX is a two-letter code referring to the class of requirement (Hardware, software, etc.) The numbers may not be continuous to allow the addition of further requirements as they become necessary.

DC Integration Innovations intends to implement the development of the **DC-1***i* system in a several stages. The first development stage will consist of construction of a proof-of-concept prototype, be referred to as ENG0. The next phase of development will involve the construction of an ENG1 prototype, used for system optimization, miniaturization, and cost reduction. Lastly, a final production device will be produced which will be referred to as ENG2, although our schedule will only require the completion of ENG1 by December 2001.

Following each functional requirement there will be a bracketed number to indicate the development stage that it is required for. The numerical designations are as follows:

(1) A functional requirement for ENG0

- (2) A functional requirement for ENG1
- (3) A functional requirement for ENG2

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2 System Overview

The *Direct Current – Integrated in One* (**DC-1***i*) is a time division multiplexed wiring system that replaces the complication of traditional multiple wiring systems with a unified bus architecture. This new multiplexed wiring approach replaces the thousands of individual wires with a single data bus. A block diagram of the **DC-1***i* system is shown below in Figure 1.



Figure 1: DC1*i* System Overview

The **DC-1***i* system consists of a Central Control Unit (CCU) that controls the use of the unified bus. Different points on the bus provide input and output to various external devices. Each of these points is referred to as an I/O Node (ION).

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3 System Requirements

These requirements are for the overall system. Some of these requirements may necessitate other requirements for individual components, which will be listed later.

- **[SY01]** The SW must support the following numbers of channels:
 - 1 channel (1)
 - 64 channels (2)
 - 256 channels (3)
- **[SY02]** The SW must guarantee a minimum refresh rate of 50 Hz for highest priority channels and 5 Hz for lowest priority channels. (2,3)
- **[SY03]** The bus wire must carry signals reliably over distances of up to 10 meters. (2,3)
- **[SY04]** The bus wire must not contain a single point of failure. (2,3)
- **[SY05]** The CCU and IONs must be easily replaceable in the field, in the event of failure. (3)
- **[SY06]** The system must be able to detect and disable improperly configured IONs and raise an appropriate alert to the user. (3)
- **[SY07]** The system must operate reliably in an automotive environment, and must not be adversely affected by any electrical interference or mechanical shock. (2,3)
- **[SY08]** The system must make efficient use of power to avoid depleting the vehicle's battery. (2,3)
- **[SY09]** The system must have a hard-wired backup for critical signals related to safety. (2,3)

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4 Physical Requirements

These requirements specify physical constraints on the system and the individual components. It is very important to meet these requirements so that the DC-1i system may be easily implemented in automotive applications.

4.1 Power

- [PH01] The system must be able to accept a voltage input between 9.6V 16.5V.
- **[PH02]** The system must be able to operate with the electrical noise generated by an automotive ignition system.
- **[PH03]** The system must be able to operate with the noise generated by an automotive power system.
- **[PH04]** The system must not consume more than 100 mA while vehicle is operational, and 3 mA (Avg.) while the vehicle is not in operation

4.2 Operational Environment

- **(PH11)** The system must operate in ambient temperatures ranging from –50°C to 85°C
- **[PH12]** The CCU/IONs must operate in environments with moderate moisture.
- **[PH13]** The CCU/IONs must operate in environments with vibration.

4.3 Dimensional

[PH21] The CCU must not exceed the following maximum dimensions:

Maximum Width	15 cm
Maximum Height	5 cm
Maximum Depth	15 cm

[PH22] The IONs must not exceed the following maximum dimensions:

Maximum Width	10 cm
Maximum Height	3 cm

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5 Hardware Requirements

These are specific hardware requirements that the engineers have identified. These must be met in order for higher-level system requirements to be met.

5.1 Central Control Unit (CCU)

[HW01] The CCU must be powered by an external power source. (1)

- **[HW02]** The CCU must be powered by an onboard power source. (2,3)
- **[HW03]** The CCU microcontroller must be programmed off board. (1)
- **[HW04]** The CCU microcontroller must be programmable through in circuit serial programming (ICSP). (3)
- **[HW05]** The CCU must adhere to TTL standard logic levels [3]. (1,2,3)
- **[HW06]** The CCU must provide sufficient output current drive capability to drive the bus. (1,2,3)
- **[HW07]** The CCU must provide large input resistance at its inputs. (1,2,3)

5.2 Input / Output Nodes (IONs)

[HW11] The IONs must be powered by an external power supply. (1)
[HW12] The IONs must be powered by a power source on the CCU, transmitted over the bus. (2,3)
[HW13] The ION channels must be configurable by user as input or output. (1,2,3)
[HW14] The IONs must adhere to TTL standard logic levels [3]. (1,2,3)
[HW15] The ION input channels must provide sufficient current drive capability to drive the bus. (1,2,3)
[HW16] The ION output channels must provide sufficient current drive capability to drive external circuitry. (1,2,3)

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- [HW17] The IONs must provide large input resistance at its inputs. (1,2,3)
- **[HW18]** The IONs must provide low on resistance. (1,2,3)

5.3 Unified Bus

- **[HW21]** The Bus must be a closed loop to provide double wiring redundancy. (2,3)
- **[HW22]** The Bus data line must contain short circuit protection circuitry. (2,3)
- **[HW23]** The Bus must be made of minimum 24 AWG multi-stranded wire. (1,2,3)
- **[HW24]** The Bus must contain some shielding to minimize interference. (1,2,3)
- **[HW25]** The Bus must be able to handle maximum current drive capacity of input channel regardless of the number of output channels. (3)

5.4 System Diagnostic Unit (SDU)

- **[HW31]** The SDU must be sufficiently fast to capture all data channels. (3)
- **[HW32]** The SDU must be powered by a power source on the CCU, transmitted over the bus. (3)
- **[HW33]** The SDU must be compatible with a PC parallel port interface [4]. (3)





These are software requirements that must be meet in order to ensure compliance with the system requirements. They will also ensure efficient and reliable operation of the system.

- **[SW01]** The CCU act as the bus master, in accordance with the bus protocol as defined in [2]. (1,2,3)
- **[SW02]** The SW must meet the system performance requirements as defined in System Requirements. (2,3)
- **[SW03]** The SW must prioritize between different channels, and ensure that high-priority channels are guaranteed a minimum refresh rate. (2,3)
- **[SW04]** The SW must maintain a status table for all channels. Upon startup, it will scan all channels to determine those that are active, and then operate the bus using only those channels to ensure the bus is always used as efficiently as possible. (2,3)
- **[SW05]** The SW must have a power-saving mode so as to avoid draining the car's battery when the vehicle is not in operation. While in this mode, the frequency of updates will be reduced, and most channels will not be operational at all. (2,3)
- **[SW06]** The SW must compile performance statistics and store these values for retrieval and analysis via the SDU. (3)
- **[SW07]** The SW must be able to detect errors on the bus, such as transmit collisions, and take appropriate action to correct. In most cases, this would involve deactivating the associated channel. (3)
- **[SW08]** The SW must allow for changing of all system variables via the SDU. This includes changing priority of channels and deactivating particular channels. (3)

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7 Regulatory & Safety Requirements

As this system is to be implemented in automobiles, and perhaps even aircraft, there are naturally a number of safety requirements that must be met to ensure that a failure of the DC-1i system would not jeopardize human lives. For the same reason, there are a number of regulatory requirements that must be passed before the DC-1i can be deployed.

- [RS01] The DC-1i system must meet the regulatory requirements defined by the US DOT (Department Of Transportation) and CSA (Canadian Standards Association). (3)
- [RS02] The DC-1i system must conform to the specifications defined in <u>C22.2</u> <u>NO. 203.1-94 (R1999):</u> Manufactured Wiring Products. (3)
- [RS03] The DC-1i system must conform to the specifications defined in <u>C22.2</u> <u>NO. 0.3-01:</u> Test Methods for Electrical Wires and Cables. (3)
- **[RS04]** The DC-1i system must have back-up provisions in the event of system failure. These provisions must be seamless so that the user is not subject to any period of instability. (2, 3)
- **[RS05]** The DC-1i system must have special provisions for nodes controlling safety (and other critical) functions of the vehicle (including but not limited to: the braking system, airbags, and headlights). (2,3)

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8 Conclusion

This document has outlined the functional requirements for the first three stages of prototyping the DC-1i. Based on these specifications, we will continue to develop our technology.

We are committed to meet the specifications for ENG0 (1) and ENG1 (2) by December 10, 2001. In addition, we will work to include as many features of ENG2 (3) as time permits. This document will provide us with a clear path to the completion our project.

Our proposal has been well planned and researched. Our goals are now clearly defined. Our team has proven leadership, extensive technical experience as well as the motivation and funding to meet our commitments.

DC Integration Innovations is poised to revolutionize DC wiring forever.



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9 References

- Jacques Vaisey frequency considerations
- Patrick Leung microprocessing requirements
- Fred Heep component selection, component sourcing
- Coleman Cable, <u>www.colemancable.com</u>
- Digikey Canada, <u>www.digikey.ca</u>
- Maxim Integrated Products, Sunnyvale, CA

10 Technical Appendices

TTL Standard Logic Levels http://www.twysted-pair.com/74xx.htm

Interfacing the Standard Parallel Port http://www.beyondlogic.org/spp/parallel.pdf

