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October 27th, 2003

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, British Columbia
V5A 1S6

Re: ENSC 340 Design Specification for a Small Heart EKG

Dear Dr. Rawicz:

Attached with this letter is the *Design Specification for a Small Heart EKG* which is previously described in the proposal. We are developing a Small Heart EKG that will record electrical signals from a heart's surface to analyze irregular heart pulses in infants due to arrhythmias.

Avrio Medical Inc. consists of six experienced and hard working fourth-year and fifth-year engineering students who love to incorporate knowledge to aid people: Jeff Chang, Eric Chow, George Kwei, Seddrak Luu, Joe Ma and Kenny Pak. Please contact us if there are any questions or concerns via email, ensc340-wireless@sfu.ca or by phone through Seddrak Luu at 604-719-5929. Thank you.

Sincerely,

Seddrak Luu

Seddrak Luu
Chief Executive Officer
Avrio Medical Inc.

Enclosure: *ENSC 340 Design Specification for a Small Heart EKG*

Design Specification for a Small Heart EKG

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School of Engineering Science
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Date:

October 27th, 2003

Executive Summary

Open heart surgery that corrects congenital heart disease found in new born children can result in a series of complications. According to the BC Children's Hospital, one in ten children who have open heart surgery will encounter some form of medical complication. One of the more severe, sometimes lethal, complications is an arrhythmia unique to children known as Junctional Ectopic Tachycardia (JET). These young patients will enter a phase where they have an irregular rhythmic beating of their heart, leading to potentially lethal complications.

Hospitals may charge up to twenty thousand dollars per day in the Intensive Care Unit (ICU) and patients of JET may need to stay in excess of twenty days. More serious JET symptoms will lead to almost immediate death. As a result, there is a need for a system that will obtain electrical signals from the heart surface in a cost efficient way. These signals can then be analyzed by cardiologists to further aid the study of JET towards the ultimate goal of understanding why such irregular rhythmic beatings of the heart occur.

Avrio Medical Inc. (AMI) will produce a reliable high resolution cardiac mapping and analysis system, the *Avrio Small Heart EKG*. In this task, we are committed to achieve and reach international standards. Four phases are involved with the development of the product: the signal retrieval phase, the signal transmission phase, the signal processing stage and the signal analysis stage.

To ensure the reliability of our product, an exclusive test plan is designed with Food and Drug Association (FDA) and international standards in mind. In addition, two sets of internal design standards will be met. The first standard will enable us to accomplish the basic requirements of each of the four phases. These include retrieving a signal in the micro-volt range, isolating the electrical heart signals from extraneous noise, and to safely transmit the electrical heart signals to a monitor display. The second standard is to reduce signal distortion by keeping the number of wires connecting each phase to a minimal. The projected goal and timeline for the first set of standards will be achieved by mid-November, while the second set of standards will follow and be achieved by mid-December.

Table of Contents

List of Tables and Figures

Abbreviations

AAMI: Association for the Advancement of Medical Instrument
A/D: Analog to Digital
AMI: Avrio Medical Inc.
ANSI: American National Standard Institute
ASH: Asymmetric Septal Hypertrophy
AV: atrioventricular
BCRI: British Columbia Research Institute
CSA: Canadian Standards Associations
DAQ: Data Acquisition
EKG: Electrocardiogram
FDA: Food and Drug Association
IEC: International Electrotechnical Commission
IEEE: Institute of Electrical and Electronics Engineers
JET : Junctional ectopic tachycardia
SA: Sinoatrial
UL: Underwriters Laboratories, Inc.

1. Introduction

The *Avrio Small Heart EKG* is specifically designed to be used on small hearts, such as that of an infant. It should be noted, however, that prototype testing will be performed on the heart of rabbits. The *Avrio Small Heart EKG* uses custom built electrodes to effectively pick up weak electrical signals from a heart surface, and display an amplified, filtered, and analyzed version of these signals on a computer. Currently, the *Avrio Small Heart EKG* will be most widely used in a research setting to aid cardiologists understand arrhythmias in infants.

The system will be developed in 3 phases, signal retrieval, signal transmission, and signal processing/analysis. Each phase is an essential part of the complete design, and will be tested carefully to ensure the accuracy and reliability of the system.

The ultimate goal for Avrio Medical Inc. (AMI) is to develop a high resolution cardiac mapping system to detect the JET arrhythmias.

1.1 Intended Audience

This document is intended to be a design guideline for engineers within AMI. Its purpose serves as ensuring that the product developed by AMI meets the specified requirements. Marketing will use this document to arrange sales strategies. Any descriptions mentioned in this document will be protected as AMI's intellectual property.

1.2 Scope

This document describes the design specifications that must be met by the *Avrio Small Heart EKG* system. It explains how the product will be designed to meet all the functional requirements as described in the Functional Specification. It should be noted that the design specifications apply only to the prototype system.

2. System Overview

Figure 1 shows a system overview of the *Avrio Small Heart EKG*. The natural electrical signals of a heart propagated from the top of the heart to the bottom.

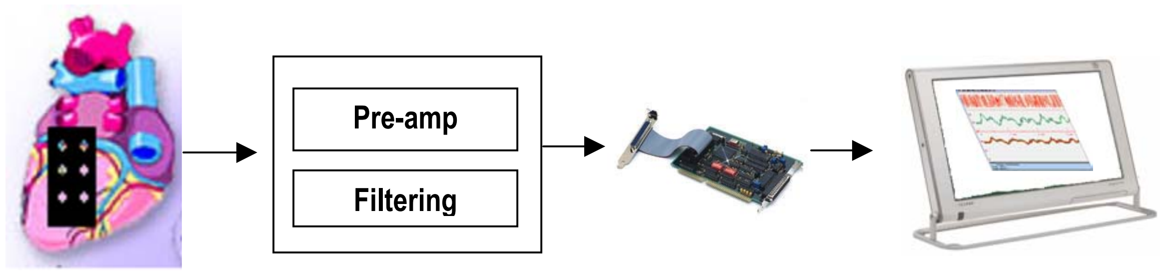


Figure 1: General Components of the Small Heart EKG

To collect and record the electrical heart signals, a 1.0cm x 1.5cm (8-pin/channel) electrode array grid will be placed onto the surface of the isolated rabbit heart. This electrode array will follow and record the intensity of the electrical signal propagation traversing the heart.

The electrode array will relay the heart's electrical signals to the Preamplifier and Filtering Module (PFM). The PFM will be responsible for increasing the signal strength and cleaning up any noise present.

Next, with a clean amplified signal, the rabbit heart's electrical information will be sent to a Digital Data Acquisition (DAQ) System. The DAQ will be responsible for converting the analog signal to a digital medium and performing all the necessary signal processing. The digital signal will be run through a set of in house developed analysis programs under the Labview program on the PC platform which will analyze the spectral patterns to diagnose the causes which cause JET syndrome.

Finally, a Data Display Unit will output all the recorded and analyzed data into an easily interpretable graphical display.

Figure 2 shows the flow chart for *Avrio Small Heart EKG.*

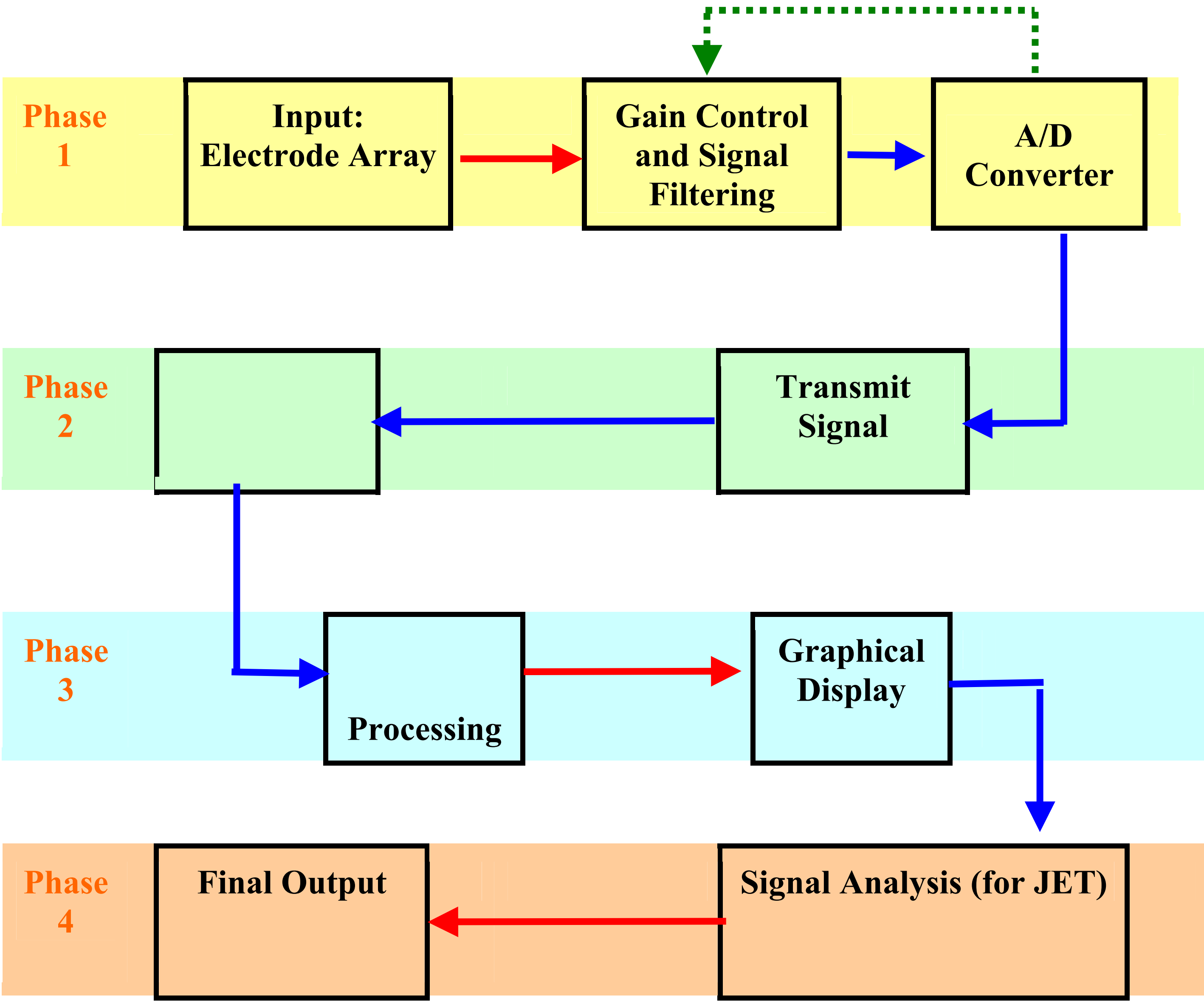
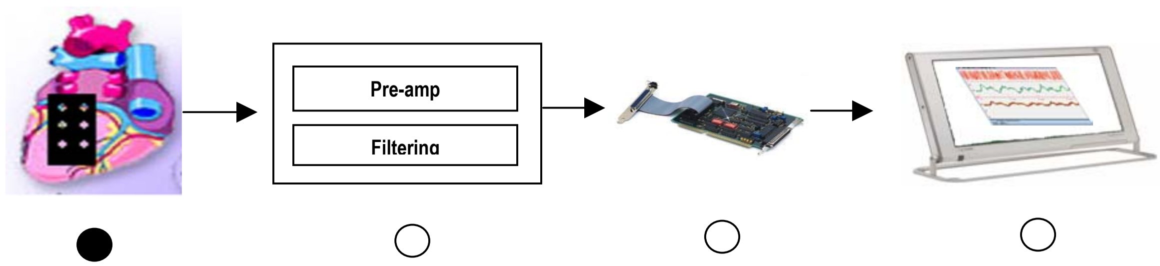


Figure 2: System Flow Chart

3. Small Heart EKG System

3.1 Electrodes Unit



The *Avrio Small Heart EKG* will be using a collection point electrodes forming an electrode array. These point electrodes are platinum wires, which are insulated with Teflon to avoid corruption of signals between wires. As shown in figure 3, the whole electrode unit consists of an upper block and a lower block with 8 holes. These holes are for the platinum wires to go through. Each hole represents a platinum wire going through, and is a point electrode.

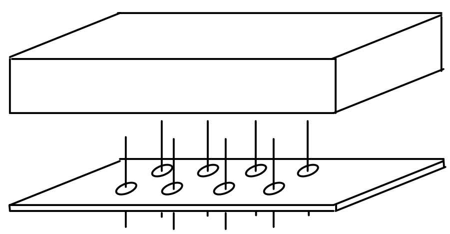


Figure 3: The Upper and Lower Layer of the Electrode Unit

The lower block is made of strong flexible and stretchable plastic sheet while the upper block is molded into the shape shown below from plastic wax material. Both plastic materials have no conductivity to avoid distortion of signals between the wires and from outside source. Accuracy is important in these electrodes as they are used in medical research. The following figure 4 shows the plasticity. The yield stress of the plastic is approximately 44.8-58.6 Mpa.

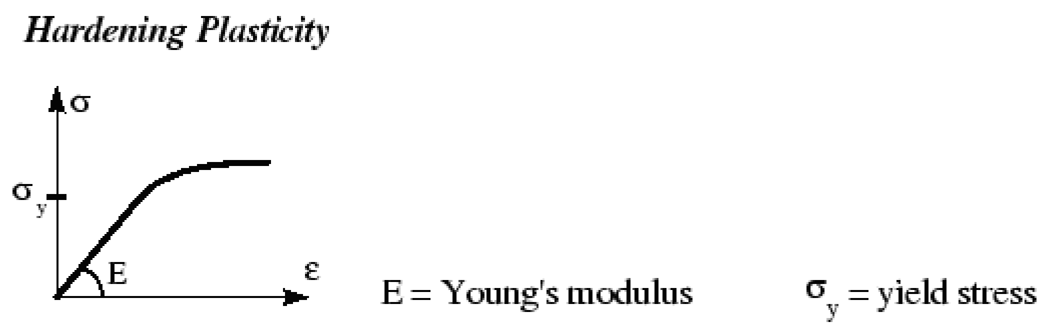


Figure 4: Hardening Plasticity Curve

For the finished prototype of the electrodes, as shown in figure 5, the upper block and the lower block will join and the platinum wires will be sandwiched in between with platinum wires protruding from the lower layer. The platinum wires will be in direct contact with the heart and will be held in place by medical tape. Medical tape is carefully placed at the side of the electrode array to provide maximum hold without interfering with the operation of the electrodes as seen in figure 5.

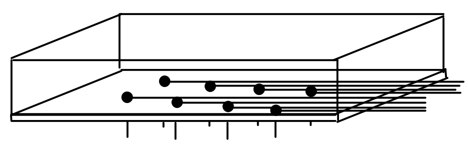


Figure 5: Side View of the Electrode Unit

Figure 6 provides a bottom view of the electrode unit.

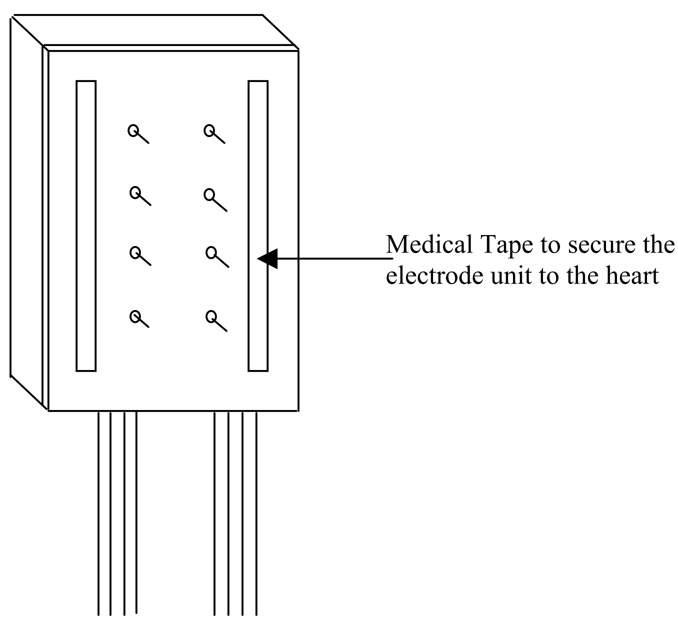


Figure 6: Bottom View of the Electrode Unit

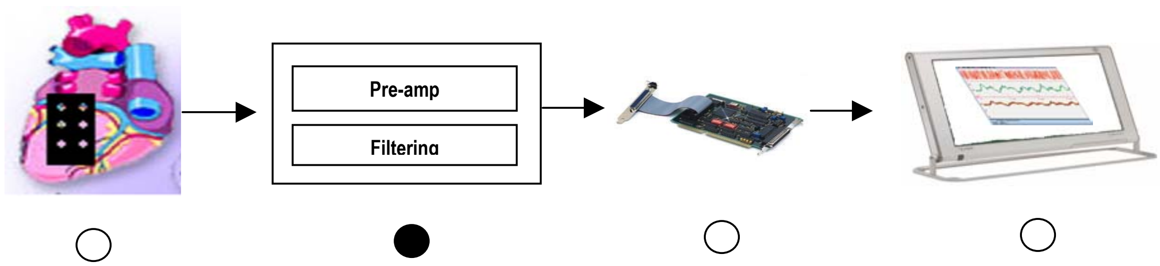
The shape of the electrode is to be designed as a rectangular shape much like what is shown in figure 6. The rectangular shape is chosen for the electrode since the area of the heart of interest, between AV and SA node, is roughly in a rectangular shape. The size of the electrode would be roughly around 1cm width by 1.5 cm length, and with a thickness of 5mm. Inter-electrode distance would be around at least 4 mm to ensure that there would be no contact between platinum wires and inter-electrode interference kept to a minimum.

The construction of the electrode array would be a challenging task since the electrode is required on such miniature scale. Without any tools suitable in the machine shop for such a small scale, the construction of the electrode array would rely on our hands and hand tools. Thus, the electrode array would appear to be less refined than if it were made with machine tools.

The electrode array requires a total of 8 platinum wires of 5 cm long. 5mm of insulation at both edges of each wire should be sanded off for contact to the heart and the connection to the pre-amp. A piece of plastic of size 1cm X 1.5cm is cut for the bottom cover. The first hole at the top left hand corner should be 3mm from the side edge of the plastic and 4mm from the top edge of the plastic. The second hole should be at 2mm to the right at parallel distance of the first hole and 3 mm from the other edge of the plastic. The third hole should be 2mm directly under first hole. The fourth hole should be 2 mm directly under the second hole. Repeat this process until all 8 holes are drilled evenly in the lower part.

String the platinum wires through the hole, but keeping only the 5mm non-insulated part of the wires outside the hole. Place all 8 wires into the each respected hole. Super glue the platinum wires to the plastic. Using cardboard, create a rectangular shaped perimeter around the plastic and glue it to the plastic. This will serve as a mold. Pour melted wax or plastic into the mold to create top of the cover. Cover the wax with appropriate size of cardboard.

3.2 Preamplifier and Filter Module (PFM) Unit



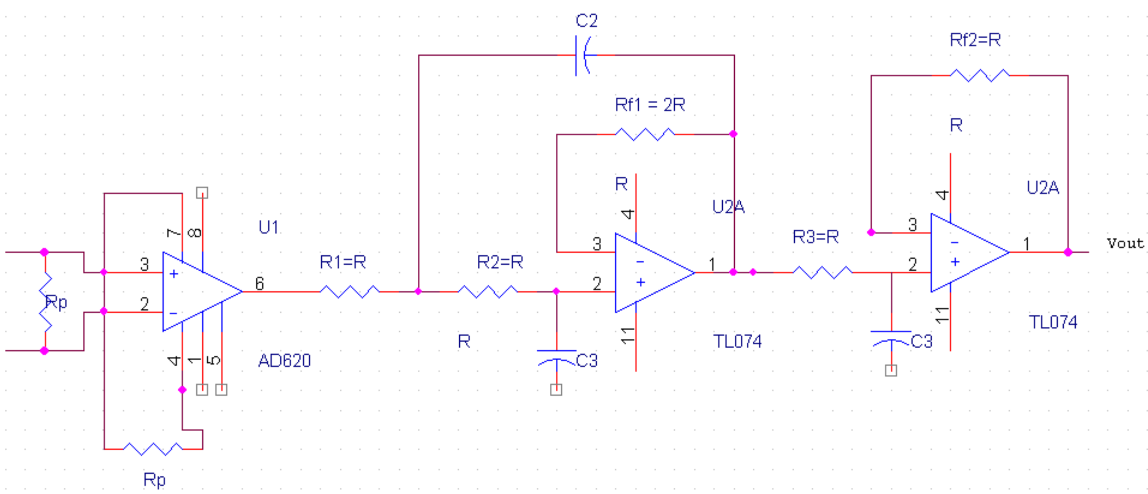


Figure 7: Schematics of Noise Reject, Amplification and Filtering Circuits

Figure 7 shows the schematics of the circuitry for noise rejection, amplification and filtering. A breakdown explanation is followed.

3.2.1 Noise Rejection and Amplification

To make proper use of our acquired signals, we use differential amplification to clean up and boost our signals. We implement the AD620 instrumentation amplifier which uses the common-mode noise rejection technique while giving us the ability to adjust output gains up to about 10,000 times.

The gain of the AD620 can be described by the following manufacturer's specification on the gain which is given below.

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

Also, the AD620 was a good choice of circuitry because of its reliable variable gains at low frequencies. We can safely obtain 1000 times gain within the range of 1-100 Hz which is well within the signal frequencies which we are obtaining from our biological specimen. This is shown in figure 8.

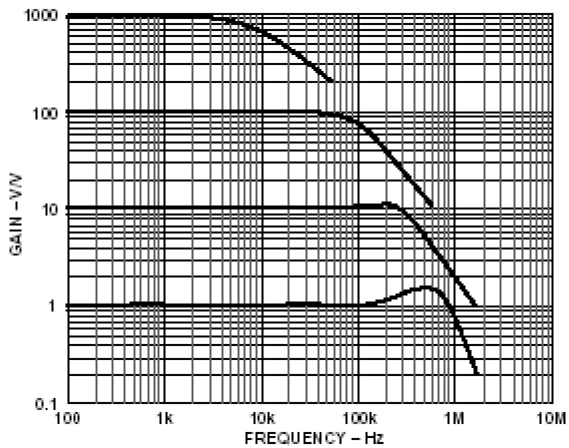


Figure 8: Gain for AD620

Below, in figure 9, is a characterization of the Common Mode Noise Rejection according to the AD620's frequency response. In the frequency of about 5Hz the AD620 does a fine job of attenuating a large amount of the noise which we could be getting into our system. For sure we can get well above 100 dB noise attenuations given at least of 10 times gain of the signal. We are most likely going to use around 100 times gain to up our very small and weak heart pulse signal which according to the graph below will allow for more than 120 dB attenuation.

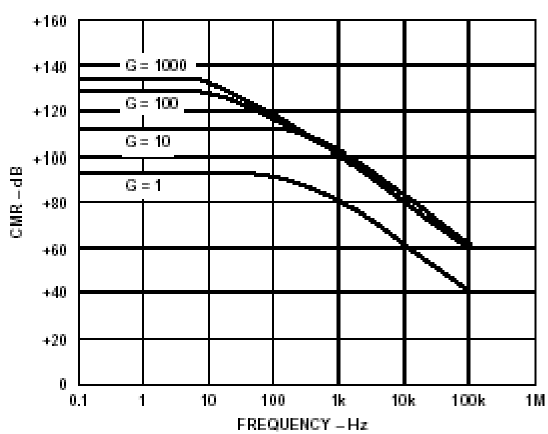


Figure 9: Characterization of the Common Mode Noise Rejection

Our electrodes feed in directly to one of the inputs on these AD620 amplifiers; the other input will be used for the reference electrode. This will then give us a relative difference between all the amplifiers/electrodes. We manually adjust the gain on the AD620 to provide an optimal signal output level given our portable 9V power supply. Detailed specification of AD620 is in Appendix A.

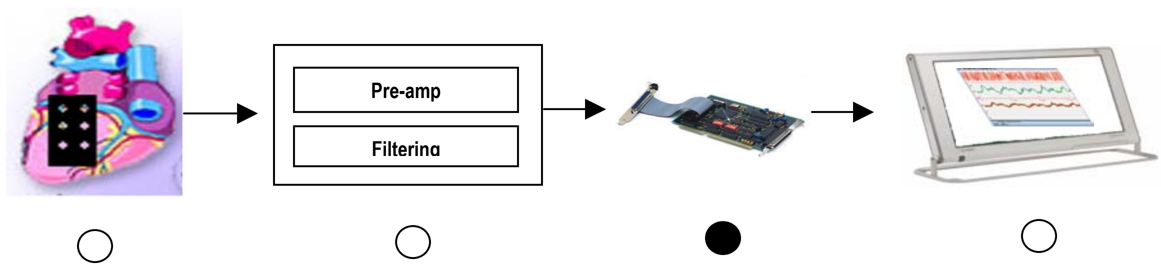
3.2.2 Signal Filtering

To remove the unwanted 60Hz standard electrical background noise we are using a third order low-pass filter with a -60dB per decade roll off. The filtering actually consists of two stages. The first stage contains a -20dB roll off in cascade with a second stage consisting of a -40dB roll of to get our desired sharp roll off. Considering that the major heart beat events we are targeting to observe are located around 5Hz, we are designing our roll off point at approximately 5Hz.

3.2.3 Power

In order to eliminate any possible interference from conventional power supplies, we use 9V batteries to power our circuits. The noise from large power supplies give us a large ‘humming’ noise which will be easily detected from our platinum tipped electrodes. Therefore, we connected two 9V batteries to provide us with a -9V to 9V power supply and an appropriate reference ground. This also aids us in the portability issue for our circuit making it much easier to place our device in convenient places and without hauling a large power supply around.

3.3 Data Acquisition – Analog to Digital Conversion



Once the electrical signals from the heart has been acquired, amplified, and filtered, the analog signals need to be digitized in order to be analyzed and displayed. For this to be done, we need two things:

1. An analog to digital conversion card. (Data Acquisition Card)
2. An input device to transfer the signals into (1)

3.3.1 Input Device

To feed the raw electrical signals into our DAQ card, we will need an adapter allowing the transfer of at least 9 separate channels; one for each electrode signal. We also need to ensure that the signals are not distorted during this transfer. For this task, we have chosen the BNC-2090 by National Instruments. The BNC-2090 has the following specifications which match our requirements:

National Instruments BNC-2090

- 22 BNC connectors for analog, digital, and timing signals
- 28 spring terminals for digital/timing signals
- Shielded, rack-mountable BNC adapter chassis
- Silk-screened component locations for passive signal conditioning

Figure 10: National Instrument Input Device BNC-2090

Through the rear of this input device are dual 68-pin connectors which we will use to transfer the signals to our DAQ card.

3.3.2 Connectors

We will be using BNC connectors to relay the electrical signals from the Preamp and Filtering Module to the BNC-2090 Input Device. Figure 11 shows the configuration of the connectors.

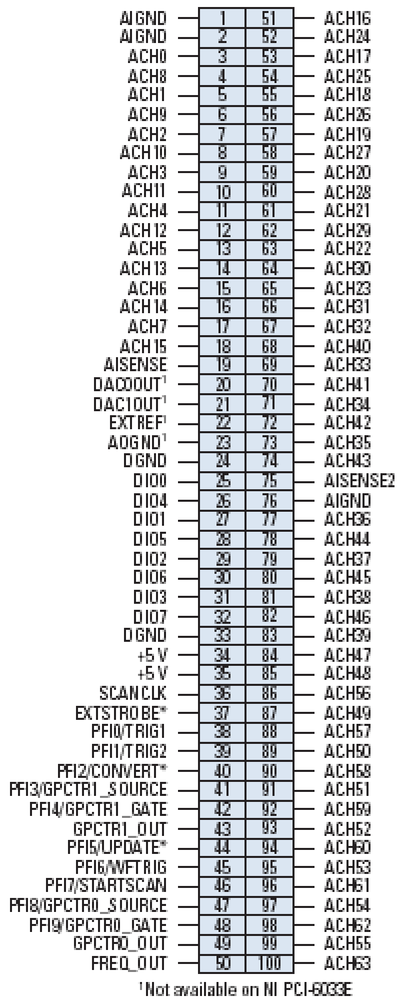


Figure 11: I/O Connector

3.3.3 Data Acquisition (DAQ) Card

The DAQ card once receiving the signals, converts them to digital information for further analysis at the computer. For our DAQ card, we need it to be able to take input of at least 9 single ended inputs, be PCI-Bus compatible, be able to take samples at a high rate for real-time signal analysis, and be Windows compatible. Considering the preceding criteria, we have chosen the NI AT-MIO-16E-10 by National Instruments. This DAQ card has the following specifications meeting our requirements:

- 100 kS/s, 12-bit resolution,
- 16 single-ended analog inputs
- Two 12-bit analog output channels
- 8 Input/0utput lines (5 V/TTL)
- two 24-bit counter/timers
- Digital triggering
- LabVIEW compatible
- Windows 2000/NT/Me/9x Operating System Compatible

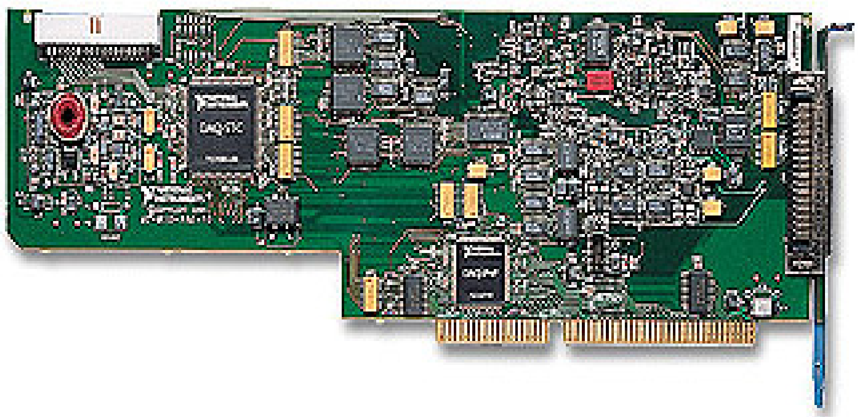


Figure 12: National Instruments AT-MIO-16E-10

Accuracy is also important in our design. The NI AT-MIO-16E-10 provides us with accurate output. Figure 13 shows the accuracy chart that is crucial in the design and figure 14 shows the hardware block diagram of the analog card.

Absolute Accuracy Nominal Range (V)		Relative Accuracy % of Reading		Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/°C)	Absolute Accuracy at Full Scale (mV)	Resolution (mV)	
Positive FS	Negative FS	24 Hrs	1 Year		Single Pt.	Averaged			Single Pt.	Averaged
10.0	-10.0	0.072	0.076	6.380	3.467	0.846	0.0010	14.826	5.729	1.114
5.0	-5.0	0.019	0.021	3.198	1.733	0.423	0.0005	4.6710	2.865	0.557
2.5	-2.5	0.072	0.076	1.608	0.867	0.211	0.0010	3.7190	1.432	0.278
1.0	-1.0	0.072	0.076	0.653	0.347	0.085	0.0010	1.4980	0.573	0.111
0.5	-0.5	0.072	0.076	0.335	0.173	0.042	0.0010	0.7570	0.286	0.056
0.25	-0.25	0.072	0.076	0.176	0.105	0.021	0.0010	0.3870	0.151	0.028
0.1	-0.1	0.072	0.076	0.081	0.061	0.008	0.0010	0.1650	0.074	0.011
0.05	-0.05	0.072	0.076	0.049	0.049	0.004	0.0010	0.0910	0.056	0.006
10.0	0.0	0.019	0.021	3.198	1.733	0.423	0.0005	5.7210	2.865	0.557
5.0	0.0	0.072	0.076	1.608	0.867	0.211	0.0010	5.6190	1.432	0.278
2.0	0.0	0.072	0.076	0.653	0.347	0.085	0.0010	2.2580	0.573	0.111
1.0	0.0	0.072	0.076	0.335	0.173	0.042	0.0010	1.1370	0.286	0.056
0.5	0.0	0.072	0.076	0.176	0.105	0.021	0.0010	0.5770	0.151	0.028
0.2	0.0	0.072	0.076	0.081	0.061	0.008	0.0010	0.2410	0.074	0.011
0.1	0.0	0.072	0.076	0.049	0.049	0.004	0.0010	0.1290	0.056	0.006

Note: Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature. One-year calibration interval recommended. The Absolute Accuracy at Full Scale calculations were performed for a maximum range input voltage (for example, 10 V for the ±10 V range) after one year, assuming 100 pt averaging of data. See overview on page 234 for an example calculation of this type.

Figure 13: Analog Input Accuracy Specifications

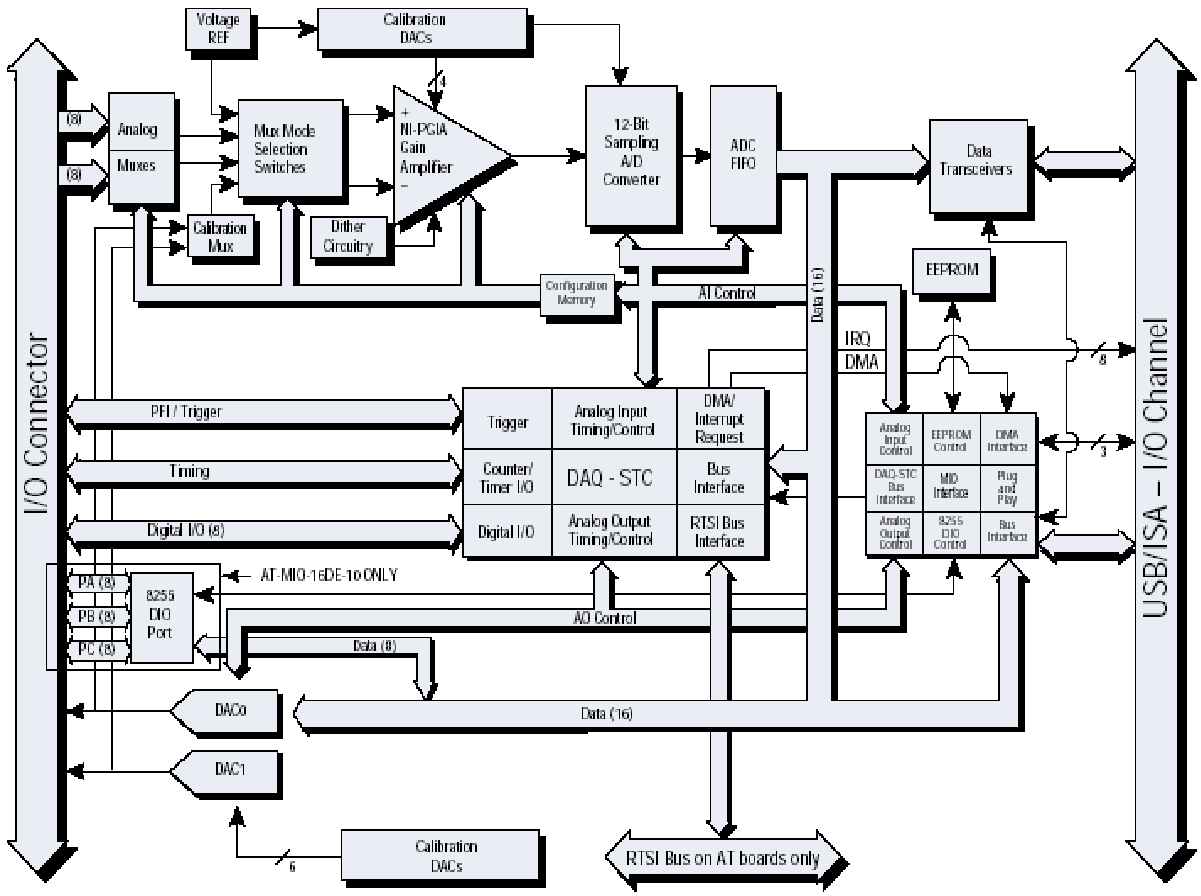
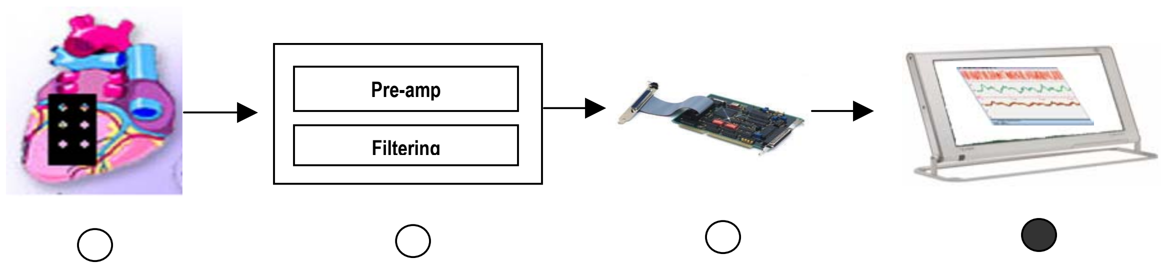


Figure 14: Hardware Block Diagram of National Instruments AT-MIO-16E-10

3.4 Data Display Unit



The goal of the software on the data display unit will be to display the electrical signal from the small heart transmitted through the electrodes. Figure 15 shows a high-level view of the program operation. The BNC-2090 data acquisition card, as described in previous section, acquires data and feeds the data into a displaying computer, on which the heart signal is display in LabView. Implementation of driver software is not necessary, as LabView already has built-in software interface and driver for the BNC-2090 data acquisition card. Therefore, we do not need to perform tasks such as signal conditioning and error checking. We assume that the existing driver software from National Instrument correctly acquires all data.

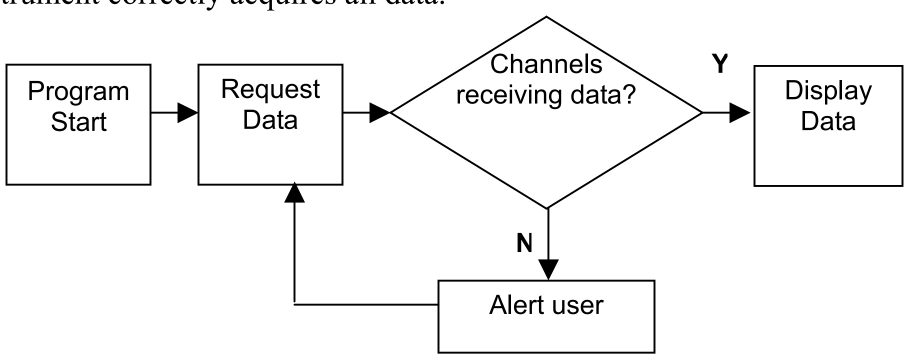


Figure 15: Block Diagram of Program Operation

The GUI will graphically display data received from the electrodes. Figure 16 shows a sample layout of the user interface. However, the layout of the final product may not be identical to the one presented.

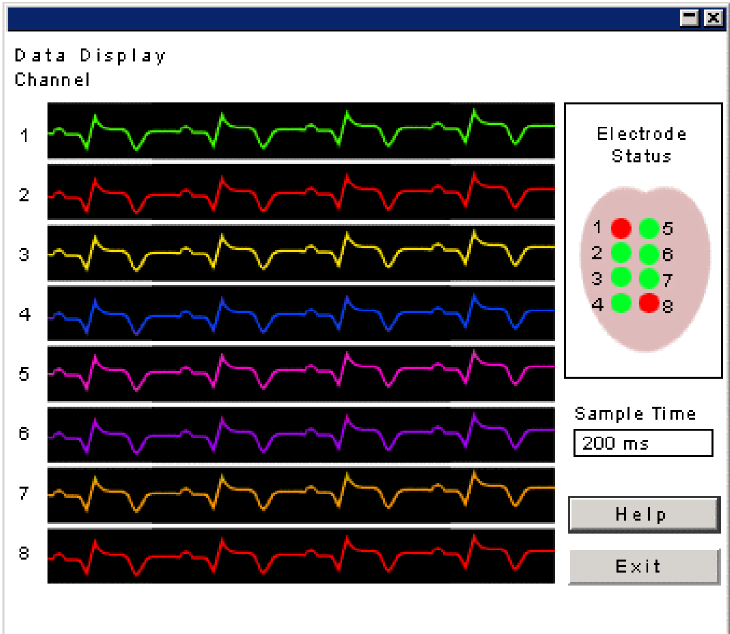


Figure 16: Layout of GUI

The GUI will consist of two buttons (exit and help), data display section, and electrodes status display section. To avoid confusion, data from all electrodes will be displayed in one window instead of in multiple windows. The GUI is built using GUI components in LabView.

3.4.1 Data Display Section

This section displays the incoming heart activity data from each electrode. Each channel is represented by a graph, on which the signal of one probe is displayed. All channels are displayed simultaneously. User can also specify sampling time (in millisecond). If time permits, we will create a mechanism through which the user can selectively view data acquired from each electrode.

3.4.2 Electrodes Status Section

The section list the electrodes detected by the system. The actual physical arrangement of the electrodes on the heart is also shown for ease of determining the working of each electrode. A green dot represents a connected electrode, and a red dot represents a disconnected electrode (indicated by no voltage input or no change in voltage input for a certain period of time)

3.4.3 Help and Exit Button

The help button provides access to an overview of the GUI and a FAQ section. Intended as a tutorial for new user of the software, the GUI overview is essentially a textual description of the various components in the GUI. The FAQ section will attempt to assist the user solving commonly encountered problems when operating the software by displaying possible causes and fixes.

When the Exit button is clicked, the software will close. Any data being monitored and displayed will be stopped and lost.

3.4.4 Data Recording

As mentioned in our functional specification, data recording is desired, but not a necessary component for our project. Due to time constraints experienced at this stage of the project, data recording may not be implemented by December. Nevertheless, the design specification of the data recording function is still being considered in this document.

The planned design of the data recording function is as follow. A button on the GUI labeled *Record* will opens a separate window, in which a list of check boxes that allow the user to choose which electrode data to record, as well as the filename of the file on which the user wish to record the data. At the bottom of this window, there will be two buttons labeled *OK* and *Cancel.* When the *OK* button is pressed the software will start recording voltage data coming from the electrodes onto ASCII files specified by the user. Upon clicking the *Cancel* button, the data recording window will close and the software will stop writing data into the ASCII text file.

4. System Test Plan

The *Avrio Small Heart EKG* is divided into three parts during the first phase of testing. The second phase of testing involves the improving of each individual parts and the examining of the whole system. The following sub-section describes these parts.

4.1 Testing Electrodes

- Nine electrodes are to be tested individually. One electrode is tested individually to ensure its workability while avoiding interference from the neighboring electrodes.
- Two electrodes are tested together, then four, eight, and finally all nine.
- Minimum distortion should be seen when increasing the number of electrodes used.

4.2 Testing Pre-Amplifiers and Filtering

- The pre-amp and filtering hardware will be constructed and tested in the lab using mock signals generated by a function generator to test its operation
- Signal is acquired and processed at the pre-amp and filtering module.
- The pre-amp and filtering module will first take in only 1 input signal at a time
- After it is verified that all electrode signals can be obtained with minimal noise and distortion, all nine electrode signals will be multiplexed into the pre-amp and filtering module.
- The signal is tested and that maximum gain is achieved without clamping the signal

4.3 Testing Analog Input Card

- A signal will feed into the card and observe whether the output is expected.
- Signal display is accompanied by LabView.

4.4 Software

- Test data with known output will be generated and processed by the display and analysis software algorithms

4.5 Total System Test on a Rabbit Heart

- All parts are connected into one system.
- The electrode grid and the electrodes is placed on the rabbit heart.
- The DAQ card is placed on the PCI slot of the computer.
- User then observes the heart signal at the different part of the heart for arrhythmia detection. Signal display is done by LabView.

5. Conclusion

This document contains the Design Specifications for the *EKG*. The Design Specification contains detailed description of the design for the cardiac mapping system. The building of the *Avrio Small Heart* EKG will be done in separate phases corresponding to the way proposed in the document. The Avrio Medical group members will be separate into mainly 2 parts and tackle two different phases at the same time. The Design Specification of the *Avrio Small Heart EKG* will be a prototype for the eventual *Avrio Infant JET Heart Monitor*.

6. Reference

AAMI Standards (http://www.aami.org)

Analog Device (http://analog.com)

Canadian Standards Associations (http://www.csa.ca)

Institute for Electrical and Electronics Engineers (http://www.ieee.org)

International Electrotechnical Commission (http://www.iec.ch)

National Instruments (http://ni.com)

Standard Council of Canada (http://www.scc.ca/standards/index_e.html)

Appendix A

AD 620 Detail Specification Sheet

ANALOG DEVICES

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES

EASY TO USE
Gain Set with One External Resistor
(Gain Range 1 to 1000)
Wide Power Supply Range (±2.3 V to ±18 V)
Higher Performance than Three Op Amp IA Designs
Available in 8-Lead DIP and SOIC Packaging
Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("B GRADE")
50 μV max, Input Offset Voltage
0.6 μV/°C max, Input Offset Drift
1.0 nA max, Input Bias Current
100 dB min Common-Mode Rejection Ratio (G = 10)

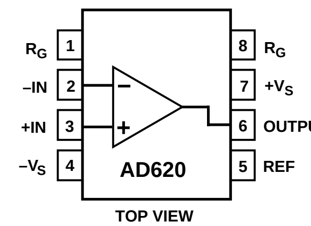
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
120 kHz Bandwidth (G = 100)
15 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
ECG and Medical Instrumentation
Transducer Interface
Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in-amp per channel.

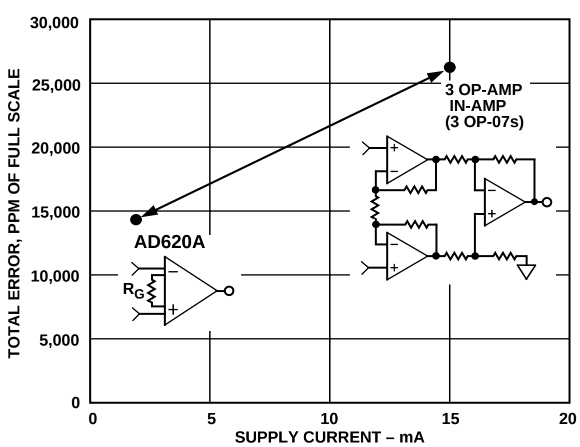


Figure 1. Three Op Amp IA Designs vs. AD620

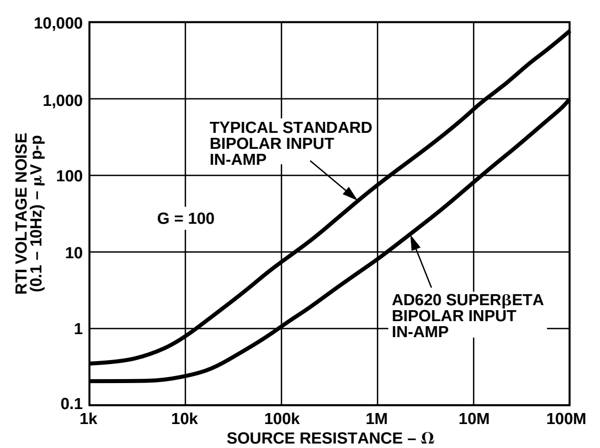


Figure 2. Total Voltage Noise vs. Source Resistance

REV. E

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AD620–SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = –10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature											
	G =1			10			10			10	ppm/°C
	Gain >1[2]			–50			–50			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
Over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ – 1.2	$-V_S$ + 1.9		$+V_S$ – 1.2	$-V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$-V_S$ + 2.1		$+V_S$ – 1.3	$-V_S$ + 2.1		$+V_S$ – 1.3	$-V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ – 1.4	$-V_S$ + 1.9		$+V_S$ – 1.4	$-V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$-V_S$ + 2.1		$+V_S$ – 1.4	$-V_S$ + 2.1		$+V_S$ – 1.4	$-V_S$ + 2.3		$+V_S$ – 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with I kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ, V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ – 1.4	$-V_S$ + 1.2		$+V_S$ – 1.4	$-V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

NOTES
[1]See Analog Devices military data sheet for 883B tested specifications.
[2]Does not include effects of external resistor R_G.
[3]One input grounded. G = 1.
[4]This is defined as the same supply range which is used to specify PSR.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] . . . . 650 mW
Input Voltage (Common Mode) . . . . ±V_S
Differential Input Voltage . . . . ±25 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range (Q) . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
  AD620 (A, B) . . . . –40°C to +85°C
  AD620 (S) . . . . –55°C to +125°C
Lead Temperature Range
  (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic Package: θ_{JA} = 95°C/W
8-Lead Cerdip Package: θ_{JA} = 110°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W

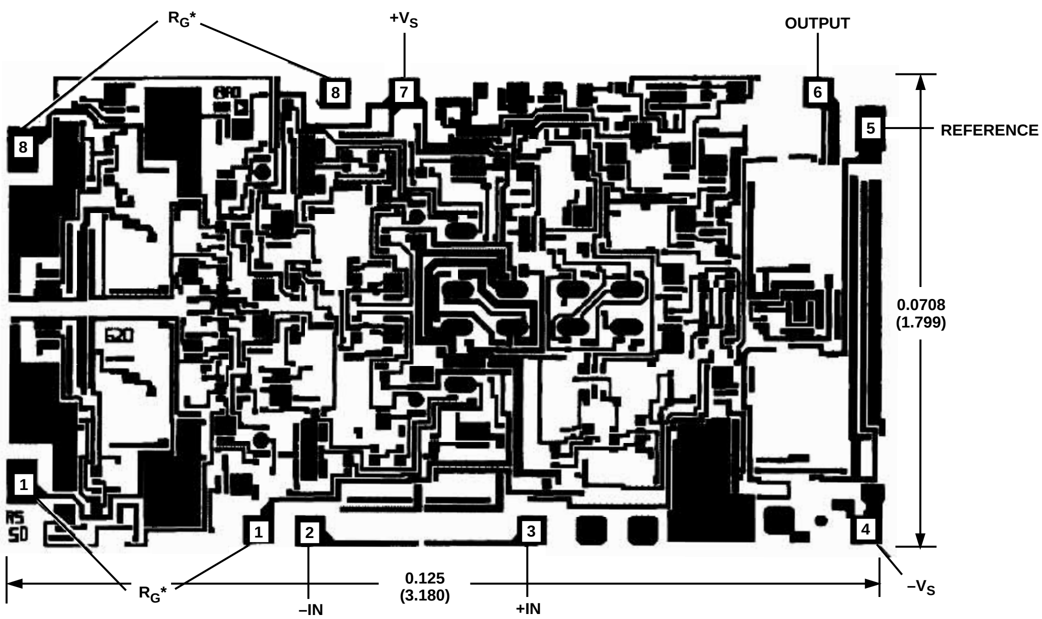
ORDERING GUIDE

Model	Temperature Ranges	Package Options*
AD620AN	–40°C to +85°C	N-8
AD620BN	–40°C to +85°C	N-8
AD620AR	–40°C to +85°C	SO-8
AD620AR-REEL	–40°C to +85°C	13" REEL
AD620AR-REEL7	–40°C to +85°C	7" REEL
AD620BR	–40°C to +85°C	SO-8
AD620BR-REEL	–40°C to +85°C	13" REEL
AD620BR-REEL7	–40°C to +85°C	7" REEL
AD620ACHIPS	–40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip; SO = Small Outline.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



*FOR CHIP APPLICATIONS: THE PADS 1R_G AND 8R_G MUST BE CONNECTED IN PARALLEL TO THE EXTERNAL GAIN REGISTER R_G. DO NOT CONNECT THEM IN SERIES TO R_G. FOR UNITY GAIN APPLICATIONS WHERE R_G IS NOT REQUIRED, THE PADS 1R_G MAY SIMPLY BE BONDED TOGETHER, AS WELL AS THE PADS 8R_G.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Characteristics (@ +25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted)

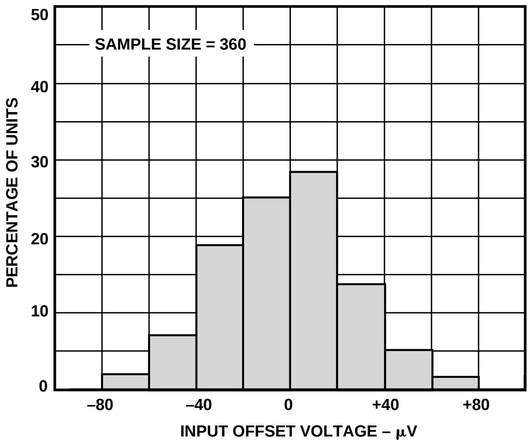


Figure 3. Typical Distribution of Input Offset Voltage

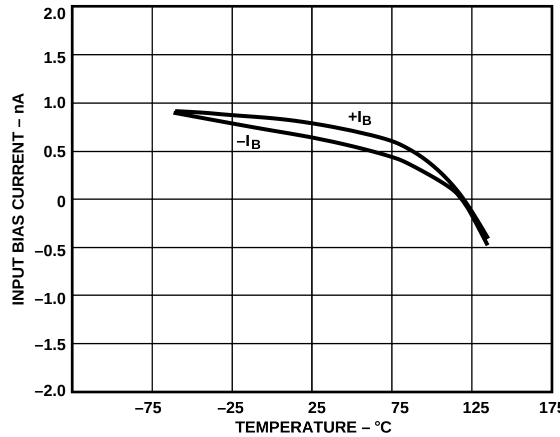


Figure 6. Input Bias Current vs. Temperature

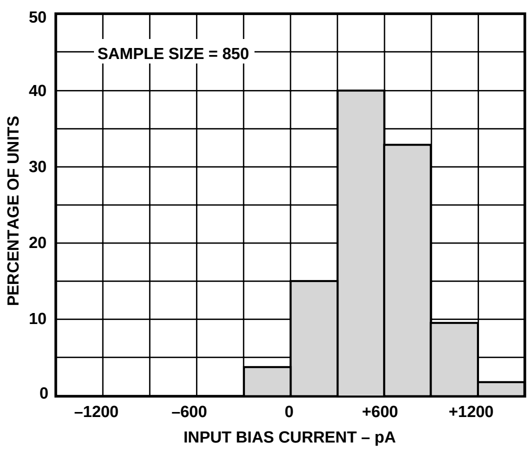


Figure 4. Typical Distribution of Input Bias Current

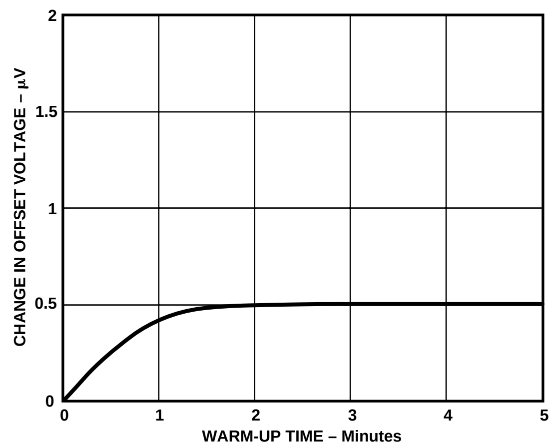


Figure 7. Change in Input Offset Voltage vs. Warm-Up Time

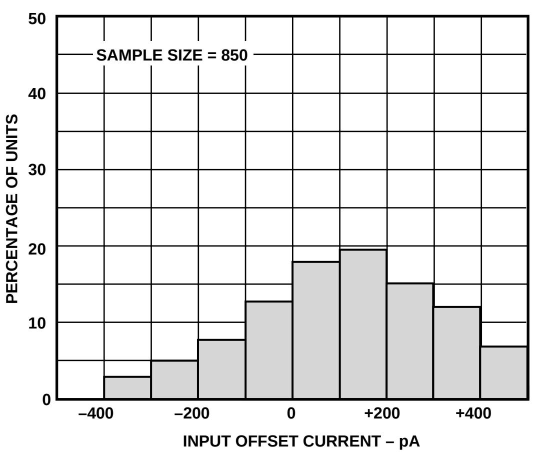


Figure 5. Typical Distribution of Input Offset Current

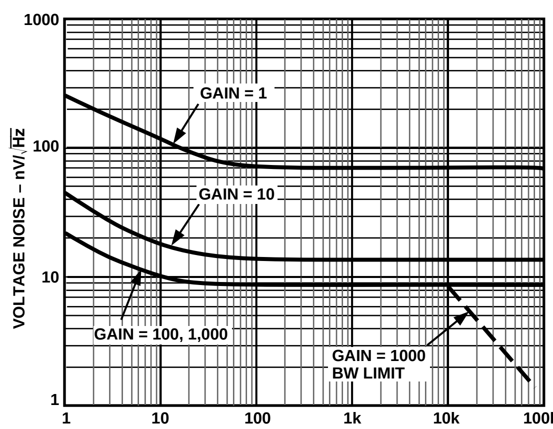


Figure 8. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

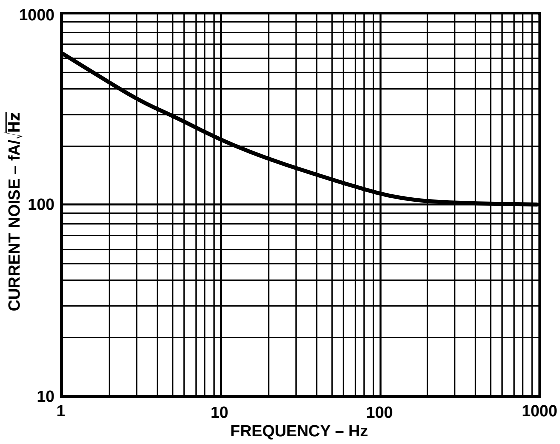


Figure 9. Current Noise Spectral Density vs. Frequency

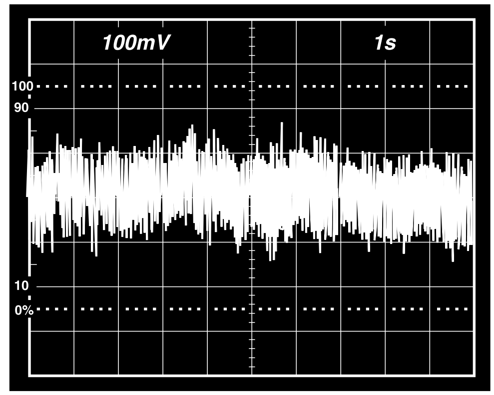


Figure 11. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

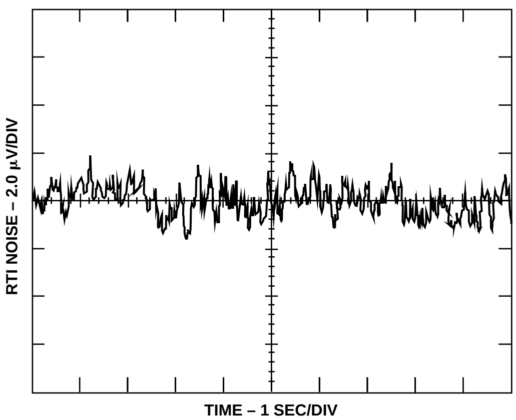


Figure 10a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

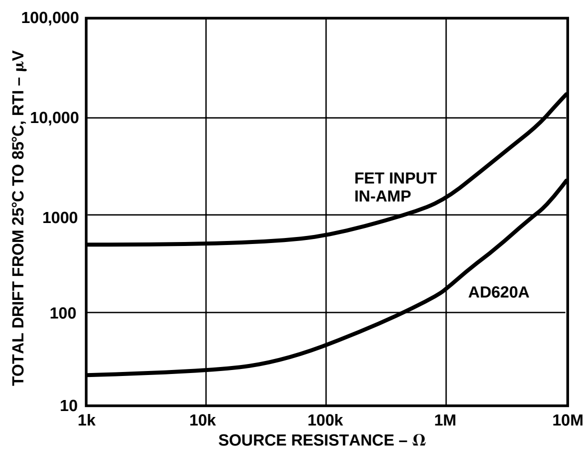


Figure 12. Total Drift vs. Source Resistance

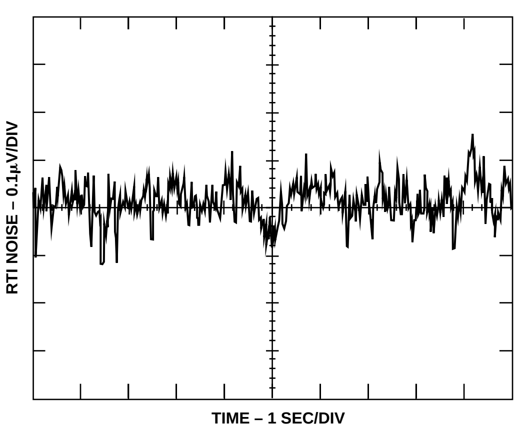


Figure 10b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

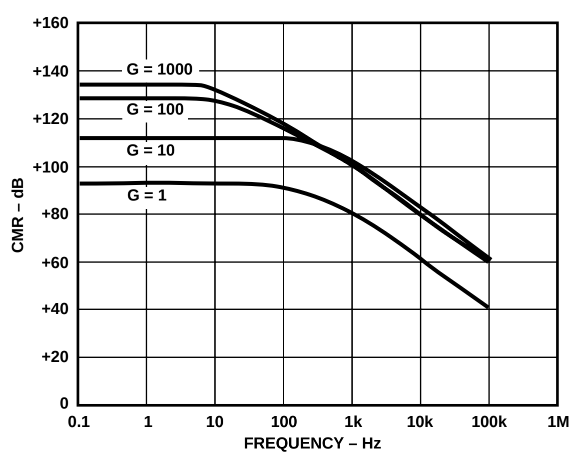


Figure 13. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

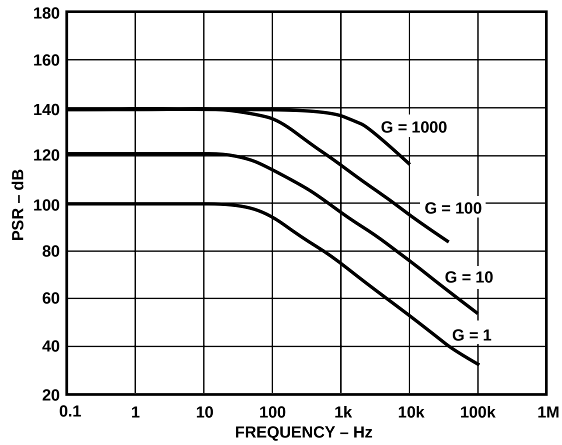


Figure 14. Positive PSR vs. Frequency, RTI (G = 1–1000)

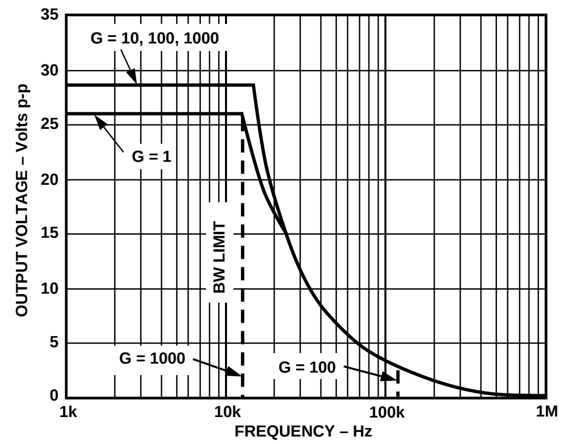


Figure 17. Large Signal Frequency Response

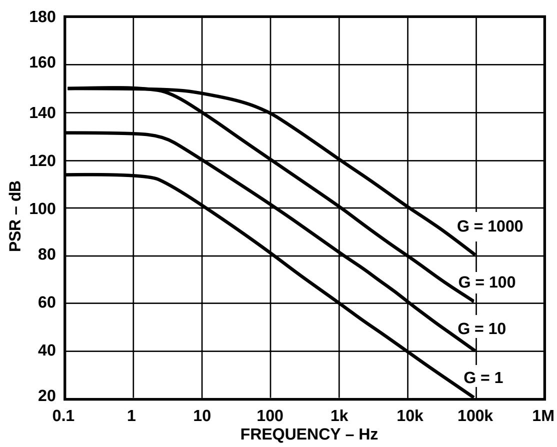


Figure 15. Negative PSR vs. Frequency, RTI (G = 1–1000)

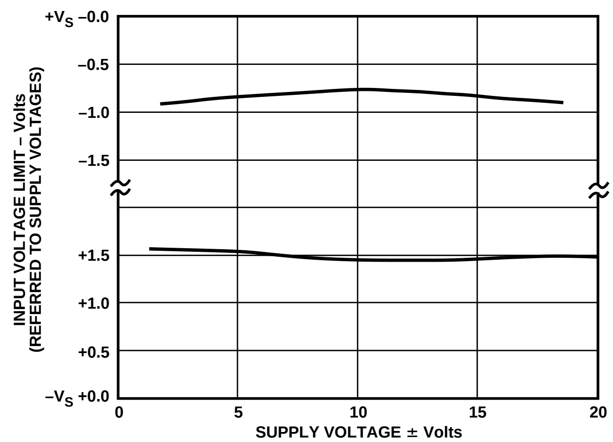


Figure 18. Input Voltage Range vs. Supply Voltage, G = 1

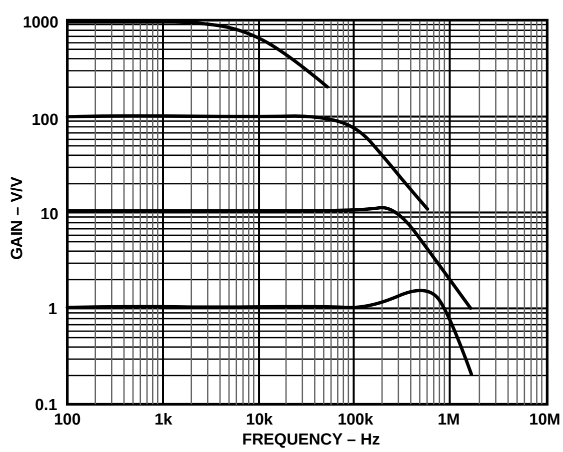


Figure 16. Gain vs. Frequency

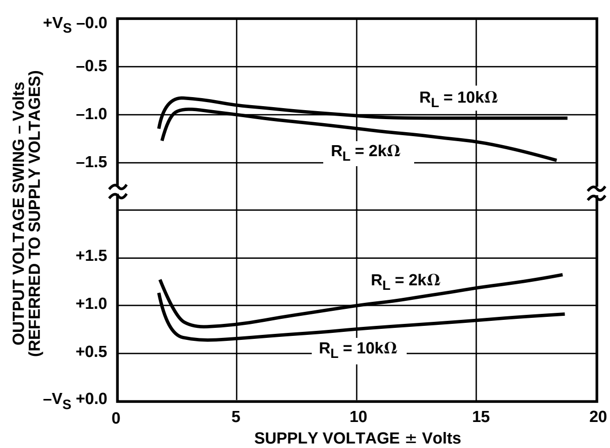


Figure 19. Output Voltage Swing vs. Supply Voltage, G = 10

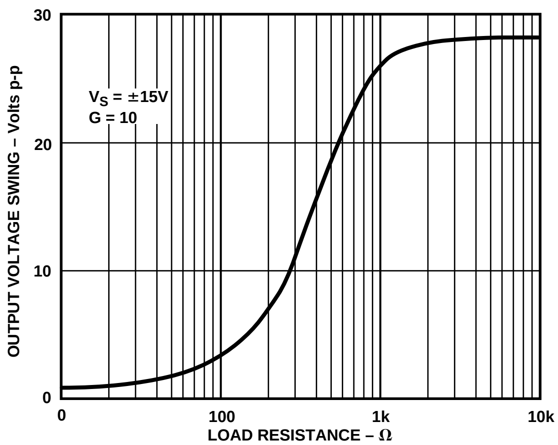


Figure 20. Output Voltage Swing vs. Load Resistance

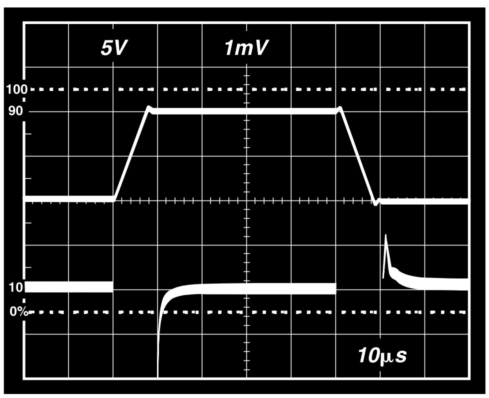


Figure 21. Large Signal Pulse Response and Settling Time G = 1 (0.5 mV = 0.01%)

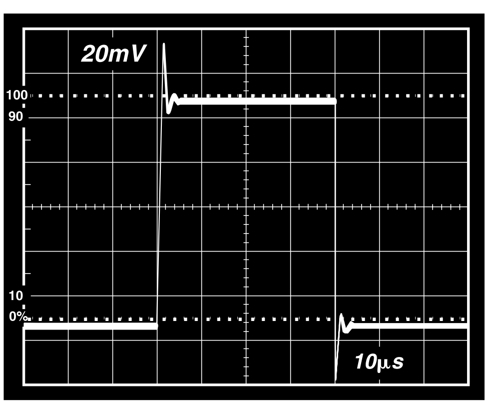


Figure 22. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

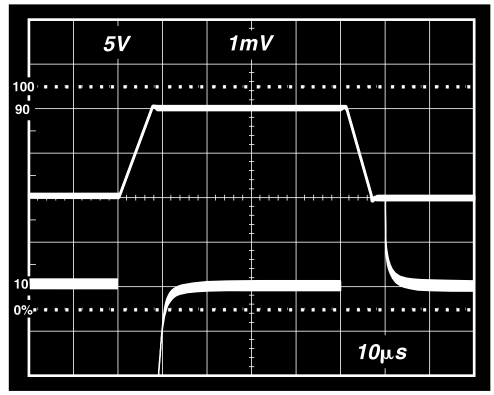


Figure 23. Large Signal Response and Settling Time, G = 10 (0.5 mV = 001%)

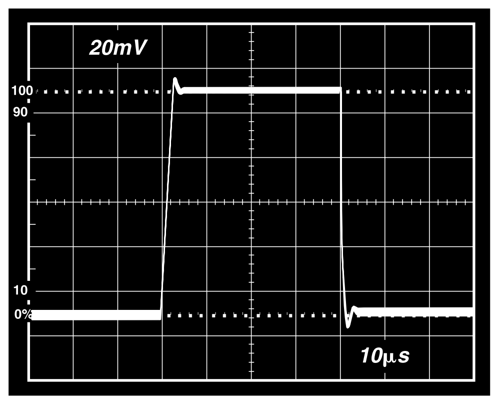


Figure 24. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

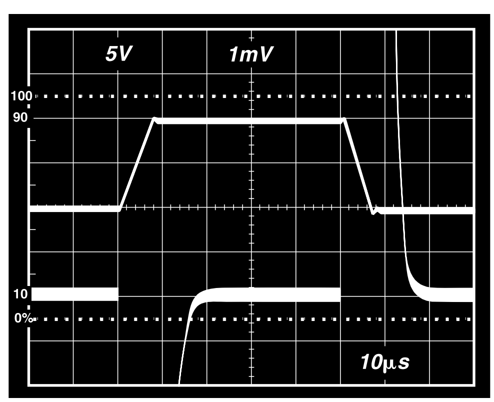


Figure 25. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

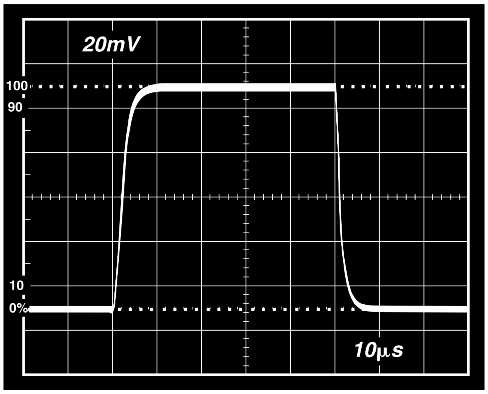


Figure 26. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

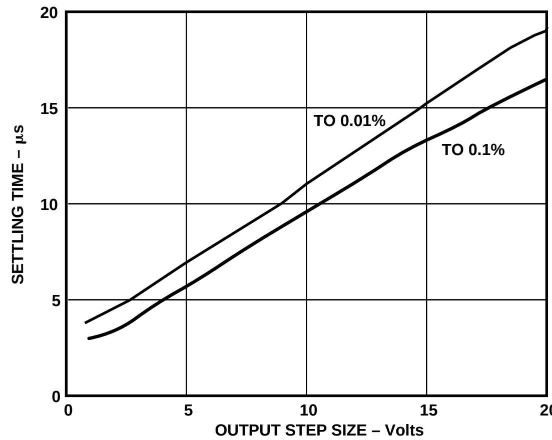


Figure 29. Settling Time vs. Step Size (G = 1)

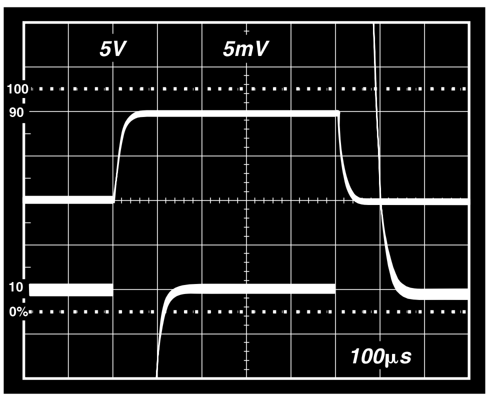


Figure 27. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

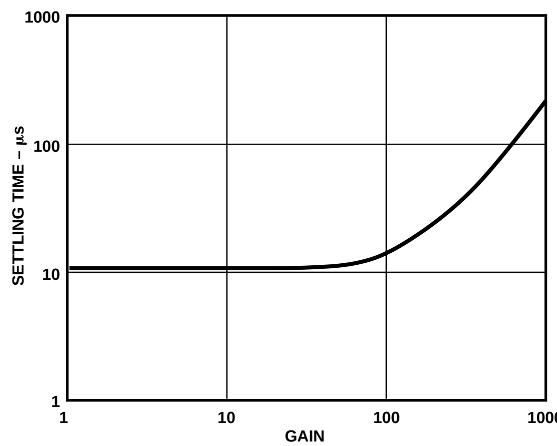


Figure 30. Settling Time to 0.01% vs. Gain, for a 10 V Step

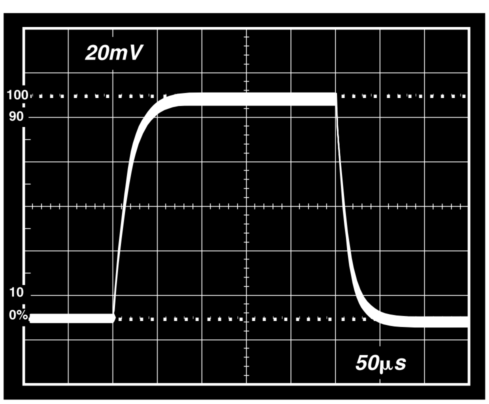


Figure 28. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

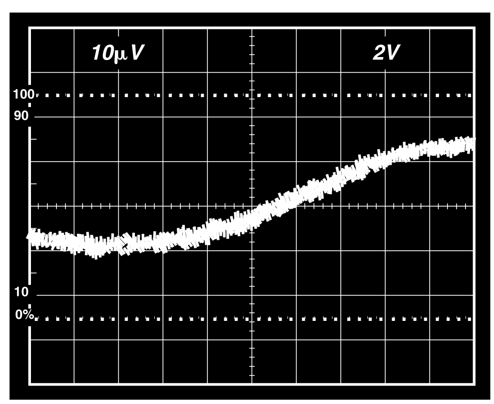


Figure 31a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 µV = 1 ppm)

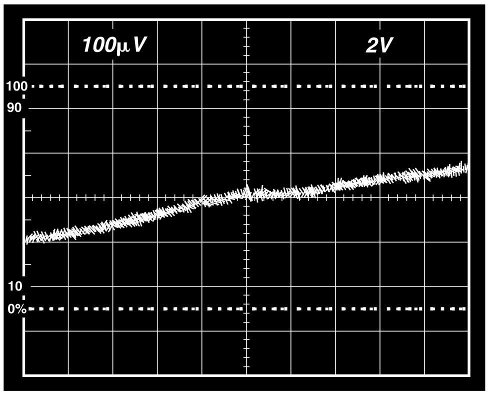


Figure 31b. Gain Nonlinearity, G = 100, R_L = 10 kΩ (100 µV = 10 ppm)

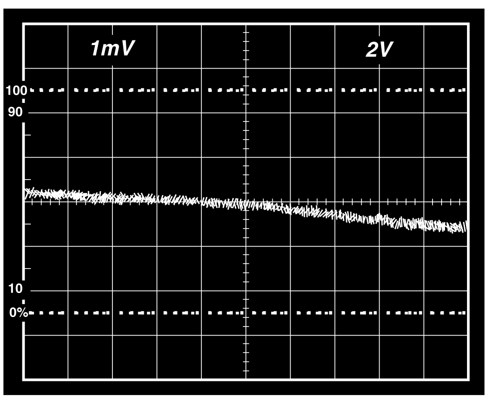


Figure 31c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ (1 mV = 100 ppm)

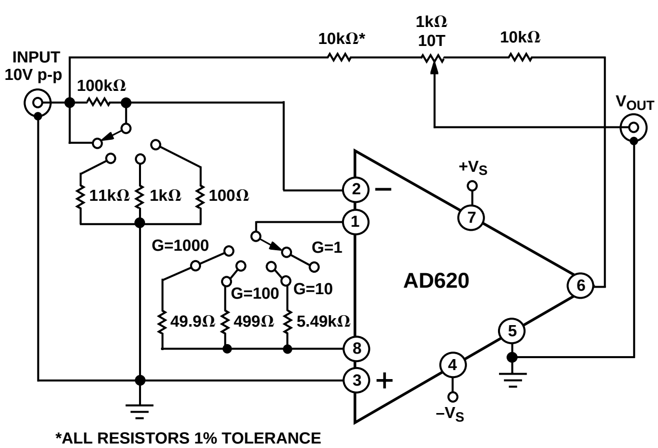


Figure 32. Settling Time Test Circuit

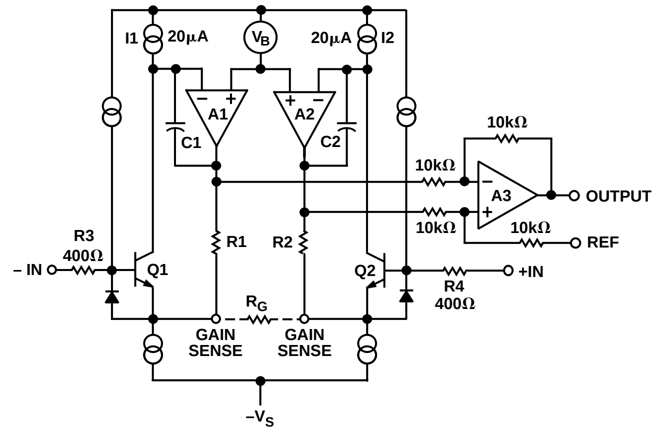


Figure 33. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 33), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/$\sqrt{Hz}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Make vs. Buy: A Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, fewer components and 10× lower supply current. In the typical application, shown in Figure 34, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of –40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.

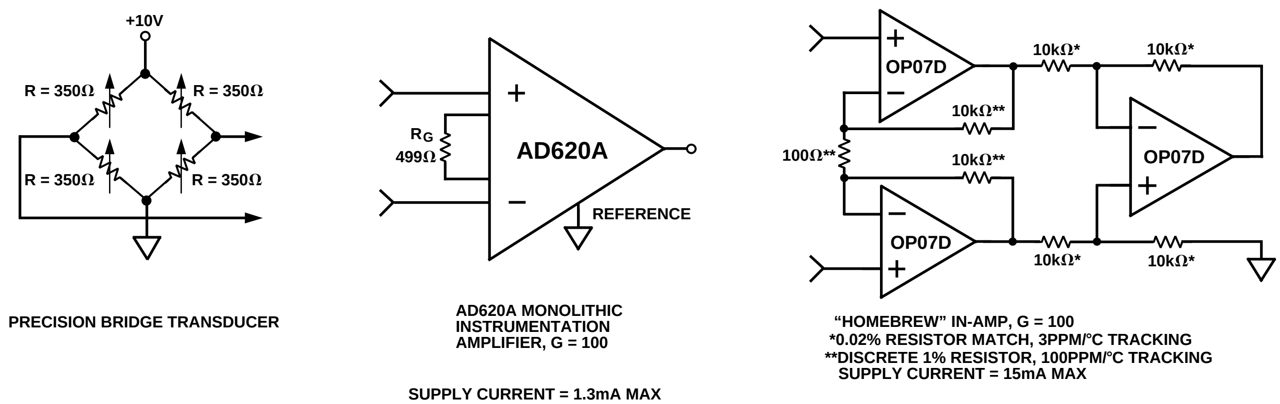


Figure 34. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × $\sqrt{2}$)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,558	11,310
DRIFT TO +85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × $\sqrt{2}$ × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100/20 mV	(2.5 µV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × $\sqrt{2}$)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	28,134

G = 100, V_S = ±15 V.

(All errors are min/max and referred to input.)

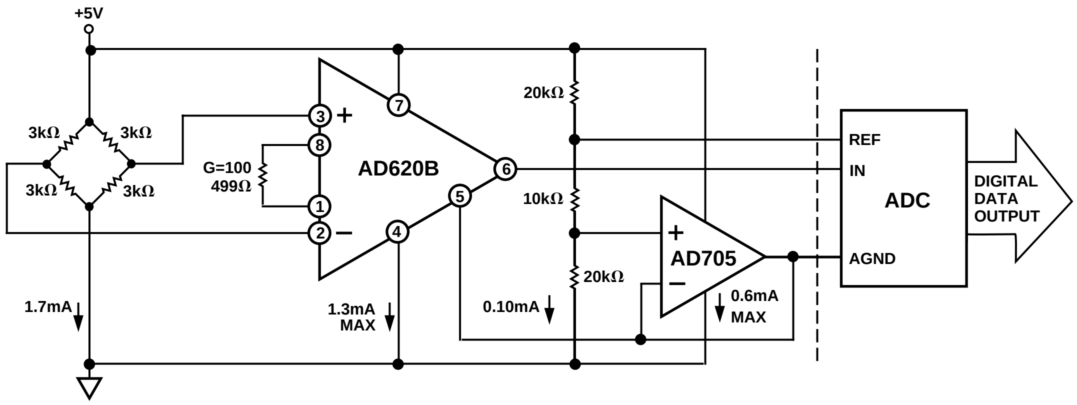


Figure 35. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

Pressure Measurement

Although useful in many bridge applications such as weigh scales, the AD620 is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 35 shows a 3 kΩ pressure transducer bridge powered from +5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic non-invasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 36) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

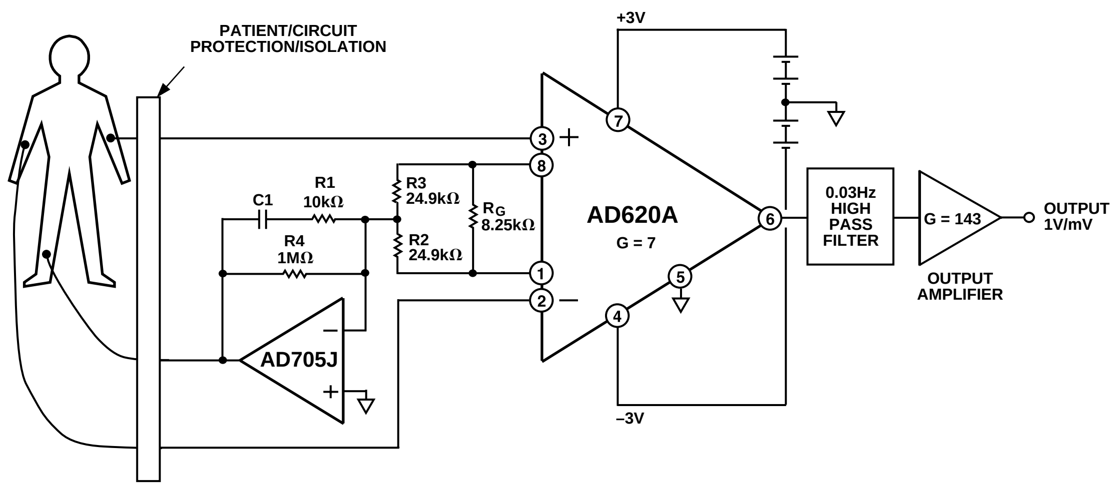


Figure 36. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620, along with another op amp and two resistors, makes a precision current source (Figure 37). The op amp buffers the reference terminal to maintain good CMR. The output voltage V_X of the AD620 appears across R1, which converts it to a current. This current less only, the input bias current of the op amp, then flows out to the load.

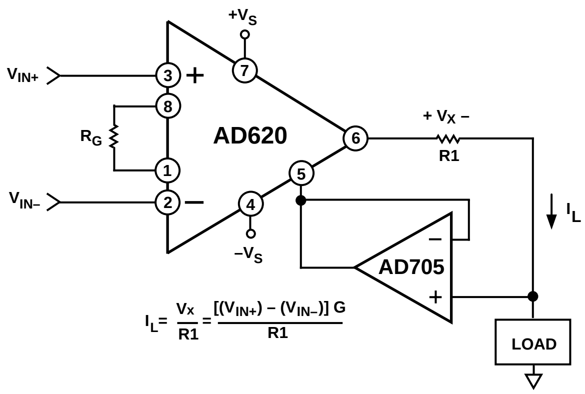


Figure 37. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620's gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1%–1% resistors. Table II shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain R_G can be calculated by using the formula:

$$R_G = \frac{49.4\ k\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance.

Table II. Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \le V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 38), where $RC \approx 1/(2\pi f)$ and where f ≥ the bandwidth of the AD620; C ≤ 150 pF. Matching the extraneous capacitance at Pins 1 and 8 and Pins 2 and 3 helps to maintain high CMR.

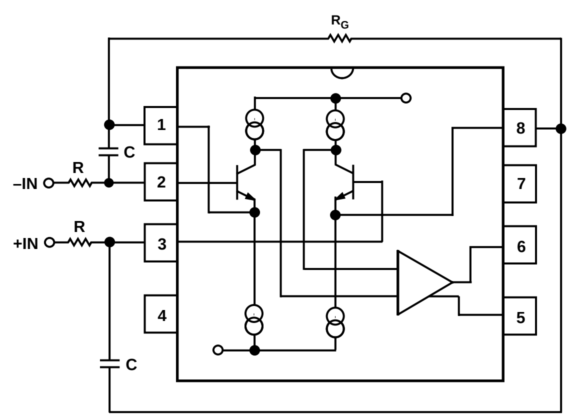


Figure 38. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers like the AD620 offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should be properly driven. Figures 39 and 40 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

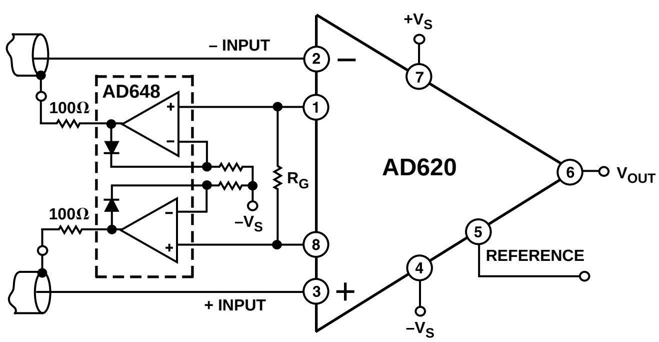


Figure 39. Differential Shield Driver

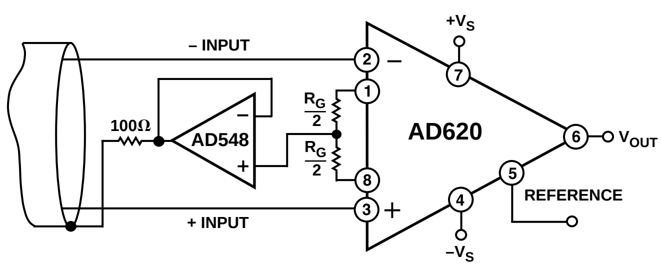


Figure 40. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 41). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

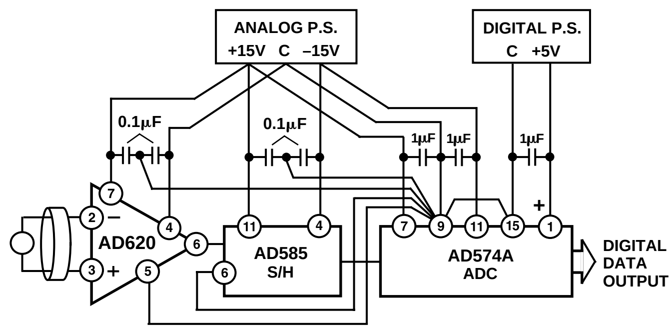


Figure 41. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 42. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

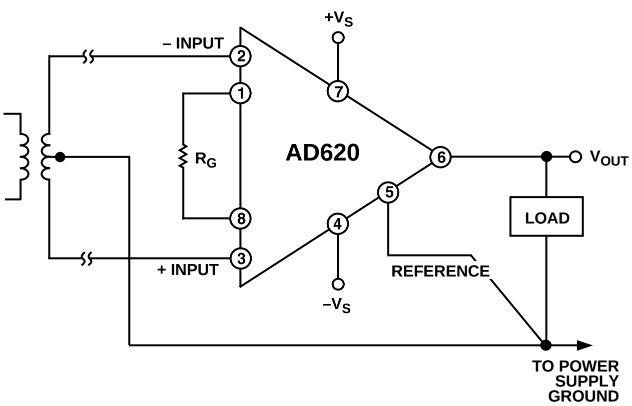


Figure 42a. Ground Returns for Bias Currents with Transformer Coupled Inputs

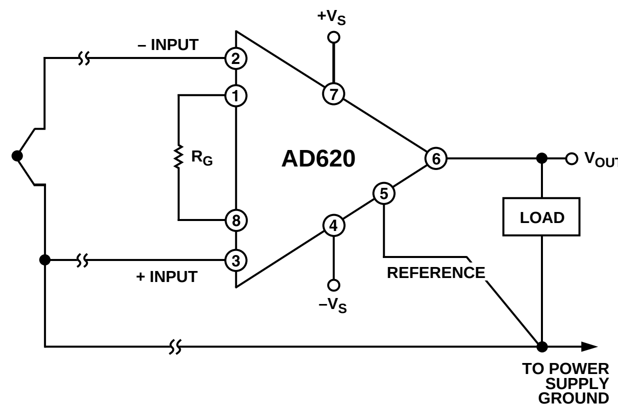


Figure 42b. Ground Returns for Bias Currents with Thermocouple Inputs

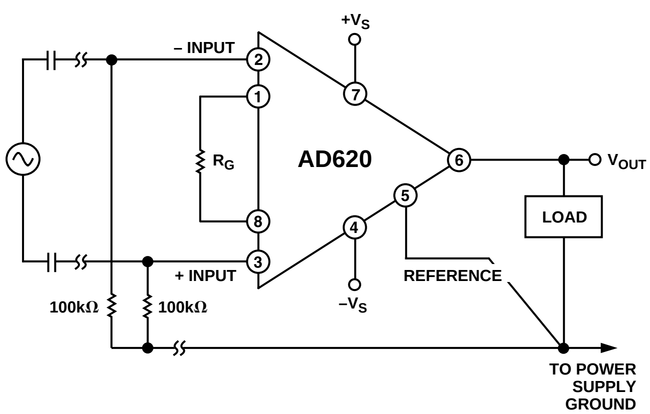
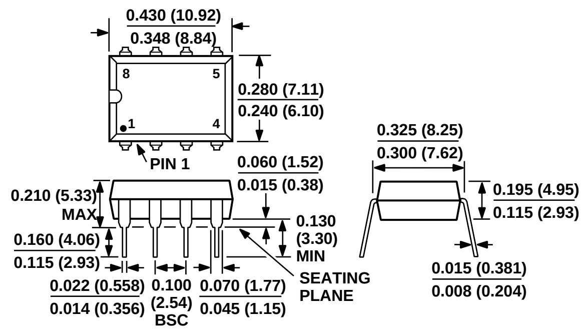


Figure 42c. Ground Returns for Bias Currents with AC Coupled Inputs

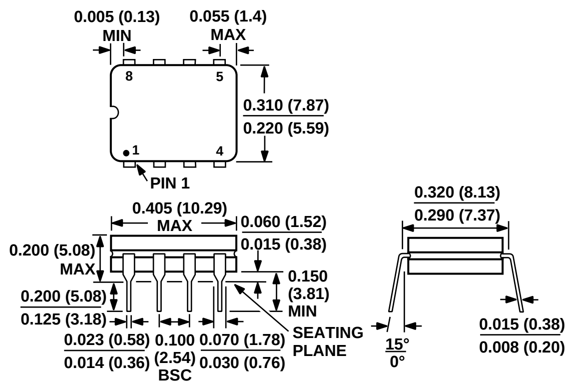
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

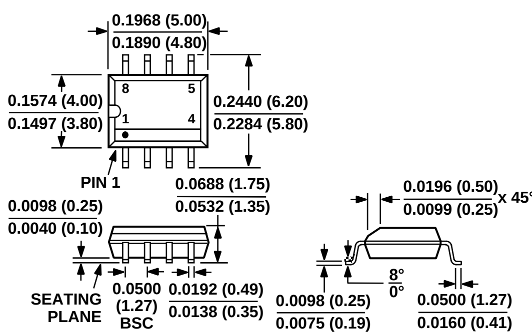
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (SO-8) Package



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