



School of Engineering Science • Burnaby, BC • V5A 1S6  
ensc440-IJtech@sfu.ca

July 5, 2006

Dr. Andrew Rawicz  
School of Engineering Science  
Simon Fraser University  
Burnaby, British Columbia  
V5A 1S6

Re: ENSC 440 Post-Mortem for a Smart Alarm Clock

Dear Dr. Rawicz,

The enclosed document, Post-Mortem for a Smart Alarm Clock, details the entire process that the Inglewood Jack Technologies team went through to develop our prototype for the ENSC 440 course. As you already know, our device was the Smart Alarm Clock, designed to help people wake up feeling refreshed every morning.

This document describes the current state of the device, and how it is different from our initial plans for development. We then discuss the challenges involved in building the Smart Alarm Clock, and future plans for the production model. Finally, we finish the discussion with an analysis on our budget and timeline performance, followed by our own inter-personal experiences in building the Smart Alarm Clock.

Inglewood Jack Technologies Inc. consists of five talented and innovative individuals who study engineering at Simon Fraser University: Albert Su, Christian Le, Herman Leung, William Ng, and Matthew Ng. If you have any questions or concerns, we will be pleased to answer them. We can be contacted via email at [ensc440-IJtech@sfu.ca](mailto:ensc440-IJtech@sfu.ca).

Sincerely,

A handwritten signature in black ink, appearing to read "Christian Le". The signature is fluid and cursive, with the first name being the most prominent.

Christian Le  
Chief Operations Officer  
Inglewood Jack Technologies, Inc.

Enclosure: Post-Mortem for a Smart Alarm Clock



# Design Specifications for a Smart Alarm Clock

**Project Team:** *Christian Le  
Herman Leung  
Matthew Ng  
William Ng  
Albert Su*

**Contact Person:** Christian Le  
ensc440-IJtech@sfu.ca

**Submitted to:** Dr. Andrew Rawicz – ENSC 440  
Steve Whitmore – ENSC 305  
School of Engineering Science  
Simon Fraser University

**Issued Date:** July 5, 2006

**Revision:** 1.0



## Table of Contents

Glossary .....	ii
1 Introduction.....	3
2 Current State of the Device.....	3
2.1 <i>Interface</i> .....	3
2.2 <i>Software</i> .....	3
2.2.1 System State Design .....	3
2.2.2 REM Detection Algorithm.....	4
2.3 <i>Embedded Software</i> .....	5
2.3.1 Programming Implementation .....	5
2.3.2 Alarm Clock Subsystem Communication.....	5
2.3.3 Bluetooth Subsystem Intercommunication .....	5
2.4 <i>Hardware</i> .....	7
2.4.1 Circuit Design .....	7
2.4.2 Pulse Measurement Device.....	8
2.4.3 Physical Enclosure .....	8
3 Design Challenges .....	8
3.1 <i>Overall System &amp; Integration</i> .....	8
3.2 <i>Software</i> .....	9
3.2.1 Pulse Detection .....	9
3.2.2 REM Detection .....	10
3.3 <i>Embedded Software</i> .....	11
3.4 <i>Hardware</i> .....	11
3.4.1 Hardware Reset.....	11
3.4.2 UART.....	12
4 Future Plans .....	12
4.1 <i>Overall System</i> .....	12
4.2 <i>REM Detection</i> .....	13
4.3 <i>Alarm Process</i> .....	13
4.3.1 Selection of Songs & Sounds.....	13
4.3.2 Improvements in Gradual Light Increase .....	13
4.4 <i>Hardware</i> .....	14
4.4.1 Microcontroller Upgrade .....	14
4.4.2 Bluetooth Enabled Pulse Measurement Device.....	14
4.4.3 Incorporation of MP3 Decoder and MMC Card on the Main Board.....	14
4.4.4 Miniaturization.....	14
5 Budgetary and Time Constraints .....	15
5.1 <i>Budget</i> .....	15
5.2 <i>Time</i> .....	16
6 Inter-Personal & Technical Experiences.....	18
6.1 <i>Christian Le</i> .....	18
6.2 <i>Herman Leung</i> .....	18
6.3 <i>Matthew Ng</i> .....	19
6.4 <i>William Ng</i> .....	20
6.5 <i>Albert Su</i> .....	21



7	Conclusion .....	21
8	References.....	22

## **Glossary**

<b>CVS</b>	concurrent versions system
<b>FSM</b>	finite state machine
<b>I2C</b>	Inter-Integrated Circuit
<b>IJ Tech</b>	Inglewood Jack Technologies
<b>JTAG</b>	Joint Test Action Group
<b>LED</b>	light emitting diode
<b>REM</b>	rapid eye movement
<b>SAC</b>	Smart Alarm Clock
<b>STK</b>	Synthesis Toolkit
<b>UART</b>	Universal Asynchronous Receiver Transmitter
<b>USART</b>	Universal Synchronous-Asynchronous Receiver Transmitter



## **1 Introduction**

Throughout the past six months, Inglewood Jack Technologies (IJ Tech) has been actively pursuing the completion of a proof-of-concept model of the Smart Alarm Clock (SAC) system. In the prototype development stage, we focused on technical feasibility, circadian rhythm understanding and market analysis by the production of a working prototype. Towards concurrent design and systematic integration, the SAC is modularized into four subsystems: the Alarm Clock Subsystem, the Music Player Subsystem, the Light Control Subsystem and the Pulse Measurement Subsystem. Team members form groups according to their individual strengths for subsystem development. Regular group communication through various mediums and consistent integration effort for product dependability results in a proof-of-concept model that complies and exceeds the standards imposed upon the product by the functional specifications. After extensive component and system tests, we strongly believe in the market potential of the SAC and have plans to design a production model.

In the *Post-Mortem for a Smart Alarm Clock*, we provide detailed description of our development, deviations from our original specifications and future developmental recommendations for our product. Comparisons between the projected and actual budget, as well as discrepancies between the proposed and final time constraints with the proof-of-concept model are also outlined. In addition, team members involved in the development of the SAC proof-of-concept model will reflect on their technical experiences gained and team dynamics experienced from participating in the project.

## **2 Current State of the Device**

### **2.1 Interface**

The user menu matched what was described in the functional specifications. Moreover, this user menu would be very similar as in the potential production model. A change in the initial design was adding features that could easily be shown in the product demo, but not seen in the production model. This included modifying the display of the initial music volume for the alarm-waking process, and adding the ability to display the heart rate of the user on the numeric LCD screen (which is generally for displaying the time).

The AM/PM light emitting diodes (LEDs) are not labelled in the prototype, but will be in the production model. We will also convey to the user that if no LEDs are lit up, then the clock is in 24 hour display mode as opposed to the 12 hour display mode.

### **2.2 Software**

#### **2.2.1 System State Design**

The high-level system state design has deviated significantly from the originally planned finite state machine (FSM) implementation. Initially, the Alarm Clock Subsystem is to provide a high-level, centralized control over all the subsystems and the abstracted software modules. As time progressed, however, various software processes were localized to their respective subsystems and modules. The reasoning behind this is that



the localized approach was faster to develop and easier to test than the centralized approach. The lack of a concurrent versions system (CVS) prohibited group members from centralizing their code unless countless hours are spent through manual integration.

Although the approached design method differs from the original implementation, the conceptual idea remained the same. The functions that must be performed at each state are still performed, with the exception of the Monitoring State and the Alarming State.

### **2.2.1.1 Monitoring State**

During the monitoring state, processing of the user's pulse rate and determination of the rapid eye movement (REM) sleep stage was computed "on-the-fly." This meant that the amount of data history that must be kept was significantly lower than what was initially anticipated. The current implementation does not require the access of external memory storage, (i.e. the MMC) and hence is more memory efficient.

### **2.2.1.2 Alarming State**

The method of waking the user in the alarming state has also been modified slightly. It was initially planned to let the user have as much as 90% of his or her final REM stage before initiating the Music Player Subsystem. However, a more conservative estimate of 50% based on previous REM duration was used instead. This ensures that the music is played before the possibility that the user has exited the current REM stage.

## **2.2.2 REM Detection Algorithm**

At the time the design specification was written, not much was known about how heart rate actually varies throughout the night. In order to gain further understanding into this, we had to find a way to simultaneously capture the heart rate throughout the night while determining the current sleep stage of the user.

Using a sleep stage tracking device called REMView, the user's current sleep stage was determined by a combination of eye-lid and head motion sensors. Heart rate data is logged using our Pulse Monitor Module concurrently. The process was repeated multiple times across different group members to ensure proper variation of data. From the data, mean heart rate and variance was calculated using different averaging window duration of 1, 2, 3, 4 and 5 minutes. The results were then compared with the captured data from REMView to determine the heart rate trend during a REM stage.

The method used to determine REM stage was not based on variance threshold detection. Since different people have different variance threshold levels, and the variance threshold level may change throughout the night, it was not a feasible method of detection as originally proposed in the design specification. It was later settled upon using a relative rate of change of variance as the determination criteria. If the relative increase in variance was large, we are transitioning from non-REM to REM. Similarly, if variance drops consistently, it means that we are transitioning from REM to non-REM.



## **2.3 Embedded Software**

### **2.3.1 Programming Implementation**

The development of the embedded software was done using a microcontroller Joint Test Action Group (JTAG) debugger. Rather than coding on our development kits, loading and developing code was done directly on the Alarm Clock and Light Control Subsystem boards. Using this strategy saved time, and also the chance of performing real-time debugging.

### **2.3.2 Alarm Clock Subsystem Communication**

The microcontroller in the Alarm Clock Subsystem communicated with other devices mainly with the Inter-Integrated Circuit (I2C) bus. Through the bus, the microcontroller communicated with the IO expander, which could send or receive data from user buttons, AM/PM LEDs, and the pulse measurement device.

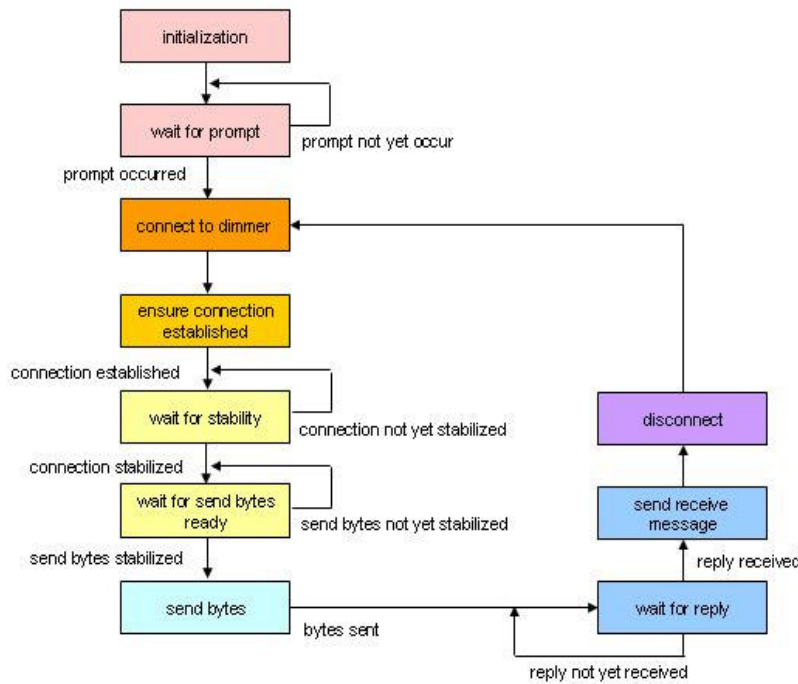
Also on the I2C bus was the music amplifier; communication on the bus to this device controlled the output volume of music and sound from the Music Player Subsystem. By sending instructions on the bus to the amplifier, the gradual increase of music during the alarm process was achieved.

### **2.3.3 Bluetooth Subsystem Intercommunication**

As specified in the design specification, wireless intercommunication between the Alarm Clock Subsystem and the Light Control Subsystem was established through the use of a Bluetooth interface. A Universal Synchronous-Asynchronous Receiver Transmitter (USART) interface acts as the basis through which the Bluetooth protocol is employed for subsystem intercommunication. We pursued two Bluetooth intercommunication algorithms to approach the problem, in hope to find a balance between simplicity of algorithm and maintenance of linkage between the two subsystems. Stringent testing was conducted to simulate the behaviour of the Bluetooth intercommunication under various situations to establish its capabilities and limitations.

In the final implementation of the Bluetooth intercommunication algorithm, a time dependent finite state machine (FSM) method was utilized. Figure 1 illustrates the algorithm flowchart for the Alarm Clock Subsystem.

**Alarm Clock Subsystem**



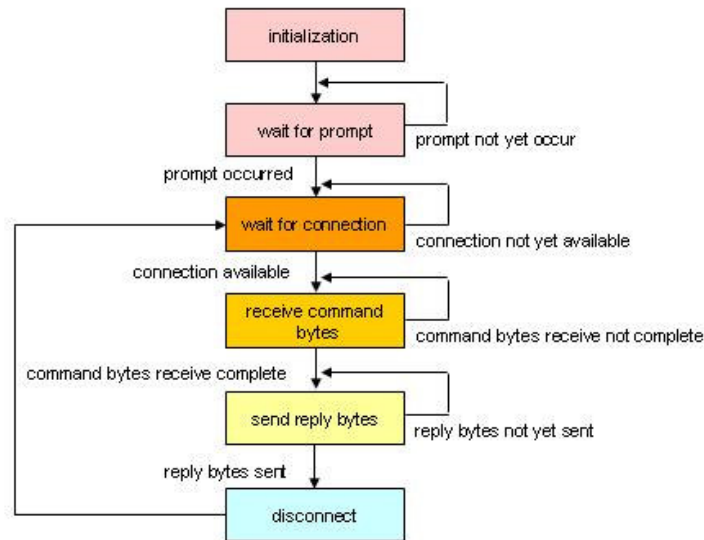
**Figure 1: Alarm Clock Subsystem Bluetooth Algorithm**

Due to the complexity of the algorithm, we focused on the key steps involved in establishing the linkage between the two subsystems under consideration. The error recovery algorithm and time dependent nature of the Bluetooth algorithm are not illustrated. After initialization of the USART and the Bluetooth device, the Alarm Clock Subsystem repeatedly attempts a connection with the dimmer, or the Light Control Subsystem, at regular intervals until a linkage is established. Upon achieving interconnection stability, the communication process between the two subsystems occur, while the Bluetooth algorithm ensures that the process does not remain in a specific state for a prolonged period of time; if it does, this denotes a firmware or hardware error. Also, a constant connection verification is in place to reassure that the linkage between the two subsystems is in place during the communication process.

While the Alarm Clock Subsystem acts as the master to send command messages, the Light Control Subsystem takes the role of the slave to receive and respond to the commands. A high level flowchart which summarizes the Bluetooth algorithm for the Light Control Subsystem is shown in Figure 2.



**Light Control Subsystem**



**Figure 2: Light Control Subsystem Bluetooth Algorithm**

Similar to the illustration of the Alarm Clock Subsystem Bluetooth algorithm, we ignore the error recovery and time dependency processes to focus on the key algorithm. The notable difference in the algorithms for the two subsystems is that the Light Control Subsystem acts to receive the command bytes and replies with verification messages. A fixed connection established through applying the unique Bluetooth address for the two modules integrated into the Alarm Clock Subsystem and the Light Control Subsystem ensures that the linkage will not be interfered by other Bluetooth devices within reception circumference. The algorithm design also eliminates reliance on holding the microcontroller for a prolonged period of time, such that process multitasking can be realized for both the subsystems in discussion. Command protocols sent between the Alarm Clock Subsystem and the Light Control Subsystem complies with was initially proposed in the design specification.

## 2.4 Hardware

### 2.4.1 Circuit Design

The electronics design in the project is perhaps the part that deviated the least from the initial proof of concept model envisioned. Most of the issues encountered were solved by tweaking component values, while others are worked around through software. The major difference is the implementation of the JTAG programming interface in our system. The initial plan was to use the development kit to program our microcontrollers then swap them into our system. However, this was too inconvenient and we needed a real time debugging interface.



### **2.4.2 Pulse Measurement Device**

Being the central theme behind our project, the pulse measurement device must work; this required a complete redesign midway through our development. The initial mechanical design was great on paper but it proved to be unreliable when prototyped. During the redesign, efforts were spent in actual implementation then documentation. Ideas were thrown around, built, and tested to finally yield a pulse measurement device that gave reliable readings. The new device is very different but it surely kept the user's finger constrained and limited the amount of ambient light.

### **2.4.3 Physical Enclosure**

At the time the functional specification was drafted, the physical dimensions of the circuit boards were unknown and our group was over optimistic that a suitable plastic enclosure could easily be obtained. Because of the two LCD displays on the front face, the front of our enclosure must have clear windows. Failing to search for similar enclosures, we decided to build our own and settled on a see through enclosure to showcase our proud prototype. The dimensions of our alarm clock is larger than anticipated because the size of the enclosed circuit boards.

## **3 Design Challenges**

### **3.1 Overall System & Integration**

As with any project, the overall communication between subsystems and modules is a tough, and sometimes, excruciating task. It was no exception for the SAC; as perfect as the individual subsystems worked by themselves, getting them to communicate to each other was one of the challenges in development.

Knowing that integration would be a challenge, several steps were taken in advance when developing the subsystems. All these subsystems would eventually be communicating with each other. Thus, team members not only had to focus on the subsystem they were developing, but also keeping in mind that their work had to accommodate the needs of other subsystems. One easy example was the use of common variables; if one subsystem depended on the values from another subsystem, it was important to know where these values were and also when they would be valid.

To limit the number of problems, there was constant communication between team members. Subsystem code would continuously be available such that they could be referred by anyone needing them. There was also the use of pseudo code, diagrams, flowcharts, and anything else to simplify the understanding of what needed to be done.

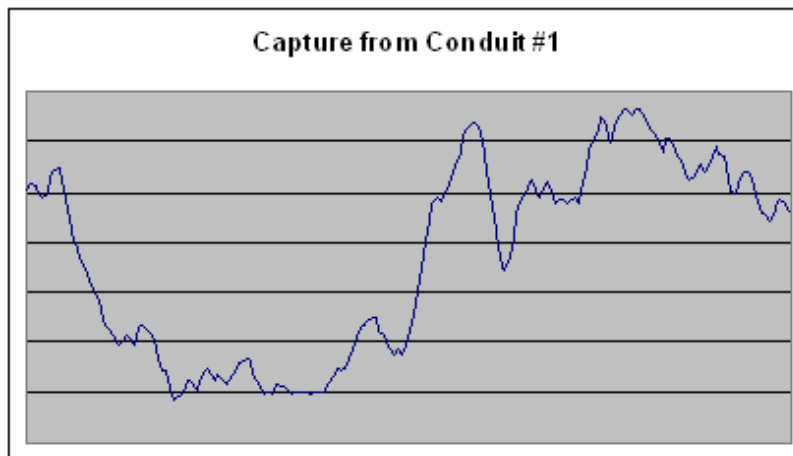
Another challenge with integrating the individual subsystems was the use of wait statements. Generally, wait statements allow a subsystem to 'wait' for certain events to occur such that the needed results are valid. This waiting period takes up a significant amount of processor time, and actually prevents other subsystems from operating correctly.

The easy solution was to remove wait statements whenever possible, allowing all subsystems to obtain the necessary amount of processing power. In order to achieve this, it was necessary to code all subsystems in a “case statement” fashion. Each subsystem was given a chance to perform a certain number of events, depending on the state that it was in. By using this strategy, wait statements were reduced and all subsystems could coincide with one another. In the case where it was extremely necessary to use wait statements, the waiting periods had to be as small as possible.

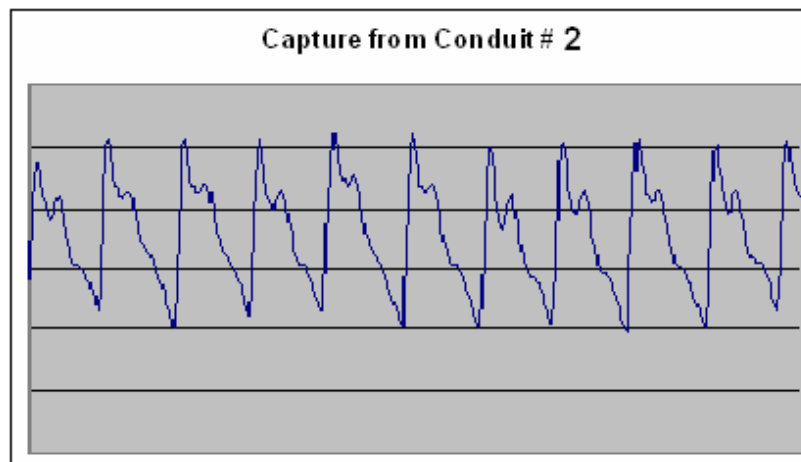
## **3.2 Software**

### **3.2.1 Pulse Detection**

The pulse detection part of the system was a major challenge. The ability to determine the user’s pulse rate accurately highly depends on the condition of the captured sample data from the hardware pulse monitor conduit. The first version of the pulse monitor conduit consistently gave poor data. Shown in Figure 3 is the capture from conduit 1, while Figure 4 shows the capture from conduit 2.



**Figure 3: Heart Rate Capture from Conduit 1**



**Figure 4: Heart Rate Capture from Conduit 2**

From the two figures, it is easy to see that conduit 2 results in a more distinguishable pattern for heart rate processing. Initial attempts at processing data captured from the first conduit led to incomprehensible results. It was not until conduit 2 was ready before proper pulse processing detection algorithm could begin development. However, regardless of the improved performance of conduit 2, both conduits failed to capture meaningful data when there was excessive hand motion. Thus, we relied on software to deal with anomalies in the data. Sufficient error handling was implemented to deal with larger or smaller than normal beat-to-beat counts. Moreover, the relative change between successive heart beat counts was also limited.

### 3.2.2 REM Detection

It was discovered that the heart rate variance data does not correspond completely with REM stages. There are incidences where the variance is significantly higher than neighbouring times, but REMView failed to register a REM stage. Thus, the accuracy of REMView was in question. Nonetheless, for other parts of the data where both high variance and REM stage were detected, we can see that a correlation does exist. Shown in Figure 5 below is the result of a typical night of capture.

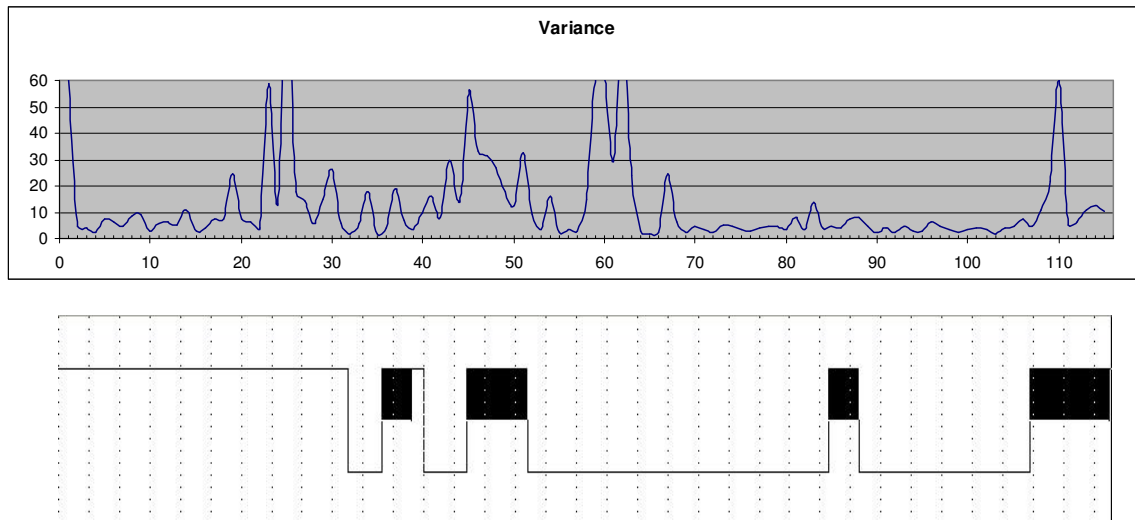


Figure 5: Heart Rate Variance (top) versus REM Stage (bottom) for a 3 Minute Window

From Figure 5, we see spikes of variance during periods of REM, denoted by raised black bars. Areas not denoted by black bars but are still raised represent the waking stage (ie. when the user is conscious). It is evident that variance corresponds well with either the waking stage or the REM stage. As mentioned previously, there are incidences where high variance does not result in a REM stage. Looking on the variance graph when the X-axis is around 60, a large variance can be seen. However, the corresponding data from REMView indicates that this is non-REM. To overcome this uncertainty, we captured as much data as possible. Over 15 nights worth of data was captured from four different group members.



Calculating REM “on-the-fly” was a notoriously difficult task. The system must be able to anticipate the onset of REM with only past inputs and not future inputs (i.e. the system is causal). With this restriction, false detection couldn’t be avoided since we simply may not have had enough information to predict future events. Fortunately, since the alarm clock only needed to “predict” the onset of REM during the monitoring window and not during the earlier portion of the night, it was actually possible to determine REM in the earlier portion of the night more accurately. This is essential, since we needed to calculate the average duration of REM stage. In the event that multiple, false REM stages were detected, our average duration of REM would be very low. This corresponds to waking the user up earlier than expected during his or her final REM stage before the deadline. When analyzing the duration of the REM stages for the earlier portion of the night, a minimum duration for a REM stage must be met before the system interprets it as being valid.

### **3.3 Embedded Software**

Accomplishing the Bluetooth algorithm for subsystem intercommunication imposes unique challenges which required creative approaches to isolate the state or process that results in linkage failure. As a Bluetooth algorithm is in place on both the Alarm Clock Subsystem and the Light Control Subsystem, establishing the side that caused a linkage failure is difficult. Further, no runtime debugging software exists for us to pinpoint the exact process leading to software failure. Along with persistence in trial and error, we devised a scheme which employs the LED on the Synthesis Toolkit (STK) development board as a real-time breakpoint tool such that firmware problems could be isolated and eliminated. Due to insufficiency in documentation provided with the Bluetooth devices, an extended period of time was required to understand the behaviour of the Bluetooth modules and decipher whether error in establishing Bluetooth connection was a result of embedded software or hardware failure.

### **3.4 Hardware**

#### **3.4.1 Hardware Reset**

In the initial design, it was anticipated to power the Alarm Clock Subsystem, Music Player Subsystem, and Pulse Measurement Subsystem using a single 9V power adapter (“wall wart”). The 9V source was able to power the system without trouble for most scenarios but we experienced unexpected hardware resets during music playback at a high volume. The problem was not found until very late in the development cycle when the system topology was fixed; many alternatives were therefore limited by the available board space and compatibility with the existing design.

The 5V voltage regulator was unable to regulate during high current surges by the audio amplifier; the drop in supply voltage caused the power monitoring circuit to reset the entire system. Potential solutions were tested to filter the spikes on the supply line, but the ultimate problem was the adapter itself not having the capability to drive such a heavy load. The 9V unregulated supply dropped to less than 5V plus the needed dropout voltage required by the regulator, thus there was little to none voltage regulation. The solution



was to replace the 9V adapter with a 12V adapter with higher current capability; this ensured a large design margin.

### **3.4.2 UART**

The Universal Asynchronous Receiver Transmitter (UART) was used to communicate with the Bluetooth module, which formed the link between the Light Control Subsystem and the Alarm Clock Subsystem. There were intermittent problems experienced by the on-chip UART of the microcontroller, particularly with receiving bytes sent by the Bluetooth module. This issue required a significant amount of time to debug as it was difficult to isolate the problem to the Bluetooth link or the UART link. After days of debugging, we attributed the issue to the UART's baud rate generator which derives its clock from the microcontroller's RC oscillator.

The RC oscillator is factory calibrated for operations at 5V; however our chip is powered by 3.3V to easily interface with the MP3 decoder chip and MMC. The inaccurate system clock did not allow the UART to receive properly, meaning a more accurate clock source was needed. Once again, this issue was not found until later stages of the project which meant there was no space for an external oscillator to clock the system. Fortunately, we found ways of calibrating the RC oscillator with the 32.768kHz watch crystal already used for the real-time clock and a short software routine that runs when the system is first powered up.

## **4 Future Plans**

### **4.1 Overall System**

After having thoroughly tested the alarm clock, making it more marketable can be best accomplished by tweaking the accuracy and comfort of the pulse conduit. The attribute of the SAC that will cause consumers to worry the most about is whether or not wearing the pulse sensor will be comfortable at bedtime. In addition, they will wonder if the clock is actually able to accurately measure what stage of sleep they are currently in. Users would not like to be woken up in a non-REM stage or early in the REM cycle.

Another great way to make the clock more marketable is to make the SAC smaller and more compact. Nowadays consumers tend to buy the product that saves space in the room. If the SAC can be made smaller in size, with the LCD screen and buttons retaining their current size, the SAC's overall appearance would be more attractive.

This clock is very complex, and the prototype has already been designed such that it is easy to learn about using its features. The directional button allows the consumer to navigate the menus very easily. The only improvement that can be made is to make the directional button into a directional pad, as users with larger hands or poor eyesight will then have an easier time operating the device.



## **4.2 REM Detection**

We can further improve upon our current REM detection algorithm. From our experience with analyzing the captured heart rate data and REM data, we realized that hard-coded threshold values for the determination of REM cannot be used. This is not to say that they can be ignored altogether. Instead, a form of fuzzy logic must be used to determine the different degrees of REM that employs a combination of methods. From the heart rate data alone, both the mean and variance can be used to determine the existence of REM. Our current approach only utilized variance, while ignoring the mean. A much more sophisticated fuzzy logic can be developed that employs both as an indicator of REM. Moreover, if certain threshold values can be adaptive (i.e. adapting to a particular user), an even better algorithm can be developed.

Another part of the algorithm that can be improved upon is the ability to predict the transition from REM to non-REM. Although this requires predicting the end of a REM stage based on present data, it is a nice path to pursue. The ability to implement this feature means that maximizing the user's final REM stage can be better achieved. It may also be beneficial to add a REM prediction algorithm to see if a later REM stage will occur before the hard deadline. The SAC can thus ignore the first detected REM stage in the monitoring window period if it is "too early" to wake the user. Similar to the adaptive algorithm method, the average duration between two successive REM stages can be used in the prediction.

Further improvements on REM detection requires more data capture from different control groups. Instead of using REMView to provide the basis of REM detection for comparison, better devices and indicators must be used, such as brain wave, respiration, body motion, temperature, etc. These tests, although too time consuming to pursue during the initial prototype development, are an absolute necessity before the product can be sold on the market.

## **4.3 Alarm Process**

### **4.3.1 Selection of Songs & Sounds**

During the alarm-waking process, a song is taken from MMC memory and played up to the alarm deadline. At the alarm deadline, a new alarm sound is played until the user turns it off. The choice of song and sound, however, cannot be chosen by the user on the prototype. Our plans would be to implement the option of the user to choose from a variety of songs and sounds that he/she has stored onto the MMC card. The choices of these songs can be done within the user menu.

### **4.3.2 Improvements in Gradual Light Increase**

Another improvement in the alarm process would be the gradual increase in light. The increase in light in the bedside lamp was very slow in the beginning; during the SAC demo, it took minutes before one could actually see a change in the intensity. This is due to the amount of voltage being sent to the bedside lamp. When the Light Control Subsystem is initially sending low amounts of voltage, this amount is not large enough to



heat the filament to produce light. Because of this behaviour, modifications to the Light Control Subsystem would be to start the gradual light increase at a higher initial voltage instead of zero. Doing this allows an instant, and more importantly a visual, change in the light intensity.

## **4.4 Hardware**

### **4.4.1 Microcontroller Upgrade**

At first, there was no sense of the kind of processing needed for detecting sleep behaviour, managing a file system, running a user menu, and keeping a Bluetooth link all concurrently. Some of these functions did not even come up during our initial project brainstorm. The current microcontroller (Atmel ATmega32) is exhausted in performing these tasks leaving little room for more effective but computation intensive sleep detection algorithms. The ATmega32 is only an 8-bit microcontroller with no support for floating point operations; the use of a more advanced microcontroller or microprocessor will allow our software designers to fully exploit their creativity. With the use of floating point arithmetic, we can detect the user's pulse rate with better accuracy and the possibility of processing REM detection in the frequency domain rather than the time domain.

### **4.4.2 Bluetooth Enabled Pulse Measurement Device**

To minimize the risk of choking/struggling the user and boosting the comfort level of our Pulse Measurement Device, a redesign is needed. The current device currently has a very crude mechanical fixture and it communicates through a long ribbon cable. An application specific mechanical design will be utilized to ensure reliable pulse measurements without sacrifice of user's comfort. In terms of the electronics, power consumption must be decreased dramatically to maximize the battery life of this wireless device.

### **4.4.3 Incorporation of MP3 Decoder and MMC Card on the Main Board**

Instead of using the MP3 development board as in the current implementation, the actual MP3 decoder chip and a connector for the MMC Card will be placed on the main board of the alarm clock. This will decrease cost dramatically and save space, which is a necessity in the production model.

### **4.4.4 Miniaturization**

Reducing the size of the circuit boards will minimize cost related to printed circuit boards and enclosures. On top of this, it will make our devices more similar in size to current alarm clocks in the market as opposed to our rather large prototype. Making the alarm clock small and aesthetically pleasing is crucial for product penetration.



## 5 Budgetary and Time Constraints

### 5.1 Budget

Table 1 tabulates the estimate cost for the development phase of the SAC proof-of-concept device proposed during the initialization of the project.

**Table 1: Initial Budgetary Estimate**

Module	Component Description	Cost
Alarm Console	MP3 Decoder Module and Development Kit	\$ 220
	LCD Modules	\$ 90
	Audio Amplifier and Speakers	\$ 30
	Microprocessor and Development Kit	\$ 120
	Buttons and Inputs	\$ 20
Light Controller	Microcontroller and Development Kit	\$ 15
	Power Regulation and AC-DC Conversion	\$ 30
	Light Dimmer Analog Circuitry	\$ 15
	Buttons and Inputs	\$ 10
Wireless Intercommunication module	Wireless Communication Module Development Kit	\$ 700
Prototype Development	Boards and Miscellaneous Components	\$ 150
Contingency (15% of total cost)	May include, but not solely entitled to, extra components required and shipping costs	\$ 210
	<b>Total</b>	<b>\$ 1610</b>

During the development process, we revised the estimated cost to a less conservative figure of \$1000 CND. Careful choices of components for a balance of functionality and cost, active pursuing of corporate sponsorship and thoughtful design to eliminate component wastage enabled us to incur a consolidated cost less than our estimated expenditure.

Table 2 summarizes the cost of materials acquired and the total incurred costs for the project.



**Table 2: Actual Consolidated Cost**

Module	Component Description	Cost
Alarm Console	MP3 Decoder Module and Development Kit	\$ 256.83
	LCD Modules	\$ 75.76
	Audio Amplifier and Speakers	\$ 26.66
	Microprocessor and Development Kit	\$ 121.71
	Buttons and Inputs	\$ 5.45
	Watch Crystal	\$ 84.57
Light Controller	Microcontroller and Development Kit	\$ 0
	Power Regulation and AC-DC Conversion	\$ 55.38
	Light Dimmer Analog Circuitry	\$ 0
	Buttons and Inputs	\$ 5.45
Wireless Intercommunication module	Bluetooth Wireless Communication Module Development Kit (Sponsored by A7 Engineering)	\$ 0
Prototype Development	Boards and Miscellaneous Components	\$ 123.91
	Total	\$ 755.72

Our final incurred cost for the developmental phase of the project is \$755.72 CND. Of the total cost, we have secured \$350 from the Engineering Student Society Endowment Fund (ESSEF). In addition, we are in progress of applying for the Wighton Fund to cover the remainder of the development cost. A series of cost reduction measures and efforts to secure funding for the project enabled the team to focus on the technical development throughout the past six months.

## 5.2 Time

The next page shows a table of IJ Tech’s project timeline. The table compares the initial goals of the project to the actual dates in which parts of the project were completed. Explanations of any delays on the tasks are also discussed.

Overall, there was obviously a delay in the completion and implementation of the SAC prototype. The main reason behind the delay was the underestimation of understanding and detecting REM stages in sleep. Clearly, sleep cycles are a topic outside the knowledge of engineering, and researching the topic took longer than expected.

Another reason lies behind IJ Tech’s desire to produce a prototype that had little, if not, no bugs or defects. Instead of removing features and making a strong attempt to finish a prototype by semester’s end, the extension was taken to enhance and improve the quality of the SAC features and capabilities.



**Table 3: Analysis of IJ Tech Timeline**

Task	Projected Date	Actual Date	Comments
Project Proposal	January 22 <sup>nd</sup>	January 22 <sup>nd</sup>	Proposal was completed on time after a change in project topic due to problems associated with ownership of intellectual property.
Research	January 29 <sup>th</sup>	May 20 <sup>th</sup>	Research on circadian rhythm and REM sleep has been conducted on an ongoing basis. Accuracy comparison and REM sleep pattern collection were done as additional research tasks towards the end of the developmental stage.
Progress Report	February 5 <sup>th</sup>	February 5 <sup>th</sup>	Progress report was done on time with significant progress on our project.
Functional Specification	February 19 <sup>th</sup>	February 19 <sup>th</sup>	Functional specifications have been carefully drafted and agreed upon by all team members.
Design Specification	March 5 <sup>th</sup>	March 5 <sup>th</sup>	Design specification reviewed carefully by members associated to each subsystem and agreed upon by all team members.
Development Alarm Clock Subsystem	February 26 <sup>th</sup>	May 15 <sup>h</sup>	Severe delay due to problems associated with the USART and Bluetooth linkage embedded software development.
Development Music Player Subsystem	February 26 <sup>th</sup>	February 26 <sup>th</sup>	Although shipping of MP3 components were delayed, the contingency period imposed enabled us to complete the subsystem on time.
Development Pulse Measurement Subsystem	February 26 <sup>th</sup>	May 30 <sup>th</sup>	Pulse measurement conduit was redesigned to add user comfort while remaining compliant to functional specification.
Development Light Control Subsystem	February 26 <sup>th</sup>	May 15 <sup>h</sup>	Severe delay due to problems associated with the USART and Bluetooth linkage embedded software development.
Integration	March 26 <sup>th</sup>	June 22 <sup>nd</sup>	Additional features were added during the integration phase. Memory constraints and variable conflicts resulted in a minor delay. Due to delays from the developmental stage, integration was postponed. A “demonstration mode” was added to better display unit functionalities
Testing	March 26 <sup>th</sup>	June 22 <sup>nd</sup>	Testing occurred concurrently with integration. The stage was shorter than expected because subsystem development had been completed carefully to reduce number of defects for integration testing.
Documentation	March 31 <sup>st</sup>	June 24 <sup>th</sup>	Marketing and technical presentations were completed one week prior to demonstration for editing and practicing. A website that contains a user manual was completed ahead of schedule.
Demonstration	April 8 <sup>th</sup>	June 29 <sup>th</sup>	Demonstration was completed flawlessly in terms of Smart Alarm Clock system operations.



## **6 Inter-Personal & Technical Experiences**

### **6.1 Christian Le**

I would like to start off by thanking the members in the IJ Tech group. There is so much talent and character on this team, and many of them have made significant sacrifices in their daily routine to make this project successful.

The ENSC 440 project course is known for its challenges, sleepless nights, making people's lives miserable, and on some occasions, degrading the morale of those who take it. There is no question that I still feel that way about ENSC 440. ☺

Nevertheless, there have been a lot of positives out of the project experience that I will remember. I am glad that after six months of work, we were able to build a device that we could be proud of. We had a great team, a good product in the end, and more importantly, experiences that will only help us in the engineering field.

From a technical side, I realized that there was a significant amount of self-learning. Most of the knowledge I used was not from previous courses, instead from online researching and documentation. My first job in developing the Smart Alarm Clock was communication between different components in the Alarm Clock Subsystem. Later on, I was also a major contributor to the user menu, alarm-waking process, and integration. Through all this development, there is quite the need to push yourself to work. There are no deadlines except for the final product due date. This flexibility is a double-edge sword: you can ease off on the work during busy times, but there is definitely a necessity to consistently work on the project before the lack of effort gets out of hand.

Integrating code and subsystems is no laughing matter. It is a challenge itself along with developing the individual subsystems themselves. I've learned that to make integration as simple as possible, a good foundation needs to be formed; every developer needs to understand that their own subsystems must be designed such that it can be incorporated with the work of others. If that frame of mind is not there, the final integrating procedures become a bigger obstacle than it already is.

### **6.2 Herman Leung**

The development of this project has been a challenging and stressful period; it really tests what's in you. Although the technical design that I was assigned to is relatively easy, I took away a lot more in terms of inter-personal experience, or more generally life experiences. Throughout the past 6 months I found out a lot about myself: my strengths, weaknesses, the kind of work I prefer, and the role I like to take in a design team.

Being mostly involved in the hardware design and building part of the development, I was probably given the most predictable tasks as there were little uncertainties compared to the psychology side of this project. Hardware is my interest and I am glad to be able to fully use my skills to complete a truly amazing project. However, it was at times very stressful to be the hardware designer and the technician; for anything that goes wrong,



you are the first to attend the situation. Furthermore, I always felt obligated to ensure the hardware is working properly to not hinder the progress of others. Since there is only one prototype, development stops when the board stops working.

Building of the prototype took place early in the development cycle which meant I was not bombarded with work at the end. Other than the minor modifications and few problems encountered with the hardware, I devoted my time to help with the software and give input to other parts of the project. This has allowed me to gain a bit more exposure to embedded software. I was given the chance to polish up my weakness and find out the kind of working environment I liked. I enjoy working in smaller teams where my opinion is valued and I can make certain judgement calls in my work; this is valuable information that will benefit my career.

Aside from the technical side of the project, the experience gained working as a team as a start-up company is priceless. You learn how to utilize the best resources as a team to maximize your output, but at the same time how to hold back your emotions when all fails. Sleepless nights, a tight budget, and compounding problems really put a test on friendships. I am glad that no friends were harmed in the making of this project. Even though the project is important, there were also other things occurring in our lives. Throughout the project, I was troubled by personal issues. This project was put me through some hardship and I am thankful to have true friends that ease the pain and sorrow when the world seemed to have tumbled and kept me going to pursue a flawless project.

### **6.3 Matthew Ng**

Completing this project with close friends has been a very rewarding experience. So much time was invested in total, and majority of this time was invested into researching its feasibility and planning out this project. Without careful planning, I realized that it's very easy to miss details when developing the project. In addition, with good planning we can narrow down and agree on what details should not be included in the project given the strict time constraint.

Working on this project gave me a general idea of what it would be like to be an entrepreneur. I found out that to start a company, I must sacrifice many nights of sleep and I have to decrease the amount of spending on my personal life, and invest more in the business.

The past six months has been very technically challenging. In particular, this project has been a good reminder about how difficult embedded software programming can be. There were many problems that arose when I was debugging, and could not conclude whether or not the problem was software or hardware related. However, more often than not it was a software problem, or it was simply just a cable that wasn't connected properly.

Another very rewarding experience I attained from working on this project was researching about a person's sleep. This helped me realize that I wasn't sleeping enough, and that I usually wasn't waking up at the right instance in time because I used a loud and



obnoxious alarm clock to wake me up every morning. Finally I know why I'm groggy every time I wake up. I now try to sleep at least eight hours a night, and am seriously considering purchasing an alarm clock that is able to wake me up at the end of a REM cycle. Alternatively, I can use this prototype.

Finally, I'd just like to thank all my group members for their hard work and dedication on this project. Even though working in a group can be frustrating, without everybody's contribution this Smart Alarm Clock wouldn't get completed on time.

#### **6.4 William Ng**

The past six months has truly been a fun, challenging and at times conflicting experience as the CFO of the team. Being involved in all three sectors of technical development, budgetary control and market analysis, I have always tried to find a balancing point such that we can achieve a quality engineering product under budget constraint and with market potential. The remarkable scope of the project, which spans from psychology to system engineering, may sometimes be overwhelming, but is at all times a valuable learning arena towards what amazing results team work and cooperation can establish.

In the technical front, the main tasks that I was responsible for were the development of a Bluetooth wireless linkage algorithm between subsystems, a USART layer for hardware-firmware interfacing, a function generator automation script for testing and demonstration, as well as a pulse measurement conduit design. The testing phase is quite a memorable experience having to sleep with the REMView device for collecting data on sleeping pattern on a bed that extends no wider than 36 centimetres for four consecutive nights.

As for finance, my primary goal is to incur a final developmental cost that is lower than a non-conservative estimate. Bookkeeping is always interesting because from a business perspective, we are to lower our cost through all possible means, but from an engineering viewpoint we want to incur the cost of making valuable mistakes and purchasing better quality parts. I much appreciate a team effort to choose components wisely and find corporate sponsors such that our financial is achieve while still having a high quality proof-of-concept model developed. Further, I analyzed the market potential of our proposed product and would like to thank all those who have completed my marketing survey.

A well-known entrepreneur once described entrepreneurship spirit as 70% dedication and certitude, with the remaining 30% the courage to explore the uncertainties and test out our luck. Each one of our team member have shown the full 70% in dedication through their relentless effort to develop a flawless prototype, while maintaining communication and teamwork throughout the past six months. Another 20% goes to our willingness to try something that remained as psychology theories and engineering concepts until now. The final 10% is in trusting our luck in finding each others as team partners in this project. Thank you team!



## **6.5 Albert Su**

Who knew REM detection could be so difficult?

When our group was first formed in December of 2005, we had absolutely no clue what we were going to do for this project course. Many ideas were bounced between group members, and we were even very close on settling on a particular idea that almost seemed promising. Alas, someone brought up the question: “What if we can help people get more sleep?” After a bit of research, we found that no device on earth can help you get more sleep unless you are willing to cut back on other things in life. “What if you can wake up feeling better?” Well that question certainly did it, and committed us for the next six months.

All in all, this has been an interesting experience. From the initial conception, to research to planning and finally to development; it was pretty amazing how much we really accomplished. Neither of us knew what REM stage was besides having something to do with “very rapid eye movement”. During the initial planning phase, I had the opportunity to read many articles on sleep and on numerous occasions consulted a PhD student in psychology regarding this. Finally, we convinced ourselves that this will be the product that will forever change the world.

This project gave me the opportunity to experience first hand what its like to start a start-up company: sleepless nights, pressuring deadlines, accumulating bills. You probably don’t know who you truly are or what you are capable of doing unless you face these stressful conditions. Sometimes it can be very difficult to keep your emotions in check, but thankfully our group members were all very understanding.

What else have I learned? Although it sounds cliché, planning does go a long way. A lot of trouble and headache can be avoided if more time was taken to plan. Many quotes can be pulled from the web that tells you the importance of planning, but perhaps a simple “just do it” will suffice. Trust me. Another important aspect is communication – it is very important to keep that active at all times. Problems and uncertainties can be dealt with more effectively only if good communication exists. Also you won’t feel as bad if you know that other group members are spending their Friday nights working on the project as well.

## **7 Conclusion**

Over the past six months, Inglewood Jack Technologies have successfully developed a proof-of-concept model of the Smart Alarm Clock. Through the developmental phase, our team gained extensive understanding of the circadian rhythm and came up with innovative engineering solutions towards a functional Smart Alarm Clock. The completion of detailed marketing analysis as well as thorough functionality test promises market potential for the product, and our team is currently considering further development of a production model.



## **8 References**

- [1] “Functional Specification for a Smart Alarm Clock,” Inglewood Jack Technologies.  
February 2006.
- [2] “Design Specification for a Smart Alarm Clock,” Inglewood Jack Technologies.  
March 2006.