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February 2, 2006

Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, British Columbia
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Re: ENSC 440 Design Specification for the GKS Digital Hydra Octophonic Guitar Pickup

Dear Dr. Rawicz,

GKS Digital is in the process of designing a new means to connect an electric guitar to a home computer. This project, the Hydra Octophonic pickup, records eight streams of audio directly to a computer.

The purpose of this design specification is to detail the design that is required to satisfy the Functional Specification for the Hydra approved late last year. Due to our iterative design methodology, this document acts both as a guide and as an active document as development progresses. The snapshot that is attached is the design as of the functional prototype demonstration, and includes both current design as well as some forward looking design for the final production version. This specification is outlined in the attached document, *Hydra Octophonic Guitar Pickup - Functional Specification.*

Sincerely,

Eli Gibson

CEO

GKS Digital

Enclosure: Hydra Octophonic Guitar Pickup – Design Specification

cc: Mr. Steve Whitmore, Mr. Mike Sjoerdsma, Mr. Brad Oldham

Hydra

Octophonic Guitar Pickup

Design Specification

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Submitted to: Dr. Andrew Rawicz
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Mr. Steve Whitmore
Mr. Brad Oldham
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Executive Summary

Over the past two decades, a digital revolution in audio has shaken the professional recording industry to its foundation. The insatiable desire of musicians to create music combined with access to affordable recording technologies has caused a shift in the balance of power from the recording industry to the musician. Lower costs have caused the pool of recording artists to swell considerably and have allowed some of these home recording musicians to become superstars.

The GKS Digital Hydra Octophonic Guitar Pickup harnesses this trend, making it even easier for amateur and professional guitarists to record music at home. The Hydra is an electric guitar accessory that allows a musician to record signals from individual strings directly to a home computer, and manipulate these signals into the music of their creative fancy.

The development of the Hydra is at the end of the second development iteration. There is a proof of concept hardware prototype, with recording and audio analysis software. After the third iteration of development, GKS Digital will have a ready-for-market product, with feature complete hardware and software.

This document describes the design specification of the Hydra as of the end of the second iteration of development. It outlines necessary design constraints for hardware, firmware and software components.

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1. Introduction

The Hydra is an electric guitar accessory that allows musicians to record the sounds from individual strings directly to a home computer, and manipulate the sounds to fulfill their creative desires. The Hydra hardware can be installed in most electric guitars with minimal effort and modification to the guitar. The Hydra will come packaged with the user-friendly Chimera modeling software that allows the musician to effortlessly transform their guitar tone. The coupling of the Hydra hardware with the Chimera software will allow musicians significantly more freedom to create their music, their way.

As of the end of January 2006, the Hydra/Chimera prototype includes both a hardware interface to a guitar and modeling and analysis software. The timing for the commercial production of the GKS Digital Hydra is dependant on a number of external market factors.

1.1. *Scope*

This document describes the design requirements necessary to meet the functional specification for the Hydra. It is a snapshot of a dynamic design document that is modified as iterative design progresses. This snapshot includes both the current design solution as of the functional prototype demonstration, and some forward looking design considerations for future iterations and final product implementation.

1.2. *Intended Audience*

This document is intended primarily for design teams developing the system, or components of the system. While it can be used in its static form, it is intended as an actively changing document. A basic familiarity with reading datasheets is assumed, and appropriate datasheets are referenced when appropriate.

1.3. *Glossary*

ADC	**a**nalog to **d**igital **c**onverter, a device which converts continuous (analog) signals into quantized digital signals
ASIO	**A**udio **S**tream **I**nput/**O**utput is a standard developed by Steinberg to allow low latency audio processing of multi-channel audio.
Bit Clock	a clock signal with the same rate as the data source that is being transmitted
Chimera	GKS Digital's software package allowing recording and modeling of sound from a guitar equipped with the Hydra
FIFO	**f**irst **i**n **f**irst **o**ut refers to a buffer that outputs data in the same order it was input to the buffer.
GPIF	**g**eneral **p**rogrammable **i**nter**f**ace (I/F)

Hydra	GKS Digital's hardware interface which installs into an electric guitar
L/R Clock	a clock signal sent that is synchronized with time division multiplexing of the left and right channels of the audio data being transmitted
MB	**m**ega**b**yte, equivalent to 1,000,000 bytes
MBps	**m**ega**b**yte **p**er **s**econd, the transfer of 1,000,000 bytes or 8,000,000 bits of information every second
Mbps	**m**ega**b**it **p**er **s**econd, the transfer of 1,000,000 bits of information every second
Octophonic	a system having eight audio channels
Opamp	**op**erational **amp**lifier, a class of devices capable of being used as amplifiers, buffers and as part of many other useful analog circuits.
PC	a **p**ersonal **c**omputer
Piezoelectric	a physical effect which converts mechanical stress to electrical voltages within a crystal
Plugin	a software module that can be added to another application by an end user.
TDM	**t**ime **d**ivision **m**ultiplexing, a process in which multiple signals are broken into short time frames and then the frames are sent alternately from each signal along the same signal path.
TI	**T**exas **I**nstruments Inc., a manufacturer of a variety of semiconductor devices for a plethora of applications
USB	**U**niversal **S**erial **B**us, a computer industry standard bus for high speed serial communications between a device and a home computer
USB 2.0 Full Speed	a version of USB 2.0 equivalent to USB 1.1, which allows for sustained data transfers up to 12 Mbps
USB 2.0 High Speed	a version of USB 2.0 which allows for sustained data transfers up to 480 Mbps
Vendor Request	a USB control message that is specific to a given product

2. Specifications

2.1. *System Overview*

In a typical electric guitar the sound is produced from the metal guitar strings vibrating above a set of magnetic coils. The sum of the electric signals from the vibration of each string is sent over a conducting cable to the guitar amplifier where the signal is filtered and amplified to produce the final guitar sound.

The Hydra augments the capabilities of a standard guitar by allowing the vibrations of each string to be detected individually. The signal from each string is then digitized and transmitted over a USB connection to the player's computer. The Chimera software package then allows a musician to use digital filters to change the sound of their guitar to suit their creative needs. The Chimera software also interfaces with industry standard audio applications to allow further post-processing and mixing to create the final musical output.

The design of the Hydra is broken into several modules connected by inter-module interfaces. The basic modules and their interconnections are shown in Figure 1.

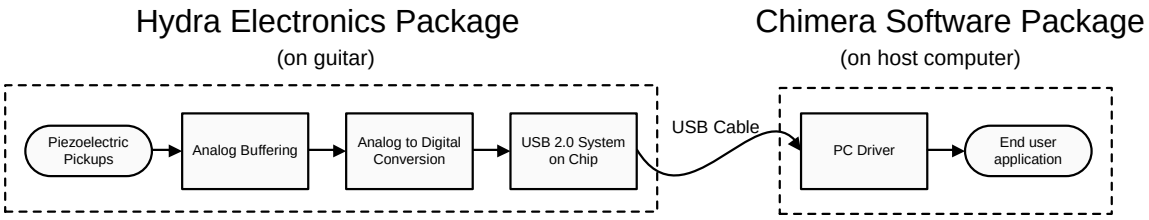

Figure 1: System overview

The individual modules and connections will be discussed further below. For details about the formats of the data in various modules, please see Appendix B.

2.2. *Hardware Design Specifications*

The hardware component of the Hydra is responsible for converting the analog signals coming from each guitar string into a digital representation and transmitting them to a computer over a USB 2.0 High Speed interface.

The hardware subsystem consists of a guitar bridge outfitted with piezoelectric saddles, an input buffer, a set of four analog to digital converters (ADCs), and a USB 2.0 System on Chip, as well as supporting hardware including power regulation and signal manipulation.

This section will describe the requirements of the hardware, and the proposed design to satisfy these constraints.

2.2.1. Hardware Requirements

The hardware must

- measure string vibrations and magnetic pickup levels,
- sample the aforementioned signals at 96kHz, 24 bit resolution,
- minimize noise and distortion in the recorded signal,
- transmit the recorded signal over the USB,
- consume less than 500 mA.

2.2.2. Piezoelectric Pickups

The system receives audio signals from the guitar through piezoelectric transducers installed in the guitar's bridge. The Graph Tech "Ghost" bridge system [1] comes in a variety of different physical configurations suitable for use in a large number of guitar types. The pickups are capable of output voltages well above 5 V under heavy playing and are suitable for representing a large range of dynamics without requiring any amplification. The signal from each string is transmitted along a wire passing from the bridge in to the body cavity of the guitar.

2.2.3. Instrument Signal Buffering

The signals from each of the piezoelectric pickups must be buffered to prevent loading by the ADC inputs. The buffering is accomplished with high-speed low-noise operational amplifiers (opamps) designed for professional audio applications. The selected opamp is the TI OPA4350 [2] which provides four independent channels and provides precision, low-noise amplification in a small package. The output power spectral density of the noise from the opamps is specified as 5 nV / Hz at 1 kHz. The opamps are configured in a negative feedback unity gain configuration with the input level centered around 2.5 V through the use of a voltage divider. See the hardware schematic in Appendix A for details.

2.2.4. Analog to Digital Conversion

To ensure maximum audio fidelity in the digital recording, high-quality audio analog to digital converters must be used. The TI PCM1803 [3] was selected for its high quality output with lower passive part requirements and lower costs than competing solutions. This chip can accept several different input clocks depending on the desired sampling rate and quality. The Hydra uses the highest audio conversion quality available by providing a 36.864 MHz clock rate, resulting in a 96 kHz sampling rate. Each PCM1803 chip is capable of simultaneously converting two channels of audio so four chips must be utilized on the Hydra.

2.2.4.1. PCM 1803 Setup

In order for the four ADC chips to work in parallel, they must be synchronized. The PCM1803 provides for this by allowing one chip to act as a master and the others as slaves. In the slave mode, the L/R clock and bit clock output pins become high impedance inputs and are used for synchronization of data transfer. The L/R and bit clocks of the master ADC are then connected to the L/R and bit clock pins of the three slave converters as well as the USB chip to allow the data transfers to be synchronized.

Table 1 shows the necessary control settings for the desired operational mode of the PCM1803 converters:

Pin	Mode 0	Mode 1	FMT 0	FMT 1	BYPAS	OSR
Setting (Master)	0	1	1	0	0	0
Setting (Slave)	0	0	1	0	0	0

Table 1: ADC control settings

The mode settings set the master ADC to master mode with a 384 x 96kHz clock rate, and the slave ADCs into slave mode. [3 (p. 12)]

The format settings set the ADCs in to "MSB first I2S" data format mode [3 (p. 13)]. This data mode was selected to allow the system to recognize the change of the L/R clock on one cycle and begin recording on the following cycle to appease the state machine requirements of the USB chip. The details of the state machine are described in the firmware section of this document.

The bypass pins are set low in order to utilize the ADCs' built in high pass filter to reject any DC offset in the signal.

The oversampling feature is disabled since it is not available on the PCM1803 concurrently with the 96 kHz sampling rate used in the product.

2.2.5. USB 2.0 Microcontroller

The USB 2.0 Microcontroller must be able to read the incoming data from the ADCs and convert that data into a datastream to be sent via the USB 2.0. Currently, the only suitable microcontroller to meet the functional needs of the Hydra is the Cypress CY7C68013 EZ-USB FX2™ USB Microcontroller [4,5] (USB Microcontroller). The following requirements must be met by the selected chip:

- 6 high speed digital input pins for the following signals: ADC data 1-4, Bit Clock, L/R Clock,
- USB 2.0 output,
- USB bus-powered operation,
- System on Chip.

As shown in Figure 2, the USB Microcontroller is capable of receiving the ADC signals through its General Programmable Interface (GPIF) port.

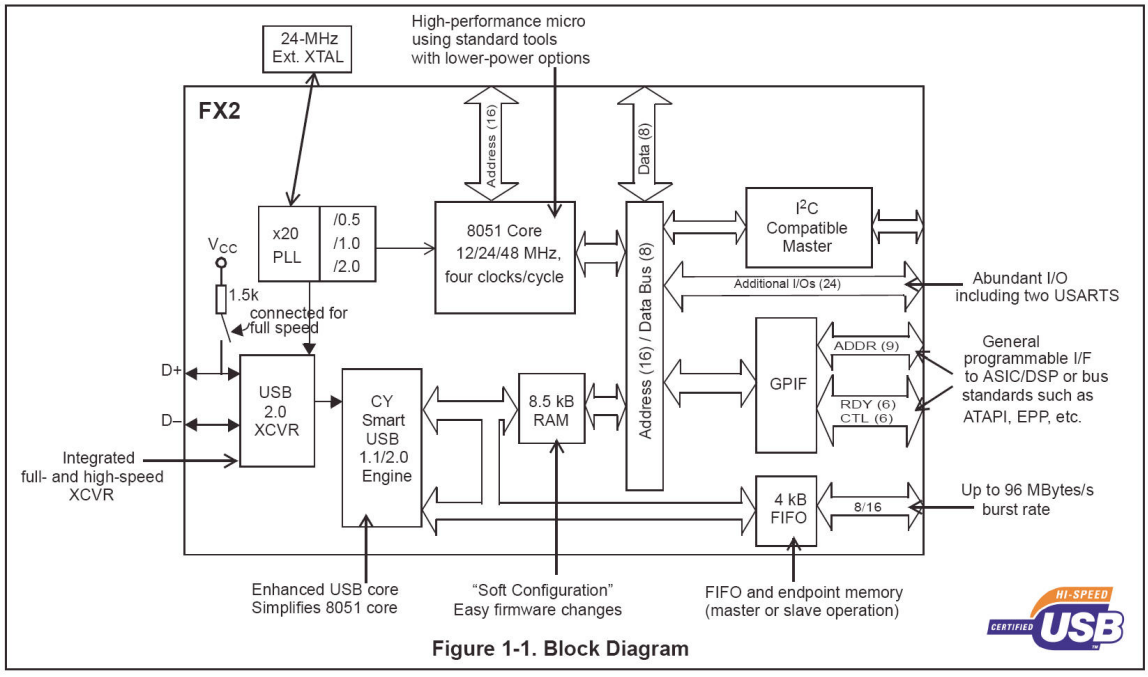

Figure 2: CY7C68013 USB Microcontroller block diagram. [4]

The chip is also entirely self-contained and requires only a 24 MHz external clock source as supporting hardware.

2.2.6. Clock Generation

Two different clock signals are required by the system. The USB Microcontroller uses a 24 MHz crystal in a parallel configuration as the oscillator for an internal clock generation circuit. The ADCs require a variable clock frequency depending on the desired sampling rate, 48 or 96 kHz. The TI PLL1707 [6] dual phase locked loop clock generator allows generation of the necessary clock frequencies and also allows the frequency to be varied during operation. This may be important if a future design implements hardware downsampling. Table 2 shows the important characteristics of the clock subsystems.

Device	Clock Frequency	Configuration	Capacitance
USB Microcontroller	24 MHz	Parallel	22pF
Clock generator	27 MHz	Parallel	22pF
ADCs	12.880 or 36.864 MHz	3.3V input	n/a

Table 2: Clock Subsystem characteristics

2.2.7. Power Supply

The power supply must operate off the 5V power line available through a standard USB 2.0 port. In order to allow all the devices in the circuit to operate, the supply needs to provide voltages of: ground, 3.3V and 5V. The current and ripple characteristics of the power supply should fulfill the requirements of the table given in Table 3.

Supply Voltage	Current Limit	Expected Draw	Peak to Peak Ripple (peak to peak)	Ripple Frequency	Nominal Efficiency
3.3V	500 mA	300 mA	< 20 mV	>400 kHz	>65%
5.0 V	150 mA	60 mA	< 20 mV	>400 kHz	>90%

Table 3: Power supply characteristics

The 5.0 V power rail must provide clean power with an absolute minimum of ripple and noise below the audio sampling rate of 96 kHz. The USB 2.0 interface is able to provide a minimum of 500 mA of current at a voltage which may drift from 4.25 V to 5.0 V depending on the characteristics of the load and the host interface. The power supply must deal with this potential voltage change without impeding the operation of the Hydra. The following chips listed in Table 4 meet the above specifications and could be used within the power supply.

Description	Manufacturer	Part Number
3.3V LDO with reset	TI	TPS7330[7]
5.0V Stepup regulator	Maxim	MAX1724[8]

Table 4: Power regulation chips

Figure 3 shows the block diagram of the power supply design.

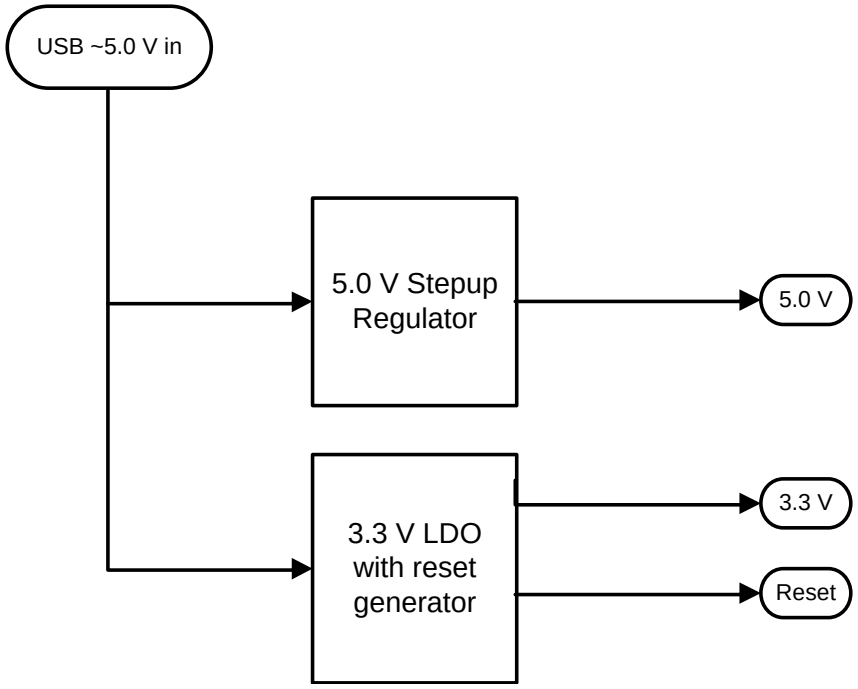

Figure 3: Power supply design

2.2.7.1. Power on Delay

In order to prevent overloading of the host USB 2.0 interface as well as potentially damaging various components, the main circuitry of the Hydra is not to be powered on until after the power supply voltages have stabilized. The power on sequence is shown below in Figure 4.

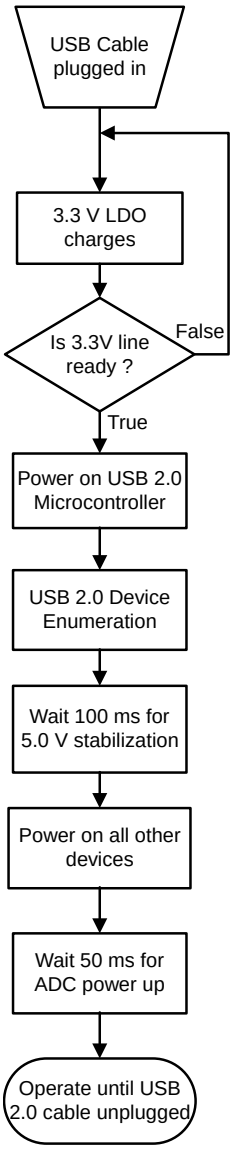

Figure 4: Power on sequence

2.2.8. Hardware Digital Logic

Some digital logic circuitry is required in order to maximise the data throughput of the GPIF in the USB Microcontroller. Since the ADCs provide 4 outputs, but the GPIF records in 8 bit blocks, there must be interconnecting logic to delay the ADC outputs, allowing 2 bits per ADC to be recorded each read. While a full cycle delay would be optimal, it is possible, and cheaper to implement this with a half-cycle delay. For implementing the half-cycle delay, the TI SN74HC175 [9] flip-flop is utilized, as its timing characteristics allow a half-cycle implementation.

2.3. *Hardware Interfacing*

2.3.1. Instrument to ADCs

The piezoelectric pickups must be buffered as the input resistance of the ADCs would otherwise load them. Amplification is not necessary as the pickups are capable of outputting signals in excess of 5V peak to peak. Care should be taken to design the preamplication section so as to minimize harmonic distortion and noise.

2.3.2. ADCs to USB Microcontroller

Once the ADCs have converted the signals to digital form, they must be delivered to the USB Microcontroller. The USB Microcontroller needs the data itself, as well as 2 clocks that allow for synchronization with the data. The bit clock connects to the GPIF clock. The L/R clock connects to the READY control input of the GPIF. The half cycle delay is used to maximise the data throughput, as discussed above. The four data signals are taken one from each ADC data output pin. The block diagram of the ADC to USB Microcontroller interconnection is shown in Figure 5.

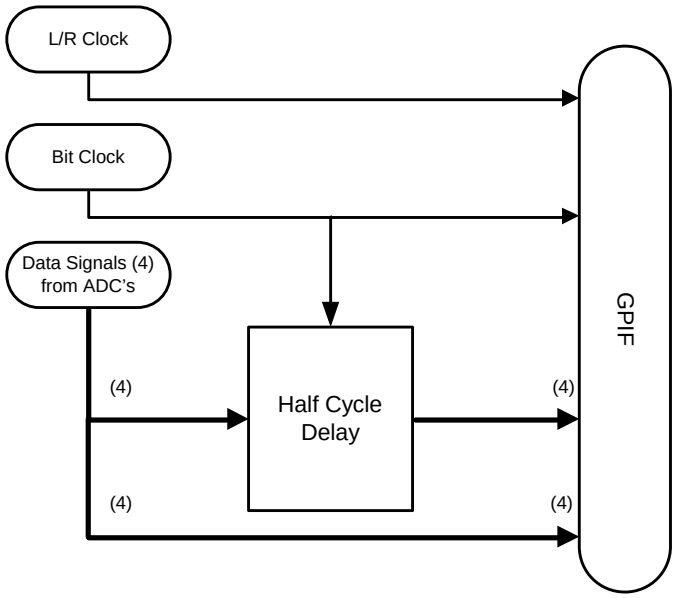

Figure 5: ADC to USB Microcontroller interconnection block diagram

2.3.3. USB Microcontroller to Host Computer

The USB Microcontroller connects to the host computer via a standard USB 2.0 certified B-to-A cable. The B connector in the Hydra will be connected to the Hydra PCB via a ribbon cable to allow for flexible mounting within the guitar as per the user's preference.

2.4. *Firmware Interface Specifications*

This section will describe the requirements of the firmware, and the proposed design to satisfy these constraints.

2.4.1. Firmware Requirements

The firmware must be able to

- record data clocked by the Bit Clock signal from the ADCs,
- keep the data aligned so that the beginning and ending of the data samples is recoverable,
- maintain a throughput of 3.072MB/s,
- recover if the host computer does not maintain this throughput, and
- start and stop recording at the request of the host computer.

2.4.2. Firmware Architecture

The USB communication firmware is made up of 2 components: the application framework to handle the high speed data throughput, and the USB framework to process non-data USB messages. The firmware architecture is shown graphically in Figure 6.

2.4.2.1. Application Framework

The Application Framework is further comprised of 2 components: the serial interface engine (SIE) to send data to the host computer over USB, and the General Programmable Interface (GPIF) to collect data from the ADC hardware.

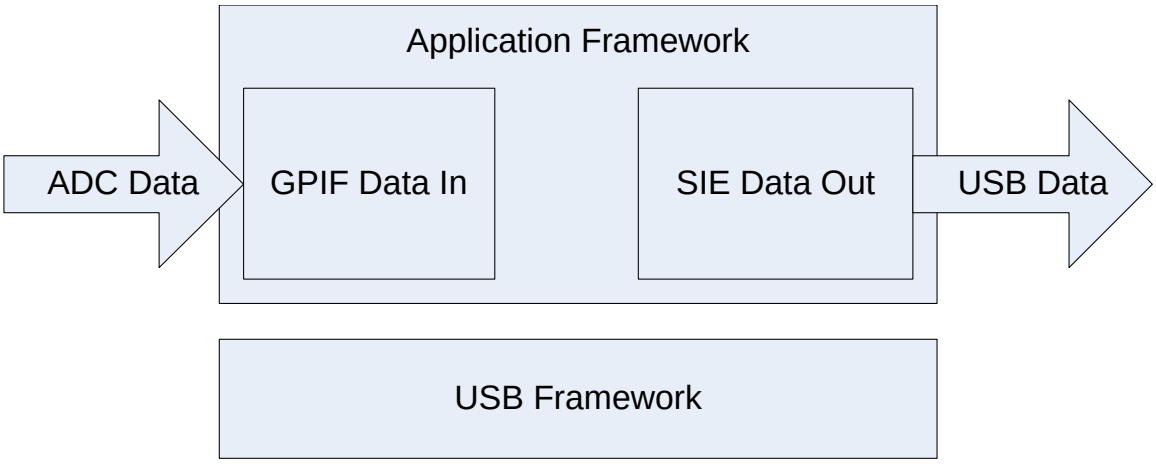

Figure 6: Firmware Architecture

2.4.2.2. SIE

The SIE handles the USB data communication. It takes First In First Out (FIFO) buffers that have been filled and committed (queued for sending) and sends them across the USB. In this implementation, the FIFO buffers are configured to hold four 768 byte packets. This quad-buffering prevents data loss due to synchronization problems between the computer and the USB Microcontroller chip. These packets are automatically committed when the last data byte is set, and are sent when the host computer requests the data. The format of the packets is discussed in Appendix B. The USB communication uses the low-bandwidth, high-speed isochronous mode [5 (p. 1-6)]. Low bandwidth refers to the use of one packet per microframe. High speed refers to the use of 8 microframes per frame, or 8000 microframes per second. The USB isochronous mode eliminates much of the communication overhead of the USB specification, and guarantees a minimum throughput, at the cost of reduced error checking. This communication mode has a theoretical maximum throughput of 8.192 MB/s, which is sufficient to transfer the 3.072MB/s required for our application.

2.4.2.3. GPIF

The GPIF is a state machine that is run on dedicated hardware, independent of the internal clock of the USB Microcontroller. It is clocked using the bit clock of the ADCs. It consists of 4 stages: *SyncL*, *Sync*R, *ReadData*, and *Pause*. The *SyncL* and *Sync*R stages ensure that the data is collection is synchronized with the L/R Clock from the ADCs, and that the USB Microcontroller buffers are not all full. The *ReadData* and *Pause* stages collect data at every other clock cycles, to allow the delay buffer to fill. The stage machine is shown in Figure 7 as a state flow diagram. The value *FifoFull* is an internal value jointly controlled by the GPIF and SIE which is set high when all 4 buffers are filled. The value LRCLK is an external value read from the ADCs' L/R Clock line. Each rectangle is one stage, which occupies one cycle of the ADCs' Bit Clock.

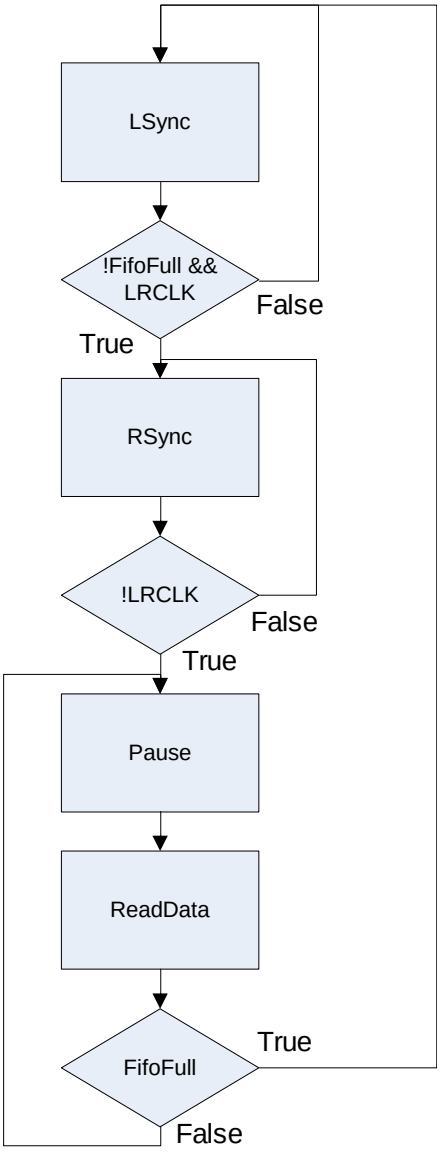

Figure 7: GPIF state flow diagram

The standard operation of the GPIF state machine is to synchronize to the falling edge of the L/R Clock signal and then alternate between *ReadData* and *Pause* for the duration of recording (controlled externally). There are situations where this does not occur. When the buffers become full, the *ReadData*/*Pause* cycle is aborted, and the state machine returns to the synchronization phase. Since the data continues to arrive while this synchronization occurs, some data loss occurs. Because the state machine is resynchronized with the L/R Clock signal, the data loss will be an integer multiple of samples from each of the 8 channels. This data loss should not occur during normal operation, due to the guaranteed throughput of the isochronous USB mode; however, it can occur if problems occur on the host machine. The GPIF state machine is started and stopped by the USB Framework discussed below.

2.4.2.4. Data Interconnection

The GPIF and SIE pass data through high bandwidth connections to the USB Microcontroller FIFOs. USB Microcontroller hardware controls the status flags that prevent data from being overwritten (*FifoFull*), and that automatically commit the data to be sent across the USB when a firmware defined amount of data has been recorded.

2.4.2.5. USB Framework

The USB Framework handles some of the low level details of the USB specification, including the standby mode control, enumeration, and handshaking protocols, as well as the high level device configuration, recording controls, power reset controls. The low level functionality is handled by the USB Microcontroller framework, provided by Cypress. The power reset controls are handled in the initialization phase of the firmware. The USB Microcontroller uses the output pin PA1 to trigger the reset chip. For the purpose of the prototype, the power rest controls are not implemented as the development board power system is sufficient. The high level recording controls are implemented through the use of Vendor Requests, simple control messages that are dependant on the peripheral firmware. There are 2 Vendor Requests needed: one to trigger recording, and the other to stop recording. These are assigned Vendor Request codes 0xB6 and 0xB7 respectively. The handler of the request to trigger recording must ensure that recording is not currently occurring, and then start the GPIF state machine. The request to stop recording must abort the GPIF state machine, and clean up all the remaining data, including clearing the unsent and unfinished FIFO buffers.

2.5. *Software*

2.5.1. Software Requirements

The software consists of 2 components, the driver and the user applications.

The driver must be able to:

- actively poll the USB host with a sustained frequency greater than 8kHz,
- transform the USB packets into a usable data format,
- store the data in a usable form that allows low latency.

The user application will vary greatly. For the purpose of the functional prototype, the software must be able to:

- accept data from the driver,
- manipulate the audio to demonstrate the strengths of the Hydra,
- record raw data for verification purposes.

2.5.2. Software Architecture

The software subsystem is comprised of a series of data paths from the USB, through a driver, through a host application, then through modeling algorithms. The data format and characteristics at each of these stages are described in Appendix B.

2.5.2.1. Host

Although not a part of the Chimera product, the host should be mentioned briefly for completeness' sake. The host software is one of many audio applications which supports ASIO drivers, and audio effect plugins. They allow recording of one or more channels of audio from a driver and handle the audio processing and final mixing of the audio. The host contains the user interface that the user interacts with, including mechanisms for loading the Chimera driver and the Chimera audio plugins. The initialization and recording of the Chimera driver is controlled by this host application.

2.5.2.2. Driver

The driver handles USB communication on the host computer, translation from the hardware format to the final audio format, and interfaces with the host application. In order to allow 8 channels of low latency audio, and to allow interfacing with industry standard host applications, the driver should eventually be implemented as an ASIO driver. For the purposes of the functional prototype, however, the driver shall be included as a source code module compiled into various applications.

When the host application instructs the driver to initialize, the driver must enumerate the USB devices on the host computer to find the Hydra, and then connect to the device. When the host application instructs the driver to start or stop recording, the driver must send appropriate Vendor Requests to the Hydra.

During recording, the driver rapidly polls the USB interface for isochronous data packets. In order to ensure constant data collection, the driver should be written to use the asynchronous transfer mechanism of the CyAPI. This allows processing to occur while the USB driver continues to wait for more data. The driver receives data in 768 byte packets, containing 32 samples per channel for a total of 576 bytes of usable information per packet. The data packet is translated to remove the meaningless components, and to split the interleaved channels into 8 separate channels.

Once the data has been collected, the driver converts the data into a standard audio format. Generally this will be 96kHz 24bit PCM audio, although it may vary from application to application. In the production driver, the results will be written directly to the ASIO communication buffers to minimize the latency. At the request of the host application, the driver can downsample the audio (by integer factors), and decrease the resolution. In the prototype, however, the data will be recorded into application specific processing buffers. Furthermore, in the prototype no resolution changes will be implemented.

2.5.2.3. User Application: Prototype Demonstration Software

The prototype demonstration software will show the advantages of the octophonic output for audio analysis, specifically pitch detection. The software will detect the lowest harmonic on each string. It will translate this into MIDI control messages for notes as well as pitch bends.

The pitch detection will use the YIN algorithm [10] on a downsampled version of the audio stream. The audio stream will be downsampled to 6 kHz which allows enough precision to differentiate to within a semitone, sufficient for determining which fret is being played. In order to capture the necessary frequency range (82Hz-1250Hz), the algorithm must be calculated over at least 33 ms, or 200 samples.

The MIDI control messages can be generated using the WIN32 API MIDI function, combined with software MIDI loopback software. These control messages can then be fed into any application that accepts MIDI in.

3. Conclusion

GKS Digital is committed to producing high-quality, flexible and easy to use music equipment. This document has set out the design specification for the Hydra and Chimera product, sufficient to meet our commitment to excellence. These specifications encompass both a hardware interface to be attached to a guitar, as well as a software package to give musicians significant flexibility . With the functional prototype implemented with these specifications, GKS Digital has met its commitment to complete of the first two stages of development. The development of a final product encompassing the full set of specifications will be completed at a later date, pending appropriate circumstances.

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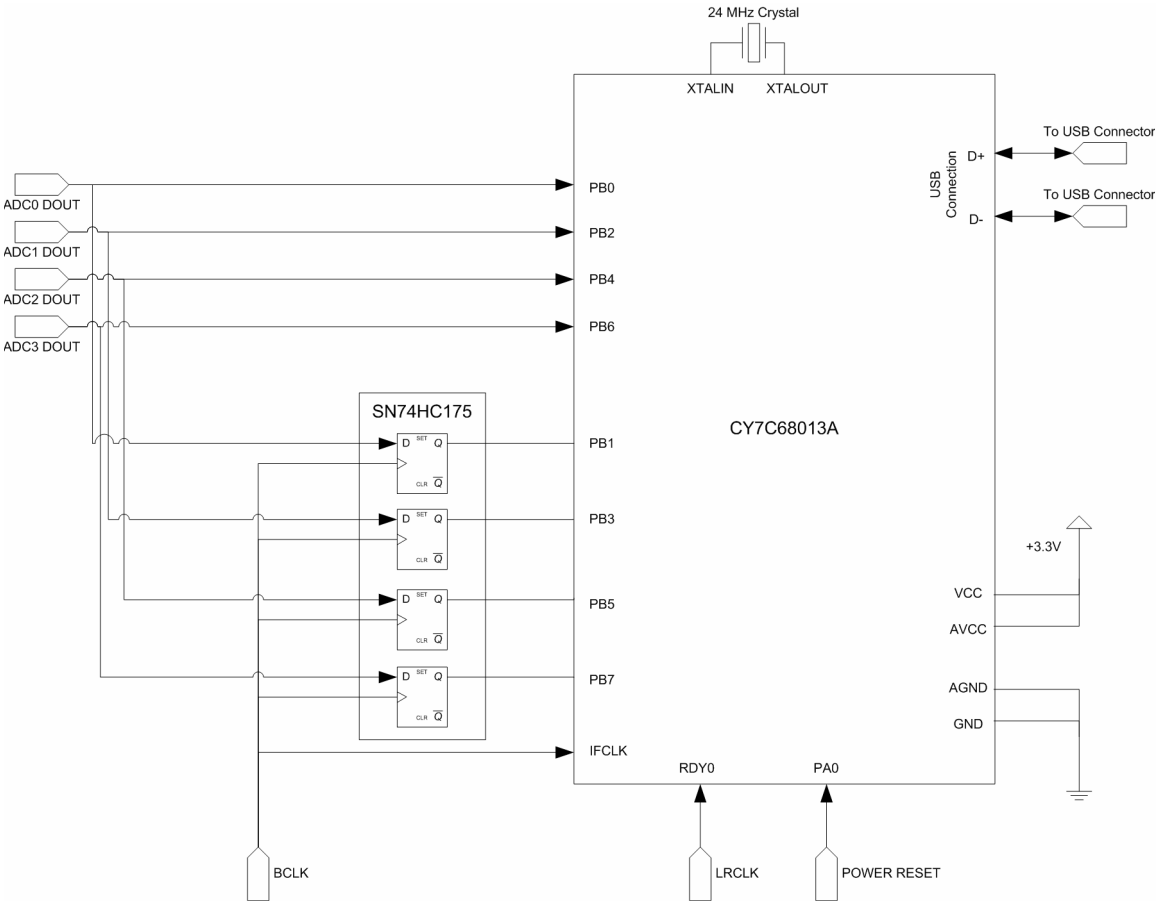
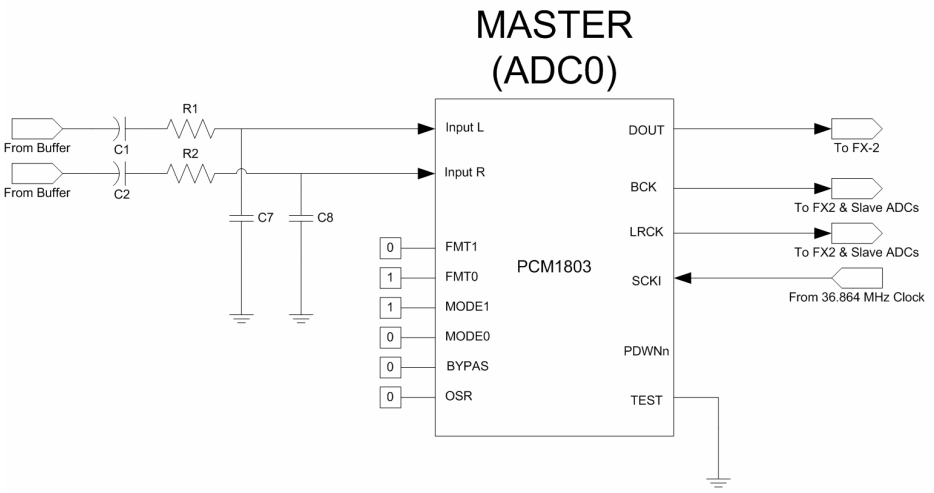
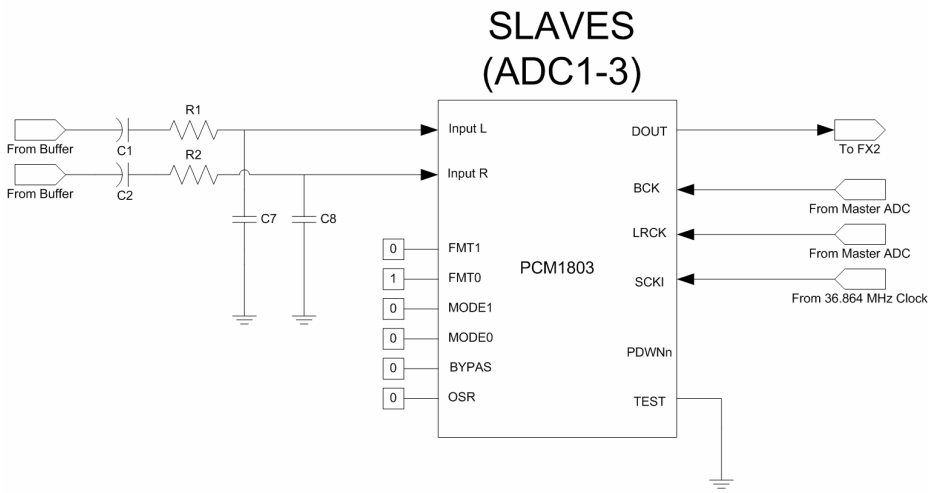
5. Appendix A: Schematics

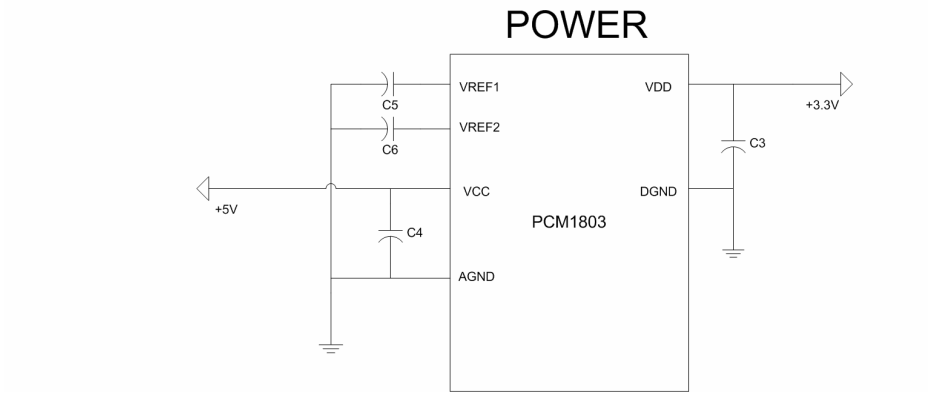
5.1. *FX2 I/O and Supply Schematic*



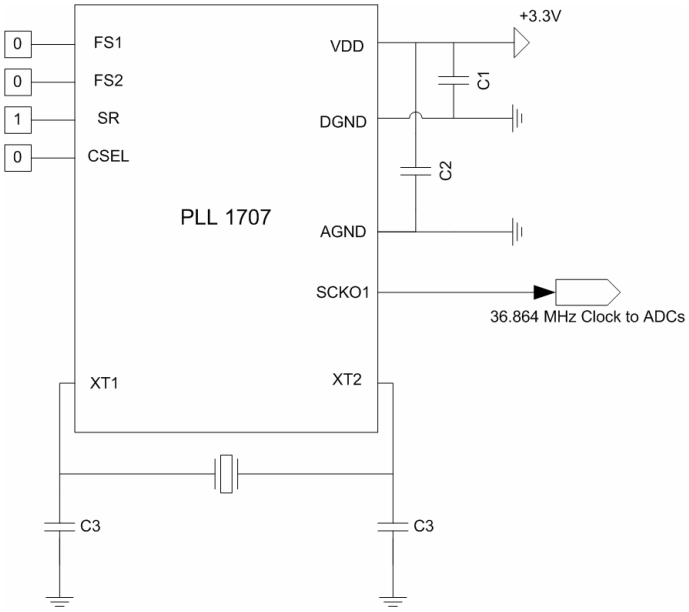
5.2. *ADC Schematics*



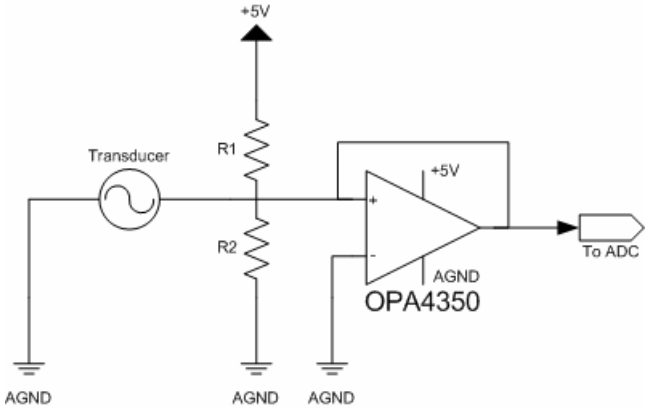




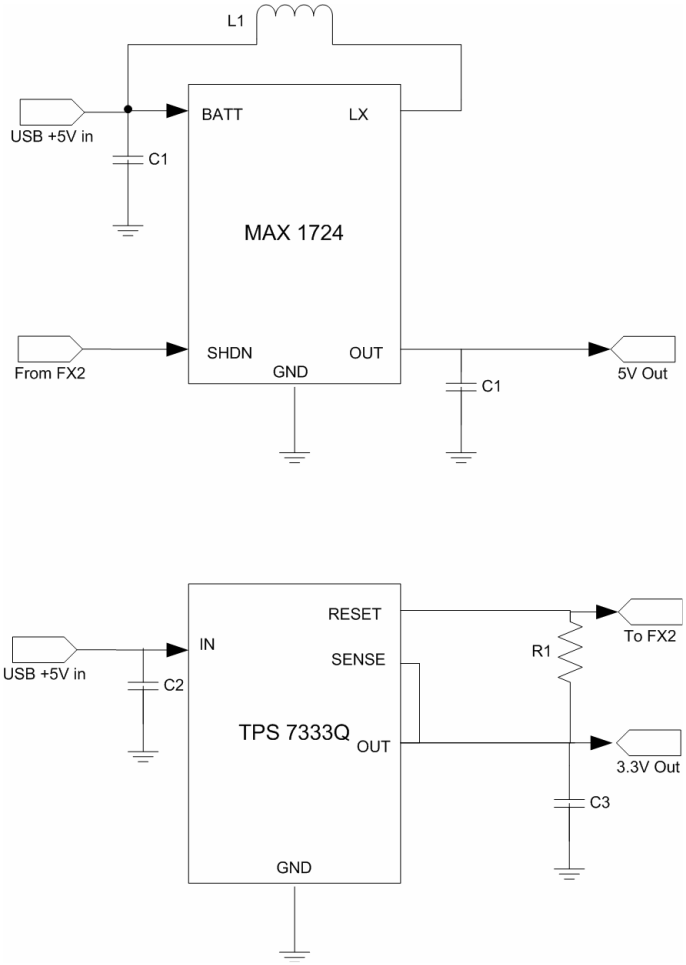
5.3. *Clock Generation Schematic*



5.4. *Input Stage Schematic*



5.5. *Power Supply Schematic*



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6. Appendix B: Data Flow and Formats