FORTRESS SYSTEMS

POST MORTEM

TO:

Dr. ANDREW RAWICZ

Dr. MIKE SJOERDSMA

FROM

MAIKEL SAAD

JOHNSON LAM

PATRICK BEAULIEU

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1.0 INTRODUCTION:

1.1 Document Scope:

The following document outlines the limitations encountered throughout the semester due to many constraints, which include time and hardware constraints, and how solutions were established. However some solutions required diversion from the original plans which were discussed in the functional specification and the design specification documents. Furthermore this document outlines each team member's experiences as well as fortress systems future plans.

1.2 Intended Audience:

This document is intended to be viewed by primarily course Instructors and professors for evaluating the performance of our project. It will be also used by engineers within safe fortress systems for future development.

2.0 Background and Motivation:

One would not expect the deaf community to be large, but according to statistics collected in the USA consensus in the year 2000, there are 6.5 million people who are profoundly hard of hearing in North America. Such a huge market is in demand for innovative solution to their many every day challenges. One of the many challenges which face the deaf community is one's awareness of the surrounding environment. Such limitations expose the deaf and hard of hearing alike to, among many problems, a lack of safety. Therefore fortress systems accepted the responsibility of improving the safety of the hard of hearing and deaf. Fortress systems initial product enhances the safety and awareness of the deaf and hard of hearing.

3.0 Overall System Description:

At the final stage of our Sense Vibe project development, we have a few changes to our project design while maintaining the primary functionality. Our project consists of a system that requires microphones as input, operational amplifiers acting as signal conditioners, a digital signal processing micro controller and vibrating motors as output feedback component. Figure 3.1 illustrates the operation flow of our Sense Vibe; the details regarding each process block will be discussed in the following subsections.

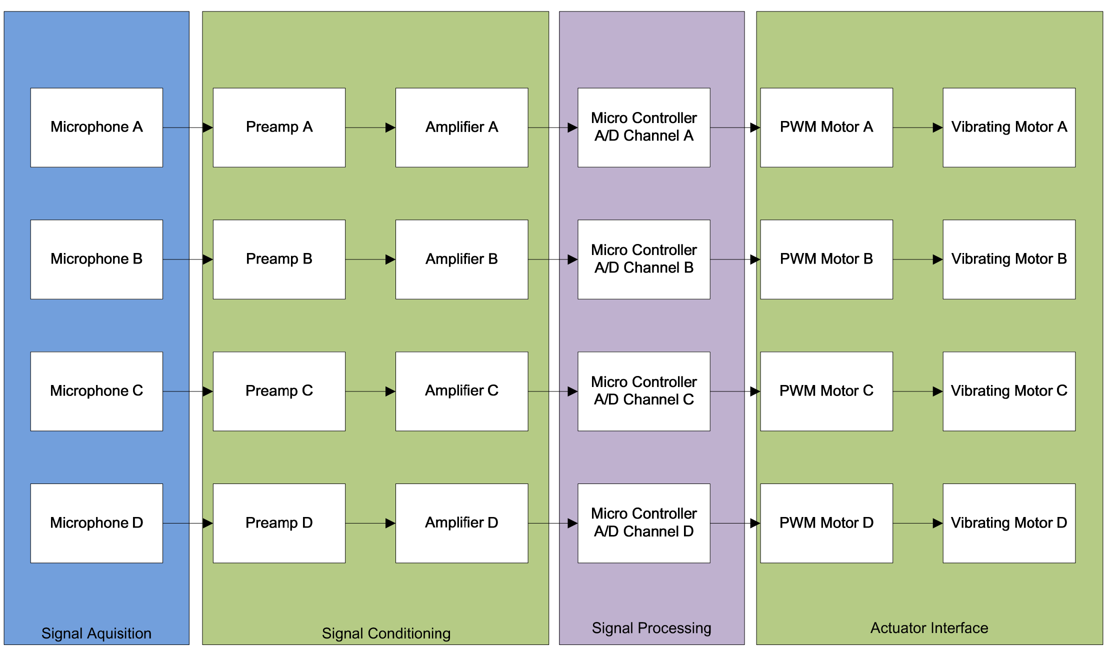

Figure3.1: High Level System Overview

3.1 Signal Acquisition

To allow the Sense Vibe system to recognize the actual environment, there will be passive input signals into our four unidirectional microphones with predefined orientations as illustrate in the following figure. The microphone signals will be filtered and pre-amplified into a more stable AC output signal (approx. 0.7Vrms)

3.2 Signal Conditioning

The AC signal output from the preamplifier will require 2 stages signal conditioning. The first stage will be signal amplification where each of the four channels signal will be amplified into +2.5V and -2.5V signals. This approach is to maximize the A/D converter reading within the microcontroller. After the small signal amplification stage DC offset will be applied to the signal. This second stage will bring the input signal into 0V to +5V for the microcontroller for the quantization procedure and prevent the A/D converter from damaging.

There is a variable resistor for DC offset biasing to the second stage; this adjustment will enhance the system stability by setting the DC offset voltage in the closest approximation in the center of the A/D converter range. As long as the A/D converter is reading +2.70 V when no inputs are detected by the microphones, the actuator system should be in idle mode.

3.3 Signal Processing

The signal is processed in real time at a sampling rate of 10 KHz. The input from each microphone is amplified, filtered, and shifted upward in order for it to be fed into the microcontroller. in addition, the input from each microphone is integrated to find the signal power for a fixed window, which is then processed with a threshold to determine if a motor should be on/off during window period.

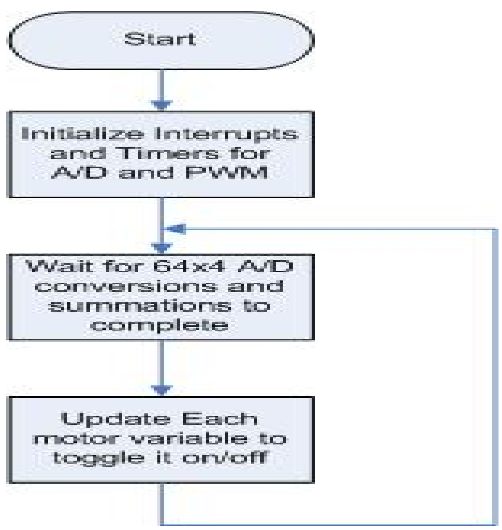

Figure 3.2: Signal Processing Overview

3.4 Actuator Interface

The actuator interface consists of a motor driver and four vibrating motors. Vibrating motors are mounted below each of the corresponding microphones to indicate the sound direction. In this subsystem, the motor driver is operated by PWM signals and will drive each of the four 2N3904 NPN transistor in saturation mode. By varying the bandwidth of the pulse, the powers that deliver to these motors will be under control. To prevent overloading to the motor driver, the base resistors limit the current draw of 63mA (instead of 100mA rated) through the motors and transistors. There are one diode being placed across the collector and emitter of each NPN transistors, these prevent the high voltage spikes that are generated by the vibrating motors at the instant of startup.

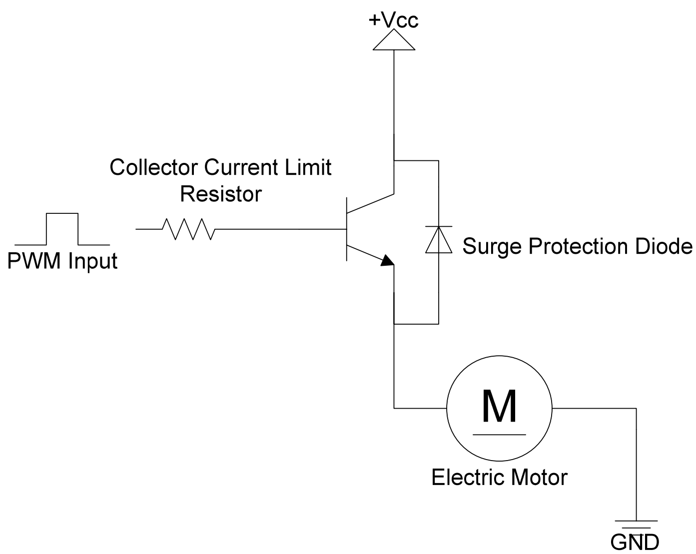

Figure 3.3: PWM driver circuit diagram

4.0 LIMITATIONS AND SOLUTIONS:

During the design process of an electronic device many issues and surprises arise. A solution is required for each problem encountered. Such solutions may require deviation from the original plans and therefore the finished product is different from the planned product. Fortress systems encountered many of such issues mainly due to hardware limitations.

The HC11 microcontroller used has a low clock rate. This limited the software developers in terms of optimization and the integration of additional features due to the need for efficient and short code. Such limitations decreased the quality of the final product as well as contributed significantly to the difficulty of the development of the code. Such limitations also deprived the developers of the ability to sample at the nyquist rate for human speech, which is 44 KHz.

The microcontroller only allowed a sampling rate of 10 KHz, which in turn prevents the system from recognizing input to the microphones of frequency higher than 5 KHz. This causes a severe limitation due to the fact that human speech is in the range of 20 Hz to 20 KHz. To solve this issue, fortress systems decided, in the future, to utilize a processor at a sufficient speed for an optimal final product.

Another key factor in the lack of optimality of the final product is the lack of directionality of the microphones as well as the echoes and reverberations experienced indoors. Such limitations could be avoided by utilizing microphones with better directionality.

5.0 FUNCTIONAL DEVIATIONS:

Due to the constraints upon the resources available to the developers in the design process, deviations from the planned product are necessary. Fortress systems found a necessity to deviate from the functional specification due to time limitations. Fortress systems decided, during the design process, to disregard the user interface originally planned. Furthermore fortress systems decided to continue without the time averaging of threshold adjustment.

6.0 DESIGN DEVAITIONS:

During the design process, among many issues that arise, there are many subtle points the developer recognizes as a key addition to the product. Fortress systems encountered such subtle points as the need to add a fourth channel in the system. Such a channel includes a fourth microphone as well as a fourth motor. However there were deviations from the design specification for the sampling rate due to the limitations on the microcontroller described above. The sampling rate utilized is 10 KHz rather than the one originally planned which was 44 KHz.

7.0 FUTURE IMPROVEMENTS AND PLANS

Due to the many surprises and issues that arise during the design process, fortress systems has considered many improvements to its design procedure. Such procedures include careful planning, early and frequent testing, as well as many early attempts at integration.

8.0 BUDGET AND TIMELINE:

8.1 BUDGET:

Fortress systems' budget outline as planned versus the actual outcome is best described in Table 8.1. The deviation of the actual from the planned is due to the fact that the developers did not foresee the need for an amp and preamp stages in the system prior to the design process.

Item	Estimated	Actual
Uni-Directional Microphones	$30	$16
Pre-Amplifier	N/A	$20
Signal Amplifier	N/A	$10
Vibrating Motor	$20	$18
68HC11 Micro-controller DEVL. Board	Free	Free
Arm Attachment	$20	$16
Misc. Expenses (Shipping etc)	N/A	$10
Total:	$70	$90

Table 8.1: Budget outline for planned versus actual

8.2 TIMELINE:

Fortress systems faced many challenges due to the time constraint for this project. For future development, fortress systems will plan the allotted time more carefully as well as increase the time available by initializing the design process early. The timeline for this project as was planned versus the actual is best described through Figure 8.1.

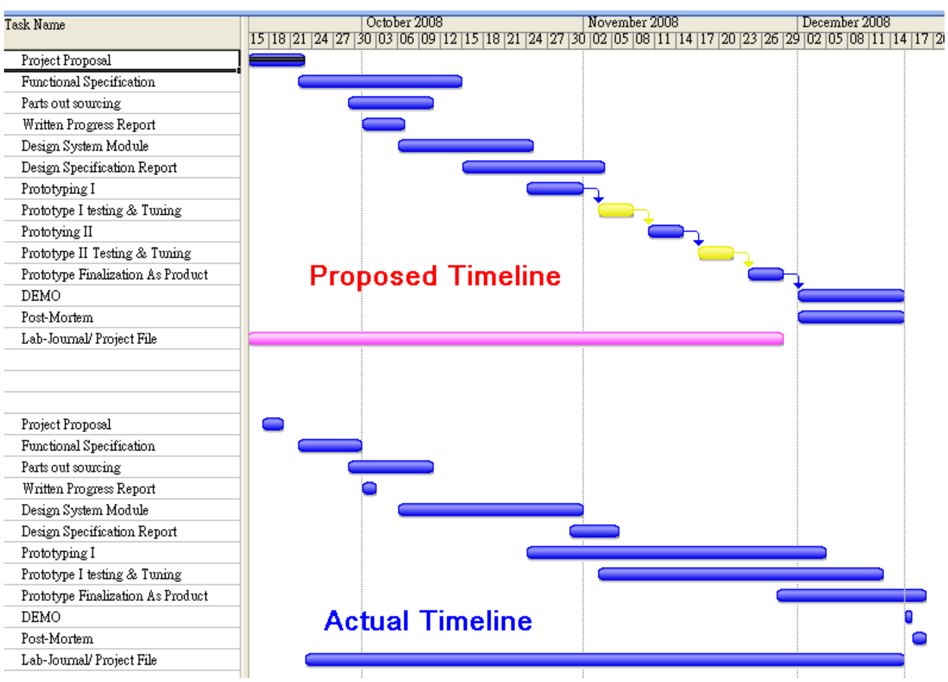

Figure 8.1: proposed and actual timeline

9.0 INTERPERSONAL AND TECHNICAL EXPERIENCE

9.1 MIKE SAAD:

This project has taught me many lessons. I learned to finish the assigned tasks on time otherwise the group will fall behind and there will be less time to optimize the final product. Also I learned to do every assigned task despite time constraints otherwise the group's trust in my ability to perform in the beginning will be destroyed. Such a loss in trust will cause my workload and therefore my contribution to the project to decrease as the project progresses, which in turn will make me useless and destroy group dynamics. I also learned to better plan my time.

9.2 JOHNSON LAM:

As the project progresses there were interesting and unexpected challenges ahead of me. The time that was spent on the project was much more than I anticipated. I believe the preparation of the project was insufficient and have caused the hardware design ended in a bottleneck situation. The hardware selections indeed can be revised to optimize the current system performance but it requires much more extensive research that my small group cannot handle within the allowable time.

Team dynamics is another experience I have gained after this project. I understand that if every member in the group is working properly and complete their tasks in the given time, the more time we can fine tune the current project settings or make more appropriate changes of its design. However, in reality unexpected things do occur and we have to prepare to encounter any possibility of significant delay

9.3 PATRICK BEAULIEU

As I mentioned in our presentation, I found out that it is very important to plan ahead for 440/305 before you take it. Having a group and a solid project idea ahead of time would have helped a lot. Initially we struggled to get a project idea that met the class requirements and was suitable for completion; that got us behind in the first couple weeks due to our rejected proposal. Fortunately, after that we came up with a solid feasible idea that could be accomplished with minimal resources. In hindsight, it may have been better to choose more modern hardware to implement our idea but our familiarity with the old HC11 helped our accelerated development process.

I also learned a lot about team dynamics. I've been in many group projects before, but never in a very dysfunctional group. In the end, I was forced to learn how to handle bad group situations.

On the technical front, I was able to reacquaint myself with the HC11 and assembly language coding. I also got a good taste of the necessary requirements in a real-time embedded system. It was a positive experience being able to create a product/device in an end to end way, from concept to design to implementation. Also, being able to apply coursework in the bigger picture rather than small specific pieces was a good experience. Seeing my signal processing theory, my embedded systems knowledge and electronics experience come together to make a larger system was a great affirmation of the things I have learned throughout my time here at SFU.

10.0 CONCLUSION:

Fortress systems has learned many lessons from the development of this project. The lessons learned range from team dynamics to hardware selection decisions to better planning. Although there were some disfunctionality in the team dynamics, fortress systems has managed to complete the task at hand and learn to avoid such team dynamic problems if they do arise in the future. Fortress systems has learned that it is very important to make well-planned hardware decisions prior to the design process as well as to increase the allotted time as much as possible.