
mnemosyne
Innovations Incoporated
CheckList™
Assistive Memory System

The Mnemosyne Team

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Chief Executive Officer

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Chief Operations Officer

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Chief Technical Officer

Surbhi Seru

Chief Marketing Officer

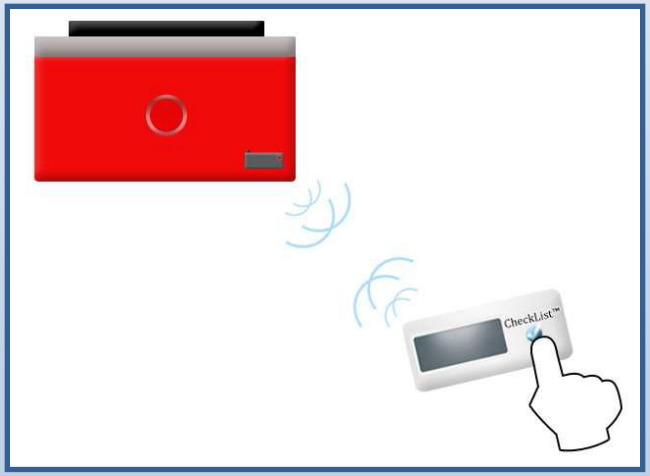
Mnemosyne Innovations

Outline

- Introduction
- System Overview
- High Level System Design
- Market Analysis
- Budget and Timeline
- Future Development
- Lessons Learned
- Conclusion
- Acknowledgements

Introduction

- CheckList™ alleviates problem of forgetfulness
- Portable memory aid device
- Prevents items from being left behind
- Easy to use

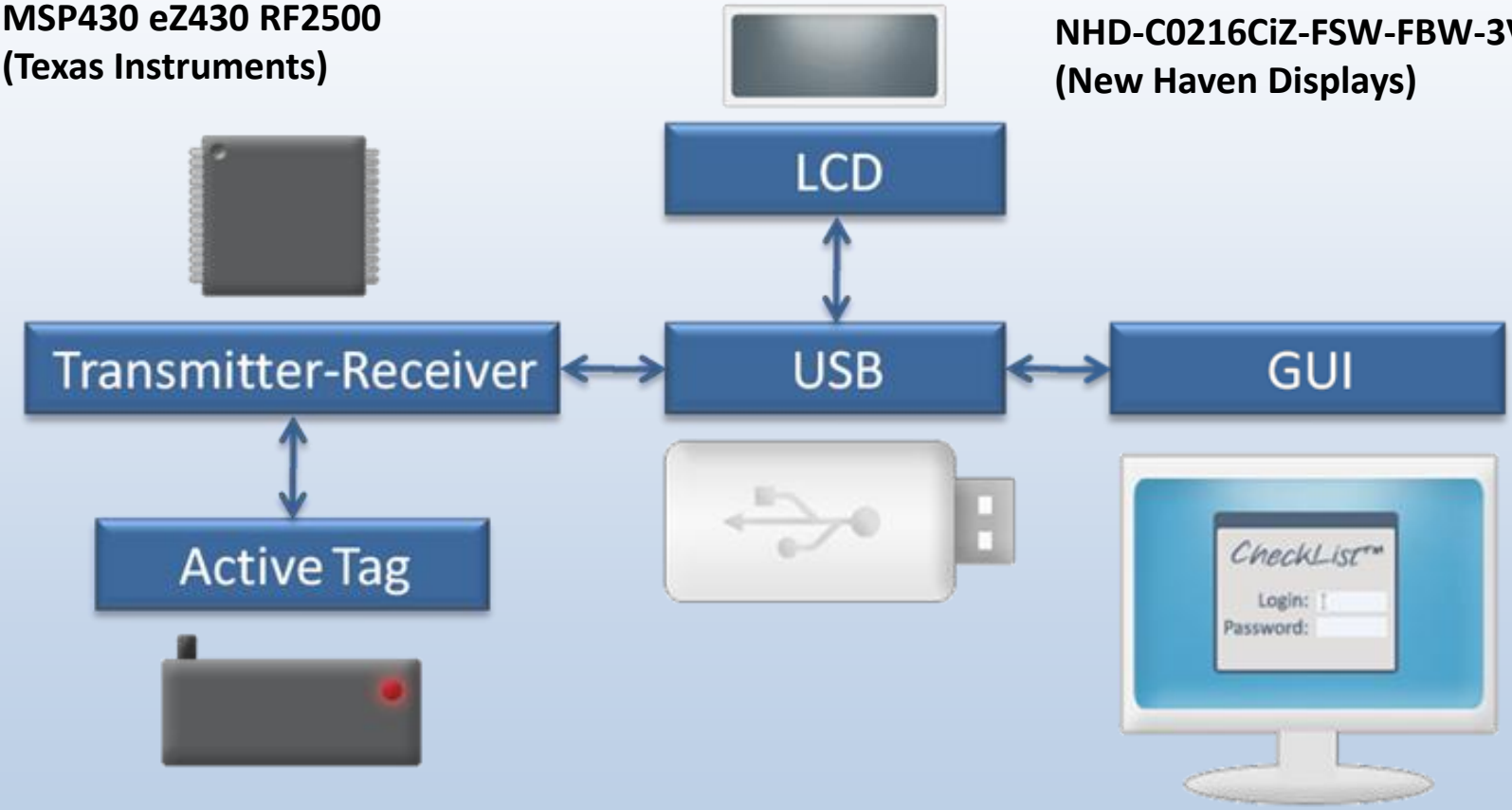


All you need to remember is your CheckList™

System Overview

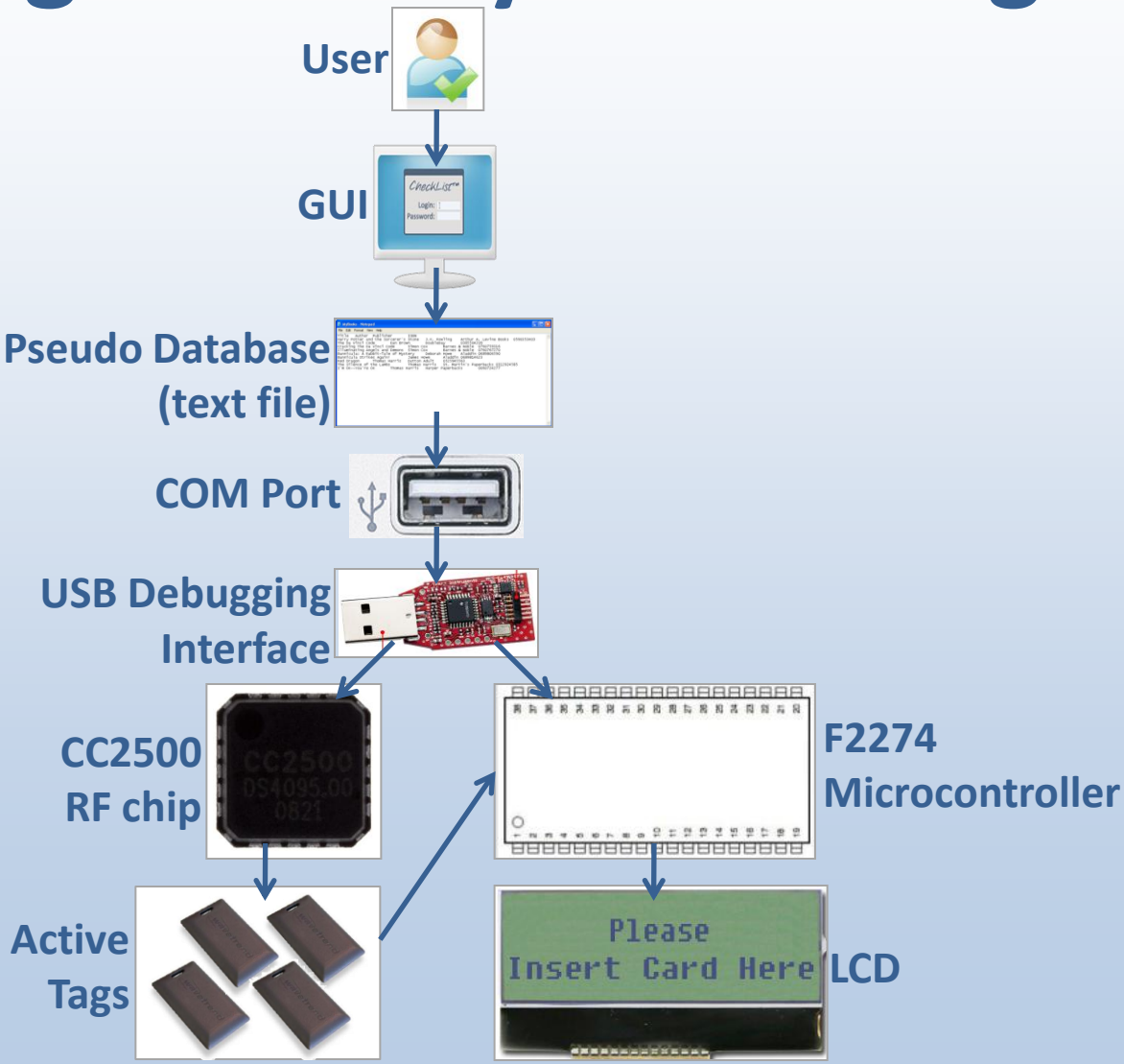
MSP430 eZ430 RF2500
(Texas Instruments)

NHD-C0216CiZ-FSW-FBW-3V3
(New Haven Displays)



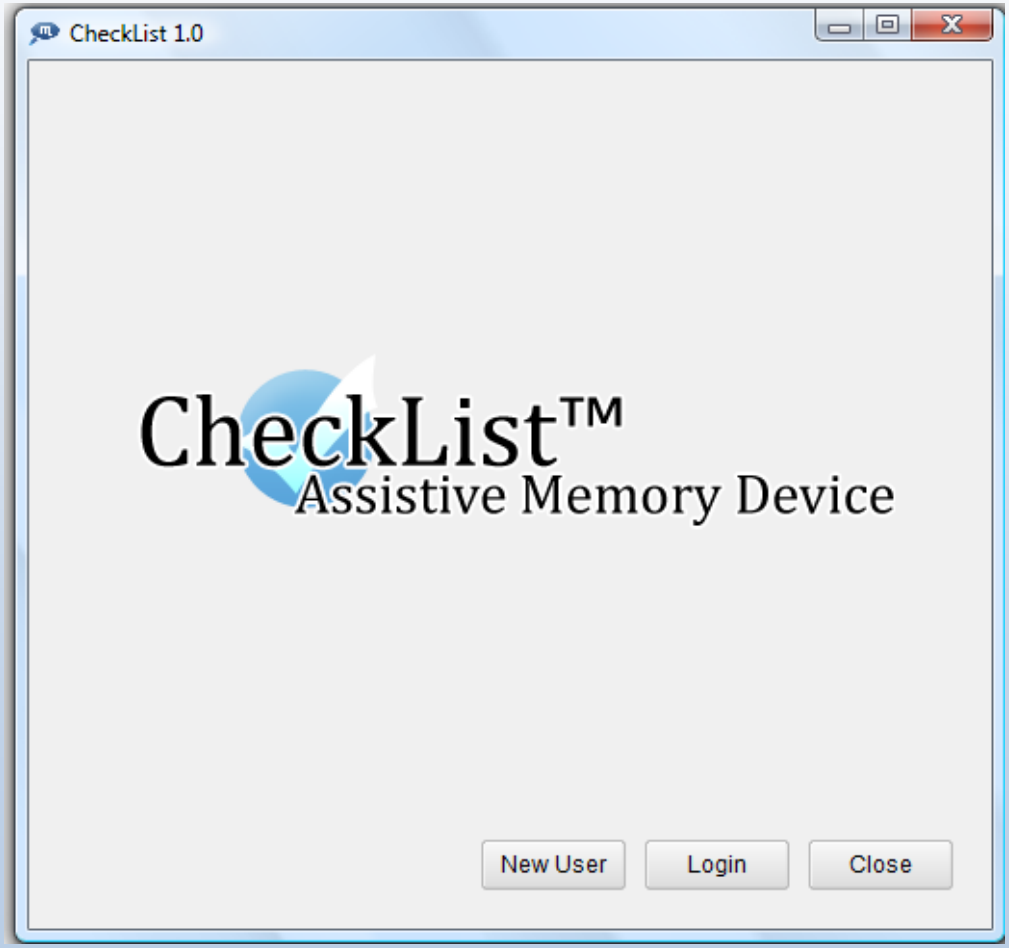
Visual C++ and QT application development platform

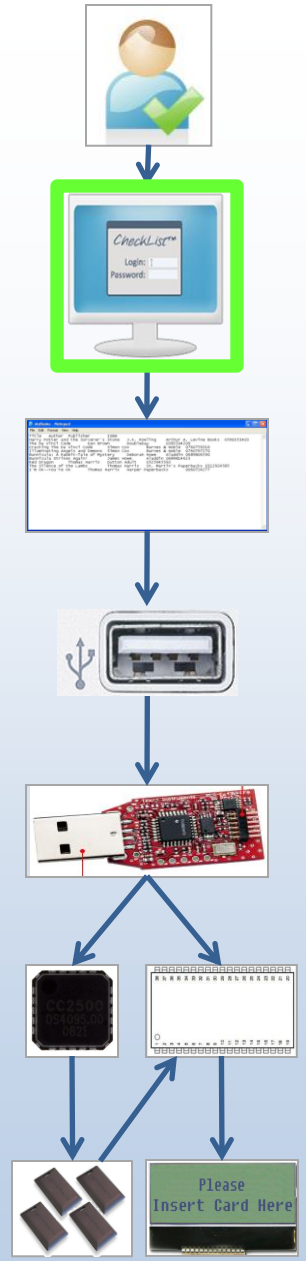
High Level System Design



Graphical User Interface (GUI)

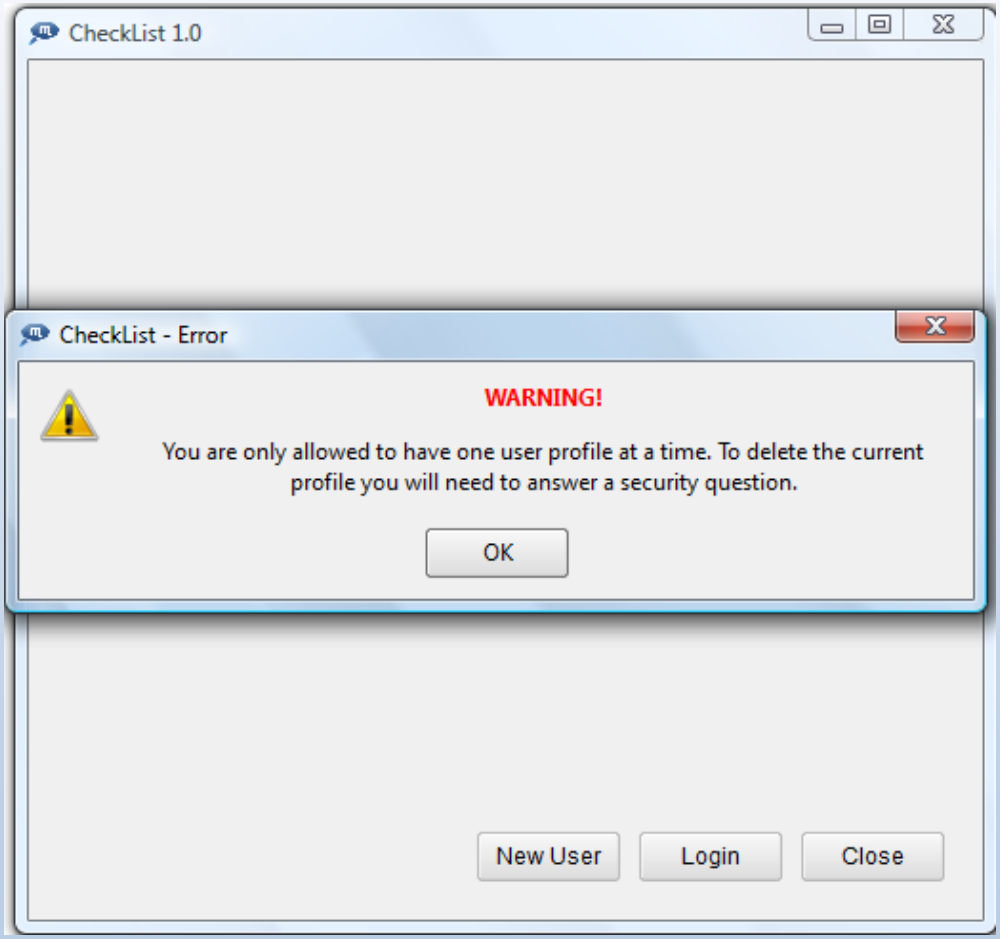
- Welcome Window

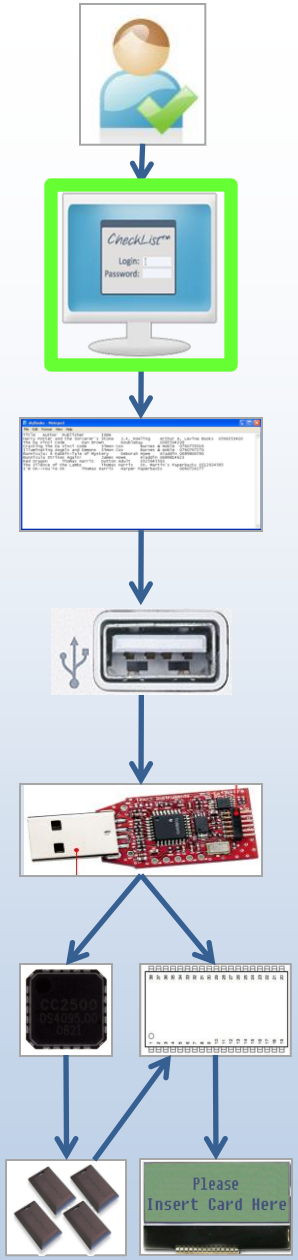




Graphical User Interface (GUI)

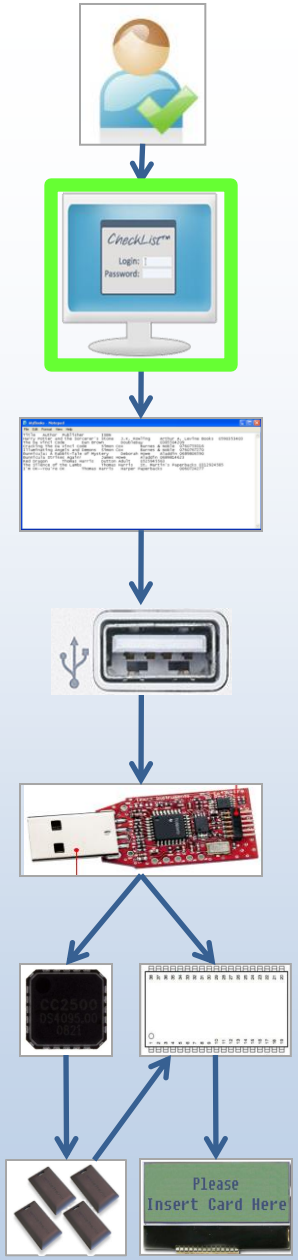
- Only 1 user profile permitted





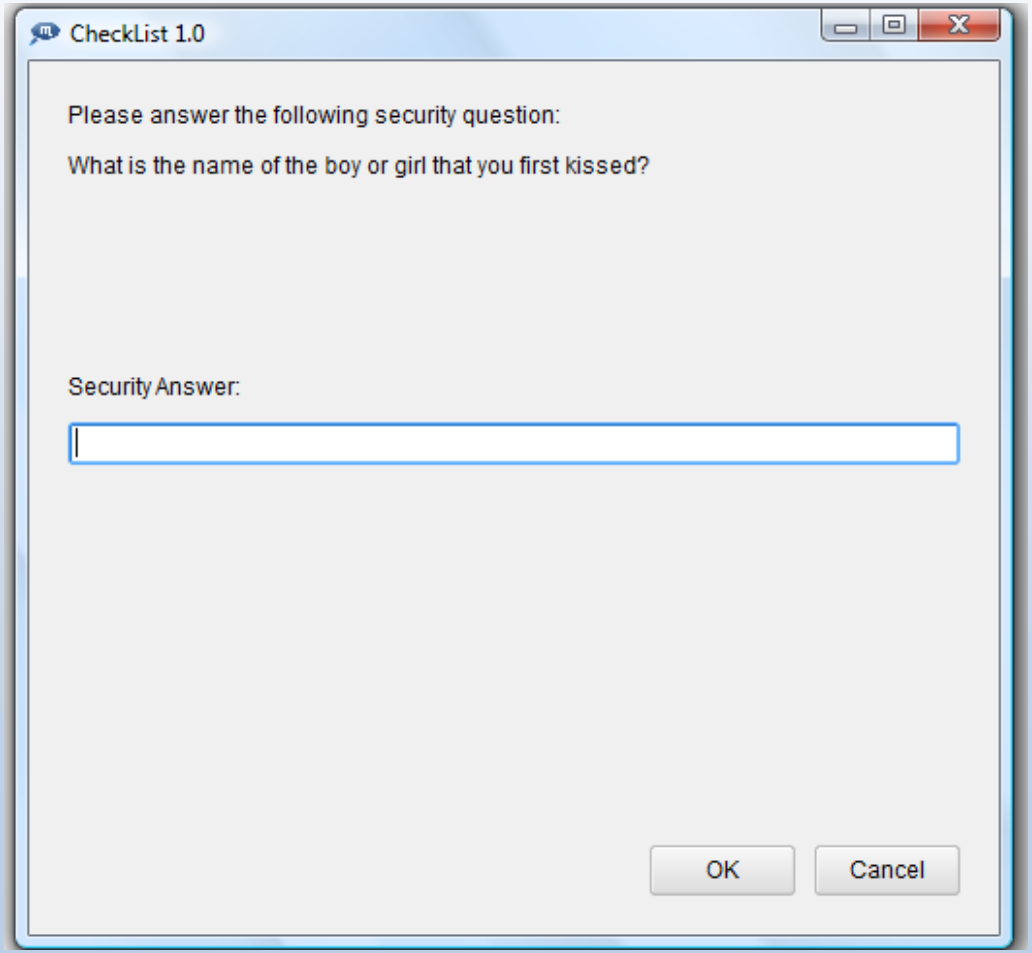
Graphical User Interface (GUI)

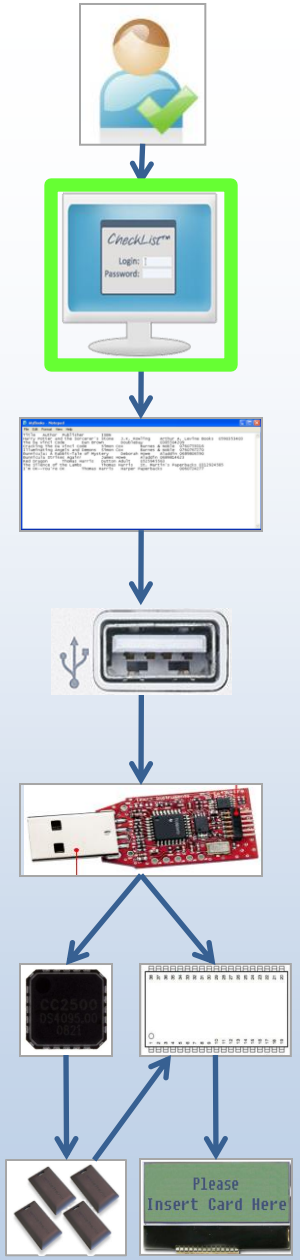
- Login Window – CheckList™



Graphical User Interface (GUI)

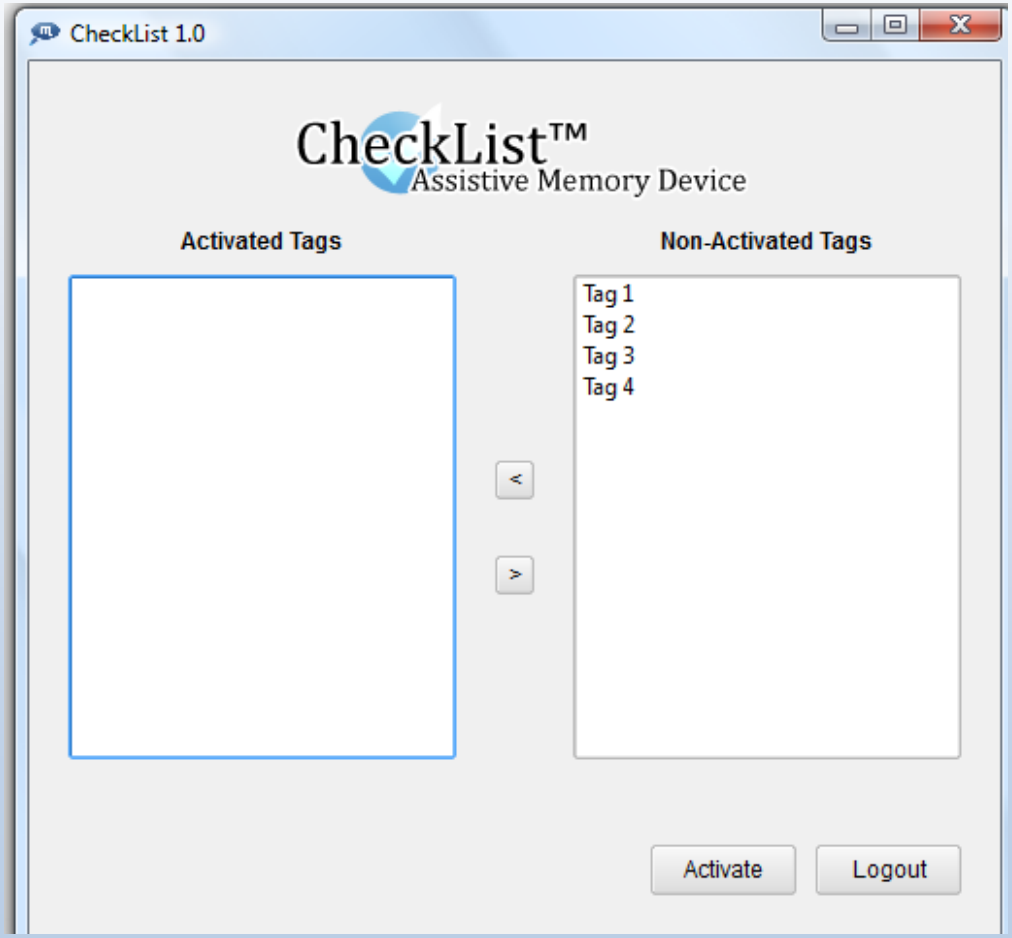
- Security Question Option

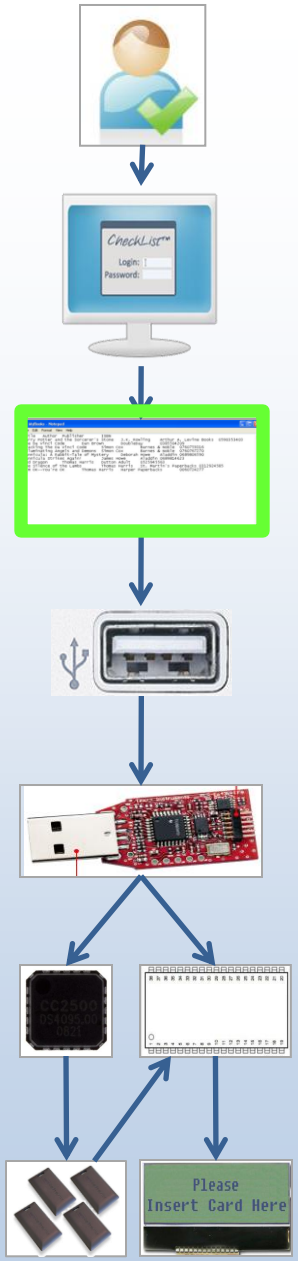




Graphical User Interface (GUI)

- Activating/Deactivating Tags





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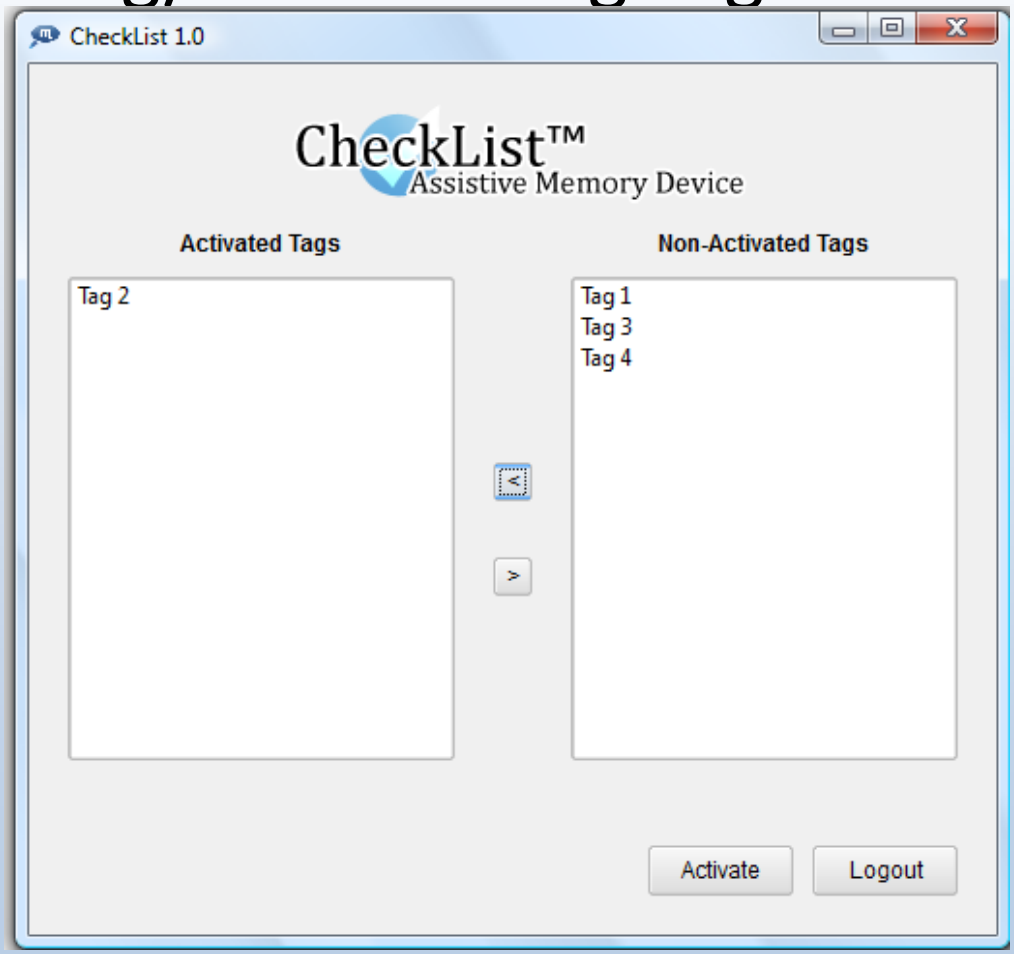
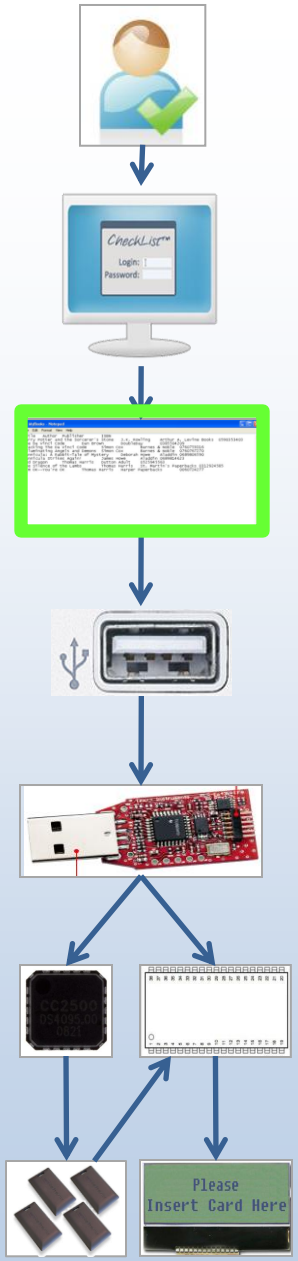
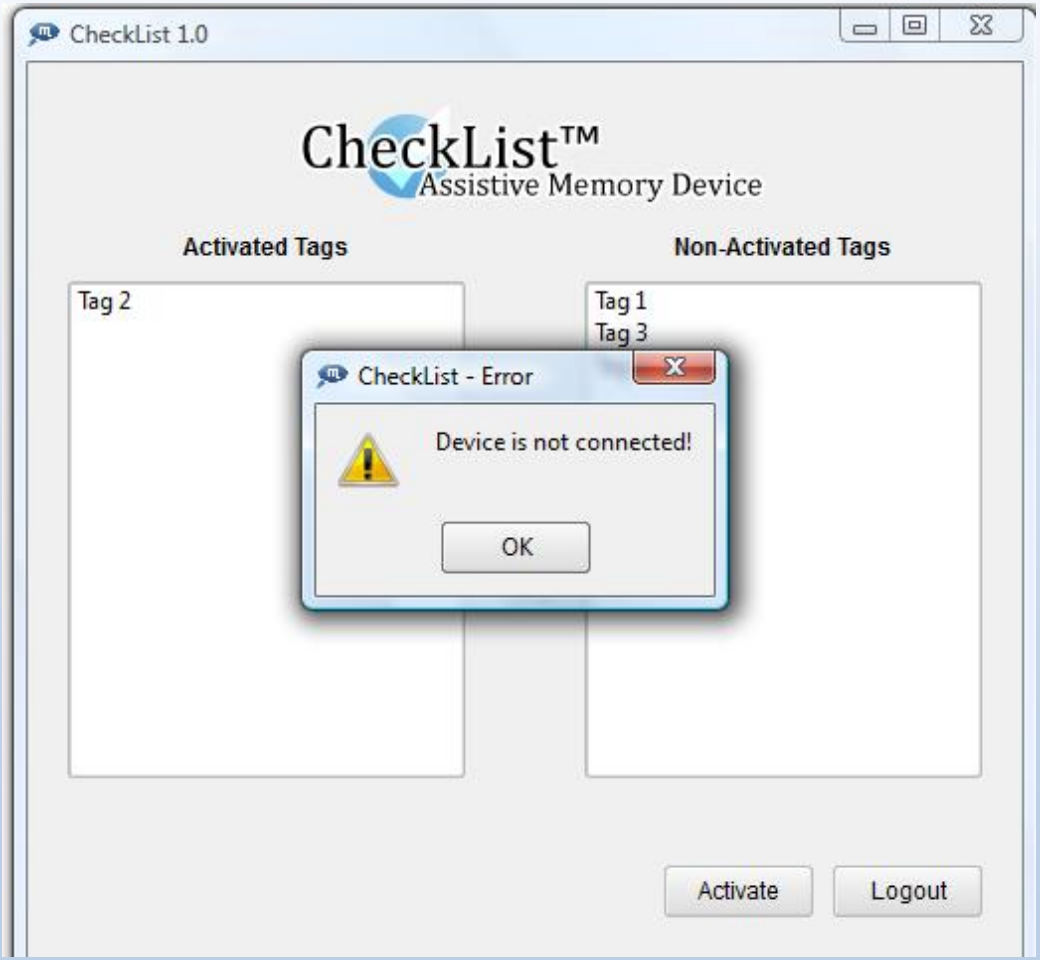
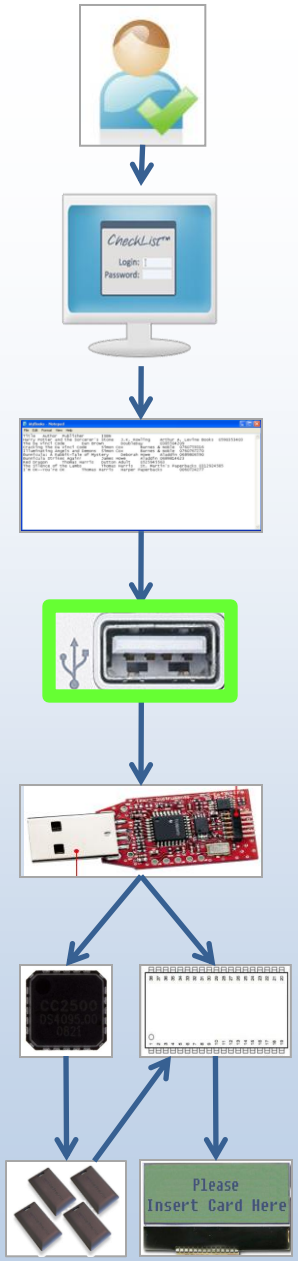




Graphical User Interface (GUI)

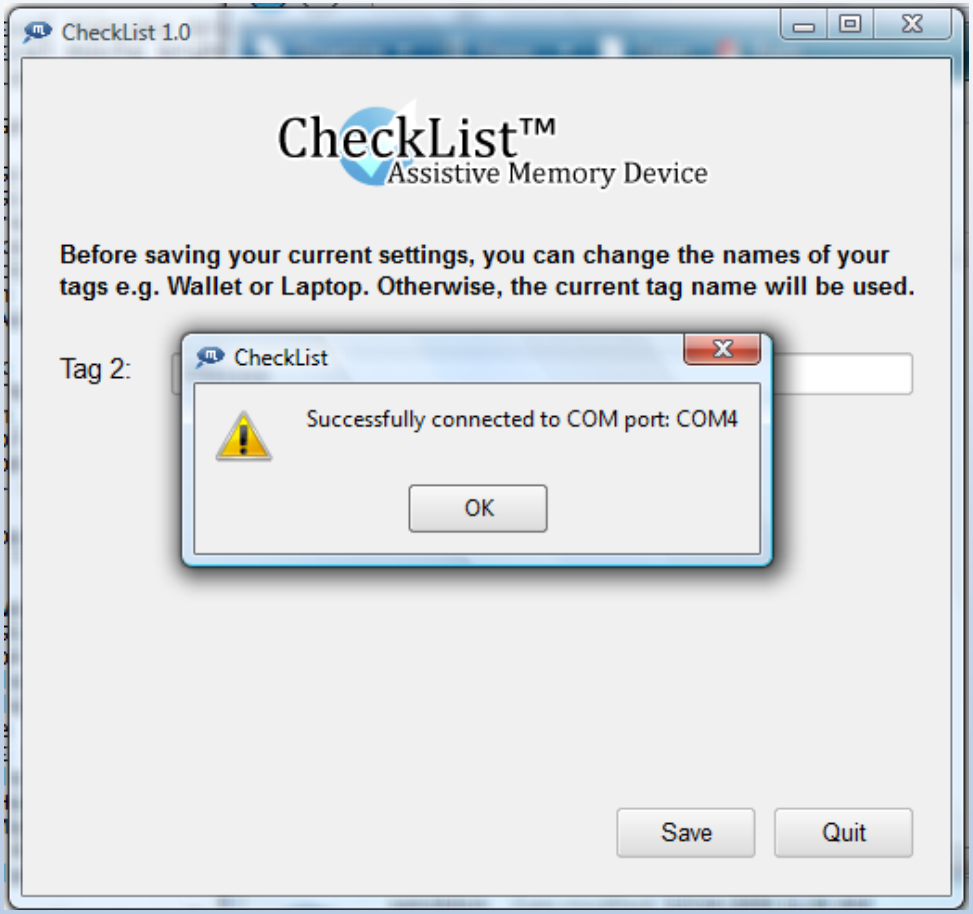
- Unsuccessful Connection with COM Port

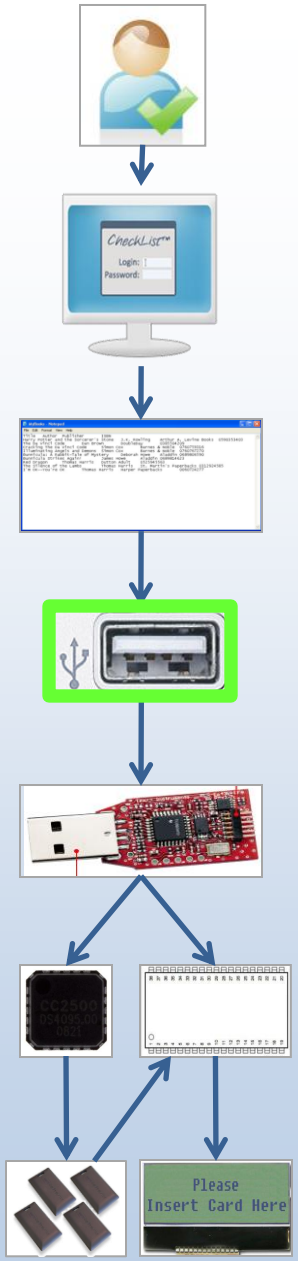




Graphical User Interface (GUI)

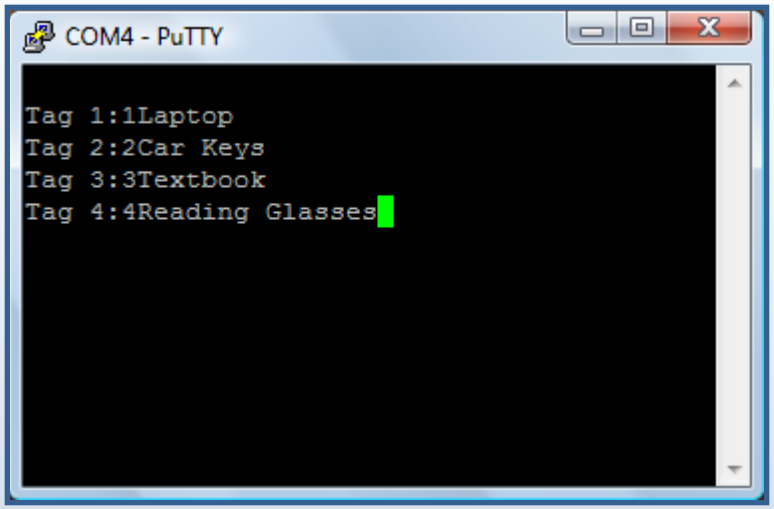
- Successful Connection with COM Port

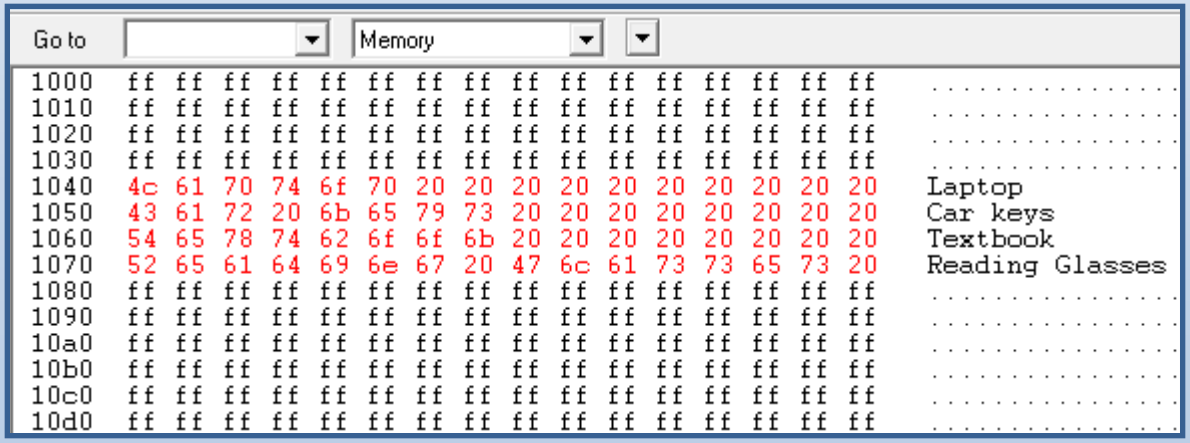




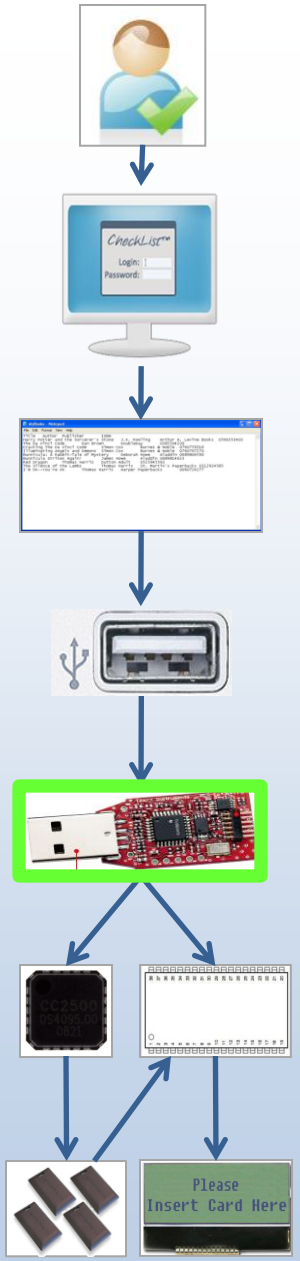
Detection Unit

Data is read from COM port …





… and stored in appropriate memory locations



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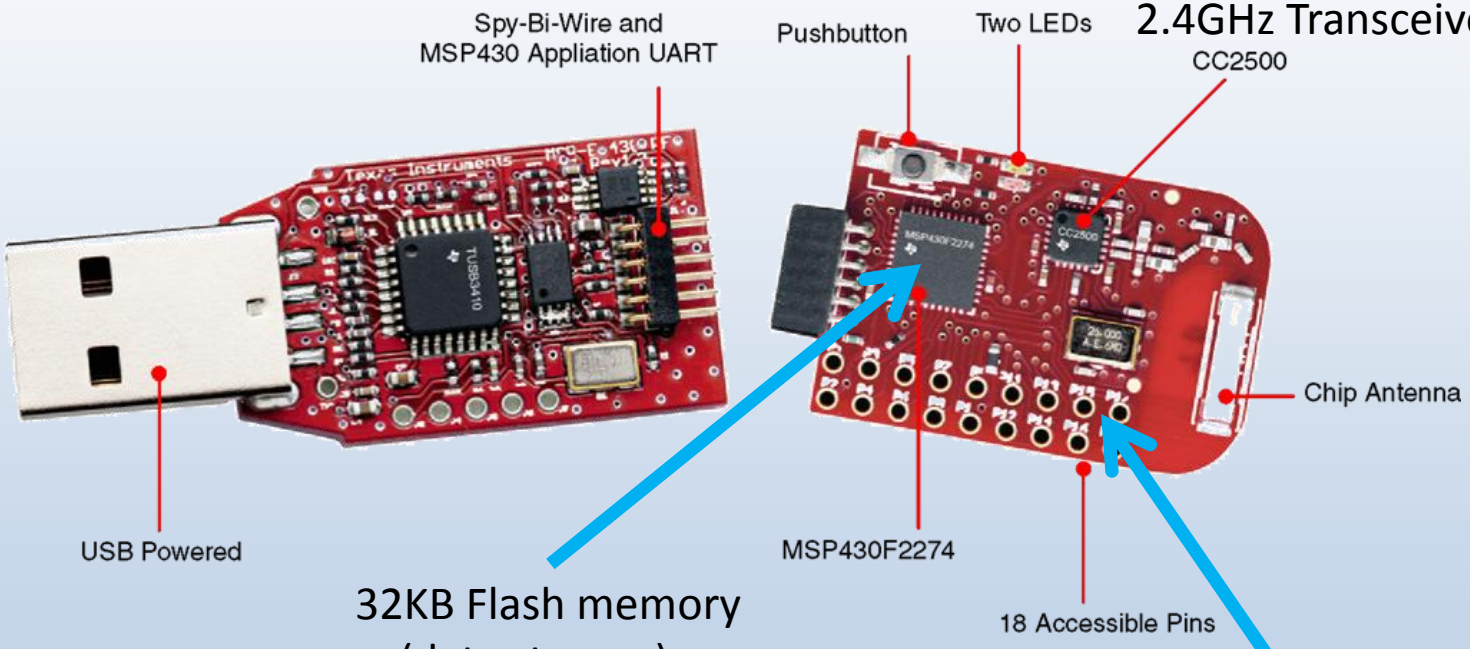

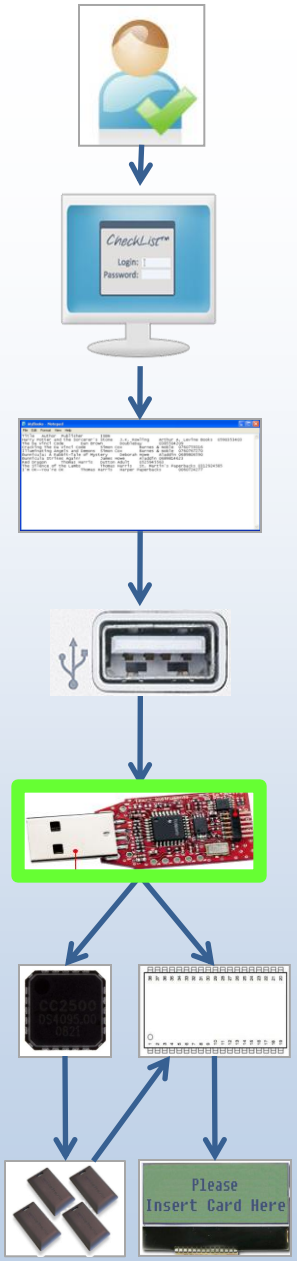

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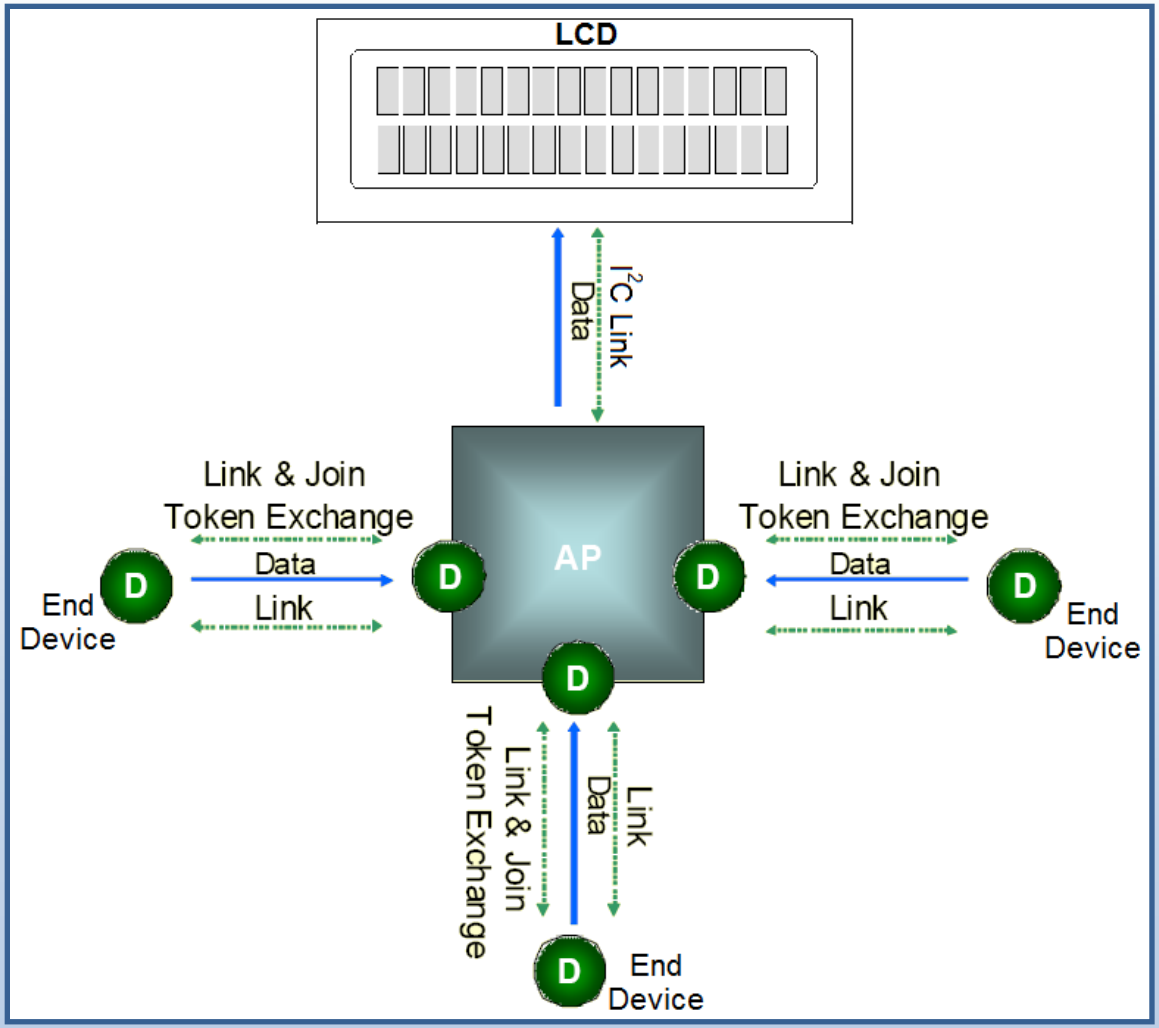
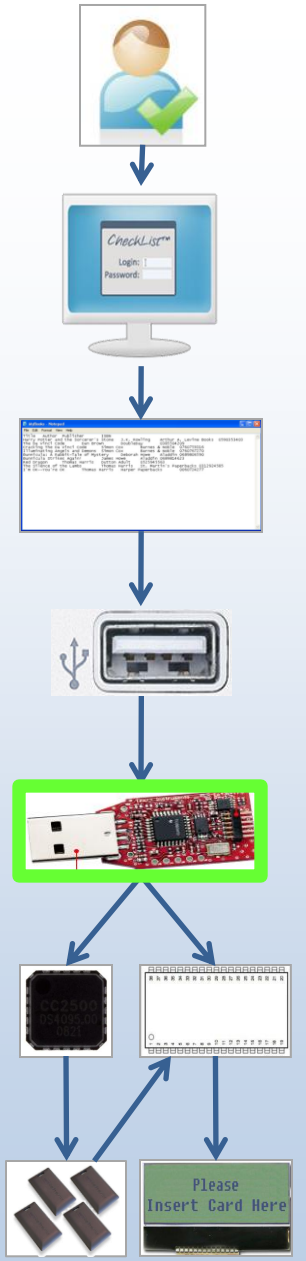
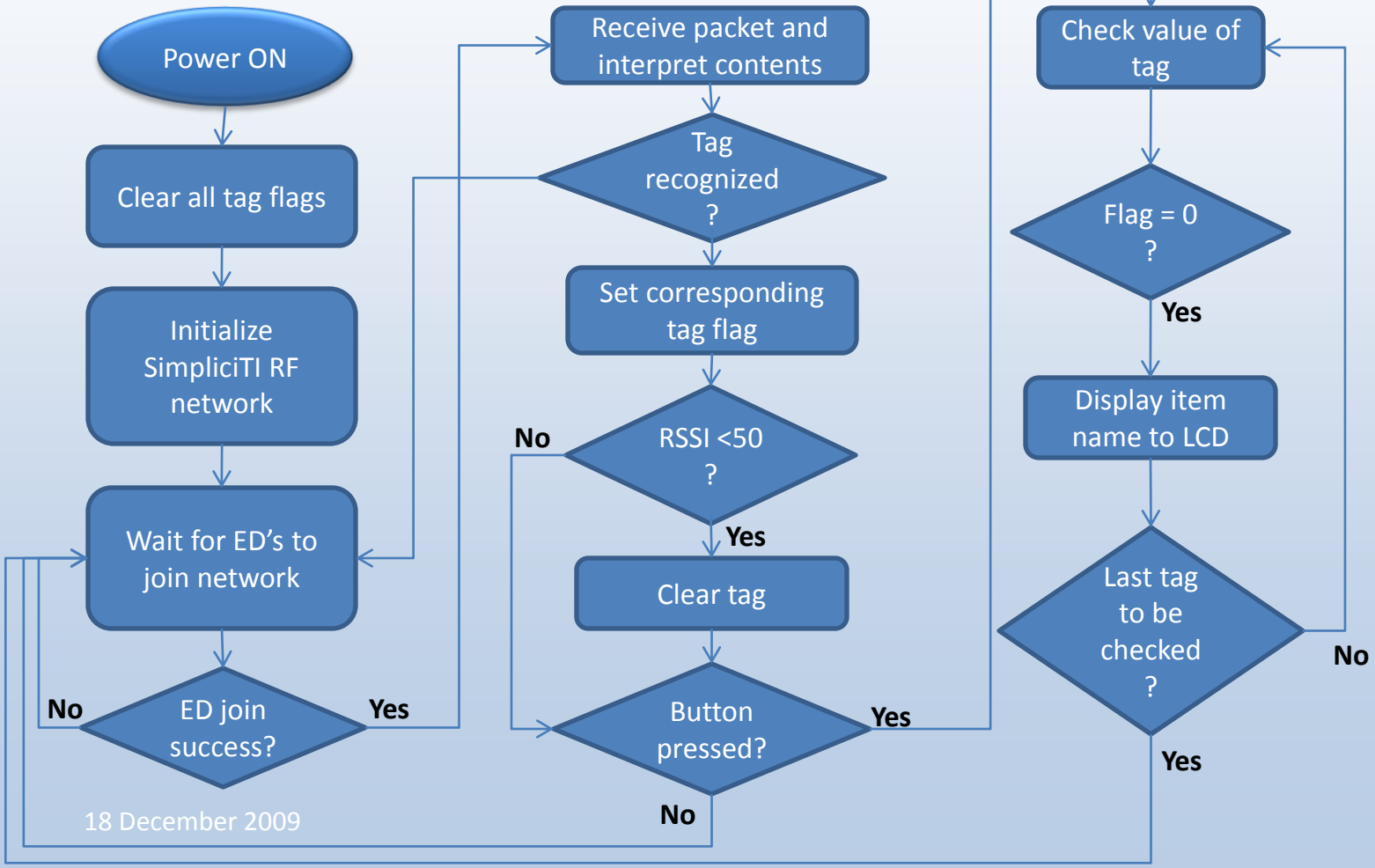
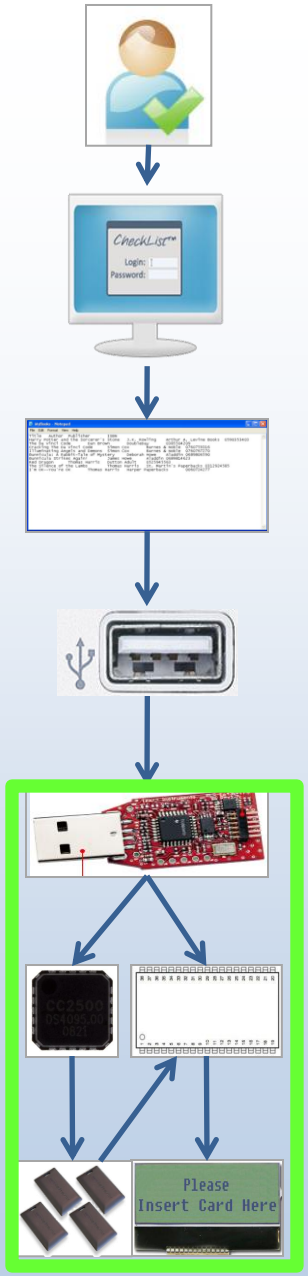




Detection Unit

- Missing Item Tag Detection





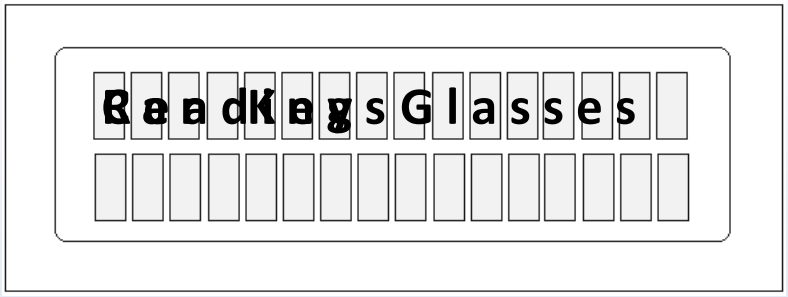
Detection Unit

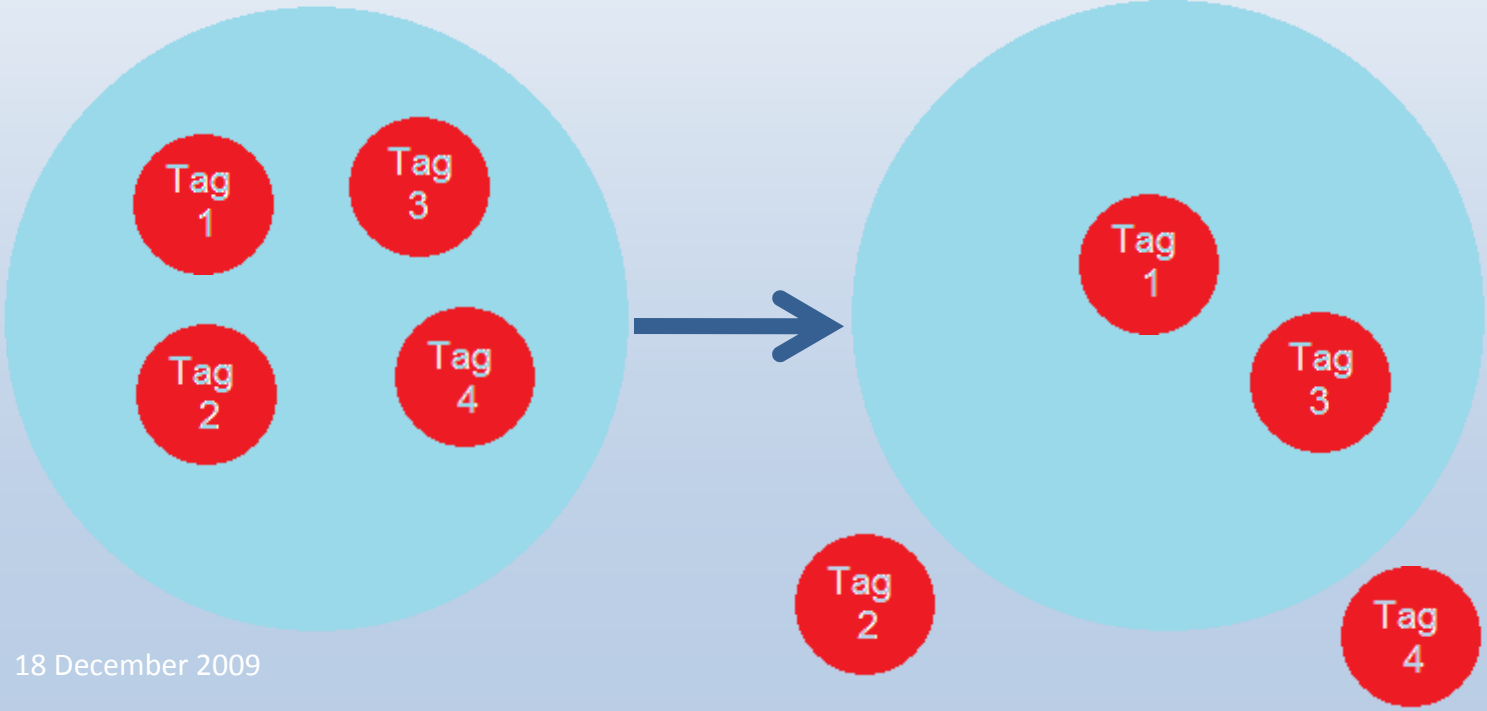
Tag1: Laptop

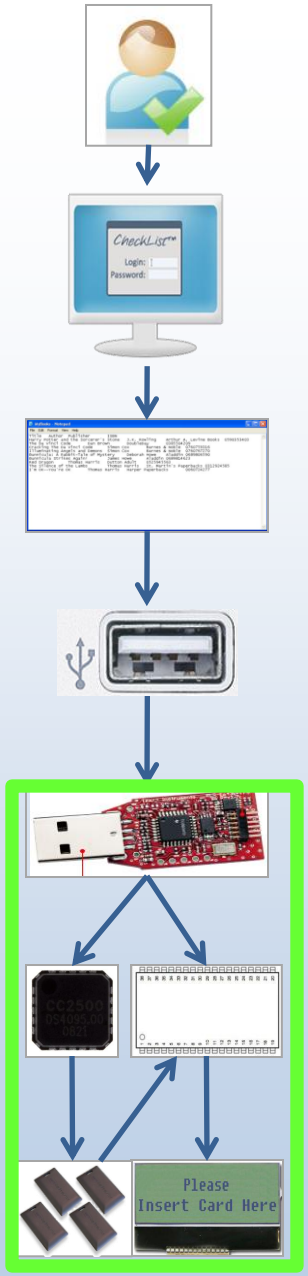
Tag2: Car Keys

Tag3: Textbook

Tag4: Reading glasses







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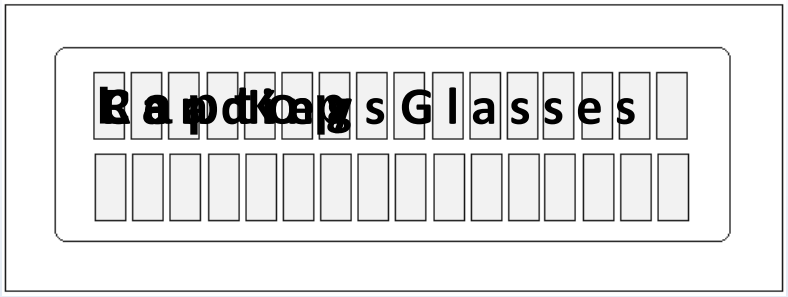

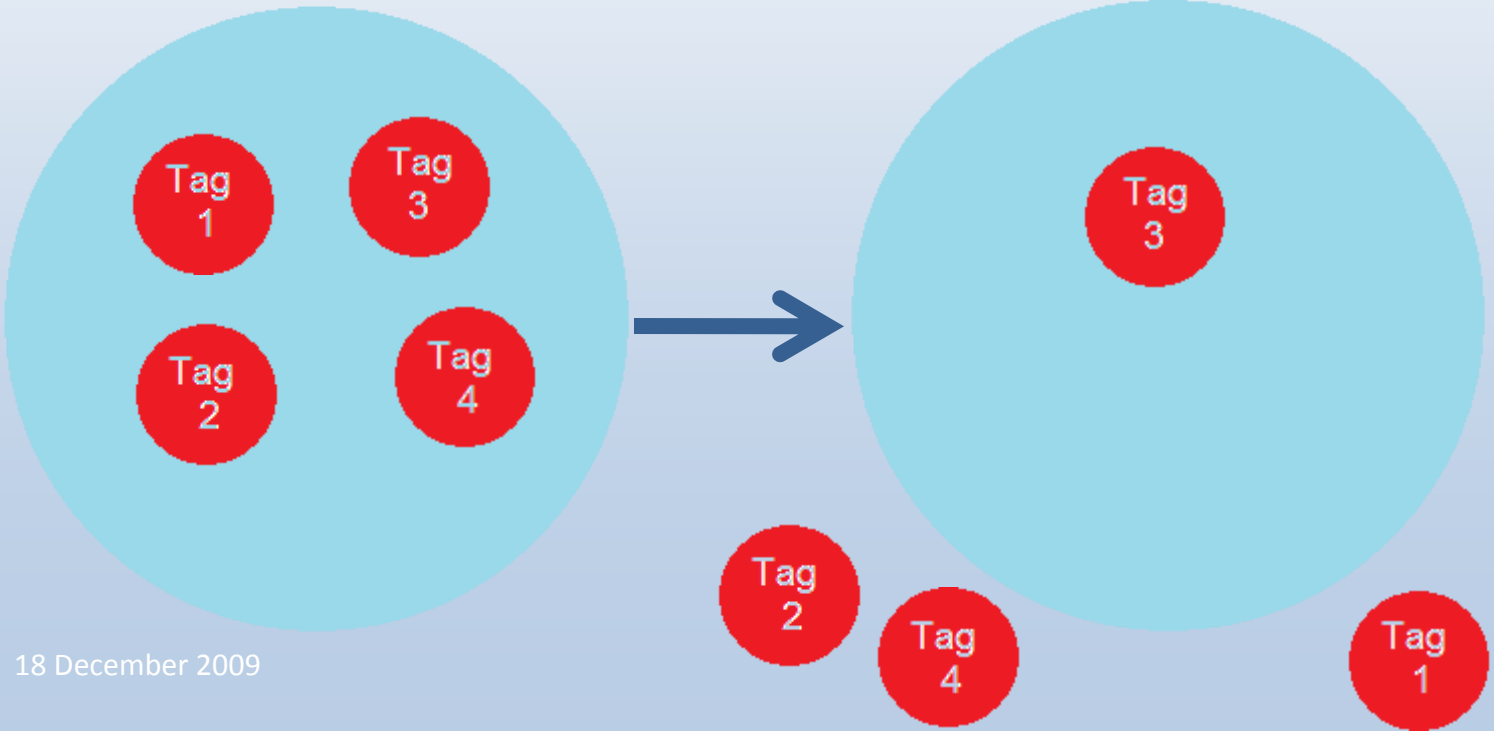

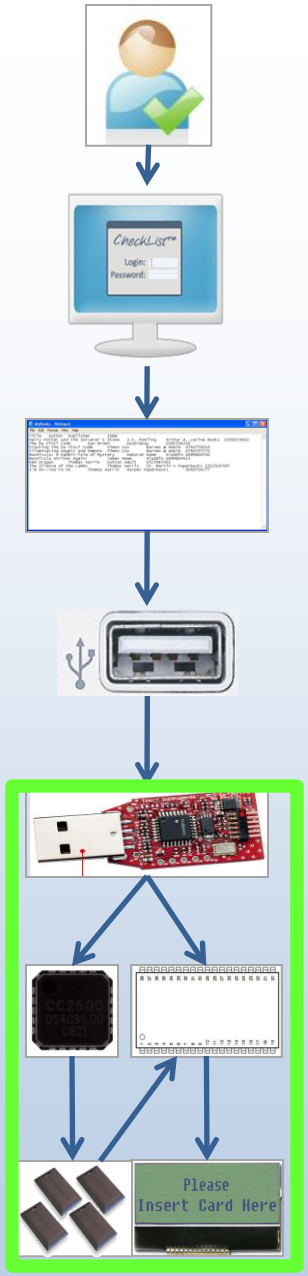

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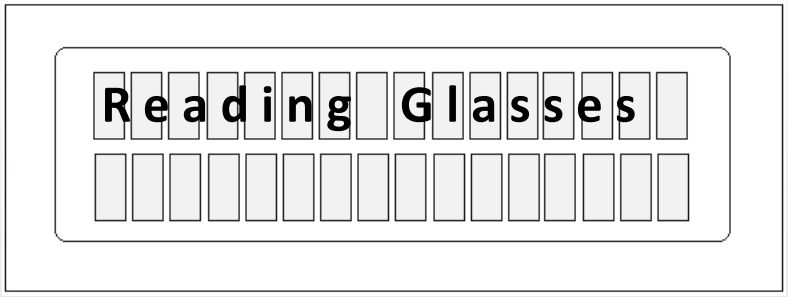

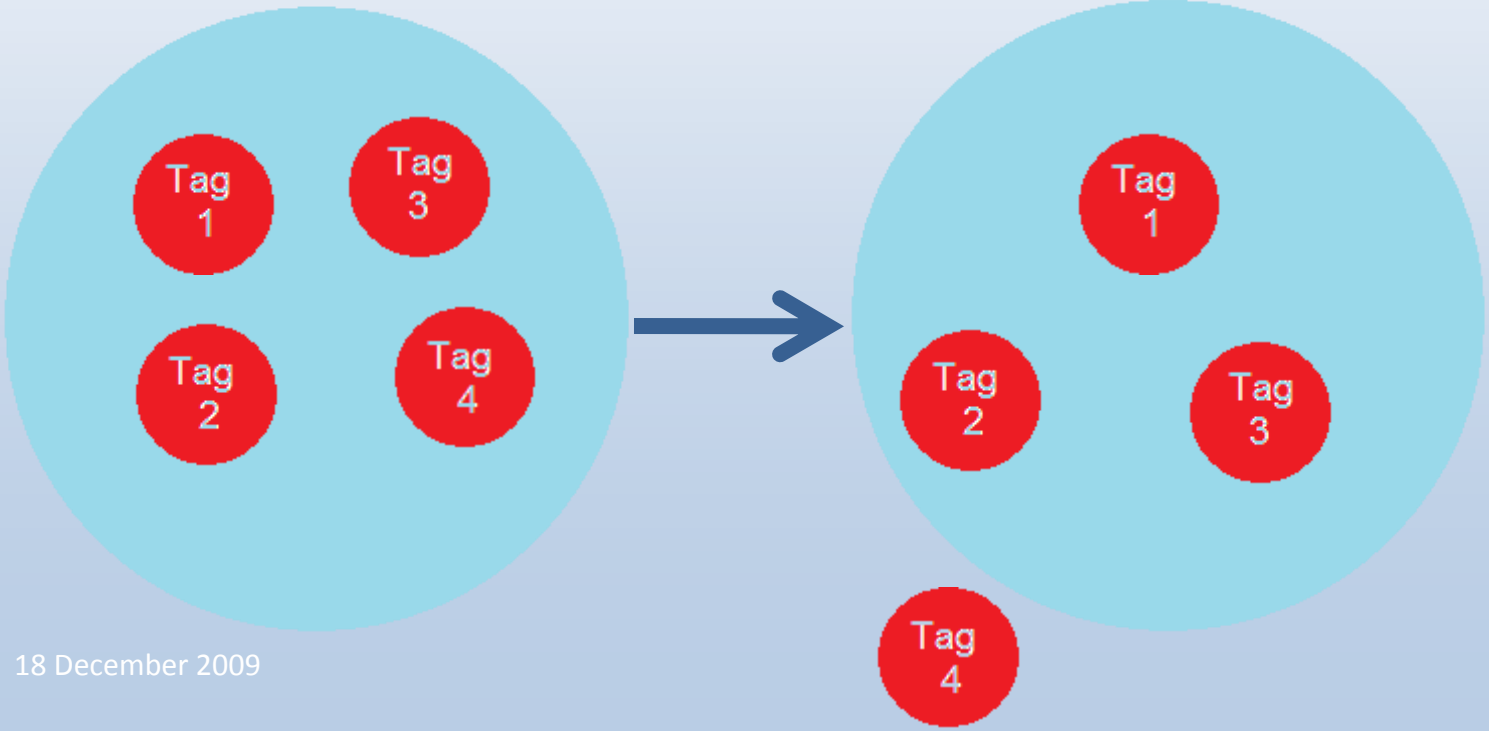

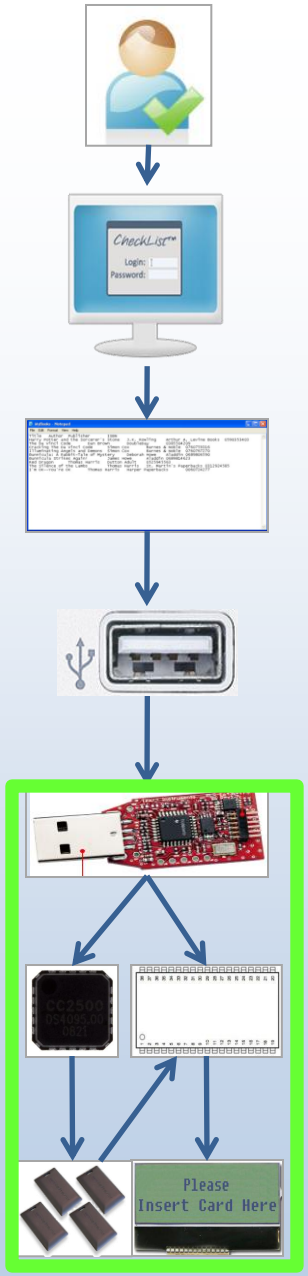

Mnemosyne Innovations

Market Analysis

- Target markets:
  - Households
    - Many things to keep track of
  - Professionals
    - Ensure important work-related items are not forgotten
  - Travellers
  - Healthcare
    - Dementia patients
    - Alzheimer's patients
  - Anyone and everyone!

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Market Analysis

- Current solutions:
  - Paper-based
    - Post-It Notes™
    - To-do lists
    - Planners or agendas
  - Electronic-based
    - Computer applications
    - Personal Digital Assistants (PDAs)
    - Cell phones or smart phones

- All require users to manually check for items

Mnemosyne Innovations

Market Analysis

- Our proposed solution: CheckList™
  - Simple: easy for general public to use
  - RF-based: eliminates manually checking for items
  - Portable: can be used in any environment or situation
  - Inexpensive: affordable for most people

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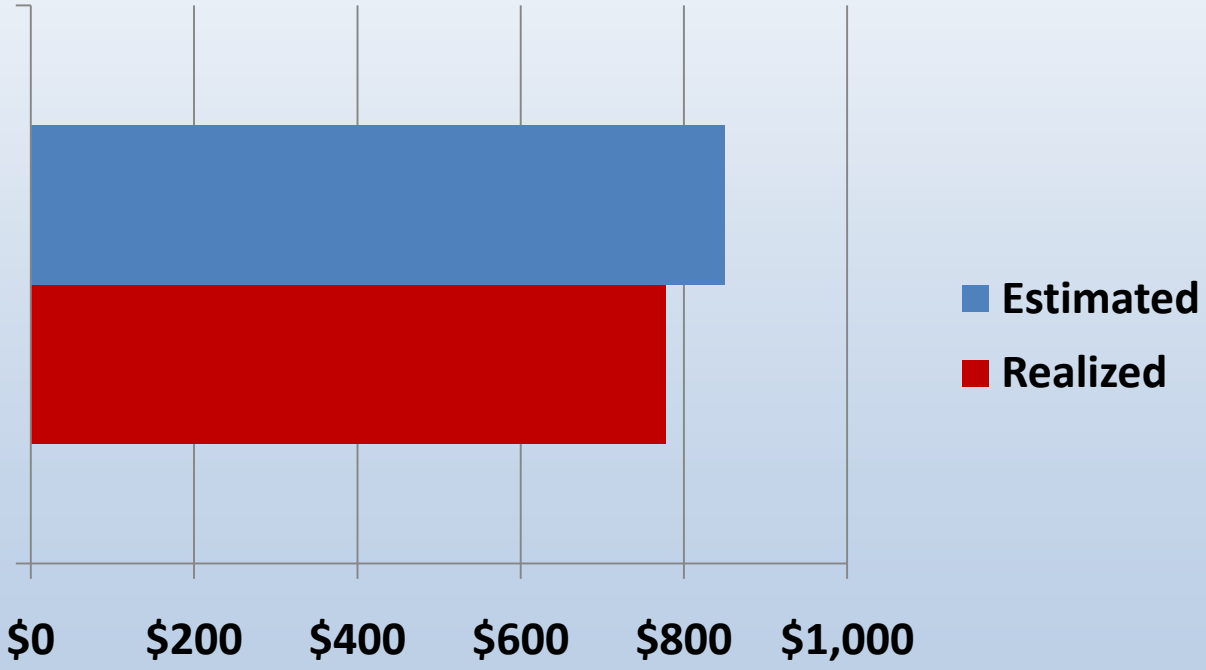
Market Analysis

ITEM	1000 UNITS		MASS PRODUCED	
	PARTS	RETAIL PRICE	PARTS	RETAIL PRICE
1 detection unit	$22.70	$45.00	$11.35	$23.00
1 active tag	$4.63	$10.00	$2.16	$4.50
1 detection unit and 4 active tags	$41.23	$82.00	$20.62	$41.00
10 active tags	$46.30	$90.00	$23.15	$46.00

Budget

- Estimated Cost: $850
- Realized Cost: $778



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Budget

COMPONENT	ESTIMATED COST
LCD	$40.00
RF Transmitter/Receiver	$300.00
RF Tags	$40.00
Controller/Processor	$250.00
USB Interface	$30.00
Power Supplies	$40.00
Prototyping Board	$50.00
Contingency	$100.00
TOTAL COST	**$850.00**

Mnemosyne Innovations

Budget

COMPONENT	REALIZED COST
LCD	$169.00
RF Transmitter/Receiver	$138.00
RF Tags	$149.00
Other Components	$68.00
Power Supplies	$73.00
Miscellaneous	$181.00
TOTAL COST	**$778.00**

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Budget

Lost expenses:

- LCDs purchased initially were not used ($136)
- Other components purchased to use with LCDs (also not used):
  - Voltage regulators ($5)
  - Level shifters ($10)
- Purchased extra components and supplies
  - Batteries
  - Device cases

Mnemosyne Innovations

Budget

- Could construct another proof-of-concept prototype for less
  - $80 (1 detection unit and 1 tag)
  - No extra components
- Cost of 1000 retail units even less
  - $27 (1 detection unit and 1 tag)
  - No extra modules on boards
  - Purchasing power

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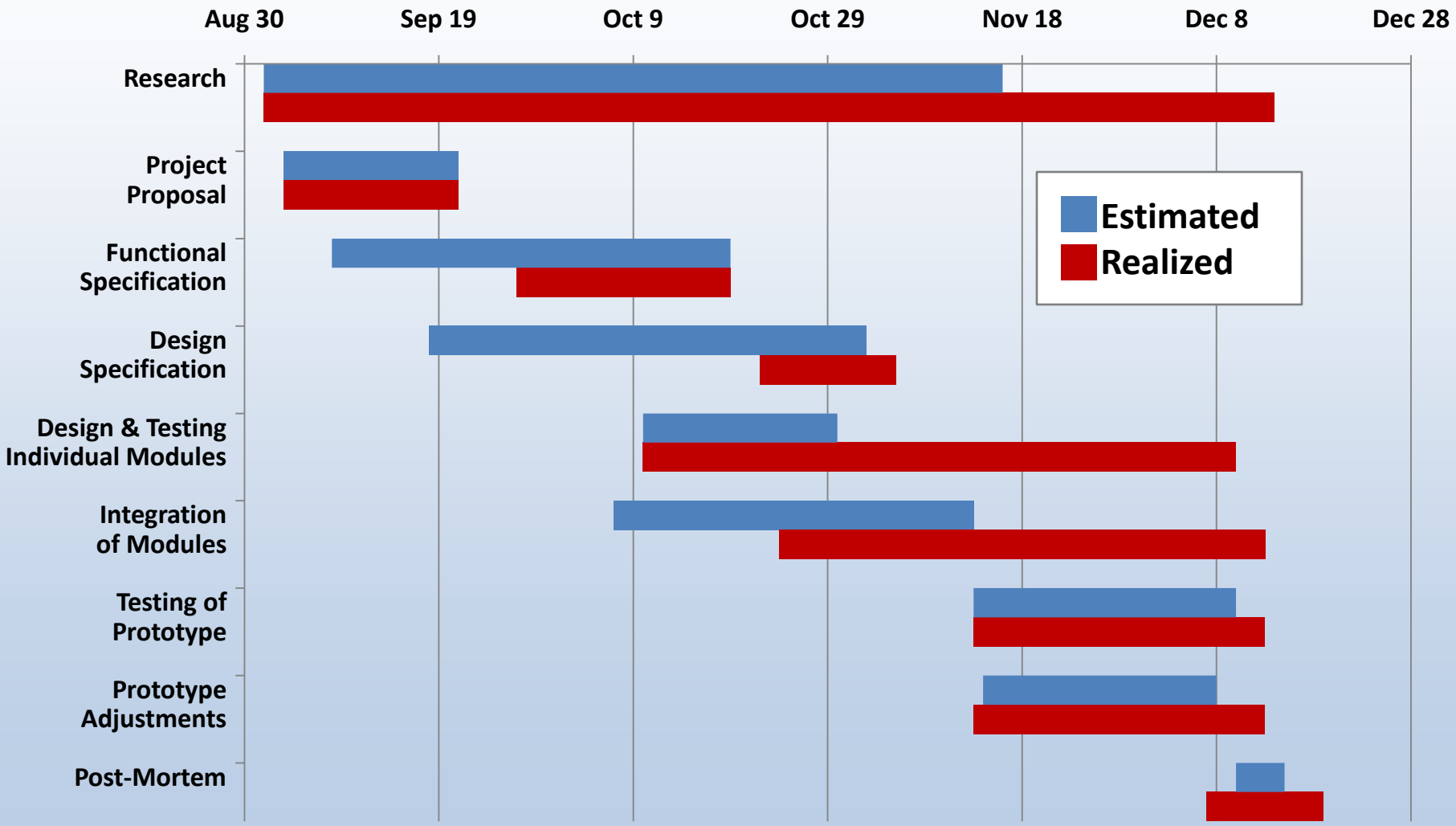
Timeline



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Team Dynamics

- Well defined roles and responsibilities
  - Priyanka: LCD-MCU interface implementation and testing
  - Rachel: GUI design, implementation and testing
  - Ana: LCD-MCU interface implementation and testing; RF detection implementation and testing
  - Surbhi: Hardware assembly, implementation and testing
- Everyone helped with other areas when needed
- All documentation was a combined effort

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Lessons Learned

- Research must be done thoroughly
- Ask for help and advice when you need it
- Perfectionism is inefficient
- Communication is critical

Future Development

- Smaller size
  - Develop custom chips
  - Implement device on custom printed circuit boards
- Longer battery life
  - Remove all extra power-consuming components
  - Implement on-off switch for LCD backlight
- Continuous mode
  - Constantly check for presence of tags
  - Audible alarm if a tag leaves the vicinity

Conclusion

- Mnemosyne Innovation's CheckList™ Prototype successfully created
  - Has future potential (low cost + high effectiveness)
  - Filling niche in the market
- ENSC 440 valuable experience
  - Technical
  - Soft skills

Mnemosyne Innovations

Acknowledgements

- John Bird, ENSC 440 Instructor
- Steve Whitmore, ENSC 305 Instructor
- Jason Lee, ENSC 305/440 Teaching Assistant
- Kourosh Khosraviani, Graduate Student
- Brandon Ngai, CiBER Lab Researcher
- Pranav Gupta, Undergraduate Student
- Thomas Watteyne, UC Berkeley Post-Doc Researcher

Thank You


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CheckList™
Assistive Memory System

Questions?

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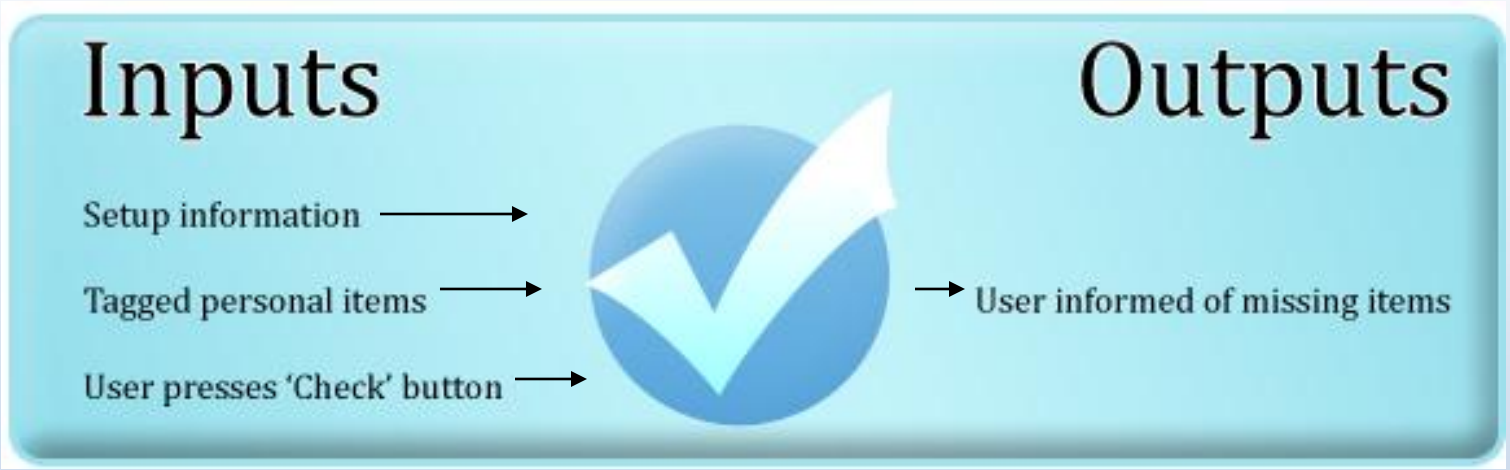
High Level Functional Diagram



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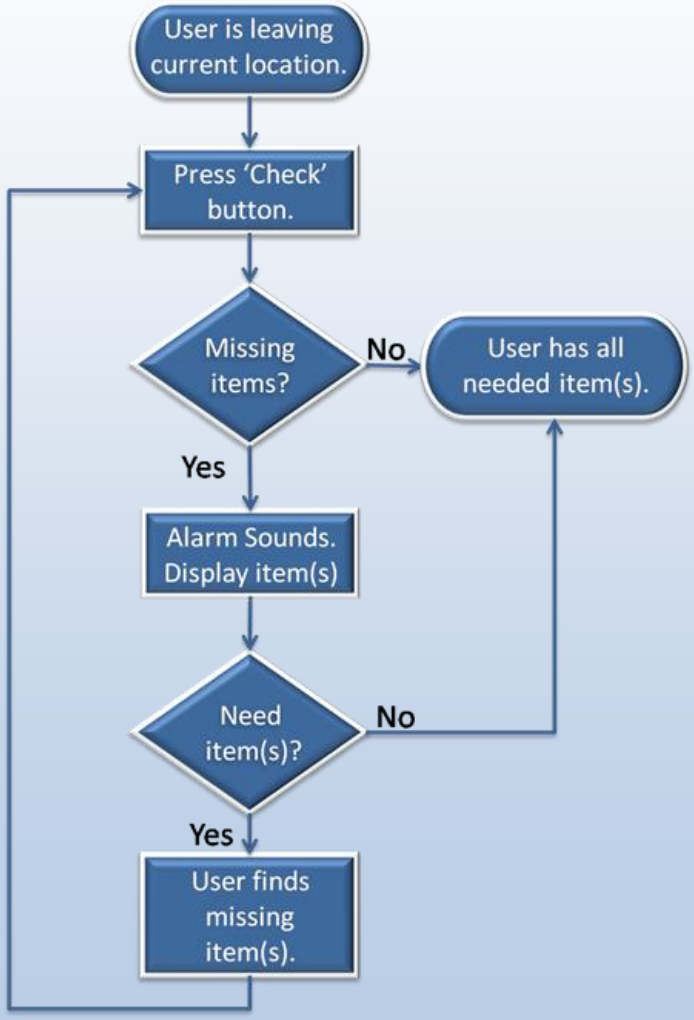
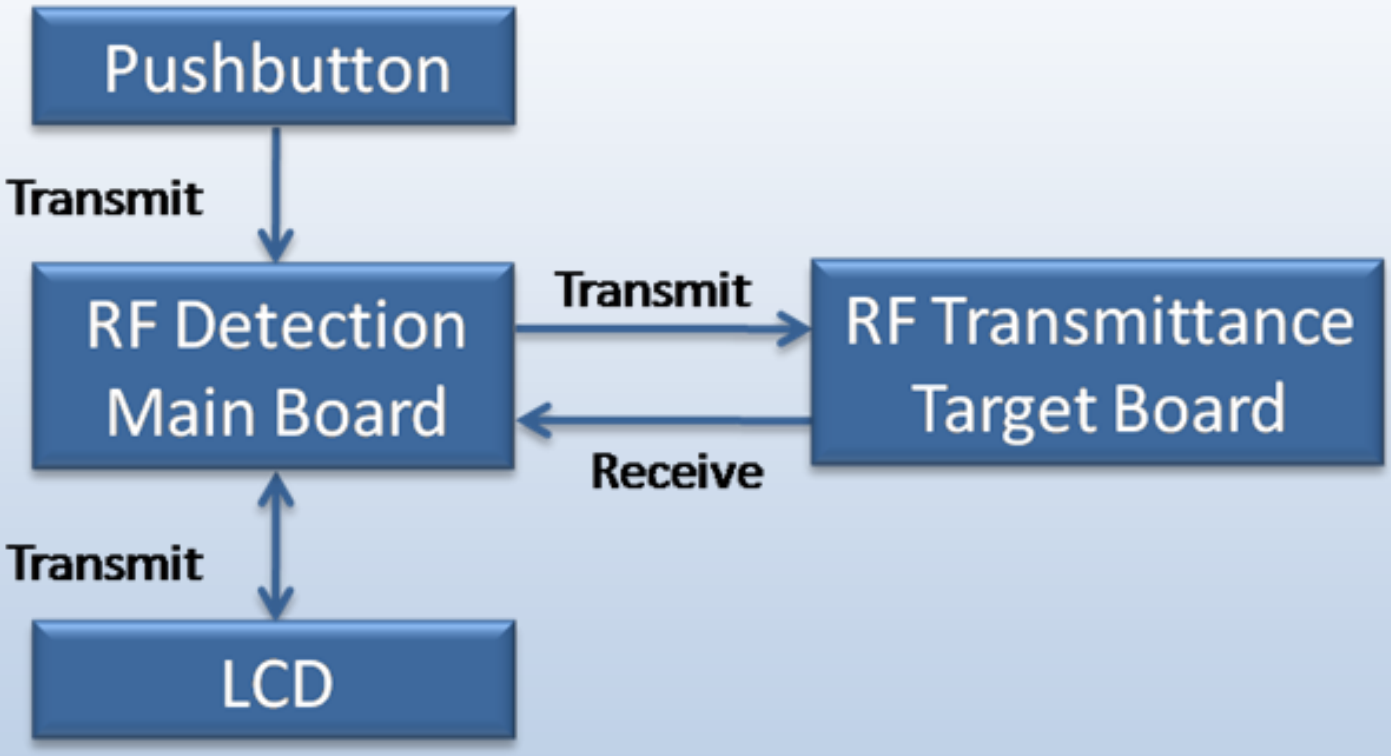
System Flowchart



Hardware Flowchart



MSP430 eZ430 RF2500

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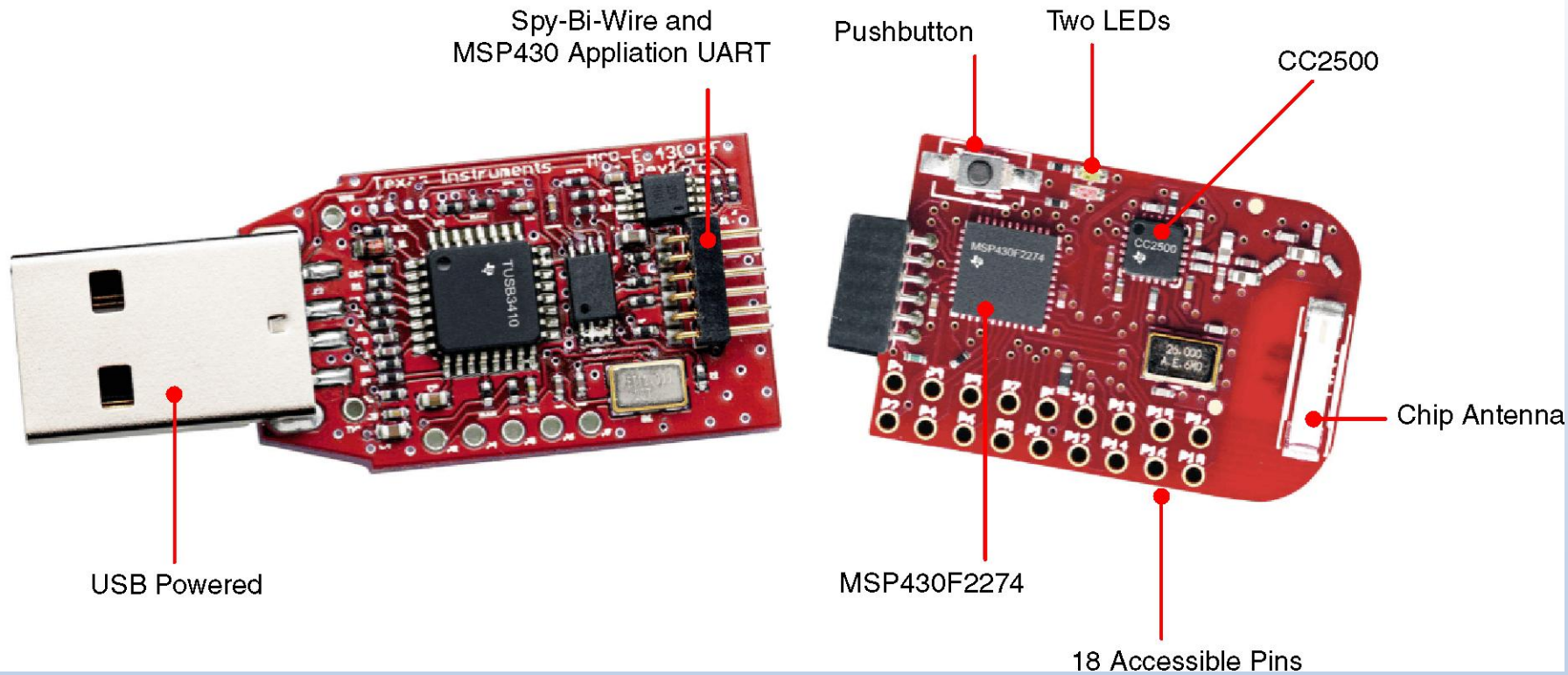


MSP430 eZ430 RF2500

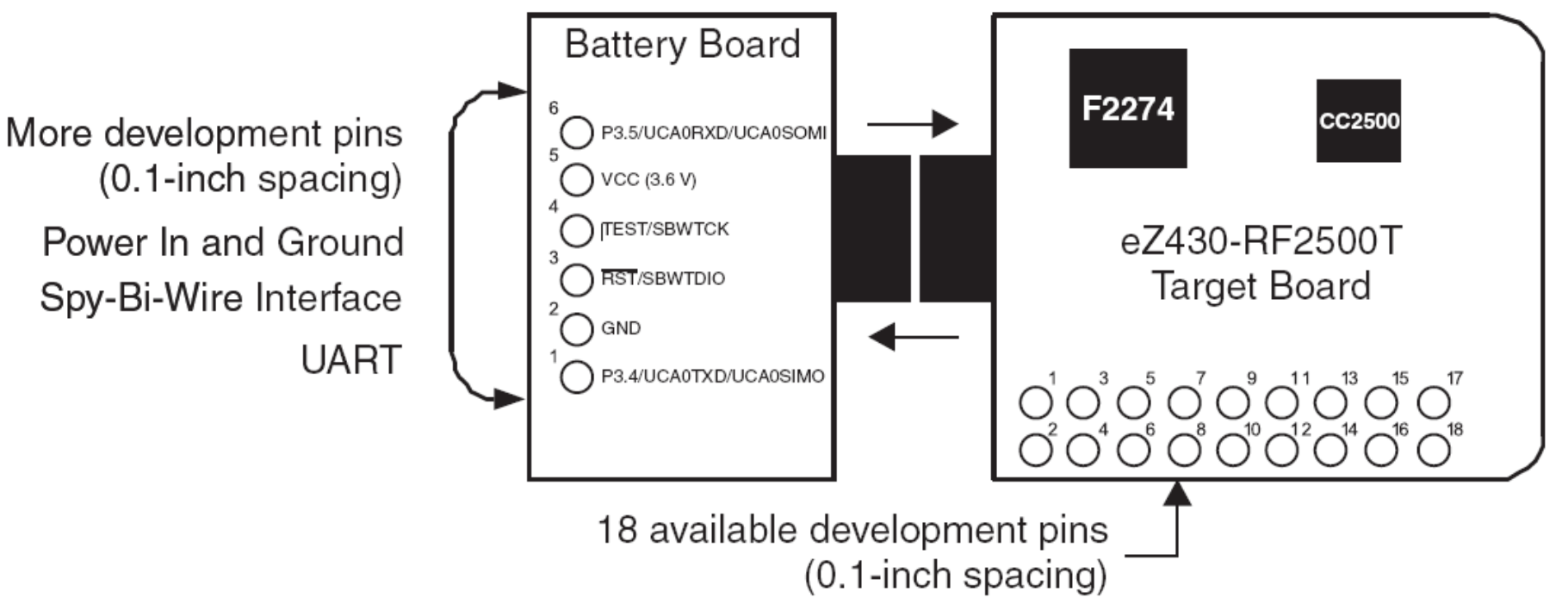


Figure 3. eZ430-RF2500 Development Tool

mnemosyne Innovations

GND →
3V →
VCC

Table 1. eZ430-RF2500T Target Board Pinouts

Pin	Function	Description
1	GND	Ground reference
2	VCC	Supply voltage
3	P2.0 / ACLK / A0 / OA0I0	General-purpose digital I/O pin / ACLK output / ADC10, analog input A0
4	P2.1 / TAINCLK / SMCLK / A1 / A0O	General-purpose digital I/O pin / ADC10, analog input A1 Timer_A, clock signal at INCLK, SMCLK signal output
5	P2.2 / TA0 / A2 / OA0I1	General-purpose digital I/O pin / ADC10, analog input A2 Timer_A, capture: CCI0B input/BSL receive, compare: OUT0 output
6	P2.3 / TA1 / A3 / VREF– / VeREF– / OA1I1 / OA1O	General-purpose digital I/O pin / Timer_A, capture: CCI1B input, compare: OUT1 output / ADC10, analog input A3 / negative reference voltage output/input
7	P2.4 / TA2 / A4 / VREF+ / VeREF+ / OA1I0	General-purpose digital I/O pin / Timer_A, compare: OUT2 output / ADC10, analog input A4 / positive reference voltage output/input
8	P4.3 / TB0 / A12 / OA0O	General-purpose digital I/O pin / ADC10 analog input A12 / Timer_B, capture: CCI0B input, compare: OUT0 output
9	P4.4 / TB1 / A13 / OA1O	General-purpose digital I/O pin / ADC10 analog input A13 / Timer_B, capture: CCI1B input, compare: OUT1 output
10	P4.5 / TB2 / A14 / OA0I3	General-purpose digital I/O pin / ADC10 analog input A14 / Timer_B, compare: OUT2 output
11	P4.6 / TBOUTH / A15 / OA1I3	General-purpose digital I/O pin / ADC10 analog input A15 / Timer_B, switch all TB0 to TB3 outputs to high impedance
12	GND	Ground reference
13	P2.6 / XIN (GDO0)	General-purpose digital I/O pin / Input terminal of crystal oscillator
14	P2.7 / XOUT (GDO2)	General-purpose digital I/O pin / Output terminal of crystal oscillator
15	P3.2 / UCB0SOMI / UCB0SCL	General-purpose digital I/O pin USCI_B0 slave out/master in when in SPI mode, SCL I2C clock in I2C mode
16	P3.3 / UCB0CLK / UCA0STE	General-purpose digital I/O pin USCI_B0 clock input/output / USCI_A0 slave transmit enable
17	P3.0 / UCB0STE / UCA0CLK / A5	General-purpose digital I/O pin / USCI_B0 slave transmit enable / USCI_A0 clock input/output / ADC10, analog input A5
18	P3.1 / UCB0SIMO / UCB0SDA	General-purpose digital I/O pin / USCI_B0 slave in/master out in SPI mode, SDA I2C data in I2C mode

SCL →

SDA →

Table 2. Battery Board Pinouts

Pin	Function	Description
1	P3.4 / UCA0TXD / UCA0SIMO	General-purpose digital I/O pin / USCI_A0 transmit data output in UART mode (UART communication from 2274 to PC), slave in/master out in SPI mode
2	GND	Ground reference
3	$\overline{\text{RST}}$ / SBWTDIO	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
4	TEST / SBWTCK	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
5	VCC (3.6V)	Supply voltage
6	P3.5 / UCA0RXD / UCA0SOMI	General-purpose digital I/O pin / USCI_A0 receive data input in UART mode (UART communication from 2274 to PC), slave out/master in when in SPI mode

MSP430-F2274

- 16-MIPS performance
- 200-ksps 10-bit SAR ADC
- Two built-in operational amplifiers
- Watchdog timer, 16-bit Timer_A3 and Timer_B3
- USCI module supporting UART/LIN, (2) SPI, I2C, or IrDA
- Five low-power modes drawing as little as 700 nA in standby

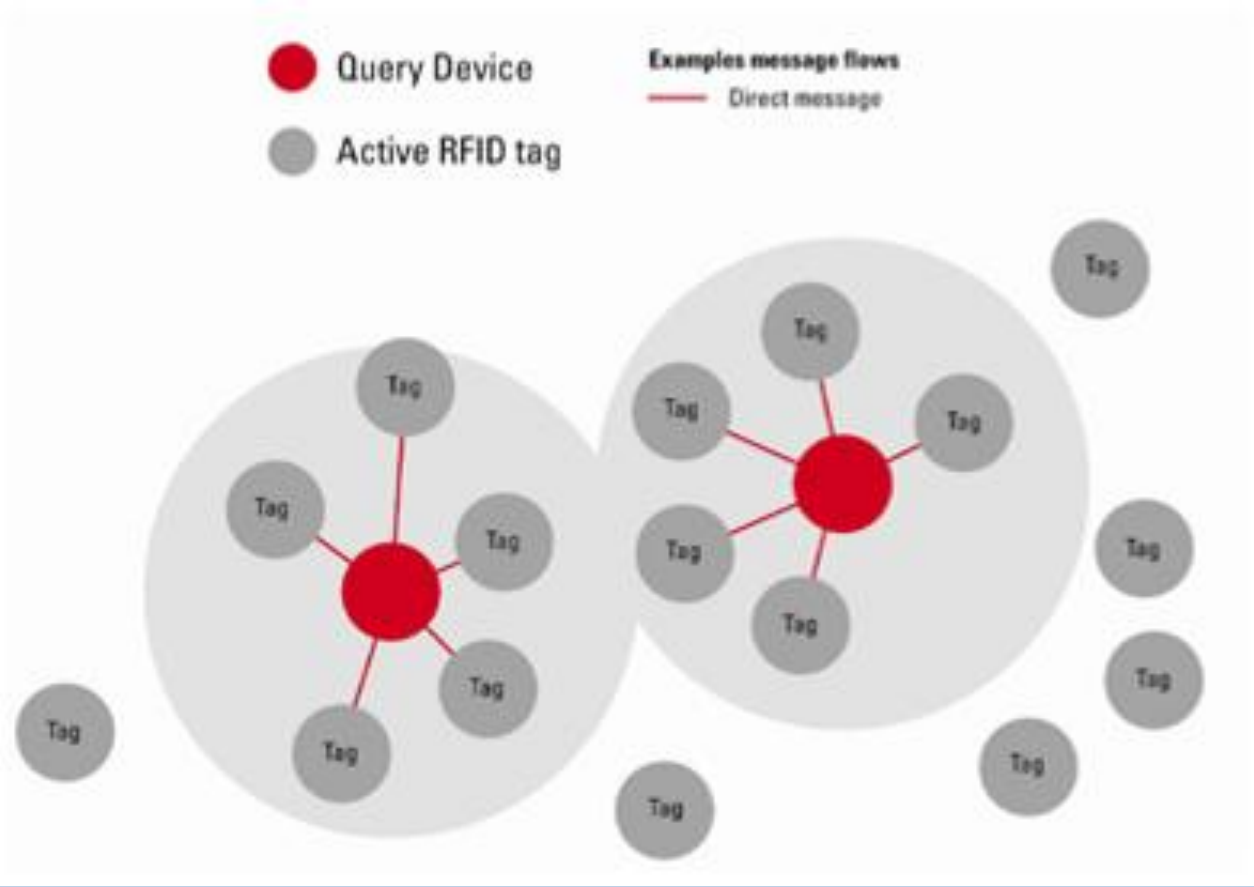
PARAMETER	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS				
Operating supply voltage	1.8		3.6	V
Operating free-air temperature range	-40		85	°C
CURRENT CONSUMPTION				
Active mode at 1 MHz, 2.2 V		270	390	µA
Standby mode		0.7	1.4	µA
Off mode with RAM retention		0.1	0.5	µA
OPERATING FREQUENCY				
VCC ≥ 3.3 V			16	MHz

CC2500

- 2.4-GHz radio-frequency (RF) transceiver
- Programmable data rate up to 500 kbps
- Low current consumption

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS					
Operating supply voltage		1.8		3.6	V
CURRENT CONSUMPTION					
RX input signal at the sensitivity limit, 250 kbps	Optimized current		16.6		mA
	Optimized sensitivity		18.8		mA
RX input signal 30 dB above the sensitivity limit, 250 kbps	Optimized current		13.3		mA
	Optimized sensitivity		15.7		mA
Current consumption TX (0 dBm)			21.2		mA
Current consumption TX (-12 dBm)			11.1		mA
RF CHARACTERISTICS					
Frequency range		2400		2483.5	MHz
Data rate (programmable)		1.2		500	kbps
Output power (programmable)		-30		0	dBm
Sensitivity, 10 kbps	Optimized current, 2-FSK, 230-kHz RX filter bandwidth, 1% PER		-99		dBm
	Optimized sensitivity		-101		dBm
Sensitivity, 250 kbps	Optimized current, 500-kHz RX filter bandwidth, 1% PER		-87		dBm
	Optimized sensitivity		-89		dBm

SimpliciTI Networking Protocol



I2C Communication

USCI Block Diagram: I2C Mode

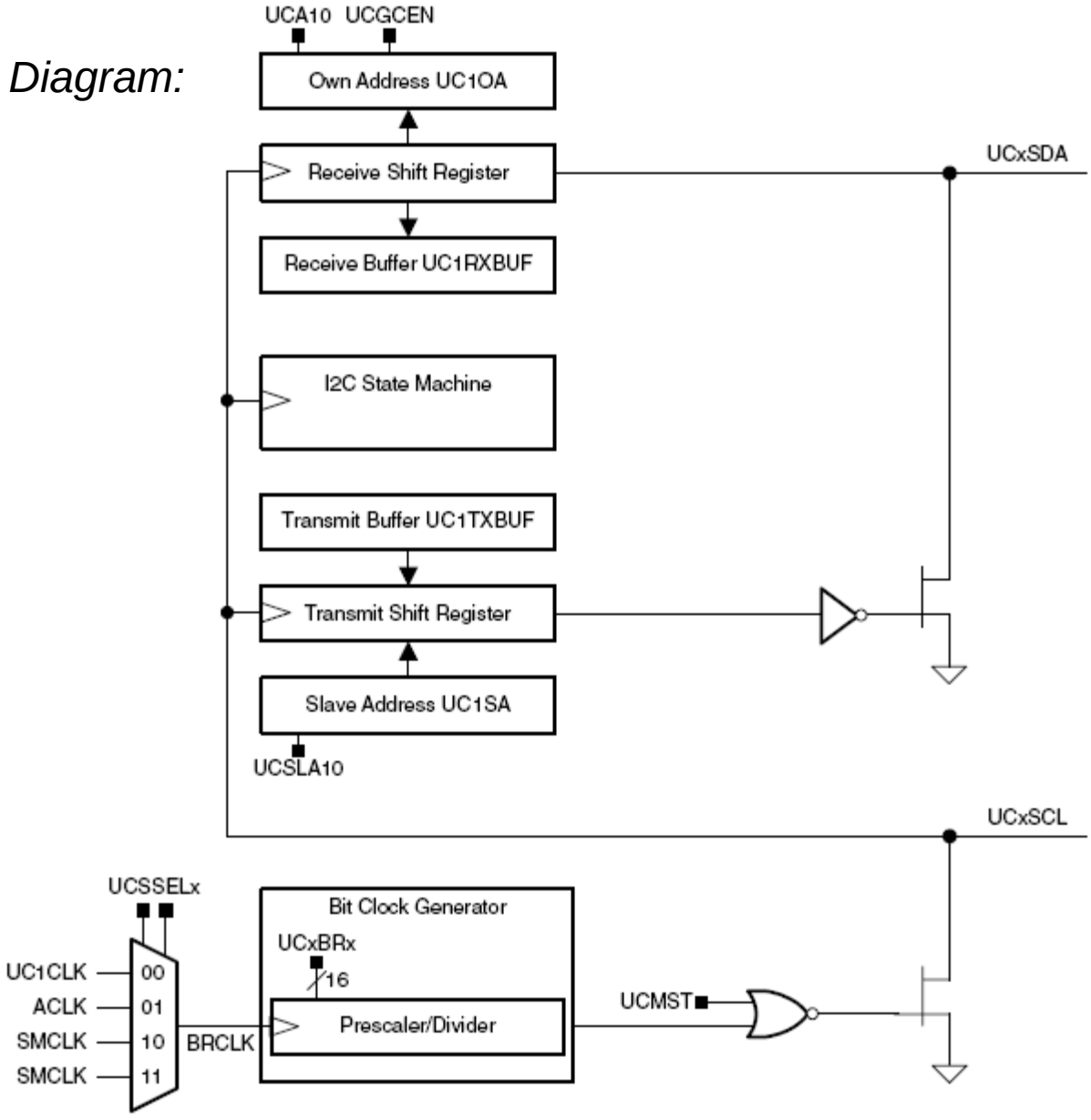


Figure 17–2. I²C Bus Connection Diagram

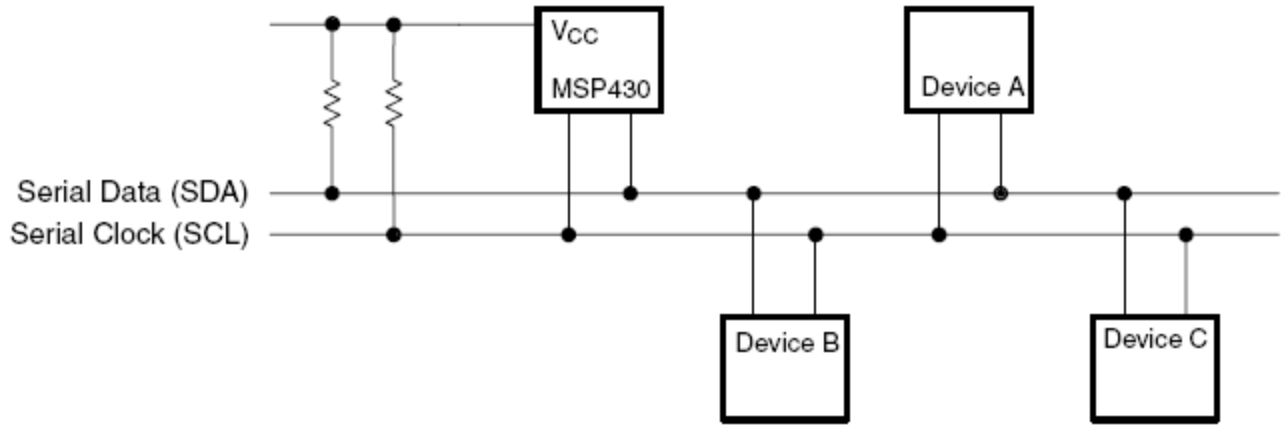


Figure 17–3. I²C Module Data Transfer

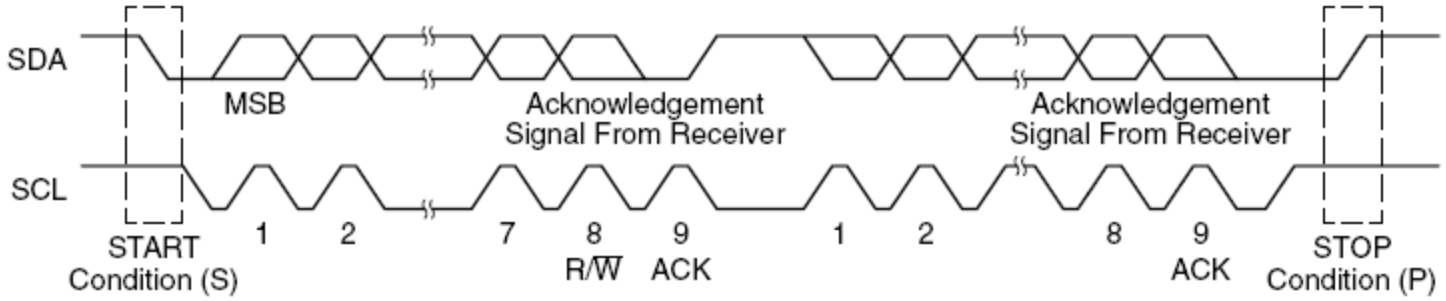
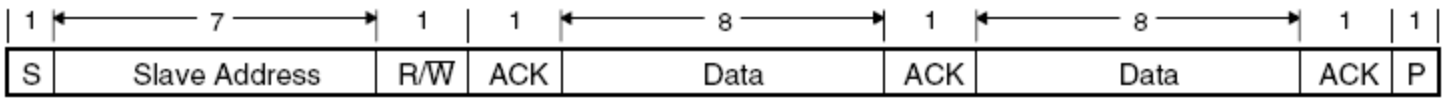


Figure 17–5. I²C Module 7-Bit Addressing Format



0x3E 0 1 1 1 1 1 0

0

0x7C

***For New LCD**

17.3.5 I²C Clock Generation and Synchronization

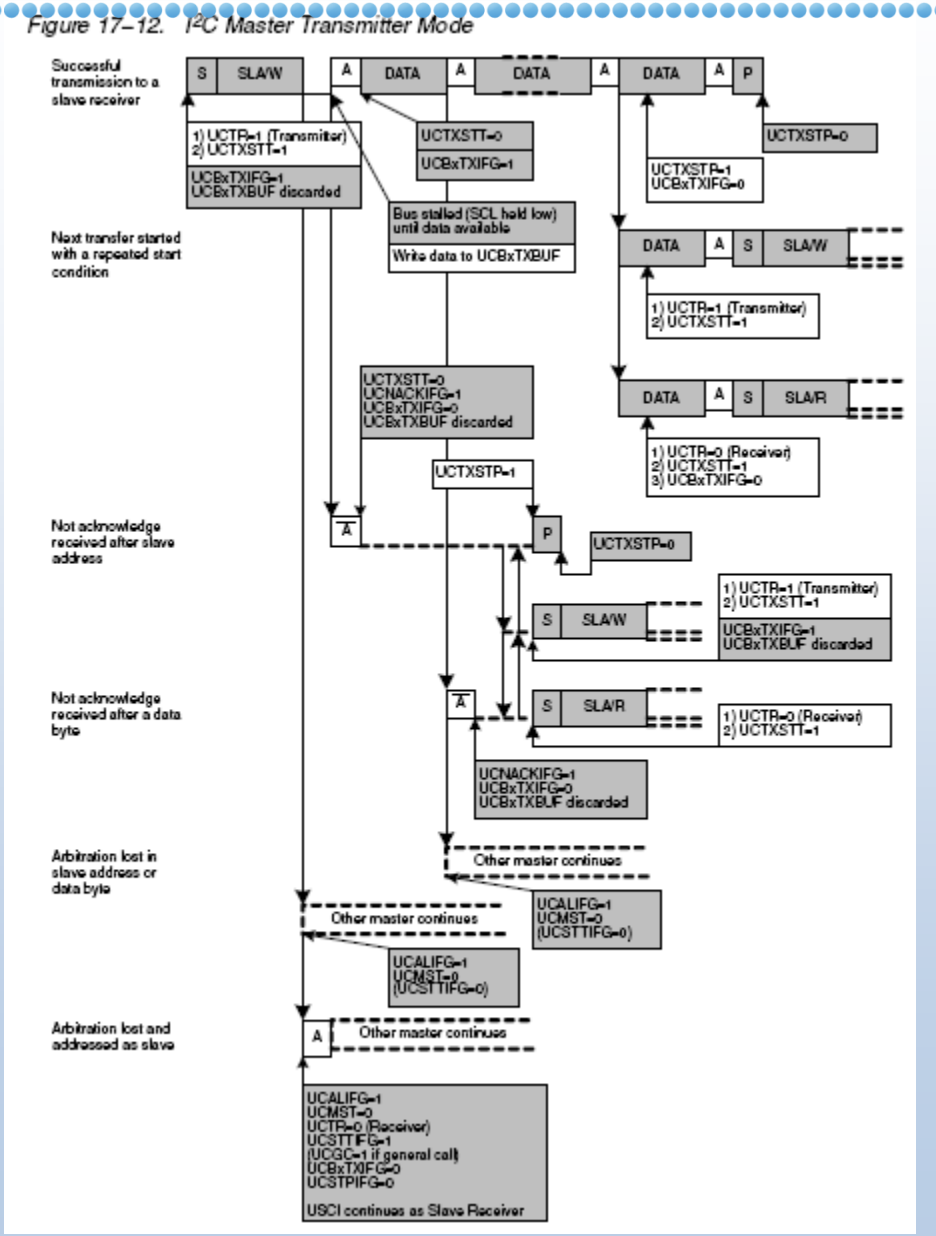
$$f_{BitClock} = \frac{f_{BRCLK}}{UCBRx}$$

The minimum high and low periods of the generated SCL are

$$t_{LOW,MIN} = t_{HIGH,MIN} = \frac{UCBRx/2}{f_{BRCLK}}$$ when UCBRx is even and

$$t_{LOW,MIN} = t_{HIGH,MIN} = \frac{(UCBRx - 1)/2}{f_{BRCLK}}$$ when UCBRx is odd.

Figure 17–12. I²C Master Transmitter Mode



Basic Clock Module: Block Diagram

Low Frequency Oscillator

High Frequency Oscillator ***(not present in F2274)***

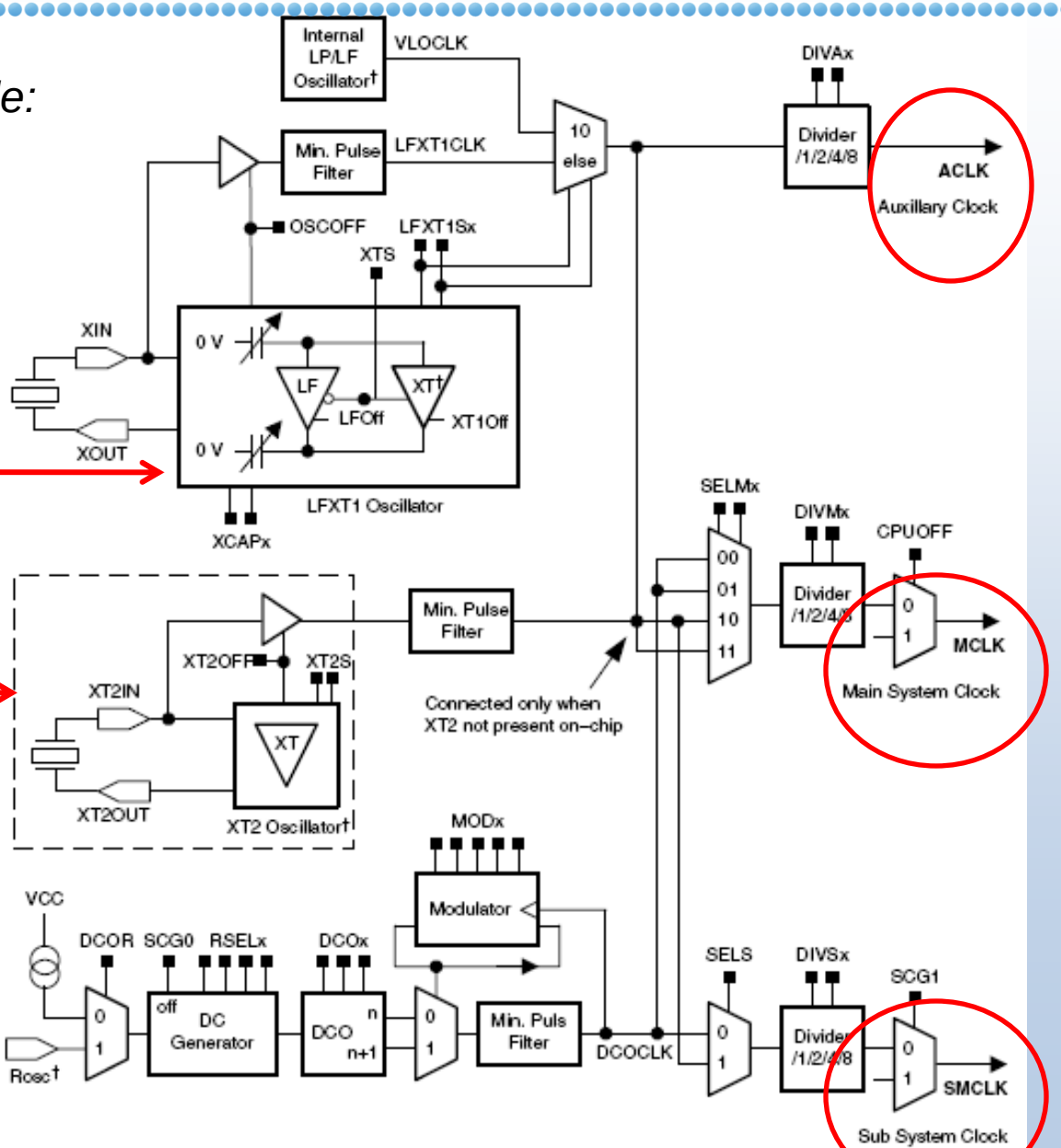
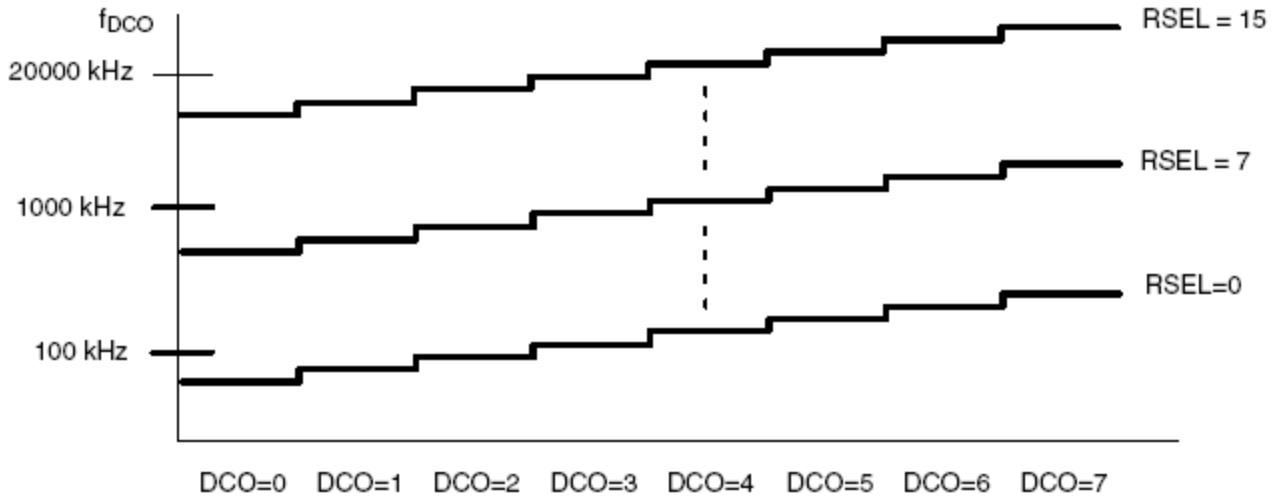


Figure 5–5. Typical DCOx Range and RSELx Steps



UCBxCTL0, USCI_Bx Control Register 0

7	6	5	4	3	2	1	0
UCA10	UCSLA10	UCMM	Unused	UCMST	UCMODEx=11		UCSYNC=1
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	r–1

UCA10 Bit 7 Own addressing mode select
- 0 Own address is a 7-bit address
- 1 Own address is a 10-bit address

UCSLA10 Bit 6 Slave addressing mode select
- 0 Address slave with 7-bit address
- 1 Address slave with 10-bit address

UCMM Bit 5 Multi-master environment select
- 0 Single master environment. There is no other master in the system. The address compare unit is disabled.
- 1 Multi master environment

Unused Bit 4 Unused

UCMST Bit 3 Master mode select. When a master looses arbitration in a multi-master environment (UCMM = 1) the UCMST bit is automatically cleared and the module acts as slave.
- 0 Slave mode
- 1 Master mode

UCMODEx Bits 2–1 USCI Mode. The UCMODEx bits select the synchronous mode when UCSYNC = 1.
- 00 3-pin SPI
- 01 4-pin SPI (master/slave enabled if STE = 1)
- 10 4-pin SPI (master/slave enabled if STE = 0)
- 11 I^2C mode

UCSYNC Bit 0 Synchronous mode enable
- 0 Asynchronous mode
- 1 Synchronous mode

UCBxCTL1, USCI_Bx Control Register 1

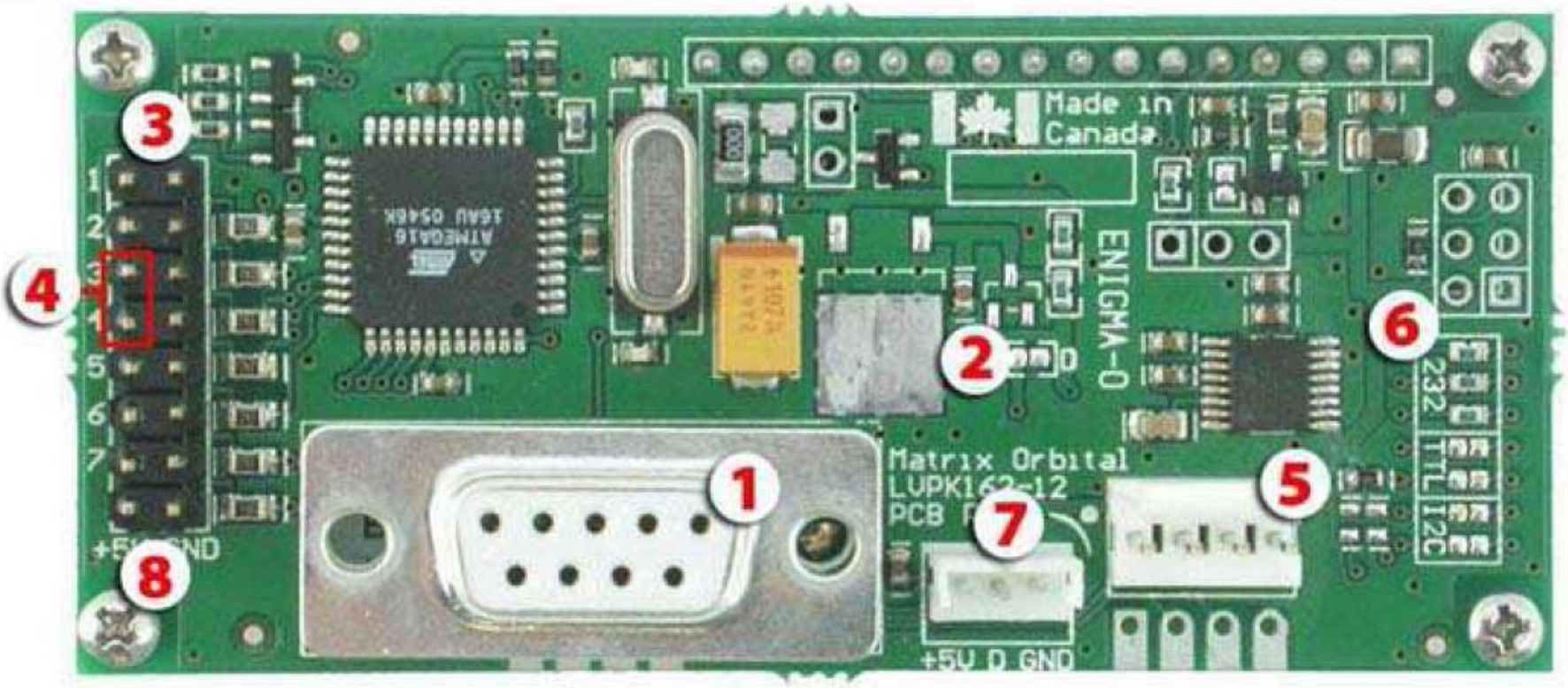
7	6	5	4	3	2	1	0
UCSSELx		Unused	UCTR	UCTXNACK	UCTXSTP	UCTXSTT	UCSWRST
rw–0	rw–0	r0	rw–0	rw–0	rw–0	rw–0	rw–1

UCSSELx	Bits 7-6	USCI clock source select. These bits select the BRCLK source clock. 00 UCLKI 01 ACLK 10 SMCLK 11 SMCLK
Unused	Bit 5	Unused
UCTR	Bit 4	Transmitter/Receiver 0 Receiver 1 Transmitter
UCTXNACK	Bit 3	Transmit a NACK. UCTXNACK is automatically cleared after a NACK is transmitted. 0 Acknowledge normally 1 Generate NACK
UCTXSTP	Bit 2	Transmit STOP condition in master mode. Ignored in slave mode. In master receiver mode the STOP condition is preceded by a NACK. UCTXSTP is automatically cleared after STOP is generated. 0 No STOP generated 1 Generate STOP
UCTXSTT	Bit 1	Transmit START condition in master mode. Ignored in slave mode. In master receiver mode a repeated START condition is preceded by a NACK. UCTXSTT is automatically cleared after START condition and address information is transmitted. Ignored in slave mode. 0 Do not generate START condition 1 Generate START condition
UCSWRST	Bit 0	Software reset enable 0 Disabled. USCI reset released for operation. 1 Enabled. USCI logic held in reset state.

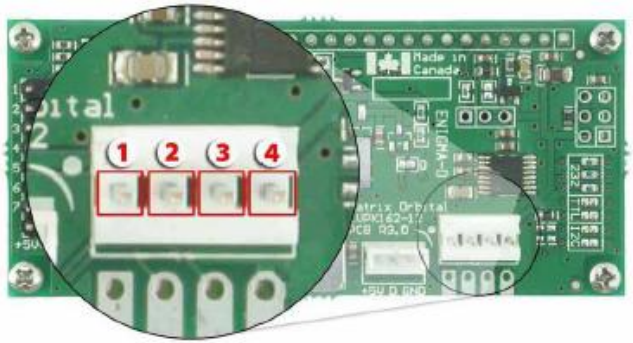
LCD # 1

LK162-12

(Matrix Orbital)



1 DB-9 Connector
2 Power Through DB9 Jumper
3 GPOs
4 Manual Override
5 Power / Data Connector
6 Protocol Select Jumpers
7 Optional Dallas 1-Wire Bridge
8 Keypad Interface



Pin 1 PWR *(See table 1)*
Pin 2 Rx \ SCL (I^2C clock)
Pin 3 Tx \ SDA (I^2C data)
Pin 4 GND

Figure 13: Power Connector and Pin out

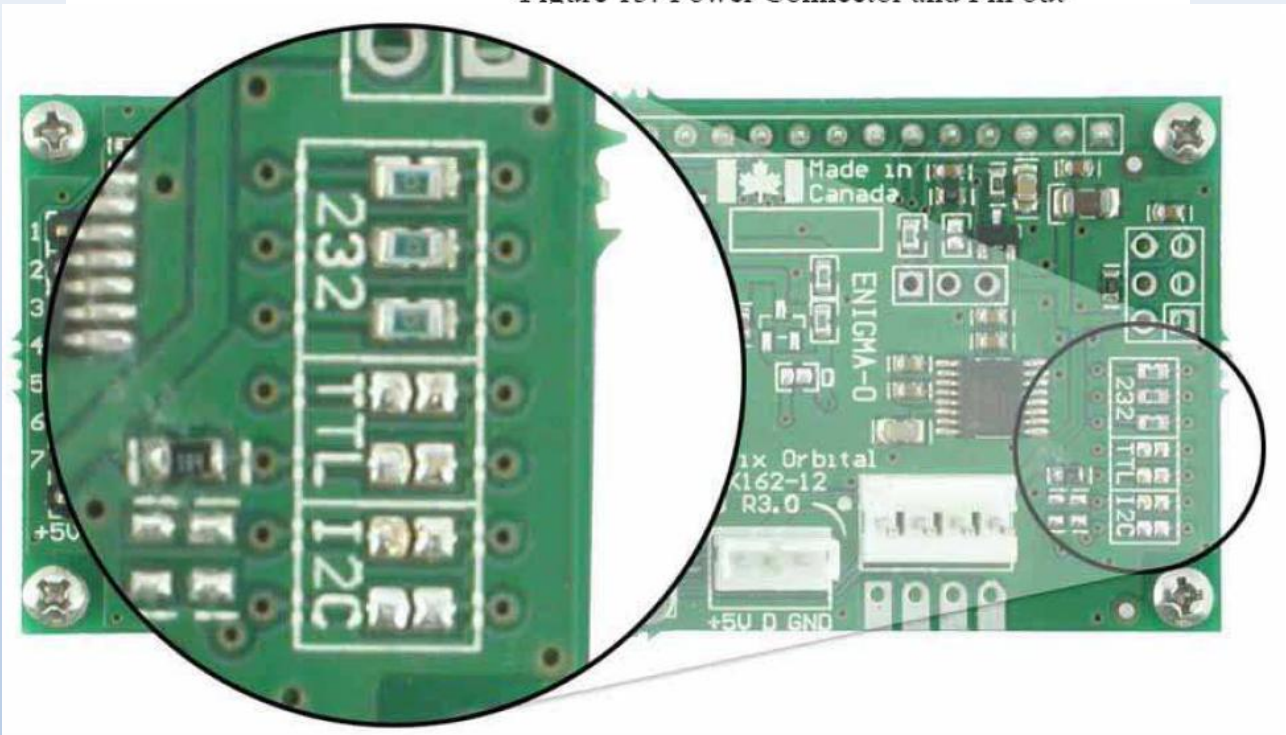


Figure 14: Protocol Select Jumpers

Table 1: Power Requirements

	Standard	-V	-VPT
Supply Voltage	+5Vdc ±0.25V	+9V to +15V	+9V to +35V
Backlight On Supply	115 mA typical		
Backlight Off Supply	9 mA		

Table 70: Electrical Specifications

	Standard	Wide Voltage (V)
Supply Voltage	+5Vdc ±0.25V	+9V to +15V
Minimum Current	40mA typical	
Backlight On (YG & IY)	add 90mA (130mA) typical	
Backlight On (R)	add 100mA (140mA) typical	
Backlight On (GW & WB)	add 30mA (70mA) typical	

Table 3: I^2C Transaction Algorithm

START	Toggle SDA high to low
Address	0x50
Information	0x48 0x45 0x4C 0x4C 0x4F
STOP	Toggle SDA low to high

Voltage Regulation

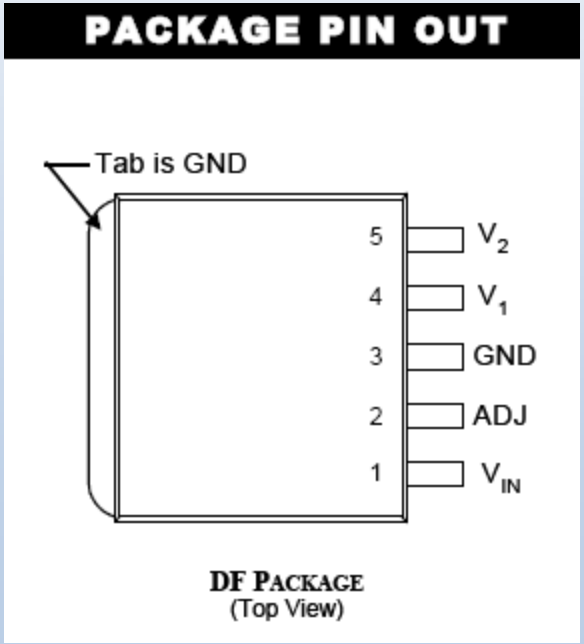
(LX 8816)

Dual Channel 1A Low Dropout Regulator

(Microsemi)

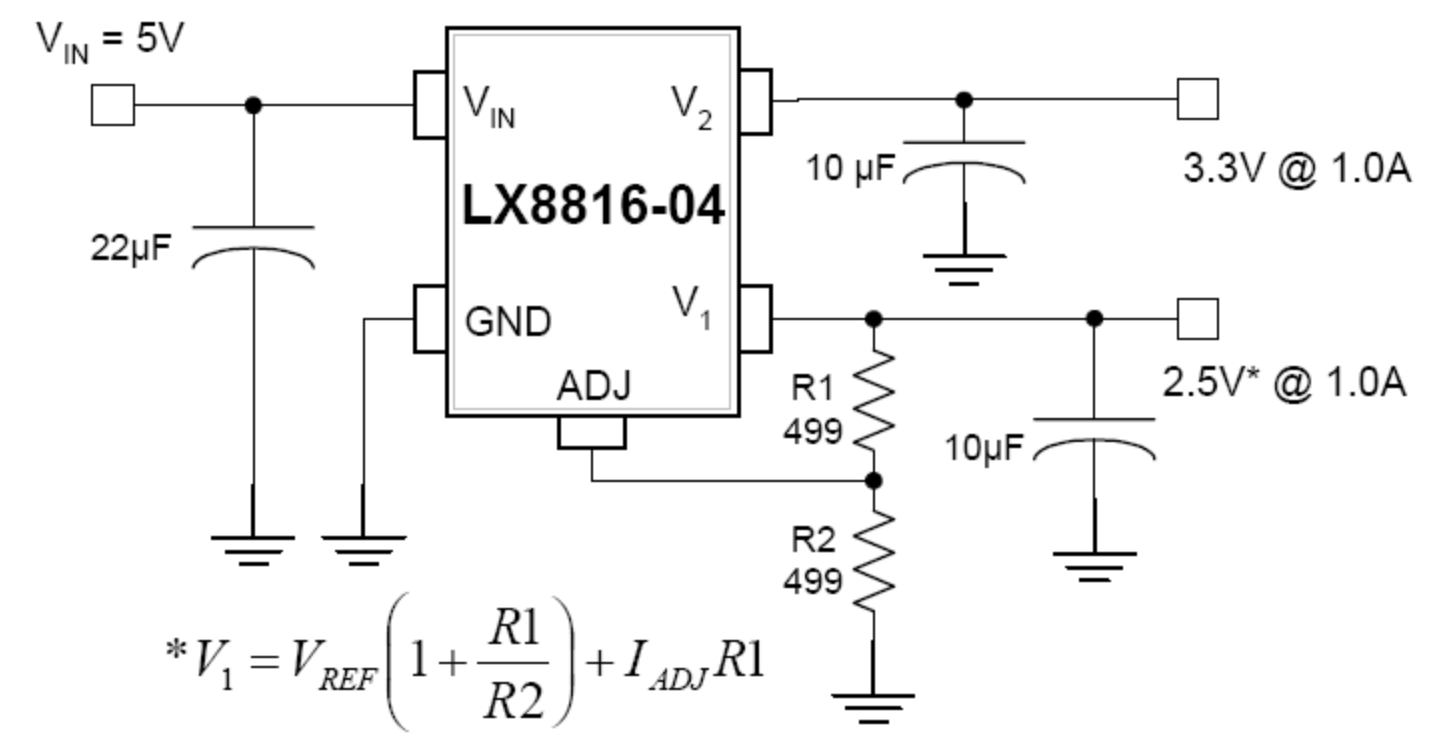
Key Features

- 2 independent regulated outputs
- Independent thermal and current limit protection.
- First - 3.3 V fixed voltage output
- Second – Adjustable voltage output – i.e. 5V in our case



FUNCTIONAL PIN DESCRIPTION	
PIN NAME	**DESCRIPTION**
V_{IN}	Positive unregulated supply input for the regulator. Bypass to GND with at least 2.2µF capacitance having low ESR for good transient response.
ADJ	Adjustable Input. The output voltage can be set by two external resistors with the following relationship: $V_1 = V_{REF} * (1 + R1 / R2) + I_{ADJ} * R1$ where R1 is the resistor connected between V_1 and ADJ, and R2 is the resistor connected between ADJ and GND.
GND	Common terminal for ground reference. The input and output bypass capacitors should be connected to this pin. In addition the tab on the S-Pak package and pin 3 are also used for heat sinking the device.
V_1	Adjustable regulator output (Regulator #1) It is recommended to bypass to GND with at least 2.2uF. Size your output capacitor to meet the transient loading requirement. If you have a very dynamic load, a lower ESR capacitor will improve the response to these load steps.
V_2	Fixed regulator output (Regulator #2). It is recommended to bypass to GND with at least 2.2µF. Size your output capacitor to meet the transient loading requirement. For dynamic loads, a lower ESR capacitor will improve the response to these load steps.

Voltage Regulator Circuit



Level Translation

(PCA9306)

Dual Bidirectional I2C-bus and SMBus voltage-level translator

(NXP - Philips)

Key Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I2C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I2C-bus and SMBus compatible
- Allows voltage level translation between:
  s(ref)(2) ← in our case

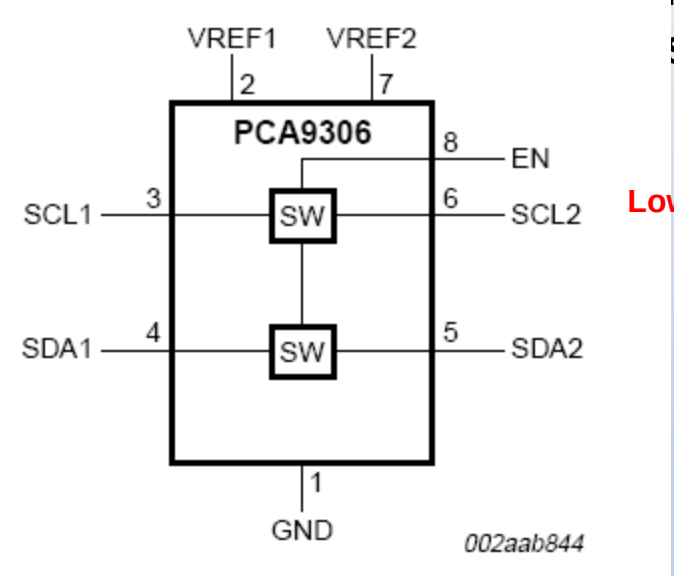
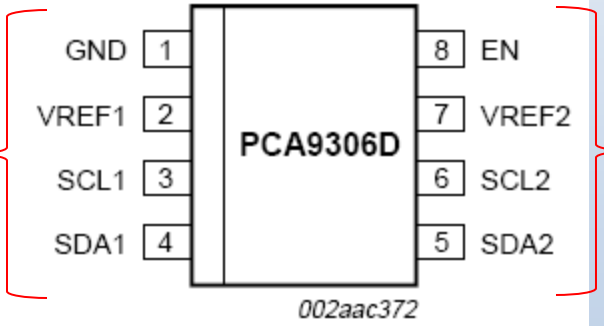


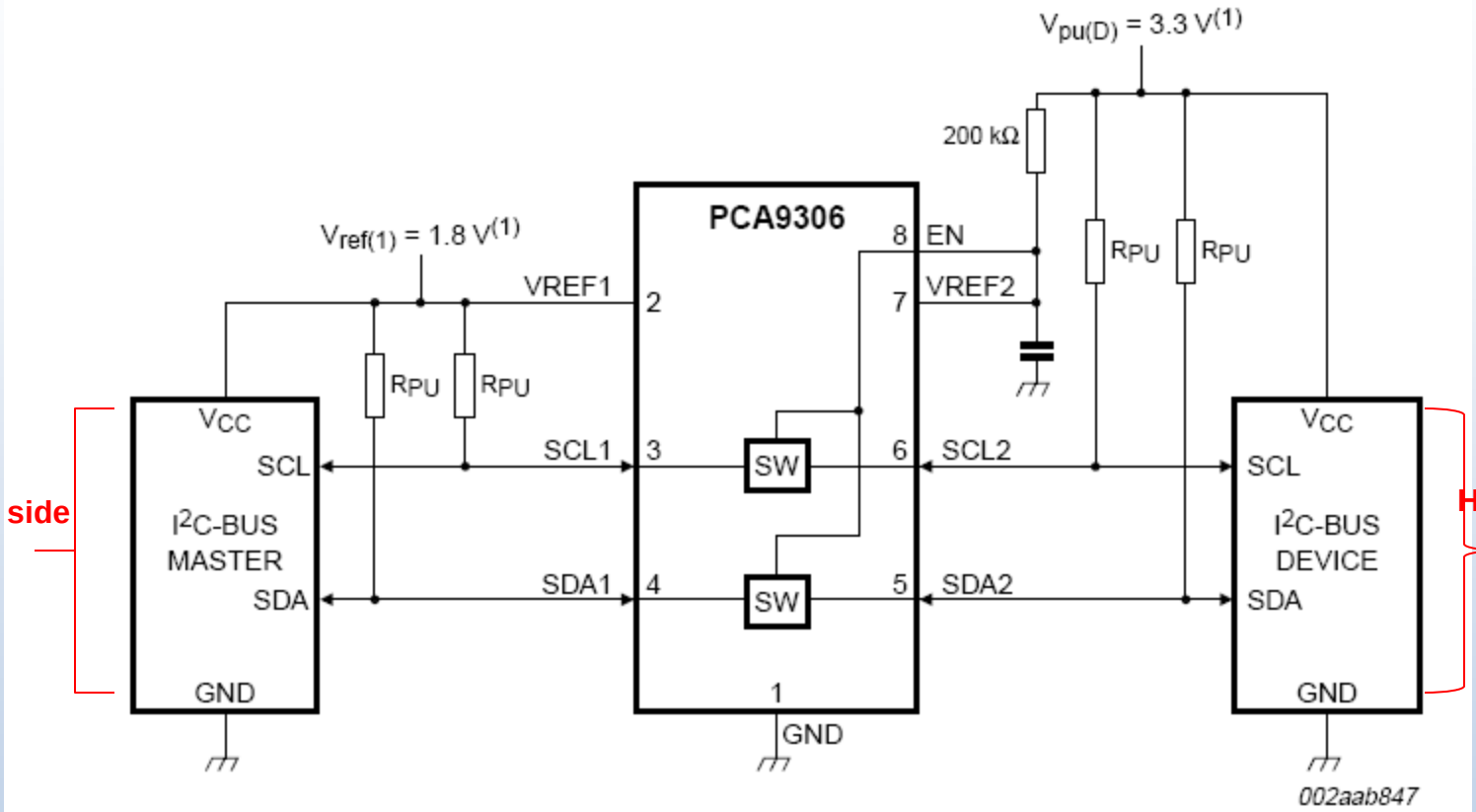
Fig 1. Logic diagram of PCA9306 (positive logic)

Low voltage side (MSP)



High voltage side (LCD)

Fig 6. Pin configuration for SO8



Low voltage side (MSP)

High voltage side (LCD)

(1) The applied voltages at $V_{ref(1)}$ and $V_{pu(D)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Fig 9. Typical application circuit (switch always enabled)

Sizing the Pull-up Resistor

$$R_{PU} = \frac{V_{pu(D)} - 0.35\ V}{0.015\ A}$$

Table 10. Pull-up resistor values

Calculated for V_{OL} = 0.35 V; assumes output driver V_{OL} = 0.175 V at stated current.

$V_{pu(D)}$	Pull-up resistor value (Ω)					
	15 mA		10 mA		3 mA	
	Nominal	+10 %[1]	Nominal	+10 %[1]	Nominal	+10 %[1]
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

[1] +10 % to compensate for V_{CC} range and resistor tolerance.

LCD # 2

NHD-C0216CiZ-FSW-FBW-3V3

COG (Chip-on-Glass) Liquid Crystal Display Module

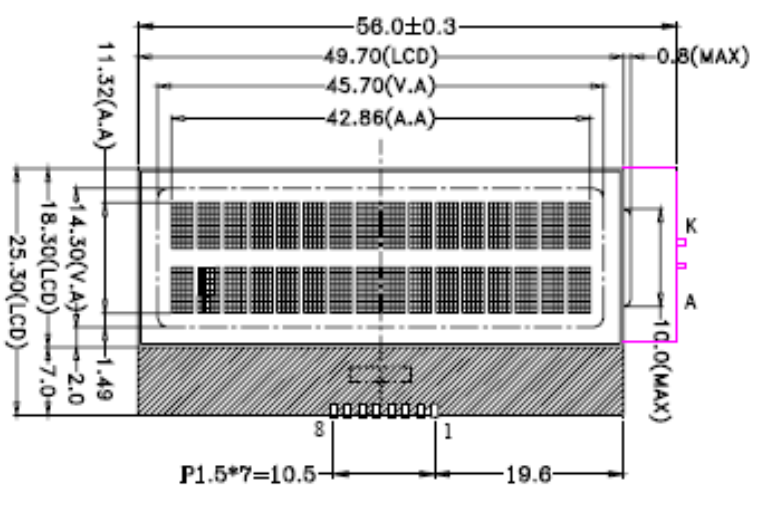
(New Haven Display)

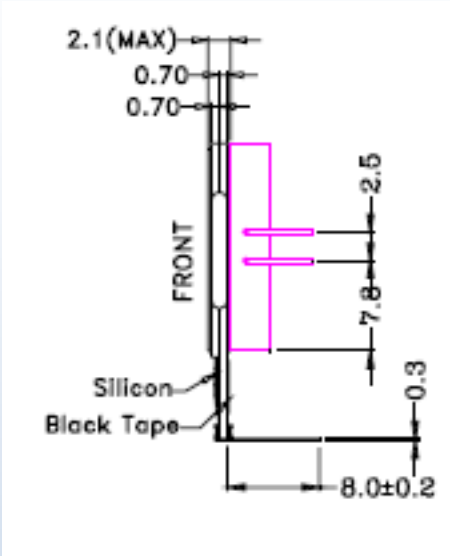
Functions and Features

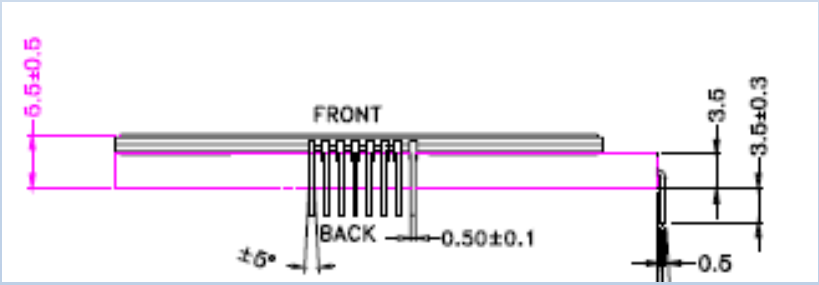
- **2 lines x 16 characters**
- **Built-in ST7032i-oD with I²C interface**
- **5x8 pixels with cursor**
- **3V power supply**
- **1/16 duty, 1/5 bias**
- **RoHS Compliant**

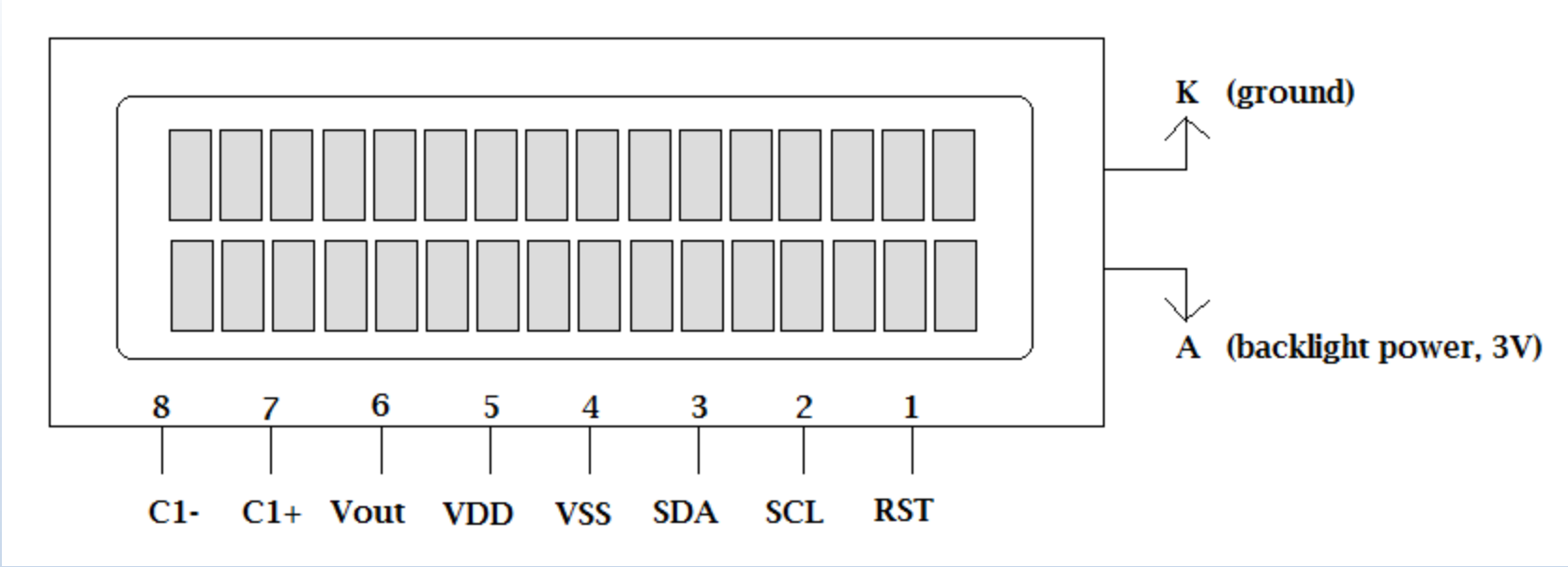
Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-20	-	+70	°C
Storage Temperature Range	Tst	Absolute Max	-30	-	+80	°C
Supply Voltage	VDD		2.7	3.0	3.3	V
Supply Current	IDD	Ta=25°C,VDD=3.0V	-	0.3	0.5	mA
Supply for LCD (contrast)	VDD-Vo	**Ta=25°C**	-	5.0	-	V
"H" Level input	VIH		2.2	-	VDD	V
"L" Level input	VIL		0	-	0.6	V
"H" Level output	VOH		2.4	-	-	V
"L" Level output	VOL		-	-	0.4	V
Backlight supply voltage	VLED		-	3.0	-	V
Backlight supply current	ILED	VLED=3.0V	-	15	20	mA


56.0±0.3
49.70(LCD)
45.70(V.A)
42.86(A.A)
11.32(A.A)
0.8(MAX)
25.30(LCD)
18.30(LCD)
14.30(V.A)
1.49
2.0
7.0
K
A
1.0(MAX)
8
1
P1.5*7=10.5
19.6


2.1(MAX)
0.70
0.70
FRONT
2.5
7.8
0.3
Silicon
Black Tape
8.0±0.2


5.5±0.5
FRONT
3.5
3.5±0.3
BACK
0.50±0.1
±5°
0.5

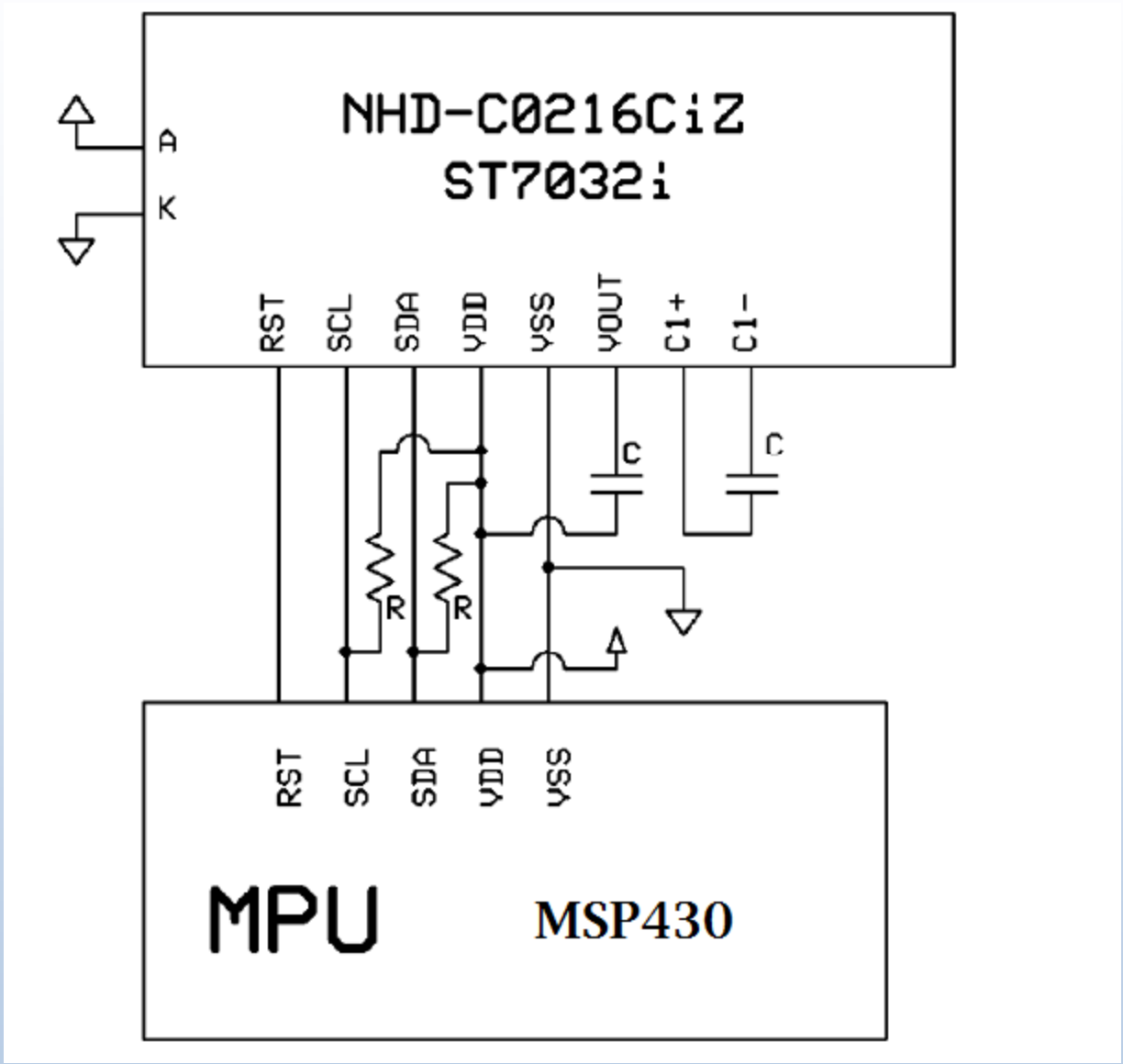

K (ground)
A (backlight power, 3V)
8
7
6
5
4
3
2
1
C1-
C1+
Vout
VDD
VSS
SDA
SCL
RST

Pin Description and Wiring Diagram

Pin No.	Symbol	External Connection	Function Description
1	RST	MPU	Active LOW Reset Signal
2	SCL	MPU	Serial clock
3	SDA	MPU	Input Data
4	Vss	Power Supply	Ground
5	VDD	Power Supply	Power supply for logic for LCD (3.0V)
6	VOUT	Power Supply	DC/DC voltage converter. Connect to 1uF capacitor to VDD
7	C1+	CAP	Voltage booster circuit. Connect to 1uF cap to PIN8
8	C1-	CAP	Voltage booster circuit. Connect to 1uF cap to PIN7
A	LED+	Power Supply	Power supply for Backlight(3.0V)
K	LED-	Power Supply	Backlight Ground

Recommended LCD connector: 1.5mm pitch pins

Backlight connector: A and K pins **Mates with**: -


NHD-C0216CiZ
ST7032i
A
K
RST
SCL
SDA
VDD
VSS
VOUT
C1+
C1-
C
C
R
R
RST
SCL
SDA
VDD
VSS
MPU
MSP430

Slave Address = 0x7C

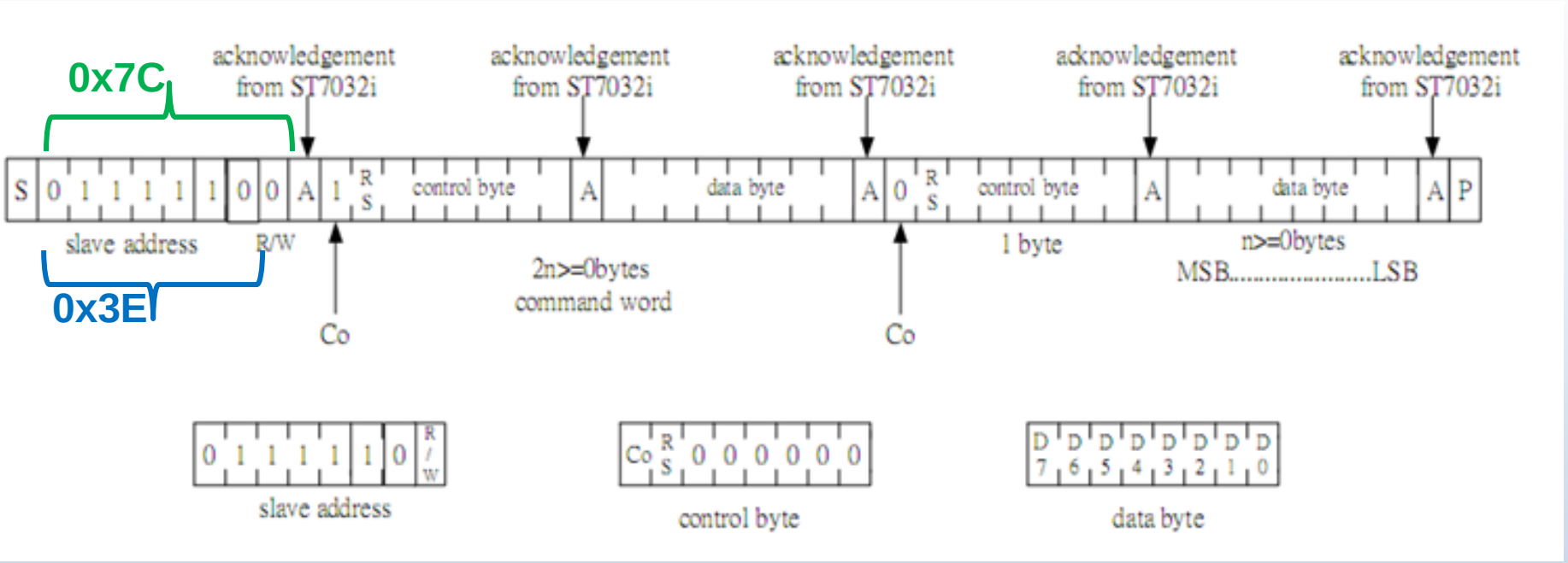
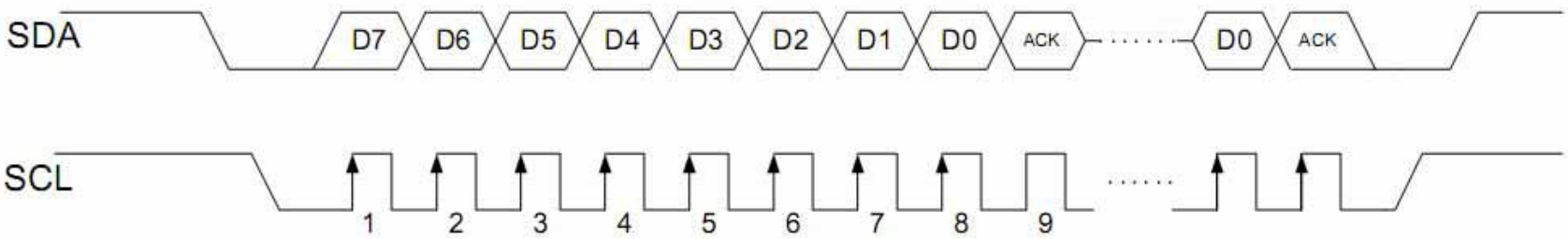


Figure 5. 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.


SDA
D7
D6
D5
D4
D3
D2
D1
D0
ACK
D0
ACK
SCL
1
2
3
4
5
6
7
8
9

➢ instruction table at "Extension mode"

(when "EXT" option pin connect to Vss, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC= 380KHz	OSC= 540kHz	OSC= 700KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note * : this bit is for test command, and must always set to "0"

Instruction table 0(IS=0)														
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	**26.3 us**	**18.5 us**	**14.3 us**
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	**26.3 us**	**18.5 us**	**14.3 us**

Instruction table 1(IS=1)														
Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	**26.3 us**	**18.5 us**	**14.3 us**
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	**26.3 us**	**18.5 us**	**14.3 us**
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	**26.3 us**	**18.5 us**	**14.3 us**
Follower control	0	0	0	1	1	0	Fon	Rab 2	Rab 1	Rab 0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	**26.3 us**	**18.5 us**	**14.3 us**
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	**26.3 us**	**18.5 us**	**14.3 us**

Mnemosyne Innovations

ST7032-0D (ITO option OPR1=1, OPR2=1)

Controller Information Built-in ST7032i eD

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Table 1. Various kinds of operations according to RS and R/W bits.

I2C Acknowledge

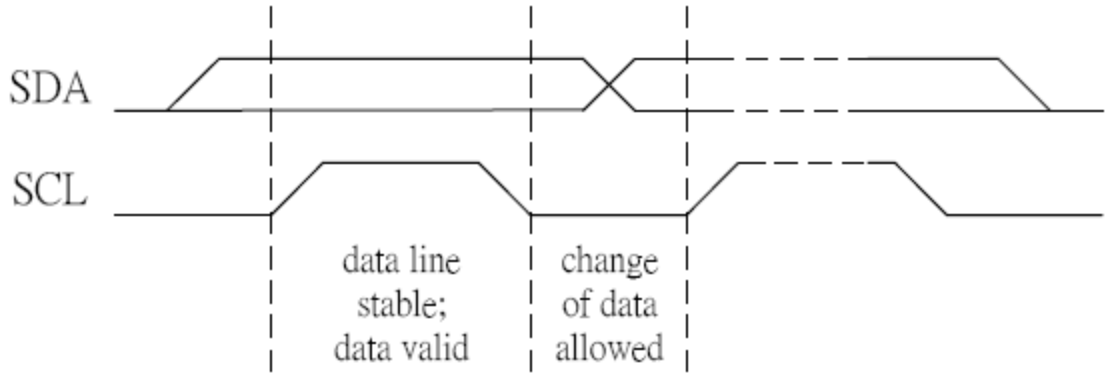


Figure 1. Bit transfer

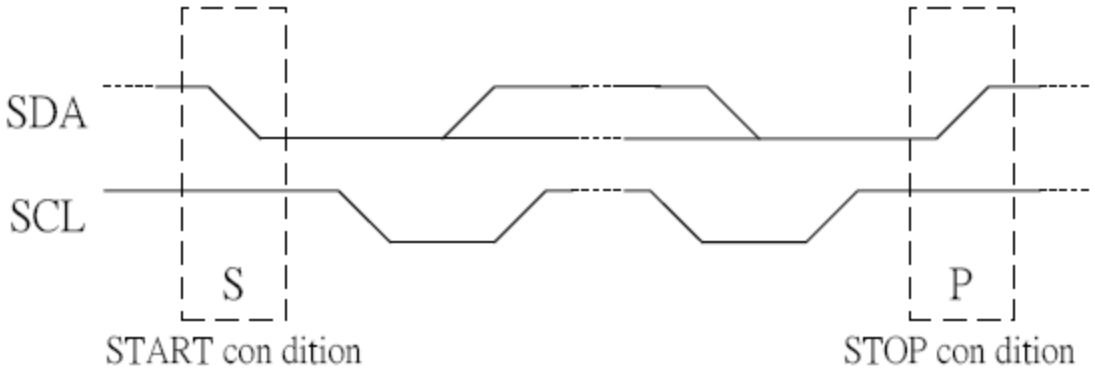


Figure 2. Definition of START and STOP conditions

I2C Acknowledge (cont.)

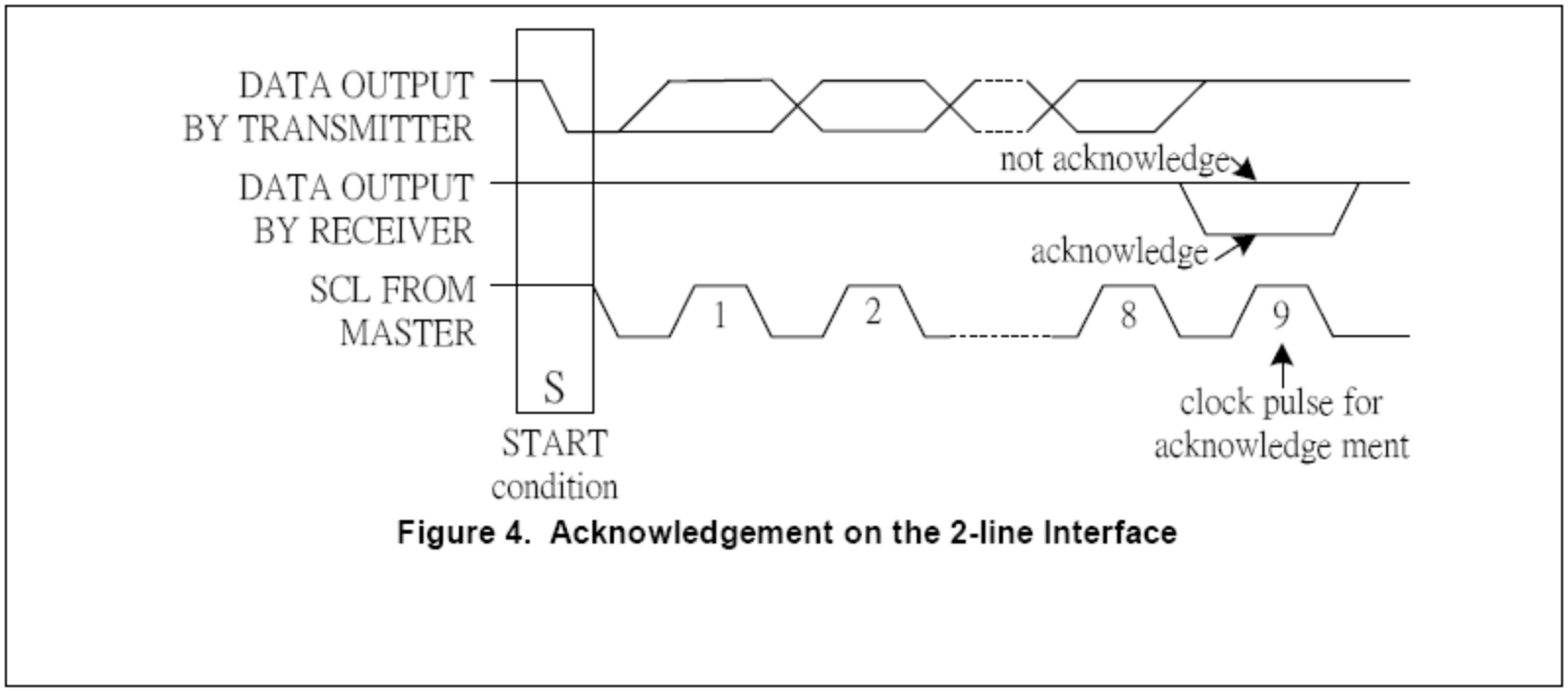
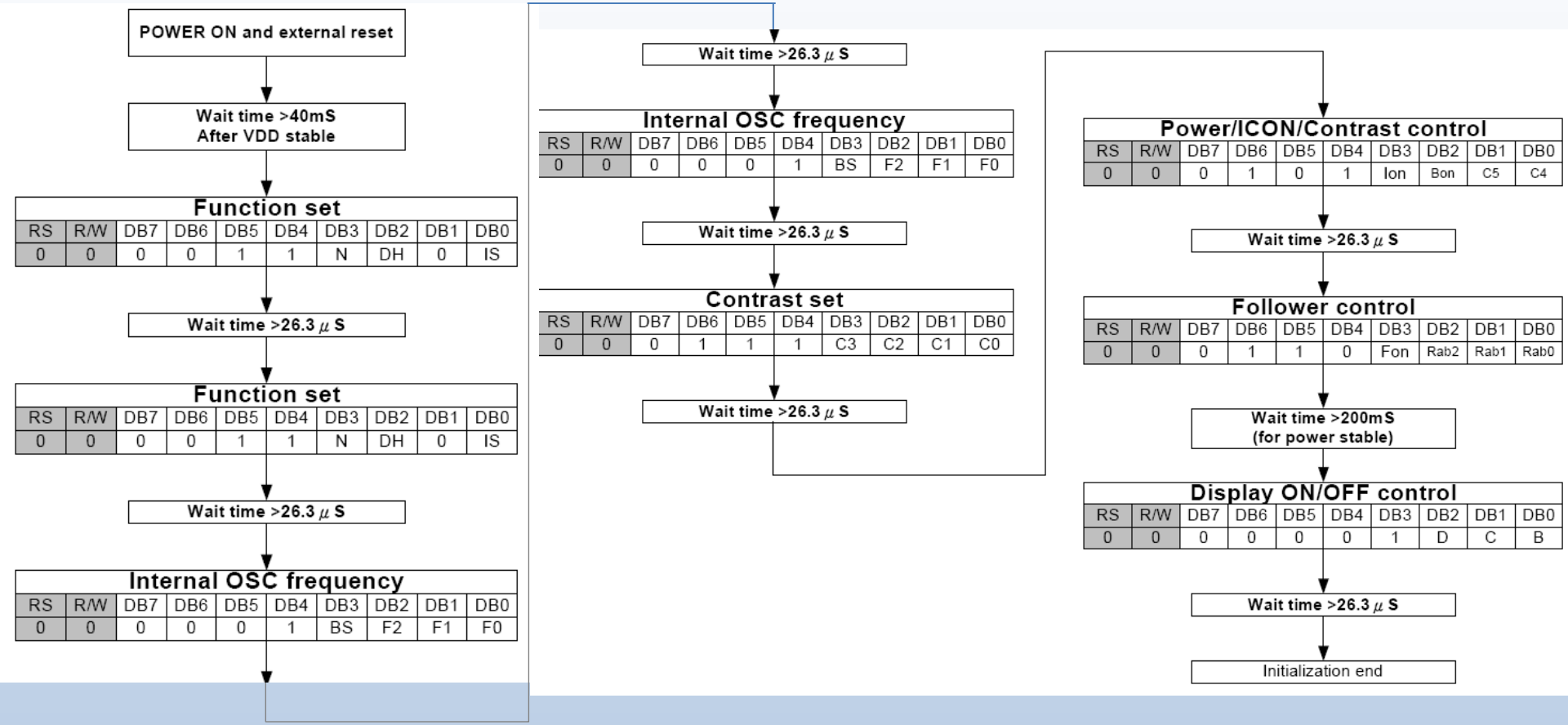


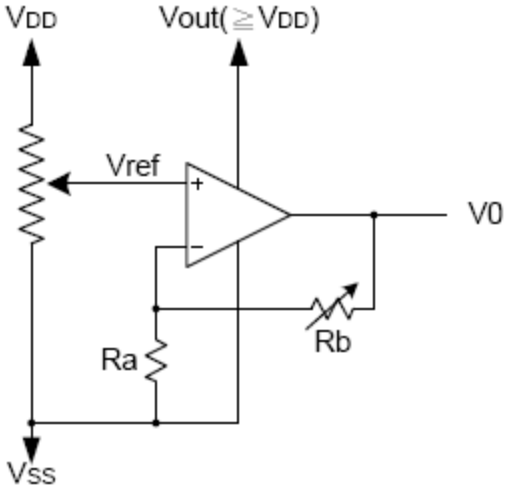
Figure 4. Acknowledgement on the 2-line Interface

I2C Interface - Register Loading Process



V0 Voltage Follower Value Calculation

- V0 voltage follower value calculation



$$V0=(1+\frac{Rb}{Ra})*Vref$$

$$While\ Vref=VDD*(\frac{\alpha+36}{100})$$

α = 37 , V_{REF} = 2.19 V and if 1 + (Rb/Ra) = 2.5

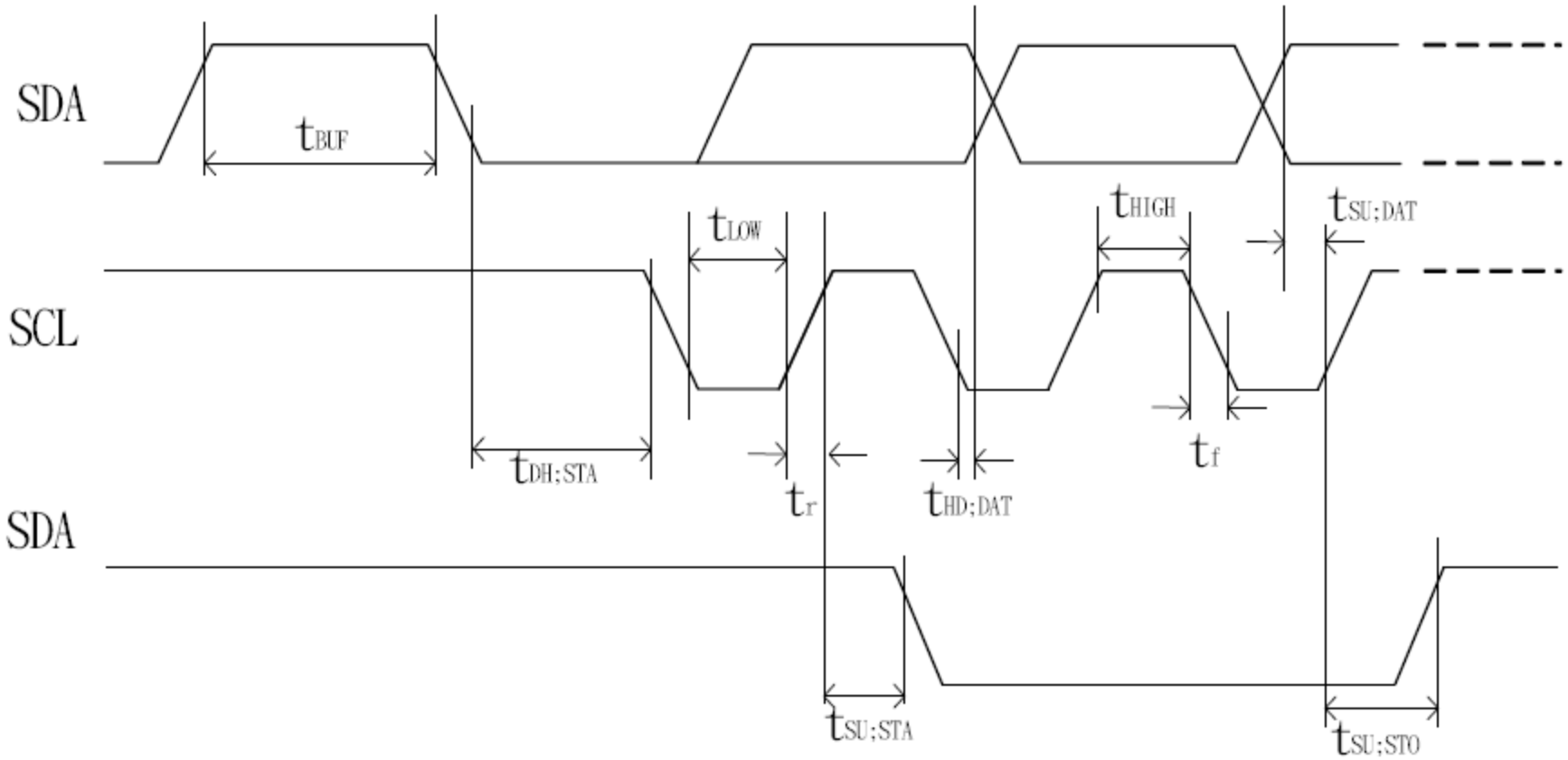
Then V_0 = 5.475 V

Therefore:

$C_5, C_4, C_3, C_2, C_1, C_0$ = 1 0 0 1 0 1

R_{ab2} , R_{ab1} , R_{ab0} = 1 0 1

- **I2C interface**

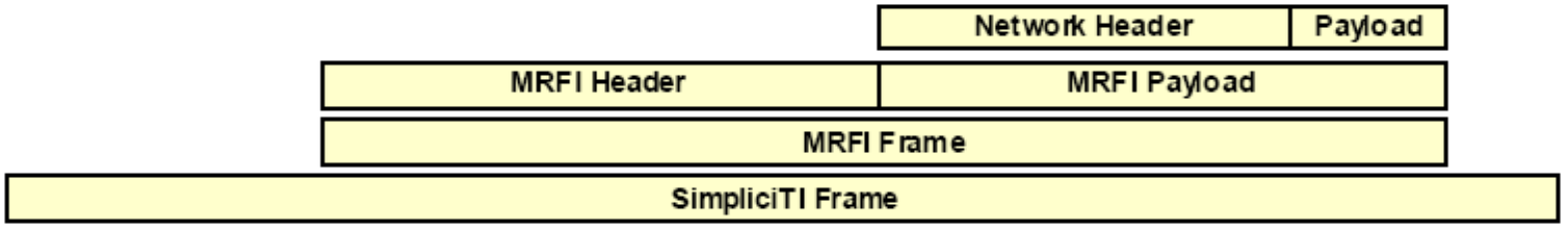


(Ta =-30°C to 85°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SI	$t_{SU;DAT}$	—	**180**	–	100	–	ns
Data hold time		$t_{HD:DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SI	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

SimpliciTI Frame Format

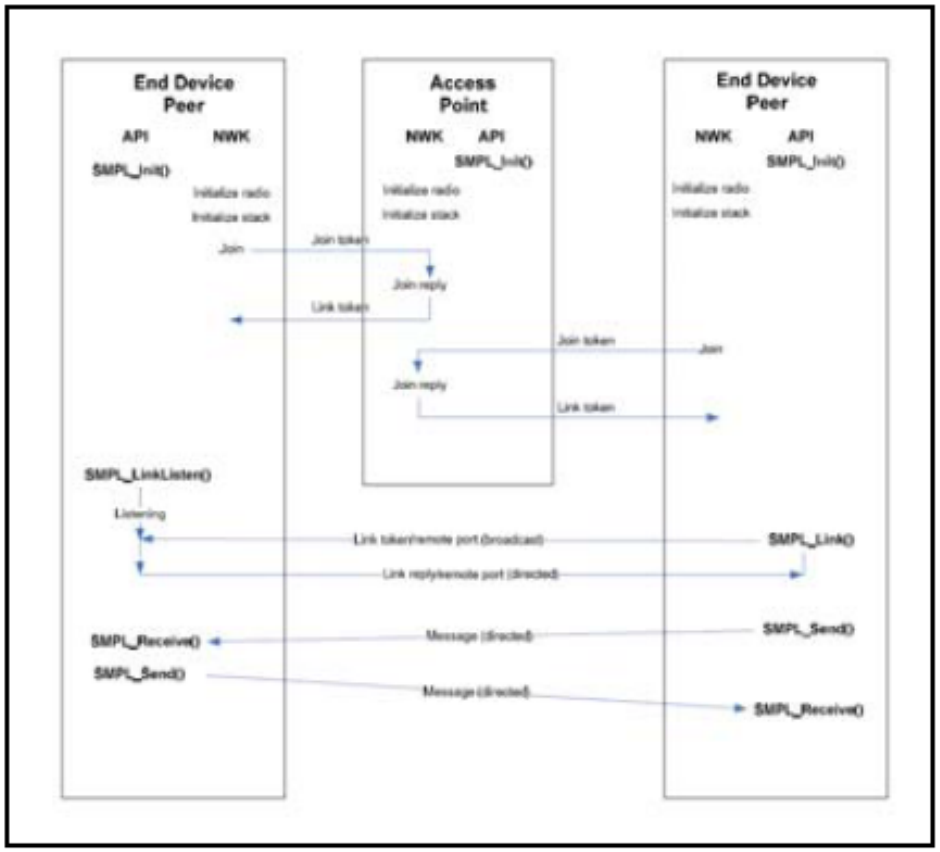
PREAMBLE	SYNC	LENGTH	Misc	DST ADDR	SRC ADDR	PORT	DEVICE INFO	TRACT ID	App Payload	FCS
RD*	RD*	1	RD*	4	4	1	1	1	n	RD*



Field	Definition	Comments
PREAMBLE	Radio synchronization	Inserted by Radio HW
SYNC	Radio synchronization	Inserted by Radio HW
LENGTH	Length of remaining frame in bytes	Inserted by FW on Tx, Partially filterable on Rx.
MISC	Radio dependent (needed for future IEEE radio support)	Currently set to 0.
DSTADDR	Destination address	Inserted by FW. LSB filterable. 0x00 and 0xFF LSB values reserved for broadcast. LSB:MSB formatted.
SRCADDR	Source address	Inserted by FW
PORT	Application port number (bits 5-0)	Inserted by FW. Port 0x20-0x3D for customer applications, Port 0x00-0x1F for NWK applications
DEVICE INFO	Receiver type (bit 7-6), Sender Type (5-4) & Hop count (2-0)	Inserted by FW.
TRACTID	Transaction ID	Inserted by FW. Discipline depends on context.
APP PAYLOAD	Application data	$0 \leq n \leq 52$ (50 if FCS)
FCS	Radio append bytes	CRC checksum (Tx), RSSI, LQI and CRC status (Rx)

* **RD = Radio-Dependent. Populate by MRFI or handled by the radio hardware.**

Join & Link Tokens



- In networks with an AP, only devices with a matching Join token can join the network
- Devices not matching the join token fail the join request. Their default link token (defined at build) will be used
- Only devices with identical Link tokens can link together. In networks with an AP, the link token is distributed by the AP

Networks with no AP do not join, they link only